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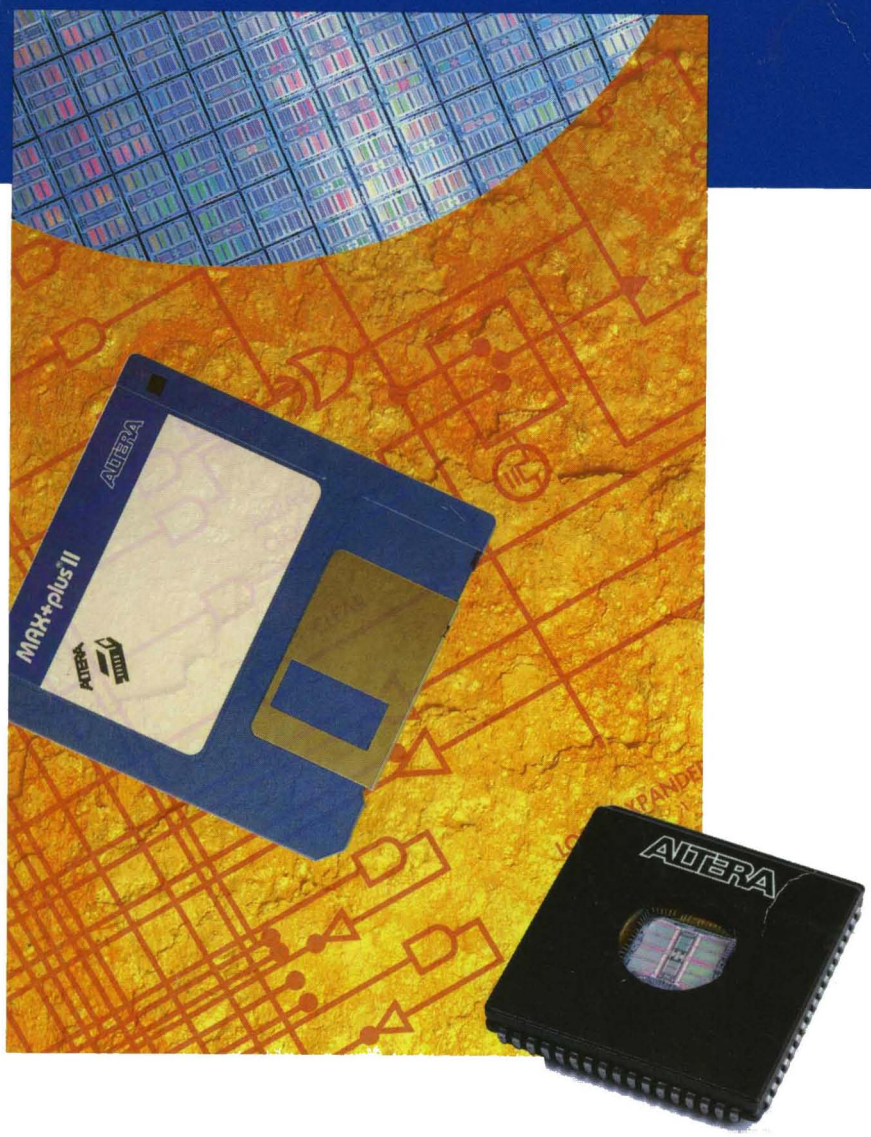

Data Book

September 1991

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About this Data Book

September 1991

This data book contains complete information about Altera's Classic, MAX 5000, MAX 7000, STG, and SAM EPLDs, development systems, and development software. For complete information about the Micro Channel EPLDs and the associated development system and software, refer to Altera's ***Micro Channel Adapter Handbook***.

For immediate assistance on technical questions, call:

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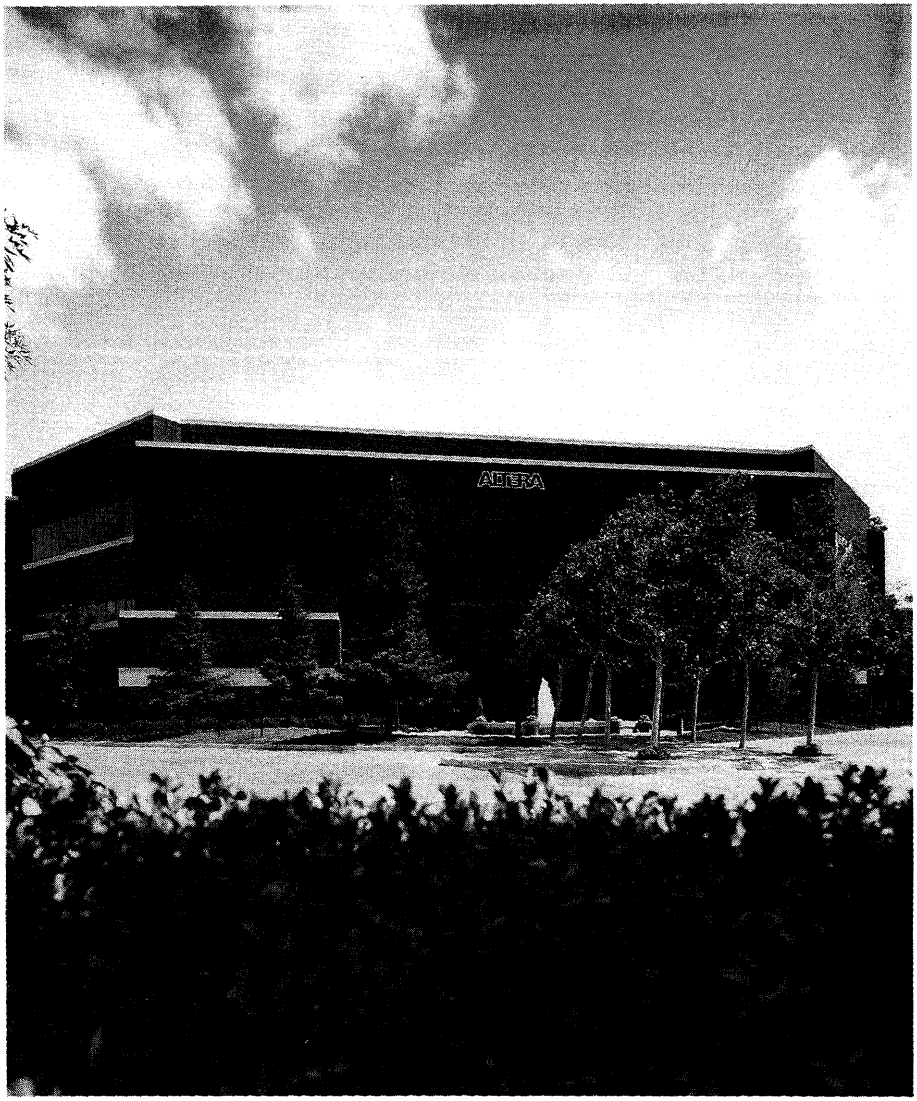
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Programmable Logic Overview

September 1991, ver. 2

Data Sheet

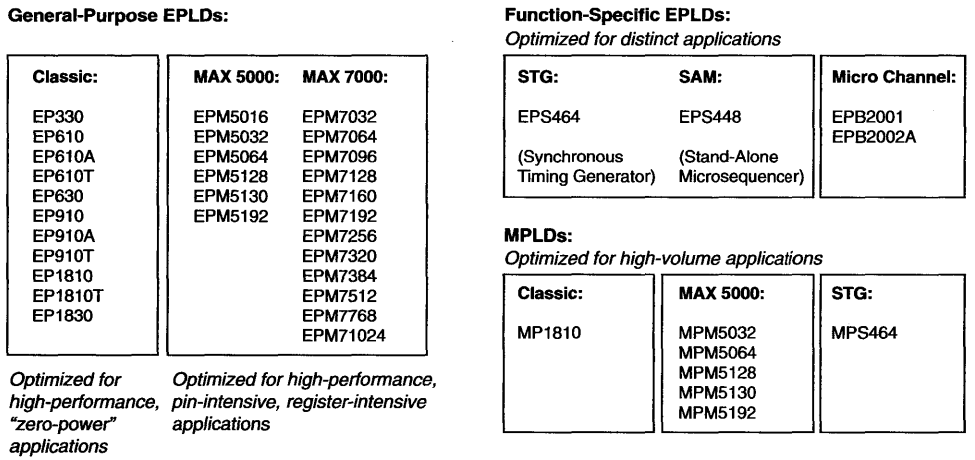
Introduction

Programmable Logic Devices (also described as PALs, PLAs, FPLAs, PLDs, EPLDs, EEPLDs, LCAs, and FPGAs) combine the logistical advantages of standard, fixed integrated circuits with the architectural flexibility of custom devices. These devices allow engineers to electrically program standard, off-the-shelf logic elements to meet the specific needs of their applications. Proprietary logic functions can be designed and fabricated in-house, eliminating the long engineering lead times, high tooling costs, complex procurement logistics, and dedicated inventory problems associated with custom Application-Specific Integrated Circuit (ASIC) devices, such as gate arrays and standard cells.

The key to this "off-the-shelf ASIC" capability is reprogrammable CMOS technology, which is used to create Erasable Programmable Logic Devices (EPLDs). Altera has taken advantage of speed and density advances in CMOS memory products to create sophisticated EPLDs that solve many logic design problems.

Altera provides the broadest line of CMOS EPLDs in the industry, with products ranging in density from 300 to 40,000 maximum gates, offered in a variety of packages with 20 to 288 pins. These EPLDs, together with Altera development software, enable system manufacturers to create custom logic functions for a wide variety of applications. See Figure 1.

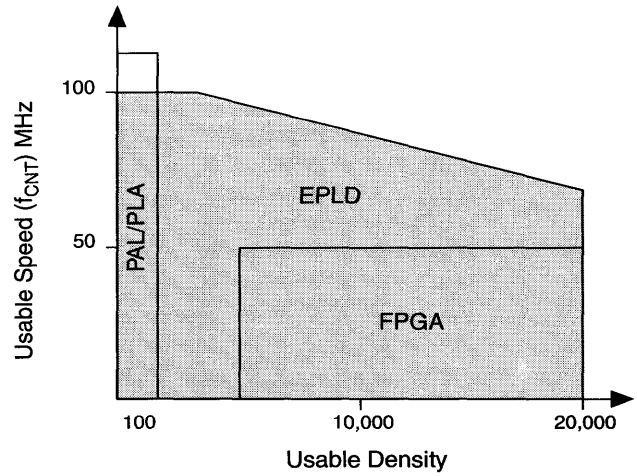
Figure 1. Altera EPLD Families



EPLDs can be used to integrate complete printed circuit boards of TTL, PAL, and FPGA devices into a single package. EPLDs are also valuable for prototyping high-density custom devices, which enables designers to test markets and evaluate systems before committing to expensive engineering development cycles and tooling charges. For most of today's applications, EPLDs not only ensure faster time-to-market, but also provide a lower total cost than custom ASIC solutions.

Altera concentrates on creating high-performance device architectures and easy-to-use, highly productive CAE software. Altera products meet the demands of designers who require complete solutions to logic integration that include both PAL speed and FPGA density. See Figure 2.

Figure 2. PLD Speed vs. Density



EPLD Families

Altera offers several families of EPLDs that satisfy many common board- and system-integration needs. EPLD families are divided into two architectural categories: the first provides maximum flexibility for general-purpose logic replacement; the second is specialized for performing specific system design tasks.

- General-purpose EPLDs are available in a variety of integration densities, ranging from PAL replacements to high-density devices that integrate thousands of TTL and random logic gates. These EPLDs are the Classic, MAX 5000, and MAX 7000 EPLD families.
  - The Classic architecture includes 20- to 68-pin EPLDs that feature zero-standby power, propagation delays (t_{PD}) as low as 12 ns, and counter frequencies up to 100 MHz.

- The Multiple Array Matrix (MAX) 5000 architecture includes 20- to 100-pin EPLDs that combine the high speed and ease-of-use of PAL devices with the density of FPGA devices. High-density MAX 5000 EPLDs can consolidate 20 to 25 PAL packages and over 100 TTL functions while offering system clock rates up to 50 MHz.

- The MAX 7000 family represents the second generation of the MAX architecture. These EPLDs range from 44 to 288 pins, provide integration densities of 1,200 to 40,000 maximum gates, and offer system clock rates up to 70 MHz.

❑ Function-specific EPLDs provide optimized integration for specific system design tasks. They are classified by their system design focus.

- The EPB2001 and EPB2002A Micro Channel EPLDs are bus-oriented devices designed to integrate all required add-on card logic for a Micro Channel bus interface.

- The EPS464 Synchronous Timing Generator (STG) and EPS448 Stand-Alone Microsequencer (SAM) EPLDs offer the logic and speed required for complex control logic, state machines, and imaging and display applications.

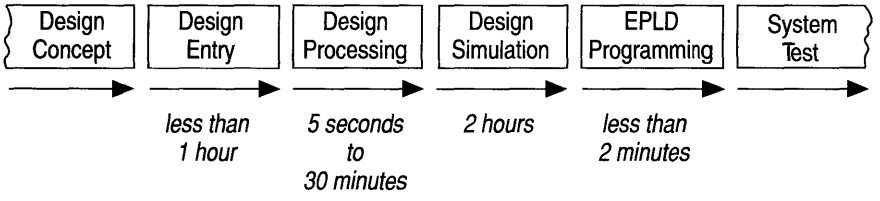
❑ Mask-Programmed Logic Devices (MPLDs) provide a low-cost masked alternative to EPLDs for customers with high-volume production.

A variety of package options is offered, including dual in-line (DIP), J-lead chip carrier (JLCC), small-outline integrated circuit (SOIC), quad flat pack (QFP), and pin-grid array (PGA) packages. EPLDs are available in windowed (erasable) ceramic packages or one-time-programmable (OTP) plastic versions. In addition, Mask-Programmed Logic Devices (MPLDs) are available for high-volume applications.

Software Tools

Altera software products are developed together with the EPLD architectures, so features are placed where they are most appropriate—in either software or hardware. The result is efficient software tools that offer familiar design entry methods and rapid design completion. See Figure 3. With Altera's CAE development tools, users can take a logic circuit from

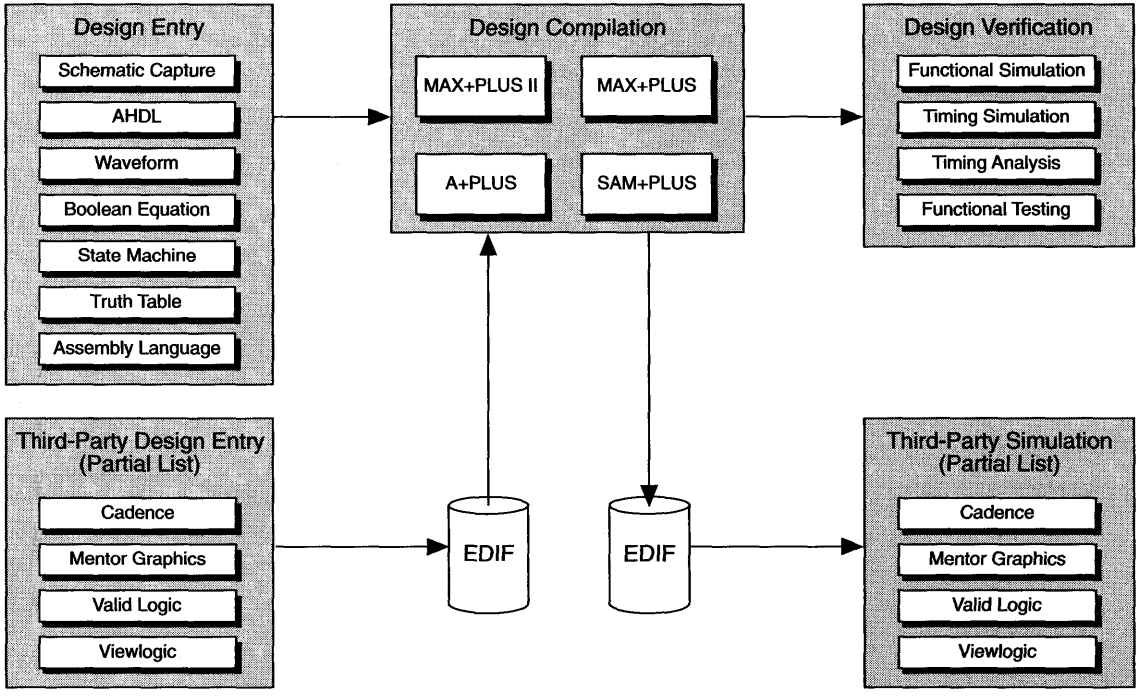
Figure 3. EPLD Design Methodology: from Concept to Silicon in Hours



design entry to device programming in a matter of hours. Design processing is typically completed in minutes, allowing several design iterations to be completed in a single day.

Altera software is available for IBM PC-AT, PS/2, and compatible computers, and workstations (HP/Apollo and Sun). Several design entry options are available: hierarchical schematic capture (with basic gate and complete TTL macrofunction libraries), the Altera Hardware Description Language (AHDL), Boolean equation, state machine, truth table, waveforms, netlist, and microcoded assembly language. See Figure 4. Design entry methods can be freely combined to create a single EPLD design. Design compilers perform minimization and logic synthesis, design fitting (analogous to automatic place-and-route), and generate programming data. Design verification via functional simulation, timing simulation, and delay prediction for speed-critical paths is also available. Hardware for programming EPLDs is offered by Altera and a variety of third-party vendors.

Figure 4. Altera Design Environment



Software interfaces to other design tools are provided by Altera and third-party translators, and via industry-standard EDIF netlists. Many third-party compilers also support Altera EPLDs directly.

EPLD Architecture

The Altera approach to logic design eliminates the necessity of mastering the inner complexities of EPLD architectures. The user can work with familiar design entry tools (e.g., TTL macrofunctions or a high-level state machine language), and the Altera software automatically translates the design into the format required to fit the EPLD architecture. For detailed architecture and pin-out descriptions of each device, refer to individual EPLD data sheets in this data book.

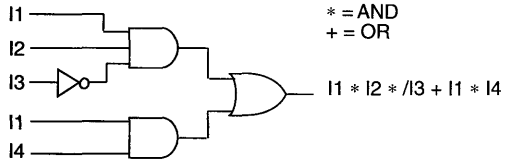
Basic Concepts

Altera general-purpose EPLDs provide dedicated input pins, user-configurable I/O pins, and programmable flip-flop and clock options that ensure maximum flexibility for integrating random logic functions.

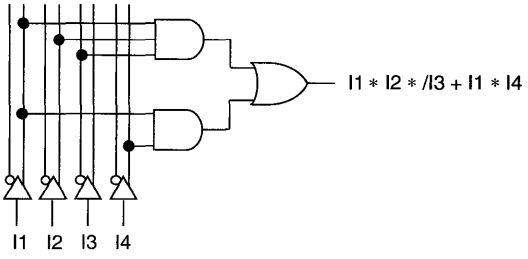
Each EPLD also contains an AND array that provides product terms. A product term is simply an *n*-input AND gate, where *n* is the number of connections. EPLD schematics use a shorthand AND-array notation to represent several large AND gates with common inputs. Figure 5 shows three different representations of the same logic function. Circuit A is presented in classic logic notation; Circuit B has been modified to a sum-of-products notation; and Circuit C is written in AND-array notation. A dot represents a connection between an input (vertical wire) and one of the 8-input AND gates. No dot implies no connection: the AND-gate input is unused and floats to a logic 1.

Figure 5. AND-Array Notation

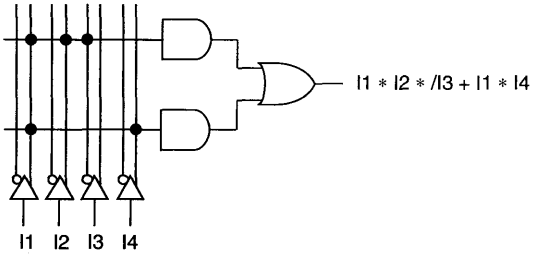
Circuit A: Typical Circuit



Circuit B: Circuit A drawn with complementary output buffers



Circuit C: Circuit B with 8-input AND gates in AND-array notation



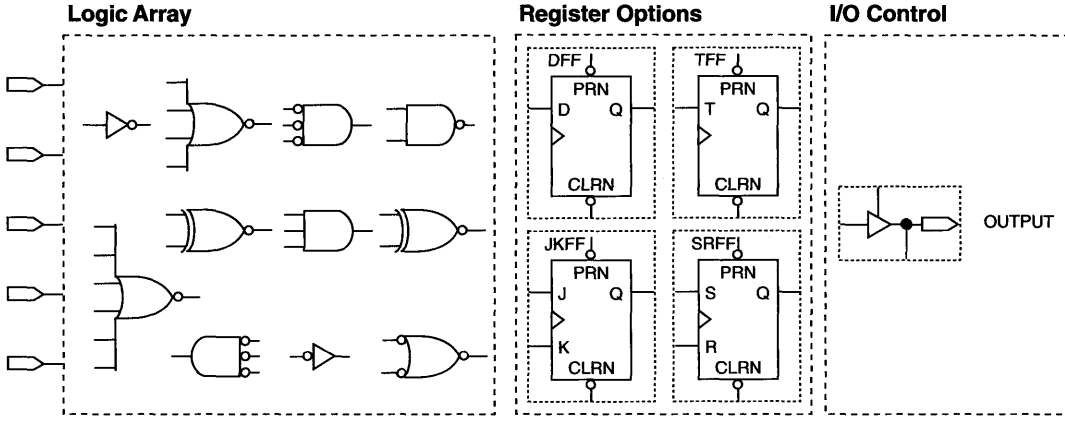
The 2 × 8 AND-array of Circuit C can produce any Boolean function of four variables (provided only two product terms are required) when expressed in sum-of-products form. Any Boolean expression—no matter how complex—can be written in sum-of-products form. Outputs of the two AND gates in Figure 5 are called product terms (or p-terms).

Macrocell Architecture

The fundamental building block of an Altera EPLD is the macrocell. Each macrocell consists of three parts (see Figure 6):

- The logic array implements all combinatorial logic functions.
- The programmable register provides D, T, JK, or SR options. The register can also be bypassed.
- Programmable I/O allows each I/O pin to be configured as a dedicated output, input, or bidirectional pin.

Figure 6. The Macrocell

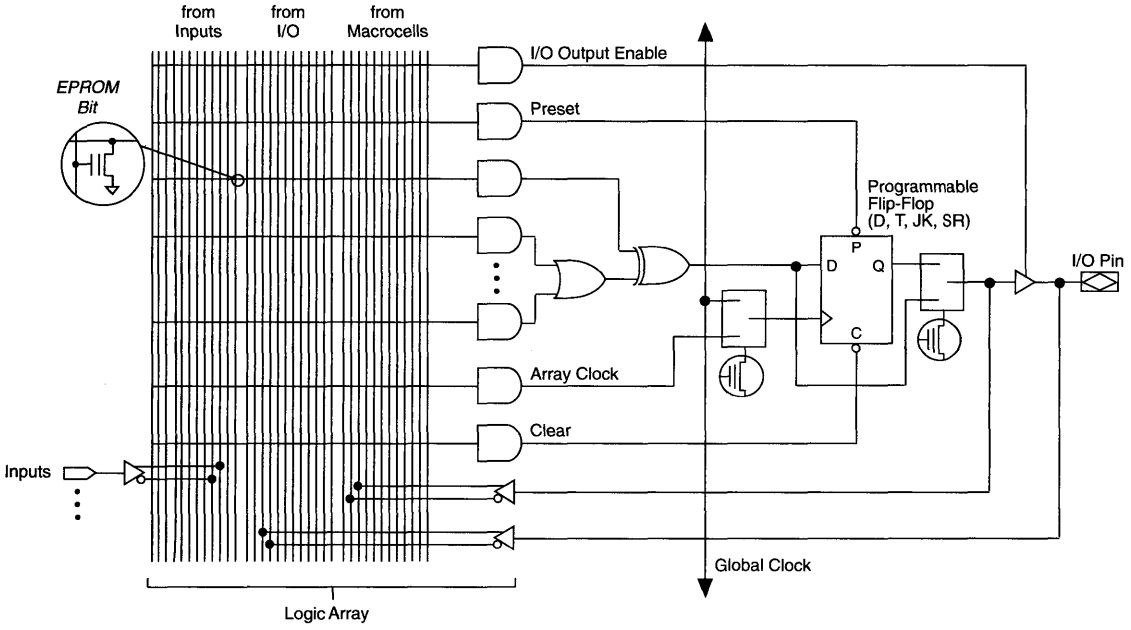


Logic Array

The logic array consists of a programmable-AND/fixed-OR array. Inputs to the AND array come from the true and complement of the dedicated input and clock pins, and from the macrocell and I/O feedback paths.

For each macrocell, the logic array typically contains 10 product terms that are distributed among the combinatorial and sequential resources. See Figure 7. Connections are opened during the programming process. Therefore, any product term may be connected to the true and complement of any array input signal. When both the true and complement of any signal are left intact, a logical false results on the output of the product term. If both the true and complement connection are open, a logical "don't care" results for that input. If all inputs for the product term are programmed opened, a logical true results on the output of the product term.

Figure 7. Detailed EPLD Macrocell Architecture



Several product terms feed a fixed OR whose output connects to an exclusive-OR (XOR) gate. The second input to the XOR function is controlled by a programmable resource (usually a product term) that allows the logic array output to be inverted. Altera software uses this gate to implement active-high or active-low logic, complex mutually exclusive and arithmetic functions, or to reduce the number of product terms to implement a function (by applying De Morgan's inversion). Figure 8 shows an OR function that requires six product terms in its current form. By using the "programmable" XOR gate and De Morgan's inversion, the OR function can be transformed into a NAND function:

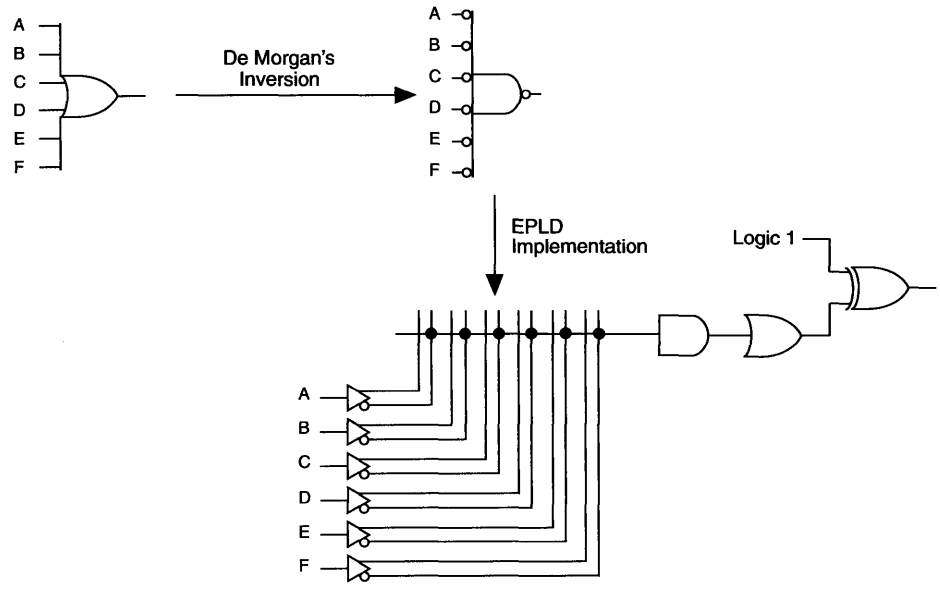
```
A+B+C+D+E+F = /(/A*/B*/C*/D*/E*/F)
```

This inversion from OR to AND translates the equation and reduces the number of fixed OR terms required in the logic array. Altera software automatically applies De Morgan's inversion and other logic synthesis techniques to optimize the use of the logic array.

Programmable Flip-Flops

Programmable flip-flops are used to create a variety of logic functions that use a minimum of EPLD resources. Each flip-flop can be programmed to provide a conventional D, T, JK, or SR function. MAX 5000 EPLD flip-flops can also be configured as flow-through latches. If the flip-flop is not required for macrocell logic, it may be simply bypassed. Macrocell flip-flops also have an asynchronous Clear and Preset capability that allows complete emulation of any TTL macrofunction.

Figure 8. Logic Minimization with De Morgan's Inversion



Programmable Clock

In general-purpose EPLDs (except the EP330), each internal flip-flop can be clocked from a dedicated global clock (also known as a synchronous clock), any input or I/O pin, or any internal logic function. For each flip-flop, a multiplexer selects either a pin or product-term source for the clock, so that flip-flops can be clocked independently or in user-defined groups. EPLD registers are positive-edge-triggered with data transitions that occur on the rising edge of the dedicated global clock.

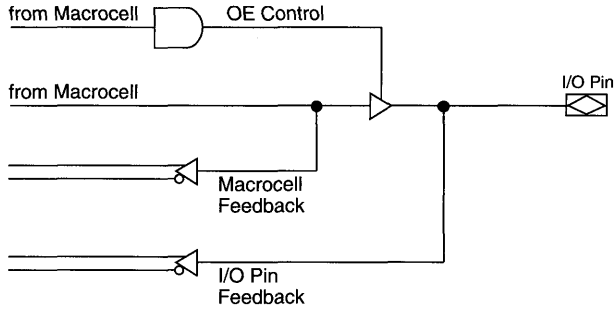
When the clock is driven by a product term, flip-flops can be configured for either positive- or negative-edge-triggered operation. In addition, product-term clocks allow gated-clock and clock-enable logic to be implemented. However, global clock signals have faster clock-to-output delay times than internally generated product-term clock signals.

I/O Control Block

The EPLD I/O block contains a tri-state buffer controlled by a macrocell product term, and drives the I/O pin (see Figure 9). I/O pins can be configured as dedicated outputs, bidirectional outputs, or as additional dedicated inputs. Most EPLDs have "dual feedback," whereby the macrocell feedback is decoupled from the I/O pin feedback. Dual feedback makes it possible to implement a buried function in the macrocell while the I/O pin is used simultaneously as a dedicated input. Applications that require bus-oriented functions or many buried flip-flops such as counters, shift registers, and state machines are easily accommodated by this programmable I/O block.

Figure 9. I/O Control Block

The decoupled I/O control block features dual feedback to maximize use of the EPLD pins.



Zero-Power/ Turbo Operation

CMOS technology generally implies lower power dissipation than older bipolar technology. In fact, Altera pioneered true "zero-standby" power operation. By using a unique input-transition detection scheme, most Classic EPLDs require only microamp currents during quiescent periods. This feature saves power in applications clocked at low to medium frequencies. Each input is connected to a transition-detection circuit consisting of an XOR gate, delay element, and OR gate. The trigger output of the OR gate activates logic array power-up on any transition, allowing new input conditions to propagate to EPLD outputs. The logic array is then automatically powered down to await the next transition. The transition-detection circuitry adds an additional 30% to 40% delay to the EPLD input/output path. Consequently, a programmable Turbo Bit is provided to disable the input transition detection circuitry and permanently enable the logic array, giving the user a choice of either extra speed or lower power consumption. The EPLD also exhibits better system noise rejection characteristics in the turbo mode, which should be used where noisy environments are a problem. The Turbo Bit is included in the EPLD programming file.

Altera CMOS EPROM Technology

Until Altera invented the first EPLD—the EP300—in 1984, the only technology used for Programmable Logic Devices (PLDs) was bipolar and fuse-based. The active elements on these devices were constructed from traditional bipolar transistors (i.e., TTL), with arrays of fuses providing programmable interconnect structures. These fuse elements consisted of a variety of exotic metal alloys and/or polysilicon structures, but all relied on the physical destruction of fuses to open connections by passing large currents through their small geometries.

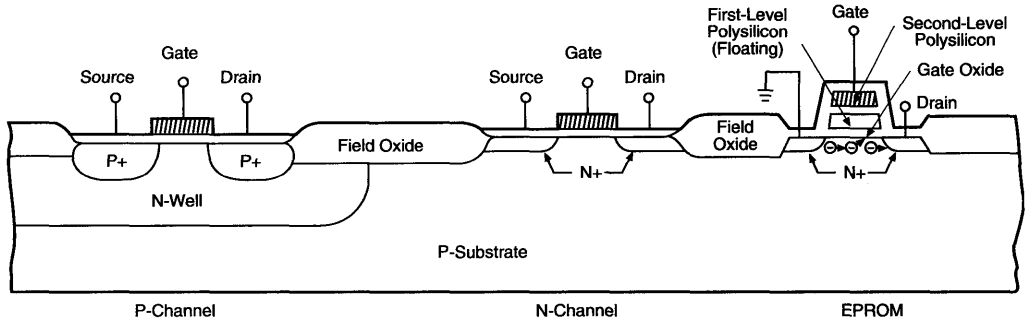
The melting process in bipolar PLD fuses is difficult to control and often results in poor and unpredictable programming yields. Since the process is irreversible, guaranteed results are impossible. The power-hungry bipolar

technology also severely limits integration levels. Altera's pioneering efforts have replaced bipolar technology with CMOS, and fuses with reprogrammable EPROM bits. These EPLD bits are much smaller than fuses, electrically programmable, and UV-erasable. EPLDs are fully factory-tested, guaranteeing 100% programming yield at the customer site. CMOS technology also provides low-power operation that allows higher integration levels.

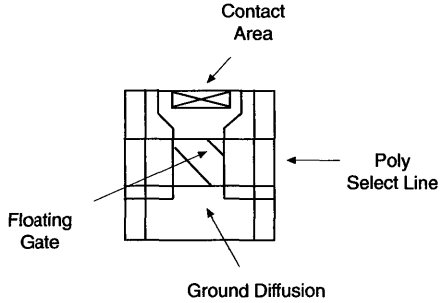
The EPROM cell operates via floating-gate charge injection. The programming process consists of placing sufficient voltage (typically >12 V) on the drain of the transistor to create a strong electric field and energize electrons to jump from the drain region to the floating gate. Electrons are attracted to the floating gate and become trapped when the voltage is removed. If the gate remains at a low voltage during programming, electrons are not attracted and the floating gate remains uncharged. Trapped charge changes the threshold of the EPROM cell from a relatively low value with no charge present ("erased") to a higher value when programmed. Figure 10 shows a basic cross-section of the cell technology.

Figure 10. CMOS EPLD Technology

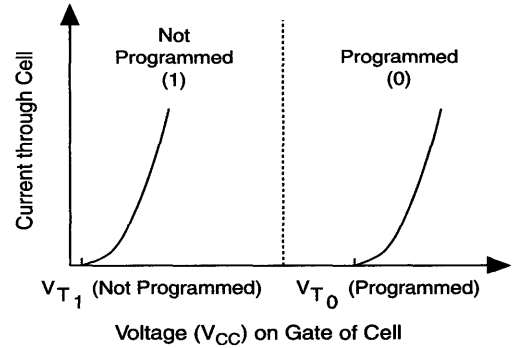
Cross Section



EPROM Cell



EPROM Threshold Shift



Within the EPLD's programmable array, a sense amplifier/comparator is placed at the end of each product-term line. By setting a reference voltage into it—halfway between the programmed and unprogrammed levels—the state of the EPROM cells along the product term is sensed and used to select the desired logic function. Low-threshold cells with a logic 1 placed on their select gates (i.e., associated input) tend to pull the product-term line down and cause the logic term to change to a logic 0. Transistors with high thresholds do not conduct even when their gates are at a logic 1, and effectively represent a no-connect. This technology—pioneered with EPROM memory in the early 1970s—made possible Altera EPLDs that can be tested, programmed, and operated reliably. Altera devices currently use state-of-the-art 0.8-micron, CMOS EPROM technology; work is underway to move to even smaller geometries. Because the basic logic array consists of *N*-channel EPROM transistors, EPLD characteristics are optimized to maximize performance of the *N*-channel device. This approach minimizes overall input-to-output delays on the chip.

EPROM Cell Margin

To ensure reliable operation in user systems, all EPLDs undergo substantial factory testing prior to shipment. Foremost among these tests are cell-margin tests, which guarantee the in-service retention of EPROM bit programming. Cell-margin testing determines the amount of charge trapped on the floating gate structure.

Charge loss occurs when electrons leak from the floating gate structure over time, and results in a net reduction in programmed cell threshold. Charge gain results from an accumulation of charge on the floating gate, usually caused by electric fields produced by operating the EPLD. Since charge loss and charge gain mechanisms can affect program retention, Altera reliability evaluation includes EPLD burn-in at temperatures of up to 250° C for periods of a week or more. This burn-in period corresponds to more than 100,000 years of operation at 70° C.

Figure 11. EPROM Cell Margin

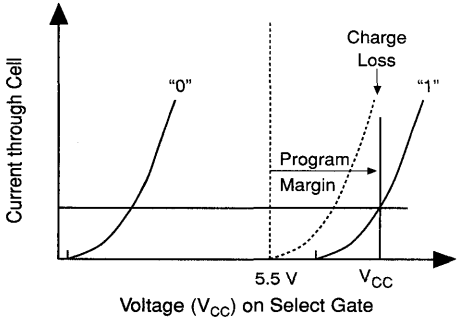
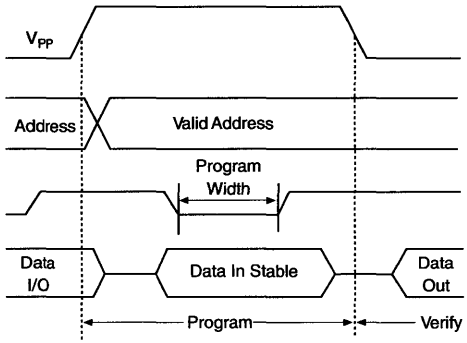


Figure 11 illustrates the concept of cell margin. As mentioned earlier, EPROM arrays depend on cell threshold shifts for correct operation. Zero and One I-V characteristics for the EPROM cell are shown. Program margin is a measure of the spread between the actual device threshold and the minimum required device threshold for correct operation.

To calibrate cell margins, Altera EPLDs are subjected to special test modes that allow EPROM-bit gate voltages to be controlled externally. Cell margins are measured by varying this voltage, a method that accurately monitors cell charge and retention.

Figure 12 shows a typical programming cycle for Altera EPLDs. The normal programming procedure consists of the following steps:

Figure 12. Programming Waveforms



1. The programming pin (V_{PP}) is raised to the super-high-input level (nominally 12.5 V).
2. Row and column addresses are placed on the designated pins.
3. Programming data is placed on the designated pins.
4. The programming algorithm is executed with a sequence of 100-µs programming pulses separated by program verify cycles.
5. Overprogram or margin pulses may be applied to doubly ensure EPLD programming.

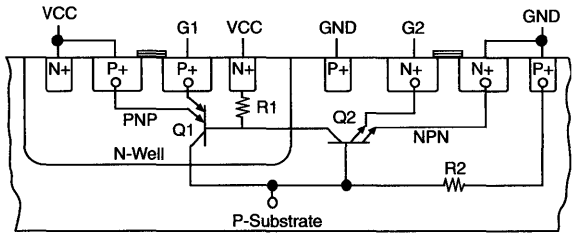
The programming operation is typically performed eight bits at a time on either Altera-supplied or other approved programming hardware. Altera EPLDs also feature a Security Bit (i.e., verify-protect bit) that can be programmed to prevent any interrogation of the device's contents. The Security Bit can be set during the programming process to ensure EPLD design security.

Latch-Up

Parasitic bipolar transistors are present in the fundamental structure of CMOS devices. Typically, the base-emitter and base-collector junctions of these transistors are not forward-biased, so the transistors are not turned on. Figure 13 shows a cross-section of a CMOS wafer and primary parasitic transistors. By connecting the *P*-type substrate to the most negative voltage available on-chip (V_{SS}) and the *N*-type well structure to the most positive voltage on-chip (V_{CC}), all junctions should, in theory, remain reverse-biased. However, two factors can alter this ideal state.

Figure 13. Parasitic Bipolar Transistors in CMOS

Source of Latch-Up



As shown in Figure 13, parasitic resistors also occur in the CMOS structure. These resistors are of no concern as long as currents do not flow through the structure laterally. But if any of the associated diodes turn on for any reason, I-R drops may occur in the structure. The initial turn-on of these diodes usually is the result of power-supply or I/O-pin transients that exceed the limits of V_{SS} and V_{CC}. These transients may be induced by signal ringing and other inductive effects in the system.

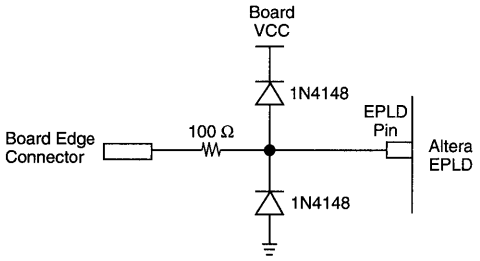
A problem may exist if parasitic structures begin to conduct, since the effect is regenerative and reinforces itself until potentially destructive currents flow. This is the silicon-controlled rectifier (SCR) effect called "latch-up." Figure 13 shows that as current flows through the parasitic transistor, the I-R drop through the resistor increases, further forward-biasing the base-emitter junction. The cycle continues until the current is limited by drops in the primary current path. However, this current might reach a level that permanently damages internal circuitry.

Altera components have been designed to eliminate the effects of latch-up, including power-supply and I/O-pin transients. Under reasonable system operating conditions, all EPLDs are guaranteed to withstand input voltage extremes of between V_{SS} – 1 V and V_{CC} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins. To minimize the possibility of inducing latch-up, Altera recommends a few general system design guidelines for power and input sequencing to the EPLD. For example, voltages and logic inputs should normally be applied in the following order:

1. V_{SS} or GND
2. V_{CC} (+5 V)
3. Inputs

When removing power from the EPLD, the order should be reversed: first, inputs are removed or taken low, then V_{CC} is removed or lowered. Simultaneous application of inputs and V_{CC} to the device, which might occur as a power supply ramps during power-up, should be safe. Care should be taken to ensure that inputs cannot rise faster than supply under extreme conditions.

Figure 14. Hot Socket Protection

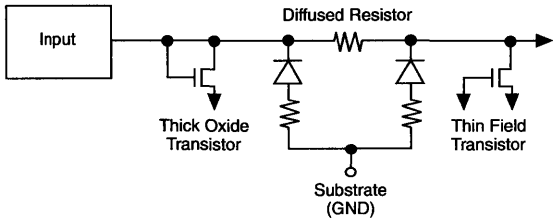


In some applications, boards are "hot-socketed" in the field. The circuitry shown in Figure 14 is recommended to ensure that latch-up-inducing levels are not applied to the EPLD under these conditions. Normally, this circuitry is required only if the EPLD has inputs tied directly to the edge connector. The diodes clamp the inputs at acceptable levels and the series resistor further limits the injection of current into the EPLD input and clamp diodes. This interface provides maximum protection.

Electrostatic Discharge

Electrostatic discharge (ESD) can cause device failure when improper handling occurs. EPLD handling during the programming cycle increases exposure to potential static-induced failure. Voltages into the tens of kilovolts can be generated by the human body during normal activity. Wearing ground straps during device handling and grounding all surfaces that come in contact with components reduces the likelihood of damage.

Figure 15. EPLD Input Protection Structure



Altera components include special structures that reduce the effects of ESD at the pins. Figure 15 shows a typical input structure. Diode structures as well as specialized field-effect transistors shunt harmful voltages to ground before destructive currents will flow. Altera EPLDs typically withstand ESD voltages >2 kV, and are thus safe under normal handling conditions.

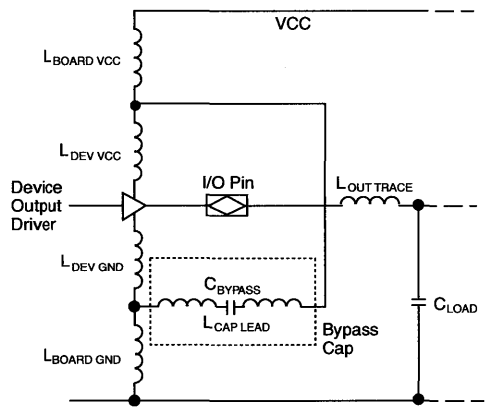
Output Drive Characteristics

The CMOS push-pull output stages used on Altera EPLDs provide good AC and DC load-driving capability in a system environment. I_{OL} and I_{OH} specifications for general-purpose EPLDs are guaranteed at 4 mA to 24 mA, depending on the device. AC output characteristics are typically specified with 35 pF output loads. Additional output capacitive loading affects the device output delay. The timing parameter used is $\mathbf{t_{PD}}$ (input-output combinatorial delay). The incremental delay per picoFarad of capacitance is typically ≤ 0.1 ns at room temperature.

System Noise

Large switching currents can flow through power supply and output pins during high-performance operation. If a 50-pF capacitor is charged from 0 to 5 V in 10 ns, a dynamic current of 24 mA will flow. If 24 outputs on an EPLD switch simultaneously (for example, in an EP910), the total transient current can exceed 600 mA! This current can severely degrade V_{CC} supply voltage due to the inductive properties of the device and system environment. Figure 16 shows the distribution of typical inductances that can contribute to the problem.

Figure 16. Board-Level Noise Problem



The key to controlling these inductive effects is to adequately decouple the V_{CC} supply to ground at each EPLD with a suitable capacitor or combination of capacitors. This capacitor can then act as a reservoir of charge to supply the transient switching needs of the device. Altera recommends that a 0.2 µF capacitor be connected from each V_{CC} pin to ground at the device. High-quality capacitors with low internal and lead inductance (monolithic ceramic or tantalum) should be used, and leads must be kept short to limit series inductance that degrades capacitor effectiveness. Careful decoupling of the power supply is good design practice.

Product Selection Guide

September 1991, ver. 2

Data Sheet

Introduction

This Product Selection Guide summarizes the range of products available from Altera:

- ❑ General-purpose EPLDs
- ❑ Function-specific EPLDs
- ❑ Military-qualified EPLDs
- ❑ Programmable logic development systems
- ❑ Programmable logic software
- ❑ Software warranty
- ❑ Programming hardware & adapters

For detailed descriptions of the Altera products listed here, refer to the individual data sheets in this data book and to the *Micro Channel Adapter Handbook*.

Classic EPLDs

Table 1 gives information on the Classic family of general-purpose, zero-standby-power EPLDs. Classic EPLDs are suitable for random logic, and TTL and PAL integration.

Table 1. General-Purpose Classic EPLDs

EPLD (1)	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Macrocells (Registers)	Dedicated Inputs	I/O	Number of Pins
EP330	P,L,S	C	-12	12	125	75	75	8	10	8	20
EP330	P,L,S	C	-15	15	100	75	75	8	10	8	20
EP610	P,L,S	C	-15	15	83.3	90	0.15	16	4	16	24; 28
EP610	P,L,S	C,I	-20	20	62.5	90	0.15	16	4	16	24; 28
EP610	D,P,J,L,S	C	-25	25	47.6	60	0.15	16	4	16	24; 28
EP610	D,P,J,L,S	C,I	-30	30	41.7	60	0.15	16	4	16	24; 28
EP610	D,P,J,L,S	C,I,M	-35	35	37.0	60	0.15	16	4	16	24; 28
EP610A	P,L,S	C	-10	10	100	90	90	16	4	16	24; 28
EP610A	P,L,S	C	-12	12	83.3	90	90	16	4	16	24; 28
EP610T	P,L,S	C	-15	15	83.3	90	90	16	4	16	24; 28
EP610T	P,L,S	C	-20	20	62.5	90	90	16	4	16	24; 28
EP610T	P,L,S	C	-25	25	47.6	90	90	16	4	16	24; 28
EP630	P,L,S	C	-15	15	83.3	90	0.15	16	4	16	24; 28
EP630	P,L,S	C	-20	20	62.5	90	0.15	16	4	16	24; 28
EP910	D,P,J,L	C	-30	30	41.7	80	0.15	24	12	24	40; 44
EP910	D,P,J,L	C,I	-35	35	37.0	80	0.15	24	12	24	40; 44
EP910	D,P,J,L	C,I,M	-40	40	32.3	80	0.15	24	12	24	40; 44
EP910A	P,L	C	-15	15	83.3	150	150	24	12	24	44
EP910A	D,P,J,L	C	-25	25	62.5	150	150	24	12	24	40; 44
EP910T	P,L	C	-30	30	41.7	115	115	24	12	24	40; 44
EP1810	L	C	-20	20	62.5	225	0.15	48	16	48	68
EP1810	L	C,I	-25	25	50.0	225	0.15	48	16	48	68
EP1810	J,L,G	C	-35	35	40.0	180	0.15	48	16	48	68
EP1810	J,L,G	C,I,M	-45	45	33.3	180	0.15	48	16	48	68
EP1810T	L	C	-20	20	62.5	250	250	48	16	48	68
EP1810T	L	C,I	-25	25	50.0	250	250	48	16	48	68
EP1810T	L	C	-35	35	40.0	215	215	48	16	48	68
EP1830	L	C	-20	20	62.5	225	0.15	48	16	48	68
EP1830	L	C	-25	25	50.0	225	0.15	48	16	48	68

Notes to tables 1, 2, 3, 4, and 5 are listed on page 21.

MAX 5000 EPLDs

Table 2 provides information on the MAX (Multiple Array MatriX) 5000 family of general-purpose EPLDs. MAX 5000 EPLDs are suitable for register-intensive random logic, and TTL and PAL integration.

Table 2. General-Purpose MAX 5000 EPLDs

EPLD	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Macrocells (Registers)	Dedicated Inputs	I/O	Number of Pins
EPM5016	D,P,J,L,S	C	-15	15	100.0	115	110	16	8	8	20
EPM5016	D,P,J,L,S	C,I	-17	17	83.3	115	110	16	8	8	20
EPM5016	D,P,J,L,S	C,I,M	-20	20	62.5	115	110	16	8	8	20
EPM5032	D,P,J,L,S	C	-15	15	83.3	155	150	32	8	16	28
EPM5032	D,P,J,L,S	C	-17	17	83.3	155	150	32	8	16	28
EPM5032	D,P,J,L,S	C,I	-20	20	71.4	155	150	32	8	16	28
EPM5032	D,P,J,L,S	C,I,M	-25	25	62.5	155	150	32	8	16	28
EPM5064	J,L	C	-1	25	62.5	135	125	64	8	28	44
EPM5064	J,L	C,I	-2	30	50.0	135	125	64	8	28	44
EPM5064	J,L	C,I,M		35	40.0	135	125	64	8	28	44
EPM5128	J,L,G	C	-1	25	62.5	250	225	128	8	52	68
EPM5128	J,L,G	C,I	-2	30	50.0	250	225	128	8	52	68
EPM5128	J,L,G	C,I,M		35	40.0	250	225	128	8	52	68
EPM5130	J,L,G,Q,W	C	-1	25	62.5	275	250	128	20	64	84; 100
EPM5130	J,L,G,Q,W	C	-2	30	50.0	275	250	128	20	64	84; 100
EPM5130	J,L,G,Q,W	C,I,M		35	40.0	275	250	128	20	64	84; 100
EPM5192	J,L,G,Q,W	C	-1	25	62.5	380	360	192	8	64	84; 100
EPM5192	J,L,G,Q,W	C	-2	30	50.0	380	360	192	8	64	84; 100
EPM5192	J,L,G,Q,W	C,I,M		35	40.0	380	360	192	8	64	84; 100

Notes to tables 1, 2, 3, 4, and 5 are listed on page 21.

Function-Specific EPLDs

Tables 3 and 4 provide information on the function-specific Synchronous Timing Generator (STG) and Stand-Alone Microsequencer (SAM) EPLDs. These EPLDs are suitable for implementing high-performance state machines, waveform generators, and control logic.

Table 5 gives information on the Micro Channel EPLDs, which provide all the essential functions to interface a PS/2 add-on card with the Micro Channel bus. (Refer to the *Micro Channel Adapter Handbook* for detailed information on these EPLDs.)

Table 3. STG EPLDs

EPLD (1)	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Macrocells (Registers)	Dedicated Inputs	I/O	Number of Pins
EPS464	J,L,Q	C	-20	20	71.4	125	120	64	4	32	44
EPS464	J,L,Q	C	-25	25	50.0	125	120	64	4	32	44

Table 4. SAM EPLDs

EPLD	Pkg. (2)	Temp. (3)	Speed Grade	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Microcode EPROM	Branch EPLD	Stack	Dedicated Inputs	I/O	Number of Pins
EPS448	D,P,J,L	C	-30	30	140	95	448 × 36	768 p-term	15 × 8	8	16	28
EPS448	D,P,J,L	C	-25	25	140	95	448 × 36	768 p-term	15 × 8	8	16	28
EPS448	D,P,J,L	C,I,M	-20	20	140	95	448 × 36	768 p-term	15 × 8	8	16	28

Table 5. Micro Channel EPLDs

EPLD	Package (2)	Temperature (3)	Description	Number of Pins
EPB2001	J,L	C	Single-chip interface adapter for PS/2 Micro Channel	84
EPB2002A	L,P	C	DMA arbitration support chip for PS/2 Micro Channel	28

Notes to Tables 1, 2, 3, 4 & 5:

(1) Preliminary data is shown for some parameters. Consult individual device data sheets for complete information.

(2) Package configurations:
- D: Windowed ceramic dual in-line package (CerDIP).
- P: One-time-programmable plastic dual in-line package (PDIP).
- J: Windowed ceramic J-lead chip carrier (JLCC).
- L: One-time-programmable plastic J-lead chip carrier (PLCC).
- G: Windowed ceramic pin-grid array (PGA).
- S: One-time-programmable plastic small-outline integrated circuit (SOIC).
- Q: One-time-programmable plastic quad flat pack (PQFP).
- W: Windowed ceramic quad flat pack (WQFP).

(3) Operating temperature:
- C: Commercial (0° C to 70° C).
- I: Industrial/Automotive (–40° C to 85° C).
- M: Military (–55° C to 125° C).

Military-Qualified EPLDs

Table 6 provides information on Altera's military-qualified Classic EPLDs; Table 7 gives information on military-qualified MAX 5000 EPLDs.

Table 6. Military-Qualified Classic EPLDs

EPLD *(1)*	Pkg. *(2)*	Assurance Level *(3)*	t_{PD1} (ns)	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Macrocells (Registers)	Dedicated Inputs	I/O	Number of Pins	Altera Military Drawing *(4)*
EP310	D	883B	50	31.3	40	0.9	8	10	8	20	02D-00179
8863501RA	D	DESC	50	31.3	40	0.9	8	10	8	20	
EP320	D	883B	45	30.3	40	—	8	10	8	20	02D-00209
EP600	D	883B	55	22.2	60	—	16	4	16	24	02D-00194
EP600	J	883BX	55	22.2	60	—	16	4	16	28	02D-00194
8686401LA	D	DESC	55	22.2	60	—	16	4	16	24	
8686401XX	J	DESC	55	22.2	60	—	16	4	16	28	
EP610	D	883B	35	37.0	100	0.9	16	4	16	24	02D-00522
EP610	J	883BX	35	37.0	100	0.9	16	4	16	28	02D-00522
8947601LX	D	DESC	35	37.0	100	0.9	16	4	16	24	
8947601XX	J	DESC	35	37.0	100	0.9	16	4	16	28	
EP900	D,J	883B	60	20.0	100	—	24	12	24	40;44	02D-00521
8854801QA	D	DESC	60	20.0	100	—	24	12	24	40	
8854801XX	J	DESC	60	20.0	100	—	24	12	24	44	
EP910	D,J	883B	40	32.3	150	0.9	24	12	24	40;44	02D-00935
EP1800	J,G	883B	75	18.2	180	—	48	16	48	68	02D-00509
8854902YC	G	DESC	75	18.2	180	—	48	16	48	68	
EP1810	J,G	883B	45	33.3	240	0.9	48	16	48	68	02D-00782
8946901YC	J,G	DESC	45	33.3	240	0.9	48	16	48	68	

Table 7. Military-Qualified MAX 5000 EPLDs

EPLD (1)	Pkg. (2)	Assurance Level (3)	t_{PD1} (ns)	f_{MAX} (MHz)	I_{CC3} (mA) Active	I_{CC1} (mA) Standby	Macrocells (Registers)	Dedicated Inputs	I/O	Number of Pins	Altera Military Drawing (4)
EPM5032	D,J	883B	25	62.5	225	200	32	8	16	28	02D-00828
90611XXLA	D	DESC	25	62.5	225	200	32	8	16	28	
90611XXXA	J	DESC	25	62.5	225	200	32	8	16	28	
EPM5128	J,G	883B	35	40.0	350	300	128	8	52	68	02D-01015
89468XXXA	J	DESC	35	40.0	350	300	128	8	52	68	
89468XXYC	G	DESC	35	40.0	350	300	128	8	52	68	

Notes to Tables 6 & 7:

(1) All military-qualified EPLDs are rated to military temperatures (–55° C to 125° C). Preliminary data is shown for some other parameters. Consult individual device data sheets for complete information.

(2) Package configurations:
D: Windowed ceramic dual in-line package (CerDIP).
J: Windowed ceramic J-lead chip carrier (JLCC).
G: Windowed ceramic pin-grid array (PGA).

(3) Product assurance levels:
883B: Processed to MIL-STD-883, current revision.
883BX: Processed to MIL-STD-883, current revision with modified J-lead package dimension.
DESC: DESC Standard Military Drawing (SMD). Consult Altera or DESC for availability.

(4) A Military Product Drawing (MPD) is prepared in accordance with the appropriate military specification format. When a Source Control Drawing (SCD) is necessary, the appropriate MPD is required for proper SCD preparation.

Development Systems & Software

Altera opens up system design possibilities with the broadest line of high-density CMOS programmable logic devices available. Altera also provides a complete set of logic design tools that run in popular environments, including PC (Windows version 3.0 or higher), PC (DOS), HP/Apollo (Domain), and Sun (UNIX). See Figure 1. An EDIF netlist interface allows the workstation user to enter designs and perform board-level simulation for EPLDs with tools supplied by companies such as Cadence, Mentor Graphics, Valid Logic, Viewlogic, and Logic Automation.

Altera's MAX+PLUS II design software allows the designer to quickly and efficiently enter, compile, and verify designs with 20,000 or more gates right on a standard PC, HP/Apollo workstation, or Sun workstation. When the design is complete, it can be programmed into one or more high-performance Altera EPLDs and tested in-system.

Table 8 shows the software and hardware development products available from Altera. Programmable Logic Development Systems (with the PLDS- or PLCAD- prefix) are stand-alone combinations of hardware and software. Programmable Logic Software packages (with the PLS- prefix) are software-only products that can be used together with programming hardware from Altera or third-party manufacturers. Each package is described in this data sheet. Table 9 shows which EPLDs each software package supports.

Figure 1. Altera Support for Development Environments

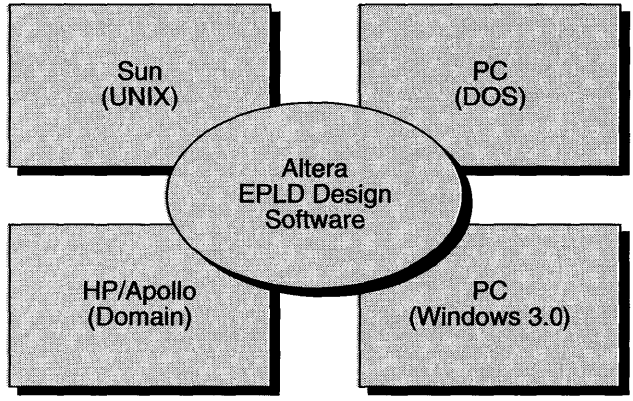


Table 8. Altera Development Systems & Software

	Design Entry							Design Compilation & Verification							
MAX+PLUS II:	Schematic Capture	AHDL	Waveform Entry	State Machine Entry	Boolean Equation Entry	Assembly Language Entry	Table Entry	Functional Simulation	Timing Simulation	Timing Analysis	Waveform Editing	Design Partitioning	Multi-EPLD Simulation	EDIF Interface	Programming Hardware
PLDS-HPS	✔	✔	✔	✔	✔			✔	✔	✔	✔	✔	✔	✔	✔
PLS-HPS	✔	✔	✔	✔	✔			✔	✔	✔	✔	✔	✔	✔	
PLS-OS		✔		✔	✔							✔		✔	
PLS-ES		✔		✔	✔										
PLS-WS/HP		✔		✔	✔							✔		✔	
PLS-WS/SN		✔		✔	✔							✔		✔	
MAX+PLUS:															
PLDS-MAX	✔	✔		✔	✔				✔	✔	✔				✔
PLS-MAX	✔	✔		✔	✔				✔	✔	✔				
A+PLUS:															
PLCAD-SUPREME	✔			✔	✔			✔							✔
PLS-SUPREME	✔			✔	✔			✔							
SAM+PLUS:															
PLDS-SAM				✔		✔		✔							✔
PLS-SAM				✔		✔		✔							
MCMap:															
PLDS-MCMAP							✔								✔
PLS-MCKIT							✔								
MAX+PLUS, A+PLUS & SAM+PLUS:															
PLDS-ENCORE	✔	✔		✔	✔	✔		✔	✔	✔	✔				✔
EDIF Interface:															
PLS-EDIF														✔	

Table 9. Altera Development System & Software EPLD Support

Development System/Software	MAX 7000	MAX 5000	Classic	STG	SAM	Micro Channel
MAX+PLUS II:						
PLDS-HPS	✔	✔	✔	✔		
PLS-HPS	✔	✔	✔	✔		
PLS-OS	✔	✔	✔	✔		
PLS-ES		*(1)*	✔			
PLS-WS/HP	✔	✔	✔	✔		
PLS-WS/SN	✔	✔	✔	✔		
MAX+PLUS:						
PLDS-MAX		✔				
PLS-MAX		✔				
A+PLUS:						
PLCAD-SUPREME			✔			
PLS-SUPREME			✔			
SAM+PLUS:						
PLDS-SAM					✔	
PLS-SAM					✔	
MCMap:						
PLDS-MCMAP						✔
PLS-MCKIT						✔
MAX+PLUS, A+PLUS & SAM+PLUS:						
PLDS-ENCORE		✔	✔		✔	
EDIF Interface:						
PLS-EDIF		✔				

Note:
(1) PLS-ES supports the single-LAB EPM5016 and EPM5032 MAX 5000 EPLDs.

MAX+PLUS II

MAX+PLUS II Windows 3.0-based development software is a fully integrated package for designing logic with Altera's Classic, MAX 5000, MAX 7000, and STG EPLDs. The complete MAX+PLUS II system provides an intuitive graphical interface that supports hierarchical graphic, text, and waveform design entry with over 300 TTL macrofunctions. It includes the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, and truth table entry methods. MAX+PLUS II provides highly automated compilation, design partitioning, timing simulation and analysis, delay prediction for speed-critical paths, automatic error location, device programming and verification, a design archiver, and a detailed on-line help system. MAX+PLUS II also imports and exports standard EDIF netlist files, providing a convenient workstation interface. MAX+PLUS II is available in six configurations to fit every design need:

PLDS-HPS: Complete MAX+PLUS II Development System. This package provides the complete MAX+PLUS II software, including graphic, waveform, and text design entry with AHDL; automated compilation; design partitioning; timing simulation; timing analysis; programming software and hardware (a Logic Programmer card and the Master Programming Unit [MPU]); a bidirectional EDIF interface; programming adapters; and sample EPLDs. PLDS-HPS supports Altera's MAX 7000, MAX 5000, Classic, and Synchronous Timing Generator (STG) EPLDs.

PLS-HPS: "High-Performance System" that provides the complete MAX+PLUS II software. This software-only version of PLDS-HPS includes graphic, waveform, and text design entry with AHDL; automated compilation; design partitioning; timing simulation; timing analysis; programming software; and a bidirectional EDIF interface. PLS-HPS supports Altera's MAX 7000, MAX 5000, Classic, and STG EPLDs.

PLS-OS: "Open System" version of the MAX+PLUS II software for the user who already has third-party CAE software for schematic capture and simulation. This package includes text design entry with AHDL; automated compilation; design partitioning; programming software; and a bidirectional EDIF interface. PLS-OS supports Altera's MAX 7000, MAX 5000, Classic, and STG EPLDs.

PLS-ES: "Entry System" version of the MAX+PLUS II software for the user who needs to develop logic circuits for Altera's small- and medium-size, fast EPLDs. This package includes text design entry with AHDL and automated compilation. PLS-ES supports Altera's Classic EPLDs, as well as the single-LAB MAX 5000-family EPM5016 and EPM5032 EPLDs.

PLS-WS/HP: Provides an HP/Apollo workstation-compatible version of the MAX+PLUS II Compiler (with design partitioning), and a bidirectional EDIF 2 0 0 netlist interface for transferring designs between

the Compiler and Mentor Graphics design entry and logic verification tools. PLS-WS/HP also includes the MAX+PLUS II TTL MacroFunction Library (with over 300 basic gate and TTL macrofunctions).

PLS-WS/SN: Provides a SPARCstation-compatible version of the MAX+PLUS II Compiler (with design partitioning), and a bidirectional EDIF 2 0 0 netlist interface for transferring designs between the Compiler and Valid Logic, Viewlogic, Synopsys, or other design entry and logic verification tools. PLS-WS/SN also includes the MAX+PLUS II TTL MacroFunction Library (with over 300 basic gate and TTL macrofunctions).

MAX+PLUS

MAX+PLUS software is a fully integrated system for designing logic with MAX 5000 EPLDs. It features hierarchical graphic and text design entry with over 300 basic gate and TTL macrofunctions. It includes AHDL, which supports state machine, Boolean equation, and truth table entry. The MAX+PLUS Compiler provides logic minimization, automatic device selection, architecture optimization, and design fitting. MAX+PLUS software also supports error location, user-defined macros, full timing simulation, delay prediction for speed-critical paths, timing analysis, and a design archiver. MAX+PLUS is available in two configurations:

PLDS-MAX: Fully integrated programmable logic development system for working with MAX 5000 EPLDs. It includes MAX+PLUS design entry, processing, verification, and programming software; standard Altera programming hardware; an assortment of programming adapters; and several sample EPLDs.

PLS-MAX: Fully integrated programmable logic development software for working with MAX 5000 EPLDs. This software-only version of PLDS-MAX includes MAX+PLUS design entry, processing, verification, and programming software.

A+PLUS

A+PLUS software transforms input design files into standard JEDEC Files for programming Classic EPLDs. The Altera Design Processor (ADP) provides logic minimization, automatic EPLD selection, architecture optimization, and design fitting.

A+PLUS software supports LogiCaps schematic capture, state machine, Boolean equation, truth table, and netlist design entry. A+PLUS includes over 100 TTL macrofunctions, the Altera Design Librarian (ADLIB) for creating user-defined macrofunctions, and the Functional Simulator (FSIM). LogicMap II software uses standard Altera hardware and the JEDEC File created by A+PLUS design processing to program Altera Classic EPLDs.

A+PLUS is available in two configurations:

PLCAD-SUPREME: Complete A+PLUS development system. This package includes the Altera Design Processor, LogiCaps schematic capture, TTL macrofunctions, ADLIB, FSIM, and LogicMap II software; standard Altera programming hardware; several programming adapters; and selected sample EPLDs.

PLS-SUPREME: Complete A+PLUS development software. This software-only version of PLCAD-SUPREME includes the Altera Design Processor, LogiCaps schematic capture, TTL macrofunctions, ADLIB, FSIM, and LogicMap II software.

SAM+PLUS

SAM+PLUS software translates state machine or microcoded assembly language input design files into standard JEDEC Files for programming Stand-Alone Microsequencer (SAM) EPLDs. SAM+PLUS software includes the Altera State Machine Language (ASMILE) and Assembly Language (ASM). The SAM Design Processor (SDP) provides logic minimization, architecture optimization, and design fitting. SAM+PLUS also includes SAMSIM, an interactive functional simulator created specifically for verifying SAM designs. SAM+PLUS is available in two configurations:

PLDS-SAM: Programmable logic development system for working with SAM EPLDs. It includes SAM+PLUS and LogicMap II software, standard Altera programming hardware, one programming adapter, and sample EPLDs.

PLS-SAM: Programmable logic development software for working with SAM EPLDs. This software-only version of PLDS-SAM consists of SAM+PLUS software.

MCMap

MCMap software implements designs for Micro Channel EPLDs, which perform all interface functions required between an IBM PS/2 add-on card and the IBM PS/2 Micro Channel bus. It provides interactive, table-driven design entry; performs real-time error checking; and generates a JEDEC File for device programming. MCMap is available in the following configurations (for more information on MCMap software and Micro Channel EPLDs, see the ***Micro Channel Adapter Handbook***):

PLDS-MCMAP: Programmable logic development system for working with Micro Channel EPLDs. It includes MCMap and LogicMap II software, standard Altera programming hardware, one programming adapter, and sample EPLDs.

PLS-MCKIT: Programmable logic development software for working with Micro Channel EPLDs. This software-only version of PLDS-MCMAP consists of MCMap software.

Design Entry

Altera development systems and software provide a variety of design entry methods:

- ❑ Schematic Capture
- ❑ Altera Hardware Description Language (AHDL)
- ❑ Waveform
- ❑ State Machine
- ❑ Boolean Equation
- ❑ Altera Assembly Language (ASM)
- ❑ Table

Schematic Capture

Schematic capture offers a What-You-See-Is-What-You-Get approach to hierarchical logic design that is both intuitive and fast. The extensive primitive and macrofunction libraries provide basic building blocks for constructing a design. Designers can also create their own libraries of custom functions. With MAX+PLUS and MAX+PLUS II, the designer can automatically generate symbols for custom functions, which can be incorporated into other designs.

AHDL

The Altera Hardware Description Language (AHDL) is a high-level, modular language used to create hierarchical logic designs. AHDL supports state machines, truth tables, Boolean equations, arithmetic operators, group operations, and macrofunctions. With MAX+PLUS II, automatic design partitioning is available.

Waveform Entry

Waveform design entry enables the designer to specify logic by entering the desired input and output waveforms. Combinatorial logic, registered logic, and state machines can be synthesized automatically to generate the waveforms specified by the designer.

State Machine Entry

State machine design entry allows the designer to describe the logical operation of both Mealy and Moore state machine designs using a high-level language description featuring `IF-THEN` and `CASE` statements, truth tables, and Boolean equations.

Boolean Equation Entry

Boolean equation design entry allows the designer to describe the logic of a design with Boolean equations.

Altera Assembly Language Entry

Altera Assembly Language (ASM) provides microcoded control design entry for SAM EPLDs. This entry method provides access to the advanced features of the SAM EPLDs, including the on-chip stack and loop counter.

Table Entry

Table design entry provides interactive tabular design entry with real-time error checking and automatically generated utilization reports for Micro Channel EPLDs.

Design Compilation & Verification

Altera development systems and software provide several applications and features that check designs for errors, synthesize logic, fit designs into EPLDs, and test design logic. Major features of design compilation and verification are:

- ❑ Timing Simulation
- ❑ Functional Simulation
- ❑ Timing Analysis
- ❑ Waveform Editing
- ❑ Design Partitioning
- ❑ Multi-EPLD Simulation

Timing Simulation

A timing simulator tests the logical operation and internal timing of a logic design. It allows a designer to model a design before it is programmed into an EPLD. Altera timing simulators can be run in interactive mode with menu commands or in batch mode.

Functional Simulation

A functional simulator uses specified design information to model the logical operation of an EPLD before the design is actually committed to silicon. A functional simulator does not model the actual timing of a device. Altera functional simulators can be run in interactive mode with menu commands or in batch mode.

Timing Analysis

A timing analyzer analyzes the performance of a design. It enables a logic designer to trace all possible signal paths to determine the speed-critical and performance-limiting paths in the design.

Waveform Editing

A waveform editor creates a file that contains input vector waveforms that drive simulation, and the buried logic and output node names to be simulated. A waveform editor also allows the designer to view and interpret the outputs of simulation.

Design Partitioning

Design partitioning automatically divides very large designs into two or more devices from the same EPLD family. Designs can be partitioned into multiple devices automatically or according to the designer's specifications. The designer can guide partitioning by making resource and device assignments to optimize design placement on the EPLD.

Multi-EPLD Simulation

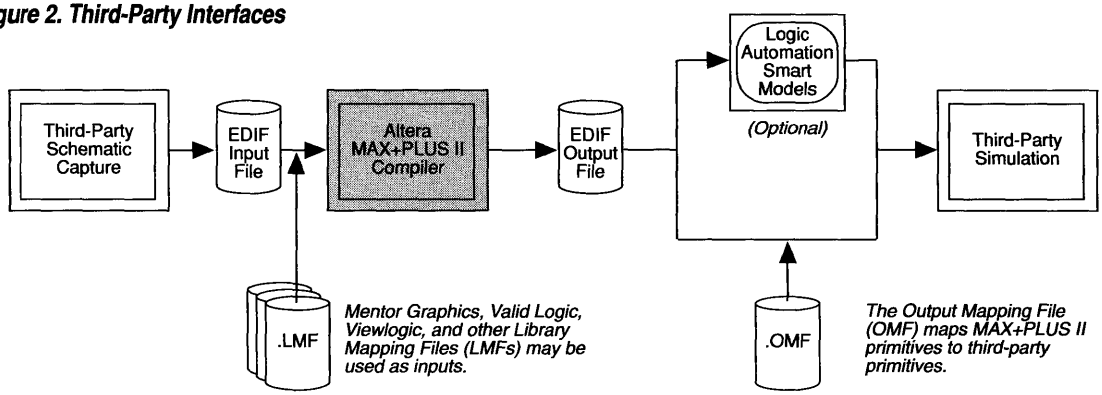
Multi-EPLD simulation allows logic designs that are partitioned into multiple devices to be simulated together.

EDIF Interface

To satisfy the needs of workstation-based designers, Altera provides an interface to third-party CAE tools from Mentor Graphics, Valid Logic, Viewlogic, Synopsys, and others. EDIF interface software enables the designer to import and export files that conform to the Electronic Design Interchange Format (EDIF) Version 2 0 0 standard. EDIF files can be imported into or exported from MAX+PLUS and MAX+PLUS II.

Designers can enter logic designs with third-party design entry tools and transfer their designs to MAX+PLUS or MAX+PLUS II for processing. Altera-provided Library Mapping Files (LMFs) facilitate this transfer. Once the logic has been synthesized and fitted into the selected Altera EPLD, it can be transferred to third-party design verification tools. EPLDs can therefore be simulated to perform system-level design verification (see Figure 2).

Figure 2. Third-Party Interfaces



The following Altera development packages provide third-party interfaces:

- PLDS-HPS
- PLS-HPS
- PLS-OS
- PLS-WS/HP
- PLS-WS/SN
- PLDS-ENCORE *(requires PLS-EDIF software)*
- PLDS-MAX *(requires PLS-EDIF software)*
- PLS-MAX *(requires PLS-EDIF software)*

Software Warranty

The renewable, one-year software warranty agreements for development products provide software and documentation updates for all registered owners of Altera development systems. The software warranty should be ordered with one of the following codes:

- PLAESW-HPS (for PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES)
- PLAESW-MAX (for PLDS-MAX & PLS-MAX)
- PLAESW-SUP (for PLCAD-SUPREME & PLS-SUPREME)
- PLAESW-WS (for PLS-WS/HP & PLS-WS/SN)

Programming Hardware & Adapters

Altera programming hardware can be purchased in the Altera Stand-Alone Programmer (PL-ASAP) package. Alternatively, the designer can purchase a Master Programming Unit (MPU), Logic Programmer card (LP6), and adapters that support each EPLD. These alternatives are described below.

PL-ASAP: Contains the hardware and software needed to set up an independent programming station capable of programming all Altera EPLDs. It includes programming software, an LP5 or LP6 Logic Programmer card, and the MPU. No design entry, processing, or simulation tools are included.

LP5 & LP6: Software-controlled Logic Programmer cards for use with all Altera programmable logic development systems. The LP5 card interfaces with IBM PS/2 Models 50, 60, 70, and 80 or compatible computers; the LP6 card interfaces with IBM-AT or compatible computers.

MPU: Serves as the base unit for programming all Altera EPLDs. It can directly program EP320 and EP330 DIP EPLDs; adapters are required to program all other EPLDs.

Adapters: Table 10 shows the adapters available for Altera EPLDs. Adapter names consist of the four-letter prefix shown on the left, plus the corresponding device number on the right. Individual adapters may be ordered separately.

Table 10. EPLD Adapter Support

EPLD	Package	Part Number *(1)*
EP330	J-Lead	PLEJ330
	SOIC	PLES330
EP600/610/610A/610T/630	DIP	PLED610
	J-lead	PLEJ610
	SOIC	PLES610
EP900/910/910A/910T	DIP	PLED910
	J-lead	PLEJ910
EP1800/1810/1810T/1830	J-lead	PLEJ1810
	J-lead	PLMJ1810 *(2)*
	PGA	PLEG1810
EPM5016	DIP	PLED5016
	J-lead	PLEJ5016
	SOIC	PLES5016
EPM5032	DIP	PLED5032
	DIP	PLMD5032 *(2)*
	J-lead	PLEJ5032
	SOIC	PLES5032
EPM5064	J-lead	PLEJ5064
EPM5128	J-lead	PLEJ5128
	J-lead	PLMJ5128 *(2)*
	PGA	PLEG5128
EPM5130	J-lead	PLEJ5130
	J-lead	PLMJ5130 *(2)*
	PGA	PLEG5130
	QFP	PLEQ5130
EPM5192	J-lead	PLEJ5192
	J-lead	PLMJ5192 *(2)*
	PGA	PLEG5192
EPS448	DIP	PLED448
	J-lead	PLEJ448
EPS464	J-lead	PLEJ464
	J-lead	PLMJ464 *(2)*
	QFP	PLEQ464
EPB2001	J-lead	PLEJ2001

Notes to Table 10:

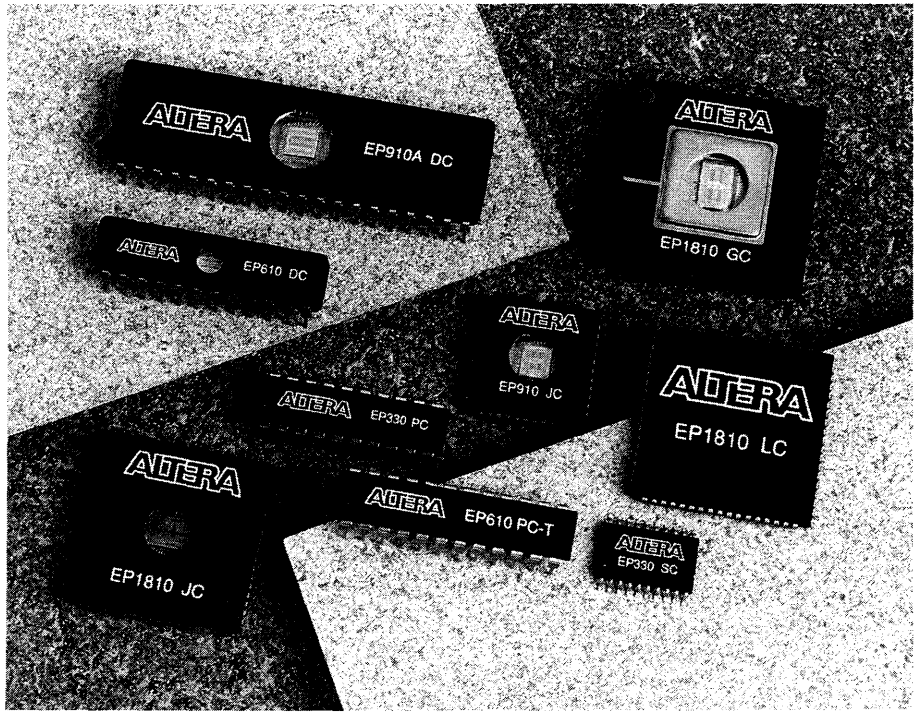
(1) See the *PLED/J/S/Q & PLMD/J/S/Q Data Sheet* in this data book for more information.

(2) Supports functional testing and continuity checking.

Contents

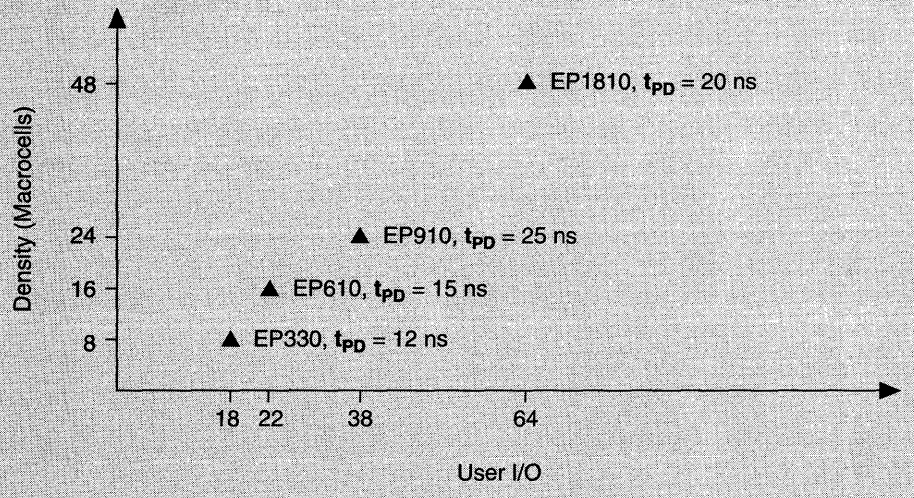
September 1991

Section 2 Classic EPLDs


ALTERA
EP910A DC
ALTERA
EP610 DC
ALTERA
EP1810 GC
ALTERA
EP910 JC
ALTERA
EP330 PC
ALTERA
EP1810 LC
ALTERA
EP610 PC-T
ALTERA
EP330 SC
ALTERA
EP1810 JC

Classic EPLDs

A High-Speed, Low-Power Integration Solution



- Altera Classic EPLDs offer the industry's most comprehensive solution to high-speed, low-power logic integration.
- Classic architecture combines the familiarity of PALs with superior macrocell and I/O flexibility.
- Classic EPLDs allow designers to use the same architecture to solve a broad range of integration problems.
- In non-turbo (or standby) mode, Classic EPLDs consume very low power.
- Non-volatile EPROM technology aids prototype development.
- Classic EPLDs easily integrate multiple standard 20-pin PAL and GAL devices.
- High pin-to-macrocell ratio is ideal for pin-intensive designs.
- A full selection of packages is available, including DIP, J-lead, PGA, and SOIC footprints in windowed ceramic and one-time-programmable (OTP) plastic packages.
- Classic EPLDs provide t_{PD} as low as 12 ns and internal counter rates as high as 100 MHz.
- EP1810 EPLD designs can be easily converted to custom masked silicon for very-high-volume production.
- Classic EPLDs are supported with MAX+PLUS II and A+PLUS PC- and workstation-based design tools that allow design entry, compilation, simulation, and programming.
- Multiple design entry options are available, including schematic capture, waveform, truth table, state machine, Boolean equation, and netlist entry.
- Logic compilation and fitting is performed in minutes.
- Extensive third-party support is available for design entry, compilation, and programming.

EP330 EPLD

High-Performance 8-Macrocell Device

September 1991, ver. 2

Data Sheet

Features

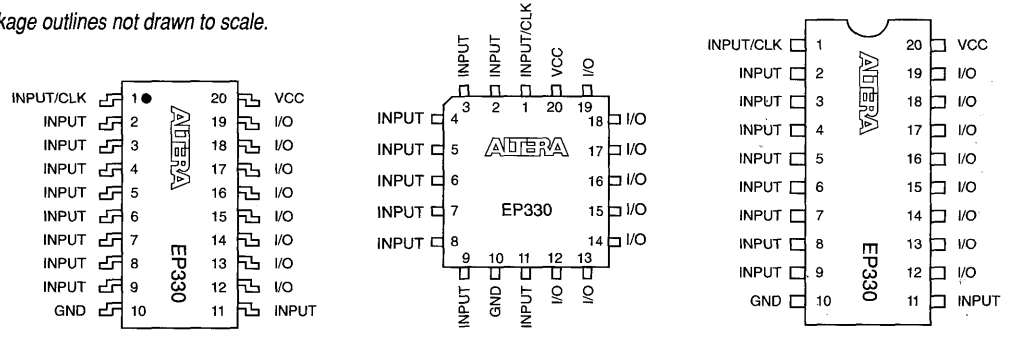
- High-performance 8-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Low power; I_{CC} = 45 mA (typical)
- Available in one-time-programmable (OTP) plastic chip carrier packages
  - 20-pin dual in-line package (PDIP)
  - 20-pin J-lead chip carrier (PLCC)
  - 20-pin, 300-mil small-outline IC (SOIC)
- Macrocell flip-flops can be individually programmed for registered or combinatorial operation
- Direct replacement for GAL 16V8 and most 20-pin PAL devices
- "Quiet" outputs minimize output switching noise found in other high-speed CMOS devices
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP330 Erasable Programmable Logic Device (EPLD) provides a high-speed, low-power, pin-compatible replacement for 20-pin programmable logic devices such as PALs and GALs. The EP330 EPLD is available in 20-pin OTP plastic DIP, J-lead, and SOIC packages. See Figure 1.

Figure 1. EP330 Package Pin-Out Diagrams

Package outlines not drawn to scale.



The EP330 EPLD can accommodate up to 18 inputs and 8 outputs. Each of the 8 macrocells contains a programmable-AND/fixed-OR structure that implements logic with up to 8 product terms. An additional product term in each macrocell controls Output Enable.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in active-high and active-low modes. Thus, EP330 devices may be configured as drop-in replacements for PAL and GAL devices such as the 16R8 and 16V8. See *Application Note 2* for more information.

The EP330 CMOS EPROM technology reduces active power consumption to less than 50% of the power required by equivalent bipolar devices, without sacrificing speed. This reduced power consumption makes these EPLDs highly desirable for a wide range of applications. Additionally, EP330 EPLDs are 100% generically testable.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform design entry, and an EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD. MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

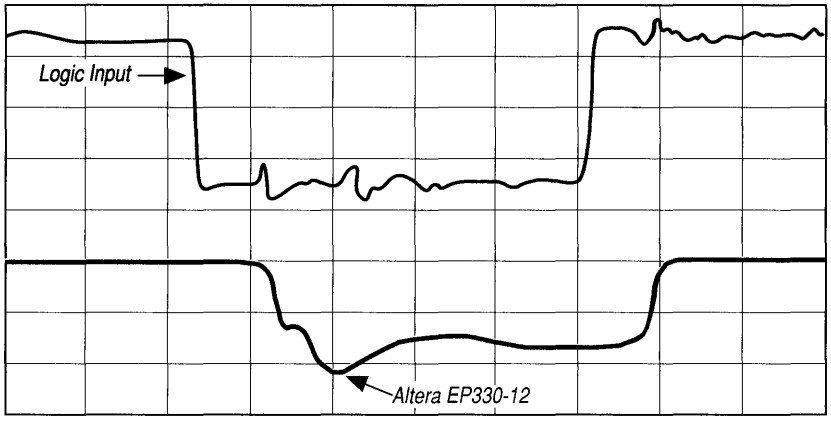
EP330 EPLD Output Characteristics

The EP330 combines high performance with low noise. For example, Figure 2 shows the switching performance of the EP330-12, Altera's 12-ns version of the EP330 EPLD. The EPLD's "quiet" outputs allow designs to run fast with high system reliability. In addition, enhanced output current capability (I_{OL} = 24 mA) allows the EP330 to directly integrate designs requiring high-current drive, such as bus interfaces. The EP330 EPLD is available with t_{PD} values of 12 ns and 15 ns.

Functional Description

The EP330 EPLD uses CMOS EPROM technology to configure connections in a programmable-AND logic array. EPROM connections are also used to control the output/feedback options, such as registered or combinatorial feedback, in active-high or active-low modes.

Figure 2. EP330-12 Output Switching Performance

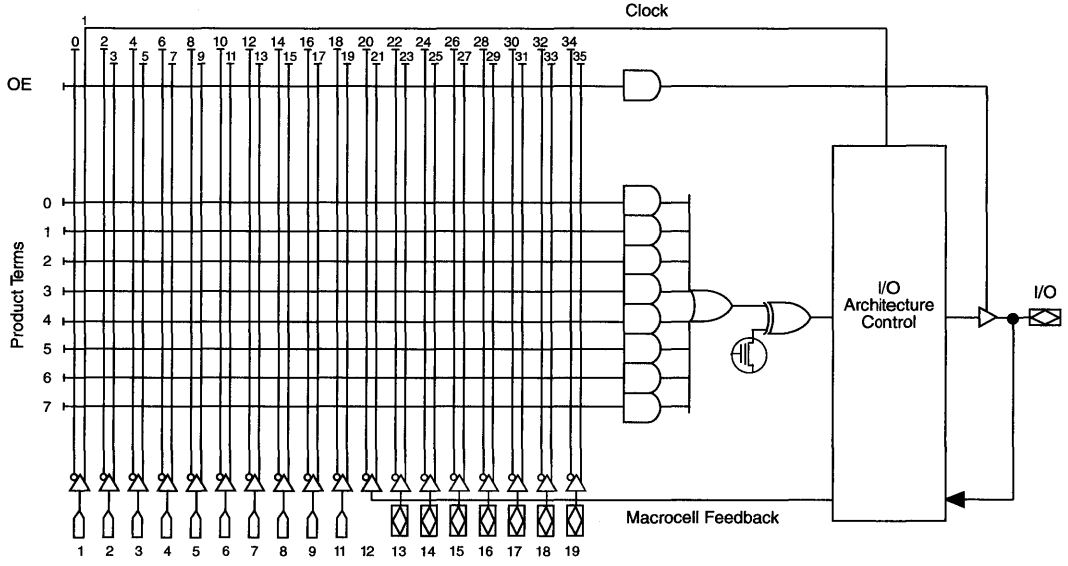


Timebase = 10.0 ns/division

Channel 1 = 1.000 V/division
Channel 2 = 2.000 V/division

An EP330 EPLD has ten dedicated data inputs and eight I/O pins that can be configured for input, output, or bidirectional operation. Figure 3 shows the EP330 macrocell.

Figure 3. EP330 Macrocell



The EP330 block diagram is shown in Figure 4. The internal architecture of this device has a sum-of-products (AND/OR) structure. Inputs to the programmable-AND array come from the true and complement signals of the 10 dedicated input pins, and the true and complement forms of the 8 feedback signals from the I/O architecture control blocks. The 36-input AND array has 72 product terms distributed equally among the 8 macrocells. Each product term represents a 36-input AND gate.

The outputs of eight product terms are ORed together; then the output of the OR gate is fed as an input to an XOR gate. The XOR function allows the designer to use the invert-select EPROM cell to specify the polarity of the output signal. If the EPROM cell is programmed, the true form of the signal (active high) is passed; if not, the complement of the signal (active low) is passed. The XOR output then feeds the I/O architecture control block, in which the output is configured for registered or combinatorial operation. In registered mode, the output is registered via a positive-edge-triggered D-type flip-flop. The feedback signal comes from the output of the flip-flop. In combinatorial mode, the output is not registered, and the feedback signal comes directly from the I/O pin.

Output Enable Product Term

The Output Enable (OE) product term determines whether an output signal will propagate to the output pin. If the output of the OE product term is high, output to the pin is enabled. If the output is low, the output buffer becomes a high-impedance node and does not allow the output signal to reach the output pin. The I/O pin can then be used as a dedicated input. This OE product term allows true bidirectional operation in combinatorial mode.

The EP330 device contains eight OE product terms, one for each I/O pin. All outputs can be enabled or disabled simultaneously by using an identically programmed product term at each of the outputs. Outputs can be enabled under other conditions by defining a different OE product term for each output.

I/O Architecture

Figure 5 shows the output configurations available for the eight I/O pins. Either registered or combinatorial outputs can be individually specified for each macrocell. Any I/O pin can be configured as a dedicated input by choosing no output and pin feedback.

In combinatorial mode, active-high or active-low output polarity with pin feedback or no feedback can be chosen. In registered mode, active-high or active-low output polarity with the internal registered feedback or no feedback are available. In the erased state, the I/O architecture is configured for combinatorial active-low output with pin feedback.

Figure 4. EP330 Block Diagram

Numbers in parentheses are for J-lead packages.

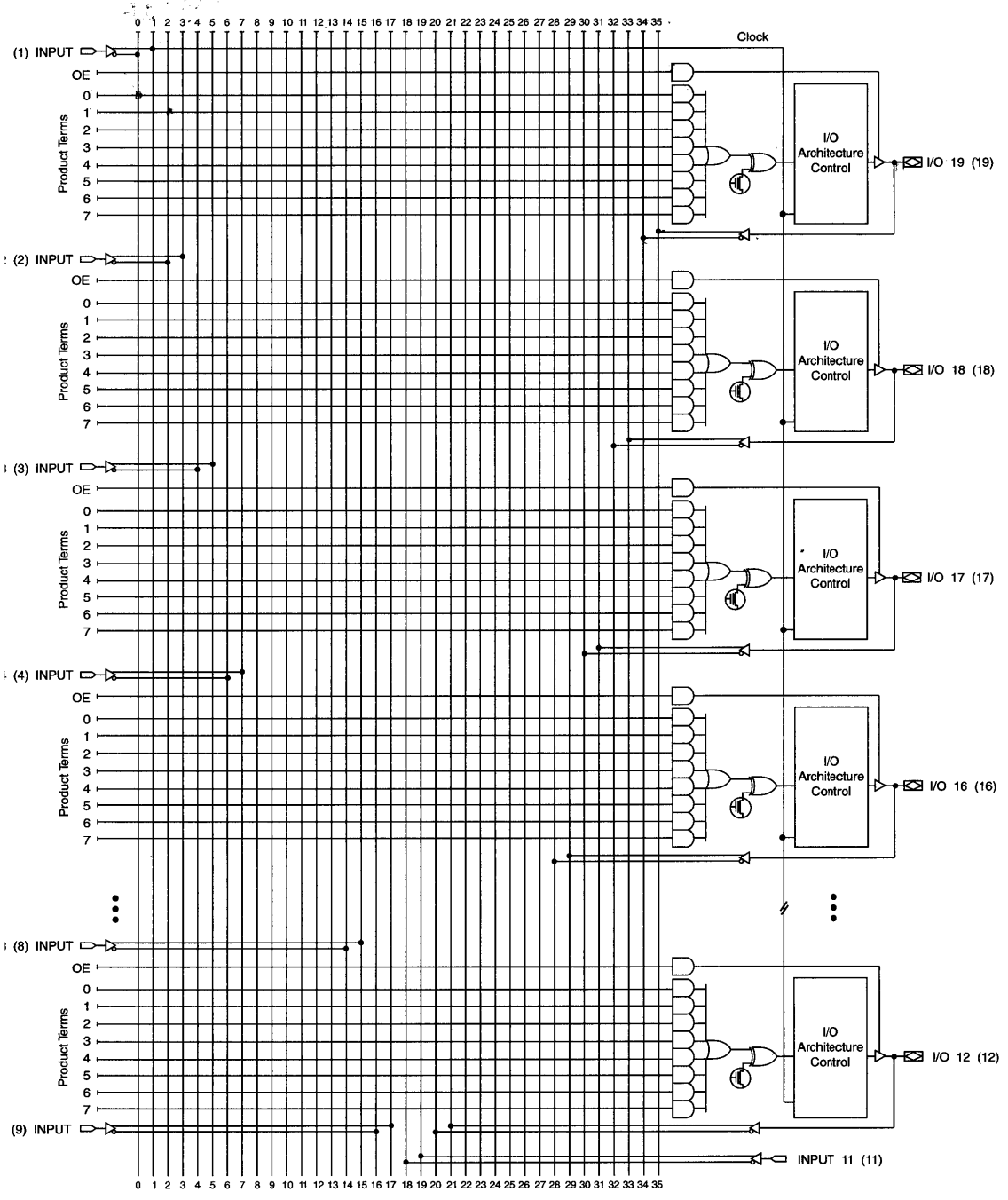
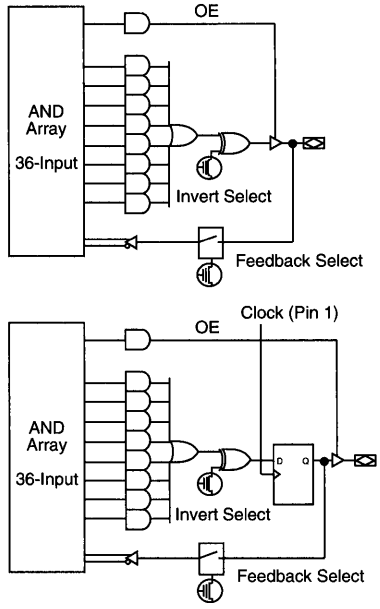


Figure 5. EP330 I/O Configurations



Combinatorial I/O Selection

Output/Polarity	Feedback
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

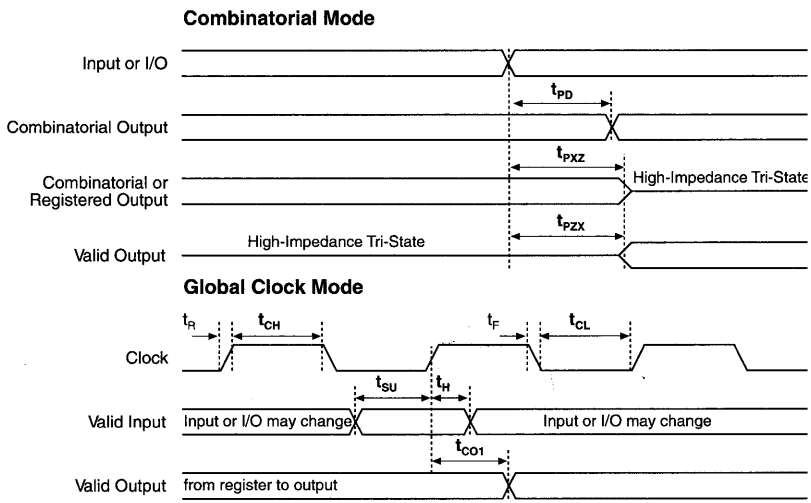
Registered I/O Selection

Output/Polarity	Feedback
D Register/High	D Register, None
D Register/Low	D Register, None
None	D Register

The switching waveforms for the EP330 EPLD are shown in Figure 6.

Figure 6. EP330 Switching Waveforms

t_R and t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Functional Testing

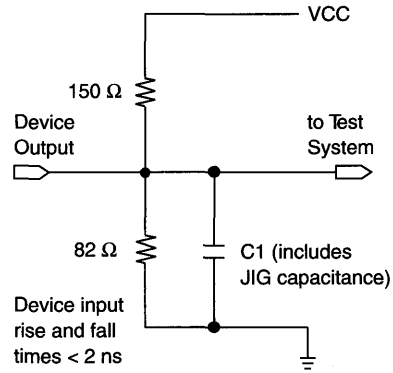
The EP330 EPLD is fully functionally tested and guaranteed through complete testing of each EPROM bit and all internal logic elements. This testing ensures a 100% programming yield.

The testing process eliminates traditional problems associated with fuse-programmed circuits. An EP330 EPLD allows test programming patterns to be used and then erased. The ability to use application-independent, general-purpose tests is called generic testing and is unique to EPLDs.

AC test measurements are performed under the conditions shown in Figure 7.

Figure 7. EP330 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Design Security

An EP330 EPLD contains a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security by making programmed data within EPROM cells invisible. The Security Bit, along with all other program data, is reset by erasing the device.

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–160	160	mA
I_{OUT}	DC output current, per pin		–50	50	mA
P_D	Power dissipation			800	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*See Note (2)*		20	ns
t_F	Input fall time	*See Note (2)*		20	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		40	75	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		45	75	mA

Capacitance

See Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF

AC Operating Conditions *See Note (4)*

			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15	ns
t_{PD2}	I/O input to non-registered output			13		16	ns
t_{PZX}	Input to output enable			12		15	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		12		15	ns
t_{IO}	I/O input pad and buffer delay			1		1	ns

Global Clock Mode			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	125		100		MHz
t_{SU}	Setup time		6		8		ns
t_H	Hold time		0		0		ns
t_{CH}	Clock high time		4		5		ns
t_{CL}	Clock low time		4		5		ns
t_{CO1}	Clock to output delay			8		10	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	100		83.3		MHz

Notes to tables:

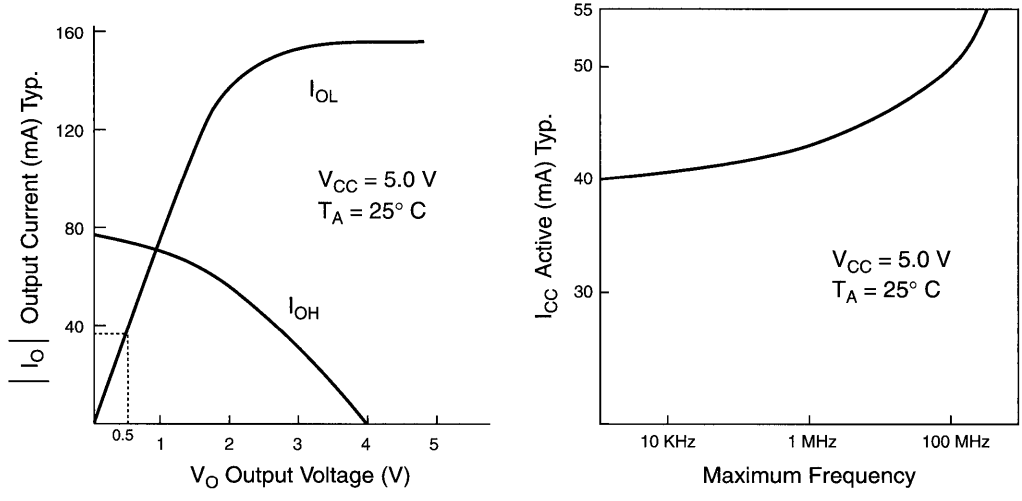
1) Minimum DC input is –0.3 V. During transitions, inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
2) For all clocks: t_R and t_F = 20 ns.
3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
   V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
5) Measured with a device programmed as an 8-bit counter.
6) Capacitance measured at 25° C. Sample-tested only. Pin 11 (high-voltage pin during programming) has maximum capacitance of 20 pF.
7) Sample-tested only for an output change of 500 mV.
8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP330-12, EP330-15
Industrial	(–40° C to 85° C)	EP330-15
Military	(–55° C to 125° C)	Consult factory

Figure 8 shows output drive characteristics for EP330 I/O pins and typical supply current versus frequency for the EP330 EPLD.

Figure 8. EP330 Output Drive Characteristics and I_{CC} vs. Frequency



EP610 EPLDs

High-Performance 16-Macrocell Devices

September 1991, ver. 2

Data Sheet

Features

- High-density replacement for TTL and 74HC with up to 600 gates
- High-performance 16-macrocell EPLD with t_{PD} = 15 ns and counter frequencies up to 83 MHz
- Zero-power operation (20 µA standby)
- Advanced CMOS EPROM technology to allow device erasure and reprogramming
- Individual clocking of all registers, or banked register operation from two global Clock inputs
- 16 macrocells with configurable I/O architecture, allowing up to 20 inputs and 16 outputs
- Programmable registers providing D, T, SR, or JK flip-flops with individual asynchronous Clear control
- 100% generically testable to provide 100% programming yield
- Programmable Security Bit for total protection of proprietary designs
- Available in 24-pin, 300-mil SOIC; 24-pin, 300-mil DIP; or 28-pin J-lead chip carriers
- Extensive third-party software and programming support

General Description

Altera's EP610 Erasable Programmable Logic Devices (EPLDs) can implement up to 600 equivalent gates of SSI and MSI logic functions in space-saving windowed ceramic or one-time-programmable (OTP) plastic 24-pin, 300-mil dual in-line package (CerDIP and PDIP) and 28-pin J-lead (JLCC and PLCC) packages, or OTP plastic 24-pin, 300-mil small-outline integrated circuit (SOIC) packages.

The EP610 EPLDs use sum-of-products logic that provides a programmable-AND/fixed-OR structure. These EPLDs accommodate combinatorial and sequential logic functions with up to 20 inputs and 16 outputs. The EP610 EPLDs also offer 60% more logic and 6 more flip-flops than a CMOS 22V10 device.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in active-high and active-low modes.

EP610 EPLDs can individually program D, T, SR, or JK flip-flop operation for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths in the AND array. These features make it possible to simultaneously implement a variety of logic functions.

The CMOS EPROM technology in the EP610 EPLDs can reduce active power consumption to less than 40% of the power required by equivalent bipolar devices, without losing speed. This reduced power consumption makes the EP610 EPLDs highly desirable for a wide range of applications. Moreover, these devices are 100% generically testable and can be erased with UV light. Designs and design modifications can be implemented quickly, eliminating the need for post-programming testing.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform entry, and EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD. MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

EP610 EPLDs

The EP610 EPLD is pin-, function-, and JEDEC-File-compatible with the EP610A, EP610T, and EP630 EPLDs. JEDEC Files generated for an EP610 EPLD can be used for programming these devices.

EP610

The EP610 EPLD combines high speed with low power. It can implement a 16-bit counter at up to 83.3 MHz, and typically consumes 5 mA when operating at 1 MHz. The EP610 EPLD is available with maximum t_{PD} values of 15, 20, 25, 30, and 35 ns. Both MIL-STD-883B-compliant and DESC-approved parts are available.

EP610A

The EP610A EPLD is a high-speed version of the EP610 device. It has a maximum t_{PD} of 10 ns, which is ideal for high-speed address decoding. The EP610A EPLD offers a 36% faster clock-to-output delay (t_{CO} = 6 ns) than a CMOS 22V10 and can easily integrate logic operating at today's faster system speeds. The EP610A EPLD is fabricated on an advanced 0.8-micron process, and supports 16-bit counter frequencies of up to 100 MHz.

EP610T

The EP610T EPLD is a lower-cost version of the EP610 device. This device operates in Turbo mode only. The Turbo Bit in the EPLD is preset at the factory. The EP610T EPLD is available with maximum t_{PD} values of 15 ns, 20 ns, and 25 ns.

EP630

The EP630 EPLD combines speed with a low-power standby mode. This device can implement a 16-bit counter at up to 83 MHz, and typically consumes 5 mA when operating at 1 MHz. It is available with maximum t_{PD} values of 15 ns and 20 ns.

Functional Description

The EP610 EPLDs use CMOS EPROM technology to configure connections in a programmable-AND logic array. EPROM connections are also used to construct a highly flexible programmable I/O architecture that provides advanced functions for user-programmable logic.

EP610 EPLDs have 4 dedicated data inputs, 2 global clock inputs, and 16 I/O pins that can be configured for input, output, or bidirectional operation on a macrocell-by-macrocell basis.

Each EP610 macrocell (see Figure 1) contains 10 product terms for the following functions: 8 product terms are dedicated to logic implementation; 1 product term is used for Clear control of the internal register; and 1 product term implements either Output Enable or an array Clock.

Figure 1. EP610 Macrocell

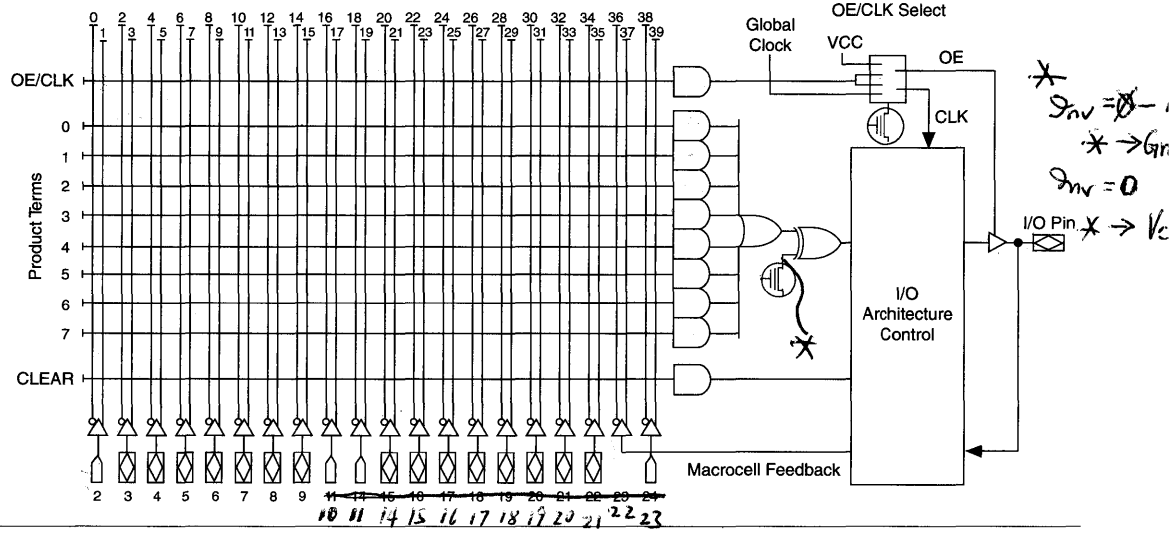
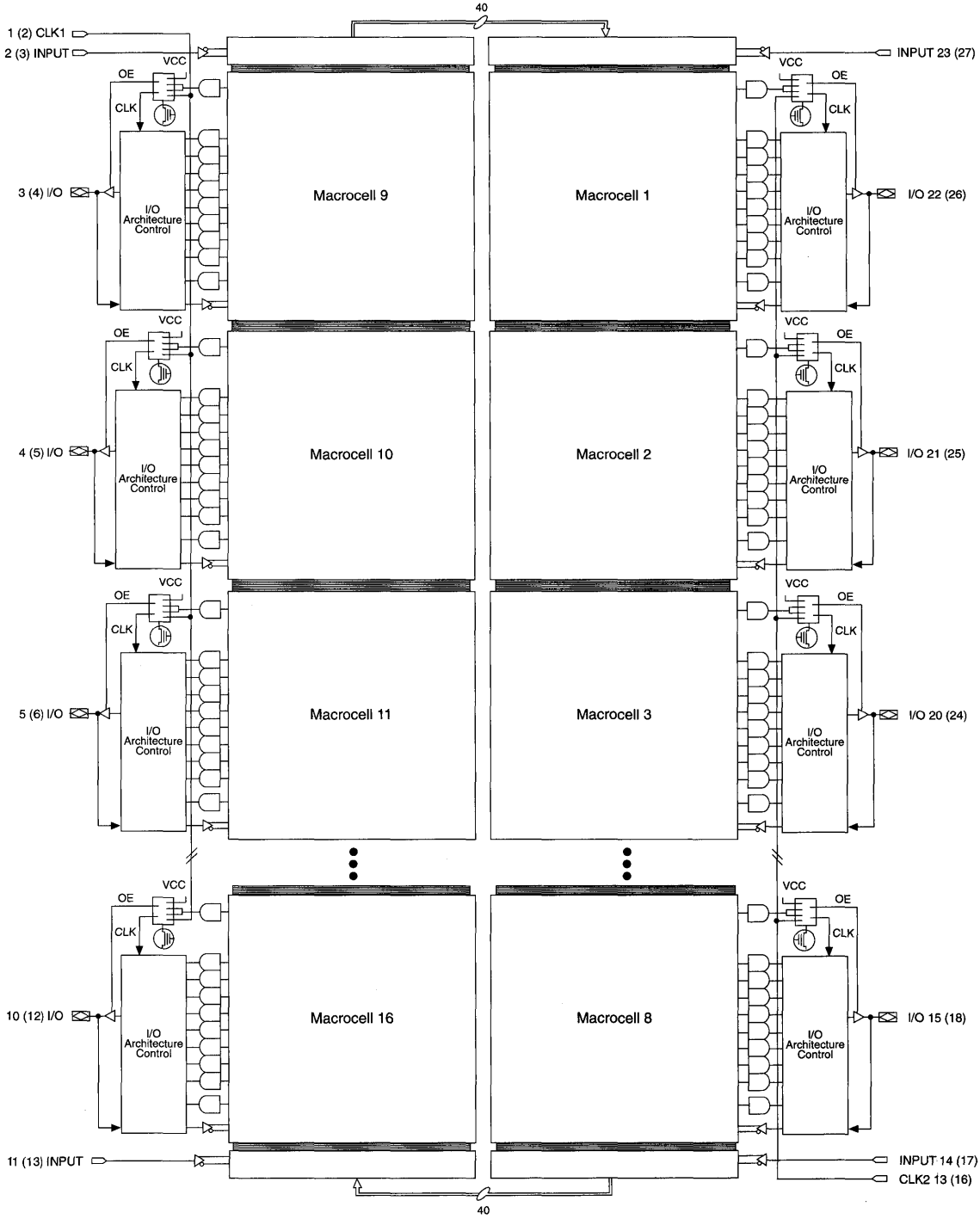


Figure 2 shows the complete block diagram of an EP610 EPLD. The internal device architecture has a sum-of-products (AND/OR) structure. Inputs to the programmable-AND array come from the true and complement signals of the 4 dedicated data inputs and 16 I/O feedback signals. The 40-input AND array has 160 product terms distributed among the 16 macrocells. Each product term represents a 40-input AND gate.

Figure 2. EP610 Block Diagram *Numbers in parentheses are for J-lead packages.*



In the erased state, the true and complement of the AND-array inputs are connected to the product terms. An EPROM control cell is located at each intersection of an AND-array input and a product term. During programming, selected connections are opened, allowing any product term to be connected to a true or complement array input signal with the following results:

- If both the true and complement of an array input signal are connected, the output of the AND gate is a logic low.
- If both the true and complement of any array input signal are programmed "open," a logic "don't care" results for that input.
- If all inputs for a given product term are programmed "open," the output of the corresponding AND gate is a logic high.

Two dedicated Clock inputs (which are not available in the AND array) provide the signals used for global clocking of EP610 internal registers. Each signal is positive-edge-triggered and has control over 8 registers: CLK1 controls macrocells 9 to 16; CLK2 controls macrocells 1 to 8. The programmable I/O architecture allows each of the 16 internal registers to have a global or array (product-term) Clock.

I/O Architecture

The EP610 architecture provides each macrocell with over 50 programmable I/O configurations. Each macrocell can be configured for combinatorial or registered output, with programmable output polarity. One of four register types (D, T, JK, and SR) can be implemented in each macrocell without additional logic. I/O feedback selection can be programmed for registered or input feedback. The I/O architecture can also individually clock each internal register from any internal signal.

OE/CLK Selection

Figure 3 shows the two modes of operation provided by the OE/CLK Select multiplexer. This multiplexer, which is controlled by a single EPROM bit, can be individually configured at each I/O pin.

In Mode 0, the tri-state output buffer is controlled by a single product term. If the output of the AND gate is high, then the output buffer is enabled. If the output is low, the output buffer has a high-impedance value. In this mode, the macrocell flip-flop is clocked by its global Clock input signal (CLK1 or CLK2). In the erased state, the OE/CLK Select multiplexer is configured to Mode 0.

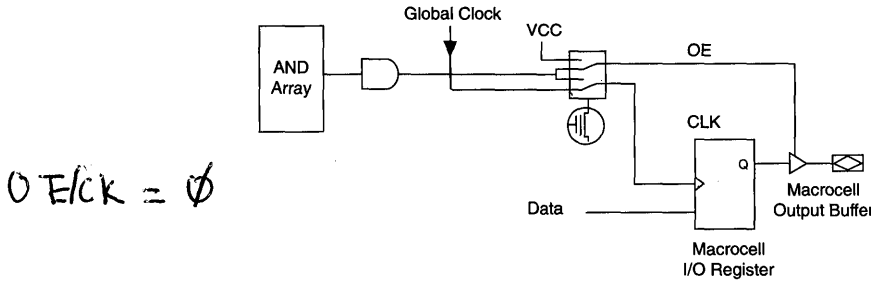
In Mode 1, the Output Enable buffer is always enabled, allowing the macrocell flip-flop to be triggered from an array Clock signal generated by the OE/CLK product term. This mode allows flip-flops to be individually clocked from any of the AND-array input signals. With true and complement signals in the AND array, the flip-flop can be configured to trigger on a rising or falling edge. This product-term-controlled clock configuration also allows implementation of gated clock structures.

Figure 3. OE/CLK Select Multiplexer

Mode 0:

The register is clocked by the global Clock signal, which can be connected to seven other macrocells. The output is enabled by the logic from the product term.

OE = Array (Product Term)
CLK = Global

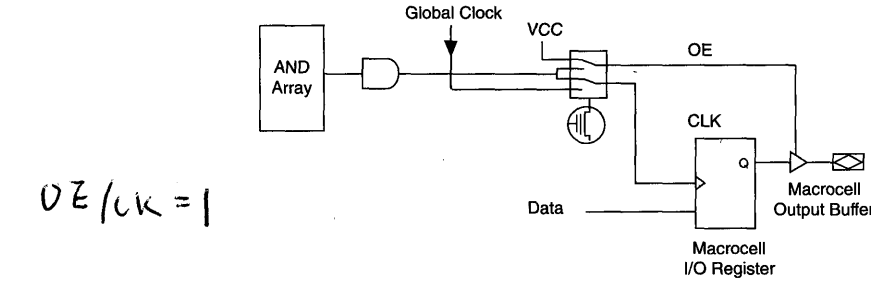


OE/CK = Ø

Mode 1:

The output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated in EP610 EPLDs.

OE = Enabled
CLK = Array

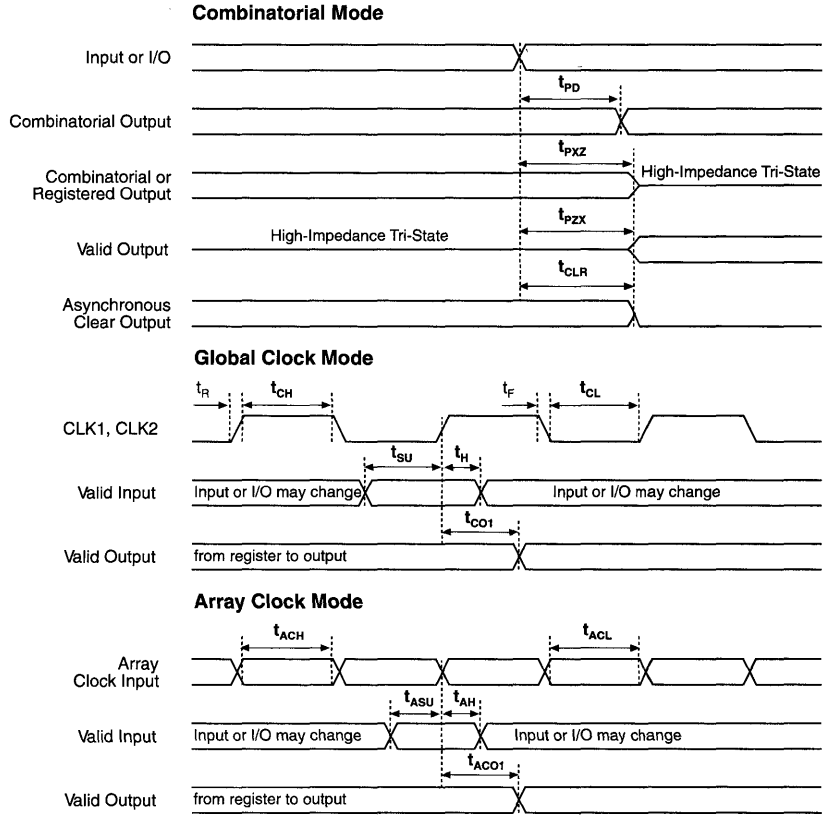


OE/CK = 1

Figure 4 shows waveforms for the following modes: combinatorial, global Clock, and array Clock.

Figure 4. EP610 Switching Waveforms

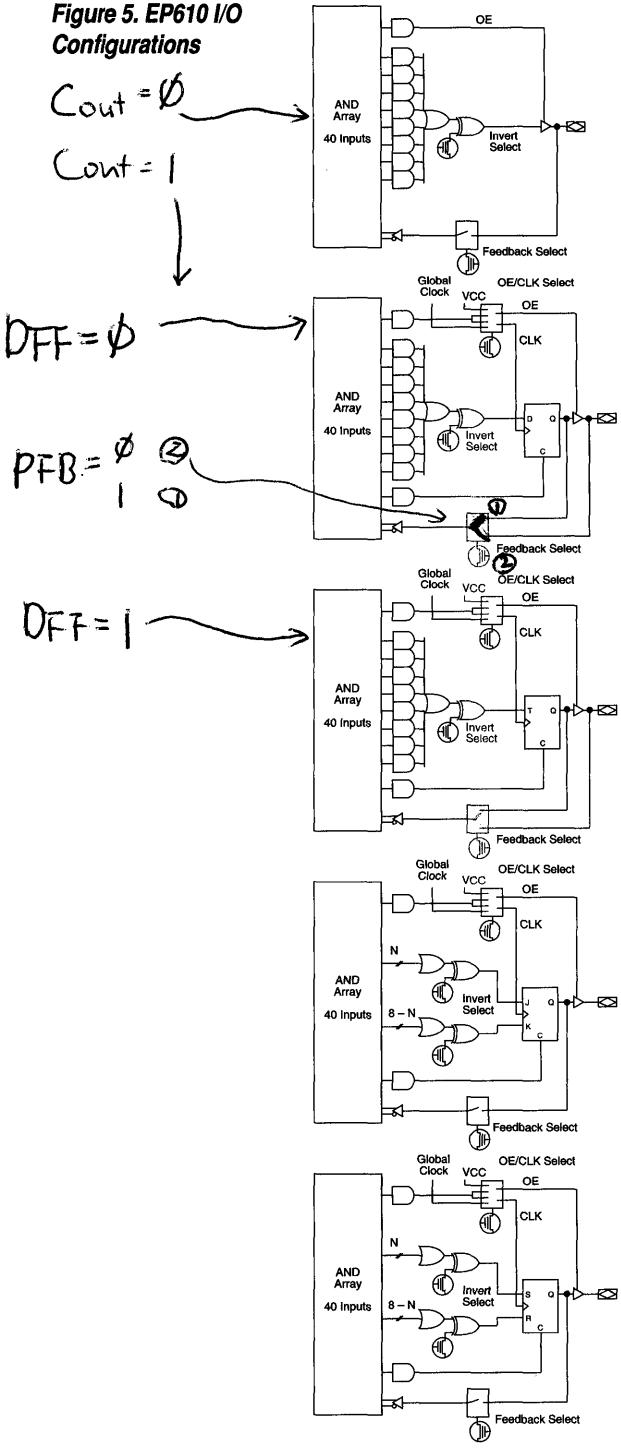
t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Output/ Feedback Selection

Output configurations available with the EP610 EPLDs are shown in Figure 5. Each macrocell can be individually configured with combinatorial output or with any of the four register outputs. All registers have an individual asynchronous Clear function controlled by a dedicated product term. When this product term is a logic high, the macrocell register is immediately loaded with a logic low. The Clear function is performed automatically during power-up.

Figure 5. EP610 I/O Configurations



Combinatorial

I/O Selection

Output/Polarity	Feedback
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

D Flip-Flop

I/O Selection

Output/Polarity	Feedback
D Register/High	D Register, Pin, None
D Register/Low	D Register, Pin, None
None	D Register
None	Pin

Function Table

D	Q_n	Q_{n+1}
L	L	L
L	H	L
H	L	H
H	H	H

T Flip-Flop

I/O Selection

Output/Polarity	Feedback
T Register/High	T Register, Pin, None
T Register/Low	T Register, Pin, None
None	T-Register
None	Pin

Function Table

T	Q_n	Q_{n+1}
L	L	L
L	H	H
H	L	H
H	H	L

JK Flip-Flop

I/O Selection

Output/Polarity	Feedback
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

Function Table

J	K	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

SR Flip-Flop

I/O Selection

Output/Polarity	Feedback
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

Function Table

S	R	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H

The combinatorial configuration has eight product terms ORed together to generate the output signal. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls the Output Enable buffer.
- The Feedback-Select multiplexer allows the user to choose I/O (pin) feedback or no feedback to the AND array.

The D or T register has eight product terms ORed together that are available to the register input. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls asynchronous Clear.
- The OE/CLK Select multiplexer configures the mode of operation to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback, I/O feedback, or no feedback to the AND array.

If the JK or SR register is selected, eight product terms are shared between two OR gates. The outputs of the OR gates feed the two primary register inputs. This configuration has the following characteristics:

- The MAX+PLUS II and A+PLUS development systems optimize the allocation of product terms for each register input.
- One product term controls asynchronous Clear.
- The Invert Select EPROM bits control output polarity.
- The OE/CLK Select multiplexer configures the mode of operation to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback or no feedback to the AND array.

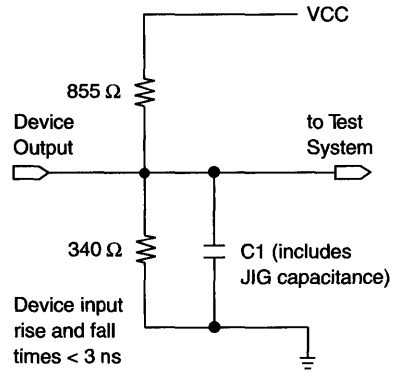
Any I/O pin can be configured as a dedicated input by selecting no output with I/O feedback. In the erased state, the I/O architecture is configured for combinatorial active-low output with I/O feedback.

Functional Testing

EP610 EPLDs are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements. A 100% programming yield is ensured. This testing process eliminates problems associated with fuse-programmed circuits by allowing test programming patterns to be used and then erased. The ability to use application-independent, general-purpose tests, called generic testing, is unique to EPLDs. AC test measurements are performed under the conditions shown in Figure 6.

Figure 6. EP610 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Design Security

The EP610 EPLDs contain a programmable design Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the EPLD cannot be copied or retrieved. This feature provides a high level of design security by making programmed data within EPROM cells invisible. The Security Bit, as well as all other program data, is reset by erasing the EPLD.

Turbo Bit

EP610 EPLDs contain a programmable Turbo Bit, set with the design software, to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit is programmed (Turbo = On), the low-standby-power mode (I_{CC1}) is disabled, making the circuit less sensitive to V_{CC} noise transients created by the low-power mode power-up/power-down cycle. All AC values are tested with the Turbo Bit programmed.

If the design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). In this mode, some AC parameters may increase. To determine worst-case timing, values from the AC Non-Turbo Adder specifications must be added to the corresponding AC parameter.

Features

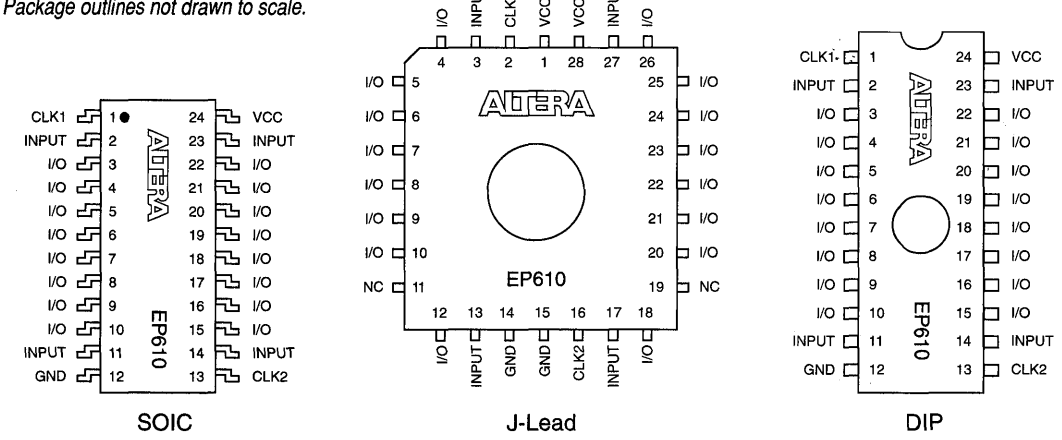
- Highest-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610A, EP610T, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages:
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 28-pin J-lead chip carrier (JLCC and PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP610 Erasable Programmable Logic Device (EPLD) can implement up to 600 equivalent gates of SSI and MSI logic functions. It is available in space-saving windowed ceramic or OTP plastic 24-pin, 300-mil DIP and 28-pin J-lead packages, or OTP plastic 24-pin, 300-mil SOIC packages. See Figure 7.

Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*See Note (3)*		100 (50)	ns
t_F	Input fall time	*See Note (3)*		100 (50)	ns

DC Operating Conditions

See Notes (2), (4), (5)

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (6)*	-15, -20, -25, -30, -35		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*	-15, -20		5	10	mA
			-25, -30, -35		5	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*	-15, -20		45	90	mA
			-25, -30, -35		45	60 (75)	mA

Capacitance *See Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions: EP610-15 and EP610-20 *See Note (5)*

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*See Note (7)*	83.3		62.5		0	MHz

Array Clock Mode

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	71.4		55.5		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (7)*	71.4		55.5		0	MHz

AC Operating Conditions: EP610-25, EP610-30, and EP610-35 *See Note (5)*

			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (10)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns

Global Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*See Note (11)*	47.6		41.7		37.0		0	MHz
t_{SU}	Input setup time		21		24		27		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		10		11		12		0	ns
t_{CL}	Clock low time		10		11		12		0	ns
t_{CO1}	Clock to output delay			15		17		20	0	ns
t_{CNT}	Minimum clock period			25		30		35	0	ns
f_{CNT}	Internal maximum frequency	*See Note (7)*	40.0		33.3		28.6		0	MHz

Array Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*See Note (11)*	47.6		41.7		37.0		0	MHz
t_{ASU}	Input setup time		8		8		8		30	ns
t_{AH}	Input hold time		12		12		12		0	ns
t_{ACH}	Clock high time		10		11		12		0	ns
t_{ACL}	Clock low time		10		11		12		0	ns
t_{ACO1}	Clock to output delay			27		32		37	30	ns
t_{ACNT}	Minimum clock period			25		30		35	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (7)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15 and EP610-20 EPLDs: maximum V_{PP} is 14.0 V.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns. For EP610-15 and EP610-20 clocks: t_R and t_F = 20 ns.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as a 16-bit counter.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35 EPLDs: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

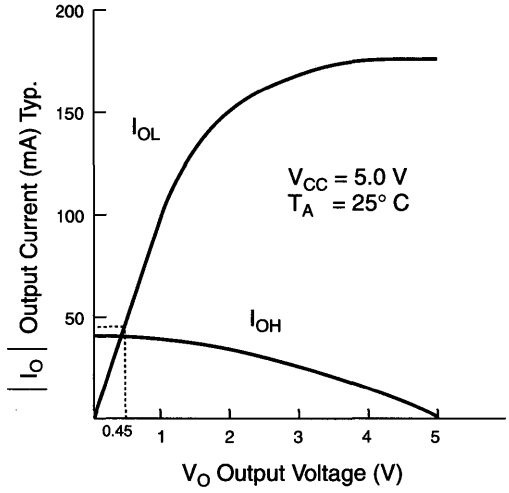
Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP610-15, EP610-20, EP610-25, EP610-30, EP610-35
Industrial	(–40° C to 85° C)	EP610-20, EP610-30, EP610-35
Military	(–55° C to 125° C)	EP610-35

Note: Only military-temperature-range devices are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

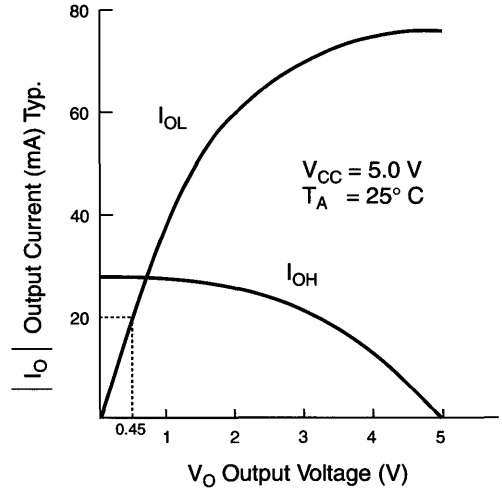
Figure 8 shows the output drive characteristics for EP610 I/O pins and typical supply current versus frequency for the EP610 EPLDs.

Figure 8. EP610 Output Drive Characteristics and I_{CC} vs. Frequency

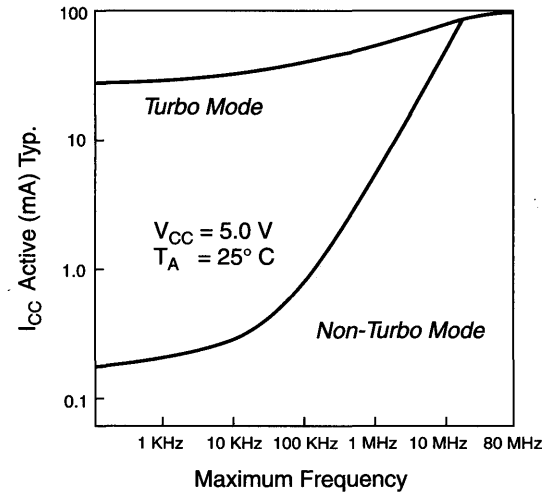
EP610-15 and EP610-20 EPLDs



EP610-25, EP610-30, and EP610-35 EPLDs



All EP610 EPLDs



Features

Advance Information

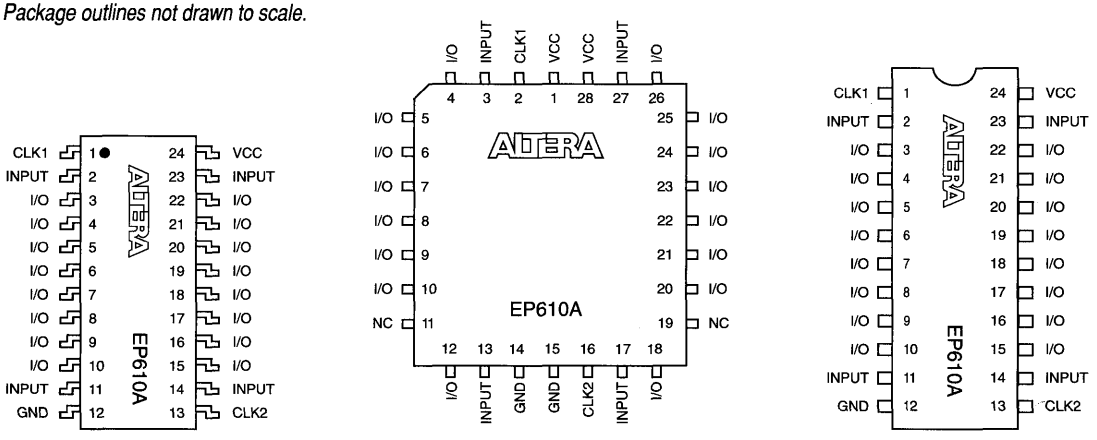
- Highest-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610T, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in reprogrammable plastic chip carrier packages:
  - 24-pin dual in-line package (PDIP)
  - 24-pin small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP610A Erasable Programmable Logic Device (EPLD) is a high-speed version of the EP610 EPLD. It offers enhanced performance and is available in reprogrammable plastic 24-pin, 300-mil DIP; 24-pin SOIC; and 28-pin J-lead chip carrier packages. It is also available with maximum t_{PD} values of 10 ns and 12 ns. See Figure 9.

Figure 9. EP610A Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		45	90	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		45	90	mA

Capacitance

See Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		16	pF

AC Operating Conditions *See Note (3)*

			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O input to non-registered output			10		12	ns
t_{PZX}	Input to output enable			10		12	ns
t_{PXZ}	Input to output disable, *See Note (6)*	C1 = 5 pF		10		12	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		10		12	ns

Global Clock Mode			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (7)*	100		83.3		MHz
t_{SU}	Input setup time		8		8		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		5		6		ns
t_{CL}	Clock low time		5		6		ns
t_{CO1}	Clock to output delay			6		6	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*See Note (4)*	100		83.3		MHz

Array Clock Mode			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (7)*	100		83.3		MHz
t_{ASU}	Input setup time		5		6		ns
t_{AH}	Input hold time		5		6		ns
t_{ACH}	Clock high time		5		6		ns
t_{ACL}	Clock low time		5		6		ns
t_{ACO1}	Clock to output delay			12		13	ns
t_{ACNT}	Minimum clock period			10		12	ns
f_{ACNT}	Internal maximum frequency	*See Note (4)*	100		83.3		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 16-bit counter.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF.
(6) Sample-tested only for an output change of 500 mV.
(7) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	Consult factory
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Features

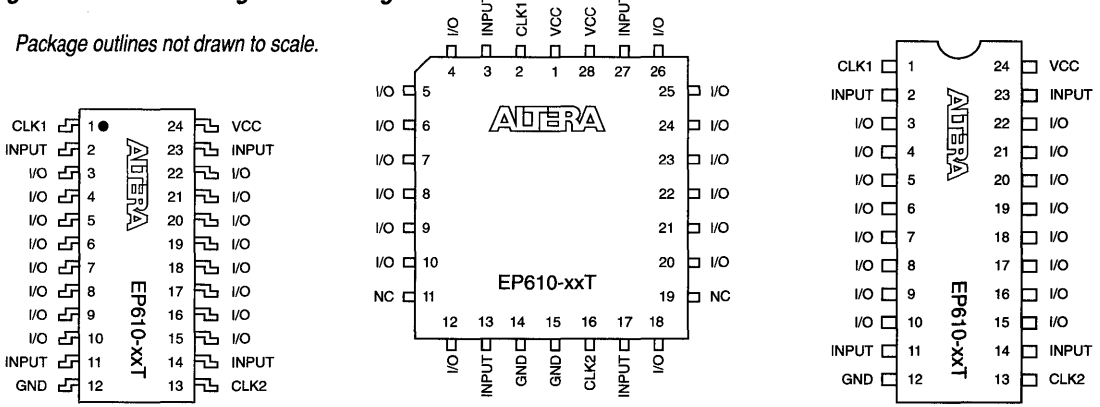
- High-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610A, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in low-cost one-time-programmable (OTP) plastic chip carrier packages
  - 24-pin, 300-mil dual in-line package (PDIP)
  - 24-pin small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option allowing independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP610T Erasable Programmable Logic Device (EPLD) is a low-cost, high-performance version of the EP610 device. This EPLD operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device is preset at the factory. The EP610T EPLD is available in OTP plastic 24-pin, 300-mil DIP; 24-pin SOIC; and 28-pin J-lead chip carrier packages with maximum t_{PD} values of 15 ns, 20 ns, and 25 ns. See Figure 10.

Figure 10. EP610T Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*See Note (2)*		100	ns
t_F	Input fall time	*See Note (2)*		100	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		60	90	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		60	90	mA

Capacitance

See Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

Symbol	Parameter	Conditions	EP610-15T Min	EP610-15T Max	EP610-20T Min	EP610-20T Max	EP610-25T Min	EP610-25T Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output			17		22		27	ns
t_{PZX}	Input to output enable			15		20		25	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		15		20		25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20		27	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	ns

Global Clock Mode			EP610-15T		EP610-20T		EP610-25T		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
f_{MAX}	Maximum frequency	*See Note (8)*	83.3		62.5		47.6		MHz
t_{SU}	Input setup time		9		11		21		ns
t_{H}	Input hold time		0		0		0		ns
t_{CH}	Clock high time		6		8		10		ns
t_{CL}	Clock low time		6		8		10		ns
t_{CO1}	Clock to output delay			11		13		15	ns
t_{CNT}	Minimum clock period			12		16		25	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	83.3		62.5		40.0		MHz

Array Clock Mode			EP610-15T		EP610-20T		EP610-25T		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
f_{MAX}	Maximum frequency	*See Note (8)*	71.4		55.5		47.6		MHz
t_{ASU}	Input setup time		6		8		8		ns
t_{AH}	Input hold time		6		8		12		ns
t_{ACH}	Clock high time		7		9		10		ns
t_{ACL}	Clock low time		7		9		10		ns
t_{ACO1}	Clock to output delay			15		20		27	ns
t_{ACNT}	Minimum clock period			14		18		25	ns
f_{ACNT}	Internal maximum frequency	*See Note (5)*	71.4		55.5		40.0		MHz

Notes to tables:

1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15T and EP610-20T: Maximum V_{PP} is 14.0V.
2) For EP610-15T and EP610-20T EPLDs: t_R and t_F = 40 ns. For EP610-15T and EP610-20T clocks: t_R and t_F = 20 ns.
3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
5) Measured with a device programmed as a 16-bit counter.
6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25T: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
7) Sample-tested only for an output change of 500 mV.
8) The f_{MAX} values represent the highest frequency for pipelined data.

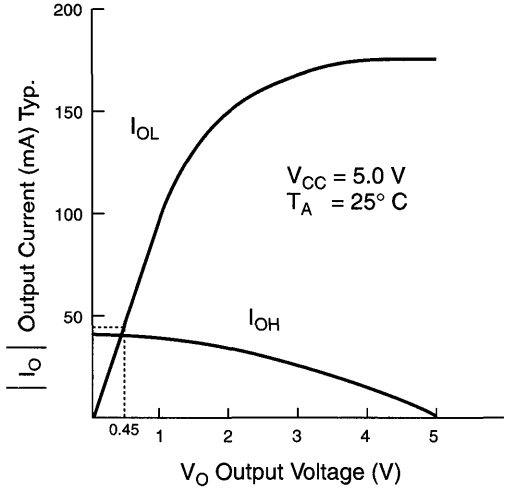
Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP610-15T, EP610-20T, EP610-25T
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

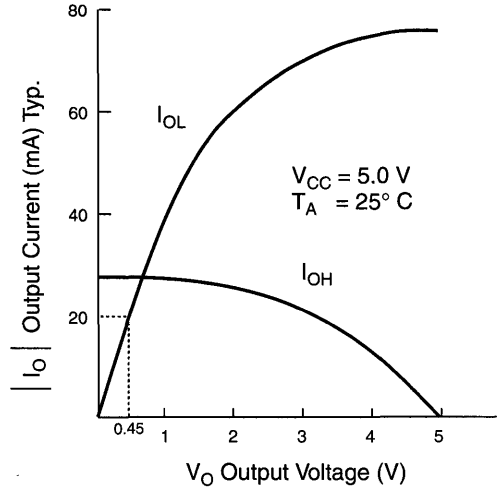
Figure 11 shows the output drive characteristics for EP610T I/O pins and typical supply current versus frequency for the EP610T EPLD.

Figure 11. EP610T Output Drive Characteristics and I_{CC} vs. Frequency

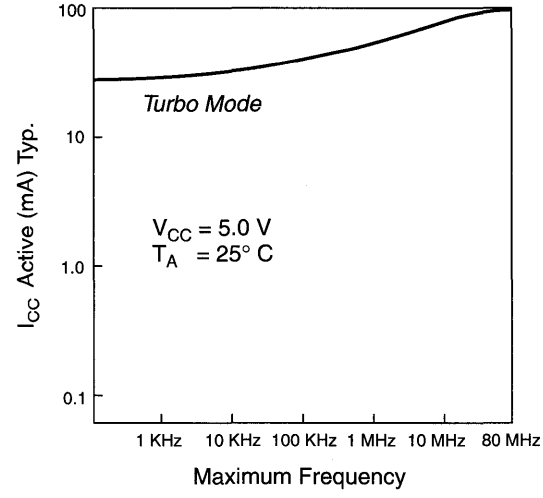
EP610-15T and EP610-20T EPLDs



EP610-25T EPLD



All EP610T EPLDs



Features

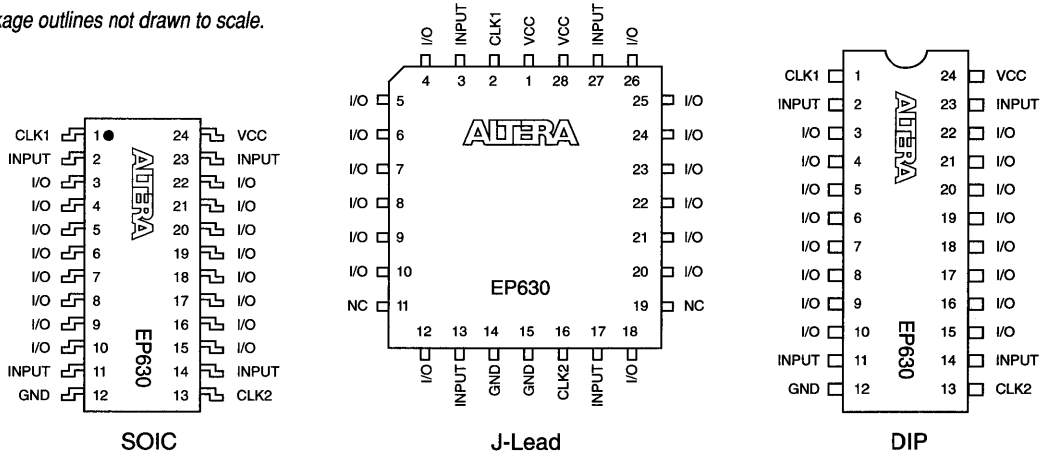
- High-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610A, and EP610T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in one-time-programmable (OTP) plastic chip carrier packages
  - 24-pin, 300-mil dual in-line package (PDIP)
  - 24-pin, 300-mil small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP630 Erasable Programmable Logic Device (EPLD) is a fast, low-power version of the EP610 device. The EP630 EPLD can implement a 16-bit counter at up to 83 MHz and typically consumes 5 mA when operating at 1 MHz. The EP630 EPLD is available in OTP plastic 24-pin, 300-mil DIP; 24-pin, 300-mil SOIC; and 28-pin J-lead chip carrier packages. It is available with maximum t_{PD} values of 15 ns and 20 ns. See Figure 12.

Figure 12. EP630 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*See Note (2)*		40	ns
t_F	Input fall time	*See Note (2)*		40	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (5)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		5	10	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		45	90	mA

Capacitance *See Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (9)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode

			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_H	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*See Note (6)*	83.3		62.5		0	MHz

Array Clock Mode

			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	71.4		55.5		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (6)*	71.4		55.5		0	MHz

Notes to tables:

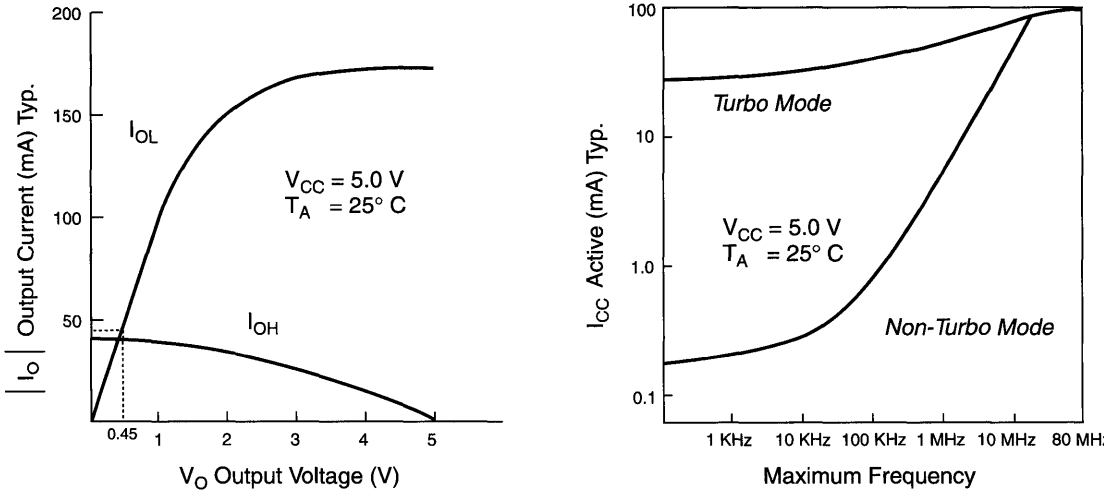
(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(6) Measured with a device programmed as a 16-bit counter.
(7) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only.
(8) See "Turbo Bit" earlier in this data sheet.
(9) Sample-tested only for an output change of 500 mV.
(10) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP630-15, EP630-20
Industrial	(–40° C to 85° C)	EP630-20
Military	(–55° C to 125° C)	Consult factory

Figure 13 shows the output drive characteristics for EP630 I/O pins and typical supply current versus frequency for the EP630 EPLD.

Figure 13. EP630 Output Drive Characteristics and I_{CC} vs. Frequency



EP910 EPLDs

High-Performance 24-Macrocell Devices

September 1991, ver. 2

Data Sheet

Features

- High-density replacement for TTL and 74HC with up to 900 gates
- High-performance 24-macrocell EPLD with t_{PD} = 25 ns and counter frequencies up to 40 MHz
- Zero-power operation (20 µA standby)
- Advanced CMOS EPROM technology to allow device erasure and reprogramming
- Individual clocking of all registers, or banked register operation from two global Clock inputs
- 24 macrocells with configurable I/O architecture, allowing up to 36 inputs and 24 outputs
- Programmable registers providing D, T, SR, or JK flip-flops with individual asynchronous Clear control
- 100% generically testable to provide 100% programming yield
- Programmable Security Bit for total protection of proprietary designs
- Available in 40-pin DIP and 44-pin J-lead chip carriers
- Extensive third-party software and programming support

General Description

Altera's EP910 Erasable Programmable Logic Devices (EPLDs) can implement up to 900 equivalent gates of SSI and MSI logic. These EPLDs are available in windowed ceramic or one-time-programmable (OTP) plastic 40-pin dual in-line packages (CerDIP and PDIP) and 44-pin J-lead chip carriers (JLCC and PLCC).

EP910 EPLDs use sum-of-products logic that consists of a programmable-AND/fixed-OR structure. They accommodate combinatorial and sequential logic functions with up to 36 inputs and 24 outputs.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in active-high and active-low modes.

EP910 macrocells can be individually programmed for D, T, JK, or SR flip-flop operation, or configured for combinatorial operation. In addition, each register can be individually clocked from any of the input or feedback paths in the AND array. These features make it possible to simultaneously implement a variety of logic functions. For example, EP910 EPLDs are ideal for integrating several 20- and 24-pin PAL devices.

The CMOS EPROM technology in EP910 EPLDs can reduce power consumption to less than 20% of the power required by equivalent bipolar

devices, without losing speed. This reduced power consumption makes EP910 EPLDs desirable for a wide range of applications. Moreover, these EPLDs are 100% generically testable and can be erased with UV light. Designs and design modifications can be implemented quickly, eliminating the need for post-programming testing.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD. MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

EP910 EPLDs

The EP910 EPLD is pin-, function-, and JEDEC-File-compatible with the EP910A and EP910T EPLDs. JEDEC Files generated for an EP910 EPLD can be used for programming these devices.

EP910

The EP910 EPLD combines high speed with low power. It can implement a 24-bit counter at up to 33 MHz, and typically consumes 6 mA when operating at 1 MHz. The EP910 EPLD is available with maximum t_{PD} values of 30 ns, 35 ns, and 40 ns. Both MIL-STD-883B-compliant and DESC-approved parts are available.

EP910A

The EP910A is a high-speed version of the EP910 EPLD. It is available with maximum t_{PD} values of 15 ns and 25 ns, which are ideal for high-speed address decoding. The EP910A is fabricated on an advanced 0.8-micron process, and supports 16-bit counter frequencies of up to 83 MHz.

EP910T

The EP910T EPLD is a lower-cost version of the EP910 device. This device operates in Turbo mode only. The Turbo Bit in the EPLD is preset at the factory. The EP910T EPLD is available with a maximum t_{PD} value of 30 ns.

Functional Description

EP910 EPLDs use CMOS EPROM technology to configure connections in a programmable-AND logic array. EPROM connections are also used to construct a highly flexible programmable I/O architecture that provides advanced functions for user-programmable logic.

EP910 EPLDs have 12 dedicated data inputs, 2 global Clock inputs, and 24 I/O pins that can be individually configured for input, output, or bidirectional operation. Figure 1 shows the EP910 macrocell. Each macrocell contains 10 product terms for the following functions: 8 product terms are dedicated to logic implementation; 1 product term is used for asynchronous Clear control of the internal register; and 1 product term implements either Output Enable or an array Clock.

Figure 1. EP910 Macrocell

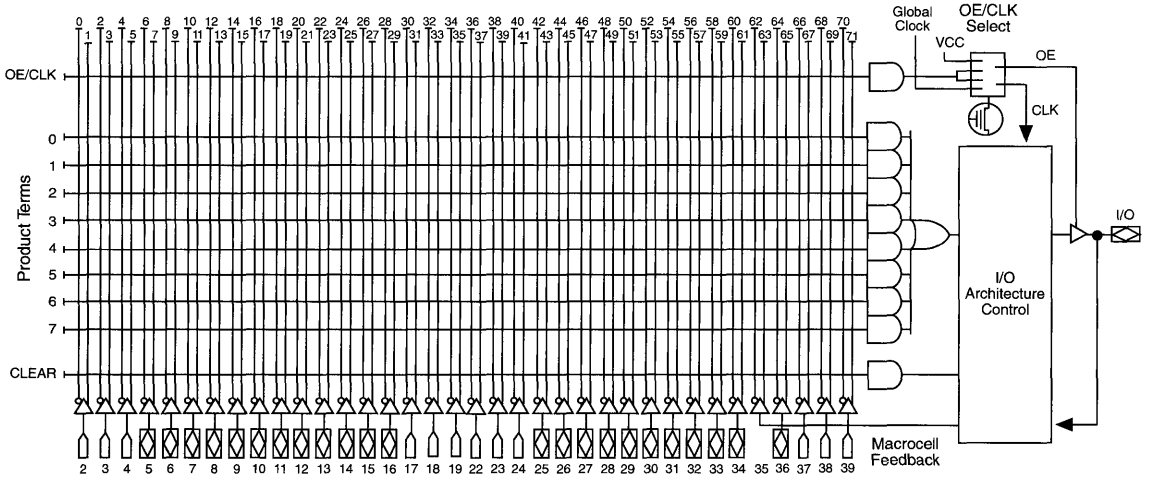
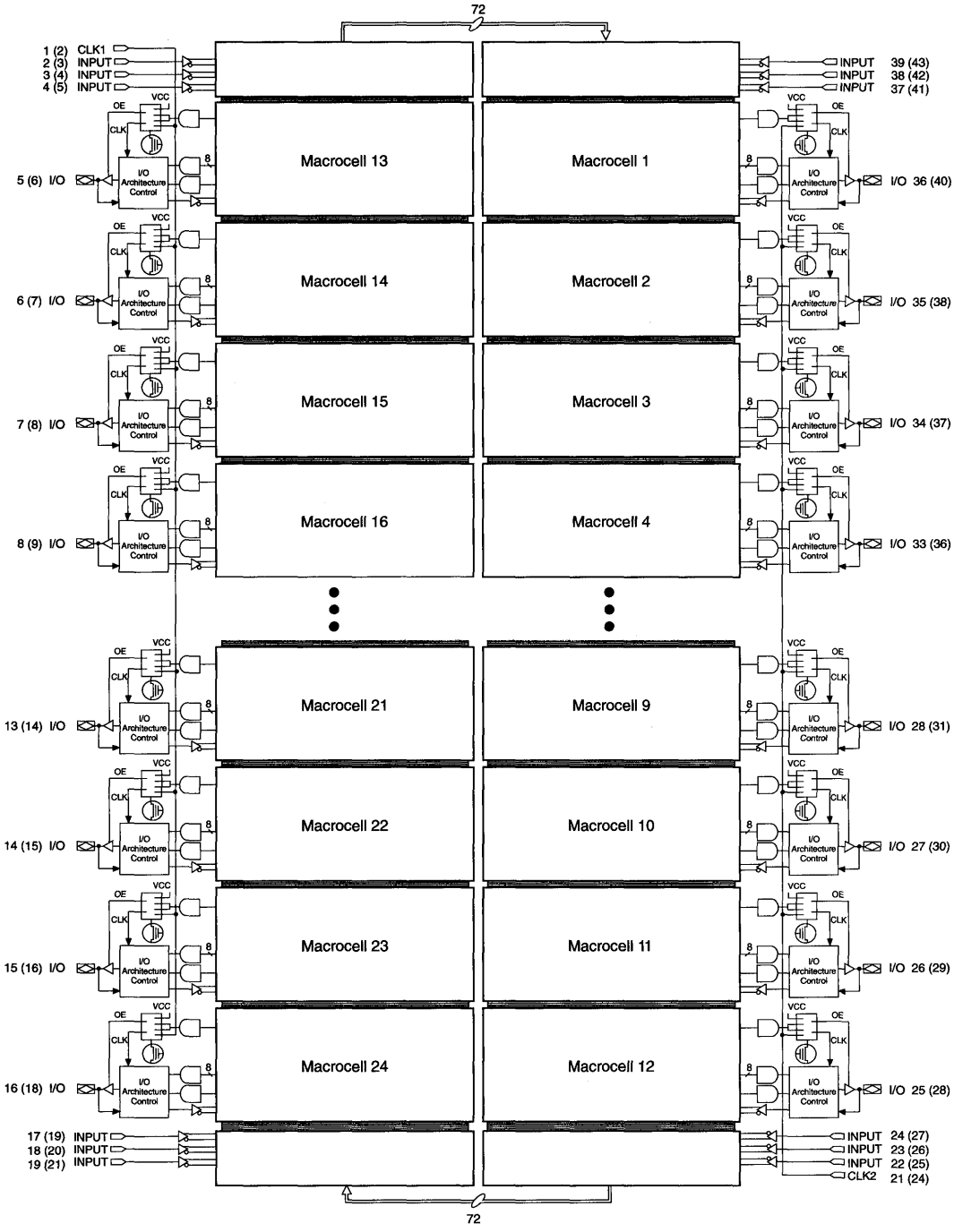


Figure 2 shows the block diagram of an EP910 EPLD. The internal device architecture has a sum-of-products (AND-OR) structure. Inputs to the programmable-AND array come from the true and complement signals of the 12 dedicated data inputs and the 24 I/O feedback signals. The 72-input AND array has 240 product terms that are distributed equally among the 24 macrocells. Each EP910 product term represents a 72-input AND gate.

Figure 2. EP910 Block Diagram *Numbers in parentheses are for J-lead packages.*



In the erased state, the true and complement of the AND-array inputs are connected to the product terms. An EPROM control cell is located at each intersection of an AND-array input and a product term. During the programming process, selected connections are opened, allowing any product term to be connected to the true or complement of an array input signal with the following results:

- If both the true and complement of an array input signal are connected, the output of the AND gate is a logic low.
- If both the true and complement of any array input signal are programmed "open," a logic "don't care" results for that input.
- If all 72 inputs for a given product term are programmed "open," the output of the corresponding AND gate is a logic high.

Two dedicated Clock inputs (which are not available in the AND array) provide the signals used for global clocking of EP910 internal registers. Each signal is positive-edge-triggered and has control over 12 registers. CLK1 controls macrocells 13 to 24; CLK2 controls macrocells 1 to 12. The programmable I/O architecture allows each of the 24 internal registers to have a global- or array-Clock (product-term) mode.

I/O Architecture

EP910 architecture provides each macrocell with over 50 programmable I/O configurations. Each macrocell can be configured for combinatorial or registered output, with programmable output polarity. Four register types (D, T, JK, and SR) may be implemented in each macrocell without requiring additional logic. I/O feedback selection can be programmed for registered or input feedback. The I/O architecture can also individually clock each internal register from any internal signal.

OE/CLK Selection

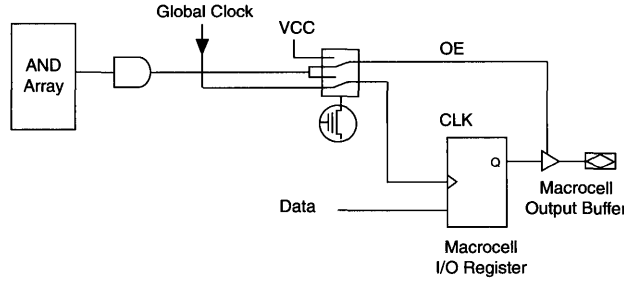
Figure 3 shows the two modes of operation provided by the OE/CLK Select multiplexer. This multiplexer, controlled by a single EPROM bit, may be individually configured at each I/O pin.

Figure 3. OE/CLK Select Multiplexer

Mode 0:

The register is clocked by the global Clock signal, which can be connected to eleven other macrocells. The output is enabled by the logic from the product term.

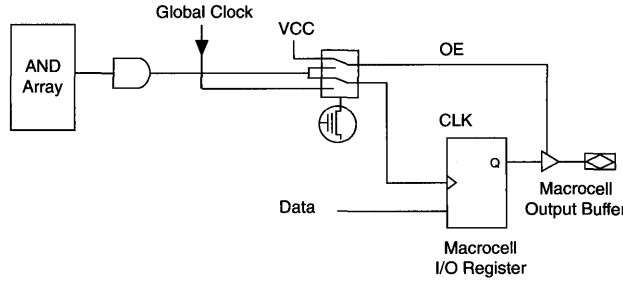
OE = Array (Product Term)
CLK = Global



Mode 1:

The output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated in EP910 EPLDs.

OE = Enabled
CLK = Array



In Mode 0, the tri-state output buffer is controlled by a single product term If the output of the AND gate is high, the output buffer is enabled. If the output is low, the output buffer has a high-impedance value. In this mode the macrocell flip-flop is clocked by its global Clock input signal (CLK1 or CLK2). In the erased state, the OE/CLK Select multiplexer is configured to Mode 0.

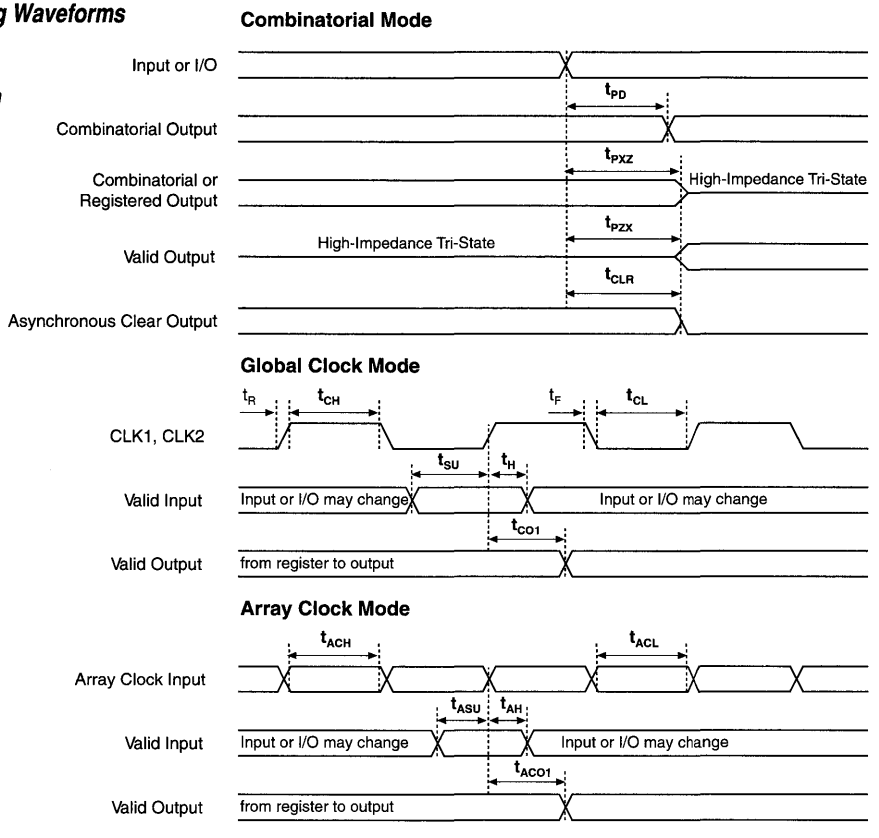
In Mode 1, the Output Enable buffer is always enabled, so the macrocell flip-flop can be triggered from an array Clock signal generated by the OE/CLK product term. This mode allows flip-flops to be individually clocked from any of the 72 AND-array input signals. With both true and complement signals in the AND array, the flip-flop can be configured to

trigger on a rising or falling edge. This product-term-controlled clock configuration also allows implementation of gated clock structures.

Figure 4 shows waveforms for the following modes: combinatorial, global Clock, and array Clock.

Figure 4. EP910 Switching Waveforms

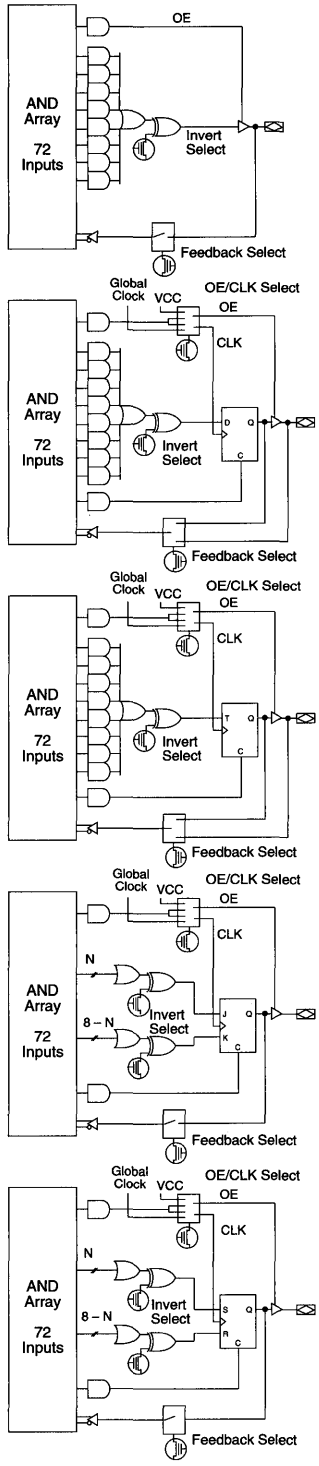
t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Output/ Feedback Selection

Output configurations available with EP910 EPLDs are shown in Figure 5. Each macrocell can be individually configured with combinatorial output or with any of the four register outputs. All registers have an individual asynchronous Clear function controlled by a dedicated product term. When this product term is a logic high, the macrocell register is immediately loaded with a logic low. The Clear function is performed automatically during power-up.

Figure 5. EP910 I/O Configurations



Combinatorial

I/O Selection

Output/Polarity	Feedback
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

D Flip-Flop

I/O Selection

Output/Polarity	Feedback
D Register/High	D Register, Pin, None
D Register/Low	D Register, Pin, None
None	D Register
None	Pin

Function Table

D	Q_n	Q_{n+1}
L	L	L
L	H	L
H	L	H
H	H	H

T Flip-Flop

I/O Selection

Output/Polarity	Feedback
T Register/High	T Register, Pin, None
T Register/Low	T Register, Pin, None
None	T-Register
None	Pin

Function Table

T	Q_n	Q_{n+1}
L	L	L
L	H	H
H	L	H
H	H	L

JK Flip-Flop

I/O Selection

Output/Polarity	Feedback
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

Function Table

J	K	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

SR Flip-Flop

I/O Selection

Output/Polarity	Feedback
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

Function Table

S	R	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H

The combinatorial configuration has eight product terms ORed together to generate the output signal. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls the Output Enable buffer.
- The Feedback Select multiplexer allows the user to choose I/O (pin) feedback or no feedback to the AND array.

The D or T register configuration has eight product terms ORed together that are available to the register input. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls asynchronous Clear.
- The OE/CLK Select multiplexer configures the mode of operation to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback, I/O feedback, or no feedback to the AND array.

If the JK or SR register is selected, eight product terms are shared between two OR gates. The outputs of the OR gates feed two primary register inputs. This configuration has the following characteristics:

- The MAX+PLUS II or A+PLUS development system optimizes the allocation of product terms for each register input.
- One product term controls asynchronous Clear.
- The Invert Select EPROM bits control output polarity.
- The OE/CLK Select multiplexer configures the operation mode to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback or no feedback to the AND array.

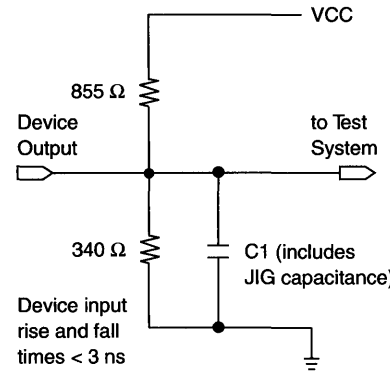
Any I/O pin can be configured as a dedicated input by selecting no output with I/O feedback. In the erased state, the I/O architecture is configured for combinatorial active-low output with I/O feedback.

Functional Testing

EP910 EPLDs are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements. A 100% programming yield is ensured. This testing process eliminates traditional problems associated with fuse-programmed circuits by allowing test programming patterns to be used and then erased. This ability to use application-independent, general-purpose tests, called generic testing, is unique to EPLDs. AC test measurements are performed under the conditions shown in Figure 6.

Figure 6. EP910 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable input noise immunity.



Design Security

EP910 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security by making programmed data within EPROM cells invisible. The Security Bit, as well as other program data, is reset by erasing the EPLD.

Turbo Bit

EP910 EPLDs contain a programmable Turbo Bit, set with design software, to control the automatic power-down feature that enables the low-standby-power mode (I_{CC1}). When the Turbo Bit is programmed (Turbo = On), the low-standby-power mode is disabled, making the circuit less sensitive to V_{CC} noise transients created by the low-power mode power-up/power-down cycle. All AC values are tested with the Turbo Bit programmed.

If the design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). In this mode, some AC parameters may increase. To determine worst-case timing, values from the AC Non-Turbo Adder specifications must be added to the corresponding AC parameter.

Features

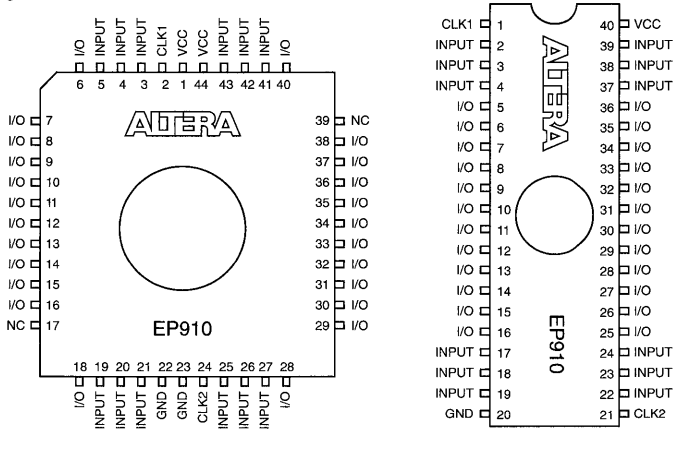
- High-performance 24-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP910A and EP910T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in windowed ceramic and one-time-programmable (OTP) plastic chip carrier packages
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP910 Erasable Programmable Logic Device (EPLD) can implement up to 900 equivalent gates of SSI and MSI logic. It is available in windowed ceramic or OTP plastic 40-pin DIP and 44-pin J-lead chip carrier packages. See Figure 7.

Figure 7. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*See Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*See Note (3)*		100 (50)	ns
t_F	Input fall time	*See Note (3)*		100 (50)	ns

DC Operating Conditions

See Notes (2), (4), (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (6)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*		6	20	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*		45	80 (100)	mA

Capacitance *See Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

MAC Operating Conditions *See Note (5)*

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
tPD1	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
tPD2	I/O input to non-registered output			33		38		43	30	ns
tPZX	Input to output enable			30		35		40	30	ns
tPXZ	Input to output disable	C1 = 5 pF, *See Note (10)*		30		35		40	30	ns
tCLR	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
tIO	I/O input pad and buffer delay			3		3		3	0	ns

Global Clock Mode

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
fMAX	Maximum frequency	*See Note (11)*	41.7		37.0		32.3		0	MHz
tSU	Input setup time		24		27		31		30	ns
tH	Input hold time		0		0		0		0	ns
tCH	Clock high time		12		13		15		0	ns
tCL	Clock low time		12		13		15		0	ns
tCO1	Clock to output delay			18		21		24	0	ns
tCNT	Minimum clock period			30		35		40	0	ns
fCNT	Internal maximum frequency	*See Note (7)*	33.3		28.6		25.0		0	MHz

Array Clock Mode

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
fMAX	Maximum frequency	*See Note (11)*	33.3		31.3		29.4		0	MHz
tASU	Input setup time		10		10		10		30	ns
tAH	Input hold time		15		15		15		0	ns
tACH	Clock high time		15		16		17		0	ns
tACL	Clock low time		15		16		17		0	ns
tACO1	Clock to output delay			33		38		43	30	ns
tACNT	Minimum clock period			30		35		40	0	ns
fACNT	Internal maximum frequency	*See Note (7)*	33.3		28.6		25.0		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot t –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all clocks: t_R and t_F = 100 ns (50 ns).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logi transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as a 24-bit counter.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance fo dedicated clock inputs only. Pin 21 (high-voltage pin during programming) has maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

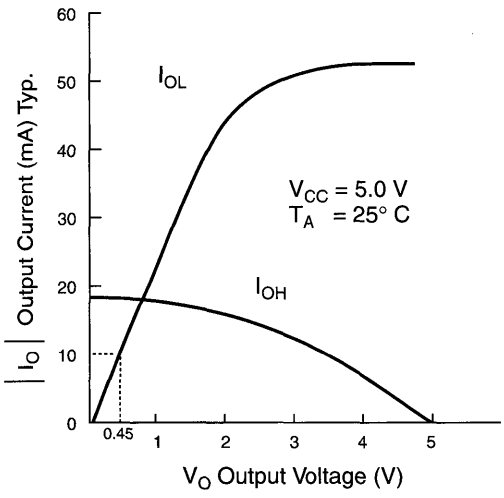
Product Availability

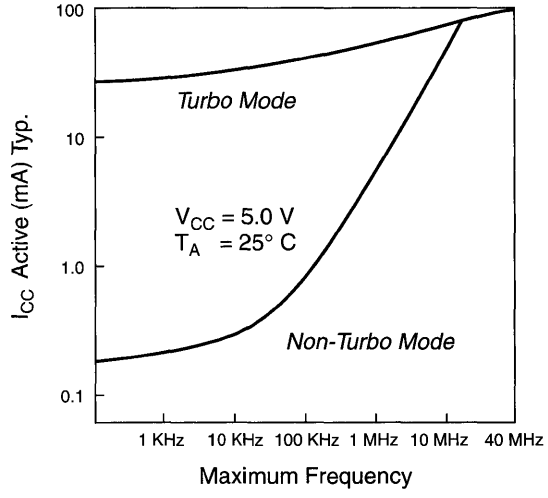
Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP910-30, EP910-35, EP910-40
Industrial	(–40° C to 85° C)	EP910-35, EP910-40
Military	(–55° C to 125° C)	EP910-40

Note: Only military-temperature-range devices are listed above. MIL-STD-883-complian product specifications are provided in Military Product Drawings (MPDs), available b calling Altera's Marketing Department at (408) 984-2800. These MPDs should be used t prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Figure 8 shows the output drive characteristics for EP910 I/O pins an typical supply current versus frequency for the EP910 EPLD.

Figure 8. EP910 Output Drive Characteristics and I_{CC} vs. Frequency





Features

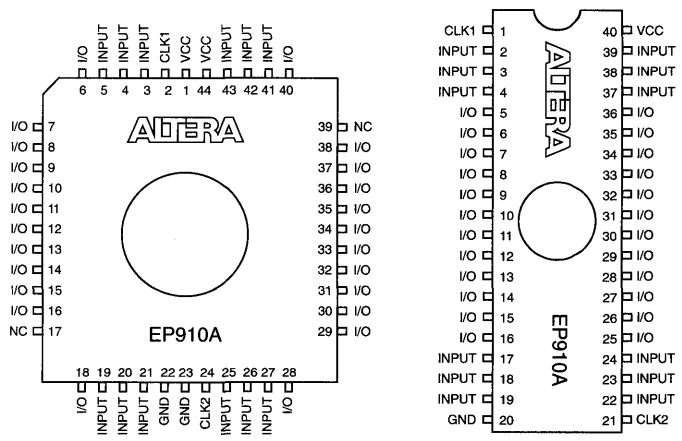
- Highest-performance 24-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP910 and EP910T EPLDs
- Available in windowed ceramic and plastic one-time-programmable (OTP) chip carrier packages
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP910A Erasable Programmable Logic Device (EPLD) is a pin-compatible version of the EP910 EPLD. It offers enhanced performance and is available in 600-mil, 40-pin DIP and 44-pin J-lead chip carrier packages (see Figure 9). The EP910A EPLD contains 24 macrocells with user-configurable I/O architecture for up to 36 inputs and 24 outputs.

Figure 9. EP910A Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		120	150	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		120	150	mA

Capacitance

See Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (3)*

			EP910A-15 *Note (6)*		EP910A-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		25	ns
t_{PD2}	I/O input to non-registered output			15		25	ns
t_{PZX}	Input to output enable			15		25	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		15		25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		25	ns

Global Clock Mode			EP910A-15 *Note (6)*		EP910A-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	83.3		62.5		MHz
t_{SU}	Input setup time		10		15		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		6		8		ns
t_{CL}	Clock low time		6		8		ns
t_{CO1}	Clock to output delay			8		15	ns
t_{CNT}	Minimum clock period			14		25	ns
f_{CNT}	Internal maximum frequency	*See Note (4)*	71.4		40		MHz

Array Clock Mode			EP910A-15 *Note (6)*		EP910A-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	83.3		62.5		MHz
t_{ASU}	Input setup time		6		8		ns
t_{AH}	Input hold time		6		8		ns
t_{ACH}	Clock high time		7		12		ns
t_{ACL}	Clock low time		7		12		ns
t_{ACO1}	Clock to output delay			15		25	ns
t_{ACNT}	Minimum clock period			14		25	ns
f_{ACNT}	Internal maximum frequency	*See Note (4)*	71.4		40		MHz

Notes to tables:

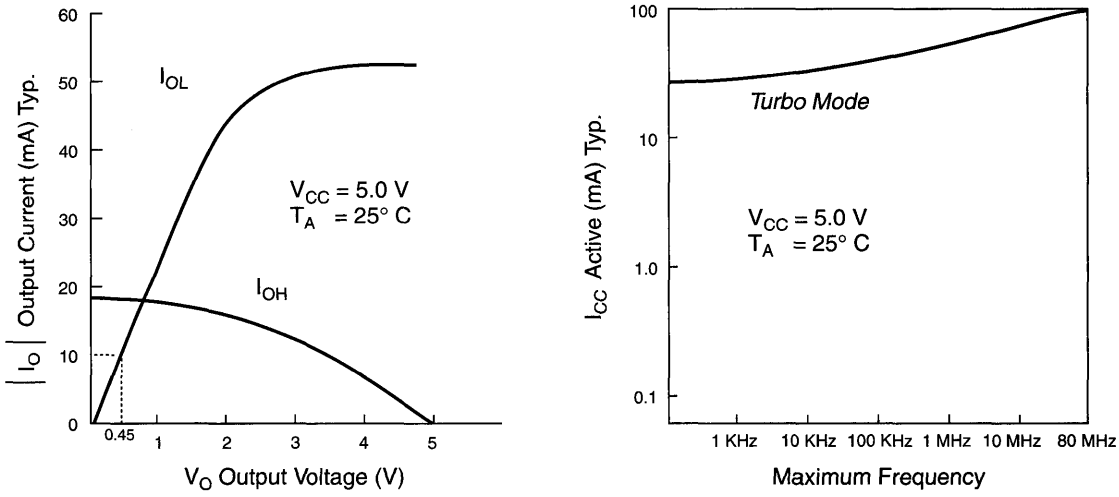
(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 24-bit counter.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(6) This version is under development. Specifications are subject to change. Consult factory for additional information.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP910A-25
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Figure 10 shows the output drive characteristics for EP910A I/O pins and typical supply current versus frequency for the EP910A EPLD.

Figure 10. EP910A Output Drive Characteristics and I_{CC} vs. Frequency



Features

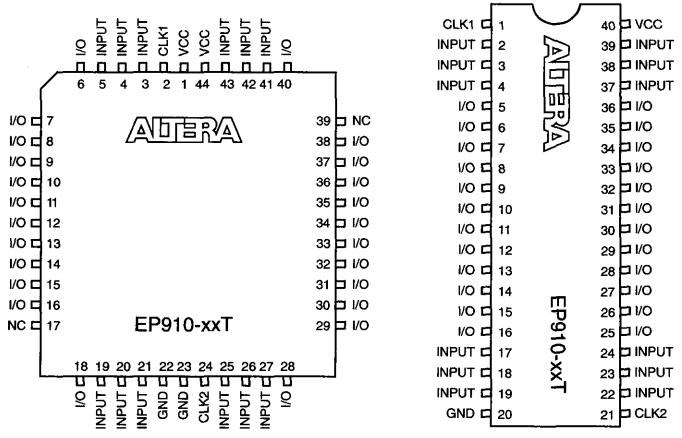
- High-performance 24-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Pin, function, and JEDEC-File-compatible with Altera's EP910 and EP910A EPLDs
- Available in low-cost one-time-programmable (OTP) plastic chip carrier packages
  - 44-pin J-lead chip carrier (PLCC)
  - 40-pin dual in-line package (PDIP)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP910T Erasable Programmable Logic Device (EPLD) is a low-cost, high-performance version of the EP910 device. This EPLD operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device is preset at the factory. The EP910T EPLD is available in OTP plastic 40-pin, 600-mil DIP and 44-pin J-lead packages with maximum t_{PD} values of 30 ns. See Figure 11.

Figure 11. EP910T Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*See Note (2)*		100	ns
t_F	Input fall time	*See Note (2)*		100	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		80	115	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		80	115	mA

Capacitance

See Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30	ns
t_{PD2}	I/O input to non-registered output			33	ns
t_{PZX}	Input to output enable			30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33	ns
t_{IO}	I/O input pad and buffer delay			3	ns

Global Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	41.7		MHz
t_{SU}	Input setup time		24		ns
t_{H}	Input hold time		0		ns
t_{CH}	Clock high time		12		ns
t_{CL}	Clock low time		12		ns
t_{CO1}	Clock to output delay			18	ns
t_{CNT}	Minimum clock period			30	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	33.3		MHz

Array Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	33.3		MHz
t_{ASU}	Input setup time		10		ns
t_{AH}	Input hold time		15		ns
t_{ACH}	Clock high time		15		ns
t_{ACL}	Clock low time		15		ns
t_{ACO1}	Clock to output delay			33	ns
t_{ACNT}	Minimum clock period			30	ns
f_{ACNT}	Internal maximum frequency	*See Note (5)*	33.3		MHz

Notes to tables:

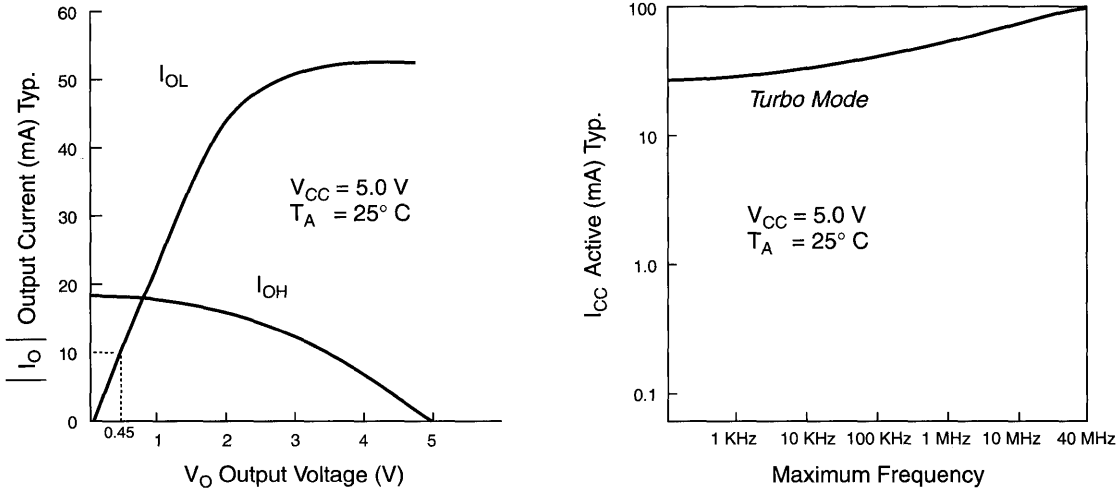
1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
2) For all clocks: t_R and t_F = 100 ns.
3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
5) Measured with a device programmed as a 24-bit counter.
6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
7) Sample-tested only for an output change of 500 mV.
8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP910-30T
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Figure 12 shows the output drive characteristics for EP910T I/O pins and typical supply current versus frequency for the EP910T EPLD.

Figure 12. EP910T Output Drive Characteristics and I_{CC} vs. Frequency



EP1810 EPLDs

High-Performance 48-Macrocell Devices

September 1991, ver. 2

Data Sheet

Features

- High-density replacement for TTL and 74HC
- High-performance 48-macrocell EPLD with t_{PD} = 20 ns and counter frequencies up to 50 MHz
- Zero-power operation (50 µA typical standby)
- Advanced CMOS EPROM technology allowing devices to be erased and reprogrammed
- Individual clocking of all registers or banked register operation from four global Clock inputs
- Programmable registers providing D, T, JK, or SR flip-flops with individual asynchronous Clear control
- 48 macrocells with configurable I/O architecture, allowing up to 64 inputs and 48 outputs
- 100% generically testable to provide 100% programming yield
- Programmable Security Bit for total protection of proprietary designs
- Available in 68-pin J-lead and PGA packages
- Extensive third-party software and programming support

General Description

The EP1810 Erasable Programmable Logic Devices (EPLDs) offer LSI density, TTL-equivalent speed, and low power consumption. Each EPLD can replace 20 to 30 SSI and MSI packages. These EPLDs are available in 68-pin windowed ceramic and one-time-programmable plastic J-lead (JLCC and PLCC), and windowed ceramic pin-grid array (PGA) packages.

EP1810 EPLDs are designed as LSI replacements for traditional low-power Schottky TTL logic circuits and low-density Programmable Logic Devices (PLDs). These devices have the integration density to replace five CMOS 22V10 devices. The speed and density of the EP1810 EPLDs enable them to implement high-performance, complex functions, such as dedicated peripheral controllers and intelligent support chips. IC count and power requirements are considerably reduced with EP1810 EPLDs, thus minimizing the total size and system cost and significantly increasing reliability.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD.

MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

EP1810 EPLDs use EPROM technology to configure logic connections. User-defined logic functions may be constructed by selectively programming EPROM cells within the EPLD. Moreover, these EPLDs are 100% generically testable and can be erased with UV light. Designs and design modifications can be implemented quickly, eliminating the need for post-programming testing.

EP1810 EPLDs

The EP1810 EPLD is pin-, function-, and JEDEC-File-compatible with the EP1810T and EP1830 EPLDs. JEDEC Files generated for an EP1810 EPLD can be used for programming EP1810T and EP1830 devices.

EP1810

The EP1810 EPLD combines speed with low power. It can implement four 12-bit counters at up to 50 MHz, and typically consumes less than 20 mA when operating at 1 MHz. It is available with maximum t_{PD} values of 20, 25, 35, and 45 ns. Both MIL-STD-883B-compliant and DESC-approved parts are available.

EP1810T

The EP1810T EPLD is a lower-cost version of the EP1810 device. This device operates in Turbo mode only. The Turbo Bit in the EPLD is preset at the factory. The E1810T EPLD is available with maximum t_{PD} values of 20 ns, 25 ns, and 30 ns.

EP1830

The EP1830 is a fast, low-power version of the EP1810 device. This device can implement four 12-bit counters at up to 50 MHz and typically consumes 20 mA when operating at 1 MHz. It is available with a maximum t_{PD} values of 20 ns and 25 ns.

Functional Description

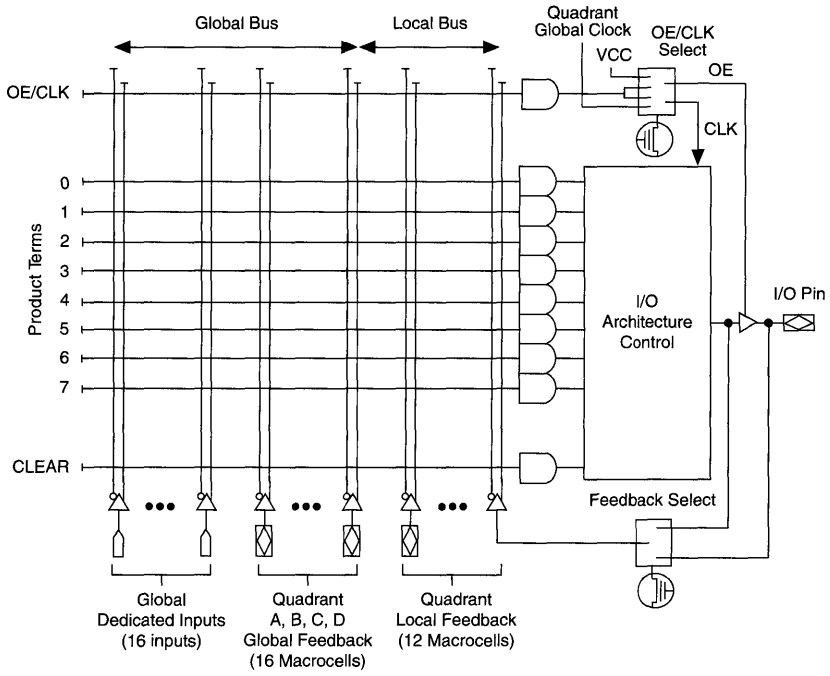
EP1810 EPLDs use CMOS EPROM cells to configure internal logic functions. The architecture is 100% user-configurable, accommodating a variety of independent logic functions.

EP1810 EPLDs have 48 macrocells, 16 dedicated data inputs (4 of which can also be used as global Clock inputs), and 48 I/O pins that can be individually configured for input, output, or bidirectional operation on a macrocell-by-macrocell basis. Each macrocell contains 10 product terms for the following functions: 8 product terms are dedicated to logic

implementation; 1 product term is used for Clear control of the internal register; and 1 product term implements either Output Enable or an array Clock.

Of the 48 macrocells, 32 are local (see Figure 1) and 16 are global macrocells (see Figure 2). Local macrocells offer a multiplexed feedback path (with pin or macrocell feedback) and drive the local bus in their quadrants. Global macrocells feature two dedicated feedback paths: one feeds the local bus; the other feeds the global bus. This process, called dual feedback, allows global macrocells to implement buried logic functions while the associated I/O pin is used as an input. Dual feedback ensures maximum I/O flexibility.

Figure 1. EP1810 Local Macrocell



Each macrocell consists of a logic array, a tri-state I/O buffer, and a selectable register element that can be programmed for D, T, JK, or SR operation, or bypassed for combinatorial functions. Each macrocell also has programmable output polarity. The logic array has a sum-of-products (AND/OR) structure. The 88 inputs to the programmable-AND array come from true and complement signals of the 16 dedicated data inputs, the 12 I/O feedback signals, and the 16 global feedback signals. The EP1810 EPLD has a total of 480 product terms distributed among 48 macrocells. Each product term represents an 88-input AND gate.

Figure 2. EP1810 Global Macrocell

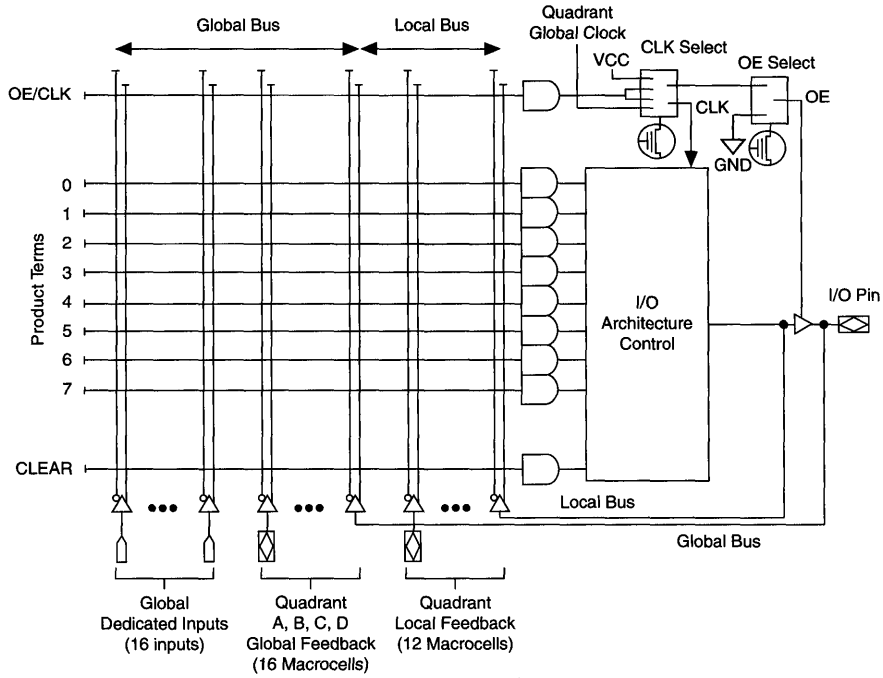


Figure 3 shows the complete block diagram of an EP1810 EPLD. The EP1810 device has four identical quadrants, each containing 12 macrocells. Internal bus structures in these EPLDs feed input signals into the macrocells. Macrocell outputs drive the external pins and internal buses.

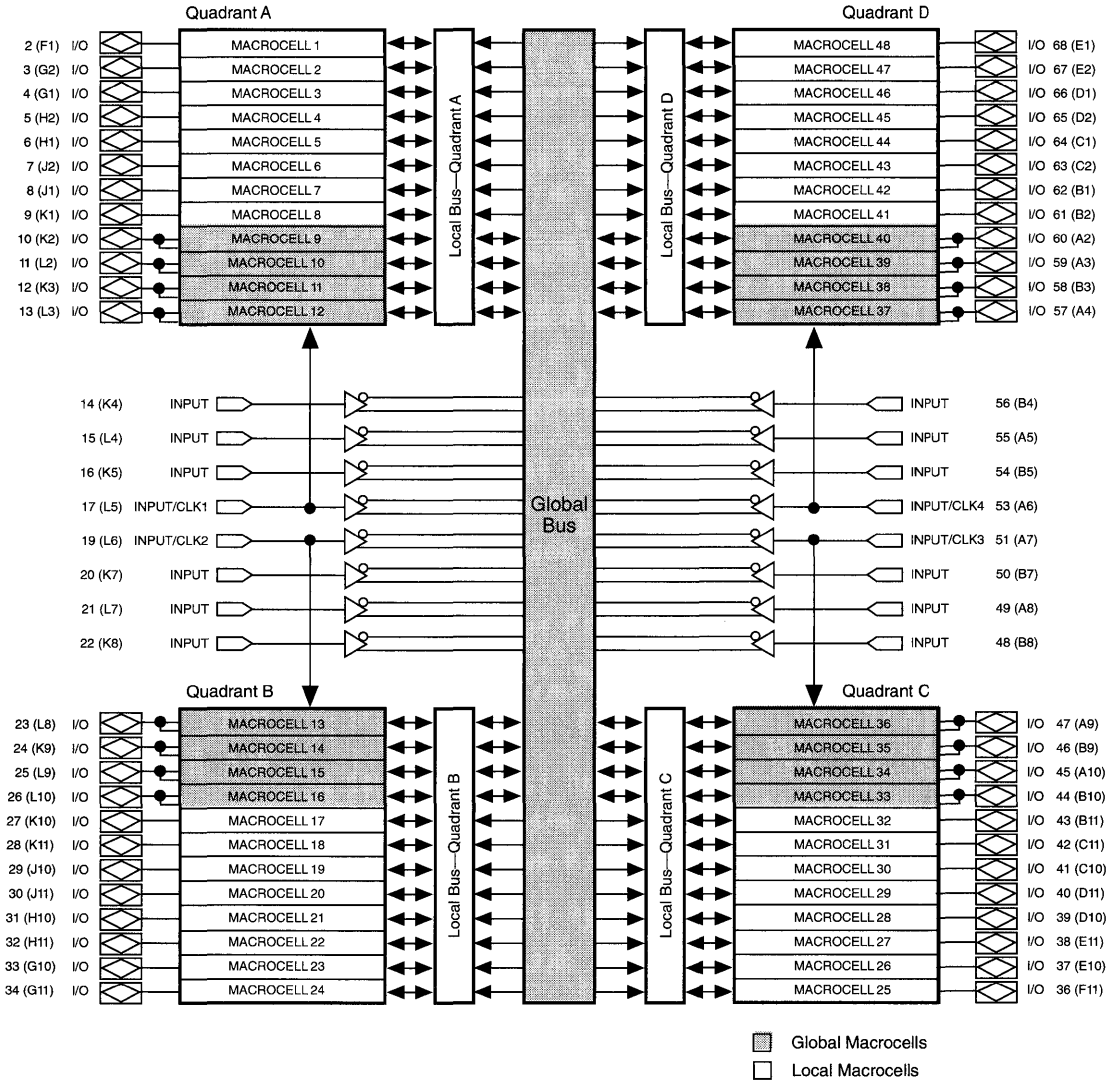
In the erased state, the true and complement of the AND-array inputs are connected to the product terms. An EPROM control cell is located at each intersection of an AND-array input and a product term. During programming, selected connections are opened, allowing any product term to be connected to a true or complement array input signal.

Clock Options

Each internal flip-flop in EP1810 EPLDs can be clocked independently or in user-defined groups. Each internal register may select its clock source from a dedicated global Clock pin or a product term within the macrocell. Any input or internal logic function can be used as a clock.

Four dedicated inputs also provide global Clock signals (CLK1 to CLK4) to the flip-flops. One global Clock is located in each quadrant; each of which is connected directly to an EP1810 external pin. Global Clocks provide clock-to-output delay times that are faster than internally generated clock signals. Array Clocks provide individual clocking on a macrocell-by-macrocell basis, either directly from pins or through internal logic.

Figure 3. EP1810 Block Diagram



Array clock signals allow flip-flops to be configured for positive- or negative-edge-triggered operation. When global Clocks are used, the flip-flops are triggered by the positive edge, i.e., data transitions occur on the rising edge of the clock.

Both global and local macrocells have the same timing characteristics. Switching waveforms for combinatorial, global Clock, and array Clock modes are shown in Figure 4. The timing model is shown in Figure 5.

Figure 4. EP1810 Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

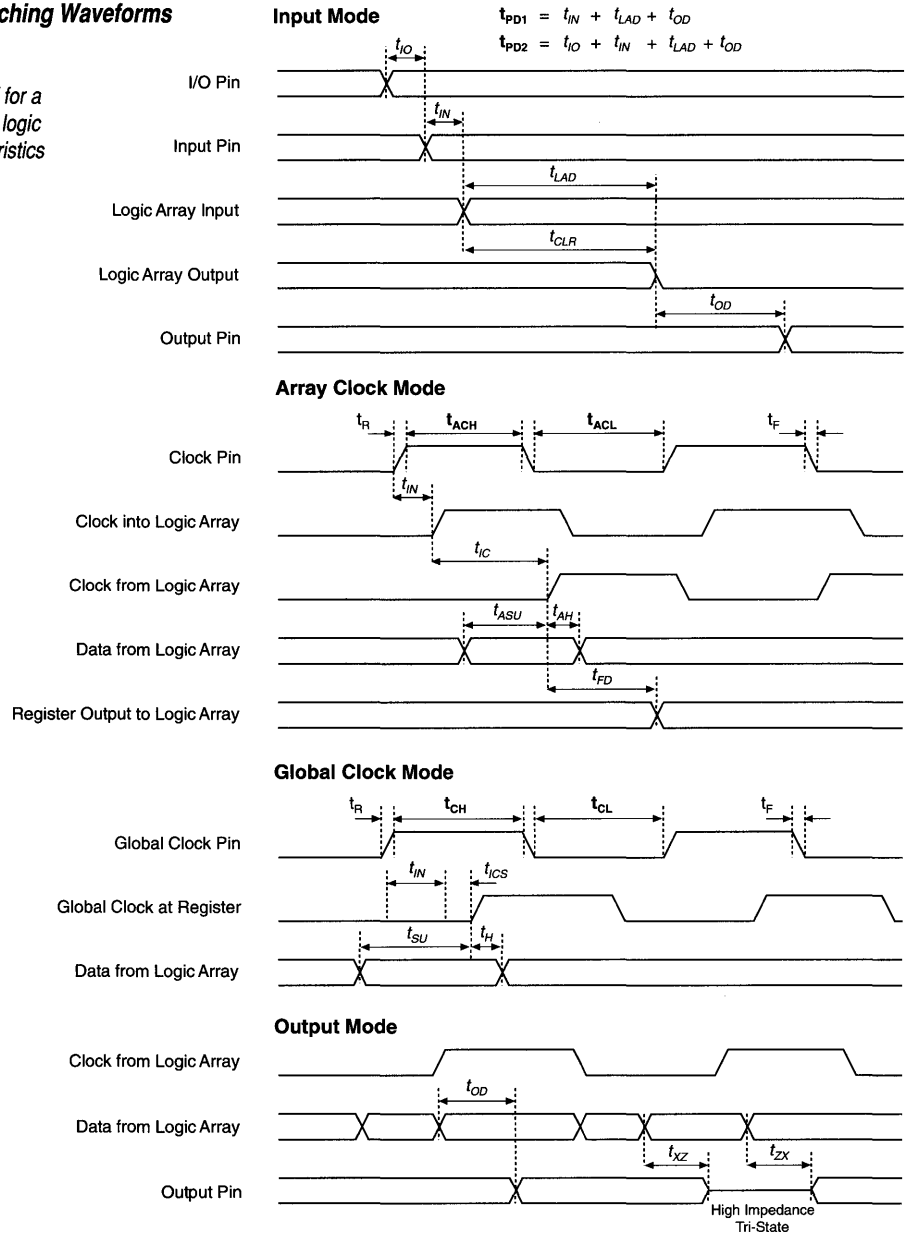
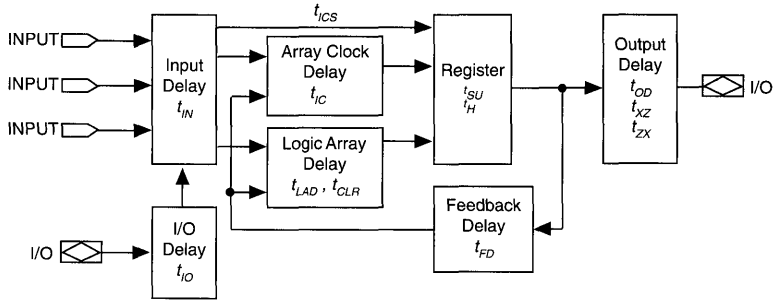


Figure 5. EP1810 Timing Model

If the register is bypassed, the delay between the logic array and the output buffer is zero.

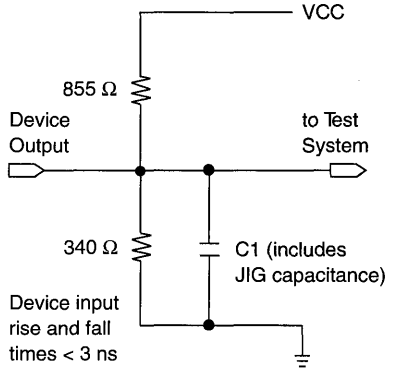


Functional Testing

EP1810 EPLDs are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements. A 100% programming yield is ensured. These EPLDs allow test programs to be used and then erased during early stages of production. The ability to use application-independent, general-purpose tests—called generic testing—is unique to EPLDs. The EPLDs also contain on-board test circuitry that allows verification of functions and AC specifications for one-time-programmable packages. AC test measurements are performed under the conditions shown in Figure 6.

Figure 6. EP1810 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Design Security

EP1810 EPLDs contain a programmable Security Bit that controls access to the programmed information. If this Security Bit is used, a proprietary design implemented in the device cannot be copied or retrieved. Since this option makes programmed data within EPROM cells invisible, the designer has a high level of design security. The Security Bit, as well as all other program data, is reset by erasing the EPLD.

Turbo Bit

All EP1810 EPLDs contain a Turbo Bit, set with the design software, to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit is programmed (Turbo = On), the low-standby-power mode (I_{CC1}) is disabled, making the circuit less sensitive to V_{CC} noise transients from the non-turbo mode power-up/power-down cycle. All AC values are tested with the Turbo Bit programmed.

If the design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). When operating in this mode, some AC parameters may increase. To determine worst-case timing, values given in the AC Non-Turbo Adder specifications must be added to the AC parameter.

Features

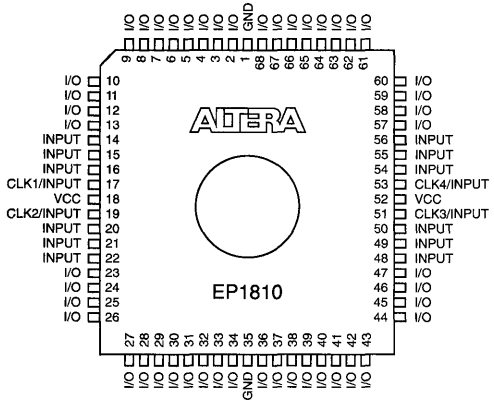
- Highest-performance 48-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 20, 25, 35, and 45 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810T and EP1830 EPLDs
- Available in 68-pin windowed ceramic or one-time-programmable (OTP) plastic J-lead chip carrier and windowed ceramic pin-grid array (PGA) packages
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

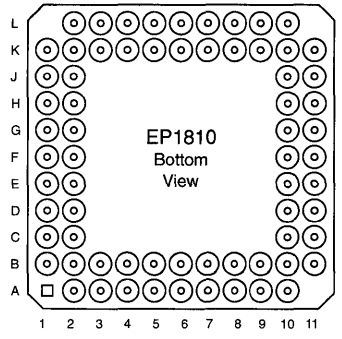
The EP1810 Erasable Programmable Logic Device (EPLD) offers LSI density, TTL-equivalent speed, and low power consumption. It is available in 68-pin windowed ceramic and OTP plastic J-lead chip carrier and windowed ceramic PGA packages. See Figure 7.

Figure 7. EP1810 Package Pin-Out Diagrams

See Table 1 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.



J-Lead



PGA

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*See Note (3)*		50	ns
t_F	Input fall time	*See Note (3)*		50	ns

DC Operating Conditions

See Notes (2), (4), (5)

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current	V_I = V_{CC} or GND	-20, -25		50	150	µA
	(non-turbo standby)	I_O = 0, *See Note (6)*	-35, -45		35	150	µA
I_{CC2}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		20	40	mA
	(non-turbo mode)	f = 1.0 MHz, *See Note (7)*	-35, -45		10	30 (40)	mA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		180	225	mA
	(turbo mode)	f = 1.0 MHz, *See Note (7)*	-35, -45		100	180 (240)	mA

Capacitance *See Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions: EP1810-20, EP1810-25 *See Note (5)*

External Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output			22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*See Note (7)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*See Note (10)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay			6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

AC Operating Conditions: EP1810-35, EP1810-45 *See Note (5)*

External Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*See Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output			40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*See Note (7)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*See Note (10)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*See Note (9)*	**Unit**
t_{IN}	Input pad and buffer delay			7		7	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		27	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay			9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		9		11	0	ns
t_{SU}	Register setup time		10		11		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		27	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP1810-20, EP1810-25, EP1810-35, EP1810-45
Industrial	(–40° C to 85° C)	EP1810-25, EP1810-40, EP1810-45 *(12)*
Military	(–55° C to 125° C)	EP1810-45 *(13)*

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20 and EP1810-25: maximum V_{PP} is 14.0 V.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For EP1810-20 and EP1810-25 clocks: t_R and t_F = 20 ns.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as four 12-bit counters.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP1810-35 and EP1810-45: Pin 19 (high-voltage pin during programming) has a maximum capacitance of 160 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) The f_{MAX} values represent the highest frequency for pipelined data.
(11) Sample-tested only for an output change of 500 mV.
(12) DC/AC specifications for EP1810-40 (industrial) are available by calling Altera's Marketing Department at (408) 984-2800.
(13) Only military-temperature-range devices are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Table 1 shows the pin-outs for the EP1810 PGA package.

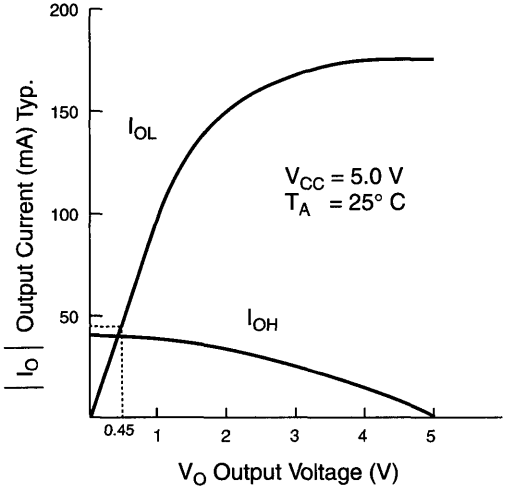
Table 1. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O

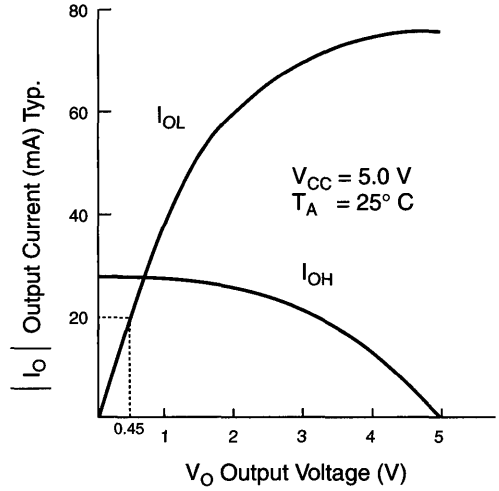
Figure 8 shows output drive characteristics for EP1810 I/O pins and typical supply current versus frequency for the EP1810 EPLD.

Figure 8. EP1810 Output Drive Characteristics and I_{CC} vs. Frequency

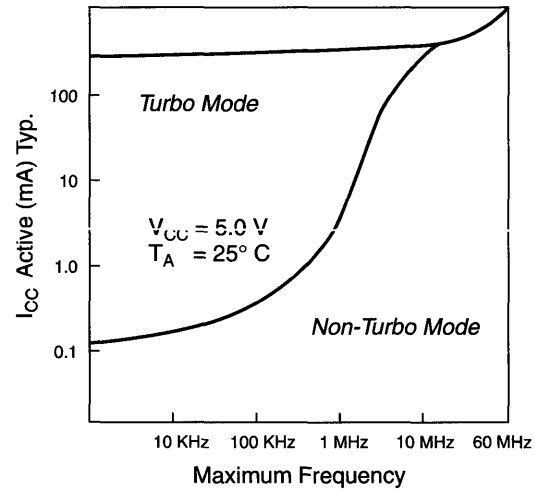
EP1810-20 and EP1810-25 EPLDs



EP1810-35 and EP1810-45 EPLDs



All EP1810 EPLDs



Features

- Highest-performance 48-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 20 ns, 25 ns, and 35 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810 and EP1830 EPLDs
- Available in 68-pin, one-time-programmable (OTP) plastic J-lead chip carrier package (PLCC)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
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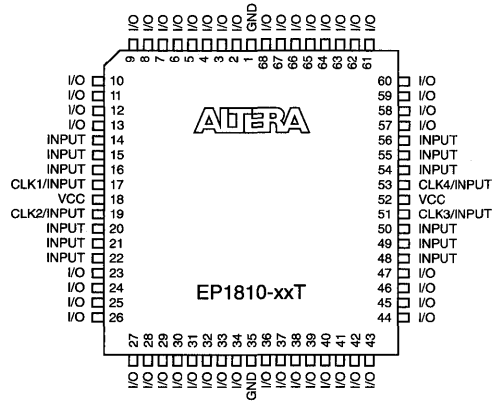
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP1810T Erasable Programmable Logic Device (EPLD) is a low-cost, high-performance version of the EP1810 device. This EPLD operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device is preset at the factory. The EP1810T EPLD is available in OTP plastic 68-pin J-lead chip carrier packages with maximum t_{PD} values of 20 ns, 25 ns, and 35 ns. See Figure 9. It contains 48 macrocells with user-configurable I/O architecture for up to 64 inputs and 48 outputs.

Figure 9. EP1810T Package Pin-Out Diagram

Package outline not drawn to scale.



J-Lead

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*See Note (2)*		50	ns
t_F	Input fall time	*See Note (2)*		50	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load	-20T, -25T		180	250	mA
			-35T		120	215	mA
I_{CC3}	V_{CC} supply current (turbo mode)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (5)*	-20T, -25T		180	250	mA
			-35T		120	215	mA

Capacitance

See Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EP1810-20T		EP1810-25T		EP1810-35T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25		35	ns
t_{PD2}	I/O input to non-registered output			22		28		40	ns
t_{SU}	Global clock setup time		13		17		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18		20	ns
t_{CH}	Global clock high time		8		10		12		ns
t_{CL}	Global clock low time		8		10		12		ns
t_{ASU}	Array clock setup time		8		10		10		ns
t_{AH}	Array clock hold time		8		10		15		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25		35	ns
t_{CNT}	Minimum global clock period			20		25		35	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	50		40		28.6		MHz
f_{MAX}	Maximum frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters			EP1810-20T		EP1810-25T		EP1810-35T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		7	ns
t_{IO}	I/O input pad and buffer delay			2		3		5	ns
t_{LAD}	Logic array delay			9		12		19	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6		9	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *See Note (8)*		6		6		9	ns
t_{SU}	Register setup time		8		10		10		ns
t_{H}	Register hold time		8		10		15		ns
t_{IC}	Array clock delay			9		12		19	ns
t_{ICS}	Global clock delay			4		5		4	ns
t_{FD}	Feedback delay			3		3		6	ns
t_{CLR}	Register clear time			9		12		24	ns

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20T and EP1810-25T: maximum V_{PP} is 14.0 V.
(2) For EP1810-20T and EP1810-25T clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as four 12-bit counters.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP1810-35T: Pin 19 (high-voltage pin during programming) has a maximum capacitance of 160 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) Sample-tested only for an output change of 500 mV.

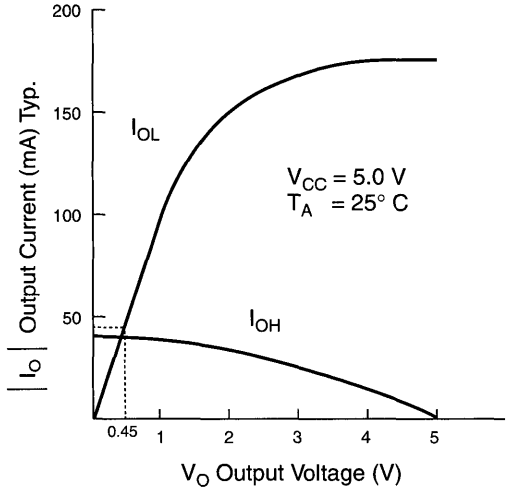
Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP1810-20T, EP1810-25T, EP1810-35T
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

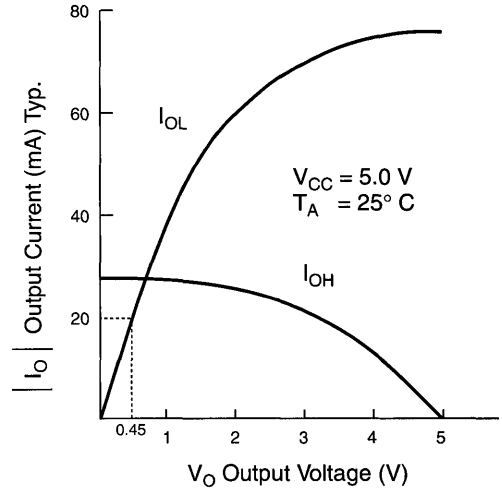
Figure 10 shows the output drive characteristics for EP1810T I/O pins and typical supply current versus frequency for the EP1810T EPLD.

Figure 10. EP1810T Output Drive Characteristics and I_{CC} vs. Frequency

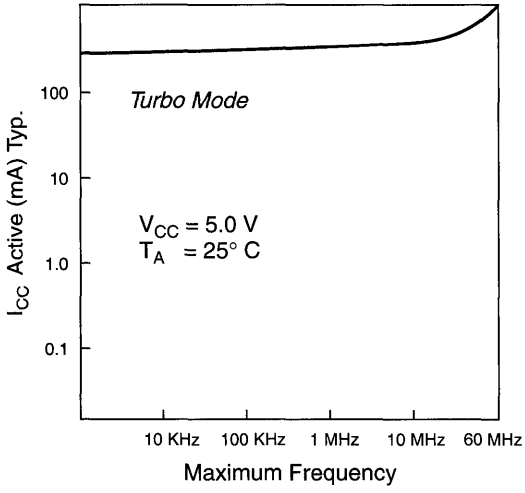
EP1810-20T and EP1810-25T EPLDs



EP1810-35T EPLD



All EP1810T EPLDs



Features

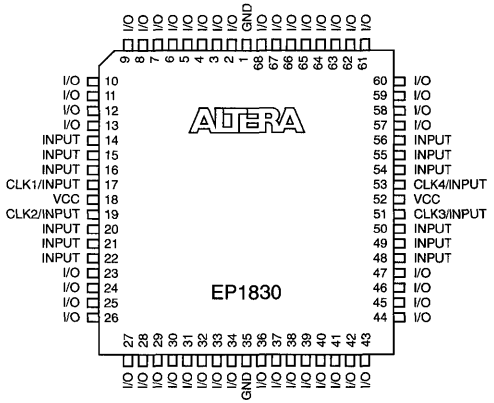
- High-performance 48-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 20 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810 and EP1810T EPLDs
- Available in 68-pin, one-time-programmable (OTP) plastic J-lead chip carrier package (PLCC)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP1830 Erasable Programmable Logic Device (EPLD) is a fast, low-power version of the EP1810 device. The EP1830 can implement four 12-bit counters at up to 50 MHz and typically consumes 20 mA when operating at 1 MHz. The EP1830 EPLD is available in OTP plastic 68-pin J-lead chip carrier packages with maximum t_{PD} values of 20 ns and 25 ns. See Figure 11.

Figure 11. EP1830 Package Pin-Out Diagram

Package outline not drawn to scale.



J-Lead

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*See Note (2)*		50	ns
t_F	Input fall time	*See Note (2)*		50	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND I_O = 0, *See Note (5)*		50	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		20	40	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		180	225	mA

Capacitance *See Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EP1830-20		EP1830-25		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output			22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Internal maximum frequency	*See Note (6)*	50		40		0	MHz
f_{MAX}	Maximum frequency	*See Note (9)*	62.5		50		0	MHz

Internal Timing Parameters			EP1830-20		EP1830-25		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay			6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (10)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

Notes to tables:

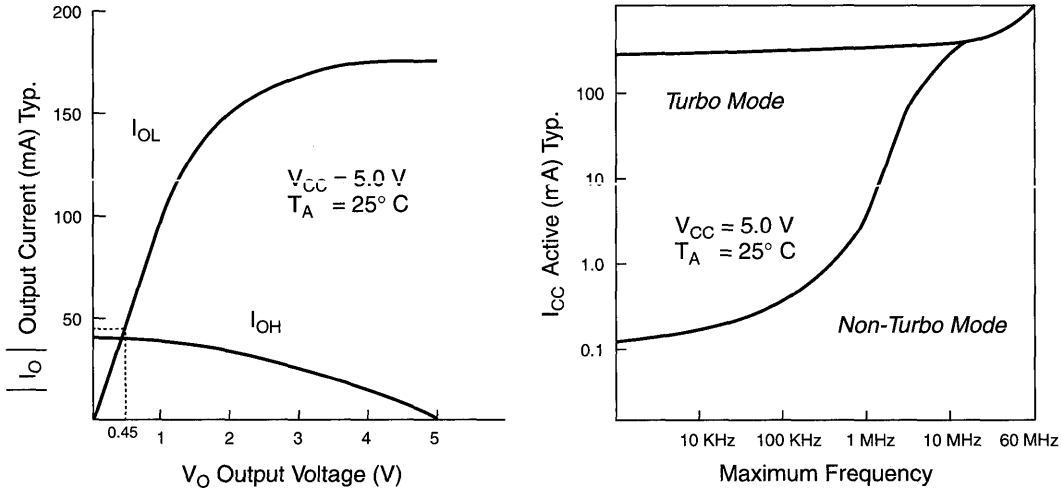
(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) When in non-turbo mode, an EPLD automatically enters standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(6) Measured with a device programmed as four 12-bit counters.
(7) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only.
(8) See "Turbo Bit" earlier in this data sheet.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) Sample-tested only for an output change of 500 mV.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP1830-20, EP1830-25, EP1830-30
Industrial	(–40° C to 85° C)	EP1830-25
Military	(–55° C to 125° C)	Consult factory

Figure 12 shows the output drive characteristics for EP1830 I/O pins and typical supply current versus frequency for the EP1830 EPLD.

Figure 12. EP1830 Output Drive Characteristics and I_{CC} vs. Frequency



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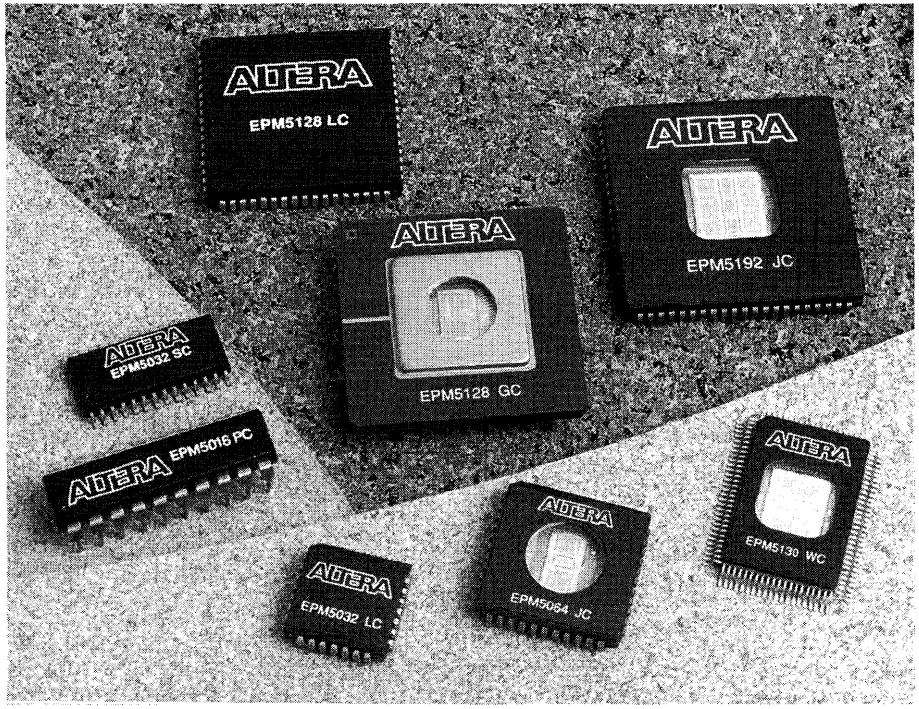
Section 3 MAX 5000 EPLDs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ALTERA
EPM5192 JC
ALTERA
EPM5128 GC
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EPM5032 SC
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EPM5016 PC
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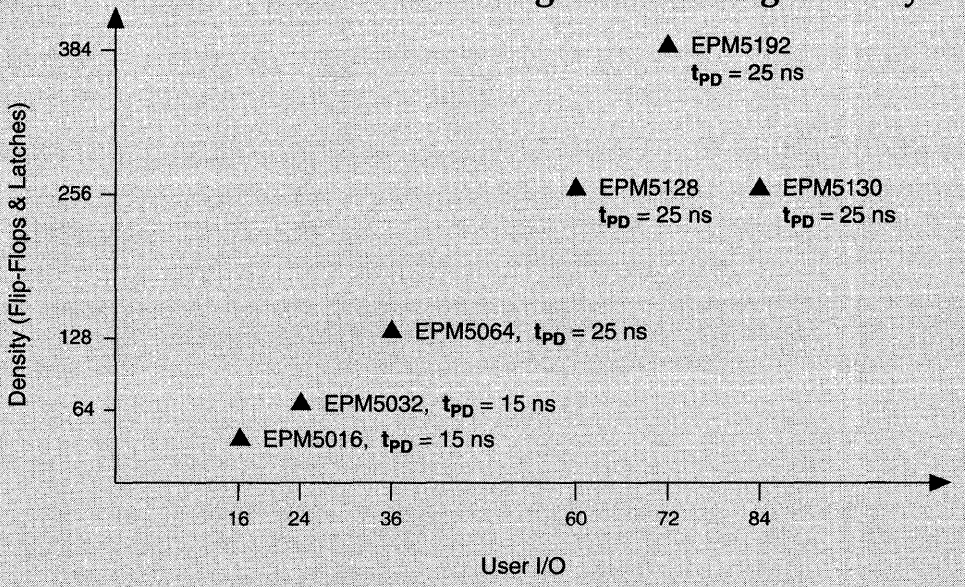
EPM5130 WC
ALTERA
EPM5064 JC
ALTERA
EPM5032 LC

MAX 5000 EPLDs

The Complete Industry-Standard Programmable Logic Family



- Altera Multiple Array MatriX (MAX) 5000 EPLDs offer the industry's most comprehensive family of programmable logic building blocks.
- Advanced MAX 5000 architecture provides the speed, ease of use, and familiarity of PAL devices with the density of programmable gate arrays.
- Modular family structure solves design tasks from fast 20-pin address decoders to 100-pin LSI custom peripherals.
- Non-volatile, reprogrammable EPROM technology aids prototype development.
- High sequential logic capacity provides up to 384 registers and latches.
- Up to 66 product terms per output ensure efficient design of complex state machines.
- All popular 7400-series functions are emulated exactly to facilitate conversion of existing CMOS and TTL designs.
- Multi-device PAL and PLA designs are easily integrated.
- MAX 5000 EPLDs provide 15-ns combinatorial delays, counter frequencies up to 100 MHz, pipelined data rates up to 100 MHz, and high-complexity designs with true system-clock rates up to 66 MHz.
- A full selection of packages is provided, including DIP, SOIC, J-lead, PGA, and QFP formats in windowed ceramic and plastic one-time-programmable versions.
- EPLDs easily convert to custom-masked silicon for very-high-volume production.
- MAX 5000 EPLDs are supported with MAX+PLUS and MAX+PLUS II PC- and workstation-based design tools offering hierarchical schematic, Altera Hardware Description Language (AHDL), and waveform design entry methods; an efficient logic synthesis-based compilation; and full timing simulation.
- Logic compilation and automatic place-and-route of 600- to 7,500-gate designs are performed in minutes.
- EDIF industry-standard workstation and third-party CAE tool interfaces are available.

EPM5016 to EPM5192 EPLDs

High-Speed, High-Density MAX 5000 Devices

September 1991, ver. 2

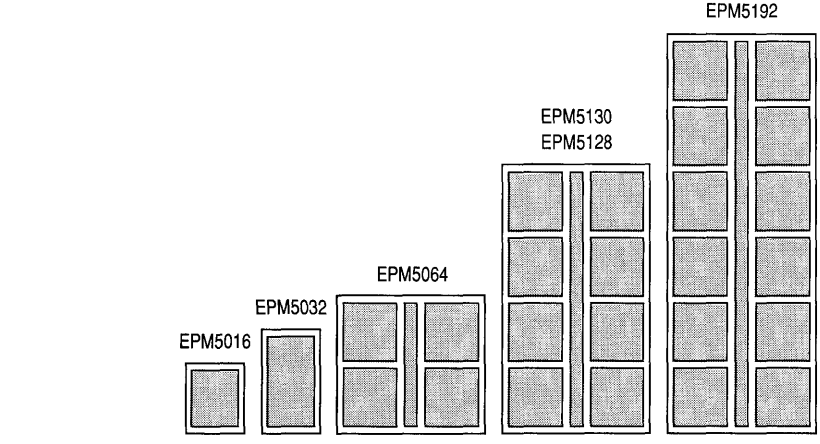
Data Sheet

Features

- Complete family of CMOS EPLDs solves design tasks ranging from fast 20-pin address decoders to 100-pin LSI custom peripherals.
- The advanced MAX 5000 architecture combines the speed, ease of use, and familiarity of PAL devices with the density of programmable gate arrays.
- MAX 5000 EPLDs provide 15-ns combinatorial delays, counter frequencies up to 100 MHz, pipelined data rates of 100 MHz, and high-complexity designs with true system clock rates up to 66 MHz.
- Available in a wide variety of packages, including DIP, SOIC, J-lead, PGA, and QFP formats in windowed ceramic and plastic one-time-programmable versions.
- MAX+PLUS and MAX+PLUS II PC- and workstation-based development tools compile large designs in minutes.
- An industry-standard EDIF interface to workstation and third-party CAE tools is available.

Figure 1 shows the MAX 5000 modular architecture.

Figure 1. MAX 5000 Modular Architecture



	EPM5016	EPM5032	EPM5064	EPM5130 / EPM5128	EPM5192
Macrocells	16	32	64	128	192
Maximum Flip-Flops	21	42	84	168	252
Maximum Latches	32	64	128	256	384
Pins	20	28	44	100/84/68	100/84

Family Highlights

- **Multiple Array MatriX (MAX) 5000 architecture solves speed, density, and design flexibility problems**
  - Advanced macrocell array provides registered, combinatorial, or flow-through latch operation.
  - Expander product-term array automatically provides additional combinatorial or registered logic.
  - Decoupled I/O block with dual feedback on I/O pins allows flexible pin utilization.
  - Programmable Interconnect Array (PIA) provides automatic 100% routing in devices with multiple LABs.
  - Each macrocell supports combinatorial and registered operation, using single or multiple clocks within a single EPLD.
- **MAX 5000 Performance**
  - Pipelined data rates up to 100 MHz
  - Counters as fast as 100 MHz
  - t_{PD} performance from 15 ns to 25 ns
  - Advanced 0.8-micron CMOS EPROM technology
- **MAX 5000 Logic Density**
  - 16- to 192-macrocell devices
  - 20- to 100-pin packages
  - 32 to 384 flip-flops and latches
  - More than 32 product terms on a single macrocell
  - Product-term expansion on any data or control path
- **MAX+PLUS & MAX+PLUS II Design Tools**
  - Design entry via unified, hierarchical schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry (waveform entry in MAX+PLUS II only)
  - Fast, automatic design processing with logic synthesis
  - Automatic design partitioning into multiple EPLDs (MAX+PLUS II only)
  - Automatic device fitting, no hand-editing needed
  - Hardware and software design verification tools
- **EDIF interface to MAX+PLUS & MAX+PLUS II provides paths to Viewlogic Systems, Valid Logic Systems, Mentor Graphics, and other workstation-based CAE tools.**

General Description

MAX 5000 Erasable Programmable Logic Devices (EPLDs) represent a revolutionary step in programmable logic: they combine innovative architecture and state-of-the-art process to offer optimum performance, logic density, flexibility, and the highest speeds and densities available in general-purpose reprogrammable logic. These EPLDs are high-speed, high-density replacements for SSI and MSI TTL and CMOS packages and conventional PLDs. For example, an EPM5192 replaces over 100 7400-series SSI and MSI TTL and CMOS packages, integrating complete subsystems into a single package, saving board area, and reducing power consumption.

The MAX 5000 EPLDs range in density from 16 to 192 macrocells. They are divided into two groups: higher-speed EPLDs (EPM5016 and EPM5032) and higher-density EPLDs (EPM5064, EPM5128, EPM5130, and EPM5192). The higher-speed devices achieve system clock frequencies of 66 MHz, and are capable of counter frequencies of 100 MHz.

Logic Array Blocks The EPM5016 and EPM5032 EPLDs have a single Logic Array Block (LAB). The EPM5064, EPM5128, EPM5130, and EPM5192 EPLDs contain multiple LABs. Each LAB contains a macrocell array, an expander product-term array, and a decoupled I/O block. Expander product terms (expanders) are unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. Thus, expressions requiring up to 66 product terms can be implemented in a single macrocell. Signals in the higher-density devices are routed between multiple LABs by a Programmable Interconnect Array (PIA) that ensures 100% routability. This multiple array architecture enables MAX 5000 EPLDs to offer the speed of smaller arrays with the integration density of larger arrays.

Modular Architecture The modular architecture of MAX 5000 EPLDs provides integration solutions over a wide range of logic densities. Migration from one type of device to another is easy. For example, the EPM5128 and EPM5130 EPLDs have the same logic capacity, but have packages optimized to handle different I/O requirements. Over the entire family, a wide range of packaging options for both through-hole and surface-mount applications is available. Plastic one-time-programmable (OTP) packages are available for economical volume production.

Logic Design Entry Logic designs are created and programmed into MAX 5000 EPLDs with the MAX+PLUS and MAX+PLUS II development systems. These complete CAE systems offer hierarchical design entry tools, automatic design compilation and fitting, timing simulation, and device programming. The MAX+PLUS and MAX+PLUS II Compilers feature advanced logic synthesis algorithms, allowing designs to be entered in a variety of high-level formats while ensuring the most efficient use of EPLD resources. The combination of a flexible architecture and advanced CAE tools ensures rapid design cycles so that a design may go from conception to completion in single day. Interfaces to third-party tools are also available to allow design entry and logic simulation on a variety of workstation platforms.

Functional Description

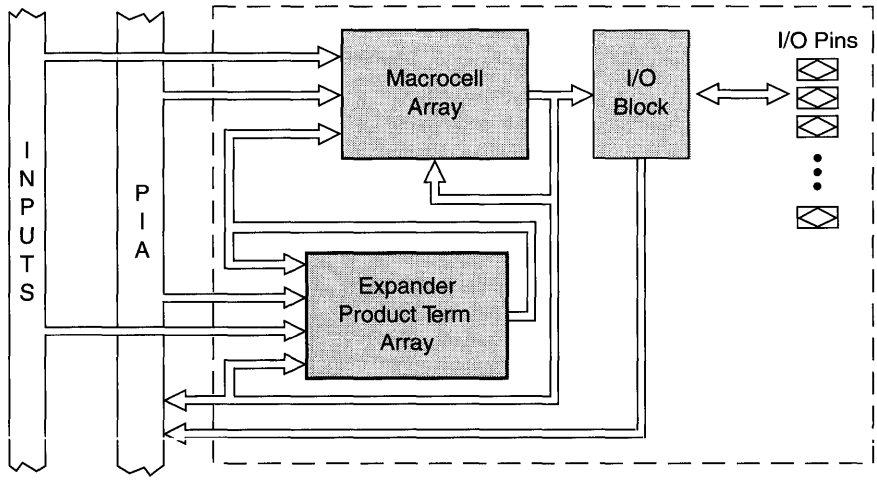
MAX 5000 EPLDs use CMOS EPROM cells to configure logic functions within the devices. The device architecture is user-configurable to accommodate a variety of independent logic functions, and the EPLDs can be erased for quick and efficient iterations during design development and debug cycles.

Logic Array Block

MAX 5000 EPLDs contain from 1 to 12 Logic Array Blocks (LABs). Each LAB, shown in Figure 2, consists of a macrocell array, an expander product-term array, and an I/O control block. (The number of macrocells and expanders in the arrays varies with each device.) Macrocells are the primary resource for logic implementation, but if needed, expanders can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms. Flexible macrocells and allocable expanders facilitate variable product-term designs without the waste associated with fixed product-term architectures. Thus, PAL or PLA devices are easily integrated into MAX 5000 EPLDs. The outputs of the macrocells feed the decoupled I/O block, which consists of a group of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192 EPLDs, multiple LABs are connected by a Programmable Interconnect Array (PIA).

Figure 2. Logic Array Block

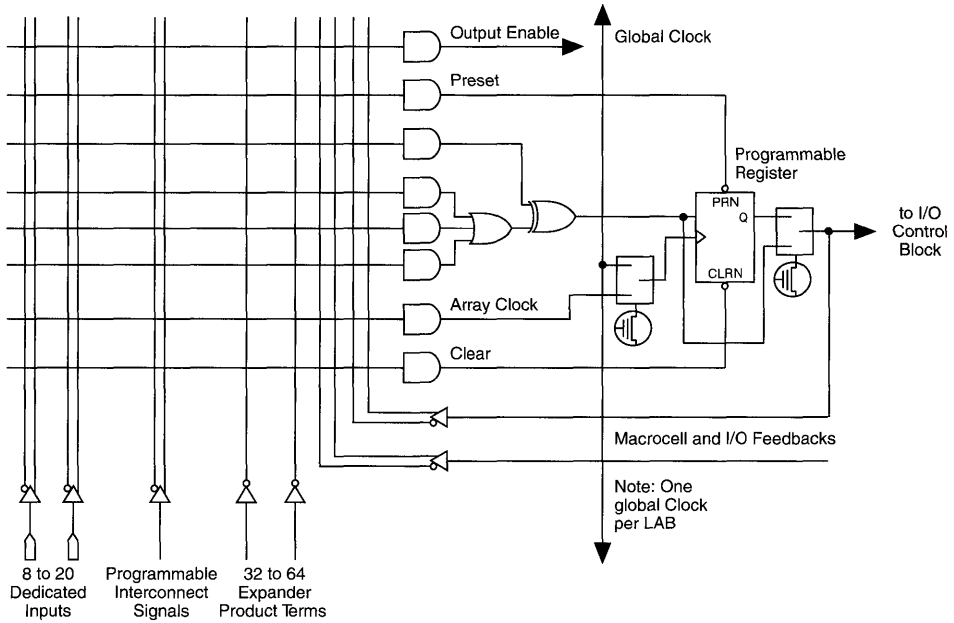
The LAB consists of a macrocell array, an expander product-term array, and a decoupled I/O block. The flexibility of the LAB ensures high speeds and efficient device utilization.



Macrocells

The MAX 5000 macrocell, shown in Figure 3, consists of a programmable logic array and an independently configurable register. This register may be programmed for D, T, JK, or SR operation, as a flow-through latch, or bypassed for purely combinatorial operation. Combinatorial logic is implemented in the programmable logic array, which consists of three product terms ORed together that feed one input of an XOR gate. The second input to the XOR gate is also controlled by a product term that makes it possible to implement active-high or active-low logic. The XOR gate is also used for complex XOR arithmetic logic functions and for De Morgan's inversion to reduce the number of product terms. The output of the XOR gate feeds the programmable register, or bypasses it for purely combinatorial operation. The logic array ensures high speed while

Figure 3. MAX 5000 Macrocell



eliminating inefficient, unused product terms. Also, expanders can be allocated to enhance the capability of the logic array.

Additional product terms, called secondary product terms, are used for Output Enable, Preset, Clear, and Clock logic. Preset and Clear product terms drive the active-low asynchronous Preset and asynchronous Clear inputs to the configurable flip-flop. The Clock product term allows each register to have an independent Clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin may use the Output Enable product term to control the active-high tri-state buffer in the I/O control block. These secondary product terms allow 7400-series TTL functions to be emulated exactly.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device. All macrocell outputs are globally routed within a LAB and also feed the PIA to provide efficient routing of signal-intensive designs.

Clock Options

Each LAB has two clocking modes: array (asynchronous) and global (synchronous). During array clocking, each flip-flop is clocked by a product term. Thus, any input or internal logic may be used as a clock. Systems that require multiple clocks are easily integrated into MAX 5000 EPLDs. Array

clocking also allows each flip-flop to be configured for positive- or negative-edge-triggered operation, giving the macrocell a high degree of flexibility.

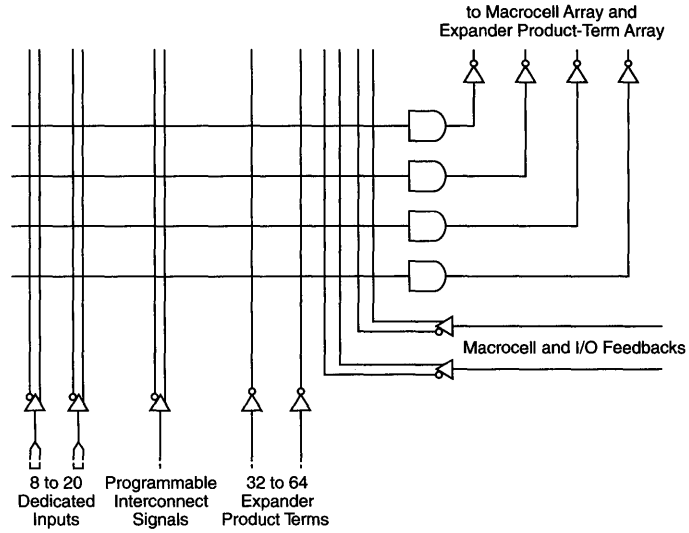
Global clocking is provided by a dedicated Clock signal (CLK). This direct connection provides enhanced clock-to-output delay times. Since each LAB has one global clock, all flip-flop clocks within it are positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global clock, it may be used as a dedicated input.

Expander Product Terms

The expander product-term array (Figure 4) contains unallocated, inverted product terms that enhance the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs for MAX 5000 EPLDs.

Figure 4. Expander Product Terms

Expander product terms are unallocated logic that can be used and shared by all macrocells in an LAB. Sharing allows efficient integration of complex combinatorial functions.



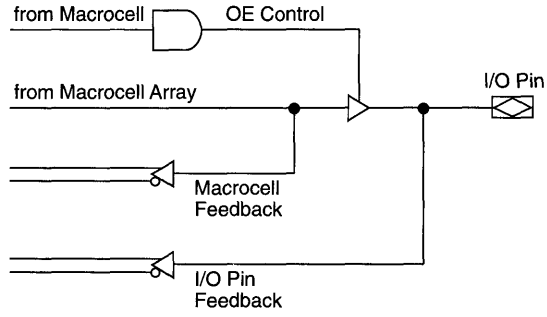
Expanders are fed by all signals in the LAB. One expander may feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flip-flops or latches.

I/O Control Block

Each LAB has an I/O control block (Figure 5) that consists of a user-configurable I/O control function for each I/O pin. The I/O control block is fed by the macrocell array. The tri-state buffer is controlled by a dedicated macrocell product term, and drives the I/O pad.

Figure 5. I/O Control Block

The decoupled I/O control block features dual feedback to maximize use of device pins.



Each MAX 5000 EPLD has dual feedback—a feedback path both before and after the tri-state buffer—for every I/O pin. The tri-state buffer decouples the I/O pins from the macrocells so that all registers within the LAB can be "buried." Thus, I/O pins can be configured as dedicated input, output, or bidirectional pins. In multi-LAB devices, I/O pins feed the PIA.

Programmable Interconnect Array

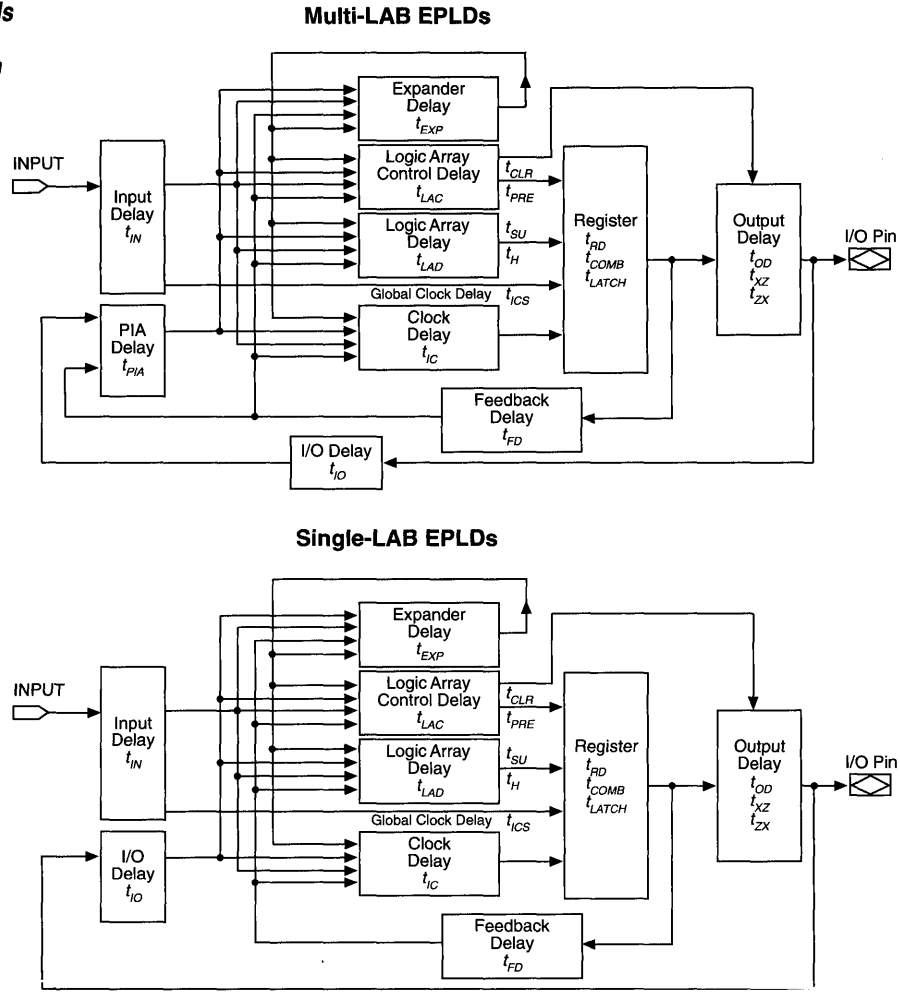
The higher-density MAX 5000 devices (EPM5064, EPM5128, EPM5130, and EPM5192) use a Programmable Interconnect Array (PIA) to route signals between the various LABs. The PIA routes only the signals required for implementing logic in an LAB, and is fed by all macrocell feedbacks and all I/O pin feedbacks. Unlike channel routing in masked or programmable gate arrays—where routing delays are variable and path-dependent—the PIA has a fixed delay. Because the PIA eliminates skew between signals, timing performance is easy to predict.

Timing Model

Timing within MAX 5000 EPLDs is easily determined with MAX+PLUS and MAX+PLUS II software or with the models shown in Figure 6. MAX 5000 EPLDs have fixed internal delays, which allow the user to determine the worst-case timing for any design. For complete timing information, both MAX+PLUS and MAX+PLUS II software provide point-to-point delay prediction, full timing simulation, and detailed timing analysis.

Figure 6. Timing Models

Design performance can be predicted with these timing models and the device performance specifications.



The timing models shown in Figure 6 can be used together with the internal timing parameters for a particular EPLD to derive timing information. External timing parameters are derived from a sum of internal parameters and represent pin-to-pin timing delays. Figure 7 shows the internal timing waveforms for these devices. Refer to *Application Brief 75* for further information on MAX 5000 EPLD timing.

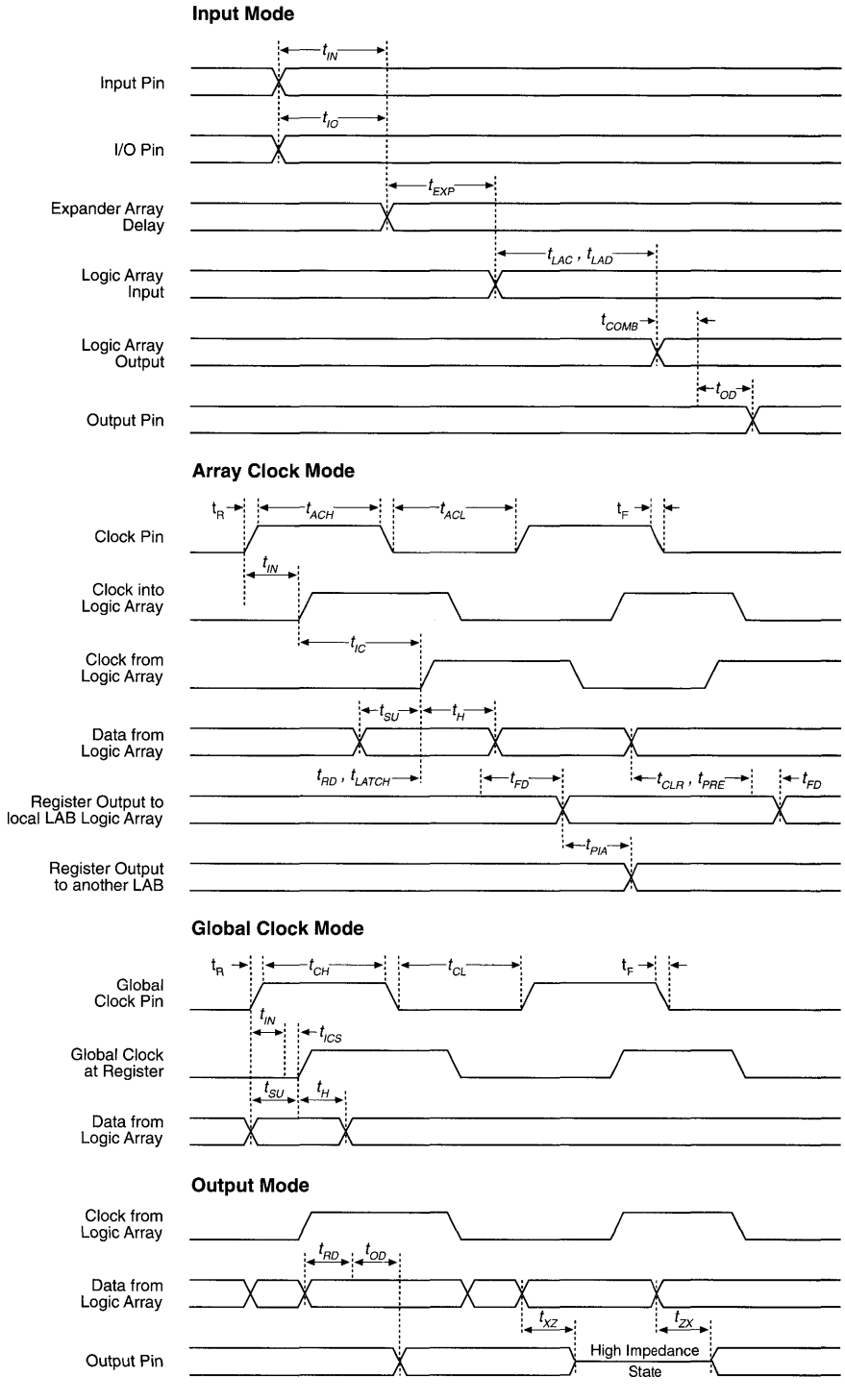
Design Security

MAX 5000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset by erasing the EPLD.

Figure 7. Switching Waveforms

In multi-LAB EPLDs, I/O pins used as inputs can traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



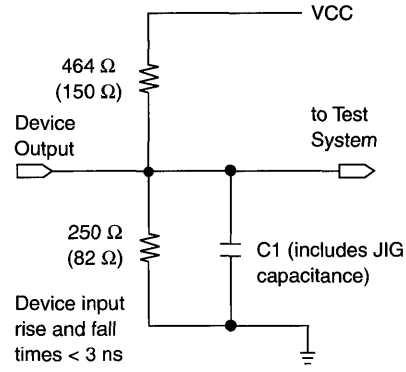
Functional Testing

MAX 5000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are performed under the conditions shown in Figure 8.

Figure 8. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable input noise immunity.

Note: Numbers in parentheses are for the EPM5016 EPLD.



Test programs can be used and then erased during early stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices. EPLDs also contain on-board logic test circuitry to allow verification of function and AC specifications of devices in windowless packages.

MAX+PLUS & MAX+PLUS II Development Systems

The MAX+PLUS and MAX+PLUS II development systems are unified CAE systems for integrating designs into MAX 5000 EPLDs. Table 1 summarizes the features available in each MAX+PLUS and MAX+PLUS II package.

Designs can be entered as logic schematics with the Graphic Editor or as state machines, truth tables, and Boolean equations with the Altera Hardware Description Language (AHDL); waveform design entry is also available with MAX+PLUS II software. Logic synthesis and minimization optimize the logic of a design. Automatic design partitioning into multiple EPLDs is also available with MAX+PLUS II software. Errors in a design are automatically located and highlighted in the original design file. Design verification and timing analysis are performed with built-in timing simulators, timing analyzers, and delay prediction.

Table 1. MAX 5000 EPLD Development Systems & Software Packages

	Design Entry					Design Compilation & Verification							
MAX+PLUS II:	Schematic Capture	AHDL	Waveform Entry	State Machine Entry	Boolean Equation Entry	Functional Simulation	Timing Simulation	Timing Analysis	Waveform Editing	Design Partitioning	Multi-EPLD Simulation	EDIF Interface	Programming Hardware
PLDS-HPS	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
PLS-HPS	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	
PLS-OS		✔		✔	✔					✔		✔	
PLS-ES		✔		✔	✔								
PLS-WS/HP		✔		✔	✔					✔		✔	
PLS-WS/SN		✔		✔	✔					✔		✔	
MAX+PLUS:													
PLDS-MAX	✔	✔		✔	✔		✔	✔	✔				✔
PLS-MAX	✔	✔		✔	✔		✔	✔	✔				

Hosted on IBM PS/2, PC-AT, or compatible machines, and workstations (e.g., HP/Apollo and Sun), MAX+PLUS and MAX+PLUS II give designers the tools to quickly and efficiently create complex logic designs. Further details about the MAX+PLUS and MAX+PLUS II development systems are available in the *PLDS-MAX & PLS-MAX*, *PLS-WS/HP*, *PLS-WS/SN*, and *PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES* data sheets in this data book.

Device Programming

MAX 5000 EPLDs can be programmed on an IBM PS/2, PC-AT, or compatible computer with an Altera Logic Programmer card, the Master Programming Unit (MPU), and an appropriate device adapter. These items are included in the complete PLDS-MAX and PLDS-HPS Development Systems or may be purchased separately. MAX 5000 EPLDs can also be programmed with third-party hardware (see the *Third-Party Development & Programming Support Data Sheet* in this data book). Contact Altera or your programming equipment manufacturer for more information.

Notes:

Features

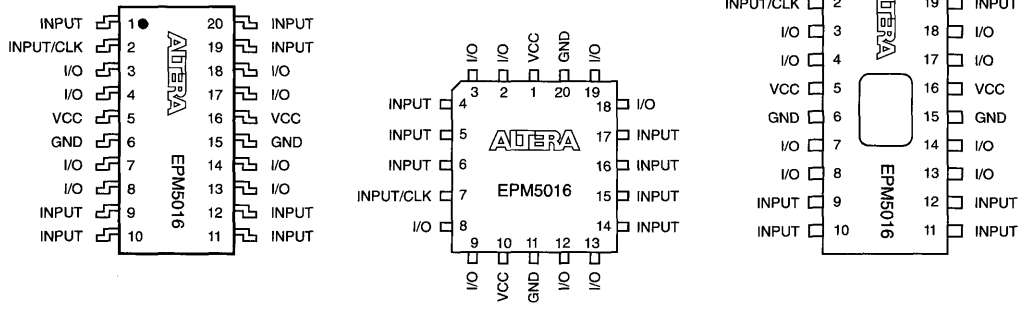
- High-speed 20-pin DIP, J-lead, or SOIC single-LAB MAX 5000 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- 16 individually configurable macrocells
- 32 expander product terms (expanders) that allow 34 product terms in a single macrocell
- Up to 21 flip-flops or 32 latches
- Up to 10 input latches that can be constructed with cross-coupled expanders
- 24-mA output drivers to allow direct interfacing to system buses
- Programmable I/O architecture allowing up to 16 inputs and 8 outputs
- Available in 20-pin windowed ceramic DIP package, or plastic one-time-programmable (OTP) DIP, J-lead (PLCC), and 300-mil SOIC packages

General Description

The Altera EPM5016 EPLD is a Multiple Array MatriX (MAX) 5000-family CMOS EPLD that is optimized for speed. It can integrate multiple SSI and MSI TTL and 74HC devices. In addition, it can replace any 20-pin PAL or PLA device with logic left over for further integration. See Figure 9.

Figure 9. EPM5016 Package Pin-Out Diagrams

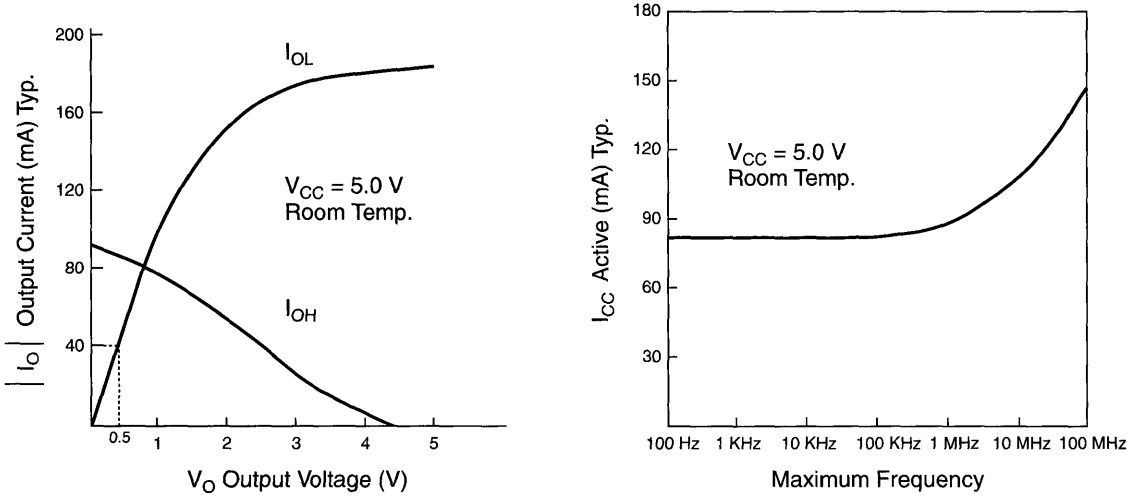
Package outlines not drawn to scale.



SOIC J-Lead DIP

Figure 10 shows output drive characteristics of EPM5016 I/O pins and typical supply current versus frequency for the EPM5016 EPLD.

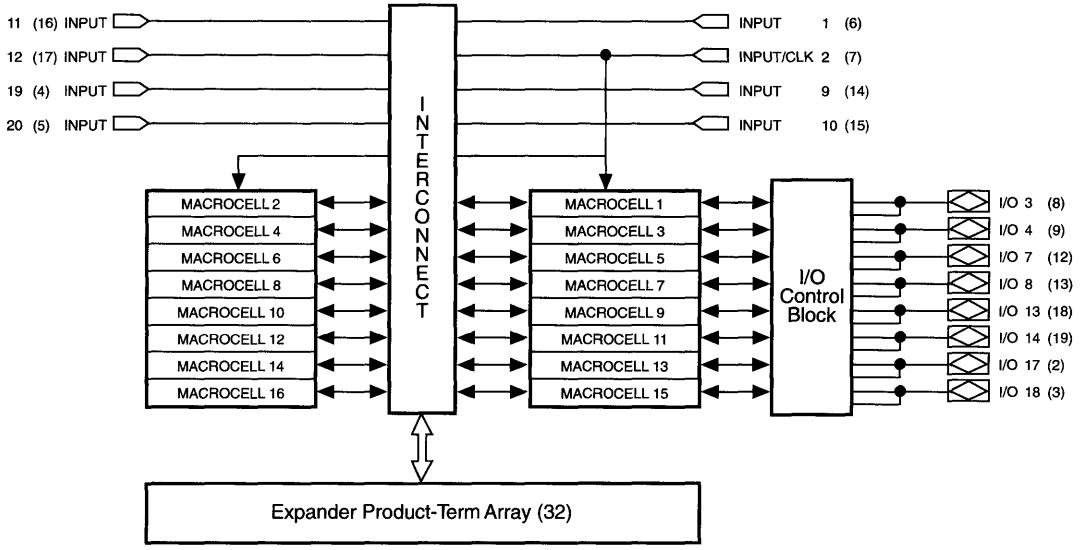
Figure 10. EPM5016 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5016 EPLD contains 16 macrocells (see Figure 11). The expander product-term array for the EPM5016 EPLD contains 32 expanders. The I/O control block contains 8 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility.

Figure 11. EPM5016 Block Diagram

The EPM5016 has 16 macrocells and 32 expanders. Numbers in parentheses are for the PLCC package.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			200	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		80	110 (150)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		85	115 (175)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20	ns
t_{PD2}	I/O input to non-registered output			15		17		20	ns
t_{SU}	Global clock setup time		6		8		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		9		11		13	ns
t_{CH}	Global clock high time		5		6		8		ns
t_{CL}	Global clock low time		5		6		8		ns
t_{ASU}	Array clock setup time		5		7		9		ns
t_{AH}	Array clock hold time		5		7		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		17		20	ns
t_{ACH}	Array clock high time	*See Note (6)*	4		5		7		ns
t_{ACL}	Array clock low time		6		7		9		ns
t_{CNT}	Minimum global clock period			10		12		16	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	100		83.3		62.5		MHz
t_{ACNT}	Minimum array clock period			10		12		16	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	100		83.3		62.5		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	100		83.3		62.5		MHz

Internal Timing Parameters *See Note (8)*			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		5		5	ns
t_{IO}	I/O input pad and buffer delay			4		5		5	ns
t_{EXP}	Expander array delay			5		8		10	ns
t_{LAD}	Logic array delay			6		7		9	ns
t_{LAC}	Logic control array delay			4		5		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5	ns
t_{ZX}	Output buffer enable delay			7		7		8	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8	ns
t_{SU}	Register setup time		2		5		8		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		6		8		9		ns
t_{IC}	Array clock delay			6		6		8	ns
t_{ICS}	Global clock delay			0		1		2	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			3		6		6	ns
t_{CLR}	Register clear time			3		6		6	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as a 16-bit counter.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5016-15, EPM5016-17, EPM5016-20
Industrial	(–40° C to 85° C)	EPM5016-20
Military	(–55° C to 125° C)	Consult factory

Features

- High-speed 28-pin DIP, J-lead, or SOIC single-LAB MAX 5000 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 76 MHz
  - Pipelined data rates up to 83 MHz
- 32 individually configurable macrocells
- 64 expander product terms (expanders) that allow 66 product terms on a single macrocell
- Up to 42 flip-flops or 64 latches
- Up to 21 input latches that can be constructed with cross-coupled expanders
- Programmable I/O architecture allowing up to 24 inputs and 16 outputs
- Available in 28-pin windowed ceramic or plastic one-time-programmable (OTP) DIP and J-lead packages, as well as plastic OTP 300-mil SOIC packages

General Description

The Altera EPM5032 EPLD is a Multiple Array MatriX (MAX) 5000-family CMOS EPLD optimized for speed. It can integrate multiple SSI and MSI TTL and 74HC devices. In addition, it can replace multiple 20-pin PAL or PLA devices with logic left over for further integration. See Figure 12.

Figure 12. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale.

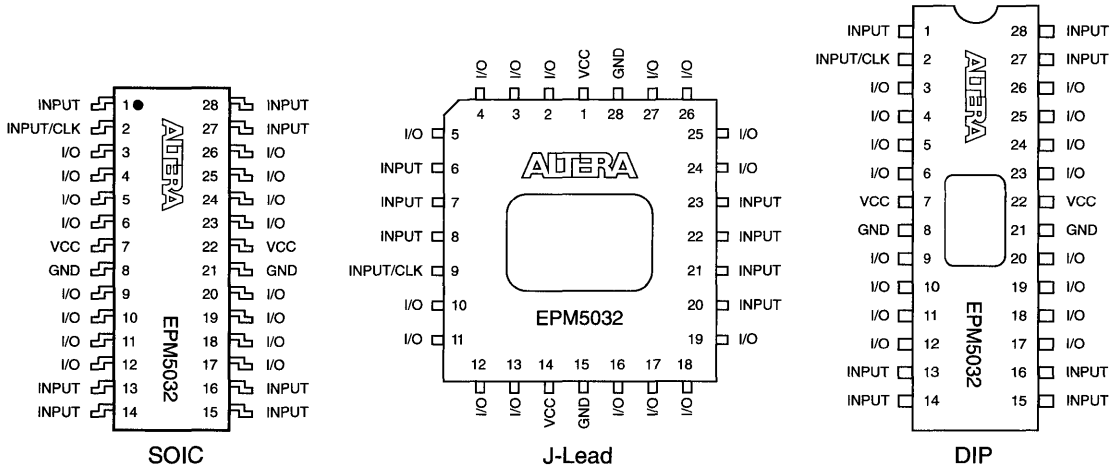
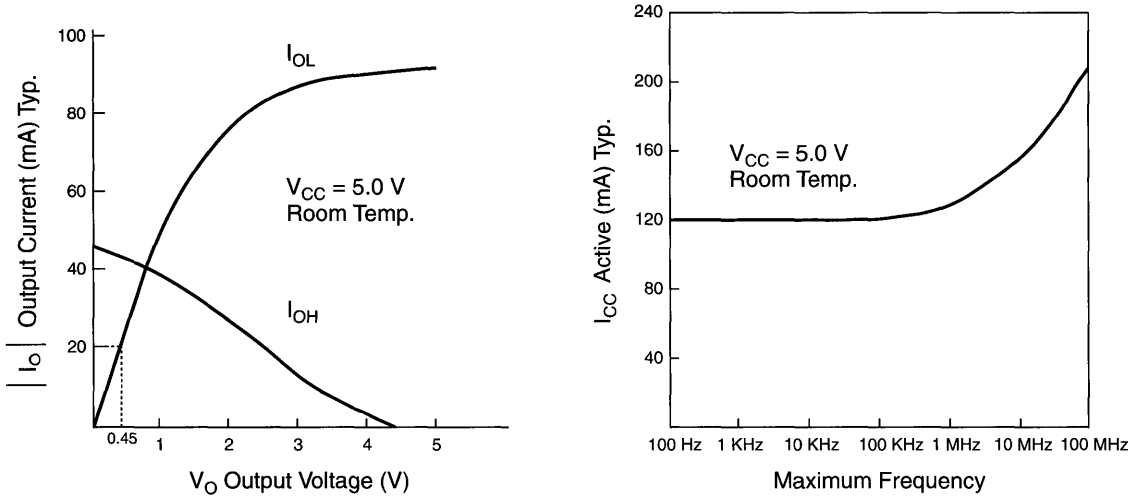


Figure 13 shows output drive characteristics of EPM5032 I/O pins and typical supply current versus frequency for the EPM5032 EPLD.

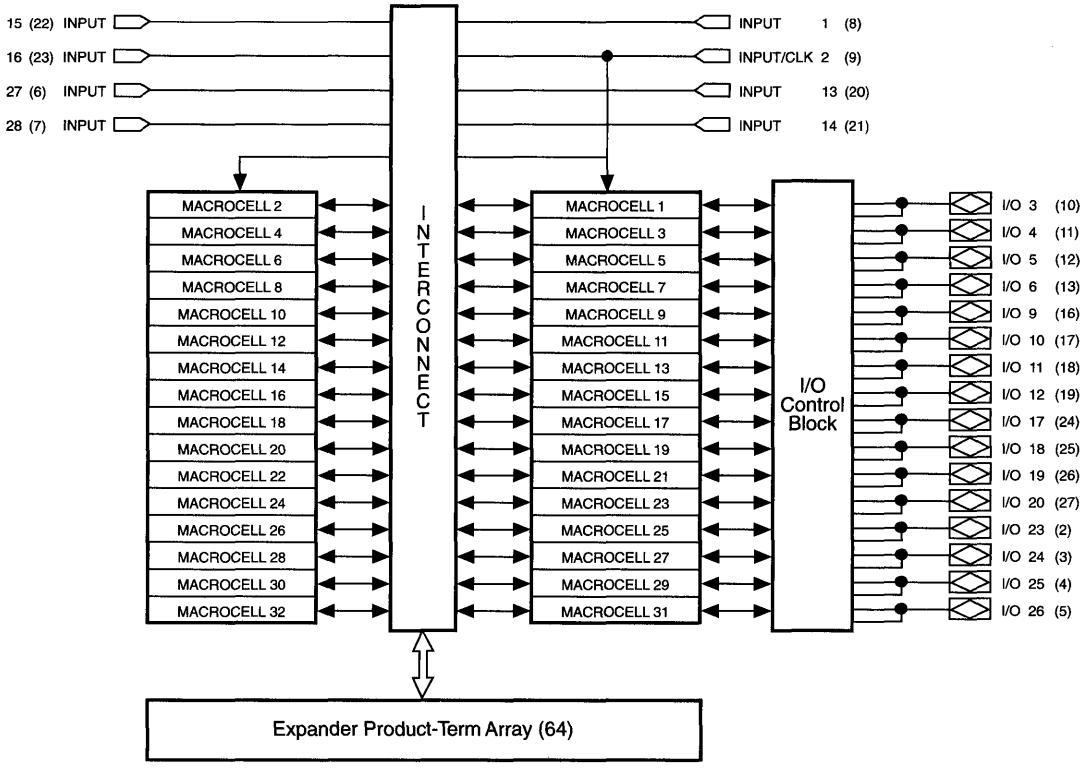
Figure 13. EPM5032 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5032 EPLD contains 32 macrocells (see Figure 14). The EPM5032 expander product-term array contains 64 expanders. The I/O control block contains 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility.

Figure 14. EPM5032 Block Diagram

The EPM5032 has 32 macrocells and 64 expanders. Numbers in parentheses are for J-lead packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		120	150 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		125	155 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{PD2}	I/O input to non-registered output			15		17		20		25	ns
t_{SU}	Global clock setup time		9		10		12		15		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		10		12		15	ns
t_{CH}	Global clock high time		6		6		7		8		ns
t_{CL}	Global clock low time		6		6		7		8		ns
t_{ASU}	Array clock setup time		7		8		9		12		ns
t_{AH}	Array clock hold time		7		8		9		12		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		20		25	ns
t_{ACH}	Array clock high time	*See Note (6)*	6		6		7		9		ns
t_{ACL}	Array clock low time		7		8		9		11		ns
t_{CNT}	Minimum global clock period			13		14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	76.9		71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			13		14		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	76.9		71.4		62.5		50		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	83.3		83.3		71.4		62.5		MHz

Internal Timing Parameters *See Note (8)*			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		5		5		7	ns
t_{IO}	I/O input pad and buffer delay			4		5		5		7	ns
t_{EXP}	Expander array delay			8		8		10		15	ns
t_{LAD}	Logic array delay			6		7		9		10	ns
t_{LAC}	Logic control array delay			4		5		7		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5		5	ns
t_{ZX}	Output buffer enable delay			7		7		8		11	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8		11	ns
t_{SU}	Register setup time		5		5		5		8		ns
t_{LATCH}	Flow-through latch delay			1		1		1		3	ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		3	ns
t_{H}	Register hold time		6		6		9		12		ns
t_{IC}	Array clock delay			6		8		8		10	ns
t_{ICS}	Global clock delay			1		1		2		3	ns
t_{FD}	Feedback delay			1		1		1		1	ns
t_{PRE}	Register preset time			5		5		6		9	ns
t_{CLR}	Register clear time			5		5		6		9	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 32-bit counter.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5032-15, EPM5032-17, EPM5032-20, EPM5032-25
Industrial	(–40° C to 85° C)	EPM5032-25
Military	(–55° C to 125° C)	EPM5032-25

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Features

- High-density 64-macrocell general-purpose MAX 5000 EPLD
- 128 shareable expander product terms providing flexible logic expansion
  - Over 32 product terms in a single macrocell
  - 64 additional latches provided by cross-coupled expanders
- Multi-LAB MAX architecture with t_{PD} = 25 ns, counter frequencies up to 50 MHz, and pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 36 inputs and 28 outputs
- 44-pin J-lead package that easily integrates 10 standard PALs in 1/2 square inch of board space; windowed ceramic or plastic one-time-programmable packages for volume production

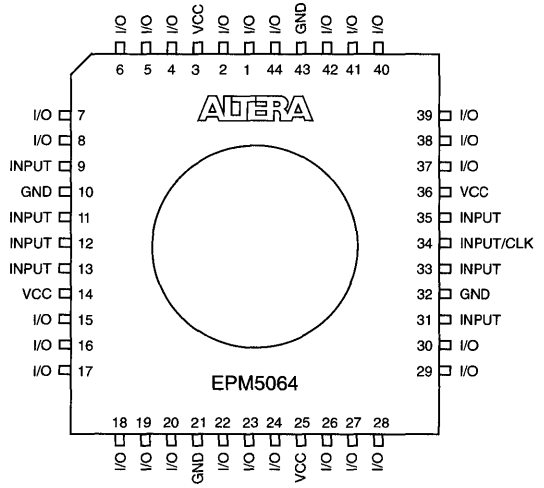
General Description

The Altera EPM5064 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that serves as a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. In addition, it can integrate multiple 20- and 24-pin low-density PLDs. For example, the EPM5064 EPLD can integrate the logic contained in over 10 standard 20-pin PALs.

Figure 15 shows the package pin-out for the EPM5064 J-lead package. This package occupies only 1/2 square inch of board space.

Figure 15. EPM5064 Package Pin-Out Diagram

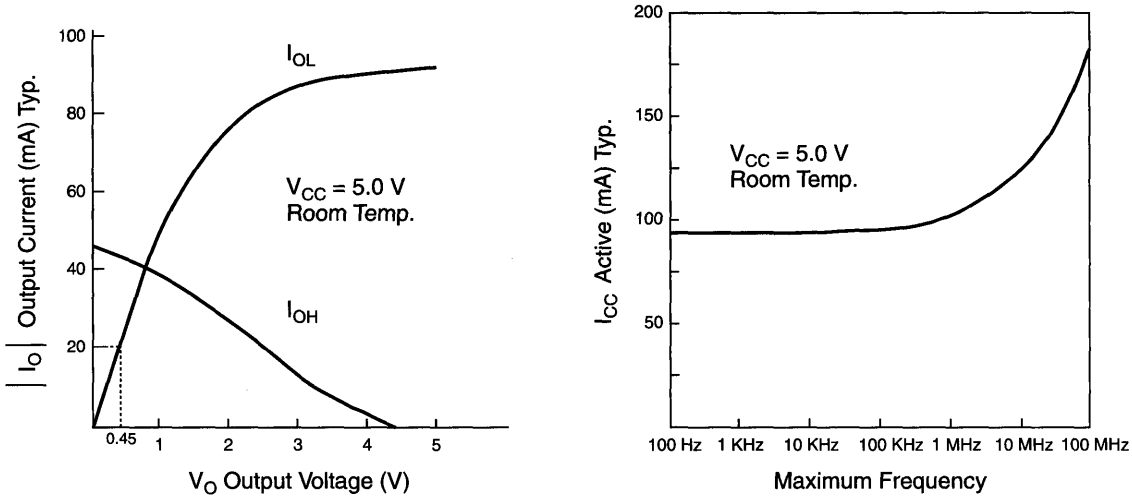
Package outline not drawn to scale.



J-Lead

Figure 16 shows output drive characteristics of EPM5064 I/O pins and typical supply current versus frequency for the EPM5064 EPLD. The high integration density of the EPM5064 EPLD often greatly reduces system power requirements.

Figure 16. EPM5064 Output Drive Characteristics and I_{CC} vs. Frequency

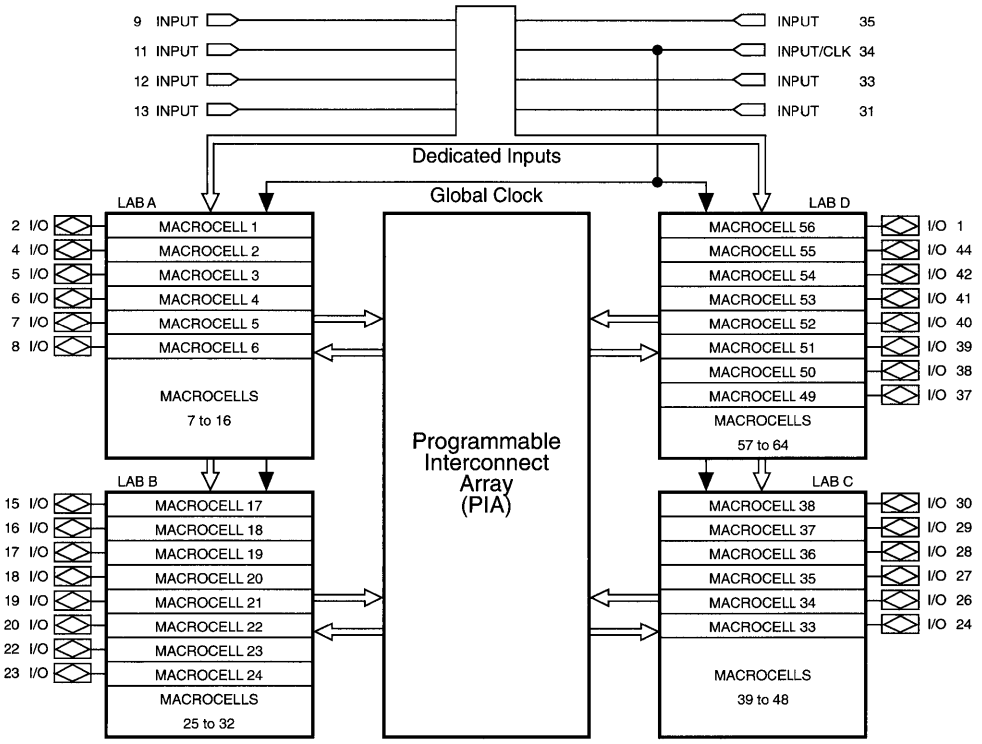


The EPM5064 consists of 64 macrocells equally divided into 4 Logic Array Blocks (LABs) that each contain 16 macrocells (see Figure 17). Each LAB also contains 32 expander product terms. The flexibility of the LABs allows easy integration of any common PLD.

The EPM5064 EPLD has 8 dedicated input pins, one of which can be used as a global system clock that provides enhanced clock-to-output delays. The device has 28 I/O pins that can be configured for input, output, or bidirectional data flow. The I/O pins feature dual-feedback to allow any macrocell to be buried. Two of the LABs have 8 I/O pins (ensuring high speed for 8-bit bus functions) and the other two LABs have 6 I/O pins.

Figure 17. EPM5064 Block Diagram

The EPM5064 EPLD has 64 macrocells divided into 4 Logic Array Blocks.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		90	125 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		95	135 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		12		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5064-1, EPM5064-2, EPM5064
Industrial	(–40° C to 85° C)	EPM5064
Military	(–55° C to 125° C)	EPM5064

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Features

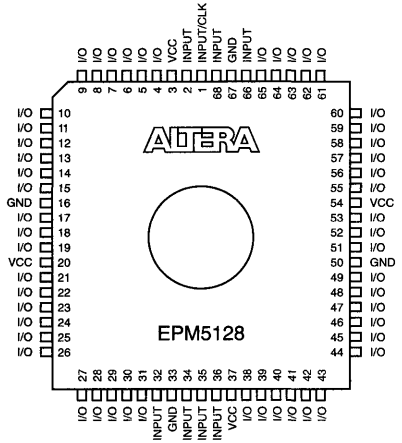
- High-density 128-macrocell general-purpose MAX 5000 EPLD
- 256 shareable expander product terms that allow over 32 product terms in a single macrocell
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in 68-pin windowed ceramic or plastic one-time-programmable (OTP) J-lead packages and in 68-pin windowed ceramic PGA packages

General Description

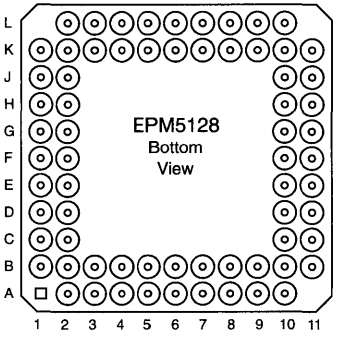
The Altera EPM5128 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. For example, a 74161 counter uses only 3% of the EPM5128 EPLD. The EPM5128 EPLD can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs. Figure 18 shows the J-lead and PGA package diagrams for the EPM5128 EPLD.

Figure 18. EPM5128 Package Pin-Out Diagrams

See Table 2 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.



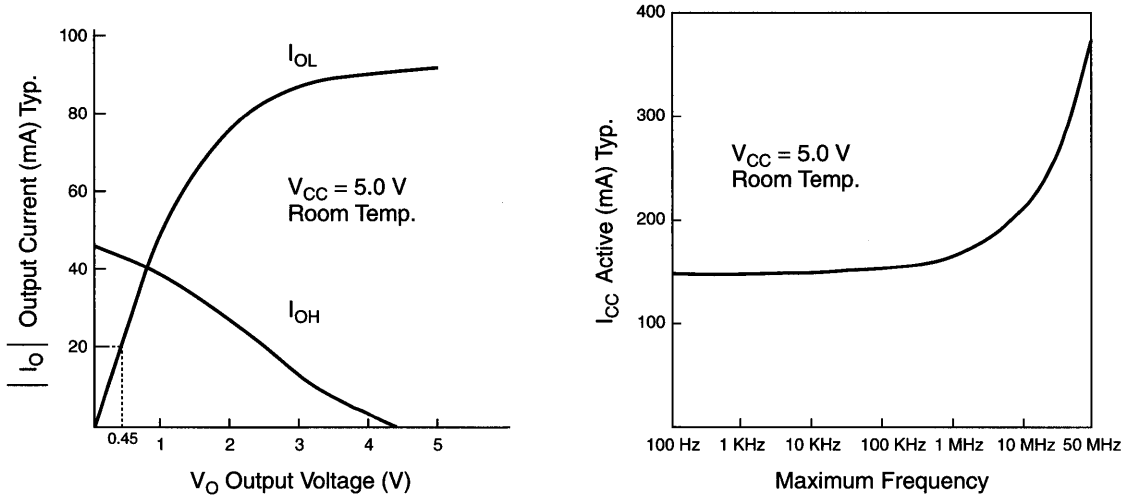
J-Lead



PGA

Figure 19 shows output drive characteristics of EPM5128 I/O pins and typical supply current versus frequency for the EPM5128 EPLD.

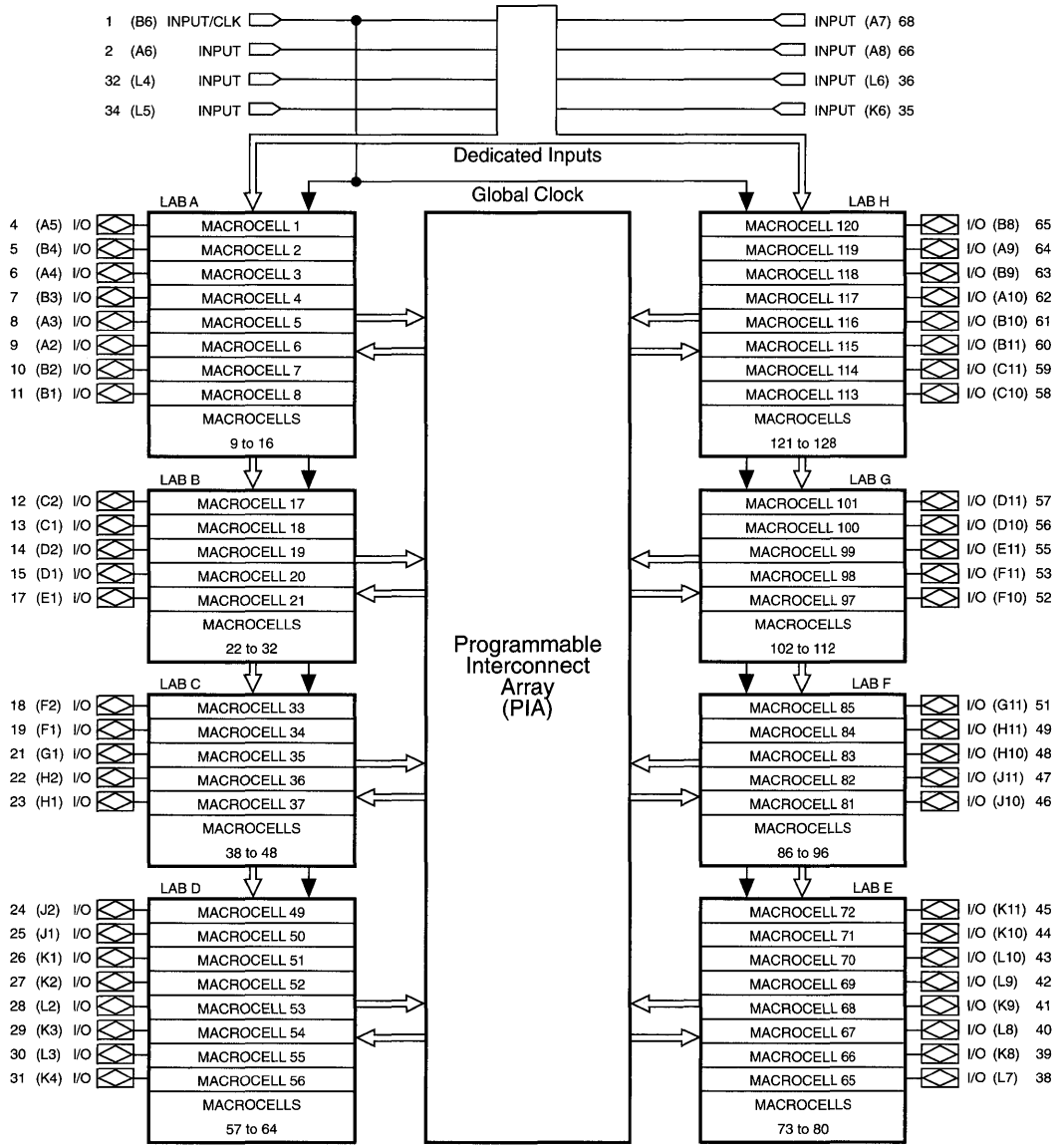
Figure 19. EPM5128 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5128 EPLD consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) that each contain 16 macrocells (see Figure 20). Each LAB also contains 32 expander product terms. The EPM5128 EPLD has 8 dedicated input pins, one of which may be used as a global (synchronous) system clock. The EPM5128 device contains 52 I/O pins that can be configured for input, output, or bidirectional data flow. Four of the LABs have 8 I/O pins, and the other 4 have 5 I/O pins.

Figure 20. EPM5128 Block Diagram

Numbers in parentheses are for PGA packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the maximum frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5128-1, EPM5128-2, EPM5128
Industrial	(–40° C to 85° C)	EPM5128
Military	(–55° C to 125° C)	EPM5128

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Table 2 shows the pin-outs for the EPM5128 PGA package.

Table 2. EPM5128 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	I/O	K4	I/O
A3	I/O	B10	I/O	F11	I/O	K5	GND
A4	I/O	B11	I/O	G1	I/O	K6	INPUT
A5	I/O	C1	I/O	G2	VCC	K7	VCC
A6	INPUT	C2	I/O	G10	GND	K8	I/O
A7	INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	INPUT
B4	I/O	E2	GND	J10	I/O	L6	INPUT
B5	VCC	E10	VCC	J11	I/O	L7	I/O
B6	INPUT/CLK	E11	I/O	K1	I/O	L8	I/O
B7	GND	F1	I/O	K2	I/O	L9	I/O
B8	I/O	F2	I/O	K3	I/O	L10	I/O

Features

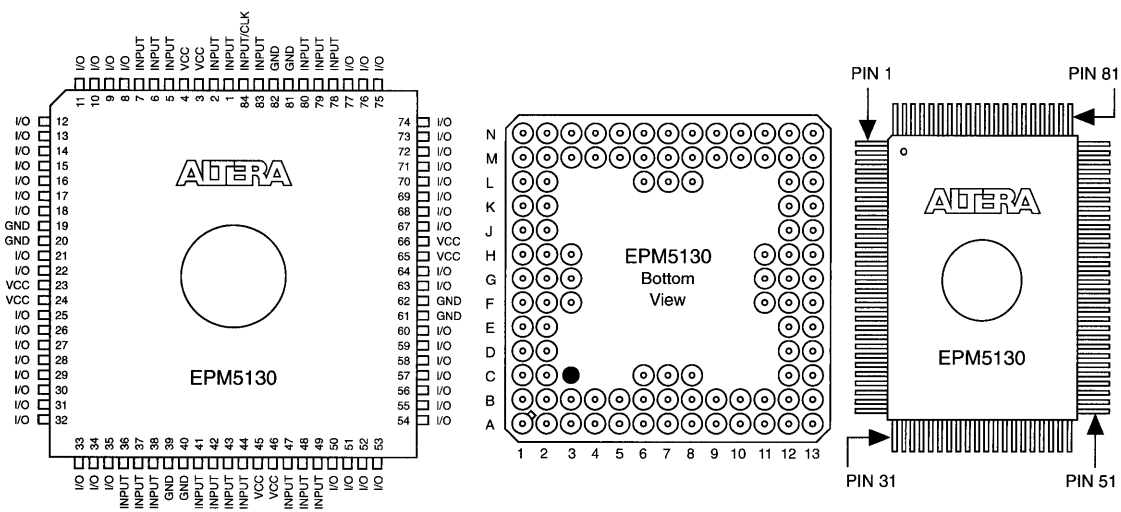
- High-density 128-macrocell general-purpose MAX 5000 EPLD
- 128 macrocells optimized for pin-intensive applications, easily integrating over 60 TTL MSI and SSI components
- High pin count for 16- or 32-bit data paths
- 256 shareable expander product terms
  - More than 32 product terms in a single macrocell
  - 128 additional latches provided by cross-coupling expanders
  - All inputs can be latched without using macrocells
- 20 high-speed dedicated inputs for fast latching of 16-bit functions
- Multi-LAB architecture ensuring high speeds
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Fast clock-to-output delays for bus-oriented functions
- Programmable I/O architecture that allows up to 84 inputs or 64 outputs in windowed ceramic PGA, and windowed ceramic and one-time-programmable (OTP) plastic QFP packages
- Programmable I/O architecture that allows up to 68 inputs or 48 outputs in windowed ceramic and plastic OTP J-lead packages

General Description

The EPM5130 EPLD (see Figure 21) is a user-configurable, high-performance Multiple Array Matrix (MAX) 5000-family EPLD that is optimized for pin-intensive designs. It provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic.

Figure 21. EPM5130 Package Pin-Out Diagrams

See Table 3 in this data sheet for QFP pin-outs and Table 4 for PGA pin-outs. Package outlines not drawn to scale.



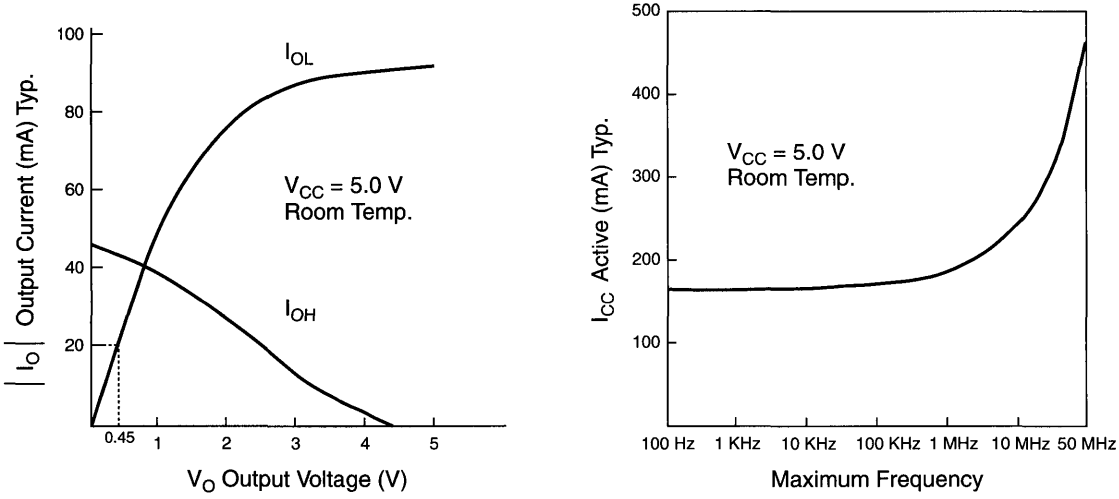
J-Lead PGA QFP

The EPM5130 EPLD is available in windowed ceramic 84-pin J-lead chip carrier (JLCC), 100-pin pin-grid array (PGA), and 100-pin quad flat pack (WQFP) packages, as well as OTP plastic J-lead (PLCC) and QFP packages.

A single EPM5130 EPLD can quickly integrate multiple 20- and 24-pin low-density PLDs and high-pin-count subsystems, such as custom DMA controllers. In addition, it can handle a 32-bit data path application with enough I/O to allow the required control signals to be implemented.

Figure 22 shows output drive characteristics of EPM5130 I/O pins and typical supply current versus frequency for the EPM5130 EPLD.

Figure 22. EPM5130 Output Drive Characteristics and I_{CC} vs. Frequency

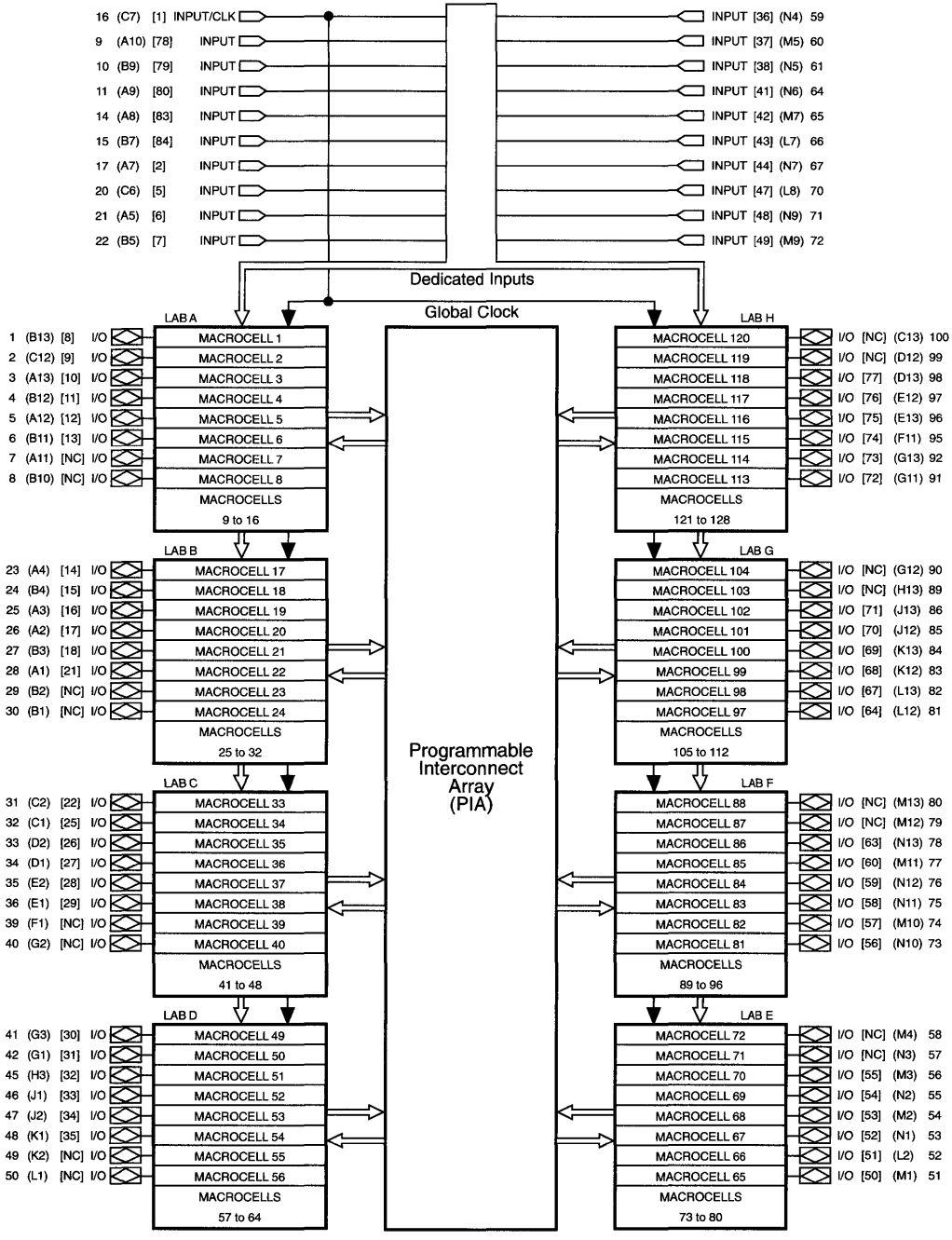


The EPM5130 EPLD consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs), each containing 16 macrocells and 32 expander product terms (see Figure 23). Expander product terms can be used and shared by all macrocells in the device to ensure efficient use of device resources. Because the LAB is very compact, the high speeds required by most I/O subsystems are maintained.

The EPM5130 EPLD has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a global (synchronous) clock to provide enhanced clock-to-output delays for bus-oriented functions. The EPM5130 EPLD also has 64 I/O pins, 8 in each LAB, that can be configured for input, output, or bidirectional data flow. Dual feedback on the I/O pins provides the most efficient use of device pin resources.

Figure 23. EPM5130 Block Diagram

Numbers in parentheses are for PGA packages; numbers in brackets are for J-lead packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		175	250 (325)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		180	275 (375)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5130-1, EPM5130-2, EPM5130
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Table 3 shows the pin-outs for the EPM5130 QFP package.

Table 3. EPM5130 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	26	I/O	51	I/O	76	I/O
2	I/O	27	I/O	52	I/O	77	I/O
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	INPUT	34	I/O	59	INPUT	84	I/O
10	INPUT	35	I/O	60	INPUT	85	I/O
11	INPUT	36	I/O	61	INPUT	86	I/O
12	GND	37	GND	62	GND	87	GND
13	GND	38	GND	63	GND	88	GND
14	INPUT	39	I/O	64	INPUT	89	I/O
15	INPUT	40	I/O	65	INPUT	90	I/O
16	INPUT/CLK	41	I/O	66	INPUT	91	I/O
17	INPUT	42	I/O	67	INPUT	92	I/O
18	VCC	43	VCC	68	VCC	93	VCC
19	VCC	44	VCC	69	VCC	94	VCC
20	INPUT	45	I/O	70	INPUT	95	I/O
21	INPUT	46	I/O	71	INPUT	96	I/O
22	INPUT	47	I/O	72	INPUT	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	I/O	74	I/O	99	I/O
25	I/O	50	I/O	75	I/O	100	I/O

Table 4 shows the pin-outs for the EPM5130 PGA package.

Table 4. EPM5130 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	I/O	B13	I/O	G11	I/O	M2	I/O
A2	I/O	C1	I/O	G12	I/O	M3	I/O
A3	I/O	C2	I/O	G13	I/O	M4	I/O
A4	I/O	C6	INPUT	H1	VCC	M5	INPUT
A5	INPUT	C7	INPUT/CLK	H2	VCC	M6	GND
A6	VCC	C8	GND	H3	I/O	M7	INPUT
A7	INPUT	C12	I/O	H11	GND	M8	VCC
A8	INPUT	C13	I/O	H12	GND	M9	INPUT
A9	INPUT	D1	I/O	H13	I/O	M10	I/O
A10	INPUT	D2	I/O	J1	I/O	M11	I/O
A11	I/O	D12	I/O	J2	I/O	M12	I/O
A12	I/O	D13	I/O	J12	I/O	M13	I/O
A13	I/O	E1	I/O	J13	I/O	N1	I/O
B1	I/O	E2	I/O	K1	I/O	N2	I/O
B2	I/O	E12	I/O	K2	I/O	N3	I/O
B3	I/O	E13	I/O	K12	I/O	N4	INPUT
B4	I/O	F1	I/O	K13	I/O	N5	INPUT
B5	INPUT	F2	GND	L1	I/O	N6	INPUT
B6	VCC	F3	GND	L2	I/O	N7	INPUT
B7	INPUT	F11	I/O	L6	GND	N8	VCC
B8	GND	F12	VCC	L7	INPUT	N9	INPUT
B9	INPUT	F13	VCC	L8	INPUT	N10	I/O
B10	I/O	G1	I/O	L12	I/O	N11	I/O
B11	I/O	G2	I/O	L13	I/O	N12	I/O
B12	I/O	G3	I/O	M1	I/O	N13	I/O

Features

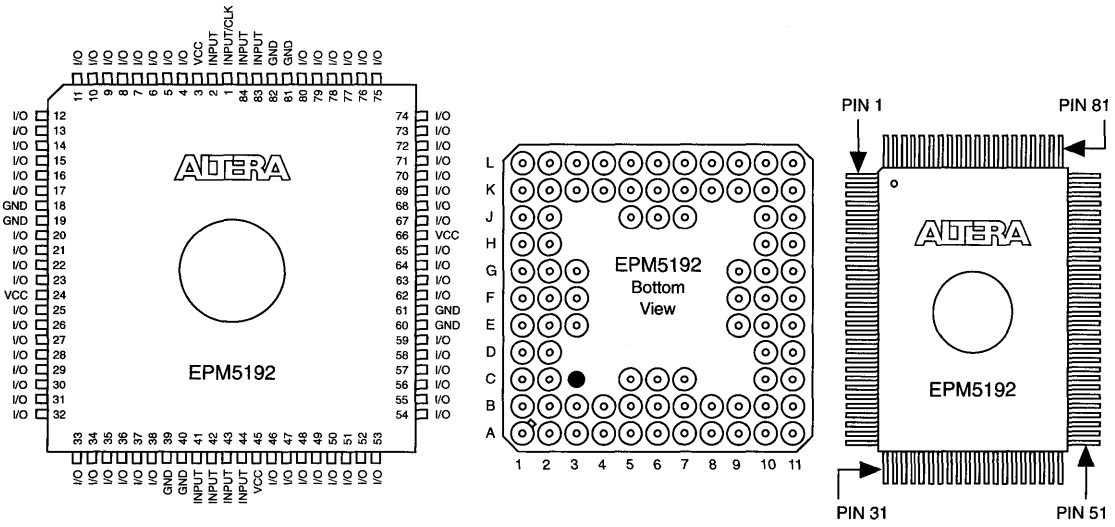
- 192 macrocells for easy replacement of over 100 TTL devices and for integration of complete logic boards into a single package
- 384 shareable expander product terms that offer flexibility for register and combinatorial logic expansion
- Multi-LAB architecture that ensures high speeds
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) J-lead packages, 84-pin windowed ceramic PGA packages, and 100-pin windowed ceramic and plastic OTP QFP packages

General Description

Altera's EPM5192 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that provides high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. Package pin-out diagrams for the EPM5192 EPLD are shown in Figure 24.

Figure 24. EPM5192 Package Pin-Out Diagrams

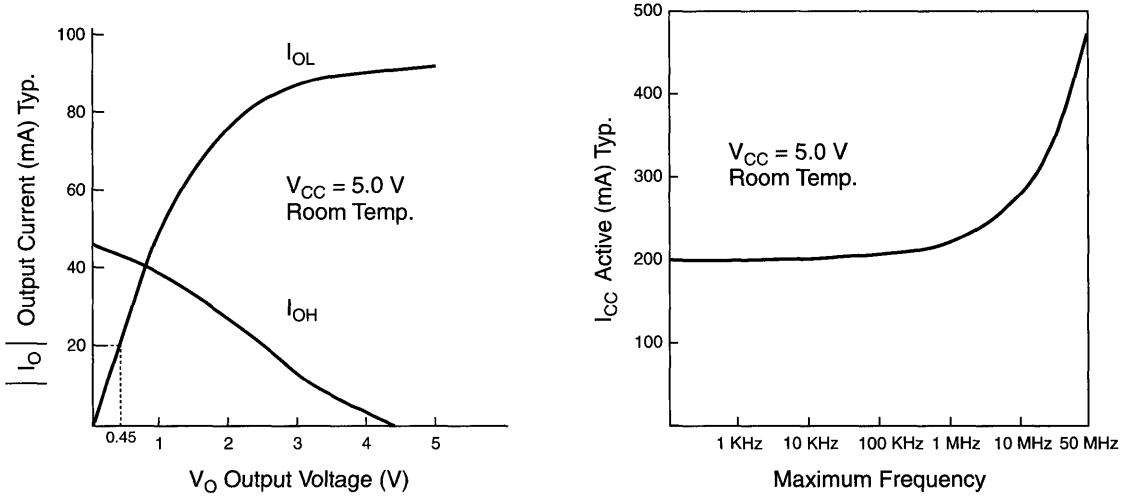
See Table 5 in this data sheet for QFP pin-outs and Table 6 for PGA pin-outs. Package outlines not drawn to scale.



The EPM5192 EPLD can replace over 100 TTL SSI and MSI components and integrate the logic contained in over 20 22V10 devices. In addition, it accommodates other low-density PLDs of all sizes. These features allow the EPM5192 EPLD to easily integrate complete systems into a single device.

Figure 25 shows output drive characteristics of EPM5192 I/O pins and typical supply current versus frequency for the EPM5192 EPLD.

Figure 25. EPM5192 Output Drive Characteristics and I_{CC} vs. Frequency

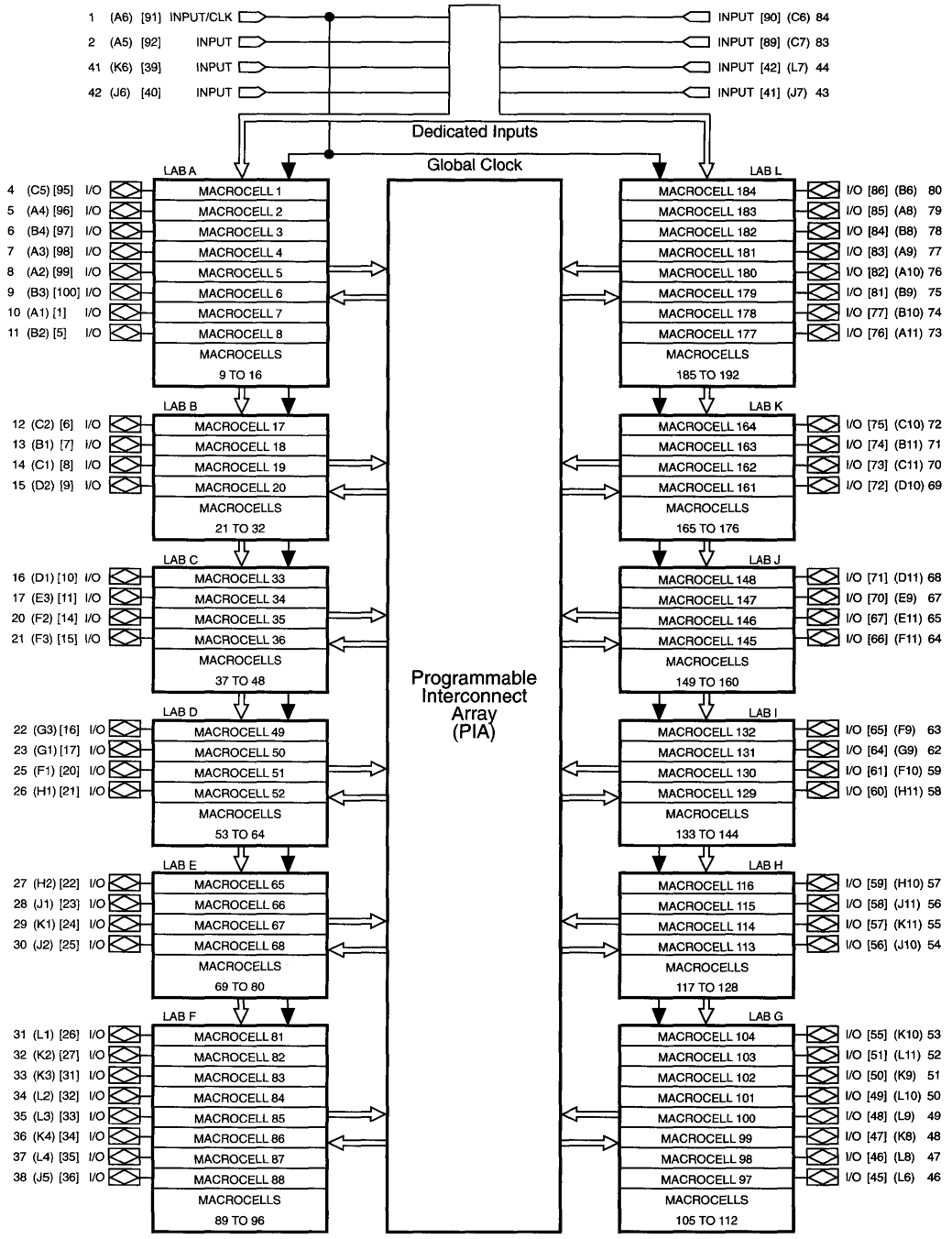


The EPM5192 EPLD consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs) that each contain 16 macrocells and 32 expander product terms (see Figure 26). Because each LAB is very compact, high performance is maintained and device resources are used efficiently.

The EPM5192 EPLD has 8 dedicated input pins, one of which can be used as a global (synchronous) clock. The EPM5192 EPLD can mix global and array (asynchronous) clocking in a single device, facilitating easy integration of multiple subsystems. It also has 64 I/O pins that can be configured for input, output, or bidirectional data flow, providing an interface to high-speed, bus-oriented applications.

Figure 26. EPM5192 Block Diagram

Numbers in parentheses are for PGA packages; numbers in brackets are for QFP packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM5192-1, EPM5192-2, EPM5192
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Table 5 shows the pin-outs for the EPM5192 QFP package.

Table 5. EPM5192 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	26	I/O	51	I/O	76	I/O
2	NC	27	I/O	52	NC	77	I/O
3	NC	28	NC	53	NC	78	NC
4	NC	29	NC	54	NC	79	NC
5	I/O	30	NC	55	I/O	80	NC
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	I/O	34	I/O	59	I/O	84	I/O
10	I/O	35	I/O	60	I/O	85	I/O
11	I/O	36	I/O	61	I/O	86	I/O
12	GND	37	GND	62	GND	87	GND
13	GND	38	GND	63	GND	88	GND
14	I/O	39	INPUT	64	I/O	89	INPUT
15	I/O	40	INPUT	65	I/O	90	INPUT
16	I/O	41	INPUT	66	I/O	91	INPUT/CLK
17	I/O	42	INPUT	67	I/O	92	INPUT
18	NC	43	VCC	68	NC	93	VCC
19	VCC	44	NC	69	VCC	94	NC
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	I/O	74	I/O	99	I/O
25	I/O	50	I/O	75	I/O	100	I/O

Note: NC represents "not connected."

Table 6 shows the pin-outs for the EPM5192 PGA package.

Table 6. EPM5192 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	I/O	B11	I/O	F9	I/O	K2	I/O
A2	I/O	C1	I/O	F10	I/O	K3	I/O
A3	I/O	C2	I/O	F11	I/O	K4	I/O
A4	I/O	C5	I/O	G1	I/O	K5	GND
A5	INPUT	C6	INPUT	G2	VCC	K6	INPUT
A6	INPUT/CLK	C7	INPUT	G3	I/O	K7	VCC
A7	GND	C10	I/O	G9	I/O	K8	I/O
A8	I/O	C11	I/O	G10	GND	K9	I/O
A9	I/O	D1	I/O	G11	GND	K10	I/O
A10	I/O	D2	I/O	H1	I/O	K11	I/O
A11	I/O	D10	I/O	H2	I/O	L1	I/O
B1	I/O	D11	I/O	H10	I/O	L2	I/O
B2	I/O	E1	GND	H11	I/O	L3	I/O
B3	I/O	E2	GND	J1	I/O	L4	I/O
B4	I/O	E3	I/O	J2	I/O	L5	GND
B5	VCC	E9	I/O	J5	I/O	L6	I/O
B6	I/O	E10	VCC	J6	INPUT	L7	INPUT
B7	GND	E11	I/O	J7	INPUT	L8	I/O
B8	I/O	F1	I/O	J10	I/O	L9	I/O
B9	I/O	F2	I/O	J11	I/O	L10	I/O
B10	I/O	F3	I/O	K1	I/O	L11	I/O

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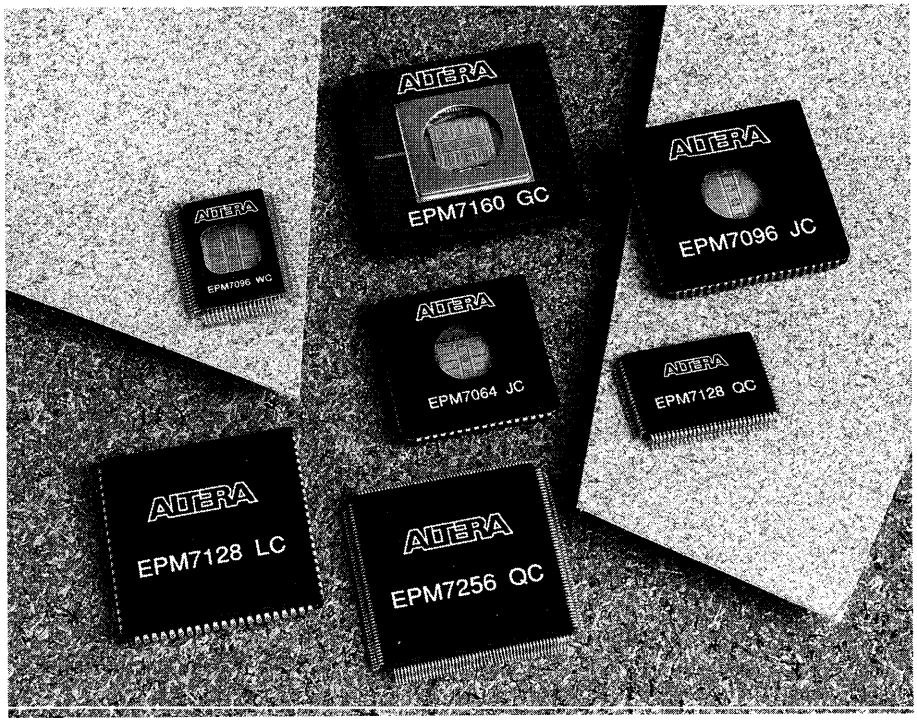
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MAX 7000 EPLD Overview

High-Performance, High-Pin-Count Devices

September 1991, ver. 1

Data Sheet

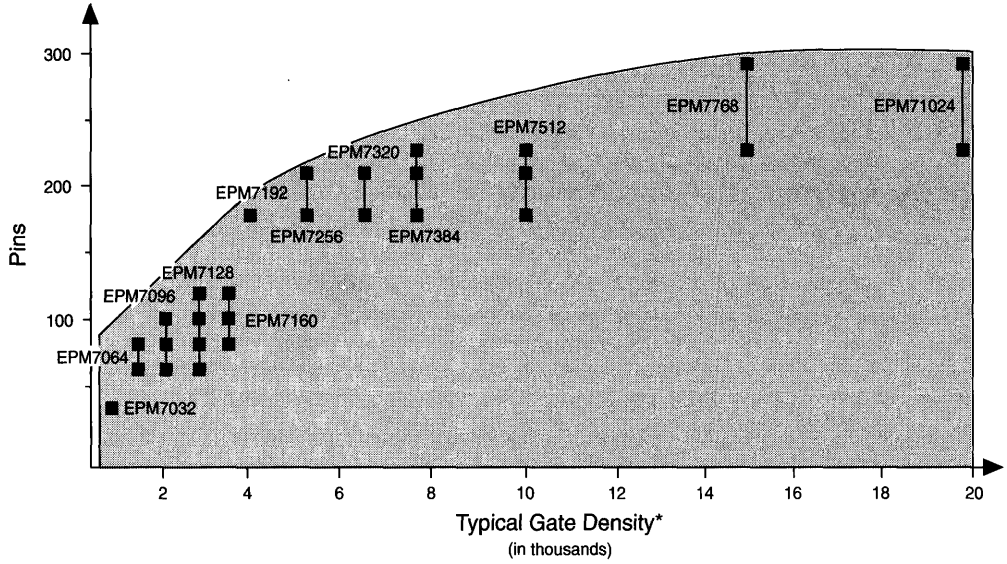
Introduction

- High-density, high-speed CMOS EPLDs with second-generation Multiple Array MatriX (MAX) architecture
- Complete EPLD family with logic density up to 20,000 typical gates
- Fast, 15-ns pin-to-pin logic delays with 70-MHz true system-clock frequency (including interconnect)
- Programmable power-saver mode
- 44 to 288 pins available in J-lead, PGA, and QFP packages
- User-defined I/O options for bus-interface functions
- Enhanced Programmable Interconnect Array (PIA) that provides a fast, fixed delay from any internal source to any destination in the EPLD
- Advanced macrocell to efficiently place logic for optimum speed and density
- Programmable registers providing D, T, JK, or SR flip-flops with individual Clear, Preset, and Clock controls
- High pin-to-logic ratio for I/O-intensive data path applications and 32-bit microprocessor support logic
- Full software support for PC and workstation platforms (including HP/Apollo and Sun) with Altera's MAX+PLUS II software
  - Hierarchical schematic capture with over 300 TTL and custom macrofunctions
  - Altera Hardware Description Language (AHDL) for Boolean equation, state machine, and truth table design entry
  - Waveform design entry
  - Logic synthesis and minimization
  - Device fitting within minutes
  - Full timing simulation
  - Automatic multi-EPLD partitioning and simulation
  - EDIF netlist interface for additional design entry and simulation support with popular CAE tools (Mentor Graphics, Valid Logic, Viewlogic, Synopsys)

General Description

MAX (Multiple Array MatriX) 7000 EPLDs use a second-generation MAX architecture to build devices with logic densities up to 20,000 typical gates. The MAX 7000 EPLDs shown in Figure 1 support 15-ns pin-to-pin logic delays and 70-MHz clock frequencies. MAX 7000 EPLDs are offered in erasable windowed ceramic and plastic J-lead chip carrier (JLCC and PLCC), pin-grid array (PGA), and quad flat pack (QFP) packages, providing 44 to 288 pins.

Figure 1. MAX 7000 Pin Count vs. Typical Gate Density



** Typical gate density is 50% of maximum gate density.*

Initially fabricated on the proven 0.8-micron double-metal CMOS process, the MAX 7000 devices are 100% generically testable, guaranteeing high device reliability. A programmable Security Bit ensures total protection of proprietary designs.

MAX 7000 EPLDs are the first programmable logic devices (PLDs) with programmable speed/power optimization. Speed-critical portions of the design can run at high speed/full power while the remainder runs at reduced speed/quarter power, making the MAX 7000 family the most power-efficient logic family available.

Altera's MAX+PLUS II development software fully exploits the density and flexibility of the MAX 7000 family. MAX+PLUS II Windows 3.0-based development software is a fully integrated package for designing logic with Altera's Classic, MAX 5000, MAX 7000, and STG EPLDs.

The complete MAX+PLUS II system provides an intuitive graphical interface that supports hierarchical graphic, text, and waveform design entry with over 300 TTL macrofunctions. It includes the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, and truth table entry methods. MAX+PLUS II provides highly automated compilation, automatic multi-EPLD partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a detailed on-line help system. MAX+PLUS II also imports and exports standard EDIF netlist files, providing a convenient workstation interface.

For more information about MAX+PLUS II, see the *PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES; PLS-WS/HP;* and *PLS-WS/SN* data sheets in this data book.

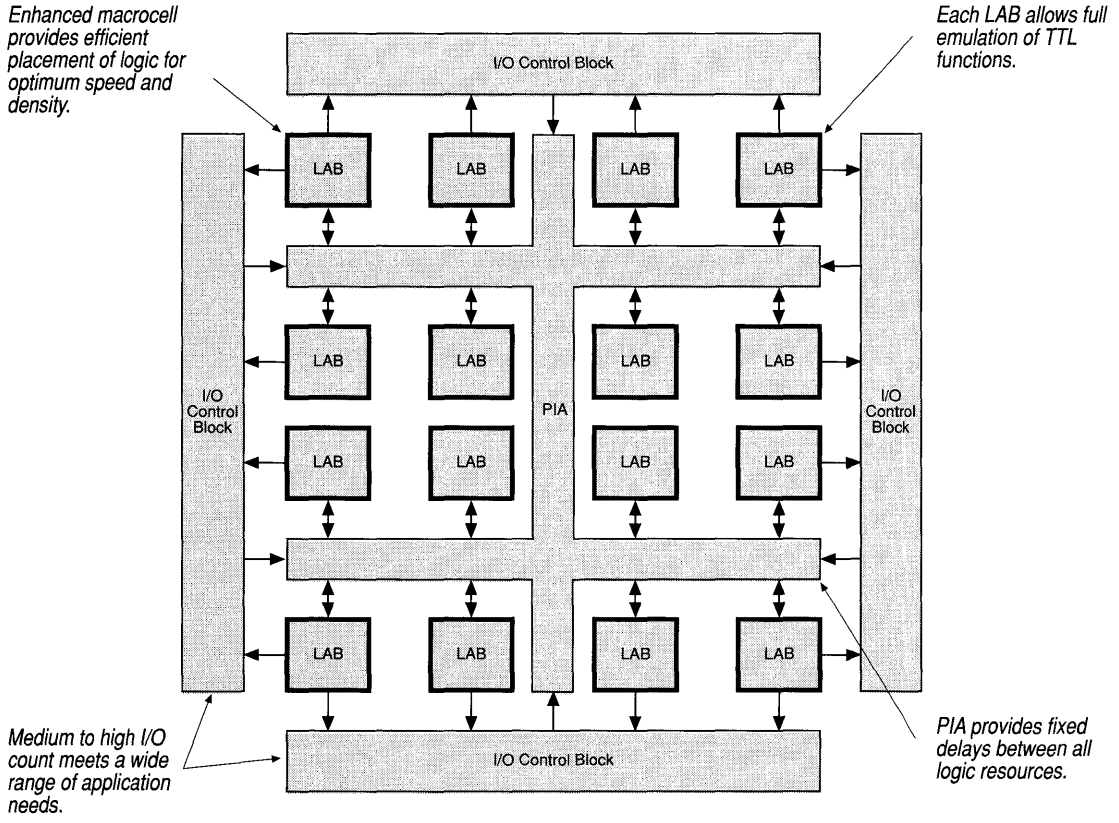
Functional Description

The MAX 7000 family incorporates many of the same features of its successful predecessor, the MAX 5000 family. In addition, the MAX 7000 architecture (shown in Figure 2) includes significant enhancements that deliver even more speed, density, and design flexibility.

The MAX 7000 architecture includes the following five basic elements:

- Logic array blocks
- Macrocells
- Logic expanders (shared and parallel)
- Enhanced programmable interconnect array
- I/O control blocks

Figure 2. MAX 7000 Block Diagram



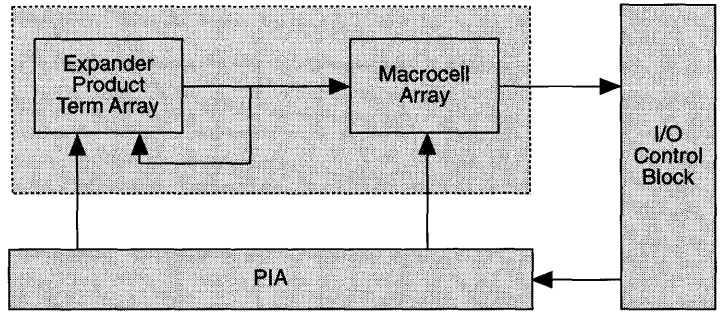
Logic Array Blocks

The MAX architecture is based on the concept of linking small, high-performance, flexible logic array modules called Logic Array Blocks (LABs), shown in Figure 3. Multiple LABs are linked together via a dedicated programmable network called a Programmable Interconnect Array (PIA).

Each LAB contains 16 modular logic building blocks, called macrocells, and up to 16 shared logic expanders. Logic expanders can provide additional logic resources to any of the macrocells in an LAB. Furthermore, since all macrocells within an LAB share logic inputs, if one macrocell uses a specific logic input or a shared logic expander, it is also available to all other macrocells within that LAB.

Each LAB is fed by inputs from the PIA, providing sufficient fan-in for the 16 macrocells to implement a wide range of typical logic functions. If more inputs are needed, for example in very wide data paths, several LABs can be used in parallel.

Figure 3. Logic Array Block (LAB)



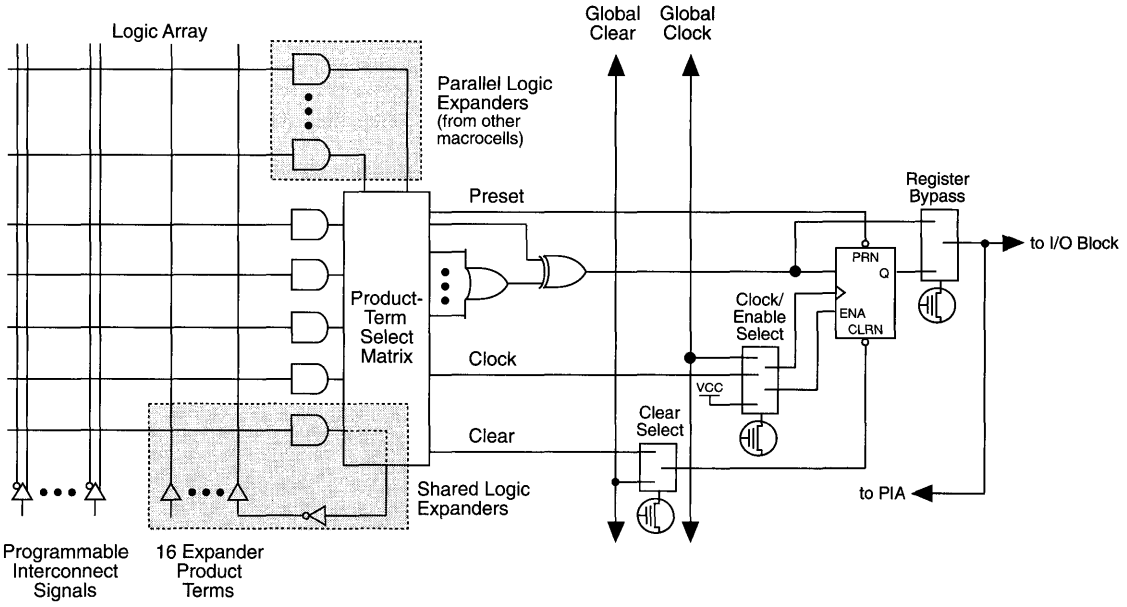
Macrocells

Macrocells within the LAB provide both sequential and combinatorial logic capability, thus ensuring the most efficient implementation of a wide range of logic functions. The MAX 7000 macrocell is shown in Figure 4.

Each macrocell has one flip-flop that can be programmed for D, T, JK, or SR operation with programmable clock control, individually configured for each macrocell. If necessary, the flip-flops can be bypassed for combinatorial operation.

Along with a programmable flip-flop, each macrocell also contains five basic product terms. These product terms can be allocated by a product-term select matrix as primary inputs for combinatorial functions; as

Figure 4. MAX 7000 Macrocell



secondary inputs for either an additional XOR input or individual Clear, Preset, Clock, and Clock Enable logic functions for the flip-flops; or as logic expanders to assist the generation of complex logic functions.

In addition, global Clock, Clear, and Output Enable control signals come in directly from device pins, eliminating the logic array delay and minimizing control-function delays.

The Clock Enable function allows flip-flops to be controlled by the logic array, even when they are clocked from the fast global Clock. This feature facilitates the implementation of high-speed synchronous designs. The Clock Enable function also allows each macrocell register to be clocked individually.

Logic Expanders

Whereas most logic can be implemented with the five basic product terms in each macrocell, some logic functions are more complex and require more product terms. Instead of using another macrocell to supply the additional logic resources, expanders are available to provide additional product terms directly to any macrocell. Unlike MAX 5000 EPLDs, which have only shared expanders, MAX 7000 EPLDs have both shared and parallel logic expanders (see Figure 4).

The 16 shared logic expanders in each LAB can be viewed as a pool of uncommitted single product terms with inverting outputs that feed back into the LAB. Use of shared logic expanders enables PLA-like flexibility by allowing each shared logic expander output to be shared across all the macrocells in an LAB. Shared logic expanders can also be used to build additional register functions such as input latches.

Parallel logic expanders, on the other hand, utilize unused product terms from macrocells in the LAB to construct fast, complex logic. Parallel logic expanders cause only a 2-ns delay because they are connected by the product-term select matrix in parallel with the five basic product terms in the borrowing macrocell.

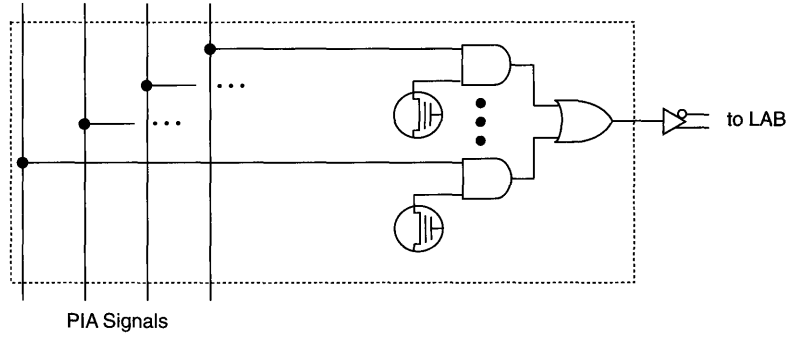
The ability to allocate additional product terms to any macrocell means that logic can be synthesized with the fewest logic resources at the fastest possible speed.

Programmable Interconnect Array

The MAX 7000 enhanced PIA is a programmable wiring path between LABs that allows any signal source to reach any destination on the device. Although it is fed by all macrocell and I/O pin feedbacks, this fast, low-skew PIA routes only the signals required to implement logic in each LAB.

The MAX 7000 PIA, shown in Figure 5, introduces a very fast, uniform logic delay into every logic signal path, representing a sevenfold improvement over MAX 5000 EPLDs. The MAX 7000 architecture uses a series of two-input AND gates that feed an OR function. The EPROM transistor controls one input of the AND gate and regulates the selection of the PIA signal to the LAB.

Figure 5. MAX 7000 Programmable Interconnect Array (PIA)



I/O Control Blocks

In most PLD architectures, when an I/O pin is used as an input, the macrocell associated with that pin cannot be used, i.e., it is wasted. The MAX 7000 architecture, like the MAX 5000 architecture, avoids this waste by decoupling I/O pins and macrocell logic resources. If the macrocells' I/O pins are used as dedicated inputs, the macrocells can still be used for buried logic because they provide independent I/O pin and macrocell feedback paths into the programmable logic array. Thus, logic in MAX 7000 EPLDs is never wasted as a result of I/O pin requirements.

MAX 7000 EPLDs provide two global Output Enable signals that allow communication with more than one bus at a time. Since they are global signals, both Output Enables can be directly controlled from device pins for high-speed operation.

Routing: MAX vs. FPGAs

The ability to interconnect all points in the MAX 7000 architecture ensures rapid, automatic design completion. While high-density programmable gate array designs require significant manual intervention and can take hours or even days to route, typical MAX 7000 designs can be automatically routed in minutes.

Furthermore, incremental, additive delays between various points (frequently up to 50 ns) can cause debilitating skew and glitch problems in field-programmable gate arrays (FPGAs). This unpredictable timing requires additional iterations of the design. MAX 7000 EPLDs provide a single uniform delay between any signal source and all signal destinations.

Programmable Speed/Power Control

The MAX 7000 family offers a programmable speed/power tradeoff that supports quarter-power operation across selected signal paths or the entire device. Since only a small fraction of all gates operates at maximum frequency in most logic applications, this feature allows typical power savings of over 75% when compared to standard PLD implementations.

Unlike other low-power PLDs, which offer only half- or quarter-power operation across the entire device, each macrocell in MAX 7000 EPLDs can be programmed by the designer for either high-speed or quarter-power operation. The low (< 10 ns) speed penalty for quarter-power operation applies only to those macrocells selected for low power. As a result, speed-critical portions of the design can run at high speed while the remainder of the design can operate at quarter power, allowing an optimized combination of high speed and low power not available in any other programmable logic device.

Notes:

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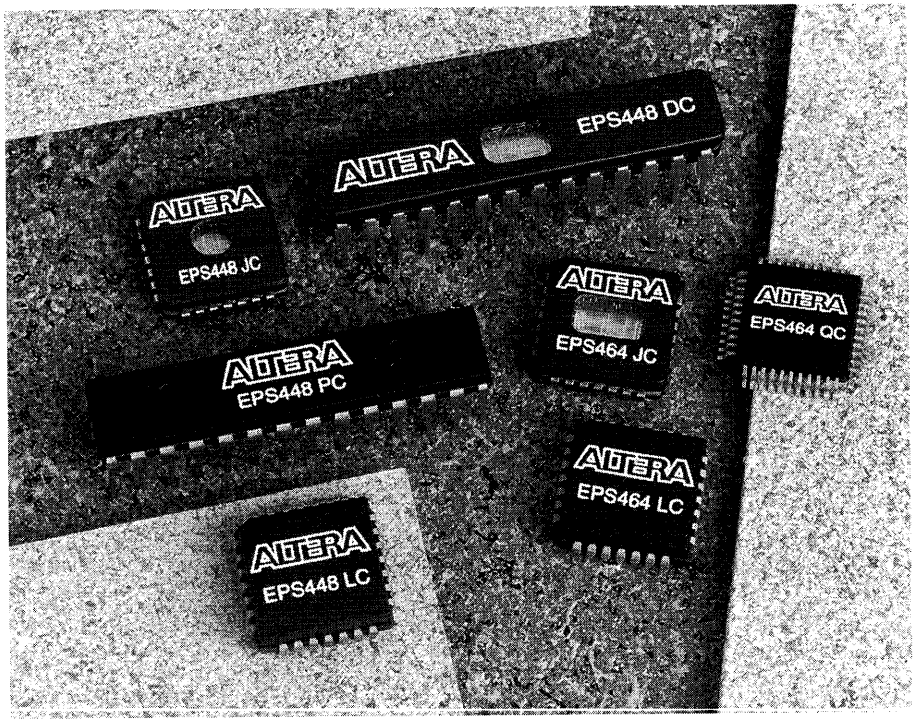
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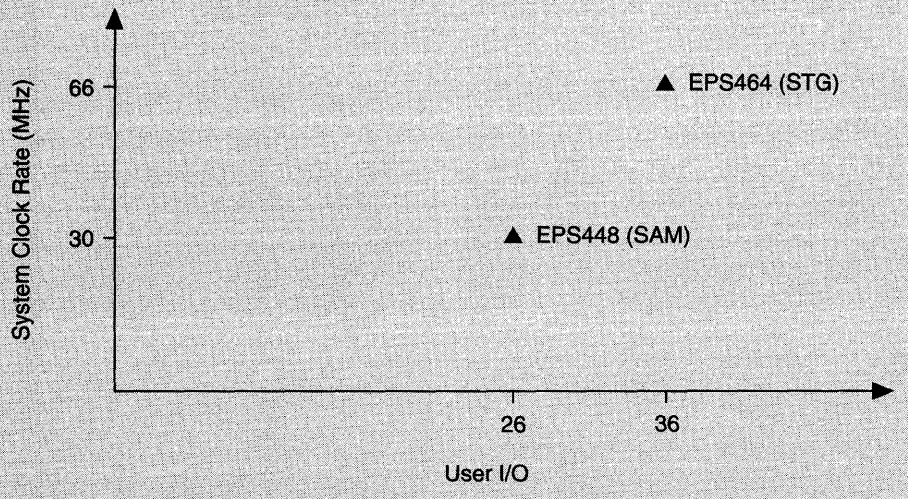
STG & SAM EPLDs

Synchronous State Machine & Waveform Generation Devices



EPS464: Synchronous Timing Generator

- Generates complex control timing waveforms for all types of imaging applications (CCD imagers, video displays, optical disks, etc.).
- Programmable architecture implements NTSC, PAL, and SECAM synchronization standards for TV/video applications.
- Powerful macrocell structure supports complex waveform and state machine designs.
- Programmable I/O supports up to 36 inputs and 32 outputs.
- "Quiet" outputs minimize output switching noise.
- 66-MHz clock frequency
- 44-pin J-lead or 44-pin plastic QFP package
- Supported by MAX+PLUS II design tools that allow graphic, text, and waveform design entry; compilation; simulation; and programming

EPS448: Stand-Alone Microsequencer

- Provides efficient solutions for state machines, bus- and memory-control functions, graphics, and DSP algorithm controllers.
- On-chip reprogrammable microcode EPROM up to 448 words deep
- Prioritized, multiway branch control
- 15 × 8 stack for implementing subroutines, nested loops, branch control, and other iterative functions
- 8-bit loop counter for timing and delay loops
- 30-MHz clock frequency
- 28-pin, 300-mil DIP or J-lead package
- Vertically and horizontally cascadable
- Supported by SAM+PLUS design tools which include Altera State Machine Input Language (ASMILE), Assembly Language (ASM), SAM Design Processor (SDP), and Functional Simulator (SAMSIM)

EPS464 STG EPLD

Synchronous Timing Generator

September 1991, ver. 2 **Data Sheet**

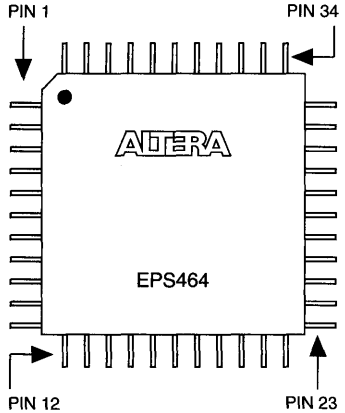
Features

- High-performance Synchronous Timing Generator (STG) EPLD ideal for custom waveform generation and state machine designs
- Generates complex control timing waveforms for imaging and display applications, such as CCD imagers, video displays, and optical disks
- High-performance 66-MHz clock frequency
- Programmable I/O support for up to 36 inputs and 32 outputs
- Noise-resistant input buffers with 250-mV hysteresis and "quiet" output buffers for noise immunity and reliable operation
- Powerful macrocell architecture optimized for
  - Modulo-*n* binary and Gray-code counters
  - Complex state machines
  - Multiple product-term JK flip-flops for waveform generation
  - Phase comparator and clock oscillator functions
- Programmable architecture that implements NTSC, PAL, and SECAM synchronization standards for TV and video applications
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) plastic J-lead chip carrier and plastic QFP packages
- MAX+PLUS II software support includes waveform, schematic capture, and text design entry; logic synthesis; multi-device logic partitioning; and full timing simulation.

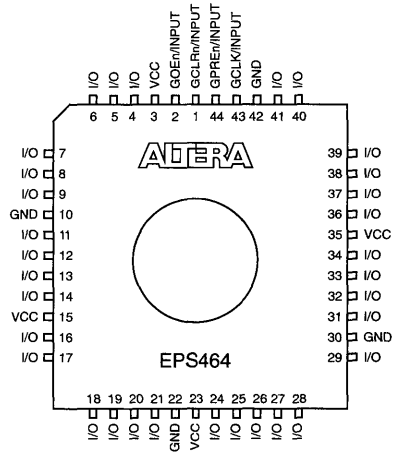
Figure 1 shows the EPS464 pin-out diagrams.

Figure 1. EPS464 Package Pin-Out Diagrams

PQFP pin numbers are shown in Table 1. Package outlines not drawn to scale.



QFP



J-Lead

General Description

The Altera EPS464 Erasable Programmable Logic Device (EPLD) provides an integrated solution for synchronous timing and waveform generation applications. Each of the EPS464 outputs can generate customized waveforms to meet various system requirements. Applications include TV/video synchronization signals (e.g., NTSC, PAL, SECAM, HDTV), CCD timing controllers, high-performance state machines, and memory controllers. The EPS464 EPLD is available in 44-pin windowed ceramic J-lead (JLCC), OTP plastic J-lead (PLCC), and EIAJ-standard plastic quad flat pack (PQFP) packages.

The EPS464 EPLD has 32 I/O pins that can be independently configured for input, output, or bidirectional operation. It also has 4 dedicated input pins that can be programmed as general-purpose inputs or as system-wide control signals (Clock, Clear, Preset, and Output Enable) for each macrocell and I/O pin.

The EPS464 EPLD has 64 macrocells that are optimized for waveform synthesis applications. The advanced macrocell structure of the EPS464 EPLD allows integration of complex logic functions, with over 100 product terms available to any one macrocell. Each of the 64 internal flip-flops can be programmed for D, T, JK, or SR operation. JK and SR flip-flops are well suited for pattern-generation applications, since simple set and reset operations can be used to define the transitions of output waveforms.

Logic designs for the EPS464 EPLD are created with Altera's MAX+PLUS II development system using any combination of graphic, text, and waveform design entry tools.

Functional Description

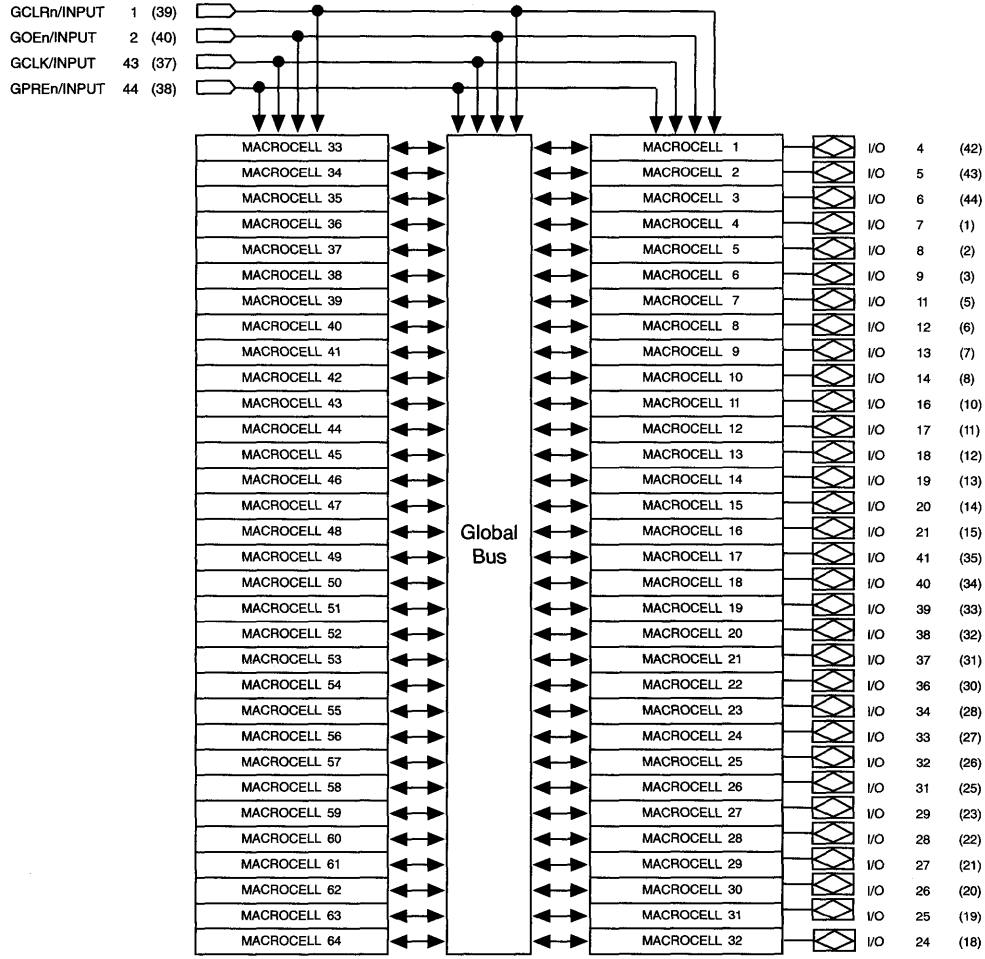
The EPS464 is a 64-macrocell EPLD that has been optimized for timing and waveform synthesis applications. Thirty-two macrocells are connected to I/O pins; the other 32 macrocells are available for buried logic and state machine registers. See Figure 2. The high logic density and large number of macrocells allow the designer to create multiple counters inside the EPS464 and to add state machines and combinatorial logic to enhance the integration of designs.

All EPS464 macrocells are fed by a global bus, which supports 50-MHz system speeds and eliminates placement-dependent interconnect delays between device resources.

The EPS464 EPLD uses CMOS EPROM cells to configure all combinatorial and sequential logic functions in the device. It is user-configurable to accommodate the variety of independent logic blocks typically used in waveform generation and random-logic integration applications. The EPLDs can be erased for quick and efficient iterations during development and debug cycles.

Figure 2. EPS464 Block Diagram

Numbers in parentheses are for PQFP packages.

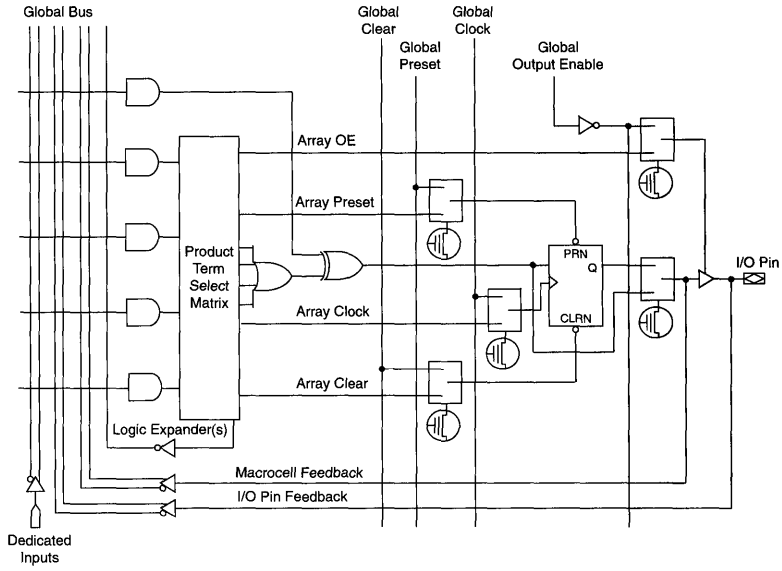


Macrocells

The EPS464 macrocell, shown in Figure 3, consists of three functional blocks: a product-term array, a product-term select matrix, and a programmable register.

Each programmable register can be configured as a D, T, JK, or SR flip-flop and is positive-edge-triggered. Register types can be specified by the designer or by the MAX+PLUS II software, which automatically selects the most efficient flip-flop type to implement a given logic function. The register can also be bypassed for fast combinatorial operation.

Figure 3. EPS464 Macrocell



Combinatorial logic is implemented in the product-term array, which consists of five product terms. Four product terms feed the product-term select matrix, and the fifth feeds one input of an XOR gate, making it possible to implement active-high or active-low logic. The XOR gate is also used to build complex arithmetic logic functions and for De Morgan's inversion to reduce the number of product terms required for a design.

Based on the logic requirements of the design, the product-term select matrix individually directs the macrocell's product-term resources to the four-input OR gate, the Clock, Clear, or Preset controls on the register, the Output Enable controls on the I/O pins, or up to four expander product terms. The product-term select matrix can also connect V_{CC} or GND to the control resources to permanently enable or disable logic functions.

Register Control Functions

The macrocell's register control functions (Clock, Clear, and Preset) can be driven from product terms or from the dedicated input pins. Selection is made on an individual basis, ensuring efficient macrocell resource utilization. Connecting the control functions (GPREn, GCLRn, and GCLK) directly to the dedicated inputs guarantees fast operation. Generating these signals using product terms provides design flexibility.

Expander Product Terms

The EPS464 EPLD provides up to 256 logic expanders that are inverted product terms which are fed back into the global bus. Expanders can be used and shared by all product terms in the EPS464 to build complex logic functions, allowing the software to factor logic expressions and combine product terms efficiently. If the expanders are not used for combinatorial

logic, they can be used to build additional flip-flops or latches. This flexibility allows the designer to fully use the silicon resources packed into each EPS464 device.

I/O Control Block

The EPS464 EPLD has 32 I/O pins, each of which can be configured for input, output, or bidirectional operation. Each macrocell that feeds an I/O pin has a tri-state buffer between the macrocell output and the I/O pin. The EPS464 provides dual feedback, with feedback paths before and after the tri-state buffer, so that if an I/O pin is configured as an input, the associated macrocell is not wasted and can be used for buried logic. The Output Enable for each tri-state buffer can be controlled by the dedicated active-low global Output Enable input (GOEn), or by a product term within the macrocell.

The input pins on the EPS464 EPLD have input protection circuitry to prevent ESD damage and reduce the possibility of latch-up. They also provide input hysteresis to prevent spurious switching due to noisy inputs. The outputs are designed for reduced output switching noise, offering quiet and reliable operation.

Design Security

The EPS464 EPLD contains a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since data programmed in an EPROM cell is invisible. The Security Bit that controls this function is reset when the device is erased.

Timing Model

Timing in the EPS464 EPLD can be analyzed either with MAX+PLUS II software or with a timing model. The actual values for each parameter are shown under AC Operating Conditions in this data sheet. The EPS464 has fixed internal delays that allow the user to determine the worst-case timing for any design. The individual delays are predetermined and are not dependent on routing or layout considerations. For complete timing information, MAX+PLUS II provides a timing simulator with 0.1-ns resolution, delay prediction for point-to-point delay calculation, and a detailed timing analyzer for system-level performance evaluation.

Figure 4 shows the switching waveforms for EPS464 devices. The EPS464 timing model is shown in Figure 5. For additional information, see *Application Brief 75*. This application brief describes MAX 5000-family timing, which is similar to that of the EPS464 EPLD.

Figure 4. EPS464 Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

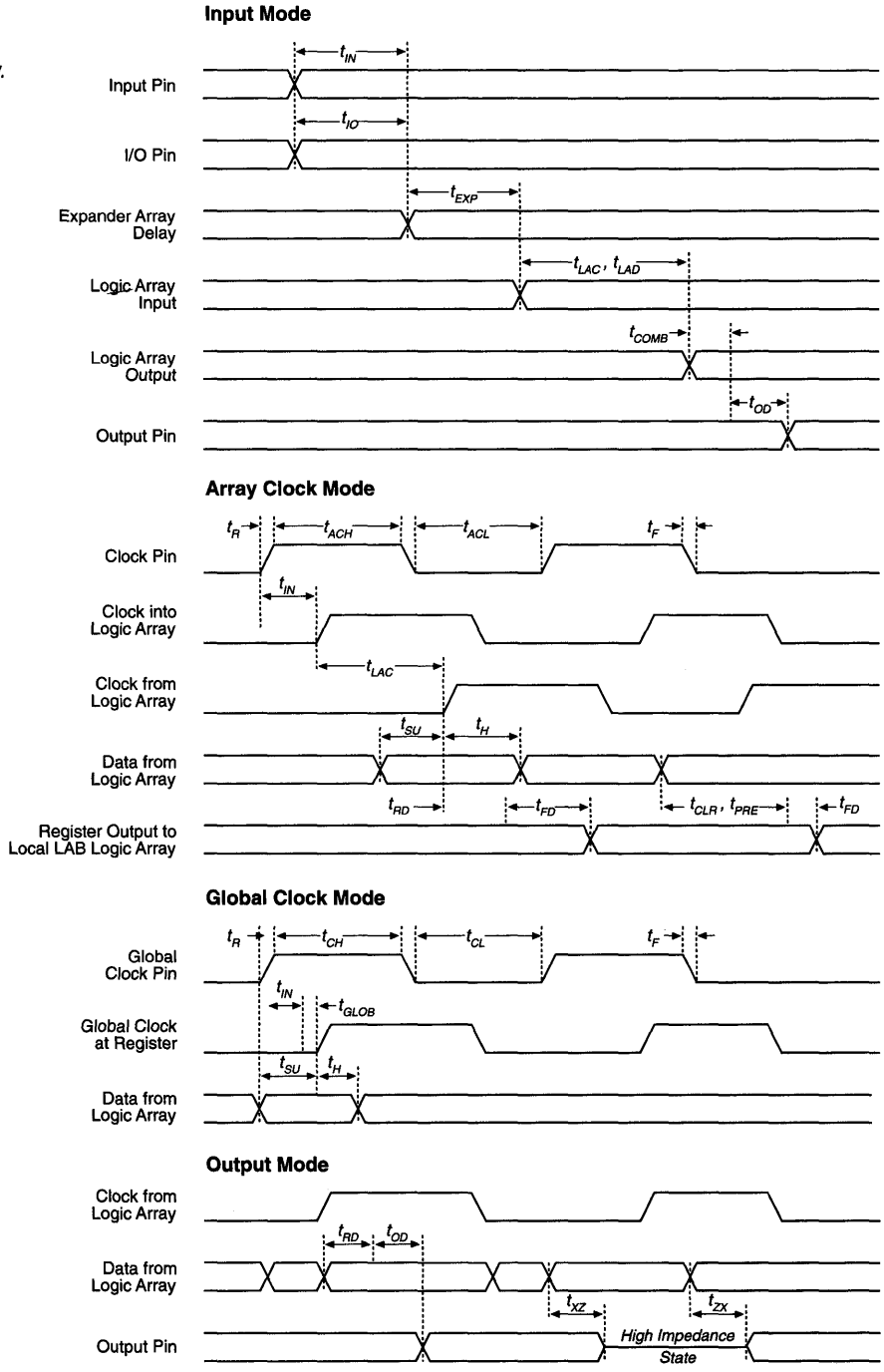
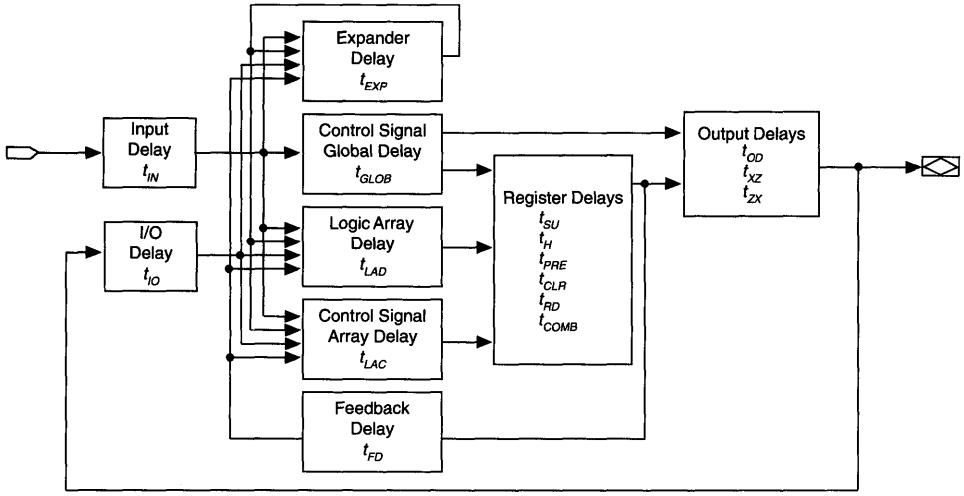


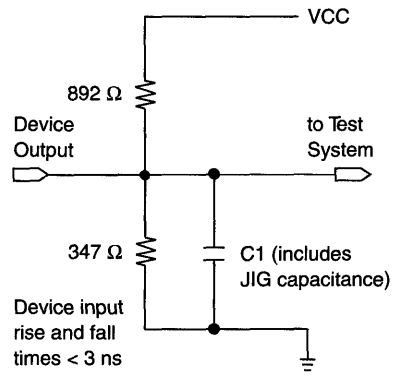
Figure 5. EPS464 Timing Model



Functional Testing

EPS464 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are performed under the conditions shown in Figure 6.

Figure 6. AC Test Conditions



Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.

Typical Application

The EPS464 EPLD is well suited for waveform generation and state machine applications. Output waveforms are decoded from internal counters or state registers to set or reset the specified waveform (i.e., perform a low-to-high or high-to-low transition).

Typical applications for the EPS464 EPLD range from video control signal generation to complex state machine designs. The CCD application shown in Figure 7 combines both of these design applications, demonstrating how many functions can be integrated into a single EPS464 device.

This design retrieves image data from a CCD array and formats it into a standard NTSC signal. Twenty of the macrocells are configured for counters (9 bits horizontal and 11 bits vertical). These macrocells count pixels per line and lines per screen, respectively. Changes in the values are made easily because the design is implemented with the Altera Hardware Description Language (AHDL), which allows counter values to be stored as constants. The generic NTSC waveform generator is available in the MAX+PLUS II TTL MacroFunction Library. The AHDL file containing the NTSC macrofunction can be edited to fit a particular application, or incorporated as a module within a larger design.

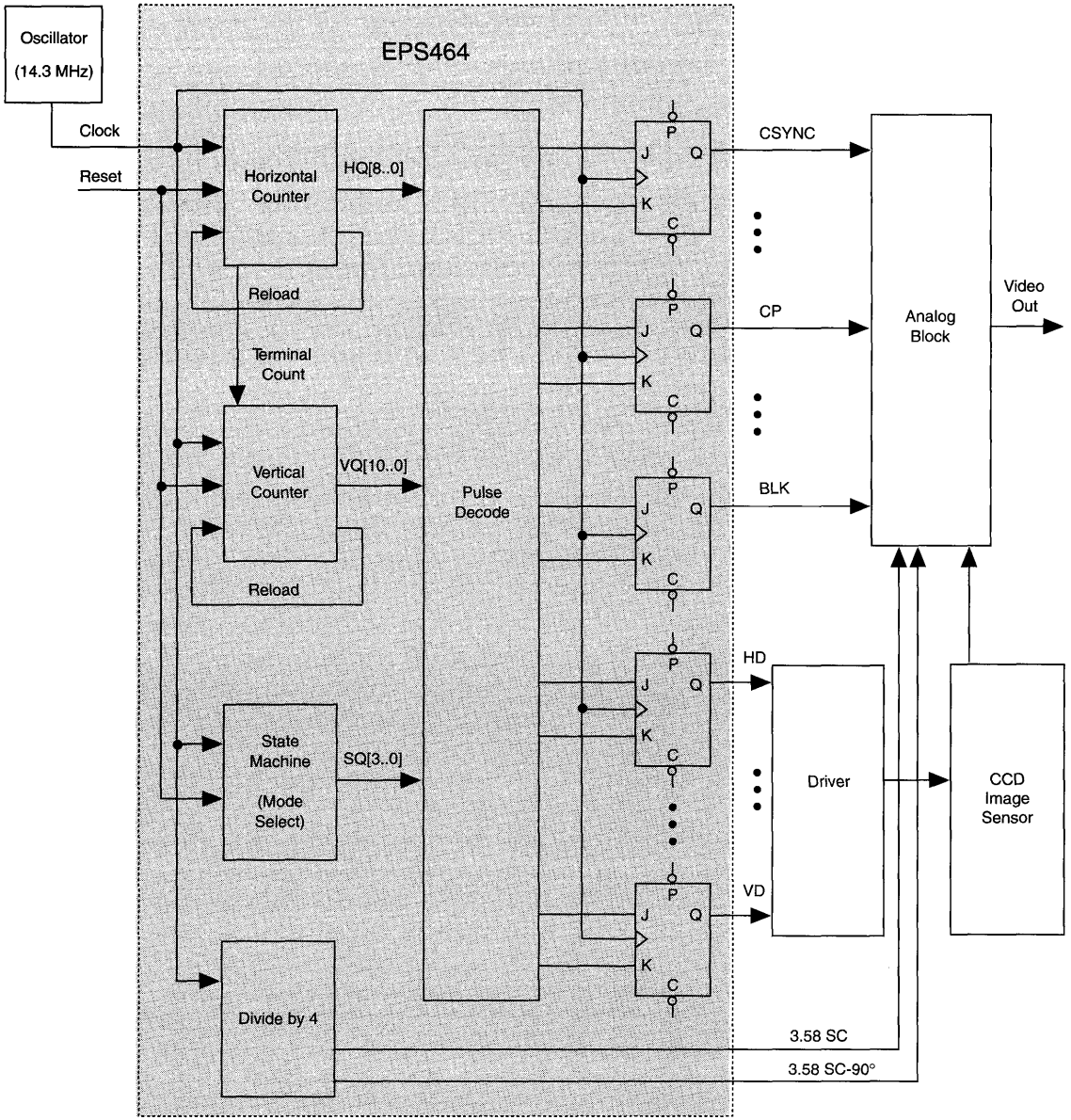
Four macrocells are used to implement a state machine that divides the pattern generation into distinct sections. Each phase in the NTSC signal is represented by a different state. The counters and state machine registers are decoded and connected to internal synchronous JK registers to set and reset the output waveforms.

The CCD application also uses an output clock that has been synthesized from the input clock using a divide-by-four stage. The synthesized clock is available at an output pin and connected to the analog control block, ensuring that analog data is synchronized with the control signals from the EPS464 EPLD. Incorporating the clock divider into the EPS464 device provides greater accuracy relative to the other control signals and eliminates the need for external discrete components.

This CCD application consumes only half of the logic resources of an EPS464 EPLD, leaving a significant amount of logic to implement secondary functions and integrate discrete support logic circuitry.

The large number of macrocells available in the EPS464 EPLD provides design flexibility for many other applications such as video synchronizers, disk controllers, communications processors, and complex controllers.

Figure 7. CCD Application



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–0.5	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–1.0	13.0	V
V_I	DC input voltage		–0.5	5.5	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–55	125	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.4	V
i_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		100	120	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		105	125	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *See Note (3)*

External Timing Parameters			EPS464-20		EPS464-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		7		10		ns
t_{CL}	Global clock low time		7		10		ns
t_{ASU}	Array clock setup time		6		8		ns
t_{AH}	Array clock hold time		6		7		ns
t_{ACO1}	Array clock to output delay			20		25	ns
t_{ACH}	Array clock high time		7		10		ns
t_{ACL}	Array clock low time		7		10		ns
t_{CNT}	Minimum global clock period			15		20	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	66.7		50		MHz
t_{ACNT}	Minimum array clock period			15		20	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	66.7		50		MHz
f_{MAX}	Maximum clock frequency	*See Note (5)*	71.4		50		MHz

Internal Timing Parameters			EPS464-20		EPS464-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		6	ns
t_{IO}	I/O input pad and buffer delay			5		6	ns
t_{EXP}	Expander array delay			13		15	ns
t_{LAD}	Logic array delay			8		11	ns
t_{LAC}	Logic control array delay			7		10	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5	ns
t_{ZX}	Output buffer enable delay			6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6	ns
t_{SU}	Register setup time		5		7		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			2		3	ns
t_{H}	Register hold time		7		8		ns
t_{GLOB}	Global control delay			1		3	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C, V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Measured with a device programmed as four 16-bit counters.
(5) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPS464-20, EPS464-25
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Figure 8 shows the output drive characteristics for EPS464 I/O pins and typical supply current vs. frequency for the EPS464 EPLD.

Figure 8. EPS464 Output Drive Characteristics and I_{CC} vs. Frequency

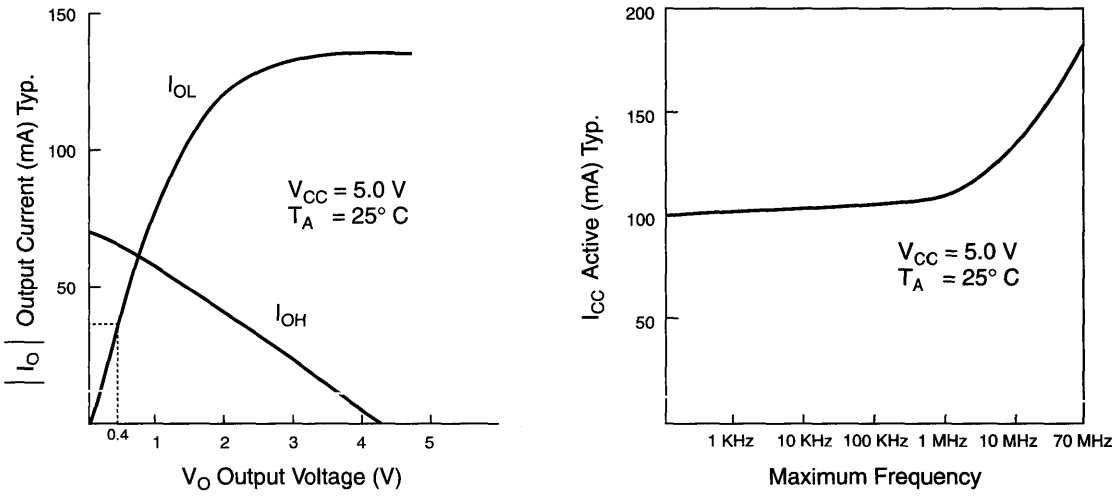


Table 1 shows the pin-outs for the EPS464 PQFP package.

Table 1. EPS464 PQFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	12	I/O	23	I/O	34	I/O
2	I/O	13	I/O	24	GND	35	I/O
3	I/O	14	I/O	25	I/O	36	GND
4	GND	15	I/O	26	I/O	37	INPUT/GCLK
5	I/O	16	GND	27	I/O	38	INPUT/GPREn
6	I/O	17	VCC	28	I/O	39	INPUT/GCLRn
7	I/O	18	I/O	29	VCC	40	INPUT/GOEn
8	I/O	19	I/O	30	I/O	41	VCC
9	VCC	20	I/O	31	I/O	42	I/O
10	I/O	21	I/O	32	I/O	43	I/O
11	I/O	22	I/O	33	I/O	44	I/O

Notes:

EPS448 SAM EPLD

Stand-Alone Microsequencer

September 1991, ver. 3 **Data Sheet**

Features

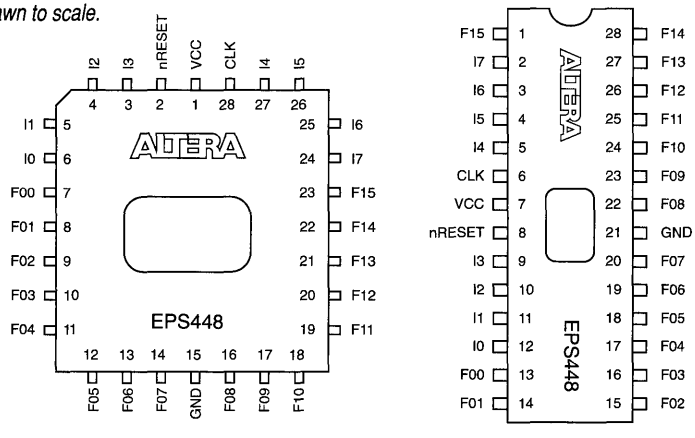
- ❑ User-configurable Stand-Alone Microsequencer (SAM) for implementing high-performance controllers
- ❑ On-chip reprogrammable microcode EPROM up to 448 words deep
- ❑ 15 × 8-bit stack
- ❑ Loop counter
- ❑ Prioritized multiway control branching
- ❑ 8 general-purpose branch-control inputs and 16 general-purpose control outputs
- ❑ Cascadable to expand the number of outputs or states
- ❑ Low-power CMOS technology
- ❑ Available in 28-pin, 300-mil windowed ceramic dual in-line packages (CerDIP) and 28-pin windowed ceramic and one-time-programmable (OTP) plastic J-lead chip carriers (JLCC and PLCC)
- ❑ Clock frequencies up to 30 MHz
- ❑ High-level support with SAM+PLUS design tools includes Altera State Machine Input Language (ASMILE), Assembly Language (ASM), SAM Design Processor (SDP), and SAMSIM functional simulator.

General Description

The EPS448 EPLD is a function-specific, user-configurable Stand-Alone Microsequencer (SAM). It is available in a 28-pin windowed ceramic and OTP plastic J-lead chip carrier, and 300-mil windowed ceramic DIP packages. See Figure 1.

Figure 1. EPS448 Package Pin-Out Diagrams

Package outlines not drawn to scale.



J-Lead DIP

The on-chip EPROM of each EPS448 device (up to 448 words) is integrated with branch-control logic, a pipeline register, a stack, and a loop counter. This generic microcoded architecture can efficiently implement a broad range of high-performance controllers, from state machines to waveform-generation applications.

The 1.2-micron CMOS EPROM technology allows the EPS448 EPLD to operate at 30-MHz clock frequency while still benefitting from low CMOS power consumption. This technology also facilitates 100% generic testability, which eliminates the need for post-programming testing.

Altera's SAM+PLUS software provides design entry, logic optimization, and functional simulation for EPS448 designs. With SAM+PLUS, designs are entered in either state machine or microcoded format. The software automatically performs logic minimization and design fitting. The designer can then simulate the design or program it directly to create customized working silicon. Programming takes only a few minutes with standard Altera programming hardware and LogicMap II software. New users can purchase the complete PLDS-SAM Development System with programming hardware included; PLS-SAM is a software-only package for existing Altera systems.

Applications

Ideal EPS448 applications include programmable sequence generators (i.e., state machines), bus and memory control functions, graphics and DSP algorithm controllers, and other high-performance control logic. EPS448 devices can be cascaded horizontally for greater output capabilities and vertically for deeper microcode memory. See *Application Brief 65 (Vertical Cascading of EPS448 SAM EPLDs).*

EPS448 as a State Machine

EPS448 architecture easily implements synchronous state machines. The device's internal EPROM memory and pipeline register allow up to 448 unique states to be specified. Its branch-control logic allows single-clock, multiway branching based on the eight inputs, the current device state, and the user-defined transition conditions. Design entry is simplified with the Altera State Machine Input Language (ASMILE) supported by SAM+PLUS software. This high-level language uses `IF-THEN` statements to define state transitions and truth tables to define or tri-state the outputs on a state-by-state basis.

EPS448 as a Microcoded Controller

EPS448 architecture provides several advanced features that make it suitable for use as a complex microcoded controller. The EPS448 EPLD's 448-word on-chip EPROM is integrated with a microcode sequencer consisting of branch-control logic, a stack, and a loop counter. The branch-control logic—

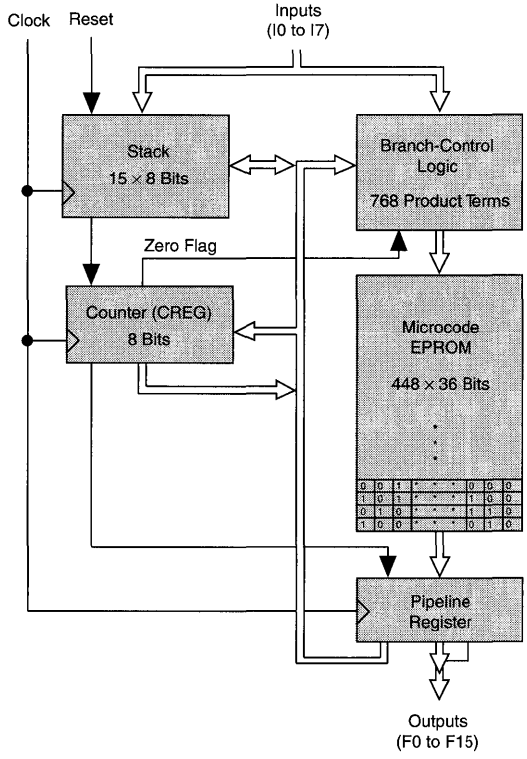
fed by the 8 general-purpose inputs, the counter, the stack, and the pipeline register—provides flexible, multiway microcode branch capability in a single clock cycle, enhancing throughput beyond that of conventional controllers or sequencers.

For microcoded controllers, SAM+PLUS software offers the high-level Assembly Language (ASM) design entry format. This language consists of powerful instructions (i.e., opcodes) that easily implement conditional branches, subroutine calls, multi-level `FOR-NEXT` loops, and dispatch functions (i.e., branching to an externally specified address). For more information, see "Instruction Set" later in this data sheet.

Functional Description

As shown in Figure 2, the EPS448 EPLD consists of microcode EPROM, a 36-bit pipeline register, branch-control logic, a 15 × 8-bit stack, and an 8-bit loop counter.

Figure 2. EPS448 Block Diagram



The branch-control logic generates the address of the next state and applies it to the microcode memory. The outputs of the microcode memory represent user-defined outputs and internal control values associated with the next state. These new values are clocked into the pipeline register on the leading edge of the clock and become the current state. The new values in the pipeline register—along with the counter, stack, and inputs—are used by the branch-control logic to generate the new next-state address.

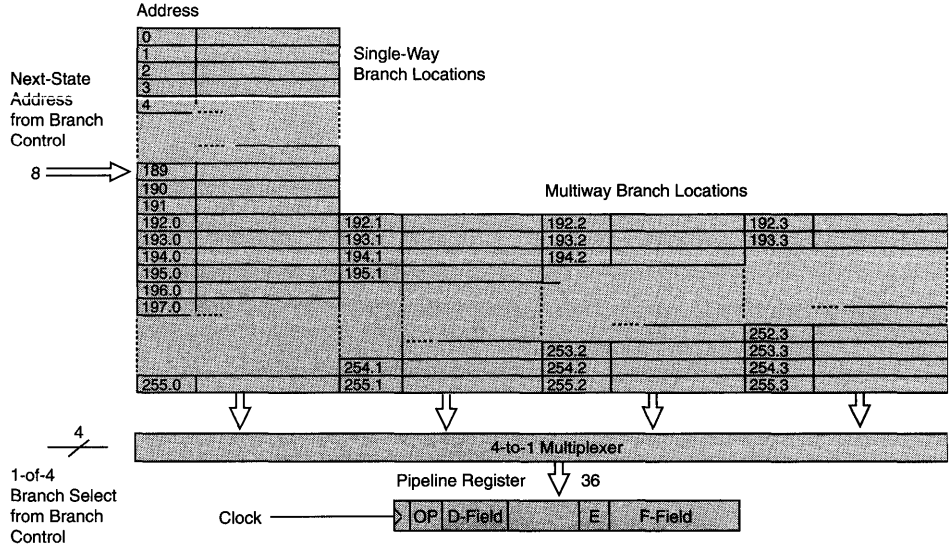
Microcode EPROM and Pipeline Register

The microcode EPROM is organized into 448 36-bit words, each of which can be viewed as a single state location. Each of the 36 bits is divided into the following categories:

F-field (16 bits) consists of user-defined outputs at device pins.
Q-field (8 bits) provides the next-state address.
D-field (8 bits) is a general-purpose field used either as a constant or as an alternative next-state address.
OP-field (3 bits) contains the instruction (opcode).
E-field (1 bit) enables or tri-states the device outputs.

As shown in Figure 3, the microcode memory is organized as 256 addresses. Addresses 0 through 191 contain a single 36-bit word, which is associated with the desired next state. This state information is clocked into the pipeline register on the rising edge of the clock, and the outputs become valid one clock-to-output delay (t_{CO}) later.

Figure 3. Microcode Memory



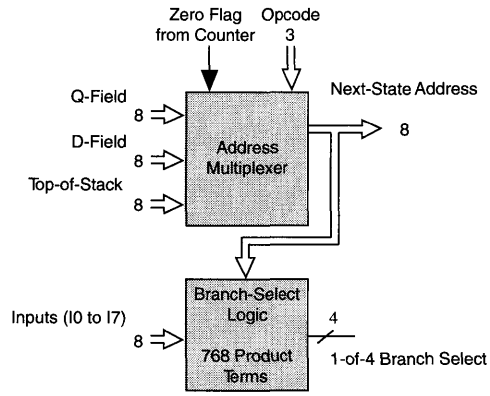
Addresses 192 through 255 access 4 unique 36-bit words, each of which corresponds to a different possible next state. (The extensions .0, .1, .2, and .3 are added to the addresses to distinguish the four states.) These 64 addresses make up the multiway branch locations, and are used to perform single-clock, four-way branching. Whenever the next-state address falls within the multiway branch locations, the branch-control logic makes the necessary 1-of-4 selection based on the next-state address and user-defined input conditions.

Branch-Control Logic Block

The branch-control logic is the key to the high-performance sequencing ability of the EPS448 EPLD. This block determines the next state to be clocked into the pipeline register, based on the current status of the pipeline register, the counter, the stack, and the eight input pins.

The branch-control logic is divided into two segments: the address multiplexer and the branch-select logic. See Figure 4.

Figure 4. Branch-Control Logic



The address multiplexer provides the next-state address to the microcode memory. The next-state address can come from the Q-field, the D-field, or the top-of-stack. The selection is based on the instruction in the pipeline register and the condition of the zero flag from the counter.

The branch-select logic is a programmable logic block with 768 product terms, 16 inputs, and 4 outputs. It is used to perform a 2-, 3-, or 4-way branch based on user-defined input conditions. When the next-state address falls within the multiway branch range of memory—i.e., any address greater than 191—the branch-select logic performs the necessary 1-of-4 selection. When the next-state address is less than 192, no selection is required and the branch-select logic is turned off.

The conditions controlling the multiway branch are defined by the user with a simple IF-THEN-ELSE format, as shown in the following example:

```
IF      (cond3)    THEN   select 201.3
ELSEIF  (cond2)    THEN   select 201.2
ELSEIF  (cond1)    THEN   select 201.1
ELSE                      select 201.0
```

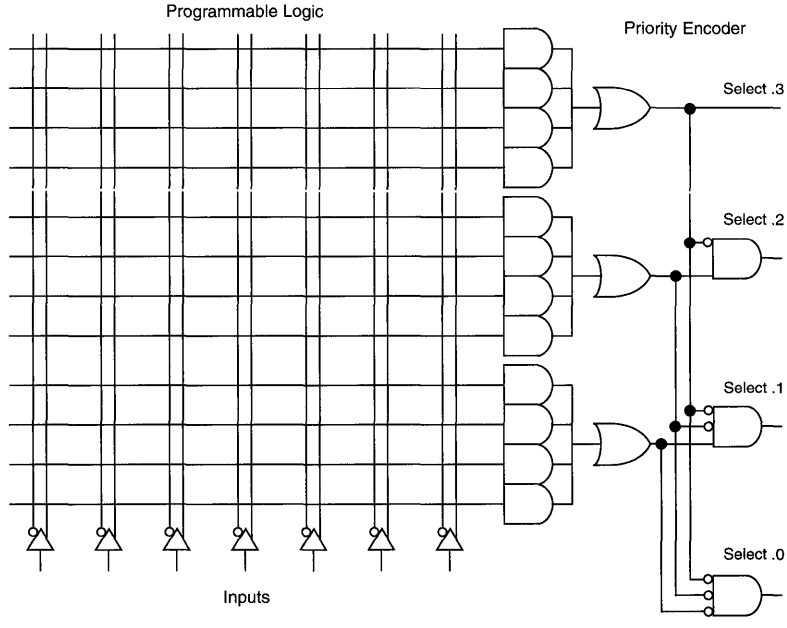
The conditions are prioritized so that if the first condition (i.e., cond3) is met, then microword 201.3 is selected and clocked into the pipeline register, regardless of the results of cond2 and cond1. If none of the conditions are met, then microword 201.0 is clocked into the pipeline register.

The three conditional expressions are user-defined. They may contain any logical equation that is based on the inputs and can be reduced to four product terms, as shown in the following example:

```
I1 * /I2 * /I4
+ I3 * /I4 * /I5 * /I6 * /I7
+ I0
+ I2 * /I4 * /I5
```

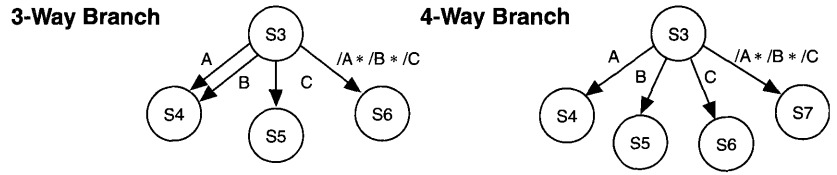
A unique set of 12 product terms is present in each of the 64 available multiway branch locations for a total of 768 product terms. See Figure 5.

Figure 5. Branch Logic in a Multiway Branch Location



The EPS448 EPLD is designed so that the number of available product terms is always sufficient for a design. Prioritization provides an effective product-term count of more than 12 per location. A tradeoff between the number of product terms and the number of possible branches can be made simply by placing identical state information in 2 locations, as shown in Figure 6.

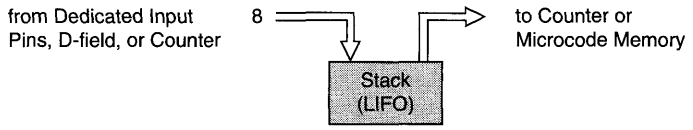
Figure 6. Multiway Branching vs. Product-Term Needs



Stack

The EPS448 stack is a Last-In First-Out (LIFO) arrangement that consists of 15 8-bit words. The top of stack may be used as the next-state address or popped into the counter. Values may be pushed onto the stack from either the D-field in the pipeline register or from the counter. Thus subroutines, nested loops, and other iterative structures may be implemented efficiently. The logic levels on the 8 dedicated input pins may also be pushed onto the stack to allow external address specification in a dispatch function or to externally load the counter. See Figure 7.

Figure 7. Stack



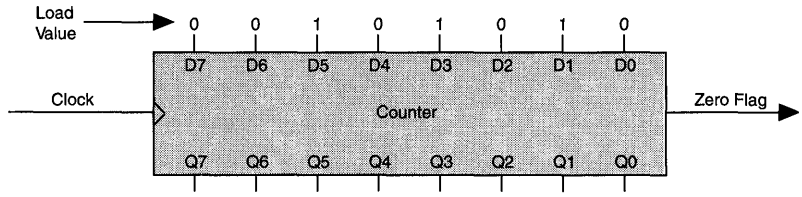
The pushing or popping of the stack occurs on the leading edge of the clock. The stack is "zero-filled" so that a pop from an empty stack will reset all 8 bits to zero. On the other hand, a push to an already full stack will write over the top-of-stack, leaving the other 14 values unchanged.

Loop Counter

The EPS448 EPLD contains an eight-bit loop counter called count register (CREG), which is useful for controlling timing loops and determining branch-control functions. The CREG is a down counter that may be loaded directly from the D-field of the pipeline register or from the top-of-stack.

The value of the CREG may be saved and restored by pushing and popping it to and from the stack. See Figure 8.

Figure 8. Loop Counter (CREG)



The CREG is loaded or decremented on the leading edge of the clock. It will not decrement once it reaches zero, thereby preventing roll-over. A zero flag indicates when the counter has reached zero. This flag is used with the LOOPNZ command to control program flow. (See "Instruction Set" later in this data sheet.) Single-instruction delay loops are easily constructed, and nested loops or delays of arbitrary length may be generated in combination with the stack.

Output Enable Control

Each microcode word contains an OE bit (i.e., the E-field) that enables the outputs when E = 1, and causes high impedance when E = 0. This bit is accessible through instruction set commands provided with SAM+PLUS software. This output-enable capability allows EPS448 EPLDs to be vertically cascaded to increase the number of states.

nRESET Pin

The nRESET pin acts as a master reset for the EPS448 EPLD, causing it to empty the stack, clear the counter, and load the microword at address 0 into the pipeline register. The nRESET signal is useful for system reset or for synchronizing several EPS448 devices that are cascaded vertically or horizontally.

The nRESET signal must be held low for at least three rising clock edges to reset the EPS448 EPLD. An nRESET of one rising clock edge causes the EPS448 device to enter into a supervisor mode; an nRESET of two clock edges leads to an undefined state.

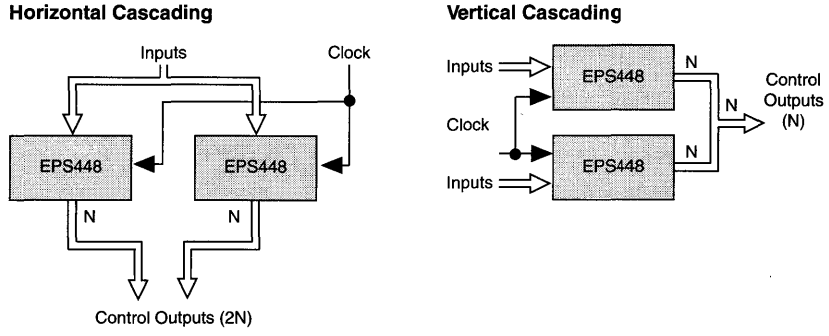
The outputs of the startup address (00 Hex) appear at the pins when the fourth clock edge after nRESET goes low, and are maintained until the third clock edge after nRESET returns to high.

When the EPS448 EPLD is operating in noisy environments, a glitch on the nRESET pin during one setup cycle (t_{SUR}) before the clock edge might initiate a supervisor mode. To prevent this effect, a capacitor of at least 0.1 µF should be connected from the nRESET input to ground.

Horizontal and Vertical Cascading

EPS448 EPLDs, like memory- and bit-slice devices, can be cascaded to provide greater functionality (Figure 9). If an application requires more output lines, two or more EPS448 devices can be cascaded horizontally. Likewise, if an application requires more states, two or more EPS448 EPLDs can be cascaded vertically. In either case, no speed penalty is incurred. The designer can also simultaneously cascade EPS448 devices horizontally and vertically. Designs with horizontal cascading are fully supported by the SAM+PLUS development software. However, vertical cascading requires the designer to make certain tradeoffs to split the design. Refer to *Application Brief 65 (Vertical Cascading of EPS448 SAM EPLDs)* for more information.

Figure 9. Horizontal and Vertical Cascading



Instruction Set

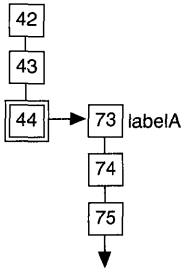
The instruction set used to enter designs for the EPS448 EPLD consists of a compact assortment of powerful commands that allows efficient implementation of multiway branching, subroutines, nested `FOR-NEXT` loops, and dispatch functions. These instructions are used only with Assembly Language (ASM) design entry.

Each command in the instruction set is described and illustrated here. In the following descriptions, `labelA` and `labelB` represent arbitrary labels located in the ASM file. These symbolic labels are converted by the SAM+PLUS software into 8-bit absolute addresses. (SAM+PLUS allows the designer to use the high-level Assembly Language without worrying about the actual values that are placed in the various fields.) The parameter constant is any 8-bit number (0 to 255 decimal, 0 to FF hexadecimal) that represents an address, a mask, or a constant.

For simplicity, it is assumed that the sample destination labels in the following descriptions are not in the multiway branch block. See "Multiway Branching" later in this data sheet for more details about this capability.

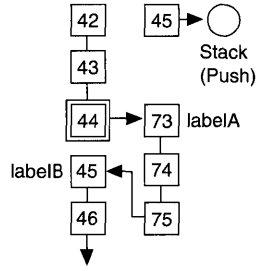
CONTINUE

This command causes execution to continue with the next sequential instruction in the ASM file. In this example, the current address is 44, and CONTINUE instructs SAM+PLUS to go to address 45 in the ASM file.



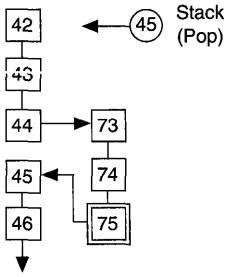
JUMP labelA

This instruction causes execution to branch to the indicated location. In this example, address 44 contains the instruction JUMP labelA ; labelA is located at address 73. The next instruction will come from labelA.



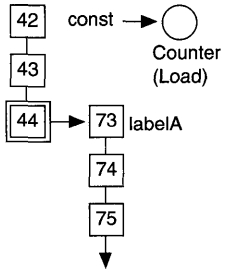
CALL labelA RETURNTO labelB

This instruction pushes the address of labelB onto the stack and makes labelA the next-state address. CALL labelA without the RETURNTO command makes labelB default to the next instruction in the ASM file. In this example, the address location 44 contains the instruction CALL labelA; labelA is located at address 73. The instruction pushes the address of the next instruction (45) onto the stack and causes the next instruction to come from address 73. The RETURN instruction at address 75 returns the execution to address 45. The CALL command is typically used to call a subroutine.



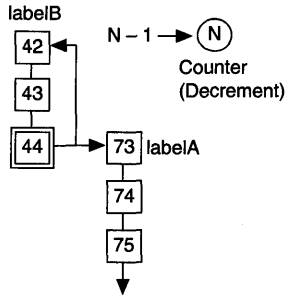
RETURN

This command causes the address of the next instruction to come from the top-of-stack and pops that value off the stack. In this example, the instruction at address 44 calls the subroutine at address 73 and pushes the value 45 onto the stack. The RETURN instruction at address 75 pops the value 45 off of the top-of-stack and causes execution to continue with address 45. RETURN is most frequently used to return from a subroutine.



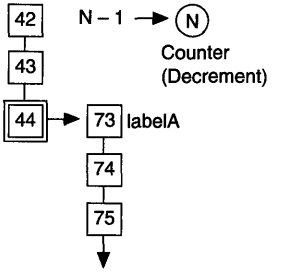
LOADC constant GOTO labelA

This command loads the counter with the specified value and then executes the instruction at labelA. If GOTO is not included in the instruction, labelA defaults to the next instruction in the ASM file. In this example, the instruction LOADC 173D GOTO labelA is located at address 44. This means that the decimal value 173 is loaded into the counter and the next state comes from labelA at address 73. LOADC is typically used to load the counter before entering a FOR-NEXT loop or a wait-state generator.



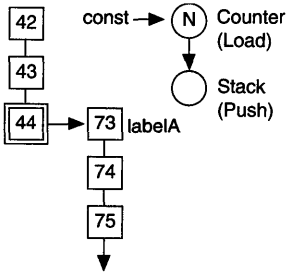
LOOPNZ labelB ONZERO labelA

This instruction jumps to one of two addresses based on the value of the zero flag, and decrements the counter if it is not already zero. If it is zero (i.e., zero flag = 1), the next instruction comes from labelA. If it is not zero (i.e., zero flag = 0), the next instruction comes from labelB. If the ONZERO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is LOOPNZ labelB ONZERO labelA, where labelB is located at address 42 and labelA at address 73. If the counter is not at zero, the instruction at address 42 is executed and the counter is decremented. If the counter is already at zero, the instruction at address 73 is executed and the counter remains at zero. LOOPNZ is typically used to implement FOR-NEXT loops.



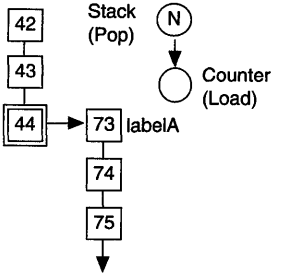
DECNZ GOTO labelA

This command decrements the counter if it is not zero and then jumps to the instruction specified at labelA. If GOTO is not included in the instruction, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is DECNZ GOTO labelA, where labelA is located at address 73. The counter is decremented if it is not zero and the next instruction comes from address 73. DECNZ is typically used to conditionally decrement the counter.



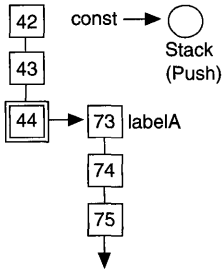
PUSHLOADC constant GOTO labelA

This instruction pushes the current value of the counter onto the stack, loads a new value into the counter, and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSHLOADC 153D GOTO labelA, where labelA is located at address 73. The value in the counter is pushed onto the stack, the decimal value 153 is loaded into the counter, and the next instruction comes from address 73. PUSHLOADC is useful for implementing FOR-NEXT loops.



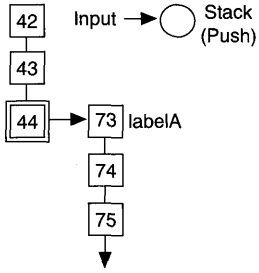
POPC GOTO labelA

This command pops the top-of-stack into the counter and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is POPC GOTO labelA, where labelA is located at address 73. The current value at the top-of-stack is removed from the stack (i.e., popped) and loaded into the counter. The next instruction comes from address 73. POPC is typically used with the PUSHLOADC instruction to implement nested FOR-NEXT loops.



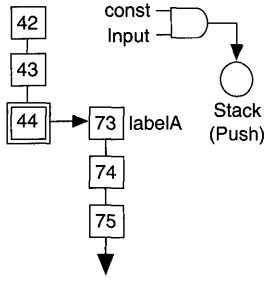
PUSH constant GOTO labelA

This command pushes the value of the constant onto the stack and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSH 34D GOTO labelA, where labelA is located at address 73. The decimal value 34 is pushed onto the stack and the next instruction comes from address 73. PUSH is typically used to store a value on the stack.



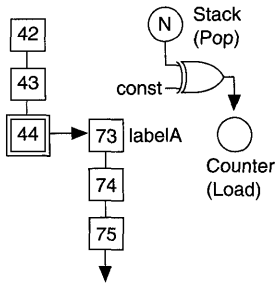
PUSHI GOTO labelA

This instruction pushes the eight inputs (I7 to I0) onto the stack. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSHI GOTO labelA, where labelA is located at address 73. At the leading edge of the clock, the eight inputs are pushed onto the stack. Typically, address 73 would have a RETURN instruction that would cause execution to jump to the address represented by the recently pushed input pins, implementing a dispatch function. This instruction can also be used to load the counter with an externally specified variable. To do so in this example, address 73 would have a POPC instruction.



ANDPUSHI constant GOTO labelA

This command pushes the eight inputs (I7 to I0) onto the stack. It is identical to the PUSHI GOTO labelA command, except that the inputs are first bit-wise ANDed with a constant to allow the masking of irrelevant inputs. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is ANDPUSHI 34D GOTO labelA, where labelA is located at address 73. At the leading edge of the clock, the eight inputs are masked with the decimal constant 34 and pushed onto the stack. The next instruction comes from address 73. ANDPUSHI is an advanced instruction typically used to branch to an externally specified resource or to externally load the counter.



POPXORC constant GOTO labelA

This instruction pops the top-of-stack, bit-wise XORs it with a constant, loads the results into the counter, and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is POPXORC 25D GOTO labelA, where labelA is located at address 73. The top-of-stack is popped off the stack, XORed with decimal 25, and the result is loaded into the counter. The next state comes from address 73. POPXORC is an advanced instruction typically used to compare the inputs against a known value and then branch on the basis of the result.

Table 1 summarizes the effects of each instruction on the address multiplexer, the stack, and the counter.

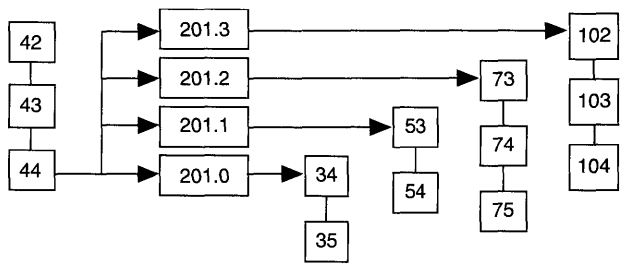
Table 1. Instruction Set Summary

Instruction	Definition	Next-State Address	Effect on Stack	Effect on Counter
CONTINUE	Continue with next instruction	labelA	None	Hold
JUMP	Jump to a label	labelA	None	Hold
CALL	Call subroutine	labelA	labelB	Hold
RETURN	Return from subroutine	labelA	Pop	Hold
LOADC	Load CREG	labelA	None	Constant
LOOPNZ	Loop/decrement on non-zero	labelA or labelB	None	Decrement
DECNZ	Decrement CREG on non-zero	labelA	None	Decrement
PUSHLOADC	Push CREG to stack and load CREG	labelA	CREG	Constant
POPC	Pop stack to CREG	labelA	Pop	Stack
PUSH	Push constant to stack	labelA	Push	Hold
PUSHI	Push inputs to stack	labelA	Inputs	Hold
ANDPUSHI	Push masked inputs to stack	labelA	Inputs (ANDed) Constant	Hold
POPXORC	XOR stack with constant and send result to CREG	labelA	Pop	Stack XOR Constant

Multiway Branching

Multiway branching provides an added dimension to the capabilities of the instruction set. For example, a JUMP labelA to an address within the multiway branch block forces the branch-select logic to decide which of the four words to send to the pipeline register. This selection is based on user-defined functions of the inputs. See Figure 10.

Figure 10. Jumping to a Multiway Branch Address



Any of the 13 available commands can be enhanced with multiway branching. For example, location 44 in Figure 10 can be a CALL to a subroutine, and address 201 can contain the starting instruction for 4 unique subroutines. The routine that is actually executed depends on the user-defined condition of the inputs. The following ASM code can be used to implement this example:

```
44D:    [Output Spec] CALL labelA;
201D:   IF          cond1     THEN  [out 1]    JUMP 102D;
           ELSEIF   cond2     THEN  [out 2]    JUMP 73D;
           ELSEIF   cond3     THEN  [out 3]    JUMP 53D;
           ELSE                     [out 4]    JUMP 34D;
```

Design Security

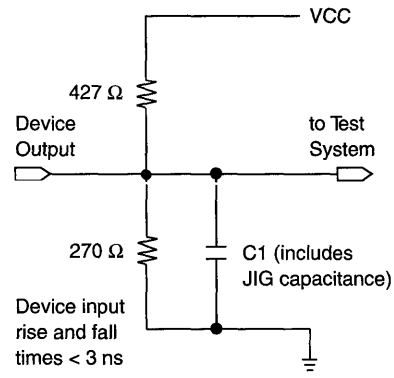
The EPS448 EPLD contains a programmable design Security Bit that controls access to the data programmed into the EPLD. If this Security Bit is used, a proprietary design implemented in the EPLD cannot be copied or retrieved. It provides a high level of design control because programmed data within EPROM cells is invisible. The Security Bit, along with all other program data, is reset by erasing the EPLD.

Functional Testing

The EPS448 EPLD is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. AC test measurements are performed under the conditions shown in Figure 11.

Figure 11. EPS448 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable input noise immunity.



Since the EPS448 EPLD is erasable, Altera can use and then erase test programs during early stages of production flow. This ability to use application-independent, general-purpose tests is called generic testing and is unique among user-defined LSI logic devices. EPS448 EPLDs also contain on-board test circuitry to allow verification of function and AC specifications after they are packaged in windowless packages.

Figure 12 shows output drive characteristics for EPS448 I/O pins and typical supply current versus frequency for the EPS448 EPLD.

Figure 12. EPS448 Output Drive Characteristics and I_{CC} vs. Frequency

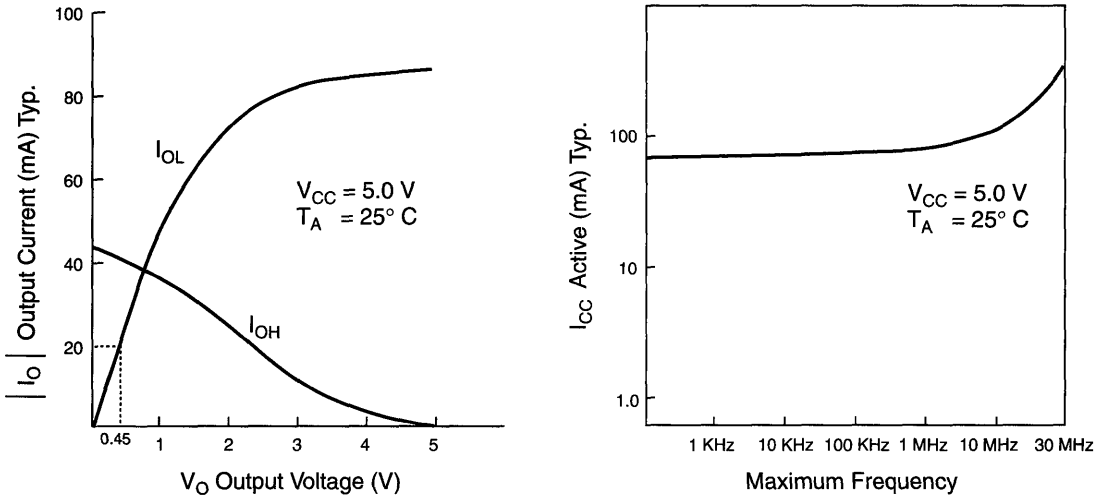
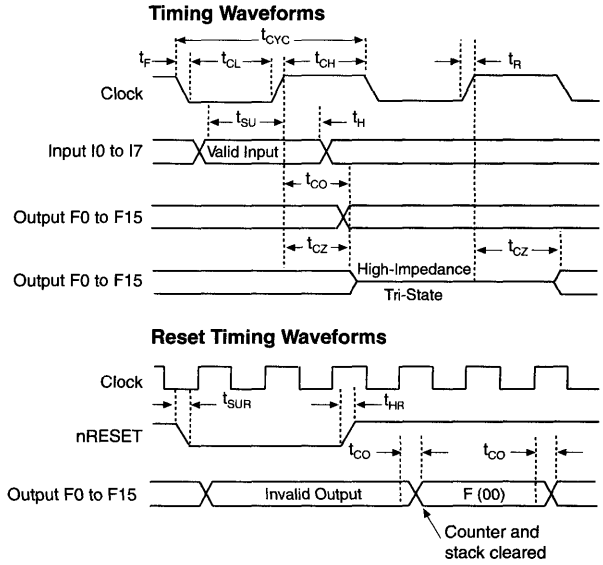


Figure 13 shows EPS448 timing and reset timing waveforms.

Figure 13. EPS448 Switching Waveforms

If nRESET is held low for more than three clock edges, then the outputs associated with the boot address (00 Hex) will remain at the pins until the third clock after nRESET goes high.



5 STG & SAM EPLDs

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–10	85	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			500 (100)	ns
t_F	Input fall time			500 (100)	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –8 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –4 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 8 (4) mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND, *See Note (5)*	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *See Note (6)*		60	95 (120)	mA
I_{CC3}	V_{CC} supply current (active)	No load, 50% duty cycle, f = 1.0 MHz		90	140 (200)	mA

Capacitance *See Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{RST}	nRESET pin capacitance			75	pF

AC Operating Conditions *See Note (3)*

			EPS448-30		EPS448-25		EPS448-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
f_{CYC}	Maximum frequency	C1 = 35 pF	30		25		20		MHz
t_{CYC}	Minimum clock cycle			33.3		40		50	ns
t_S	Input setup time		16.5		20		22		ns
t_H	Input hold time		0		0		0		ns
t_{CO}	Clock to output delay	C1 = 35 pF		16.5		20		22	ns
t_{CZ}	Clock to output disable or enable			16.5		20		22	ns
t_{CL}	Global clock low time		11		12		15		ns
t_{CH}	Global clock high time		11		12		15		ns
t_{SUR}	nRESET setup time		16.5		18		18		ns
t_{HR}	nRESET hold time		5		5		5		ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Typical values are for T_A = 25° C, V_{CC} = 5 V.
(5) For 1.0 < V_I < 3.8, the nRESET pin will source up to 200 µA.
(6) This condition applies when the present state is a single-way branch location.
(7) Capacitance is measured at 25° C. Sample-tested only.

Product Availability

Operating Temperature		Availbility
Commercial	(0° C to 70° C)	EPS448-20, EPS448-25, EPS448-30
Industrial	(–40° C to 85° C)	EPS448-20
Military	(–55° C to 125° C)	EPS448-20

Note: Only military temperature-range EPLDs are listed above. MIL-STD-883B-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Notes:

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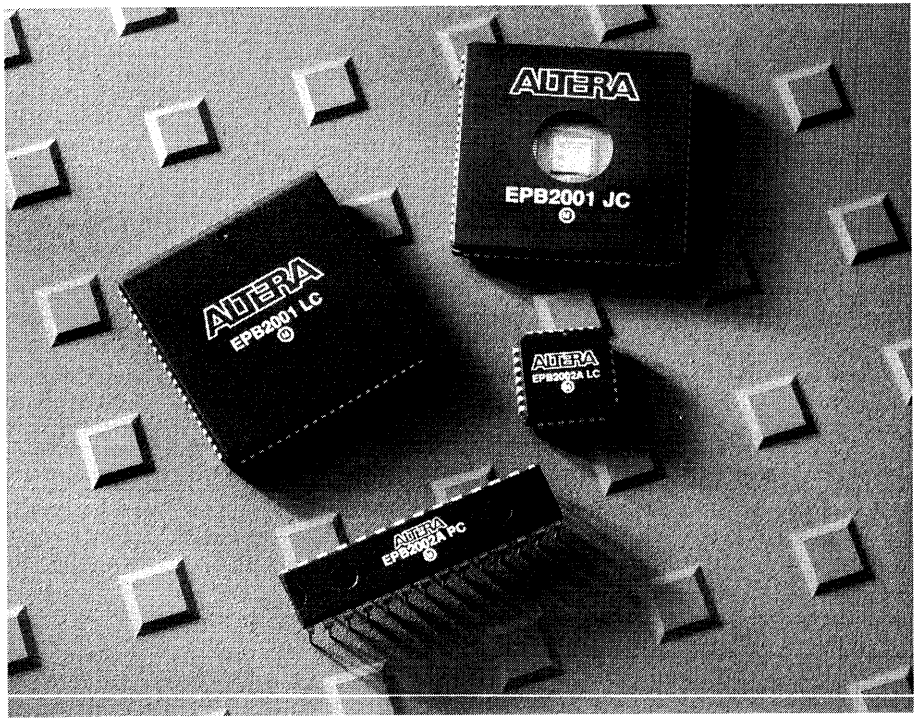
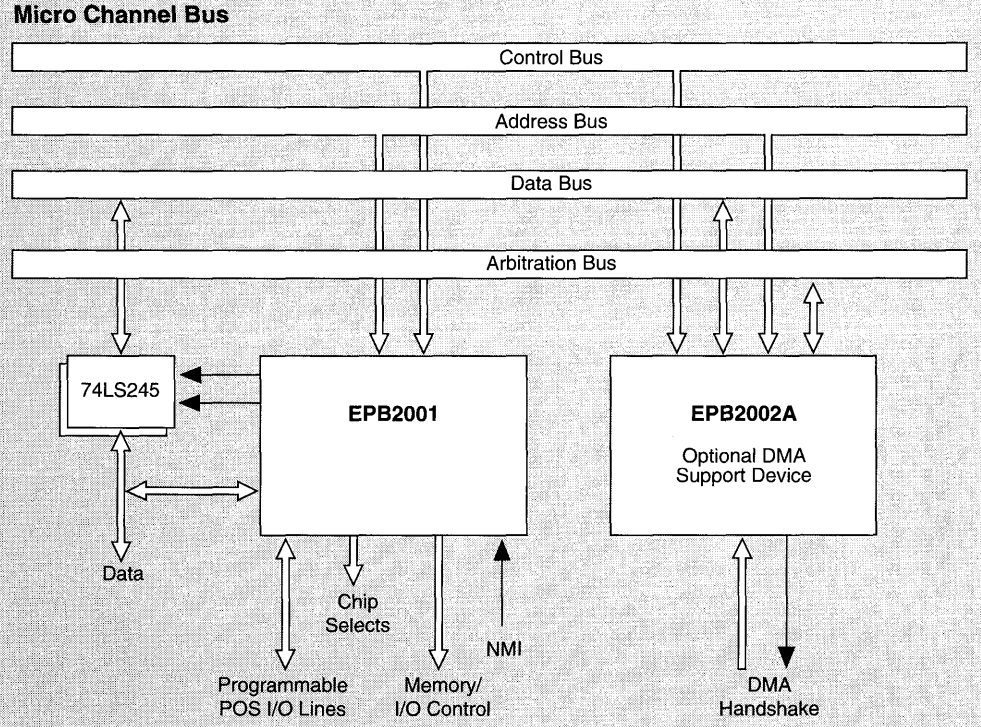
Section 6 Micro Channel EPLDs


ALTERA
EPB2001 JC
ALTERA
EPB2001 LC
ALTERA
ALTERA
EPB2202A PC

Micro Channel EPLDs

Altera User-Configurable Micro Channel Interface



- 100% Micro Channel-compatible architecture eliminates design debug problems and allows faster board design time.
- 30-mA power-supply current conserves limited board power for memory, I/O, and other essential ICs.
- 25-ns address decoding supports high-speed, zero "wait-state" data transfers.
- EPROM board ID POS registers eliminate extra ID registers.
- Programmable POS register I/O gives the designer a choice of POS bits accessible on board.
- Multiple I/O or address decode ranges (up to 8 per chip-select output) provide multiple addressing options for the designer's board.
- 8 programmable chip-select outputs eliminate the need for extra address decoder PLDs and glue logic ICs.
- 24 Micro Channel address inputs support full address decoding from the Micro Channel bus.
- 24-mA current drive outputs eliminate extra buffer ICs.
- Channel-check interrupt support enables the board to use bus Non-Maskable Interrupts for fast CPU interrupt response.
- Optional 28-pin EPB2002A EPLD provides DMA arbitration support.
- Altera's MCMap Development System simplifies Micro Channel design and eliminates design errors.
- See the ***Micro Channel Adapter Handbook*** for more information.

Contents

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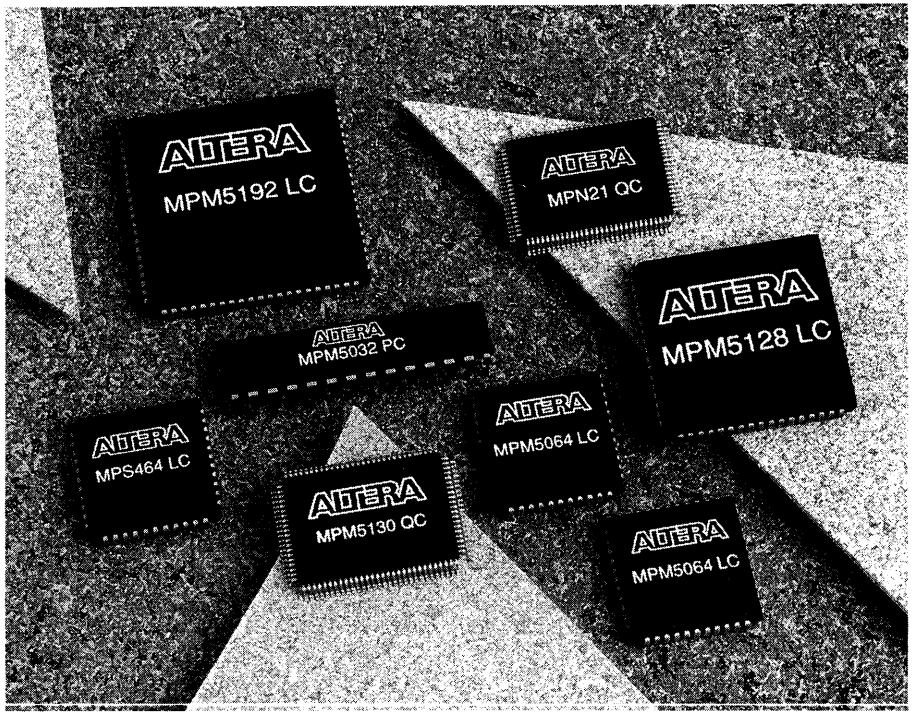
Section 7 **MPLDs**


ALTERA
MPM5192 LC
ALTERA
MPN21 QC
ALTERA
MPM5128 LC
ALTERA
MPM5032 PC
ALTERA
MPM5064 LC
ALTERA
MPS464 LC
ALTERA
MPM5130 QC
ALTERA
MPM5064 LC

MPLDs
Mask-Programmed Logic Devices

September 1991, ver. 1 **Data Sheet**

Features

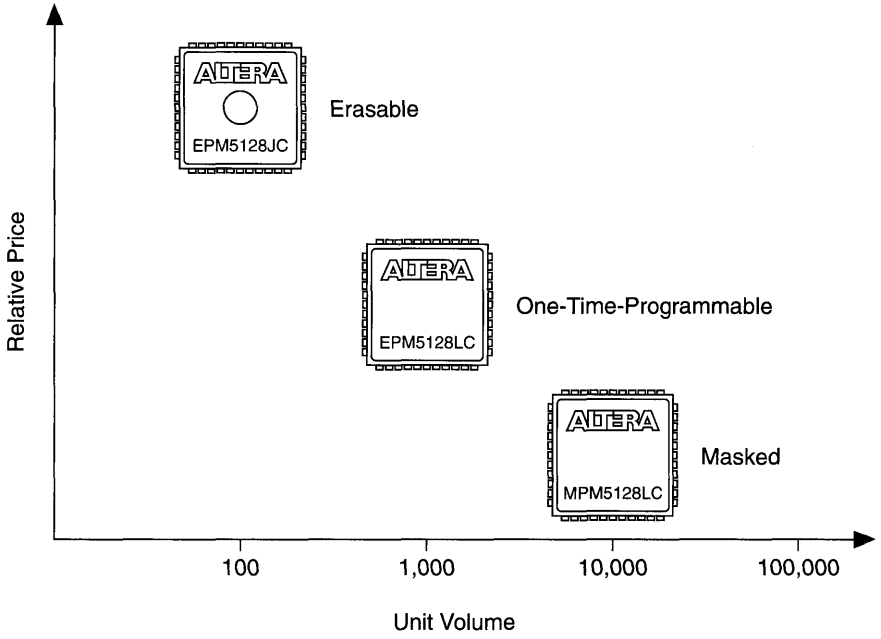
- Masked versions of EPLD designs
- Reduced cost for large-volume applications
- Available for EP1810, EPM5032, EPM5064, EPM5128, EPM5130, EPM5192, and EPS464 EPLDs
- Pin-, function-, and timing-compatible with original EPLD design
- Conversion process handled by Altera
- Fast turn-around to reduce time-to-market
- Test vectors generated by Altera
- Low power
- *N*-to-1 option combines multiple EPLDs into a single MPLD

General Description

The Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to EPLD designs. By using a generic CMOS process and removing all EPROM cells, Altera passes considerable savings on to customers who anticipate high-volume production. The combination of Altera EPLDs and MPLDs provides the best of both worlds: the fast time-to-market offered by EPLDs, and the low cost and low risk offered by MPLDs. See Figure 1.

Figure 1. EPLD/MPLD Economics

As volumes increase during production, a design can move from windowed ceramic EPLDs to one-time-programmable EPLDs, and finally to MPLDs.



The EPLD-to-MPLD conversion is handled by Altera so that no redesign effort is required. Altera guarantees that the MPLD meets the worst-case AC and DC parameters of the original EPLD design. In addition, Altera automatically generates test vectors with over 95% fault coverage.

EPLD/MPLD Compatibility

An Altera MPLD is guaranteed to be pin-, function-, and timing-compatible with the original EPLD design. This guarantee ensures that the MPLD can replace the EPLD without interrupting production.

Pin compatibility guarantees that both the pin-out and DC specifications of the MPLD match those of the original EPLD design. In addition, the MPLD typically will consume less than one-tenth of the power of the equivalent EPLD, depending on the design and operating conditions.

Functional compatibility of the MPLD is ensured by directly mapping the primitives within the EPLD (product terms, programmable flip-flops, etc.) to specially designed elements within the MPLD. Altera employs a proprietary logic synthesis program that uses the Simulator Netlist File (.SNF) generated by MAX+PLUS or MAX+PLUS II software. (Designs developed with A+PLUS software are converted to MAX+PLUS II format.) The SNF reflects the final synthesis, placement, and routing of the original EPLD design. The conversion process pays special attention to the wide fan-in of product terms and the wide fan-out of registers commonly found in EPLD applications.

An MPLD is guaranteed to meet the worst-case timing parameters of the corresponding EPLD, as specified in the EPLD data sheet. Provided that the design engineer performs worst-case analysis of the EPLD, the same analysis will hold for the MPLD. Therefore, the timing of the original design and the overall system is maintained when the EPLD is replaced with an MPLD.

Design for Testability

Test vector generation is one of the most time-consuming tasks required for ASIC design. A significant advantage of EPLDs is that they are fully tested before they are shipped and are verified at programming time; test vectors are not required.

MPLD designs include a partial-scan testing structure that parallels the testability available in EPLDs. The partial-scan structure allows Altera to create test vectors with over 95% fault coverage for all stuck-at and open faults. This high fault coverage is maintained regardless of whether synchronous or asynchronous design techniques are used.

The built-in design-for-testability frees the design engineer from the burden of creating a testable design and test vectors. In fact, customer-provided simulation vectors are optional for EPLD-to-MPLD conversions.

N-to-1 MPLD Conversion Option

Many applications use multiple EPLDs on a single board for both prototyping and production. In some applications it may be desirable to perform prototyping with multiple EPLDs, but shift to a single-device implementation for high-volume production. Altera's EPLD-to-MPLD conversion program provides this capability with the "*N*-to-1" conversion option, which offers the benefits of developing with EPLDs even when production constraints require a high-density single-device solution.

The *N*-to-1 MPLD conversion works in conjunction with the design partitioning feature in MAX+PLUS II software. Partitioning allows a design engineer to create a large design without concern for design size or fitting constraints. MAX+PLUS II automatically partitions the design and fits each portion into a separate EPLD. Multiple EPLDs can be used for design prototyping while simulation and timing analysis can be completed on the top-level design.

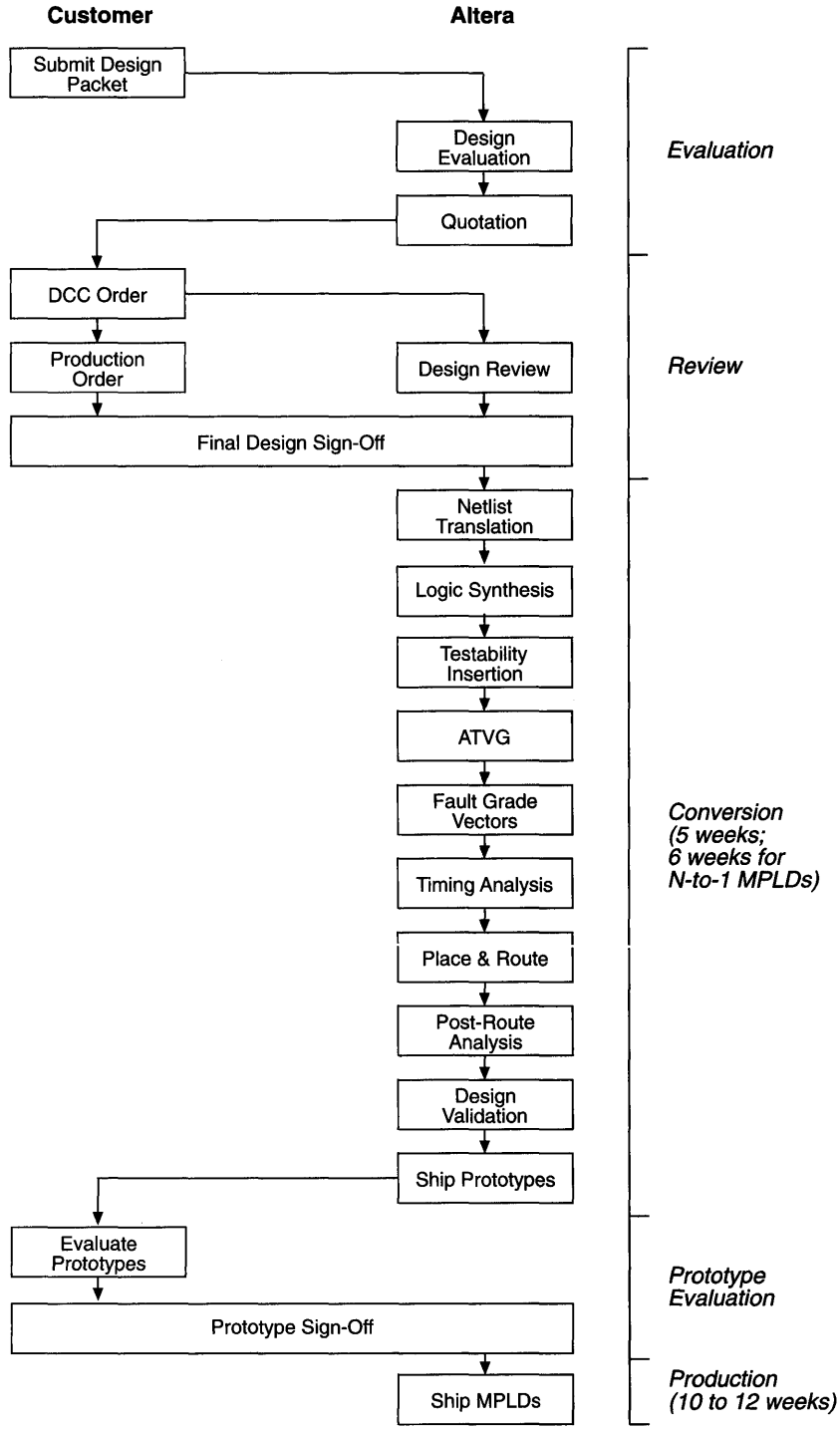
The *N*-to-1 option combines a multi-EPLD design into a single MPLD that is function- and timing-compatible with the original multi-EPLD solution. The package and pin-out are determined by the application's requirements. A wide range of package options is available.

Quick, Seamless Conversion

One of the principal objectives of Altera's EPLD-to-MPLD conversion program is to minimize the design engineer's involvement in the conversion. The engineer simply submits design files created with A+PLUS, MAX+PLUS, or MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off. By handling the conversion process, Altera frees the engineer to begin developing the next-generation project.

The MPLD design flow chart (see Figure 2) shows how easily an EPLD can be converted to an MPLD. To submit a design for quotation, an ***MPLD Conversion Information & Order Forms*** workbook can be obtained from the local Altera representative. The design engineer needs only to submit the design files and the workbook's *Checklist*, *Information Form*, and *Questionnaire* to Altera. Altera then performs a design evaluation and returns a price quote for the conversion.

Figure 2. MPLD Conversion Design Flow



After the customer submits an order for the Design Conversion Cost (DCC), an Altera engineer reviews the design and submits a *Final Design Sign-Off Form* for customer approval. This form describes the specifications of the MPLD in detail. After sign-off, Altera begins the design conversion.

The design conversion includes netlist translation, logic synthesis, testability insertion, Automatic Test Vector Generation (ATVG), fault grading, timing analysis, place-and-route, post-route timing analysis, design validation, and the manufacture of the prototypes. The entire conversion, from final design sign-off to prototype delivery, takes less than 5 weeks (6 weeks for *N*-to-1 conversion). Production quantities are delivered 10 to 12 weeks after the customer returns the *Prototype Sign-Off Form*.

Conclusion

The two most important design goals faced by engineers today are reducing time-to-market and system cost. The combination of Altera EPLDs and MPLDs provides a solution that fills these needs, allowing a company to take a product to market quickly, without raising the cost or risk of production.

Notes:

Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EP1810/EP1800 EPLD designs
- Zero-power operation (typically 10 µA standby)
- Active power of 10 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 50-MHz clock rates
- TTL and CMOS I/O compatibility
- MAX+PLUS II and A+PLUS development system support, featuring schematic capture, Boolean equation, state machine, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and functional and timing simulation (AHDL, waveform design entry, and timing simulation available only in MAX+PLUS II software)
- Available in a plastic 68-pin J-lead chip carrier (PLCC) package

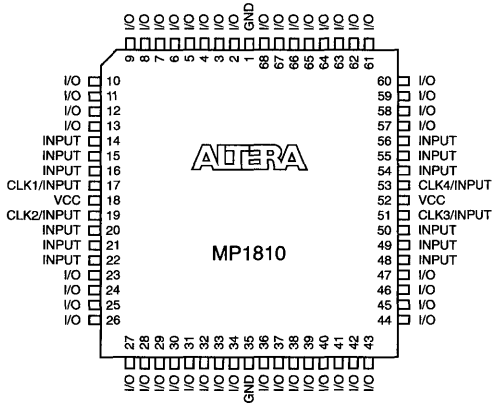
General Description

Altera's MP1810 MPLD provides a high-volume replacement for EP1810/EP1800 designs. It is pin-, function- and timing-compatible with existing EP1810/EP1800 designs. MP1810 designs are created with Altera's MAX+PLUS II or A+PLUS development system and prototyped with EP1810 EPLDs. The source files are then converted to produce the MPLD. The MP1810 MPLD is available in a 68-pin PLCC package. See Figure 3.

This data sheet provides minimum and maximum AC and DC parametric values for the MP1810 MPLD. For additional information, refer to the *EP1810 EPLDs: High-Performance 48-Macrocell Devices Data Sheet* in this data book.

Figure 3. MP1810 Package Pin-Out Diagram

Package outline not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			50	ns
t_F	Input fall time			50	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		10		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		0.5		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *See Note (3)*

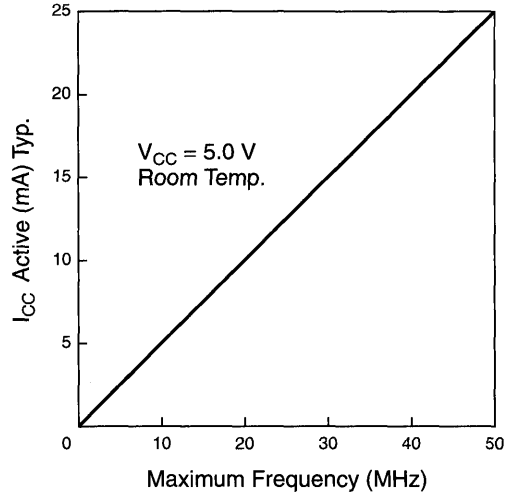
External Timing Parameters			MP1810-25		MP1810-35		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		35	ns
t_{PD2}	I/O input to non-registered output			28		40	ns
t_{SU}	Global clock setup time		17		25		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		18		20	ns
t_{CH}	Global clock high time		10		12		ns
t_{CL}	Global clock low time		10		12		ns
t_{ASU}	Array clock setup time		10		10		ns
t_{AH}	Array clock hold time		10		15		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		35	ns
t_{CNT}	Minimum global clock period			25		35	ns
f_{CNT}	Maximum internal frequency	*See Note (4)*	40		28.6		MHz
f_{MAX}	Maximum clock frequency	*See Note (5)*	50		40		MHz

Notes to tables:

1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
4) Measured with a device programmed as four 12-bit counters.
5) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 4 shows typical supply current versus frequency for MP1810 MPLDs.

Figure 4. MP1810 I_{CC} vs. Frequency



Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EPM5032 EPLD designs
- Zero-power operation (typically 8 µA standby)
- Active power of 8 mA at 20 MHz
- High speed (t_{PD} = 20 ns) with 71-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in plastic 28-pin dual in-line (PDIP) and J-lead chip carrier (PLCC) packages

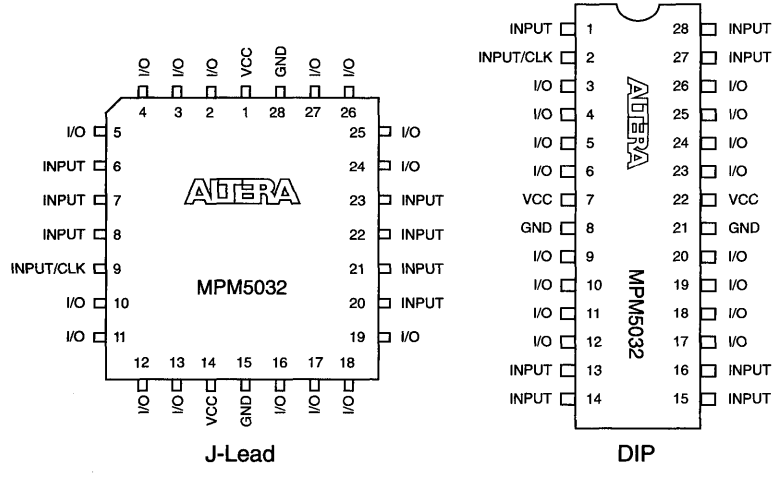
General Description

Altera's MPM5032 MPLD provides a high-volume replacement for EPM5032 designs. It is pin-, function-, and timing-compatible with existing EPM5032 designs. MPM5032 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5032 EPLDs. The source files are then converted to produce the MPLD. The MPM5032 MPLD is available in 28-pin DIP and PLCC packages. See Figure 5.

This data sheet provides minimum and maximum AC and DC parametric values for the MPM5032 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Figure 5. MPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		8		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		0.4		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

IC Operating Conditions *See Note (3)*

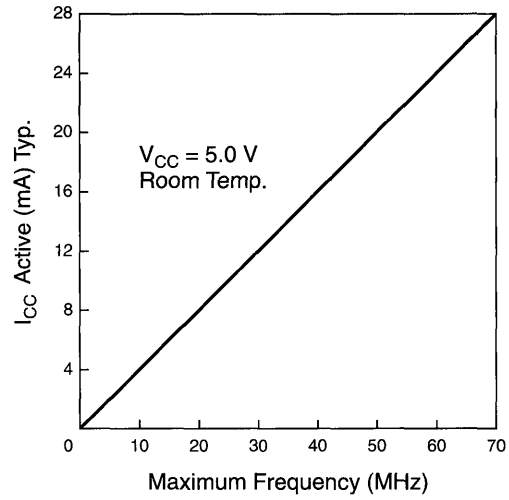
External Timing Parameters			MPM5032-20 *Note (5)*		MPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		7		8		ns
t_{CL}	Global clock low time		7		8		ns
t_{ASU}	Array clock setup time		9		12		ns
t_{AH}	Array clock hold time		9		12		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	ns
t_{ACH}	Array clock high time	*See Note (6)*	7		9		ns
t_{ACL}	Array clock low time		9		11		ns
t_{CNT}	Minimum global clock period			16		20	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	62.5		50		MHz
t_{ACNT}	Minimum array clock period			16		20	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	62.5		50		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	71.4		62.5		MHz

Notes to tables:

1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
4) Measured with a device programmed as a 32-bit counter.
5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
7) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 6 shows typical supply current versus frequency for MPM5032 MPLDs.

Figure 6. MPM5032 I_{CC} vs. Frequency



Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EPM5064 EPLD designs
- Zero-power operation (typically 15 µA standby)
- Active power of 15 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 62.5-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in a 44-pin plastic J-lead chip carrier package (PLCC)

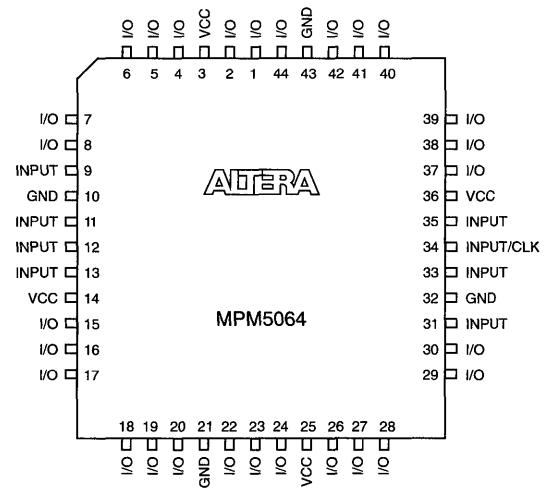
General Description

Altera's MPM5064 MPLD provides a high-volume replacement for EPM5064 designs. It is pin-, function-, and timing-compatible with existing EPM5064 designs. MPM5064 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5064 EPLDs. The source files are then converted to produce the MPLD. The MPM5064 MPLD is available in a 44-pin PLCC package. See Figure 7.

This data sheet provides minimum and maximum AC and DC parametric values for the MPM5064 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Figure 7. MPM5064 Package Pin-Out Diagram

Package outline not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		15		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		0.75		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (3)*

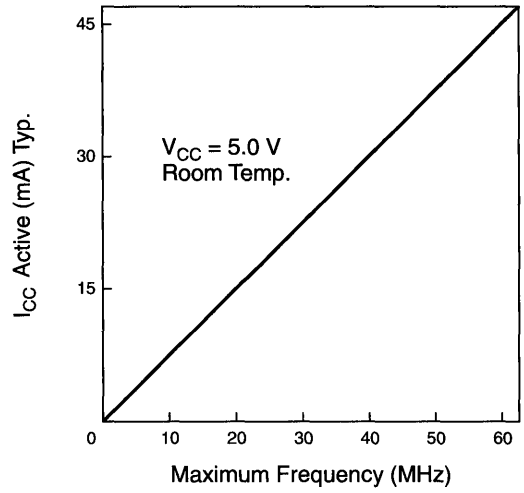
External Timing Parameters			MPM5064-1 *Note (5)*		MPM5064-2		MPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
(3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
(4) Measured with a device programmed as four 16-bit counters.
(5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 8 shows typical supply current versus frequency for MPM5064 MPLDs.

Figure 8. MPM5064 I_{CC} vs. Frequency



Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EPM5128 EPLD designs
- Zero-power operation (typically 25 µA standby)
- Active power of 30 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 62.5-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in a 68-pin plastic J-lead chip carrier package (PLCC)

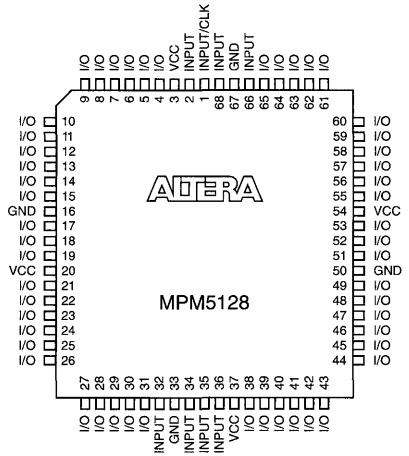
General Description

Altera's MPM5128 MPLD provides a high-volume replacement for EPM5128 designs. It is pin-, function-, and timing-compatible with existing EPM5128 designs. MPM5128 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5128 EPLDs. The source files are then converted to produce the MPLD. The MPM5128 MPLD is available in a 68-pin PLCC package. See Figure 9.

This data sheet provides minimum and maximum AC and DC parametric values for the MPM5128 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Figure 9. MPM5128 Package Pin-Out Diagram

Package outline not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		25		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		1.5		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (3)*

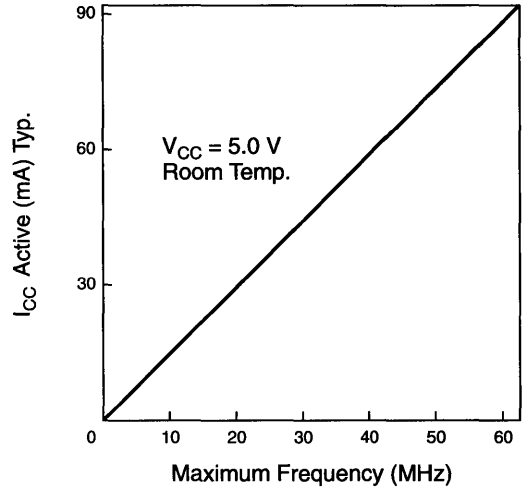
External Timing Parameters			MPM5128-1 *Note (5)*		MPM5128-2		MPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Notes to tables:

1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
4) Measured with a device programmed as eight 16-bit counters.
5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
7) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 10 shows typical supply current versus frequency for MPM5128 MPLDs.

Figure 10. MPM5128 I_{CC} vs. Frequency



Features

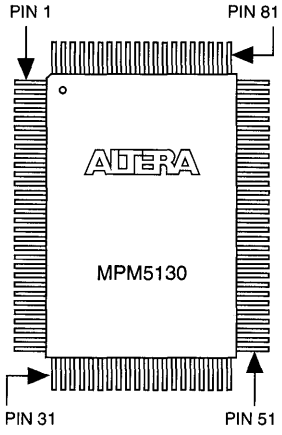
- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EPM5130 EPLD designs
- Zero-power operation (typically 25 µA standby)
- Active power of 30 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 62.5-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in 100-pin plastic quad flat pack (QFP) and pin-grid array (PGA) packages

General Description

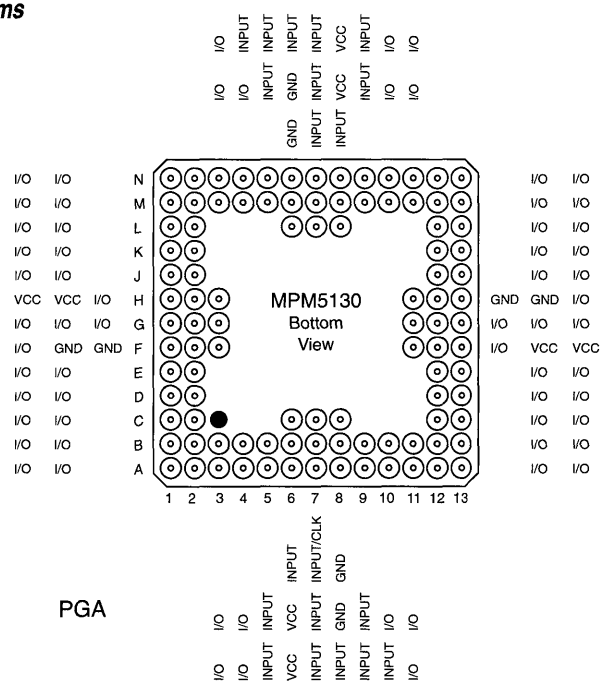
Altera's MPM5130 MPLD provides a high-volume replacement for EPM5130 designs. It is pin-, function-, and timing-compatible with existing EPM5130 designs. MPM5130 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5130 EPLDs. The source files are then converted to produce the MPLD. The MPM5130 MPLD is available in 100-pin QFP and PGA packages. See Figure 11.

Figure 11. MPM5130 Package Pin-Out Diagrams

See Table 1 in this data sheet for QFP pin-outs.
Package outlines not drawn to scale.



QFP



PGA

This data sheet provides minimum and maximum AC and DC parametric values for the MPM5130 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		25		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		1.5		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (3)*

External Timing Parameters			MPM5130-1 *Note (5)*		MPM5130-2		MPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Measured with a device programmed as eight 16-bit counters.
(5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 12 shows typical supply current versus frequency for MPM5130 MPLDs. Table 1 shows the pin-outs for the MPM5130 QFP package.

Figure 12. MPM5130 I_{CC} vs. Frequency

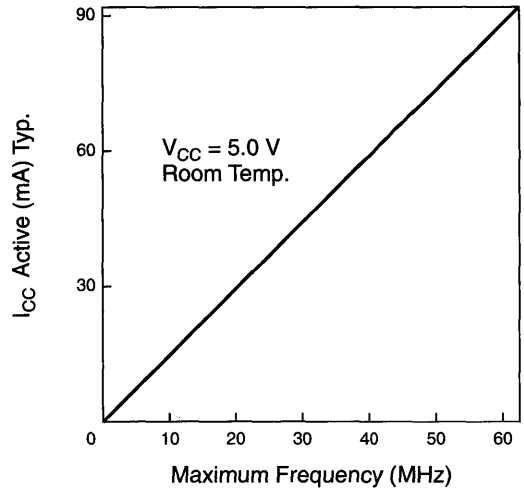


Table 1. MPM5130 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	21	INPUT	41	I/O	61	INPUT	81	I/O
2	I/O	22	INPUT	42	I/O	62	GND	82	I/O
3	I/O	23	I/O	43	VCC	63	GND	83	I/O
4	I/O	24	I/O	44	VCC	64	INPUT	84	I/O
5	I/O	25	I/O	45	I/O	65	INPUT	85	I/O
6	I/O	26	I/O	46	I/O	66	INPUT	86	I/O
7	I/O	27	I/O	47	I/O	67	INPUT	87	GND
8	I/O	28	I/O	48	I/O	68	VCC	88	GND
9	INPUT	29	I/O	49	I/O	69	VCC	89	I/O
10	INPUT	30	I/O	50	I/O	70	INPUT	90	I/O
11	INPUT	31	I/O	51	I/O	71	INPUT	91	I/O
12	GND	32	I/O	52	I/O	72	INPUT	92	I/O
13	GND	33	I/O	53	I/O	73	I/O	93	VCC
14	INPUT	34	I/O	54	I/O	74	I/O	94	VCC
15	INPUT	35	I/O	55	I/O	75	I/O	95	I/O
16	INPUT/CLK	36	I/O	56	I/O	76	I/O	96	I/O
17	INPUT	37	GND	57	I/O	77	I/O	97	I/O
18	VCC	38	GND	58	I/O	78	I/O	98	I/O
19	VCC	39	I/O	59	INPUT	79	I/O	99	I/O
20	INPUT	40	I/O	60	INPUT	80	I/O	100	I/O

Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EPM5192 EPLD designs
- Zero-power operation (typically 30 µA standby)
- Active power of 40 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 62.5-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in 84-pin plastic J-lead chip carrier (PLCC) and 100-pin plastic quad flat pack (QFP) packages

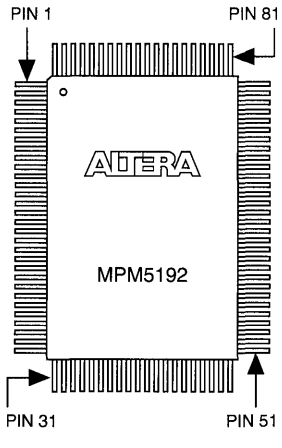
General Description

Altera's MPM5192 MPLD provides a high-volume replacement for EPM5192 designs. It is pin-, function-, and timing-compatible with existing EPM5192 designs. MPM5192 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5192 EPLDs. The source files are then converted to produce the MPLD. The MPM5192 is available in 84-pin PLCC and 100-pin QFP packages. See Figure 13.

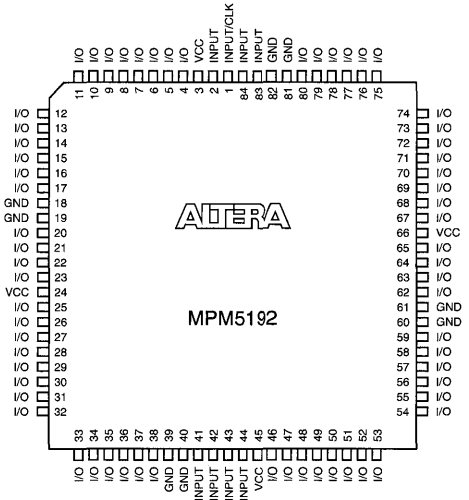
This data sheet provides minimum and maximum AC and DC parametric values for the MPM5192 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Figure 13. MPM5192 Package Pin-Out Diagrams

See Table 2 in this data sheet for QFP pin-outs. Package outlines not drawn to scale.



QFP



J-Lead

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		30		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		2.3		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (3)*

External Timing Parameters			MPM5192-1 *Note (5)*		MPM5192-2		MPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
(3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
(4) Measured with a device programmed as twelve 16-bit counters.
(5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 14 shows typical supply current vs. frequency for MPM5192 MPLDs. Table 2 shows the pin-outs for the MPM5192 QFP package.

Figure 14. MPM5192 I_{CC} vs. Frequency

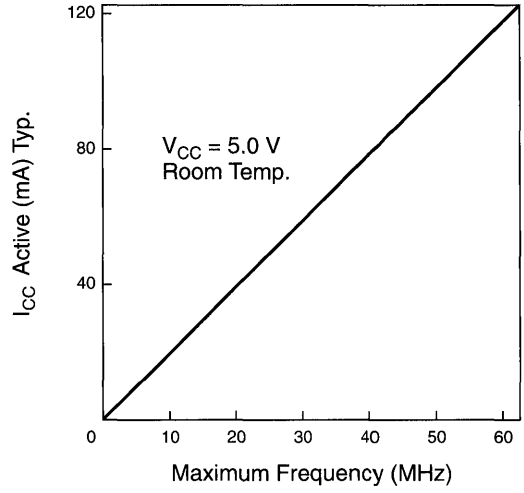


Table 2. MPM5192 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	21	I/O	41	INPUT	61	I/O	81	I/O
2	NC	22	I/O	42	INPUT	62	GND	82	I/O
3	NC	23	I/O	43	VCC	63	GND	83	I/O
4	NC	24	I/O	44	NC	64	I/O	84	I/O
5	I/O	25	I/O	45	I/O	65	I/O	85	I/O
6	I/O	26	I/O	46	I/O	66	I/O	86	I/O
7	I/O	27	I/O	47	I/O	67	I/O	87	GND
8	I/O	28	NC	48	I/O	68	NC	88	GND
9	I/O	29	NC	49	I/O	69	VCC	89	INPUT
10	I/O	30	NC	50	I/O	70	I/O	90	INPUT
11	I/O	31	I/O	51	I/O	71	I/O	91	INPUT/CLK
12	GND	32	I/O	52	NC	72	I/O	92	INPUT
13	GND	33	I/O	53	NC	73	I/O	93	VCC
14	I/O	34	I/O	54	NC	74	I/O	94	NC
15	I/O	35	I/O	55	I/O	75	I/O	95	I/O
16	I/O	36	I/O	56	I/O	76	I/O	96	I/O
17	I/O	37	GND	57	I/O	77	I/O	97	I/O
18	NC	38	GND	58	I/O	78	NC	98	I/O
19	VCC	39	INPUT	59	I/O	79	NC	99	I/O
20	I/O	40	INPUT	60	I/O	80	NC	100	I/O

Note: NC represents "not connected."

Features

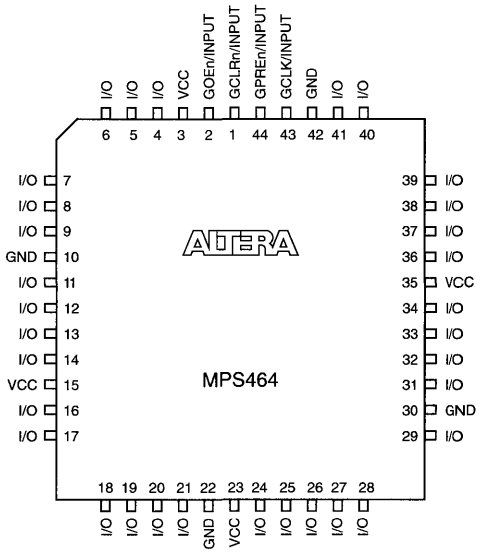
- CMOS, Mask-Programmed Logic Device (MPLD) ideal for implementing synchronous timing logic functions
- High-volume replacement for EPS464 EPLD designs
- Zero-power operation (typically 15 µA standby)
- Active power of 15 mA at 20 MHz
- High speed (t_{PD} = 20 ns) with 71-MHz clock rates
- TTL I/O compatibility
- MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- Available in 44-pin plastic J-lead chip carrier (PLCC) package

General Description

Altera's MPS464 MPLD provides a high-volume replacement for EPS464 designs. It is pin-, function-, and timing-compatible with existing EPS464 designs. MPS464 designs are created with Altera's MAX+PLUS II development system and prototyped with EPS464 EPLDs. The source files are then converted to produce the MPLD. The MPS464 MPLD is available in a 44-pin PLCC package. See Figure 15.

Figure 15. MPS464 Package Pin-Out Diagram

Package outline not drawn to scale.



J-Lead

This data sheet provides minimum and maximum AC and DC parametric values for the MPS464 MPLD. For additional information, refer to the *EPS464 STG EPLD: Synchronous Timing Generator Data Sheet* in this data book.

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–0.5	7.0	V
V_I	DC input voltage	*See Note (1)*	–0.5	5.5	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	125	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.4	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		15		µA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		0.75		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *See Note (3)*

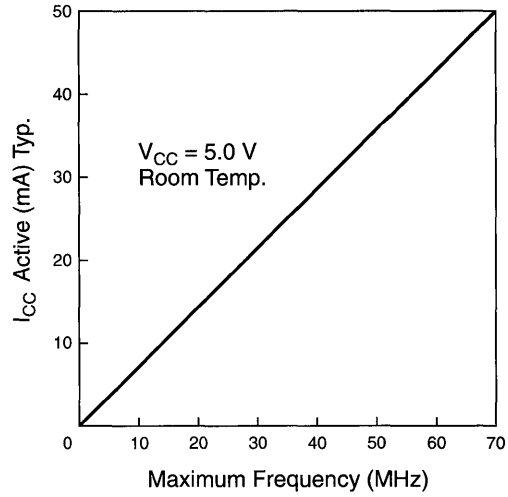
External Timing Parameters			MPS464-20 *Note (5)*		MPS464-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		7		10		ns
t_{CL}	Global clock low time		7		10		ns
t_{ASU}	Array clock setup time		6		8		ns
t_{AH}	Array clock hold time		6		7		ns
t_{ACO1}	Array clock to output delay			20		25	ns
t_{ACH}	Array clock high time		7		10		ns
t_{ACL}	Array clock low time		7		10		ns
t_{CNT}	Minimum global clock period			15		20	ns
f_{CNT}	Max. internal global clock frequency	*See Note (4)*	66.7		50		MHz
t_{ACNT}	Minimum array clock period			15		20	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (4)*	66.7		50		MHz
f_{MAX}	Maximum clock frequency	*See Note (6)*	71.4		50		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Measured with a device programmed as four 16-bit counters.
(5) This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
(6) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 16 shows typical supply current versus frequency for MPS464 MPLDs.

Figure 16. MPS464 I_{CC} vs. Frequency



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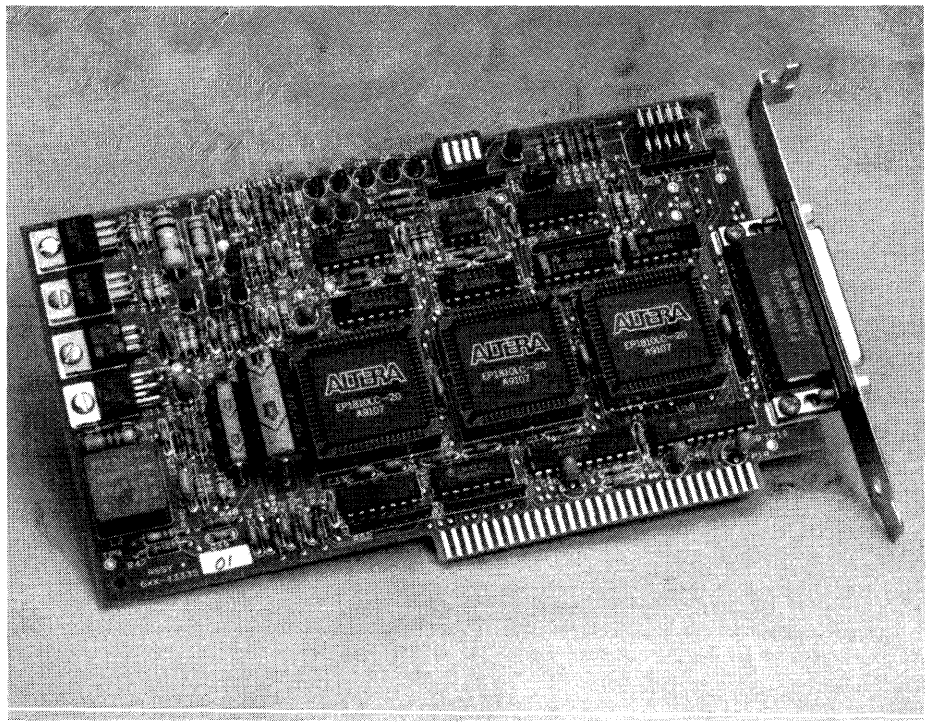
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Operating Requirements for EPLDs

September 1991, ver. 3 **Data Sheet**

Introduction

Altera EPLDs combine a unique architecture with an advanced CMOS EPROM process that provides exceptional performance with low power. Systems that use any high-performance CMOS devices must be designed with care to obtain maximum performance with minimum problems.

Operating Conditions

Operation of Altera EPLDs at conditions above those listed under "Absolute Maximum Ratings" in the EPLD data sheets may cause permanent damage to the devices. These ratings are stress ratings only. Functional operation of the device at these conditions or at any other conditions above those indicated in the operational sections of these data sheets is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. Altera EPLDs contain circuitry to protect device pins from high-static voltages or electric fields; however, precautions should be taken to avoid voltages higher than maximum-rated voltages.

For proper operation, input and output pins must be in the range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs must be tied to V_{CC} or GND. Unused I/O pins should be tied to V_{CC} or GND, or left unconnected ("reserved"). Specific requirements are given in the EPLD pin-out in the Report File (utilization report) for a design. Each set of V_{CC} and GND pins must be connected directly at the device, with power supply decoupling capacitors of at least 0.2 µF connected between them. For effective decoupling, each V_{CC} pin must be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as that found in monolithic-ceramic types.

Noise Precautions

If eight or more EPLD output pins are switching simultaneously, precautions must be taken to minimize system noise. Certain board layouts can induce switching noise into the system from high-speed devices due to transmission-line effects and radiated coupling. These effects can be minimized by using printed circuit boards with embedded V_{CC} and GND planes and by restricting trace length in a board to under 8 inches. If long board traces or highly capacitive loads are impossible to avoid, a small series resistance (10 to 30 Ω) usually lessens undershoot and overshoot voltages if they cause a problem in a printed circuit board layout.

Turbo Bit

Some Classic EPLDs contain a programmable Turbo Bit, set with the development or programming software, to control the automatic power-down feature that enables low-standby-power mode. When the Turbo Bit is programmed (Turbo = On), the low standby power mode (I_{CC1}) is disabled, making the circuit less sensitive to V_{CC} noise transients created

by the low-power mode power-up/power-down cycle. Typical I_{CC} versus frequency data for both turbo and non-turbo mode is given in each EPLD data sheet. All AC values are tested with the Turbo Bit programmed on.

If a design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). In this mode, some AC parameters may increase. To determine worst-case timing, values from the AC Non-Turbo Adder specifications in the EPLD data sheet must be added to the corresponding AC parameter.

Altera EPLDs begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Since fluorescent lighting and sunlight fall into this range, opaque labels should be placed over the EPLD window to ensure long-term reliability. The recommended erasure procedure for EPLDs is exposure to UV light with a wavelength of 2,537 Å. Required erasure times assuming use of a lamp with a 12,000 $\mu W/cm^2$ power rating are given in Table 1; some low-power erasers may take longer.

Table 1. EPLD Erasure Times

Part Number	Erasure Time
EP610, EP910, EP910A, EP1810, EPS448	45 minutes
EPM5016, EPM5032, EPM5064, EPM5128, EPM5130, EPM5192, EPB2001, EPS464	1 hour

Altera EPLDs may be damaged by long-term exposure to high-intensity UV light. Altera EPLDs may be erased and reprogrammed as often as necessary if the recommended erasure exposure levels are used.

ESD and Latch-Up Protection

EPLD input, I/O, and clock pins have been designed to resist the electrostatic discharge (ESD) damage and latch-up inherent in CMOS structures. Unless otherwise noted, each of the EPLD pins will withstand voltage energy levels exceeding 1,500 V, per method specified by MIL-STD-883C. The pins will not latch up for input voltages in the range $V_{SS} - 1$ V to $V_{CC} + 1$ V with currents up to 100 mA. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Additionally, the programming pin is designed to resist latch-up to the 13.5 V maximum device limit.

Power Calculations

As with any CMOS device, power is a function of frequency and internal node switching. To obtain the most accurate power information, current consumption should be measured after the design is completed and the EPLD is placed in the system.

Conclusion

If the precautions given in this data sheet are followed during system and board design, Altera EPLDs should provide superior system performance and design flexibility, regardless of design size or production volume.

Contents

September 1991

Section 9 Development Products

PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES

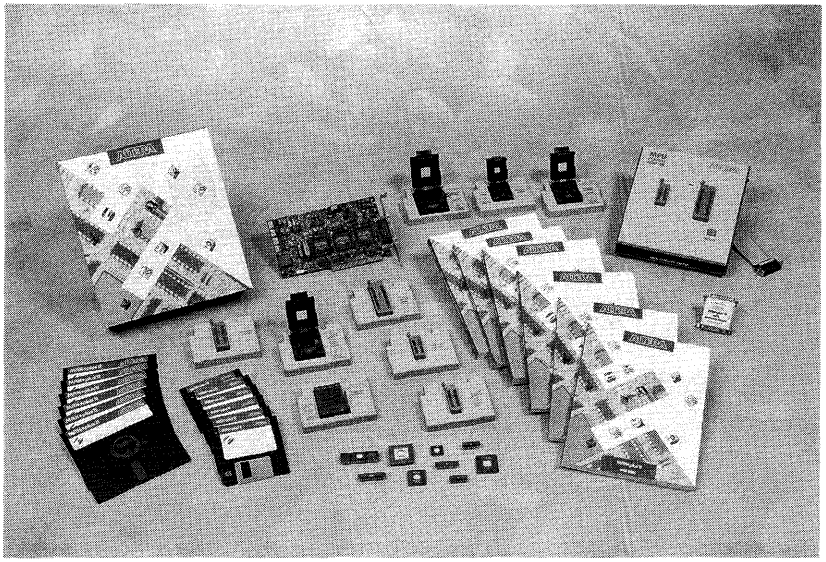
MAX+PLUS II Programmable Logic Development System & Software

September 1991, ver. 1

Data Sheet

Features...

- MAX+PLUS II is the single, unified development system for Altera's Classic, MAX 5000, MAX 7000, and STG EPLDs.
- MAX+PLUS II runs under Microsoft Windows version 3.0 to provide a highly intuitive graphical user interface, efficient memory management, multi-tasking capability, and extensive printer/plotter support.
- MAX+PLUS II offers hierarchical graphic, text, and waveform design entry:
  - Graphic Editor for schematic designs
  - Text Editor for high-level text descriptions
  - Waveform Editor for design entry and editing/viewing simulation inputs and results
- The Altera Hardware Description Language (AHDL) supports state machines, Boolean equations, truth tables, and arithmetic and relational operations.
- Applications run concurrently, allowing multiple files and editors to be active simultaneously, while simulations or compilations run in the background.
- Automatic error location is provided for the Graphic, Text, and Waveform Editors.
- Partitioning automatically divides large designs into multiple EPLDs.



...and More Features

- ❑ Logic synthesis and minimization support efficient design processing so that even large designs are compiled in a very short time.
- ❑ Functional simulation allows rapid turnaround for detailed functional debugging.
- ❑ The interactive timing simulator supports multi-EPLD designs and probes for viewing internal nodes.
- ❑ The bidirectional EDIF 2 0 0 netlist interface is compatible with a variety of third-party CAE schematic capture and simulation tools.
- ❑ Complete information is instantly accessible with on-line, context-sensitive help.
- ❑ The Windows Clipboard quickly moves design information between MAX+PLUS II and other Windows applications.
- ❑ MAX+PLUS II runs on 386-based IBM PC-AT, PS/2, or compatible computers.

General Description

MAX+PLUS II is an integrated CAE tool for designing logic with Altera's Classic, MAX 5000, MAX 7000, and Synchronous Timing Generator (STG) EPLDs. MAX+PLUS II includes design entry and processing, multi-EPLD partitioning, timing simulation, and device programming support. It runs under the Windows 3.0 graphical environment on 386-based IBM PC-AT, PS/2, and compatible machines. Figure 1 shows a block diagram of MAX+PLUS II.

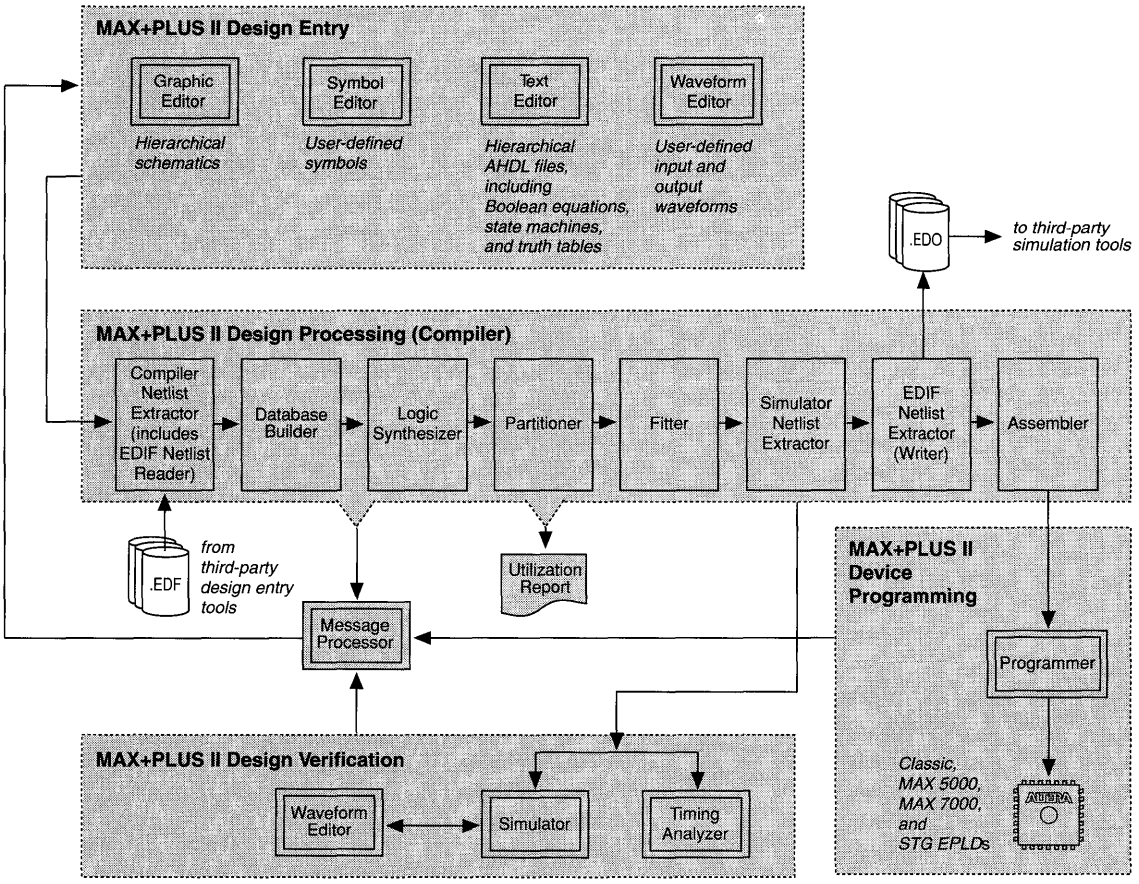
The PLDS-HPS Development System includes MAX+PLUS II software; all hardware required to program Classic, MAX 5000, MAX 7000, and STG EPLDs; and sample devices. PLS-HPS, PLS-OS, and PLS-ES are software-only packages. See "Package Contents" later in this data sheet for more information.

MAX+PLUS II supports three hierarchical design entry methods: (1) schematic designs are entered with the Graphic Editor; (2) text descriptions in the Altera Hardware Description Language (AHDL) or EDIF 2 0 0 netlists are entered with the Text Editor; and (3) waveforms are entered with the Waveform Editor. All editors can be used concurrently, with multiple files open at any time. In addition, MAX+PLUS II includes a library of over three hundred 7400-series TTL and custom macrofunctions for both schematic and text designs.

The MAX+PLUS II Compiler synthesizes and optimizes designs for Altera EPLDs in minutes. It uses advanced logic synthesis and minimization techniques together with heuristic fitting rules to efficiently place designs within a family of EPLDs. MAX+PLUS II then uses a programming file created by the Compiler and standard Altera programming hardware to program the EPLDs.

MAX+PLUS II features advanced multi-device partitioning that automatically splits large designs into multiple EPLDs, allowing the user

Figure 1. MAX+PLUS II Block Diagram



to create large system-level designs. The Partitioner lets the user specify speed-critical paths for optimum EPLD selection and design placement.

The MAX+PLUS II Simulator performs powerful, event-driven timing simulation. It supports multi-EPLD simulations and interactively displays timing results in the Waveform Editor. With the Waveform Editor, the user can enter, modify, and group input vectors; view simulation errors; and compare simulation runs.

MAX+PLUS II system integration is superb. The Compiler reports any design errors to the Message Processor, which automatically highlights the source of an error in the Graphic, Text, or Waveform Editor. MAX+PLUS II is fully integrated with the Windows Clipboard. The designer uses the Clipboard to quickly copy design information from one editor to another, while extensive on-line help provides instant information on all aspects of

the system. The Hierarchy Display lets the designer move between hierarchical design files by simply selecting an icon.

Design Entry

MAX+PLUS II design entry files—graphic, text, and waveform—can be mixed freely. In addition to AHDL Text Design Files (.TDF), MAX+PLUS II supports Altera Design Files (.ADF) and State Machine Files (.SMF) created for use with A+PLUS software. MAX+PLUS II also accepts EDIF 2 0 0 netlists produced with popular CAE schematic tools from vendors such as OrCAD, Viewlogic, FutureNet, Mentor Graphics, and Valid Logic.

The MAX+PLUS II Graphic, Symbol, Text, and Waveform Editors provide a number of common features and commands to make design entry and debugging smooth and trouble-free, including **Cut**, **Copy**, and **Paste** commands for text, objects, and areas, and global search-and-replace. Speed-critical paths can be determined with the MAX+PLUS II Timing Analyzer. All editing commands can be reversed with the **Undo** command.

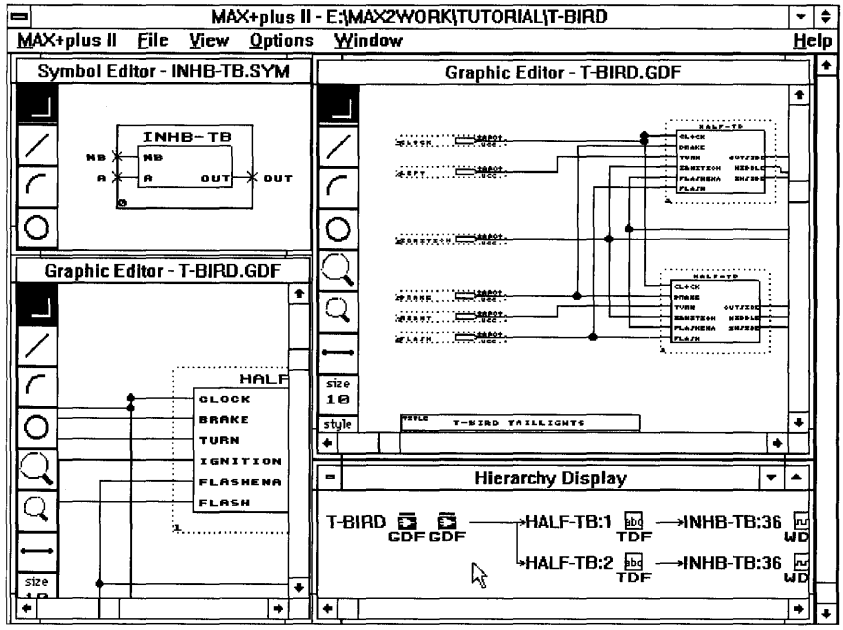
The Graphic, Symbol, Text, and Waveform Editors can open windows on several files at the same time. For example, a Waveform Editor window can display simulation results, while the Text Editor shows an AHDL description. At the same time, the user can open two windows of the Graphic Editor that display different levels of a design's hierarchy, or different areas of the same design file. If one design is displayed in two windows of an editor, any edits made in one window are automatically reflected in the other.

Graphic & Symbol Editors

The Graphic Editor (Figure 2) provides a convenient tool for schematic design entry. Designers can enter probes into the schematic to easily trace a specific signal (e.g., flip-flops, logic outputs) during simulation. Tag-and-drag editing can be used to quickly move individual symbols, groups of items, or entire areas. During a move, a net can be broken or connections can be preserved with orthogonal rubberbanding. Other Graphic Editor features include the ability to group nodes into buses, locate the source and destination of nets, and make quick node name changes with the search-and-replace feature.

The MAX+PLUS II Compiler automatically generates a symbol that represents a design file, which can then be used in a higher-level schematic. The designer can use the Symbol Editor to modify input and output pin placement or to customize the appearance of an automatically created symbol. See Figure 2.

Figure 2. MAX+PLUS II Graphic Editor

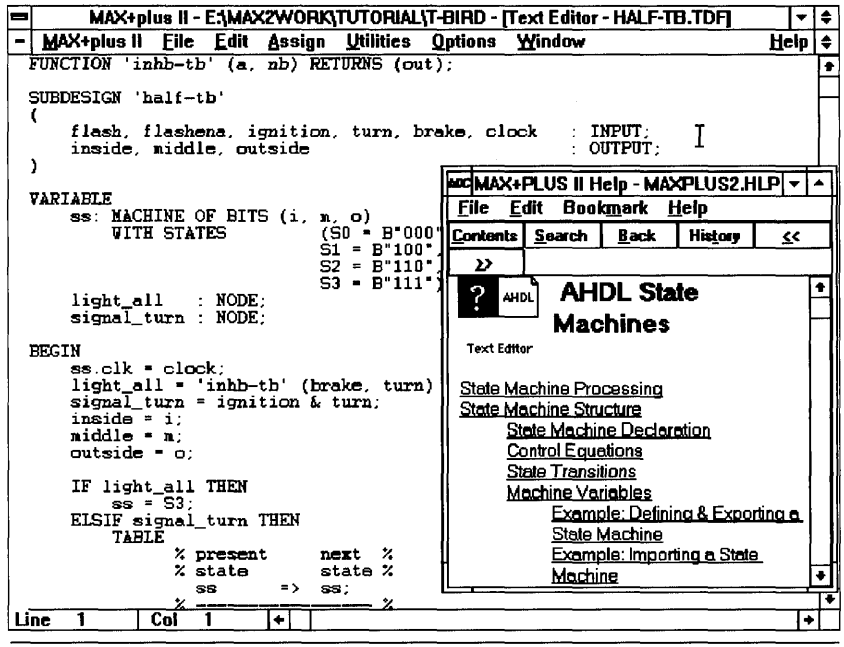


Text Editor & AHDL

The MAX+PLUS II Text Editor lets the user view and edit any ASCII text file in the MAX+PLUS II environment, including Altera Hardware Description Language (AHDL) Text Design Files (.TDF), Vector Files (.VEC), Report Files (.RPT), and EDIF netlists. A Text Editor window that contains a TDF is shown in Figure 3.

AHDL is a high-level modular language used to create logic designs for Altera EPLDs. It provides design entry for state machines, truth tables, and Boolean equations. The language syntax supports arithmetic and relational operations such as addition, subtraction, equality, and magnitude comparisons. Standard Boolean functions, e.g., AND, OR, NAND, NOR, XOR, and XNOR, are also included. Since AHDL supports groups, operations can be performed on a byte- or word-wide basis as well as on single variables. The designer can also assign logic to specific macrocells within EPLDs using AHDL. Together, these features make it easy to implement complex designs in a concise, high-level description.

Figure 3. MAX+PLUS II Text Editor & AHDL



Waveform Editor

The MAX+PLUS II Waveform Editor (Figure 4) is used to create and edit waveform designs. In addition, the Waveform Editor functions as a logic analyzer that allows the designer to create simulation inputs and view simulation results.

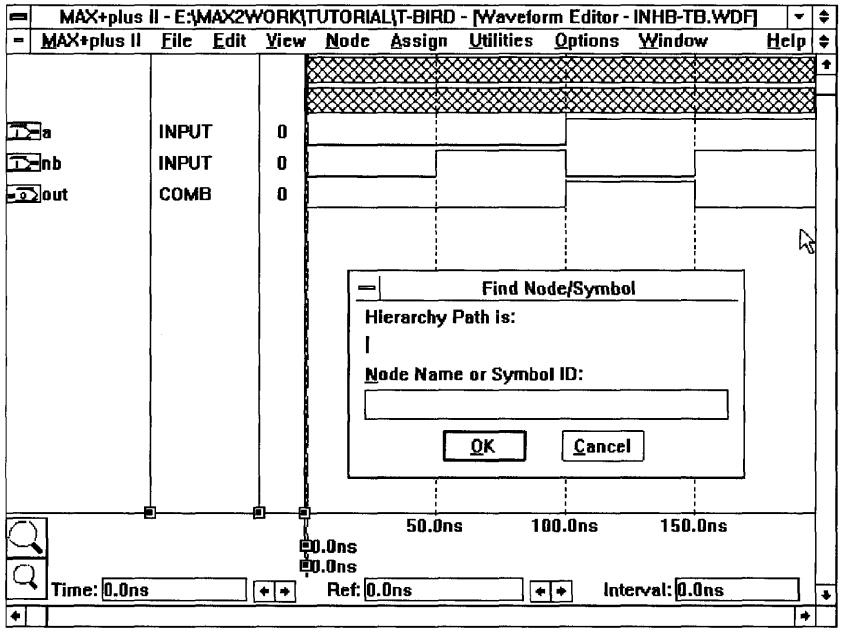
Designs that generate timing signals are best described with waveforms. The Compiler's advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms.

Registered and combinatorial logic as well as state machines can be described with waveforms. The Compiler determines the optimal number of state bits and state variable assignments.

The Waveform Editor can define and modify Waveform Design Files (.WDF) and input vectors for simulation. The designer can:

- copy, cut, paste, repeat, and stretch waveforms;
- add or delete internal nodes, flip-flops, and state machines;
- combine waveforms into binary, octal, decimal, or hexadecimal buses;
- compare the differences between two simulations by simulating a design, editing the input vectors, simulating the design again, and then superimposing two sets of input and output waveforms for easy comparison.

Figure 4. MAX+PLUS II Waveform Editor



Hierarchy Display

The MAX+PLUS II Hierarchy Display shows the current design hierarchy—including all lower-level design files—which can be a mixture of graphic, text, and waveform files. The user selects one or more files, and MAX+PLUS II then opens the appropriate editor to display the design. This context-sensitive feature makes it easy to move around the design hierarchy.

Clipboard

The Windows Clipboard is a temporary storage location that allows users to pass design information between editors. Text from a Text Editor file can be copied into the Graphic, Symbol, and Waveform Editors, or to another Text Editor file. Schematics can be copied between Graphic Editor files, and waveforms can be pasted from one Waveform Editor file to another. Information can also be pasted into other Windows applications.

Macrofunction Library

The MAX+PLUS II TTL MacroFunction Library contains over three hundred 7400-series TTL, bus, and EPLD-optimized functions. All have been optimized for greatest speed and device utilization, and—due to the flexible architecture of Altera EPLDs—all perform true TTL emulation. Table 1 lists a selection of the available macrofunctions.

Table 1. Partial List of MAX+PLUS II Macrofunctions

Type	Macrofunctions
Adder	8FADD, 7480, 7482, 7483, 74183, 74283, 74385
ALU	74181, 74182, 74381, 74382
AND-OR Gate	7452
Comparator	8MCOMP, 7485, 74518, 74684, 74686, 74688
Code Converter	74184, 74185
Counter	4COUNT, 8COUNT, 16CUDSLR, GRAY4, UNICNT, 7493, 74160, 74161, 74162, 74163, 74190, 74191, 74192, 74193, 74393...
Decoder	7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 74138, 74139, 74154, 74155, 74156...
Encoder	74147, 74148
Frequency Divider	FREQDIV, 7456, 7457
Latch	INPLTCH, NANDLTCH, NORLTCH, 7475, 7477, 74116, 74259, 74279, 74373...
Multiplier	MULT2, MULT4, MULT24, 74261...
Multiplexer	21MUX, 74151, 74153, 74157, 74158, 74298...
Parity Generator	74180, 74280
Register	7470, 7471, 7472, 7473, 7474, 7476, 7478, 74173, 74174, 74175, 74178, 74273, 74374...
Shift Register	BARRELST, 7491, 7494 ,7496, 7499, 74164, 74165, 74166, 74179, 74194, 74198...
SSI Gate	CBUF, INHB, 7400, 7402, 7404, 7408, 7410, 7411, 7420, 7421...

EDIF Support

MAX+PLUS II has a built-in bidirectional EDIF 200 netlist interface, providing a convenient bridge to popular CAE schematic capture and simulation tools. Any CAE software package that produces EDIF 200 netlists can export designs to MAX+PLUS II with Library Mapping Files (.LMF) that convert third-party CAE functions to equivalent Altera primitives and macrofunctions. Altera provides a number of ready-made LMFs for software packages from Mentor Graphics, Valid Logic, and Viewlogic, but users can also create their own LMFs to map any CAE software library. MAX+PLUS II then automatically generates a symbol from an EDIF file, so that the file can be incorporated into a MAX+PLUS II schematic. EDIF files can also be incorporated into AHDL designs.

EDIF netlists can also be exported from MAX+PLUS II to third-party CAE tools, allowing the user to simulate EPLD designs with the simulation software of choice. Output Mapping Files (.OMF) can convert Altera primitives and macrofunctions to equivalent third-party functions.

Design Processing

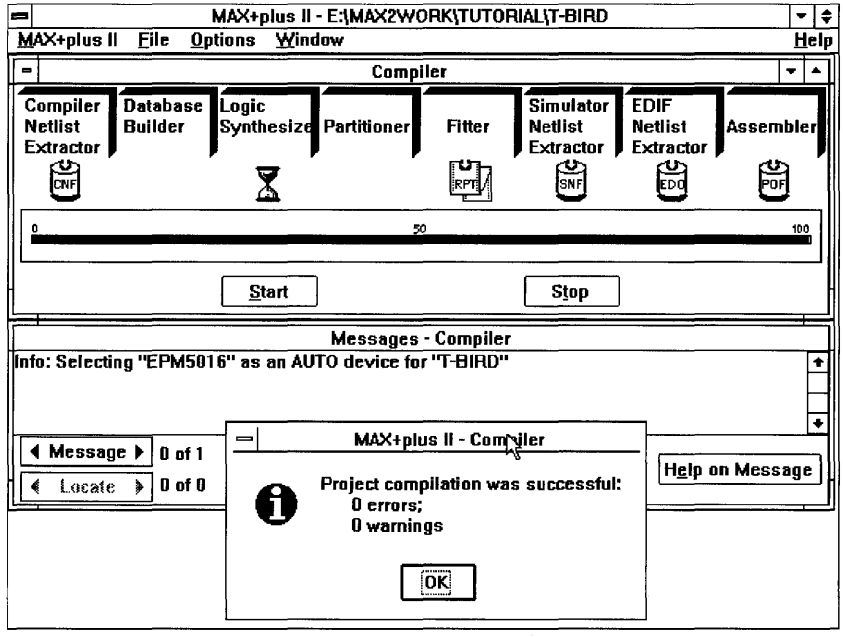
The MAX+PLUS II Compiler processes designs for all Altera general-purpose EPLDs, including the Classic, MAX 5000, MAX 7000, and STG EPLDs (see Figure 5).

Compiler options simplify design processing and analysis. The user can specify the degree of detail of the Report File (.RPT) that shows how an EPLD has been utilized and the target EPLD family for the design. The user can also choose to create a Simulator Netlist File (.SNF) for the MAX+PLUS II Simulator or an EDIF Output File (.EDO) for third-party simulators.

The first module of the compiler, the Compiler Netlist Extractor, extracts the netlist used to define the design. This module also contains a built-in EDIF Netlist Reader. The Compiler Netlist Extractor checks design rules for any errors. If errors are found, they are displayed by the Message Processor, which can then locate them in the appropriate design file. A successfully extracted design is built into a database and passed to the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the target architecture. The design is first minimized with SALSA (Speedy Altera Logic Simplification Algorithm), which removes any unused logic within the design. The Logic Synthesizer uses expert synthesis rules based on the target architecture (Classic, MAX 5000, MAX 7000, or STG) to

Figure 5. MAX+PLUS II Compiler



factor and map logic within the chosen EPLD structure. It then uses advanced synthesis algorithms that ensure the most efficient use of silicon resources.

For large system-level designs, the Partitioner is invoked. The Partitioner uses a sophisticated "Min-Cut" algorithm to separate the logic design into multiple EPLDs from the same family, relieving the designer of the time-consuming task of manually splitting a large design into smaller designs. The user can control the design's partitioning by entering specific chip assignments for flip-flops and pins in the source design files.

After partitioning, the Fitter applies heuristic rules to optimally place the synthesized design into one or more EPLDs. In devices with Programmable Interconnect Array (PIA) structures—i.e., larger MAX 5000 and MAX 7000 EPLDs—or with local/global bus structures such as the EP1810 EPLD, the Fitter also automatically routes signals across this interconnect. This Fitter action relieves the designer of tedious place-and-route tasks. The Report File (.RPT) issued by the Fitter shows design implementation as well as any unused resources in the EPLDs.

The Simulator Netlist Extractor optionally generates a netlist from the compiled design if the user desires simulation or timing analysis data.

The EDIF Netlist Extractor optionally writes an EDIF 200 netlist that contains all post-synthesis function and delay information for the completed design, so that it can be integrated into a workstation environment. Detailed specifications and test cases of Altera's EDIF output, as well as simulation libraries and conversion software for Viewlogic and Valid Logic software, are available from Altera Applications.

Finally, the Assembler module creates one or more Programmer Object Files (.POF) and/or JEDEC Files (.JED) from the compiled design. The MAX+PLUS II Programmer uses these files and standard Altera hardware to program the desired EPLDs.

Message Processor

The MAX+PLUS II Message Processor is the clearinghouse for all messages generated during compilation, simulation, timing analysis, and programming. For example, if an error occurs during compilation, the Message Processor displays a brief description of the error. The user then selects the error message, chooses the **Locate** button, and the troublesome logic is highlighted in the appropriate editor. Or, if a set-up time violation occurs during simulation, the Message Processor opens not only the Waveform Editor to highlight the portion of the simulation waveform where the violation occurred, but also the appropriate editor to show the specific flip-flop location in the original design file.

Functional Simulation

Functional simulation allows the user to test the logical operation of a design before compilation is completed. The designer can quickly identify and correct logical errors in a design without first having to synthesize, partition, and fit the logic into an EPLD. Functional simulation is performed in the MAX+PLUS II Simulator. The Waveform Editor displays the results of functional simulation and provides easy access to all nodes in a design, including combinatorial functions.

Timing Simulation

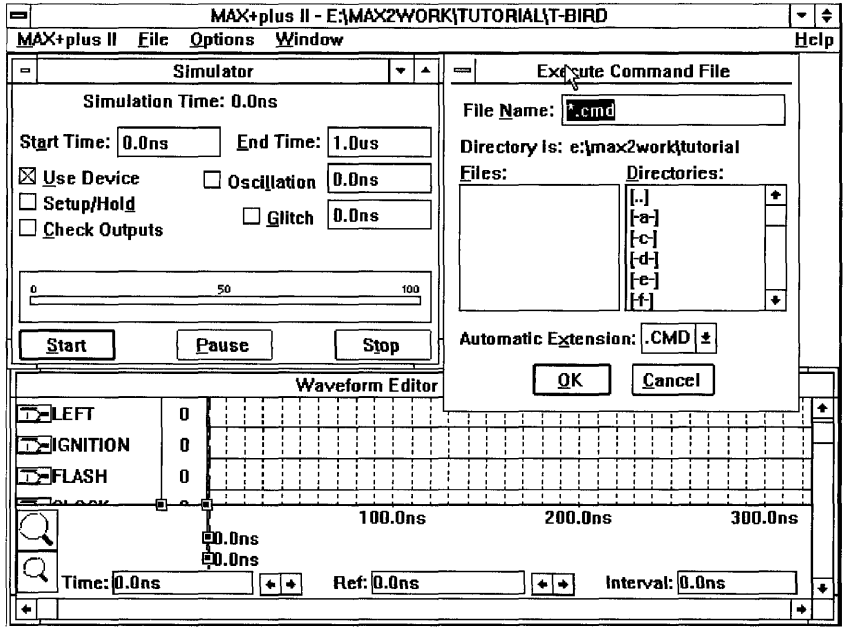
The Simulator (Figure 6) uses the virtual memory capability of Windows to perform large, multi-EPLD simulations.

The designer either defines input stimuli with a straightforward vector input language, or draws waveforms directly with the Waveform Editor. Simulation results can be viewed in the Waveform Editor, or printed out as text or waveform files.

The Simulator uses the Simulator Netlist File (.SNF) extracted from a compiled design to perform timing simulation with 0.1-ns resolution. The user can specify commands either interactively or in a batch file to perform a variety of tasks, such as halting the simulation when user-defined conditions are met or forcing flip-flops high or low.

If flip-flop setup or hold times have been violated, the Message Processor notifies the user of where and when the problem occurred. Also, if the user-defined minimum pulse width and period of oscillation are violated

Figure 6. The MAX+PLUS II Simulator



during simulation, the Message Processor can locate the offending node in the original design file, and display the time at which the problem took place in the Waveform Editor.

Differences between two simulations are viewed in the Waveform Editor, where the simulation results can be superimposed for easy comparison.

Timing Analysis

MAX+PLUS II software includes powerful analysis tools for analyzing the timing of a completed design. The user simply tags start and end points in the Graphic, Text, or Waveform Editor or Timing Analyzer to determine the shortest and longest propagation delays. The Timing Analyzer also determines setup and hold time requirements at device pins, as well as maximum clock frequency. Critical paths identified by the Timing Analyzer can be traced in the editors.

Device Programming

All hardware and software necessary for programming and verifying EPLDs is available from Altera. The MAX+PLUS II Programmer allows you to program, verify, examine, blank-check, and test Classic, MAX 5000, MAX 7000, and STG EPLDs. The programming hardware includes an add-on card (for IBM PC-AT, PS/2, or compatibles) that drives the Altera Master Programming Unit (MPU). For MAX 7000 EPLDs and selected high-pin-count devices, the MPU supports functional testing, so that vectors developed during simulation can be applied to the EPLD at programming time to verify the functionality of the device. The MPU also performs continuity checking to ensure adequate electrical contact between the programming adapter and the EPLD.

In addition, Data I/O and a variety of third-party manufacturers provide programming support for Altera EPLDs.

Package Contents

PLDS-HPS

The complete MAX+PLUS II development system includes both hardware and software:

- ❑ Graphic, Symbol, Text, and Waveform Editors
- ❑ AHDL
- ❑ Bidirectional EDIF interface
- ❑ Compiler support for all Altera Classic, MAX 5000, MAX 7000, and STG EPLDs
- ❑ Partitioner
- ❑ Simulator and Timing Analyzer
- ❑ Hierarchy Display and Message Processor
- ❑ Programmer
- ❑ Documentation
- ❑ Master Programming Unit (MPU)
- ❑ Programming card (LP6 for 386- or 486-based IBM PC-AT or compatible; LP5 for IBM PS/2 Model 70 or higher or compatible)

- ❑ Programming adapters (PLED5016, PLED5032, PLEJ5064, PLEJ5128, PLEG5130, PLEJ5192, PLED610, PLED910, PLEJ1810)
- ❑ Sample EPLDs

PLS-HPS

The "High-Performance System" contains the complete MAX+PLUS II software. It includes:

- ❑ Graphic, Symbol, Text, and Waveform Editors
- ❑ AHDL
- ❑ Bidirectional EDIF interface
- ❑ Compiler support for all Altera Classic, MAX 5000, MAX 7000, and STG EPLDs
- ❑ Partitioner
- ❑ Simulator and Timing Analyzer
- ❑ Hierarchy Display and Message Processor
- ❑ Programmer
- ❑ Documentation

PLS-OS

The "Open System" is targeted for the user who already has third-party CAE software for schematic capture and simulation. It includes:

- ❑ Text Editor
- ❑ AHDL
- ❑ Bidirectional EDIF interface
- ❑ Compiler support for all Altera Classic, MAX 5000, MAX 7000, and STG EPLDs
- ❑ Partitioner
- ❑ Hierarchy Display and Message Processor
- ❑ Programmer
- ❑ Documentation

PLS-ES

The "Entry System" is designed for the user who needs MAX+PLUS II software to develop logic circuits for Altera's small, fast EPLDs. It includes:

- ❑ Text Editor
- ❑ AHDL
- ❑ Compiler support (without Partitioner) for all Altera Classic EPLDs and the EPM5016 and EPM5032 MAX 5000 EPLDs
- ❑ Hierarchy Display and Message Processor
- ❑ Documentation

Ordering Information

PLDS-HPS	(IBM PC-AT or compatible)
PLDS-HPS/PS	(IBM PS/2 Model 70 and higher or compatible)
PLS-HPS	(IBM PC-AT, PS/2, or compatible)
PLS-OS	(IBM PC-AT, PS/2, or compatible)
PLS-ES	(IBM PC-AT, PS/2 or compatible)

System Requirements

Minimum System Configuration

- ❑ 386- or 486-based IBM PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ 4 Mbytes of memory
- ❑ DOS version 3.1 or higher
- ❑ Microsoft Windows version 3.0 or higher
- ❑ Microsoft Windows-compatible graphics card and monitor
- ❑ 20 Mbytes free disk space
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ 2- or 3-button mouse compatible with Microsoft Windows 3.0
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Recommended System Configuration

- ❑ 33-MHz 386- or 486-based IBM PC-AT computer, or compatible
- ❑ 8 Mbytes of memory
- ❑ DOS version 3.3 or higher
- ❑ Microsoft Windows version 3.0 or higher
- ❑ 12-ms seek-time hard drive with 20 Mbytes free disk space
- ❑ Microsoft Windows-compatible graphics card and monitor with a resolution of greater than 800 × 600 pixels
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ 2- or 3-button mouse compatible with Microsoft Windows 3.0
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

PLDS-MAX & PLS-MAX

MAX+PLUS Programmable Logic Development System & Software

September 1991, ver. 1

Data Sheet

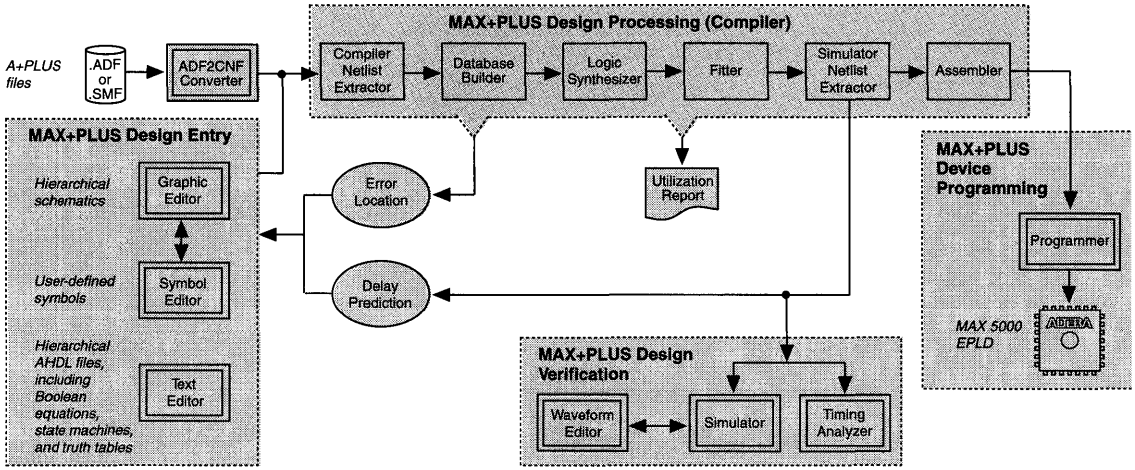
Features

- ❑ Software support for MAX 5000 (Multiple Array MatriX) EPLDs
- ❑ Hierarchical design entry methods for both graphic and text designs
  - Multi-level schematic and hardware language descriptions
  - Over three hundred 7400-series TTL and bus macrofunctions optimized for MAX 5000 architecture
  - Altera Hardware Description Language (AHDL) for state machines, Boolean equations, truth tables, arithmetic and relational operations
  - Delay prediction and timing analysis for graphic and text designs
- ❑ Logic synthesis and minimization for quick and efficient processing
- ❑ Compiles a 100% utilized EPM5128 in only 10 minutes
- ❑ Automatic error location for schematics and AHDL text files
- ❑ Interactive Simulator with probe assignments for internal nodes
- ❑ Waveform Editor for entering and editing simulation vector waveforms and viewing simulation results
- ❑ Runs on IBM PC-AT, PS/2, or compatible computers
- ❑ EDIF industry-standard workstation and third-party interfaces available separately

General Description

MAX+PLUS is a unified CAE system for designing logic with Altera's MAX 5000 EPLDs. It includes design entry, design processing, timing simulation, and device programming support. MAX+PLUS runs on IBM PC-AT, PS/2, and compatible computers and provides all tools to quickly and efficiently create, verify, and program complex logic designs. Figure 1 shows a block diagram of MAX+PLUS.

Figure 1. MAX+PLUS Block Diagram



The PLDS-MAX Development System includes MAX+PLUS software, al hardware required to program MAX 5000 EPLDs, and device samples PLS-MAX is a software-only package. See "Package Contents" later in this data sheet for more information.

Designs may be entered with a variety of design entry methods. MAX+PLUS supports hierarchical entry of both Graphic Design Files (.GDF) with the MAX+PLUS Graphic Editor, and Text Design Files (.TDF) in the Altera Hardware Description Language (AHDL) with the MAX+PLUS Text Editor The Graphic Editor offers advanced features such as multiple hierarchy levels, symbol editing, and an extensive library of 7400-series TTL macrofunctions and basic SSI gates. AHDL designs can be mixed into any level of the hierarchy or used stand-alone. AHDL is tailored especially for EPLD designs and includes support for complex Boolean and arithmetic functions, relational comparisons, state machines with automatic state variable assignment, truth tables, and function calls.

MAX+PLUS includes the MAX+PLUS Compiler, which synthesizes and optimizes designs in minutes. It uses advanced logic synthesis and minimization techniques together with heuristic fitting rules to efficiently place designs into MAX 5000 EPLDs. The Compiler creates a programming

file that the MAX+PLUS Programmer uses to program MAX 5000 EPLDs with standard Altera programming hardware.

Simulations are performed with an event-driven timing simulator. The MAX+PLUS Simulator interactively displays timing results in the MAX+PLUS Waveform Editor. Hardcopy table and waveform output is available. With the Waveform Editor, input vector waveforms can be entered, modified, grouped, and ungrouped. The Waveform Editor can also compare simulation runs and highlight the differences between them.

MAX+PLUS also provides features such as automatic error location and delay prediction. If a design contains an error in a schematic or an AHDL text file, MAX+PLUS reports the error *and* takes the user to the location of the error in the original schematic or text file. Propagation delays of critical paths can also be determined from within both the Graphic and Text Editors with the delay prediction feature. After the source and destination nodes are tagged, the shortest and longest timing delays are calculated.

Design Entry

MAX+PLUS provides a seamless design framework that uses a consistent graphical user interface throughout. This framework simplifies all stages of the design cycle: design entry, processing, verification, and programming.

MAX+PLUS offers both graphic and text design entry methods. GDFs are entered with the MAX+PLUS Graphic Editor; Boolean equations, state machines, and truth tables are entered in the Altera Hardware Description Language (AHDL) with the MAX+PLUS Text Editor. The ability to freely mix graphic and text files at all levels of the design hierarchy, and to use a top-down or bottom-up design method, makes design entry simple and versatile. As the designer traverses the hierarchy, the Text Editor is automatically invoked for text files, and the Graphic Editor is invoked for schematics.

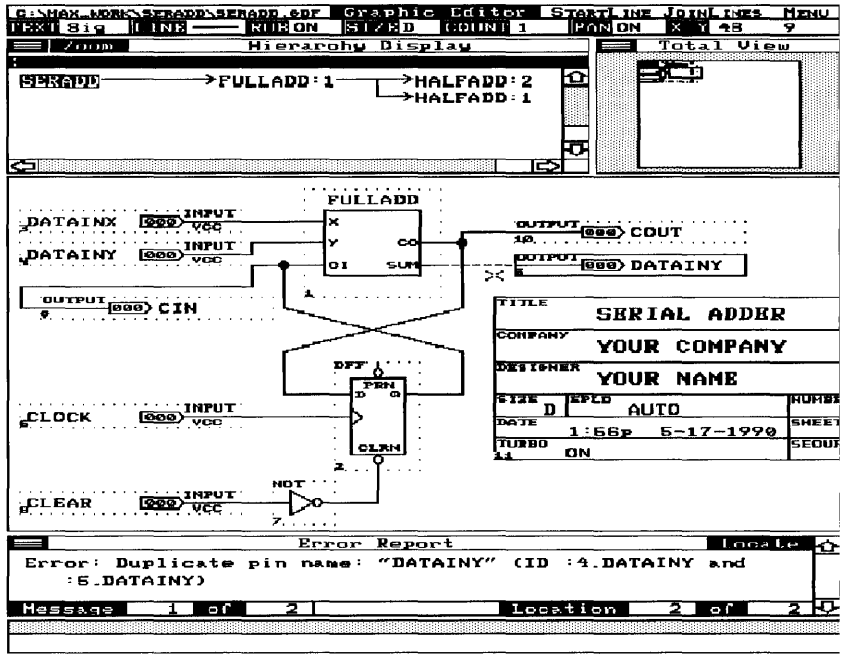
When a text or graphic file is saved, MAX+PLUS automatically generates a symbol for this file. This symbol, and the design it represents, can then be used as a subdesign in a higher-level schematic or in another design.

MAX+PLUS also accepts third-party netlists from OrCAD, and Data I/O (ABEL, FutureNet DASH), as well as existing EPLD designs implemented with Altera's A+PLUS, and Intel's iPLDS or iPLDS II systems. EDIF netlists can be converted with Altera's PLS-EDIF software and then imported into MAX+PLUS.

Graphic & Symbol Editors

The MAX+PLUS Graphic Editor (Figure 2) provides a mouse-driven, multi-windowed environment in which commands are entered via pop-up menus or simple keystrokes. The Hierarchy Display window lists all schematics used in a design. The designer navigates the hierarchy by clicking a mouse button on the name of the design to be opened. The Total

Figure 2. MAX+PLUS Graphic Editor



View window shows the entire design. By clicking inside this window, the main work window is moved to the corresponding area of the schematic. The Error Report window lists all warnings and errors in the compiled design; selecting an error with the mouse highlights the problem node and symbol. A design is entered in the main work window, which can be enlarged by closing the auxiliary windows.

When entering a design, the user can choose from a library of over 300 7400-series TTL and special-purpose macrofunctions that are optimized for MAX 5000 architecture. In addition, the designer can create custom functions that can be used in any MAX+PLUS design.

Tag-and-drag editing is used to move individual symbols or entire areas. Lines remain connected with orthogonal rubberbanding. Designs are printed on an Epson FX-compatible printer; HP7475A, 7485B, and 7495A plotters; or a Houston Instruments 695-compatible plotter.

The MAX+PLUS Symbol Editor enables the designer to create or modify a custom symbol that represents a GDF or TDF. It is also possible to modify input and output pin placement on an automatically generated symbol.

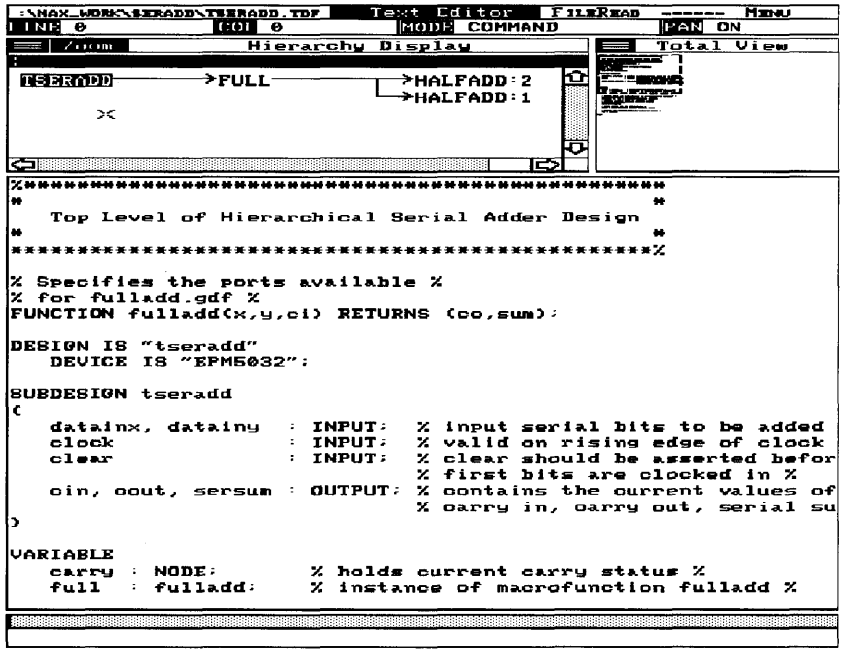
A symbol represents a lower-level design that is described by a GDF or TDF. The design can be displayed with a single command that invokes the Graphic Editor for schematics or the Text Editor for AHDL designs.

Text Editor & AHDL

The MAX+PLUS Text Editor, shown in Figure 3, enables the user to view and edit text files within the MAX+PLUS environment. Any ASCII text file, including AHDL TDFs, Vector Files (.VEC), Table Files (.TBL), and Report Files (.RPT), can be viewed and edited in the Text Editor.

The Text Editor parallels the Graphic Editor's structure with Hierarchy Display and Total View windows for moving through hierarchy levels and around the design. It also provides automatic error location. If an error is found in a TDF during compilation, the Text Editor is automatically invoked and the line of AHDL code where the error occurred is highlighted.

Figure 3. MAX+PLUS Text Editor



AHDL is a high-level, modular language used to create logic designs for MAX 5000 EPLDs. It is completely integrated into MAX+PLUS, so AHDL files may be created, edited, compiled, simulated, and programmed from within MAX+PLUS.

AHDL supports state machines, truth tables, and Boolean equations, as well as arithmetic and relational operations. It is hierarchical, so that frequently used functions such as TTL and bus macrofunctions can be incorporated into a design. AHDL also supports complex arithmetic and relational operations—such as addition, subtraction, equality, and

magnitude comparisons—with the automatically generated logic functions. Standard Boolean functions, e.g., AND, OR, NAND, NOR, XOR, and XNOR are also included. Groups are fully supported so operations can be performed on byte- or word-wide functions as well as on single variables. AHDL also allows the designer to specify the location of resources (e.g., latches, flip-flops, and pins) within MAX 5000 EPLDs. Together, these features make it easy to implement complex designs in a concise, high-level description (see Figure 4).

Figure 4. Sample AHDL File

```
TITLE "Timed Add and Compare Function.";

DESIGN IS "add_cmp" DEVICE IS "EPM5128-2";

FUNCTION 74161 (LDN,A,B,C,D,ENT,ENP,CLRN,CLK)
RETURNS (QA,QB,QC,QD,RCO);

SUBDESIGN add_cmp (
                a[7..0],        % inputs for adder/comparator %
                b[7..0],
                cmpen,
                clock,reset     :INPUT;

                result[7..0],
                elapse[3..0],
                equal,
                less_than,
                grtr_than,
                done            :OUTPUT;
)
VARIABLE
        timer           : 74161; % timer is 74161 counter %
        register[7..0]  : DFF;   % register is an octal FF %
        flag            : NODE;

BEGIN
% set up accumulate register %
        result[] = register[];
        register[].clrn = reset;
        register[].clk = clock;
% this is the actual addition %
        register[] = a[] + b[];
% set flag high if register is not empty %
        flag = (register[] != 0);
        done = flag;
% connect inputs for timer (74161) %
        timer.enp = cmpen & flag;
        timer.clk = clock;
        timer.clrn = reset;
% elapse is the number of clock cycles it takes to do addition %
        elapse[3..0] = (timer.QA,timer.QB,timer.QC,timer.QD);
% the comparator section %
        equal = ( a[] == b[]);
        less_than = (a[] < b[]);
        grtr_than = (a[] > b[]);
END;
```

Macrofunction Library

The MAX+PLUS TTL MacroFunction Library contains the most commonly used 7400-series macrofunctions such as counters, decoders, encoders, shift registers, flip-flops, latches, and multipliers, as well as special bus macrofunctions, all of which increase design productivity. The flexible architecture of MAX 5000 EPLDs (which includes asynchronous Preset and Clear) ensures true TTL device emulation. Altera has also created special-purpose bus macrofunctions for designs that use buses. All macrofunctions have been optimized to provide the best speed and part utilization. Table 1 lists a selection of the MAX+PLUS macrofunctions.

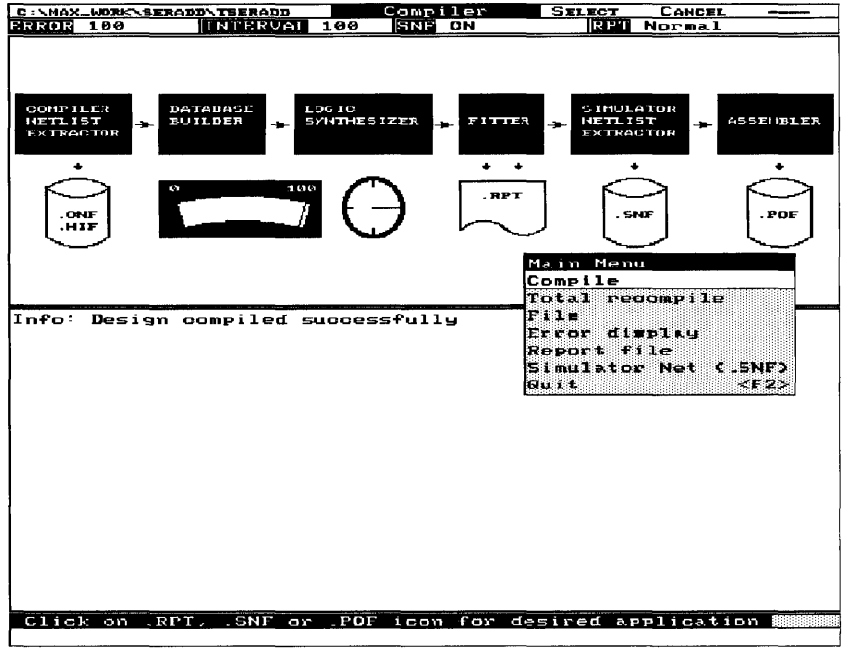
Table 1. Partial List of MAX+PLUS Macrofunctions

Type	Macrofunctions
Adder	8FADD, 7480, 7482, 7483, 74183, 74283, 74385
ALU	74181, 74182, 74381, 74382
AND-OR Gate	7452
Comparator	8MCOMP, 7485, 74518, 74684, 74686, 74688
Code Converter	74184, 74185
Counter	4COUNT, 8COUNT, 16CUDSLR, GRAY4, UNICNT, 7493, 74160, 74161, 74162, 74163, 74190, 74191, 74192, 74193, 74393...
Decoder	7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 74138, 74139, 74154, 74155, 74156...
Encoder	74147, 74148
Frequency Divider	FREQDIV, 7456, 7457
Latch	INPLTCH, NANDLTCH, NORLTCH, 7475, 7477, 74116, 74259, 74279, 74373...
Multiplier	MULT2, MULT4, MULT24, 74261...
Multiplexer	21MUX, 74151, 74153, 74157, 74158, 74298...
Parity Generator	74180, 74280
Register	7470, 7471, 7472, 7473, 7474, 7476, 7478, 74173, 74174, 74175, 74178, 74273, 74374...
Shift Register	BARRELST, 7491, 7494 ,7496, 7499, 74164, 74165, 74166, 74179, 74194, 74198...
SSI Gate	CBUF, INHB, 7400, 7402, 7404, 7408, 7410, 7411, 7420, 7421...

Design Processing

The MAX+PLUS Compiler processes designs in minutes (see Figure 5). It offers several options that speed the processing and analysis of a design. For example, the user can specify the degree of detail of the Report File (.RPT), as well as the maximum number of errors to be detected before processing halts. The user may also select whether to extract a netlist file for simulation.

Figure 5. MAX+PLUS Compiler



The Compiler compiles a design in increments. If a design has been compiled previously, only the new portion is compiled to save time.

The first module of the Compiler, the Compiler Netlist Extractor, extracts a netlist from each file. At this time, design rules are checked for any errors. If errors are found, the Graphic Editor or Text Editor is invoked after the compilation, depending on whether the error occurred in a GDF or TDF. The Error Report window displays the error and its location. The Compiler Netlist Extractor also generates a Hierarchy Interconnect File (.HIF) that describes the hierarchy of the total design. This information is used by the Database Builder, which flattens the hierarchical design, examines design logic, and checks for schematic boundary connectivity and syntax errors.

The Logic Synthesizer module translates and optimizes the user-defined logic for the MAX 5000 architecture. The design is first minimized with SALSA (Speedy Altera Logic Simplification Algorithm). Any unused logic is automatically removed. This module uses expert system synthesis rules to factor and map logic within the multi-level MAX 5000 architecture. It then chooses the approach that ensures the most efficient use of silicon resources.

The next module, the Fitter, uses heuristic rules to place the synthesized design into the chosen MAX 5000 EPLD. For MAX 5000 devices with a

Programmable Interconnect Array (PIA), the Fitter also routes the signals across this interconnect structure, so the designer doesn't have to worry about place and route issues. The Fitter issues a Report File (.RPT) that shows how the design is implemented and which resources in the EPLD are unused. The designer can then determine how much additional logic may be placed in the EPLD.

Next, the Simulator Netlist Extractor optionally generates a Simulator Netlist File (.SNF) that is used to perform timing simulation. Finally, the Assembler creates a Programmer Object File (.POF) from the compiled design that is used by the MAX+PLUS Programmer to program the EPLD.

The advanced synthesis and minimization techniques employed by the Compiler allow designs to be placed within the MAX 5000 architecture in a matter of minutes. For example, a 16-bit counter/shift register compiles in less than 1 minute on a 16-MHz 386-based PC. The Compiler is equally efficient when compiling complex designs: 5 serially linked multiplier/adder circuits that use 100% of the macrocells and 95% of all expander product terms in an EPM5128 take only 10 minutes to compile on a 20-MHz 386-based PC.

Design Verification

The MAX+PLUS II Simulator, Timing Analyzer, and Waveform Editor allow the designer to test the logic of a compiled project.

Simulator

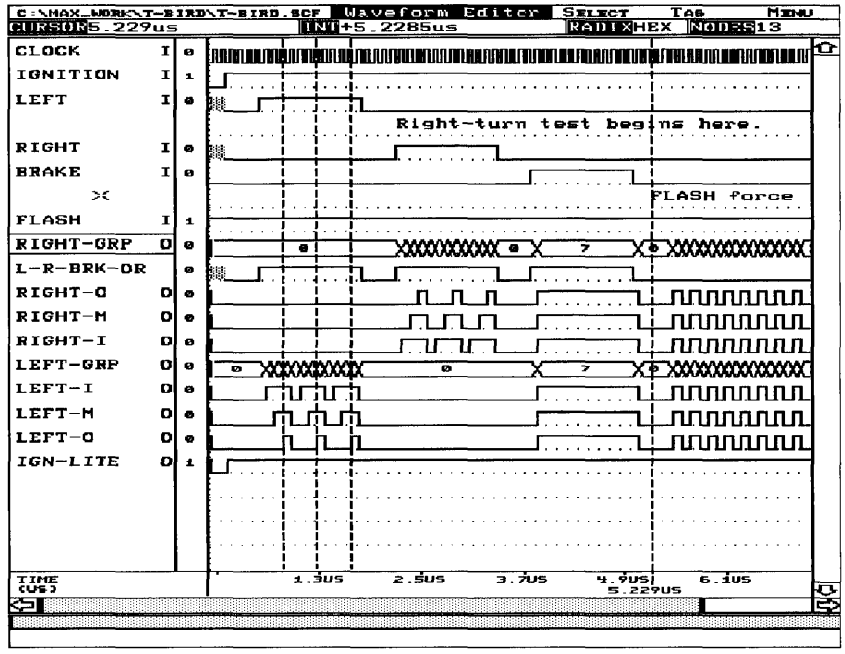
The Simulator uses the Simulator Netlist File (.SNF) extracted from the compiled design to perform timing simulation with 0.1-ns resolution. Simulator commands are provided to halt the simulation based on user-defined conditions; to force and group nodes; and to detect glitches, setup and hold violations, and unwanted oscillation. For example, if flip-flop setup or hold times have been violated, a pulse is shorter than the minimum pulse width specified, or a node oscillates for longer than the specified time, the Simulator issues a warning.

The designer can define input stimuli with a straightforward vector input language, or draw waveforms directly in the Waveform Editor. A Command File (.CMD) is used for batch operation, or commands can be entered interactively.

Waveform Editor

The MAX+PLUS Waveform Editor, shown in Figure 6, provides a mouse-driven environment for editing and viewing waveforms. It functions as a logic analyzer, enabling the user to observe simulation results. Simulated waveforms can be viewed and manipulated at multiple zoom levels. Nodes can be added, deleted, and combined into buses. Buses can contain

Figure 6. MAX+PLUS Waveform Editor



up to 32 signals that are represented in binary, octal, decimal, or hexadecimal format. Logical operators can also be used on pairs of waveforms, so that waveforms can be inverted, ORed, ANDed, or XORed.

The Waveform Editor includes sophisticated editing features to define and modify input vectors. The designer can use the mouse and familiar commands to create and copy waveforms, to repeat waveform patterns, and to move and copy blocks of waveforms. For example, all or part of a waveform can be compressed to simulate an increase in clock frequency.

The Waveform Editor can also compare and highlight the differences between two different simulations. A user can simulate a design, observe and edit the results, and then resimulate the design; the Waveform Editor can then show the results superimposed on each other to highlight the differences.

Delay Prediction & Probes

MAX+PLUS includes powerful analysis tools to verify and analyze the completed design. Delay prediction is performed interactively in the Graphic Editor, Text Editor, or Simulator. Detailed timing analyses can be performed with the MAX+PLUS Timing Analyzer.

The delay prediction feature provides instant feedback on the timing of the processed design. After selecting the start and end points of a path, the

designer can determine the shortest and longest propagation delays of speed-critical paths.

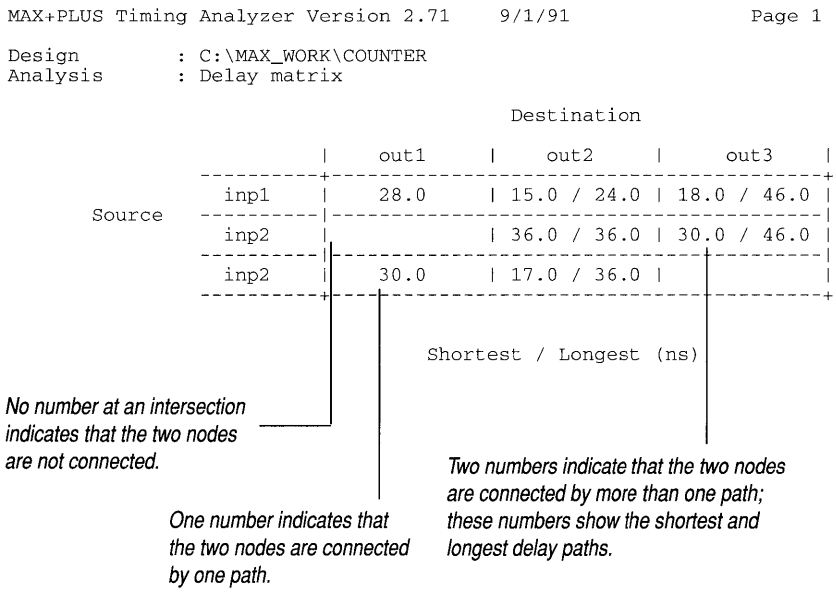
In addition, the designer can use probes to mark internal nodes in a design. A probe is entered in a Graphic Editor schematic by selecting any node and then assigning a unique name to define the probe. This name is then used in the Graphic Editor, Simulator, and Waveform Editor to identify the node, for example, to predict internal timing delays.

Timing Analysis

The MAX+PLUS Timing Analyzer (MTA) provides user-configurable reports that help the designer to analyze critical delay paths, setup and hold times, and overall system performance of any MAX 5000 EPLD design. Critical paths identified by these reports can be highlighted in a GDF.

The MTA calculates timing delays between multiple source and destination nodes and creates a connection matrix that gives the shortest and longest delay paths between all specified source and destination nodes (Figure 7). The MTA also displays the detailed paths and delays between specified sources and destinations.

Figure 7. Timing Analysis Matrix



The setup/hold option provides information on setup and hold time requirements at the device pins for all pins that feed the D, CLK, or ENABLE inputs of flip-flops and latches. Critical source nodes can be specified individually or for all pins. Information is displayed in a table with one set of setup and hold times per flip-flop or latch.

The MTA also allows the user to print a complete list of all accessible nodes in a compiled design, i.e., all nodes in the optimized design that can be displayed during simulation or delay prediction.

All MTA functions can be executed in batch mode with an MTA command file, so the user can specify all information needed to configure the output.

SNF2GDF Converter

The Simulator Netlist File-to-Graphic Design File (SNF2GDF) Converter converts the MAX+PLUS Simulator Netlist File (.SNF) into logic schematics that contain basic gates and flip-flop elements. These GDFs show how the high-level description has been synthesized and placed into the MAX 5000 architecture. SNF2GDF uses the SNF's delay and connection information to create a series of schematics that are fully annotated with propagation delay and setup and hold time information at each logic gate, regardless of whether the original design was created in a schematic, with AHDL, or with another design entry method. Certain speed paths of a design can be specified for conversion, so the user can graphically analyze only those paths that are considered critical. See Figures 8 and 9.

Device Programming

The MAX+PLUS Programmer software for programming and verifying MAX 5000 EPLDs is provided with the PLDS-MAX and PLS-MAX development systems. PLDS-MAX also contains programming hardware and several device adapters.

The MAX+PLUS Programmer drives the IBM PC-AT or PS/2 add-on card and uses standard Altera programming hardware. If the Security Bit of a device is off, the designer can also read the contents of a MAX 5000 device and use this information to program additional EPLDs.

Data I/O and other third-party manufacturers also provide programming support for Altera EPLDs.

Figure 8. Original Schematic File

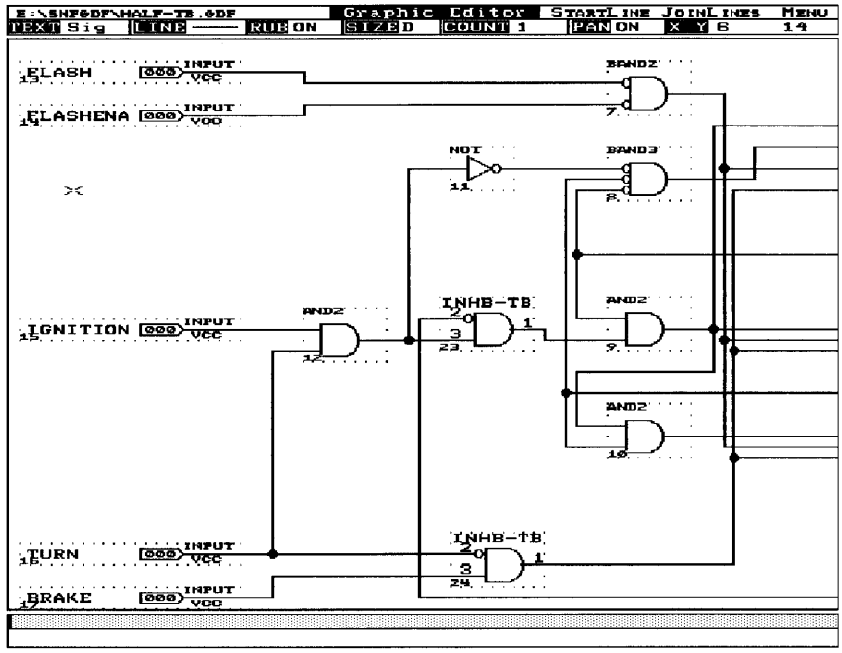
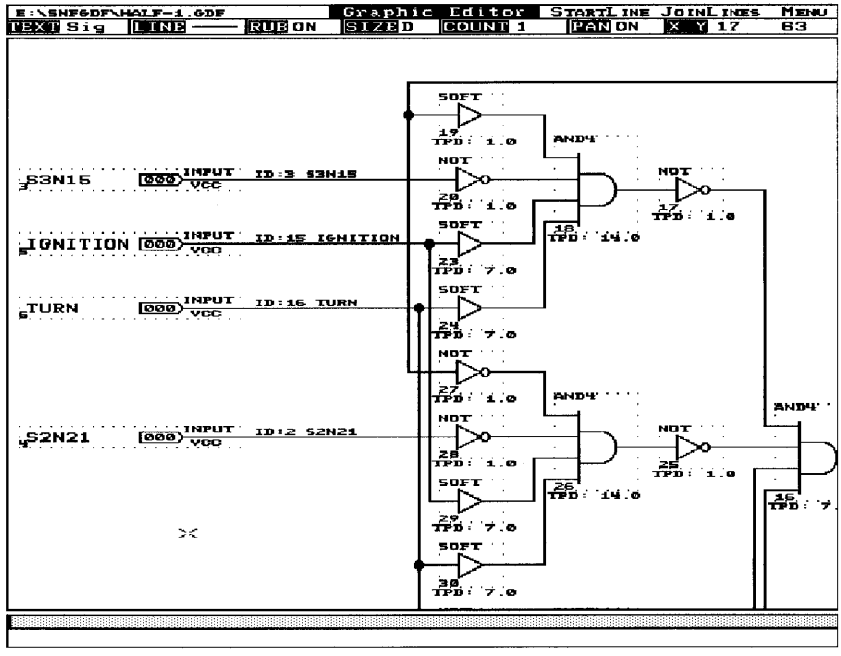


Figure 9. Schematic Converted and Annotated with SNF2GDF



Package Contents

PLDS-MAX

The complete MAX+PLUS development system includes:

- ❑ Graphic, Symbol, and Text Editors
- ❑ AHDL
- ❑ MAX+PLUS TTL MacroFunction Library
- ❑ Compiler support for all Altera MAX 5000 EPLDs
- ❑ Simulator
- ❑ Waveform Editor
- ❑ Timing Analyzer (MTA)
- ❑ SNF2GDF Converter
- ❑ Documentation
- ❑ Master Programming Unit (MPU)
- ❑ Programming card (LP6 for IBM PC-AT or compatible; LP5 for IBM PS/2 Model 50 or higher or compatible)
- ❑ Programming adapters (PLED5016, PLED5032, PLEJ5064, PLEJ5128)
- ❑ Sample EPLDs

PLS-MAX

The complete MAX+PLUS software includes:

- ❑ Graphic, Symbol, and Text Editors
- ❑ AHDL
- ❑ MAX+PLUS TTL MacroFunction Library
- ❑ Compiler support for all Altera MAX 5000 EPLDs
- ❑ Simulator
- ❑ Waveform Editor
- ❑ Timing Analyzer (MTA)
- ❑ SNF2GDF Converter
- ❑ Documentation

Ordering Information

PLDS-MAX	(IBM PC-AT or compatible)
PLDS-MAX/PS	(IBM PS/2 Model 50 and higher or compatible)
PLS-MAX	(IBM PC-AT, PS/2, or compatible)

System Requirements

Minimum System Configuration

- ❑ IBM PC-AT, PS/2 Model 50 or higher, or compatible computer
- ❑ DOS version 3.1 or higher
- ❑ 640 Kbytes of memory
- ❑ 1 Mbyte of expanded memory with version 3.2 or higher of Lotus/Intel/Microsoft (LIM) Expanded Memory Specification
- ❑ 20 Mbytes free disk space
- ❑ VGA or EGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ 3-button serial-port mouse or 2-button Microsoft-compatible serial-port or bus mouse (plus a serial port for a serial-port mouse)
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Recommended System Configuration

- ❑ 33-MHz 386- or 486-based IBM PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ DOS version 3.3 or higher
- ❑ 640 Kbytes of memory
- ❑ 2 Mbytes of expanded memory with LIM 3.2-compatible driver
- ❑ 20 Mbytes free disk space
- ❑ VGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ Serial port and 3-button serial-port mouse
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Notes:

PLCAD-SUPREME & PLS-SUPREME

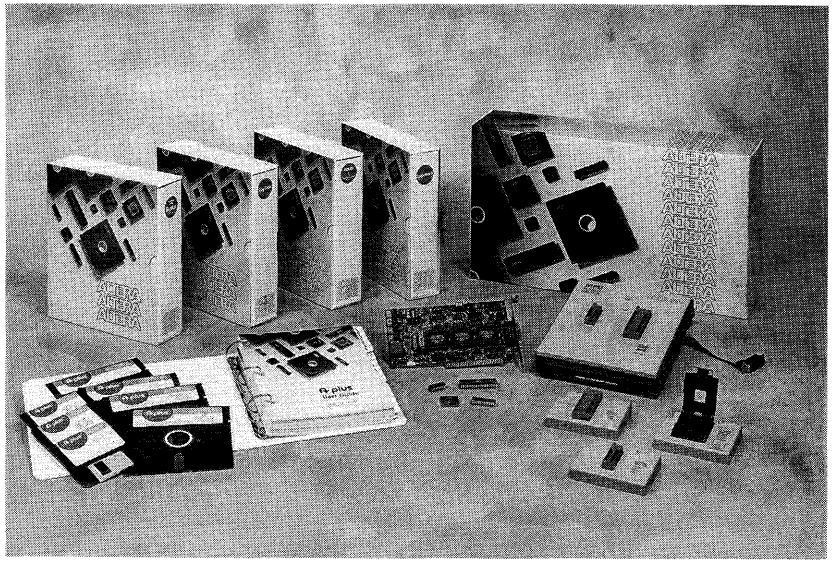
A+PLUS Programmable Logic Development System & Software

September 1991, ver. 1

Data Sheet

Features

- High-level support for Altera's general-purpose Classic EPLDs
- Multiple design entry methods
  - LogiCaps schematic capture
  - Boolean equation and netlist
  - State machine and truth table
- Complete symbol library of basic gates and over 120 TTL macrofunctions
- Support for user-defined macrofunctions with ADLIB software
- Fast and efficient design processing to ensure rapid design cycles
  - Elimination of unused gates
  - Automatic pin and part assignments
  - SALSA logic minimization
  - Device Fitter to optimize Classic EPLD resources
- Functional simulation for quick design verification
  - Easy definition of inputs with state tables, vector patterns, or predefined patterns
  - State table or graphic waveform output formats (on-screen or hard-copy)
  - Access to buried nodes within the design
- Runs on IBM PC-AT, PS/2, or compatible computers



General Description

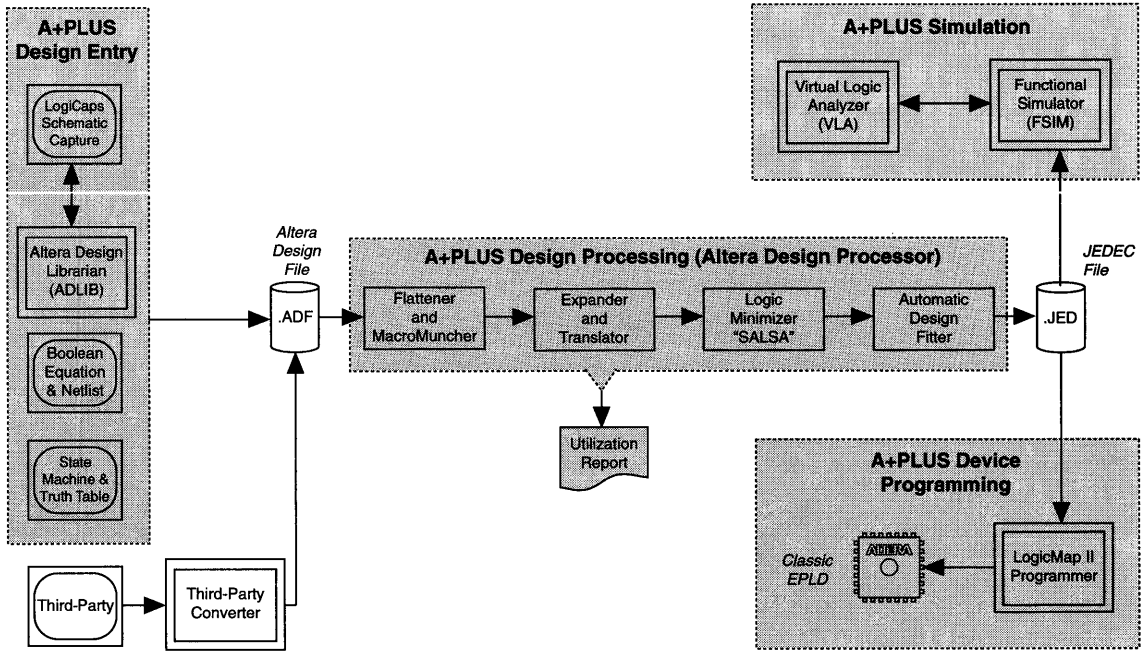
A+PLUS is a comprehensive CAE system for designing logic with Altera Classic EPLDs. A+PLUS provides multiple design entry methods, including LogiCaps schematic capture, Boolean equation, state machine, truth table, and netlist design entry. These entry methods can be combined, allowing the designer to choose the methods that best suit each design. Figure 1 shows a block diagram of A+PLUS.

A+PLUS includes the Altera Design Processor (ADP), which consists of integrated modules that produce an industry-standard JEDEC File (.JED) for EPLD programming. The ADP implements logic minimization, automatic EPLD selection, architecture optimization, and fitting. The ADP also produces documentation that shows minimized logic and EPLD utilization.

A+PLUS also includes a Functional Simulator (FSIM) to verify designs, and LogicMap II software to program EPLDs. A+PLUS runs on an IBM PC-AT, PS/2, or compatible computer and offers comprehensive support for Altera's Classic EPLDs.

PLCAD-SUPREME is a complete development system that includes A+PLUS software, all hardware required to program Classic EPLDs, and device samples. PLS-SUPREME is a software-only package. See "Package Contents" later in this data sheet for more information.

Figure 1. A+PLUS Block Diagram



Design Entry

A+PLUS provides the following design entry methods: LogiCaps schematic capture, Boolean equation, netlist, state machine, and truth table design entry.

LogiCaps Schematic Capture

Logic schematics are created with LogiCaps, which allows the user to quickly construct a wide range of logic circuits. LogiCaps provides two libraries that can be supplemented with libraries created by the user:

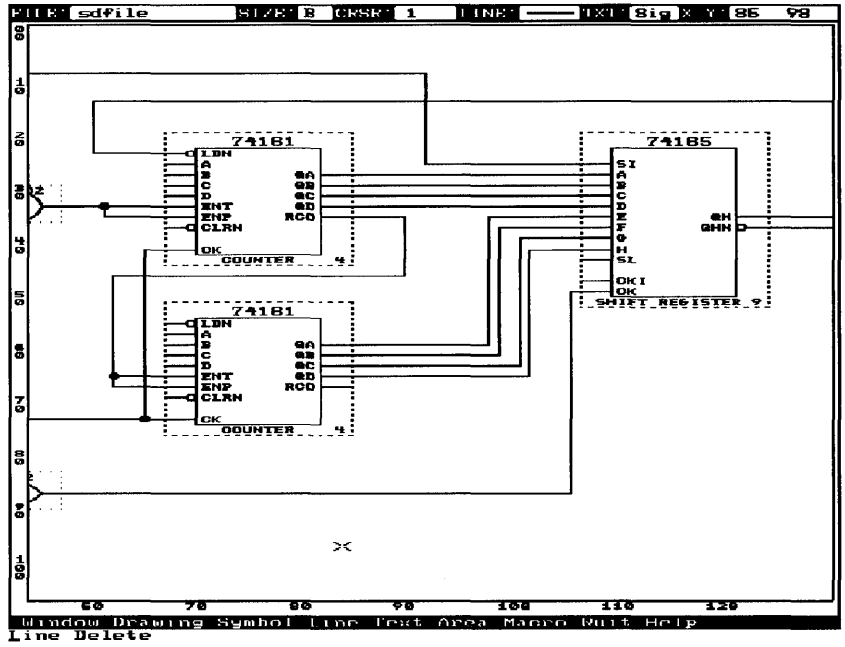
- The A+PLUS Primitive Library includes basic logic gates and flip-flops.
- The A+PLUS TTL MacroFunction Library has more than 120 TTL-equivalent macrofunctions, including counters, decoders, and comparators. This library also includes A+PLUS-specific macrofunctions that are optimized for the Classic EPLD architecture. See Table 1.
- User-defined libraries can be created easily with the Altera Design Librarian (ADLIB), which allows custom development of new macrofunction elements.

Table 1. Partial List of A+PLUS Macrofunctions

Type	Macrofunctions
Adder	7480, 7482, 7483, 74183, 8FADD
Comparator	7485, 74158, 74518, 8MCOMP
Converter	74184, 74185
Counter	7493, 74160, 74161, 74162, 74163, 74190, 74191, 74393, 74160T, 74161T, 74162T, 74163T, 74190T, 74191T, 74192T, 74193T, 8COUNT, 4COUNT, 16CUDSLR, UNICNT2, GRAY4
Decoder	7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 74138, 74139, 74154, 74155, 74156
Flip-Flop	7470, 7471, 7472, 7473, 7474, 7476, 7478, 74173, 74174, 74175, 74273, 74374
Frequency Divider	FREQDIV
Latch	7475, 7477, 74116, 74259, 74279, 74373, NANDLTCH, NORLTCH
Multiplier	74261, MULT2, MULT24, MULT4
Multiplexer	74147, 74148, 74151, 74153, 74157, 74158, 74298, 21MUX
Parity Generator	74180, 74280
Shift Register	7491, 7494, 7496, 7499, 74164, 74165, 74166, 74178, 74179, 74194, 74198, BARRELST, UNICNT2
SSI Function	7400, 7402, 7404, 7408, 7410, 7411, 7420, 7421, 7427, 7430, 7432, 7486, INHB, CBUF
Storage Register	7498, 74278
True/Comp Element	7487
ALU	74181

LogiCaps features easy-to-use mouse and keyboard command entry. Tag-and-drag editing with orthogonal rubberbanding, multiple zoom levels, and a dual-window display mode simplifies schematic entry. See Figure 2. Schematics can be printed on Epson FX- and LQ-series printers, and HP7475A, and 7585B, and 7495A drafting plotters. An Altera Design File (.ADF) is generated when a design is saved and can be linked with other design files or processed directly with the ADP to generate a JEDEC File (.JED).

Figure 2. Schematic Design Entry with LogiCaps



Boolean Equation Entry

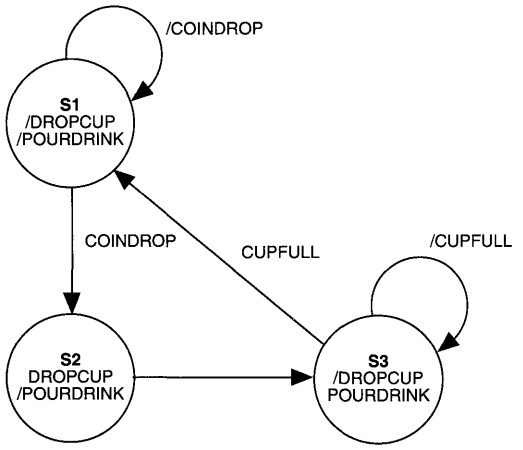
The ADF syntax supports Boolean equation design entry and features free-form entry of all syntactical elements. Boolean equations need not be entered with a minimized sum-of-products form because the ADP automatically minimizes the equations before generating the JEDEC File (.JED) for programming. An ADF is created with any standard text editor (in non-document mode). Once a design has been entered, it can be linked with schematic or state machine files, or directly processed by the ADP.

State Machine and Truth Table Entry

State machine designs are entered in Altera's State Machine File (.SMF) format (see Figure 3). This high-level language description features

IF-THEN statements, CASE statements, and truth tables. Outputs of state machines may be defined conditionally or unconditionally, allowing flexible output structures to be merged with other portions of the design. SMF syntax also allows multiple state machines to be defined in a single file. Truth tables may also be used to specify random logic. Once a design has been entered, A+PLUS automatically generates state equations and transforms state machine descriptions, automatically choosing D or T flip-flops for the state variables to ensure the most efficient use of EPLD resources.

Figure 3. State Machine Diagram and Partial State Machine File




```
MACHINE: dispenser
  CLOCK:   CLK
  STATES:  [DROPCUP   POURDRNK]
  S1       [   0         0    ]
  S2       [   1         0    ]
  S3       [   0         1    ]

S1:
  IF COINDROP THEN S2
  % No outputs %
S2:
  S3
S3:
  IF CUPFULL THEN S1
```

Design Processing

The Altera Design Processor (ADP) consists of a series of modules that automatically transforms the design into a JEDEC File (.JED) used to program the EPLD. First, the Flattener module "flattens" the high-level macrofunctions to low-level gate primitives. Next, the ADP analyzes the complete logic circuit and removes unused gates and flip-flops. This "MacroMunching" feature enables the designer to freely use macrofunctions without worrying about optimizing the logic.

When the ADP detects macrofunctions with unconnected inputs, it assigns "intelligent" default values: active-high inputs default to GND, active-low inputs default to V_{CC}. Thus, the ADP enhances productivity by automatically performing some of the designer's "busy work."

The Translator module checks the design for logical completeness and consistency. For example, it ensures that no two logic function outputs are tied together and that all logic nodes have an origin. Also, if AUTO is entered as the EPLD name, the Translator automatically selects the EPLD best suited to the logic requirements of the design.

The Expander module expands the Boolean equations into sum-of-products form, checks for evidence of combinatorial feedback, and removes redundant factors from product terms.

Logic minimization of designs is performed by the Minimizer module. Minimization tools include Boolean minimization with SALSA (Speedy Altera Logic Simplifying Algorithm), which yields results that are superior to other heuristic reduction techniques. The Minimizer uses algorithms that select equations best represented by a complemented AND/OR function. This feature reduces product-term demands generated by complex logic functions. Moreover, for Altera EPLDs with programmable flip-flops, the Minimizer determines which type of flip-flop yields the most efficient solution and, if necessary, converts the architecture to D or T flip-flops.

The fully minimized design is then transferred to the Fitter module. The fitting routine relies on algorithms based on artificial intelligence software techniques to place and route the logic into the specified EPLD. If a pin assignment is specified, the Fitter matches the request. If no pin assignments are specified, the Fitter automatically finds the best fit for all pins.

Regardless of whether a fit is achieved, the Fitter generates a Utilization Report (.RPT) that documents macrocell and pin assignments, input and output pin names, and buried registers, as well as any unused resources. At the end of design processing, the Assembler module generates an industry-standard JEDEC programming file.

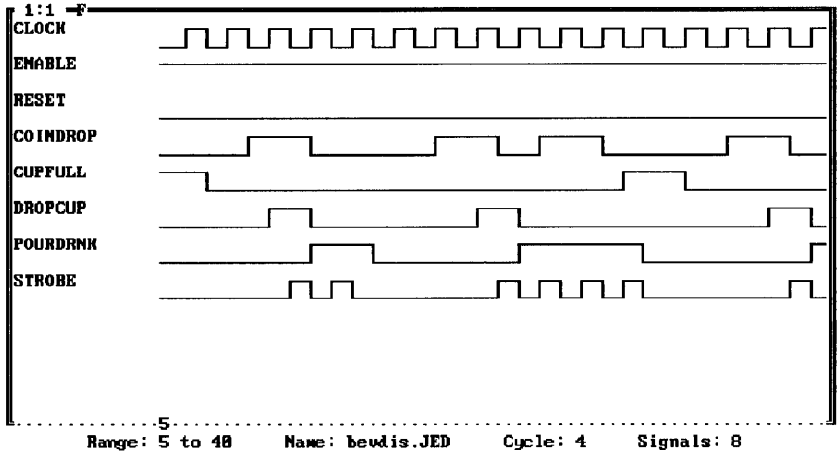
Simulation

The Functional Simulator (FSIM) is a convenient and easy-to-use tool for testing design logic before it is committed to silicon. FSIM uses the JEDEC File (.JED) generated by the ADP. Input logic values with state tables, vector patterns, or predefined patterns may be defined with any standard text editor. Design debugging is aided with the BREAK, FORCE, SAVE, and RESTORE commands; buried nodes can also be accessed. Interactive simulation results are displayed either graphically with the Virtual Logic Analyzer (VLA) or in a tabular format. The results may be printed in either format with an Epson or compatible printer. Figure 4 shows the output of the VLA. The designer can simulate interactively from the keyboard, or a Command File (.CMD) can be generated to perform batch-mode simulation.

Device Programming

LogicMap II programming software is included in the A+PLUS package. The software uses the Altera Super-Adaptive Programming (ASAP) algorithm, which significantly reduces the time required to program an EPLD. LogicMap II uses the JEDEC File (.JED) created by A+PLUS and Altera programming hardware to program the target EPLD. LogicMap II also reads and produces JEDEC Files from programmed EPLDs and verifies programmed devices.

Figure 4. Virtual Logic Analyzer Output



PLCAD-SUPREME provides all hardware necessary for programming and verifying Classic EPLDs. The hardware includes an add-on card for IBM PC-AT, PS/2, or compatible computers that drives the Altera Master Programming Unit (MPU). If the Security Bit of a device is off, the designer can also read the contents of a Classic device and use this information to program additional EPLDs.

Data I/O and several other third-party manufacturers also provide programming support for Altera EPLDs.

Package Contents

PLCAD-SUPREME

The complete A+PLUS development system includes both hardware and software:

- ❑ LogiCaps schematic capture
- ❑ Boolean equation, netlist, state machine, and truth table design entry
- ❑ Altera Design Processor (ADP)
- ❑ Functional Simulator (FSIM)
- ❑ Virtual Logic Analyzer (VLA)
- ❑ LogicMap II programming software
- ❑ Documentation
- ❑ Master Programming Unit (MPU)
- ❑ Programming card (LP6 for IBM PC/AT or compatible; LP5 for IBM PS/2 Model 50 or higher or compatible)
- ❑ Programming adapters (PLED610, PLED910, PLEJ1810)
- ❑ Sample EPLDs

PLS-SUPREME

The complete A+PLUS software includes:

- ❑ LogiCaps schematic capture
- ❑ Boolean equation, netlist, state machine, and truth table design entry
- ❑ Altera Design Processor (ADP)
- ❑ Functional Simulator (FSIM)
- ❑ Virtual Logic Analyzer (VLA)
- ❑ LogicMap II programming software
- ❑ Documentation

Ordering Information

PLCAD-SUPREME	(IBM PC-AT or compatible)
PLCAD-SUPREME/PS	(IBM PS/2 Model 50 and higher or compatible)
PLS-SUPREME	(IBM PC-AT, PS/2, or compatible)

System Requirements

Minimum System Configuration

- ❑ IBM PC-AT, PS/2 Model 50 or higher, or compatible computer
- ❑ DOS version 3.1 or higher
- ❑ 640 Kbytes of memory
- ❑ 20 Mbytes free disk space
- ❑ VGA or EGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ 3-button serial-port mouse or 2-button Microsoft-compatible serial-port or bus mouse (plus a serial port for a serial-port mouse)
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Recommended System Configuration

- ❑ 20-MHz or higher 386-based IBM PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ DOS version 3.3 or higher
- ❑ 640 Kbytes of memory
- ❑ 20 Mbytes free disk space
- ❑ VGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ Serial port and 3-button serial-port mouse
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

PLDS-SAM & PLS-SAM

SAM+PLUS Programmable Logic Development System & Software

September 1991, ver. 1

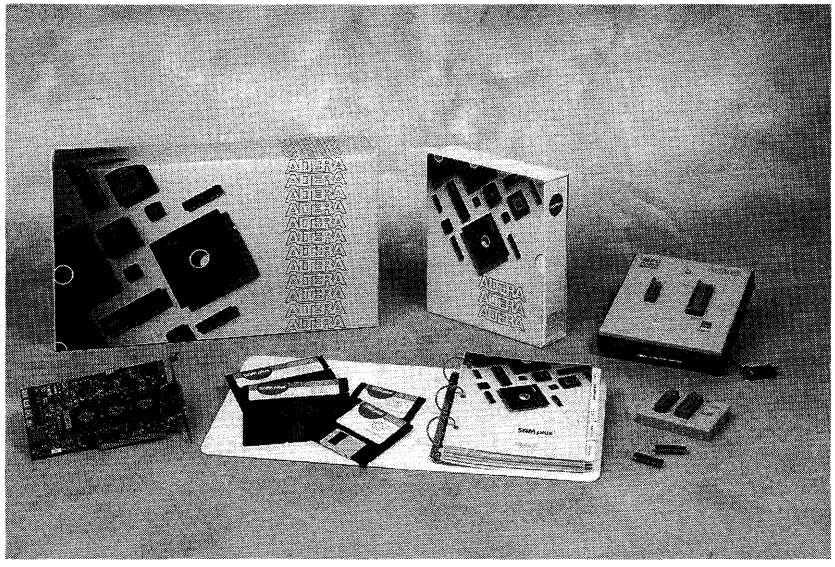
Data Sheet

Features

- ❑ Software support for Altera's EPS448 Stand-Alone Microsequencer (SAM) EPLDs
- ❑ Altera State Machine Input Language (ASMILE) entry method
- ❑ Assembly Language (ASM) entry method
- ❑ User-definable macros
- ❑ SAM Design Processor (SDP) that generates industry-standard JEDEC Files (.JED)
- ❑ SAMSIM interactive functional simulator with Virtual Logic Analyzer (VLA) user interface
- ❑ Disassembler to examine assembly code during simulation
- ❑ Full support for horizontal cascading of multiple EPS448 EPLDs
- ❑ Device programming with LogicMap II software and Altera programming hardware
- ❑ Runs on IBM PC-AT, PS/2 and compatible computers

General Description

SAM+PLUS provides a complete software solution for implementing state machine and microcoded applications in Altera's EPS448 SAM EPLD. SAM+PLUS is a comprehensive, easy-to-use system that includes state machine and assembly language design entry, design processing with the SAM Design Processor (SDP), and design debugging with SAMSIM. The



EPS448 EPLD is programmed with Altera's LogicMap II software and programming hardware. Figure 1 shows a block diagram of SAM+PLUS .

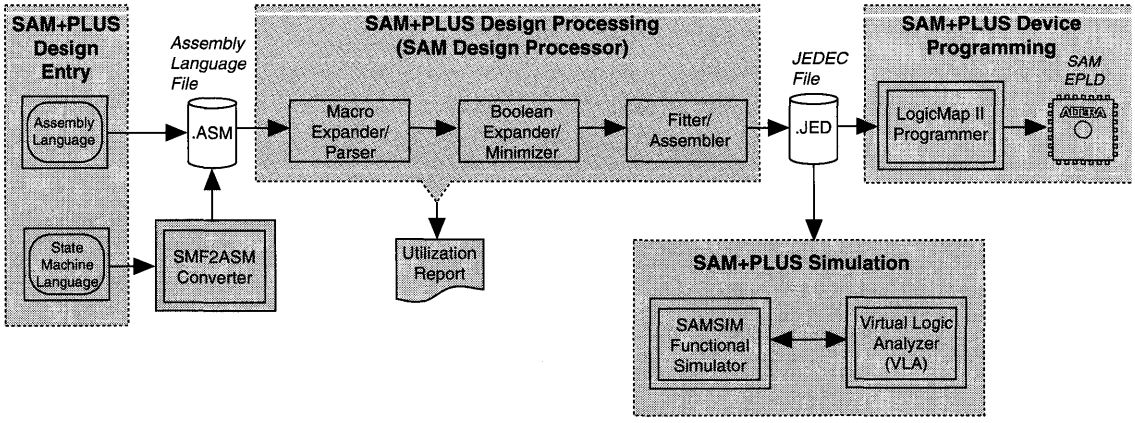
The PLDS-SAM Development System includes SAM+PLUS software, all hardware required to program SAM EPLDs, and device samples. PLS-SAM is a software-only package. See "Package Contents" later in this data sheet for more information.

The SDP accepts two forms of design entry—state machine and assembly language—and automatically generates an industry-standard JEDEC File (.JED) for simulation and programming. SAMSIM is an interactive functional simulator created especially to verify state machine and microcoded designs implemented in EPS448 EPLDs.

Designs are entered in either the Altera State Machine Input Language (ASMILE) or the Altera Assembly Language (ASM). A standard text editor is used to create the input file with either method. If ASMILE is used, the State Machine File (.SMF) is processed by a converter to produce an ASM file. The various modules of the SDP then process the ASM file. The SDP produces three outputs: a JEDEC File used to simulate and program the EPS448 EPLD, an error log file, and a utilization report file that shows how resources within the EPLD are used.

After the JEDEC File is created, the user can simulate the design with the SAMSIM functional simulator, which provides an interactive design-debugging environment. The disassembler converts object code back into the original ASM source code during simulation, and the Virtual Logic Analyzer (VLA) provides on-screen examination of input and output waveforms.

Figure 1. SAM+PLUS Block Diagram



Horizontal cascading (i.e., using multiple EPS448 EPLDs to increase the number of outputs) is fully supported in design entry, processing, simulation, and programming. Multiple EPS448 EPLDs are listed in a single source file, but separate report and JEDEC Files are created for each device.

Finally, the EPS448 EPLD is programmed with LogicMap II software and Altera programming hardware.

State Machine Design Entry

SAM+PLUS software supports high-level state machine design entry through ASMILE. A designer can use this language with any standard text editor to create a file describing a state machine. The State Machine File-to-Assembly Language File (SMF2ASM) Converter translates the SMF into an equivalent ASM file before sending it to the SDP.

ASMILE provides a simple yet comprehensive means of converting a conceptual state diagram into a simple text description. Figure 2 shows the state diagram for a 68020 bus arbiter. Each circle represents a state; the values within the circles represent the output values for that state; and the expressions adjacent to the arrows represent the conditional branches between states.

Figure 2. State Diagram for a 68020 Bus Arbiter

R Bus request input
A Bus grant acknowledge input
G Bus grant output
T Tri-state control to bus-control logic
X Don't care

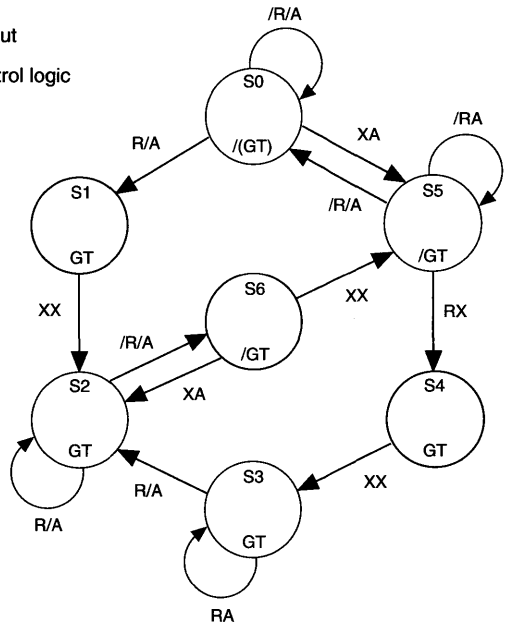


Figure 3 shows the ASMILE description of the state machine shown in Figure 2. The states and their respective outputs have been defined in the States Section with a truth table, and the transitions between states have been defined with simple IF-THEN constructs. Once this file is created, it can be submitted to the SDP without any further modifications.

Figure 3. State Machine File

```
DESIGNER NAME
COMPANY NAME
9/1/91
68020 Bus Arbitration Controller for EPS448 SAM EPLD

PART:     EPS448
INPUTS:   REQUEST ACK
OUTPUTS:  GRANT TRISTATE
MACHINE:  BUSARBITER
CLOCK:    CLK

% The state table defines the outputs for each state %
STATES:   [  GRANT TRISTATE  ]
S0        [    0       0     ]
S1        [    1       1     ]
S2        [    1       1     ]
S3        [    1       1     ]
S4        [    1       1     ]
S5        [    0       1     ]
S6        [    0       1     ]

% Transition specifications %
S0:   IF REQUEST*/ACK THEN S1
      IF ACK THEN S5
      S0
S1:   S2
S2:   IF /REQUEST */ACK +ACK THEN S6
      S2          % IMPLIED ELSE %
S3:   IF /REQUEST THEN S6
      IF REQUEST*/ACK THEN S2
      S3
S4:   S3
S5:   IF /REQUEST*/ACK THEN S0
      IF REQUEST THEN S4
      S5
S6:   S5

END$
```

Assembly Language Design Entry

Direct ASM design entry is also available for those who prefer to use EPS448 EPLDs for microcoded controller designs. This entry method provides access to the advanced features of the EPS448 device, including the on-chip stack and loop counter. Thirteen instructions directly control such functions as multiway branching, subroutines, nested FOR-NEXT loops, and dispatch calls (i.e., jumping to an externally specified address).

User-defined macros that allow users to define their own instruction mnemonics are also available, providing a higher-level design entry approach. Macros can also be used to define values for various output fields so that the designer does not have to work at the binary level.

Figure 4 shows an example of an ASM file in which macros have been used to define the seven new instructions GOTOS0 through GOTOS6.

Figure 4. Assembly Language File

```
DESIGNER NAME
COMPANY NAME
9/1/91
68020 Bus Arbitration Controller for EPS448 SAM EPLD

PART:    EPS448
INPUTS:  REQUEST ACK
OUTPUTS: GRANT TRISTATE

MACROS:
GOTOS0 = "[00] JUMP S0"
GOTOS1 = "[11] JUMP S1"
GOTOS2 = "[11] JUMP S2"
GOTOS3 = "[11] JUMP S3"
GOTOS4 = "[11] JUMP S4"
GOTOS5 = "[01] JUMP S5"
GOTOS6 = "[01] JUMP S6"

PROGRAM:
%   BUSARBITER   %
%   CLK          %
0D:  GOTOS0;
S0:  IF REQUEST*/ACK THEN GOTOS1;
     ELSEIF ACK THEN   GOTOS5;
     ELSE GOTOS0;
S1:   GOTOS2;
S2:  IF /REQUEST*/ACK+ACK THEN GOTOS6;
     ELSE GOTOS2;
S3:  IF /REQUEST THEN GOTOS6;
     ELSEIF REQUEST*/ACK THEN GOTOS2;
     ELSE GOTOS3;
S4:  GOTOS3;
S5:  IF /REQUEST*/ACK THEN GOTOS0;
     ELSEIF REQUEST THEN GOTOS4;
     ELSE [01] JUMP S5;
S6:  GOTOS5;

END$
```

Design Processing

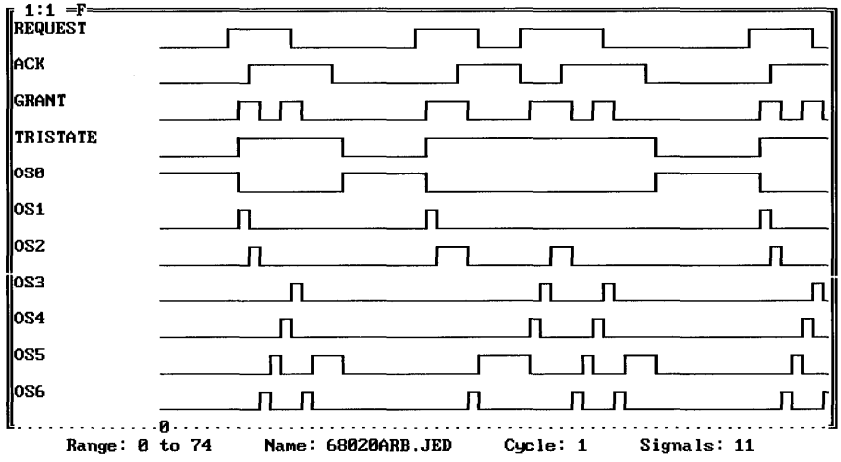
The SDP takes an ASM file and creates an optimized JEDEC File for the target EPLD. This process includes the following steps:

- The user-defined macros are expanded.
- The design is parsed, and any syntax or connection errors are listed in an error log file.
- The Boolean expressions that define the transition conditions are minimized.
- The design is fitted into the EPS448 EPLD and an industry-standard JEDEC programming file is generated. A utilization report that shows how the design is implemented in the EPS448 EPLD is also created.

Simulation

Once a design has been processed, it can be simulated with the SAMSIM Functional Simulator. SAMSIM provides a comprehensive design debugging environment. The Virtual Logic Analyzer (VLA) displays the input and output waveforms interactively, providing multiple zoom levels, split screens, and differential time displays (see Figure 5). The internal state of the EPS448 EPLD, including the stack and counter, can be examined and modified. An online disassembler can convert the actual object code back into the original ASM source code.

Figure 5. Virtual Logic Analyzer



Device Programming

LogicMap II programming software is included in the SAM+PLUS package. The software uses the Altera Super Adaptive Programming (ASAP) algorithm, which significantly reduces the time required to program an EPLD. LogicMap II uses the JEDEC File created by SAM+PLUS and Altera programming hardware to program the EPS448 EPLD. LogicMap II also reads and produces JEDEC Files from EPS448 EPLDs and verifies programmed devices.

PLDS-SAM provides all hardware necessary for programming and verifying the EPS448 EPLD. The hardware includes an add-on card for IBM PC-AT, PS/2, or compatible computers that drives the Altera Master Programming Unit (MPU). If the Security Bit of a device is off, the designer can also read the contents of an EPS448 device and use this information to program additional EPLDs.

Data I/O and several other third-party manufacturers also provide programming support for Altera EPLDs.

Package Contents

PLDS-SAM

The complete SAM+PLUS development system includes both hardware and software:

- ❑ Altera State Machine Language (ASMILE)
- ❑ Assembly Language (ASM)
- ❑ SAM Design Processor (SDP)
- ❑ Functional Simulator (SAMSIM)
- ❑ Disassembler
- ❑ Virtual Logic Analyzer (VLA)
- ❑ LogicMap II programming software
- ❑ Documentation
- ❑ Master Programming Unit (MPU)
- ❑ Programming card (LP6 for IBM PC-AT or compatible; LP5 for IBM PS/2 Model 50 or higher or compatible)
- ❑ Programming adapter (PLED448)
- ❑ Sample EPLDs

PLS-SAM

The complete SAM+PLUS software includes:

- ❑ Altera State Machine Language (ASMILE)
- ❑ Assembly Language (ASM)
- ❑ SAM Design Processor (SDP)
- ❑ Functional Simulator (SAMSIM)
- ❑ Disassembler
- ❑ Virtual Logic Analyzer (VLA)
- ❑ Documentation

Ordering Information

PLDS-SAM	(IBM PC-AT or compatible)
PLDS-SAM/PS	(IBM PS/2 Model 50 and higher or compatible)
PLS-SAM	(IBM PC-AT, PS/2, or compatible)

System Requirements

Minimum System Configuration

- ❑ IBM PC-AT, PS/2 Model 50 or higher, or compatible computer
- ❑ DOS version 3.1 or higher
- ❑ 640 Kbytes of memory
- ❑ 20 Mbytes free disk space
- ❑ VGA or EGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Recommended System Configuration

- ❑ 20-MHz or higher 386-based PC-AT computer; PS/2 Model 70 or higher, or compatible computer
- ❑ DOS version 3.3 or higher
- ❑ 640 Kbytes of memory
- ❑ 20 Mbytes free disk space
- ❑ VGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

PLDS-ENCORE

MAX+PLUS, A+PLUS & SAM+PLUS Programmable Logic Development System

September 1991, ver. 2

Data Sheet

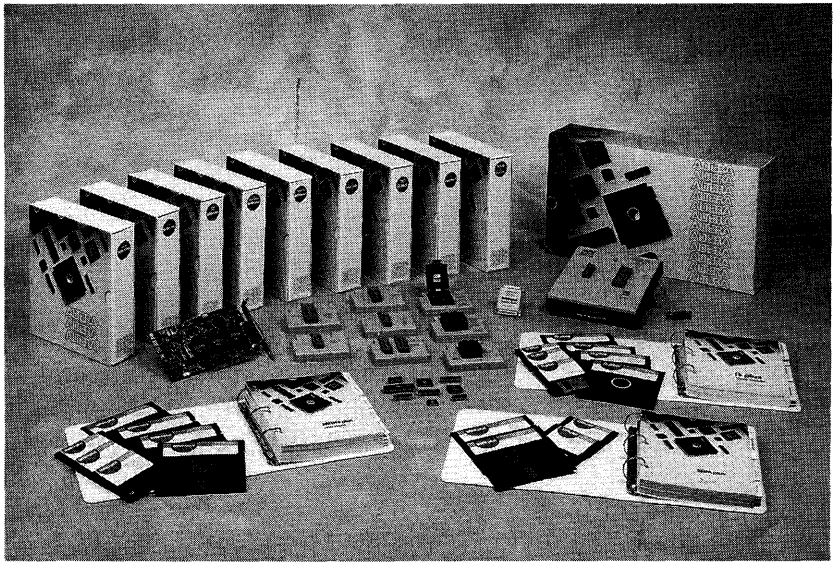
Contents

- PLS-MAX—MAX+PLUS Programmable Logic Software
- PLS-SUPREME—A+PLUS Programmable Logic Software
- PLS-SAM—SAM+PLUS Programmable Logic Software
- PL-ASAP—Altera Stand-Alone Programmer:
  - Software-controlled Logic Programmer interface card
  - Master Programming Unit (MPU)
- Programming adapters:
  - PLED5016 – PLEJ5128 – PLEJ1810
  - PLED5032 – PLED610 – PLED448
  - PLEJ5064 – PLED910
- Sample EPLDs for evaluation

General Description

PLDS-ENCORE supports design entry, logic optimization, design verification, and design programming for all Classic, MAX 5000, and SAM EPLDs.

MAX 5000 (Multiple Array MatriX) EPLD designs are implemented with PLS-MAX—MAX+PLUS Programmable Logic Software. Designs can be entered with any combination of hierarchical schematic files, and hierarchical text files containing Boolean equations, state machines, and truth tables in the Altera Hardware Description Language (AHDL). Over



three hundred 7400-series TTL and special-purpose macrofunctions are available for design entry. MAX+PLUS also includes a fast and efficient design compiler, automatic error location, delay prediction, interactive timing simulation, timing analysis, and device programming applications.

Classic EPLD designs are implemented with PLS-SUPREME (A+PLUS Programmable Logic Software). PLS-SUPREME supports schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. It includes LogiCaps schematic capture, TTL MacroFunction Library, Altera Design Librarian (ADLIB), State Machine Entry, Altera Design Processor, Functional Simulator (FSIM), and LogicMap II software.

SAM (Stand-Alone Microsequencer) EPLD designs are implemented with PLS-SAM (SAM+PLUS Programmable Logic Software). SAM+PLUS includes state machine and microcode design entry, the SAM Design Processor, the SAMSIM Functional Simulator, and LogicMap II software.

The PLDS-ENCORE Development System includes all necessary hardware—a Logic Programmer card, Master Programming Unit, and a range of programming adapters—to program Classic, MAX 5000, and SAM EPLDs at the designer's desktop.

Individual PLDS-ENCORE components can be purchased separately. However, PLDS-ENCORE provides a full range of EPLD logic development support at a significant savings compared with the cost of purchasing each individual software application separately.

See the individual data sheets for PLDS-ENCORE components (in this data book) for additional information on Altera software and hardware.

Package Contents

PLDS-ENCORE

The PLDS-ENCORE Development System includes both hardware and software:

- ❑ PLS-SUPREME development software
- ❑ PLS-MAX development software
- ❑ PLS-SAM development software
- ❑ Documentation
- ❑ Programming card (LP6 for 386- or 486-based IBM PC-AT or compatible, LP5 for IBM PS/2 Model 50 or higher or compatible)
- ❑ Master Programming Unit (MPU)
- ❑ Programming adapters (PLED5016, PLED5032, PLEJ5064, PLEJ5128, PLED610, PLED910, PLEJ1810, PLED448)
- ❑ Sample EPLDs

Ordering Information

PLDS-ENCORE	(IBM PC-AT or compatible)
PLDS-ENCORE/PS	(IBM PS/2 Model 50 and higher or compatible)

System Requirements

Minimum System Configuration

- ❑ IBM PC-AT, PS/2 Model 50 or higher, or compatible computer
- ❑ DOS version 3.1 or higher
- ❑ 640 Kbytes of memory
- ❑ 1 Mbyte of expanded memory with version 3.2 or higher of Lotus/Intel/Microsoft (LIM) Expanded Memory Specification
- ❑ 20 Mbytes free disk space
- ❑ VGA or EGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ 3-button serial-port mouse or 2-button Microsoft-compatible serial-port or bus mouse (plus a serial port for a serial-port mouse)
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Recommended System Configuration

- ❑ 33-MHz 386- or 486-based IBM PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ DOS version 3.3 or higher
- ❑ 640 Kbytes of memory
- ❑ 2 Mbytes of expanded memory with LIM 3.2-compatible driver
- ❑ 20 Mbytes free disk space
- ❑ VGA graphics display
- ❑ 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- ❑ Serial port and 3-button serial-port mouse
- ❑ Full-length 8-bit slot for programming card
- ❑ Parallel port

Notes:

PLS-EDIF

Bidirectional EDIF Netlist Interface to MAX+PLUS Software

September 1991, ver. 3

Data Sheet

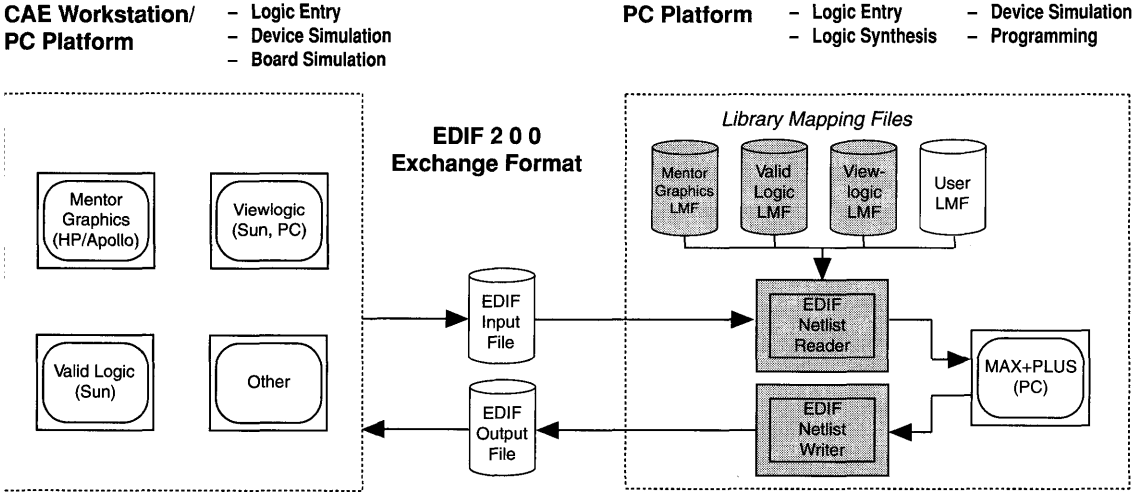
Features

- Provides a bidirectional netlist interface between MAX+PLUS and other major CAE software packages
- Supports the industry-standard Electronic Design Interchange Format (EDIF) version 2 0 0
- Allows MAX 5000 EPLD designs to be created with workstation CAE tools and transferred to MAX+PLUS for compilation; compiled designs can be returned to the workstation for device- or system-level simulation
- Altera EDIF netlist reader imports EDIF netlists into MAX+PLUS.
- Altera-provided Library Mapping Files convert basic gate and many common TTL functions from Mentor Graphics, Valid Logic, and Viewlogic CAE tools to equivalent MAX+PLUS functions.
- Altera EDIF netlist writer produces post-synthesis logic and delay information used during device- or board-level simulation with popular CAE tools.
- PLS-EDIF runs on IBM PC-AT, PS/2, or compatible computers.

General Description

The Altera PLS-EDIF toolkit is a bidirectional EDIF netlist interface between PC- or workstation-based CAE software packages and the Altera MAX+PLUS Programmable Logic Development System. See Figure 1.

Figure 1. PLS-EDIF Block Diagram *Shading indicates items provided with PLS-EDIF.*



PLS-EDIF (Bidirectional EDIF Netlist Interface to MAX+PLUS Software) allows designers to enter and verify logic designs for Altera MAX 5000 EPLDs with third-party CAE tools. The EDIF 2 0 0 netlist exchange format provides a two-way bridge between MAX+PLUS and third-party schematic capture and simulation tools. PLS-EDIF runs on an IBM PS/2, PC-AT, or compatible computer.

Any CAE software package that produces EDIF 2 0 0 netlists can use the PLS-EDIF interface to MAX+PLUS. EDIF netlists are imported into MAX+PLUS with the Altera EDIF Netlist Reader (EDF2CNF Converter). Library Mapping Files (.LMF) are used with the EDIF Netlist Reader to map library functions from third-party CAE tools to the MAX+PLUS library functions. LMFs are provided for Mentor Graphics, Valid Logic, and Viewlogic software, but designers can create their own LMFs to map any CAE software library.

After a design is imported into MAX+PLUS, it is compiled with the sophisticated MAX+PLUS Compiler, which uses advanced logic synthesis and minimization techniques together with heuristic fitting rules to optimize the design for MAX 5000 EPLD architecture. MAX 5000 devices are then programmed with a Programmer Object File (.POF) created by the MAX+PLUS Compiler and standard Altera or third-party programming hardware.

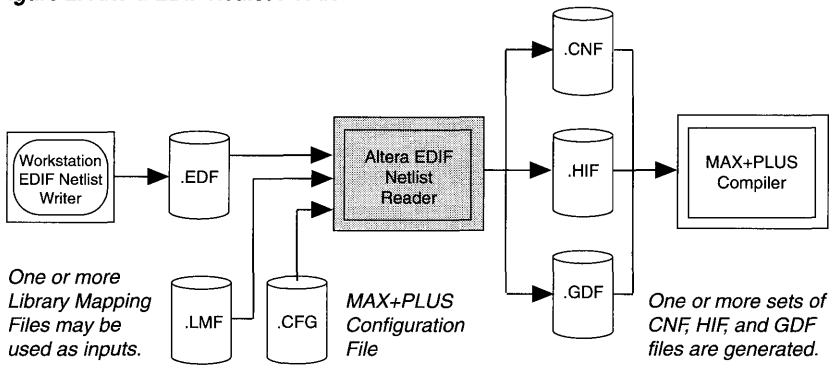
EDIF netlists can be exported from MAX+PLUS with the Altera EDIF Netlist Writer (SNF2EDF Converter). This EDIF Netlist Writer generates an EDIF output file from a compiled MAX+PLUS design. The EDIF file contains the post-synthesis information used by CAE simulators to perform device- or board-level simulation.

PLS-EDIF provides an open environment that allows designers to use popular third-party CAE tools to create and simulate MAX 5000 EPLD designs. The designer may use a preferred workstation schematic capture package to enter a logic design, quickly convert it with the Altera EDIF Netlist Reader, and compile it with MAX+PLUS. Likewise, designs compiled in MAX+PLUS and converted with the Altera EDIF Netlist Writer can be transferred to a workstation for simulation. Together, the PLS-EDIF netlist reader and writer allow MAX 5000 EPLD designs to be entered and simulated with the CAE software and platform of choice.

Altera EDIF Netlist Reader

The Altera EDIF Netlist Reader generates one or more MAX+PLUS Compiler Netlist Files (.CNF) from an EDIF input file. For each CNF, a Hierarchy Interconnect File (.HIF) and a Graphic Design File (.GDF) are also created. See Figure 2. The CNF contains the logic and connectivity data for a design file, while the HIF defines the hierarchical connections between design files. The GDF is a token symbol that represents the actual design data in the CNF. This symbol—and the underlying logic—may be used in a logic schematic in the MAX+PLUS Graphic Editor.

Figure 2. Altera EDIF Netlist Reader



The Altera EDIF Netlist Reader can convert any EDIF 2 0 0 netlist with the following characteristics:

- EDIF level 0
- keyword level 0
- view type NETLIST
- cell type GENERIC

The Altera EDIF Netlist Reader gives designers the flexibility to design logic solely with workstation CAE tools, or to mix design inputs from a variety of platforms and software packages. For example, a third-party workstation CAE schematic converted with the EDIF Netlist Reader may be combined with an Altera Hardware Description Language (AHDL) state machine in MAX+PLUS. Designers can choose the entry methods and platforms that best meet their needs.

LMFs are used with the Altera EDIF Netlist Reader to convert functions of third-party CAE tools to equivalent MAX+PLUS functions. This direct substitution is beneficial because MAX+PLUS functions are optimized for both logic utilization and performance in MAX 5000 EPLD designs.

Workstation nformation

The Altera EDIF Netlist Reader has been specifically tested for use with Mentor Graphics, Valid Logic, and Viewlogic CAE software packages. LMFs for these products are also provided with the PLS-EDIF toolkit.

Mentor Graphics

To design logic and create an EDIF file with Mentor Graphics software, the following applications are required:

- NETED (Mentor Graphics graphics editor) version 7.0 or higher
- EXPAND (Mentor Graphics schematic file translator) version 7.0 or higher
- EDIFNET (Mentor Graphics EDIF netlist writer) version 7.0_2.5 or higher

Table 1 lists the Mentor Graphics basic functions that are mapped to MAX+PLUS-compatible functions.

Table 1. Mentor Graphics Library Mapping File (Basic Functions)

Mentor Graphics Function	MAX+PLUS-Compatible Function	
AND#	AND#	(#=2,3,4,5,6)
BUF	SCLK	
DELAY	MCELL	
DFF	DFF2	
INV	NOT	
JKFF	JKFF2	
LATCH	MLATCH	
NAND#	NAND#	(#=2,3,4,5 6,9)
NOR#	NOR#	(#=2,3,4,6,8,16)
OR#	OR#	(#=2,3,4,6,8)
XFER	TRI	
XNOR2	XNOR	
XOR2	XOR	

Note: Contact Altera Applications for the most up-to-date list of mappings.

/alid Logic

To design logic and create an EDIF file with Valid Logic software, the following applications are required:

- ValidGED (Valid Logic graphics editor) version 10.4 or higher
- ValidCompiler (Valid Logic compiler) version 1.4 or higher
- WEDIFNET (Valid Logic EDIF netlist writer) version 1.1 (SUN4-P1) or higher

Table 2 lists the Valid Logic basic functions that are mapped to MAX+PLUS-compatible functions.

Table 2. Valid Logic Library Mapping File (Basic Functions)

Valid Logic Function	MAX+PLUS-Compatible Function
INV	EXP
LS00	NAND2
LS02	NOR2
LS04	NOT
LS08	AND2
LS10	NAND3
LS11	AND3
LS20	NAND4
LS21	AND4
LS27	NOR3
LS28	NOR2
LS30	NAND8
LS32	OR2
LS37	NAND2
LS40	NAND4
LS74	DFF2
LS86	XOR
LS126	TRI
LS386	XOR

Note: Contact Altera Applications for the most up-to-date list of mappings.

Viewlogic

To design logic and create an EDIF file with Viewlogic software, th following applications are required:

- Viewdraw (Viewlogic graphics editor) version 3.25 or higher
- EDIFNETO (Viewlogic EDIF netlist writer) version 4.0 or higher

Table 3 lists the Viewlogic BUILT-IN functions that are mapped t MAX+PLUS-compatible functions.

Table 3. Viewlogic Library Mapping File (BUILT-IN Functions)

Viewlogic Function	MAX+PLUS-Compatible Function	
AND#	AND#	(#=2,3,4,8)
ANDNOR22	2A2NOR2	
BUF	SOFT	
DAND#	DAND#	(#=2,3,4,8)
DELAY	MCELL	
DOR#	DOR#	(#=2,3,4,8)
DXOR#	DXOR#	(#=2,3,4,8)
JKFFRE	JKFFRE	
MUX41	MUX41	
NAND#	NAND#	(#=2,3,4,8)
NOR#	NOR#	(#=2,3,4,8)
NOT	NOT	
OR#	OR#	(#=2,3,4,8)
TRIAND#	TAND#	(#=2,3,4,8)
TRIBUF	TRIBUF	
TRINAND#	TNAND#	(#=2,3,4,8)
TRINOR#	TNOR#	(#=2,3,4,8)
TRINOT	TRINOT	
TRIOR#	TOR#	(#=2,3,4,8)
UBDEC38	DEC38	
UDFDL	UDFDL	
UJKFF	UJKFF	
XNOR2	XNOR	
XNOR#	XNOR#	(#=3,4,8)
XOR2	XOR	
XOR#	XOR#	(#=3,4,8)

Note: Contact Altera Applications for the most up-to-date list of mappings.

LMF Support for TTL Macrofunctions

In addition to mapping the basic functions listed above, Altera-provided LMFs map various TTL macrofunctions from Mentor Graphics, Valid Logic, and Viewlogic to their MAX+PLUS-compatible equivalents. Table 4 shows macrofunction mappings that are either included in an LMF provided with PLS-EDIF or available from Altera Applications.

Table 4. TTL Function Mappings in Altera-Provided LMFs (Part 1 of 3)

MAX+PLUS	Mentor Graphics	Valid Logic	Viewlogic
7400	74LS00	LS00	74LS00
7402	74LS02	LS02	74LS02
7404	74LS04	LS04	74LS04
7408	74LS08	LS08	74LS08
7410	74LS10	LS10	74LS10
7411	74LS11	LS11	74LS11
7420	74LS20	LS20	74LS20
7421	74LS21	LS21	74LS21
7427	74LS27	LS27	74LS27
7428	74LS28	LS28	74LS28
7430	74LS30	LS30	74LS30
7432	74LS32	LS32	74LS32
7437	74LS37	LS37	74LS37
7440	74LS40	LS40	74LS40
7442	74LS42	LS42	74LS42
7451	74LS51	LS51	74LS51
7454	74LS54	LS54	74LS54
7455	74LS55	LS55	74LS55
7473	74LS73A	LS73	74LS73A
7474	74LS74A	LS74	74LS74A
7475	74LS75	LS75	74LS75
7476	74LS76A	LS76	74LS76A
7477	74LS77	—	74LS77
7478	—	LS78	74LS78A
7483	74LS83A	LS83	74LS83A
7485	74LS85	LS85	74LS85
7486	74LS86	LS86	74LS86
7490	74LS90	LS90	74LS90
7491	74LS91	LS91	74LS91
7492	74LS92	LS92	74LS92
7493	74LS93	LS93	74LS93
7495	74LS95B	LS95	74LS95B
7496	74LS96	LS96	74LS96
74107	74LS107A	LS107	74LS107A
74109	74LS109A	LS109	74LS109A
74112	74LS112A	LS112	74LS112A
74113	74LS113A	LS113	74LS113A

Table 4. TTL Function Mappings in Altera-Provided LMFs (Part 2 of 3)

MAX+PLUS	Mentor Graphics	Valid Logic	Viewlogic
74114	74LS114A	LS114	74LS114A
74133	74LS133	LS133	74LS133
74138	74LS138	LS138	74LS138
74139	74LS139A	LS139	74LS139
74147	74LS147	LS147	74LS147
74148	74LS148	LS148	74LS148
74151	74LS151	LS151	74LS151
74153	74LS153	LS153	74LS153
74154	74LS154	LS154	—
74155	74LS155A	—	74LS155A
74156	74LS156	—	74LS156
74157	74LS157	LS157	74LS157
74158	74LS158	LS158	74LS158
74160	74LS160A	LS160	74LS160A
74161	74LS161A	LS161	74LS161A
74162	74LS162A	LS162	74LS162A
74163	74LS163A	LS163	74LS163A
74164	74LS164	LS164	74LS164
74165	74LS165	LS165	74LS165
74166	74LS166	LS166	74LS166
74168	74LS168A	—	—
74169	74LS169A	LS169	74LS169
74173	74LS173A	LS173	74LS173A
74174	74LS174	LS174	74LS174
74175	74LS175	LS175	74LS175
74181	74LS181	LS181	74LS181
74183	74LS183	LS183	74LS183
74190	74LS190	LS190	74LS190
74191	74LS191	LS191	74LS191
74192	74LS192	LS192	74LS192
74193	74LS193	LS193	74LS193
74194	74LS194A	LS194A	74LS194A
74195	74LS195A	LS195	74LS195A
74196	74LS196	LS196	74LS196A
74197	74LS197	LS197	74LS197
74240	74LS240	LS240	74LS240
74241	74LS241	LS241	74LS241
74244	74LS244	LS244	74LS244
74251	74LS251	LS251	74LS251
74253	74LS253	LS253	74LS253
74257	74LS257	LS257	74LS257
74258	74LS258A	LS258	74LS258
74259	—	LS259	74LS259

Table 4. TTL Function Mappings in Altera-Provided LMFs (Part 3 of 3)

MAX+PLUS	Mentor Graphics	Valid Logic	Viewlogic
74260	74LS260	LS260	74LS260
74261	—	LS261	—
74273	74LS273	LS273	74LS273
74279	74LS279	LS279	74LS279
74280	74LS280	LS280	74LS280
74283	74LS283	LS283	74LS283
74290	74LS290	LS290	74LS290
74293	74LS293	LS293	74LS293
74299	74LS299	LS299	74LS299
74348	74LS348	LS348	74LS348
74353	74LS353	LS353	74LS353
74365	74LS365A	LS365	74LS365A
74366	74LS366A	LS366	74LS366A
74367	74LS367A	LS367	74LS367A
74368	74LS368A	LS368	74LS368A
74373	74LS373	LS373	74LS373
74374	74LS374	LS374	74LS374
74377	74LS377	LS377	74LS377
74379	74LS379	LS379	74LS379
74381	74LS381	LS381	74LS381
74390	74LS390	LS390	74LS390
74393	74LS393	LS393	74LS393

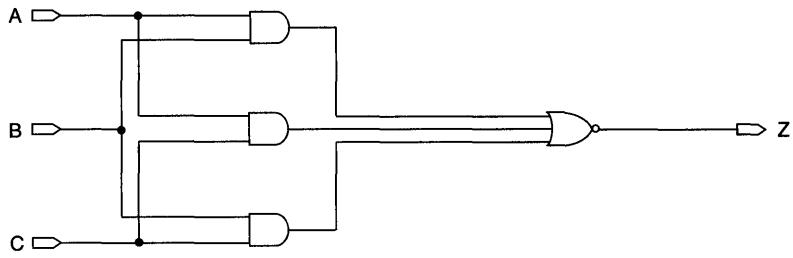
Note: Contact Altera Applications for the most up-to-date list of mappings.

Custom Library Mapping Files

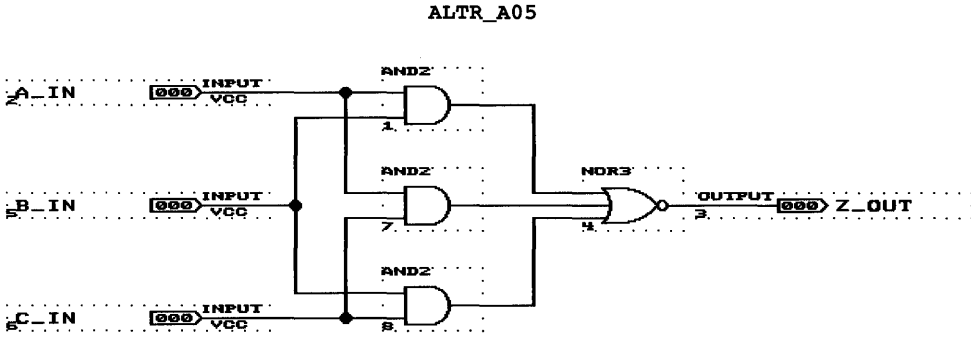
Designers can map their commonly used third-party functions to MAX+PLUS-compatible equivalents by modifying an LMF or creating a new one. If no equivalent function currently exists in MAX+PLUS, the designer can create the function with the MAX+PLUS Graphic Editor or Text Editor and then map it in an LMF. Figure 3 demonstrates this process.

Figure 3. Creating an LMF Mapping

Step 1: Select a third-party function for mapping.



Step 2: Design an equivalent circuit with the MAX+PLUS Graphic Editor.



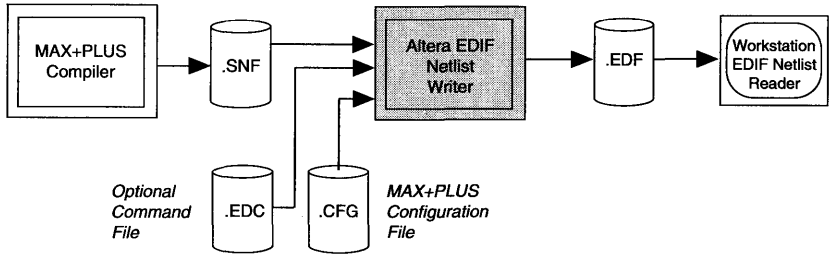
Step 3: Map the third-party function to the MAX+PLUS function in an LMF.

```
LIBRARY new_lib

%User Library Mapping File%

BEGIN
FUNCTION ALTR_A05 (A_IN, B_IN, C_IN)
RETURNS (Z_OUT)
FUNCTION "A05" ("A", "B", "C")
RETURNS ("Z")
END
```

Altera EDIF Netlist Writer

The Altera EDIF Netlist Writer creates an industry-standard level 0 EDIF file from a MAX+PLUS Simulator Netlist File (.SNF). The SNF, which is optionally generated during compilation of a MAX 5000 EPLD design, contains all post-synthesis functional and delay information for the completed design. This design-specific information is also contained in the EDIF output file after conversion, so it can be integrated into a workstation environment for simulation. The user can customize the EDIF output file for various workstation environments with an optional command file that renames certain constructs, or changes the EDIF level or keyword level. See Figure 4.

Figure 4. Altera EDIF Netlist Writer



The EDIF output file may have one of two formats. The first format expresses all delays with special EDIF property constructs. The second expresses combinatorial delays with port-delay constructs and registered delays with path-delay constructs—a format that is especially useful for behavioral simulators. Figure 5 shows an example in both formats.

Figure 5. EDIF File Formats

Format 1: Combinatorial delays expressed with property constructs

```
( instance xor2_5
   ( viewRef view1
      ( cellRef XOR2
   ( property TPD ( integer 20 ) ( unit TIME ) ) )
```

Format 2: Combinatorial delays expressed with port-delay constructs

```
( instance xor2_5
   ( viewRef view1
      ( cellRef XOR2
   ( portInstance &1
      ( portDelay
         ( derivation CALCULATED
         ( delay ( e 20 -10 ) ) ) ) ) )
```

Package Contents

- PLS-EDIF software for IBM PC-AT, PS/2, or compatible computers
  - EDIF Netlist Reader
  - EDIF Netlist Writer
  - Library Mapping Files for Mentor Graphics, Valid Logic Systems and Viewlogic Systems functions
  - MAX+PLUS macrofunctions for Mentor Graphics, Valid Logi Systems, and Viewlogic Systems libraries
  - Sample files
- Documentation

Ordering Information

PLS-EDIF (IBM PC-AT, PS/2, or compatible)

System Requirements

- IBM PC-AT, PS/2 Model 50 or higher, or compatible computer
- DOS version 3.1 or higher
- 640 Kbytes of memory
- 1 Mbyte of expanded memory with version 3.2 or higher of Lotus, Intel/Microsoft (LIM) Expanded Memory Specification
- VGA or EGA display
- 20-Mbyte free disk space
- 1.2-Mbyte, 5 1/4-inch or 1.44-Mbyte, 3 1/2-inch floppy disk drive
- MAX+PLUS version 2.71 or higher
- Workstation-to-PC network hardware and software with the ability t transfer ASCII files

PLS-WS/HP

MAX+PLUS II Programmable Logic Software for HP/Apollo Workstations

September 1991, ver. 3 **Data Sheet**

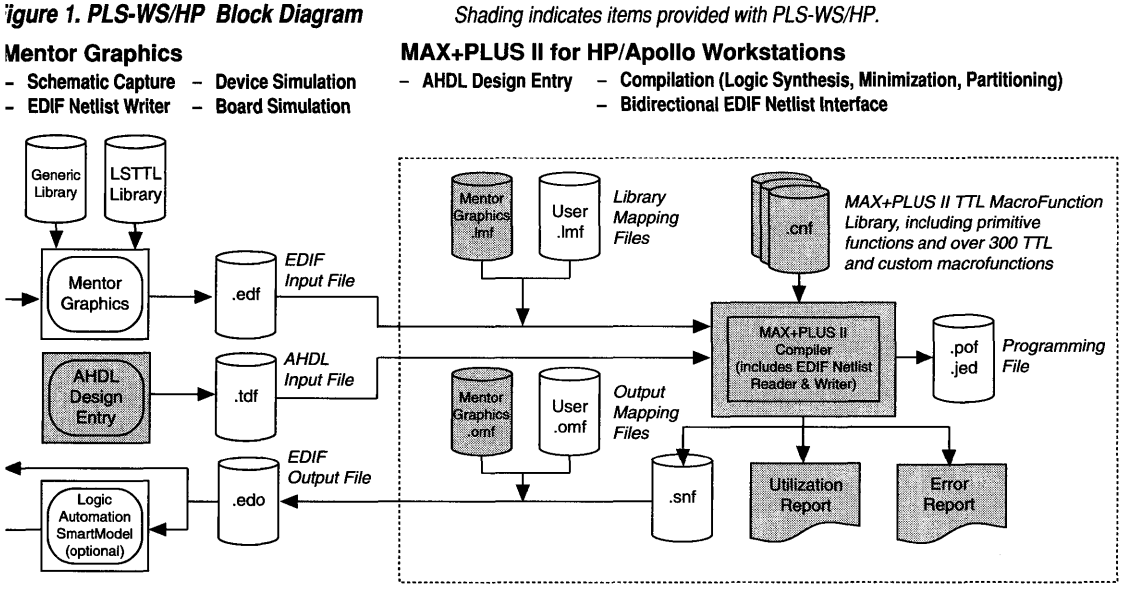
Features

- Software support for Classic, MAX 5000, MAX 7000, and STG EPLDs
- Runs on Hewlett Packard/Apollo Series 3000, 3500, 4000, 4500, and HP400 computers with Domain/OS SR 10.3 operating system
- Provides hierarchical design entry for graphic and text designs
  - Schematic capture with Mentor Graphics' NETED software
  - AHDL supporting state machines, Boolean equations, truth tables, and arithmetic and relational operations
- Full Altera/Mentor Graphics cross-compatibility via bidirectional EDIF 2 0 0 netlist interface
- Logic synthesis and minimization for efficient device utilization with the MAX+PLUS II Compiler
- Partitioning to automatically split large designs among multiple EPLDs
- Generates post-synthesis timing simulation data for use with Logic Automation's SmartModels and Mentor Graphics' QuickSim simulator
- Produces EPLD programming files for use with an Altera PC-based programmer (PL-ASAP) or third-party programming hardware

General Description

The Altera PLS-WS/HP package brings the MAX+PLUS II development software to HP/Apollo Series 3000, 3500, 4000, 4500, and HP400 workstations (see Figure 1). PLS-WS/HP includes Altera Hardware

Figure 1. PLS-WS/HP Block Diagram *Shading indicates items provided with PLS-WS/HP.*



Description Language (AHDL) design entry, bidirectional EDIF netlist interface, Mentor Graphics library support, advanced logic synthesis, automatic partitioning, and design fitting in the HP/Apollo computer environment. Together, MAX+PLUS II and Mentor Graphics software provide the tools to quickly and efficiently create, compile, and verify logic designs for Classic, MAX 5000, MAX 7000, and STG EPLDs.

Design Entry

PLS-WS/HP supports both schematic and text design entry options. Hierarchical schematic designs are entered with the Mentor Graphics NETED schematic capture program. Hierarchical Text Design Files (.tdf) created in AHDL can be used separately or mixed with NETED schematic designs.

Mentor Graphics/ EDIF

NETED schematics are converted into EDIF 2 0 0 netlist files with the Mentor Graphics EDIFNET netlist writer. The MAX+PLUS II Compiler automatically processes these EDIF Input Files (.edf) when the design is compiled (see Figure 2). In addition, symbols from the Mentor Graphics generic and LSTTL libraries can be mapped to corresponding primitive and TTL functions in the MAX+PLUS II TTL MacroFunction Library with a Library Mapping File (.lmf). Table 1 shows the generic functions and Table 2 shows the LSTTL functions mapped in the LMF provided with PLS-WS/HP. Users can add to this LMF or create a new LMF.

Figure 2. Design Entry with PLS-WS/HP

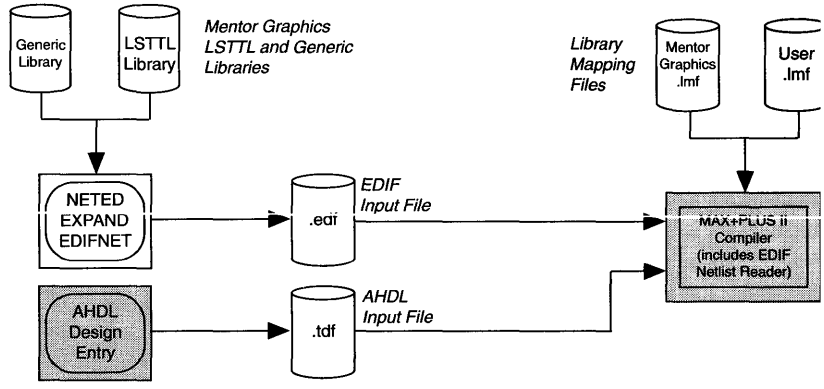


Table 1. Mentor Graphics Library Mapping File—Primitives

Mentor Graphics Generic Function	MAX+PLUS II Primitive Function	
AND#	AND#	(#=2,3,4,5,6)
BUF	SCLK	
DELAY	MCELL	
DFF	DFF2	
INV	NOT	
JKFF	JKFF2	
LATCH	MLATCH	
NAND#	NAND#	(#=2,3,4,5 6,9)
NOR#	NOR#	(#=2,3,4,6,8,16)
OR#	OR#	(#=2,3,4,6,8)
XFER	TRI	
XNOR2	XNOR	
XOR2	XOR	

Note: Contact Altera Applications for the most up-to-date list of mappings.

Table 2. Mentor Graphics Library Mapping File—Macrofunctions (Part 1 of 3)

Mentor Graphics 74LSTTL Function	MAX+PLUS II TTL Macrofunction
74LS00	7400
74LS02	7402
74LS04	7404
74LS08	7408
74LS10	7410
74LS11	7411
74LS20	7420
74LS21	7421
74LS27	7427
74LS28	7428
74LS30	7430
74LS32	7432
74LS37	7437
74LS40	7440
74LS42	7442
74LS51	7451
74LS54	7454
74LS55	7455
74LS73A	7473
74LS74A	7474
74LS75	7475

Table 2. Mentor Graphics Library Mapping File—Macrofunctions (Part 2 of 3)

Mentor Graphics 74LSTTL Function	MAX+PLUS II TTL Macrofunction
74LS76A	7476
74LS77	7477
74LS83A	7483
74LS85	7485
74LS86	7486
74LS90	7490
74LS91	7491
74LS92	7492
74LS93	7493
74LS95B	7495
74LS96	7496
74LS107A	74107
74LS109A	74109
74LS112A	74112
74LS113A	74113
74LS114A	74114
74LS133	74133
74LS138	74138
74LS139A	74139
74LS147	74147
74LS148	74148
74LS151	74151
74LS153	74153
74LS154	74154
74LS155A	74155
74LS156	74156
74LS157	74157
74LS158	74158
74LS160A	74160
74LS161A	74161
74LS162A	74162
74LS163A	74163
74LS164	74164
74LS165	74165
74LS166	74166
74LS168A	74168
74LS169A	74169
74LS173A	74173
74LS174	74174
74LS175	74175
74LS181	74181
74LS183	74183

Table 2. Mentor Graphics Library Mapping File—Macrofunctions (Part 3 of 3)

Mentor Graphics 74LSTTL Function	MAX+PLUS II TTL Macrofunction
74LS190	74190
74LS191	74191
74LS192	74192
74LS193	74193
74LS194A	74194
74LS195A	74195
74LS196	74196
74LS197	74197
74LS240	74240
74LS241	74241
74LS244	74244
74LS251	74251
74LS253	74253
74LS257	74257
74LS258A	74258
74LS260	74260
74LS273	74273
74LS279	74279
74LS280	74280
74LS283	74283
74LS290	74290
74LS293	74293
74LS299	74299
74LS348	74348
74LS353	74353
74LS365A	74365
74LS366A	74366
74LS367A	74367
74LS368A	74368
74LS373	74373
74LS374	74374
74LS377	74377
74LS379	74379
74LS381	74381
74LS390	74390
74LS393	74393

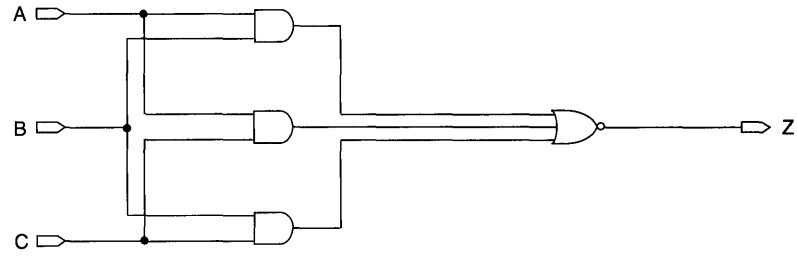
Note: Contact Altera Applications for the most up-to-date list of mappings.

Custom Library Mapping Files

To create a new mapping between a Mentor Graphics symbol and a MAX+PLUS II primitive or macrofunction, the designer follows the process shown in Figure 3. First, the designer selects a NETED function to map. If no equivalent function currently exists in the MAX+PLUS II TTL MacroFunction Library, the designer can create the function in a TDF. Finally, the designer maps the Mentor Graphics function to the MAX+PLUS II function in an LMF.

Figure 3. Creating an LMF Mapping

Step 1: Select a Mentor Graphics function for mapping.



Step 2: Design an equivalent circuit in AHDL if no equivalent function exists in the MAX+PLUS II TTL MacroFunction Library.

```
TITLE "ALTR_A05" ;
DESIGN IS "ALTR_A05" ;
SUBDESIGN ALTR_A05
(  A_IN, B_IN, C_IN : INPUT ;
   Z_OUT : OUTPUT ;
)
VARIABLE
   X1, X2, X3 : NODE ;
BEGIN
   Z_OUT = !(X1 # X2 # X3) ;
   X1 = A_IN & B_IN ;
   X2 = A_IN & C_IN ;
   X3 = B_IN & C_IN ;
END ;
```

Step 3: Map the Mentor Graphics function to the AHDL function in an LMF.

```
LIBRARY user_lib
% User Library Mapping File %

BEGIN
FUNCTION ALTR_A05 (A_IN, B_IN, C_IN)
RETURNS (Z_OUT)
FUNCTION "A05" ("A", "B", "C")
RETURNS ("Z")
END
```

AHDL

AHDL is a high-level, modular language used to create logic designs for Altera EPLDs. AHDL files can be created with any standard text editor. See Figure 4 for a sample AHDL file.

AHDL supports state machines, truth tables, and Boolean equations, as well as arithmetic and relational operations. It is hierarchical, so that frequently used functions such as TTL and bus macrofunctions can be incorporated into a design. AHDL also supports complex arithmetic and relational operations—such as addition, subtraction, equality, and magnitude comparisons—with the automatically generated logic functions. Standard Boolean functions, including AND, OR, NAND, NOR, XOR, and XNOR

Figure 4. Sample AHDL File

```
TITLE "Timed Add and Compare Function";

DESIGN IS "add_cmp" DEVICE IS "EPM5128-2";

FUNCTION 74161 (LDN,A,B,C,D,ENT,ENP,CLRN,CLK)
RETURNS (QA,QB,QC,QD,RCO);

SUBDESIGN add_cmp (
                a[7..0],      % inputs for adder/comparator %
                b[7..0],
                cmpen,
                clock,reset   :INPUT;

                result[7..0],
                elapse[3..0],
                equal,
                less_than,
                grtr_than,
                done          :OUTPUT;
)
VARIABLE
        timer           : 74161; % timer is 74161 counter %
        register[7..0]  : DFF;   % register is an octal FF %
        flag            : NODE;
BEGIN
% set up accumulate register %
        result[] = register[];
        register[].clrn = reset;
        register[].clk = clock;
% this is the actual addition %
        register[] = a[] + b[];
% set flag high if register is not empty %
        flag = (register[] != 0);
        done = flag;
% connect inputs for timer (74161) %
        timer.enp = cmpen & flag;
        timer.clk = clock;
        timer.clrn = reset;
% elapse is the number of clock cycles it takes to do addition %
        elapse[3..0] = (timer.QA,timer.QB,timer.QC,timer.QD);
% the comparator section %
        equal = ( a[] == b[]);
        less_than = (a[] < b[]);
        grtr_than = (a[] > b[]);
END;
```

are also included. Groups are fully supported so operations can be performed on byte- or word-wide functions as well as on single variables. AHDL also allows the designer to specify the location of resources (e.g., latches, flip-flops, and pins) within Altera EPLDs. Together, these features make it easy to implement complex designs in a concise, high-level description.

Design Processing

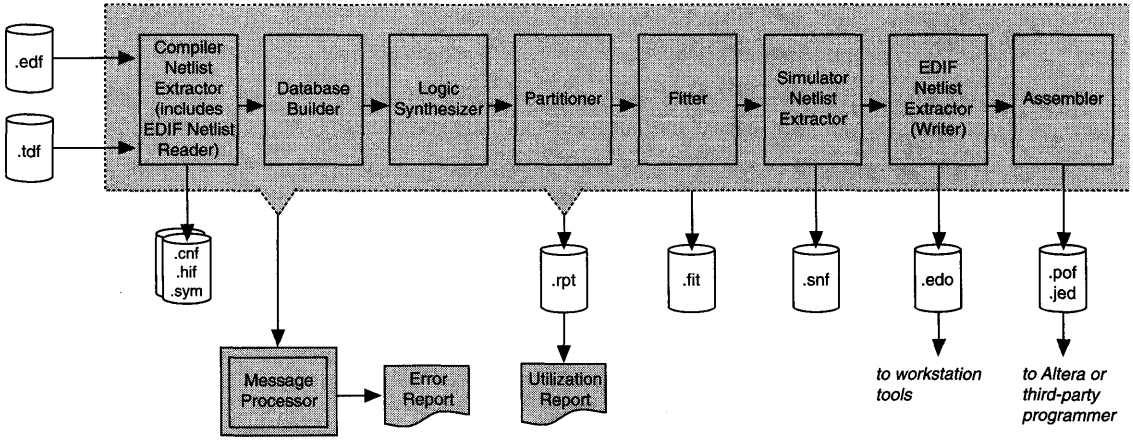
The MAX+PLUS II Compiler processes designs for all Altera general-purpose EPLDs, including the Classic, MAX 5000, MAX 7000, and STG EPLDs (see Figure 5).

Compiler options simplify design processing and analysis. The user can specify up to two LMFs for the Compiler to use in processing EDIF Input Files, and can choose to create an EDIF Output File (.edo) for use with Mentor Graphics simulation tools. Other options specify the degree of detail of the Report File (.rpt) that shows how EPLDs have been utilized and the target EPLD family for the design.

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist used to define the design from the EDIF Input Files (.edf) and AHDL Text Design Files (.tdf). At this time, design rules are checked for any errors. If errors are found, they are displayed by the Message Processor. A successfully extracted design is built into a database and passed to the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the target architecture. The design is first minimized with SALSA (Speedy Altera Logic Simplification Algorithm), which removes any unused logic within the design. The Logic Synthesizer uses expert synthesis rules based on the target architecture (Classic, MAX 5000, MAX 7000, STG) to factor and map logic within the chosen EPLD structure.

Figure 5. MAX+PLUS II Compiler



It then uses advanced synthesis algorithms that ensure the most efficient use of silicon resources.

For large system-level designs, the Partitioner is invoked. The Partitioner uses a sophisticated "Min-Cut" algorithm to separate the logic design into multiple EPLDs from the same family, relieving the designer of the time-consuming task of manually splitting a large design into smaller designs. The user can control the design's partitioning by entering specific chip assignments for flip-flops and pins in the source design files.

After partitioning, the Fitter applies heuristic rules to optimally place the synthesized design into one or more EPLDs. In devices with Programmable Interconnect Array (PIA) structures—i.e., larger MAX 5000 and MAX 7000 EPLDs—or with local/global bus structures such as the EP1810 EPLD, the Fitter also automatically routes signals across this interconnect to relieve the designer of tedious place-and-route tasks. The Report File (.rpt) issued by the Fitter shows design implementation as well as any unused resources in the EPLDs.

The Simulator Netlist Extractor optionally generates a Simulator Netlist File (.snf) that contains logic and timing information. This SNF is used by the EDIF Netlist Extractor to create EDIF Output Files (.edo).

The EDIF Netlist Extractor optionally writes an EDIF 2 0 0 netlist that contains all post-synthesis function and delay information for the completed design, so that it can be integrated into the workstation environment. An EDIF Output File is created for each device used in the design. An Altera-provided or user-created Output Mapping File (.omf) can be used to map MAX+PLUS II functions to Mentor Graphics functions in the EDIF Output File. (Detailed specifications and samples of Altera's EDIF output are available from Altera Applications.)

Finally, the Assembler module creates one or more Programmer Object Files (.pof) and/or JEDEC Files (.jed) from the compiled design. These files are used with standard Altera hardware to program the desired EPLDs. Third-party programming support is also available.

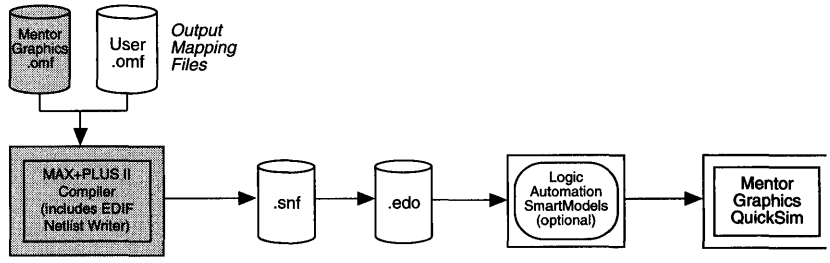
Simulation

After compilation, the user can simulate the design or program EPLDs directly. The Logic Automation SmartModels for Classic and MAX 5000 EPLDs can convert the EDIF Output Files generated by the MAX+PLUS II Compiler into a behavioral model for use with the Mentor Graphics QuickSim simulator. See Figure 6.

Device Programming

The POFs or JEDEC Files produced by the Compiler can be used with an Altera PC-based programmer or third-party programming hardware. (See the *PL-ASAP Data Sheet* in this data book for more information about the Altera Stand-Alone Programmer.)

Figure 6. Simulation with PLS-WS/HP



Package Contents

- Quarter-inch cartridge tape (QIC-24, 9 track) containing all PLS-WS/HP programs and files:
  - MAX+PLUS II Compiler (includes Altera EDIF Netlist Reader and Writer)
  - MAX+PLUS II TTL MacroFunction Library
  - Library Mapping File for mapping Mentor Graphics functions to MAX+PLUS II functions
  - Output Mapping File for mapping MAX+PLUS II functions to Mentor Graphics functions
  - Sample files
- Documentation

Ordering Information

PLS-WS/HP (HP/Apollo workstations)

Note: MAX+PLUS software that supports MAX 5000 EPLDs is available now. MAX+PLUS II software that supports Classic, MAX 5000, MAX 7000, and STG EPLDs will be available in February 1992.

System Requirements

- HP/Apollo Series 3000, 3500, 4000, 4500, or HP400 workstation with 20 Mbytes of free disk space
- Domain/OS SR 10.1 or 10.3 operating system
- Quarter-inch cartridge (QIC-24, 9 track) 60-Mbyte tape drive
- Schematic capture and EDIF conversion software:
  - Mentor Graphics NETED (graphics editor) version 7.0 or higher
  - Mentor Graphics EXPAND (schematic file translator) version 7.0 or higher
  - Mentor Graphics EDIFNET (EDIF 2 0 0 netlist writer) version 7.0_2.5 or higher
- EDIF conversion and simulation software:
  - Logic Automation SmartModels for Classic and MAX 5000 EPLDs (optional)
  - Mentor Graphics QuickSim version 7.0 or higher

PLS-WS/SN

MAX+PLUS II Programmable Logic Software for Sun Workstations

September 1991, ver. 1

Data Sheet

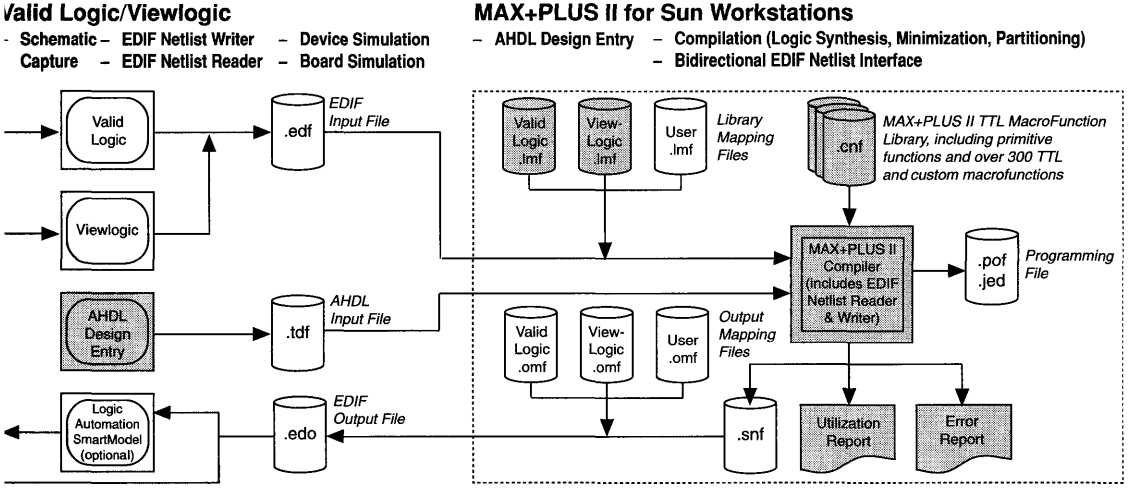
Features

- Software support for Classic, MAX 5000, MAX 7000, and STG EPLDs
- Runs on Sun SPARCstations with SunOS version 4.1.1 or higher
- Provides hierarchical design entry for graphic and text designs
  - Schematic capture with Valid Logic's ValidGED or Viewlogic's Viewdraw software
  - AHDL supporting state machines, Boolean equations, truth tables, and arithmetic and relational operations
- Full Altera/Valid Logic and Altera/Viewlogic cross-compatibility via bidirectional EDIF 2 0 0 netlist interface
- Logic synthesis and minimization for efficient device utilization with the MAX+PLUS II Compiler
- Partitioning to automatically split large designs among multiple EPLDs
- Generates post-synthesis timing simulation data for use with the Valid Logic RapidSIM or Viewlogic Viewsim chip- and board-level simulators or with Logic Automation's SmartModels
- Produces EPLD programming files for use with an Altera PC-based programmer (PL-ASAP) or third-party programming hardware

General Description

The Altera PLS-WS/SN package brings the MAX+PLUS II development software to Sun Microsystems SPARCstations (see Figure 1). PLS-WS/SN includes Altera Hardware Description Language (AHDL) design entry, bidirectional EDIF netlist interface, Valid Logic and Viewlogic library

Figure 1. PLS-WS/SN Block Diagram *Shading indicates items provided with PLS-WS/SN.*



support, advanced logic synthesis, and design fitting in the Sun computer environment. Together, MAX+PLUS II and Valid Logic or Viewlogic software provide the tools to quickly and efficiently create, compile, and verify logic designs for Classic, MAX 5000, MAX 7000, and STG EPLDs.

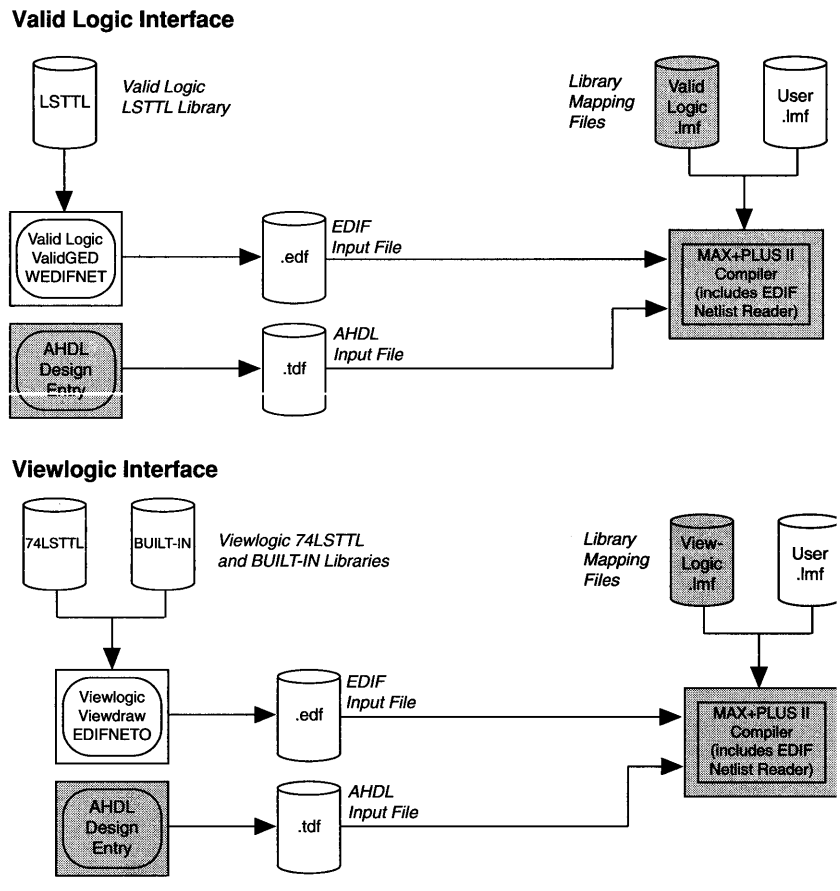
Design Entry

PLS-WS/SN supports both schematic and text design entry options. Hierarchical schematic designs are entered either with ValidGED by Valid Logic or with Viewdraw by Viewlogic (see Figure 2). Hierarchical Text Design Files (.tdf) are created in AHDL and can be used separately or mixed with schematic designs.

Valid Logic/EDIF

ValidGED schematics are converted into EDIF 2 0 0 netlist files with the Valid Logic WEDIFNET netlist writer. The MAX+PLUS II Compiler automatically processes these EDIF Input Files (.edf) when the design is

Figure 2. Design Entry with PLS-WS/SN



compiled. Symbols from the Valid Logic LSTTL library can be mapped to corresponding primitive and TTL functions in the MAX+PLUS II TTL MacroFunction Library with the Altera-provided Library Mapping File (.lmf) for Valid Logic users. Table 1 shows the primitive mappings and Table 3 shows the macrofunction mappings provided in this LMF.

Table 1. Valid Logic Library Mapping File—Primitives

Valid Logic Primitive Function	MAX+PLUS II Primitive Function
INV	EXP
LS00	NAND2
LS02	NOR2
LS04	NOT
LS08	AND2
LS10	NAND3
LS11	AND3
LS20	NAND4
LS21	AND4
LS27	NOR3
LS28	NOR2
LS30	NAND8
LS32	OR2
LS37	NAND2
LS40	NAND4
LS74	DFF2
LS86	XOR
LS126	TRI
LS386	XOR

Note: Contact Altera Applications for the most up-to-date list of mappings.

Viewlogic/EDIF

Viewdraw schematics are converted into EDIF 2 0 0 netlist files with Viewlogic's EDIFNETO netlist writer. The MAX+PLUS II Compiler automatically processes these EDIF Input Files (.edf) when the design is compiled. Symbols from the Viewlogic 74LSTTL and BUILT-IN libraries can be mapped to corresponding primitive and TTL functions in the MAX+PLUS II TTL MacroFunction Library with the Altera-provided LMF for Viewlogic users. Table 2 shows the primitive mappings and Table 3 shows the macrofunction mappings provided in this LMF.

Table 2. Viewlogic Library Mapping File—Primitives

Viewlogic BUILT-IN Function	MAX+PLUS II Primitive Function	
AND#	AND#	(#=2,3,4,8)
ANDNOR22	2A2NOR2	
BUF	SOFT	
DAND#	DAND#	(#=2,3,4,8)
DELAY	MCELL	
DOR#	DOR#	(#=2,3,4,8)
DXOR#	DXOR#	(#=2,3,4,8)
JKFFRE	JKFFRE	
MUX41	MUX41	
NAND#	NAND#	(#=2,3,4,8)
NOR#	NOR#	(#=2,3,4,8)
NOT	NOT	
OR#	OR#	(#=2,3,4,8)
TRIAND#	TAND#	(#=2,3,4,8)
TRIBUF	TRIBUF	
TRINAND#	TNAND#	(#=2,3,4,8)
TRINOR#	TNOR#	(#=2,3,4,8)
TRINOT	TRINOT	
TRIOR#	TOR#	(#=2,3,4,8)
UBDEC38	DEC38	
UDFDL	UDFDL	
UJKFF	UJKFF	
XNOR2	XNOR	
XNOR#	XNOR#	(#=3,4,8)
XOR2	XOR	
XOR#	XOR#	(#=3,4,8)

Note: Contact Altera Applications for the most up-to-date list of mappings.

Table 3. Valid Logic & Viewlogic Library Mapping Files—Macrofunctions (Part 1 of 3)

Valid Logic LSTTL Function	Viewlogic 74LSTTL Function	MAX+PLUS II TTL Macrofunction
LS00	74LS00	7400
LS02	74LS02	7402
LS04	74LS04	7404
LS08	74LS08	7408
LS10	74LS10	7410
LS11	74LS11	7411
LS20	74LS20	7420
LS21	74LS21	7421
LS27	74LS27	7427
LS28	74LS28	7428
LS30	74LS30	7430
LS32	74LS32	7432
LS37	74LS37	7437
LS40	74LS40	7440
LS42	74LS42	7442
LS51	74LS51	7451
LS54	74LS54	7454
LS55	74LS55	7455
LS73	74LS73A	7473
LS74	74LS74A	7474
LS75	74LS75	7475
LS76	74LS76A	7476
—	74LS77	7477
LS78	74LS78A	7478
LS83	74LS83A	7483
LS85	74LS85	7485
LS86	74LS86	7486
LS90	74LS90	7490
LS91	74LS91	7491
LS92	74LS92	7492
LS93	74LS93	7493
LS95	74LS95B	7495
LS96	74LS96	7496
LS107	74LS107A	74107
LS109	74LS109A	74109
LS112	74LS112A	74112
LS113	74LS113A	74113
LS114	74LS114A	74114
LS133	74LS133	74133
LS138	74LS138	74138
LS139	74LS139	74139

Table 3. Valid Logic & Viewlogic Library Mapping Files—Macrofunctions (Part 2 of 3)

Valid Logic LSTTL Function	Viewlogic 74LSTTL Function	MAX+PLUS II TTL Macrofunction
LS147	74LS147	74147
LS148	74LS148	74148
LS151	74LS151	74151
LS153	74LS153	74153
LS154	—	74154
—	74LS155A	74155
—	74LS156	74156
LS157	74LS157	74157
LS158	74LS158	74158
LS160	74LS160A	74160
LS161	74LS161A	74161
LS162	74LS162A	74162
LS163	74LS163A	74163
LS164	74LS164	74164
LS165	74LS165	74165
LS166	74LS166	74166
LS169	74LS169	74169
LS173	74LS173A	74173
LS174	74LS174	74174
LS175	74LS175	74175
LS181	74LS181	74181
LS183	74LS183	74183
LS190	74LS190	74190
LS191	74LS191	74191
LS192	74LS192	74192
LS193	74LS193	74193
LS194A	74LS194A	74194
LS195	74LS195A	74195
LS196	74LS196A	74196
LS197	74LS197	74197
LS240	74LS240	74240
LS241	74LS241	74241
LS244	74LS244	74244
LS251	74LS251	74251
LS253	74LS253	74253
LS257	74LS257	74257
LS258	74LS258	74258
LS259	74LS259	74259
LS260	74LS260	74260
LS261	—	74261
LS273	74LS273	74273

Table 3. Valid Logic & Viewlogic Library Mapping Files—Macrofunctions (Part 3 of 3)

Valid Logic LSTTL Function	Viewlogic 74LSTTL Function	MAX+PLUS II TTL Macrofunction
LS279	74LS279	74279
LS280	74LS280	74280
LS283	74LS283	74283
LS290	74LS290	74290
LS293	74LS293	74293
LS299	74LS299	74299
LS348	74LS348	74348
LS353	74LS353	74353
LS365	74LS365A	74365
LS366	74LS366A	74366
LS367	74LS367A	74367
LS368	74LS368A	74368
LS373	74LS373	74373
LS374	74LS374	74374
LS377	74LS377	74377
LS379	74LS379	74379
LS381	74LS381	74381
LS390	74LS390	74390
LS393	74LS393	74393

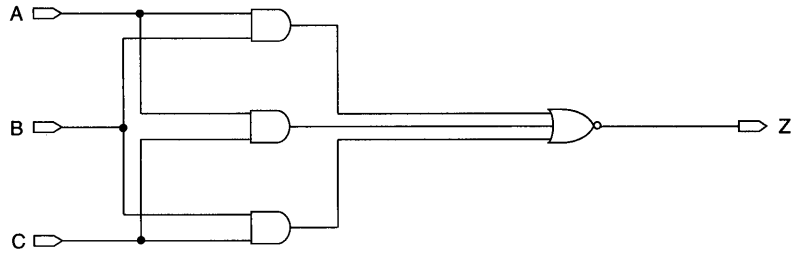
Note: Contact Altera Applications for the most up-to-date list of mappings.

Custom Library Mapping Files

Designers can add to the Altera-provided LMFs or create a new LMF. To create a new mapping between a Valid Logic or Viewlogic symbol and a MAX+PLUS II primitive or macrofunction, the designer follows the process shown in Figure 3. First, the designer selects a Valid Logic or Viewlogic function to map. If no equivalent function currently exists in the MAX+PLUS II TTL MacroFunction Library, the designer can create the function in a TDF. Finally, the designer maps the Valid Logic or Viewlogic function to the MAX+PLUS II function in an LMF.

Figure 3. Creating an LMF Mapping

Step 1: Select a Valid Logic or Viewlogic function for mapping.



Step 2: Design an equivalent circuit in AHDL if no equivalent circuit exists in the MAX+PLUS II TTL MacroFunction Library.

```
TITLE "ALTR_A05" ;
DESIGN IS "ALTR_A05" ;
SUBDESIGN ALTR_A05
(
   A_IN, B_IN, C_IN : INPUT ;
   Z_OUT : OUTPUT ;
)
VARIABLE
   X1, X2, X3 : NODE ;
BEGIN
   Z_OUT = !(X1 # X2 # X3) ;
   X1 = A_IN & B_IN ;
   X2 = A_IN & C_IN ;
   X3 = B_IN & C_IN ;
END ;
```

Step 3: Map the Valid Logic or Viewlogic function to the AHDL function in an LMF.

```
LIBRARY user_lib

% User Library Mapping File %

BEGIN
FUNCTION ALTR_A05 (A_IN, B_IN, C_IN)
RETURNS (Z_OUT)
FUNCTION "A05" ("A", "B", "C")
RETURNS ("Z")
END
```

AHDL

AHDL is a high-level, modular language used to create logic designs for Altera EPLDs. AHDL files can be created with any standard text editor.

AHDL supports state machines, truth tables, and Boolean equations, as well as arithmetic and relational operations. It is hierarchical, so that frequently used functions such as TTL and bus macrofunctions can be incorporated into a design. AHDL also supports complex arithmetic and

relational operations—such as addition, subtraction, equality, and magnitude comparisons—with the automatically generated logic functions. Standard Boolean functions, including AND, OR, NAND, NOR, XOR, and XNOR are also included. Groups are fully supported so operations can be performed on byte- or word-wide functions as well as on single variables. AHDL also allows the designer to specify the location of resources (e.g., latches, flip-flops, and pins) within Altera EPLDs. Together, these features make it easy to implement complex designs in a concise, high-level description (see Figure 4).

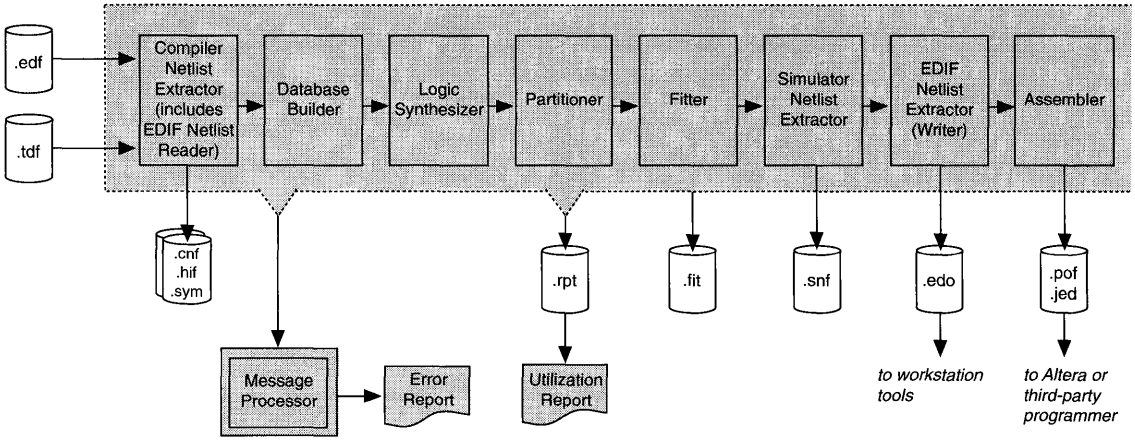
Figure 4. Sample AHDL File

```
TITLE "Timed Add and Compare function.";

DESIGN IS "add_cmp" DEVICE IS "EPM5128-2";

FUNCTION 74161 (LDN,A,B,C,D,ENT,ENP,CLRN,CLK)
RETURNS (QA,QB,QC,QD,RCO);

SUBDESIGN add_cmp (
                a[7..0],        % inputs for adder/comparator %
                b[7..0],
                cmpen,
                clock,reset     :INPUT;

                result[7..0],
                elapse[3..0],
                equal,
                less_than,
                grtr_than,
                done            :OUTPUT;
)
VARIABLE
        timer           : 74161; % timer is 74161 counter %
        register[7..0]  : DFF;   % register is an octal FF %
        flag            : NODE;
BEGIN
% set up accumulate register %
        result[] = register[];
        register[].clrn = reset;
        register[].clk = clock;
% this is the actual addition %
        register[] = a[] + b[];
% set flag high if register is not empty %
        flag = (register[] != 0);
        done = flag;
% connect inputs for timer (74161) %
        timer.enp = cmpen & flag;
        timer.clk = clock;
        timer.clrn = reset;
% elapse is the number of clock cycles it takes to do add %
        elapse[3..0] = (timer.QA,timer.QB,timer.QC,timer.QD);
% the comparator section %
        equal = ( a[] == b[]);
        less_than = (a[] < b[]);
        grtr_than = (a[] > b[]);
END;
```

Design Processing

The MAX+PLUS II Compiler processes designs for all Altera general-purpose EPLDs, including the Classic, MAX 5000, MAX 7000, and STG EPLDs (see Figure 5).

Figure 5. MAX+PLUS II Compiler



Compiler options simplify design processing and analysis. The user can specify up to two LMFs for the Compiler to use in processing EDIF Input Files (.edf), and can choose to create an EDIF Output File (.edo) for use with Valid Logic, Viewlogic, or other third-party simulation tools. Other options specify the degree of detail of the Report File (.rpt) that shows how EPLDs have been utilized and the target EPLD for the design.

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist used to define the design from the EDIF Input Files (.edf) and AHDL Text Design Files (.tdf). At this time, design rules are checked for any errors. If errors are found, they are displayed by the Message Processor. A successfully extracted design is built into a database and passed to the Logic Synthesizer.

The Logic Synthesizer module translates and optimizes the user-defined logic for the target architecture. The design is first minimized with SALSA (Speedy Altera Logic Simplification Algorithm), which removes any unused logic within the design. The Logic Synthesizer uses expert synthesis rules based on the target architecture (Classic, MAX 5000, MAX 7000, STG) to factor and map logic within the chosen EPLD structure. It then uses advanced synthesis algorithms that ensure the most efficient use of silicon resources.

For large system-level designs, the Partitioner is invoked. The Partitioner uses a sophisticated "Min-Cut" algorithm to separate the logic design into multiple EPLDs from the same family, relieving the designer of the time-consuming task of manually splitting a large design into smaller designs. The user can control the design's partitioning by entering specific chip assignments for flip-flops and pins in the source design files.

After partitioning, the Fitter applies heuristic rules to optimally place the synthesized design into one or more EPLDs. In devices with Programmable Interconnect Array (PIA) structures—i.e., larger MAX 5000 and MAX 7000 EPLDs—or with local/global bus structures such as the EP1810 EPLD, the Fitter also automatically routes signals across this interconnect to relieve the designer of tedious place-and-route tasks. The Report File (.rpt) issued by the Fitter shows design implementation as well as any unused resources in the EPLDs.

The Simulator Netlist Extractor optionally generates a Simulator Netlist File (.snf) that contains logic and timing information. This SNF is used by the EDIF Netlist Extractor to create EDIF Output Files.

The EDIF Netlist Extractor optionally writes an EDIF 2 0 0 netlist that contains all post-synthesis function and delay information for the completed design, so that it can be integrated into the workstation environment. An EDIF Output File (.edo) is created for each device used in the design. An Altera-provided or user-created Output Mapping File (.omf) can be used to map MAX+PLUS II functions to Valid Logic or Viewlogic functions in the EDIF Output File. (Detailed specifications and samples of Altera's EDIF output are available from Altera Applications.)

Finally, the Assembler module creates one or more Programmer Object Files (.pof) and/or JEDEC Files (.jed) from the compiled design. These files are used with standard Altera hardware to program the desired EPLDs. Third-party programming support is also available.

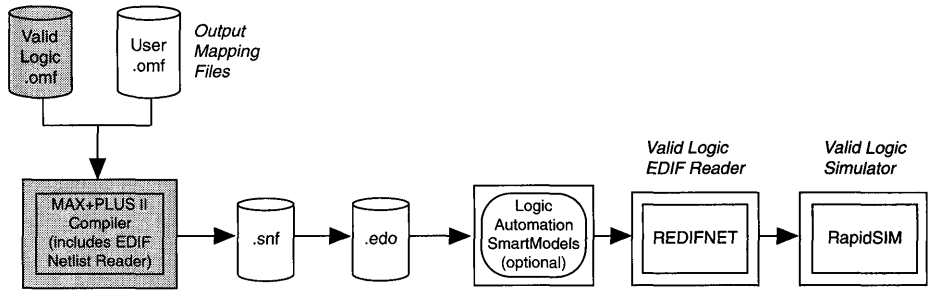
Simulation

Valid Logic users can convert the EDIF Output File (.edo) with the Valid Logic EDIF reader (REDIFNET) for chip- or board-level simulation with the Valid Logic RapidSIM simulator. Viewlogic users can convert the EDIF file with Viewlogic's EDIF reader (EDIFNETI) for chip- and board-level simulation in the Viewsim simulator. See Figure 6.

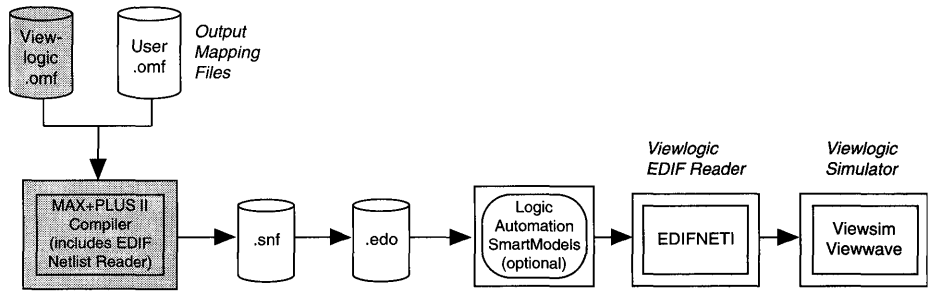
Valid Logic and Viewlogic users can also use the Logic Automation SmartModels for Classic and MAX 5000 EPLDs to directly convert the EDIF Output File (.edo) into a behavioral model for chip- or board-level simulation with RapidSIM or Viewsim.

Figure 6. Simulation with PLS-WS/SN

Valid Logic Interface



Viewlogic Interface



Device Programming

The POFs or JEDEC Files produced by the Compiler can be used with an Altera PC-based programmer or third-party programming hardware. (See the *PL-ASAP Data Sheet* in this data book for more information about the Altera Stand-Alone Programmer.)

Package Contents

- ❑ Quarter-inch cartridge tape (QIC-24, 9 track) containing all PLS-WS/SN programs and files:
  - MAX+PLUS II Compiler (includes Altera EDIF Netlist Reader and Writer)
  - MAX+PLUS II TTL MacroFunction Library
  - Library Mapping File for mapping Valid Logic functions to MAX+PLUS II functions
  - Library Mapping File for mapping Viewlogic functions to MAX+PLUS II functions
  - Output Mapping File for mapping MAX+PLUS II functions to Valid Logic functions
  - Output Mapping File for mapping MAX+PLUS II functions to Viewlogic functions
  - Sample files
- ❑ Documentation

Ordering Information

PLS-WS/SN (Sun SPARCstations)

Note: MAX+PLUS software that supports MAX 5000 EPLDs is available now. MAX+PLUS II software that supports Classic, MAX 5000, MAX 7000, and STG EPLDs will be available in December 1991.

System Requirements

- ❑ Sun Microsystems SPARCstation with 20 Mbytes of free disk space
- ❑ SunOS version 4.1 or higher operating system
- ❑ Quarter-inch cartridge (QIC-24, 9 track) 60-Mbyte tape drive

Valid Logic Users:

- ❑ Schematic capture/EDIF conversion software:
  - ValidGED (graphics editor) version 10.4 or higher
  - ValidCompiler (compiler) version 1.4 or higher
  - Valid WEDIFNET (EDIF netlist writer) version 1.1 or higher
- ❑ EDIF conversion/simulation software:
  - Valid REDIFNET (EDIF netlist reader) version 1.1 or higher
  - Valid RapidSIM version 1.1 or higher
  - Logic Automation SmartModels for Classic or MAX 5000 EPLDs (optional)

Viewlogic Users:

- ❑ Schematic capture/EDIF conversion software:
  - Viewlogic Viewdraw (graphics editor) version 3.25 or higher
  - Viewlogic EDIFNETO (EDIF netlist writer) version 4.0 or higher
- ❑ EDIF conversion/simulation software:
  - Viewlogic EDIFNETI (EDIF netlist reader) version 4.1 or higher
  - Viewlogic Viewsim version 4.0 or higher
  - Viewlogic Viewwave (optional) version 3.01 or higher
  - Logic Automation SmartModels for Classic or MAX 5000 EPLDs (optional)

Notes:

Software Utility Programs

ntroduction

Altera provides a variety of software utility programs that complement the MAX+PLUS II, MAX+PLUS, A+PLUS, SAM+PLUS, and MCMap development systems.

These programs are available via Altera's electronic bulletin board service (BBS) from the EAU (Electronic Application Utilities) directory. The BBS telephone number is (408) 249-1100; operation of the BBS is described in this data book and Altera software manuals. These utility programs can also be obtained by calling Altera Applications at 1 (800) 800-EPLD. Customers outside North America can obtain copies of these programs from their local Altera representative or distributor. All utility programs operate on an IBM PC-AT, and on IBM PS/2 Model 50 or higher, or compatible computers with DOS version 3.1 or higher.

PAL2EPLD

(EAU002) The PAL2EPLD utility converts 20-pin PAL designs into EP320 or EP330 designs. It directly converts PAL JEDEC Files into EP320/EP330 JEDEC Files.

310-to-320/30 Converter

(EAU003) The EP310-to-EP320/EP330 JEDEC File Converter automatically converts EP310 JEDEC Files to EP320/EP330-compatible JEDEC Files.

LogiCaps Plotter nterface

(EAU004) An Altera customer has written an interface program between LogiCaps and Houston Instruments plotters. This EAU provides information on how to obtain the interface program.

JEDPACK

(EAU005) The JEDPACK utility compacts the size of JEDEC Files, freeing up space on the computer's hard disk while retaining EPLD programming information. This utility is handy for archiving JEDEC Files generated by MAX+PLUS II, A+PLUS, SAM+PLUS, and MCMap.

Address Decoder

(EAU006) The DECODER utility automatically generates Boolean equations for address decoding applications. The program accepts a user-specified address bus width with upper and lower address bounds. It generates equations that can be placed into a MAX+PLUS/MAX+PLUS II-compatible Text Design File (.TDF) or an A+PLUS-compatible Altera Design File (.ADF).

JEDSUM

(EAU007) The JEDSUM utility calculates the EPROM data checksum, file transmission checksum, and number of programmed architecture bits in the JEDEC File for a Classic, SAM, or Micro Channel EPLD. The EPROM data checksum is often useful for documenting programming files.

AVEC

(EAU008) The AVEC utility adds functional test vectors to Classic EPLD JEDEC Files. AVEC translates the table output files generated by the A+PLUS Functional Simulator into JEDEC-standard test vectors. Third-party programmers (e.g., Data I/O 29B and UniSite 40 machines) have built-in hardware drivers that can apply these vectors to the programmed EPLD. Note, however, that Altera EPLDs are 100% generically tested before they leave the factory, so post-programming functional testing is not required.

BACKPIN

(EAU009) The BACKPIN utility extracts the pin assignments—assigned during design fitting—contained in an A+PLUS-generated JEDEC File and places them into the corresponding LogiCaps schematic drawing. If the Altera Design Processor (ADP) is set up to make pin assignments automatically, BACKPIN can then place the ADP's pin assignments back into the LogiCaps schematic drawing. The same pin assignments are then retained even if additional changes are made to the circuit design.

LEF2ABEL

(EAU012) The LEF2ABEL utility translates a Logic Equation File (.LEF) generated by the Altera Design Processor (ADP) to ABEL format. A+PLUS users may thus take advantage of the ADP's SALSA Minimizer to generate an optimized ABEL input file.

PAL2ADF

(EAU013) The PAL2ADF utility converts PALASM 1 or 2 files to the A+PLUS-, MAX+PLUS-, and MAX+PLUS II- compatible ADF input format.

LCA2ADF

(EAU016) The LCA2ADF utility converts LCA design files for XC2000- and XC3000-series devices into the A+PLUS-, MAX+PLUS-, and MAX+PLUS II- compatible ADF format. The target device may be a larger-size EPLD, such as the EP1810, EPM5064, EPM5128, EPM5130, or EPM5192.

LEF2AHDL

(EAU017) The LEF2AHDL utility converts an A+PLUS-generated Logic Equation File (.LEF) to a MAX+PLUS/MAX+PLUS II-compatible Text Design File (.TDF) in the Altera Hardware Description Language (AHDL).

PLD2EQN

(EAU018) The PLD2EQN utility converts JEDEC Files from a variety of 20- and 24- pin PAL and GAL devices (e.g., 16V8, 20V8, 22V10, 16L8, 16R8, 23S8) into the A+PLUS-compatible ADF and MAX+PLUS/MAX+PLUS II-compatible AHDL Text Design File (.TDF) formats. This utility allows users to combine multiple PALs and GALs into a single Altera EPLD.

ABEL2MAX

(EAU019) The ABEL2MAX utility converts ABEL version 4.0 design files (with the extension .TT2) into the MAX+PLUS/MAX+PLUS II-compatible Text Design File (.TDF) format.

PL-ASAP
Altera Stand-Alone Programmer

September 1991, ver. 2

Data Sheet

Features

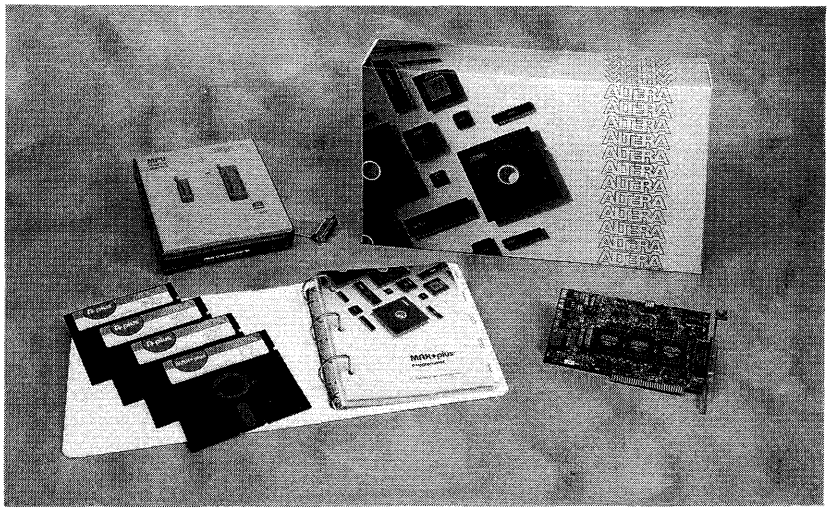
- ❑ Independent programming station
- ❑ Programming support for all Altera EPLDs
- ❑ Hardware extension to existing Altera systems
- ❑ Included in the price of PLDS-HPS, PLDS-MAX, PLCAD-SUPREME, PLDS-SAM, PLDS-ENCORE, and PLDS-MCMAP systems

General Description

The Altera Stand-Alone Programmer, PL-ASAP, provides the hardware and software needed for programming Altera EPLDs. PL-ASAP is designed for customers who wish to program Altera devices at a "programming station" separate from their design station, or who require a hardware extension to existing Altera systems. It includes only the materials required for EPLD programming; software tools for design entry, processing, and verification are sold separately.

PL-ASAP includes the software-controlled LP5 or LP6 Logic Programmer card. The LP6 interfaces with IBM PC-AT or compatible computers; the LP5 interfaces with IBM PS/2 Model 50, 60, 70, 80, or compatible computers.

The Master Programming Unit (MPU) programs Altera 20-pin EP310, EP320, and EP330 DIP devices directly; all other Altera EPLDs can be programmed with optional plug-in adapters. The Logic Programmer card generates all programming waveforms and voltages, so the MPU requires no additional power supply.



The MPU automatically tests for continuity between the device and programming socket before programming. In addition, the MPU can also be used with the MAX+PLUS II Waveform Editor for functional testing and verification of programmed EPLDs. Test vectors can be created with the Waveform Editor, applied to the EPLD, and the resulting EPLD outputs can be viewed within the Waveform Editor. However, functional testing is supported only with adapters with the prefix PLM-. (See the *PLED/J/G/S/Q & PLMD/J/G/S/Q Programming Adapters Data Sheet* in this data book for more information.)

Package Contents

- ❑ Software-controlled Logic Programmer interface card
- ❑ Master Programming Unit (MPU)
- ❑ Device programming software for all Altera EPLDs
- ❑ Documentation

Ordering Information

PL-ASAP	(IBM PC-AT or compatible)
PL-ASAP/PS	(IBM PS/2 Models 50, 60, 70, 80, or compatible)

PL-MPU

EPLD Master Programming Unit

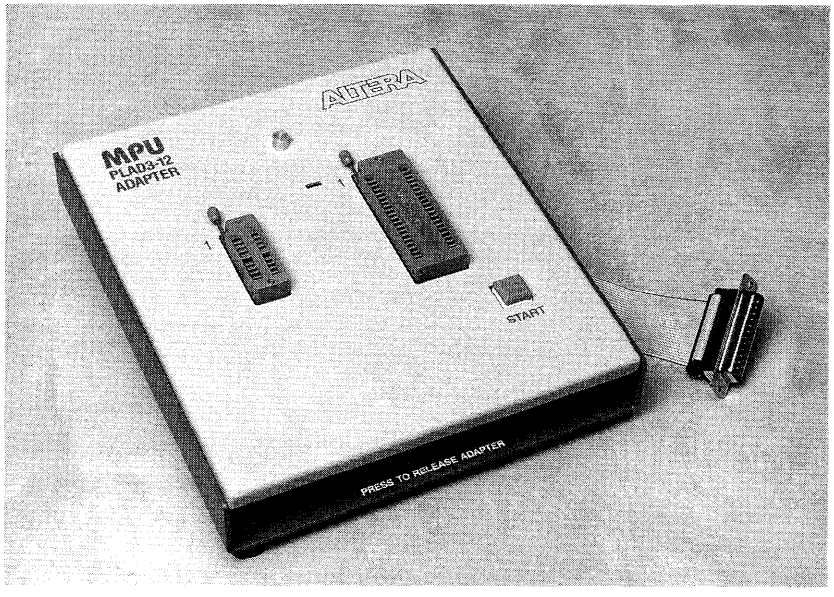
September 1991, ver. 1 **Data Sheet**

Features

- ❑ Master Programming Unit for all Altera EPLDs
- ❑ Direct programming of Altera EP310, EP320, and EP330 DIP EPLDs
- ❑ Support for all other Altera EPLDs via optional plug-in adapters
- ❑ Pin-to-socket continuity testing verifies proper EPLD contact with programmer socket
- ❑ Allows test vectors to be applied to programmed device for functional testing and verification
- ❑ START programming button makes programming successive EPLDs easy and efficient
- ❑ Indicator LED shows when unit is active
- ❑ Included in the price of PLDS-HPS, PLDS-ENCORE, PLDS-MAX, PLDS-SAM, PLCAD-SUPREME, PLDS-MCMAP, and PL-ASAP packages

General Description

The Altera Master Programming Unit (MPU) is a hardware module that programs all Altera EPLDs. The MPU directly supports the 20-pin EP310, EP320, and EP330 EPLDs (DIP packages only), and serves as the base unit for programming all other Altera EPLDs. Programming adapters that support each EPLD (DIP, J-lead, PGA, QFP, and SOIC packages) plug directly into the MPU.



9 Development Products

The MPU can test for continuity between the device and programming socket before programming. In addition, the MPU can also be used with the MAX+PLUS II Waveform Editor for functional testing and verification of programmed EPLDs. Test vectors can be created with the Waveform Editor, applied to the EPLD, and the resulting EPLD outputs can be viewed within the Waveform Editor. However, continuity and functional testing are supported only with adapters with the prefix PLM-. (See the *PLED/J/G/S/Q & PLMD/J/G/S/Q Programming Adapters Data Sheet* in this data book for more information.)

The MPU includes a 45-inch ribbon cable terminated with a 25-pin D-type connector that interfaces with an Altera Logic Programmer card. Programming or functional test information is transmitted from the programming card (installed in any full expansion slot of the computer) through the ribbon cable to the MPU. A programming indicator LED on the MPU lights up when the unit is active. The Logic Programmer card generates all programming waveforms and voltages, so the MPU requires no additional power supply.

Ordering Information

PL-MPU (IBM PC-AT, PS/2, or compatible)

PLED/J/G/S/Q & PLMD/J/G/S/Q

Programming Adapters

September 1991, ver. 1

Data Sheet

Features

- Programming adapters for Altera EPLDs
- Adapters plug directly into Master Programming Unit (MPU)
- Zero-insertion-force sockets for easy device insertion and extraction

General Description

The PLED, PLMD, PLEJ, PLMJ, PLEG, PLMG, PLES, PLMS, PLEQ, and PLMQ are socket adapters for programming Altera EPLDs that are not directly supported by the MPU. All adapters with the PLM- prefix allow functional test vectors to be applied to and read from EPLDs. Test vectors can be created with the MAX+PLUS II Waveform Editor and applied to the EPLD. The resulting EPLD outputs can be viewed in the Waveform Editor.

Each adapter contains a zero-insertion-force dual in-line package (DIP), J-lead (JLCC and PLCC), pin-grid array (PGA), small-outline IC (SOIC), or quad flat pack (WQFP and PQFP) socket. The adapters plug directly into the MPU, which supplies programming waveforms and voltages to the adapters. Table 1 gives a complete list of available adapters.

Ordering Information

Order by the adapter part number shown in Table 1.

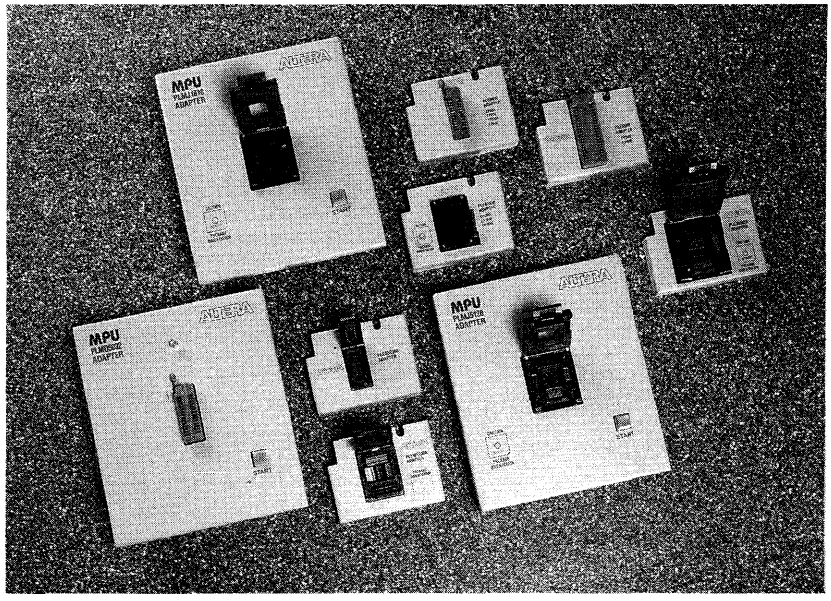


Table 1. EPLD Adapter Support

EPLD	Package	Part Number
EP330	J-Lead	PLEJ330
	SOIC	PLES330
EP600/610/610A/610T/630	DIP	PLED610
	J-lead	PLEJ610
	SOIC	PLES610
EP900/910/910A/910T	DIP	PLED910
	J-lead	PLEJ910
EP1800/1810/1810T/1830	J-lead	PLEJ1810
	J-lead	PLMJ1810 *(1)*
	PGA	PLEG1810
EPM5016	DIP	PLED5016
	J-lead	PLEJ5016
	SOIC	PLES5016
EPM5032	DIP	PLED5032
	DIP	PLMD5032 *(1)*
	J-lead	PLEJ5032
	SOIC	PLES5032
EPM5064	J-lead	PLEJ5064
EPM5128	J-lead	PLEJ5128
	J-lead	PLMJ5128 *(1)*
	PGA	PLEG5128
EPM5130	J-lead	PLEJ5130
	J-lead	PLMJ5130 *(1)*
	PGA	PLEG5130
	QFP	PLEQ5130
EPM5192	J-lead	PLEJ5192
	J-lead	PLMJ5192 *(1)*
	PGA	PLEG5192
EPS448	DIP	PLED448
	J-lead	PLEJ448
EPS464	J-lead	PLEJ464
	J-lead	PLMJ464 *(1)*
	QFP	PLEQ464
EPB2001	J-lead	PLEJ2001

Notes:
(1) Supports functional testing and continuity checking.

PLAESW-HPS, PLAESW-MAX PLAESW-SUP & PLAESW-WS

Extended Software Warranties

September 1991, ver. 1

Data Sheet

Features

- ❑ Software and documentation update service for registered owners of Altera's development systems
- ❑ Access to Altera Applications telephone support hotline
- ❑ Discounts on additional software options
- ❑ Design assistance from Altera Applications via the electronic bulletin board service (BBS)
- ❑ Access to Altera Electronic Application Utilities, Notes, and Briefs

General Description

PLAESW-HPS, PLAESW-MAX, PLAESW-SUP, and PLAESW-WS are software warranty and customer-support products that provide access to the latest EPLD development information. The Extended Software Warranty ensures that customers receive all new software and documentation when development software is upgraded to provide new features and to support new EPLDs. Customer-support services include a telephone hotline to Altera Applications Engineers for assistance with design work. A 24-hour electronic bulletin board and design upload service is available via modem. The Extended Software Warranty also guarantees discounts on future Altera development software purchases.

Ordering Information

PLAESW-HPS	(for PLDS-HPS, PLS-HPS, PLS-ES & PLS-OS)
PLAESW-MAX	(for PLDS-MAX & PLS-MAX)
PLAESW-SUP	(for PLCAD-SUPREME & PLS-SUPREME)
PLAESW-WS	(for PLS-WS/HP & PLS-WS/SN)

Notes:

Third-Party Development & Programming Support

September 1991, ver. 3

Data Sheet

Introduction

Altera recognizes the importance of third-party support tools and works closely with many third-party vendors to ensure high-quality support for EPLDs. Tables 1 through 4 provide an overview of third-party design entry tools, logic compilers, simulators, and device programmers. Current support (at the time of printing) is shown; contact Altera's Applications Department at 1 (800) 800-EPLD for the most up-to-date information.

Table 1. Third-Party Design Entry Tools

Company	Product	Design Entry Format	EPLDs Supported
Accel Technologies, Inc.	Tango-Schematic	Schematic	Classic *(1)*; MAX 5000 *(1)*
	Tango-PLD	Text	Classic
Cadence Design Systems, Inc.	Amadeus	Schematic	Classic; EPM5016, EPM5032
	PLD Solution	Text	Classic; EPM5016, EPM5032
Capilano Computing Systems Ltd.	MacABEL	Text	Classic; EPM5016, EPM5032
Data I/O Corp.	ABEL-4	Text	Classic; EPM5016, EPM5032
	FutureNet DASH	Schematic	Classic; EPM5016, EPM5032
Dazix	ACE	Schematic	MAX 5000*(1)*
ISDATA GmbH	LOG/iC	Text	Classic; EPM5016, EPM5032
Logical Devices, Inc.	CUPL	Text	Classic
	MacCUPL	Text	Classic
Mentor Graphics Corp.	NETED	Schematic	Classic *(1)*; MAX 5000 *(1)*
Minc Inc.	PLDesigner	Text	Classic
	PGADesigner	Text	MAX 5000 *(1)*
OrCAD Systems Corp.	SDT IV	Schematic	Classic; MAX 5000 *(1)*
	PLD	Text	Classic
Racal-Redac	Visula	Schematic	Classic; MAX 5000 *(1)*
Valid Logic Systems, Inc.	ValidGED	Schematic	Classic *(1)*; MAX 5000 *(1)*
	SystemPLD	Text	Classic
	SystemPGA	Text	MAX 5000 *(1)*
Viewlogic Systems, Inc.	Viewdraw	Schematic	Classic *(1)*; MAX 5000 *(1)*

Note:
(1) Information exchange occurs via EDIF 2 0 0 netlist format.

Table 2. Third-Party Logic Compilers

Company	Product	EPLDs Supported
Accel Technologies, Inc.	Tango-PLD	Classic
Cadence Design Systems, Inc.	PLD Solution	Classic; EPM5016, EPM5032
Capilano Computing Systems Ltd.	MacABEL	Classic; EPM5016, EPM5032 *(1)*
Data I/O Corp.	ABEL-4	Classic; EPM5016, EPM5032 *(1)*
ISDATA GmbH	LOG/iC	Classic; EPM5016, EPM5032
Logical Devices, Inc.	CUPL	Classic
	MacCUPL	Classic
Mentor Graphics Corp.	AutoLogic	Classic; MAX 5000
	PLDSynthesis	Classic
Minc Inc.	PLDesigner	Classic
	PGADesigner	MAX 5000 *(2)*
OrCAD Systems Corp.	PLD	Classic
Racal-Redac	System Expert	Classic *(2)*; MAX 5000 *(2)*
Synopsys, Inc.	Design Compiler	Classic *(2)* MAX 5000 *(2)*
Valid Logic Systems, Inc.	SystemPLD	Classic
	SystemPGA	MAX 5000 *(2)*

Notes:
(1) This compiler directly supports the EPM5016 and EPM5032 EPLDs. Multi-LAB devices (EPM5064, EPM5128, EPM5130, EPM5192) are supported by the ABEL-FPGA package and the Altera-supplied ABEL2MAX Converter.
(2) Information exchange occurs via EDIF 2 0 0 netlist format.

Table 3. Third-Party Logic Simulators

Company	Product	EPLDs Supported
Acugen Software, Inc.	ATGEN, AADELAY	Classic
(Test Vector Generation)	AAMAX	MAX 5000
Aldec, Inc.	Susie	Classic
Cadence Design Systems, Inc.	Verilog	Classic *(1), (2)*; MAX 5000 *(1), (2)*
Capilano Computing Systems Ltd.	MacABEL	Classic; EPM5016, EPM5032
Data I/O Corp.	ABEL-4	Classic; EPM5016, EPM5032
ISDATA GmbH	LOG/iC	Classic
Logic Automation Inc.	SmartModel	Classic; MAX 5000 *(2)*
Logical Devices, Inc.	CUPL	Classic
	MacCUPL	Classic
Mentor Graphics Corp.	QuickSim	MAX 5000 *(1), (2)*
Minc Inc.	PLDesigner	Classic
	PGADesigner	MAX 5000 *(2)*
OrCAD Systems Corp.	VST IV	Classic
Racal-Redac	CADAT	Classic
Valid Logic Systems, Inc.	RapidSim	Classic *(2)*; MAX 5000 *(2)*
Viewlogic Systems, Inc.	Viewsim	Classic *(2)*; MAX 5000 *(2)*

Notes:
(1) Supported by Logic Automation SmartModels.
(2) Information exchange occurs via EDIF 2 0 0 netlist format.

Table 4. Third-Party Programming Hardware

Company	Product	EPLDs Supported
Advin Systems Inc.	PILOT	Classic
American Advantech Corp.	PC-UPROG	Classic
BP Microsystems, Inc.	CP-1128 PLD-1128	Classic
BYTEK Corp.	MULTIPROGRAMMER	Classic
Data I/O Corp.	29B/LogicPak	Classic
	2900	Classic; MAX 5000
	60 A/H	Classic
	UniSite 40	Classic; MAX 5000; SAM, STG
Digelec, Inc.	UP-803	Classic
	DigiPack	Classic
Logical Devices, Inc.	ALLPRO	Classic
Japan Macnics Corp.	PROMAC P3	Classic
SMS GmbH	SPRINT Expert	Classic; MAX 5000
Stag Microsystems Ltd.	ZL30, ZL30A	Classic
	PPZ	Classic
	SYSTEM3000	MAX 5000
Sunrise Electronics, Inc.	T-10	Classic

Note:
The companies listed above as well as several other manufacturers are continually developing support for Classic, MAX 5000, MAX 7000, and STG EPLDs. Altera strongly recommends that you contact specific manufacturers to determine the most current support status.

Third-Party Vendors

Table 5 lists telephone numbers for third-party vendors. Altera strongly recommends direct contact with manufacturers for specific details or product features and availability. Altera can accept no responsibility for the suitability or accuracy of third-party development software or programming hardware.

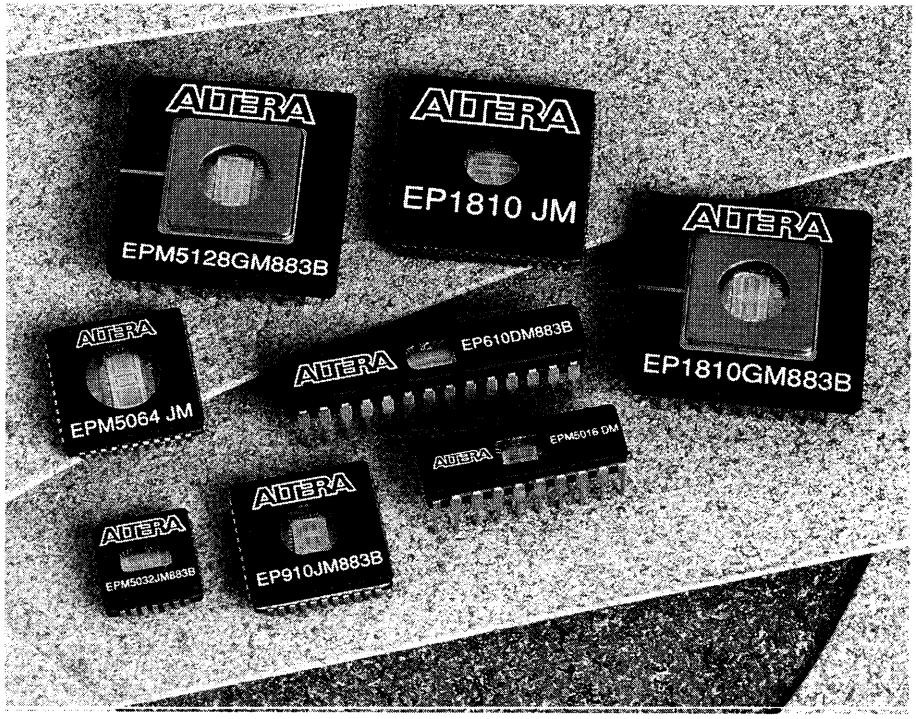
Table 5. Manufacturers of Third-Party Tools

Company	Telephone Number
Accel Technologies, Inc.	(619) 554-1000
Acugen Software, Inc.	(603) 891-1995
Advin Systems Inc.	(408) 243-7000
Aldec, Inc.	(805) 499-6867
American Advantech Corp.	(408) 293-6786
BP Microsystems, Inc.	(713) 461-9430
BYTEK Corp.	(407) 994-3520
Cadence Design Systems, Inc.	(408) 943-1234
Capilano Computing Systems Ltd.	(604) 669-6343
Data I/O Corp.	(800) 247-5700
Digelec, Inc.	(818) 701-9677
ISDATA GmbH	Germany (49) 7 21/69 30 92
Logic Automation Inc.	(503) 690-6900
Logical Devices, Inc.	(800) 331-7766
OrCAD Systems Corp.	(503) 690-9881
Mentor Graphics Corp.	(503) 626-7000
Minc Inc.	(719) 590-1155
Japan Macnics Corp.	Japan (81) 45 939 6150
Quadtree Software Corp.	(213) 597-5995
Racal-Redac	(201) 848-8000
SMS GmbH	Germany (49) 7522 5018
Stag Microsystems Ltd.	(408) 988-1118
Sunrise Electronics, Inc.	(818) 914-1926
Valid Logic Systems, Inc.	(408) 432-9400
Viewlogic Systems, Inc.	(800) 422-4660

Contents

September 1991

Section 10 **Military Products**


ALTERA
EPM5128GM883B
ALTERA
EP1810 JM
ALTERA
EP1810GM883B
ALTERA
EPM5064 JM
ALTERA
EP610DM883B
ALTERA
EPM5016 DM
ALTERA
EPM5032JM883B
ALTERA
EP910JM883B

September 1991, ver. 2 Data Sheet

ntroduction

Tables 1 through 7 provide information on military-temperature-range, MIL-STD-883B-qualified, and DESC EPLDs. For detailed information, refer to individual data sheets in this data book, or call Altera Marketing at (408) 984-2800.

MIL-STD-883-compliant product specifications are provided in military product drawings (MPDs) that are available on request from Altera Marketing. An MPD is prepared in accordance with the appropriate military specification format and should be used for preparing Source Control Drawings (SCDs). Refer to *Source Control Drawings* in this data book for a description of SCD generation.

Table 1. Classic Military-Temperature-Range EPLDs

EPLD	Package *(1)*	t_{PD1} (ns)
EP320	D	45
EP610	D, J	35
EP910	D, J	40
EP1810	J, G	45

Table 2. MAX 5000 Military-Temperature-Range EPLDs

EPLD *(2)*	Package *(1)*	t_{PD1} (ns)
EPM5032	D, J	25
EPM5064	J	35
EPM5128	J, G	35
EPM5130	G	35
EPM5192	J, G	35

Notes to tables 1, 2, 3, 4, 5, 6, and 7 are listed on page 375.

Table 3. SAM Military-Temperature-Range EPLDs

EPLD	Package (1)	f_{MAX}
EPS448	D, J	20 MHz

Table 4. Classic MIL-STD-883B-Qualified EPLDs

EPLD	Package (1)	t_{PD1} (ns)	Altera Military Drawing
EP310DM883B	D	50	02D-00179
EP320DM883B	D	45	02D-00209
EP600DM883B	D	55	02D-00194
EP600JM883BX	J	55	02D-00194
EP610DM883B	D	35	02D-00522
EP610JM883BX	J	35	02D-00522
EP900DM883B	D	60	02D-00521
EP900JM883B	J	60	02D-00521
EP910DM883B	D	40	02D-00935
EP910JM883B	J	40	02D-00935
EP1800GM883B	G	75	02D-00509
EP1800JM883B	J	75	02D-00509
EP1810GM883B	G	45	02D-00782
EP1810JM883B	J	45	02D-00782

Table 5. MAX 5000 MIL-STD-883B-Qualified EPLDs

EPLD	Package (1)	t_{PD1} (ns)	Altera Military Drawing
EPM5032DM883B	D	25	02D-00828
EPM5032JM883B	J	25	02D-00828
EPM5128GM883B	G	35	02D-01015
EPM5128JM883B	J	35	02D-01015

Notes to tables 1, 2, 3, 4, 5, 6, and 7 are listed on page 375.

Table 6. Classic DESC EPLDs

EPLD	Package *(1)*	t_{PD1} (ns)	DESC Order Number
EP310DM883B	D	50	8863501RA
EP600DM883B	D	55	8686401LA
EP600JM883BX	J	55	8686401XX
EP610DM883B	D	35	8947601LX
EP610JM883BX	J	35	8947601XX
EP900DM883B	D	60	8854801QA
EP900JM883B	J	60	8854801XX
EP1800GM883B	G	75	8854902YC
EP1810GM883B	G	45	8946901YC
EP1810JM883B	J	45	8946901XX

Table 7. MAX 5000 DESC EPLDs

EPLD	Package *(1)*	t_{PD1} (ns)	DESC Order Number
EPM5032DM883B	D	25	90611XXLA
EPM5032JM883B	J	25	90611XXXA
EPM5128GM883B	G	35	89468XXYC
EPM5128JM883B	J	35	89468XXXA

Note to Tables 1, 2, 3, 4, 5, 6 & 7:

(1) Package configurations:
D: Windowed ceramic dual in-line package (CerDIP)
J: Windowed ceramic J-lead chip carrier (JLCC)
G: Windowed ceramic pin-grid array (PGA)

(2) These MAX 5000 EPLDs are still being qualified. Contact Altera Marketing for current information.

Notes:

Source Control Drawings
for Military-Qualified EPLDs

September 1991, ver. 2

Data Sheet

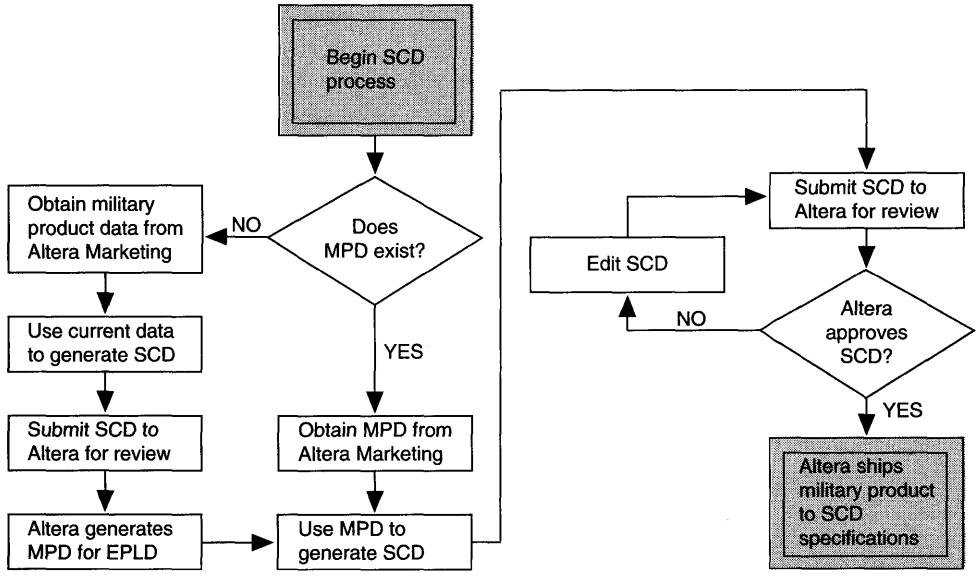
General Description

Source Control Drawings (SCDs) are documents created by military subcontractors for documentation control. An SCD can be generated for commercial EPLDs that are or will be qualified for MIL-STD-883B.

An SCD should be based on a Military Product Drawing (MPD) provided by Altera. When an MPD is not available, the user should contact Altera's Marketing Department for current data. An SCD generated from information in Altera's commercial data book is not acceptable. Altera's MPDs contain information on the scope, reference documents, MIL-STD-883B requirements, quality assurance provisions, and preparation of delivery for EPLDs. Characteristics of device screening—such as burn-in testing, AC/DC electrical properties, timing waveforms, and package dimensions—are also detailed in MPDs. These specifications may differ from those for Altera's commercial EPLDs. Altera will not approve an SCD from a military subcontractor until the described MPD requirements are met.

Figure 1 shows the process flow for generating an SCD for Altera's military products.

Figure 1. Generation of a Source Control Drawing



Notes:

Total-Dose Radiation Hardness of Altera EPLDs

September 1991, ver. 3

Application Brief 51

ntroduction

Altera has measured the EPROM process in a series of tests, for both Classic and MAX 5000 EPLDs. This application brief summarizes the results of these tests.

Classic EPLDs

Tests for the Classic EPLDs were performed under the following conditions:

- Tested in conformance with Method 1019.2 of MIL-STD-883C
- Radiation hardness to 14 krad (Si) under worst-case conditions

For the Classic EPLDs, the EP600DM was used for evaluation. Based on the failure mechanisms determined by the tests, results for this product are expected to be typical of all Altera Classic EPLDs.

The EP600 functions properly at the worst-case military power-supply range (V_{CC} = 5.5 V) until total doses in excess of 10 krad (Si) are reached. Conditions that are not worst-case provide total-dose tolerance far in excess of 10 krad (Si).

The experiments were conducted with a Cobalt-60 isotope source with a dose rate of 750 krad (Si) per minute (±10%). Test units were powered up with V_{CC} = 5.0 V and all other pins connected to ground, both during and after the irradiation, until measurements were made. All conditions of temperature control, dose rate, and electrical bias conformed to Method 1019.2 of MIL-STD-883C.

Numerous key parameters were measured. The margin of programmed EPROM cells, as indicated by the maximum V_{CC} value for error-free verification and functional operation of the part, proved to be the most important. The following five parameters were monitored:

- Programmed cell margin (from V_{CC} maximum)
- Erased cell margin (from V_{CC} minimum)
- AC timing (from t_{PD})
- I_{CC} standby vs. input voltage level
- Output-high and output-low drive currents

These measurements made it possible to monitor the extent of EPROM-cell programming, and to detect changes in junction leakage and transistor threshold voltage.

Degradation of programmed EPROM cell margins was the first cause of failure in all experiments. The rate of this degradation—and thus the total-dose radiation tolerance—was observed to be a strong function of irradiation. If the control (top) gate was biased at V_{CC} during the irradiation, the tendency for the cell to lose charge was greatly reduced. In this case, total-dose radiation tolerance observed was greater than 30 krad (Si) for 5.5 V operation, and greater than 40 krad (Si) for 5.0 V operation. If, on the other hand, the control gate was grounded during the irradiation, the total-dose radiation tolerance was reduced to about 14 krad (Si) for 5.5 V operation, and to about 18 krad (Si) for 5.0 V operation. This behavior suggests that energetic holes created in the bulk silicon by the radiation and attracted toward the floating gate by its negative (programmed) charge are the dominant cause of cell charge loss.

When the control gate of these EPROM cells is grounded during irradiation, the worst-case result of about 14 krad (Si) for 5.5 V operation is the best estimate of the radiation tolerance of these products. Most radiation-tolerance experiments on EPROM technologies include control gates that are biased at V_{CC} during at least part of the irradiation.

MAX 5000 EPLDs

Tests for the MAX 5000 EPLDs were performed at radiation hardness to 6.5 krad (Si) under worst-case V_{CC}.

For the MAX 5000 EPLDs, the EPM5032DC was used for evaluation. The tests were conducted with a Cobalt-60 isotope source with a dose rate of 117 rad (SI)/s. All irradiation was performed at room temperature (25° C, ±3°), while device-under-test (DUT) V_{CC} was set to 5.5 V. Nine input pins were pulled to V_{CC} through 1-kΩ resistors and three were tied directly to GND. All output pins were pulled up to V_{CC} through 1-kΩ resistors, while the reserved I/O pins were left open. These specifications provided a realistic control-gate bias distribution for a typical design.

Total-dose-induced functional failure thresholds are highly sensitive to measurement voltage. Under the worst-case military power-supply range (V_{CC} = 5.5 V), the EPM5032 test devices function properly until total doses in excess of 6.5 krad (Si) are reached. For V_{CC} = 5.0 V, proper functioning occurs above 13.0 krad (Si) and 17.5 krad (Si) for V_{CC} = 4.5 V.

Timing parameters were measured using V_{CC} = 5.0 V. No significant change in maximum operating speed or propagation-delay times occurred at levels as high as 10 krad (Si).

Conclusion

The differences in the test results between the EP600 and EPM5032 EPLDs indicate that actual device types used in a final design should be separately evaluated to verify total-dose effects. The evaluation should include a complete functional test at the expected operating supply-voltage extremes as well as extensive parametric measurements. More complex devices may

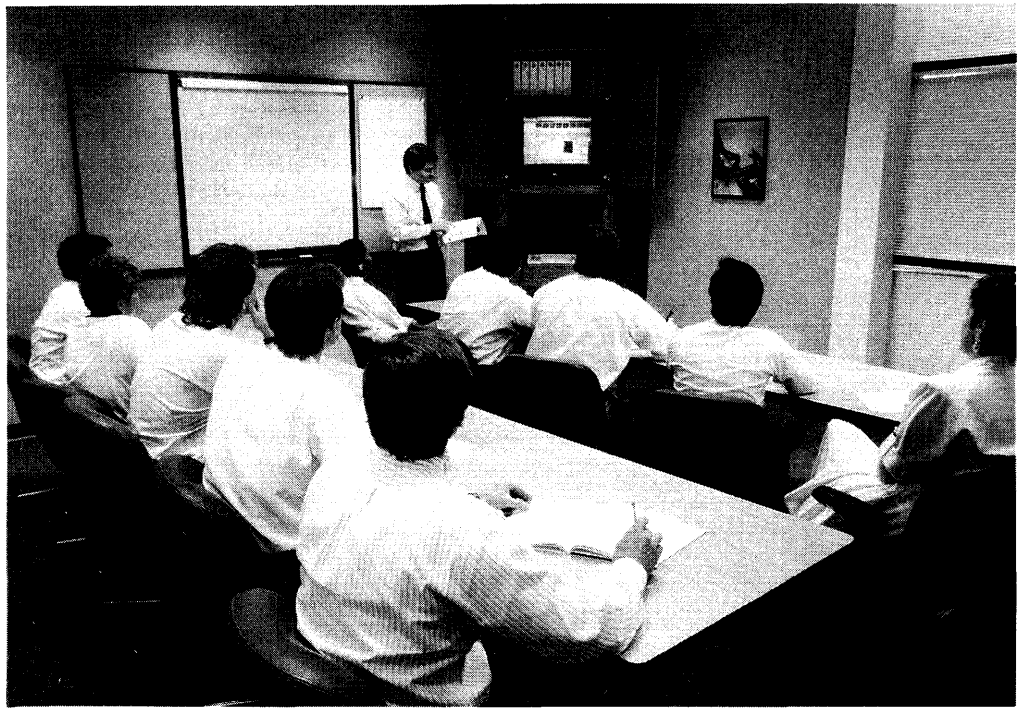
show greater increase in response to irradiation if additional features that have not been checked in these test devices—such as the Programmable Interconnect Array (PIA)—are included.

Programmed cell margin fell linearly with increasing total radiation dose. Therefore, to maximize radiation hardness, it is important to program an adequate cell margin into the EPLD before irradiation. Designers are advised to use Altera-approved programming systems that provide optimized cell programming.

Notes:

September 1991

ection 11 General Information



Electronic Bulletin Board Service

September 1991, ver. 2

ntroduction

Altera provides an electronic bulletin board service (BBS) for continuous access to up-to-date EPLD and development tool information, electronic application notes and briefs, data sheet updates, customer newsletters, and useful utility programs. The BBS also supports file transfers to and from the Altera Applications Engineering Department. Owners of A+PLUS, MAX+PLUS, and MAX+PLUS II software can refer to their user manuals for detailed information on using the BBS.

Modem Number:
(408) 249-1100

The telephone number for the BBS is (408) 249-1100. To connect to the BBS via modem, the following equipment and configuration are required:

- ❑ 1200 or 2400 baud rate
- ❑ Bell Standard 212A or compatible modem
- ❑ Data format: 8 data bits, 1 stop bit, no parity

The following file transfer protocols are supported:

- ❑ Xmodem (Checksum)
- ❑ Xmodem-CRC (CRC)
- ❑ Ymodem (1K-Xmodem)
- ❑ Ymodem-G (1K-Xmodem-G)
- ❑ ASCII (Non-Binary)
- ❑ Kermit

-ogging On

After the BBS connection has been established, the user can choose between graphic (for EGA or VGA displays) or non-graphic display mode. The user is then prompted for his or her name; a new user can also choose a password. Each name and password are recorded for future log-ons.

A series of screens appears automatically: the Altera News screen, the Personal Mail screen, and the Settings screen. The Main Menu, from which all functions are accessed, appears next. The most commonly used functions are: **F)ile Directories, U)pload a File**, and **D)ownload a File**. On-line help is available with the **H)elp Functions** command. The **F)ile Directories** command displays a list of directories containing files that can be downloaded. (Uploaded files are stored in a private directory.)

⁼ile Jploading

The File Upload service is available for uploading files that require analysis or correction by an Altera Applications Engineer. All files that are uploaded to the Altera BBS are automatically stored in a private directory. When a file is uploaded, the file description should include the name of the Altera Applications Engineer who has been asked to examine the file.

File Downloading

Files can be copied from the following six directories:

1. From-Altera File Directory

This directory is a general directory for downloading files from Altera Applications, for example, after a problem or question has been analyzed

2. Electronic Application Briefs

This directory contains Electronic Application Briefs (EABs) and Notes (EANs), which provide up-to-date information on using Altera EPLDs effectively.

3. Electronic Application Utilities

This directory contains Electronic Application Utilities (EAUs) that complement Altera software and aid EPLD design. Three commonly used utilities are described below. All available utilities are described in *Application Brief 73 (Software Utility Programs)* in this data book.

PLD2EQN The PLD2EQN utility converts common PAL/GAL/PLA JEDEC Files to Altera Hardware Description Language (AHDL) files that are compatible with the MAX+PLUS and MAX+PLUS II software. This utility can also produce an Altera Design File (ADF) that is compatible with A+PLUS software.

JEDSUM The JEDSUM utility calculates the EPROM data checksum, file transmission checksum, and the number of programmed architecture bits contained in an EPLD JEDEC File.

ABEL2MAX The ABEL2MAX utility converts .TT2 files generated by Data I/O's ABEL software (version 4.0 or higher) into Altera Hardware Description Language (AHDL) files that are compatible with the MAX+PLUS and MAX+PLUS II software.

4. Altera Customer Newsletters

This directory contains Altera newsletters that provide current news on EPLDs and development tools, and a Question & Answer forum that answers many common questions asked by Altera customers.

5 & 6. A+PLUS and MAX+PLUS Macrofunction Exchange Libraries

These directories are used to publicly exchange A+PLUS, MAX+PLUS and MAX+PLUS II macrofunctions. Customers can download any macrofunctions in this directory. Macrofunctions that have been uploaded to be shared with other users are also placed here by the system operator ("Sysop").

Ordering Information

September 1991, ver. 4

Ordering EPLDs

Figure 1 shows how an EPLD part number is constructed. For information on specific package, grade, and speed combinations, refer to individual EPLD data sheets or the *Product Selection Guide* in this data book, or telephone the Altera Marketing Department at (408) 984-2800.

MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs) that are available on request from Altera Marketing. These MPDs should be used for the preparation of Source Control Drawings (SCDs).

Figure 1. EPLD Package Ordering Codes

EP 910 L C -30 T

amily Signature:
P: General-purpose Classic EPLD
PM: MAX 5000 & MAX 7000 EPLD
PS: STG & SAM EPLD
PB: Micro Channel EPLD

evice Type:
P: 310, 320, 330, 600, 610, 610A, 630, 900, 910, 910A, 1800, 1810, 1830
PM: 5016, 5032, 5064, 5128, 5130, 5192
PS: 448, 464
PB: 2001, 2002A

ackage Type:
: Windowed ceramic dual in-line package (CerDIP)
: One-time-programmable plastic dual in-line package (PDIP)
: Windowed ceramic J-lead chip carrier (JLCC)
: One-time-programmable plastic J-lead chip carrier (PLCC)
i: Windowed ceramic pin-grid array (PGA)
: One-time-programmable plastic small-outline integrated circuit (SOIC)
/: Windowed ceramic quad flat pack (WQFP)
: One-time-programmable plastic quad flat pack (PQFP)

Turbo:
(Optional) Turbo Bit has been preset at the factory. This option is only available for plastic EPLDs.

Speed Grade:
See the *Product Selection Guide* or individual EPLD data sheets in this data book for speed/product relationships (e.g., -15, -20, or blank).

Operating Temperature/Military Processing:
C: Commercial temperature (0° C to 70° C)
I: Industrial temperature (–40° C to 85° C)
M: Military temperature (–55° C to 125° C). This temperature range applies to all military EPLDs, i.e., all EPLDs with a code that contains the letter M.
M883B: Processed to MIL-STD-883, current revision
M883BX: Processed to MIL-STD-883, current revision with modified J-lead package dimension
MB: Fully compliant with deviation to MIL-STD-883, current revision (consult Altera on specific deviations)
M5962: DESC Standard Military Drawing (SMD)

Examples:

EP610PC-25T	EP610 in a plastic dual in-line package, commercial temperature range, -25 speed grade (t_{PD1} = 25 ns), turbo-only operation.
EP1810GI-45	EP1810 in a windowed ceramic pin-grid array package, industrial temperature range, -45 speed grade (t_{PD1} = 45 ns).
EPM5032DM883B	EPM5032 in a windowed ceramic dual in-line package, MIL-STD-883B-qualified.
EPS448LC-25	EPS448 in a plastic J-lead chip carrier package, commercial temperature range, -25 speed grade (f_{MAX} = 25 MHz).

Ordering Software & Hardware

This section provides the ordering codes for Altera development system and software, programming hardware, and adapters. Refer to individua data sheets in this data book for detailed information on software anc hardware products.

Development Systems & Software

Table 1 lists the ordering codes for the basic development system anc software configurations.

Table 1. Altera Development Systems & Software

Platform:	Ordering Code:	Software Packages: MAX+PLUS II	MAX+PLUS	A+PLUS	SAM+PLUS	MCMAP	Altera EPLDs Supported: MAX 7000	MAX 5000	Classic	STG	SAM	Micro Channel	EDIF Interface	Programming Hardware (1)
PC/Windows 3.0	PLDS-HPS	✔					✔	✔	✔	✔			✔	✔
	PLS-HPS	✔					✔	✔	✔	✔			✔	
	PLS-OS	✔					✔	✔	✔	✔			✔	
	PLS-ES	✔						(2)	✔					
PC/DOS	PLDS-ENCORE		✔	✔	✔			✔	✔		✔			✔
	PLDS-MAX		✔					✔						✔
	PLS-MAX		✔					✔						
	PLCAD-SUPREME			✔					✔					✔
	PLS-SUPREME			✔					✔					
	PLDS-SAM				✔						✔			✔
	PLS-SAM				✔						✔			
	PLDS-MCMAP					✔						✔		✔
	PLS-MCKIT					✔						✔		
	PLS-EDIF							✔					✔	
Workstation	PLS-WS/HP	✔					✔	✔	✔	✔			✔	
	PLS-WS/SN	✔					✔	✔	✔	✔			✔	

Notes:

(1) Development systems are available with programming hardware that supports IBM PS/2 and compatible computer Simply add "/PS" to the end of the product designation (e.g., PLDS-HPS/PS).

(2) PLS-ES supports only the following MAX 5000 EPLDs: EPM5016 and EPM5032.

Software Warranty

The renewable, one-year software warranty agreements for development products provides software and documentation updates for all registered owners of Altera development systems. The software warranty should be ordered with one of the following codes:

- ❑ PLAESW-HPS (for PLDS-HPS, PLS-HPS, PLS-OS & PLS-ES)
- ❑ PLAESW-MAX (for PLDS-MAX & PLS-MAX)
- ❑ PLAESW-SUP (for PLCAD-SUPREME & PLS-SUPREME)
- ❑ PLAESW-WS (for PLS-WS/HP & PLS-WS/SN)

Programming Hardware & Adapters

The LP6 Logic Programmer card interfaces with IBM PC-AT (or compatible) computers. It should be ordered by the following code:

- ❑ PLP6

The Master Programming Unit (MPU) can directly program EP320 and EP330 DIP EPLDs; adapters are required to program all other EPLDs. The MPU should be ordered by the following code:

- ❑ PL-MPU

PL-ASAP includes programming software, a Logic Programmer card, and the MPU. It should be ordered by the following code (to order a package with programming hardware that supports IBM PS/2 and compatible computers, simply add "/PS" to the end of the ordering code):

- ❑ PL-ASAP

Table 2 lists the part numbers for programming adapters.

Table 2. EPLD Adapter Support

EPLD	Package	Part Number *(1)*
EP330	J-Lead	PLEJ330
	SOIC	PLES330
EP600/610/610A/610T/630	DIP	PLED610
	J-lead	PLEJ610
	SOIC	PLES610
EP900/910/910A/910T	DIP	PLED910
	J-lead	PLEJ910
EP1800/1810/1810T/1830	J-lead	PLEJ1810
	J-lead	PLMJ1810 *(2)*
	PGA	PLEG1810
EPM5016	DIP	PLED5016
	J-lead	PLEJ5016
	SOIC	PLES5016
EPM5032	DIP	PLED5032
	DIP	PLMD5032 *(2)*
	J-lead	PLEJ5032
	SOIC	PLES5032
EPM5064	J-lead	PLEJ5064
EPM5128	J-lead	PLEJ5128
	J-lead	PLMJ5128 *(2)*
	PGA	PLEG5128
EPM5130	J-lead	PLEJ5130
	J-lead	PLMJ5130 *(2)*
	PGA	PLEG5130
	QFP	PLEQ5130
EPM5192	J-lead	PLEJ5192
	J-lead	PLMJ5192 *(2)*
	PGA	PLEG5192
EPS448	DIP	PLED448
	J-lead	PLEJ448
EPS464	J-lead	PLEJ464
	J-lead	PLMJ464 *(2)*
	QFP	PLEQ464
EPB2001	J-lead	PLEJ2001

Notes:
(1) Refer to the *PLED/J/S/Q & PLMD/J/S/Q Data Sheet* for more information.
(2) Supports functional testing and continuity checking.

EPLD Package Outlines

September 1991, ver. 2

Data Sheet

ntroduction

This data sheet provides package outlines for all Altera EPLDs. Table 1 shows the type of packages, lead materials, and lead finishes available.

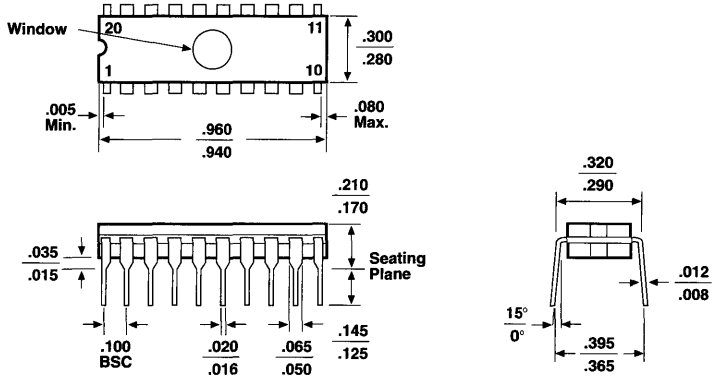
Table 1. EPLD Packages

Package Type	Package Code	Lead Material	Lead Finish
Ceramic dual in-line	D	Alloy 42	Solder dip over tin flash (Military) Matte tin plate
Plastic dual in-line	P	Copper	Solder dip (60/40)
Ceramic J-lead	J	Alloy 42	Solder dip (60/40)
Plastic J-lead	L	Copper	Solder plate (60/40)
Ceramic pin-grid array	G	Alloy 42	Gold over nickel plate
Plastic small-outline IC	S	Copper	Solder plate (60/40)
Ceramic quad flat pack	W	Alloy 42	Matte tin plate
Plastic quad flat pack	Q	Copper	Solder plate (60/40)

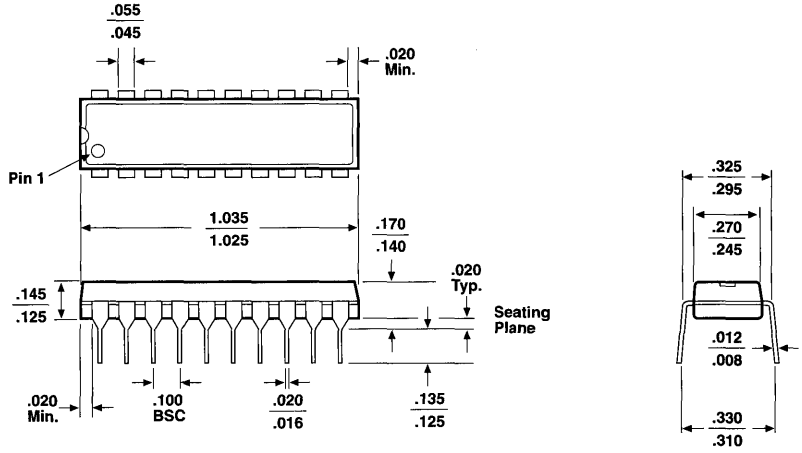
Package outlines are listed here in ascending size order. The dimensions shown are nominal with a tolerance of 0.020 in (0.51 mm) unless otherwise indicated. Maximum lead coplanarity is 0.004 in. (0.10 mm).

20-Pin Ceramic Dual In-Line Package (CerDIP)

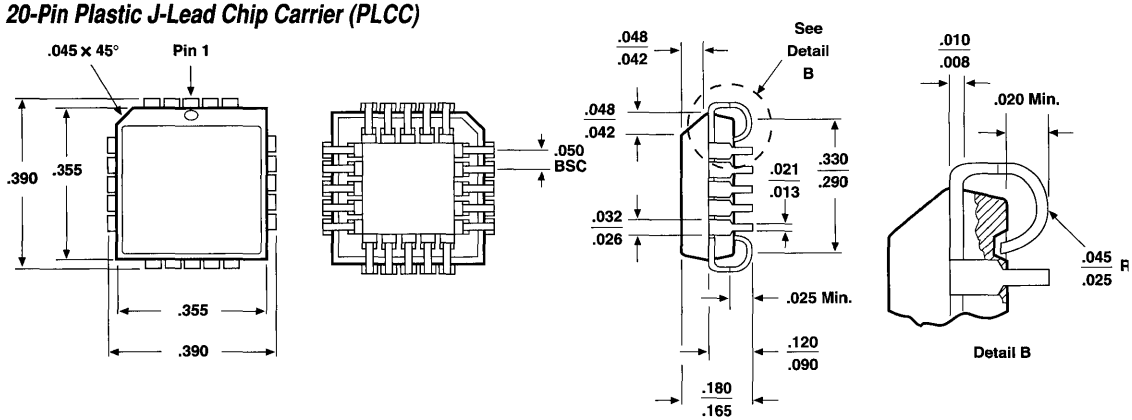
For military-qualified product, see case outline D-8 in Appendix C of MIL-M-38510.



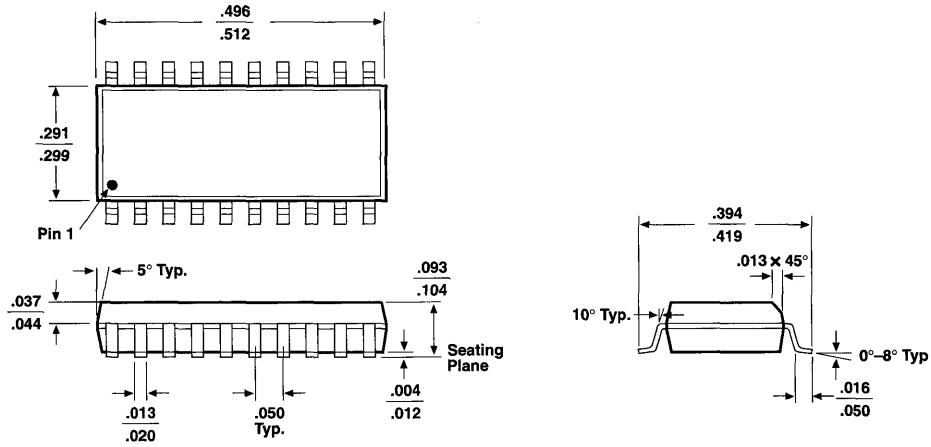
20-Pin Plastic Dual In-Line Package (PDIP)



20-Pin Plastic J-Lead Chip Carrier (PLCC)

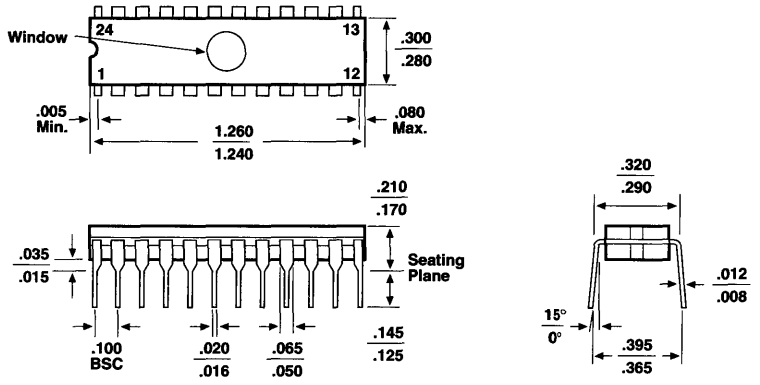


20-Pin Plastic Small-Outline IC (SOIC)

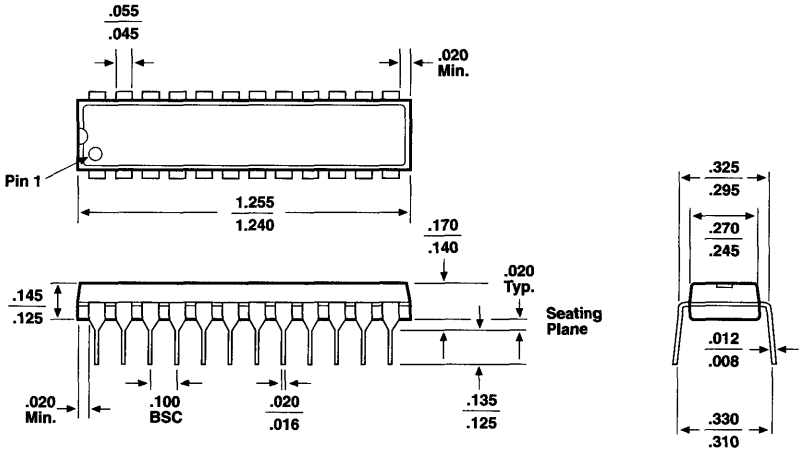


24-Pin Ceramic Dual In-Line Package (CerDIP)

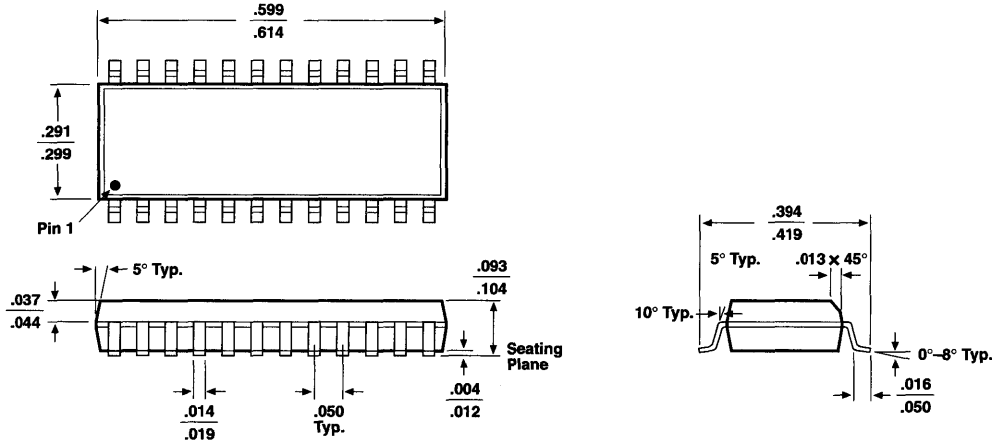
For military-qualified product, see case outline D-9 in Appendix C of MIL-M-38510.



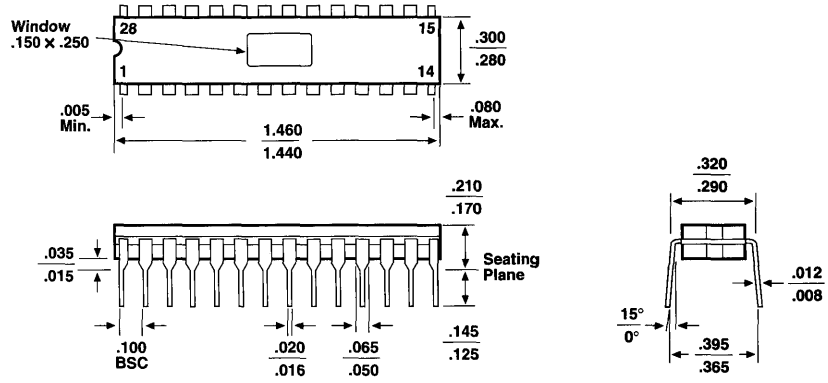
24-Pin Plastic Dual In-Line Package (PDIP)



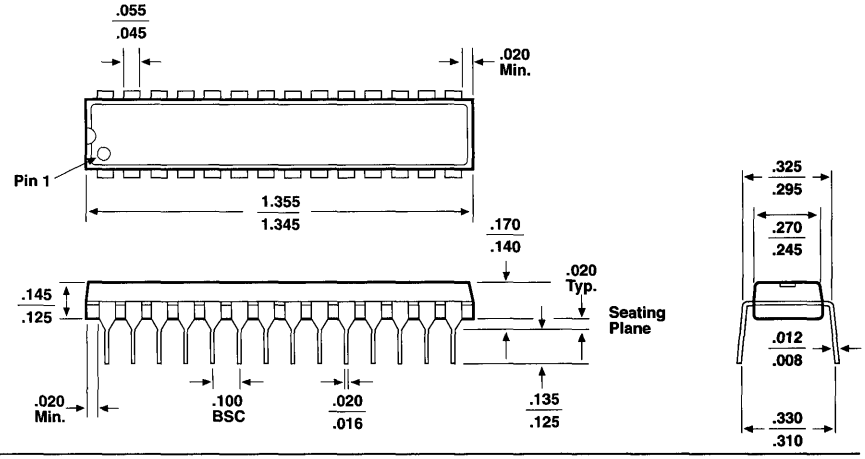
24-Pin Plastic Small-Outline IC (SOIC)



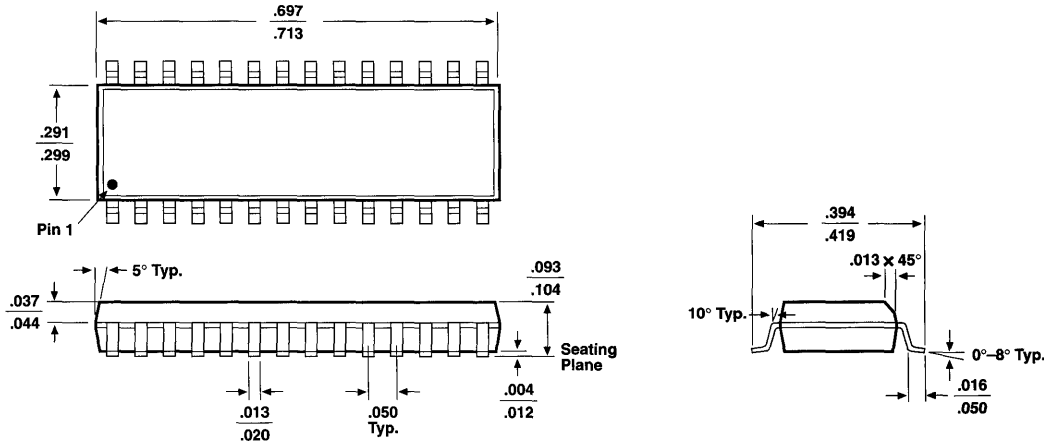
28-Pin Ceramic Dual In-Line Package (CerDIP)



28-Pin Plastic Dual In-Line Package (PDIP)

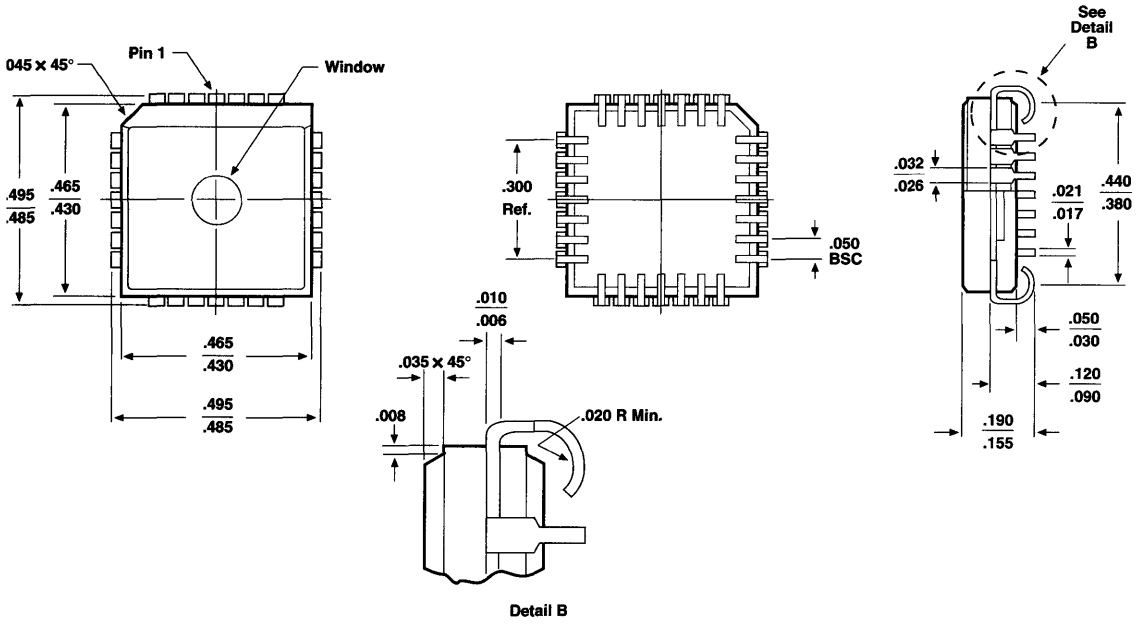


28-Pin Plastic Small-Outline IC (SOIC)

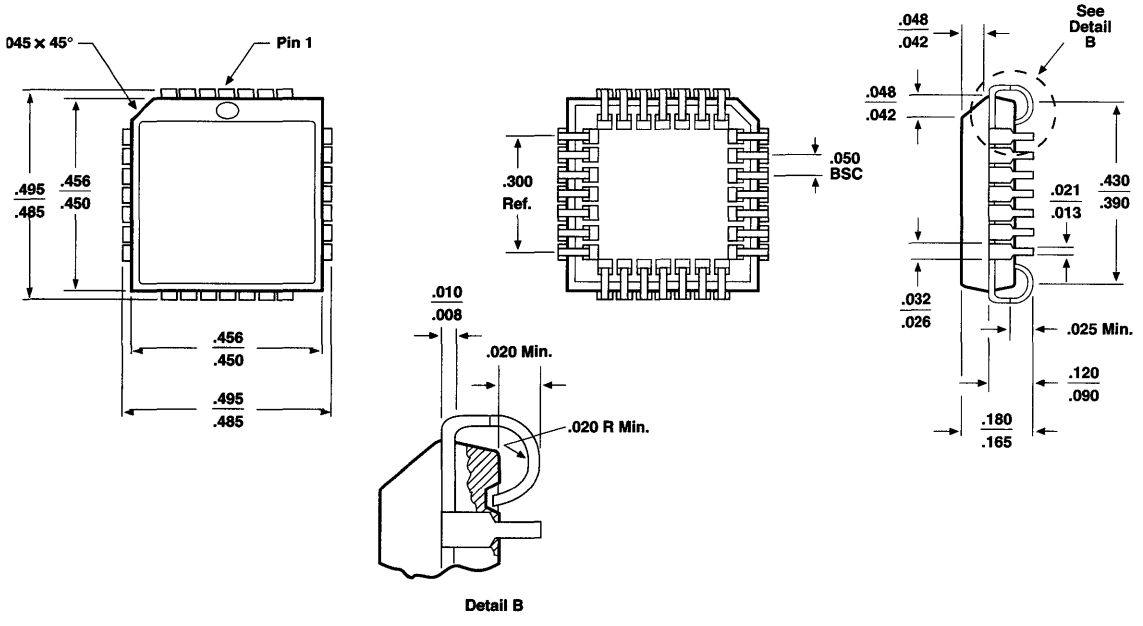


?8-Pin Ceramic J-Lead Chip Carrier (JLCC)

For military-qualified product, see case outline in Altera Military Product Drawing 02D-00194.

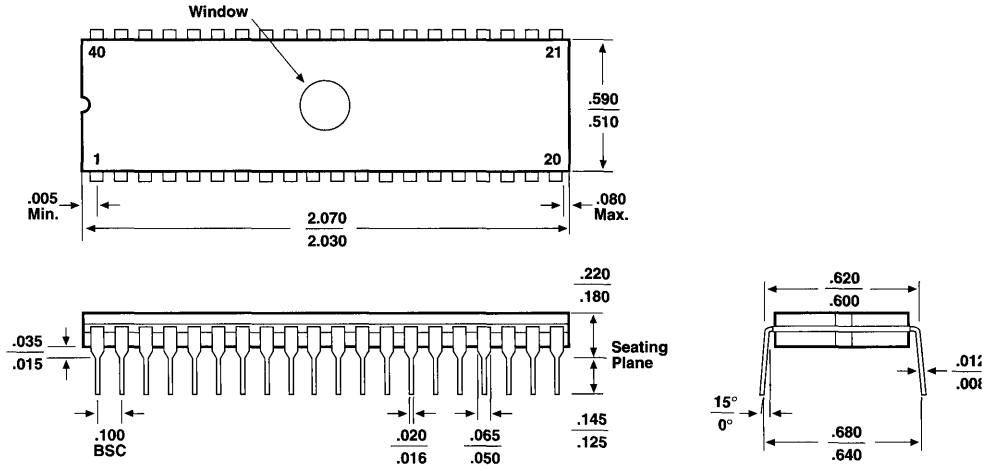


?8-Pin Plastic J-Lead Chip Carrier (PLCC)

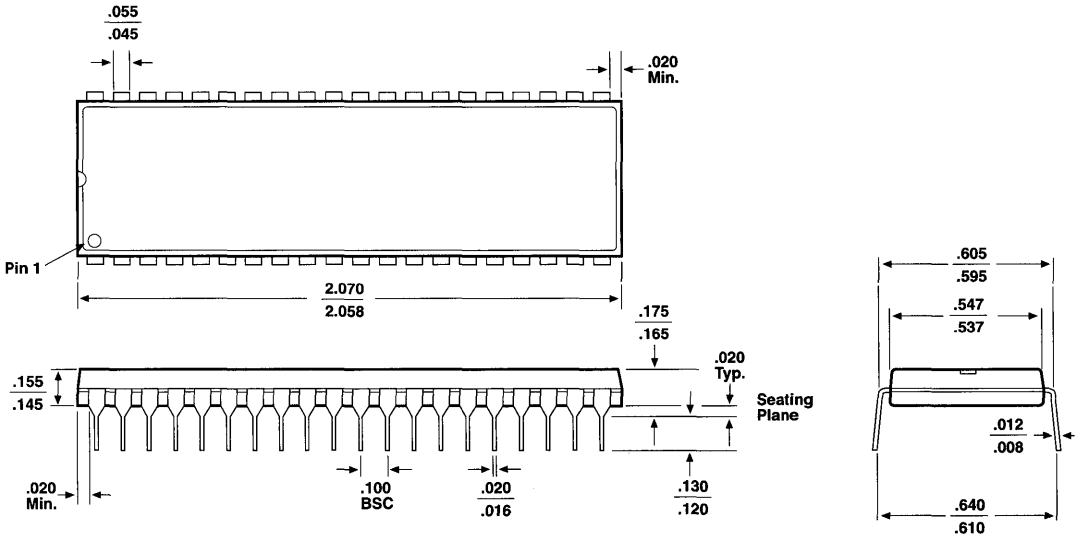


40-Pin Ceramic Dual In-Line Package (CerDIP)

For military-qualified product, see case outline D-5 in Appendix C of MIL-M-38510.

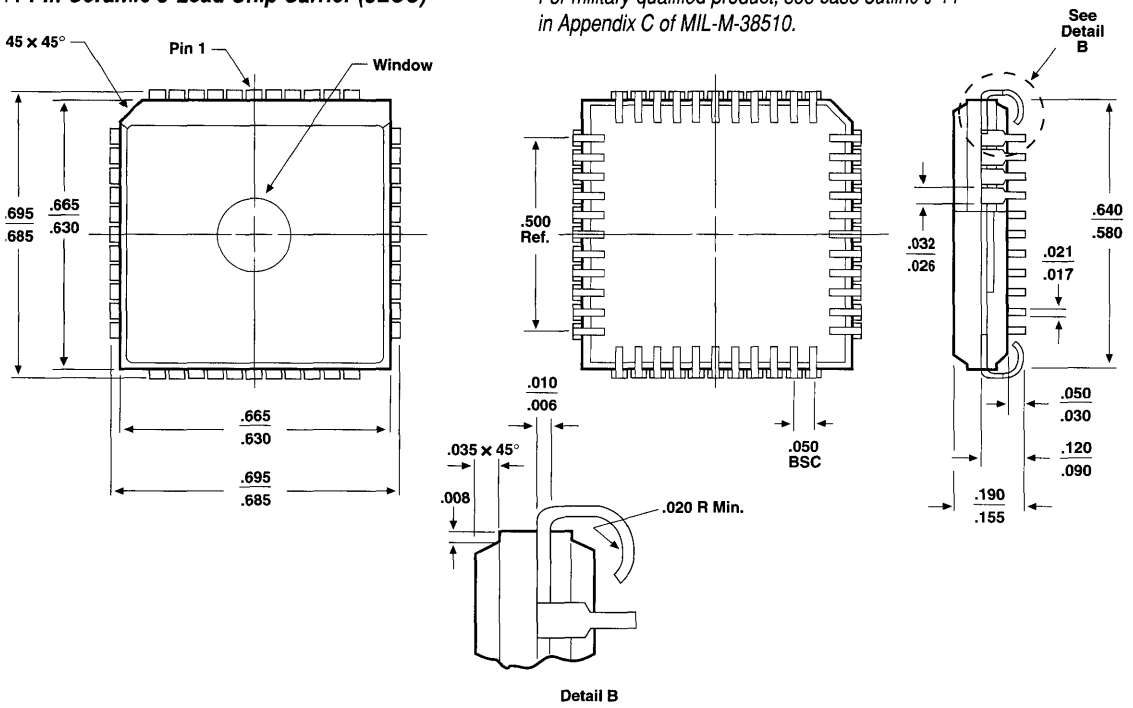


40-Pin Plastic Dual In-Line Package (PDIP)

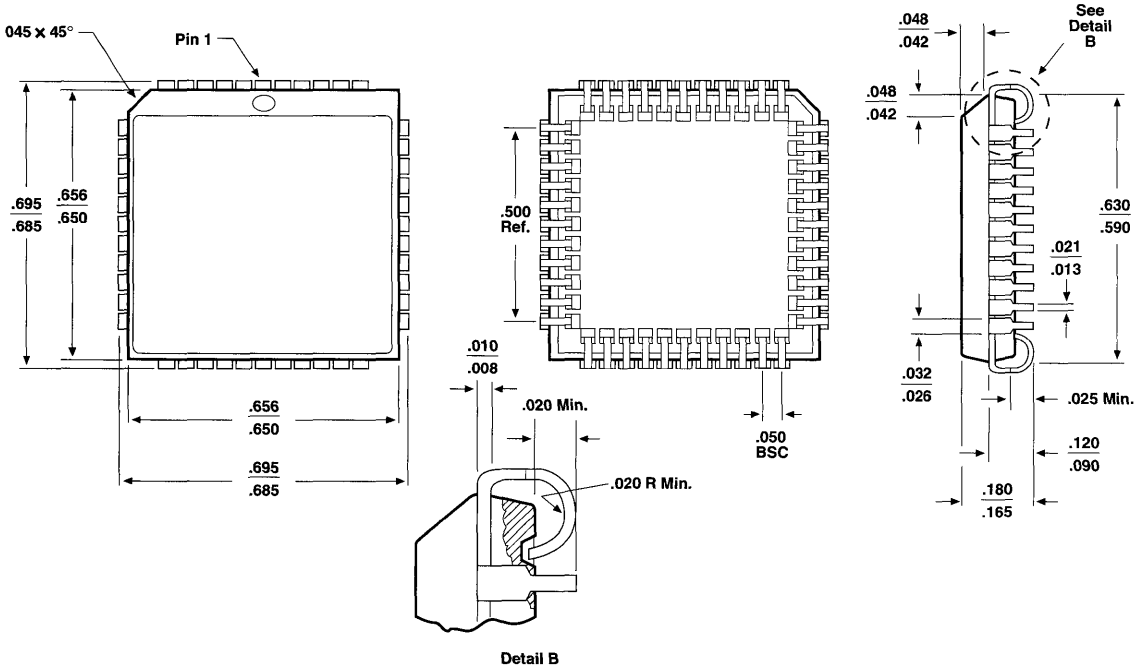


84-Pin Ceramic J-Lead Chip Carrier (JLCC)

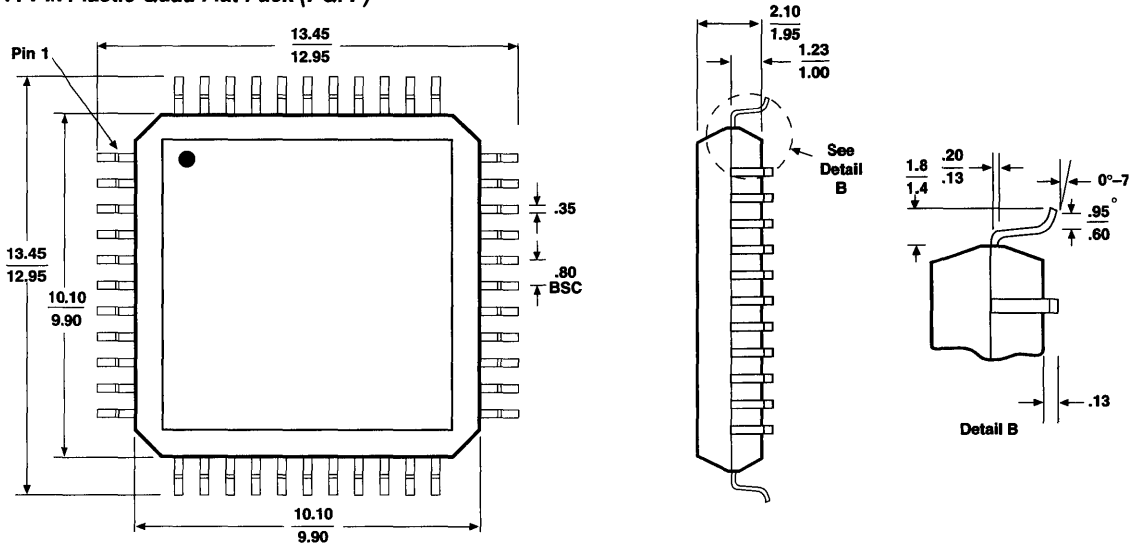
For military-qualified product, see case outline J-11 in Appendix C of MIL-M-38510.



84-Pin Plastic J-Lead Chip Carrier (PLCC)

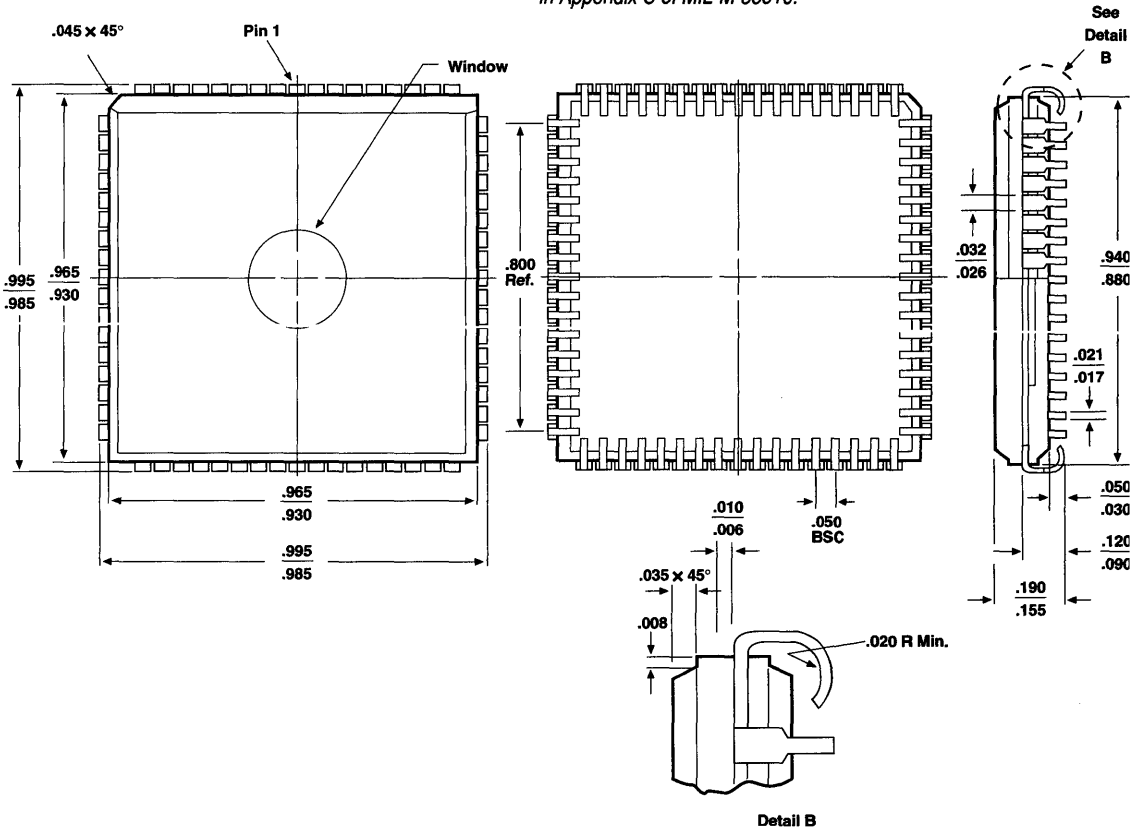


44-Pin Plastic Quad Flat Pack (PQFP)

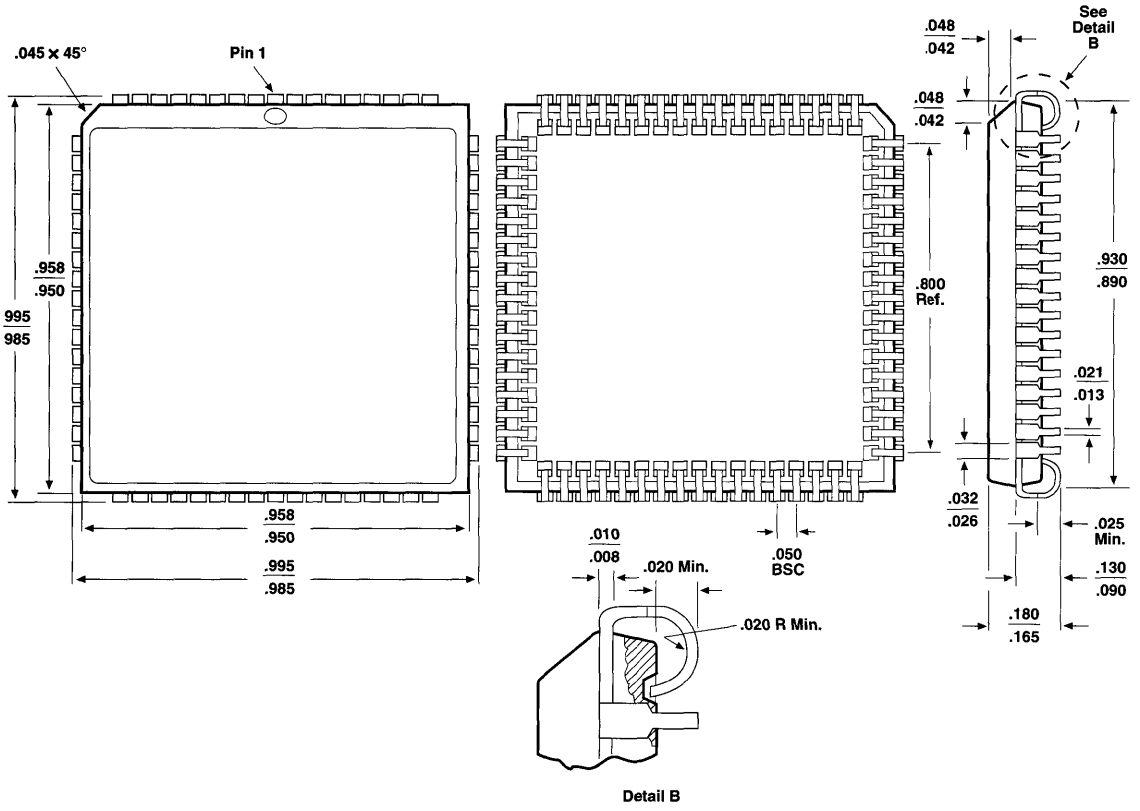


68-Pin Ceramic J-Lead Chip Carrier (JLCC)

For military-qualified product, see case outline C-J2 in Appendix C of MIL-M-38510.

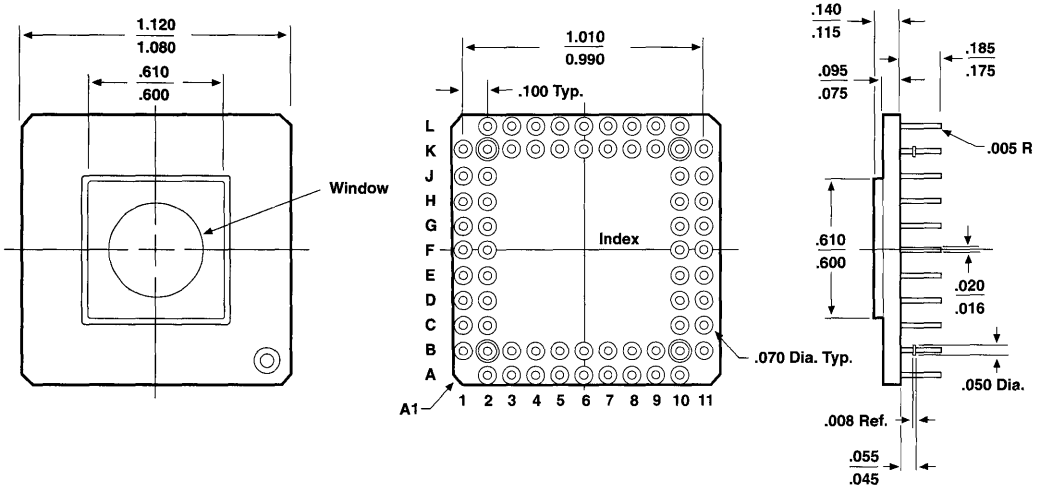


68-Pin Plastic J-Lead Chip Carrier (PLCC)

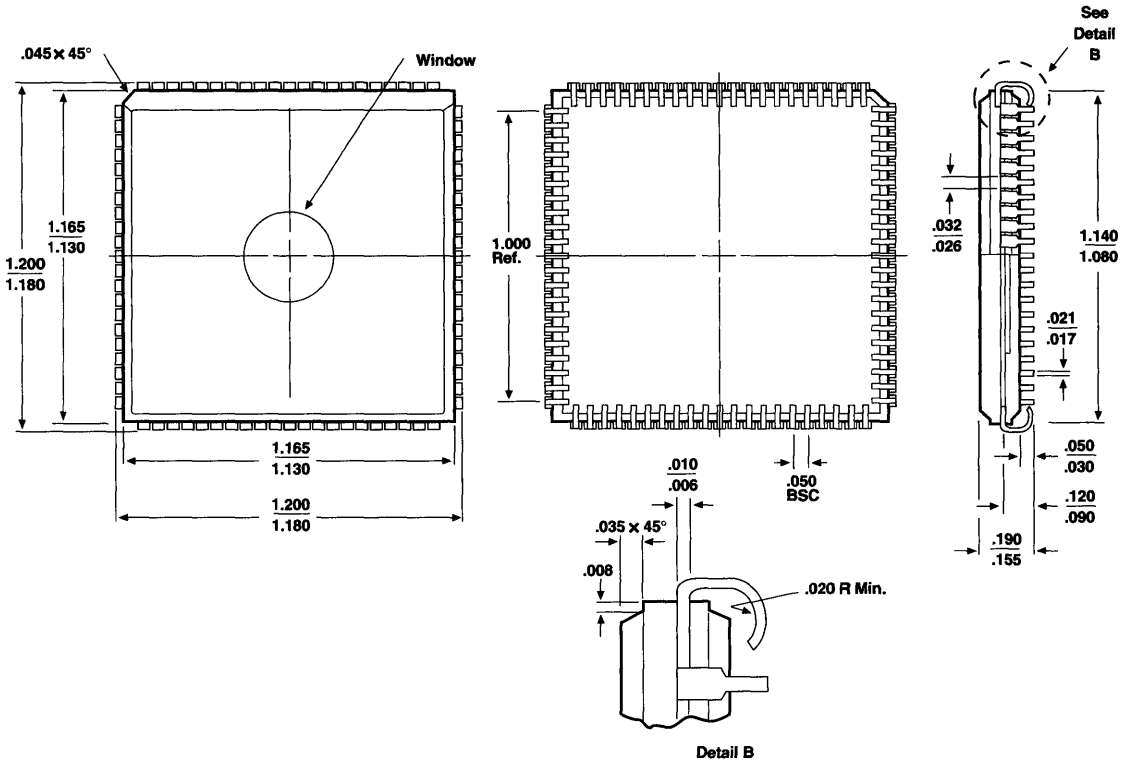


68-Pin Ceramic Pin-Grid Array (PGA)

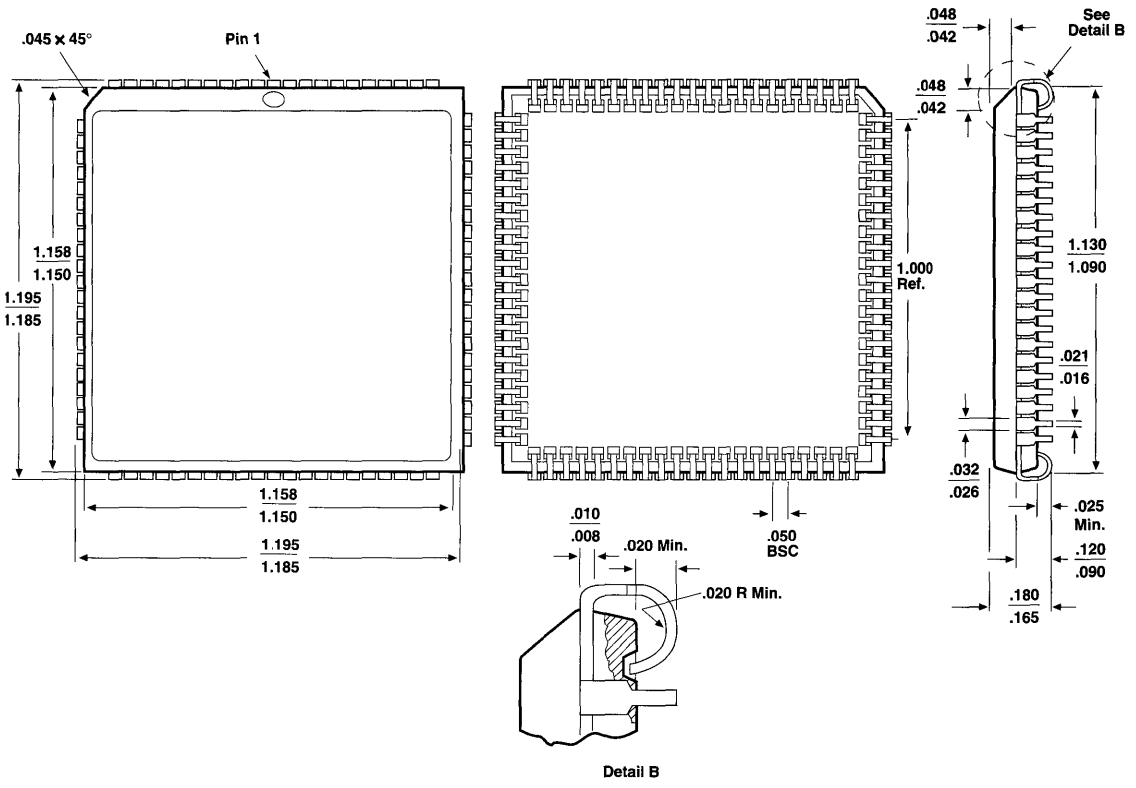
For military-qualified product, see case outline in Altera Military Product Drawing 02D-00205.



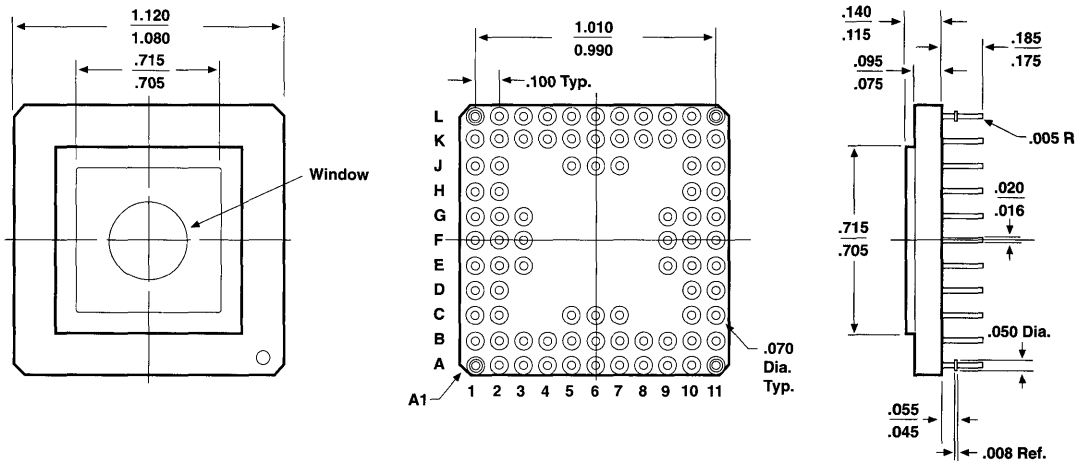
84-Pin Ceramic J-Lead Chip Carrier (JLCC)



84-Pin Plastic J-Lead Chip Carrier (PLCC)



84-Pin Ceramic Pin-Grid Array (PGA)



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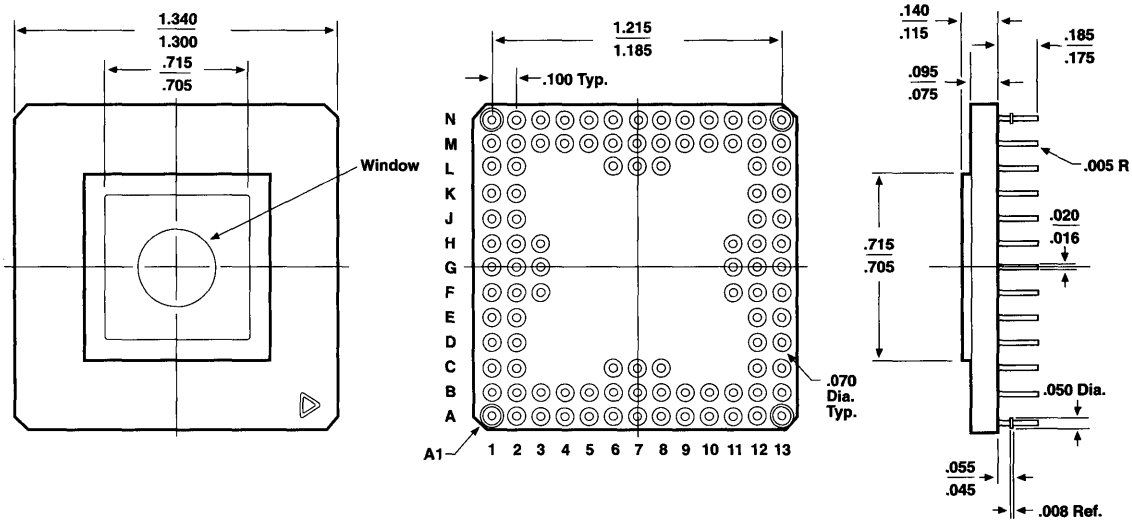
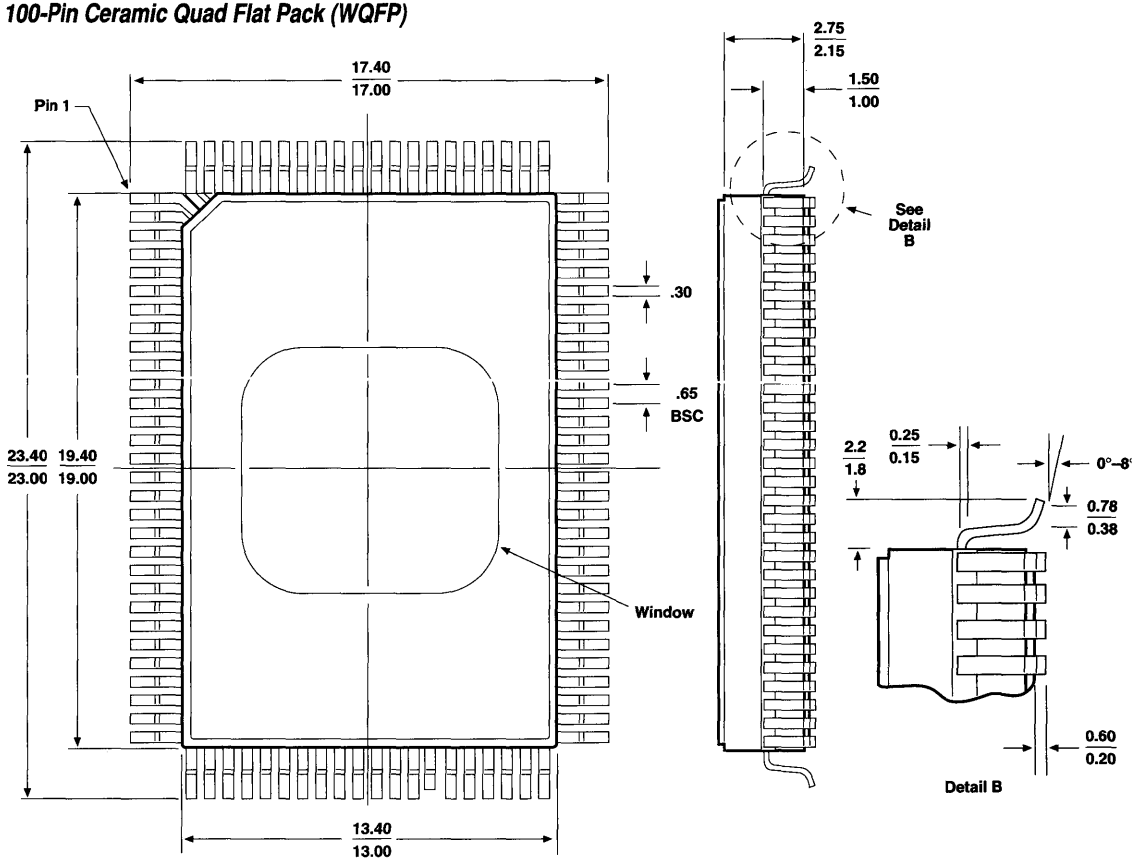
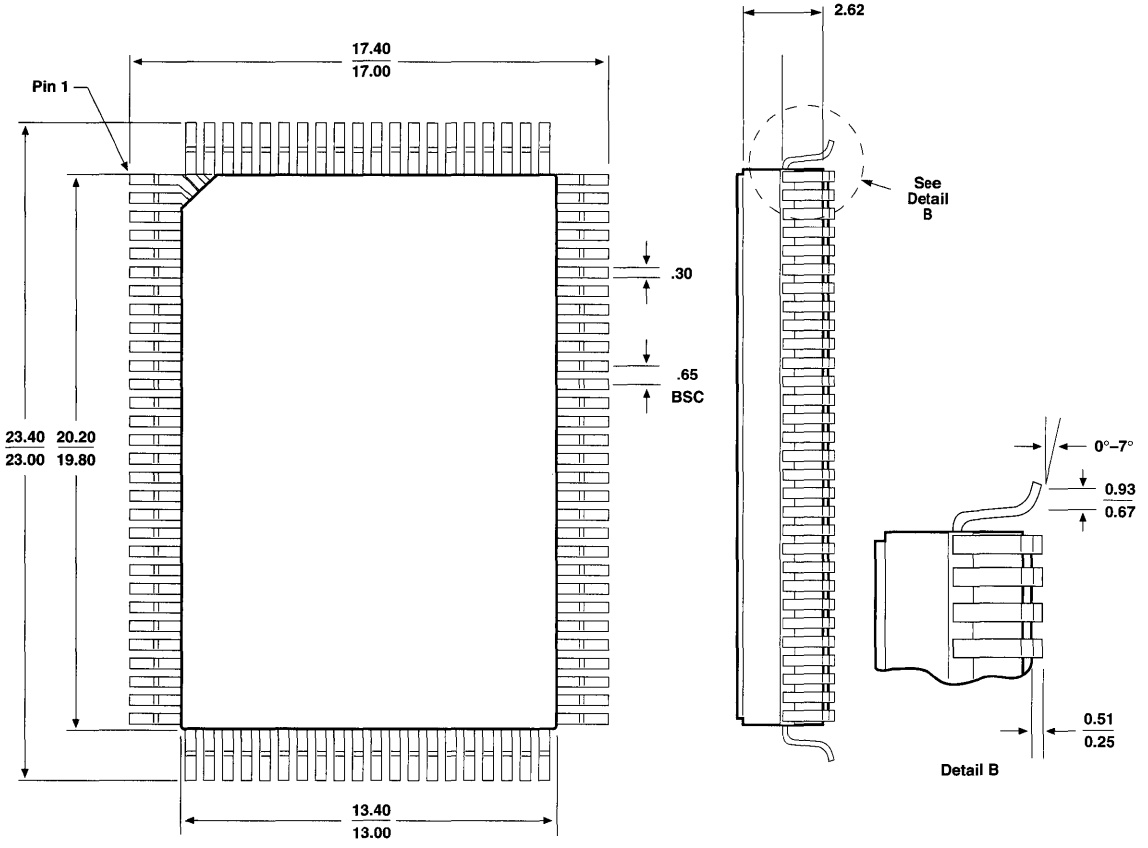


100-Pin Ceramic Quad Flat Pack (WQFP)



100-Pin Plastic Quad Flat Pack (PQFP)



Notes:

Thermal Resistance (°C/W)

September 1991, ver. 2

Data Sheet

ntroduction

Tables 1 and 2 give thermal resistance data for Altera Classic and MAX 5000 EPLDs. All thermal characteristics are measured using the Temperature Sensitive Parameter (TSP) test method described in MIL-STD-883C, Method 1012.1. Thermal resistance values were measured with the package at 25° C ambient temperature with no backplane or heat sink, and are accurate to ±5° C/W.

Table 1. Thermal Resistance of Classic EPLDs

EPLD	Number of Pins	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EP330	20	PDIP	68	19
		SOIC	88	17
EP610	24	CerDIP	60	10
		PDIP	55	18
		SOIC	77	17
EP610	28	JLCC	90	12
		PLCC	74	13
EP630	24	PDIP	50	17
		SOIC	77	17
EP630	28	PLCC	65	13
EP910	40	CerDIP	40	12
		PDIP	49	23
EP910	44	JLCC	67	5
		PLCC	58	10
EP1810	68	JLCC	47	12
		PLCC	44	13
		PGA	38	6
EP1830	68	PLCC	39	10

Note:

(1) The formula for determining θ_{JX} is $\theta_{JX} = (T_J - T_A)/PD$, where T_J = die junction temperature; T_A = ambient temperature; and PD = power being dissipated in the device causing a temperature rise at the die junction. T_J is determined by characterizing the relationship between the forward-biased voltage and temperature of the isolation diode between the power and ground pins of the IC.

Table 2. Thermal Resistance of MAX 5000 EPLDs

EPLD	Number of Pins	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EPM5016	20	CerDIP	62	10
		PDIP	61	27
		PLCC	C.F.	C.F.
		SOIC	C.F.	C.F.
EPM5032	28	CerDIP	44	12
		PDIP	48	19
		JLCC	69	9
		PLCC	59	10
		SOIC	C.F.	C.F.
EPM5064	44	JLCC	62	15
		PLCC	C.F.	C.F.
EPM5128	68	JLCC	39	11
		PLCC	C.F.	C.F.
		PGA	32	2
EPM5130	100	WQFP	C.F.	C.F.
		PQFP	C.F.	C.F.
		PGA	26	4
EPM5192	84	JLCC	30	4
		PLCC	C.F.	C.F.
		PGA	27	2

Notes:

(1) The formula for determining θ_{JX} is $\theta_{JX} = (T_J - T_A)/PD$, where T_J = die junction temperature; T_A = ambient temperature; and PD = power being dissipated in the device causing a temperature rise at the die junction. T_J is determined by characterizing the relationship between the forward-biased voltage and temperature of the isolation diode between the power and ground pins of the IC.

(2) C.F. = Consult factory.

Selecting Sockets for J-Lead Packages

September 1991, ver. 4

Application Brief 46

Introduction

EPLDs solve many of the problems designers face today. They offer low cost, low power, high reliability, and most importantly, high integration density. Altera offers windowed ceramic and one-time-programmable (OTP) plastic J-lead chip carrier (JLCC/PLCC) versions of many EPLDs to further reduce the "real estate" demands of a system. These small packages are generally intended for surface mounting. This application brief discusses the following topics:

- Types of sockets available for J-lead EPLDs
- Criteria for selecting burn-in or production sockets
- Carrier boards for use with wire-wrap panels and J-lead packages
- Results of Altera's evaluation of 44-, 68-, and 84-pin production sockets for use with windowed ceramic J-lead EPLDs

Despite recent advances, the acceptance of surface-mounting technology has been slower than expected, although considerable research and use have proved its feasibility. Most industrial applications still use traditional through-hole soldering. Surface-mount assembly places unique demands on the development and manufacturing processes by requiring different CAD symbols for PC board layout, different test and reliability procedures for buried vias within PC boards, and a different soldering process for production (vapor phase vs. wave solder). Bonding EPLDs to a PC board also removes the possibility of convenient erasure and reprogramming, which are particularly important during development.

A popular compromise that preserves the advantages of J-lead packages without the complications of surface mounting is to socket the J-lead EPLD. Conventional mounting techniques can then be used, either by through-hole soldering to a PC board or by mounting in a socketed carrier board for wire wrap.

Mechanical Considerations

There are two distinct types of sockets: burn-in and production sockets. Burn-in sockets are zero-insertion-force sockets. Since they will not deform the device's leads, they are the preferred carrier for an EPLD during the prototyping phase of a design. Older model burn-in sockets had the disadvantage of being significantly larger than production sockets. Newer burn-in sockets are now available with dimensions similar to those of production sockets. Using a burn-in socket during prototyping is the best way to prolong the life of a windowed ceramic EPLD.

Once a design enters the production phase, cost becomes a major concern. Low-cost production sockets, designed to hold a device permanently and securely, are widely available. Obviously, they must exert a reasonable force on the leads to prevent the device from popping out. After several insertions, this force can deform the leads, and eventually the leads can short out or fail to make contact, making the EPLD unusable. Therefore, Altera strongly recommends using a burn-in socket during the design and development phases of a project.

Production sockets must be chosen carefully. If the EPLD needs to be removed many times for reprogramming, low-insertion-force sockets that will not significantly deform the device pins for as many as 10 insertions are preferable. For high-stress environments (e.g., strong G-forces, thermal shock, high humidity), sockets with high insertion forces and optional retention clips are available. To further reduce the possibility of deforming device pins, most manufacturers of high-quality sockets include a stand-off inside the socket that prevents a device from being forced too far into a socket and having its pins bent.

Socket Evaluation

Altera has tested several production sockets for use with 44-, 68-, and 84-pin windowed ceramic J-lead EPLDs. Each socket underwent three tests:

- The change in the gap between the corner pins of each device was measured before and after each of 10 insertions.
- Each pin of the socket was wired in series and tested for open or short circuits lasting longer than 10 µs. This opens-and-shorts test was performed while the socket was attached to a vibration block. The amplitude of vibration was 3.0 mm peak-to-peak at a frequency that varied from 10 Hz to 55 Hz to 10 Hz, in 1-minute cycles for 2 hours. The vibration test was performed on all three axes at a temperature of 70° C.
- The actual point of contact between the socket pin and the device lead was photographed to determine the direction of the forces between them and the amount of surface contact.

Sockets from seven manufacturers were tested. Tables 1, 2, and 3 show the results of the opens-and-shorts tests for the 44-, 68-, and 84-pin production sockets that passed the tests. Ranking was determined by the socket's ability to maintain the EPLD's pin integrity after multiple device insertions. For more information about these socket tests, call Altera Applications at 1 (800) 800-EPLD.

Table 1. Summary of 44-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat Inc. PCS-044A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
AMP, Inc. 821575-1	Large pin deformation. Contact force has a downward component. No retainer clip option.

Table 2. Summary of 68-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat Inc. PCS-068A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-68-2	Low pin deformation. Contact force has a downward component. Has a retainer clip option.
3M/Textool Corporation 2-0068-06234-070-038-077	Moderate pin deformation. Contact force is lateral. Has a retainer clip option.
AMP, Inc. 821574-1	Moderate pin deformation. Contact force has a downward component. No retainer clip option.

Table 3. Summary of 84-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat Inc. PCS-084A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-84-2	Moderate pin deformation. Contact force has a downward component. Has a retainer clip option.
Burndy Corp. QILE-84P-410T	Large pin deformation. Very tight fit. No retainer clip option.
AMP, Inc. 821573-1	Large pin deformation. Very tight fit. No retainer clip option.

Vendors may provide additional information about their products, such as material selection, prevention of solder ingress during wave soldering, or lead shape. Altera recommends qualifying sockets before committing to a particular vendor.

Table 4 shows the contact distance for Altera EPLDs. These measurements should be used to select a socket (preferably with internal stand-offs) for use with Altera EPLDs.

Table 4. EPLD Contact Distances

EPLD *(1)*	Pin Count	Contact Distance (mils)	
		Minimum	Maximum
EP330L, EPM5016L	20	385	395
EP610J, EPM5032J, EPS448J	28	485	495
EP610L, EP630L, EP610AL EPM5032L, EPB2002AL, EPS448L	28	485	495
EP910J, EP910AJ, EPM5064J, EPS464J	44	685	695
EP910L, EP910AL, EPM5064L, EPS464L	44	685	695
EP1810J, EPM5128J	68	985	995
EP1810L, EP1830L, EPM5128L	68	985	995
EPB2001J, EPM5192J	84	1180	1200
EPB2001L, EPM5192L	84	1185	1195

Note:
(1) J = Windowed ceramic J-lead chip carrier (JLCC)
L = One-time-programmable plastic J-lead chip carrier (PLCC)

Packaging Options for Wire-Wrap Applications

Wire-wrap applications require a through-hole mount compatible with the J-lead package. The sockets specified do not typically mechanically conform to most wire-wrap panels. Wire-wrap cards have machine receptacles in rows with 100-mil spacing between receptacles and 300-mil spacing between rows.

Carrier boards provide an effective way to bridge the gap. Mounting a socket to a carrier board provides the convenience of wire wrap with only a small real estate penalty. Some carrier boards have signal routing with shorter paths or 45-degree bends to minimize signal reflection.

Manufacturers

Table 5 lists corporate offices of the vendors noted in this application brief. Contact the appropriate vendor for additional information.

Table 5. Manufacturers

Company	Product	Telephone Number
3M/Textool Corporation	Production Sockets	(800) 225-5373
AMP, Inc.		(800) 552-6752
Augat Inc.		(800) 999-9863
Burndy Corporation		(408) 245-2590
ITT/Cannon Corporation		(714) 261-5300
3M/Textool Corporation	Test and Burn-In Sockets	(800) 225-5373
AMP, Inc.		(800) 552-6752
Advanced Interconnections Corporation		(401) 823-5200
Dai-Ichi Seiko Co., Ltd. (Japan)		011-81-0482-53-3131
Emulation Technology, Inc.		(408) 982-0660
Advanced Interconnections Corporation	Carrier Boards and Wire Wrap Adapters	(401) 823-5200
Emulation Technology, Inc.		(408) 982-0660

Information in this application brief is based on tests performed by Altera and information provided to Altera by various vendors, and is believed to be accurate. Altera assumes no liability for the use of third-party products mentioned in this publication.

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September 1991

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