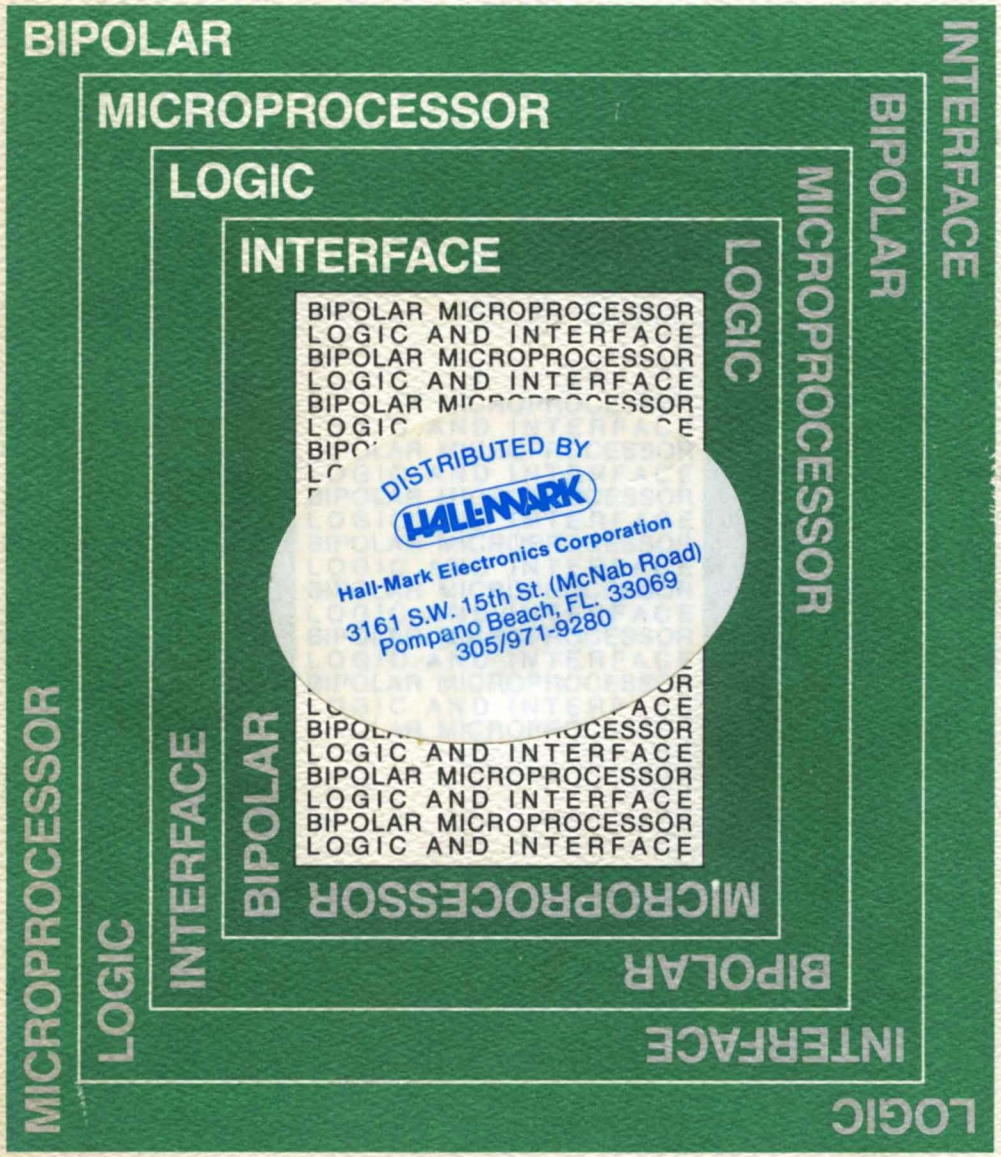
Bipolar Microprocessor Logic and Interface

Am2900 Family
1985 Data Book



ADVANCED MICRO DEVICES

Advanced Micro Devices

Bipolar Microprocessor Logic and Interface Data Book

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Am29818	Diagnostics Register, 8 Bits
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MSI Logic	
Am2921	One-of-Eight Decoder, Three-State, Polarity Control
Am2922	8-Input Multiplexer with Control Register
Am2923	8-Input Multiplexer
Am2924	Three-to-Eight Decoder/Demultiplexer
Am29806	6-Bit Comparator
Am29809	9-Bit Comparator
Am25S05	Four-Bit by Two-bit Two's Complement Multiplier
Am25S07	Hex/Quad Parallel D Registers with Register Enable
Am25S08	Hex/Quad Parallel D Registers with Register Enable
Am25S09	Quad Two-Input, High-Speed Register
Am25S10	4-Bit Shifter, Three-State Outputs
Am25S18	Quad D Register with Standard and Three-State Outputs
Am25LS07	Hex/Quad Parallel D Registers with Register Enable
Am25LS08	Hex/Quad Parallel D Registers with Register Enable
Am25LS09	Quad Two-Input, High-Speed Register
Am25LS14A	8-Bit Serial/Parallel Multiplier
Am25LS15	4-Bit Serial/Parallel Adder/Subtractor
Am25LS22	8-Bit Serial/Parallel Register, Sign-Extend
Am25LS23	8-Bit Shift Register, Synchronous Clear
Am25LS2513	Eight-to-Three Line Priority Encoder, Three-State
Am25LS2517	4-Bit ALU/Function Generator
AM25LS2518	Quad D Register with Standard and Three-State Outputs
Am25LS2519	Quad Register with Two Independently Controlled Three-State Outputs
Am25LS2520	Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control
Am25LS2521	8-Bit Comparator
Am25LS2521A	Fastest (IMOX) Version of 25LS2521
Am25LS2535	8-Input Multiplexer with Control Register
Am25LS2536	8-Bit Decoder with Control Storage
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Am25LS2538	One-of-Eight Decoder with Three-State Outputs and Polarity Control
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Am25LS2548	Chip Select Address Decoder
Am25LS2568	BCD Decode Up/Down Counter, Three-State
Am25LS2569	4-Bit Up/Down Counter, Three-State

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Part Number	Description
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Am26LS27	Dual Party-Line Transceivers, Serial
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Am26LS29	Quad Driver RS423, Three-State
Am26LS30	Quad Driver RS422/423
Am26LS31	Quad Driver RS422, High-Speed
Am26LS32	Quad Differential Line Receivers
Am26LS32B	Quad Differential Line Receiver RS422/423
Am26LS33	Quad Differential Line Receiver, High Common Mode
Am26LS38	Quad Differential Backplane Transceiver
Am7960	Coded Data Transceiver
Am7990	Local Area Network Controller for Ethernet
Am7991	Serial Interface Adapter

Description	4 Bits	8 Bits	9 Bits	10 Bits
Bus Drivers	2912	2958 2959 2965 2966		29827 29828
Bus Transceivers (Bidirectional)	2926 2929 26S10 26S11 26S12A	2946 2947 2948 2949	29833 29834 29863 29864 29853 29854	29861 29862
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Systems Design Considerations and Training

Bipolar Technologies

Advanced Micro Devices emphasizes Research and Development expenditures for developing the most advanced technologies for Bipolar processing, circuit design, and Very Large Scale Integration (VLSI).

Today, Advanced Micro Devices' bipolar products combine ECL-internal circuitry, the super high performance IMOX™ process, and VLSI integration to offer the system designer the most compact high performance integrated circuits. This, plus AMD's systems solution approach to design problems, makes the Am2900 Family the best choice for fastest applications.

IMOX

First introduced in 1980, IMOX is the name of Advanced Micro Devices' proprietary bipolar process. IMOX is an acronym which means: 1) Ion-IMplantation of dopants for tighter parameter control and lower power consumption; and, 2) OXide-isolation of transistor structures which results in faster transistor switching and tighter packing. Older, LS-type processes used diffused isolation for isolating transistor structures; this had the disadvantage of a large die area and high parasitic capacitance.

AMD is also applying IMOX to bring out higher-speed versions of earlier Am2900 devices. Figure 1 shows the evolution of the Am2901 Four-bit Microprocessor Slice. First introduced in 1975, the Am2901 has been repeatedly redesigned and is now available in the IMOX Am2901C version, which is less than half the size and more than twice the speed of the original Am2901 — and costs less. The current generation IMOX process has an 8 micron pitch (pitch equals the total of the width of metal lines plus the spacings between metal lines). In 1983, AMD brought into full scale production a completely new Fabrication Facility in San Antonio, Texas which will feature the state-of-the-art in process and masking equipment, and allow products which feature the IMOX process but with a pitch of only 4 microns, by late 1983. This version of IMOX is termed IMOX-S2. The 50% reduction in metal pitch will dramatically increase the level of integration of new products and also provides > 30% increase in device speed.

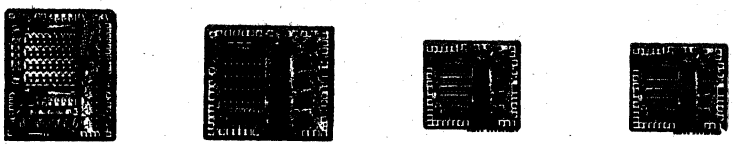
ECL-INTERNAL CIRCUITRY

All Am2900 devices today are TTL-compatible on inputs and outputs and use standard +5V and ground for supply voltages. TTL is a good interface standard for systems design today, but TTL gates are slow, and ECL gates are much faster. To offer TTL-compatibility but near-ECL speeds to our customers, AMD has adopted a circuit design approach which features all ECL-circuitry for the internal circuitry of all LSI and VLSI devices (see Figure 2).

This approach, ECL-internal circuitry, provides near-ECL speeds to TTL-I/O designers. Of course the ECL gate structures inside the device are completely transparent to system designers because of the 100% adherence to TTL standards for I/O specs. Also, these chips only require +5V and ground because internal gates are not the same type of ECL gates as those used with 10K or 100K logic. The final point to note is that ECL has a reputation for being very power intensive. While the Am2900 Family are not low-power devices, they do significantly reduce the total power usage in a high performance systems design because of the large number of SSI/MSI devices they replace. These ECL gates are not run at the very high power levels of traditional ECL circuits.

Figure 1. Bipolar Speed/Density Improvements

Am2901 FOUR-BIT MICROPROCESSOR SLICE



540 GATES 800mW 40-PIN DIP

DIE SIZE	Am2901 33,000 MILS²	Am2901A 20,000 MILS²	Am2901B 15,000 MILS²	Am2901C 15,000 MILS²
SPEED A, B → G, P	80ns	65ns	50ns	37ns
TECHNOLOGY	LOW-POWER SCHOTTKY	DUAL LAYER METAL ION-IMPLANTATION	PROJECTION PRINTING	ECL INTERNAL TTL I/O IMOX
	1975	1977	1978	1981

IMOX is a trademark of Advanced Micro Devices, Inc.

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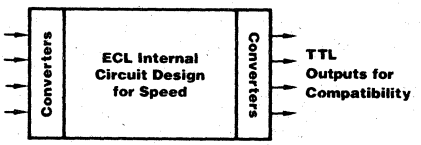
Using internal ECL with TTL-I/O does involve paying a translation speed penalty at the inputs and outputs of the device, but because these devices are LSI and VLSI with many levels of internal gating between input and output, the translation penalty is more than compensated for by the extra performance gained by the multiple layers of high speed ECL gates. Figure 3 shows an approximate comparison of the IMOX- with-internal-ECL approach to other process/circuit offerings available to designers utilizing high speed TTL compatible ICs. IMOX offers an excellent combination of high speed and relatively low power. The speed comes not only from the IMOX process but also from the use of ECL gates for internal circuitry. The FAST and AS/ALS Families are populated primarily with MSI devices where ECL-internal gating is not feasible due to the few layers of internal gating relative to the TTL/ECL translation delay penalty. Note also that Am2900/IMOX devices use an order of magnitude less power per gate than traditional ECL 10K and 100K devices.

BIPOLAR VLSI

Advanced Micro Devices is the leader in high integration, high performance integrated circuits. Our largest device to date, the Am29116, is a 2500-gate device measuring 68,000 square mils in area, and currently in development are devices of four times that complexity using our new IMOX-S2 process. AMD's emphasis on Very Large Scale Integration bipolar is best illustrated in Figure 4 below.

Figure 4 demonstrates AMD's commitment and leadership in large scale integration bipolar since the introduction of the original Am2901 in 1975. Another graphic demonstration of the growing complexity of our devices is the relative die sizes of successively complex arithmetic processors, as shown in Figure 5.

Figure 2. Am2900 Circuit Design for Maximum Speed



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- All ECL would be only 7–15% faster
- Practical approach for LSI/VLSI

Figure 3.

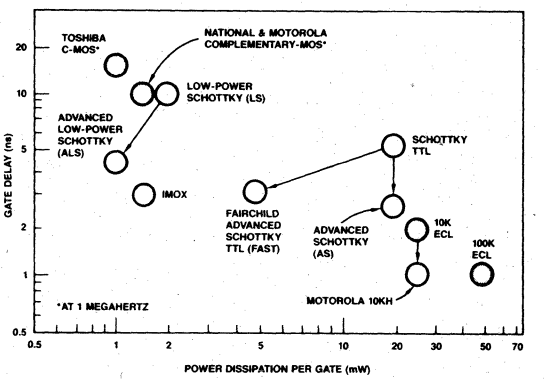

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Figure 4. Am2900 Bipolar LSI/VLSI

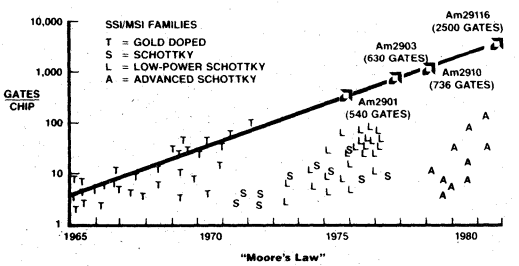

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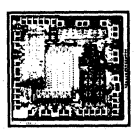
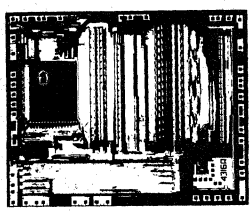
Figure 5.

74LS374 MSI



Am2901C LSI



Am29116 VLSI

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DESIGNER'S GUIDE TO HIGH PERFORMANCE LOW-POWER SCHOTTKY LOGIC

By David A. Laws and Roy J. Levy.

INTRODUCTION

Advanced Micro Devices is a leading supplier of low-power Schottky MSI and LSI devices. Two basic families of product are offered:

Am54/74LS Series
- Typical tpd 10ns/gate at 2mW
- Typical Register fmax = 40MHz

Pin for pin and electrical alternate source devices to the standard performance LS logic family.

Am25LS Series
- Typical tpd 5ns/gate at 2mW
- Typical Register fmax = 65MHz

Advanced Micro Devices' proprietary high performance LS logic family. This includes both original designs and enhanced specification versions of the Am54/74LS devices. Improvements include twice the fan-out over the military temperature range, higher noise margin and faster switching speeds.

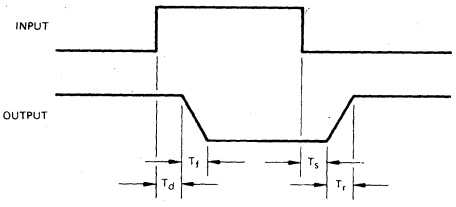
THE SCHOTTKY DIODE STRUCTURE

The major components of switching delays in digital integrated circuits are listed in Figure 1. One of the most significant of these is the storage time constant of a transistor driven into saturation Ts. Older TTL circuits minimized this parameter with process technique known as gold doping. This increased the rate of recombination of charge stored in the base region.

The desired result of improved speed was achieved. Unfortunately it also reduced available design β at low temperatures and was marginally effective when hot. This resulted in lowered performance over the full military temperature range.

The development of the Schottky diode provides a more effective solution. A feature of the Schottky diode is its lower forward voltage at a given current level compared to a diffused (P-N) diode of the same area, Figure 2. Connecting a Schottky diode between the base and collector of a transistor, Figure 3, will shunt excess base current drive from the base to the collector, once the collector drops to a low enough voltage to forward bias the Schottky. This prevents the build up of stored charge and eliminates the Ts component of the delay.

A Schottky diode is formed at a metal to semiconductor junction when the semiconductor doping is at the level normally found in the collector region of TTL devices. A Schottky-clamped transistor is constructed by extending the metal contact for the base region over the collector as shown in Figure 4. The same metallization structure forms a simple ohmic contact at the base, collector and emitter contact window because of the higher doping levels in the silicon at these locations.



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Parameters	Determining Factors
T_d	R, C
T_f	β, Cob, Base Drive, Signal Amplitude
T_s	Storage Time Constant of a Saturated Transistor
T_r	Cob, Signal Amplitude

Figure 1. Major Causes of Propagation Delay.

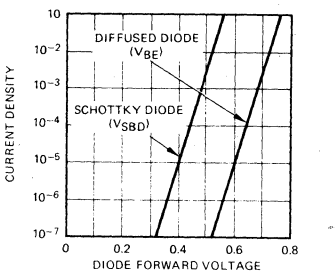

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Figure 2. Comparison of V_F for Schotty and Diffused Diodes.

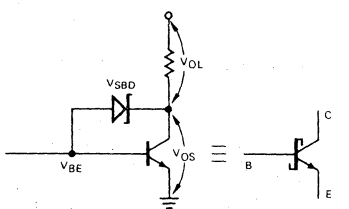

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Figure 3. Schottky Clamped Transistor and its Convential Circuit Symbol

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The selection of the forward voltage drop across the Schottky diode, V_{SBD}, is a compromise between a high value to insure a minimum V_{OL} but low enough to prevent charge storage in the base. Platinum silicide Schottky diodes provide this optimum voltage drop. Platinum is deposited and platinum-silicide is formed by sintering and annealing. As aluminum has a high affinity for silicon, in order to prevent the aluminum interconnect metallization from diffusing through the platinum material, with resulting lower V_{SBD}, a barrier of tungsten-titanium is evaporated after the platinum and before the aluminum metallization. This structure has been extensively evaluated and proven to have excellent reliability characteristics. It is now widely employed in the manufacture of Schottky devices. Reliability data is available from Advanced Micro Devices on request.

CHARACTERISTICS OF SCHOTTKY DEVICES

The primary reason for the development of Schottky devices was to improve AC (switching) performance and the first integrated circuits to employ this technique offered propagation delays as fast as 3ns. However, their fast rise and fall times and high power requirements have restricted their application to highest performance systems. It was realized that the technique could be used to decrease the charging current required to achieve the 10ns speed specification of older TTL gates. This insures considerably lower operating power requirements. The resulting family of devices are known as Low-Power Schottky (LS) circuits.

2. D.C. Circuit Characteristics

CIRCUIT CONFIGURATIONS

The basic circuit design configuration of a Low-Power Schottky gate is similar to that of the original standard TTL elements. However, certain refinements have been made to optimize device performance when fabricated with the LS process.

In order to analyze the circuit configuration, Table 1 shows terms used in describing Advanced Micro Devices' LS circuits:

TABLE 1.

D.C. CIRCUIT PARAMETER DEFINITIONS

I_{IL}	The current out of an input at a specified LOW voltage.
I_{IH}	The current into an input at a specified HIGH voltage.
I_{OL}	The current into an output when in the LOW state.
I_{OH}	The current out of an output when in the HIGH state (pull-up circuit only).
I_{SC}	The current out of an output in the HIGH state when shorted to ground. (Also called I_{OS})
V_{CC}	The range of supply voltage over which the device is guaranteed to operate.
V_{IL}	The guaranteed maximum input voltage that will be recognized by the device as a logic LOW.
V_{IH}	The guaranteed minimum input voltage that will be recognized by the device as a logic HIGH.
V_{OL}	The maximum guaranteed logic LOW voltage at the output terminal while sinking the specified load current I_{OL}.
V_{OH}	The minimum guaranteed logic HIGH voltage at the output terminal when sourcing the specified source current I_{OH}.
I_{OZH}	Three-state off-state output current, high level voltage applied.
I_{OZL}	Three-state off-state output current, low-level voltage applied.

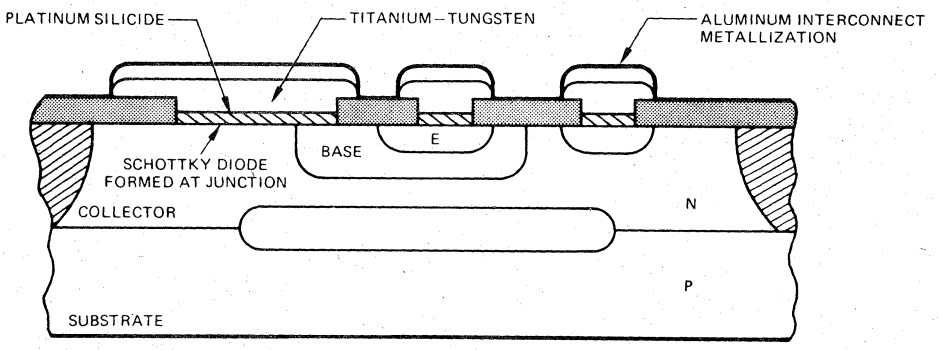

Figure 4. Schottky Diode Clamped Transistor Structure.

Both the input and output structures of the LS devices themselves have evolved through a number of configurations as designers have attempted to optimize circuit performance.

Depending on the function of the device any one of four commonly used inputs may be employed. The significant characteristics of each of these configurations are summarized in Figure 5.

The first LS designs used the familiar multi-emitter TTL input of Figure 5a. However because of low breakdown voltage and slow speed it is now used only where the geometry offers a significant advantage in circuit mask layout.

The second and still most widely used structure is the simple DTL style input of Figure 5b. This is the fastest version and it has good input breakdown voltage. In output functions having

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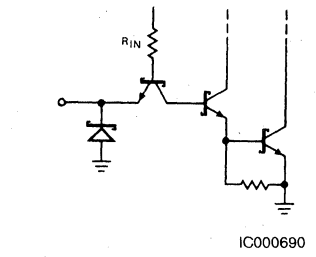
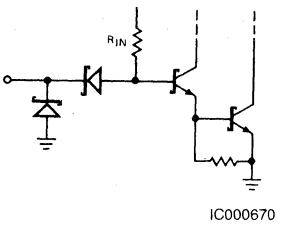
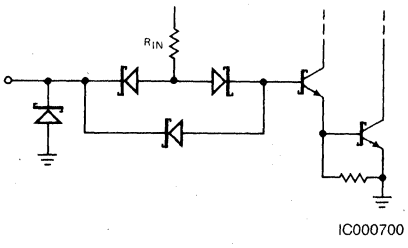
only a single gate delay between input and output, such as a three-state enable input, the low threshold of the DTL configuration causes the output node to be at a sufficiently low voltage to risk leakage problems at high temperature. The input of Figure 5c raises the threshold by one diode to overcome this problem (Figure 6). However because it is slower and uses more silicon area, its use is limited to special situations. A PNP input, Figure 5d, insures low d.c. loading for devices with common input/output pins such as the Am25LS23. However it is slow and has low breakdown voltage, comparable to the multi-emitter TTL structure.



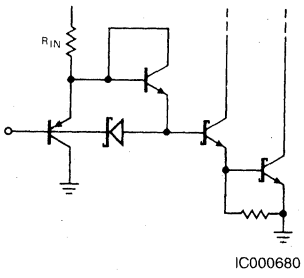
a) TTL



b) DTL



c) High Threshold



d) PNP

	DTL	HIGH V_{th}	TTL	PNP
Threshold @ 25°C	1.0V	1.4V	1.3V	1.5V
C_{in}	5.5pF	4.5pF	3.5pF	4.0pF
I_{IL}	αR_{IN}	αR_{IN}	αR_{IN}	αB_{PNP}
Input BV	> 15	> 15	≈8	≈8
Gate Delay, ns	5+, 5 –	5+, 6.5 –	5.5+, 7.5 –	5+, 6.5 –

Figure 5. Low-Power Schottky Input Configurations.

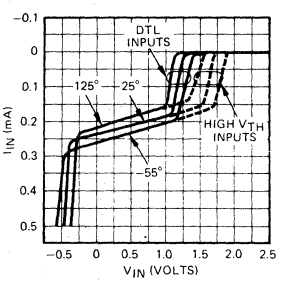


Figure 6. LS Input Characteristics for DTL and High Threshold Inputs.

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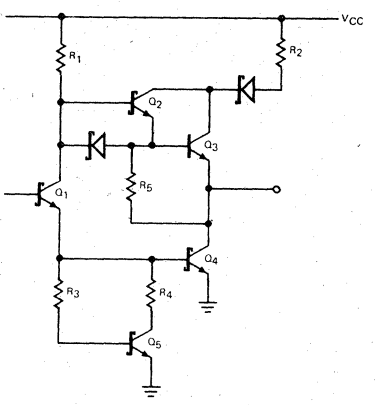
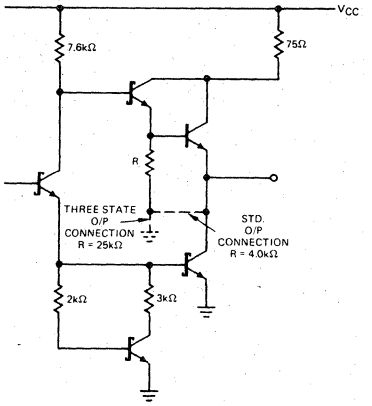
Figure 7 compares the early LS output configuration with the design most frequently used today. The change was made to provide clamping of positive ringing and to allow the higher I_{SC} currents now specified (see section 3). The typical V_{OH} versus I_{OH} curves of Figure 8 are similar for both versions.

This example displays an I_{SC} of approximately 35mA. Note that both of these designs include the "squaring" network (R_3,R_4 and Q_5) at the base of the output pulldown transistor, Q_4, which was not included on standard TTL families. The result of this is a sharp transition of V_{OUT} with V_{IN} shown in Figure 9 for a simple gate function.

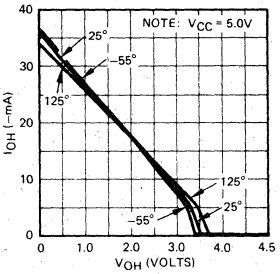


IC000650



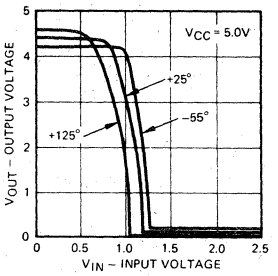
IC000660

Figure 7. Low-Power Schottky Output Configurations.



OP001530

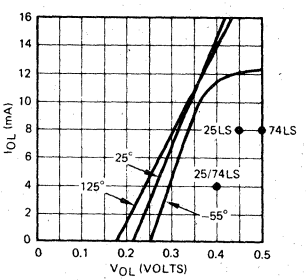
Figure 8. Typical V_{OH} for Low-Power Schottky.



OP001540

Figure 9. Typical Output Versus Input Voltage Characteristic.

The typical V_{OL} versus I_{OL} output characteristics of LS devices are shown in Figure 10. Most 74LS functions are specified at V_{OL} = 0.4V at I_{OL} = 4mA and 0.5V at 8mA. Am25LS are specified at 0.45V for I_{OL} = 8mA. Some newer designs are being guaranteed at I_{OL} of 12mA and 24mA. This curve indicates that lack of β at low temperature will not permit existing designs to be guaranteed to these higher values without severe yield loss.



OP001520

Figure 10. Typical LS V_{OL} Versus I_{OL} Characteristics.

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INPUT/OUTPUT LEVELS

Table 2 shows the guaranteed D.C. parameters of the Am54LS/74LS and second generation Am25LS families. Input current requirements (I_{IH}, I_{IL}) and therefore output drive needs (I_{OH}, I_{OL}) are significantly reduced over older TTL.

A one unit load input current at logic HIGH, I_{IH}, for Am54LS/74LS is 20μA, compared with 40μA for Am54/74 standard TTL. Similarly at logic LOW, I_{IL} is reduced to −0.36mA from −1.6mA.

Corresponding reductions in the output drive requirements are I_{OL} = 4mA vs. 16mA at V_{OL} = 0.4V and I_{OH} = −400μA compared to 800μA.

FAN-OUT CAPABILITY

The fan-out capability of a logic family indicates the number of inputs which can be driven by a single output. It is defined as the maximum output drive current divided by the input current available.

Logic HIGH Fan-out = I_{OH}/I_{IH}
Logic LOW fan-out = I_{OL}/I_{IL}

Table 3 shows the fan-out capabilities of typical functions from the three families. The lower current operating levels of LS devices allow them to be specified at a logic LOW fan-out over the commercial range of more than twice that of standard TTL (22 vs. 10). The Am25LS family allows this advantage to be extended to the military range.

D.C. NOISE MARGIN

The D.C. noise margins of digital system are defined from Figure 11 as follows:
Logic HIGH Noise Margin = $V_{OH1} - V_{IH2}$
Logic LOW Noise Margin = $V_{IL2} - V_{VOL1}$

These parameters for LS devices are shown in Table 2. LS has a minimum logic HIGH output voltage of V_{OH} = 2.5V for military and 2.7V for the commercial temperature range. For standard TTL, V_{OH} is 2.4V. V_{IH} is 2.0V for both families.

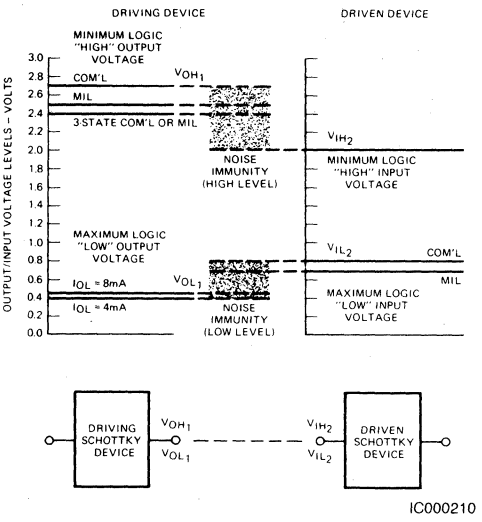

Figure 11. Input/Output Voltage Interface Conditions.

TABLE 2
COMPARISON OF TTL DC PARAMETERS

Parameters	54LS/74LS LOW-POWER SCHOTTKY					25LS LOW-POWER SCHOTTKY					Units
	Conditions		Min	Typ	Max	Conditions		Min	Typ	Max	
V_{OL}	I_{OL} = 4.0mA				0.4	I_{OL} = 4.0mA				0.4	V
	I_{OL} = 8.0mA (COM'L Only)				0.5	I_{OL} = 8.0mA (MIL, COM'L)				0.45	
V_{OH}	I_{OH} = −400μA	MIL	2.5	3.4		I_{OH} = −440μA	MIL	2.5	3.4		V
		COM'L	2.7	3.4			COM'L	2.7	3.4		
V_{IL}	Logic LOW	MIL			0.7	Logic LOW	MIL			0.7	V
		COM'L			0.8		COM'L			0.8	
V_{IH}	Logic HIGH		2.0			Logic HIGH		2.0			V
I_{IL}	V_{IN} = 0.4V				−0.36	V_{IN} = 0.4V				−0.36	mA
I_{IH}	V_{IN} = 2.7V				20	V_{IN} = 2.7V				20	μA

Parameter	54S/74S AND 25S SCHOTTKY TTL					STANDARD TTL					Units
	Condition		Min	Typ	Max	Condition		Min	Typ	Max	
V_{OL}	I_{OL} = 20mA			0.3	0.5	I_{OL} = 16mA			0.2	0.4	Volts
V_{OH}	I_{OH} = −1.0mA	MIL	2.5	3.4		I_{OH} = −300μA		2.4	3.4		Volts
		COM'L	2.7	3.4							
V_{IL}	Logic LOW				0.8	Logic LOW				0.8	Volts
V_{IH}	Logic HIGH		2.0			Logic HIGH		2.0			Volts
I_{IL}	V_{IN} = 0.5V				−2.0	V_{IN} = 0.4V				−1.6	mA
I_{IH}	V_{IN} = 2.7V				50	V_{IN} = 2.4V				40	μA

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Table 3 compares the guaranteed noise margin values for the standard TTL and LS devices. LS devices offer improved margin over standard TTL in the logic HIGH state, which is the most critical with regard to noise generation. At a similar fan-out, 10 for standard TTL and 11 for LS, noise margins in the LOW state are the same over the commercial range.

Military LS devices have a 100mV lower noise margin in the LOW state than standard TTL. In most systems, this does not present a problem as the lower power supply currents being switched with LS generally result in lower system noise generation.

The logic levels guaranteed over the operating temperature ranges are of course worst case. Figures 12 and 13 show the typical values to be considerably better than these.

Am25LS D.C. FEATURES

The D.C. advantages offered by second generation Am25LS over 54/74LS devices can be seen from Table 3 as:

1. In the logic LOW state at a fan-out of 22 (8mA), Am25LS has 50mV greater noise margin (350mV vs. 300mV).
2. Am25LS products are guaranteed at a fan-out of 22 (8mA) over the military range. Am54LS is specified at fan-out of 10 (4mA) only.
3. Am25LS offers a symmetrical fan-out of 22 in both logic HIGH and logic LOW states, allowing full use of the logic LOW drive capability.

TABLE 3
FAN-OUT AND NOISE MARGIN COMPARISON OF TTL AND LS FAMILIES.

a) LOGIC "HIGH" STATE

FAMILY	INPUT CURRENT I_{IH}	OUTPUT CURRENT I_{OH}	FAN-OUT		NOISE MARGIN	
			MILITARY	COMMERCIAL	MILITARY	COMMERCIAL
54/74	40μA	−800μA	20	20	400mV	400mV
54LS/74LS	20μA	−400μA	20	20	500mV	700mV
25LS	20μA	−440μA	22	22	500mV	700mV

b) LOGIC "LOW" STATE

FAMILY	INPUT CURRENT I_{IL}	OUTPUT CURRENT I_{OL}	FAN-OUT		NOISE MARGIN	
			MILITARY	COMMERCIAL	MILITARY	COMMERCIAL
54/74	−1.6mA	16mA	10	10	400mV	400mV
54LS/74LS	−0.36mA	4mA	11	11	300mV	400mV
		8mA	No Spec.	22	No Spec.	300mV
25LS	−0.36mA	4mA	11	11	300mV	400mV
		8mA	22	22	250mV	350mV

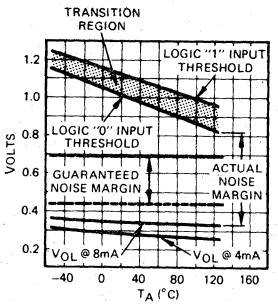

Figure 12. LS Logic "O" Noise Margin.

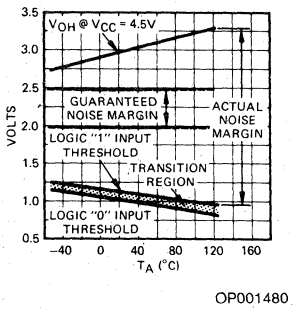

Figure 13. LS Logic "1" Noise Margin.

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3. Switching Characteristics

INTRODUCTION

Many Low-Power Schottky functions have been designed specifically to replace standard TTL elements in existing system designs. Their A.C. performance characteristics usually meet or exceed the limits of the earlier devices. The switching terms which are used on data sheets to describe the A.C. performance of these designs are summarized in Table 4. The more important parameters are discussed in detail in this section.

TABLE 4.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.3V logic level unless otherwise noted.)

f_{MAX}	The highest operating clock frequency.
t_{PLH}	The propagation delay time from an input change to an output LOW-to-HIGH transition.
t_{PHL}	The propagation delay time from an input change to an output HIGH-to-LOW transition.
t_{PW}	Pulse width. The time between the leading and trailing edges of a pulse, measured at the 50% points.
t_r	Rise time. The time required for a signal to change from 10% to 90% of its measured values.
t_f	Fall time. The time required for a signal to change from 90% to 10% of its measured values.
t_s	Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.
t_h	Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.
t_{HZ} also t_{PHZ}	HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).
t_{LZ} also t_{PLZ}	LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).
t_{ZH} also t_{PZH}	Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.
t_{ZL} also t_{PZL}	Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

PROPAGATION DELAYS

The standard designations for delays through combinatorial logic networks are t_{PHL} and t_{PLH}. A delay from an input change to an output going LOW is called t_{PHL}, while t_{PLH} is the delay from an input change to an output going HIGH.

Figure 14 shows a typical waveform with the output changing during the interval indicated by the diagonal, sloping line. Note that all switching times shown are measured at the 1.3 volt logic level.

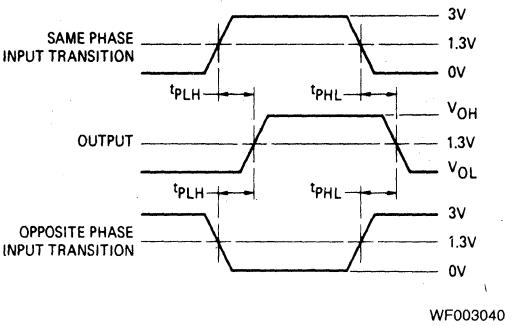

Figure 14. Propagation Delay.

Typical values for a single gate propagation delay t_{PHL} in Low-Power Schottky functions are 8–10ns into a 15pF load. Higher performance LS families such as Am25LS, exhibit delays in the 4 – 6ns range. These propagation delays will increase by 2 – 4ns at an output loading of 50pF or approximately 0.1ns per pF.

EDGE RATES

The rise and fall times of Low-Power Schottky devices are similar to those of standard TTL. Into a 50pF load fall time, t_f, is typically 6–8ns, while rise time, t_r, is in the 9–12ns range. A.C. parameters are measured at $t_f \leqslant 6$ns and $t_r \leqslant 15$ns.

As with standard TTL, careful P.C. board layout rules should be employed to avoid problems which can occur at these relatively fast edge rates. In particular, precautions should be taken to insure that transmission line effects do not cause false switching or ringing and oscillation problems on lines longer than 18 inches. See Section 4 for more information.

SEQUENTIAL DEVICES

Set-up time, t_s, hold time, t_h, are the most important parameters for specifying sequential elements such as latches, flipflops and registers.

For these synchronous devices, inputs must be stable for a certain period of time before the clock or enable pulse. This interval is the region in time during which devices are "sampling" their inputs. As an example, consider a latch with a D input and an active LOW clock. The latch will store the information present on its input just before the clock goes HIGH. The question is, how long does the input level have to be present and stable before the clock goes HIGH? A particular device will "sample" its input at some exact instant, but in a group of devices some are slower than others. The result is an interval of some time called set-up time during which all devices, fast or slow, will "sample" their inputs.

All devices exhibit a hold time. That is a period of time after the clock or enable pulse transition during which the data cannot be changed without loss of input intelligence. This hold time occurs after the clock goes HIGH. Figure 15 shows the input requirements and definitions for data entry.

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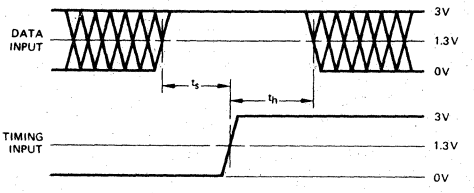

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Figure 15. Set-up and Hold Time Definitions.

f_{MAX}

A frequently misunderstood parameter on data sheets is maximum clock frequency f_{MAX}. This was defined by the early TTL manufacturers as the maximum toggle frequency which can be attained by the device under ideal conditions with no constraints on t_r, t_f, pulse width, or duty cycle. Although f_{MAX} as specified cannot usually be attained in an operating system, it is a relatively easy parameter to test and provides a convenient measure of comparative performance between different devices.

EFFECTS OF TEMPERATURE AND POWER SUPPLY VARIATIONS

Standard TTL devices exhibit severe degradation in A.C. performance at the recommended limits of the operating temperature and power supply voltage ranges.

At elevated temperature and/or high V_{CC} levels, charge storage begins to slow down A.C. response. At the other extreme, low temperature and/or low V_{CC}, the loss of β causes a similar problem. These combined effects can cause more than 50% degradation in performance over the full military temperature and power supply extremes.

Low-Power Schottky technology reduces the impact of both of these effects on performance. β degradation at cold temperatures is far less severe and Schottky clamping largely eliminates the effects of charge storage at high temperature.

TABLE 5. GUIDELINES FOR TYPICAL VARIATION OF A.C. PARAMETERS WITH COMBINED TEMPERATURE AND V_{CC} VARIATION

Temperature Range	V_{CC} Variation (Nominal 5V)	AC Derating Factor	
		System	Component
COM'L, 0°C to +70°C	None	5%	10%
COM'L, 0°C to +70°C	±0.25V	15%	30%
MIL, −55°C to +125°C	None	15%	30%
MIL, −55°C to +125°C	±0.5V	25%	50%

The system's designer would like a factor which will allow his system to meet specification with minimum design overkill. However, the component engineer often requires maximum delays to be guaranteed. For system design guidelines, the AC derating factors of Table 5 may be useful.

It must be emphasized that the values of Table 5 are typical. However as it is unlikely that any given system will contain all worst case devices they will usually yield a fairly safe prediction of the system performance which can be achieved.

Individual components will of course be slower than these typical numbers. These must be reflected on procurement specifications. A general rule of thumb would be to double the system design guidelines of Table 5. Am25LS specifications are published with worst case parameters guaranteed over the operating power supply and temperature ranges, as well as at a realistic system load condition of 50pF. A typical example of this format is shown in Table 6.

SHORT CIRCUIT OUTPUT CURRENT

To improve performance, in 1975 TI lowered the short-circuit current limiting resistor value. This increased the I_{SC} (I_{OS}) range from −6 to −42mA up to −30 to −130mA. The overall delay when driving very large capacitive loads (> 150pF) was reduced somewhat as a result. However, the inherent circuit performance still dominates in normal applications such that the Am25LS and other high performance families remain faster even when driving large capacitive loads.

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TABLE 6
Am25LS2513 THREE-STATE PRIORITY ENCODER
A.C. SPECIFICATION FORMAT FOR V_{CC} AND TEMPERATURE EXTREMES AND 50pF LOAD CONDITION

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\overline{I}_i$ to An (In-phase)	C_L = 15 pF, R_L = 2.0 kΩ		17	25	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{I}_i$ to An (Out-phase)			11	17	ns
t_{PHL}				12	18	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			7.0	11	ns
t_{PHL}				24	36	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			11	17	ns
t_{PHL}				23	34	
t_{PLH}	$\overline{EI}$ to An			12	18	ns
t_{PHL}				14	21	
t_{ZH}	G_1 or G_2 to An			23	40	ns
t_{ZL}				20	37	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			20	30	ns
t_{ZL}				18	27	
t_{HZ}	G_1 or G_2 to An	C_L = 5.0 pF, R_L = 2.0 kΩ		17	27	ns
t_{LZ}				19	28	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			16	24	ns
t_{LZ}				18	27	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

			COMMERCIAL		MILITARY		
			Am25LS		Am25LS		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	$\overline{I}_i$ to An (In-phase)	C_L = 50 pF, R_L = 2.0 kΩ		31		37	ns
t_{PHL}				30		34	
t_{PLH}	$\overline{I}_i$ to An (Out-phase)			22		27	ns
t_{PHL}				22		25	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			15		18	ns
t_{PHL}				48		60	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			19		21	ns
t_{PHL}				46		57	
t_{PLH}	$\overline{EI}$ to An			22		25	ns
t_{PHL}				27		32	
t_{ZH}	G_1 or G_2 to An			42		49	ns
t_{ZL}				43		49	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			36		43	ns
t_{ZL}				35		43	
t_{HZ}	G_1 or G_2 to An	C_L = 5.0 pF, R_L = 2.0 kΩ		34		40	ns
t_{LZ}				34		40	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			30		35	ns
t_{LZ}				31		35	

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4. Design Guidelines

POWER SUPPLY CONSIDERATIONS

The recommended power supply voltage (V_{CC}) for all TTL circuits, including LS, is +5V. Commercial temperature range devices, designated 74LS or in the case of Am25LS with the suffix C, are specified with a ±5% supply tolerance (±250mV) over the ambient range 0°C to 70°C. Military range parts, designated 54LS or in the case of Am25LS with the suffix M, are guaranteed with a ±10% supply tolerance (±500mV) over an ambient temperature range of −55°C to +125°C. The power supply should be well regulated with a ripple less than 5% and with regulation better than 5%. Even though LS devices generate significantly smaller power supply spikes when switching than standard TTL, on-board regulation is still preferable to isolate this noise to one board.

A low-inductance transmission line power distribution bus with good RF decoupling is necessary for large systems. On all boards, ceramic decoupling capacitors of 0.01μF to 0.1μF should be used at least one for every five packages, and one for every one-shot (monostable), line driver and line receiver package. In addition, a larger tantalum capacitor of 20μF to 100μF should be included on each card. On boards containing a large number of packages, a low impedance ground system is essential. The ground can either be a bus or a ground which is incorporated with the V_{CC} supply to form a transmission line power system. Separate power transmission systems can be attached to the board to provide this same feature without the cost of a multi-layer PC card.

UNUSED INPUTS

An unused input to an AND or NAND gate should not be left floating as it can act as an antenna for noise. On devices with storage, such as latches, registers and counters, it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. This technique optimizes switching speed as the distributed capacitance associated with the floating input, bond wire and package leads is eliminated. To terminate, the input should be held between 2.4V and the maximum input voltage. One method of achieving this is to connect the unused input to V_{CC}. Most LS inputs have a breakdown voltage >7V and require no series resistor. Devices specified with a maximum 5.5 volt breakdown should use a 1kΩ to 10kΩ current limiting series resistor to protect against V_{CC} transients. Another method is to connect the unused input to the output of an unused gate that is forced HIGH. Do not connect an unused input to another input of the same NAND or AND function. Although recommended for standard TTL, with LS this increases the input coupling capacitance and reduces A.C. noise immunity.

TRANSMISSION LINE EFFECTS

The relatively fast rise and fall times of Low-Power Schottky TTL (5 to 15ns) can cause transmission line effects with interconnections as short as 18 inches. With one TTL device driving another and the driver switching from LOW to HIGH, if the propagation delay of the interconnection is long compared to the signal rise time, the arrangement can behave like a transmission line driven by a generator with a non-linear output.

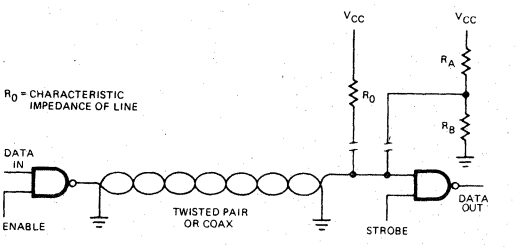
The initial voltage step at the output, just after the driver has switched, propagates down the line and reflects at the end. In the typical case where the line is open ended or terminated in an impedance greater than its characteristics impedance (Z_{OL}), the reflected wave arrives back at the source and increases V_{OUT}. If the total round-trip delay is longer than the rise time of the driving signal, a staircase response results at the driver output and along the line. If one of the driven devices is connected close to the driver, the initial output voltage (V_{OUT}) seen by it might not exceed V_{IH}. The state of the input is undetermined until after the round trip of the transmission line, thus slowing down the response of the system.

The longest interconnection that should be used with LS devices without incurring problems due to line effects is in the 10-12 inch range.

With longer interconnections, transmission line techniques should be used for maximum speed. Good system operation can be obtained by designing around 100 ohm lines. A 0.026 inch (0.65mm) trace on a 0.062 inch epoxy-glass board ($E_r = 4.7$) with a ground plane on the other side represents a 100Ω line. 28 to 30 gauge wire (0.25 to 0.30mm) twisted pair line has a characteristic impedance of 100 to 115Ω.

LINE DRIVING AND RECEIVING

For lines longer than 2 feet, twisted pairs or coaxial cable should be used. The characteristic impedance of the transmission media should be approximately 120Ω such as twisted pairs of #26 wire or 100Ω coax. A possible choice is cables with a characteristic impedance R_O of 100Ω such as ribbon cable or flat cable with controlled impedance. Resistive pull-ups at the receiving end can be used to increase noise margin. Where reflection effects are unacceptable, the line must be terminated in its characteristic impedance. A method shown in Figure 16 has the output of the line tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. As the output impedance of the LS driver is low and must sink the current through it, in addition to the current from the inputs being driven, a useful technique is to terminate the line in a voltage divider with two resistors, each twice the line impedance.



$$R_A = R_B = 2Z_O$$
$$R_A = Z_O$$

Figure 16. LS Driving Twisted Pair.

This reduces the extra sink current by 50%. Where the line exceeds five feet in length it is preferable to dedicate gates solely to line driving.

For additional noise immunity when driving long lines, a differential line driver and line receiver may be used. These dedicated line interface circuits drive a twisted pair of wires differentially, permit easy termination of lines and provide excellent common mode noise rejection.

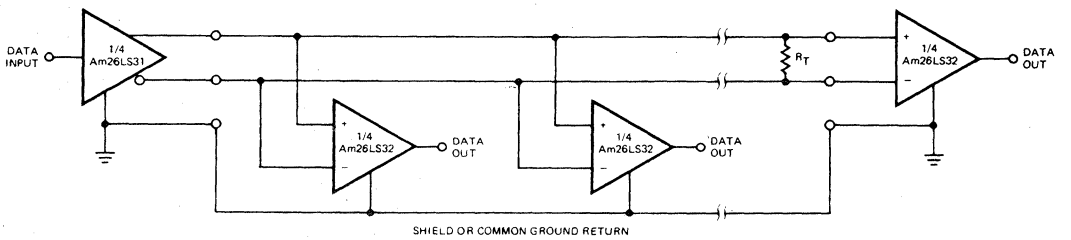
The Am26LS31 driver and Am26LS32 and Am26LS33 are quad differential line drivers and receivers satisfying the interface requirements of EIA RS-422 and 423 as well as military applications, Figure 17. They are designed to operate off the standard 5V power supplies of the LS logic devices. More applications information on line termination techniques is provided on the above mentioned device data sheets.

Refer to Page 13-1 for Essential Information on Military Devices

CROSS-TALK AND RINGING

These two problems may be experienced with all forms of high speed digital logic. Crosstalk is the coupling of energy from one circuit to another via real or parasitic capacitance and inductance. Ringing is the possible rebound of the signal into the input threshold region (0.8 – 2.0V) following a HIGH-to-LOW level change. When a driver switches from a HIGH-to-LOW state the output voltage should fall below the threshold value. However, a line having a very low characteristic impedance does not allow transistor Q5 in the NAND gate example to saturate, and the resulting output voltage may not be low enough to switch an adjacent device until two or more line delay times. The low current levels at which LS devices operate, coupled with the low output impedance in both HIGH and LOW Logic states, minimize crosstalk effects. Input clamp diodes provided on all LS devices are extremely effective in reducing ringing phenomenon.

Care should be taken to insure that signals with falling edges faster than 2.5-3ns/volt are not coupled into the input of an LS function. Even though the signal may not pass into the threshold region, if the pulse edge is fast enough, sufficient energy may be capacitively coupled onto a sequential device to cause it to change state: High speed Schottky elements in a test setup can exceed this limit. However in an active system, the edges will generally be slowed sufficiently to eliminate any problem.



AF001890

Figure 17. Differential Line Driving and Receiving with the Am26LS31 and Am26LS32.

DEFINITION OF STANDARD TERMS

DEFINITION OF A.C. SWITCHING TERMS

(All switching times are measured at the 1.3V logic level for Low-Power Schottky and the 1.5V logic level for Schottky unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

DEFINITION OF D.C. TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input

O Output

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

I_{OZH} Three-state off-state output current, HIGH-level voltage applied.

I_{OZL} Three-state off-state output current, LOW-level voltage applied.

V_{CC} The range of supply voltage over which the device is guaranteed to operate.

V_{IL} The guaranteed maximum input voltage that will be recognized by the device as a logic LOW.

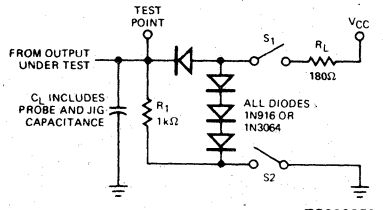
V_{IH} The guaranteed minimum input voltage that will be recognized by the device as a logic HIGH.

V_{OL} The maximum guaranteed logic LOW voltage at the output terminal while sinking the specified load current I_{OL}.

V_{OH} The minimum guaranteed logic HIGH voltage at the output terminal when sourcing the specified source current I_{OH}.

PARAMETER MEASUREMENTS

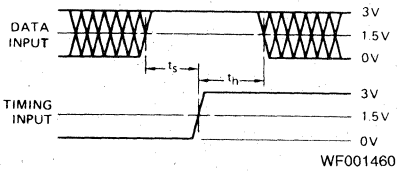
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



TC000350

Note: For standard totem-pole outputs, remove R_1. S_1 and S_2 closed.

SET UP, HOLD, AND RELAESE TIMES



WF001460

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

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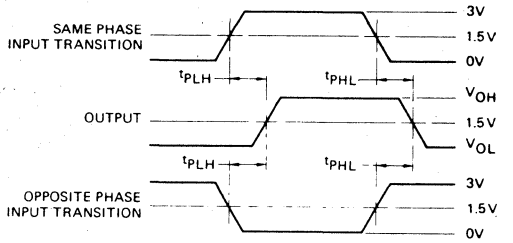
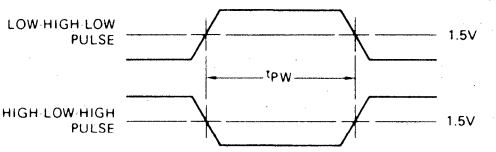
PROPAGATION DELAY



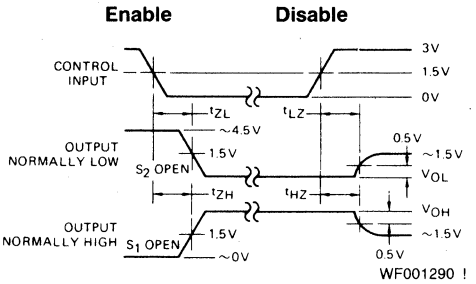
WF001420

PULSE WIDTH



WF001270

ENABLE AND DISABLE TIMES



WF001290 !

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns for Schottky.
Rate $\leq$ 1.0MHz; $Z_0 = 50\Omega$; $t_r \leq 15$ns; $t_f \leq 6$ns for Low-power Schottky.

Refer to Page 13-1 for Essential Information on Military Devices

Am2900 Components Continuously Become Faster and Faster

MORE SPEED: NO MORE POWER

There's a good old tried and proven way to make faster IC's — burn more power. (That's the only real difference between "LS" and "S" devices). But that solution isn't satisfactory for LSI devices like the Am2900 Family. Power is constrained to existing levels for reliability reasons.

Am2900 parts are always designed to obtain the maximum speed at a power level which is safe for the package types and operating environment of the part. To increase speeds, new technologies must be used to build faster components at no increase in power.

NEW CIRCUIT DESIGN TECHNIQUES MAKE FASTER GATES

One way to make faster components is to use new circuit design techniques. The most obvious is internal ECL, which provides very fast gates at similar power levels to LS TTL. The Am29116 reaches microcycle times of 100ns through the use of internal ECL. Other design techniques, such as low-level logic (with very small logic swings on-chip), can also provide higher speeds without introducing the time penalty of ECL to TTL conversion.

Finally, very low power gates used in non-critical speed paths make more power available for use in critical speed paths. As the 2900 Family develops, all these technologies will be used within a single component to achieve the highest speeds without increasing power. The Am2903A is one of the first products to take advantage of this mixed circuit technology.

IMPROVED PROCESS CONTROL ALLOWS TIGHTER SPECS

Today's 2900 parts are carefully characterized over a wide range of voltages, temperatures, and process parameters before an AC specification is published. As manufacturing technology improves, the process is subject to smaller run-to-run variations, so that all of the product is closer to design nominal. This makes it possible to specify parameters more closely to typical without incurring large yield losses. The first product reflecting this is the Am2903.

WHAT'S GOOD FOR THE GOOSE IS GOOD FOR THE GANDER

Many new tools in production technology are emerging, primarily spurred by the emphasis on high-speed MOS memories. The same tools, such as projection masking, also provide for smaller geometries in bipolar circuits. As MOS gets faster, so does bipolar. The Am2901C obtains its speed improvement over the Am2901B through these tools.

PROCESS TECHNOLOGY TAKES A QUANTUM LEAP

Current generation LSI/VLSI bipolar devices call for state-of-the-art processing technologies. IMOX™ ion-implanted micro-oxide technology gives the Am2901C its performance improvement over the Am2901B. IMOX also generates incredible packing densities – the Am29116 has 2500 gates on a single bipolar chip!

DESIGN FOR THE FUTURE

Every Am2900 part will undergo an evolution as new technologies become practical for production. Every part type will continuously become faster. The results are easy to observe – increases in performance at no additional cost (see Figure 1).

Most existing 2900 designs can be offered in higher performance versions simply by substitution of the 2901C for the 2901B, the 2909A for the 2909, and 2903A for the 2903, and so forth. Your 2900 design won't run out of speed in a few years. Advanced Micro Devices' 2900 Family will serve tomorrow's needs as well as today's.

Figure 1. Price/Performance Improvements

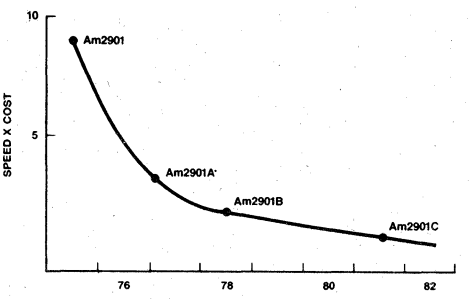


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Figure 2. Bipolar Speed/Density Improvements

Am2901 FOUR-BIT MICROPROCESSOR SLICE

540 GATES 800mW 40-PIN DIP

DIE SIZE	Am2901 33,000 MILS^2	Am2901A 20,000 MILS^2	Am2901B 15,000 MILS^2	Am2901C 15,000 MILS^2
SPEED A, B→G, P	80ns	65ns	50ns	37ns
TECH-NOLOGY	LOW-POWER SCHOTTKY	DUAL LAYER METAL ION-IMPLANTATION	PROJECTION PRINTING	ECL INTERNAL TTL I/O IMOX
	1975	1977	1978	1981

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INTRODUCTION

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems — circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

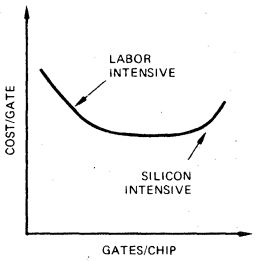

Figure 1.

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product — it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

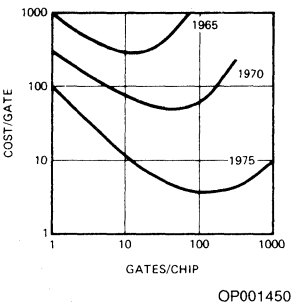

Figure 2.

GENERATION I — SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10–20 each. The circuits were useful in many systems. They consisted of gates — 7400, 7410, 7420 — and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II — MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20–50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic was around 500 gates chip.

GENERATION III — The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions was needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

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The Am2900 Family includes circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast — utilizing Low-Power Schottky TTL technology and AMD's proprietary IMOX™ technology; they are expandable; they are flexible — useful in emulation; and they are driven under microprogram control.

IMOX AND ECL — THE NEXT STEP

Ever increasing complexity placed greater and greater demands on existing process technologies. Advanced Micro Devices responded to this challenge by introducing its revolutionary IMOX ion-implanted micro-oxide technology in 1980. Oxide isolation generated faster transistor switching and tighter packaging. Ion-implantation meant tighter parameter control and lower power consumption. The bottom line — an unequalled combination of speed and density culminating in the Am29116 with a staggering 2500 gates-per-chip. Figure 3 shows this climb in gate density.

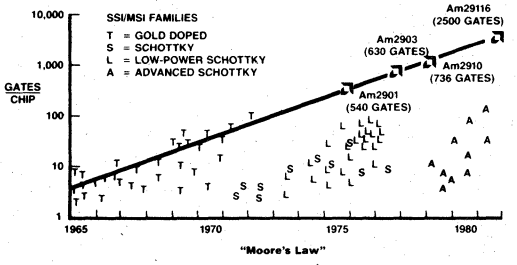

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Figure 3. Am2900 Bipolar LSI/VLSI

Future refinements of IMOX and new device technologies will keep AMD on the leading edge in bipolar LSI/VLSI. Designed to take advantage of these improvements in process technology, a new family of microprogrammable 32-bit controller products will set the pace for bipolar VLSI in the mid-1980s.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am8086.

While an Am8086 can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am8086 design will, therefore, almost always be cheaper. But the Am8086, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, e.g., sixteen bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10–100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform — reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 4 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901C array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901Cs), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901C registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901Cs and sent out to the memory address register (MAR). The four status bits from the 2901Cs ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909A, 2910A, or 2911A is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901C instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901C array (see Figure 19, 2901C data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or an 8086 instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 4 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located — the μPC, the stack, or the direct inputs — and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two.

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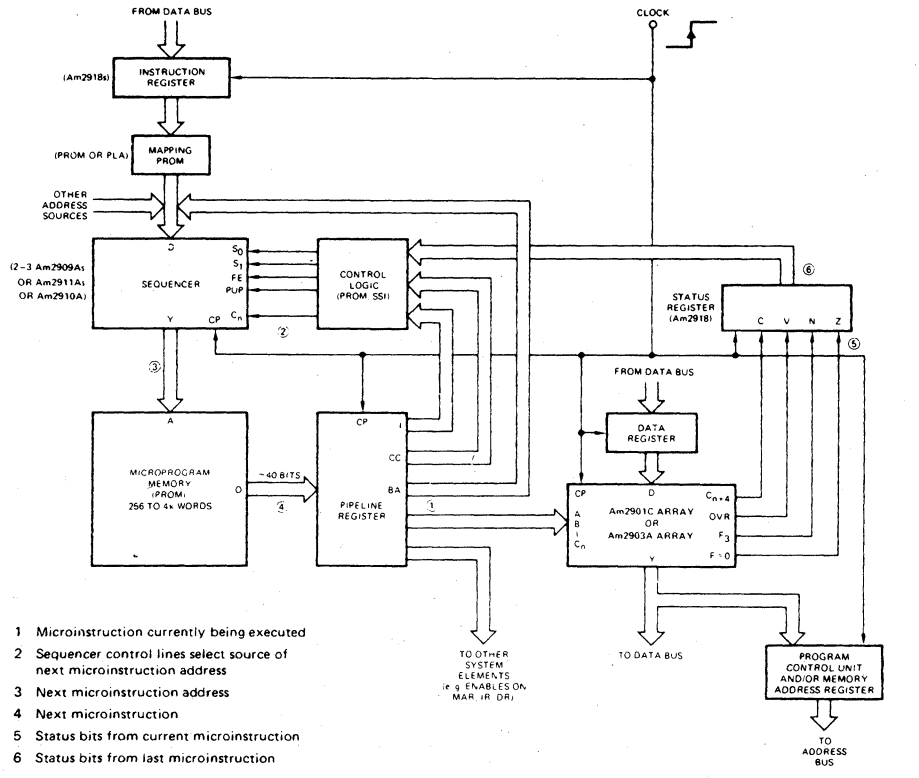
The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 4.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901Cs are executing one instruction, the next instruction is being fetched from ROM.

Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901Cs. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

Figure 4.



The system shown in Figure 4 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901C working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.

Am29100 High-Performance Controller Products

A BETTER WAY IS HERE

A new family of products from Advanced Micro Devices makes high-performance controller design a snap.

MICROPROGRAMMING; BEST FOR COMPUTERS, BEST FOR CONTROLLERS

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high-speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low-speed applications, but when the demand for speed and intelligence goes up, they cannot keep pace. Controllers need something better: the 29100 Family.

The 29100 Family products have been designed from the ground up with peripheral control applications in mind. They are fast, they are optimized for bit-manipulation, character handling, data communication and long, sophisticated microprograms and they are designed to work together in a system.

FAST LIKE YOU'VE NEVER HAD

The central element of our new high-speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a slice – it's a complete 16-bit processor, with three-input ALU, 32 scratchpad registers, an accumulator, data latch, barrel shifter, priority encoder and status register with conditional code generation logic. But the Am29116 is far more than a very fast number cruncher – it's been optimized for controller-oriented applications. It's instruction set has instructions often needed in controllers that are not available in any other processor.

A WHOLE FAMILY OF FAST LSI CONTROLLER PARTS

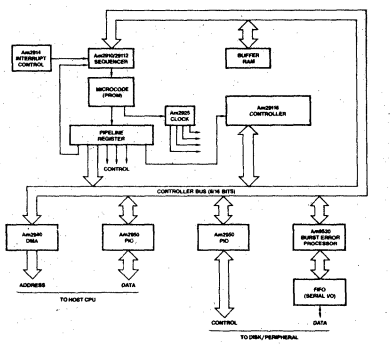
There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

TYPICAL CONFIGURATION USING THE 2900 CONTROLLER FAMILY

A typical intelligent controller configuration is shown below. The basic controller consists of the Am29116, a microprogram control unit and a high-speed buffer memory. Each microinstruction includes: a) a 16-bit instruction field to the Am29116, b) next-microinstruction selection bits, c) control for the buffer memory, d and e) control for the interface circuits and f) possibly an 8 or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.

HIGH-PERFORMANCE INTELLIGENT CONTROLLER



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The Am29500 Family

A High-Performance Architecture
For Digital Signal/Array Processing

The new system designs of the '80s will continue to press the performance limits of technology. Parallel processing and pipelined architectures will become the standard approach. The new architectures are best implemented with a chip set that has been designed from the ground up with high speed array processing in mind.

The Am29500 Family is designed specifically for these new architectures. Every key product feature supports the system end objective of maximum performance and flexibility. These include:

- Microprogrammable, parallel functions
- Pipeline organization used throughout
- IMOX™ process and ECL internal structures
- TTL I/O for easy interfacing

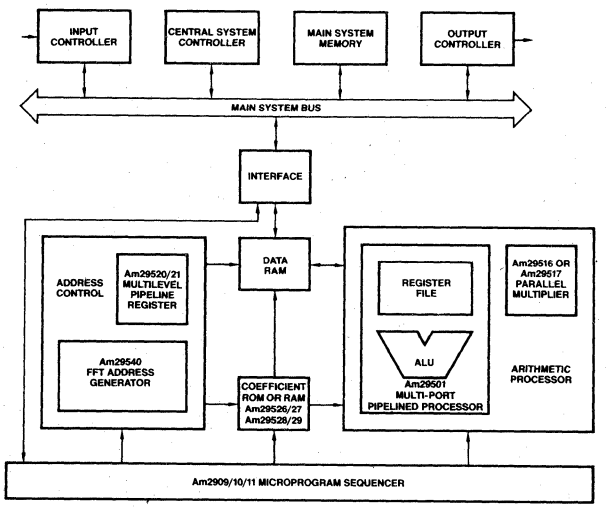
The first members of the family are targeted for the efficient execution of DSP and array processing algorithms. The most common algorithms include Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) digital filters and Fast Fourier Transform (FFT) processors.

The first major building blocks are designed to support maximum performance signal processing applications.

Included are:

- **Am29501 Multi-Port Pipelined Processor**
  A specialized parallel processor which executes multiple simultaneous data operations. Its Register/ALU structure provides the key functional element for a high performance signal processing system. Eight-bit slice!
- **Am29540 FFT Address Sequencer**
  This algorithm-specific VLSI chip generates data and coefficient addresses for the Fast Fourier Transform. It supports a wide variety of FFT algorithms in either radix-2 or radix-4.
- **Am29516/29517 High Speed 16 x 16-Bit Parallel Multipliers**
  Both are 16 x 16-bit Parallel Multipliers. The Am29516 is pin and functionally compatible with the MPY-16HJ, but with an added multiplexer to output the LSP at the MSP port. The Am29517 is the same function, but with clock enables for microprogrammed applications.
- **Am29520/29521 Multilevel Pipeline Registers**
  Both devices contain four 8-bit registers for dual two-stage (FFT butterfly) or single four-stage (general purpose) data or address pipelining. Combined load-and-shift (Am29520) or separate load-and-shift (Am29521) control options are available.
- **Am29526/29527/29528/29529 High-Speed Sine/Cosine Function Generators**
  The sine and cosine functions are necessary for Fast Fourier Transforms (FFT). The Am29526/527 generate the most significant and least significant byte of the 16-bit sine function and the Am29528/529 generate the most significant and least significant byte of the 16-bit cosine function. The sine and cosine functions are generated to provide a range of θ for a half cycle, $0 \leqslant \theta \leqslant \pi$, in increments of $\pi/2048$. All four units have a 50ns maximum commercial generation time.

HIGH PERFORMANCE SIGNAL PROCESSOR



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A high-performance signal processor may be constructed as shown in the diagram. The processor is built entirely with new Am29500 digital signal processing and Am2900 devices. Such a processor is attached as a slave to the main system bus to perform the multitude of arithmetic operations which prevail in DSP algorithms.

Using this architecture it is possible to implement a radix-2 FFT butterfly in four instruction cycles. This allows a 1024-point complex FFT to be performed in approximately 2ms.

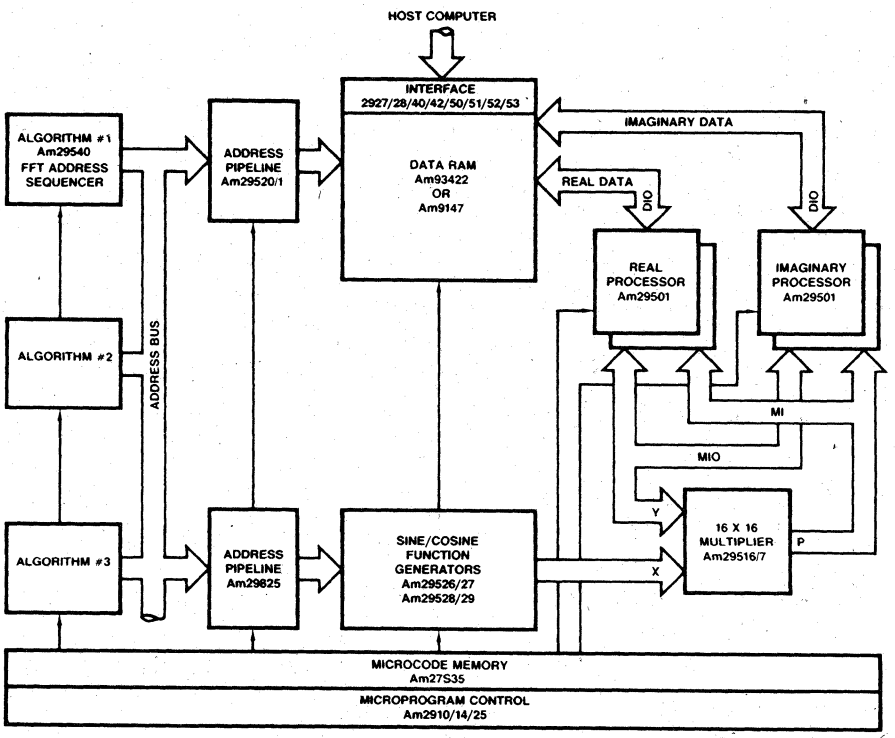
Fast multiplication is the key to high-speed digital-signal processing and high-speed array processing. In addition to the Am29516 and Am29517, Advanced Micro Devices is developing an extensive family of multipliers. The first addition to the high-performance multiplier group:

- Am29510 High-Performance 16 x 16 Bit Multiply Accumulator
  The multiply accumulator provides single cycle multiply accumulation or subtraction. The Am29510 is a pin- and function-compatible alternate source for the TRW TDC1010J. As illustrated with the Am29516/517, the multiply accumulator will have a speed improvement over existing multiply accumulators.
- Am295XX to be announced.

  –*More Multipliers*
  A proliferation of the existing multiplier architectures will generate a complete family of multipliers and multiplier accumulators.

  –*Floating Point Processors* (FPP)
  A 32-bit FPP capable of performing single-cycle double-precision floating-point addition, subtraction, and multiplication. The FPP performs the arithmetic operations in DEC or IEEE format. Available 1984.

Am29500 ARRAY PROCESSOR



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Am2960-70 Memory Support Family System Overview

Memory system designs are increasingly shaped by three requirements:

1. Higher system performance
2. More memory capacity in less space
3. Increased reliability

The Am2960-70 Memory Support Family is a family of LSI building blocks which excels in satisfying these three requirements and provides a complete systems solution for designs using 64K or 256K DRAMS. The family members include:

Am2960 Error Detection and Correction Unit
Am2961/62 EDC Bus Buffers
Am2964B Dynamic Memory Controller (64K DRAM Version)
Am2965/66 Dynamic RAM Drivers
Am2968 Dynamic Memory Controller (256K DRAM Version)
Am2969 Timing Controller
Am2970 Timing Controller
Am8163/67 System and Timing Controller for MOS MPUs

These are general purpose products. They will support any suppliers' DRAMs and will work with any processor type: 8086, 80186, 80286, 68000, Z8000, and Am2900 processors. They may also be used to support word widths of any size from 8 bits to 64 bits.

Figure 1 shows the system interconnection for a typical memory system for 256K DRAMs, and Figure 2 shows the system interconnection for a typical memory system using 64K DRAMs. In both cases, the memory support subsystem interfaces to the System Data Bus, Address Bus, and control signals. Also, in both cases all, or almost all, of the memory support functions are handled by AMD LSI devices. This simplifies the design of the memory system and, more importantly, allows the board space available for DRAMs to be maximized because the LSI solution for control and error correction is very compact.

ERROR DETECTION AND CORRECTION

It is important that memory systems function reliably. The number of bytes of storage is increasing rapidly in memory systems at the same time that the density of the MOS DRAMs is growing. With 64K and 256K DRAMs, alpha particle sensitivity is much greater than that of smaller DRAMs because of the reduced size of the memory cells and the smaller stored charge of the cell. A Technical Report follows the Am2960 data sheet in this section and is entitled "Am2960 Boosts Memory Reliability." This technical report gives some statistics on soft error rates for DRAMs and demonstrates the dramatic increase in memory reliability gained from the use of Hamming Code Error Detection and Correction schemes, such as those used by the Am2960 EDC (Error Detection and Correction) unit.

Data interface between the dynamic memories, the Am2960 EDC chip and the system data bus is accomplished by means of the Am2961/62 bus buffers. Figure 3 depicts the architecture of these devices along with a simplified block diagram of the Am2960. The Am2961 is inverting between the system data bus and the EDC bus while the Am2962 is noninverting. As shown in Figure 3, the Am2961 and Am2962 contain two internal latches, a multiplexer, and a RAM driver output buffer.

These devices feature 4-bit-wide data paths to and from the RAM, the EDC, and the system data bus. The bus-input (BI) latch is used predominantly in byte WRITE operations, so that an incoming byte from the system data bus can be stored while the memory is being read, and any necessary correction made in the bytes not being changed. The bus-output (BO) latch is used predominantly for storing the output data if the processor is in the single-step mode. In the single-step mode it is necessary to hold the output data on the system data bus, but the memory must be released for refresh.

The Am2960 Error Detection and Correction Unit contains all the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code and to correct the data word when check bits are supplied. Operating on the data read from memory, the Am2960 will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for data logging.

The Am2960 also features two diagnostic modes in which diagnostic data can be forced into portions of the device to simplify device testing and to execute system diagnostic functions.

The 16-bit Diagnostic Latch is loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. It contains check bit information in one byte and control information in the other, and is used for driving the device when in the Internal Control mode, or for supplying check bits when in one of the Diagnostic modes.

The control logic determines the specific operating mode. Normally the control logic is driven by external control inputs; however, in the Internal Control mode, the control signals are instead read from the Diagnostic Latch.

The Am2960 is a very fast EDC device, but even faster versions will soon be available. A speed selected version, the Am2960-1, is described in the Am2960 data sheet, and an IMOX™ version, the Am2960A, will be available by early 1985. All speed-improved versions have identical functions and are electrically plug-compatible with the current Am2960.

MEMORY SYSTEM CONTROL AND TIMING

Two Dynamic Memory Controllers are available for generating address, $\overline{RAS}$, and $\overline{CAS}$ signals for memory banks. The Am2964B is designed to work with 64K DRAMs of which each device can handle up to four banks for a total control capacity of 256K words. The new Am2968 is designed to work with 256K DRAMs and can also handle up to four banks for a total control capacity of 1 Megaword (the words

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can be as many bits wide as desired). Also, the Am2968 does not require external driver chips as does the Am2964B – the Am2968 has the memory drivers, with all of the undershoot control and speed features of the Am2965/66, built right into its address, $\overline{RAS}$, and $\overline{CAS}$ outputs.

For generating the timing and control signals required by the Am2964B/68 and the Am2960/61/62, there are several different devices available, optimized for different system requirements. For MOS Microprocessor systems, use the Am8163 or Am8167. Both of these devices will interface

Figure 1. Am2900 High Performance Memory Subsystem Using 256K DRAMs

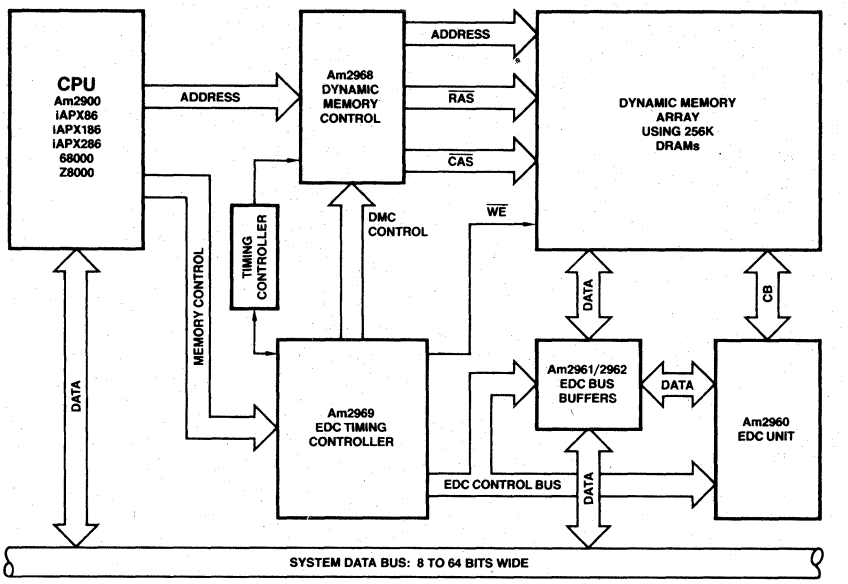

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Figure 2. Am2900 High Performance Memory Subsystem Using 64K DRAMs

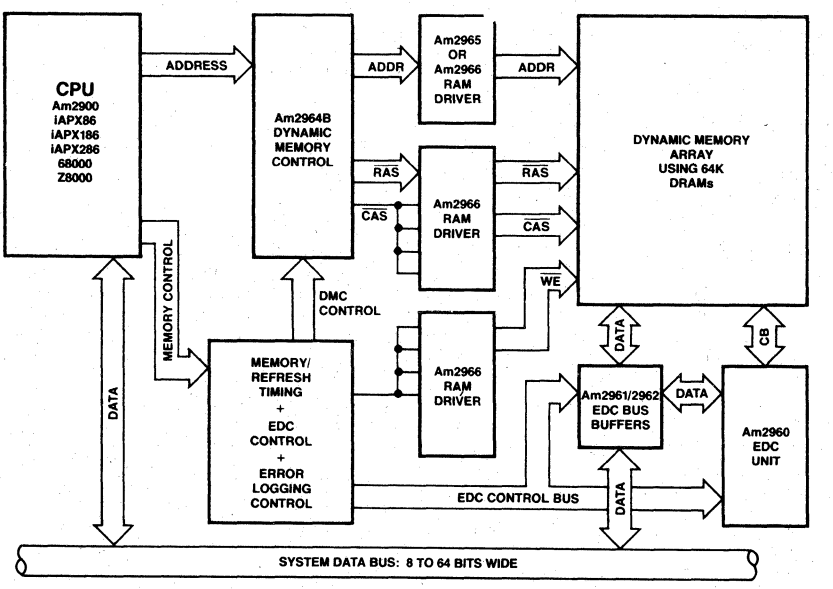

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Figure 3. EDC Data Path

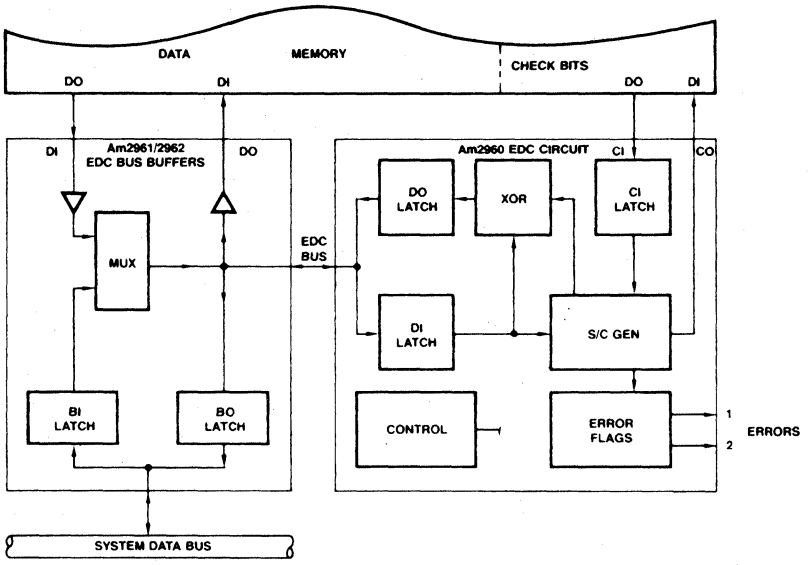

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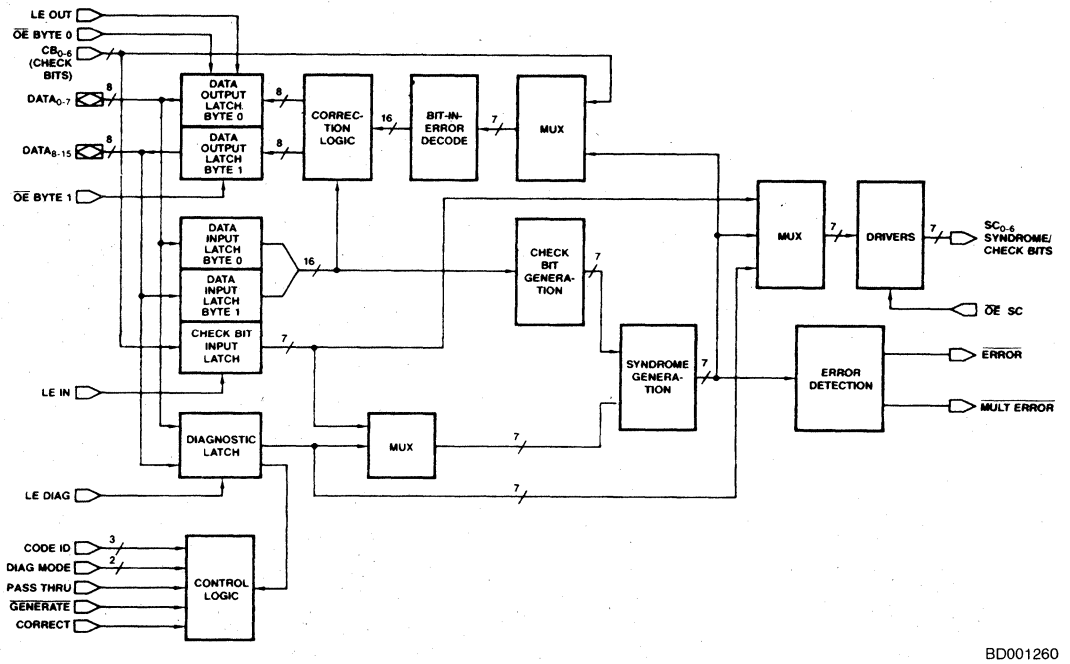
Figure 4. Am2960 Block Diagram



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easily to iAPX86/186/286, Z8000, or 68000 microprocessors. The Am8163 and Am8167 provide the control signals and timing signals for the memory controllers, the EDC, and the data bus buffers – in addition, the Am8163/67 decode the memory system control signals directly from the MOS Microprocessor, requiring in most cases only a single PAL™ for interfacing.

For high-performance Am2900-based processors or other high-speed processor designs, use the Am2969 or Am2970 to generate timing and control signals.

Following is a description of the function of the Am2964B/65/66 for Dynamic Memory Control for 64K DRAMs. The Am2968 incorporates these features and more into a single IC for use with 256K DRAMs.

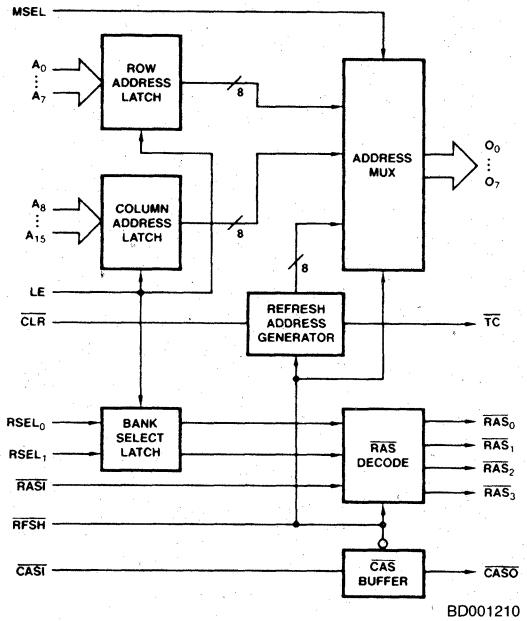
The Am2964B Dynamic Memory Controller is used to provide all address handling, as well as $\overline{RAS}$ and $\overline{CAS}$ decoding and control. A block diagram of the Am2964B Dynamic Memory Controller is shown in Figure 5. The device contains 18 input latches for capturing an 18-bit address for memory control; the two highest order addresses are decoded in the Am2964B to select one of four banks of RAM by selecting one of the four $\overline{RAS}$ outputs.

The Am2964B is designed to operate with either 16K Dynamic RAMs or 64K Dynamic RAMs. Thus, the designer either uses 14 of the multiplexer address inputs and 7 of the address outputs or all 16 of the multiplexer address inputs and all 8 of the address outputs as needed by the memory. In the case of 16K Dynamic RAMs, 7 address inputs are provided to the RAM during the $\overline{RAS}$ LOW signal, and then the 8-bit multiplexer is switched so that 7 upper address bits are provided to the RAM for the $\overline{CAS}$ LOW part of the cycle. The Am2964B Dynamic Memory Controller contains an 8-bit refresh counter that is used to supply the refresh address to the dynamic memory during the refresh cycle. This counter can be used in either the 128 or 256 line refresh mode. A $\overline{CAS}$ buffer is included in the dynamic memory controller so that the $\overline{CAS}$ output can be inhibited during refresh.

Normal operation of the Dynamic Memory Controller is to provide the address, close the input address latches and kick off a normal memory cycle. This is accomplished by bringing the $\overline{RASI}$ input LOW, which will cause one of the $\overline{RAS}$ outputs to go LOW. After the required memory timing, the MSEL input will be used to switch the multiplexer to the other address latch, then, the $\overline{CASI}$ input will be driven LOW causing the $\overline{CASO}$ output to go LOW and execute the $\overline{CAS}$ part of the memory cycle. The refresh cycle is executed by driving the $\overline{RFSH}$ input LOW which causes the multiplexer to connect the refresh counter to its address outputs. Then, the $\overline{RASI}$ input is driven LOW which causes all four $\overline{RAS}$ outputs to go LOW. This will simultaneously refresh all four banks of dynamic RAMs controlled by the Am2964B Dynamic Memory Controller. When either the $\overline{RFSH}$ or $\overline{RASI}$ input is brought HIGH, the refresh counter is advanced so it will be ready for the next refresh cycle.

As can be seen in Figure 1, Dynamic RAM Drivers can be used in large memory systems to buffer the Address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE\ ENABLE}$ signals to the RAMs. The Am2965 and Am2966 are pin compatible devices with the Am74S240 and Am74S244. These RAM drivers are specifically designed for driving dynamic RAMs and feature high capacitance drive, guaranteed maximum undershoot of less than −0.5 volts and high V_{OH} of greater than V_{CC} −1.15 volts. The Am2965 is inverting and the Am2966 is noninverting. The devices feature symmetrical rise and fall times and have guaranteed minimum and maximum t_{PD} specifications for both 50pF and 500pF loads.

Figure 5. Am2964B Dynamic Memory Controller



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Am2900 Family Applications Literature

Available from AMD's Customer Education Center

Bit-Slice Design: Controllers and ALUs, White D.E., Garland STPM Press, N.Y. © 1981 Price: $34.50 + Tax + Shipping ISBN 0-8240-7103-4	This book provides the inexperienced bit-slice design engineer with an easily understood description of how a computer control unit and ALU is built with the fundamental Am2900 devices (Am2901B, Am2909/11, Am2903, Am2910 and Am2914). This book forms the basis of the introductory bit-slice design course (ED2900A) at the AMD Customer Education Center.
Bit-Slice Microprocessor Design, Mick and Brick, McGraw-Hill Publishing Co. 1221 Avenue of the Americas New York, N.Y. 10020 Price: $18.50 + Tax + Shipping ISBN 0-07-041781-4	This comprehensive book discusses in detail the design of a microprogrammed computer using the Am2900 Family for the more experienced bit-slice designer. The book also includes sections on DMA design with the Am2940/Am2942 and Program Control Unit design with the Am2930/Am2932. The book's chapters are: I – Computer Architecture II – Microprogrammed Design III – The Data Path IV – The Data Path, Part Two V – Program Control Unit VI – Interrupt VII – Direct Memory Access VIII – The Hex 29 IX – The Super Sixteen
ED2900A Study Guide Price: $18.00 + Tax + Shipping	This study guide is used in conjunction with the ED2900A course and complements Bit-Slice Design: Controllers and ALUs. The study guide contains example design problems, exercises and example AMSYS® 29 programs.
Microprogram Design with the Am2900 Family	A discussion of the 'instruction-cracking' problem in microprogrammed machines. Discusses ways to translate op codes into microprogram addresses and control lines. Order 00575A - MPR

ORDERING INFORMATION

The above literature may be ordered directly from:

Customer Education Center
Advanced Micro Devices, Inc.
490–A Lakeside Drive, MS: 71
Sunnyvale, CA 94086

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School of Advanced Engineering

BIPOLAR APPLICATION DESIGN COURSES

AMD's School of Advanced Engineering offers graduate-level instruction in designing with the newest technologies. Bipolar design courses take you from the basics of bit-slice architecture through basic design with the 2900 Family on to the microprogram development system and its application to your design and finally to emulation and CPU architecture where students create microcode to drive an actual system, using the writable control store of the AmSYS29 development system.

For More Information:

Contact your AMD Sales Representative or write to:

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School of Advanced Engineering
Customer Education Center
490-A Lakeside Drive
P.O. Box 453
Sunnyvale, California 94086 U.S.A.

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Macro Meta Assembler from Microtec*

The Macro Meta Assembler is a valuable programming tool for those faced with the problem of writing micro-programs for bit slice processors such as the AMD 2901 and other similar microprogrammable microprocessors. It is a necessity for anyone faced with the problem of micro-programming any wide-word driven micro-sequencer system.

The Macro Meta Assembler is an enhanced version of Microtec's Meta Assembler. It is totally upward compatible, yet can perform many functions that are difficult or impossible with more basic packages.

The principal new feature of the Macro Meta Assembler is a powerful macro facility that enables the user to define variable length microinstructions using a single mnemonic; to encode complex overlayed instructions, and to encode non-contiguous fields. Macros may be passed a variety of parameter types: Symbols, Numbers, Opcodes, and Character Strings. Within the Macro-expansion parameters may be dynamically concatenated to existing text or other parameters, Symbols may be declared Local to the current Macro or be defined globally, and a wide variety of operators have been implemented for use with conditional Macro expansion. Macro calls may be nested and may be recursive.

Other features that have been added to the language include the availability of boolean and relational operators in expressions, automatic generation of parity bits and entry point PROMs.

The Meta Assembler consists of three separate programs: the Definition Program, the Assembly Program, and the PROM Formatter Program. These programs allow the user to define a unique assembly language, assemble a program written in the user-defined language, and organize the resulting object module into arrays that are compatible with the target ROM/PROM memories.

The Definition Program allows the user to define instruction mnemonics and their associated formats. Instruction lengths may vary from 1 to 128 bits. An instruction format is defined by breaking the microword into fields as variables, constants, or "don't care" bits. The variable fields are filled in at Assembly time. Default values and certain permanent attributes may also be assigned to variable fields at Definition time. The Definition Program produces an output listing and a disk file which contains the symbols and instruction mnemonics. This Definition file is used by the Assembly program as a reference when assembling a program.

The Assembly Program is similar to a traditional two-pass assembler. A symbolic source program utilizing the mnemonics and symbols defined in the Definition Program is read as input; a program listing and object module are generated as output. The Assembler provides symbolic addressing, relative addressing, paged addressing, and other features found in typical assembly programs. The instruction syntax and assembler directives are compatible with those utilized by AMD in its literature and software products. Additional directives have been implemented for versatile listing and output controls.

Both the Definition Program and the Assembly Program are implemented with Conditional Assembly Operators. Conditional statements may be nested up to 16 levels and can be made dependent on general expressions, character string equality, and symbol definition status. A full cross reference table is provided in both programs.

The following directives are included in Microtec's Macro Meta Assembler Program:

MACRO	– Define a Macro
ENDM	– End a Macro Definition
EXITM	– Alternater Macro Exit
LOCAL	– Define a Macro Local Symbol
IF	– Conditional Assembly if Expression is Non-Zero
ELSE	– Conditional Assembly Statement Converse
ENDIF	– Conditional Assembly Statement End
IFC	– Conditional Assembly if Character Strings Compare
IFNC	– Conditional Assembly if Character Strings Don't Compare
IFD	– Conditional Assembly if Symbol Defined
IFND	– Conditional Assembly if Symbol Not Defined
MAP	– Generate Entry Point Table
DUP	– Duplicate a Line (in timesharing version of AMDASM)
DATA	– Define Data Word (in timesharing version of AMDASM)

The PROM Formatter Program reads the object module produced by the Assembly Program and translates the format into one that can be read by a PROM programmer. BNPF, Data I/O ASCII hexadecimal, and the Step Engineering format are supported. Microwords in the object module can be divided into organizations that are compatible with the target PROM/ROM array. The length and width of PROMS may be specified as well as the value of "don't care" bits. The PROM Formatter has three new features that add to the versatility of the program: single bit parity generation; column switching; and column overlaying.

The Macro Meta Assembler is written in ANSI Fortran and will run on any general purpose digital computer that has a Fortran IV compiler, a word length of at least 16 bits, a disk or magnetic tape facility and 20–24K words of program memory. In most systems these programs can be run in an overlayed mode if the required memory is not available.

The programs are well commented and modular. A detailed manual, source listing, test programs, and test program output listings accompany each software order. The test programs allow the operation of the software to be verified quickly and easily. A manual is available for a small fee, if further information is desired.

For additional information, contact Microtec, P.O. Box 60337, Sunnyvale, California 94088. Telephone (408) 733-2919.

*This information was provided by Microtec. AMD is not associated with Microtec and does not guarantee their products.

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Meta Assembler Program from Microtec*

Microtec has available a Meta Assembler program for the AMD 2900 microprocessor and other similar microprogrammable microprocessors. The Assembler is compatible with AMD's AMDASM program, but is written in ANSI standard Fortran IV and will run on any machine that has:

1. A Fortran IV compiler
2. A word length of at least 16 bits
3. A disc or magnetic tape facility
4. 18K words of Random Access Memory (in most systems these programs can be run in an overlayed mode if the required memory is not available)

The Meta Assembler Software Package actually consists of three separate programs, a Definition Program, an Assembly Program, and a PROM Formatter Program.

The Definition Program allows the user to define instruction mnemonics and their associated formats. Instruction lengths may vary from 1 to 128 bits. Symbolic Constants and reserved words may also be defined in the Definition Program. An instruction format is defined by breaking the microword into fields and defining the fields as constants, don't care bits, or variables which are filled in at assembly time. Default values and certain permanent attributes may also be assigned to variable fields at Definition time. The Definition Program produces an output listing and a disk file consisting of the defined symbols and instruction mnemonics. This Definition file is used by the Assembly program as a reference when assembling a program.

The Assembly program operates like a traditional assembler. A symbolic source program utilizing the mnemonics and symbols defined in the Definition Program is read as input, and a listing and object module are generated as output. The Assembler provides symbolic addressing, relative addressing, paged addressing, and other features found in typical assembly programs. The instruction syntax and assembler directives are compatible with those utilized by AMD in its literature and software products. Additional directives have been implemented to provide for versatile listing and output controls.

Conditional Assembly statements are provided in both the Definition and Assembly programs. These statements may be nested up to 16 levels and can be made dependent on general expression. A full cross reference table is also provided in both programs.

Some features of Microtec's Meta Assembler are particularly helpful when assembling code for microprogrammable machines. The existence of don't care bits and instruction overlaying are included among these features. Bits of a microword which are not relevant to a particular instruction format may be defined as don't care bits. Don't care bits are printed as X's on the listing and do not have to be defined until the PROM Formatter program is executed. An instruction format with don't care bits can be overlayed with other instruction formats. Therefore when useful, an instruction format can be used to define only part of the microword, padding out the word with don't care bits.

The PROM Formatter Program reads the object module file produced by the Assembly program and translates the format into one that can be read by a PROM programmer. Both BNPF and Data I/O's ASCII hexadecimal format are supported. Microwords in the object module can be broken up into organizations that are compatible with the target PROM/ROM array. Users may specify PROMs of any width and length, as well as the value of don't care bits. Any or all PROMs may be listed and/or punched.

The programs are well commented and modular. A detailed manual, source listing, test programs, and test program output listings accompany each software order. The test programs allow the operation of the software to be verified quickly and easily. If the information given here is not sufficient, a manual is available for a small fee.

Coming soon is M29 AMD'S New Meta Assembler. Contact your local sales office for details.

For additional information, contact Microtec, P.O. Box 60337 Sunnyvale, Ca. 94088 (408) 733-2919

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Videotape Seminar Kits

Advanced Micro Devices regularly prepares and presents seminars wordwide that describe the function and application of its Am2900 Family products. These seminars may also be presented at local factory or design centers through arrangement with the field Applications Engineer located at the AMD Sales Office.

It is now also possible to order the following seminars in videotape form with literature kits.

- 2Am29116 Sixteen-Bit Biplor Microprocessor and Peripherals
- 2Am29500 Array Processing/Digital Signal Processing Familly

The videotape is a 2 – 3 hour seminar covering the products function in detail and demonstrating aspects of system integration using the products, The literature kit includes a slide booklet, data sheets of all products covered in the seminar, and other relevant material.

These kits may be ordered from AMD's Customer Education Center. Contact your AMD Sales Representative for more infomation.

	Order Code	Prices(USA)
Am29116 Sixteen-Bit Biplor Microprocessor and Peripherals – Videotape (includes one set of literature)	Am29116–VIDEO	$99/Videotape
– Literature Kit (each additional set)	Am29116–LIT	$5/set
Am29500 Array Processing (Digital Signal Processing Familly) – Videotape (includes one set of literature)	Am29116–VIDEO	$99/Videotape
– Literature Kit (each additional set)	Am29116–LIT	$5/set

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Am29300 Family

Am29323

32-Bit Parallel Multiplier

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- 32-Bit Three-Bus Architecture
  - The device has two 32-bit input ports and one 32-bit output port with maximum multiply time of 80ns
- Single Clock with Register Enables
  - The Am29323 is controlled by one clock with individual register enables
- Supports Multiprecision Multiplication
  - The device has dual 32-bit registers on each data input port to perform multiprecision multiplication
- Transparent-Able Input, Output and Instruction Registers
  - Input and output registers can be made transparent independently to eliminate unwanted pipeline delay
- Supports Two's complement, unsigned or mixed mode numbers
- Data Integrity Through Master-Slave Mode and Parity Check/Generate
  - Parity check/generate catches inter-device connection errors and master/slave mode provides complete function check

GENERAL DESCRIPTION

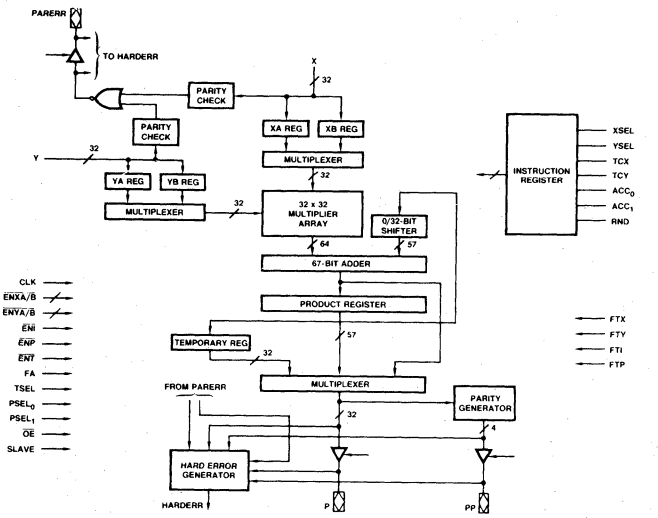
The Am29323 is a high-speed 32 x 32-Bit Parallel Multiplier with 67-Bit Accumulator. The part is designed to maximize system level performance by providing three 32-bit bus architecture and a single clock with register enables.

The Am29323 further enhances the system throughput by providing individual register feedthrough controls, byte parity checking on both input ports and generation on the output port, as well as, dual input registers on each data input bus to support multiprecision multiplication. The Am29323 can manage a wide variety of data types such as Two's complement, unsigned or mixed mode input formats. 64 x 64 bit multiplication can be performed in seven clock cycles, including input and output. Additional features provided are format adjust control allowing for standard output or left shifted output suitable for Two's complement arithmetic. The part also features master/slave operation.

The Am29323 is designed with the IMOX™ process, which allows internal ECL circuits with TTL compatible I/O. The device is housed in a 168-lead pin-grid-array package.

BLOCK DIAGRAM

The Am29323 High-Speed 32 x 32-Bit Parallel Multiplier



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Am29325

32-Bit Floating Point Processor

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Single VLSI device performs high-speed floating-point arithmetic
  - Floating-point addition, subtraction and multiplication in a single clock cycle
  - Internal architecture supports sum-of-products, Newton-Raphson division
- 32-bit, 3-bus flow-through architecture
  - Programmable I/O allows interface to 32- and 16-bit systems
- IEEE and DEC formats
  - Performs conversions between formats
  - Performs integer ◄► floating point conversions
- Six flags indicate operation status
- Register enables eliminate clock skew
- Input and output registers can be made transparent independently

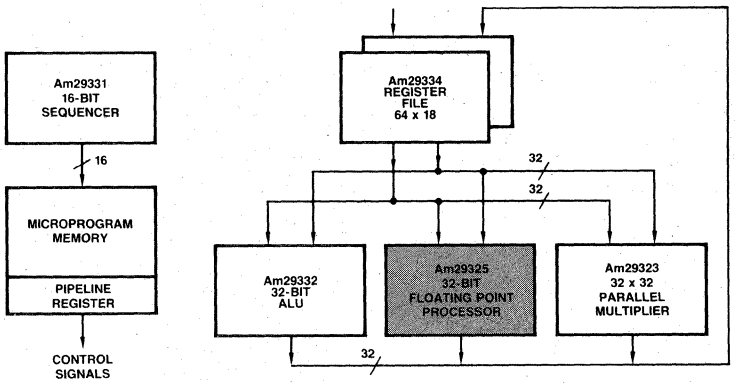
GENERAL DESCRIPTION

The Am29325 is a high-speed floating-point processor unit. It performs 32-bit single-precision floating-point addition, subtraction, and multiplication operations in a single LSI integrated circuit, using the format specified by the proposed IEEE floating-point standard P754. The DEC single-precision floating-point format is also supported. Operations for conversion between 32-bit integer format and floating-point format are available, as are operations for converting between the IEEE and DEC floating-point formats. Any operation can be performed in a single clock cycle. Six flags – invalid operation, inexact result, zero, not-a-number, overflow, and underflow – monitor the status of operations.

The Am29325 has a 3-bus, 32-bit architecture, with two input buses and one output bus. This configuration provides high I/O bandwidth, allows access to all buses and affords a high degree of flexibility when connecting this device in a system. All buses are registered, with each register having a clock enable. Input and output registers may be made transparent independently. Two other I/O configurations, a 32-bit, 2-bus architecture and a 16-bit, 3-bus architecture, are user-selectable, easing interface with a wide variety of systems. Thirty-two-bit internal feedforward data paths support accumulation operations, including sum-of-products and Newton-Raphson division.

Fabricated with the high-speed IMOX™ bipolar process, the Am29325 is powered by a single 5-volt supply. The device is housed in a 144-pin pin-grid-array package.

Am29300 FAMILY HIGH PERFORMANCE SYSTEM BLOCK DIAGRAM



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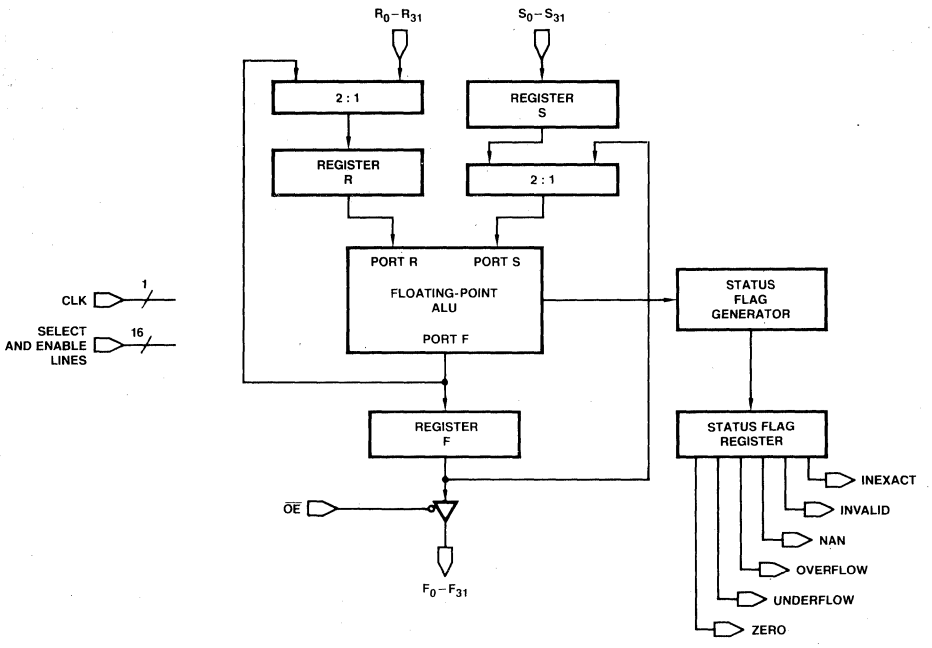
RELATED PRODUCTS

- Am29323 – 32 x 32 Parallel Multiplier
- Am29332 – 32-Bit ALU
- Am29331 – 16-Bit Sequencer
- Am29334 – 64 x 18 Four-Port Dual-Access Register File

BLOCK DIAGRAM
Am29325



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DEFINITION OF TERMS

AFFINE MODE

One of two modes affecting the handling of operations on infinities – see the **Operations with Infinities** section under **Operation in IEEE Mode** below.

BIASED EXPONENT

The true exponent of a floating-point number, plus a constant. For IEEE floating-point numbers, the constant is 127; for DEC floating-point numbers, the constant is 128. See also **True Exponent**.

BUS

Data input or output channel for the floating-point processor.

DEC RESERVED OPERAND

A DEC floating-point number that is interpreted as a symbol and has no numeric value. A DEC reserved operand has a sign of 1 and a biased exponent of 0.

DESTINATION FORMAT

The format of the final result produced by the floating-point ALU. The destination format can be IEEE floating-point, DEC floating-point or integer.

FINAL RESULT

The result produced by the floating-point ALU.

FRACTION

The twenty-three least-significant bits of the mantissa.

INFINITELY PRECISE RESULT

The result that would be obtained from an operation if both exponent range and precision were unbounded.

INPUT OPERANDS

The value or values on which an operation is performed. For example, the addition 2 + 3 = 5 has input operands 2 and 3.

MANTISSA

The portion of a floating-point number containing the number's significant bits. For the floating-point number 1.101×2^{-3}, the mantissa is 1.101.

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DEFINITION OF TERMS (Cont)

NAN (Not-a-Number)

An IEEE floating-point number that is interpreted as a symbol, and has no numeric value. A NAN has a biased exponent of 255_{10} and a non-zero fraction.

PORT

Data input or output channel for the floating-point ALU.

PROJECTIVE MODE

One of two modes affecting the handling of operations on infinities – see the **Operations with Infinities** section under **Operation in IEEE Mode** below.

ROUNDED RESULT

The result produced by rounding the infinitely precise result to fit the destination format.

TRUE EXPONENT (or Exponent)

Number representing the power of two by which a floating-point number's mantissa is to be multiplied. For the floating-point number 1.101×2^{-3}, the true exponent is -3.

PIN DESCRIPTION

R_0-R_{31}	R operand bus, input. R_0 is the least-significant bit.
S_0-S_{31}	S operand bus, input. S_0 is the least-significant bit.
F_0-F_{31}	F operand bus, output. F_0 is the least-significant bit.
CLK	Clock input for the internal registers.
$\overline{ENR}$	Register R clock enable, input. When $\overline{ENR}$ is LOW, register R is clocked on the LOW-to-HIGH transition of CLK. When $\overline{ENR}$ is HIGH, register R retains the previous contents.
$\overline{ENS}$	Register S clock enable, input. When $\overline{ENS}$ is LOW, register S is clocked on the LOW-to-HIGH transition of CLK. When $\overline{ENS}$ is HIGH, register S retains the previous contents.
$\overline{ENF}$	Register F clock enable, input. When $\overline{ENF}$ is LOW, register F is clocked on the LOW-to-HIGH transition of CLK. When $\overline{ENF}$ is HIGH, register F retains the previous contents.
FT_0	Input register feedthrough control, input. When FT_0 is HIGH, registers R and S are transparent.
FT_1	Output register feedthrough control, input. When FT_1 is HIGH, register F and the status flag register are transparent.
I_0-I_2	Operation select lines, inputs. Used to select the operation to be performed by the ALU. See the **ALU Operation Select Table** for a list of operations and the corresponding codes.
I_3	ALU S port input select, input. A LOW on I_3 selects register S as the input to the ALU S port. A HIGH on I_3 selects register F as the input to the ALU S port.
I_4	Register R input select, input. A LOW on I_4 selects R_0-R_{31} as the input to register R. A HIGH selects the ALU F port as the input to register R.
IEEE/$\overline{DEC}$	IEEE/DEC mode select, input. When IEEE/$\overline{DEC}$ is HIGH, IEEE mode is selected. When IEEE/$\overline{DEC}$ is LOW, DEC mode is selected.
INEXACT	Inexact result flag, output. A HIGH indicates that the final result of the last operation was not infinitely precise, due to rounding.
INVALID	Invalid operation flag, output. A HIGH indicates that the last operation performed was invalid, e.g., ∞ times 0.
NAN	Not-a-number flag, output. A HIGH indicates that the final result produced by the last operation is not to be interpreted as a number. The output in such cases is either an IEEE Not-a-Number (NAN) or a DEC reserved operand.
$\overline{OE}$	Output enable, input. When $\overline{OE}$ is LOW, the contents of register F are placed on F_0-F_{31}. When $\overline{OE}$ is HIGH, F_0-F_{31} assume a high-impedance state.
ONEBUS	Input bus configuration control, input. A LOW on ONEBUS configures the input bus circuitry for two-input bus operation. A HIGH on ONEBUS configures the input bus circuitry for single-input bus operation.
OVERFLOW	Overflow flag, output. A HIGH indicates that the last operation produced a final result that overflowed the floating-point format.
PROJ/$\overline{AFF}$	Projective/affine mode select, input. Choice of projective or affine mode determines the way in which infinities are handled in IEEE mode. A LOW on PROJ/$\overline{AFF}$ selects affine mode; a HIGH selects projective mode.

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PIN DESCRIPTION (Cont)

RND_0, RND_1 Rounding mode selects, inputs. RND_0 and RND_1 select one of four rounding modes. See the **Rounding Mode Select Table** for a list of rounding modes and the corresponding control codes.

S16/$\overline{32}$ Sixteen- or thirty-two-bit I/O mode select, input. A LOW on S16/$\overline{32}$ selects the thirty-two-bit I/O mode; a HIGH selects the sixteen-bit I/O mode. In thirty-two-bit mode, inputs and output buses are 32 bits wide. In sixteen-bit mode, input and output buses are sixteen bits wide, with the least and most significant portions of the thirty-two-bit input and output words being placed on the buses during the HIGH and LOW portions of CLK, respectively.

UNDERFLOW Underflow flag, output. A HIGH indicates that the last operation produced a rounded result that underflowed the floating-point format.

ZERO Zero flag, output. A HIGH indicates that the last operation produced a final result of zero.

3

ARCHITECTURE

The Am29325 comprises a high-speed, floating-point ALU, a status flag generator, and a 32-bit data path.

Floating-Point ALU

The floating-point ALU performs 32-bit floating-point operations. It also performs floating-point-to-integer conversions, integer-to-floating-point conversions, and conversions between the IEEE and DEC floating-point formats. The ALU has two 32-bit input ports, R and S, and a 32-bit output port, F.

Conceptually, the process performed by the ALU can be divided into three stages – see Figure 1. The operation stage performs the arithmetic operation selected by the user; the output of this section is referred to as the infinitely precise result of the operation. The rounding stage rounds the infinitely precise result to fit in the destination format; the output of this stage is called the rounded result. The last stage checks for exceptional conditions. If no exceptional condition is found, the rounded result is passed through this stage. If some exceptional condition is found, e.g., overflow, underflow, or an invalid operation, this section may replace the rounded result with another output, such as $+\infty$, $-\infty$, a NAN, or a DEC reserved operand. The output of this last stage appears on port F, and is called the final result.

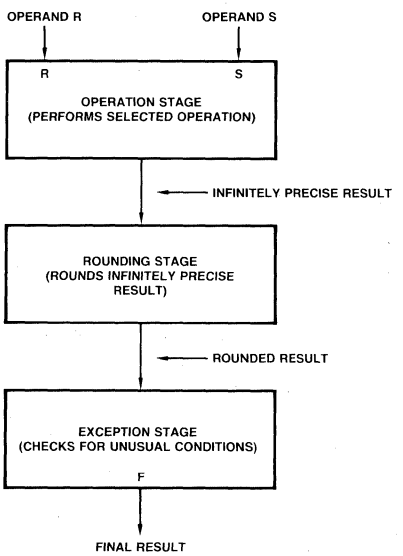
The ALU performs one of eight operations; the operation to be performed is selected by placing the appropriate control code on lines $I_0 - I_2$. The **ALU Operation Select Table** gives the control codes corresponding to each of the eight operations.

The floating-point addition operation (R PLUS S) adds the floating-point numbers on ports R and S, and places the floating-point result on port F. In IEEE mode (IEEE/$\overline{DEC}$ = HIGH) the addition is performed in IEEE floating-point format; in DEC mode (IEEE/$\overline{DEC}$ = LOW) the addition is performed in DEC format.

The floating-point subtraction operation (R MINUS S) subtracts the floating-point number on port S from the floating-point number on port R and places the floating-point result on port F. In IEEE mode (IEEE/$\overline{DEC}$ = HIGH) the subtraction is performed in IEEE floating-point format; in DEC mode (IEEE/$\overline{DEC}$ = LOW) the subtraction is performed in DEC format.

The floating-point multiplication operation (R TIMES S) multiplies the floating-point numbers on ports R and S, and places the floating-point result on port F. In IEEE mode (IEEE/$\overline{DEC}$ = HIGH) the multiplication is performed in IEEE floating-point format; in DEC mode (IEEE/$\overline{DEC}$ = LOW) the multiplication is performed in DEC format.

Figure 1. Conceptual Model of the Process Performed by the Floating-Point ALU



The floating-point constant subtraction (2 MINUS S) operation subtracts the floating-point value on port S from 2, and places the result on port F. The operand on port R is not used in this operation; its value will not affect the operation in any way. In IEEE mode (IEEE/$\overline{DEC}$ = HIGH) the operation is performed in IEEE floating-point format; in DEC mode (IEEE/$\overline{DEC}$ = LOW) the operation is performed in DEC format. This operation is used to support Newton-Raphson floating-point division; a description of its use appears in **Appendix C.**

The integer-to-floating-point conversion (INT-TO-FP) operation takes a 32-bit, two's complement integer on port R and places the equivalent floating-point value on port F. The operand on port S is not used in this operation; its value will not affect the operation in any way. In IEEE mode (IEEE/$\overline{DEC}$ = HIGH) the result is delivered in IEEE format; in DEC mode (IEEE/$\overline{DEC}$ = LOW) the result is delivered in DEC format.

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ALU OPERATION SELECT TABLE

I_2	I_1	I_0	Operation	Output Equation
0	0	0	Floating-point addition (R PLUS S)	F = R + S
0	0	1	Floating-point subtraction (R MINUS S)	F = R − S
0	1	0	Floating-point multiplication (R TIMES S)	F = R * S
0	1	1	Floating-point constant subtraction (2 MINUS S)	F = 2 − S
1	0	0	Integer-to-floating-point conversion (INT-TO-FP)	F (floating-point) = R (integer)
1	0	1	Floating-point-to-integer conversion (FP-TO-INT)	F (integer) = R (floating-point)
1	1	0	IEEE-TO-DEC format conversion (IEEE-TO-DEC)	F (DEC format) = R (IEEE format)
1	1	1	DEC-TO-IEEE format conversion (DEC-TO-IEEE)	F (IEEE format) = R (DEC format)

The floating-point-to integer conversion (FP-TO-INT) operation takes a floating-point number on port R and places the equivalent 32-bit, two's complement integer value on port F. The operand on port S is not used in this operation; its value will not affect the operation in any way. In IEEE mode (IEEE/$\overline{\text{DEC}}$ = HIGH) the operand on port R is interpreted using the IEEE floating-point format; in DEC mode (IEEE/$\overline{\text{DEC}}$ = LOW) it is interpreted using the DEC floating-point format.

The IEEE-to-DEC conversion operation (IEEE-TO-DEC) takes an IEEE-format floating-point number on port R and places the equivalent DEC-format floating-point number on port F. The operand on port S is not used in this operation; its value will not affect the operation in any way. The operation can be performed in either IEEE mode (IEEE/$\overline{\text{DEC}}$ = HIGH) or DEC mode (IEEE/$\overline{\text{DEC}}$ = LOW).

The DEC-to-IEEE conversion operation (DEC-TO-IEEE) takes a DEC-format floating-point number on port R and places the equivalent IEEE-format floating-point number on port F. The operand on port S is not used in this operation; its value will not affect the operation in any way. The operation can be performed in either IEEE mode (IEEE/$\overline{\text{DEC}}$ = HIGH) or DEC mode (IEEE/$\overline{\text{DEC}}$ = LOW).

Status Flag Generator

The status flag generator controls the state of six flags that report the status of floating-point ALU operations. The flags indicate when an operation is invalid (e.g., infinity times zero) or when an operation has produced an overflow, an underflow, a non-numerical result (e.g., a NAN or DEC reserved operand), an inexact result, or a result of zero. The flags represent the status of the most-recently-performed operation. Flag status is stored in the flag status register on the LOW-to-HIGH transition of CLK. When the output register feedthrough control FT_1 is HIGH, the flag status register is made transparent.

Data Path

The 32-bit data path consists of the R and S input buses, the F output bus, data registers R, S, and F, the register R input multiplexer, and the ALU port S input multiplexer.

Input operands enter the floating-point processor through the 32-bit R and S input buses, R_0–R_{31} and S_0–S_{31}. Results of operations appear on the 32-bit F bus, F_0–F_{31}. The F bus assumes a high-impedance state when output enable $\overline{\text{OE}}$ is HIGH.

The R and S registers store input operands; the F register stores the final result of the floating-point ALU operation. Each register has an independent clock enable ($\overline{\text{ENR}}$, $\overline{\text{ENS}}$ and $\overline{\text{ENF}}$). When a register's clock enable is LOW, the register stores the data on its input at the LOW-to-HIGH transition of CLK; when the clock enable is HIGH, the register retains its current data. All data registers are fully edge-triggered – both the input data and the register enable need only meet modest setup and hold time requirements. Registers R and S can be made transparent by setting FT_0, the input register feedthrough control, HIGH. Register F can be made transparent by setting FT_1, the output register feedthrough control, HIGH.

The register R input multiplexer selects either the R input bus or the floating-point ALU's F port as the input to register R. Selection is controlled by I_4 – a LOW selects the R input bus; a HIGH selects the ALU F port. The ALU port S input multiplexer selects either register S or register F as the input to the floating-point ALU's S port. Selection is controlled by I_3 – a LOW selects register S; a HIGH selects register F.

Data selected by I_3 and I_4 is described in the **Mux Select Tables**. When registers R and S are transparent (FT_0 = HIGH) multiplexer select I_4 must be kept LOW, so that the register R input multiplexer selects R_0–R_{31}. When register F is transparent (FT_1 = HIGH) multiplexer select I_3 must be kept LOW, so that the ALU port S input multiplexer selects register S.

MUX SELECT TABLES

I_3	Data selected for floating-point ALU S port
0	Register S
1	Register F

I_4	Data selected for register R input
0	R bus
1	Floating-point ALU port F

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I/O MODES

The Am29325 data path can be configured in one of three I/O modes: a 32-bit, two-input-bus mode; a 32-bit, single-input-bus mode; and a 16-bit, two-input-bus mode. These modes affect only the manner in which data is delivered to and taken from the Am29325; operation of the floating-point ALU is not altered. The I/O mode is selected with the ONEBUS and S16/$\overline{32}$ controls. The **I/O Mode Selection Table** lists the control codes needed to invoke each I/O mode.

I/O MODE SELECTION TABLE

S16/$\overline{32}$	ONEBUS	I/O Mode
0	0	32-bit, two-input-bus mode
0	1	32-bit, single-input-bus mode(*)
1	0	16-bit, two-input-bus mode(*)
1	1	Illegal I/O mode selection value

(*)FT_0 must be held LOW in this mode (see text).

32-Bit, Two-Input-Bus Mode

In this I/O mode, the R and S buses are configured as independent 32-bit input buses, and the F bus is configured as a 32-bit output bus. Figure 2 is a functional block diagram of the Am29325 in this I/O mode.

R and S operands are taken from their respective input buses and clocked into the R and S registers on the LOW-to-HIGH transition of CLK. Register F is also clocked on the LOW-to-HIGH transition of CLK. Figure 5(a.) depicts typical I/O timing in this mode.

32-Bit, Single-Input-Bus Mode

In this I/O mode, the R and S buses are connected to a single 32-bit multiplexed input data bus; the F bus is configured as an independent 32-bit output bus. Figure 3 is a functional block diagram of the Am29325 in this I/O mode. Note that both the R and S bus lines must be wired to the input bus.

R and S operands are multiplexed onto the input bus by the host system. The S operand is clocked from the input bus into a temporary holding register on the HIGH-to-LOW transition of CLK and is transferred to register S on the LOW-to-HIGH transition of CLK. The R operand is clocked from the input bus into register R on the LOW-to-HIGH transition of CLK. Register F is clocked on the LOW-to-HIGH transition of CLK. Figure 5(b.) depicts typical I/O timing in this mode.

When placed in this I/O mode, the data path will not function properly if the R and S registers are made transparent. Therefore input register feedthrough control FT_0 must be held LOW in this mode.

Figure 2. Functional Block Diagram for the 32-Bit, Two-Input-Bus Mode

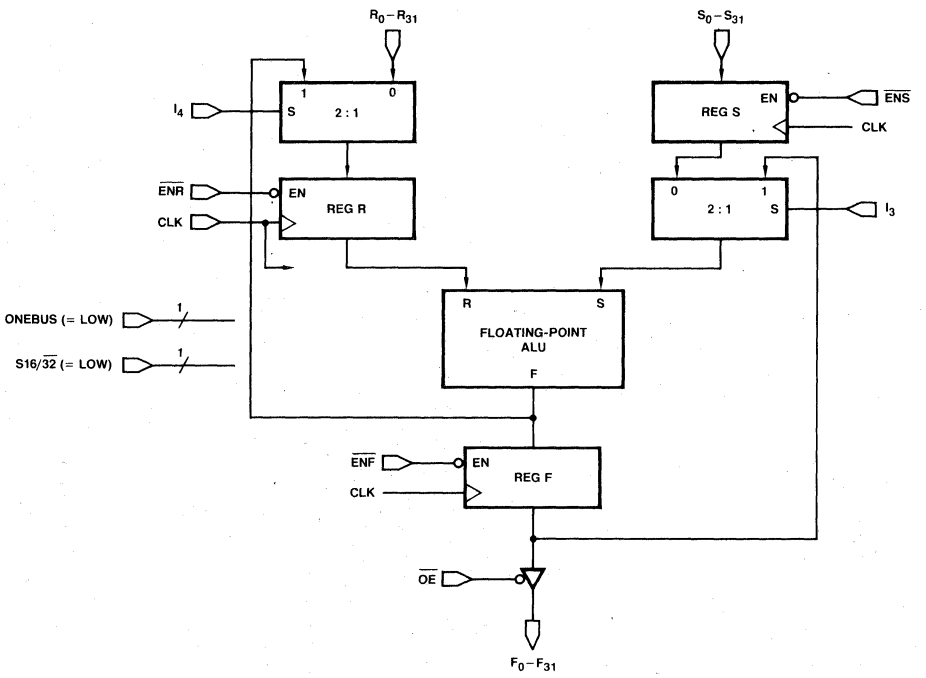

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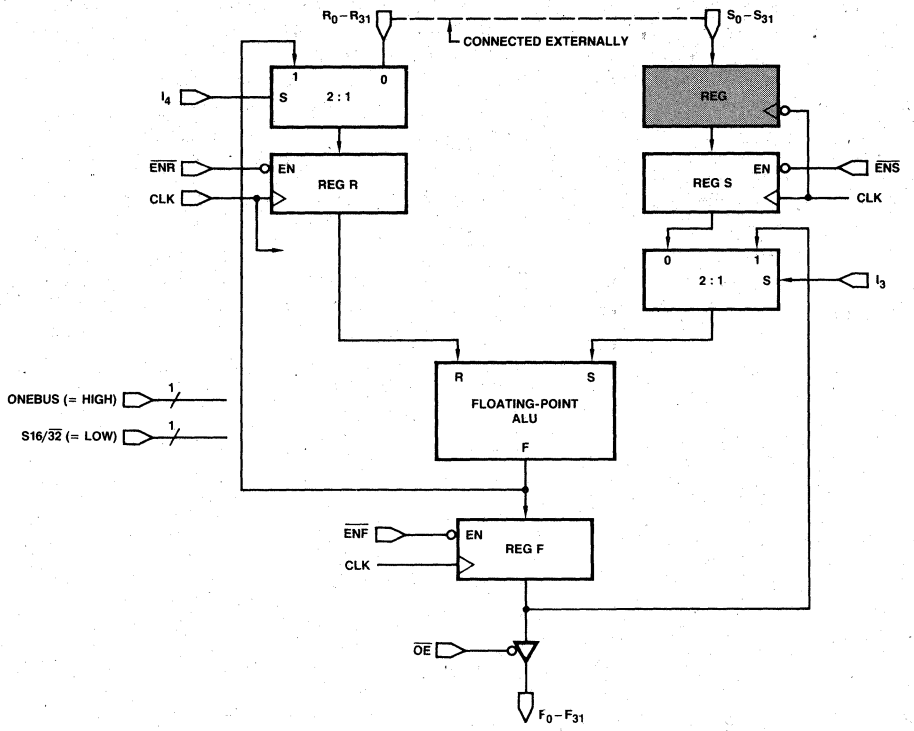
Figure 3. Functional Block Diagram for the 32-Bit, Single-Input-Bus Mode



16-Bit, Two-Input-Bus Mode

In this I/O mode, the R and S buses are configured as independent 16-bit input buses, and the F bus is configured as a 16-bit output bus. Figure 4 is a functional block diagram of the Am29325 in this I/O mode. Note that the 16 LSBs and 16 MSBs of the R, S and F buses must be wired to their respective system buses in parallel.

Thirty-two-bit operands are passed along the 16-bit data buses by time-multiplexing the 16 LSBs and 16 MSBs of each 32-bit word. For the R input bus, the host system multiplexes the 16 LSBs and 16 MSBs of the R operand onto the 16-bit R bus. The 16 LSBs of the R operand are stored in a temporary holding register on the HIGH-to-LOW transition of CLK. The 16 MSBs are clocked into register R on the LOW-to-HIGH transition of CLK; at the same time, the 16 LSBs are transferred from the temporary holding register to register R. Transfer of data from the S input bus to the S register takes place in a similar fashion. Register F is clocked on the LOW-to-HIGH transition of CLK. Circuitry internal to the Am29325 multiplexes data from register F onto the 16-bit output bus by enabling the 16 LSBs of the F output bus when CLK is HIGH, and enabling the 16 MSBs of the F output bus when CLK is LOW. Figure 5(c.) depicts typical I/O timing in this mode.

When placed in this I/O mode, the data path will not function properly if the R and S registers are made transparent. Therefore input register feedthrough control FT_0 must be held LOW in this mode. Caution must also be taken in controlling the register R input multiplexer control line, I_4, in this I/O mode. I_4 should be changed only when CLK is HIGH, in addition to meeting the setup and hold time requirements given in the **Switching Characteristics** section.

OPERATION IN IEEE MODE

When input signal IEEE/$\overline{\text{DEC}}$ is HIGH, the IEEE mode of operation is selected. In this mode the Am29325 uses the floating-point format set forth in the IEEE Proposed Standard for Binary Floating-Point Arithmetic, P754. In addition, the IEEE mode complies with most other aspects of single-precision floating-point operation outlined in the proposed standard – differences are discussed in **Appendix A.**

IEEE Floating-Point Format

The IEEE single-precision floating-point word is thirty-two bits wide, and is arranged in the format shown in Figure 6. The floating-point word is divided into three fields: a single-bit sign, an eight-bit biased exponent, and a 23-bit fraction.

The sign bit indicates the sign of the floating-point number's value. Non-negative values have a sign of 0; negative values, a sign of 1. The value zero may have either sign.

The biased exponent is an eight-bit unsigned integer field representing a multiplicative factor of some power of two. The bias value is 127. If, for example, the multiplicative factor for a floating-point number is to be 2^a, the value of the biased exponent would be a+127; a is called the true exponent.

The fraction is a 23-bit unsigned fractional field containing the 23 least-significant bits of the floating-point number's 24-bit mantissa. The weight of fraction's most significant bit is 2^{-1}; the weight of the least-significant bit is 2^{-23}.

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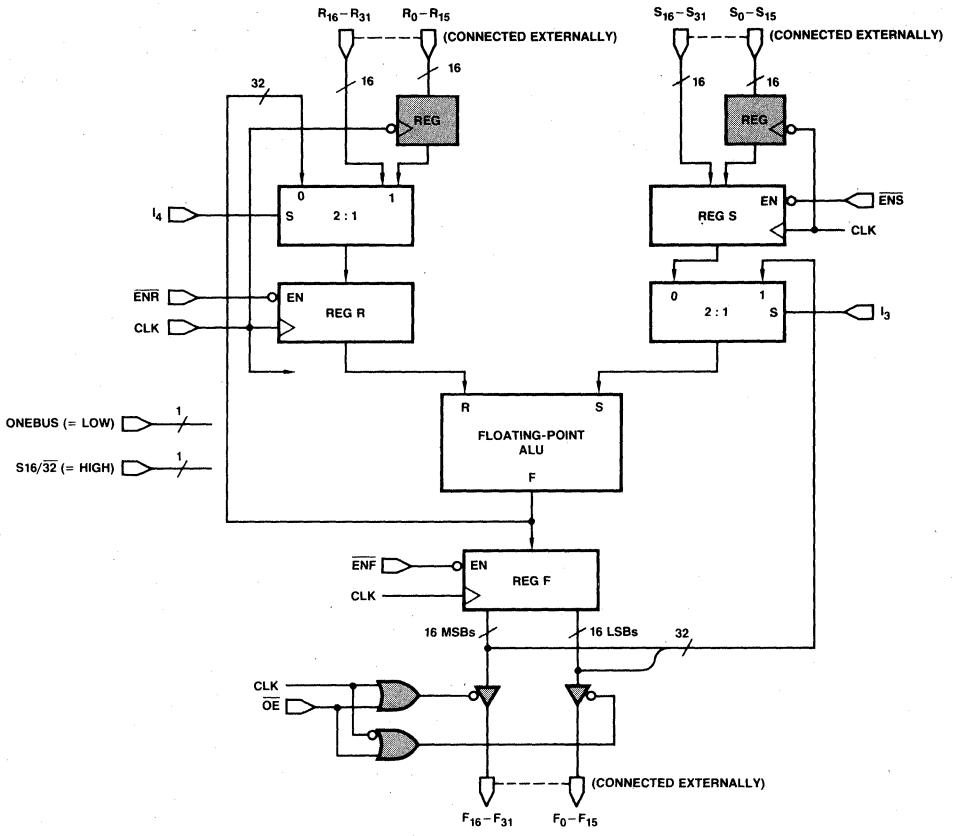
Figure 4. Functional Block Diagram for the 16-Bit, Two-Input-Bus Mode



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A floating-point number is evaluated or interpreted per the following conventions:

let s = sign bit
e = biased exponent
f = fraction

if e = 0 and f = 0 . . . value = $(-1)^{s}*(0)$ (+0, −0)

if e = 0 and f < > 0 . . . value = denormalized number

if 0 < e < 255 . . value = $(-1)^{s}*(2^{e-127})*(1.f)$ (normalized number)

if e = 255 and f = 0 . . value = $(-1)^{s}*(\infty)$ $(+\infty, -\infty)$

if e = 255 and f < > 0 . . . value = not-a-number (NAN)

Zero – The value zero can have either a positive or negative sign. Rules for determining the sign of a zero produced by an operation are given in the **Sign Bit** section on page 12.

Denormalized Number – A denormalized number represents a quantity with magnitude less than 2^{-126} but greater than zero.

Normalized Number – A normalized number represents a quantity with magnitude greater than or equal to 2^{-126} but less than 2^{128}.

Example 1:

The number +3.5 can be represented in floating-point format as follows:

$+3.5 = 11.1_2 \times 2^0$
$= 1.11_2 \times 2^1$

sign = 0

biased exponent = $1_{10}+127_{10} = 128_{10}$
$= 10000000_2$

fraction = $11000000000000000000000_2$
(the leading 1 is implied in the format)

Concatenating these fields produces the floating-point word 40600000_{16}.

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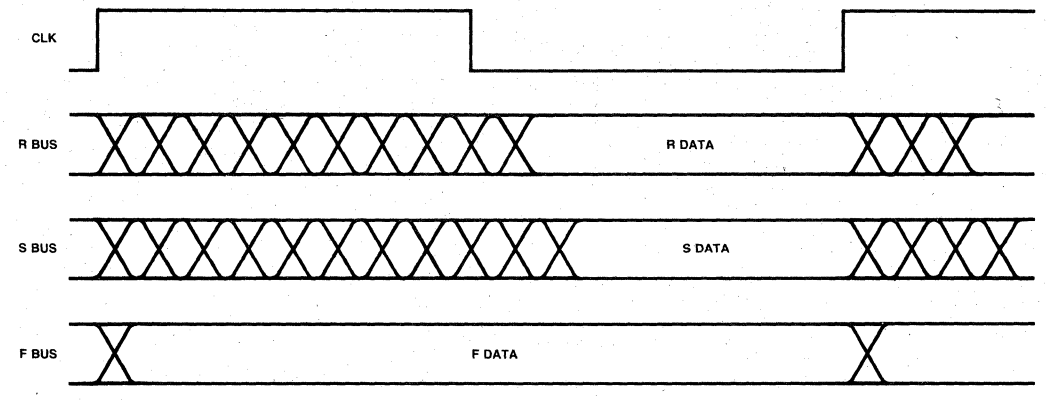
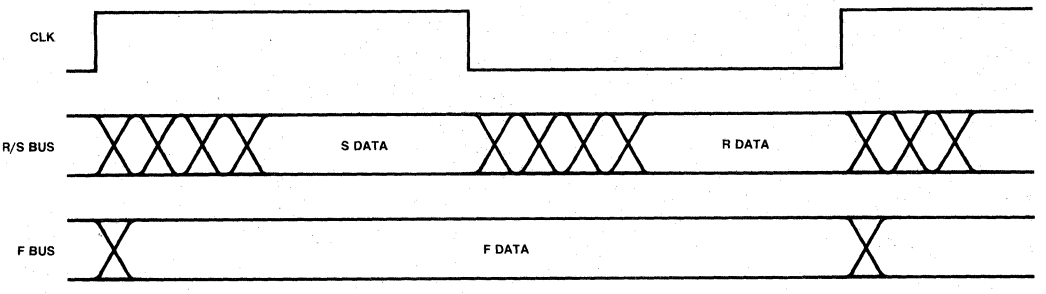
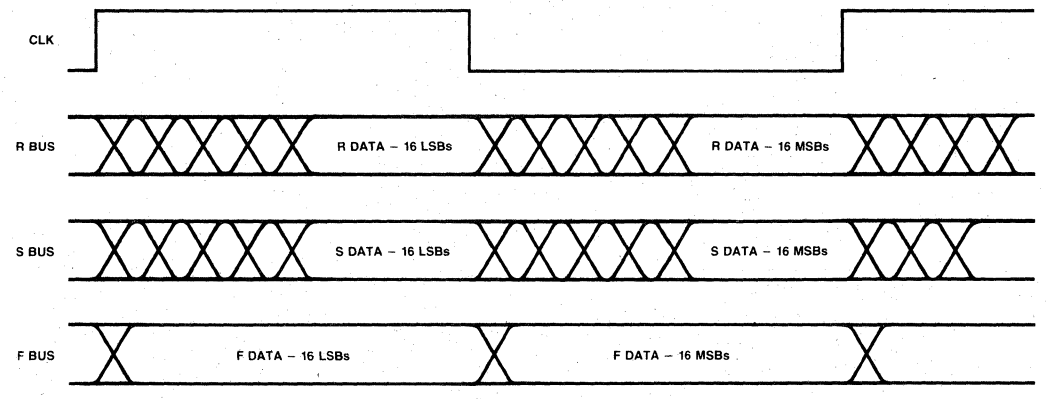
Figure 5. Typical Bus Timing for the I/O Modes, with FT_0 = LOW, FT_1 = LOW



a) 32-Bit, Two-Input-Bus Mode



b) 32-Bit, Single-Input-Bus Mode



c) 16-Bit, Two-Input-Bus Mode

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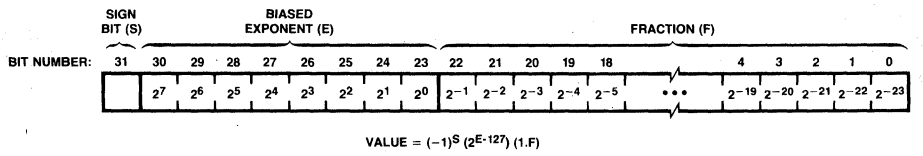
Figure 6. IEEE Mode Single-Precision Floating-Point Format



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Example 2:

The number −11.375 can be represented in floating-point format as follows:

$-11.375 = -1011.011_2 \times 2^0$
$= -1.011011_2 \times 2^3$

sign = 1

biased exponent = $3_{10}+127_{10} = 130_{10}$
$= 10000010_2$

fraction = $01101100000000000000000_2$
(the leading 1 is implied in the format)

Concatenating these fields produces the floating-point word $C1360000_{16}$.

Infinity – Infinity can have either a positive or negative sign. The way in which infinities are interpreted is determined by the state of the projective/affine mode select, PROJ/$\overline{\text{AFF}}$.

Not-a-Number – A not-a-number, or NAN, does not represent a numeric value, but is interpreted as a signal or symbol. NANs are used to indicate invalid operations, and as a means of passing process status information through a series of calculations. NANs arise in two ways: they can be generated by the Am29325 to indicate that an invalid operation has taken place (e.g., infinity times zero), or they can be provided by the user as an input operand. There are two types of NANs: signalling and quiet. These NANs have the formats shown in Figure 7.

IEEE Mode Integer Format

Integer numbers are represented as 32-bit, two's complement words; Figure 8 depicts the integer format. The integer word can represent a range of integer values from -2^{31} to $2^{31}-1$.

Figure 7. Signalling and Quiet NAN Formats

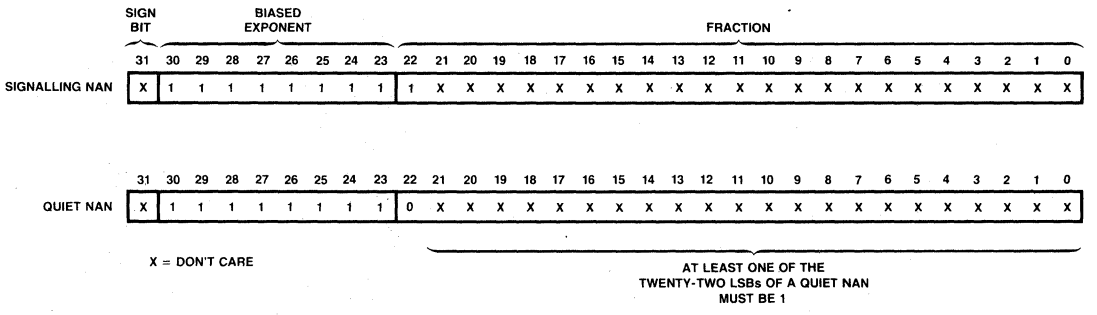

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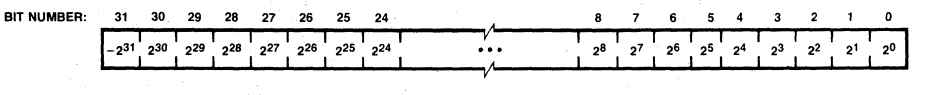
Figure 8. Thirty-Two-Bit Integer Format



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Operations

All eight floating-point ALU operations discussed in the Functional Description section above can be performed in IEEE mode. Various exceptional aspects of the R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, INT-TO-FP, and FP-TO-INT operations for this mode are described below. The IEEE-TO-DEC and DEC-TO-IEEE operations are discussed separately in the **IEEE-TO-DEC and DEC-TO-IEEE Operations** section on page 23.

Operations with NANs – NANs arise in two ways: they can be generated by the Am29325 to indicate that an invalid operation has taken place (e.g., infinity times zero), or they can be provided by the user as an input operand. There are two types of NANs: signalling and quiet. These NANs have the formats shown in Figure 7.

Signalling NANs set the invalid operation flag when they appear as an input operand to an operation. They are useful for indicating uninitialized variables, or for implementing user-designed extensions to the operations provided. The ALU never produces a signalling NAN as the final result of an operation.

Quiet NANs are generated for invalid operations. When they appear as an input operand, they are passed through most operations without setting the invalid flag, the floating-point-to-integer conversion operation being the exception.

The sign of any input operand NAN is ignored. All quiet NANs produced as the final result of an operation have a sign of 0.

When a NAN appears as an input operand, the final result of the operation is a quiet NAN that is created by taking the input NAN and forcing bit 22 LOW and bit 21 HIGH. If an operation has two NANs as input operands, the resulting quiet NAN is created using the NAN on the R port.

When a quiet NAN is produced as the final result of an invalid operation whose input operand or operands are not NANs, the resulting NAN will always have the value $7FA00000_{16}$.

The NAN flag will be HIGH whenever an operation produces a NAN as a final result.

Example 1:

Suppose the floating-point addition operation is performed with the following input operands:

R port: $3F800000_{16}$ $(1.0*2^0)$
S port: $7FC12345_{16}$ (signalling NAN)

Result: The signalling NAN on the S port is converted to a quiet NAN by forcing bit 22 LOW and bit 21 HIGH. The operation's final result will be $7FA12345_{16}$. Since one of the two input operands is a signalling NAN, the invalid flag will be HIGH; the NAN flag will also be HIGH.

Example 2:

Suppose the floating-point multiplication operation is performed with the following input operands:

R port: $FFF11111_{16}$ (signalling NAN)
S port: $7FC22222_{16}$ (quiet NAN)

Result: Since both input operands are NANs, the NAN on the R port is chosen for output. In addition to forcing bit 22 LOW, the sign bit (bit 31) is set LOW (bit 21 is already HIGH, and need not be changed). The operation's final result will be $7FB11111_{16}$. Since one of the two input operands is a signalling NAN, the invalid flag is HIGH; the NAN flag will also be HIGH.

Example 3:

Suppose the floating-point subtraction operation is performed with the following input operands:

R port: $FF800001_{16}$ (quiet NAN)
S port: $7F800000_{16}$ $(+\infty)$

Result: To create the final result, the quiet NANs sign bit (bit 31) is forced LOW and bit 21 is forced HIGH (bit 22 is already LOW, and need not be changed). The final result will be $7FA00001_{16}$. The NAN flag will be HIGH.

Operations with Denormalized Numbers – The proposed IEEE standard incorporates denormalized numbers to allow a means of gradual underflow for operations that produce non-zero results too small to be expressed as a normalized floating-point number. The Am29325 does not support gradual underflow. If a floating-point operation produces a non-zero rounded result that is not large enough to be expressed as a normalized floating-point number, the final result will be a zero of the same sign; the inexact, underflow, and zero flags will be HIGH. If an input operand is a denormalized number, the floating-point ALU will assume that operand to be a zero of the same sign.

Operations Producing Overflows – If an operation has a finite input operand or operands, and if the operation produces a rounded result that is too large to fit in the destination format, that operation is said to have overflowed.

A floating-point overflow occurs if an R PLUS S, R MINUS S, R TIMES S, or 2 MINUS S operation with finite input operand(s) produces a result which, after rounding, has a magnitude greater than or equal to 2^{128}. Positive or negative infinity will appear as the final result if the rounded result is positive or negative, respectively, and the overflow and inexact flags will be HIGH.

Integer overflow occurs when the fixed-to-floating-point conversion operation attempts to convert a number which, after rounding, is greater than $2^{31}-1$ or less than -2^{31}. The final result will be quiet NAN $7FA00000_{16}$, and the invalid operation and NAN flags will be HIGH. Note that the overflow and inexact flags remain LOW for integer overflow.

Operations Producing Underflows – If an operation produces a floating-point rounded result having a magnitude too small to be expressed as a normalized floating-point number, but greater than zero, that operation is said to have underflowed. Underflow occurs when an R PLUS S, R MINUS S, or R TIMES S operation produces a result which, after rounding, has a magnitude in the range:

$$0 < \text{magnitude} < 2^{-126}.$$

In such cases, the final result will be $+0$ (00000000_{16}) if the rounded result is non-negative, and -0 (80000000_{16}) if the rounded result is negative. The underflow, inexact, and zero flags will be HIGH.

Underflow does not occur if the destination format is integer. If the infinitely precise result of a floating-point-to-integer conversion has a magnitude greater than 0 and less than 1 but the rounded result is 0, the underflow flag remains LOW.

Operations with Infinities – In most cases, positive and negative infinity are valid input arguments for the R PLUS S, R MINUS S, R TIMES S, and 2 MINUS S operations. Those cases for which infinities are not valid inputs for these operations are listed in the **IEEE Mode Invalid Operations Table** (see next page).

Infinities in IEEE mode can be handled either as projective or affine. The projective mode is selected when PROJ/$\overline{\text{AFF}}$ is HIGH;

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the affine mode is selected when PROJ/$\overline{AFF}$ is LOW. The only differences between the modes that are relevant to Am29325 operation occur during the addition and subtraction of infinities:

Operation	Affine Mode	Projective Mode
$(+\infty)+(+\infty)$	Output $+\infty$	Output $7FA00000_{16}$ (quiet NAN), set invalid and NAN flags
$(-\infty)+(-\infty)$	Output $-\infty$	Output $7FA00000_{16}$ (quiet NAN), set invalid and NAN flags
$(+\infty)-(-\infty)$	Output $+\infty$	Output $7FA00000_{16}$ (quiet NAN), set invalid and NAN flags
$(-\infty)-(+\infty)$	Output $-\infty$	Output $7FA00000_{16}$ (quiet NAN), set invalid and NAN flags

If an R PLUS S, R MINUS S, R TIMES S, or 2 MINUS S operation has infinity as an input operand or operands, the final result, if valid, is presumed to be exact. For example, adding $+\infty$ and 2.0 will produce a final result of $+\infty$; since the result is considered exact, the inexact flag remains LOW.

Invalid Operations – If an input operand is invalid for the operation to be performed, that operation is considered invalid. When an invalid operation is performed, the floating-point ALU produces a quiet NAN as the final result, and the invalid operation flag goes HIGH. **The IEEE Mode Invalid Operations Table** lists the cases for which the invalid flag is HIGH in IEEE mode, and the final results produced for these operations.

IEEE MODE INVALID OPERATIONS TABLE

Operation	Input Operand	Final Result
R PLUS S	$(+\infty) + (-\infty)$ or $(-\infty) + (+\infty)$	$7FA00000_{16}$ (quiet NAN)
R PLUS S	$(+\infty) + (+\infty)$ or $(-\infty) + (-\infty)$ (Note 1)	$7FA00000_{16}$ (quiet NAN)
R MINUS S	$(+\infty) - (+\infty)$ or $(-\infty) - (-\infty)$	$7FA00000_{16}$ (quiet NAN)
R MINUS S	$(+\infty) - (-\infty)$ or $(-\infty) - (+\infty)$ (Note 1)	$7FA00000_{16}$ (quiet NAN)
R TIMES S	$(+0) * (+\infty)$ or $(+0) * (-\infty)$ or $(-0) * (+\infty)$ or $(-0) * (-\infty)$	$7FA00000_{16}$ (quiet NAN)
R PLUS S R MINUS S R TIMES S	R or S is a signalling NAN	(Note 2)
2 MINUS S	S is a signalling NAN	(Note 2)
FP-TO-INT	R is a signalling or quiet NAN	(Note 2)
FP-TO-INT	$R > 2^{31}-1$ or $R < -(2^{31})$	$7FA00000_{16}$ (quiet NAN)

Notes: 1. These cases are invalid in projective mode only.
2. Results for these operations are described in the **Operations with NANs** section.

The Sign Bit

For most floating-point operations, the sign bit of the final result is unambiguous, i.e., there is only one sign bit value that yields a numerically correct result. Operations that produce an infinitely precise result of zero, however, present a problem, as the IEEE floating-point format allows for representation of both +0 and −0. (It should be noted that floating-point operations producing underflow results output a zero of the same sign as the final result, and are therefore unambiguous.) The following rules can be used to determine the signs of zero produced in such cases:

R PLUS S – The operations $+x + (-x)$ and $-x + (+x)$ produce a final result of zero; the sign of the zero is dependent on the rounding mode:

Rounding Mode	Sign of Final Result
Round to nearest	0
Round toward $-\infty$	1
Round toward $+\infty$	0
Round toward 0	0

The operation $+0 + (+0)$ produces a final result of +0; the operation $-0 + (-0)$ produces a final result of −0.

R MINUS S – The operations $+x - (+x)$ and $-x - (-x)$ produce a final result of zero; the sign of the zero is dependent on the rounding mode:

Rounding Mode	Sign of Result
Round to nearest	0
Round toward $-\infty$	1
Round toward $+\infty$	0
Round toward 0	0

The operation $+0 - (-0)$ produces a final result of +0; the operation $-0 - (+0)$ produces a final result of −0.

R TIMES S – The sign of any multiplication result other than a NAN is the exclusive-OR of the signs of the input operands. Therefore, if x is non-negative,

+0 times +x produces a final result of +0,
+0 times −x produces a final result of −0,
−0 times +x produces a final result of −0,
−0 times −x produces a final result of +0.

2 MINUS S – If S equals 2, the final result is −0 for the round toward $-\infty$ mode, and +0 for all other rounding modes.

Rounding

Rounding is performed whenever an operation produces an infinitely precise result that cannot be represented exactly in the destination format. For example, suppose a floating-point operation produces the infinitely precise result

$1.10101010101010101010101\backslash 01 \times 2^3$.

In this example, the fraction portion of the mantissa has twenty-five bits; the IEEE floating-point format can accommodate only twenty-three. The backslash (\) in the mantissa represents the boundary between the first twenty-three bits of the fraction and any remaining bits. Rounding is the process by which this result is approximated by a representation that fits the destination format.

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There are four rounding modes in IEEE mode: round to nearest, round toward $+\infty$, round toward $-\infty$, and round toward 0. The rounding mode is chosen using the rounding mode select lines, RND_0 and RND_1. **The Rounding Mode Select Table** lists the select states needed to obtain the desired rounding mode.

ROUNDING MODE SELECT TABLE

RND_1	RND_0	Rounding Mode
0	0	Round to nearest
0	1	Round toward $-\infty$
1	0	Round toward $+\infty$
1	1	Round toward 0

Round to Nearest – In this rounding mode the infinitely precise result of an operation is rounded to the closest representation that fits in the destination format. If the infinitely precise result is exactly halfway between two representations, it is rounded to the representation having an LSB of zero. Rounding is performed both for floating-point and integer destination formats.

Figure 9 illustrates four examples of the round to nearest process for operations having a floating-point destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be represented exactly in the floating-point format.

Example 1:

In Figure 9(a), the infinitely precise result of an operation is:

$2^{20}+2^{-4}+2^{-5} = 1.00000000000000000000000\ 11 \times 2^{20}$.

The result is rounded to the closest representable floating-point value,

$2^{20}+2^{-3} = 1.00000000000000000000001 \times 2^{20}$.

Example 2:

In Figure 9(b), the infinitely precise result of an operation is:

$2^{20}-2^{-4}+2^{-8} = 1.11111111111111111111111\ 0001 \times 2^{19}$.

This result is rounded to the closest representable floating-point value,

$2^{20}-2^{-4} = 1.11111111111111111111111 \times 2^{19}$.

Example 3:

In Figure 9(c), the infinitely precise result of an operation is:

$-(2^{20}+2^{-3}+2^{-4})$
$= -1.00000000000000000000001\backslash 1 \times 2^{20}$.

This result is exactly halfway between two representable floating-point values. Accordingly, it is rounded to the closest representation with an LSB of zero, or

$-(2^{20}+2*2^{-3}) = -1.00000000000000000000010 \times 2^{20}$.

Example 4:

In Figure 9(d), the infinitely precise result of an operation is:

$2^{20}+3*2^{-3} = 1.00000000000000000000011 \times 2^{20}$.

This result can be represented exactly in the floating-point format, and is left unaltered by the rounding process.

Figure 9. Floating-Point Rounding Examples for Round to Nearest Mode

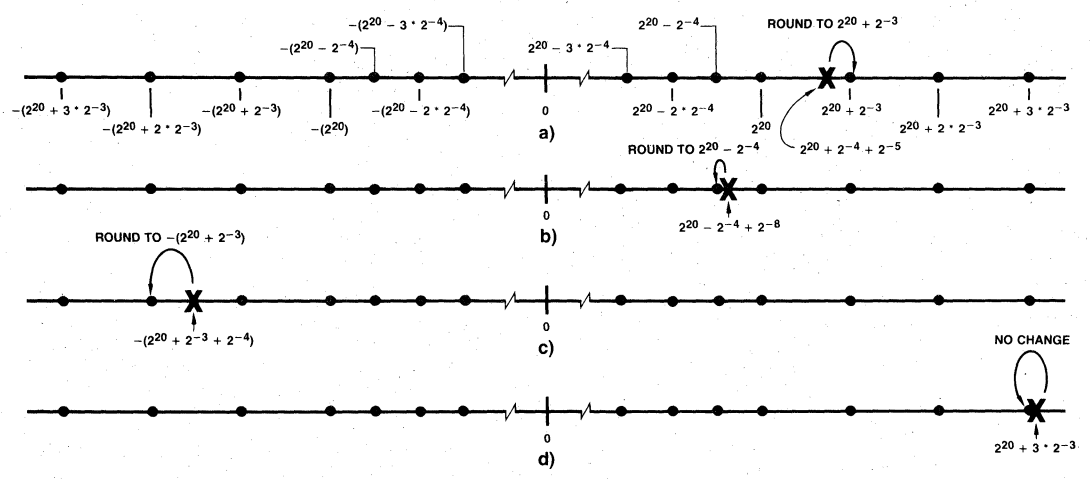

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Figure 10 illustrates four examples of the round to nearest process for operations having an integer destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be represented exactly in the integer format.

Example 1:

In Figure 10(a), the infinitely precise result of an operation is:

$2^{10}-2^{-2}$ = 00...001111111111.11.

The result is rounded to the closest representable integer value, 2^{10} = 00...010000000000.

Example 2:

In Figure 10(b), the infinitely precise result of an operation is:

$2^{10}+2^{0}+2^{-3}$ = 00...010000000001.001.

This result is rounded to the closest representable floating-point value,

$2^{10}+2^{0}$ = 00...010000000001.

Example 3:

In Figure 10(c), the infinitely precise result of an operation is:

$-(2^{10}+2^{0}+2^{-1})$ = 11...101111111110.1.

This result is exactly halfway between two representable integer values. Accordingly, it is rounded to the closest representation with an LSB of zero, or

$-(2^{10}+2*2^{0})$ = 11...101111111110.

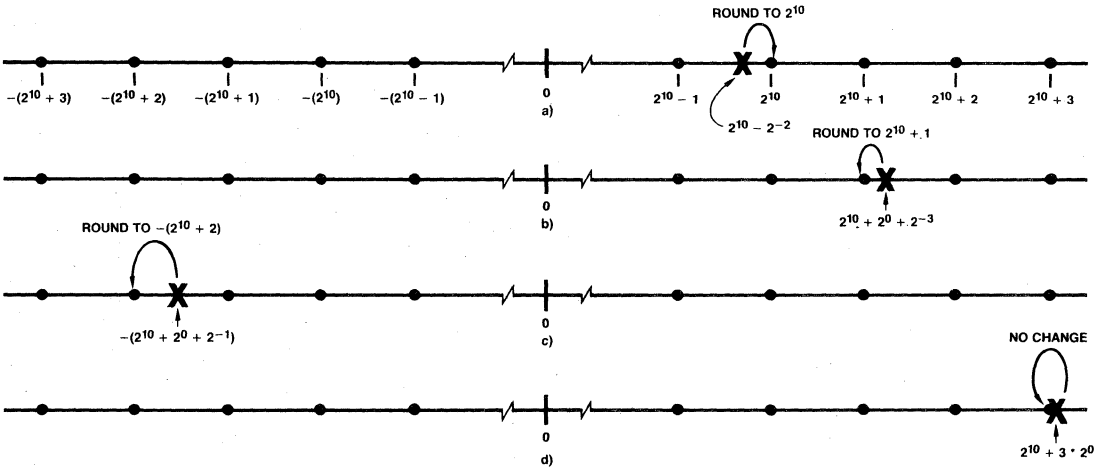
Example 4:

In Figure 10(d), the infinitely precise result of an operation is:

$2^{10}+3*2^{0}$ = 00...010000000011.

This result can be represented exactly in the integer format, and is left unaltered by the rounding process.

Figure 10. Integer Rounding Examples for Round to Nearest Mode



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Round Toward $-\infty$ – In this rounding mode the result of an operation is rounded to the closest representation that is less than or equal to the infinitely precise result, and which fits the destination format. Rounding is performed both for floating-point and integer destination formats.

Figure 11 illustrates four examples of the round toward $-\infty$ process for operations having a floating-point destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be represented exactly in the floating-point format.

Example 1:

In Figure 11(a), the infinitely precise result of an operation is:

$2^{20}+2^{-4}+2^{-5} = 1.00000000000000000000000\backslash 11 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-smaller floating-point representation:

$2^{20} = 1.00000000000000000000000 \times 2^{20}$.

Example 2:

In Figure 11(b), the infinitely precise result of an operation is:

$2^{20}-2^{-4}+2^{-8} = 1.11111111111111111111111\backslash 0001 \times 2^{19}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-smaller floating-point representation:

$2^{20}-2^{-4} = 1.11111111111111111111111 \times 2^{19}$.

Example 3:

In Figure 11(c), the infinitely precise result of an operation is:

$-(2^{20}+2^{-3}+2^{-4})$
$= -1.00000000000000000000001\backslash 1 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-smaller floating-point representation:

$-(2^{20}+2*2^{-3}) = -1.00000000000000000000010 \times 2^{20}$.

Example 4:

In Figure 11(d), the infinitely precise result of an operation is:

$2^{20}+3*2^{-3} = 1.00000000000000000000011 \times 2^{20}$.

This result can be represented exactly in the floating-point format, and is left unaltered by the rounding process.

Figure 11. Floating-Point Rounding Examples for Round Toward $-\infty$ Mode

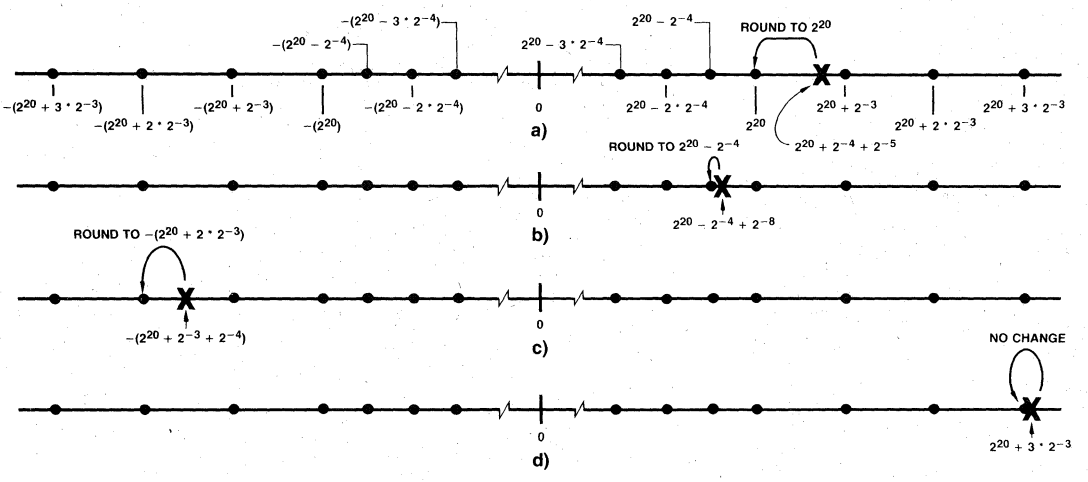

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Figure 12 illustrates four examples of the round toward $-\infty$ process for operations having an integer destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be exactly represented in the integer format.

Example 1:

In Figure 12(a), the infinitely precise result of an operation is:

$2^{10}-2^{-2}$ = 00...001111111111.11.

The result is rounded to the next-smaller representable integer value,

$2^{10}-2^{0}$ = 00...001111111111.

Example 2:

In Figure 12(b), the infinitely precise result of an operation is:

$2^{10}+2^{0}+2^{-3}$ = 00...010000000001.001.

This result is rounded to the next-smaller representable integer value,

$2^{10}+2^{0}$ = 00...010000000001.

Example 3:

In Figure 12(c), the infinitely precise result of an operation is:

$-(2^{10}+2^{0}+2^{-1})$ = 11...101111111110.1.

This result is rounded to the next-smaller representable integer value:

$-(2^{10}+2*2^{0})$ = 11...101111111110.

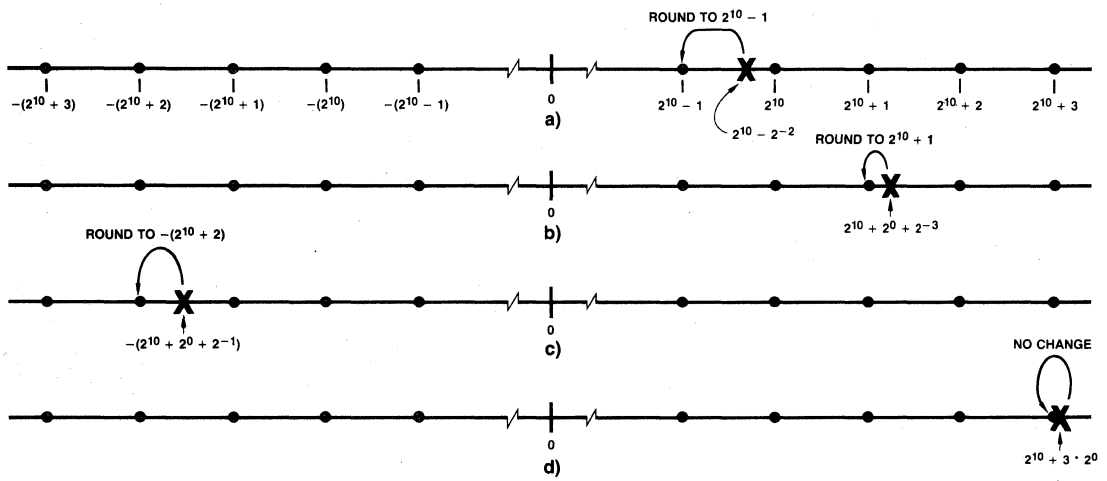
Example 4:

In Figure 12(d), the infinitely precise result of an operation is:

$2^{10}+3*2^{0}$ = 00...010000000011.

This result can be represented exactly in the integer format, and is unaltered by the rounding process.

Figure 12. Integer Rounding Examples for Round Toward $-\infty$ Mode



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Round Toward $+\infty$ – In this rounding mode the result of an operation is rounded to the closest representation that is greater than or equal to the infinitely precise result, and which fits the destination format. Rounding is performed both for floating-point and integer destination formats.

Figure 13 illustrates four examples of the round toward $+\infty$ process for operations having a floating-point destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be represented exactly in the floating-point format.

Example 1:

In Figure 13(a), the infinitely precise result of an operation is:

$2^{20}+2^{-4}+2^{-5} = 1.00000000000000000000000\backslash 11 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-larger floating-point representation:

$2^{20}+2^{-3} = 1.00000000000000000000001 \times 2^{20}$.

Example 2:

In Figure 13(b), the infinitely precise result of an operation is:

$2^{20}-2^{-4}+2^{-8} = 1.11111111111111111111111\backslash 0001 \times 2^{19}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-larger floating-point representation:

$2^{20} = 1.00000000000000000000000 \times 2^{20}$.

Example 3:

In Figure 13(c), the infinitely precise result of an operation is:

$-(2^{20}+2^{-3}+2^{-4})$
$= -1.00000000000000000000001\backslash 1 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to the next-larger floating-point representation:

$-(2^{20}+2^{-3}) = -1.00000000000000000000001 \times 2^{20}$.

Example 4:

In Figure 13(d), the infinitely precise result of an operation is:

$2^{20}+3*2^{-3} = 1.00000000000000000000011 \times 2^{20}$.

This result can be represented exactly in the floating-point format – no rounding takes place.

Figure 13. Floating-Point Rounding Examples for Round Toward $+\infty$ Mode

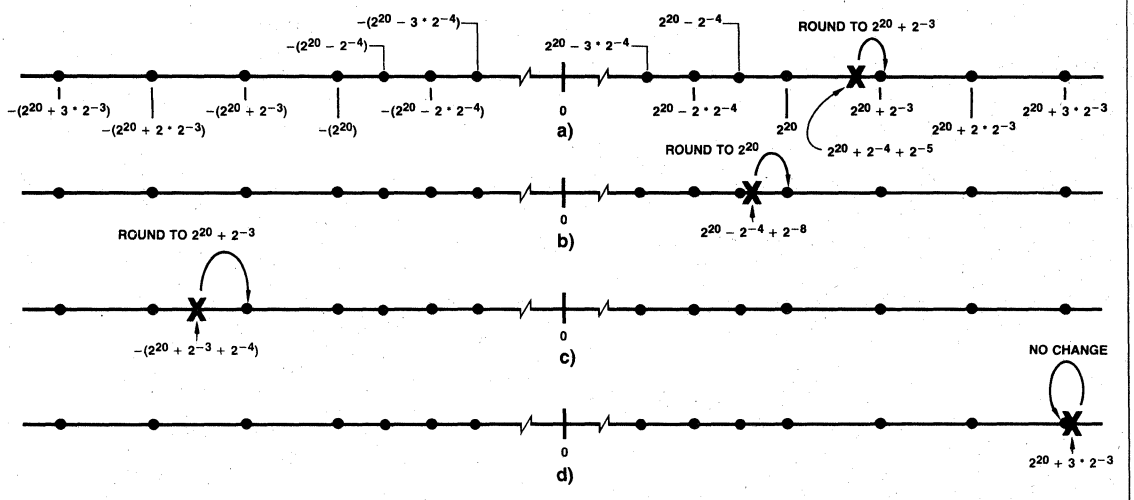

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Figure 14 illustrates four examples of the round toward $+\infty$ process for operations having an integer destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be exactly represented in the integer format.

Example 1:

In Figure 14(a), the infinitely precise result of an operation is:

$2^{10}-2^{-2}$ = 00...001111111111.11.

The result is rounded to the next-larger representable integer value,

2^{10} = 00...010000000000.

Example 2:

In Figure 14(b), the infinitely precise result of an operation is:

$2^{10}+2^{0}+2^{-3}$ = 00...010000000001.001.

This result is rounded to the next-larger representable integer value,

$2^{10}+2*2^{0}$ = 00...010000000010.

Example 3:

In Figure 14(c), the infinitely precise result of an operation is:

$-(2^{10}+2^{0}+2^{-1})$ = 11...101111111110.1

This result is rounded to the next-larger representable integer value:

$-(2^{10}+2^{0})$ = 11...1011111111110.

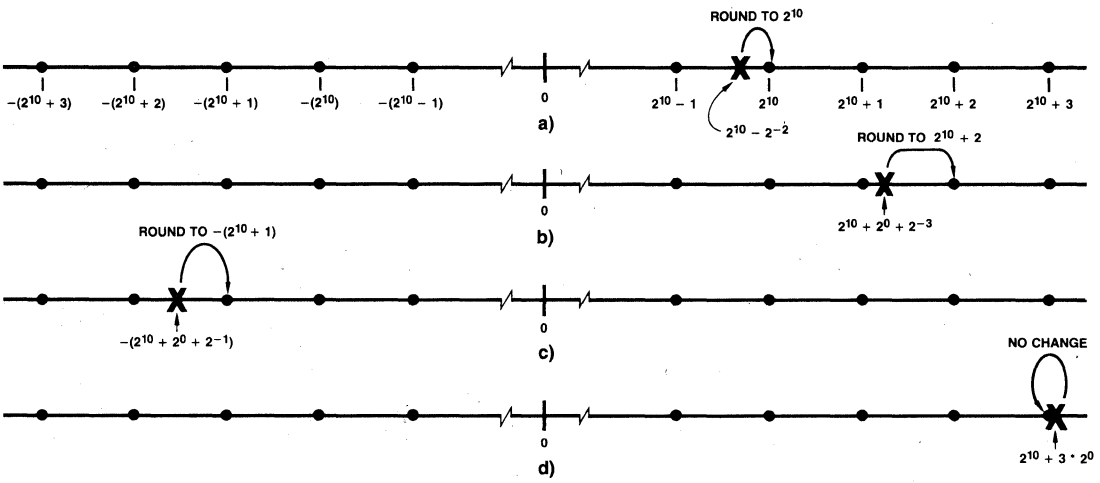
Example 4:

In Figure 14(d), the infinitely precise result of an operation is:

$2^{10}+3*2^{0}$ = 00...010000000011.

This result can be represented exactly in the integer format – no rounding takes place.

Figure 14. Integer Rounding Examples for Round Toward + ∞ Mode



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Round Toward 0 – In this rounding mode the result of an operation is rounded to the closest representation whose magnitude is less than or equal to the infinitely precise result, and which fits the destination format. Rounding is performed both for floating-point and integer destination formats.

Figure 15 illustrates four examples of the round toward 0 process for operations having a floating-point destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be represented exactly in the floating-point format.

Example 1:

In Figure 15(a), the infinitely precise result of an operation is:

$2^{20}+2^{-4}+2^{-5} = 1.00000000000000000000000\backslash 11 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to:

$2^{20} = 1.00000000000000000000000 \times 2^{20}$.

Example 2:

In Figure 15(b), the infinitely precise result of an operation is:

$2^{20}-2^{-4}+2^{-8} = .1.11111111111111111111111\backslash 001 \times 2^{19}$.

This result cannot be represented exactly in floating-point format, and is rounded to:

$2^{20}-2^{-4} = 1.11111111111111111111111 \times 2^{19}$.

Example 3:

In Figure 15(c), the infinitely precise result of an operation is:

$-(2^{20}+2^{-3}+2^{-4})$
$= -1.00000000000000000000001\backslash 1 \times 2^{20}$.

This result cannot be represented exactly in floating-point format, and is rounded to:

$-(2^{20}+2^{-3}) = -1.00000000000000000000001 \times 2^{20}$.

Example 4:

In Figure 15(d), the infinitely precise result of an operation is:

$2^{20}+3*2^{-3} = 1.00000000000000000000011 \times 2^{20}$.

This result can be represented exactly in the floating-point format, and is unaffected by the rounding process.

Figure 15. Floating-Point Rounding Examples for Round Toward 0 Mode

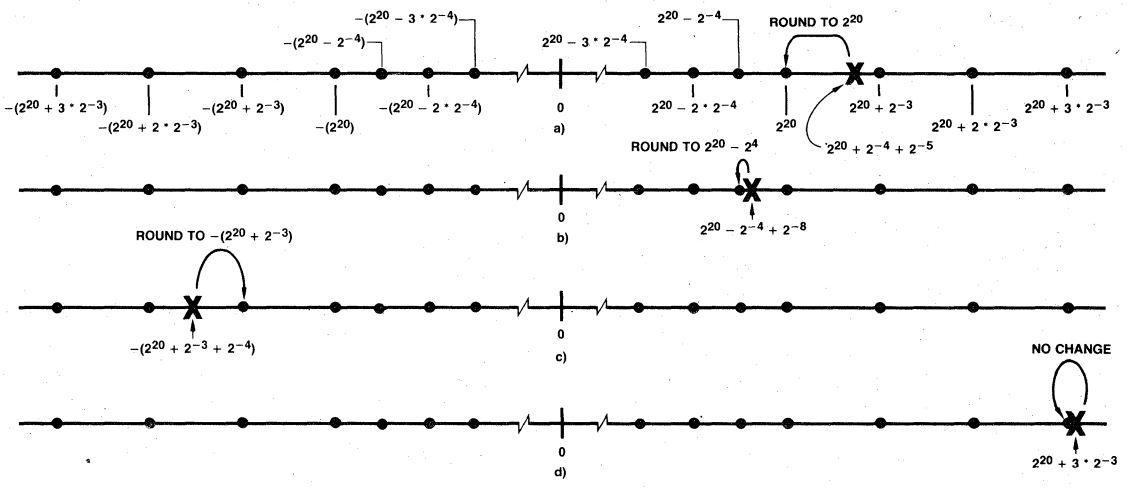

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Figure 16 illustrates four examples of the round toward 0 process for operations having an integer destination format. The infinitely precise result of an operation is represented by an X on the number line; the black dots on the number line indicate those values that can be exactly represented in the integer format.

Example 1:

In Figure 16(a), the infinitely precise result of an operation is:

$2^{10}-2^{-2}$ = 00...001111111111.11.

The result is rounded to:

$2^{10}-2^{0}$ = 00...001111111111.

Example 2:

In Figure 16(b), the infinitely precise result of an operation is:

$2^{10}+2^{0}+2^{-3}$ = 00...010000000001.001.

The result is rounded to:

$2^{10}+2^{0}$ = 00...010000000001.

Example 3:

In Figure 16(c), the infinitely precise result of an operation is:

$-(2^{10}+2^{0}+2^{-1})$ = 11...101111111110.1.

This result is rounded to:

$-(2^{10}+2^{0})$ = 11...101111111111.

Example 4:

In Figure 16(d), the infinitely precise result of an operation is:

$2^{10}+3*2^{0}$ = 00...010000000011.

This result can be represented exactly in the integer format, and is unaffected by the rounding process.

Flag Operation

The Am29325 generates six status flags to monitor floating-point processor operation. The following is a summary of flag conventions in IEEE mode:

Invalid Operation Flag – The invalid operation flag is HIGH when an input operand is invalid for the operation to be performed. **The IEEE Mode Invalid Operations Table** on page 12 lists the cases for which the invalid operation flag is HIGH in IEEE mode, and the corresponding final result. In cases where the invalid operation flag is HIGH, the overflow, underflow, zero, and inexact flags are LOW; the NAN flag will be HIGH.

Overflow Flag – The overflow flag is HIGH if an R PLUS S, R MINUS S, R TIMES S, or 2 MINUS S operation with finite input operand(s) produces a result which, after rounding, has a magnitude greater than or equal to 2^{128}. The final result will be $+\infty$ or $-\infty$.

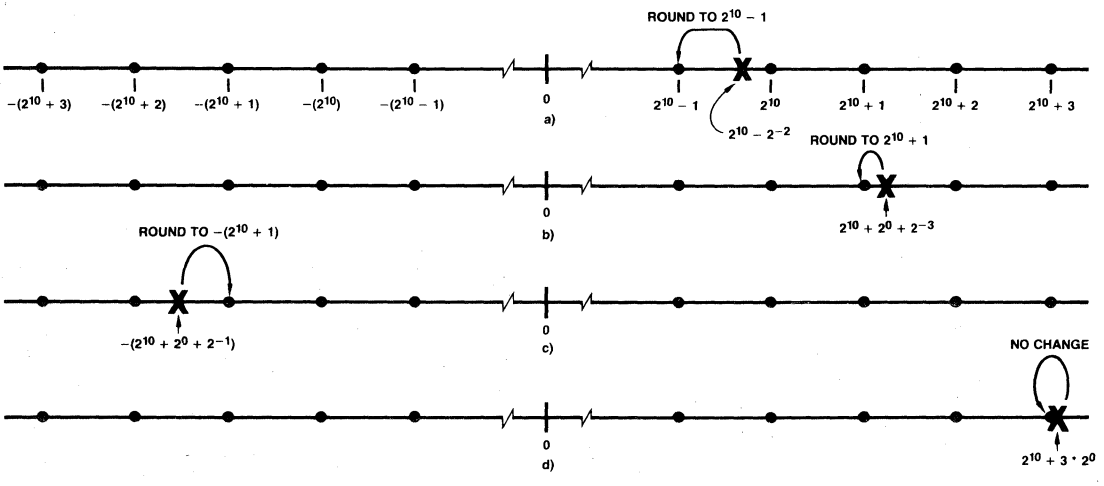
Underflow Flag – The underflow flag is HIGH if an R PLUS S, R MINUS S, or R TIMES S operation produces a result which, after rounding, has a magnitude in the range:

$$0 < \text{magnitude} < 2^{-126}.$$

The final result will be +0 (00000000_{16}) if the rounded result is non-negative, and −0 (80000000_{16}) if the rounded result is negative.

Inexact Flag – The inexact flag is HIGH if the final result of an R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, INT-TO-FP, or FP-TO-INT operation is not equal to the infinitely precise result. Note that if the underflow or overflow flag is HIGH, the inexact flag will also be HIGH.

Figure 16. Integer Rounding Examples for Round Toward 0 Mode



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Zero Flag – The zero flag is HIGH if the final result of an operation is zero. For operations producing an IEEE floating-point number, the flag accompanies outputs +0 (00000000_{16}) and −0 (80000000_{16}). For operations producing an integer, the flag accompanies the output 0 (00000000_{16}).

NAN Flag – The NAN flag is HIGH if an R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, or FP-TO-INT operation produces a NAN as a final result.

OPERATION IN DEC MODE

When input signal IEEE/$\overline{\text{DEC}}$ is LOW, the DEC mode of operation is selected. In this mode the Am29325 uses the single-precision floating-point format (floating F) set forth in Digital Equipment Corporation's VAX Architecture Manual. In addition, the DEC mode complies with most other aspects of single-precision floating-point operation outlined in the manual – differences are discussed in **Appendix B.**

DEC Floating-Point Format

The DEC single-precision floating-point word is thirty-two bits wide, and is arranged in the format shown in Figure 17. The floating-point word is divided into three fields: a single-bit sign, an eight-bit biased exponent, and a 23-bit fraction.

The sign bit indicates the sign of the floating-point number's value. Non-negative values have a sign of 0, negative values a sign of 1.

The biased exponent is an eight-bit unsigned integer field representing a multiplicative factor of some power of two. The bias value is 128. If, for example, the multiplicative factor for a floating-point number is to be 2^a, the value of the biased exponent would be a+128; a is called the true exponent.

The fraction is a 23-bit unsigned fractional field containing the 23 least-significant bits of the floating-point number's 24-bit mantissa. The weight of this field's most significant bit is 2^{-2}; the weight of the least-significant bit is 2^{-24}.

A floating-point number is evaluated or interpreted per the following conventions:

let s = sign bit
e = biased exponent
f = fraction

if e = 0 and s = 0 . . . value = 0

if e = 0 and s = 1 . . . value = DEC reserved operand

if $0 < e \leq 255$ . . value = $(-1)^{s} * (2^{e-128}) * (.1f)$ (normalized number)

Zero – The value zero always has a sign of zero.

DEC Reserved Operand – A DEC reserved operand does not represent a numeric value, but is interpreted as a signal or symbol. DEC reserved operands are used to indicate invalid operations and operations whose results have overflowed the destination format. They may also be used to pass symbolic information from one calculation to another.

Normalized Number – A normalized number represents a quantity with magnitude greater than or equal to 2^{-128} but less than 2^{127}.

Example 1:

The number +3.5 can be represented in floating-point format as follows:

$+3.5 = 11.1_2 \times 2^0$
$= .111_2 \times 2^2$

sign = 0

biased exponent = $2_{10} + 128_{10} = 130_{10}$
$= 10000010_2$

fraction = $11000000000000000000000_2$
(the leading 1 is implied in the format)

Concatenating these fields produces the floating-point word 41600000_{16}.

Example 2:

The number −11.375 can be represented in floating-point format as follows:

$-11.375 = -1011.011_2 \times 2^0$
$= -.1011011_2 \times 2^4$

sign = 1

biased exponent = $4_{10} + 128_{10} = 132_{10}$
$= 10000100_2$

fraction = $01101100000000000000000_2$
(the leading 1 is implied in the format)

Concatenating these fields produces the floating-point word $C2360000_{16}$.

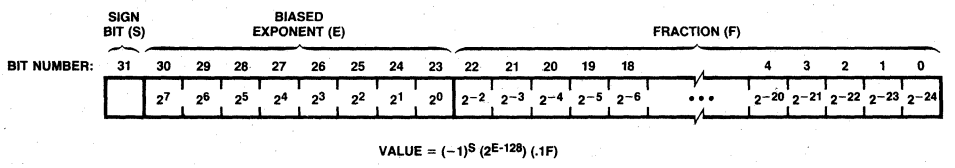
DEC Mode Integer Format

DEC mode integer format is identical to that of the IEEE mode. Integer numbers are represented as 32-bit, two's complement words; Figure 7 depicts the integer format. The integer word can represent a range of integer values from -2^{31} to $2^{31}-1$.

Operations

All eight floating-point ALU operations discussed in the General Description section can be performed in DEC mode.

Figure 17. DEC-Mode Floating-Point Format



VALUE = $(-1)^S (2^{E-128}) (.1F)$

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Various exceptional aspects of the R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, INT-TO-FP, and FP-TO-INT operations for this mode are described below. The IEEE-TO-DEC and DEC-TO-IEEE operations are discussed separately in the **IEEE-TO-DEC and DEC-TO-IEEE Operations** section on page 23.

Operations with DEC Reserved Operands – DEC reserved operands arise in two ways: they can be generated by the Am29325 to indicate that an invalid operation or floating-point overflow has taken place, or they can be provided by the user as an input operand.

When a DEC reserved operand appears as an input operand, the final result of the operation is the same DEC reserved operand. If an operation has two DEC reserved operands as inputs, the DEC reserved operand on the R port becomes the final result.

The NAN flag will be HIGH whenever an operation produces a DEC reserved operand as a final result.

Example 1:

Suppose the floating-point addition operation is performed with the following input operands:

R port: 40800000_{16} $(0.1*2^1)$
S port: 80012345_{16} (DEC reserved operand)

Result: This operation produces the DEC reserved operand on the S port, 80012345_{16}, as the final result. The NAN flag will be HIGH.

Example 2:

Suppose the floating-point multiplication operation is performed with the following input operands:

R port: 80765432_{16} (DEC reserved operand)
S port: 80000001_{16} (DEC reserved operand)

Result: Since both input operands are DEC reserved operands, the operand on the R port, 80765432_{16}, is the final result of the operation. The NAN flag will be HIGH.

Operations Producing Overflows – If an operation produces a rounded result that is too large to fit in the destination format, that operation is said to have overflowed.

A floating-point overflow occurs if a R PLUS S, R MINUS S, R TIMES S, or 2 MINUS S operation with finite input operand(s) produces a result which, after rounding, has a magnitude greater than or equal to 2^{127}. The final result in such cases will be DEC reserved operand 80000000_{16}; the overflow, inexact, and NAN flags will be HIGH.

Integer overflow occurs when the fixed-to-floating-point conversion operation attempts to convert to integer a floating-point number which, after rounding, is greater than $2^{31}-1$ or less than -2^{31}. The final result in such cases will be DEC reserved operand 80000000_{16}; the invalid operation flag will be HIGH. Note that the overflow and inexact flags remain LOW for integer overflow.

Operations Producing Underflows – If an operation produces a floating-point result which, after rounding, has a magnitude too small to be expressed as a normalized floating-point number, but greater than zero, that operation is said to have underflowed. Underflow occurs when an R PLUS S, R MINUS S, or R TIMES S operation produces a result which, after rounding, has magnitude:

$$0 < \text{magnitude} < 2^{-128}.$$

The final result in such cases will be 0 (00000000_{16}). The underflow, inexact, and zero flags will be HIGH.

Underflow does not occur if the destination format is integer. If the infinitely precise result of a floating-point-to-integer conversion has a magnitude greater than 0 and less than 1, but the rounded result is 0, the underflow flag remains LOW.

Invalid Operations – If an input operand is invalid for the operation to be performed, that operation is considered invalid. In DEC mode, there are only two invalid operations:

- Performing a floating-point-to-integer conversion on a value too large to be expressed as a 32-bit integer. In this case the final result will be DEC reserved operand 80000000_{16}, and the invalid operation and NAN flags will be HIGH.
- Performing a floating-point-to-integer conversion on a DEC reserved operand. In this case the final result will be the input DEC reserved operand, and the invalid operation and NAN flags will be HIGH.

3

Sign Bit

For all operations producing a DEC floating-point result, the sign bit of the final result is unambiguous, i.e., there is only one sign bit value that yields a numerically correct result.

Rounding

There are four rounding modes for DEC operation: round to nearest, round toward $+\infty$, round toward $-\infty$, and round toward 0. The round toward $+\infty$, round toward $-\infty$, and round toward 0 modes are performed in a manner identical to that for IEEE operation; refer to the **Rounding** section under **Operation in IEEE Mode** on page 12. The round to nearest mode is similar to that for IEEE operation, but differs in one respect: for the case in which the infinitely-precise result of an operation is exactly halfway between two representable values, DEC round to nearest mode rounds to the value with the larger magnitude, rather than to the value whose LSB is 0.

Flag Operation

The Am29325 generates six status flags to monitor floating-point processor operation. The following is a summary of flag operation in DEC mode:

Invalid Operation Flag – The invalid operation flag is HIGH if the FP-TO-INT operation is performed on a floating-point number too large to be converted to an integer, or on a DEC reserved operand. If the FP-TO-INT operation is performed on a floating-point number too large to be converted to integer, the final result is the DEC reserved operand 80000000_{16}. If the FP-TO-INT operation is performed on a DEC reserved operand, that operand becomes the final result.

Overflow Flag – The overflow flag is HIGH if an R PLUS S, R MINUS S, R TIMES S, or 2 MINUS S operation produces a result which, after rounding, has a magnitude greater than or equal to 2^{127}. The final result will be the DEC reserved operand 80000000_{16}.

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Underflow Flag – The underflow flag is HIGH if an R PLUS S, R MINUS S, or R TIMES S operation produces a result which, after rounding, has a magnitude in the range:

$$0 < \text{magnitude} < 2^{-128}.$$

The final result will be 0 (00000000_{16}) in such cases.

Inexact Flag – The inexact flag is HIGH if the final result of an R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, INT-TO-FP, or FP-TO-INT operation is not equal to the infinitely precise result. Note that if the underflow or overflow flag is HIGH, the inexact flag will also be HIGH.

Zero Flag – The zero flag is HIGH if the final result of an operation is zero. For operations producing an integer or a DEC floating-point number, the flag accompanies the output 0 (00000000_{16}). (It should be noted that any operation producing a floating-point 0 in DEC mode will output 00000000_{16}.)

NAN Flag – The NAN flag is HIGH if an R PLUS S, R MINUS S, R TIMES S, 2 MINUS S, or FP-TO-INT operation produces a DEC reserved operand as the final result.

IEEE-TO-DEC AND DEC-TO-IEEE OPERATIONS

The IEEE-TO-DEC and DEC-TO-IEEE operations are used to convert floating-point numbers between the IEEE and DEC formats. Both operations work in a manner independent of the IEEE/$\overline{\text{DEC}}$ mode control.

IEEE-TO-DEC Conversion

This operation converts an IEEE floating-point number to DEC floating-point format. Most conversions are exact; in no case does the round mode have any affect on the final result. There are, however, a few exceptional cases:

a.) If the IEEE floating-point input has a magnitude greater than or equal to 2^{127}, it is too large to be represented by a DEC floating-point number. The final result will be the DEC reserved operand 80000000_{16}; the overflow, inexact, and NAN flags will be HIGH.
b.) If the IEEE floating-point input is a NAN, the final result will be the DEC reserved operand 80000000_{16}; the invalid and NAN flags will be HIGH.
c.) If the IEEE floating-point input is a denormalized number, the final result will be a DEC 0 (00000000_{16}); the zero flag will be HIGH.
d.) If the IEEE floating-point input is +0 or −0, the final result will be a DEC 0 (00000000_{16}); the zero flag will be HIGH.

DEC-TO-IEEE Conversion

This operation converts a DEC floating-point number to IEEE floating-point format. Most conversions are exact; in no case does the round mode have any affect on the final result. There are, however, a few exceptional cases:

a.) If the DEC floating-point input is not 0, but has a magnitude less than 2^{-126}, it is too small to be expressed as a normalized IEEE floating-point number. The final result will be an IEEE floating-point 0 having the same sign as the input (00000000_{16} for positive inputs and 80000000_{16} for negative inputs); the underflow, inexact, and zero flags will be HIGH.
b.) If the DEC floating-point input is a DEC reserved operand, the final result will be quiet NAN $7FA00000_{16}$; the invalid operation and NAN flags will be HIGH.
c.) If the DEC floating-point input is 0, the final result will be IEEE floating-point +0 (00000000_{16}); the zero flag will be HIGH.

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APPENDIX A:

Differences Between the IEEE Proposed Standard for Binary Floating-Point Arithmetic and the Am29325's IEEE Mode

When operated in IEEE mode, the Am29325 High-speed Floating-Point Processor complies with the single-precision portion of the IEEE Proposed Standard for Binary Floating-Point Arithmetic (P754, draft 10.0) in most respects. There are, however, several differences:

Denormalized Numbers

The Am29325 does not handle denormalized numbers. A denormalized input will be converted to a zero of the same sign before the specified operation takes place. The operation proceeds in exactly the same manner as if the input were +0 or −0, producing the same numerical result and flags.

If the result of an operation, after rounding, has a magnitude smaller than 2^{-126}, the result is replaced by a zero of the same sign.

Representation of Overflows

In some rounding modes, the proposed IEEE standard requires that overflows be represented as the format's most positive or most negative finite number. In particular:

- When rounding toward 0, all overflows should produce a result of the largest representable finite number with the sign of the intermediate result.
- When rounding toward $-\infty$, all positive overflows should produce a result of the largest representable positive finite number.
- When rounding toward $+\infty$, all negative overflows should produce a result of the largest representable negative finite number.

The Am29325, however, always represents positive overflows as $+\infty$ and negative overflows as $-\infty$, regardless of rounding mode.

Projective Mode

The proposed IEEE standard provides only for an affine mode to control the handling of infinities. The Am29325 provides both affine and projective modes; the desired mode can be selected by the user.

Traps

The proposed IEEE standard stipulates that the user be able to request a trap on any exception. The Am29325 does not support trap operation, and behaves as if traps are disabled.

Resetting of Flags

The proposed IEEE standard states that once an exception flag has been set, it is reset only at the user's request. The Am29325's flags, however, reflect the status of the most recent operation.

Generation of the Underflow Flag

The proposed IEEE standard suggests several possible criteria for determining if underflow occurs. These criteria generate underflow flags that differ in subtle ways. The underflow criteria chosen for the Am29325 stipulate that underflow occurs if:

a) the rounded result of an operation has a magnitude in the range:

$$0 < \text{magnitude} < 2^{-126}$$

and

b) the final result is not equal to the infinitely precise result.

Since the Am29325 never produces a denormalized number as the final result of a calculation, condition (b) is true whenever (a) is true. Note, then, that the operation of the Am29325's underflow flag is somewhat different than that of an "IEEE standard" system using the same underflow criteria. For example, if an operation should produce an infinitely precise result that is exactly 2^{-127}, an "IEEE standard" system would produce that value as the final result, expressed as a denormalized number. Since that system's final result is exact, the underflow flag would remain LOW. The Am29325, on the other hand, would output zero; since its final result is not exact, the underflow flag would be HIGH.

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APPENDIX B:

Differences Between DEC VAX and Am29325 DEC Mode

Operation in DEC mode complies with most aspects of single-precision floating-point operation outlined in the Digital Equipment Corporation's VAX Architecture Manual. However, there are some differences that should be noted:

Format

The Am29325's DEC format is:

sign – bit 31
exponent – bits 30 – 23
mantissa – 22 – 0

The VAX format is:

sign – bit 15
exponent – 14 – 7
mantissa – bits 6 – 0, bits 31 – 16.

In both cases, fields are listed from MSB to LSB, with bit 31 the MSB of the 32-bit word. The Am29325's DEC format can be converted to VAX format by swapping the 16 LSBs and 16 MSBs of the 32-bit word.

Flags vs. Exceptions

In DEC VAX operation, certain unusual conditions arising during system operation may incur an exception, or an indication to the operating system that special handling is needed.

The VAX recognizes a number of arithmetic exceptions. The following exceptions are relevant to the operations supported by the Am29325:

Integer overflow trap – indicates that the last operation produced an integer overflow. The LSBs of the correct result are stored in the destination operand.

Floating-point overflow trap/fault – indicates that the last operation produced, after normalization and rounding, a floating-point number with magnitude greater than or equal to 2^{127}. A trap replaces the destination operand with the DEC reserved operand 80000000_{16}; a fault leaves the destination operand unchanged.

Floating-point underflow trap/fault – indicates that the last operation produced, after normalization and rounding, a floating-point number with magnitude less than 2^{-128}. A trap replaces the destination operand with zero; a fault leaves the destination operand unchanged.

Reserved operand fault – indicates that the last operation had a reserved operand as an input. The destination operand is unchanged.

The Am29325 does not directly support DEC traps and faults. Rather, it indicates unusual conditions by setting one or more of the six status flags HIGH. Table d2 describes flag operation in DEC mode.

Integer Overflow

In cases of integer overflow, the VAX signals the integer overflow trap and stores the LSBs of the correct result. The Am29325 sets the invalid operation flag and outputs the DEC reserved operand 80000000_{16}.

Floating-Point Underflow/Overflow Operation

The VAX Architecture Manual specifies the action to be taken on the destination operand when floating-point underflow or overflow is encountered. The Am29325 has no immediate control over this destination operand, as it resides somewhere off-chip, either in a register or memory location. This isn't so much a difference between the VAX specification and Am29325 operation as it is a difference in scope.

The Am29325 responds to floating-point underflow by producing a final result of 0 (00000000_{16}); the underflow, inexact, and zero flags will be HIGH. It responds to floating-point overflow by producing the DEC reserved operand 80000000_{16} as the final result; the overflow, inexact, and NAN flags will be HIGH.

Handling of DEC Reserved Operands

If an operation has a DEC reserved operand as an input, the Am29325 will produce that operand as the final result. If an operation has two input arguments and both are DEC reserved operands, the operand on port R becomes the final result. For the VAX, operations with a DEC reserved operand input or inputs do not modify the destination operand. As mentioned above, control of the destination operand is beyond the scope of the Am29325's operation.

Inexact Flag

The Am29325 provides an inexact flag to indicate that the final result produced by an operation is not equal to the infinitely precise result. The VAX does not provide this flag.

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APPENDIX C:

Performing Floating-Point Division on the Am29325

While the Am29325 does not have a floating-point division instruction, it can be used to evaluate reciprocals. The division:

$$C = A/B$$

can then be performed by evaluating:

$$C = A*(1/B).$$

Only a modest amount of external hardware is needed to implement the reciprocal function.

The technique for calculating reciprocals is based on the Newton-Raphson method for obtaining the roots of an equation. The roots of equation:

$$F(x) = 0$$

can be found by iteratively evaluating the equation

$$x_{i+1} = x_i - F(x_i)/F'(x_i).$$

The process begins by making a guess as to the value of x_i, and using this guess or "seed" value to perform the first iteration. Iterations are continued until the root is evaluated to the desired accuracy. The number of iterations needed to achieve a given accuracy depends both on the accuracy of the seed value and the nature of F(x).

Now consider the equation

$$F(x) = (1/x) - B.$$

The root of F(x) is 1/B. The reciprocal of B, then, can be found by using the Newton-Raphson method to find the root of F(x). The iterative equation for finding the root is

$$\begin{aligned} x_{i+1} &= x_i - F(x_i)/F'(x_i) \\ &= x_i - (1/x_i - B)/-(x_i)^{-2} \\ &= x_i\,(2 - B*x_i). \end{aligned}$$

It can be shown that, in order for this iterative equation to converge, the seed value x_0 must fall in the range

$$0 < x_0 < 2/B \quad \text{if } B > 0$$

or $$2/B < x_0 < 0 \quad \text{if } B < 0.$$

For example, if the reciprocal of 3 is to be evaluated, the seed value must be between 0 and 2/3.

The error of x_i reduces quadratically; that is, if the error of x_i is e, the error is reduced to order e^2 by the next iteration. The number of bits of accuracy in the result, then, roughly doubles after every iteration. While this is only an approximation of the actual error produced, it is a handy rule-of-thumb for determining the number of iterations needed to produce a result of a certain accuracy, given the accuracy of the seed.

Example 1:

Find the reciprocal of 7.25.

Solution:

The seed value must fall in the range

$$0 < x_0 < 2/7.25$$

or $$0 < x_0 < .275862.$$

Suppose x_0 is chosen to be .1

Iteration 1: $x_1 = x_0\,(2 - B*x_0)$
$= .1(2-(7.25)\,(.1))$
$= .1275$

Iteration 2: $x_2 = x_1\,(2 - B*x_1)$
$= .1275(2-(7.25)\,(.1275))$
$= .1371421875$

Iteration 3: $x_3 = x_2(2 - B*x_2)$
$= .1371421875*$
$(2-(7.25)\,(.1371421875))$
$= .1379265230$

The actual value of 1/7.25, to ten decimal places, is .1379310345.

The error after each iteration is:

Iteration	x_i	Error to Ten Places
0	.1	−0.0379310345
1	.1275	−0.0104310345
2	.1371421875	−0.0007888470
3	.1379265230	−0.0000045115

Example 2:

Find the reciprocal of −.3.

Solution:

The seed value must fall in the range

$$2/(-.3) < x_0 < 0$$

or $$-6.66 < x_0 < 0.$$

Suppose x_0 is chosen to be −2.0.

Iteration 1: $x_1 = x_0(2 - B*x_0)$
$= -2.0(2-(-.3)\,(-2.0))$
$= -2.8$

Iteration 2: $x_2 = x_1\,(2 - B*x_1)$
$= -2.8(2-(-.3)\,(-2.8))$
$= -3.248$

Iteration 3: $x_3 = x_2(2 - B*x_2)$
$= -3.248(2-(-.3)\,(-3.248))$
$= -3.3311488$

Iteration 4: $x_4 = x_3(2 - B*x_3)$
$= -3.3311488*$
$(2-(-.3)\,(-3.3311488))$
$= -3.333331902$

The actual value of 1/(−.3), to ten decimal places, is −3.333333333.

The error after each iteration is:

i	x_i	Error to Ten Places
0	−2.0	1.333333333
1	−2.8	0.533333333
2	−3.248	0.085333333
3	−3.3311488	0.002184533
4	−3.333331902	0.000001431

In order to implement the Newton-Raphson method on the Am29325, some means is needed to generate the seed used in the first iteration. One approach is to place a hardware seed look-up table between the R bus and the Am29325; see Table c1. A more detailed diagram of the look-up table appears in Figure c2.

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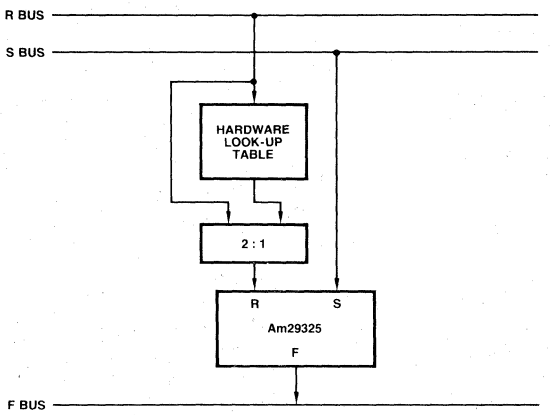
TABLE c1. CONTENTS OF THE SEED EXPONENT PROM

DEC		IEEE	
Address (16)	**Data (16)**	**Address (16)**	**Data (16)**
000	(Note 1)	100	FD
001	(Note 1)	101	FC
002	FF	102	FB
003	FE	103	FA
004	FD	104	F9
005	FC	105	F8
006	FB	106	F7
007	FA	107	F6
008	F9	108	F5
009	F8	109	F4
00A	F7	10A	F3
00B	F6	10B	F2
00C	F5	10C	F1
00D	F4	10D	F0
00E	F3	10E	EF
00F	F2	10F	EE
010	F1	110	ED
011	F0	111	EC
012	EF	112	EB
.	.	.	.
.	.	.	.
.	.	.	.
0EE	13	1EE	0F
0EF	12	1EF	0E
0F0	11	1F0	0D
0F1	10	1F1	0C
0F2	0F	1F2	0B
0F3	0E	1F3	0A
0F4	0D	1F4	09
0F5	0C	1F5	08
0F6	0B	1F6	07
0F7	0A	1F7	06
0F8	09	1F8	05
0F9	08	1F9	04
0FA	07	1FA	03
0FB	06	1FB	02
0FC	05	1FC	01
0FD	04	1FD	(Note 2)
0FE	03	1FE	(Note 2)
0FF	02	1FF	(Note 2)

Notes: 1. The reciprocals of these numbers are too large to be represented in DEC format.
2. The reciprocals of these numbers are too small to be represented in normalized IEEE format.

Figure c1. Adding a Hardware Look-Up Table to the Am29325



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The look-up table has two sections: a biased exponent look-up PROM and a fraction look-up PROM. The seed biased exponent look-up table is stored in a 512-by-8-bit PROM. This table consists of two sections – the DEC format section, which occupies addresses $000-0FF_{16}$, and the IEEE section, which occupies addresses $100-1FF_{16}$. The appropriate table will be selected automatically if address line A_8 is wired to the Am29325's IEEE/$\overline{\text{DEC}}$ pin. The equations implemented by these table sections are:

DEC table: seed biased exponent
$= 257_{10}$ – input biased exponent

IEEE table: seed biased exponent
$= 252_{10}$ – input biased exponent

Table c1 lists the contents of this PROM.

The seed fraction look-up table is stored in one or more PROMs, the number of PROMs depending on the desired accuracy of the seed value. The hardware depicted in Figure c2 uses two 4K-by-8-bit PROMs to implement a fraction look-up table whose inputs are the 12 MSBs of the input argument's fraction. These PROMs output the 16 MSBs of the seed's fraction field – the remaining 7 bits of fraction are set to 0. The equation implemented in this table is:

$$\text{seed fraction} = \frac{2}{1 + \text{input fraction}} - 1,$$

where the value of the input fraction falls in the range

$$0 \leq \text{input fraction} < 1.$$

Note that the seed fraction must also be constrained to fall in the range

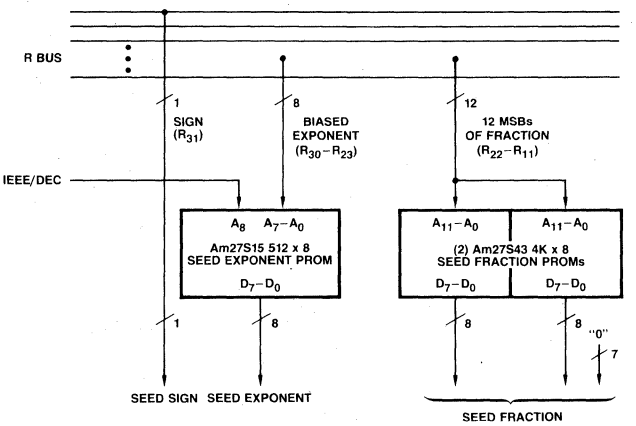
$$0 \leq \text{seed fraction} < 1.$$

Therefore, if the input fraction is 0, the corresponding seed fraction stored in the table must be $.1111...111_2$, not 1.0_2. The same seed fraction look-up table may be used for both IEEE and DEC formats. Table c2 contains a partial listing for the seed fraction look-up table shown in Figure c2.

TABLE c2. CONTENTS OF THE SEED FRACTION PROMs

Address (16)	Value of Input Fraction (10)	Value of Seed Fraction (10)	PROM Outputs (16) $R_{22}-R_{15}$	PROM Outputs (16) $R_{14}-R_7$
000	0.0	0.9999999999 (see text)	FF	FF
001	0.0002441406	0.9995118370	FF	E0
002	0.0004882812	0.9990239150	FF	C0
003	0.0007324219	0.9985362280	FF	A0
004	0.0009765625	0.9980487790	FF	80
005	0.0012207031	0.9975615710	FF	60
006	0.0014648438	0.9970745970	FF	40
007	0.0017089844	0.9965878630	FF	20
008	0.0019531250	0.9961013650	FF	00
009	0.0021972656	0.9956151030	FE	E1
00A	0.0024414063	0.9951290800	FE	C0
00B	0.0026855469	0.9946432920	FE	A1
00C	0.0029296875	0.9941577400	FE	81
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
FF6	0.9975585938	0.0012221950	00	50
FF7	0.9978027344	0.0010998410	00	48
FF8	0.9980486750	0.0009775170	00	40
FF9	0.9982910156	0.0008552230	00	38
FFA	0.9985351563	0.0007329590	00	30
FFB	0.9987792969	0.0006107240	00	28
FFC	0.9990234375	0.0004885200	00	20
FFD	0.9992675781	0.0003663450	00	18
FFE	0.9995117188	0.0002442000	00	10
FFF	0.9997558594	0.0001220850	00	08

Figure c2. The Hardware Lookup-Up Table



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With the hardware look-up table in place, the reciprocal of value B can be calculated with the following series of operations:

1.) Place B on both the R and S buses. The 2 : 1 multiplexer at the output of the hardware look-up table should select the output of the look-up table. (see Figure c3-a)

2.) Load the seed value x_0 into register R and load B into register S. Select the R TIMES S operation. (see Figure c3-b)

3.) Load product $B*x_0$ into register F. Select the 2 MINUS S operation, and select register F as the input to the ALU S port. (see Figure c3-c)

4.) Load $2-B*x_0$ into register F. Select the R TIMES S operation and select register F as the input to the ALU S port. (see Figure c3-d)

5.) Load the value x_1 $(=x_0(2-B*x_0))$ into registers R and F. Select the R TIMES S operation. (see Figure c3-e)

6.) Repeat steps 3 through 5 until the result has the accuracy desired.

Figure c3-a. Data Flow for Step 1 of the Reciprocal Procedure

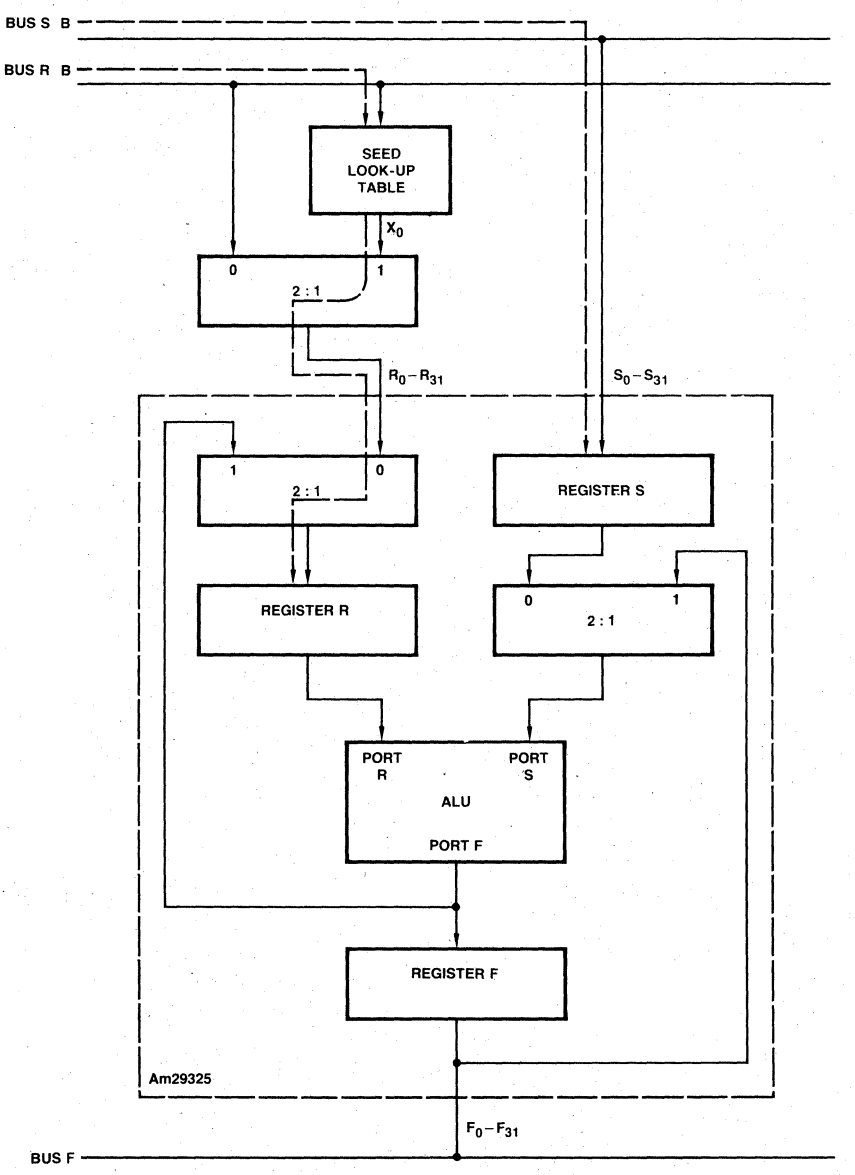

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Figure c3-b. Data Flow for Step 2 of the Reciprocal Procedure

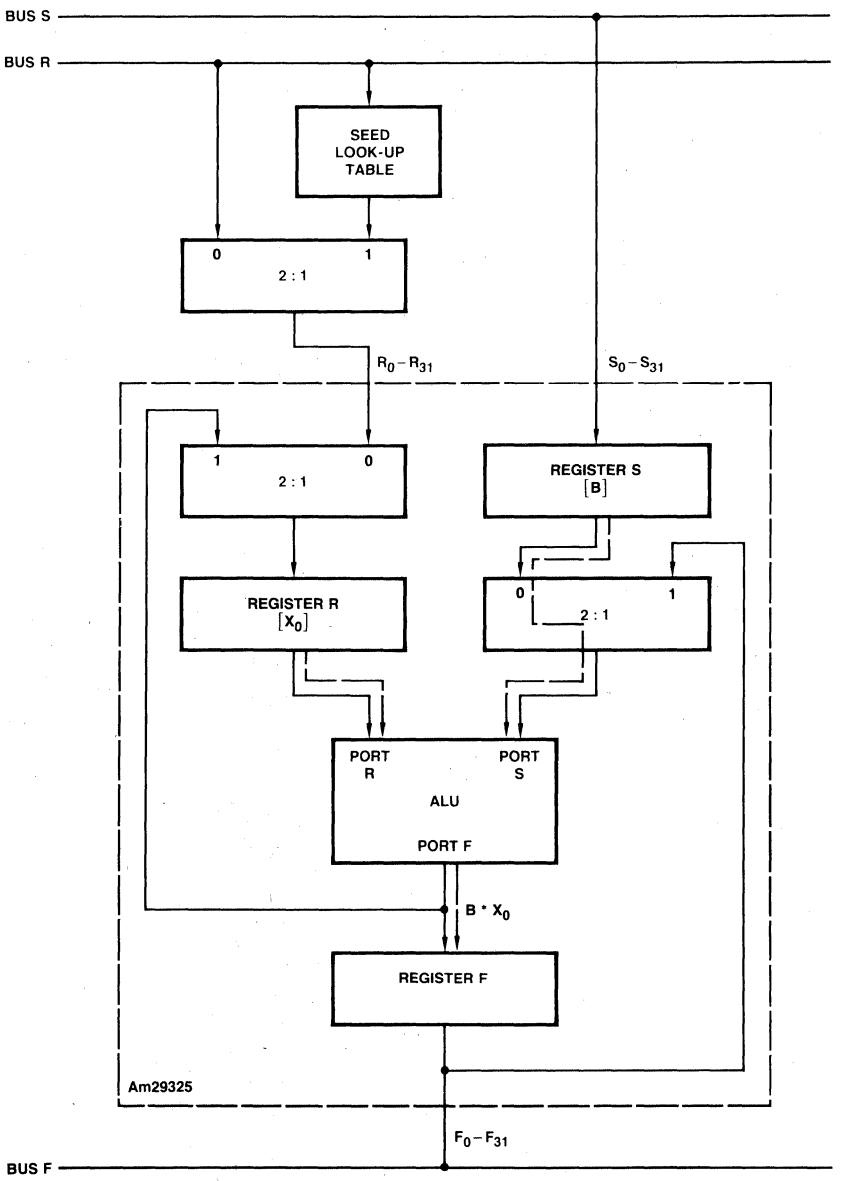

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Figure c3-c. Data Flow for Step 3 of the Reciprocal Procedure

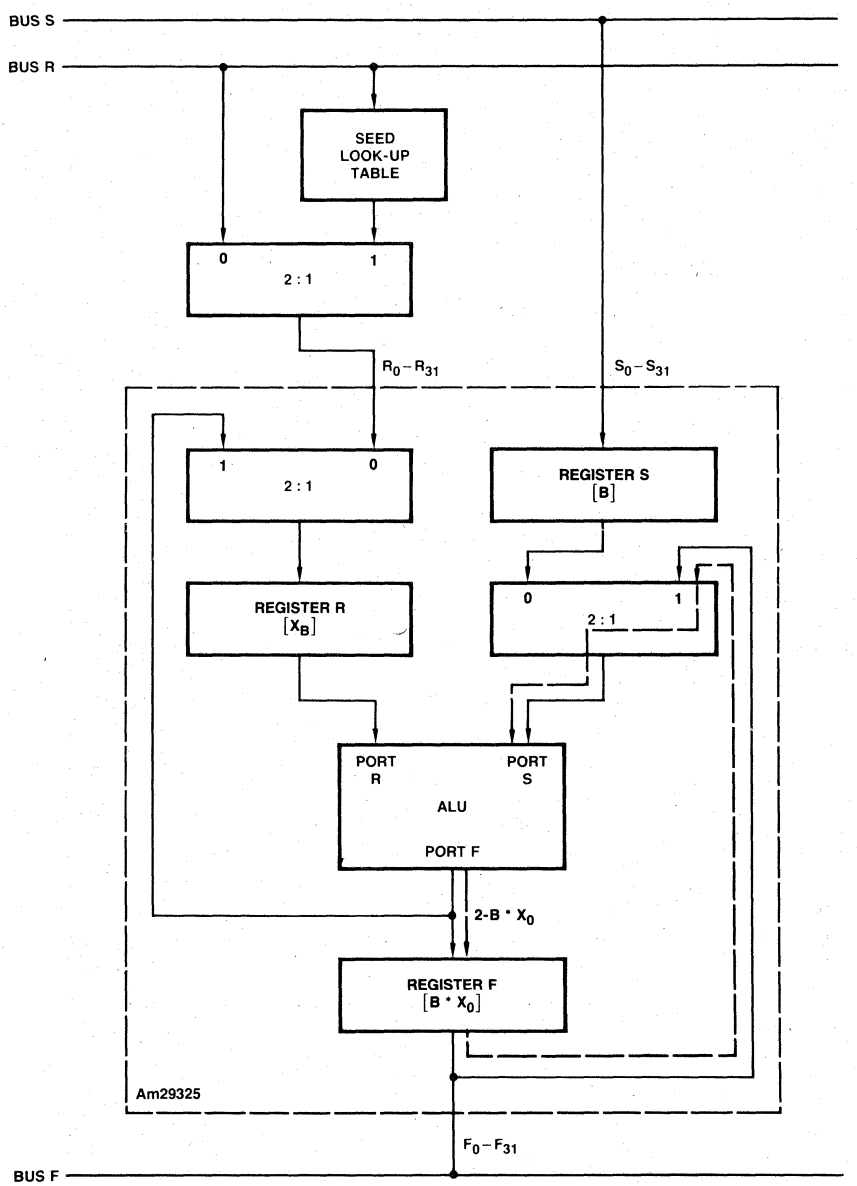

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Figure c3-d. Data Flow for Step 4 of the Reciprocal Procedure

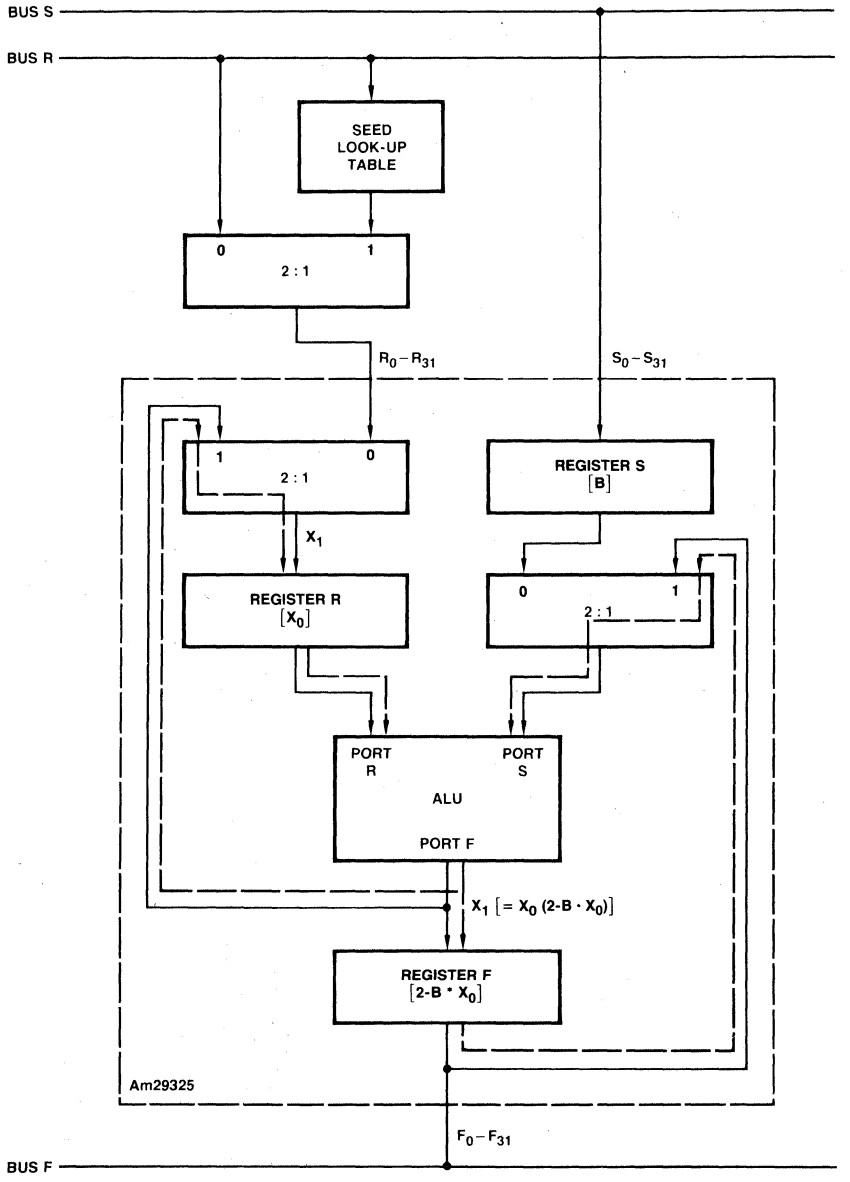

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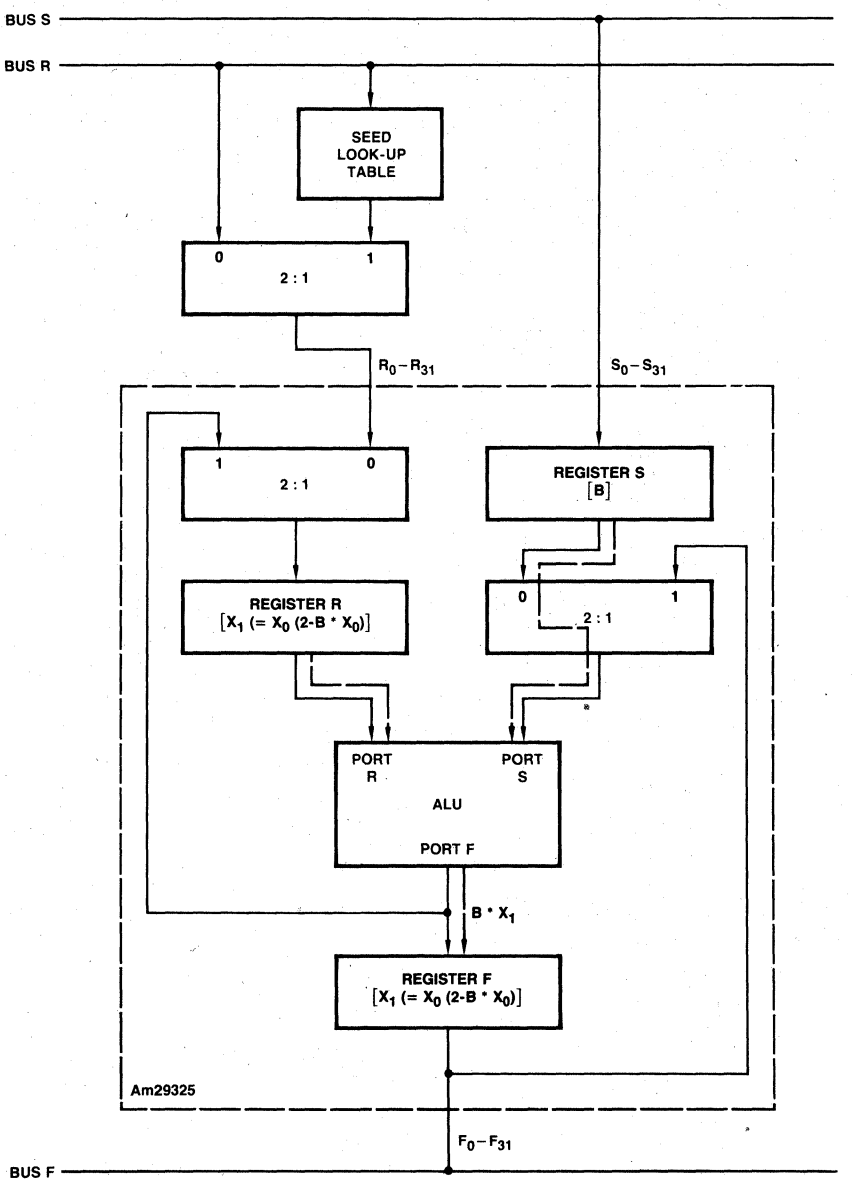
Figure c3-e. Data Flow for Step 5 of the Reciprocal Procedure



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A tabular description of the operations above is given in Table c3. The following examples, performed in IEEE format, illustrate the process.

Example 1:

Find the reciprocal of 25.3.

Solution: The IEEE floating-point representation for 25.3 is $41CA6666_{16}$. The reciprocal process is begun by feeding this value to both the seed look-up table and port S. The look-up table produces the value $.03952789_{10}$ ($3D21E800_{16}$). The reciprocal is evaluated using the procedure described above; register values for each step are given in Table c4. The expected result, to the precision of the floating-point word, is $.03952569_{10}$ ($3D21E5B1_{16}$). In this case the expected result is produced after the first iteration. All subsequent iterations produce the same result, and are therefore unnecessary.

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TABLE c3. SEQUENCE OF EVENTS FOR EVALUATING RECIPROCALS

Clock Cycle	I_0-I_2	I_3	I_4	$\overline{ENR}$	$\overline{ENS}$	$\overline{ENF}$	Register R	Register S	Register F	
1	Y	X	0	0	0	X	–	–	–	
2	R TIMES S	0	X	1	1	0	X_0	B	–	
3	2 MINUS S	1	X	1	1	0	X_0	B	$B \cdot X_0$	First iteration
4	R TIMES S	1	1	0	1	0	X_0	B	$2-B \cdot X_0$	First iteration
5	R TIMES S	0	X	1	1	0	$X_1(= X_0(2-B \cdot X_0))$	B	$X_1(= X_0(2-B \cdot X_0))$	First iteration
6	2 MINUS S	1	X	1	1	0	X_1	B	$B \cdot X_1$	Second iteration
7	R TIMES S	1	1	0	1	0	X_1	B	$2-B \cdot X_1$	Second iteration
8	R TIMES S	0	X	1	1	0	$X_2(= X_1(2-B \cdot X_1))$	B	$X_2(= X_1(2-B \cdot X_1))$	Second iteration

X = DON'T CARE

TABLE c4. INPUT BUS AND REGISTER VALUES FOR EXAMPLE 1

Clock Cycle	R Input	S Input	Register R	Register S	Register F	
1	3D21E800 (.03952789)	$41CA6666_{16}$ (25.3)	–	–	–	
2	–	–	$3D21E800_{16}$ (.03952789)	$41CA6666_{16}$ (25.3)	–	
3	–	–	$3D21E800_{16}$ (.03952789)	$41CA6666_{16}$ (25.3)	$3F8001D3_{16}$ (1.0000556)	
4	–	–	$3D21E800_{16}$ (.03952789)	$41CA6666_{16}$ (25.3)	$3F7FFC5A_{16}$ (.99984419)	
5	–	–	$3D21E5B1_{16}$ (.03952569)	$41CA6666_{16}$ (25.3)	$3D21E5B1_{16}$ (.03952569)	← Result of first iteration
6	–	–	$3D21E5B1_{16}$ (.03952569)	$41CA6666_{16}$ (25.3)	$3F7FFFFF_{16}$ (.99999994)	
7	–	–	$3D21E5B1_{16}$ (.03952569)	$41CA6666_{16}$ (25.3)	$3F800000_{16}$ (1.0)	
8	–	–	$3D21E5B1_{16}$ (.03952569)	$41CA6666_{16}$ (25.3)	$3D21E5B1_{16}$ (.03952569)	← Result of second iteration

Example 2:

Find the reciprocal of −.4725.

Solution: The IEEE floating-point representation for −.4725 is $BEF1EB85_{16}$. The reciprocal process is begun by feeding this value to both the seed look-up table and port S. The look-up table produces the value -2.11621094_{10} ($C0077000_{16}$). The reciprocal is evaluated using the procedure described above; register values for each step are given in Table c5. The expected result, to the precision of the floating-point word, is -2.116402_{10} ($C0077322_{16}$). In this case the expected result is produced after the first iteration. All subsequent iterations produce the same result, and are therefore unnecessary.

TABLE c5. INPUT BUS AND REGISTER VALUES FOR EXAMPLE 2

Clock Cycle	R Input	S Input	Register R	Register S	Register F	
1	$C0077000_{16}$ (−2.1162109)	$BEF1EB85_{16}$ (−0.4725)	–	–	–	
2	–	–	$C0077000_{16}$ (−2.1162109)	$BEF1EB85_{16}$ (−0.4725)	–	
3	–	–	$C0077000_{16}$ (−2.1162109)	$BEF1EB85_{16}$ (−0.4725)	$3F7FFA14_{16}$ (0.99990963)	
4	–	–	$C0077000_{16}$ (−2.1162109)	$BEF1EB85_{16}$ (−0.4725)	$3F8002F6_{16}$ (1.0000904)	
5	–	–	$C0077322_{16}$ (−2.116402)	$BEF1EB85_{16}$ (−0.4725)	$C0077322_{16}$ (−2.116402)	← Result of first iteration
6	–	–	$C0077322_{16}$ (−2.116402)	$BEF1EB85_{16}$ (−0.4725)	$3F800000_{16}$ (1.0)	
7	–	–	$C0077322_{16}$ (−2.116402)	$BEF1EB85_{16}$ (−0.4725)	$3F800000_{16}$ (1.0)	
8	–	–	$C0077322_{16}$ (−2.116402)	$BEF1EB85_{16}$ (−0.4725)	$C0077322_{16}$ (−2.116402)	← Result of second iteration

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APPENDIX D:

Summary of Flag Operation

Tables d1, d2, and d3 summarize flag operation for the IEEE mode, the DEC mode, and for the IEEE-TO-DEC and DEC-TO-IEEE operations.

TABLE d1. FLAG SUMMARY FOR IEEE MODE

Operation	Condition(s)	INV	OVF	UNF	INE	ZER	NAN
Any operation listed in the IEEE Invalid Operations Table		H	L	L	L	L	H
R PLUS S R MINUS S R TIMES S 2 MINUS S	Input operands are finite, $\|\text{rounded result}\| \geq 2^{128}$	L	H	L	H	L	L
R PLUS S R MINUS S R TIMES S	$0 < \|\text{rounded result}\| < 2^{-126}$	L	L	H	H	H	L
R PLUS S R MINUS S R TIMES S 2 MINUS S INT-TO-FP FP-TO-INT	Final result does not equal infinitely precise result	L	·	·	H	·	L
R PLUS S R MINUS S R TIMES S 2 MINUS S INT-TO-FP FP-TO-INT	Final result is zero	L	L	·	·	H	L
R PLUS S R MINUS S R TIMES S 2 MINUS S FP-TO-INT	Final result is a NAN	·	L	L	L	L	H

Notes: INV = Invalid operation flag
OVF = Overflow flag
UNF = Underflow flag
INE = Inexact flag
ZER = Zero flag
NAN = NAN flag
L = LOW
H = HIGH
· = State of flag depends on the input operands and the operation performed

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TABLE d2. FLAG SUMMARY FOR DEC MODE

Operation	Condition(s)	INV	OVF	UNF	INE	ZER	NAN
FP-TO-INT	Rounded result $> 2^{31}-1$ or rounded result $< -2^{31}$	H	L	L	L	L	H
FP-TO-INT	Input is a DEC reserved operand	H	L	L	L	L	H
R PLUS S R MINUS S R TIMES S 2 MINUS S	$\lvert$Rounded result$\rvert \geq 2^{127}$	L	H	L	H	L	H
R PLUS S R MINUS S R TIMES S	$0 < \lvert$rounded result$\rvert < 2^{-128}$	L	L	H	H	H	L
R PLUS S R MINUS S R TIMES S 2 MINUS S INT-TO-FP FP-TO-INT	Final result does not equal infinitely precise result	L	•	•	H	•	•
R PLUS S R MINUS S R TIMES S 2 MINUS S INT-TO-FP FP-TO-INT	Final result is zero	L	L	•	•	H	L
R PLUS S R MINUS S R TIMES S 2 MINUS S FP-TO-INT	Final result is a DEC reserved operand	•	•	L	L	L	H

Notes: INV = Invalid operation flag
OVF = Overflow flag
UNF = Underflow flag
INE = Inexact flag
ZER = Zero flag
NAN = NAN flag
L = LOW
H = HIGH
• = State of flag depends on the input operands and the operation performed

TABLE d3. FLAG SUMMARY FOR IEEE-TO-DEC AND DEC-TO-IEEE CONVERSIONS

Operation	Condition(s)	INV	OVF	UNF	INE	ZER	NAN
IEEE-TO-DEC	Input is a NAN	H	L	L	L	L	H
IEEE-TO-DEC	$\lvert$Input$\rvert \geq 2^{127}$	L	H	L	H	L	H
DEC-TO-IEEE	Input is a DEC reserved operand	H	L	L	L	L	H
DEC-TO-IEEE	$0 < \lvert$rounded result$\rvert < 2^{-126}$	L	L	H	H	H	L
DEC-TO-IEEE IEEE-TO-DEC	Final result is 0	L	L	•	•	H	L

Notes: INV = Invalid operation flag
OVF = Overflow flag
UNF = Underflow flag
INE = Inexact flag
ZER = Zero flag
NAN = NAN flag
L = LOW
H = HIGH
• = State of flag depends on the input operands and the operation performed

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias − T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs
for High State ..... −0.5V to +V_{CC} Max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage ..... +4.75 to +5.25V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage ..... +4.5 to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

3

DC CHARACTERSITICS OVER OPERATING RANGE unless otherwise specified

Parameter	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IL} or V_{IH} I_{OH} = −0.4mA		2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IL} or V_{IH} I_{OL} = 4.0mA			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = 0.4V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = 2.4V				75	μA
I_I	Input HIGH Current	V_{CC} = Max V_{IN} = 5.5V				1	mA
I_{OZH} I_{OZL}	F_0−F_{31} Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			25	μA
			V_O = .4V			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = Max V_O = 0V	F_0−F_{31} Outputs	−3		−30	mA
			Flag Outputs	−3		−30	
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max	COM'L, MIL T_A = +25°C				mA
			COM'L Only T_A = 0 to +70°C				
			COM'L Only T_A = +70°C				
			MIL Only T_A = −55 to +125°C				
			MIL Only T_A = +125°C				

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical values are for V_{CC} = +25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with $\overline{OE}$ LOW, and with all output bits (F_0−F_{31} and flag outputs) LOW.

Refer to Page 13-1 for Essential Information on Military Devices

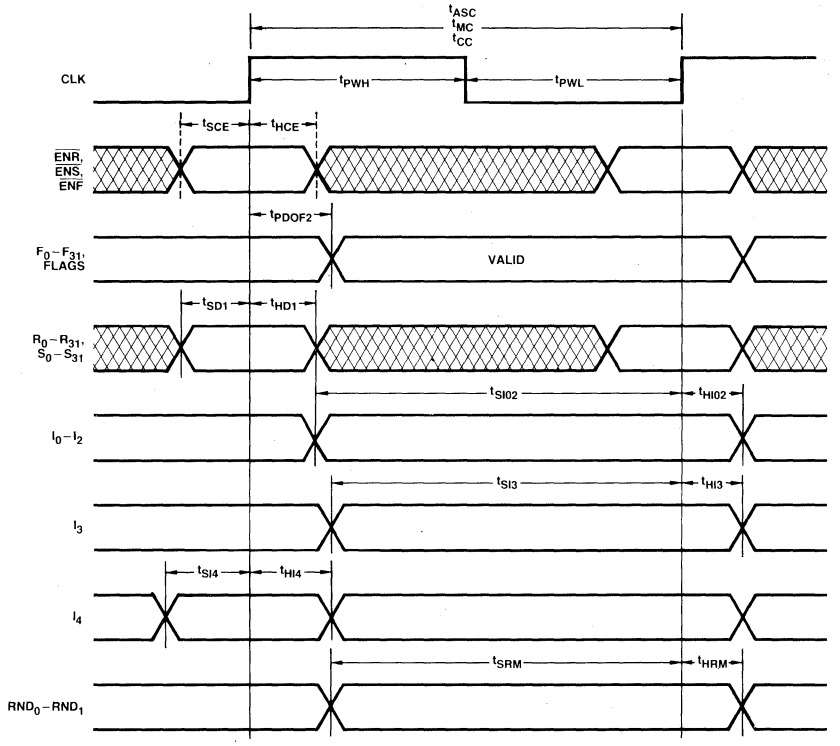
Am29325
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions	COM'L (Note 2) T_A = 25°C, V_{CC} = 5.0V Typ	COM'L (Note 2) T_A = 0 to +70°C, V_{CC} = +5V ±5% Min	COM'L (Note 2) T_A = 0 to +70°C, V_{CC} = +5V ±5% Max	MIL T_C = −55 to 125°C, V_{CC} = +5V ±10% Min	MIL T_C = −55 to 125°C, V_{CC} = +5V ±10% Max	Units
t_{ASC}	Clocked Add, Subtract Time (R PLUS S, R MINUS S, 2 MINUS S)							ns	
t_{MC}	Clocked Multiply Time (R TIMES S)							ns	
t_{CC}	Clocked Conversion Time (INT-TO-FP, FP-TO-INT, IEEE-TO-DEC, DEC-TO-IEEE)							ns	
t_{ASUC}	Unclocked Add, Subtract Time (R, S to F, Flags) for R PLUS S, R MINUS S, and 2 MINUS S Instructions							ns	
t_{MUC}	Unclocked Multiply Time (R, S to F, Flags) for R TIMES S Instruction		FT_0 = HIGH, FT_1 = HIGH					ns	
t_{CUC}	Unclocked Conversion Time (R, S to F, Flags) for INT-TO-FP, FP-TO-INT, IEEE-TO-DEC and DEC-TO-IEEE Instructions							ns	
t_{PWH}	Clock Pulse Width HIGH							ns	
t_{PWL}	Clock Pulse Width LOW							ns	
t_{PDOF1}	Clock to F_0–F_{31} and Flag Outputs		FT_0 = LOW, FT_1 = HIGH					ns	
t_{PDOF2}			FT_1 = LOW					ns	
t_{PZL}	$\overline{OE}$ Enable Time	Z to LOW						ns	
t_{PZH}		Z to HIGH						ns	
t_{PLZ}	$\overline{OE}$ Disable Time	LOW to Z						ns	
t_{PHZ}		HIGH to Z						ns	
t_{PZL16}	Clock↑ to F_0–F_{15} Enable, 16-Bit I/O Mode	Z to LOW	S16/$\overline{32}$ = HIGH, ONEBUS = LOW					ns	
t_{PZH16}		Z to HIGH						ns	
t_{PLZ16}	Clock↓ to F_0–F_{15} Disable, 16-Bit I/O Mode	LOW to Z						ns	
t_{PHZ16}		HIGH to Z						ns	
t_{PZL16}	Clock↓ to F_{16}–F_{31} Enable, 16-Bit I/O Mode	Z to LOW	S16/$\overline{32}$ = HIGH, ONEBUS = LOW					ns	
t_{PZH16}		Z to HIGH						ns	
t_{PLZ16}	Clock↑ to F_{16}–F_{31} Disable, 16-Bit I/O Mode	LOW to Z						ns	
t_{PHZ16}		HIGH to Z						ns	
t_{SCE}	Register Clock Enable Setup Time		FT_0 = LOW, FT_1 = LOW					ns	
t_{HCE}	Register Clock Enable Hold Time		FT_0 = LOW, FT_1 = LOW					ns	
t_{SD1}	R_0–R_{31}, S_0–S_{31} Setup Time (Note 1)		FT_0 = LOW					ns	
t_{HD1}	R_0–R_{31}, S_0–S_{31} Hold Time (Note 1)							ns	
t_{SD2}	R_0–R_{31}, S_0–S_{31} Setup Time (Note 1)		FT_0 = HIGH, FT_1 = LOW					ns	
t_{HD2}	R_0–R_{31}, S_0–S_{31} Hold Time (Note 1)							ns	
t_{SI02}	I_0–I_2 Instruction Select Setup Time		FT for Destination Register = LOW					ns	
t_{HI02}	I_0–I_2 Instruction Select Hold Time							ns	
t_{PDI02}	I_0–I_2 Instruction Select to F_0–F_{31}, Flags		FT_1 = HIGH					ns	
t_{SI3}	I_3 Port S Input Select Setup Time		FT_1 = LOW					ns	
t_{HI3}	I_3 Port S Input Select Hold Time							ns	
t_{SI4}	I_4 Register R Input Select Setup Time (Note 1)		FT_0 = LOW					ns	
t_{HI4}	I_4 Register R Input Select Hold Time (Note 1)							ns	
t_{SRM}	Round Mode Select Setup Time		FT for Destination Register = LOW					ns	
t_{HRM}	Round Mode Select Hold Time							ns	
t_{PRF}	Round Mode Select to F_0–F_{31}, Flags		FT_1 = HIGH					ns	

Notes: 1. See timing diagram for desired mode of operation to determine clock edge to which these setup and hold times apply.
2. At air velocity of__linear feet per minute.

Refer to Page 13-1 for Essential Information on Military Devices

CLOCKED OPERATION: FT_0 = LOW, FT_1 = LOW



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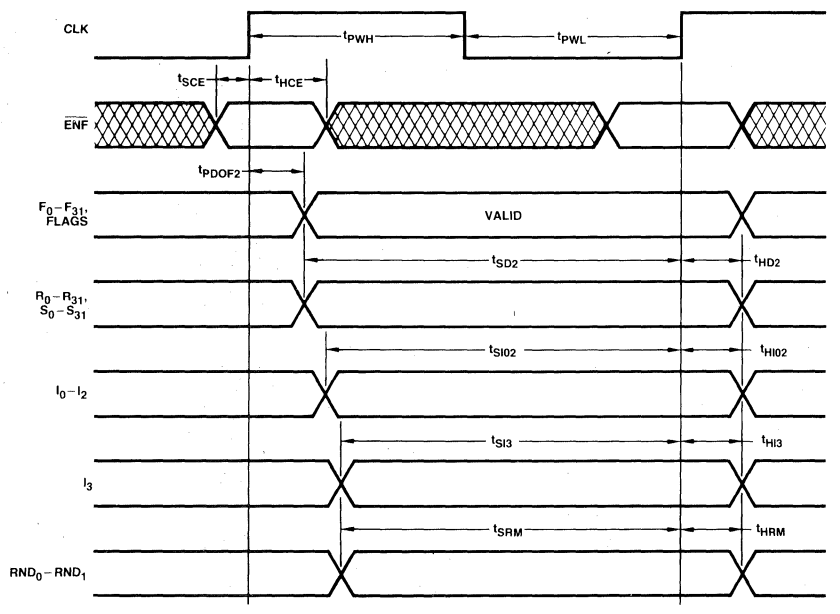
CLOCKED OPERATION: FT_0 = HIGH, FT_1 = LOW



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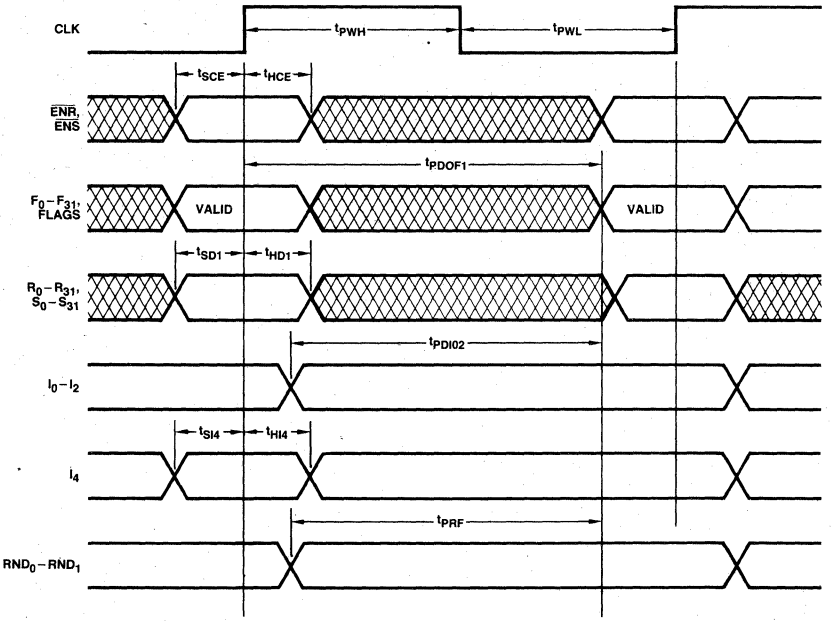
Refer to Page 13-1 for Essential Information on Military Devices

CLOCKED OPERATION: FT_0 = LOW, FT_1 = HIGH



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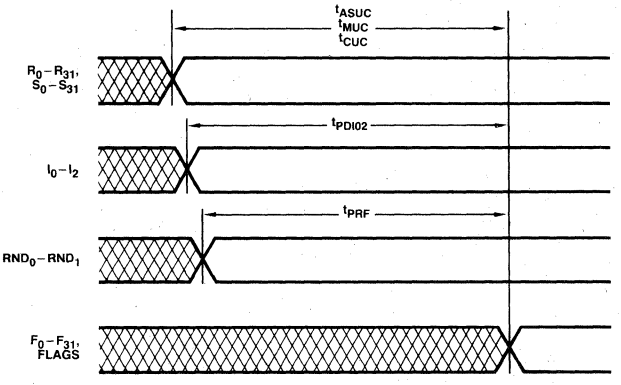
FLOW-THROUGH OPERATION (FT_0 = HIGH, FT_1 = HIGH)



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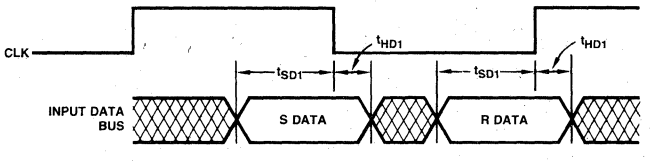
32-BIT, SINGLE-INPUT-BUS MODE



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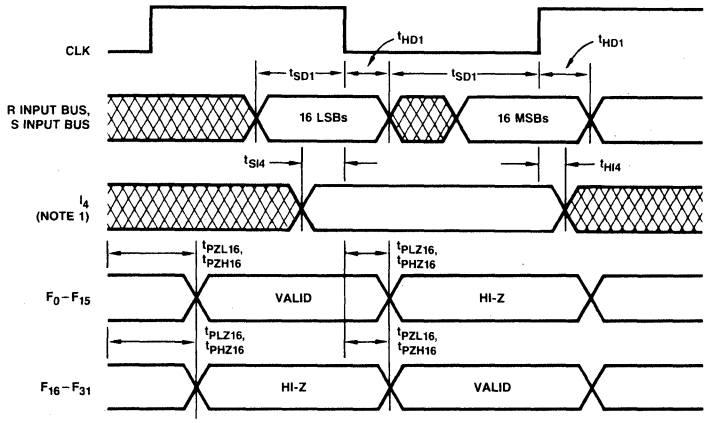
Refer to Page 13-1 for Essential Information on Military Devices

16-BIT, TWO-INPUT-BUS MODE



Note 1. I_4 has special setup and hold time requirements in this mode. All other control signals have timing requirements as shown in the diagram "Clocked operation, FT_0 = LOW, FT_1 = LOW."

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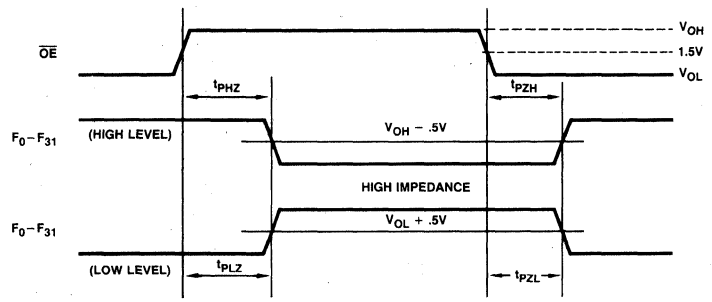
OUTPUT ENABLE/DISABLE TIMING



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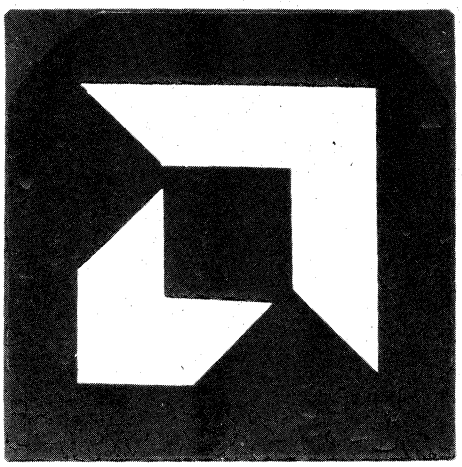
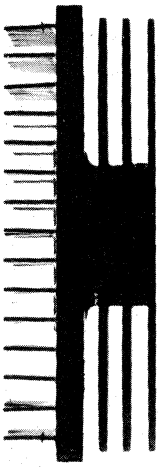
Refer to Page 13-1 for Essential Information on Military Devices

PACKAGE INFORMATION

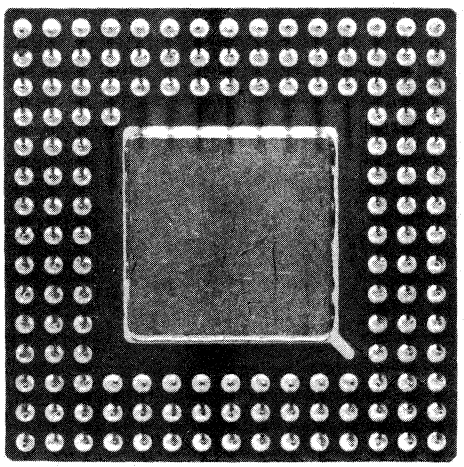
PACKAGE PHOTOGRAPHS



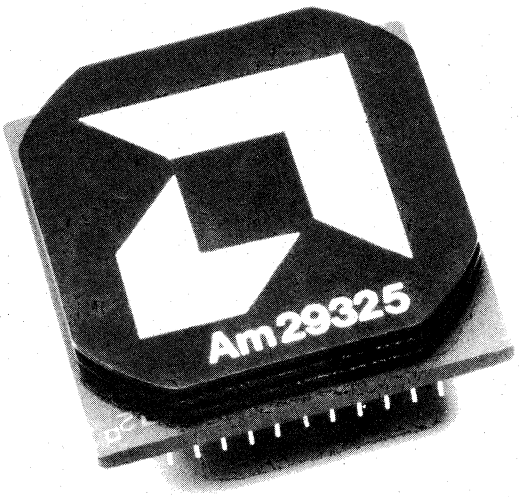
Top View



Lateral View



Bottom View



Isometric View

Refer to Page 13-1 for Essential Information on Military Devices

Am29325 PINOUT

SORTED BY PIN

Line #	Pkg Pin	Function
1	A1	Inexact
2	A2	Invalid
3	A3	F_{29}
4	A4	F_{30}
5	A5	F_{23}
6	A6	F_{26}
7	A7	F_{21}
8	A8	F_{22}
9	A9	F_{17}
10	A10	F_{18}
11	A11	F_{13}
12	A12	F_{12}
13	A13	F_{7}
14	A14	F_{8}
15	A15	F_{5}
16	B1	I_2
17	B2	NAN
18	B3	Zero
19	B4	F_{31}
20	B5	Overflow
21	B6	F_{27}
22	B7	F_{24}
23	B8	F_{19}
24	B9	F_{20}
25	B10	F_{15}
26	B11	F_{14}
27	B12	F_{9}
28	B13	F_{6}
29	B14	F_{3}
30	B15	F_{4}
31	C1	I_1
32	C2	I_0
33	C3	GND, TTL
34	C4	GND, TTL
35	C5	FL_1 Underflow
36	C6	F_{28}
37	C7	F_{25}
38	C8	V_{CC}, TTL
39	C9	V_{CC}, TTL
40	C10	F_{16}
41	C11	F_{11}
42	C12	F_{10}
43	C13	GND, TTL
44	C14	F_{2}
45	C15	F_{1}
46	D1	$\overline{ENF}$
47	D2	IEEE/$\overline{DEC}$
48	D3	$\overline{ENR}$
49	D13	GND, TTL
50	D14	GND, TTL
51	D15	GND, TTL
52	E1	I_4
53	E2	$\overline{FT_0}$
54	E3	$\overline{ENS}$
55	E13	GND, TTL
56	E14	F_{0}
57	E15	PROJ/$\overline{AFF}$
58	F1	ONEBUS
59	F2	FT_1
60	F3	S16/$\overline{32}$

SORTED BY FUNCTION

Function	Pkg Pin
$\overline{CLK}$	J1
$\overline{ENF}$	D1
$\overline{ENR}$	D3
$\overline{ENS}$	E3
F_0	E14
F_1	C15
F_2	C14
F_3	B14
F_4	B15
F_5	A15
F_6	B13
F_7	A13
F_8	A14
F_9	B12
F_{10}	C12
F_{11}	C11
F_{12}	A12
F_{13}	A11
F_{14}	B11
F_{15}	B10
F_{16}	C10
F_{17}	A9
F_{18}	A10
F_{19}	B8
F_{20}	B9
F_{21}	A7
F_{22}	A8
F_{23}	A5
F_{24}	B7
F_{25}	C7
F_{26}	A6
F_{27}	B6
F_{28}	C6
F_{29}	A3
F_{30}	A4
F_{31}	B4
FT_0	E2
FT_1	F2
GND, ECL	N3
GND, ECL	H14
GND, ECL	G13
GND, ECL	M3
GND, ECL	H13
GND, ECL	J13
GND, TTL	D15
GND, TTL	D14
GND, TTL	E13
GND, TTL	F13
GND, TTL	C4
GND, TTL	C3
GND, TTL	D13
GND, TTL	C13
I_0	C2
I_1	C1
I_2	B1
I_3	P9
I_4	E1
IEEE/$\overline{DEC}$	D2
Inexact	A1
Invalid	A2

Refer to Page 13-1 for Essential Information on Military Devices

Am29325 PINOUT (Cont)

SORTED BY PIN

Line #	Pkg Pin	Function
61	F13	GND, TTL
62	F14	S_1
63	F15	S_0
64	G1	$\overline{OE}$
65	G2	V_{CC}, ECL
66	G3	V_{CC}, ECL
67	G13	GND, ECL
68	G14	S_2
69	G15	S_3
70	H1	V_{CC}, ECL
71	H2	V_{CC}, ECL
72	H3	V_{CC}, ECL
73	H13	GND, ECL
74	H14	GND, ECL
75	H15	S_5
76	J1	CLK
77	J2	RND_0
78	J3	V_{CC}, ECL
79	J13	GND, ECL
80	J14	S_4
81	J15	S_7
82	K1	R_{31}
83	K2	RND_1
84	K3	R_{29}
85	K13	S_8
86	K14	S_9
87	K15	S_6
88	L1	R_{30}
89	L2	R_{27}
90	L3	R_{26}
91	L13	S_{13}
92	L14	S_{10}
93	L15	S_{11}
94	M1	R_{25}
95	M2	R_{28}
96	M3	GND, ECL
97	M13	S_{14}
98	M14	S_{15}
99	M15	S_{12}
100	N1	R_{24}
101	N2	R_{23}
102	N3	GND, ECL
103	N4	R_{15}
104	N5	R_{14}
105	N6	R_9
106	N7	R_8
107	N8	R_3
108	N9	R_0
109	N10	S_{28}
110	N11	S_{27}
111	N12	V_{CC}, ECL
112	N13	V_{CC}, ECL
113	N14	S_{18}
114	N15	S_{17}
115	P1	R_{21}
116	P2	R_{22}
117	P3	R_{19}
118	P4	R_{16}
119	P5	R_{11}
120	P6	R_{10}

SORTED BY FUNCTION

Function	Pkg Pin
$\overline{NAN}$	B2
$\overline{OE}$	G1
ONEBUS	F1
Overflow	B5
PROJ/$\overline{AFF}$	E15
R_0	N9
R_1	R8
R_2	R9
R_3	N8
R_4	P8
R_5	P7
R_6	R7
R_7	R6
R_8	N7
R_9	N6
R_{10}	P6
R_{11}	P5
R_{12}	R5
R_{13}	R4
R_{14}	R5
R_{15}	N4
R_{16}	P4
R_{17}	R2
R_{18}	R3
R_{19}	P3
R_{20}	R1
R_{21}	P1
R_{22}	P2
R_{23}	N2
R_{24}	N1
R_{25}	M1
R_{26}	L3
R_{27}	L2
R_{28}	M2
R_{29}	K3
R_{30}	L1
R_{31}	K1
RND_0	J2
RND_1	K2
S_0	F15
S_1	F14
S_2	G14
S_3	G15
S_4	J14
S_5	H15
S_6	K15
S_7	J15
S_8	K13
S_9	K14
S_{10}	L14
S_{11}	L15
S_{12}	M15
S_{13}	L13
S_{14}	M13
S_{15}	M14
S_{16}/$\overline{32}$	P15
S_{17}	F3
S_{18}	N15
S_{19}	N14
	R15

Refer to Page 13-1 for Essential Information on Military Devices

Am29325 PINOUT (Cont)

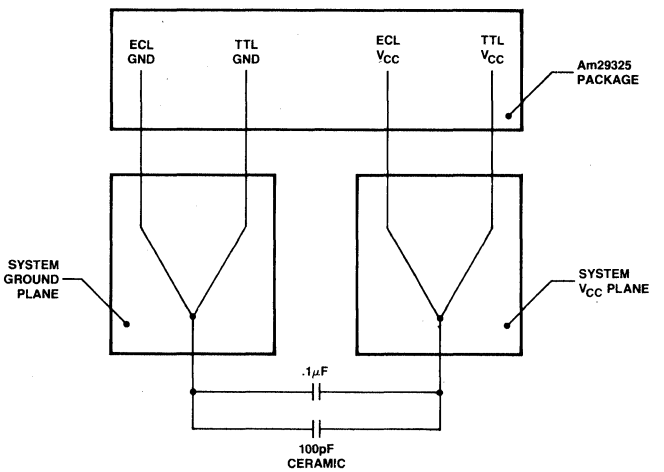
SORTED BY PIN

Line #	Pkg Pin	Function
121	P7	R_5
122	P8	R_4
123	P9	I_3
124	P10	S_{31}
125	P11	S_{26}
126	P12	S_{25}
127	P13	S_{22}
128	P14	S_{21}
129	P15	S_{16}
130	R1	R_{20}
131	R2	R_{17}
132	R3	R_{18}
133	R4	R_{13}
134	R5	R_{12}
135	R6	R_7
136	R7	R_6
137	R8	R_1
138	R9	R_2
139	R10	S_{30}
140	R11	S_{29}
141	R12	S_{24}
142	R13	S_{23}
143	R14	S_{20}
144	R15	S_{19}

SORTED BY FUNCTION

Function	Pkg Pin
S_{20}	R14
S_{21}	P14
S_{22}	P13
S_{23}	R13
S_{24}	R12
S_{25}	P12
S_{26}	P11
S_{27}	N11
S_{28}	N10
S_{29}	R11
S_{30}	R10
S_{31}	P10
Underflow	C5
V_{CC}, ECL	J3
V_{CC}, ECL	G2
V_{CC}, ECL	G3
V_{CC}, ECL	H2
V_{CC}, ECL	N13
V_{CC}, ECL	N12
V_{CC}, ECL	H3
V_{CC}, ECL	H1
V_{CC}, TTL	C8
V_{CC}, TTL	C9
Zero	B3

POWER SUPPLY WIRING CONSIDERATIONS



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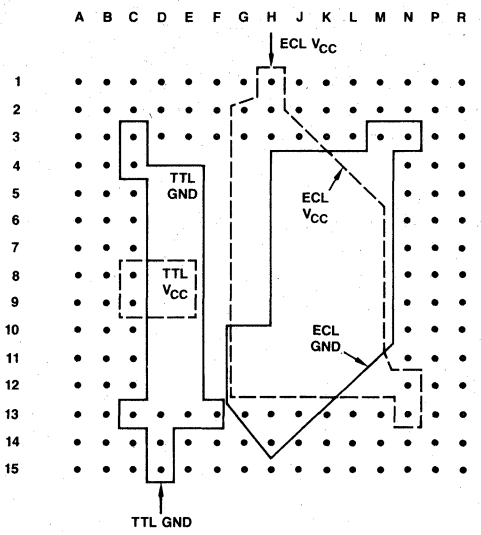
Notes: 1. All power supply pins must be connected.
2. ECL GND and TTL GND should not be connected directly into the main system ground plane. Using signal plane traces as short and wide as possible, ECL GND pins should be connected together, as should TTL GND pins, but without interconnection. These separate ground buses should be connected together and to the system ground plane at a decoupling capacitor close to the package. ECL V_{CC} and TTL V_{CC} should be treated similarly. See diagram above.

Refer to Page 13-1 for Essential Information on Military Devices

SUGGESTED PRINTED CIRCUIT BOARD LAYOUT

Bottom View



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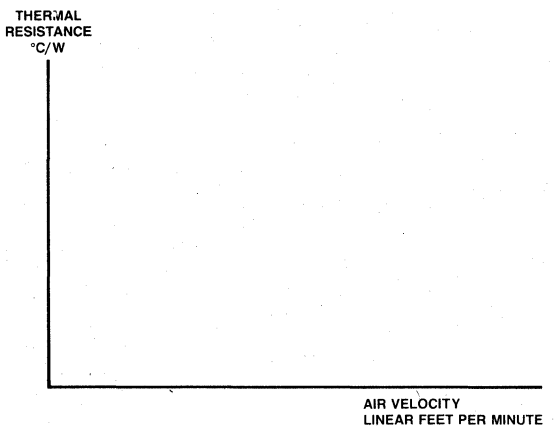
THERMAL CHARACTERISTICS



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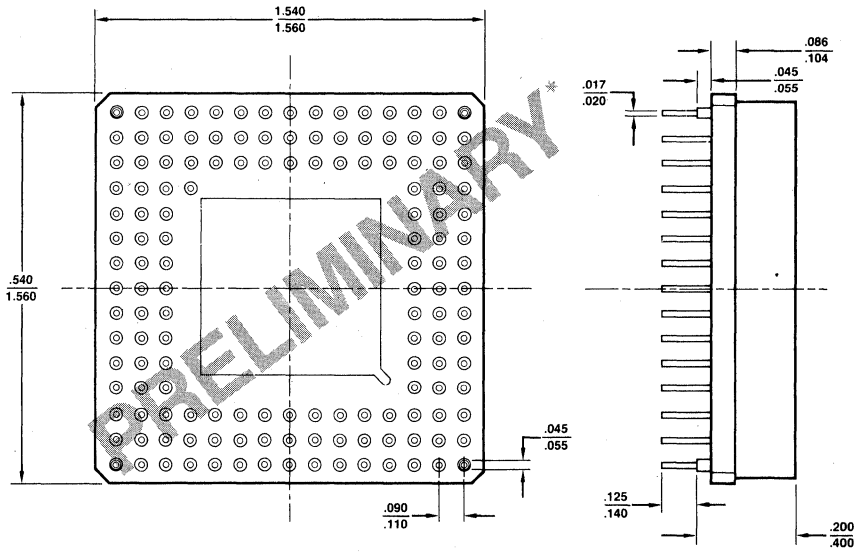
Refer to Page 13-1 for Essential Information on Military Devices

PHYSICAL DIMENSIONS



*Subject to change.

The International Standard of Quality guarantees the AQL on all electrical parameters, AC and DC, over the entire operating range.

Refer to Page 13-1 for Essential Information on Military Devices

Am29331

16-Bit Microprogram Sequencer

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **16-Bits Address Up to 64K Words**
  Like the other members of the Am29300 family, the Am29331 supports 80–90ns microcycle for the 32-bit high-performance system.
- **Real Time Interrupt Support**
  Micro-TRAP and interrupts are handled transparently at any microinstruction boundary.
- **Built-In Conditional Test Logic**
  Generates inequality evaluation branch conditions from four ALU status bits, eight external test inputs and a polarity control input.
- **Break-Point Logic**
  Built-in address comparator allows break-points in the microcode for debugging and statistics collection.
- **Master/Slave Error Checking**
  Two sequencers can operate in parallel as a master and a slave. The slave generates a fault flag for unequal results.
- **33-Level Stack**
  Provides support for interrupts, loops and subroutine nesting. It can be accessed through the D-bus to support diagnostics.

GENERAL DESCRIPTION

The Am29331 is a 16-bit wide high-speed single chip sequencer designed to control the execution sequence of microinstructions stored in the microprogram memory. The instruction set is designed to resemble high level language constructs, thereby bringing high level language programming to the micro level.

The Am29331 is interruptible at any microinstruction boundary to support real time interrupts. Interrupts are handled transparently to the microprogrammer as an unexpected procedure call. Traps are also handled transparently at any microinstruction boundary. This feature allows re-execution of the prior microinstruction. Two separate buses are provided to bring a branch address directly into the chip from two sources to avoid slow turn-on and turn-off times for different sources connected to the data input bus. Four sets of multiway inputs are also provided to avoid slow turn-on and turn-off times for different branch address sources. This feature allows implementation of table look-up or use of external conditions as part of a branch address. The thirty-three-deep stack provides the ability to support interrupts, loops and subroutine nesting. The stack can be read through the D-bus to support diagnostics or to implement multitasking at the micro-architecture level. The master/slave mode provides a complete function check for the device.

The Am29331 is designed with the IMOX™ process which allows internal ECL circuits with TTL compatible I/O. It is housed in a 120 pin-grid-array package.

RELATED PRODUCTS

Part No.	Description
Am29323	32 x 32 Parallel Multiplier
Am29325	32-Bit Floating Point Processor
Am29332	32-Bit ALU
Am29334	64 x 18 Four-Port, Dual-Access Register File

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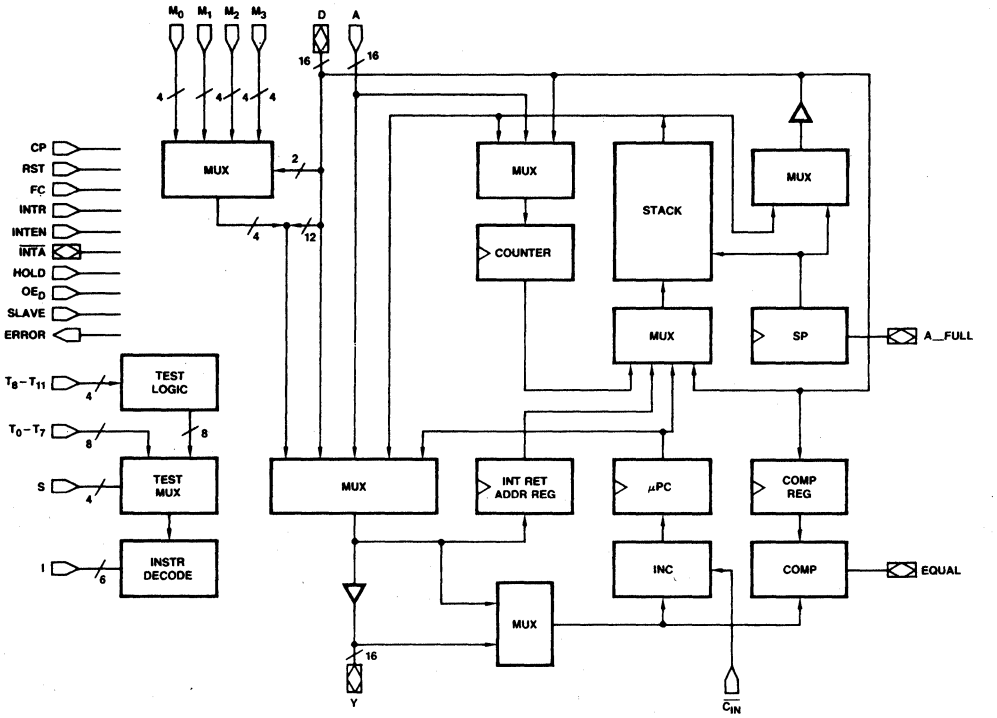
BLOCK DIAGRAM

Am29331



BD003000

Am29332

32-Bit Arithmetic Logic Unit

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Single Chip, 32-Bit ALU**
  Supports 80–90ns microcycle for the 32-bit data path. It is a combinatorial ALU with equal cycle time for all instructions
- **Flow Through Architecture**
  A combinatorial ALU with two input data ports and one output data port allows implementation of parallel or pipelined architectures
- **64-Bit In, 32-Bit Out Funnel Shifter**
  This unique functional block allows n-bit shift-up, shift-down, 32-bit barrel shift or 32-bit field extract
- **Supports All Data Types**
  It supports one-, two-, three- and four-byte data for all operations and variable-length fields for logical operations
- **Multiply and Divide Support**
  Built-in hardware to support two-bit at a time modified Booth's algorithm and one-bit at a time division algorithm
- **Extensive Error Checking**
  Parity check and generate provides data transmission check. Master/slave mode provides complete functional checking

GENERAL DESCRIPTION

The Am29332 is a 32-bit wide non-cascadable ALU with integration of functions that normally don't cascade such as barrel shifters, priority encoders and mask generators. Two input data ports and one output data port provide flow through architecture and allow the designer to implement his/her architecture with any degree of pipelining and no built-in penalties for branching. Also, the simplicity of a three-bus ALU allows easy implementation of parallel or reconfigurable architectures. The register file is off-chip to allow unlimited expansion and regular addressability.

The Am29332 supports one-, two-, three- and four-byte data for arithmetic and logic operations. It also supports multiprecision arithmetic and shift operations. For logical operations, it can support variable-length fields up to 32 bits. When fewer than four bytes are selected, unselected bits are passed to the destination without modification. The device also supports two-bit at a time modified Booth's algorithm for high-speed multiplication and one-bit at a time division. Both signed and unsigned integers for all byte aligned data types mentioned above are supported.

The Am29332 is designed to support 80–90 ns microcycle time. The device is packaged in a 168 pin-grid-array package.

RELATED PRODUCTS

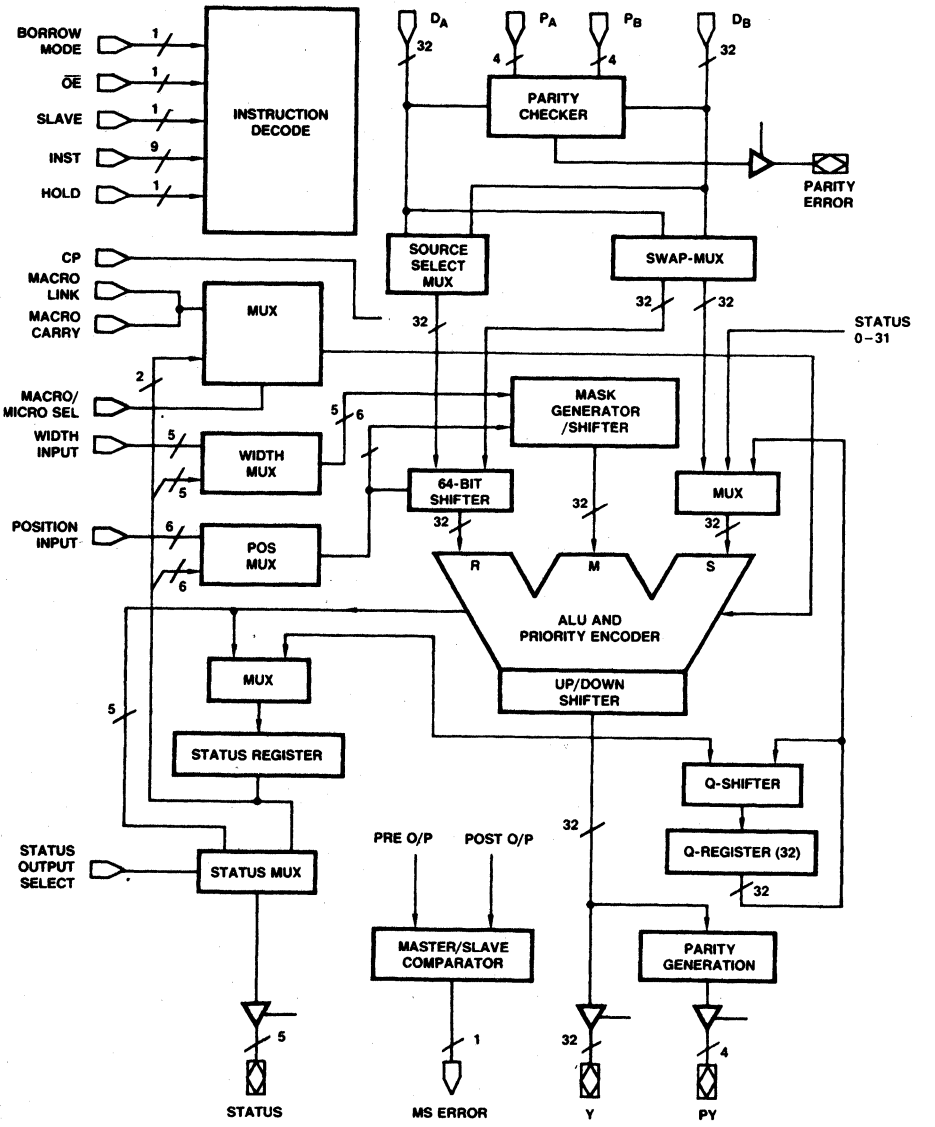
Part No.	Description
Am29323	32 x 32 Parallel Multiplier
Am29325	32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29334	64 x 18 Four-Port, Dual-Access Register File

05730A

Refer to Page 13-1 for Essential Information on Military Devices

BLOCK DIAGRAM

Am29332



BD003010

Am29334

Four-Port, Dual-Access Register File

ADVANCED INFORMATION

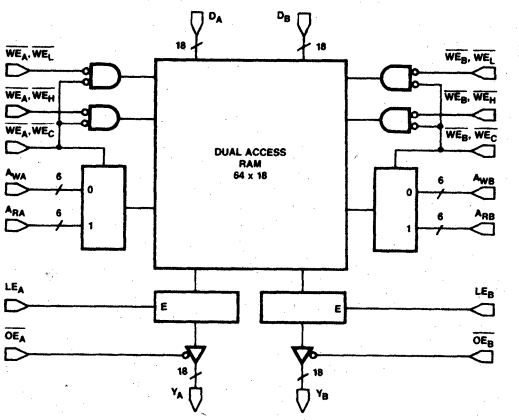
DISTINCTIVE CHARACTERISTICS

- **Fast**
  With an access time of 20ns, the Am29334 supports 80–90ns microcycle when used with the Am29300 family for 32-bit systems.
- **64 x 18 Bits Wide Register File**
  The Am29334 is a high-performance, high-speed, dual-access RAM with two READ ports and two WRITE ports.
- **Cascadable**
  The Am29334 is cascadable to support either wider word width, deeper register files, or both.
- **Simplified Timing Control**
  Control for write enable timing and for on-chip read/write multiplexer are derived from a single-phase clock input.
- **Byte Parity Storage**
  Width of 18 bits facilitates byte parity storage for each port and provides consistency with the Am29332 32-bit ALU.
- **Byte Write Capability**
  Byte-write enable pins allow byte or full word writes.

GENERAL DESCRIPTION

The Am29334 is a 64-word deep and 18-bit wide dual-access register file designed to support other members of the Am29300 family by providing high-speed storage. It has two write and two read ports for data and four 6-bit address ports. Two address ports are associated with each pair of read and write data ports; one to read data and the other to write. The device is capable of performing two reads and two writes in one cycle. The 18-bit wide register file allows storage of byte parity to support parity check and generate in the Am29332 32-bit ALU. Independent control for each read and write data port allows the Am29334 to be used as a high-speed shared memory or as a mailbox for a multiprocessor system. The device is designed to support an access time of 20ns. It is housed in a 120 pin-grid-array package.

BLOCK DIAGRAM



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RELATED PRODUCTS

Part No.	Description	Part No.	Description
Am29323	32 x 32 Parallel Multiplier	Am29331	16-Bit Microprogram Sequencer
Am29325	32-Bit Floating Point Processor	Am29332	32-Bit ALU

05731A

Refer to Page 13-1 for Essential Information on Military Devices

Am29360

32-Bit Error Detection and Correction Unit

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Boosts memory reliability
  - Corrects all single bit errors
  - Detects all double and some triple bit errors
  - Reliability of dynamic RAM memory system is increased
- Very high speed
  - Perfect for microprocessor, minicomputer and mainframe systems
- All necessary features are built-in to the Am29360 including memory testing, Reconfiguration, Diagnostics, and Data In/Out, Data Bits Out and Check Bits Out latches
- Handles data word widths from 8- to 32-bits
  - Byte writes on all word widths from 8- to 32-bits
- Diagnostics built-in
  - The processor may exercise the memory or Am29360 under software control to check for proper operations
- Built-in Memory Timing Controller (MTC)
  - Supports byte writes
  - Delay line controlled timings
  - Arbitrates between refresh and memory request
  - Refresh internal timer for generating refresh requests independent of processor

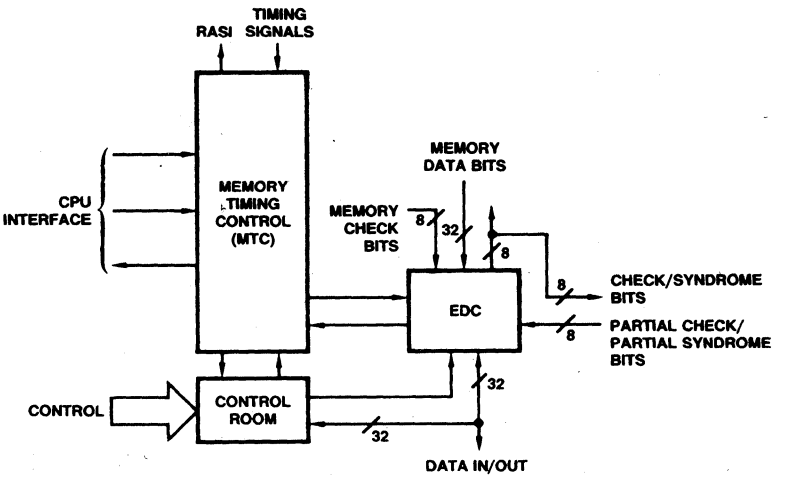
GENERAL DESCRIPTION

The Am29360 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 32-bit data field according to a modified hamming code, and to correct a data word when check bits are supplied. Operating on data read from memory, the Am29360 will correct any single-bit error and will detect all double and some triple bit errors. For 32-bit words, 7 check bits are used. In all configurations, the device makes the error syndrome bits available on output signals S/C_0-S/C_7 for data logging.

The Am29360 also features diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

The built-in MTC (Memory Timing Controller) generates all timing signals for the on-board error detection and correction function. The Am29360 also has a general purpose CPU interface and a Power-up sequence which includes eight RAS-only Wake-Up cycles, a two part Test (Read/Write, Increment) and memory Initialize.

BLOCK DIAGRAM



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Am29368

1M-Bit Dynamic Memory Controller (DMC)

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

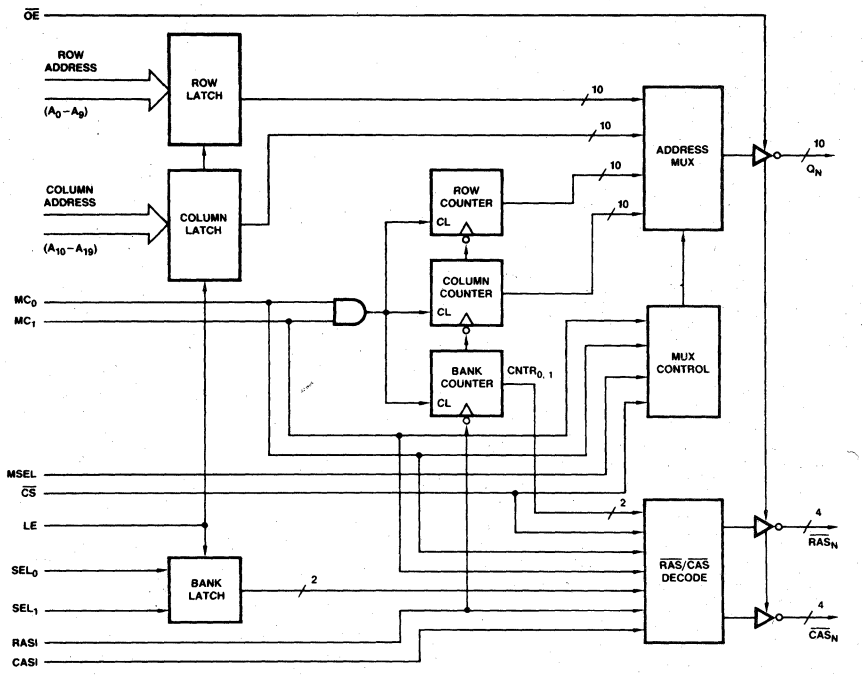
- Provides control for 16K, 64K, 256K, and 1M-bit dynamic RAMs
- Outputs directly drive up to 88 DRAMs, with a guaranteed worst-case undershoot
- Highest-order two address bits select one of four banks of RAMs
- Separate output enable for multi-channel access to memory
- Supports scrubbing operations and nibble-mode access
- IMOX™ processing

GENERAL DESCRIPTION

The Am29368 Dynamic Memory Controller (DMC) is intended to be used with today's high-performance memory systems. The DMC will act as the address controller between any processor and dynamic memory array, using its two 10-bit address latches to hold the Row and Column addresses for any DRAM up to 1M-bit. These latches, and the two Row/Column refresh address counters, feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch for the two high-order address bits is provided to select one each of the four $\overline{RAS}_N$ and $\overline{CAS}_N$ outputs.

The Am29368 has two basic modes of operation, read/write and refresh. In refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the Row Counter is used, generating up to 1024 addresses to refresh a 1024-cycle-refresh 1M-bit DRAM. When memory scrubbing is being performed, both the Row and Column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}_N$ outputs will be active while only one $\overline{CAS}_N$ is active at a time. The Am29368 is available in a 52-pin dual in-line package.

BLOCK DIAGRAM



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Am2960-2970
Dynamic Memory Support Index

Am2960-70 Memory Support Family System Overview

INTRODUCTION

Memory system designs are increasingly shaped by three requirements:

1. Higher system performance
2. More memory capacity in less space
3. Increased reliability

The Am2960-70 Memory Support Family is a family of LSI building blocks which excels in satisfying these three requirements and provides a complete systems solution for designs using 64K or 256K DRAMs. The family members include:

Am2960 Error Detection and Correction Unit
Am2961/62 EDC Bus Buffers
Am2964B Dynamic Memory Controller (64K DRAM Version)
Am2965/66 Dynamic RAM Drivers
Am2968 Dynamic Memory Controller (256K DRAM Version)
Am2969 Timing Controller
Am2970 Timing Controller
Am8163/67 System and Timing Controller for MOS MPUs

These are general purpose products. They will support any supplier's DRAMs and will work with any processor type: 8086, 80186, 80286, 68000, Z8000, and Am2900 processors. They may also be used to support word widths of any size from 8 bits to 64 bits.

Figure 1 shows the system interconnection for a typical memory system for 256K DRAMs, and Figure 2 shows the system interconnection for a typical memory system using 64K DRAMs. In both cases, the memory support subsystem interfaces to the System Data Bus, Address Bus, and control signals. Also, in both cases all, or almost all, of the memory support functions are handled by AMD LSI devices. This simplifies the design of the memory system and, more importantly, allows the board space available for DRAMs to be maximized because the LSI solution for control and error correction is very compact.

ERROR DETECTION AND CORRECTION

It is important that memory systems function reliably. The number of bytes of storage is increasing rapidly in memory systems at the same time that the density of the MOS DRAMs is growing. With 64K and 256K DRAMs, alpha particle sensitivity is much greater than that of smaller DRAMs because of the reduced size of the memory cells and the smaller stored charge of the cell. A Technical Report follows the Am2960 data sheet in this section and is entitled "Am2960 Boosts Memory Reliability." This technical report gives some statistics on soft error rates for DRAMs. It also demonstrates the dramatic increase in memory reliability gained from the use of Hamming Code Error Detection and Correction schemes, such as those used by the Am2960 EDC (Error Detection and Correction) unit.

Data interface between the dynamic memories, the Am2960 EDC chip, and the system data bus is accomplished by means of the Am2961/62 bus buffers. Figure 3 depicts the architecture of these devices along with a simplified block diagram of the Am2960. The Am2961 is inverting between the system data bus and the EDC bus while the Am2962 is noninverting. As shown in Figure 3, the Am2961 and Am2962 contain two internal latches, a multiplexer, and a RAM driver output buffer.

These devices feature 4-bit-wide data paths to and from the RAM, the EDC, and the system data bus. The bus-input (BI) latch is used predominantly in byte WRITE operations, so that an incoming byte from the system data bus can be stored while the memory is being read, and any necessary correction made in the bytes not being changed. The bus-output (BO) latch is used predominantly for storing the output data if the processor is in the single-step mode. In the single-step mode it is necessary to hold the output data on the system data bus, but the memory must be released for refresh.

The Am2960 Error Detection and Correction Unit contains all the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code and to correct the data word when check bits are supplied. Operating on the data read from memory, the Am2960 will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for data logging.

The Am2960 also features two diagnostic modes in which diagnostic data can be forced into portions of the device to simplify device testing and to execute system diagnostic functions.

The 16-bit Diagnostic Latch is loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. It contains check bit information in one byte and control information in the other, and is used for driving the device when in the Internal Control mode, or for supplying check bits when in one of the Diagnostic modes.

The control logic determines the specific operating mode. Normally the control logic is driven by external control inputs; however, in the Internal Control mode, the control signals are instead read from the Diagnostic Latch.

The Am2960 is a very fast EDC device, but even faster versions will soon be available. A speed selected version, the Am2960-1, is described in the Am2960 data sheet, and an IMOX™ version, the Am2960A, will be available by late 1984. All speed-improved versions have identical functions and are electrically plug-compatible with the current Am2960.

MEMORY SYSTEM CONTROL AND TIMING

Two Dynamic Memory Controllers are available for generating address, $\overline{RAS}$, and $\overline{CAS}$ signals for memory banks. The Am2964B is designed to work with 64K DRAMs of which each device can handle up to four banks for a total control

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capacity of 256K words. The new Am2968 is designed to work with 256K DRAMs and can also handle up to four banks for a total control capacity of 1 Megaword (the words can be as many bits wide as desired). Also, the Am2968 does not require external driver chips as does the Am2964B – the Am2968 has the memory drivers, with all of the undershoot control and speed features of the Am2965/66, built right into its address, $\overline{RAS}$, and $\overline{CAS}$ outputs.

For generating the timing and control signals required by the Am2964B/68 and the Am2960/61/62, there are several different devices available, optimized for different system requirements. For MOS Microprocessor systems, use the Am8163 or Am8167.

Figure 1. New Generation Am2900 High Performance Memory Subsystem Using 256K or 64K DRAMs

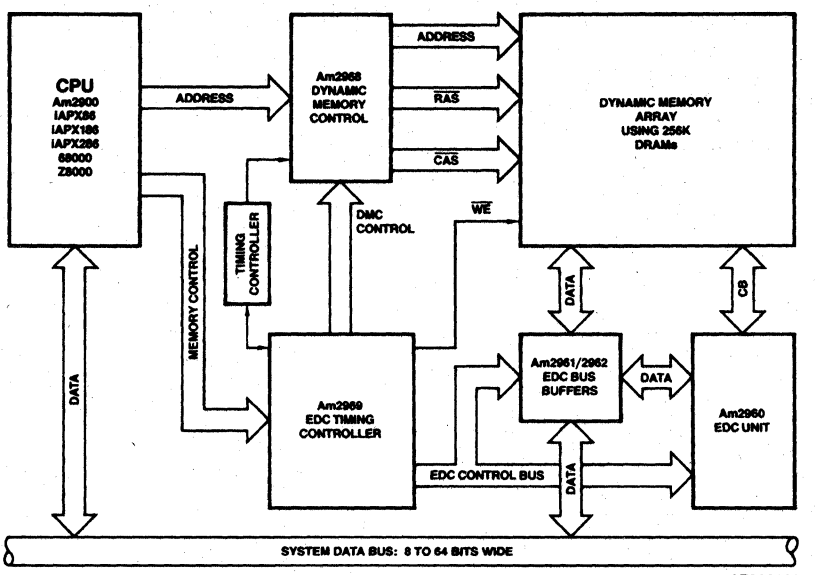

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Figure 2. Am2900 High Performance Memory Subsystem Using 64K DRAMs

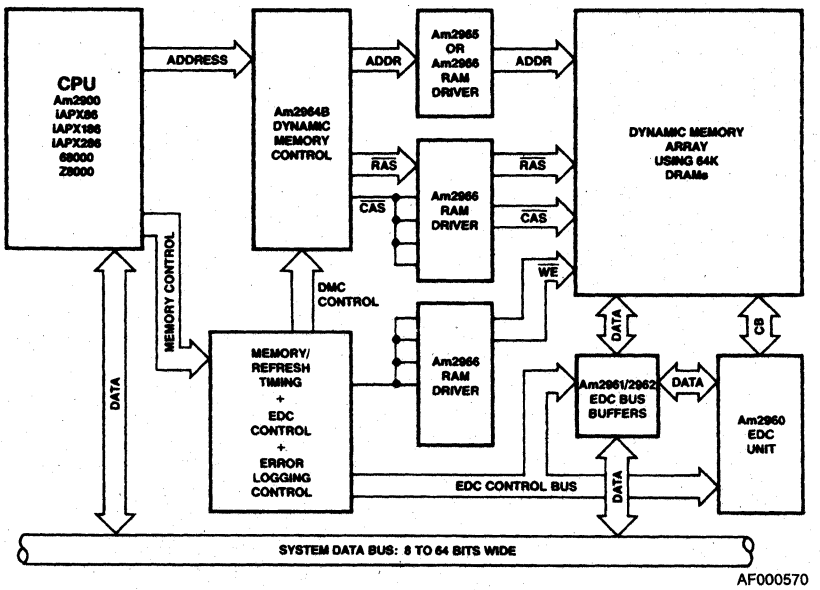

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Figure 3. EDC Data Path

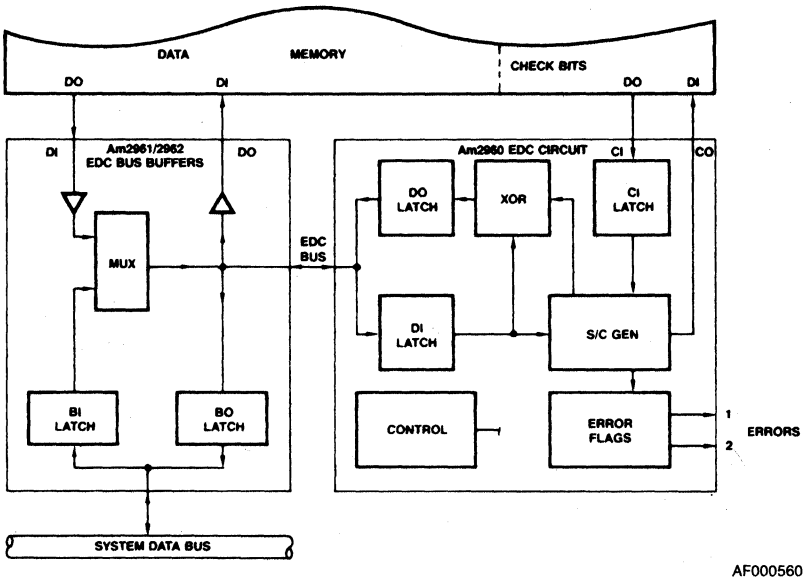

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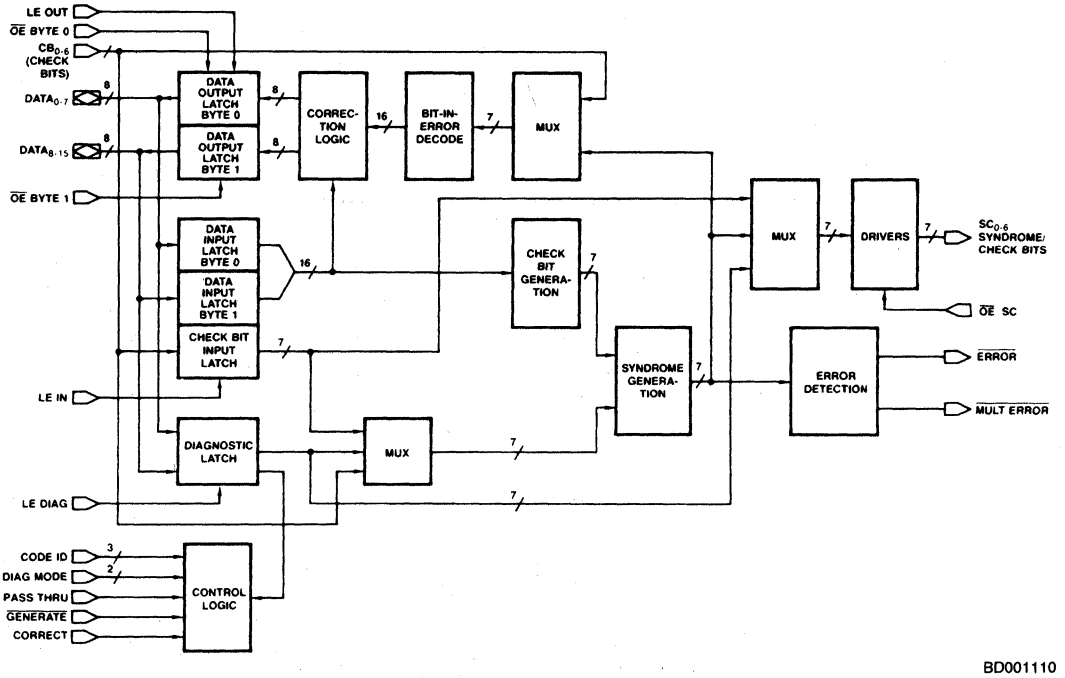
Figure 4. Am2960 Block Diagram



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Both of these devices will interface easily to iAPX86/186, Z8000, or 68000 microprocessors. The Am8163 and Am8167 provide the control signals and timing signals for the memory controllers, the EDC, and the data bus buffers – in addition, the Am8163/67 decode the memory system control signals directly from the MOS Microprocessor, requiring in most cases only a few gates and at most a single PAL™ for interfacing. In this section are detailed block diagrams of systems showing how to interface the Am2960-70 Family devices to the most popular MOS microprocessors.

For high-performance Am2900-based processors or other high-speed processor designs, use the Am2969 or Am2970 to generate timing and control signals.

Following is a description of the function of the Am2964B/65/66 for Dynamic Memory Control for 64K DRAMs. The Am2968 incorporates these features and more into a single IC for use with 256K DRAMs.

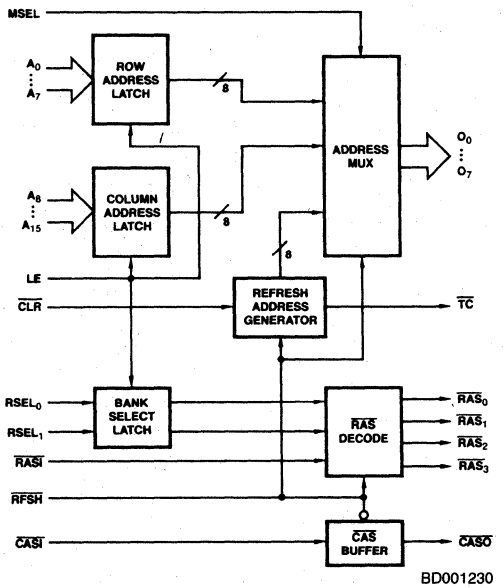
The Am2964B Dynamic Memory Controller is used to provide all address handling, as well as $\overline{RAS}$ and $\overline{CAS}$ decoding and control. A block diagram of the Am2964B Dynamic Memory Controller is shown in Figure 5. The device contains 18 input latches for capturing an 18-bit address for memory control; the two highest order addresses are decoded in the Am2964B to select one of four banks of RAM by selecting one of the four $\overline{RAS}$ outputs.

The Am2964B is designed to operate with either 16K Dynamic RAMs or 64K Dynamic RAMs. Thus, the designer either uses 14 of the multiplexer address inputs and 7 of the address outputs or all 16 of the multiplexer address inputs and all 8 of the address outputs as needed by the memory. In the case of 16K Dynamic RAMs, 7 address inputs are provided to the RAM during the $\overline{RAS}$ LOW signal, and then the 8-bit multiplexer is switched so that 7 upper address bits are provided to the RAM for the $\overline{CAS}$ LOW part of the cycle. The Am2964B Dynamic Memory Controller contains an 8-bit refresh counter that is used to supply the refresh address to the dynamic memory during the refresh cycle. This counter can be used in either the 128 or 256 line refresh mode. A $\overline{CAS}$ buffer is included in the dynamic memory controller so that the $\overline{CAS}$ output can be inhibited during refresh.

Normal operation of the Dynamic Memory Controller is to provide the address, close the input address latches and kick off a normal memory cycle. This is accomplished by bringing the $\overline{RASI}$ input LOW, which will cause one of the $\overline{RAS}$ outputs to go LOW. After the required $\overline{RAS}$ hold time, the MSEL input will be used to switch the multiplexer to the other address latch. Then the $\overline{CASI}$ input will be driven LOW, causing the $\overline{CASO}$ output to go LOW and execute the $\overline{CAS}$ part of the memory cycle. The refresh cycle is executed by driving the $\overline{RFSH}$ input LOW, which causes the multiplexer to connect the refresh counter to its address outputs. Then the $\overline{RASI}$ input is driven LOW, which causes all four $\overline{RAS}$ outputs to go LOW. This will simultaneously refresh all four banks of dynamic RAMs controlled by the Am2964B Dynamic Memory Controller. When either the $\overline{RFSH}$ or $\overline{RASI}$ input is brought HIGH, the refresh counter is advanced so it will be ready for the next refresh cycle.

As can be seen in Figure 1, Dynamic RAM Drivers can be used in large memory systems to buffer the Address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE\ ENABLE}$ signals to the RAMs. The Am2965 and Am2966 are pin-compatible devices with the Am74S240 and Am74S244. These RAM drivers are specifically designed for driving dynamic RAMs and feature high capacitance drive, guaranteed maximum undershoot of less than –0.5 volts, and high V_{OH} of greater than V_{CC} = 1.15 volts. The Am2965 is inverting and the Am2966 is noninverting. The devices feature symmetrical rise and fall times and have guaranteed minimum and maximum t_{PD} specifications for both 50pF and 500pF loads.

Figure 5. Am2964B Dynamic Memory Controller



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Am2960/Am2960A

16-Bit Error Detection and Correction Unit

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

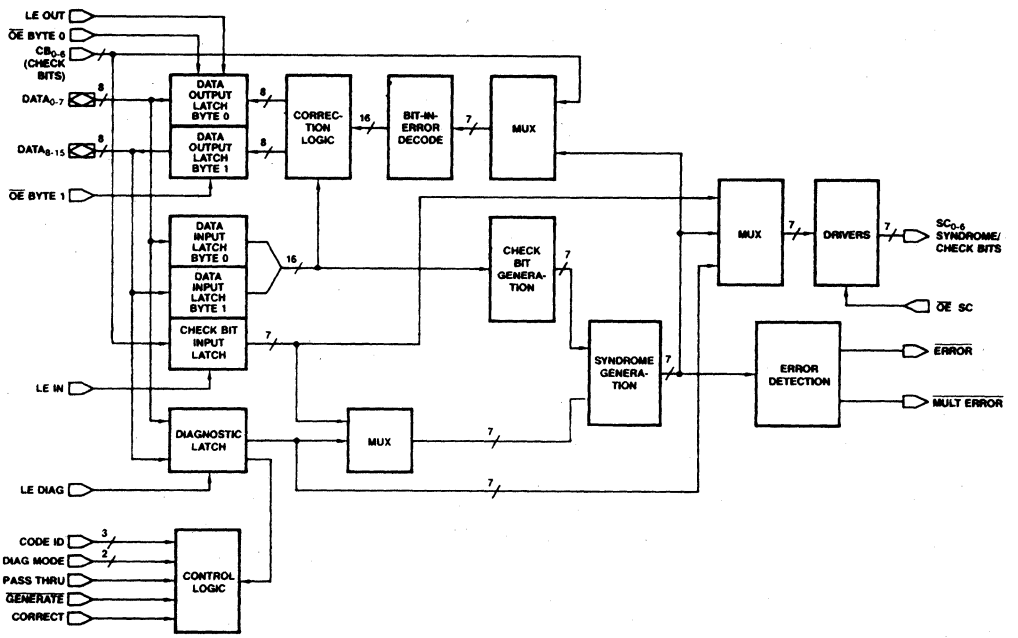
- **Boosts Memory Reliability**
  Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.
- **Very High Speed**
  Perfect for MOS microprocessor, minicomputer, and main-frame systems.
  - Data in to error detect: 32ns worst case.
  - Data in to corrected data out: 65ns worst case. High performance systems can use the Am2960 EDC in check-only mode to avoid memory system slowdown.
- **Handles Data Words From 8 Bits to 64 Bits**
  The Am2960 EDC cascades: 1 EDC for 8 bits or 16 bits, 2 for 32 bits, 4 for 64 bits.
- **Easy Byte Operations**
  Separate byte enables on the data out latch simplify the steps and cut the time required for byte writes.
- **Diagnostics Built-In**
  The processor may completely exercise the EDC under software control to check for proper operation of the EDC.

GENERAL DESCRIPTION

The Am2960 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am2960 will correct any single-bit error and will detect all double and some triple-bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Am2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

BLOCK DIAGRAM



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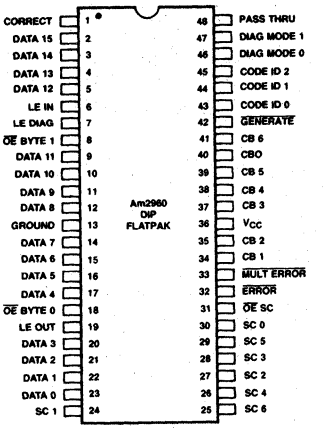
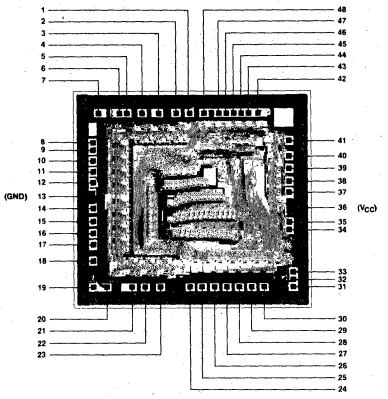
CONNECTION DIAGRAM
Top View



CD001420

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.200″ x 0.183″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2960 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 48-pin CERDIP (D-48-2)
  - X – Dice
- Am2960 — Device type
  - Cascadable 16-Bit Error Detection and Correction Unit

Valid Combinations	
Am2960 Am2960A	DC, DCB, DM, DMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

03565C

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$DATA_{0-15}$	I/O	16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
	CB_{0-6}	I	Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.
6	LE IN	I	Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
42	$\overline{\text{GENER-ATE}}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate Mode. When HIGH, the EDC is in the Detect Mode or Correct Mode. In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.
	SC_{0-6}	O	Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.
31	$\overline{\text{OE}}$ SC	I	Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
32	$\overline{\text{ERROR}}$	O	Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)
33	$\overline{\text{MULT}}$ $\overline{\text{ERROR}}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)
1	CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
19	LE OUT	I	Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.
8, 18	$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1	I	Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch, and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.
48	PASS THRU	I	Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
47, 48	DIAG $MODE_{0-1}$	I	Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.
43, 44, 45	CODE ID_{0-2}	I	Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.
7	LE DIAG	I	Latch Enable – Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 16-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode, the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

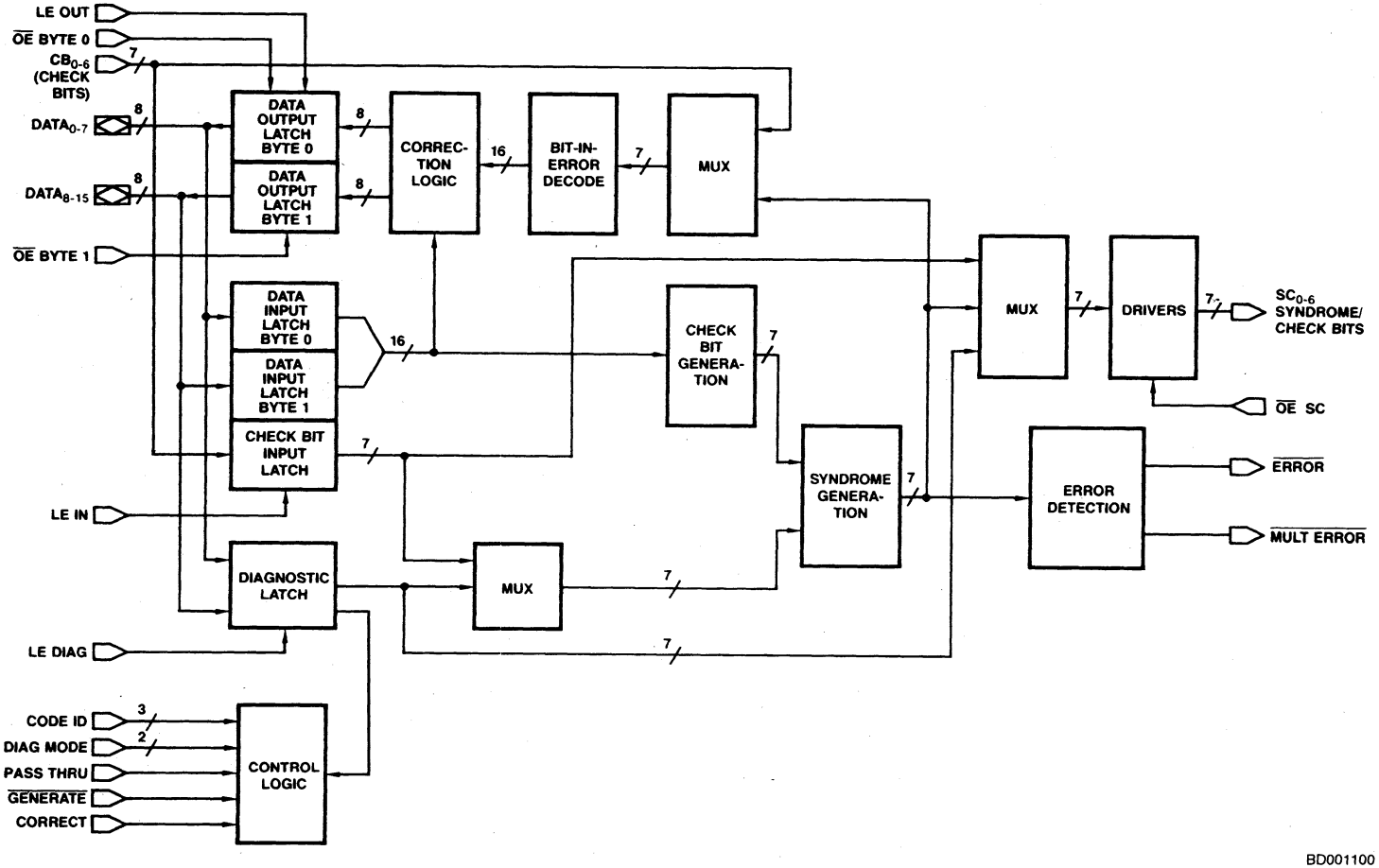
Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

BLOCK DIAGRAM



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DETAILED DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am2960 may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In fact the EDC can be configured to work on data words from 8 to 64 bits. In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID_{0-2}, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 – 16 data bits – 6 check bits – 22 bits in total.
- 32/39 code – 32 data bits – 7 check bits – 39 bits in total.
- 64/72 code – 64 data bits – 8 check bits – 72 bits in total.

CODE ID input 001 (ID_2, ID_1, ID_0) is a special code used to operate the device in Internal Control Mode (described later in this section).

Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table III indicates the operating modes selected by various combinations of the control line inputs.

Diagnostics

Table II shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization, and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits, and 8 syndrome bits in the 64-bit configuration.

Initialize Mode

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the Initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDC may be placed in initialize mode and its' outputs written in to all memory locations by the processor.

TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE II. DIAGNOSTIC MODE CONTROL.

DIAG $MODE_1$	DIAG $MODE_0$	Diagnostic Mode Selected
0	0	Non-diagnostic mode. The EDC functions normally in all modes.
0	1	Diagnostic Generate. The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	Diagnostic Detect/Correct. In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	Initialize. The outputs of the Data Input Latch are forced to zeroes (and latched upon removal of the Initialize Mode) and the check bits generated correspond to the all-zero data.

HAMMING CODE SELECTION

The Am2960 EDC uses a modified Hamming Code that allows 1. the EDC to be cascaded, 2. all double errors to be detected, 3. the gross error conditions of all 0s or 1s to be detected.

The error correction code can be selected independent of the processor with the exception of diagnostics software.

Diagnostic software run by a processor to check out the EDC system must know specifically which code is being used. This is only a problem when the EDC replaces an existing MSI implementation on an existing computer. In this case, the computer's software must first determine which of two codes (the old one used by the MSI implementation or the new one used by the EDC) is used by the computer's memory system.

This is easily determined by writing a test data word into memory and then examining whether the generated check bits are typical of the old or the new code. From then on the software runs only the diagnostic appropriate for the code used on that particular computer's memory system.

TABLE III. Am2960 OPERATING MODES

Operating Mode	Diagnostic Mode**		$\overline{\text{GENERATE}}$	
	DM_1	DM_0	0	1
Normal	0	0	Generate	Correct*
Diagnostic Generate	0	1	Diagnostic Generate	Correct*
Diagnostic Correct	1	0	Generate	Diagnostic Correct*
Initialize	1	1	Initialize	Initialize
Pass Thru	When PASS THRU is asserted, the Operating Mode is defaulted to the Pass Thru Mode.			

*Correct if the CORRECT Input is HIGH, Detect if the CORRECT Input is LOW.
**In Code $ID_{2\text{-}0}001(ID_2, ID_1, ID_0)$ DM_1 and DM_0 are taken from the Diagnostic Latch.

16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 5.)

The 16-bit configuration is shown in Figure 6.

Generate Mode

In this mode, check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0\text{-}5}$ (SC_6 is a logical one, or high).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

Figure 1 shows the data flow in the Generate Mode.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs $SC_{0\text{-}5}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001, this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected, the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. (See Figure 2.) If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit, there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are placed on outputs $SC_{0\text{-}5}$. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch

(see Table III for details). Figures 3 and 4 illustrate the flow of data during the two diagnostic modes.

Internal Control Mode

This mode is selected by CODE ID_{0-2} input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

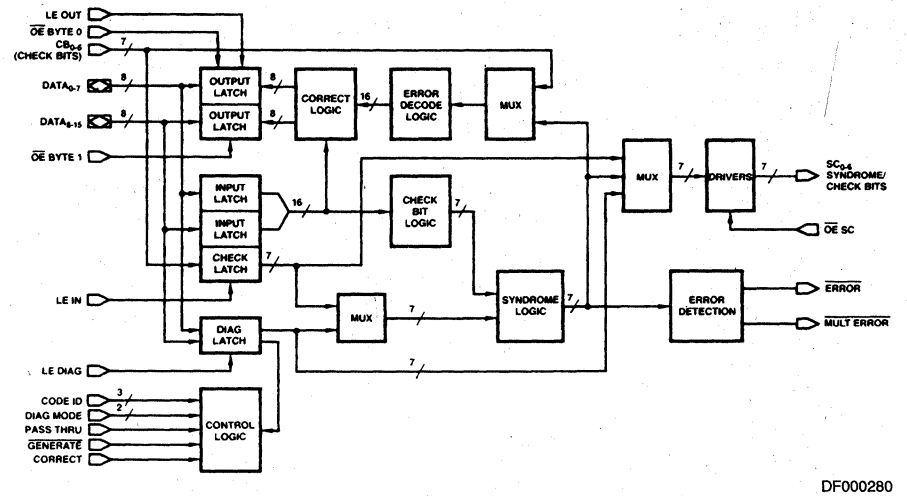


Figure 1. Check Bit Generation

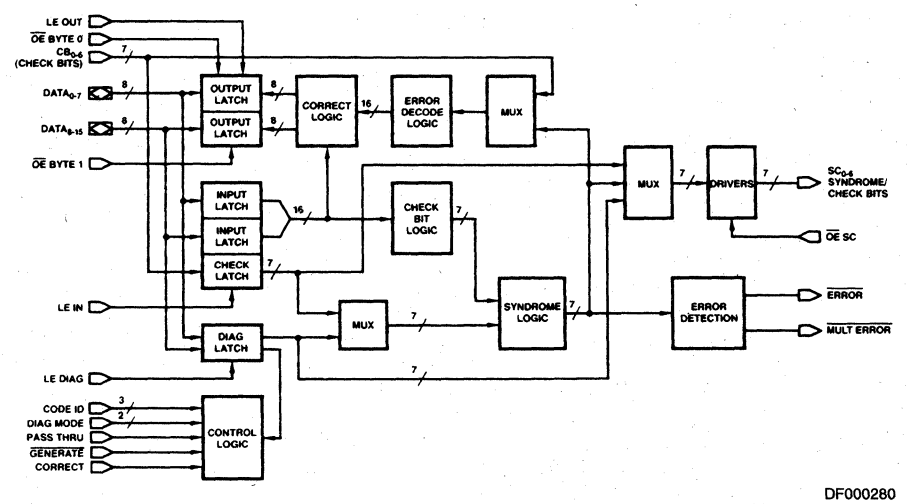


Figure 2. Error Detection and Correction

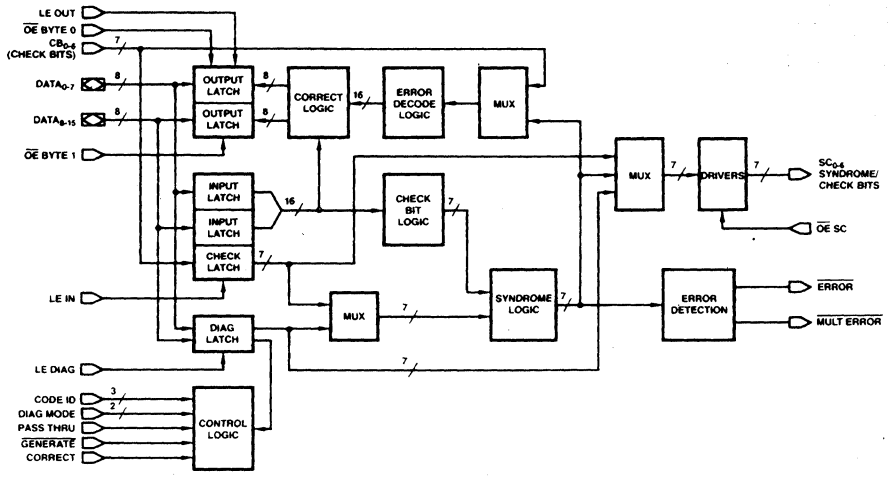


Figure 3. Diagnostic Check Bit Generation

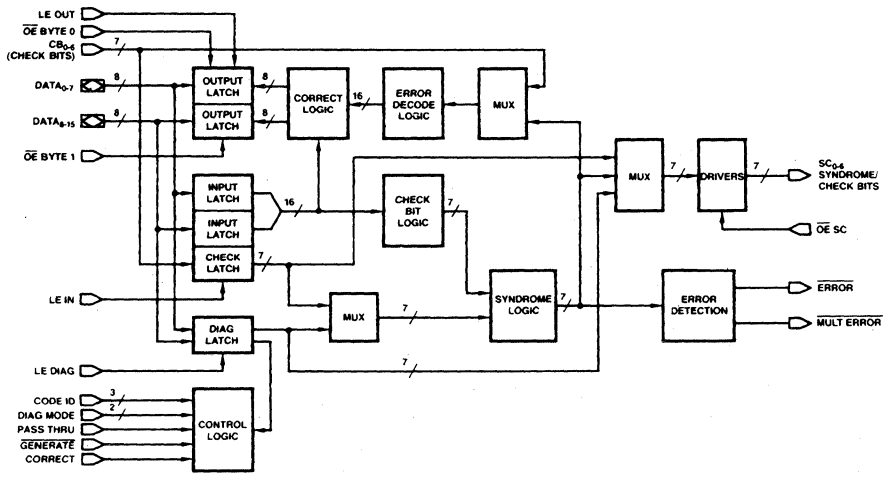
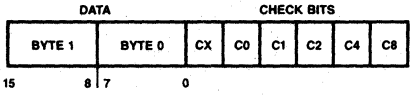


Figure 4. Diagnostic Detect and Correct



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Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

Figure 5. 16-Bit Data Format

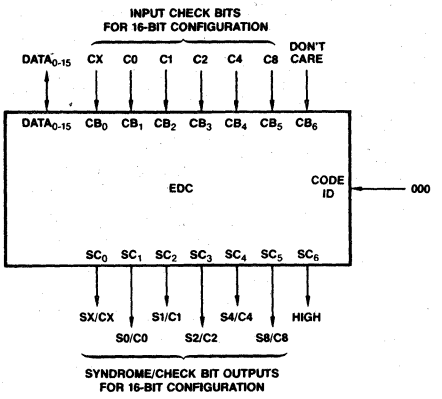

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Figure 6. 16-Bit Configuration

SYNDROME DECODE TO BIT-IN-ERROR 8-BIT MODE

Syndrome Bits S0	S1	S4	S2	0 0	1 0	0 1	1 1
0	0			*	C4	C2	5
0	1			C1	3	TM	7
1	0			C0	2	1	6
1	1			TM	4	0	TM

* – no errors detected
TM – two or more errors

TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE V.
SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits SX S0 S1	S8	0	1	0	1	0	1	0	1
	S4	0	0	1	1	0	0	1	1
	S2	0	0	0	0	1	1	1	1
0 0 0		*	C8	C4	T	C2	T	T	M
0 0 1		C1	T	T	15	T	13	7	T
0 1 0		C0	T	T	M	T	12	6	T
0 1 1		T	10	4	T	0	T	T	M
1 0 0		CX	T	T	14	T	11	5	T
1 0 1		T	9	3	T	M	T	T	M
1 1 0		T	8	2	T	1	T	T	M
1 1 1		M	T	T	M	T	M	M	T

* – no errors detected
Number – location of the single bit-in-error
T – two errors detected
M – three or more errors detected

TABLE VI.
DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE 1D 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

32-BIT DATA WORD CONFIGURATION

The 32-bit format consists of 32 data bits and 7 check bits and is referred to as 32/39 code (see Figure 7).

The 32-bit configuration is shown in Figure 8.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 – the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3—the external DATA lines for bits 16 to 31 are connected to inputs $DATA_0$ through $DATA_{15}$ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs and are selected by the MUX as inputs to the bit-in-error decoder (see block diagram). This requires external buffering and output enabling of the check bit lines, as shown. The $\overline{OE}$ SC signal can be used to control enabling of check bit inputs – when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are those of the Slice 2/3. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode, check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0\text{-}6}$ of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table X. Check bits are generated as either an XOR or XNOR of 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode, the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors, and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW. Both error indicators are HIGH if there are no errors. The valid

$\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ signals are those of Slice 2/3 – those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs $SC_{0\text{-}6}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table VII gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011, this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected, the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit, there is no automatic correction; if desired, this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs $SC_{0\text{-}6}$. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs $CB_{0\text{-}6}$. The device connections for this are shown in Figure 8. When in Correct Mode, the SC outputs must be enabled so that they are available for reading in through the CB inputs.

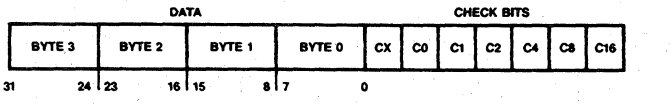
Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output latch, and the contents of the Check Bit Input Latch are placed on outputs $SC_{0\text{-}6}$ of Slice 2/3. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

TABLE VII.
SYNDROME DECODE TO BIT-IN-ERROR

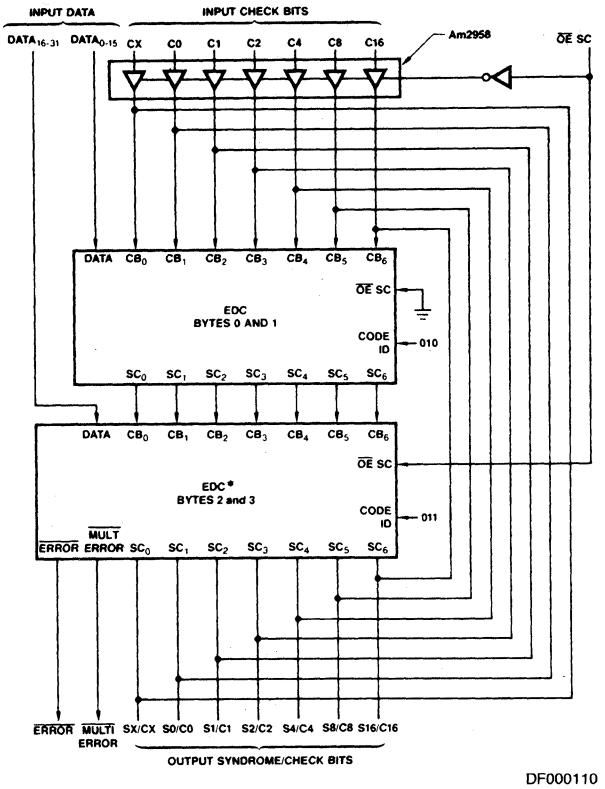
Syndrome Bits SX	S0	S1	S2	S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* – no errors detected
Number – number of the single bit-in-error
T – two errors detected
M – three or more errors detected



DF000460

Figure 7. 32-Bit Data Format



DF000110

*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice.

Figure 8. 32-Bit Configuration

TABLE VIII.
KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Component Delay from Am2960 AC Specifications, Table C
From	To	
DATA	Check Bits Out	(Data to SC) + (CB to SC, CODE ID 011)
DATA In	Corrected DATA Out	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

TABLE IX.
DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE X.
32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

64-BIT DATA WORD CONFIGURATION

The 64-bit format consists of 64 data bits, 8 check bits and is referred to as 64/72 code (see Figure 9.).

The configuration to process 64-bit format is shown in Figure 6. In this configuration, a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction, the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in the connection diagram of Figure 10. The $\overline{OE}$ SC signal can control the check bit enabling; when syndrome bit outputs are enabled, the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

The error detection signals for the 64-bit configuration differ from the 16- and 32-bit configurations. The $\overline{ERROR}$ signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected. The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected; it is LOW otherwise. All of the $\overline{MULT\ ERROR}$ outputs of the four devices are valid. $\overline{MULT\ ERROR}$ is LOW for all three ERROR cases and some DOUBLE ERROR combinations. (See TOME definition in Functional Equations section.) It is HIGH if either zero or one errors are detected.

This is a different meaning for $\overline{MULT\ ERROR}$ than in other configurations.

Generate Mode

In this mode, check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 10.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table XII. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode, the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If exactly two errors are detected, $\overline{DOUBLE\ ERROR}$ goes HIGH. If three or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW – the $\overline{MULT\ ERROR}$ output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits (see Figure 10). The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table XIII gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S1/S2/S4/S8/S16/S32 were 00100101, this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected, the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit, there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs, where they are selected as inputs to the bit-in-error decoder by the multiplexer (see Block Diagram). The device connections for this are shown in Figure 10. When in Correct Mode, the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of Check Bit Input Latch are passed through the external XOR network and appear inverted at the XOR gate outputs labeled CX to C32 (see Figure 10).

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table XIV shows the loading definitions for the DATA lines.

Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table II for details.

Internal Control Mode

This mode is selected by CODE $ID_{0\text{-}2}$, input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE $ID_{0\text{-}2}$, DIAG $MODE_{0\text{-}1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines. Table XIV gives format for loading the Diagnostic Latch.

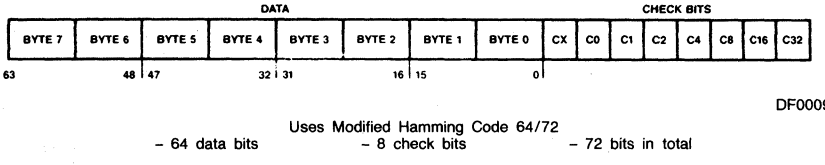
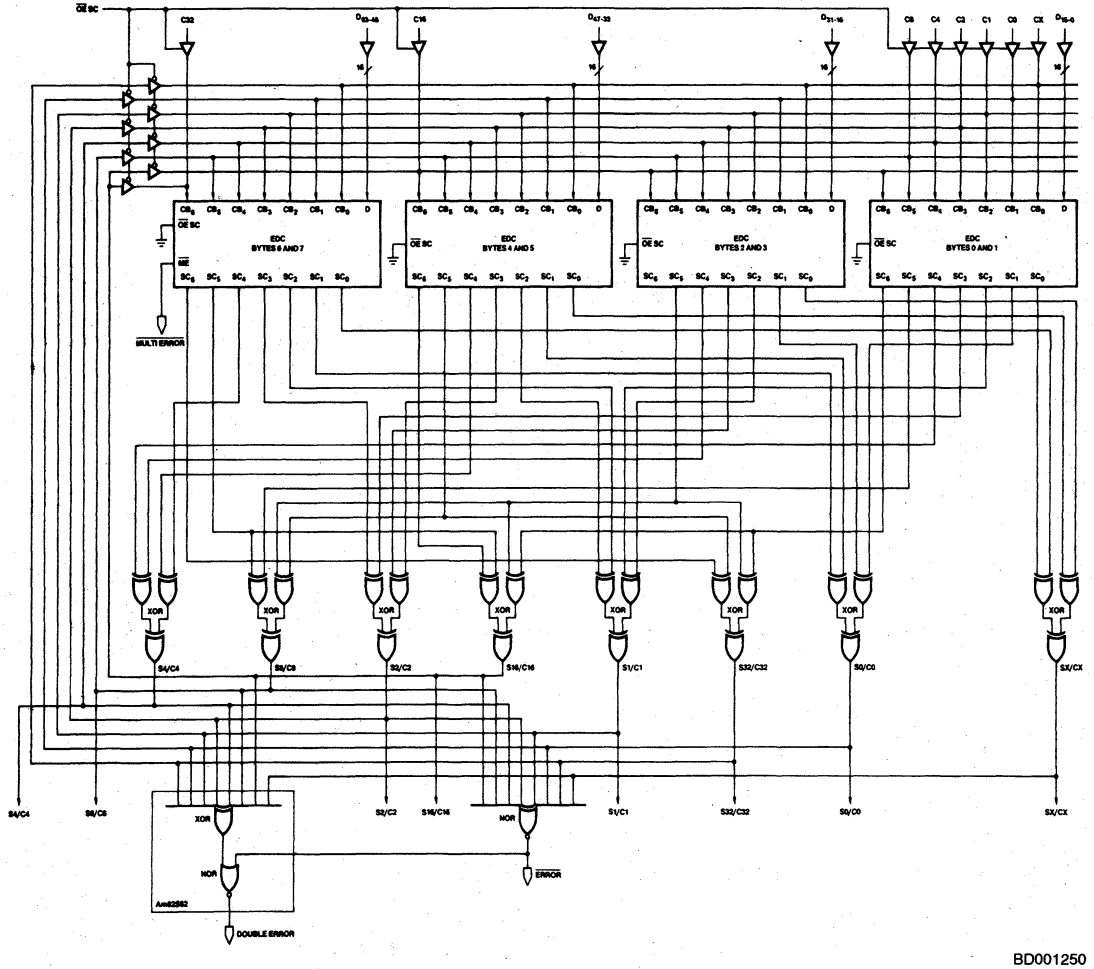


Figure 9. 64-Bit Data Format



BD001250

Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted.

Figure 10. AM2960—64-Bit Data Configuration

Refer to Page 13-1 for Essential Information on Military Devices

TABLE XI.
KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Component Delays from Am2960 AC Specifications, Table C (plus MSI)
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA In	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE XII. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

TABLE XII.
64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE (Cont.)

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE XIII. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits																		
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	CS	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* – no errors detected
Number – the number of the single bit-in-error
T – two errors detected
M – more than two errors detected

TABLE XIV. DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID 0
41	Slice 4/5 – CODE ID 1
42	Slice 4/5 – CODE ID 2
43	Slice 4/5 – DIAG MODE 0
44	Slice 4/5 – DIAG MODE 1
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID 0
57	Slice 6/7 – CODE ID 1
58	Slice 6/7 – CODE ID 2
59	Slice 6/7 – DIAG MODE 0
60	Slice 6/7 – DIAG MODE 1
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASS THRU
63	Don't Care

SYSTEM DESIGN CONSIDERATIONS

High Performance Parallel Operation

For maximum memory system performance, the EDC should be used in the Check-Only configuration shown in Figure 11. With this configuration, the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the RAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors. If an error exists, the EDC's error flags are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown. But even if the memory system had an error every hour this would mean only one error every 3-4 *billion* memory cycles. So even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. But using the Am2961/62 Data Bus Buffers allows the data word to be buffered on the memory board while check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for EDC is to have the EDC directly in the data path, as shown in Figure 12 (Correct-Always Configuration). In this configuration, data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantage is that memory system speed is slowed by the amount of time it takes for error correction on every cycle.

Usually the Correct-Always Configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high performance processors will use the high performance parallel configuration shown in Figure 11 (Check-Only Configuration).

Scrubbing Avoids Double Errors

Single-bit errors are by far the most common in a memory system, and are always correctable by the EDC.

Double-bit memory errors are far less frequent than single-bit (50 to 1, or 100 to 1) and are always detected by the EDC, but not corrected.

In a memory system, soft errors occur only one at a time. A double-bit error in a data word occurs when a single soft error is left uncorrected and is followed by another error in the data word hours, days, or weeks after the first.

"Scrubbing" memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the data word written back into

memory. Errors are not allowed to pile up, and most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor. If memory is scrubbed frequently, errors that are detected and corrected during processor accesses need not be immediately written back into memory. Instead, the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

Correction of Double-Bit Errors

In some cases, double-bit memory errors can be corrected! This is possible when one of the two bit errors is a hard error.

When a double bit error is detected, the data word should be checked to determine if one of the errors is a hard error. If so, the hard error bit may be corrected by inverting it, leaving only a single, correctable error. The time for this operation is negligible, since it will occur infrequently.

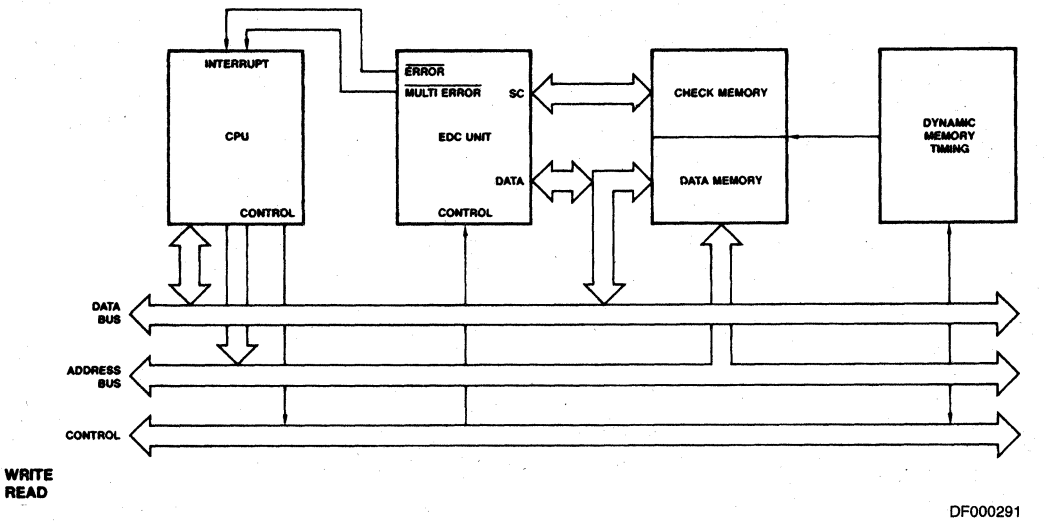


Figure 11. Check-Only Configuration

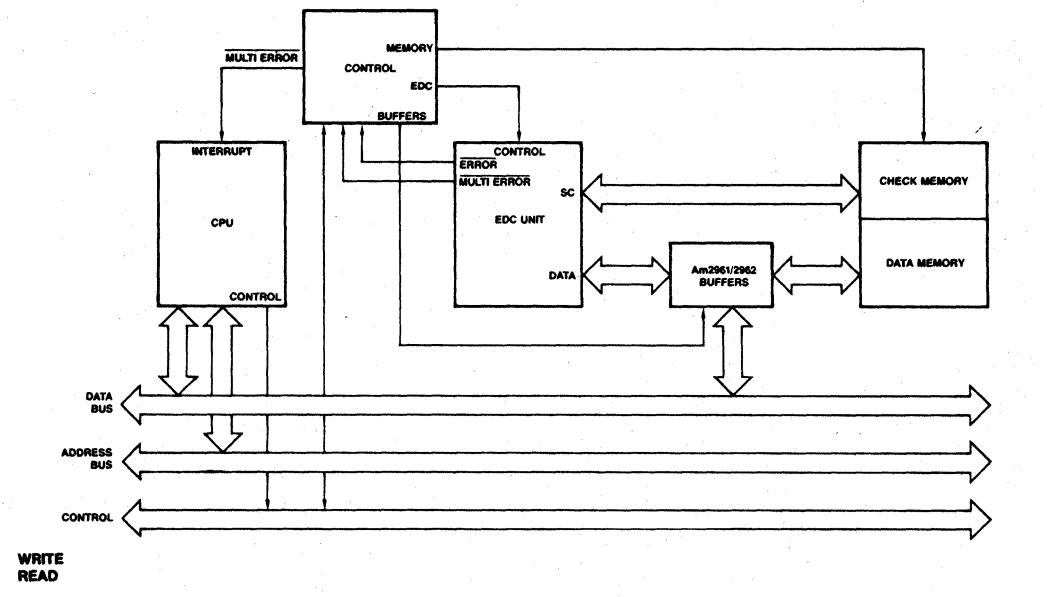


Figure 12. Correct-Always Configuration

The procedure after detection of a double error is as follows:

- Invert the data bits read from memory.
- Write the inverted data back into the same memory word.
- Re-read the memory location and XOR the newly read out value with the old. If there is no hard error, then the XOR result will be all 1's. If there is a hard error, it will have the same bit value regardless of what was written in. So it will show as a 0 after the XOR operation.
- Invert the hard error bit (this will "correct" it) leaving only one error in the data.
- The EDC can then correct the single bit error.
- Rewrite the correct data word into memory. This does not change the hard error, but does eliminate the soft error. So the next memory access will find only a single-bit, correctable error.

An example helps to illustrate the procedure:

Example of Double-Bit Error Correction When One is a Hard Error

	16 data bits	6 check bits
1. Data Read from Memory (D_1)	1111111100000011	011010
2. EDC detects a multiple error. Syndromes:		011000
3. Syndrome decode indicates a double-bit error.		
4. Invert the bits read from memory (D_1)	0000000011111100	100101
5. Write D_1 back to the same memory location		
6. Read back the memory location (D_2)	0000000011111101	100101
7. XOR D_1 and D_2	1111111111111110	111111
8. So the last data bit is the hard error. Use this to modify D_1	1111111100000010	011010
9. Pass the modified D_1 through the EDC. The EDC detects a single bit correctable error and outputs corrected data:	1111111100000000	011010
10. Write the corrected data back to memory to fix the soft error.		

Error Logging and Preventative Maintenance

The effectiveness of preventative maintenance can be increased by logging information on errors detected by the EDC. This is called error logging.

The EDC provides syndromes when errors are detected. The syndromes indicate which bit is in error. In most memory systems, each individual RAM supplies only one bit of the memory word. So the syndrome and data word address specify which RAM was in error.

Typically a permanent/hard RAM failure is preceded by a period of time where the RAM displays an increasing frequency of intermittent, soft errors. Error logging statistic can be used to detect an increasing intermittent error frequency so that the RAM can be replaced before a permanent failure occurs.

Error logging also records the location of already hard failed RAMs. With EDC a hard failure will not halt system operation. EDC can always correct single-bit errors even if it is a hard error. EDC can also correct double-bit errors where one is hard and one soft (see "Correction of Double Bit Errors" Section). The ability to continue operation despite hard errors can greatly reduce the need for emergency field maintenance. The hard-failed RAMs can be instead replaced at low cost during a regularly-scheduled preventative maintenance session.

Reducing Check Bit Overhead

Memory word widths need not be the same as the data word width of the processor. There is a substantial reduction in check bit overhead if wider memory words are used:

Memory Word		Check
# Data Bits	# Check Bits	Bit Overhead
8	5	38%
16	6	27%
32	7	14%
64	8	11%

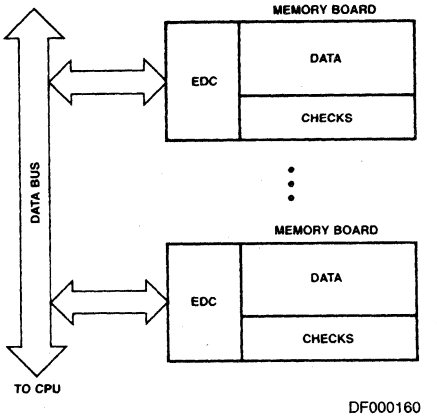


Figure 13. EDC Per Board

This reduction in check bit overhead lowers cost and increases the amount of data that can be packed on to each board.

The trade-off is that when writing data pieces into memory that are narrower than the memory word width, more steps are required. These steps are exactly the same as those described in Byte Write in the Applications section. No penalty exists for reads from memory.

EDC Per Board vs EDC Per System

The choice of an EDC per system or per board depends on the economics and the architecture of the system.

Certainly the cheaper approach is to have only one EDC per system and this is a viable solution if only one memory location is accessed at a time.

This solution does require that the system has both data and check bit lines (see Figure 14). This makes retrofitting a system difficult and creates complications if static or ROM memory, which do not require check bits, are mixed in with dynamic RAM.

If the system has an advanced architecture, it is quite likely that it is necessary to simultaneously access memory locations on different memory boards (see Figure 13). Architectural features that require this are interleaved memory, cache memory, and DMA that is done simultaneously with processor memory accesses. EDC per board is a simpler system from a design standpoint.

The EDC is designed to work efficiently in either the per system or per board configurations.

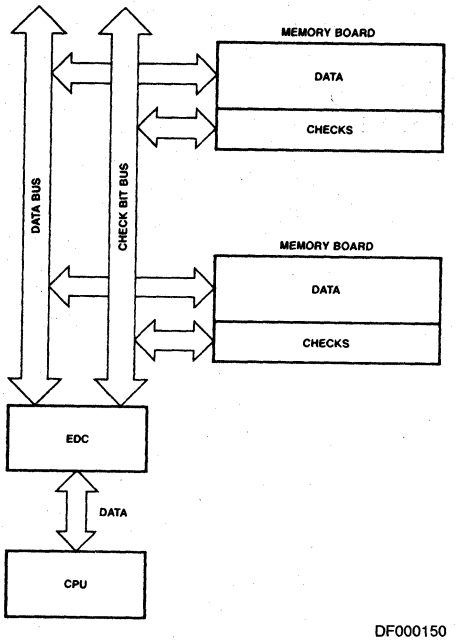


Figure 14. EDC Per System

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the AM2960 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

Definitions

D_i ← ($DATA_i$ if LE IN is HIGH or the output of bit i of the Data Input Latch if LE IN is LOW)
C_i ← (CB_i if LE IN is HIGH or the output of bit i of the Check Bit Latch if LE IN is LOW)
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)

$PA \leftarrow D0 \oplus D1 \oplus D2 \oplus D4 \oplus D6 \oplus D8 \oplus D10 \oplus D12$
$PB \leftarrow D0 \oplus D1 \oplus D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7$
$PC \leftarrow D8 \oplus D9 \oplus D10 \oplus D11 \oplus D12 \oplus D13 \oplus D14 \oplus$
$PD \leftarrow D0 \oplus D3 \oplus D4 \oplus D7 \oplus D9 \oplus D10 \oplus D13 \oplus D15$
$PE \leftarrow D0 \oplus D1 \oplus D5 \oplus D6 \oplus D7 \oplus D11 \oplus D12 \oplus D13$
$PF \leftarrow D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7 \oplus D14 \oplus D15$
$PG_1 \leftarrow D0 \oplus D4 \oplus D6 \oplus D7$
$PG_2 \leftarrow D1 \oplus D2 \oplus D3 \oplus D5$
$PG_3 \leftarrow D8 \oplus D9 \oplus D11 \oplus D14$
$PG_4 \leftarrow D10 \oplus D12 \oplus D13 \oplus D15$

Error Signals

$\overline{ERROR} \leftarrow (\overline{S6} \cdot (ID_1 + ID_2)) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU

$\overline{MULT\ ERROR}$ (16 and 32-Bit Modes) $\leftarrow \overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)}\ (\overline{ERROR})$ + TOME + GENERATE + PASSTHRU + INITIALIZE

$\overline{MULT\ ERROR}$ (64-Bit Modes) $\leftarrow \overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

TOME (Three or More Errors)*

			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			**S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S5	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1	1
			S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S1	S2	S3																	
0	0	0		0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1		0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0		0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0		0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	1		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	1	1		0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

*(S6, S5, ... S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes the syndromes are input over the Check-Bit lines. S6←C6, S5←C5, ...S1←C1, S0←C0.
**The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables XV, XVI, XVII, XVIII, XIX show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE XV.

GENERATE Mode (Check Bits)	CODE ID_{2-0}						
	000	010	011	100	101	110	111
SC_0←	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
SC_2←	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
SC_3←	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
SC_4←	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
SC_5←	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
SC_6←	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

TABLE XVI.

Detect and Correct Modes (Syndromes)	CODE ID_{2-0}						
	000	010	011*	100	101	110	111
SC_0←	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
SC_2←	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
SC_3←	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
SC_4←	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
SC_5←	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
SC_6←	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Latch operates normally.

TABLE XVII.

Diagnostic Read Mode	CODE ID_{2-0}						
	000	010	011*	100	101	110	111
SC_0←	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
SC_2←	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
SC_3←	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
SC_4←	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
SC_5←	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
SC_6←	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Latch operates normally.

TABLE XVIII.

Diagnostic Write Mode	CODE ID_{2-0}						
	000	010	011*	100	101	110	111
SC_0←	DL_0	DL_0	CB_0	DL_0	1	1	1
SC_1←	DL_1	DL_1	CB_1	DL_1	1	1	1
SC_2←	DL_2	DL_2	CB_2	DL_2	1	1	1
SC_3←	DL_3	DL_3	CB_3	DL_3	1	1	1
SC_4←	DL_4	DL_4	CB_4	DL_4	1	1	1
SC_5←	DL_5	DL_5	CB_5	DL_5	1	1	1
SC_6←	1	DL_6	CB_6	1	1	DL_6	DL_7

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE XIX.

PASS THRU Mode	CODE ID_{2-0}						
	000	010	011*	100	101	110	111
SC_0←	C0	C0	CB_0	C0	1	1	1
SC_1←	C1	C1	CB_1	C1	1	1	1
SC_2←	C2	C2	CB_2	C2	1	1	1
SC_3←	C3	C3	CB_3	C3	1	1	1
SC_4←	C4	C4	CB_4	C4	1	1	1
SC_5←	C5	C5	CB_5	C5	1	1	1
SC_6←	1	C6	CB_6	1	1	C6	C6

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

Data Correction

Tables XX to XXVI shows which data output bits are corrected (inverted) depending upon the syndromes and the CODE ID position. Note that the syndromes that determine data correction are in some cases syndromes input externally via the CB inputs and in some cases syndromes generated internally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

The tables show the number of data bit inverted (corrected) if any for the CODE ID and syndrome combination.

TABLE XX. CODE ID_{2-0} = 000*

	S5	0	0	0	0	1	1	1	1
	S4	0	0	1	1	0	0	1	1
	S3	0	1	0	1	0	1	0	1
S2	S1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXI. CODE ID_{2-0} = 010*

	CB_6	0	0	0	0	1	1	1	1
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	11	14	–	–	–	–	5
0	1	8	12	–	–	–	1	2	6
1	0	9	13	15	–	–	–	3	7
1	1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

TABLE XXII. CODE $ID_{2\text{-}0} = 011$*

	S6	0	0	0	0	1	1	1	1
	S5	0	0	0	0	1	1	1	1
	S4	0	0	1	1	0	0	1	1
	S3	0	1	0	1	0	1	0	1
S2 S1									
0 0		–	–	–	5	–	11	14	–
0 1		–	1	2	6	8	12	–	–
1 0		–	–	3	7	9	13	15	–
1 1		–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXIII. CODE $ID_{2\text{-}0} = 100$*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	0	0	0	0	1	1	1	1
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2CB_1									
0 0		–	11	14	–	–	–	–	5
0 1		8	12	–	–	–	1	2	6
1 0		9	13	15	–	–	–	3	7
1 1		10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

TABLE XXIV. CODE $ID_{2\text{-}0} = 101$*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	0	0	0	0	1	1	1	1
	CB_5	0	0	0	0	1	1	1	1
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2CB_1									
0 0		–	–	–	5	–	11	14	–
0 1		–	1	2	6	8	12	–	–
1 0		–	–	3	7	9	13	15	–
1 1		–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXV. CODE $ID_{2\text{-}0} = 110$*

	CB_0	0	0	0	0	1	1	1	1
	CB_6	1	1	1	1	0	0	0	0
	CB_5	0	0	0	0	1	1	1	1
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2CB_1									
0 0		–	–	–	5	–	11	14	–
0 1		–	1	2	6	8	12	–	–
1 0		–	–	3	7	9	13	15	–
1 1		–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXVI. CODE $ID_{2\text{-}0} = 111$*

	CB_0	0	0	0	1	1	1	1
	CB_6	1	1	1	0	0	0	0
	CB_5	1	1	1	0	0	0	0
	CB_4	0	0	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2CB_1									
0 0		–	11	14	–	–	–	–	5
0 1		8	12	–	–	–	1	2	6
1 0		9	13	15	–	–	–	3	7
1 1		10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

APPLICATIONS

Byte Write

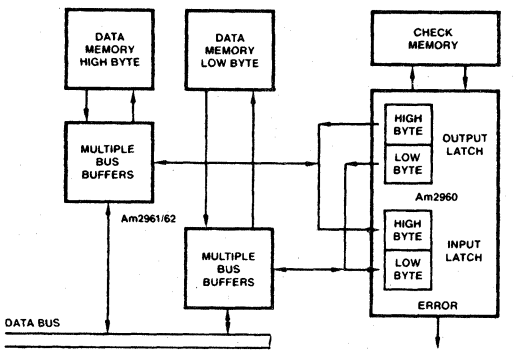
Byte operations are increasingly common for 16-bit and 32-bit processors. These complicate memory operations because check bits are generated for a complete 16-bit or 32-bit or 64-bit memory word – not for a single byte.

To write a byte into memory with EDC requires the following steps:

- Latch the byte into the Am2961/62 bus buffers (Figure 15)
- Read the complete data word from memory (Figure 15)
- Correct the complete data word if necessary (Figure 15)
- Insert the byte to be written into the data word (Figure 16)
- Generate new check bits for the entire data word (Figure 16)
- Store the data word back into memory (Figure 16)

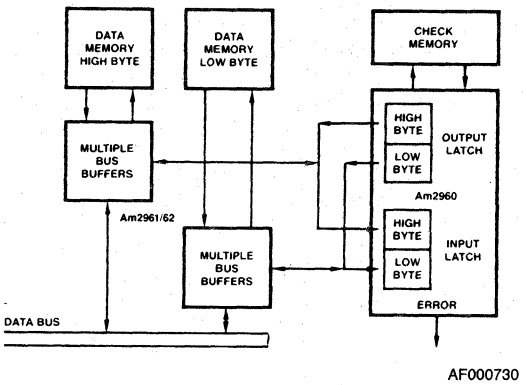
(In fact, these steps must be taken for any piece of data being written into memory that is not as wide as a full memory word.)

The Am2960 EDC is designed with the intent of keeping byte operations simple in EDC systems. The EDC has separate output enables for each byte in the Data Output Latch. As shown in Figures 15 and 16, this allows the data word to be read from memory, the new byte to be inserted among the old, and new check bits to be generated using less time and less hardware than if separate byte enables were not available.



AF000730

Figure 15. Byte Write, Phase 1: Read Out the Old Word and Correct



AF000730

Figure 16. Byte Write, Phase 2: Insert the New Byte, Generate Checks and Write Into Memory

Diagnostics

EDC is used to boost the reliability of the overall system. It is necessary to also be able to check the operation of the EDC itself. For this reason the EDC has an internal control mode, a diagnostic latch, and two diagnostic modes.

To check that the EDC is functioning properly, the processor can put the EDC under software control by setting CODE $ID_{2\text{-}0}$ to 001. This puts the EDC into Internal Control Mode. In Internal Control Mode the EDC is controlled by the contents of the Diagnostic Latch which is loaded from the DATA inputs under processor control.

The EDC is set into CORRECT Mode. The processor loads in a known set of check bits into the Diagnostic Latch, a known set of data bits into the Data In Latch, and forces data errors. The output of the EDC (syndromes, error flags, corrected data) is then compared against the expected responses. By exercising the EDC with a string of data/check combinations and comparing the output against the expected responses, the EDC can be fully checked out.

Eight Bit Data Word

Eight bit MOS microprocessors can use EDC too. Only five check bits are required. The EDC configuration for eight bits is shown in Figure 17. It operates as does the normal 16-bit configuration with the upper byte fixed at 0.

Check bit overhead for 8-bit data words can be reduced two ways. See the sections "Single Error Correction Only" and "Reducing Check Bit Overhead."

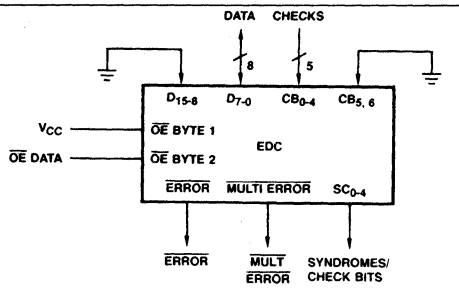


Figure 17. 8-Bit Configuration

Other Word Widths

EDC on data words other than 8, 16, 32, of 64 bits can be accomplished with the AM2960. In most cases the extra data bits can be forced to a constant, and EDC will proceed as normal. For example, a 24-bit data word is shown in Figure 18.

Single Error Correction Only

The EDC normally corrects all single-bit errors *and* detects all double-bit and some triple-bit errors. To save one check bit per word, the ability to detect double bit errors can be sacrificed – single errors are still detected and corrected.

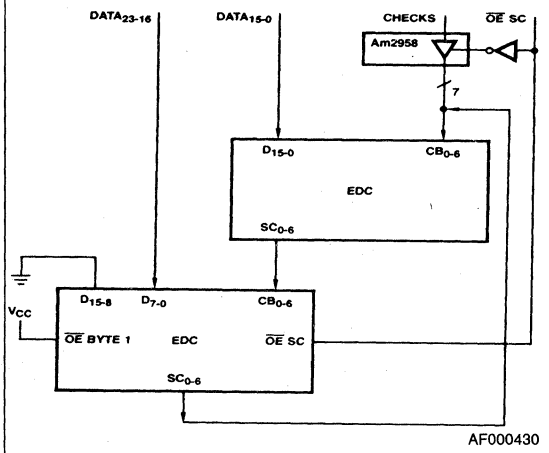


Figure 18. 24-Bit Configuration

Data Bits	Check Bits Required	
	Single Error Correction Only	Single Error Correct & Double Error Detect
8	4	5
16	5	6
32	6	7
64	7	8

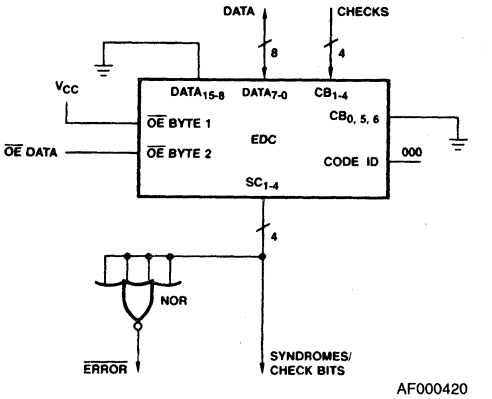


Figure 19. 8-Bit Single Error Correction Only

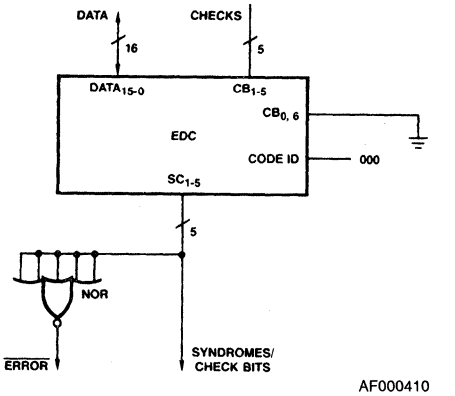
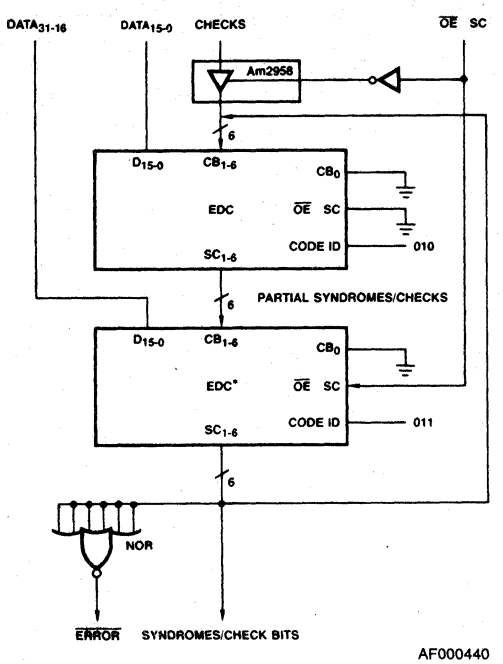


Figure 20. 16-Bit Single Error Correction Only



* The Code ID Combination for this Slice Forces the Check Bit Latch Transparent.

Figure 21. 32-Bit Single Correct Only

Figures 19, 20, 21, 22 show single error correction only configurations for 8, 16, 32, and 64-bit data words respectively.

Check Bit Correction

The EDC detects single bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

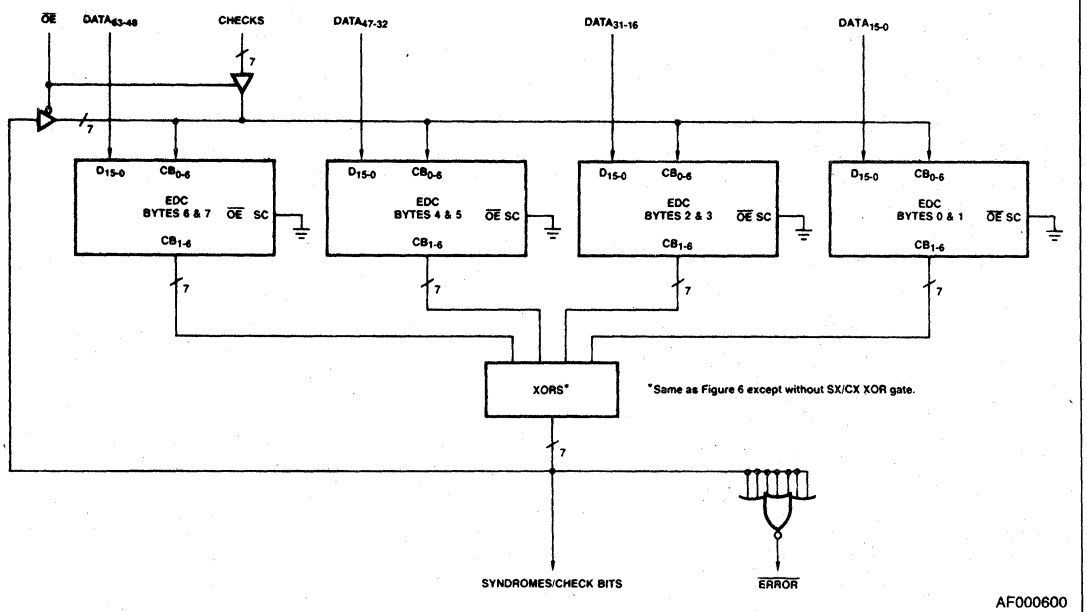
The syndromes generated by the EDC may be decoded to determine whether the single bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory (see section in System Design Considerations).

Multiple Errors

The bit-in-error decode logic uses syndrome bits S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S2, S4, S8) is produced. This is flagged a double error by the error detection logic, but the bit-in-error decoder only receives syndrome 11100 (S0, S1, S2, S4, S8), which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this inversion, the multiple error output may be connected to the correct input as in Figure 23. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.



Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch appear on the XOR Outputs Inverted.

Figure 22. 64-Bit Single Correct Only

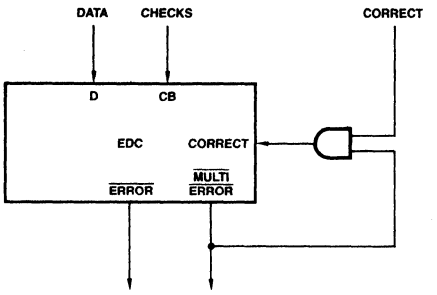


Figure 23. Inhibition of Data Modification

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Case)
Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} Max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Descriptions	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.8mA	COM'L	2.7			Volts
				MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA				0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX V_{IN} = 0.5V	$DATA_{0-15}$				−410	μA
			All Other Inputs				−360	
I_{IH}	Input HIGH Current	V_{CC} = MAX V_{IN} = 2.7V	$DATA_{0-15}$				70	μA
			All Other Inputs				50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} MAX	$DATA_{0-15}$	V_O = 2.4			70	μA
				V_O = 0.5			−410	
			SC_{0-6}	V_O = 2.4			50	
				V_O = 0.5			−50	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = V_{CC} MAX +0.5V, V_O = 0.5V			−25		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX		T_A = 25°C		275	390	mA
			COM'L	T_A = 0 to +70°C			400	
				T_A = +70°C			365	
			MIL	T_C = −55 to +125°C			400	
				T_C = +125°C			345	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2960XM, DM, FM. "COM'L" = Am2960XC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING TEST CIRCUIT

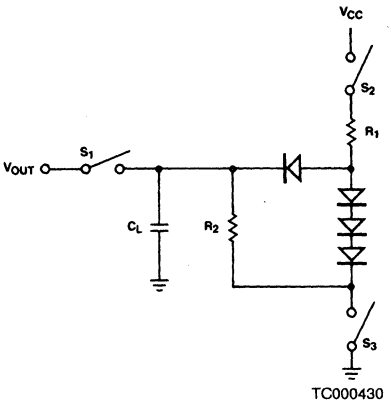


Figure 24. Three-State Outputs

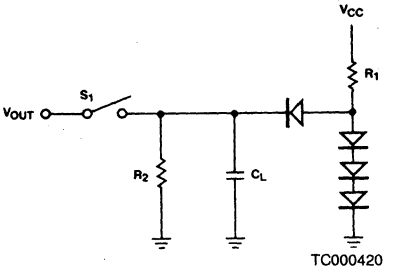


Figure 25. Normal Outputs

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function test and all A.C. tests, except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. R_2 = 1K for three-state output.
R_2 is determined by the I_{OH} at V_{OH} = 2.4V for non-three-state outputs.
5. R_1 is determined by I_{OL} (MIL) with V_{CC} = 5.0V minus the current to ground through R_2.
6. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS

Pin #	Pin Label	Test Circuit	R_1	R_2
–	D_0-D_{15}	Fig. 24	430Ω	1KΩ
24-30	SC_0-SC_6	Fig. 24	430Ω	1KΩ
32	$\overline{\text{ERROR}}$	Fig. 25	470Ω	3kΩ
33	$\overline{\text{MULTERROR}}$	Fig. 25	470Ω	3KΩ

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0.4V$ and $V_{IH} \leqslant 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.
7. Changing the CODE ID inputs can cause loss of data in some of the Am2960 internal latches. Specifically, the entire checkbit latch and bits 6 and 7 of the diagnostic latch are indeterminate after a change in CODE ID inputs.

Logic simulations should store "x" (i.e., "don't care") in these bits after CODE ID change. Test programs should reload these registers before they are used.

1. Am2960 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DC, XC.

A. Combinational Propagation Delays
C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65*	32	50
CB_{0-6} (CODE ID_{2-0}000,011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0}010,100, 101,110,111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE IN (From latched to transparent)	39	72*	39	59
LE OUT (From latched to transparent)	–	31	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE DIAG (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	6	7
CB_{0-6}	LE IN	5	6
$DATA_{0-15}$	LE OUT	44	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
$\overline{GENERATE}$	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID_{2-0}	LE OUT	81	0
LE IN	LE OUT	51	5
$DATA_{0-15}$	LE DIAG	6	8

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	30	30
$\overline{OE}$ SC	SC_{0-6}	30	30

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

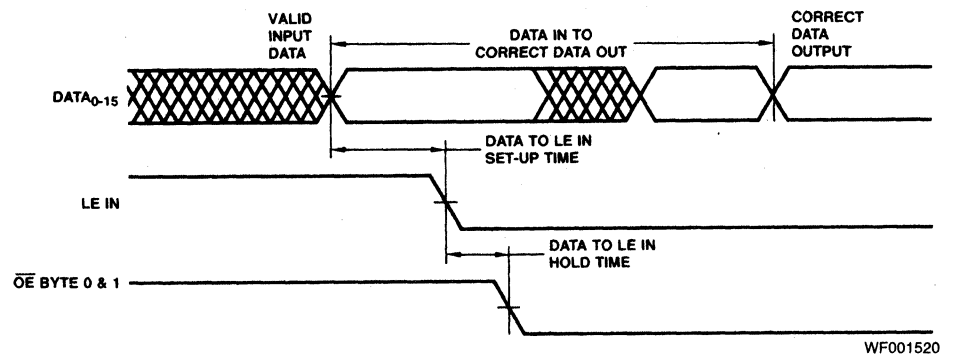


Figure D.

1. Am2960 Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960 over the military operating range of −55°C to +125°C case temperature, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73*	36	56
CB_{0-6} (CODE ID_{2-0}000,011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0}010,100, 101,110,111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE IN (From latched to transparent)	44	82*	43	66
LE OUT (From latched to transparent)	–	33	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE DIAG (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	7	7
CB_{0-6}	LE IN	5	7
$DATA_{0-15}$	LE OUT	50	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	30	0
$\overline{GENERATE}$	LE OUT	46	0
CORRECT	LE OUT	28	1
DIAG MODE	LE OUT	84	0
PASS THRU	LE OUT	30	0
CODE ID_{2-0}	LE OUT	89	0
LE IN	LE OUT	59	5
$DATA_{0-15}$	LE DIAG	7	9

C. Output Enable/Disable Times

Output disable tests performed with $C_L = 5pF$ and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	35	35
$\overline{OE}$ SC	SC_{0-6}	35	35

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

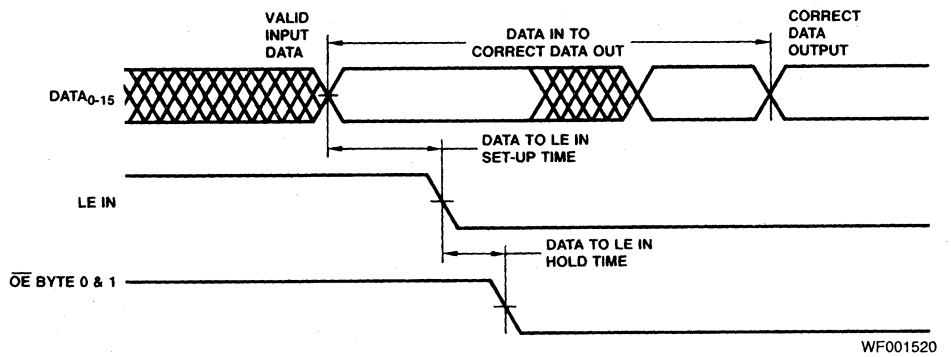


Figure D.

Am2960A Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960A over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960ADC, XC.

A. Combinational Propagation Delays

C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$				
CB_{0-6} (CODE ID_{2-0}000,011)				
CB_{0-6} (CODE ID_{2-0}010,100, 101,110,111)				
$\overline{GENERATE}$				
CORRECT (Not Internal Control Mode)				
DIAG MODE (Not Internal Control Mode)				
PASS THRU (Not Internal Control Mode)				
CODE ID_{2-0}				
LE IN (From latched to transparent)				
LE OUT (From latched to transparent)				
LE DIAG (From latched to transparent; Not Internal Control Mode)				
Internal Control Mode: LE DIAG (From latched to transparent)				
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)				

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN		
CB_{0-6}	LE IN		
$DATA_{0-15}$	LE OUT		
CB_{0-6} (CODE ID 000, 011)	LE OUT		
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT		
$\overline{GENERATE}$	LE OUT		
CORRECT	LE OUT		
DIAG MODE	LE OUT		
PASS THRU	LE OUT		
$CODE\ ID_{2-0}$	LE OUT		
LE IN	LE OUT		
$DATA_{0-15}$	LE DIAG		

C. Output Enable/Disable Times

Output disable tests performed with $C_L = 5pF$ and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$		
$\overline{OE}$ SC	SC_{0-6}		

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	

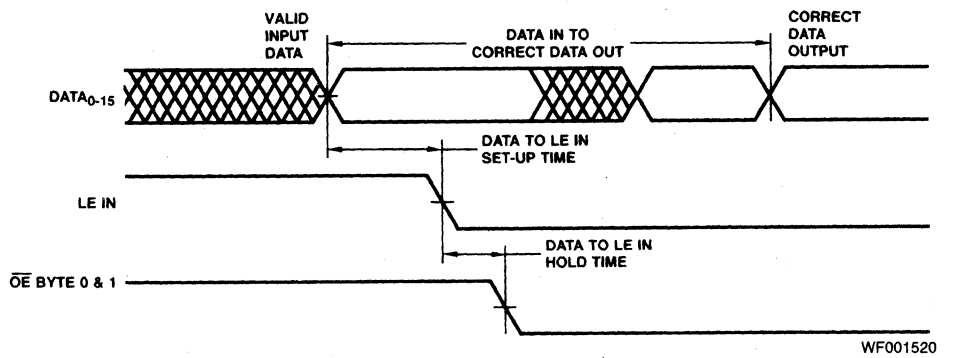


Figure D.

Am2960A Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960A over the military operating range of −55°C to +125°C case temperature, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have the maximum DC load.

This data applies to the following part numbers: Am2960ADM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$				
CB_{0-6} (CODE ID_{2-0}000,011)				
CB_{0-6} (CODE ID_{2-0}010,100, 101,110,111)				
$\overline{GENERATE}$				
CORRECT (Not Internal Control Mode)				
DIAG MODE (Not Internal Control Mode)				
PASS THRU (Not Internal Control Mode)				
CODE ID_{2-0}				
LE IN (From latched to transparent)				
LE OUT (From latched to transparent)				
LE DIAG (From latched to transparent; Not Internal Control Mode)				
Internal Control Mode: LE DIAG (From latched to transparent)				
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)				

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN		
CB_{0-6}	LE IN		
$DATA_{0-15}$	LE OUT		
CB_{0-6} (CODE ID 000, 011)	LE OUT		
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT		
$\overline{GENERATE}$	LE OUT		
CORRECT	LE OUT		
DIAG MODE	LE OUT		
PASS THRU	LE OUT		
CODE ID_{2-0}	LE OUT		
LE IN	LE OUT		
$DATA_{0-15}$	LE DIAG		

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$		
$\overline{OE}$ SC	SC_{0-6}		

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	

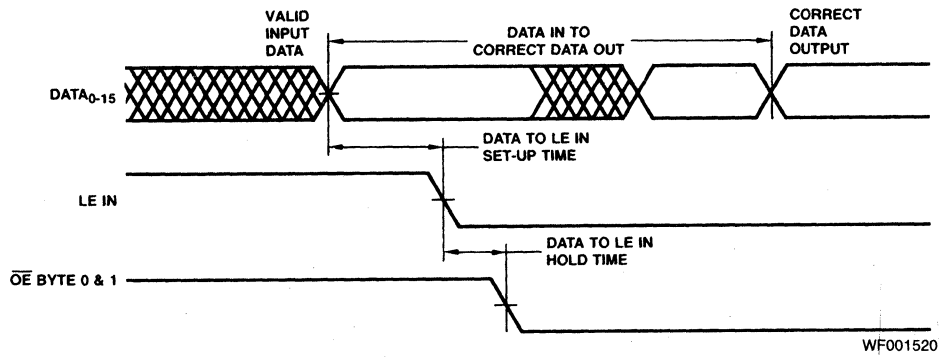


Figure D.

Am2961/Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and noninverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Space saving 24-pin 0.3″ package

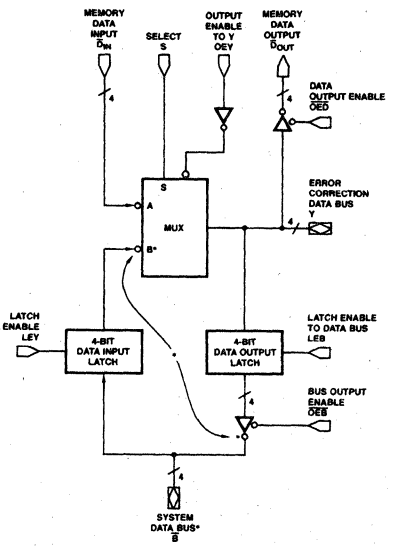
GENERAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus, thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

BLOCK DIAGRAM



BD001170

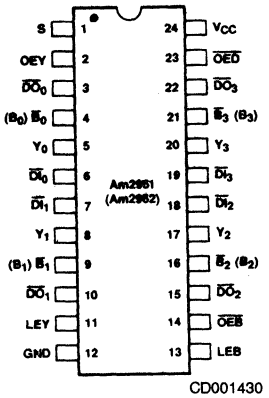
*Am2962 is the same function but noninverting to the system data bus, B.

ADVANCED INFORMATION

- 25 – 30% speed improvement plug-in replacements for Am2961/ Am2962.

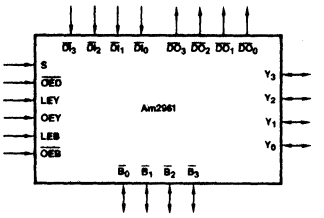
03534B

CONNECTION DIAGRAM
Top View
D-24-SLIM



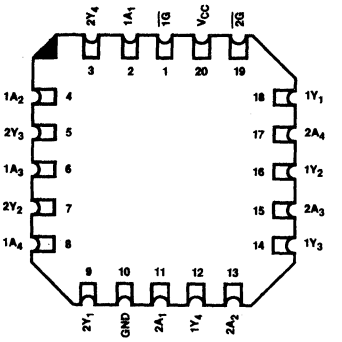
CD001430

LOGIC SYMBOL



LS000480

CONNECTION DIAGRAM
Leadless Chip Carrier
L-28-1

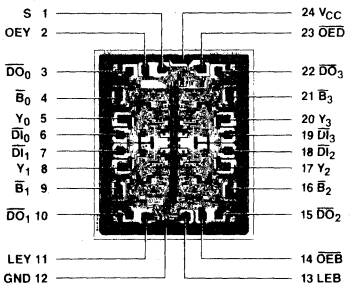


CD004860

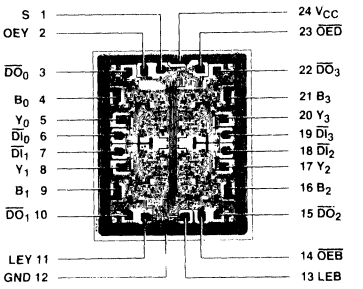
Note: Pin 1 is marked for orientation. B-Bus is noninverting for Am2962.

METALLIZATION AND PAD LAYOUT

Am2961



Am2962



DIE SIZES .102" x .087"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2961
Am2962

D — Package
D– 24-pin CERDIP (D-24-SLIM)
L – 28-pin leadless chip carrier (L-28-1)

C — Temperature (See Operating Range)
C – Commercial (0°C to +70°C)
M – Military (–55°C to +125°C)

B — Screening Option
Blank – Standard processing
B – Burn-in

Device type
4-Bit Error Correction Multiple Bus Buffers

Valid Combinations	
Am2961 Am2962	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4,9, 16,21	B_0, B_1, B_2, B_3	I/O	The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the Am2961 ($\overline{B}_I$) and noninverting for the Am2962 (B_I).
14	$\overline{OEB}$	I	The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW, data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH, the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.
13	LEB	I	Latch Enable for the Data Output Latch. When LEB is HIGH, the latch is transparent and Y–Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.
5, 8, 17, 20	Y_0, Y_1, Y_2, Y_3	I/O	The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.
11	LEY	I	The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.
2	OEY	I	Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH, data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW, the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.
1	S	I	The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).
3, 10, 15, 22	$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$	O	The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.
23	$\overline{OED}$	I	Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.
6, 7, 18, 19	$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$	I	The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI}_I$	$\overline{B}_I$* Am2961	B_I* Am2962	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

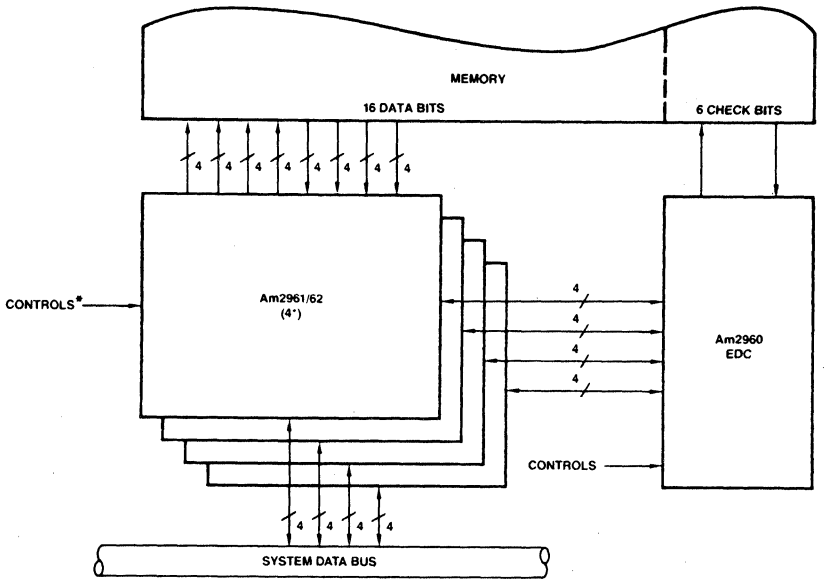
Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ Am2961	B Am2962
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

APPLICATION



AF000340

*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} Max
DC Input Voltage 5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGE – Y BUS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA		0.3	0.45	Volts
			I_{OL} = 16mA		0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	OEY = LOW			−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−30		−130	mA

DC CHARACTERISTICS OVER OPERATING RANGE – B BUS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA	2.4			Volts
			I_{OH} = −15mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA		0.3	0.45	Volts
			I_{OL} = 24mA		0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{OEB}$ = HIGH			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−50		−150	mA

Notes: 1. For conditions as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DC CHARACTERISTICS OVER OPERATING RANGE – DO OUTPUTS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = –50μA	2.5			Volts
			COM'L I_{OH} = –100μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		–50		–150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4V			–100	μA
			V_O = 2.4V			+100	

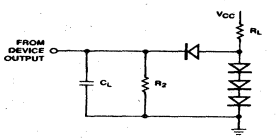
DC CHARACTERISTICS OVER OPERATING RANGE – DI INPUTS AND CONTROLS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = –18mA				–1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DI Inputs			–1.0	mA
			Controls			–1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA

DC CHARACTERISTICS OVER OPERATING RANGE – POWER SUPPLY

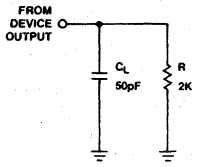
Parameters	Descriptions	Test Conditions (Note 1)	Min	Typ (Note 2)	Max	Units
I_{CC}	Power Supply Current	V_{CC} = MAX		110	155	mA

SWITCHING TEST CIRCUIT



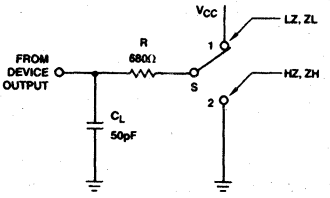
TC000400

Figure 1.



TC000530

Figure 2.



TC000410

Figure 3.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Am2961

Parameters	Description	Test Conditions		COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1, C_L = 5pF, R_L = 390Ω, R_2 = 1kΩ			25		28	ns
t_{PHL}					25		28	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)				15		18	ns
t_{PHL}					15		18	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)				25		28	ns
t_{PHL}					25		28	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)				25		30	ns
t_{PHL}					35		40	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y				18		21	ns
t_{PZL}					18		21	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y				18		21	ns
t_{PLZ}					18		21	ns
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ			25		30	ns
t_{PHL}					35		40	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)				18		21	ns
t_{PHL}					20		23	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ			26		30	ns
t_{PHL}					31		35	ns
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ			18		21	ns
t_{PZL}					18		21	ns
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$				18		21	ns
t_{PHZ}					18		21	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2, C_L = 50PF, R = 2kΩ			15		18	ns
t_{PHL}					20		23	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	Figure 3, C_L = 50pF, R = 680Ω	S = 2		28		30	ns
t_{PZL}			S = 1		28		30	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		S = 2		16		18	ns
t_{PLZ}			S = 1		24		28	ns
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ		6		6		ns
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)			9		10		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ		6		6		ns
t_H	Y to LEB Hold Time (OEY = LOW)			9		10		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Am2962

Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay B to Y (Latch Transparent,OEY = LEY = HIGH)	Figure 1 C_L = 5pF R_L = 390Ω R_2 = 1kΩ		27		28	ns
t_{PHL}				27		28	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)			15		18	ns
t_{PHL}				15		18	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)			25		28	ns
t_{PHL}				25		30	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)			25		30	ns
t_{PHL}				35		40	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y			18		21	ns
t_{PZL}				18		21	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y			18		21	ns
t_{PLZ}				18		21	ns
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ		25		30	ns
t_{PHL}				35		40	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)			20		23	ns
t_{PHL}				21		24	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1 C_L = 300p F R_L = 270Ω R_2 = 1kΩ		28		32	ns
t_{PHL}				32		36	ns
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ		18		21	ns
t_{PZL}				18		21	ns
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B			18		21	ns
t_{PHZ}				18		21	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2 C_L = 50pF R = 2KΩ		15		18	ns
t_{PHL}				20		23	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	S = 2, Figure 3 C_L = 50pF R = 680Ω		28		30	ns
t_{PZL}		S = 1		28		30	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$	S = 2		16		18	ns
t_{PLZ}		S = 1		24		28	ns
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1 C_L = 50pF R_L = 390Ω R_2 = 1kΩ	8		8		ns
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)		8		9		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ	8		8		ns
t_H	Y to LEB Hold Time (OEY = LOW)		8		9		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am2964B/Am2964C*

Dynamic Memory Controller

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Burst mode, distributed refresh or transparent refresh mode determined by user

GENERAL DESCRIPTION

The Am2964B Dynamic Memory Controller (DMC) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX for output to the dynamic RAM address lines.

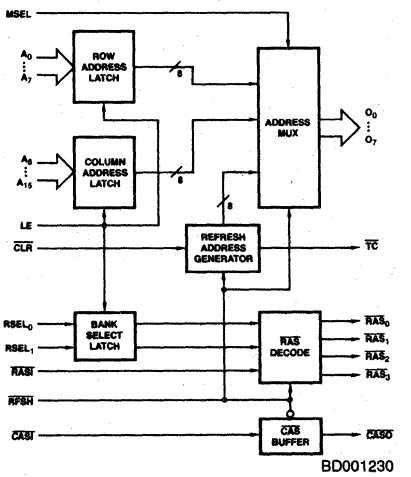
The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore allows a faster memory cycle time by the amount of skew eliminated.

The $\overline{RAS}$ Decoder allows upper addresses to select one-of-four banks of RAM by determining which bank receives a $\overline{RAS}$ input. During refresh ($\overline{RFSH}$ = LOW) the decoder mode is changed to four-of-four and all banks of memory receive a $\overline{RAS}$ input for refresh in response to a $\overline{RASI}$ active LOW input. $\overline{CAS}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{RFSH}$ LOW and toggling $\overline{RASI}$.

A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256.

BLOCK DIAGRAM



BD001230

ADVANCED INFORMATION

Am2964C

- Uses ECL internal circuitry with IMOX™ processing to offer higher performance
- Plug-in replacement for Am2964B

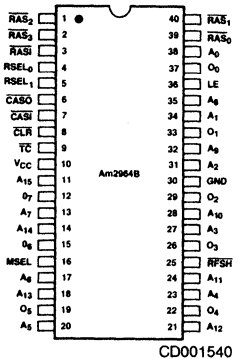
*'C' version incorporates higher speed/plug in compatability
IMOX is a trademark of Advanced Micro Devices, Inc.

03527B

Refer to Page 13-1 for Essential Information on Military Devices

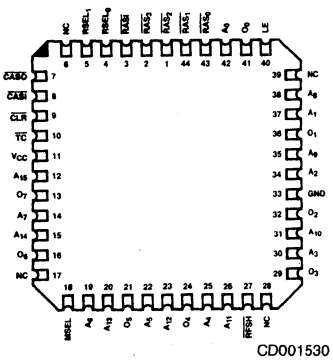
CONNECTION DIAGRAM
Top View

DIP



CD001540

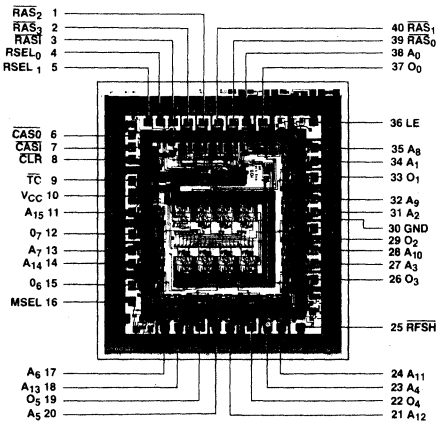
Leadless Chip Carrier



CD001530

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.156″ x 0.143″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2964B **D** **C** **B**

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 40-pin CERDIP (D-40-1)
  - L – 44-pin leadless chip carrier (L-44-1)
  - P – 40-pin plastic DIP (P-40-1)
  - X – Dice
- Am2964B — Device type
  - Dynamic Memory Controller

Valid Combinations	
Am2964B Am2964C	DC, DCB, DM, DMB LC, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$A_0 - A_7$	I	The low order Address inputs are used to latch eight Row Address inputs for the RAM. These inputs drive the outputs $O_0 - O_7$ when MSEL is HIGH.
	$A_8 - A_{15}$	I	The high order Address inputs are used to latch eight Column Address inputs for the RAM. These inputs drive the outputs $O_0 - O_7$ when MSEL is LOW.
11	A_{15}	I	A_{15} is a dual input. With normal TTL level inputs A_{15} acts as address input A_{15} for 64K RAMs. If A_{15} is pulled up to +12V through a 1KΩ resistor, the terminal count output. $\overline{TC}$, will go LOW every 128 counts (for 16K RAMs) instead of every 256 counts.
	$O_0 - O_7$	O	The RAM address outputs. The eight-bit width is designed for dynamic RAMs up to 64K.
16	MSEL	I	The Multiplexer-SELect input determines whether low order or high order address inputs appear at the multiplexer outputs $O_0 - O_7$. When MSEL is HIGH the low order address latches ($A_0 - A_7$) are connected to the outputs. When MSEL is LOW the high order address latches are connected to the outputs.
25	$\overline{RFSH}$	I	The Refresh control input. When active LOW the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{RFSH}$ LOW also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ and $\overline{RAS_3}$, go LOW in response to a LOW input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the LOW-to-HIGH transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held LOW and refresh accomplished by toggling $\overline{RASI}$.
9	$\overline{TC}$	O	The Terminal Court output. A LOW output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15}. The $\overline{TC}$ output remains active LOW until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.
8	$\overline{CLR}$	I	The refresh counter Clear input. An active LOW input at $\overline{CLR}$ resets the refresh counter to all LOW (refresh address output to all HIGH).
36	LE	I	The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.
4, 5	$RSEL_0$ and $RSEL_1$	I	The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the $\overline{RAS}$ Decoder to "$\overline{RAS}$ Select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$.
3	$\overline{RASI}$	I	The Row Address Strobe Input. During normal memory cycles the selected $\overline{RAS}$ Decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$ will go active LOW in response to an active LOW input at $\overline{RASI}$. During refresh ($\overline{RFSH}$ = LOW), all $\overline{RAS}$ outputs go LOW in response to $\overline{RASI}$ = LOW.
39, 40, 1, 2	$\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, $\overline{RAS_3}$	O	Row Address Strobe outputs ($\overline{RAS_i}$). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active LOW. All RAS_{0-3} outputs go active low in response $\overline{RASI}$ when $\overline{RFSH}$ goes LOW.
7	$\overline{CASI}$	I	The Column Address Strobe. An active LOW input at $\overline{CASI}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = LOW).
6	$\overline{CASO}$	O	The Column Address Strobe output. The active LOW $\overline{CASO}$ output strobes the Column Address into the dynamic RAM. $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = LOW).

$\overline{RAS}$ OUTPUT FUNCTION TABLE

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ FUNCTION TABLE

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTION TABLE

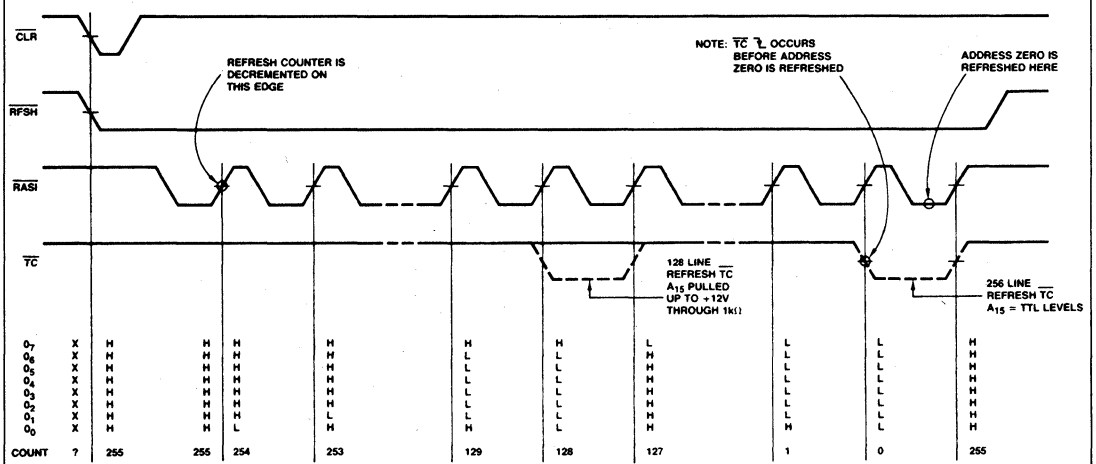
MSEL	$\overline{RFSH}$	O_0-O_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh Address

REFRESH ADDRESS COUNTER FUNCTION TABLE

A_{15}	$\overline{CLR}$	$\overline{RFSH}$	$\overline{RASi}$	$\overline{TC}$	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF_H	Clear Counter
X	H	↓	X	X	NC	Output Refresh Address No Change for Counter
X	H	↓	L	X	Count – 1	Return to Memory Cycle Mode and Decrement Counter
X	H	L	↓	X	NC	Output all RAS_i to RAM No Change for Counter
X	H	L	↓	X	Count – 1	Return RAS_i to HIGH and Decrement Counter
L or H	H	X	X	L	00_H	Terminal Count for 256 Line Refresh
+12V*	H	X	X	L	00_H and 80_H	Terminal Count for 128 Line Refresh

* Through 1KΩ resistor.

BURST REFRESH TIMING



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The timing shown assumes that burst mode applications may power-down the Am2964B with the RAM. Therefore the counter is cleared prior to executing the refresh sequence.

APPLICATION

Architecture

The Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation and $\overline{RAS}/\overline{CAS}$ control for the MOS dynamic RAM memories of any data width. The eight bit address path is designed for 64K RAMs and can be used with 16K RAMs.

Sixteen address input latches and two $\overline{RAS}$ Select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal $\overline{RAS}$ decoder to select from one-of-four banks of RAMs.

Speed With Minimum Skew

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, $\overline{RAS}$ and $\overline{CAS}$ paths is minimized (and specified) by placing these function on the same chip. The inclusion of the $\overline{CAS}$ buffer allows matching of its propagation delay, plus provides the $\overline{CAS}$ inhibit function during $\overline{RAS}$ – only refresh.

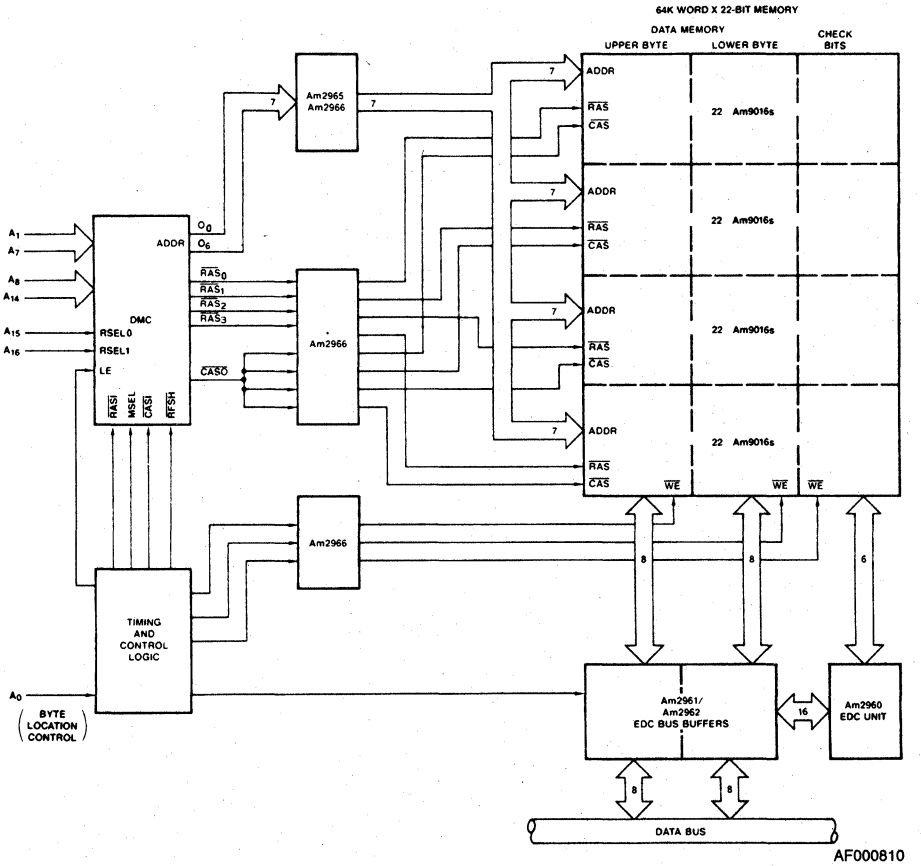
Input Latches

The eighteen input latches are transparent when LE is HIGH and latch the input data meeting set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counter

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of $\overline{RFSH}$ (or $\overline{RASI}$). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by $\overline{CLR}$. This actually causes all outputs to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting).



Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

Figure 1. Dynamic Memory Control with Error Detection and Correction

Refresh Terminal Count

The refresh counter also provides a Terminal Count output for burst mode refresh applications. $\overline{TC}$ normally occurs at count 255 (0_0 to 0_7 all LOW when $\overline{RFSH}$ is LOW). $\overline{TC}$ can be made to occur at count 127 for 128 line burst mode refresh by pulling A_{15} up to +12V through a 1KΩ±10% resistor. The counter actually cycles through 256 with $\overline{TC}$ determined by A_{15}. Otherwise, A_{15} functions as an address input when driven at normal TTL levels.

Three Input 8-Bit Address Multiplexer

The address MUX is 8-bits wide (for 64K RAMs) and has three data sources: the lower address input latch (A_0 to A_7), the upper address input latch (A_8 to A_{15}) and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source, the refresh counter, is selected when $\overline{RFSH}$ is LOW and overrides MSEL.

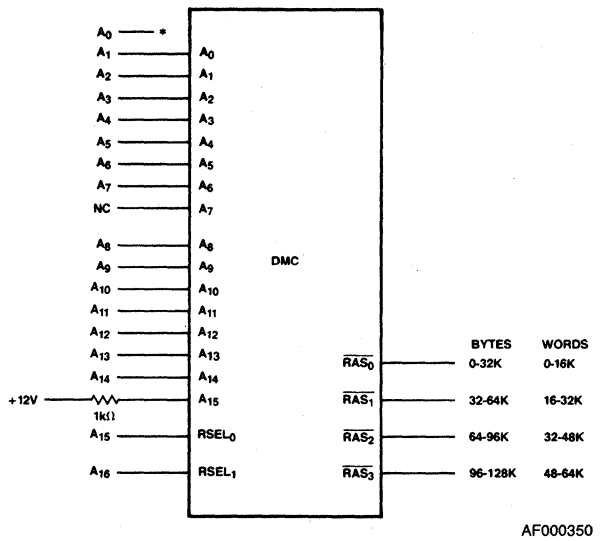
When $\overline{RFSH}$ goes LOW, the MUX selects the refresh counter address and $\overline{CASO}$ is inhibited. Also, the $\overline{RAS}$ Decoder function is changed from one-of-four to four-of-four so all $\overline{RAS}$ outputs $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW to refresh all banks of memory when $\overline{RASI}$ goes LOW. When RFSH is HIGH only one $\overline{RAS}$ output goes low. This is determined by the $\overline{RAS}$ Select inputs, $RSEL_0$ and $RSEL_1$. In either case the $\overline{RAS}$ Decoder output timing is controlled by $\overline{RASI}$ to make sure the refresh count appears at 0_0-0_7 before $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW. This assures meeting Row address Set-up time requirement of the RAM (t_{ASR}).

Maximum Performance System

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 1. Delay lines provide the most accurate timing and are recommended for $\overline{RAS}$/MSEL/$\overline{CAS}$ timing in this type of system.

Controlling 16K RAMs or Smaller Systems

16K RAMs require seven address inputs and 128 line refresh. Also, A_0 is often used to designate upper or lower byte transactions in 16-bit systems. These modifications are shown in Figure 2.



*A_0 Controls Byte Select Logic

Figure 2. Word Organized Memory Using 16K RAMs

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State..... −0.5V to V_{CC} Max
DC Input Voltage..... −0.5V to +5.5V
Output Current, Into Outputs 20mA
DC Input Current..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −1mA	$\overline{TC}$	2.5			Volts
			Others	3.0			Volts
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −15mA	All outputs except $\overline{TC}$	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	All outputs except $\overline{TC}$, I_{OL} = 16mA			0.5	Volts
			$\overline{TC}$, I_{OL} = 8mA			0.5	Volts
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{RAS}$I			−3.2	mA
			$\overline{CAS}$I, MSEL, $\overline{RFSH}$			−1.6	mA
			A_0 −A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{RAS}$I			100	μA
			$\overline{CAS}$I, MSEL, $\overline{RFSH}$			50	μA
			A_0-A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{RAS}$I			2.0	mA
			$\overline{CAS}$I, MSEL, $\overline{RFSH}$			1.0	mA
		V_{CC} = MAX, V_{IN} = 5.5V	A_0-A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX (Note 3)		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	25°C, 5V			122		mA
		0°C to 70°C	COM'L			173	mA
		70°C					
		−55°C to +125°C	MIL			164	mA
		+125°C				150	mA
I_T	A_{15} Enable Current	A_{15} connected to +12V through 1KΩ±10%				5	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), $\overline{RAS}$I and $\overline{CAS}$I are HIGH and all other inputs are LOW.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range for $C_L = 50pF$

Am2964B (Notes 5, 6)

Parameter		Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
					Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	C_L = 50pF	14		19		23	ns
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)		14		20		23	ns
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)		14		20		23	ns
4	t_{PD}	MSEL to O_i		17	9		9		ns
5	t_{PD}	MSEL to O_i		17		21		25	ns
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)		12		17		19	ns
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)		15		20		24	ns
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)		30		40		50	ns
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)		25		35		40	ns
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)		10	50		50		ns
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)		10	50		50		ns
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)		17		21		25	ns
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)		19		26		29	ns
14	t_{PW}	$\overline{CLR}$ = L		10	30		35		ns
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)		16		21		25	ns
16	t_{PD}	LE to O_i		25		35		40	ns
17	t_{PHL}	LE to $\overline{RAS_i}$		30		40		45	ns
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$		35		45		56	ns
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)		31		44		54	ns
20	t_S	A_i to LE Set-Up Time		0	5		5		ns
21	t_H	A_i to LE Hold Time		5	12		15		ns
22	t_S	$RSEL_i$ to LE Set-Up Time		0	5		5		ns
23	t_H	$RSEL_i$ to LE Hold Time		10	17		25		ns
24	t_S	$\overline{CLR}$ Recovery Time		10	16		18		ns
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)		2		5		6	ns
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)		6		8		8	ns
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)		6		8		10	ns
28	t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = ⌐, Note 10)		1		5		5	ns

Notes:
5. Minimum spec limits for t_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.
6. All AC parameters are specified at the 1.5V level.
7. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
8. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
9. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
10. O_i to $\overline{RAS_i}$ (MSEL = ⌐) skew is guaranteed maximum difference between fastest MSEL ⌐ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

03527B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range for $C_L = 50pF$

Am2964B (Notes 5, 6)

Parameter		Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
					Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	C_L = 150pF	20		25		30	ns
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)		18		24		27	ns
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)		18		24		27	ns
4	t_{PD}	MSEL to O_i		23	12		12		ns
5	t_{PD}	MSEL to O_i		23		27		31	ns
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)		17		24		26	ns
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)		19		27		30	ns
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)		34		45		55	ns
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)		32		45		55	ns
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)		10	50		50		ns
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)		10	50		50		ns
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)		21		27		30	ns
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)		25		33		36	ns
14	t_{PW}	$\overline{CLR}$ = L		10	30		35		ns
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)		21		27		31	ns
16	t_{PD}	LE to O_i		30		40		50	ns
17	t_{PHL}	LE to $\overline{RAS_i}$		34		45		54	ns
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$		39		55		60	ns
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)		38		50		62	ns
20	t_S	A_i to LE Set-Up Time		0	5		5		ns
21	t_H	A_i to LE Hold Time		5	12		12		ns
22	t_S	$RSEL_i$ to LE Set-Up Time		0	5		5		ns
23	t_H	$RSEL_i$ to LE Hold Time		10	17		25		ns
24	t_S	$\overline{CLR}$ Recovery Time		10	16		18		ns
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)		3		6		7	ns
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)		6		8		8	ns
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)		6		9		10	ns
28	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{MSEL}$ = ⌐, Note 10)		1		5		5	ns

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

SWITCHING CHARACTERISTICS over operating range for $C_L = 50pF$

Am2964C (Notes 5,6)

Parameter		Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
					Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	C_L = 50pF						ns
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)							ns
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)							ns
4	t_{PD}	MSEL to O_i							ns
5	t_{PD}	MSEL to O_i							ns
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)							ns
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)							ns
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)							ns
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)							ns
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)							ns
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)							ns
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)							ns
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)							ns
14	t_{PW}	$\overline{CLR}$ = L							ns
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)							ns
16	t_{PD}	LE to O_i							ns
17	t_{PHL}	LE to $\overline{RAS_i}$							ns
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$							ns
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)							ns
20	t_S	A_i to LE Set-Up Time							ns
21	t_H	A_i to LE Hold Time							ns
22	t_S	$RSEL_i$ to LE Set-Up Time							ns
23	t_H	$RSEL_i$ to LE Hold Time							ns
24	t_S	$\overline{CLR}$ Recovery Time							ns
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)							ns
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)							ns
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)							ns
28	t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = ⌝⌞, Note 10)							ns

Notes:
5. Minimum spec limits for t_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.
6. All AC parameters are specified at the 1.5V level.
7. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
8. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
9. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
10. O_i to $\overline{RAS_i}$ (MSEL = ⌝⌞) skew is guaranteed maximum difference between fastest MSEL ⌝⌞ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

SWITCHING CHARACTERISTICS over operating range for $C_L = 150pF$

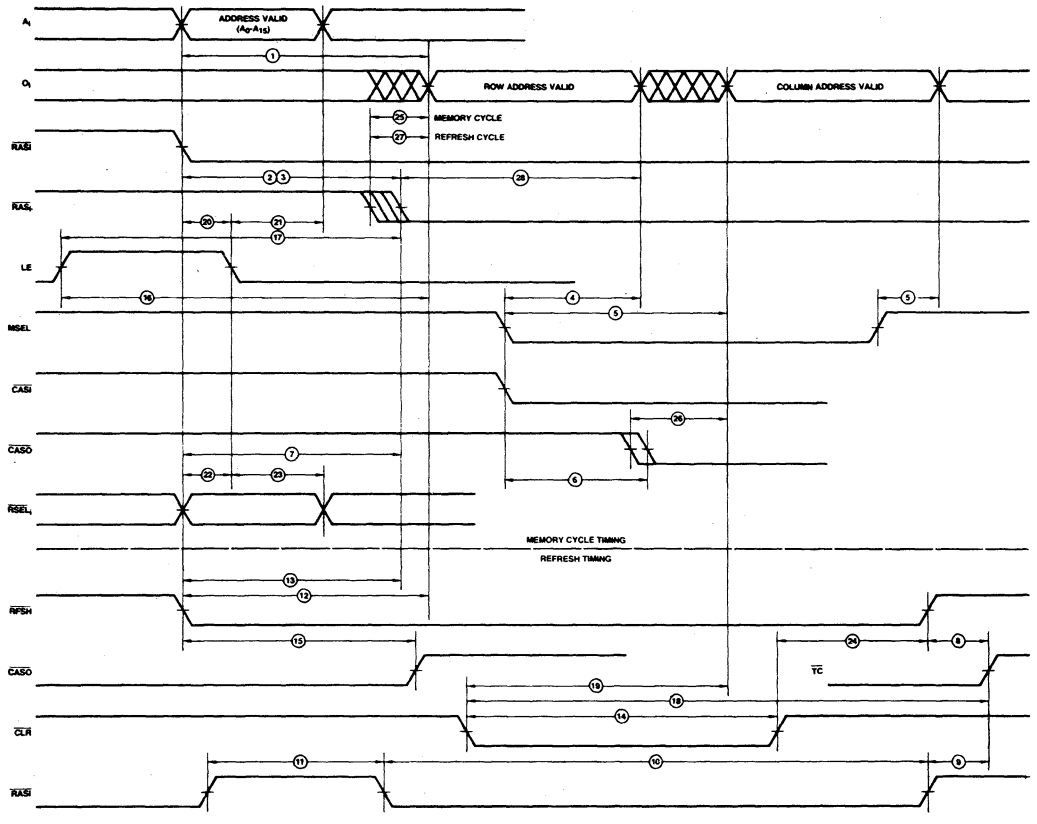
Am2964C (Notes 5,6)

Parameter		Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
					Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	C_L = 150pF						ns
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)							ns
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)							ns
4	t_{PD}	MSEL to O_i							ns
5	t_{PD}	MSEL to O_i							ns
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)							ns
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)							ns
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)							ns
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)							ns
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)							ns
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)							ns
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)							ns
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)							ns
14	t_{PW}	$\overline{CLR}$ = L							ns
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)							ns
16	t_{PD}	LE to O_i							ns
17	t_{PHL}	LE to $\overline{RAS_i}$							ns
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$							ns
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)							ns
20	t_S	A_i to LE Set-Up Time							ns
21	t_H	A_i to LE Hold Time							ns
22	t_S	$RSEL_i$ to LE Set-Up Time							ns
23	t_H	$RSEL_i$ to LE Hold Time							ns
24	t_S	$\overline{CLR}$ Recovery Time							ns
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)							ns
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)							ns
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)							ns
28	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{MSEL}$ = ⌐L, Note 10)							ns

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0.4V$ and $V_{IH} \geqslant 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.



WF001990

Hm2964B Dynamic Memory Controller Timing

Refer to Page 13-1 for Essential Information on Military Devices

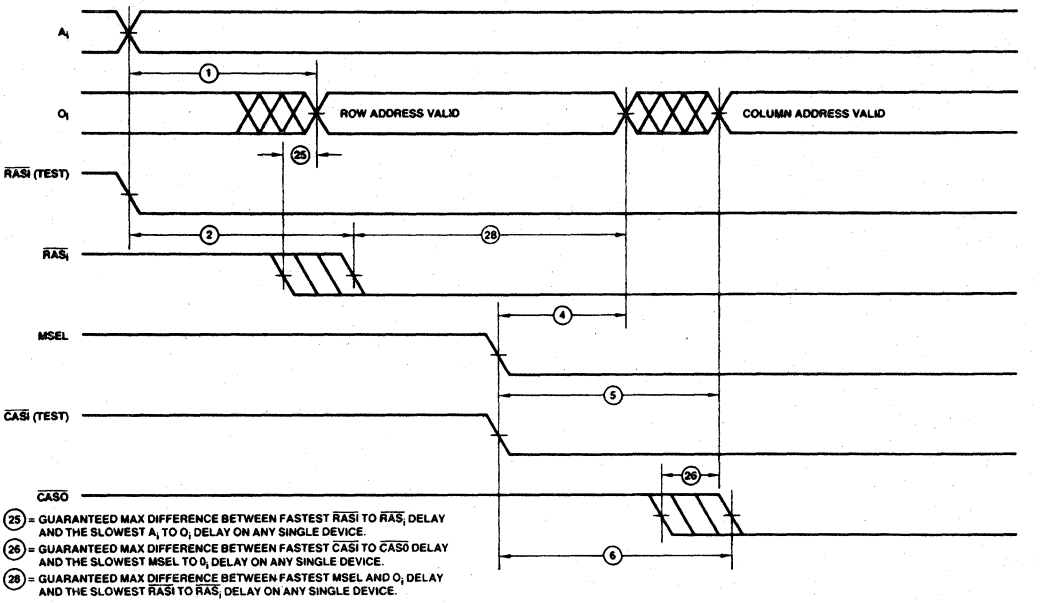
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T_1, T_2 and T_3 are as follows:

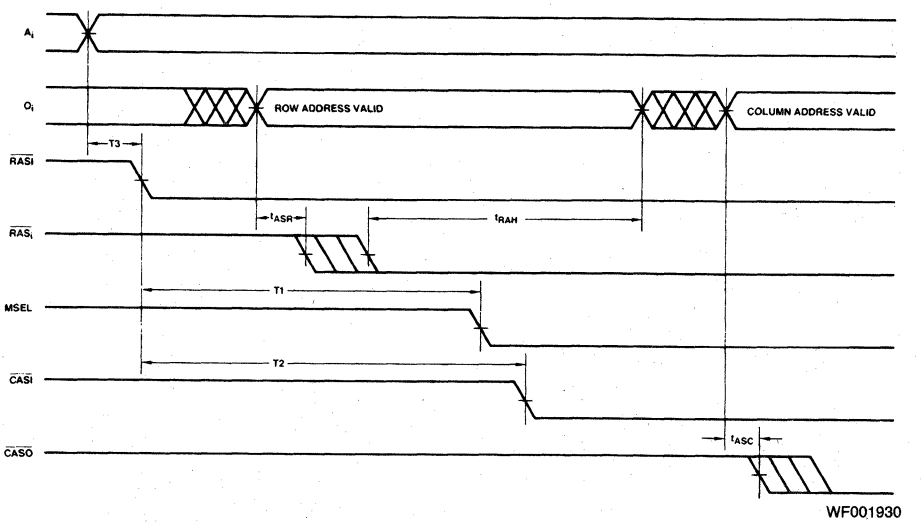
$T_1MIN = t_{RAH} + t_{28}$
$T_2MIN = T_1 + t_{26} + t_{ASC}$
$T_3MIN = t_{ASR} + t_{25}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.



WF001920

a. Specifications Applicable to Memory Cycle Timing



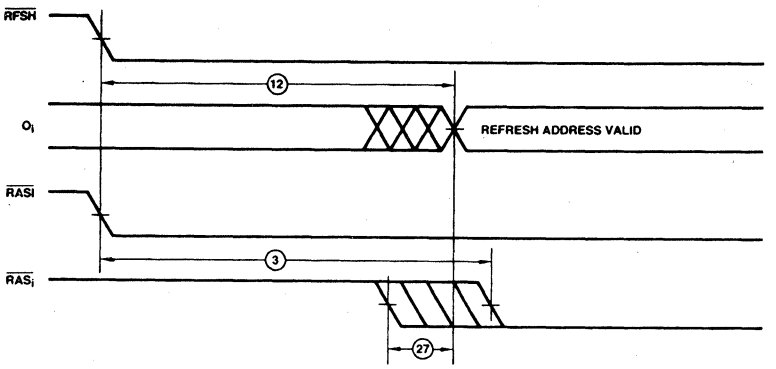
WF001930

b. Desired System Timing

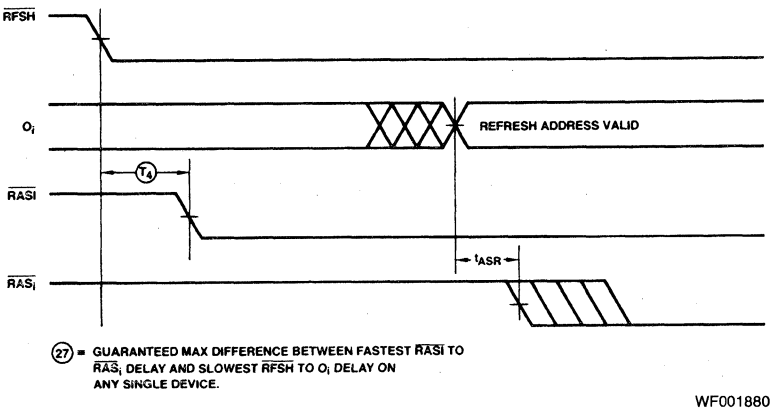
Figure 3. Memory Cycle Timing

REFRESH CYCLE TIMING

The timing relationships for refresh are shown in Figure 4.
T_4 minimum is calculated as follows: $T_4 = t_{ASR} + t_{27}$



a. Test Waveforms



b. Desired System Timing

Figure 4. Refresh Timing

Am2965/Am2966

Octal Dynamic Memory Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  V_{OH} guaranteed at V_{CC} −1.15V. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting Am2966 replaces 74S244; inverting Am2965 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down. No glitch coming out of three-state.

GENERAL DESCRIPTION

The Am2965 and Am2966 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} − 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

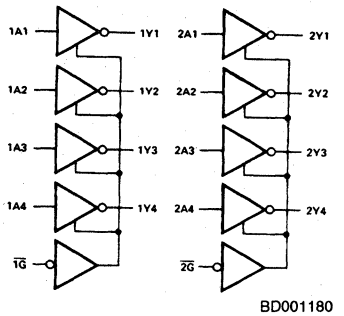
The Am2965 and Am2966 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The Am2965 has inverting drivers and the Am2966 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the Am2964 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

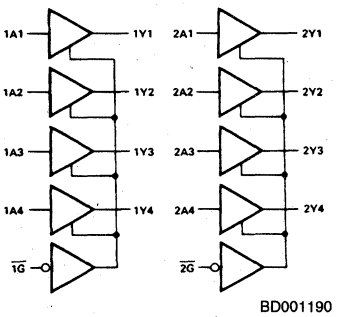
BLOCK DIAGRAM

Am2965



BD001180

Am2966



BD001190

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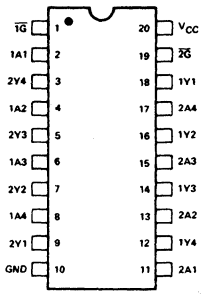
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



CD001440

Note: Pin 1 is marked for orientation

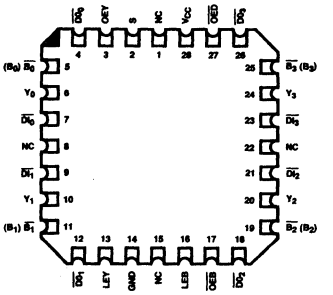
Am2965

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2966

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

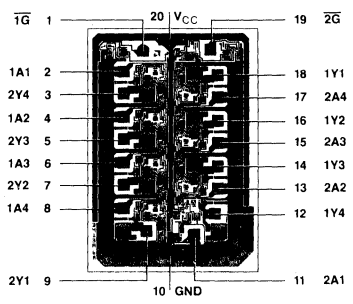
Leadless Chip Carrier



CD004870

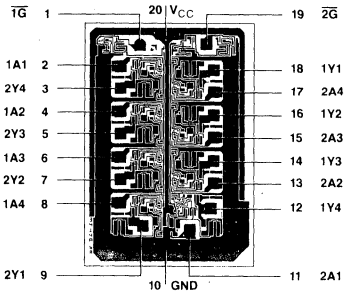
METALLIZATION AND PAD LAYOUT

Am2965



DIE SIZE 0.094" x 0.060"

Am2966



DIE SIZE 0.094" x 0.066"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2965
Am2966

D C B

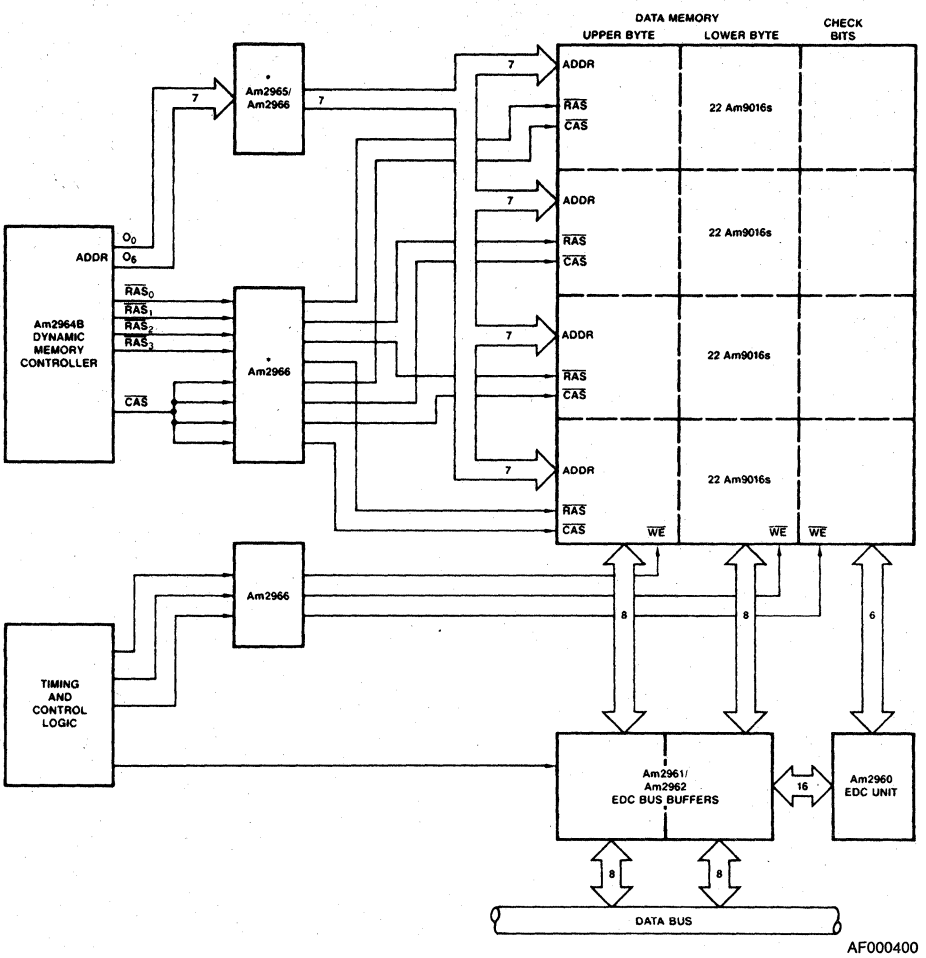
- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 20-pin CERDIP (D-20-1)
  - F – 20-pin flatpak (F-20-1)
  - L – 20-pin leadless chip carrier (L-20-1)
  - P – 20-pin plastic DIP (P-20-1)
  - X – Dice
- Device type
  - Octal Dynamic Memory Drivers with Three-state Outputs

Valid Combinations	
Am2965 Am2966	PC DC, DCB, DM, DMB FM, FMB LC, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

APPLICATION



*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient)
Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} Max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 200mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Descriptions		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	V_{CC} −1.15	V_{CC} −0.7V		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
				I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V	DATA			−200	μA
				$\overline{1G}$, $\overline{2G}$			−400	
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current		V_O = 2.7V				100	μA
I_{OZL}	Off-State Current		V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current		V_{OL} = 2.0V		50			mA
I_{OH}	Output Source Current		V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−60 (see I_{OH}		−200	mA
I_{CC}	Supply Current	Am2965	All Outputs HIGH	V_{CC} = MAX Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		Am2966	All Outputs HIGH	V_{CC} = MAX Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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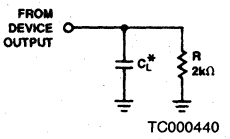
Refer to Page 13-1 for Essential Information on Military Devices

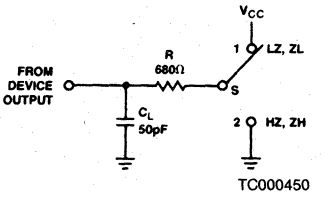
SWITCHING TEST CIRCUIT



TC000440

*t_{pd} specified at C = 50 and 500pF.

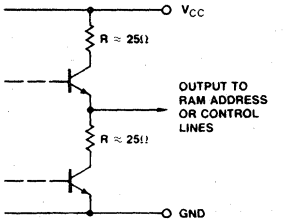
Figure 1. Capacitive Load Switching.



TC000450

Figure 2. Three-State Enable/Disable.

TYPICAL OUTPUT DRIVER



TC000520

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	18	22	30	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	5	7	15	
			C_L = 500pF	18	22	30	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			11	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			6.5	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			12	20	ns
t_{PZH}		Figures 2 and 4, S = 2			12	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 6)

Parameters	Description	Test Conditions		COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

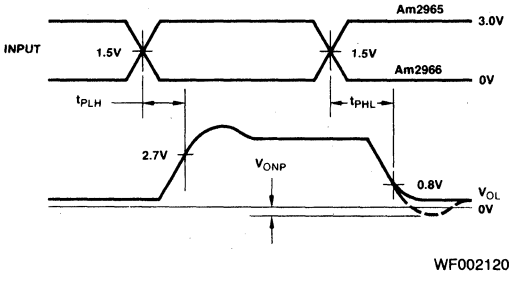
Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
7. T_C = −55 to +125°C for Flatpak versions.

05409A

Refer to Page 13-1 for Essential Information on Military Devices

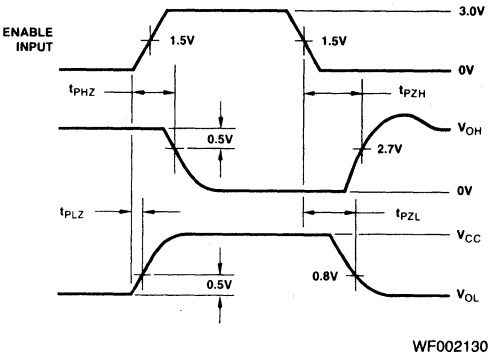
TYPICAL SWITCHING CHARACTERISTICS

VOLTAGE WAVEFORMS



$t_r = t_f = 2.5ns$
f = 2.5MHz
$t_{pw} = 200ns$

Figure 3. Output Drive Levels.



$t_r = t_f = 2.5ns$
f = 1MHz
$t_{pw} = 800ns$

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} – 1.5V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach, because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (Am2965) and non-inverting (Am2966) RAM Drivers.

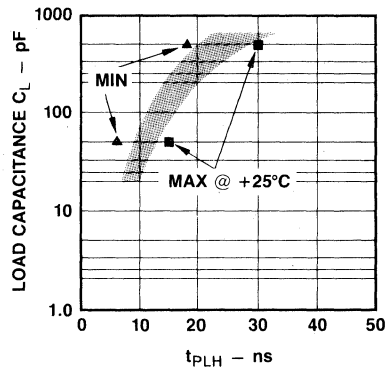


Figure 5. t_{PLH} for V_{OH} = 2.7 Vol vs. C_L.

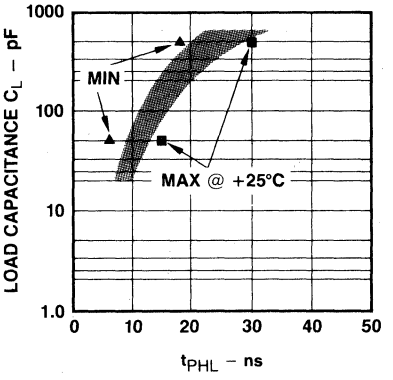


Figure 6. t_{PHL} for V_{OL} = 0.8 Volts vs. C_L.

The curves above depict the typical tPLH and tPHL for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

Am2968

Dynamic Memory Controller (DMC)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

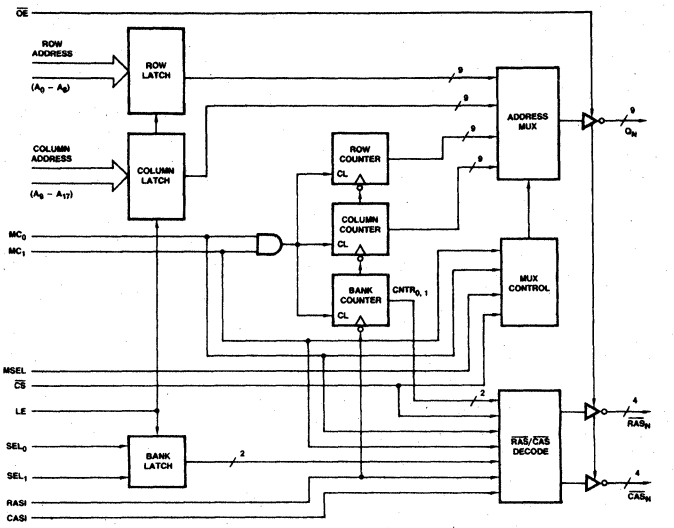
- Provides control for 16K, 64K, and 256K dynamic RAMs
- Outputs directly drive up to 88 DRAMs, with a guaranteed worst-case limit on the undershoot
- Highest-order two address bits select one of four banks of RAMs
- Separate output enable for multi-channel access to memory
- Supports scrubbing operations and nibble-mode access
- 48-pin dual in-line package

GENERAL DESCRIPTION

The Am2968 Dynamic Memory Controller (DMC) is intended to be used with today's high performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array, using its two 9-bit address latches to hold the Row and Column addresses for any DRAM up to 256K. These latches, and the two Row/Column refresh address counters, feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch for the two high-order address bits is provided to select one each of the four $\overline{RAS}_i$ and $\overline{CAS}_i$ outputs.

The Am2968 has two basic modes of operation, read/write and refresh. In refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the Row Counter is used, generating up to 512 addresses to refresh a 512-cycle-refresh 256K DRAM. When memory scrubbing is being performed, both the Row and Column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}_i$ outputs will be active while only one $\overline{CAS}_i$ is active at a time.

BLOCK DIAGRAM



BD001900

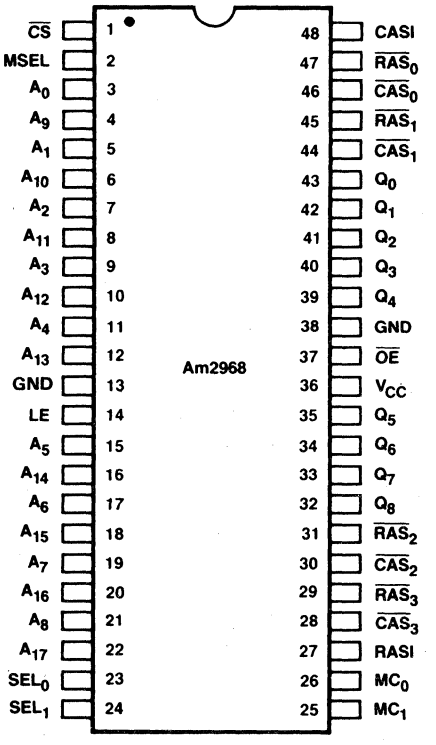
RELATED PRODUCTS

Part No.	Description
Am2960	16-Bit Error Detection and Correction Unit
Am2969 Am2970	Memory Timing Controllers

04564B

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



CD005050

CHIP PAK™
L-52-1

CD004182

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2968 **D** **C** **B**

- B: Screening Option — B – Burn-in; Blank – Standard processing
- C: Commercial (C) Devices; Military (M) Devices
- D: Package — D– 48-pin Hermetic DIP; P– 48-pin plastic DIP
- Am2968: Device Type — DMC

Valid Combinations	
Am2968	PC, PCB DC, DCB DMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CHIP PAK is a registered trademark of Advanced Micro Devices, Inc.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3 – 12 15 – 22	$A_0 - A_{17}$	I	Address Inputs. $A_0 - A_8$ are latched in as the nine-bit Row Address for the RAM. These inputs drive $Q_0 - Q_8$ when the Am2968 is in the Read/Write mode and MSEL is LOW. $A_9 - A_{17}$ are latched in as the Column Address, and will drive $Q_0 - Q_8$ when MSEL is HIGH and the DMC is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.
23, 24	SEL_0, SEL_1	I	Bank Select. These two inputs are normally the two higher-order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{RAS}_i$ and $\overline{CAS}_i$ signals after RASI and CASI go HIGH.
14	LE	I	Latch Enable. This active-HIGH input causes the Row, Column, and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.
2	MSEL	I	Multiplexer Select. This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on $MC_{0,1}$.
1	$\overline{CS}$	I	Chip Select. This active-LOW input is used to enable the DMC. When $\overline{CS}$ is active, the Am2968 operates normally in all four modes. When $\overline{CS}$ goes HIGH, the device will not enter the Read/Write mode. This allows other devices to access the same memory that the DMC is controlling (e.g., DMA controller).
37	$\overline{OE}$	I	Output Enable. This active-LOW input enables/disables the output signals. When $\overline{OE}$ is HIGH, the outputs of the DMC enter the high-impedance state. The $\overline{OE}$ signal allows more than one Am2968 to control the same memory, thus providing an easy method to expand the memory size.
26, 25	MC_0, MC_1	I	Mode Control. These inputs are used to specify which of the four operating modes the DMC should be using. The description of the four operating modes is given in Table 1.
43 – 39 32 – 35	$Q_0 - Q_8$	O	Address Outputs. These address outputs will feed the DRAM address inputs, and provide drive for memory systems up to 500 picofarads in capacitance.
27	RASI	I	Row Address Strobe Input. During normal memory cycles, the decoded $\overline{RAS}_i$ output ($\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$, or $\overline{RAS}_3$) is forced LOW after receipt of RASI. In either Refresh mode, all four $\overline{RAS}_i$ outputs will go LOW following RASI going HIGH.
47, 45, 31, 29	$\overline{RAS}_0 - \overline{RAS}_3$	O	Row Address Strobe. Each one of the Row Address Strobe outputs provides a $\overline{RAS}_i$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL_0 and SEL_1 and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.
48	CASI	I	Column Address Strobe Input. This input going active will cause the selected $\overline{CAS}_i$ output to be forced LOW.
46, 44, 30, 28	$\overline{CAS}_0 - \overline{CAS}_3$	O	Column Address Strobe. During normal Read/Write cycles the two select bits (SEL_0, SEL_1) determine which $\overline{CAS}_i$ output will go active following CASI going HIGH. When memory scrubbing is performed, only the $\overline{CAS}_i$ signal selected by $CNTR_0$ and $CNTR_1$ will be active. For non-scrubbing cycles, all four $\overline{CAS}_i$ outputs remain HIGH.

Table 1. Mode Control Function Table

MC_1	MC_0	Operating Mode
0	0	Refresh without Scrubbing. Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{RAS}_i$ outputs are active while the four $\overline{CAS}_i$ signals are kept HIGH.
0	1	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{RAS}_i$ go active in response to RASI, while only one $\overline{CAS}_i$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{CAS}_i$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	Read/Write. This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL. SEL_0 and SEL_1 are decoded to determine which $\overline{RAS}_i$ and $\overline{CAS}_i$ will be active.
1	1	Clear Refresh Counter. This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS}_i$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

ADDRESS OUTPUT FUNCTION TABLE

$\overline{CS}$	MC_1	MC_0	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
	1	1	X	Clear Refresh Counter	Zero
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

$\overline{RAS}$ OUTPUT FUNCTION TABLE

RASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	Mode	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
0	X	X	X	X	X	X	1	1	1	1
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1	X	X	Refresh with Scrubbing	0	0	0	0
		1	0	0	0	Read/Write	0	1	1	1
				0	1		1	0	1	1
				1	0		1	1	0	1
				1	1		1	1	1	0
		1	1	X	X	Clear Refresh Counter	0	0	0	0
	1	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1			Refresh with Scrubbing	0	0	0	0
		1	0			Read/Write	1	1	1	1
		1	1			Clear Refresh Counter	0	0	0	0

$\overline{CAS}$ OUTPUT FUNCTION TABLE

Inputs						Internal		Outputs			
CASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	$CNTR_1$	$CNTR_0$	$\overline{CAS}_0$	$\overline{CAS}_1$	$\overline{CAS}_2$	$\overline{CAS}_3$
1	0	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	0	0	X	X	0	1	1	1
				0	1			1	0	1	1
				1	0			1	1	0	1
				1	1			1	1	1	0
		1	1	X	X	X	X	1	1	1	1
	1	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	X	X	X	X	1	1	1	1
		1	1								
0	X	X	X	X	X	X	X	1	1	1	1

APPLICATION

ARCHITECTURE

The Am2968 provides all the required data and refresh addresses needed by the dynamic RAM memory. In normal operation, the Row and Column addresses are multiplexed to the dynamic RAM by using MSEL, with the corresponding $\overline{RAS}_i$ and $\overline{CAS}_i$ signals activated to strobe the addresses into the RAM. High capacitance drivers on the outputs allow the DMC to drive four banks of 16-bit words, including a 6-bit checkword, for a total of 88 DRAMs.

INPUT LATCHES

For those systems where addresses and data are multiplexed onto a single bus, the DMC has latches to hold the address information. The twenty input latches (Row, Column, and Bank Select) are transparent when Latch Enable (LE) is HIGH and will latch the input data meeting setup and hold time requirements when LE goes LOW. For systems where the processor has separate address and data buses, LE may be permanently enabled HIGH.

REFRESH COUNTERS

The two 9-bit refresh counters make it possible to support 128, 256, and 512 line refresh. External control over what type of refresh is to be performed allows the user maximum flexibility when choosing the refreshing scheme. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

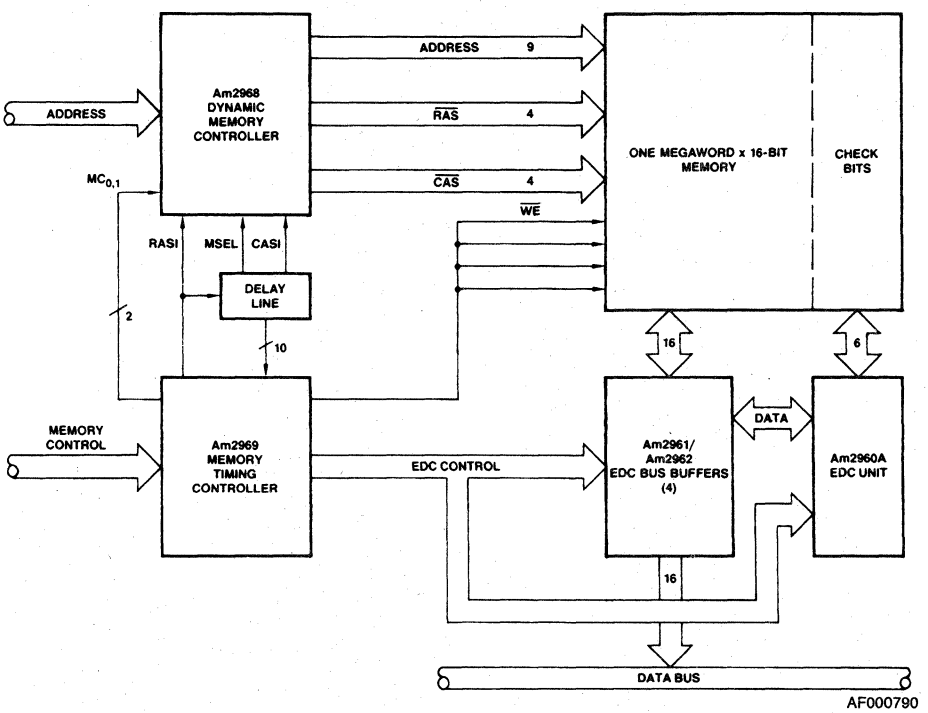
The refresh counters are advanced at the HIGH-to-LOW transition of RASI. This assures a stable counter output for the next refresh cycle.

REFRESH WITH ERROR CORRECTION

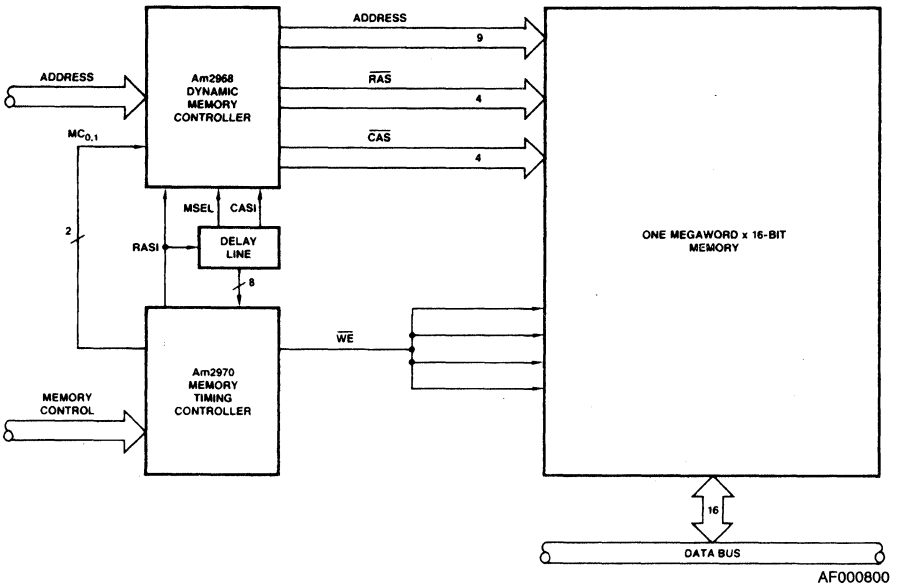
The Am2968 makes it possible to correct single-bit errors in parallel with performing dynamic RAM refresh cycles. This "scrubbing" of memory can be done periodically as a background routine when the memory is not being used by the processor. In a memory scrubbing cycle ($MC_{1,0} = 01$), the Row Address is strobed into all four banks with all four $\overline{RAS}_i$ outputs going LOW.

The Column Address is strobed into a single bank with the activated $\overline{CAS}_i$ output being selected by the Bank Counter. This type of cycle is used to simultaneously refresh the addressed row in all banks and read and correct (if necessary) one word in memory; thereby reducing the overhead associated with Error Detection and Correction. When doing refresh with memory scrubbing, both the Row and Column counters are multiplexed to the dynamic RAM address lines by using MSEL. Using the Refresh with Memory Scrubbing mode implies the presence of an error correcting facility such as the Am2960A EDC unit. When doing refresh without scrubbing, all four $\overline{RAS}_i$ still go LOW but the $\overline{CAS}_i$ outputs are all driven HIGH so as not to activate the output lines of the memory.

Figure 1.
a. One Megaword Dynamic Memory with Error Detection and Correction



b. One Megaword Dynamic Memory



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TIMING CONTROL

To obtain optimum performance and maximum design flexibility, the timing and control logic for the memory system has been kept a separate function. For systems implementing Error Detection and Correction, the Am2969 Memory Timing Controller (MTC) provides all the necessary control signals for the Am2968, Am2961/62 EDC Bus Buffers, and the Am2960A EDC unit (See Figure 1a). Systems not using EDC, can use the Am2970 MTC to provide the control for the Am2968 (See Figure 1b). Both the Am2969 and Am2970 Memory Timing Controllers use a delay line to provide the most accurate timing reference from which the control signals are derived.

DECOUPLING

Due to the high switching speeds and high drive capability of the Am2968, it is necessary to decouple the device for proper operation. (See Fig. 2a) Recommended values for decoupling capacitors are between 0.01μF and 1μF. For example to filter noise at different frequencies we can make C_1 = 0.01μF in parallel with a 1μF and C_2 = 0.01μF. It is important to mount the capacitors as close as possible to the power pins (V_{CC}, GND) to minimize lead inductance and noise.

MEMORY EXPANSION

With a 9-bit address path, the Am2968 can control up to one megaword memory when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to double the memory size by using two Am2968s. Memory can be increased in one megaword increments by adding another DMC unit. A four-megaword memory system implementing EDC is shown in Figure 3.

V_{ONP}

The guaranteed maximum undershoot voltage of the Am2968 is −0.5 volts. V_{ONP} is measured with respect to the ground of pin 38 (Fig. 2b). Note that the ground of the capacitive load must be the same as for pin 38.

Figure 2.

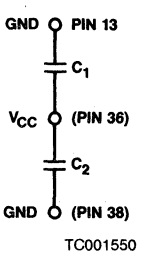


Figure 2a.

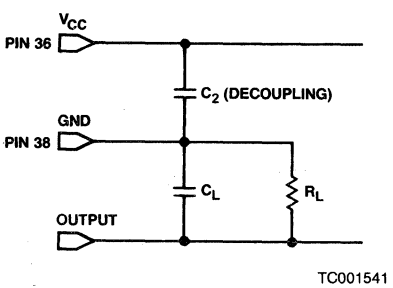


Figure 2b.

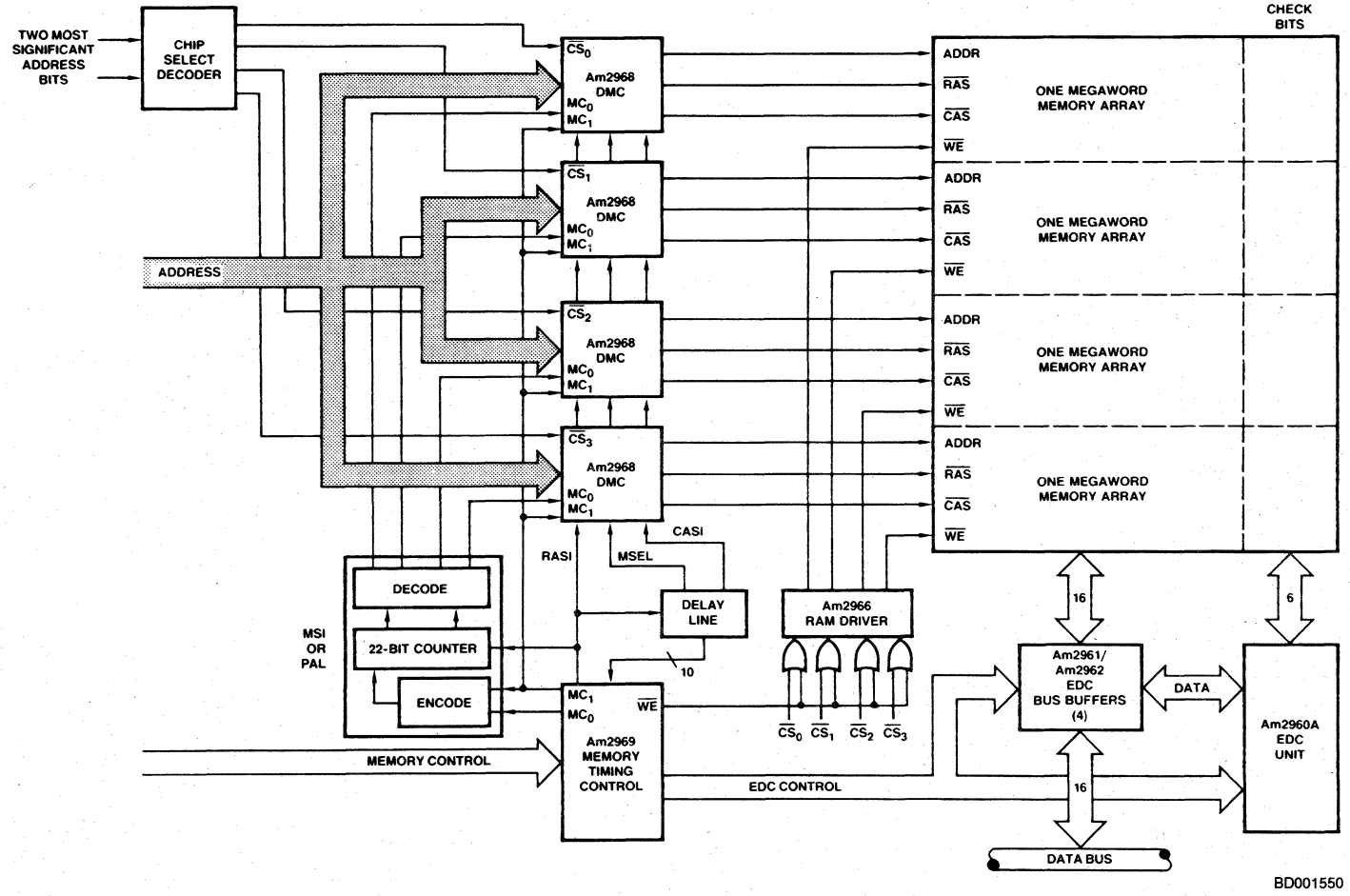


Figure 3. Four Megaword Error Correcting Memory

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
T_A ..... 0 to +70°C
V_{CC} ..... 5.0V ± 10%
Min 4.50V
Max 5.50V

Military (M) Devices
T_C ..... −55 to +125°C
V_{CC} ..... 5.0V ± 10%
Min 4.50V
Max 5.50V

Operating ranges define those limits over which the functionality of the device is guaranteed.

4

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −1mA	COMM	2.7			Volts
			MIL	2.5			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
			I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−400	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				100	μA
I_{OZH}	Off-State Current	V_O = 2.4V				50	μA
I_{OZL}	Off-State Current	V_O = 0.4V				−50	μA
I_{OL}	Output Sink Current	V_{OL} = 2.0V		45			mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX (Note 2)		−60	−95	−275	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	25°C, 5V		230		
			0°C to 70°C			280	
			+70°C		200	260	
			−55°C to 125°C			295	
			+125°C		195	255	

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under Operating Range for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

04564B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range for C_L = 50pF

Parameter		Description	Test Conditions		Typ	COMMERCIAL AND MILITARY Min	COMMERCIAL AND MILITARY Max	Units
1	t_{PD}	A_i to Q_i Delay	Fig. 4 and 6 C_L = 50pF		12	3	20	ns
2	t_{PD}	RASI to $\overline{RAS}_i$			10	3	18	ns
3	t_{PD}	CASI to $\overline{CAS}_i$			8	3	17	ns
4	t_{PD}	MSEL to Q_i			12	3	20	ns
5	t_{PD}	MC_i to Q_i			15	5	24	ns
6	t_{PD}	LE to $\overline{RAS}_i$			15		25	ns
7	t_{PD}	LE to $\overline{CAS}_i$			14		24	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$			14	3	21	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$			12	3	19	ns
10	t_{PD}	LE to Q_i			15	5	25	ns
11	t_{PWL}	RASI, CASI	C_L = 50pF		10	20		ns
12	t_{PWH}	RASI, CASI			10	20		ns
13	t_S	A_i to LE			1	5		ns
14	t_H	A_i to LE			1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i			16		23	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$			12		20	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$			11		19	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$			12		20	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$			11		18	ns
20	t_S	SEL_i to LE			1	5		ns
21	t_H	SEL_i to LE			1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)			10		17	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)			10		17	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$			2		10	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$			12		17	ns
	t_{PLZ}	Output Disable Time From LOW, HIGH	Fig. 5 and 7	S = 1	15		22	ns
	t_{PHZ}			S = 2	13		20	ns
	t_{PZL}	Output Enable Time From LOW, HIGH	Fig. 5 and 7	S = 1	13		19	ns
	t_{PZH}			S = 2	14		21	ns
	V_{ONP}	Output Undershoot Voltage	Fig. 4 and 6		0		−0.5	V

04564B

Refer to Page 13-1 for Essential Information on Military Devices

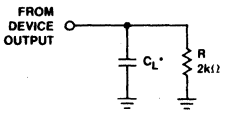
SWITCHING CHARACTERISTICS over operating range for C_L = 150pF

Parameter		Description	Test Conditions	Typ	COMMERCIAL AND MILITARY		Units
					Min	Max	
1	t_{PD}	A_i to Q_i Delay	Fig. 4 and 6 C_L = 150pF	16	9	24	ns
2	t_{PD}	RASI to $\overline{RAS}_i$		15	9	23	ns
3	t_{PD}	CASI to $\overline{CAS}_i$		14	9	22	ns
4	t_{PD}	MSEL to Q_i		17	9	26	ns
5	t_{PD}	MC_i to Q_i		18	10	28	ns
6	t_{PD}	LE to $\overline{RAS}_i$		20		28	ns
7	t_{PD}	LE to $\overline{CAS}_i$		19		27	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$		19	9	25	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$		17	9	23	ns
10	t_{PD}	LE to Q_i		20	10	27	ns
11	t_{PWL}	RASI, CASI	C_L = 150pF	10	20		ns
12	t_{PWH}	RASI, CASI		10	20		ns
13	t_S	A_i to LE		1	5		ns
14	t_H	A_i to LE		1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i		19		27	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$		14		22	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$		14		22	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$		15		23	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$		14		22	ns
20	t_S	SEL_i to LE		1	5		ns
21	t_H	SEL_i to LE		1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)		10		15	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)		10		17	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$		2		8	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$		15		17	ns
	V_{ONP}	Output Undershoot Voltage	Fig. 4 and 6	0		−0.5	V

SWITCHING CHARACTERISTICS over operating range for C_L = 500pF

Parameter		Description	Test Conditions	Typ	COMMERCIAL AND MILITARY		Units
					Min	Max	
1	t_{PD}	A_i to Q_i Delay	Fig. 4 and 6 C_L = 500pF	29	12	40	ns
2	t_{PD}	RASI to $\overline{RAS}_i$		28	12	40	ns
3	t_{PD}	CASI to $\overline{CAS}_i$		26	12	37	ns
4	t_{PD}	MSEL to Q_i		29	12	42	ns
5	t_{PD}	MC_i to Q_i		30	12	44	ns
6	t_{PD}	LE to $\overline{RAS}_i$		32		46	ns
7	t_{PD}	LE to $\overline{CAS}_i$		31		45	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$		30	12	40	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$		28	12	40	ns
10	t_{PD}	LE to Q_i		32	12	46	ns
11	t_{PWL}	RASI, CASI	C_L = 500pF	10	20		ns
12	t_{PWH}	RASI, CASI		10	20		ns
13	t_S	A_i to LE		1	5		ns
14	t_H	A_i to LE		1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i		30		45	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$		27		40	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$		26		38	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$		31		42	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$		28		41	ns
20	t_S	SEL_i to LE		1	5		ns
21	t_H	SEL_i to LE		1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)		10		18	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)		10		18	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$		2		8	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$		15		20	ns
	V_{ONP}	Output Undershoot Voltage	Fig. 4 and 6	0		−0.5	V

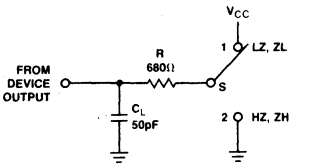
SWITCHING TEST CIRCUIT



TC000490

*t_{pd} specified at C_L = 50, 150 and 500pF

Figure 4. Capacitive Load Switching.

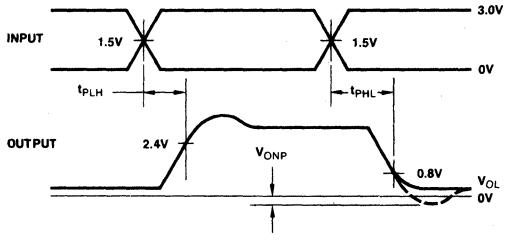


TC000510

Figure 5. Three-State Enable/Disable.

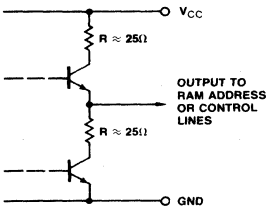
TYPICAL SWITCHING CHARACTERISTICS

VOLTAGE WAVEFORMS



WF002122

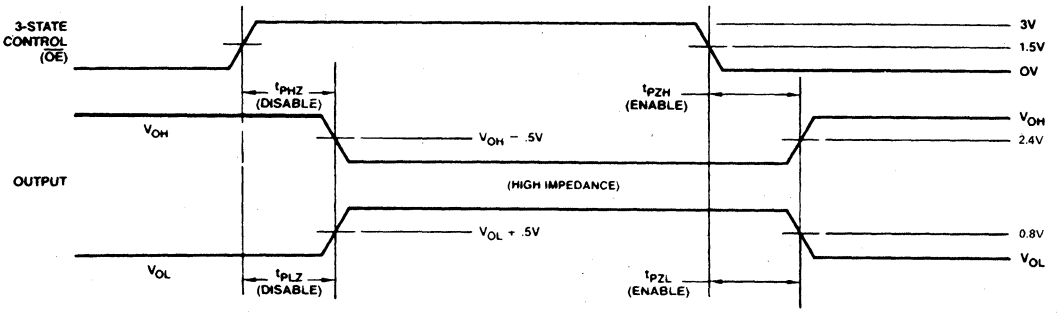
TYPICAL OUTPUT DRIVER



TC000500

Figure 6. Output Drive Levels.

THREE-STATE TIMING



WFR02941

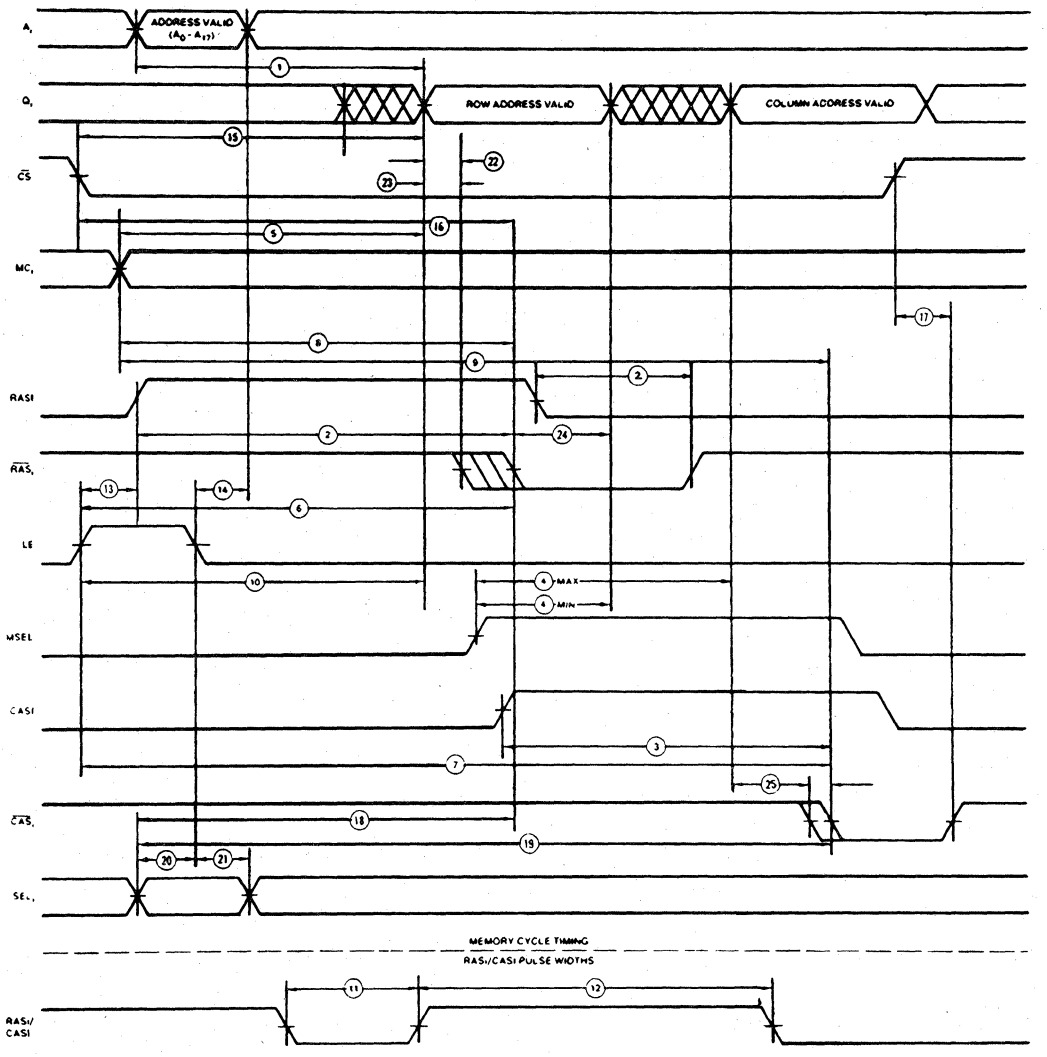
Note: Decoupling is needed for all AC tests

Figure 7. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} – 1.5V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

Am2968 Dynamic Memory Controller Timing



WF003263

04564B

Refer to Page 13-1 for Essential Information on Military Devices

MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 8. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

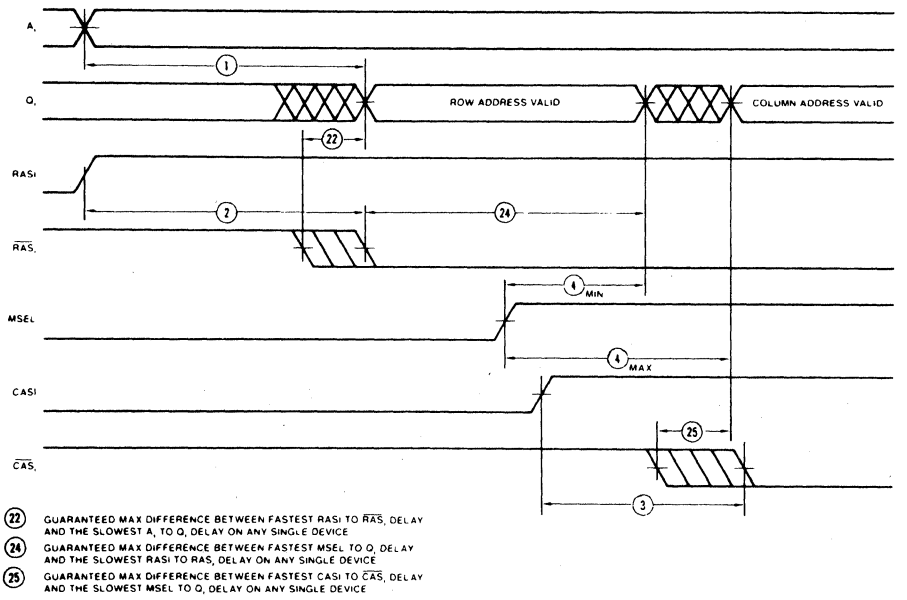
The minimum requirement for T_1, T_2 and T_3 are as follows:

T_1 MIN = $t_{ASR} + t_{22}$
T_2 MIN = $t_{RAH} + t_{24}$
T_3 MIN = $T_2 + t_{25} + t_{ASC}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.

Figure 8. Memory Cycle Timing

a. Specifications Applicable to Memory Cycle Timimg (MC_I = 1, 0)



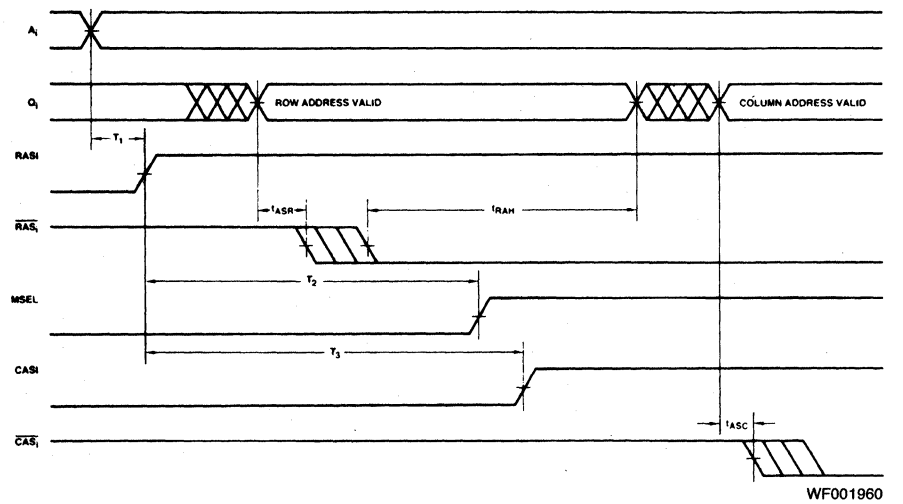
(22) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}$, DELAY AND THE SLOWEST A, TO Q, DELAY ON ANY SINGLE DEVICE

(24) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q, DELAY AND THE SLOWEST RASI TO RAS, DELAY ON ANY SINGLE DEVICE

(25) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO $\overline{CAS}$, DELAY AND THE SLOWEST MSEL TO Q, DELAY ON ANY SINGLE DEVICE

WF003281

b. Desired System Timing



WF001960

REFRESH CYCLE TIMING

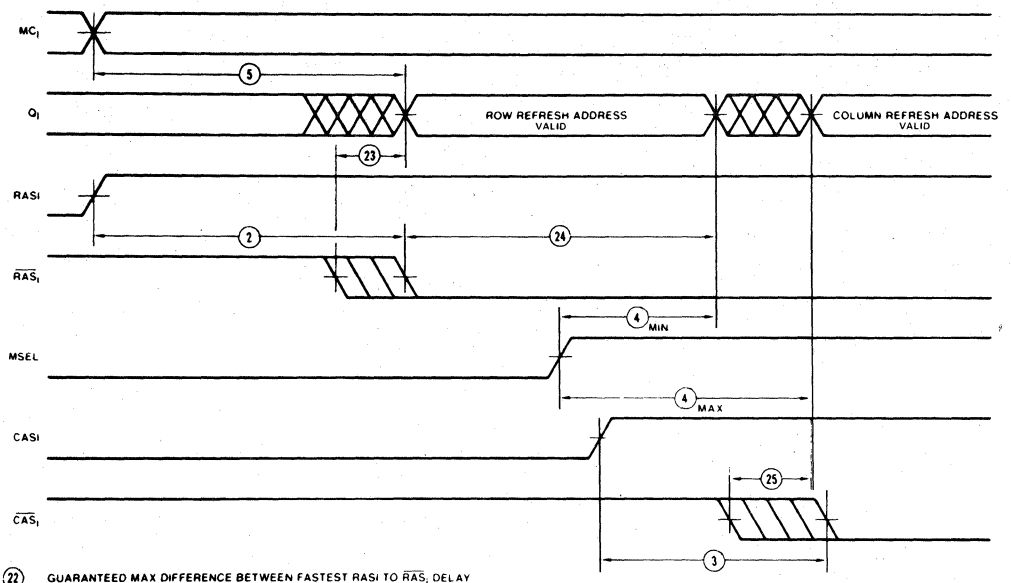
The timing relationships for refresh are shown in Figure 9.

T_4 minimum is calculated as follows:

T_4 MIN = $t_{ASR} + t_{23}$

Figure 9. Refresh Cycle Timing

a. Specifications Applicable to Refresh Cycle Timing (MC_i = 00, 01)



(22) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_i$ DELAY AND THE SLOWEST A_i to Q_i DELAY ON ANY SINGLE DEVICE

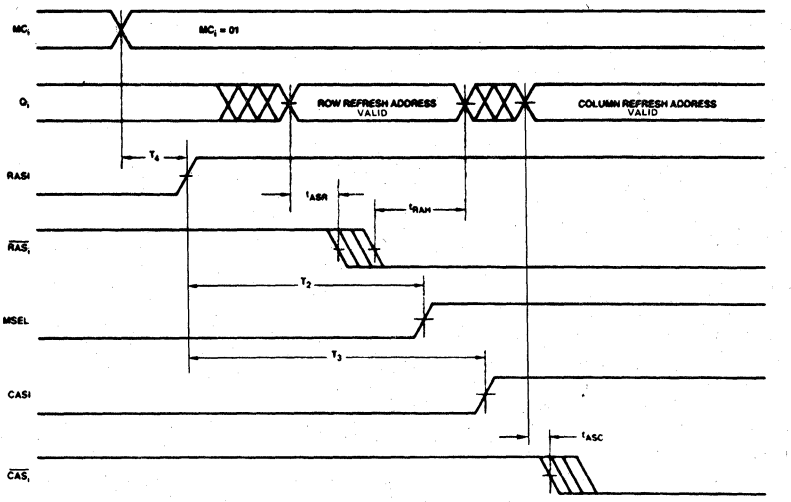
(23) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_i$ DELAY AND THE SLOWEST MC_i TO Q_i DELAY ON ANY SINGLE DEVICE

(24) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q_i DELAY AND THE SLOWEST RASI TO $\overline{RAS}_i$ DELAY ON ANY SINGLE DEVICE

(25) GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO $\overline{CAS}_i$ DELAY AND THE SLOWEST MSEL TO Q_i DELAY ON ANY SINGLE DEVICE

WF003271

b. Desired Timing: Refresh with Scrubbing

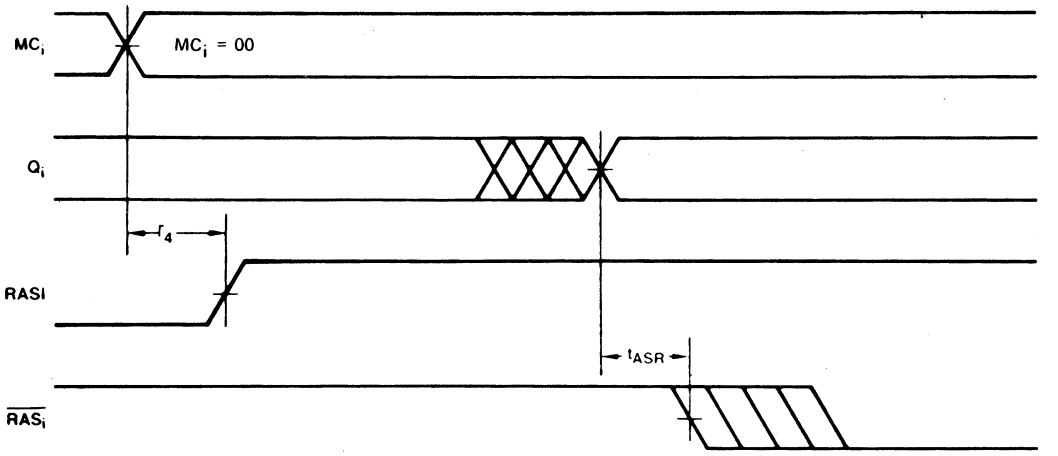


WF001981

REFRESH CYCLE TIMING

Figure 9. Refresh Cycle Timing (Cont.)

c. Desired Timing: Refresh without Scrubbing



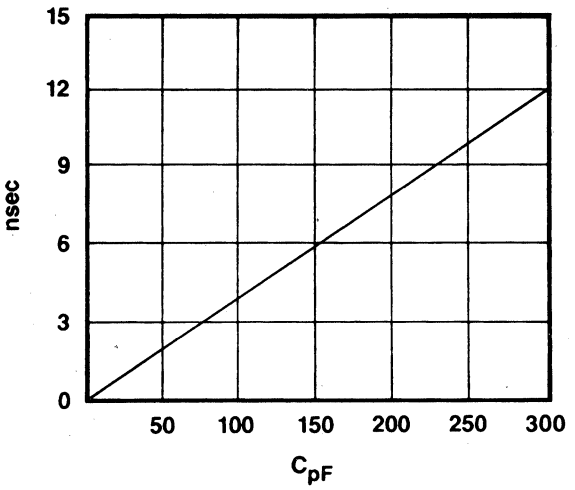
WF003251

NANOSECONDS VERSUS PICOFARADS

To help calculate how the AC performance of the DMC will vary for capacitive loads other than 50, 150, and 500pF refer to the table below.

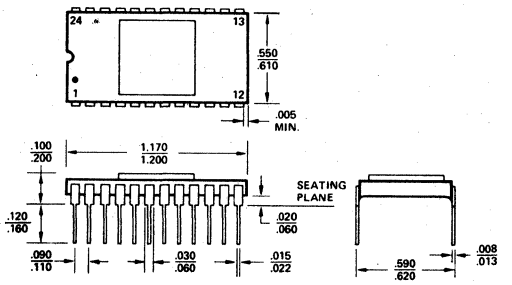
Example: For a system capacitive load of 250pF, add the delay associated with 100pF from the table to the AC specs done at 150pF.

Change in Propagation Delay versus Loading Capacitance (TYPICAL)



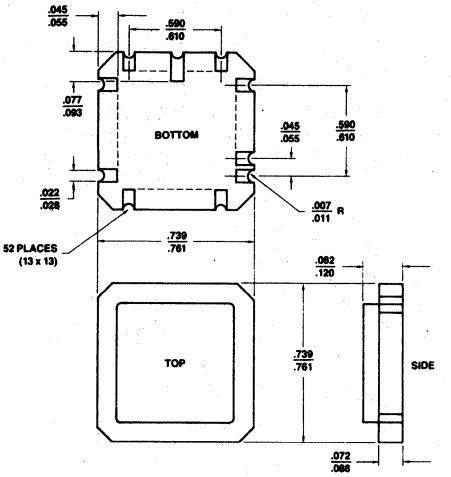
LCR00011

D-24-2



PO000960

L-52-1



PO001150

Am2969

Dynamic Memory Timing Controller

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Provides complete timing control for 64K/256K memory systems which utilize the Am2960, Am2961/62, and Am2968
- Supports byte-writes up to 32-bits wide
- Supports memory scrubbing during refresh
- Burst (up to 512-cycle), distributed, or hidden refresh
- Performs memory initialization
- Memory access/refresh request arbitration

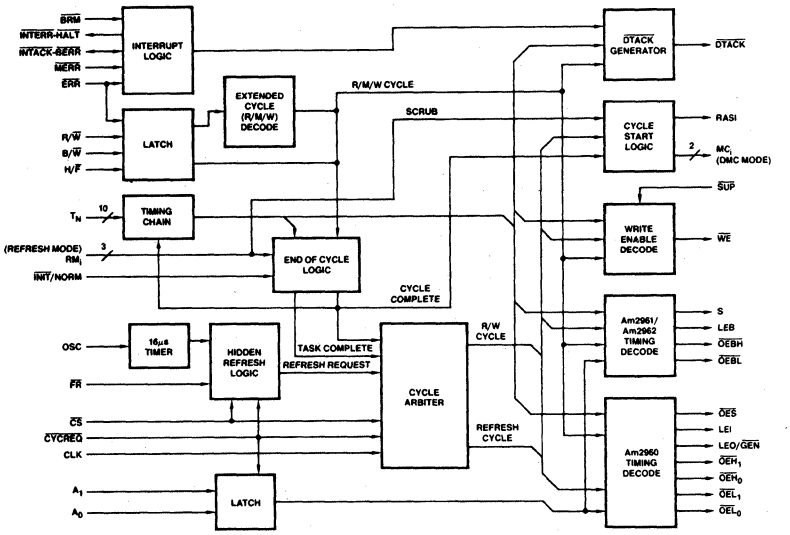
GENERAL DESCRIPTION

The Am2969 is a high-performance Memory Timing Controller (MTC). The Am2969 is designed to be used in memory systems which use the Am2968 Dynamic Memory Controller (DMC) as well as the popular Am2960 circuits for Error Detection and Correction (EDC). All of the control signals needed by the DMC and EDC circuits are generated by the Am2969 MTC. The EDC enable signals are configured for both word and byte operations including the data controls for byte write with error correction.

The Am2929 uses a delay-line to provide maximum flexibility to the memory system designer as well as allowing him to achieve maximum performance. The delay-line is the timing reference from which the MTC generates the control signals.

The Am2969 provides an internal refresh interval timer to generate refresh requests independent of the CPU. This guarantees proper refresh timing under all combinations of CPU and DMA requests.

BLOCK DIAGRAM



BD001910

RELATED PRODUCTS

Part No.	Description
Am2960/60A	16-Bit Error Detection and Correction Unit
Am2961/62	4-Bit Multiple Bus Buffers
Am2968	Dynamic Memory Controller

05221B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

A_0, A_1 — ADDRESS BITS 0 and 1, Input
These are the two least significant bits of the CPU address. They are used to control byte and 16-bit word operations. A_0 and A_1 are latched on the HIGH-to-LOW transition of $\overline{CYCREQ}$.

$\overline{BRM}$ — BUS RETRY MODE, Input
When this input is LOW, the Am2969 enters the Bus Retry Mode. In this mode the $\overline{INTERR}$ and $\overline{INTACK}$ pins assume the $\overline{BERR}$ and $\overline{HALT}$ functions respectively. An explanation of the Bus Retry Mode is given in the "Application" section.

B/$\overline{W}$ — BYTE/WORD, Input
This input indicates a byte operation is to be performed when HIGH, and a word operation when LOW.

CLK — CLOCK, Input
For systems requiring synchronous arbitration of memory access and refresh requests, this input would receive the system clock. For asynchronous arbitration this input must be tied HIGH.

$\overline{CS}$ — CHIP SELECT, Input
When $\overline{CS}$ is LOW, the MTC is enabled. A memory read/write cycle can only be performed when $\overline{CS}$ is active, while refresh cycles occur independent of $\overline{CS}$. When $\overline{CS}$ is HIGH, all memory requests (HIGH-to-LOW transition of $\overline{CYCREQ}$) will be interpreted as refresh requests ("Hidden" refresh).

$\overline{CYCREQ}$ — CYCLE REQUEST, Input
When $\overline{CS}$ is LOW, this input will generate an internal memory request for the Am2969 or the HIGH-to-LOW transition of $\overline{CYCREQ}$.

$\overline{DTACK}$ — DATA TRANSFER ACKNOWLEDGE, Output
The HIGH-to-LOW transition of $\overline{DTACK}$ informs the CPU that a write cycle has begun, or that data will be on the system bus at the correct time during a read cycle.

$\overline{ERR}$ — ERROR, Input
When this signal goes LOW, it indicates that an error has occurred on a read cycle. This input should be connected to the $\overline{ERR}$ output of the Am2960 EDC unit.

$\overline{FR}$ — FORCED REFRESH, Input
This input is used to force a refresh cycle at user-designated times. The falling edge of $\overline{FR}$ latches an internal refresh request. if the memory is busy, the refresh is done at the completion of the current cycle.

H/$\overline{F}$ — HALF/FULL, Input
This input indicates the relative size of the system bus with respect to the memory bus. It is HIGH if the system bus is half the memory width, and LOW if the system bus width is equal to the memory width.

$\overline{INTACK}$ ($\overline{BERR}$) — INTERRUPT ACKNOWLEDGE (BUS ERROR), Input (Output)
When $\overline{INTACK}$ goes LOW it will reset the Interrupt Request ($\overline{INTERR}$) output of the Am2969. In the Bus Retry Mode, this pin will act as the BUS ERROR output. An explanation for $\overline{BERR}$ is given in the "Application" section.

$\overline{INTERR}$ ($\overline{HALT}$) — INTERRUPT ERROR (HALT), Output (Output)
The $\overline{INTERR}$ output interrupts the processor if a single-bit error is detected in the "Fly-By" mode, or if a multiple-bit error is detected in the Flow-Thru mode (see "Application" section for descriptions of "Fly-By" and "Flow-Thru" modes). In the Bus Retry Mode, this pin will act as the HALT output which is explained in the "Application" section.

$\overline{INT}$/NORM — INITIALIZE/NORMAL, Input
When the Am2969 detects a falling edge on this input, it will enter the initialize mode of operation. This allows the memory to be initialized easily with a minimum of CPU overhead. When this input is HIGH, normal read/write and refresh cycles may be performed.

LEB — LATCH ENABLE BUFFER, Output
This output is intended to be connected to the LEB input of the Am2961/62 EDC Bus Buffers. It controls the latching of data going from the EDC Bus Buffers to the system bus. When LEB is HIGH, the latch is transparent; when LOW, the data is latched.

LEI — LATCH ENABLE IN, Output
This output is intended to be connected to the LE IN input of the Am2960 EDC unit. It controls the latching of data (data and check bits) into the EDC unit. The data is latched in when LEI is LOW.

LEO/$\overline{GEN}$ — LATCH ENABLE OUT/GENERATE, Output
This output is intended to be connected to the LE OUT and $\overline{GENERATE}$ inputs of the Am2960 EDC unit. LE OUT controls the latching of corrected data from the EDC into its output latch. $\overline{GENERATE}$ instructs the Am2960 to generate check bits for the data in its input latch. When LEO/$\overline{GEN}$ is HIGH, the latch is transparent; when LOW, data is latched and the EDC unit goes into the Check Bit Generation mode.

$MC_{0,1}$ — MODE CONTROL BITS 0 AND 1, Output
These outputs are connected to the $MC_{0,1}$ inputs of the Am2968 DMC. They indicate the type of memory cycle to be performed, as shown in Table A.

TABLE A. MODE SELECT TABLE

MC_1	MC_0	Mode
0	0	Refresh without Scrubbing
0	1	Refresh with Scrubbing or Initialize
1	0	Read/Write
1	1	Clear Refresh Counter

$\overline{MERR}$ — MULTIPLE ERROR, Input
This input identifies that a multiple error has been detected by the EDC unit. This input is intended to be connected to the $\overline{MERR}$ output of the Am2960.

$\overline{OEBH}$, $\overline{OEBL}$ — OUTPUT ENABLE BUS HIGH, LOW, Output
These outputs are used when interfacing to a system bus, which can either be the same width as memory or half the width. They control the multiplexing of the half-words on to the system bus from the EDC Bus Buffers. $\overline{OEBH}$ and $\overline{OEBL}$ are enabled as shown in Table B. These outputs are intended to be connected to the appropriate $\overline{OEB}$ inputs of the Am2961/62.

TABLE B. OEB TRUTH TABLE

H/$\overline{F}$	A_1	$\overline{OEBH}$	$\overline{OEBL}$
0	X	0	0
1	0	1	0
1	1	0	1

X = Don't Care

$\overline{OEH}_0$, $\overline{OEH}_1$, $\overline{OEL}_0$, $\overline{OEL}_1$ — **OUTPUT ENABLE HIGH AND LOW, Output**
These signals are used to select the appropriate output from the EDC Bus Buffers and EDC unit(s), when performing either byte writes or word writes when H/$\overline{F}$ is high. A_0 and A_1 are decoded so that the selected byte or word may be written into memory. These signals are intended to be connected to the corresponding $\overline{OE}$ inputs of the Am2960 and OEY input of the Am2961/62. Table C shows how these outputs are enabled.

$\overline{OES}$ — **OUTPUT ENABLE SYNDROMES, Output**
This output is intended to be connected to the $\overline{OE}$ $\overline{SC}$ input of the Am2960 EDC unit. It controls the feedback of the syndrome bits in the 32-bit and 64-bit modes.

OSC — **OSCILLATOR, Input**
This input signal is used to generate an internal refresh clock. It is this oscillator which initiates a refresh cycle if $\overline{FR}$ does not go active. The OSC signal may come from either external components (RC circuit) or a TTL clock source.

RASI — **ROW ADDRESS STROBE INPUT, Output**
This output is connected to the RASI input of the Am2968 DMC. It is used to start a memory access for the DMC. The RASI output is also connected to the delay line to start the timing sequence. The rising edge of RASI initiates both actions.

RM_{0-2} — **REFRESH MODE, Input**
These inputs control the type of refresh cycle the Am2969 is supposed to initiate, as specified in Table D.

R/$\overline{W}$ — **READ/WRITE, Input**
This input indicates a memory read request when HIGH, and a write request when LOW.

S — **SELECT, Output**
The S output is intended to be connected to the S input of the Am2961/62 EDC Bus Buffers. It controls the source of data for the Am2960 EDC unit. When HIGH, data comes from the system bus; when LOW, data comes from memory.

$\overline{SUP}$ — **SUPPRESS, Input**
When $\overline{SUP}$ is driven LOW, it will inhibit access to memory by disabling $\overline{WE}$. It can be used to prevent illegal access in memory-access-protected systems.

T_{1-10} — **TIMING TAPS, Input**
These inputs are the positive-edge triggered timing tap outputs from the timing reference (delay-line). They provide the necessary timing information for the Am2969 to control memory cycles. Definition of the ten timing taps is given in Table E.

$\overline{WE}$ — **WRITE ENABLE, Output**
When $\overline{WE}$ is LOW, it causes data to be written into memory. $\overline{WE}$ is inhibited if $\overline{SUP}$ is LOW, or if a multiple error is encountered during a read-modify-write cycle.

TABLE C. OUTPUT ENABLE TRUTH TABLE

H/$\overline{F}$	B/$\overline{W}$	A_1	A_0	$\overline{OEH}_1$	$\overline{OEH}_0$	$\overline{OEL}_1$	$\overline{OEL}_0$	Cycle Type
0	0	0	0	0	0	0	0	Full Word Write
0	0	0	1	0	0	0	0	
0	0	1	0	0	0	0	0	
0	0	1	1	0	0	0	0	
0	1	0	0	0	0	0	1	Byte Write
0	1	0	1	0	0	1	0	
0	1	1	0	0	1	0	0	
0	1	1	1	1	0	0	0	
1	0	0	0	0	0	1	1	Word Write
1	0	0	1	0	0	1	1	
1	0	1	0	1	1	0	0	
1	0	1	1	1	1	0	0	
1	1	0	0	0	0	0	1	Byte Write
1	1	0	1	0	0	1	0	
1	1	1	0	0	1	0	0	
1	1	1	1	1	0	0	0	

TABLE D. REFRESH MODE SELECT TABLE

RM_2	RM_1	RM_0	Refresh Mode
0	0	0	Not Scrubbing/Not Burst
0	0	1	Not Scrubbing/128-Cycle Burst
0	1	0	Not Scrubbing/256-Cycle Burst
0	1	1	Not Scrubbing/512-Cycle Burst
1	0	0	Scrubbing/Not Burst
1	0	1	Scrubbing/128-Cycle Burst
1	1	0	Scrubbing/256-Cycle Burst
1	1	1	Scrubbing/512-Cycle Burst

TABLE E. TIMING TAP DEFINITION TABLE

Tap#	Function
1	Controls when $\overline{DTACK}$ will go active during read cycles.
2	Identified when $\overline{ERR}$ flag is valid during a read cycle. Also used to control when the $\overline{RAS}$ outputs of Am2968 should be taken HIGH for read and full-word write cycles.
3	Indicates that corrected data is available at output of EDC unit during a read cycle with a single-bit error.
4	Controls when $\overline{DTACK}$ will go active during read-modify-write cycles.
5	Identifies when data and check bits are available on the memory bus during write cycles.
6	Identifies when corrected data and check bits are available on the memory bus during read-modify-write cycles.
7	Indicates that valid data is available from memory at inputs of EDC unit during read cycles.
8	Identifies when a new memory cycle may begin after a read or write cycle has been performed.
9	Controls when $\overline{RAS}$ outputs of DMC should go HIGH for read-modify-write cycles.
10	Identifies when a new memory cycle may begin after a read-modify-write cycle has been performed.

APPLICATION

ARCHITECTURE

The Am2969 MTC is designed to replace much of the MSI "glue" logic which is commonly necessary in controlling dynamic memory systems. It is responsible for controlling/arbitrating memory access and refresh, error detection and correction processes, and handshaking with the processor. The Am2969 supports both multiplexed and demultiplexed buses by controlling the output enable signals of the EDC Bus Buffers.

The Am2969 performs seven basic types of memory cycles – READ WITHOUT ERROR, READ WITH ERROR, FULL WORD WRITE, PARTIAL WORD WRITE, REFRESH, SCRUBBING, and INITIALIZE. The cycles READ WITHOUT ERROR, FULL WORD WRITE, REFRESH, and INITIALIZE are normal (read/write) accesses to memory, while the others require extended (read-modify-write) accesses.

ARBITRATION: SYNCHRONOUS vs ASYNCHRONOUS

The Am2969 arbitrates between processor (read/write) and refresh requests for a memory cycle. If both the refresh and processor cycle are requested at the same time, the processor request is serviced, first followed by the refresh request. A third type of access, memory initialization, is given priority over both processor and refresh requests. It is possible for the arbiter to be either synchronous with the system clock, or asynchronous. Synchronous arbitration requires that the inputs requesting memory, $\overline{FR}$ and $\overline{CYCREQ}$, be clocked into the Am2969 by using the CLK input. In this mode, $\overline{CYCREQ}$ and $\overline{FR}$ are examined on the negative edge of CLK. When CLK is not used (tied HIGH), the AM2969 detects is absence and enters the asynchronous mode. In this mode the first memory request to occur will be serviced, but not until after an internal delay to avoid metastable states.

FLOW-THRU vs FLY-BY READ CYCLES

The simplest way to use error-correcting memory is to extend all read cycles long enough to have single-bit errors detected before the data transfer acknowledge ($\overline{DTACK}$) is asserted. In this way, cycles can be extended by the Am2969 on detection of a single-bit error with no external logic. When a multiple-bit error is detected, the processor is interrupted and an error-handling subroutine can be initiated. The problem with this type of "flow-thru" operation is that faster memory must be used to allow for the single-bit error flag to become valid before asserting $\overline{DTACK}$. If faster memory is unavailable or undesirable, wait-states may have to be inserted into the read cycle and memory bandwidth is compromised.

In "fly-by" operation, the assumption is made that all reads will result in correct data; therefore, $\overline{DTACK}$ is asserted earlier in the cycle, which results in improved memory bandwidth. The processor will be interrupted whenever an error occurs.

One problem associated with fly-by operation comes from $\overline{DTACK}$ being asserted prior to $\overline{ERR}$ going active when a single-bit error is detected. In this case, the processor will be receiving incorrect data unknowingly. To correct this situation, additional logic may be required to cause the processor to accept the "true" corrected data.

The Am2969 determines whether flow-thru or fly-by operations should be performed by checking the relationship of T_1 and T_2. The Fly-By mode is entered when T_1 occurs before T_2, and the flow-thru mode is identified by T_2 going LOW prior to T_1.

BUS RETRY MODE

If the system processor can support a bus retry request, the Am2969 has a read access mode which offers the best of flow-thru and fly-by operation.

In this mode, read cycles are normally performed as fly-by. However, instead of interrupting the processor when a single-bit error is encountered, the Am2969 requests the last cycle to be "rerun" by asserting $\overline{BERR}$ and $\overline{HALT}$ simultaneously. An internal status flip flop is set which reserves the next processor request for a read cycle to the same location. On this access, $\overline{DTACK}$ is delayed until the erroneous data has been corrected. If a multiple error is detected, $\overline{BERR}$ is asserted and the processor can enter an error recovery subroutine.

MEMORY INITIALIZATION

Error-correcting memories are normally initialized to avoid the read errors associated with memory which powers up in a random state. The Am2969 facilitates this procedure via the $\overline{INIT}$/NORM input. The data pattern written to memory can either be all zero, using the INITIALIZE mode of the Am2960, or any desired pattern present on the system bus during the first memory cycle of the initialize routine.

Upon entering the INITIALIZE mode, the Am2969 performs eight "wake-up" cycles and then 2^{20} write/refresh cycles. Upon completion of the initialization, the Am2969 begins normal memory arbitration.

REFRESH OPERATIONS

The Am2969 can support a variety of refresh schemes. The type of refresh is controlled via the RM_{0-2} inputs. Basic refresh types include distributed, as well as 128-, 256- or 512-cycle burst.

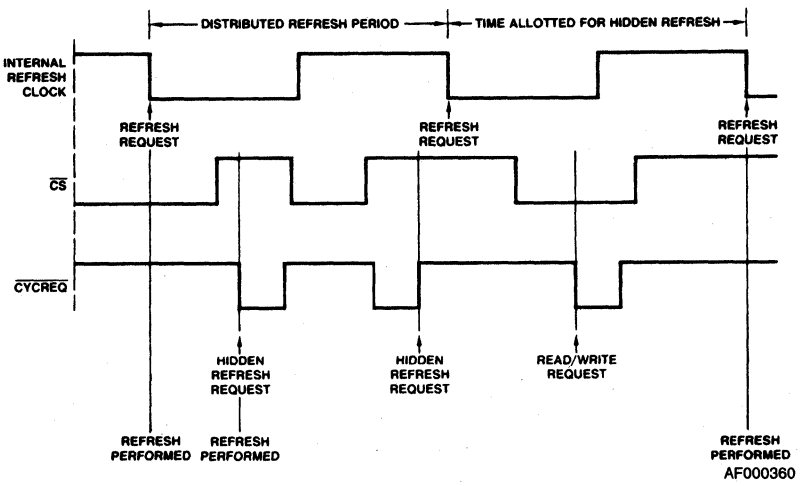
The internal refresh request is controlled by the $\overline{FR}$ input, or the output of the internal oscillator as follows:

- In the burst mode of operation, the $\overline{FR}$ input is always the refresh clock.
- The $\overline{FR}$ input can also be used as the refresh clock in the distributed refresh (non-burst) mode. However, the internal oscillator takes over as the refresh clock if it goes through three cycles without a LOW level appearing on the $\overline{FR}$ input. This provision allows the primary refresh clock ($\overline{FR}$) to be interrupted while it is in the HIGH logic state, and for refresh operations to be resumed at the internal oscillator frequency.
- It is also possible to use the on-chip oscillator as the refresh clock in distributed refresh mode. In this case, the $\overline{FR}$ input should be tied HIGH. However, since the on-chip oscillator is asynchronous to the external CLK input, it is necessary to provide a synchronous refresh clock via the $\overline{FR}$ input if synchronous arbitration is desired.

The Am2969 has the ability to increase memory bandwidth by inserting refresh requests when the processor is accessing other devices or performing I/O operations ($\overline{CYCREQ}$ = LOW, $\overline{CS}$ = HIGH). A hidden refresh can only be performed once every refresh clock period, and occurs only with distributed refreshing. When a hidden refresh is performed, the Am2969 will skip the next refresh request. Figure 1 shows the timing involved to perform a hidden refresh cycle.

Depending on the system configuration and operation, it is possible for the DRAM to appear "static," providing that a hidden refresh can be performed every refresh clock period.

Figure 1. Hidden Refresh Cycle

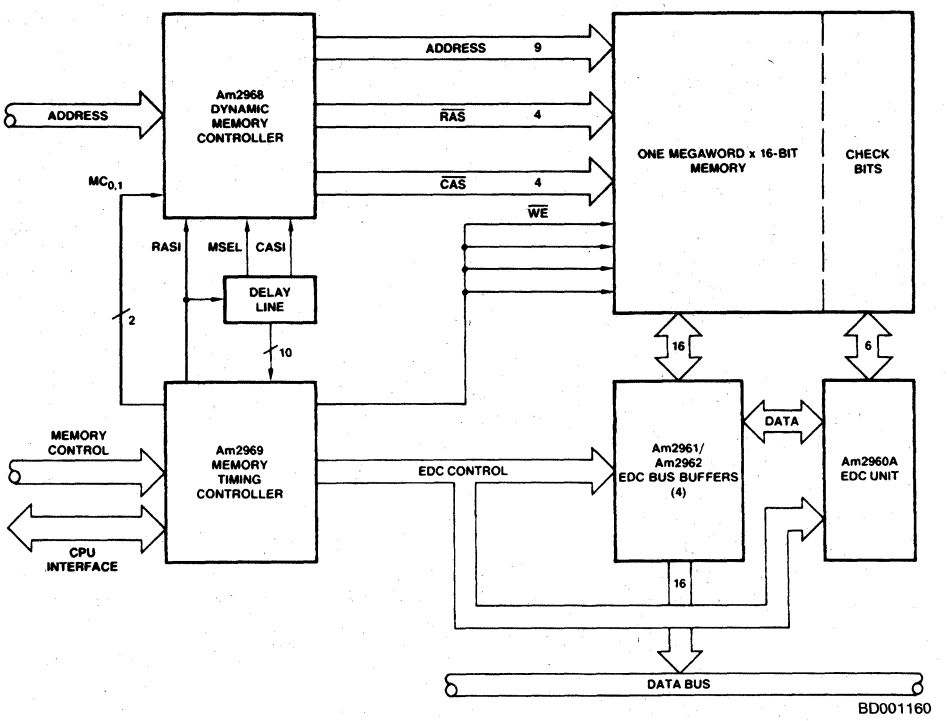


MEMORY ERROR SCRUBBING

Memory scrubbing is a housekeeping operation in which memory is checked for errors during normal refresh operations. On each refresh cycle, one memory location is read, checked for errors, and if necessary, corrected and written back to memory. This is a preventative operation to minimize the amount of error accumulation. If the processor is not attempting to access memory during a scrubbing cycle, the processing throughput for that cycle is increased over that of a system not implementing scrubbing. This is made possible because a non-scrubbing system forces the processor to wait after an error is detected, to allow the corrected data to be written back to memory. This occurs during a normal read cycle. For a scrubbing system, the extra time needed to write corrected data back into memory can be "hidden" from the processor since this occurs during refresh.

Once the $\overline{ERR}$ signal goes LOW during a scrubbing cycle, the Am2969 extends the cycle by not issuing $\overline{DTACK}$. The writing of corrected data back into memory is accomplished by controlling the output enables of the EDC unit and EDC Bus Buffers. The Am2969 is also responsible for having the Am2968 DMC perform a write cycle so that the corrected data can be written into the same memory location. If a multiple-bit error is encountered during a scrubbing cycle, $\overline{WE}$ will be inhibited. The total time required to "scrub" a one-megaword memory of all single-bit errors is 16 seconds (assuming one refresh cycle every 16 μsec).

One Megaword Dynamic Memory System with Error Detection and Correction



Am2970

Dynamic Memory Timing Controller

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Provides complete timing control for 64K/256K memory systems which utilize the Am2968 Dynamic Memory Controller
- Supports extended cycle timing needed for byte-write operations
- Internal or external control of refresh
- Burst (up to 512-cycle), distributed, or hidden refresh
- Memory access/refresh request arbitration
- 24-pin 0.3″ space-saving package

GENERAL DESCRIPTION

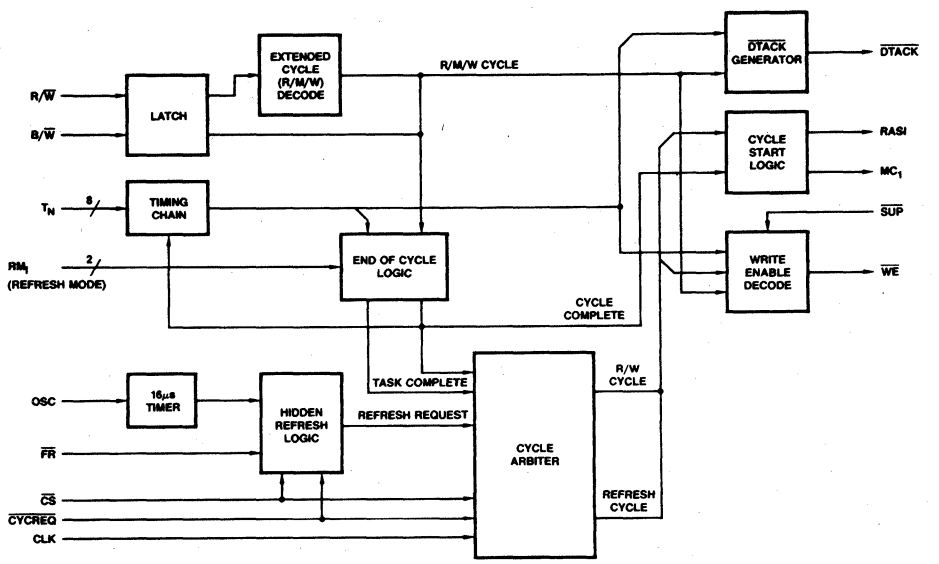
The Am2970 is a high-performance Memory Timing Controller (MTC). The Am2970 is designed to be used in memory systems which use the Am2968 Dynamic Memory Controller (DMC).

All of the control signals needed by the DMC are generated by the Am2970 MTC.

The Am2970 uses a delay-line to provide maximum flexibility to the memory system designer as well as allowing him to achieve maximum performance. The delay-line is the timing reference from which the MTC generates the control signals.

The Am2970 provides an internal refresh interval timer to generate refresh requests independent of the CPU. This guarantees proper refresh timing under all combinations of CPU and DMA requests.

BLOCK DIAGRAM



BD001130

RELATED PRODUCTS

Part No.	Description
Am2968	Dynamic Memory Controller
Am2971	Programmable Event Generator

05404B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

B/$\overline{W}$ **BYTE/WORD, Input**
This input indicates a byte operation is to be performed when HIGH, and a word operation when LOW. When B/$\overline{W}$ is LOW, the Am2970 will provide an extended cycle so that a read-modify-write operation can be performed.

CLK **CLOCK, Input**
For systems requiring synchronous arbitration of memory access and refresh requests, this input would receive the system clock. For asynchronous arbitration, this input must be tied HIGH.

$\overline{CS}$ **CHIP SELECT, Input**
When $\overline{CS}$ is LOW, the MTC is enabled. A memory read/write cycle can only be performed when $\overline{CS}$ is active, while refresh cycles occur independent of $\overline{CS}$. When $\overline{CS}$ is HIGH, all memory requests (HIGH-to-LOW transition of $\overline{CYCREQ}$) will be interpreted as refresh requests ("Hidden" refresh).

$\overline{CYCREQ}$ **CYCLE REQUEST, Input**
When $\overline{CS}$ is LOW, this input will generate an internal memory request for the Am2970 on the HIGH-to-LOW transition of $\overline{CYCREQ}$.

$\overline{DTACK}$ **DATA TRANSFER ACKNOWLEDGE, Output**
The HIGH-to-LOW transition of $\overline{DTACK}$ informs the CPU that a write cycle has begun, or that data will be on the system bus at the correct time during a read cycle.

$\overline{FR}$ **FORCED REFRESH, Input**
This input is used to force a refresh cycle at user designated times. The falling edge of $\overline{FR}$ latches an internal refresh request. If the memory is busy, the refresh is done at the completion of the current cycle.

MC_1 **MODE CONTROL, Output**
This output should be connected to the MC_1 input of the Am2970. MC_0 of the Am2970 should be tied LOW. When MC_1 is HIGH, the Am2970 will perform a read/write cycle; when LOW, refresh will be done.

OSC **OSCILLATOR, Input**
This input signal is used to generate an internal refresh clock. It is this oscillator which initiates a refresh cycle if $\overline{FR}$ does not go active. The OSC signal may come from either external components (RC circuit) or a TTL clock source.

RASI **ROW ADDRESS STROBE INPUT, Output**
This output is connected to the RASI input of the Am2970 DMC. It is used to start a memory access for the DMC. The RASI output is also connected to the delay line to start the timing sequence. The rising edge of RASI initiates both actions.

$RM_{0,1}$ **REFRESH MODE, Input**
These inputs control the type of refresh cycle the Am2970 is supposed to initiate, as specified in Table A.

R/$\overline{W}$ **READ/WRITE, Input**
This input indicates a memory read request when HIGH, and a write request when LOW.

$\overline{SUP}$ **SUPPRESS, Input**
When $\overline{SUP}$ is driven LOW, it will inhibit access to memory by disabling $\overline{WE}$. It can be used to prevent illegal access in memory-access-protected systems.

T_{1-8} **TIMING TAPS, Input**
These inputs are the positive-edge triggered timing tap outputs from the timing reference (delay-line). They provide the necessary timing information for the Am2970 to control memory cycles. Definition of the eight timing taps is given in Table B.

$\overline{WE}$ **WRITE ENABLE, Output**
When $\overline{WE}$ is LOW, it causes data to be written into memory. $\overline{WE}$ is inhibited if $\overline{SUP}$ is LOW.

TABLE A. REFRESH MODE SELECT TABLE

RM_1	RM_0	Refresh Mode
0	0	Not Burst (Distributed)
0	1	128-Cycle Burst
1	0	256-Cycle Burst
1	1	512-Cycle Burst

TABLE B. TIMING TAP DEFINITION TABLE

Tap #	Function
1	Controls when $\overline{DTACK}$ will go active during read cycles.
2	Controls when $\overline{DTACK}$ will go active during read-modify-write cycles.
3	Identifies when data is available on the memory bus during write cycles.
4	Identifies when valid data is available on the memory bus during read-modify-write cycles.
5	Indicates that valid data is available from memory during read cycles.
6	Identifies when a new memory cycle may begin after a read or write cycle has been performed.
7	Controls when $\overline{RAS}$ outputs of DMC should go HIGH for read-modify-write cycles.
8	Identifies when a new memory cycle may begin after a read-modify-write cycle has been performed.

APPLICATION

ARCHITECTURE

The Am2970 MTC is designed to replace much of the MSI "glue" logic which is commonly necessary in controlling dynamic memory systems. It is responsible for controlling/arbitrating memory access and refresh, and handshaking with the processor. The Am2970 also provides an extended (Read-Modify-Write) cycle which is needed for byte operations.

ARBITRATION: SYNCHRONOUS vs ASYNCHRONOUS

The Am2970 arbitrates between processor (read/write) and refresh requests for a memory cycle. If both the refresh and processor cycle are requested at the same time, the processor request is serviced first, followed by the refresh request. A third type of access, memory initialization, is given priority over both processor and refresh requests. It is possible for the arbiter to be either synchronous with the system clock, or asynchronous. Synchronous arbitration requires that the inputs requesting memory, $\overline{FR}$, and $\overline{CYCREQ}$ be clocked into the Am2970 by using the CLK input. In this mode, $\overline{CYCREQ}$ and $\overline{FR}$ are examined on the negative edge of CLK. When CLK is not used (tied HIGH), the Am2970 detects its absence and enters the asynchronous mode. In this mode, the first memory request to occur will be serviced, but not until after an internal delay to avoid metastable states.

REFRESH OPERATIONS

The Am2970 can support a variety of refresh schemes. The type of refresh is controlled via the $RM_{0,1}$ inputs. Basic refresh types include distributed, as well as 128-, 256-, or 512-cycle burst.

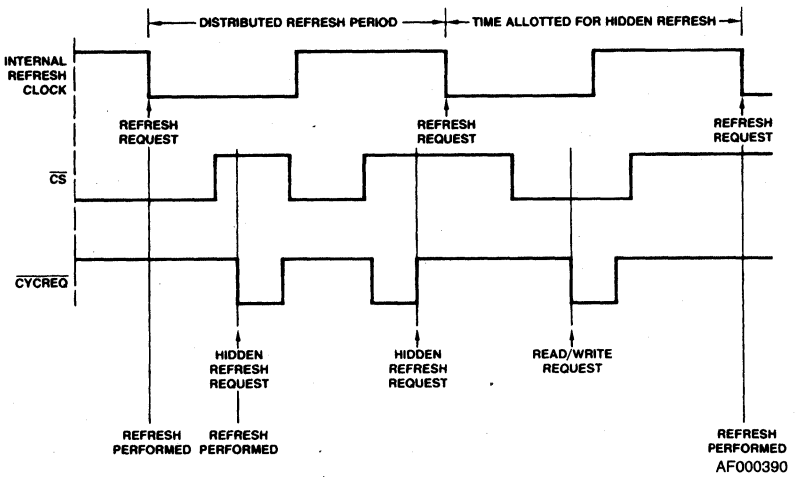
The internal refresh request is controlled by $\overline{FR}$ input, or the output of the internal oscillator as follows:

- In the burst mode of operation, the $\overline{FR}$ input is always the refresh clock.
- the $\overline{FR}$ input can also be used as the refresh clock in the distributed refresh (non-burst) mode. However, the internal oscillator takes over as the refresh clock if it goes through three cycles without a LOW level appearing on the $\overline{FR}$ input. This provision allows the primary refresh clock ($\overline{FR}$) to be interrupted while it is in the HIGH logic state, and for refresh operations to be resumed at the internal oscillator frequency.
- It is also possible to use the on-chip oscillator as the refresh clock in distributed refresh mode. In this case, the $\overline{FR}$ input should be tied HIGH. However, since the on-chip oscillator is asynchronous to the external CLK input, it is necessary to provide a synchronous refresh clock via the $\overline{FR}$ input if synchronous arbitration is desired.

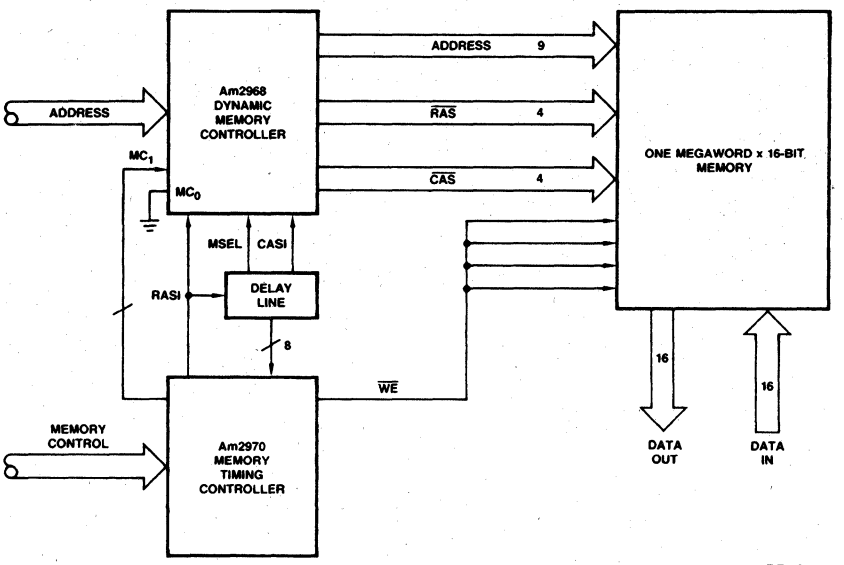
The Am2970 has the ability to increase memory bandwidth by inserting refresh requests when the processor is accessing other devices or performing I/O operations ($\overline{CYCREQ}$ = LOW, $\overline{CS}$ = HIGH). A hidden refresh can only be performed once every refresh clock period, and occurs only with distributed refreshing. When a hidden refresh is performed, the Am2970 will skip the next refresh request. Figure 1 shows the timing involved to perform a hidden refresh cycle.

Depending on the system configuration and operation, it is possible for the DRAM to appear "static," providing that a hidden refresh can be performed every refresh clock period.

Figure 1. Hidden Refresh Cycle



ONE MEGAWORD DYNAMIC MEMORY SYSTEM



BD001140

Am2971

Programmable Event Generator (PEG)

ADVANCED INFORMATION

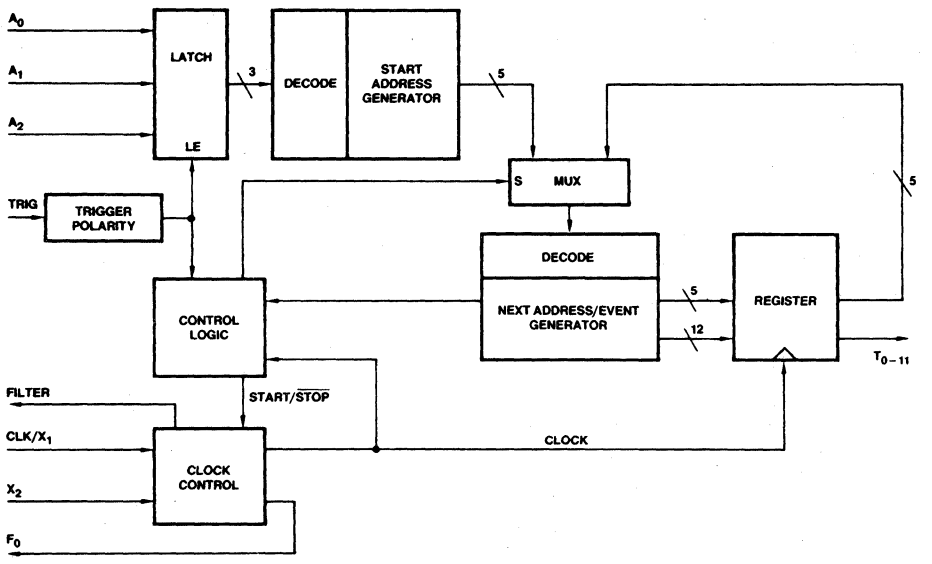
DISTINCTIVE CHARACTERISTICS

- Twelve 32-bit programmable timing events, with registered outputs
- Resolution between events down to 10ns
- Up to eight programmable starting addresses to pick first event occurrence
- Programmable clock output (F_0) frequency - 1/5 or 1/10 of internal 100MHz clock
- Internal clock reference derived from either an external clock or crystal
- 24-pin, 0.3" space saving package

GENERAL DESCRIPTION

The Am2971 is a high-performance Programmable Event Generator (PEG). The PEG is a digital replacement for an analog delay-line. It replaces several different delay-lines, because the resolution of the output signals is user selectable. The high-speed timing outputs may be used to control the Am2960 series of Dynamic Memory Support circuits (Am2968 Dynamic Memory Controller, Am2969/70 Dynamic Memory Timing Controllers), as well as being capable of generating up to 12 unique digital timing waveforms. The main advantage of the Am2971 is that all of the events are user programmable, versus the fixed, single event of a delay-line's outputs.

BLOCK DIAGRAM



BD002470

Refer to Page 13-1 for Essential Information on Military Devices

Am8163/Am8167

Dynamic Memory Timing, Refresh and EDC Controllers

DISTINCTIVE CHARACTERISTICS

- Complete CPU to dynamic RAM control interface
- $\overline{RAS}$/MSEL/$\overline{CAS}$ Sequencer to eliminate delay lines
- Complete EDC/data path controls for Word/Byte read or write
- Automatic write-back of corrected data and check bits when single errors are detected on any read cycle
- EDC error flag latches for error logging under software control
- Two timing configurations support a broad range of processors (Z80, Z8000, 8086, 8088, MC68000)

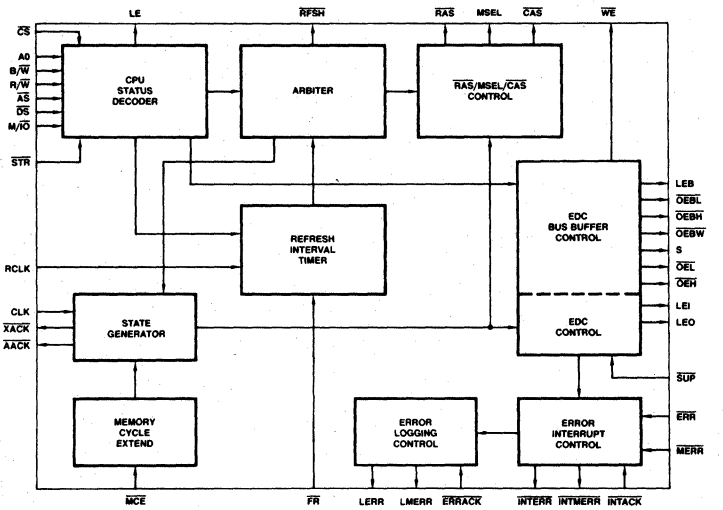
GENERAL DESCRIPTION

The Am8163 and Am8167 are high speed bus interface controllers forming an integral part of the 8086 and AmZ8000* memory support chip set using dynamic MOS RAMs with Error Detection and Correction (EDC). The complete chip set includes the Am8284A and AmZ8127 Clock Generators, the Am2964B Dynamic Memory Controller, the Am2961/62 EDC Bus Buffers, the Am2960 EDC Unit and Am2965/66 RAM Drivers.

The Am8163 and Am8167 provide all of the control interface functions including $\overline{RAS}$/Address-MUX/$\overline{CAS}$ timing (without delay lines), refresh timing, memory request/refresh arbitration and all EDC enables and controls. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction. The Am8163/7 generates bus and operating mode controls for the Am8160 EDC Unit.

The Am8163/7 uses the AmZ8127 oscillator output to generate $\overline{RAS}$/Address MUX/$\overline{CAS}$ timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA memory requests.

BLOCK DIAGRAM



BD001270

RELATED PRODUCTS

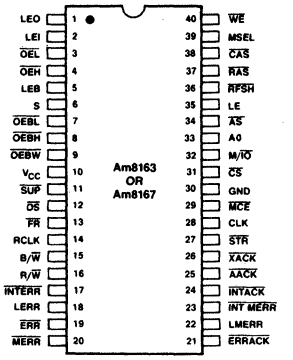
Part No.	Description	Part No.	Description
Am2960	16-Bit Error Detection and Correction Unit	Am2964B	Dynamic Memory Controller
Am2968	Dynamic Memory Controller	Am2961/62	Error Correction Bus Buffers
Am2969/70	Memory Timing Controllers	Am2965/66	Octal Dynamic Memory Drivers
Am2971	Memory Timing Controller		

*Z8000 is a trademark of Zilog.

01553A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

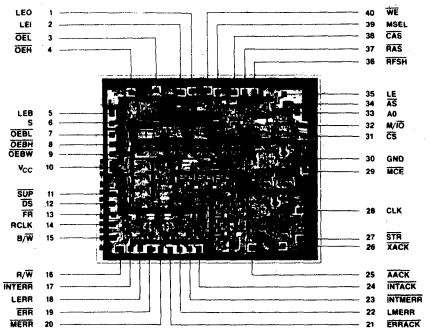


CD001550

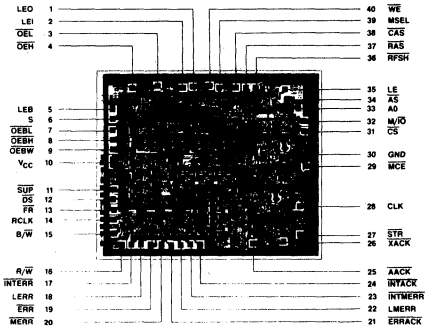
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

Am8163



Am8167



DIE SIZE 0.185" x 0.156"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am8163
Am8167 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 40-pin CERDIP (D-40-1)
  - X – Dice

Device type
Dynamic Memory Timing, Refresh, and EDC Controller

Valid Combinations	
Am8163	DC, DCB, DM, DMB XC, XM
Am8167	DC, DCB XC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

01553A

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Bus Control			
28	CLK	I	Clock. The CLK input determines memory cycle timing via the internal state machine from which the control outputs are derived. It is normally 16MHz for the Am8163 and 22MHz for the Am8167. The clock can run at lower frequencies, but not higher, because of other memory timing constraints.
14	RCLK	I	Refresh Clock. This input determines the period of the internal refresh interval ÷ 16 timer and is normally 1MHz. This results in a refresh cycle every 16 microseconds. This provides an internal refresh request to guarantee valid memory data independent of other system operating modes, (memory request, DMA, etc.).
13	$\overline{FR}$	I	Force Refresh. FR is used to force a refresh cycle at user-designated times. One example is transparent refresh during I/O operations. The refresh interval timer is reset so the next refresh occurs 16 RCLK cycles later if no other $\overline{FR}$ pulses occur. $\overline{FR}$ can be used to minimize collisions with memory requests, thereby reducing the amount of time the CPU waits for refresh.
26	$\overline{XACK}$	O	Transfer Acknowledge (open collector). This active LOW output indicates that corrected data has been latched in the Am8160 EDC output latch (as opposed to indicating data is valid on the system bus).
25	$\overline{AACK}$	O	Advanced Acknowledge (open collector). This active LOW output indicates that a memory access has started. It can be used to run without wait states when the memory system timing is synchronous with the CPU clock. Multibus or asynchronous configuration should use $\overline{XACK}$ to control the CPU Ready input.
11	$\overline{SUP}$	I	Suppress. This active LOW input inhibits access to the RAM in memory access protected systems. It must be valid before the HIGH-to-LOW transition of $\overline{DS}$ to suppress a read cycle. It must remain valid until after the cycle ($\overline{RAS}$). This is required because $\overline{SUP}$ simply inhibits $\overline{WE}$ on a write and inhibits $\overline{OEBH}$, $\overline{OEBL}$, and $\overline{OEBW}$ on a read, without halting the internal state generator.
12	$\overline{DS}$	I	Data Strobe. This active LOW input is used during read cycles to generate $\overline{OEBL}$, $\overline{OEBH}$ and $\overline{OEBW}$. These signals control when data is enabled onto the system data bus.
33	A0	I	Address Bit 0. A0 data input is latched internally on the LOW-to-HIGH transition of $\overline{AS}$. It is used during byte operations to designate whether high byte or low byte data is being accessed. A0 = LOW for high byte operations and A0 = HIGH for low byte operations with the AmZ8000 Family CPU's. A0 phasing is opposite for 8086 and inversion can be avoided by interchanging the roles of $\overline{OEL}$ and $\overline{OEH}$ (and $\overline{OEBL}$ and $\overline{OEBH}$).
34	$\overline{AS}$	I	Address Strobe. The $\overline{AS}$ input is used to control the A0 latch. When HIGH, A0 data is latched. For non-multiplexed buses, the $\overline{AS}$ input is tied LOW to make the latch transparent.
15	B/$\overline{W}$	I	Byte/$\overline{Word}$. This input designates a byte operation if HIGH and a word operation if LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine $\overline{OEH}$ and $\overline{OEL}$.
16	R/$\overline{W}$	I	Read/$\overline{Write}$. This input indicates a read operation when HIGH and a write operation when LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine the outputs $\overline{OEH}$, $\overline{OEL}$, $\overline{OEBH}$, $\overline{OEBL}$, and $\overline{OEBW}$.
32	M/$\overline{IO}$	I	Memory/$\overline{Input\text{-}Output}$. This signal serves as an active HIGH chip select for memory operations. It is used in conjunction with $\overline{CS}$ to determine if $\overline{STR}$ is valid. It must be HIGH before the LOW-to-HIGH transition of $\overline{STR}$ if the $\overline{STR}$ input command is a pulse (AmZ8000). When using a level input (multibus) to start the cycle, M/$\overline{IO}$ must become valid no later than one clock period after the HIGH-to-LOW transition of $\overline{STR}$.
31	$\overline{CS}$	I	Chip Select. This active LOW input is one of the enables for the Am8163/7. It must be LOW before the LOW-to-HIGH transition of $\overline{STR}$ when using a pulse to start a memory access. When using a level input to start the cycle, $\overline{CS}$ must become valid no later than one clock period after the HIGH-to-LOW transition of $\overline{STR}$.
27	$\overline{STR}$	I	Start. This active LOW input can be a pulse or a level. It is used to indicate when memory access is requested. It must not extend past the LOW-to-HIGH transition of $\overline{DS}$.
Address Control			
35	LE	O	Latch Enable. This output controls the LATCH ENABLE input of the Dynamic Memory Controller. When LE is HIGH, the DMC address input latch is transparent. When LE is LOW, the address is latched. This signal is $\overline{AS}$ inverted.
36	$\overline{RFSH}$	O	Refresh. This active LOW output indicates a refresh operation is to be done. The Dynamic Memory Controller uses this signal to select the refresh address output.
37	$\overline{RAS}$	O	Row Address Strobe. This active LOW output strobes the row address into memory. The $\overline{RAS}$ HIGH-to-LOW transition occurs during t_0 if $\overline{STR}$, M/$\overline{IO}$ and $\overline{CS}$ have selected a memory cycle. Additionally, $\overline{RAS}$ will be active one t-state after the $\overline{RFSH}$ HIGH-to-LOW transition occurs during refresh. The $\overline{RAS}$ LOW-to-HIGH transition at the end of each cycle starts an internally timed $\overline{RAS}$ precharge time consisting of three t-states.
39	MSEL	O	Multiplexer Select. This output controls the row and column address selection in the DMC. When MSEL is HIGH, the row address is selected and when LOW, the column address is selected. MSEL is normally HIGH and goes LOW only during memory accesses.
38	$\overline{CAS}$	O	Column Address Strobe. This active LOW output strobes the column address into memory. It is generated only during memory accesses.
Error Logging and Control			
19	$\overline{ERR}$	I	Error. This active LOW signal from the Am8160 EDC indicates when an error has occurred. The Am8163 samples this input just before the HIGH-to-LOW transition of $\overline{LEO}$. Single errors cause an automatic write-back of corrected data.
20	$\overline{MERR}$	I	Multiple Error. This active LOW signal from the EDC indicates when a multiple error has occurred. Write back to memory is inhibited if a $\overline{MULTIPLE\ ERROR}$ occurs on a read cycle.
18	LERR	O	Latched Error. This active HIGH output is set HIGH as a result of the $\overline{ERR}$ input becoming active. LERR HIGH indicates an error has occurred. LERR is normally used to control error logging. It is reset when $\overline{ERRACK}$ goes LOW.
22	LMERR	O	Latched Multiple Error. This active HIGH output is set HIGH as a result of the $\overline{MERR}$ input. When HIGH, it indicates a multiple error has occurred. It is reset when $\overline{ERRACK}$ goes low.
17	$\overline{INTERR}$	O	Interrupt Error (open collector). This active LOW output is used to interrupt the CPU when an error occurs. This can be used for diagnostics or error logging. $\overline{INTERR}$ has high output drive capability in order to drive system buses.

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Refer to Page 13-1 for Essential Information on Military Devices

Pin No.	Name	I/O	Description
Error Logging and Control (Cont.)			
23	$\overline{\text{INTMERR}}$	O	Interrupt Multiple Error (open collector). This active LOW output is used to interrupt the CPU when a multiple error occurs. This can be used for diagnostics or error logging. $\overline{\text{INTMERR}}$ has high output drive capability in order to drive system buses.
24	$\overline{\text{INTACK}}$	I	Interrupt Acknowledge. This active LOW input resets both the $\overline{\text{INTERR}}$ and $\overline{\text{INTMERR}}$ signals.
21	$\overline{\text{ERRACK}}$	I	Error Acknowledge. This active LOW input resets the error logging flags, LERR and LMERR. It is only effective when $\overline{\text{INTACK}}$ has previously cleared the interrupt flags, $\overline{\text{INTERR}}$ and $\overline{\text{INTMERR}}$.
EDC Control			
5	LEB	O	Latch Enable Bus. LEB is used to latch corrected data in the external Am8161/2 EDC Data Bus Buffers. By latching data output to the system data bus, the CPU can be operated in a single-step mode. The data latch is required to capture data so the memory can be released for refresh immediately after a read (or write) cycle.
1	LEO	O	Latch Enable Output. LEO is used to latch corrected data in the Am8160 EDC data output latch. Correct data is then available to regenerate correct check bits for the write portion of the read-modify-write cycle. LEO can also control LEY of the Am8161/2 EDC Data Bus Buffers (the input latch from the system data bus). This is required in systems where the CPU removes data from the system data bus before the Am8163/7 has completed a write cycle.
2	LEI	O	Latch Enable Input. LEI is used to control the Am8160 EDC's input latch. It is normally LOW when a memory cycle is not in progress. This prevents transitions on the bus from toggling the EDC logic, thereby reducing power dissipation and system noise. LEI latches the input data so the EDC data bus (Y bus) can be TURNED AROUND WHILE the EDC is correcting the data. Cycle time is reduced by doing these functions in parallel.
6	S	O	Select. This output controls the multiplexer that selects EDC input data. It is normally HIGH to select data from the system bus. When LOW, it selects data from memory. Since all cycles are a read-modify-writes, S switches every cycle. All memory operations take the same number of internal t-states. There is no difference in the length of a cycle on read or write, error or no error.
8	$\overline{\text{OEBH}}$	O	Output Enable Bus High. $\overline{\text{OEBH}}$ output enables the high byte data onto the system data bus during byte read operations. It is used when interfacing to 8-bit data buses or the Multibus.*
7	$\overline{\text{OEBL}}$	O	Output Enable Bus Low. $\overline{\text{OEBL}}$ output enables the low byte of data onto the system data bus during Byte Read operations. It is used when interfacing to 8-bit data buses or the Multibus.
9	$\overline{\text{OEBW}}$	O	Output Enable Bus Word. $\overline{\text{OEBW}}$ output enables data onto the system data bus. It occurs on every read cycle independent of B/$\overline{\text{W}}$. It is used for 16-bit systems or Multibus systems.
4	$\overline{\text{OEH}}$	O	Output Enable High. $\overline{\text{OEH}}$ controls the high byte of the EDC data bus (Y bus). When $\overline{\text{OEH}}$ is HIGH, the Am2961/62 are driving the bus. When $\overline{\text{OEH}}$ is LOW, the Am8160 EDC is driving the bus. $\overline{\text{OEH}}$ is HIGH during word writes and goes low on reads and byte writes.
3	$\overline{\text{OEL}}$	O	Output Enable Low. $\overline{\text{OEL}}$ controls the low byte of the EDC data bus (Y bus). When HIGH, the Am2961/62's are driving the bus. When LOW, the Am2960 is driving the bus. $\overline{\text{OEL}}$ is HIGH during word writes and goes LOW on reads and byte writes.
Other Controls			
40	$\overline{\text{WE}}$	O	Write Enable. $\overline{\text{WE}}$ controls the memory during a write operation. It is generated during a byte or word write and also during a read if a single error has occurred. $\overline{\text{WE}}$ always occurs at the end of the memory cycle. Thus, the RAM is always doing a late write.
29	$\overline{\text{MCE}}$	I	Memory Cycle Extend. This input is normally not used and is pulled up internally to produce "normal" timing. When tied LOW it extends the memory cycle (adds 5 t_2 states for Am8163 and adds 4 t_3 states for Am8167). This allows use of slower RAMs. Note that $\overline{\text{MCE}}$ affects the refresh cycle as well as the normal cycle. By adding external logic, the user may extend the cycle by 1, 2 or 3 t=states instead. This is done by keeping MCE low until 2, 3, or 4 clocks after MS for the 8163 or 2, 3, or 4 clocks after $\overline{\text{CAS}}$ for the 8167.

*Multibus is a registered trademark of Intel Corporation.

FUNCTION TABLES

Am8163/8167

R/$\overline{\text{W}}$	B/$\overline{\text{W}}$	A0	$\overline{\text{OEH}}$	$\overline{\text{OEL}}$
L	L	L	H	H
L	L	H	H	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	L
H	L	H	L	L
H	H	L	L	L
H	H	H	L	L

OEH and OEL are enabled by appropriate sequencer "T" states. (See Timing Diagram)

$\overline{\text{DS}}$	R/$\overline{\text{W}}$	B/$\overline{\text{W}}$	A0	$\overline{\text{OEBH}}$	$\overline{\text{OEBL}}$	$\overline{\text{OEBW}}$
X	L	L	L	H	H	H
X	L	L	H	H	H	H
X	L	H	L	H	H	H
X	L	H	H	H	H	H
L	H	L	L	L	H	L
L	H	L	H	H	L	L
L	H	H	L	L	H	L
L	H	H	H	H	L	L
H	X	X	X	H	H	H

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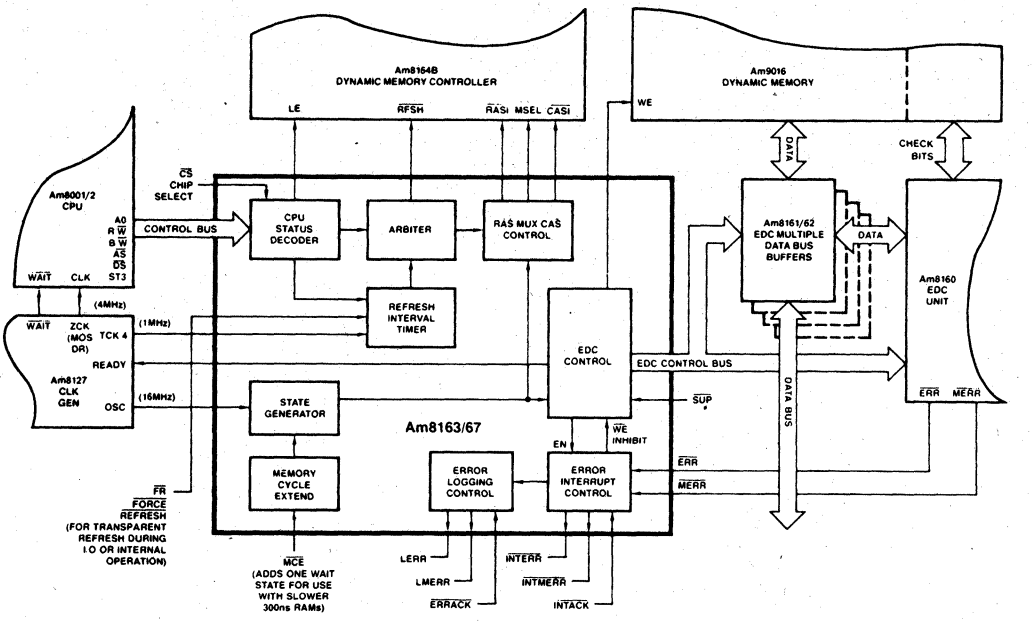
SYSTEM DIAGRAM



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Am8163/67 DETAILED DESCRIPTION

The Am8163/67 provides timing and control for Error Detection and Correction (EDC) using dynamic Random Access Memories (RAM) together with the Am2960 family of EDC devices. See Table 1 to determine which device (Am8163/67) is best suited to which processor.

The Am2960 family provides an optimized, but also flexible solution to the interface between MOS microprocessors and dynamic MOS RAMs.

The Am2960 performs the function of error detection and correction, using a modification of the well-known Hamming Code algorithm.

The Am2961 and Am2962 are bus buffers optimized for operation with the Am2960.

TABLE 1.

Processor		Am8163	Am8167
Z80A		X	
Z80B		X	
Z8000	– 4MHz	X	
	– 6MHz		X
	– 8MHz	X	X
8086	– 5MHz	X	
	– 10MHz		X
8088	– 5MHz	X	
	– 10MHz		X
68000	– 4MHz	X	
	– 6MHz		X
	– 8MHz	X	X
	– 10MHz	X	X
	– 12MHz	X	X

Note: Where X's appear in both columns, either device may be used.

The Am2964B performs address latching and multiplexing for the RAS/CAS sequence. It also contains a refresh counter that can be multiplexed onto the address outputs.

The Am2965 and Am2966 are octal memory address bus drivers, similar and pin-compatible to the popular 74LS240 and 74LS244, but with on-chip resistors that reduce the problem of undershoot on unterminated address lines.

None of the above-mentioned circuits contain timing elements. To achieve the greatest versatility, this function is concentrated in the Am8163.

The Am8163/67 performs two independent functions:

1. It provides timing and control to the Am2964B Dynamic Memory Controller, i.e., the RAS/CAS Refresh address multiplexer.
2. It provides timing and control for the 2960, 2961, or 2962 EDC circuits and interfaces with the microprocessor's interrupt lines and WAIT input.

RAS/CAS and Refresh

The Am8163/67 accepts several control signals from the microprocessor (BYTE/$\overline{\text{WORD}}$, READ/$\overline{\text{WRITE}}$, Address Strobe, Data Strobe, Memory/IO) and a Refresh clock signal from the clock generator.

From these inputs, the Am8163/67 generates control signals for the 2964B RAS/CAS and Refresh multiplexer.

The LE output, when HIGH, makes the 2964B input latches transparent. The HIGH-to-LOW transition of LE latches address information into the 2964B.

The $\overline{\text{RAS}}$ output is activated when the appropriate combination of $\overline{\text{STR}}$, M/$\overline{\text{IO}}$, and $\overline{\text{CS}}$ occur or when a refresh operation

is to be performed. MSEL goes LOW one clock period after $\overline{RAS}$ goes LOW.

$\overline{CAS}$ goes LOW a short specified delay after MSEL goes LOW. $\overline{RAS}$, MSEL and $\overline{CAS}$ go HIGH together, eight clock periods after RAS goes LOW. The RAS/CAS timing is thus derived from a high frequency (16MHz clock) without any monostables or delay lines.

The Am8163 and Am8167 are comparable except for the CAS timing sequence.

The Am8163 timing is optimized for operation with a 4MHz microprocessor clock, derived from a 16MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (62ns) and the MS to $\overline{CAS}$ delay is combinatorial, 16ns minimum.

The Am8167 timing is optimized for operation with a 5.5MHz microprocessor clock, derived from a 22MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (47ns) and the MS to $\overline{CAS}$ delay is also one oscillator period (47ns).

Dynamic Memory Refresh

The proper sequencing of refresh operations can be performed either by the CPU (transparent refresh) or by the memory controller (stand-alone refresh).

Transparent refresh, as implemented in the Z80 and Z8000 microprocessors is simple and avoids all memory contention, but it wastes processor time and is not fully compatible with DMA operation.

"Stand-alone" refresh puts the responsibility of refresh address generation and timing on the memory controller. The Am8163/67 performs the necessary timing and access arbitration. The internal refresh interval timer generates a refresh request after every 16 clock pulses on the RCLK refresh clock input (typically 1MHz). When FR (force refresh) goes LOW, the ÷ 16 counter is cleared and the internal refresh request is generated.

Refresh requests and memory requests are synchronized inside the Am8163/67 where the arbiter circuit resolves potential conflicts. If a refresh request occurs after a memory request or during a memory operation, this refresh request will be honored after the memory transaction is complete and the necessary additional precharge time has elapsed.

Similarly, if a memory request occurs after a refresh request or during a refresh operation, this memory request will not be acknowledged until the refresh operation is completed and the necessary precharge time has elapsed. When memory and refresh requests occur simultaneously, the arbiter favors the memory request.

Error Detection/Correction

The other function of the Am8163/67 is timing and control for Error Detection and Correction using the 2960, 2961 or 2962 circuits.

The Am8163/67 drives the ECC Control Bus and receives ERROR or MULTIPLE ERROR inputs from the 2960 Error Detection and Correction Unit. The Am8163/67 also interfaces with the microcomputer interrupt structure and with the error-logging circuitry.

The 2960 can support two methods of error correction: "Correct Only On Error" and "Correct Always".

"Correct Only On Error" relies on the fact that error detection is faster than correction. Data read from the memory is fed directly to the processor. A read error will insert a wait state while the error is being corrected and data is also being written back into the memory. At reasonably low error rates, this scheme achieves the highest possible throughput, but it is incompatible with all present microprocessors, since they sample their WAIT input too early in the cycle.

The Am8163/67 implements the other scheme— "Correct Always"—which is compatible with all modern microprocessors.

This scheme allocates time to insure that corrected data is sent to the CPU. Additionally, the Am8163/67 allows time after each memory read operation, to write the corrected result back into the memory. This write operation, however, is executed only if there was a single error; there is no need to write correct data back, and it is undesirable to write the wrong result of a double error.

the Am8163/67 also provides the proper control signals to allow byte write operation in 16-bit memory systems with Error Correction. The Am8163/67 automatically first performs a word read operation, retains the corrected unused byte in the 2960, and then writes the composite word and check bits into the memory. Outputs LEO, LEI, $\overline{OEH}$, $\overline{OEL}$ and S are responsible for this.

- **$\overline{OEL}$** is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 0 (even address)
- **$\overline{OEH}$** is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 1 (odd address)
- **$\overline{OEBW}$** is pulsed LOW during every read operation
- **$\overline{OEBL}$** is pulsed LOW during every read operation with A0 = 1 (odd address)
- **$\overline{OEBH}$** is pulsed LOW during every read operation with A0 = 0 (even address)

Note: The $\overline{OE}$ and $\overline{OEB}$ outputs interpret A0 in opposite ways. This is consistent with 2960/61 operation.

R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEH}$	$\overline{OEL}$	$\overline{OEBW}$	$\overline{OEBH}$	$\overline{OEBL}$
L	L	L	H	H	H	H	H
L	L	H	H	H	H	H	H
L	H	L	H	L	H	H	H
L	H	H	L	H	H	H	H
H	L	L	L	L	L	L	H
H	L	H	L	L	L	H	L
H	H	L	L	L	L	L	H
H	H	H	L	L	L	H	L

$\overline{OEBW}$, $\overline{OEBH}$, and $\overline{OEBL}$ can be active (LOW) only if: $\overline{DS}$ = $\overline{CS}$ = L AND $\overline{SUP}$ = H

Note that 16-bit memory with EDC must always be initialized with word write operations in order to allow a later byte write operation. (An uninitialized memory would most likely read multiple errors and would then not allow byte write operation.)

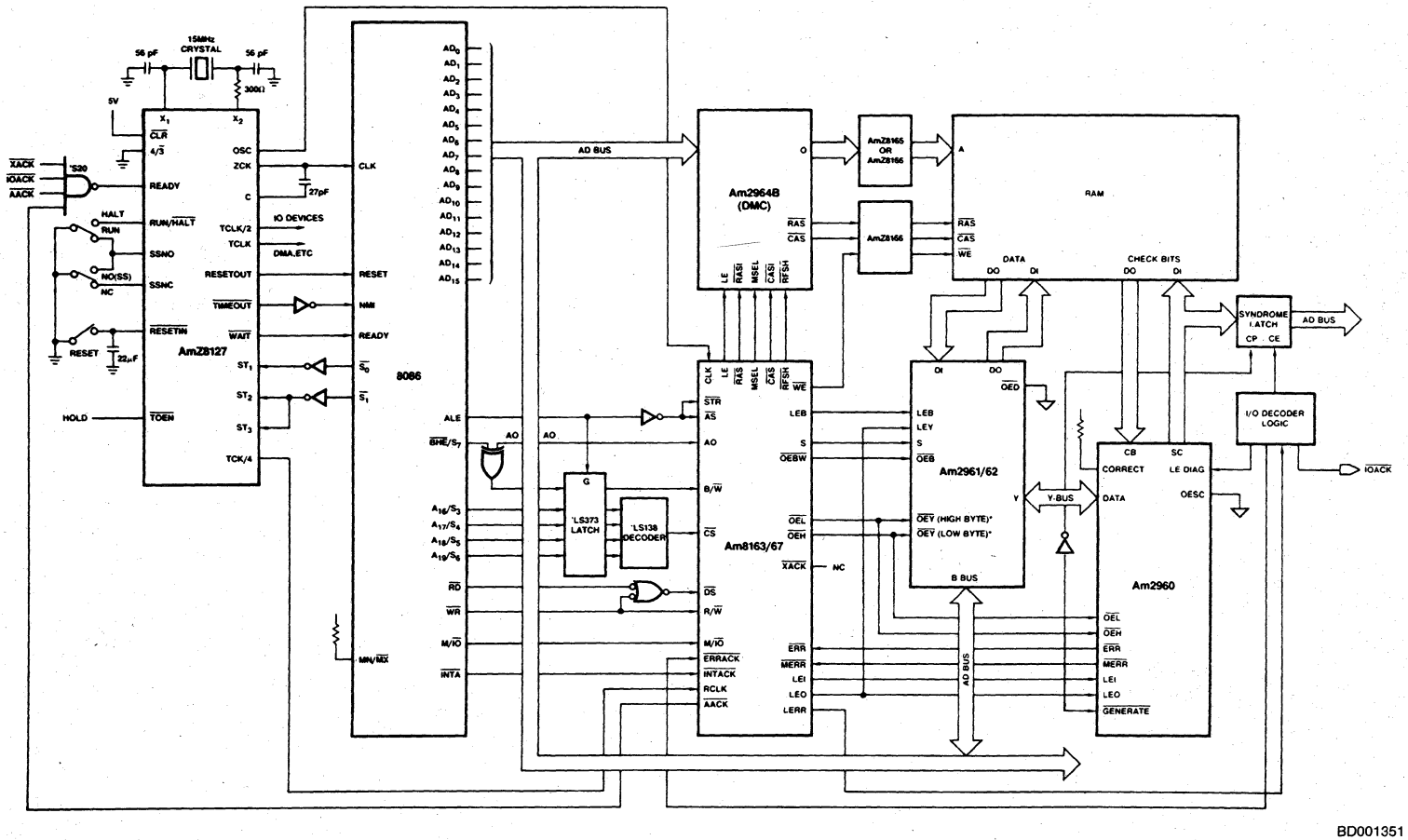
Error Interrupt Control

The Am8163/67 clocks in the $\overline{ERROR}$ and $\overline{MULTIPLE\ ERROR}$ signals coming from the 2960 and stores them in both the Interrupt Logic and in the Error Control Logic.

Interrupt Acknowledge clears both $\overline{INTERR}$ and $\overline{INTMERR}$. The latter must therefore always be the higher priority interrupt.

The Error Logic Control circuit latches up the two bits in the Error Interrupt Control circuit. The LERR and LMERR outputs are cleared by $\overline{ERRACK}$, provided that the interrupts have been cleared first. These signals are normally used to control updating of the syndrome latch or other diagnostic circuitry.

Am8163/67 APPLICATION WITH Am8086 CPU AND Am8127 CLOCK GENERATOR



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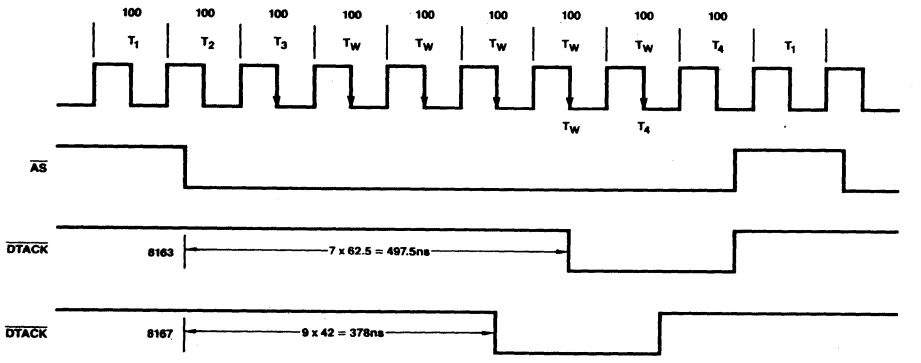
Am8163/67 APPLICATION WITH MC68000



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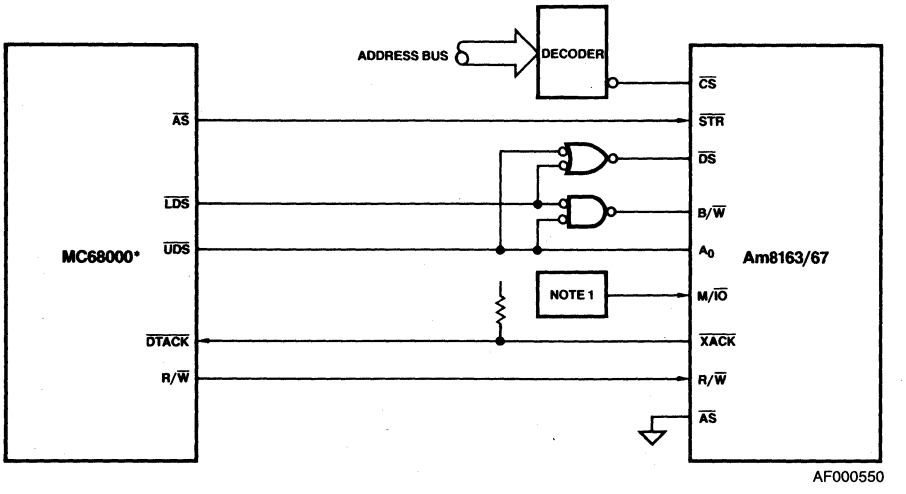

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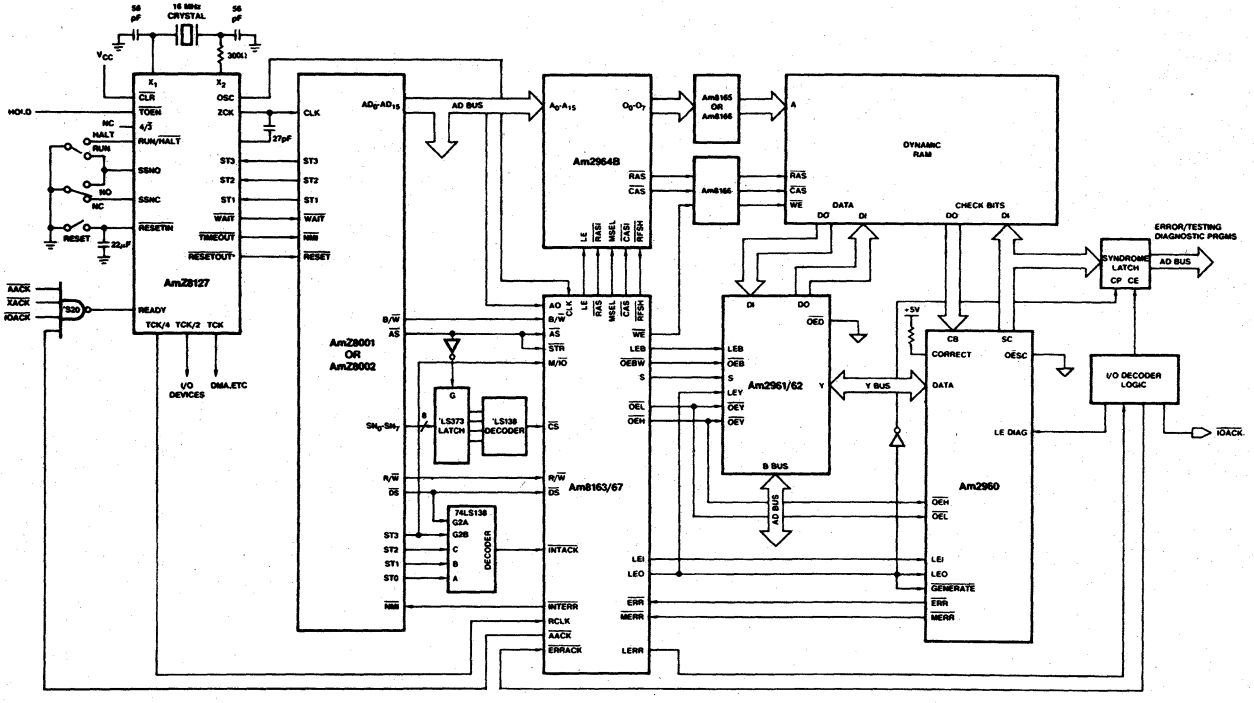
*Timing refers to 10MHz MC68000.

Note 1: M/$\overline{IO}$ may be tied HIGH or connected to an address pin. It may also be connected to an I/O port. The main consideration is not to start the 8163/67 when communicating with the 2960 Diagnostic Latch.

Am8163/67 APPLICATION WITH Am8001/2 AND Am8127 CLOCK GENERATOR



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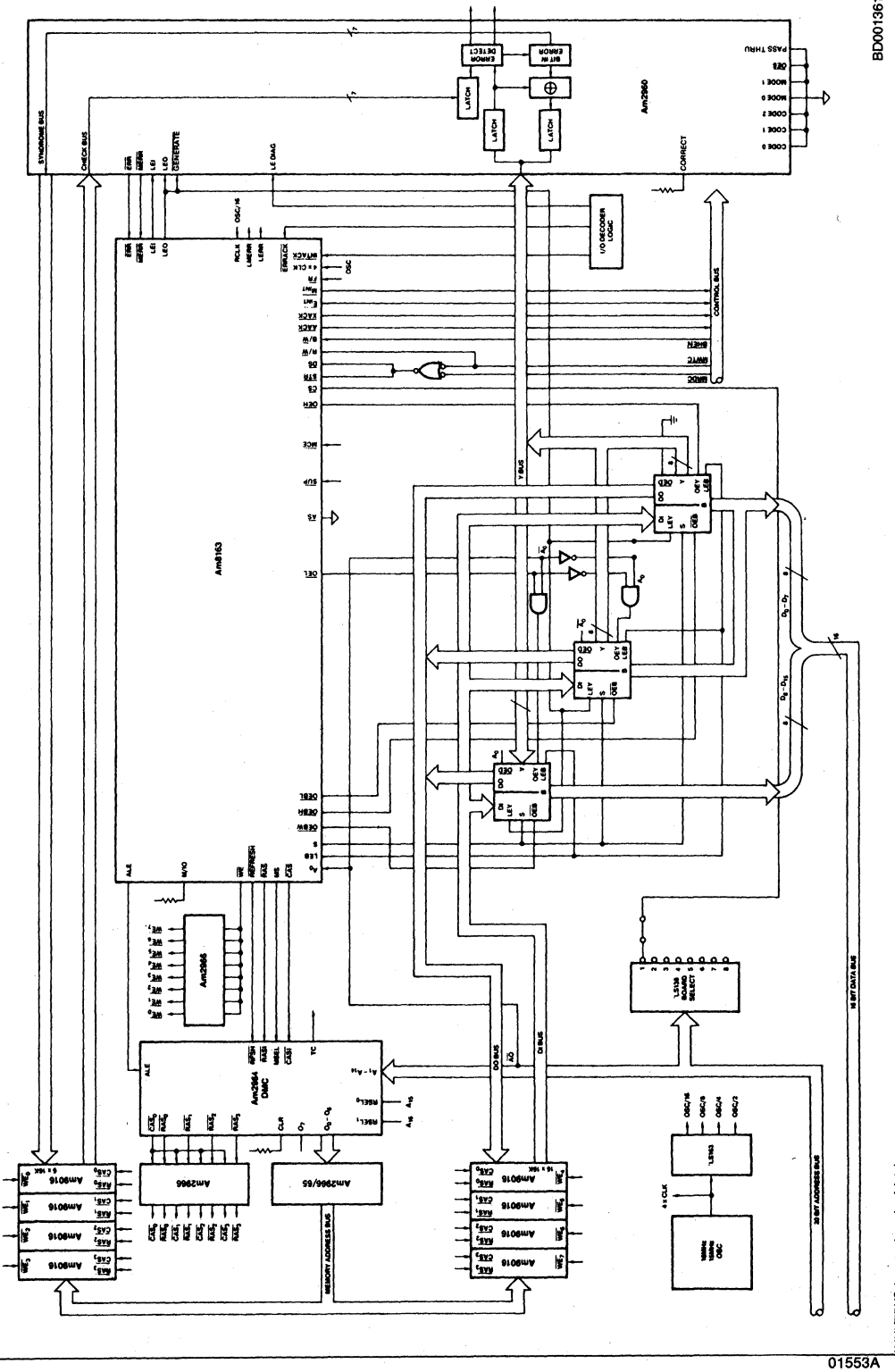
Am8163/67 APPLICATION WITH MULTIBUS*



*MULTIBUS is a trademark of Intel.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} Max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

(Group A, Subgroups 1, 2 and 3)

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	**Output(s):** All except open collectors	MIL, I_{OH} = −1.0mA	2.4			Volts
				COM'L, I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	**Output(s):** LERR, LMERR	I_{OL} = 8mA			0.50	Volts
			$\overline{CAS}$, $\overline{RAS}$, $\overline{OEBH}$, $\overline{OEBL}$	I_{OL} = 12mA			0.50	
			$\overline{OEH}$, $\overline{OEL}$, $\overline{OEBW}$, $\overline{RFSH}$	I_{OL} = 12mA			0.50	
			LEO, LEI, $\overline{WE}$	I_{OL} = 12mA			0.50	
			LEB, LE, S, MSEL	I_{OL} = 12mA			0.50	
			$\overline{INTMERR}$, $\overline{INTERR}$	I_{OL} = 16mA			0.50	
			$\overline{XACK}$, $\overline{AACK}$	I_{OL} = 32mA			0.50	
V_{IH}	Guaranteed Input Logical HIGH Voltage		**Input(s):** All		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage		**Input(s):** All	MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN	**Input(s):** All	I_{IN} = −18mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX V_{IN} = 0.5V	**Input(s):** A0, M/$\overline{IO}$, RCLK, B/$\overline{W}$, R/$\overline{W}$ $\overline{STR}$, $\overline{AS}$, $\overline{INTACK}$	MIL			−0.42	mA
				COM'L			−0.40	
			$\overline{FR}$, $\overline{SUP}$, $\overline{ERRACK}$, $\overline{MCE}$	MIL			−0.82	mA
				COM'L			−0.8	
			$\overline{CLK}$, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			−2.1	mA
				COM'L			−2.0	
			$\overline{MERR}$	MIL			−2.6	mA
				COM'L			−2.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX V_{IN} = 2.7V	**Input(s):** $\overline{MERR}$	MIL			100	µA
				COM'L			70	
			CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			70	µA
				COM'L			50	
			$\overline{FR}$, $\overline{SUP}$, $\overline{MCE}$, $\overline{ERRACK}$				40	µA
			M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$				20	
			$\overline{AS}$, $\overline{STR}$, $\overline{INTACK}$				20	
I_I	Input HIGH Current	V_{CC} = MAX V_{IN} = 5.5V	**Input(s):** CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$, $\overline{MERR}$				1.0	mA
			$\overline{SUP}$, $\overline{MCE}$, $\overline{FR}$				1.0	
		V_{CC} = MAX V_{IN} = 7.0V	M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$ $\overline{INTACK}$, $\overline{AS}$, $\overline{STR}$				0.10	
			$\overline{ERRACK}$				0.20	
I_{OH}	Output HIGH Current	V_{CC} = MIN V_{OH} = 5.5V	**Output(s):** $\overline{INTMERR}$, $\overline{INTERR}$				100	µA
			$\overline{XACK}$, $\overline{AACK}$				150	

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
I_{OS}	Output Short Circuit Current	V_{CC} = MAX + 0.5V V_O = 0.5V	**Output(s):** All (Note 3)		−15		−85	mA
I_{CC}	Power Supply Current	8163	25°C, 5V			280		mA
			0 to 70°C	COM'L			365	mA
		8167	0 to 70°C				390	mA
		8163	−55 to +125°C	MIL			385	mA
		8167	−55 to +125°C				420	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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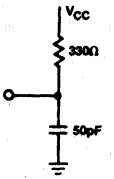
Refer to Page 13-1 for Essential Information on Military Devices

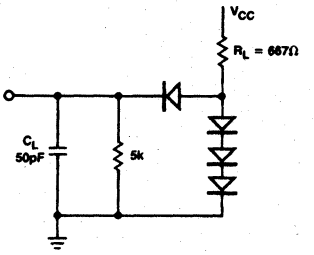
SWITCHING TEST CIRCUIT

INTERR,INT MERR



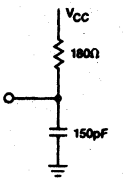
TC000640

OTHER OUTPUTS



TC000650

XACT,AACK



TC000660

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters		Description	Min	Typ	Max	Units
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	0	−4		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	0	−10		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	5	2		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 5	tp + 2		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		12	18	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		12	18	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1	0		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	9	5		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20	9		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	2	0		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp	−(tp + 10)		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10	6		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		36	41	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		26	34	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		17	22	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		21	26	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay – 8163	18	23		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay – 8167		17	22	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8163		34	43	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8167		21	26	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		30	35	ns
20	t_{PHL}	CLK to $\overline{AACK}$↓ Propagation Delay		33	41	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		17	22	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		20	26	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		16	22	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay – 8163	1.0	3.0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay – 8167		21	26	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		20	26	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		17	22	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	15	20		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8163	4.5	7.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8167		24	30	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		24	30	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0	−1.5		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0	−10		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		15	21	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		21	26	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		21	26	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		24	30	ns
36	t_{PHL}	CLK to $\overline{XACK}$↑ Propagation Delay		29	36	ns
37	t_{PLH}	DS↑ to $\overline{XACK}$↑ Propagation Delay		24	30	ns
38	t_{PHL}	DS↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		13	18	ns

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters		Description	Min	Typ	Max	Units
39	t_{PLH}	DS↑ to $\overline{OEBL}$↑, $\overline{OEBH}$↑, $\overline{OEBW}$↑ Propagation Delay		13	18	ns
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	1.5	0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	6.5	4		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		19	24	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		23	30	ns
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		30	39	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		9	14	ns
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20	9		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20	9		ns
48	t_S	$\overline{SUP}$↓ to $\overline{DS}$↓ Setup Time	0	−5		ns
49	t_H	$\overline{WE}$↑ to SUP↑ Hold Time	0	−10		ns
50	t_{PHL}	CLK to $\overline{RFSH}$↓ Propagation Delay		16	21	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8163		4tp		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8167		5tp		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8163		3tp		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8167		4tp		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8163		7tp		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8167		9tp		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8163		6tp		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8167		8tp		
55a	f_{OSC}	CLK Frequency – 8163			16	MHz
55b	f_{OSC}	CLK Frequency – 8167			22	MHz

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Refer to Page 13-1 for Essential Information on Military Devices

Switching Characteristics (Cont.)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters		Description	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	5		5		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	5		5		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	9		9		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 10		tp + 10		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		22		22	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		22		22	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1.5		1.5		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	10		10		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20		20		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	5		5		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp		−tp		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10		12		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		45		45	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		40		40	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		25		25	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		30		30	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay – 8163	16		16		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay – 8167		25		25	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8163		50		50	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8167		30		30	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		40		40	ns
20	t_{PHL}	CLK to $\overline{AACK}$↓ Propagation Delay		46		46	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		25		25	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		30		30	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		25		25	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay – 8163	0		0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay – 8167		30		30	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		30		30	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		25		25	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	10		10		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8163	4.0		4.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ – 8167		35		35	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		35		35	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0		1.0		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0		0		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		25		25	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		30		30	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		30		30	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		35		35	ns
36	t_{PHL}	CLK to $\overline{XACK}$↑ Propagation Delay		40		41	ns
37	t_{PLH}	$\overline{DS}$↑ to $\overline{XACK}$↑ Propagation Delay		35		35	ns
38	t_{PHL}	DS↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		22		22	ns
39	t_{PLH}	$\overline{DS}$↑ to $\overline{OEBL}$↑, $\overline{OEBH}$ ↑, $\overline{OEBW}$↑ Propagation Delay		22		22	ns
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	2.0		3.0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	8.0		8.0		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		28		28	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		38		38	ns
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		46		46	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		20		20	ns

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters		Description	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20		20		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20		20		ns
48	t_S	$\overline{SUP}\downarrow$ to $\overline{DS}\downarrow$ Setup Time	5		5		ns
49	t_H	$\overline{WE}\uparrow$ to SUP$\uparrow$ Hold Time	5		5		ns
50	t_{PHL}	CLK to $\overline{RFSH}\downarrow$ Propagation Delay		25		25	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8163	4tp-3ns		4tp-3ns		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8167	5tp-3ns		5tp-3ns		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8163	3tp-3ns		3tp-3ns		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8167	4tp-3ns		4tp-3ns		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8163	7tp-3ns		7tp-3ns		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8167	9tp-3ns		9tp-3ns		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8163	6tp-3ns		6tp-3ns		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8167	8tp-3ns		8tp-3ns		
55a	t_{OSC}	CLK Frequency – 8163		16		16	MHz
55b	t_{OSC}	CLK Frequency – 8167		22		22	MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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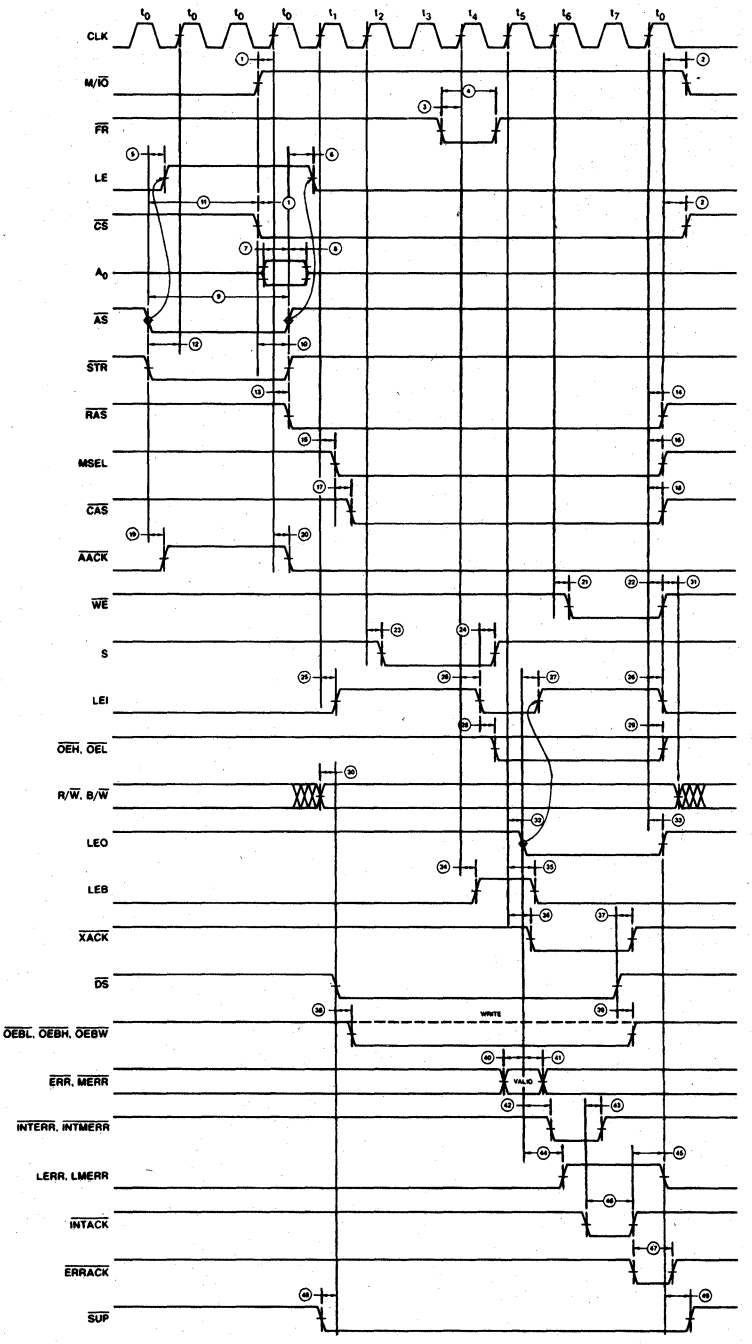
Refer to Page 13-1 for Essential Information on Military Devices

TIMING WAVEFORMS

Am8163 TIMING



WF001820

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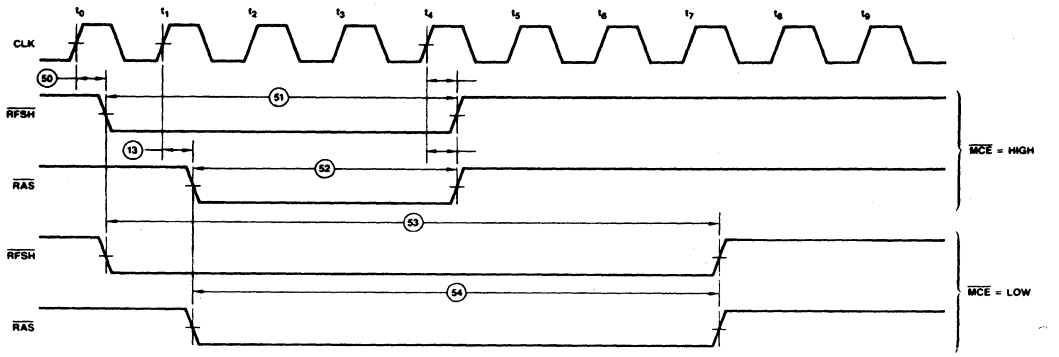
Refer to Page 13-1 for Essential Information on Military Devices

TIMING WAVEFORMS (Cont.)

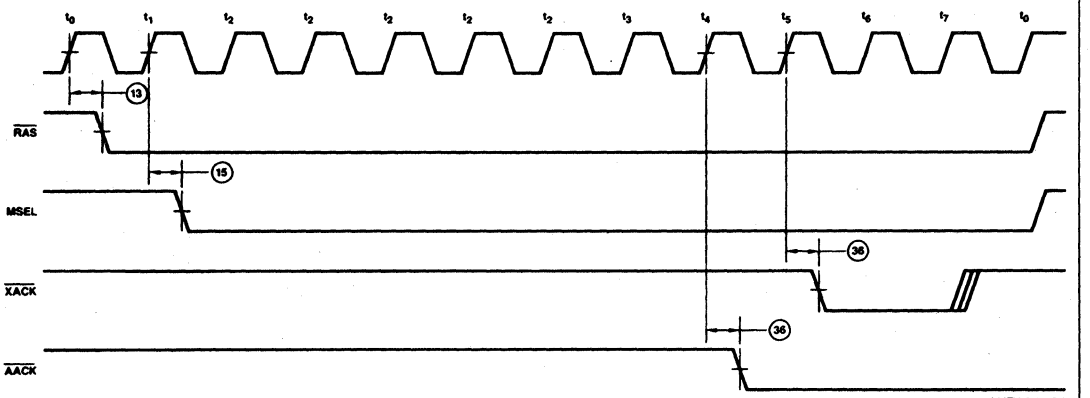
Am8163 REFRESH TIMING



WF002500

Am8163 MEMORY CYCLE EXTEND TIMING

(MCE = LOW)



WF001800

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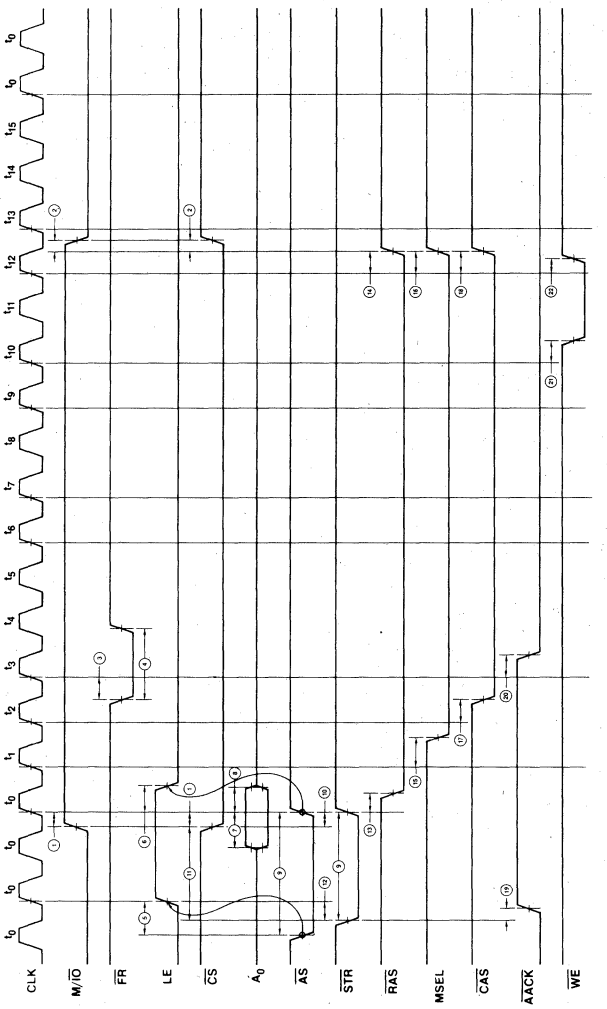

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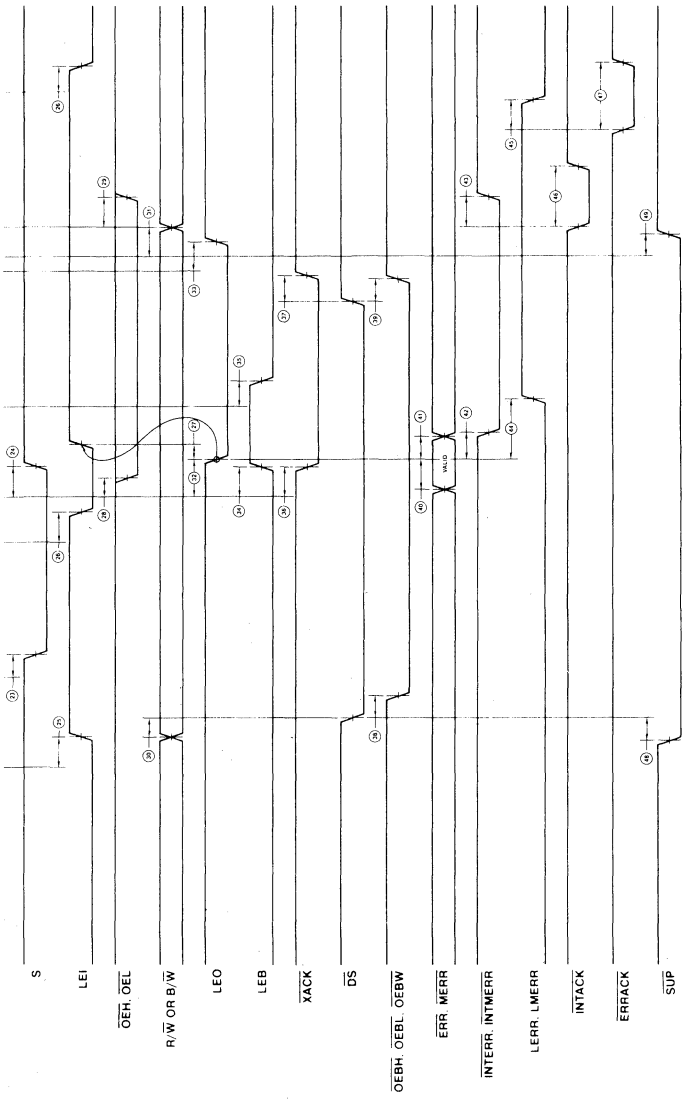
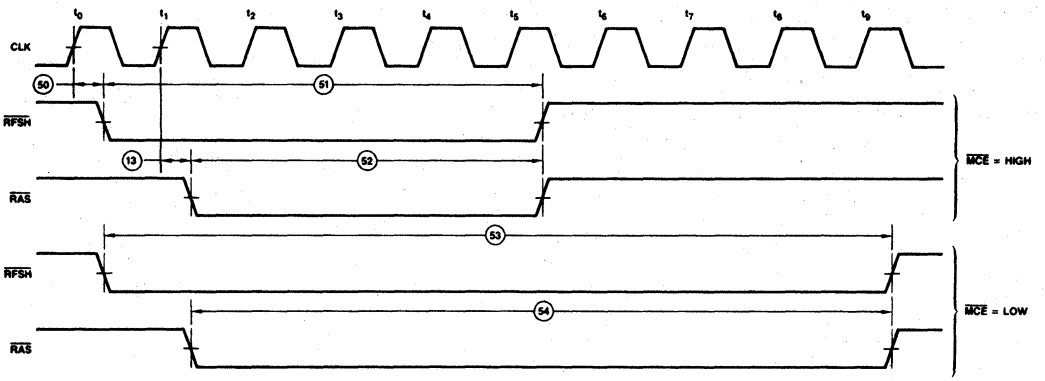
Refer to Page 13-1 for Essential Information on Military Devices


S
LEI
OEH, OEL
R/W OR B/W
LEO
LEB
XACK
DS
OEBH, OEBL, OEBW
ERR, MERR
INTERR, INTMERR
LERR, LMERR
INTACK
ERRACK
SUP
VALID

01553A

TIMING WAVEFORMS (Cont.)

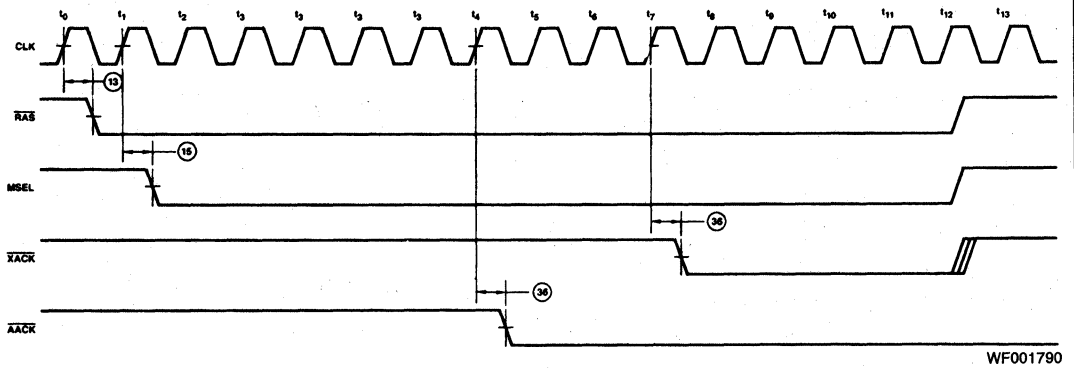
Am8167 REFRESH TIMING



WF001780

Am8167 MEMORY CYCLE EXTEND TIMING

($\overline{MCE}$ = LOW)



WF001790

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Refer to Page 13-1 for Essential Information on Military Devices

Am2900 Processors and Peripherals Family Index

Am2901B/Am2901C

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- **Two-address architecture –**
  Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU –**
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Expandable –**
  Connect any number of Am2901s together for longer word lengths.
- **Left/right shift independent of ALU –**
  Add and shift operations take only one cycle.
- **Four status flags –**
  Carry, overflow, zero, and negative.
- **Flexible data source selection –**
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.

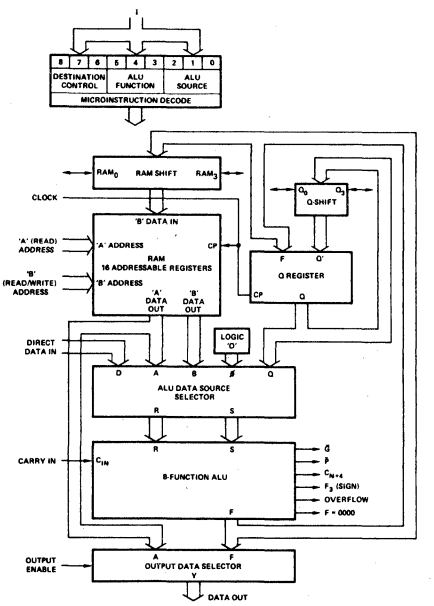
GENERAL DESCRIPTION

The Am2901 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the Am2901 permits efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. AMD's ion-implanted micro-oxide (IMOX) processing is used to fabricate the 40-lead LSI chip.

The Am2901C is a plug-in replacement for the Am2901B, but is 33% faster than the Am2901B.

MICROPROCESSOR SLICE BLOCK DIAGRAM



BD002120

IMOX is a trademark of Advanced Micro Devices.

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Refer to Page 13-1 for Essential Information on Military Devices

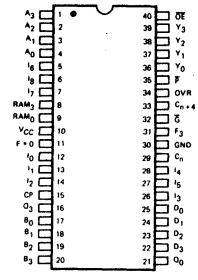
RELATED PRODUCTS

Part No.	Description
Am2902	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am27S35	Registered PROM

For applications information see Chapters III and IV of
Bit Slice Microprocessor Design,
by Mick and Brick, McGraw Hill Publishers.

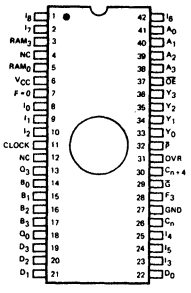
CONNECTION DIAGRAM
Top View

P-40, D-40



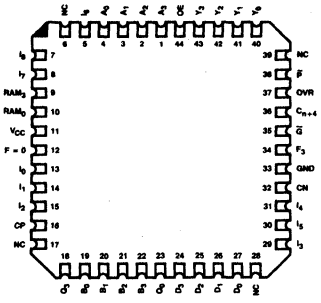
CD004110

F-42



CD004100

L-44-1

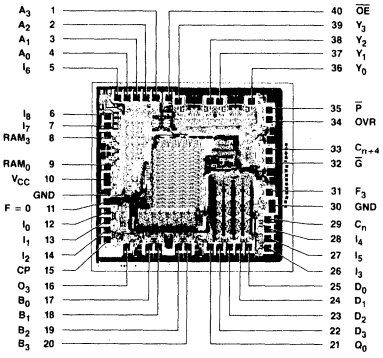


CD004120

Note: Pin 1 is marked for orientation

Figure 1.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.130" x 0.123"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2901B
Am2901C

D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 40-pin CERDIP
  - F – 42-pin flatpak
  - L – 44-pin leadless chip carrier
  - P – 40-pin plastic DIP
  - X – Dice

Device type
Four-Bit Microprocessor Slice

Valid Combinations	
Am2901B	PC DC, DCB, DMB FMB XC, XM
Am2901C	PC DC, DCB, DMB FMB LC, LMB XC, XM

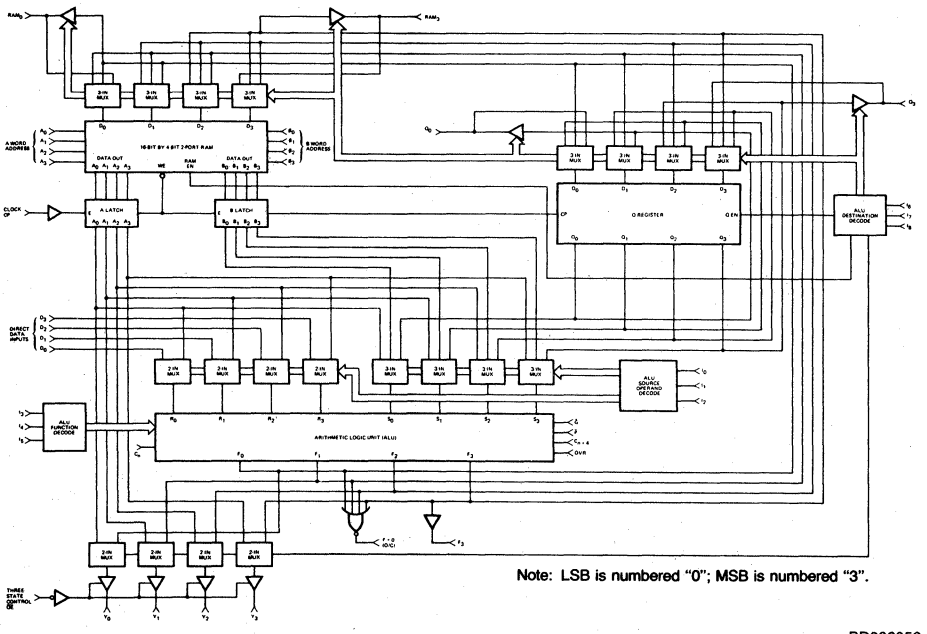
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 3, 2, 1	A_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.
17, 18 19, 20	B_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.
	I_{0-8}	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).
16	Q_3 RAM_3	I/O	A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are electrically OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).
21, 9	Q_0 RAM_0	I/O	Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.
25, 24 23, 22	D_{0-3}	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.
36, 37 38, 39	Y_{0-3}	O	The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.
40	$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).
32, 35	$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.
34	OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
11	F = 0	O	This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.
31	F_3	O	The most significant ALU output bit.
29	C_n	I	The carry-in to the internal ALU.
33	C_{n+4}	O	The carry-out of the internal ALU.
15	CP	I	The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

DETAILED Am2901C MICROPROCESSOR BLOCK DIAGRAM



Note: LSB is numbered "0"; MSB is numbered "3".

BD002050

Figure 2.

01656B

Refer to Page 13-1 for Essential Information on Military Devices

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 2, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 3. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 4. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 5.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 12 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 5.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 5.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 3. ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \bar{\vee} S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \bar{\vee} S}$

Figure 4. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 5. ALU Destination Control.

		I_{210}OCTAL							
		0	1	2	3	4	5	6	7
OCTAL I_{543}	ALU Function	ALU Source							
		A,Q	A,B	0,Q	0,B	O,A	D,A	D,Q	D,0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	−D − 1 −D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	−Q − 1 −Q	−B − 1 −B	−A − 1 −A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \bar{\vee} Q$	$A \bar{\vee} B$	Q	B	A	$D \bar{\vee} A$	$D \bar{\vee} Q$	D
7	R EX-NOR S	$\overline{A \bar{\vee} Q}$	$\overline{A \bar{\vee} B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \bar{\vee} A}$	$\overline{D \bar{\vee} Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; $\bar{\vee}$ = EX-OR

Figure 6. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 6 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 7 defines the various logic operations that the Am2901 can perform and Figure 8 shows the arithmetic functions of the device. Both carry-in LOW ($C_n = 0$) and carry-in HIGH ($C_n = 1$) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∇Q
6 1		A∇B
6 5		D∇A
6 6		D∇Q
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 7. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q-1	PASS	Q
1 3		B-1		B
1 4		A-1		A
2 7		D-1		D
2 2	1's Comp.	-Q-1	2's Comp. (Negate)	-Q
2 3		-B-1		-B
2 4		-A-1		-A
1 7		-D-1		-D
1 0	Subtract (1's Comp)	Q-A-1	Subtract (2's Comp)	Q-A
1 1		B-A-1		B-A
1 5		A-D-1		A-D
1 6		Q-D-1		Q-D
2 0		A-Q-1		A-Q
2 1		A-B-1		A-B
2 5		D-A-1		D-A
2 6		D-Q-1		D-Q

Figure 8. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 3.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R∨S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R∧S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$∧S	LOW	← Same as R∧S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R∨S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + C_n)}$	See note

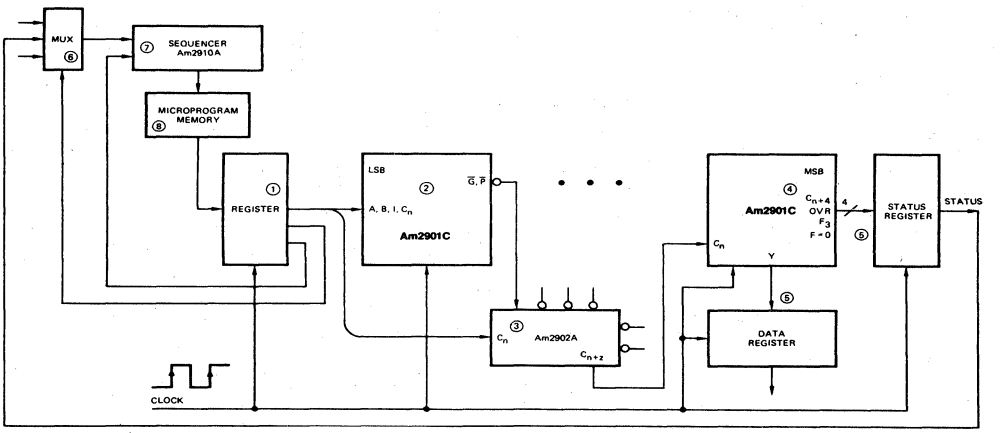
Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall$
$[\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

+ = OR

Figure 9.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901C are representative for available MSI parts.



AF001621

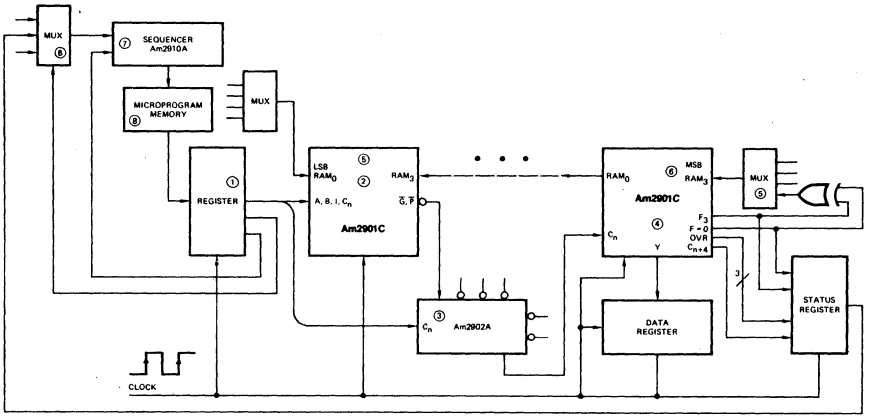
Pipelined System. Add without Simultaneous Shift.

DATA LOOP			CONTROL LOOP		
①Register	Clock to Output	9	①Register	Clock to Output	9
+ ②2901C	A, B to $\overline{G}$, $\overline{P}$	37	+ ⑥MUX	Select to Output	13
+ ③2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7	+ ⑦2910A	CC to Output	30
+ ④2901C	C_n to C_{n+4}, OVR, F_3, F = 0, Y	25	+ ⑧PROM	Access Time	40
+ ⑤Register	Setup Time	2	+ ①Register	Setup Time	2
		80ns			94ns

Minimum clock period = 94ns

01656B

Refer to Page 13-1 for Essential Information on Military Devices



AF001631

Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP		
①Register	Clock to Output	9
+ ②2901C	A, B to $\overline{G}$,$\overline{P}$	37
+ ③2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7
+ ④2901C	C_n to F_3, OVR	22
+ ⑤XOR and MUX		21
+ ⑥2901C	RAM_3 Setup	12
		108ns

CONTROL LOOP		
①Register	Clock to Output	9
+ ⑥MUX	Select to Output	13
+ ⑦2910A	CC to Output	30
+ ⑧PROM	Access Time	40
+ ①Register	Setup Time	2
		94ns

Minimum clock period = 108ns

Figure 10.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0 Y_1, Y_2, Y_3	2.4		Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4		
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4		
				I_{OH} = −600μA, F_3	2.4		
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4		
				I_{OH} = −1.6mA, $\overline{G}$	2.4		
I_{CEX}	Output Leakage Current For F = 0 Output	V_{CC} = MIN, V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L) (Note 4)		0.5	
				I_{OL} = 16mA (MIL) (Note 4)		0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA		0.5	
			C_{n+4}	I_{OL} = 10mA		0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA		0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		Clock, $\overline{OE}$		−0.36	mA
				A_0, A_1, A_2, A_3		−0.36	
				B_0, B_1, B_2, B_3		−0.36	
				D_0, D_1, D_2, D_3		−0.72	
				I_0, I_1, I_2, I_6, I_8		−0.36	
				I_3, I_4, I_5, I_7		−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 3)		−0.8	
				C_n		−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		Clock, $\overline{OE}$		20	μA
				A_0, A_1, A_2, A_3		20	
				B_0, B_1, B_2, B_3		20	
				D_0, D_1, D_2, D_3		40	
				I_0, I_1, I_2, I_6, I_8		20	
				I_3, I_4, I_5, I_7		40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 3)		100	
				C_n		200	

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters	Description	Test Conditions (Note 1)				Min	Max	Units
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX		Y_0, Y_1, Y_2, Y_3	V_O = 2.4V		50	μA
					V_O = 0.5V		−50	
				$RAM_{0, 3}$ $Q_{0, 3}$	V_O = 2.4V (Note 3)		100	
					V_O = 0.5V (Note 3)		−800	
I_{OS}	Output Short Circuit Current (Note 2)	V_{CC} = MAX + 0.5V, V_O = 0.5V		Y_0, Y_1, Y_2, Y_3, $\overline{G}$		−30	−85	mA
				C_{n+4}		−30	−85	
				OVR, $\overline{P}$		−30	−85	
				F_3		−30	−85	
				$RAM_{0, 3}$, $Q_{0, 3}$		−30	−85	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	COM'L Only (Note 4)	T_A = 0°C to +70°C			265	mA
				T_A = +70°C			220	
			MIL Only (Note 4)	T_C = −55°C to+ 125°C			280	
				T_C = +125°C			198	

Note:
1. V_{CC} conditions shown as MIN or MAX, refer to the military (±10%) or commercial (±5%) V_{CC} limits.
2. Not more than one output should be stored at a time. Duration of the short circuit test should not exceed one second.
3. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
4. "MIL" = Am2901CXM, DM, FM, LM, "COM'L" = Am2901CXC, PC, DC, LC.
5. Worst case I_{CC} is measured at the lowest temperature in the specified operating range.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment, (not functionally tested).

5

I. Am2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns. with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC
Am2901BDC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle. I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	35	35
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ⎍	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	**CP:** **Set-up Time Before H →L**	**Hold Time After H →L**	**Set-up Time Before L →H**	**Hold Time After L →H**
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change (Note 2)		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	35	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It indicates all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

II. Am2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	88ns
Maximum Clock Frequency to shift Q (50% duty cycle. I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	65	55	58	–
I345	58	58	58	48	64	56	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ⎍	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	**CP:** **Set-up Time Before H →L**	**Hold Time After H →L**	**Set-up Time Before L →H**	**Hold Time After L →H**
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change (Note 2)		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	62	0
I678	14	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	40	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

III. Am2901C Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901C over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CPC
Am2901CDC
Am2901CLC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	31ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	31ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	40	40	40	37	40	40	40	–
D	30	30	30	30	38	30	30	–
Cn	22	22	20	–	25	22	25	–
I012	35	35	35	37	37	35	35	–
I345	35	35	35	35	38	35	35	–
I678	25	–	–	–	–	–	26	26
A Bypass ALU (I = 2XX)	35	–	–	–	–	–	–	–
Clock ↓	35	35	35	35	35	35	35	28

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	CP: **Set-up Time Before H → L**	**Hold Time After H → L**	**Set-up Time Before L → H**	**Hold Time After L → H**
A, B Source Address	15	1 (Note 3)	30, 15 + T_{PWL} (Note 4)	1
B Destination Address	15	Do Not Change (Note 2)		1
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	12	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	23	23

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

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Refer to Page 13-1 for Essential Information on Military Devices

IV. Am2901C Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901C over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CDM
Am2901CFM
Am2901CLM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	32ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	32ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	48	48	48	44	48	48	48	–
D	37	37	37	34	40	37	37	–
Cn	25	25	21	–	28	25	28	–
I012	40	40	40	44	44	40	40	–
I345	40	40	40	40	40	40	40	–
I678	29	–	–	–	–	–	29	29
A Bypass ALU (I = 2XX)	40	–	–	–	–	–	–	–
Clock ⌐‾|	40	40	40	40	40	40	40	33

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	**CP:** **Set-up Time Before H →L**	**Hold Time After H →L**	**Set-up Time Before L →H**	**Hold Time After L →H**
A, B Source Address	15	2 (Note 3)	30, 15 + T_{PWL} (Note 4)	2
B Destination Address	15	Do Not Change (Note 2)		2
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	12	0

D. Output Enable/Disable Times.

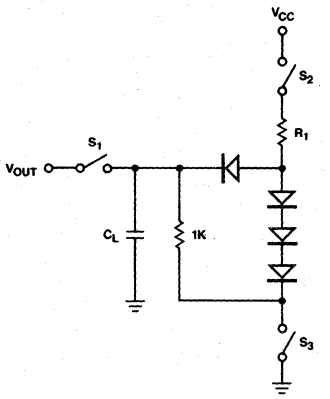
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	25	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

SWITCHING TEST CIRCUIT

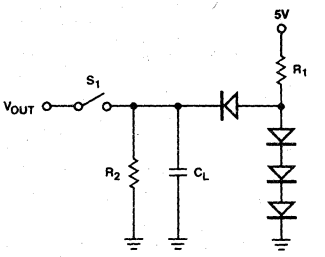
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS

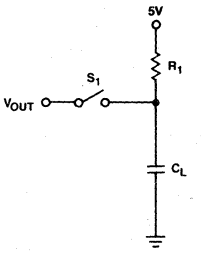


TC001080

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



TC001090

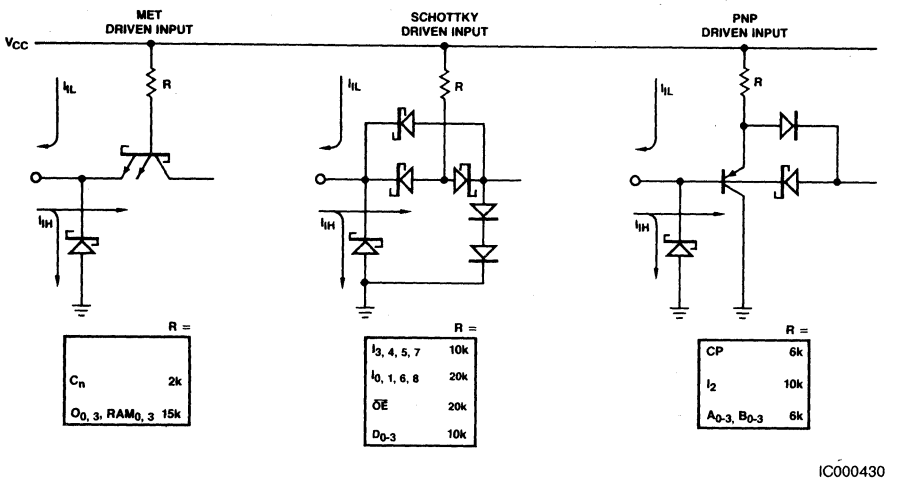
$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L=5.0pF for output disable tests.

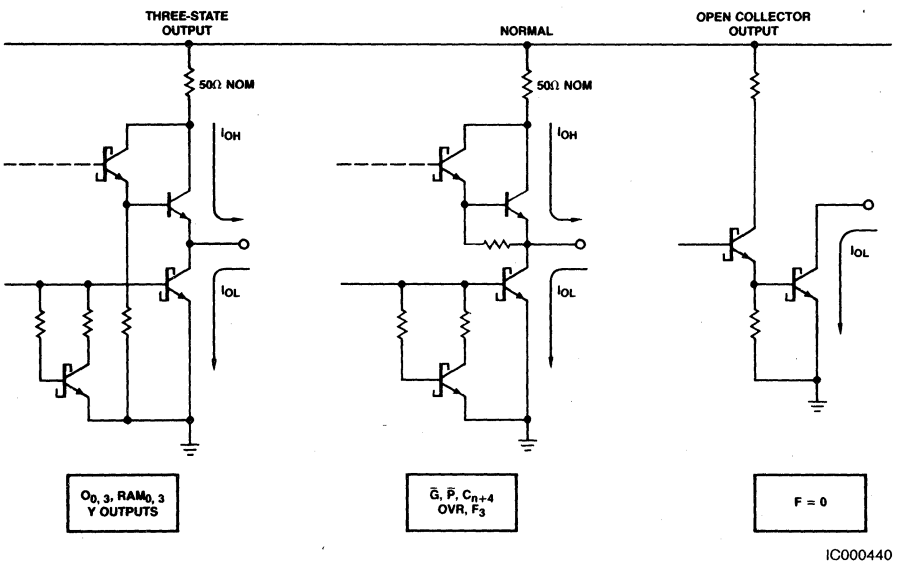
TEST OUTPUT LOADS FOR Am2901C (DIP)

Pin #	Pin Label	Test Circuit	R_1	R_2
8	RAM_3	A	560	1K
9	RAM_0	A	560	1K
11	F = 0	C	270	–
16	Q_3	A	560	1K
21	Q_0	A	560	1K
31	F_3	B	620	3.9K
32	G	B	220	1.5K
33	C_{n+4}	B	360	2.4K
34	OVR	B	470	3K
35	P	B	470	3K
36-39	Y_{0-3}	A	220	1K

TTL INPUT/OUTPUT CURRENT INTERFACES



$C_I \cong 5.0pF$, all inputs



$C_O \cong 5.0pF$, all outputs

Figure 11.

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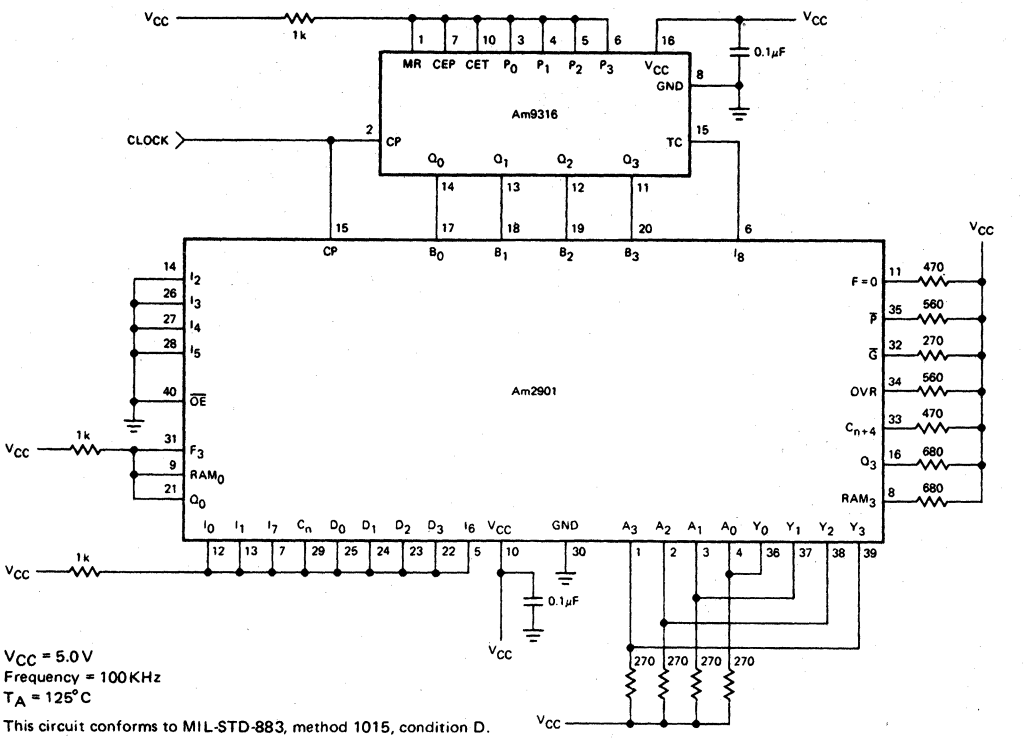
Refer to Page 13-1 for Essential Information on Military Devices

LIFE TEST AND BURN-IN CIRCUIT FOR MILITARY CLASS B PARTS.



(Contact Factory for Commercial Burn-in Conditions)

Figure 12.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

For additional information on testing, see section
"Guidelines on Testing Am2900 Family Devices"
in the Bipolar Microprocessor Logic and Interface Data Book.

Am2902A

High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries across a group of four Am2901 or Am2903 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5ns

GENERAL DESCRIPTION

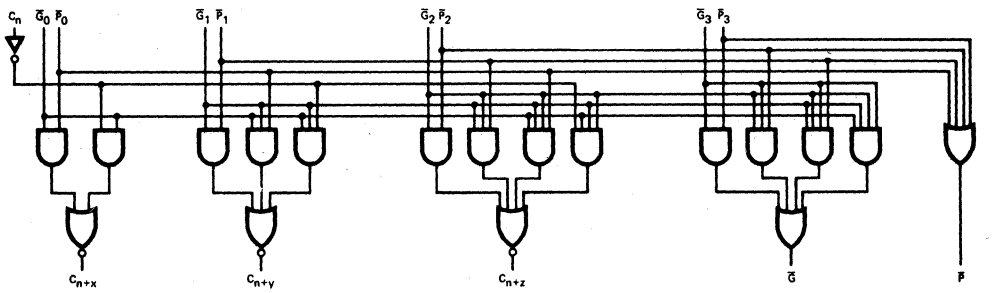
The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

BLOCK DIAGRAM



BD001680

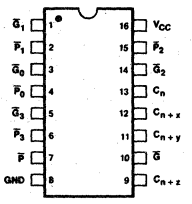
RELATED PRODUCTS

Part No.	Description
Am2901	4-Bit Microprocessor Slice
Am2903	4-Bit Microprocessor Slice
Am29203	Improved 2903
Am29501	Multiport Pipelined Processor

03595B

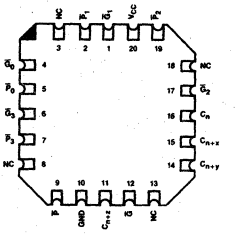
CONNECTION DIAGRAM
Top View

P-16, D-16



CD004010

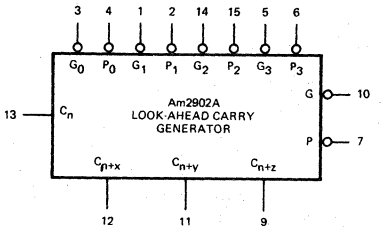
L-20-1



CD004000

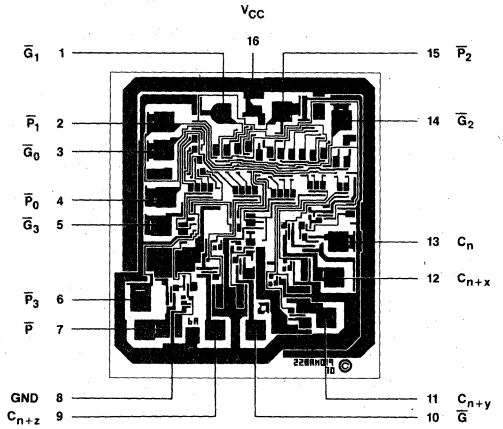
F-16 pin configuration identical to D-16, P-16.
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000850

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.062" x 0.067"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2902A **A** **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
  - X – Dice
- **A** — Speed Select
  - A – High Speed Option
- **Am2902A** — Device Type
  - Look-Ahead Carry Generator

Valid Combinations	
Am2902A	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

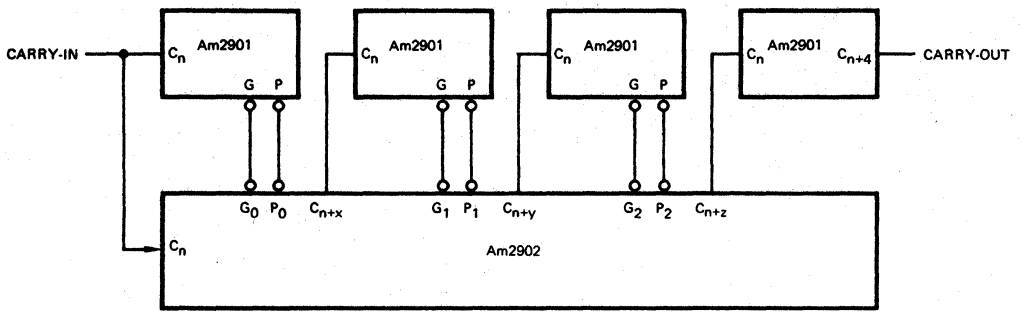
Pin No.	Name	I/O	Description
13	C_n	I	Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901 microprocessor ALU input.
12, 11, 9	C_{n+j}	O	Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n + 1, n + 2 and n + 3 microprocessor ALU slices.
1–6, 14, 15	$\overline{G}_i$, $\overline{P}_i$	I	Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n + 1, n + 2 and n + 3 microprocessor ALU slices.
10, 7	$\overline{G}$, $\overline{P}$	O	Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X		X	X	X	X	H	H					H	
X		X	X	H	H	H	X					H	
X		H	H	H	X	H	X					H	
H		H	X	H	X	H	X					H	
X		X	X	X	X	L	X					L	
X		X	X	L	X	X	L					L	
X		L	X	X	L	X	L					L	
L		X	L	X	L	X	L					L	
	H		X		X		X						H
	X		H		X		X						H
	X		X		H		X						H
	X		X		X		H						H
	L		L		L		L						L

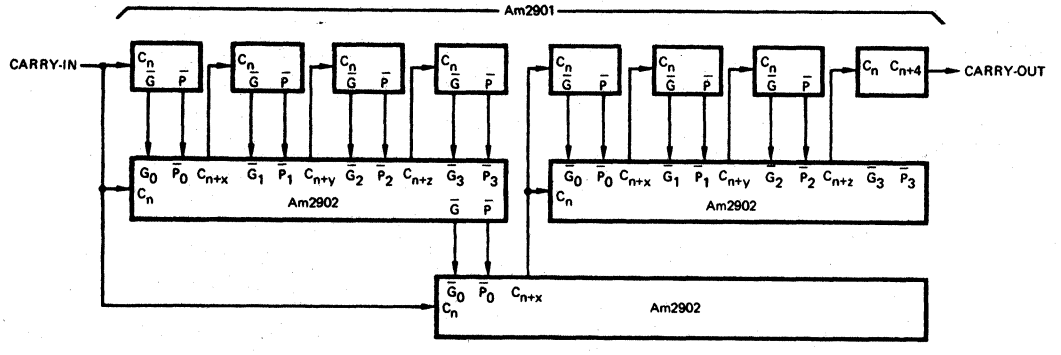
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

APPLICATIONS



AF001331

16-BIT CARRY LOOK-AHEAD CONNECTION.



AF001321

32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature with
Applied Powers ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$			−8	
			$\overline{G}_0$, $\overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	C_n			50	µA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$			200	
			$\overline{G}_0$, $\overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX All Outputs HIGH	MIL		35		mA
			COM'L		35		

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}	$C_L = 15$ pF, $R_L = 280\ \Omega$		6.5	10	ns
t_{PHL}				7	10.5	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}			4.5	7	ns
t_{PHL}				4.5	7	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$			5	7.5	ns
t_{PHL}				7	10.5	
t_{PLH}	$\overline{P}_i$ to $\overline{P}$			4.5	6.5	ns
t_{PHL}				6.5	10	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am2902A Min	COMMERCIAL Am2902A Max	MILITARY Am2902A Min	MILITARY Am2902A Max	Units
t_{PLH}	C_n to C_{n+x}, C_{n+y} or C_{n+z}	$C_L = 50$ pF, $R_L = 280\ \Omega$		13		15	ns
t_{PHL}				14		16.5	ns
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}			8		9.5	ns
t_{PHL}				9		11.5	ns
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$			12		16.5	ns
t_{PHL}				12		13.5	ns
t_{PLH}	$\overline{P}_i$ to $\overline{P}$			9.5		11.5	ns
t_{PHL}				11		12	ns

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am2903A

Four-Bit Bipolar Microprocessor Slice

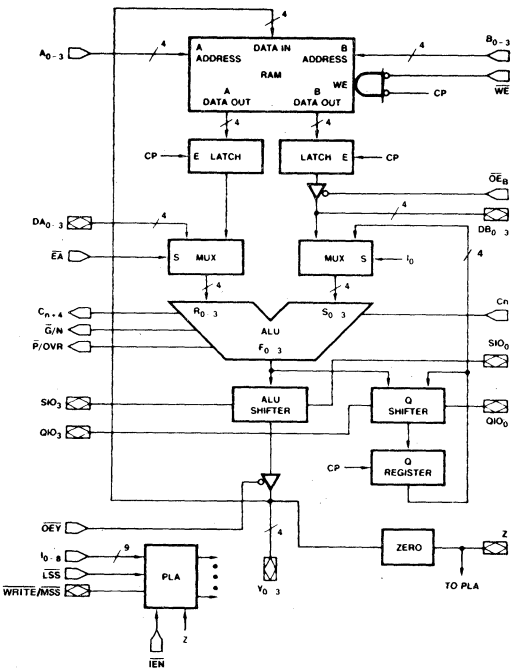
DISTINCTIVE CHARACTERISTICS

- **Expandable Register File –**
  The Am2903A includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Parity Generation and Sign Extension Circuitry –**
  Can supply parity across the entire ALU output and provide sign extension at any slice boundary.
- **Built-in Division Logic –**
  Executes non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic –**
  The mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- **Built-in Multiplication and Division Logic –**
  Performs unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.

GENERAL DESCRIPTION

The Am2903A is a four-bit expandable bipolar microprocessor slice. The Am2903A performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903A. In addition to its complete arithmetic and logic instruction set, the Am2903A provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903A is identical to the Am2903A but up to 30% faster.

BLOCK DIAGRAM



BD002784

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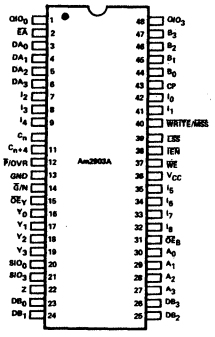
03579B

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am29705A	Two-Port RAM
Am27S35	Registered PROM

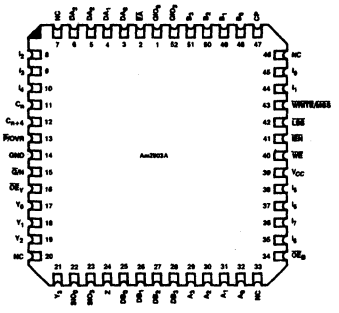
CONNECTION DIAGRAM
Top View

DIP
D-48-1
F-48-1



CD004291

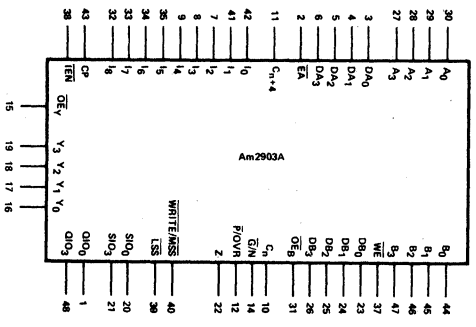
Leadless Chip Carrier
L-52-1



CD004281

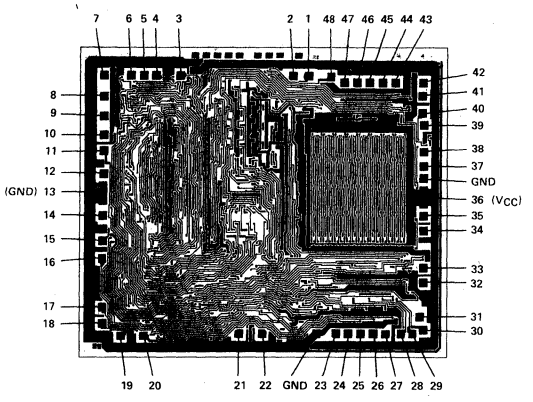
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000910

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163″ x 0.197″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2903A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 48-pin CERDIP
  - F – 48-pin flatpak
  - L – 52-pin leadless chip carrier
  - X – Dice
- **Am2903A** — Device Type
  - Four-Bit Microprocessor Slice

Valid Combinations	
Am2903A	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
	B_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
37	$\overline{WE}$	I	The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
	DA_{0-3}	I	A four-bit external data input which can be selected as one of the Am2903A ALU operand sources; DA_0 is the least significant bit.
2	$\overline{EA}$	I	A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
	DB_{0-3}	I/O	A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
31	$\overline{OE_B}$	I	A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
10	C_n	I	The carry-in input to the Am2903A ALU.
	I_{0-8}	I	The nine instruction inputs used to select the Am2903A operation to be performed.
38	$\overline{IEN}$	I	The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. $\overline{IEN}$ also controls $\overline{WRITE}$.
11	C_{n+4}	O	This output generally indicates the carry-out of the Am2903A ALU. Refer to Table 5 for an exact definition of this pin.
14	$\overline{G}$/N	O	A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
12	$\overline{P}$/OVR	O	A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
22	Z	I/O	An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
20, 21	SIO_0, SIO_3	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
1, 48	QIO_0, QIO_3	I/O	Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.
39	$\overline{LSS}$	I	An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903A array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}$/MSS pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
40	$\overline{WRITE}$/ MSS	I/O	When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}$/MSS is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
	Y_{0-3}	I/O	Four data inputs/outputs of the Am2903A. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
15	$\overline{OE_Y}$	I	A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
43	CP	I	The clock input to the Am2903A. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE Am2903A

The Am2903A is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903A allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am2903A is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE_B}$ three-state output enable, RAM data can be read directly at the Am2903A DB (I/O) port.

External data at the Am2903A Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903A high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE_B}$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during

some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903A ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E_A}$, $\overline{OE_B}$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903A executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903A executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

TABLE 1. ALU OPERAND SOURCES

$\overline{E_A}$	I_0	$\overline{OE_B}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. Am2903A ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU FUNCTIONS
L	L	L	L	0	I_0 = L: Special Functions; I_0 = H: F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 plus C_n
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n
L	L	H	H	3	F = R Plus S Plus C_n
L	H	L	L	4	F = S Plus C_n
L	H	L	H	5	F = $\overline{S}$ Plus C_n
L	H	H	L	6	F = R Plus C_n
L	H	H	H	7	F = $\overline{R}$ Plus C_n
H	L	L	L	8	F_i = LOW
H	L	L	H	9	$F_i = \overline{R}_i$ AND S_i
H	L	H	L	A	$F_i = R_i$ EXCLUSIVE NOR S_i
H	L	H	H	B	$F_i = R_i$ EXCLUSIVE OR S_i
H	H	L	L	C	$F_i = R_i$ AND S_i
H	H	L	H	D	$F_i = R_i$ NOR S_i
H	H	H	L	E	$F_i = R_i$ NAND S_i
H	H	H	H	F	$F_i = R_i$ OR S_i

L = LOW H = HIGH i = 0 to 3

Am2903As may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903As are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, G, and carry propagate, P, signals required for a lookahead carry scheme are generated by the Am2903A and are available as outputs of the least significant and intermediate slices.

The Am2903A also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903A instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903A ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903A applications section for a more detailed description of the Am2903A sign extension and parity generation/checking capability.

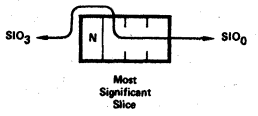
The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903A executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

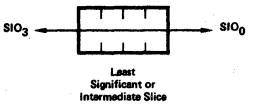
The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q

Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Figure A.
Am2903A Arithmetic Shift Path

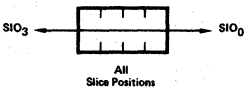


DF000430



DF000410

Am2903A Logical Shift Path



DF000420

Double-length arithmetic and logical shifting capability is provided by the Am2903A. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903A special functions and the operations which the Q Register and shifter perform for each. When the Am2903A executes instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high impedance state when $\overline{OE_Y}$ is HIGH. The DB output buffers are enabled when the $\overline{OE_B}$ input is LOW.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, $\overline{IEN}$ = LOW.

					SIO_3		Y_3		Y_2								
I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \nabla F_2 \nabla F_1 \nabla F_0 \nabla SIO_3$
∇ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0$ = LOW (Note 4)

(Hex) $I_8I_7I_6I_5$	Special Function	ALU Function	ALU Shifter Function	SIO_3		SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
				Most Sig Slice	Other Slices					
0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 1)	Hi-Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
1	(Note 5)									
2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
3	(Note 5)									
4	Increment by One or Two	$F = S + 1 + C_n$	$F \rightarrow Y$	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
5	Sign/Magnitude Two's Complement	$F = \overline{S} + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	$F \rightarrow Y$ (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
6	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
7	(Note 5)									
8	Single Length Normalize	$F = S + C_n$	$F \rightarrow Y$	F_3	F_3	Hi-Z	Log $2Q \rightarrow Q$	Q_3	Input	L
9	(Note 5)									
A	Double Length Normalize and First Divide Op	$F = S + C_n$	Log $2F \rightarrow Y$	$R_3 \nabla F_3$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
B	(Note 5)									
C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $2F \rightarrow Y$	$\overline{R_3 \nabla F}$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
D	(Note 5)									
E	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	$F \rightarrow Y$	F_3	F_3	Hi-Z	Log $2Q \rightarrow Q$	Q_3	Input	L
F	(Note 5)									

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \nabla$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \nabla F_3$ is generated at the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Not valid.

L = LOW
H = HIGH
X = Don't Care
Hi-Z = High Impedance
∇ = Exclusive OR
Parity = $SIO_3 \nabla F_3 \nabla F_2 \nabla F_1 \nabla F_0$

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903A instructions.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}$/$\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903A instruction inputs.

On the Am2903A, when $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903A instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903A divide operation (see Figure B).

Programming the Am2903A Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}$/$\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}$/$\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}$/$\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{WRITE}$/$\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{WRITE}$/$\overline{MSS}$ and $\overline{LSS}$ should not be connected together.

TABLE 5. Am2903A STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z($\overline{OE}_Y$ = LOW)		
						Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Intermediate Slice	Least Sig Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	(Note 6)									
1	8	L	(Note 6)									
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)									
4	0	L	(Note 1)	(Note 2)	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	$\overline{S}_i$ if Z = L S_i if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \nabla S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$\overline{S}_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	(Note 6)									
8	0	L	0	S_i	(Note 3)	$Q_2 \nabla Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	(Note 6)									
9	8	L	(Note 6)									
A	0	L	0	S_i	(Note 4)	$F_2 \nabla F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)									
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)									
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	G v PC_n	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)									

Notes:1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \nabla Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \nabla F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$.
6. Not valid.

L = LOW = 0
H = HIGH = 1
v = OR
$\wedge$ = AND
∇ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

Am2903A SPECIAL FUNCTIONS

The Am2903A provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903A. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

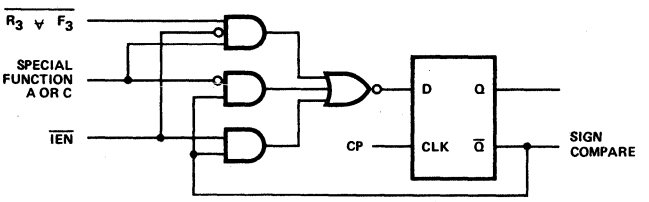
The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903A applications section for a more detailed description of these Special Functions.

Figure B. Sign Compare Flip-Flop



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The sign compare signal appears at the Z output of the most significant slice during special functions C and E. Refer to Table 5.

CYCLE TIMES FOR 16-BIT SYSTEM FOR COMMON OPERATIONS

The illustration below shows a typical configuration using 4 Am2903A Superslices, an Am2902A carry lookahead chip, and the Am2904 for shift multiplexers, status registers, and carry-in control. For the system enclosed within the dashed lines, there are four major switching paths whose values for various kinds of cycles are summarized below, and shown on the timing waveform.

1. MICROCYCLE TIME (TCHCH).
   The minimum time which must elapse between a LOW-TO-HIGH clock transition and the next LOW-TO-HIGH clock transition.
2. DATA SET-UP TIME (TDVCH).
   The minimum time which must be allowed between valid, stable data on the D inputs and the clock LOW-TO-HIGH transition.
3. D TO Y (TDVYV).
   The maximum time required to obtain valid Y output data after the D inputs are valid. This is the combinational delay through the parts from D to Y.
4. CP TO Y (TCHYV).
   The maximum time required to obtain valid Y outputs after a clock LOW-TO-HIGH transition.

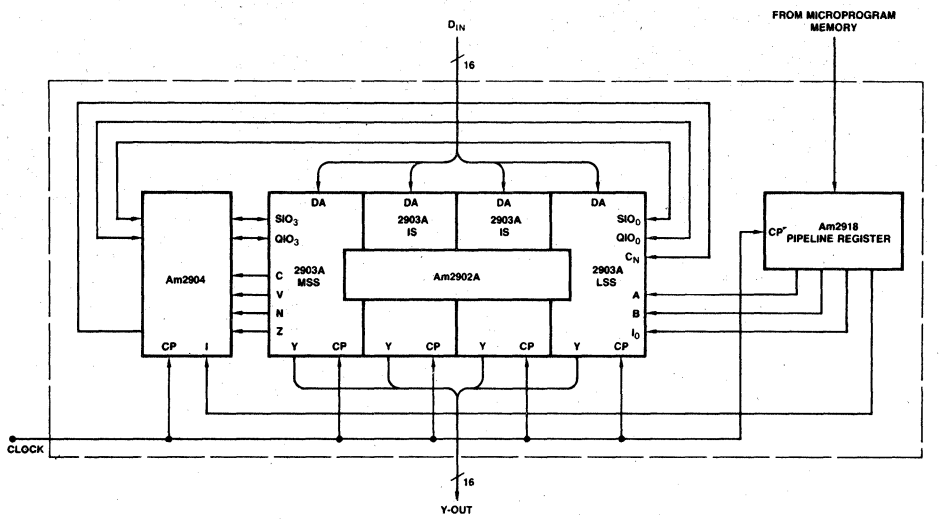
The types of cycles for which data is summarized are as follows:

1. Logic – Any logical operation without a shift.
2. Logic Rotate – Any logic operation with a rotate or shift.
3. Arithmetic – An add or subtract with no shift.
4. Multiply – The first cycle of a 2's complement multiply instruction. Subsequent cycles require less time.
5. Divide – The iterative divide cycle. The first divide instruction and the last divide (correction) instruction require less time.

Time in ns Over Commercial Operating Range

CYCLE	TCHCH	TDVCH	TDVYV	TCHYV
LOGIC	99	79	59	81
LOGIC ROTATE	118	99	79	98
ARITHMETIC	130	109	91	112
MULTIPLY	152	113	95	135
DIVIDE	139	113	95	121

16-Bit System with Am2903A, Am2902A, Am2904



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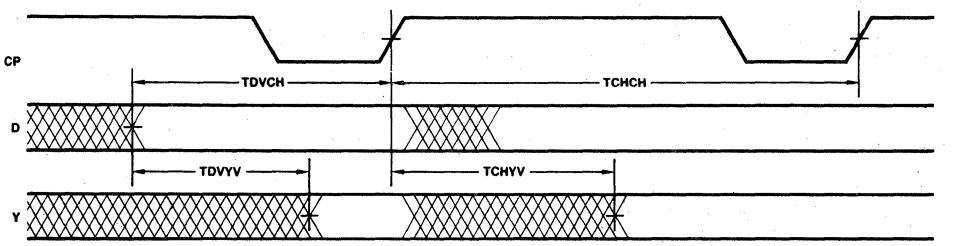
Timing Waveforms for Data in, Clock, and Y Out



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

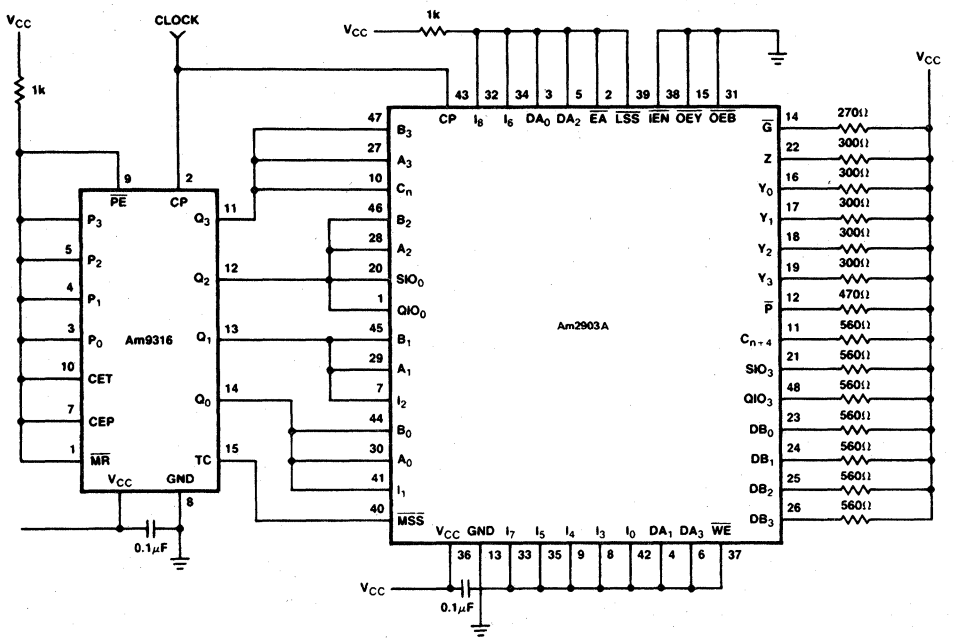
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N	2.4			Volts
				I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}	2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN, V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or = V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V (Note 4)		C_n			−3.6	mA
				Y_0, Y_1, Y_2, Y_3			−1.13	
				I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3			−0.72	
				SIO_0, SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1 DB_2, DB_3			−0.77	
				All other inputs			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V (Note 4)		C_n			200	μA
				Y_0, Y_1, Y_2, Y_3			110	
				I_0-I_4, DA_0-DA_3			40	
				SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$			90	
				All other inputs			20	

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX, (Note 4)	Y_0–Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			–1130	
			DB_{0-3}, QIO_0, $\overline{QIO_3}$, SIO_0, SIO_3, $\overline{WRITE/MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			–770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V, V_O = 0.5V			-30		-85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = –55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

Am2903A Burn-in and Life Test Circuit



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I. Am2903A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The Am2903A switching characteristics are a function of the power supply voltage, the temperature, and the operating mode of the devices. The data has been condensed onto the tables below. All numbers in the tables are in ns.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable to
A	Clock and Write Pulse	4.75 to 5.25V, 0 to 70°C	All Functions
B	Enable/Disable Times	4.75 to 5.25V, 0 to 70°C	All Functions
C	Setup and Hold Times	4.75 to 5.25V, 0 to 70°C	All Functions
1-2	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Standard Function and Increment by 1 or 2
1-3	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Multiply Instructions
1-4	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Divide Instructions
1-5	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Sign Magnitude to Two's Complement Conversion
1-6	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Single Length Normalization

I-1. Am2903A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the Am2903A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE A. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

TABLE B. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
$\overline{OEY}$	Y	25	21
$\overline{OEB}$	DB	25	21
$\overline{OEA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
I_{8765}	QIO	38	38
I_{43210}	QIO	38	38
$\overline{LSS}$	$\overline{WR}$	25	21

Note: C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE C. SETUP AND HOLD TIMES ALL FUNCTIONS

		HIGH-to-LOW		LOW-to-HIGH		
		Tpwl				
From	With Respect to	Setup	Hold	Setup	Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q (Note 1)
$\overline{WE}$ High	CP	15	Tpwl		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
$QIO_{0,\ 3}$	CP	Don't Care	Don't Care	17	3	Shift Q
I_{8765}	CP	12	–	20	0	Write into Q (Note 2)
$\overline{IEN}$ High	CP	–			0	Prevent Writing into Q
$\overline{IEN}$ Low	CP	Don't Care	Don't Care	21	0	Write into Q
I_{43210}	CP	18	–	32	0	Write into Q (Note 2)

Note 1: The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OEY}$ = 0).

Note 2: The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.

Note 3: For all other set up conditions not specified in this table, the set up time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this set up condition ensures valid writing into the Q register and sign compare flip flop.

Note 4: $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.

Note 5: A and B addresses must be set-up prior to the clock HIGH-to-LOW transition to latch data at the RAM output.

Note 6: Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.

Note 7: Because I_{8765} controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.

Note 8: The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210} relative to the clock LOW-to-HIGH transition is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified.

I-2 STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

From	To											
	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/ $\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	67	55	52	74	61	67	28	–	–	41	62	78
DA, DB	58	50	40	65	54	58	–	–	–	35	59	65
Cn	33	18	–	35	28	26	–	–	–	23	30	38
I_{8-0}	64	64	50	72	61	62	–	34	26	50	62	74
CP	58	42	43	61	54	58	22	–	22	37	54	60
$SIO_{0,3}$	23	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	44	44	44

Notes: 1. A "–" means the delay path does not exist.

Standard Functions: See Table 2

Increment SF 4: F = S + 1 + Cn
Y → Z = 17($\overline{OEY}$ = H)
$\overline{IEN}$ → $\overline{WRITE}$/ $\overline{MSS}$ = 20
$\overline{EA}$ → OUTPUT = DA → OUTPUT

I-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To										
	Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/ $\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	67	55	–	–	61	67	28	–	–	41
	IS	67	55	52	–	–	–	28	–	–	41
	LSS	67	55	52	–	–	–	28	–	–	41
DA, DB	MSS	58	50	–	–	54	58	–	–	–	35
	IS	58	50	40	–	–	–	–	–	–	35
	LSS	58	50	40	–	–	–	–	–	–	35
Cn	MSS	35	18	–	–	28	27	–	–	–	23
	IS	33	18	–	–	–	–	–	–	–	23
	LSS	33	18	–	–	–	–	–	–	–	23
I_{8-0}	MSS	94	75	–	–	88	88	–	–	26	73
	IS	94	75	71	–	–	–	–	–	26	73
	LSS	94	75	71	30	–	–	–	34	26	73
CP	MSS	58	42	–	–	54	58	22	–	22	37
	IS	58	42	43	–	–	–	22	–	22	37
	LSS	90	71	67	26	–	–	22	–	22	69
Z	MSS	64	45	–	–	58	58	–	–	–	43
	IS	64	45	41	–	–	–	–	–	–	43
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

Unsigned Multiply

SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply

SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle

SF 6: F = S + Cn if Z = 0
F = S – R – 1 + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
Y_3 = OVR ⊕ (MSS)
$Z = Q_0$ (LSS)

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified.

I-4 DIVIDE INSTRUCTIONS (SF A, SF C, SF E)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	67	61/55	–	74/–	61	67	28	–	–	62
	IS	67	55	52	74/–	–	–	28	–	–	62
	LSS	67	55	52	74/–	–	–	28	–	–	62
DA, DB	MSS	58	55/50	–	65/–	54	58	–	–	–	59
	IS	58	50	40	65/–	–	–	–	–	–	59
	LSS	58	50	40	65/–	–	–	–	–	–	59
Cn	MSS	33	33/18	–	35/–	28	27	–	–	–	32
	IS	33	18	–	35/–	–	–	–	–	–	30
	LSS	33	18	–	35/–	–	–	–	–	–	30
I_{8-0}	MSS	64/84	75/68	–	72/29	61/77	62/77	–	–	26	63/83
	IS	64/84	64/68	50/70	72/–	–	–	–	–	26	62/83
	LSS	64/84	64/68	50/70	72/–	–	–	–	34	26	62/83
CP	MSS	58/80	46/64	–	61/25	54/66	58/66	22	–	22	54/79
	IS	58	42	43	61/–	–	–	22	–	22	54
	LSS	58	42	43	61/–	–	–	22	–	22	54
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
	LSS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

Double Length Normalize and First Divide Op

SF A: $F = S + Cn$
$Y = \text{Log. } F/2$
$Q = \text{Log. } Q/2$
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{F_0}\ \overline{F_1}\ \overline{F_2}\ \overline{F_3}$

Two's Complement Divide

SF C: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
$Y = \text{Log. } F/2$
$Q = \text{Log. } Q/2$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder

SF E: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
$Y = F$
$Q = \text{Log. } Q/2$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified.

I-5 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/$\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	81	–	42	89	89	28	–		102
	IS	67	55	52	–	–	–	28	–		78
	LSS	67	55	52	–	–	–	28	–		78
DA, DB	MSS	94	76	–	37	84	84	–	–		97
	IS	58	50	40	–	–	–	–	–		65
	LSS	58	50	40	–	–	–	–	–		65
Cn	MSS	33	18	–	–	32	27	–	–		38
	IS	33	18	–	–	–	–	–	–		38
	LSS	33	18	–	–	–	–	–	–		38
I_{8-0}	MSS	85	67	–	28	82	73	–	–	26	88
	IS	85	67	63	–	–	–	–	–	26	88
	LSS	85	67	63	–	–	–	–	34	26	88
CP	MSS	94	76	–	37	84	84	22	–	22	97
	IS	58	42	43	–	–	–	22	–	22	60
	LSS	58	42	43	–	–	–	22	–	22	60
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	57	39	35	–	–	–	–	–	–	60
	LSS	57	39	35	–	–	–	–	–	–	60
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

SF 5: $F = \overline{S} + Cn$ if $Z = 0$
$F = \overline{S} + Cn$ if $Z = 1$

$Y_3 = S_3 \oplus F_3$ (MSS)
$\overline{Z} = S_3$ (MSS)

$Q = Q$
$N = F_3$ if $Z = 0$
$N = F_3 \oplus S_3$ if $Z = 1$

I-6 SINGLE LENGTH NORMALIZATION (SF 8)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/$\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	67	–	–	–	–	–	28	–	–	62
	IS	67	55	52	–	–	–	28	–	–	62
	LSS	67	55	52	–	–	–	28	–	–	62
DA, DB	MSS	58	–	–	–	–	–	–	–	–	59
	IS	58	50	40	–	–	–	–	–	–	59
	LSS	58	50	40	–	–	–	–	–	–	59
Cn	MSS	33	–	–	–	–	–	–	–	–	30
	IS	33	18	–	–	–	–	–	–	–	30
	LSS	33	18	–	–	–	–	–	–	–	30
I_{8-0}	MSS	64	37	–	29	24	24	–	–	26	62
	IS	64	64	50	29	–	–	–	–	26	62
	LSS	64	64	50	29	–	–	–	34	26	62
CK	MSS	58	29	–	26	26	29	22	–	22	54
	IS	58	42	43	26	–	–	22	–	22	54
	LSS	58	42	43	26	–	–	22	–	22	54
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

SF 8: $F = S + Cn$
$N = Q_3$ (MSS)
$Y = F$
$Q =$ Log. $Q/2$

$C_{n+4} = \overline{Q_3} \oplus Q_2$ (MSS)
$\overline{Z} = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$

$OVR = Q_2 \oplus Q_1$ (MSS)

II. Am2903A GUARANTEED MILITARY RANGE PERFORMANCE

The Am2903A switching characteristics are a function of the power supply voltage, the temperature, and the operating mode of the devices. The data has been condensed onto the tables below. All numbers are in ns.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable to
A	Clock and Write Pulse	4.75 to 5.25V, 0 to 70°C	All Functions
B	Enable/Disable Times	4.75 to 5.25V, 0 to 70°C	All Functions
C	Setup and Hold Times	4.75 to 5.25V, 0 to 70°C	All Functions
1-2	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Standard Function and Increment by 1 or 2
1-3	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Multiply Instructions
1-4	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Divide Instructions
1-5	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Sign Magnitude to Two's Complement Conversion
1-6	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Single Length Normalization

II-1. Am2903A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the Am2903A over the military operating range of 0 to + 70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE A. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and WE both Low to Write	30ns

TABLE B. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
$\overline{OEY}$	Y	25	21
$\overline{OEB}$	DB	25	21
$\overline{OEA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
I_{8765}	QIO	38	38
I_{43210}	QIO	38	35
$\overline{LSS}$	$\overline{WR}$	30	25

Note: C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE C. SETUP AND HOLD TIMES ALL FUNCTIONS

		HIGH-to-LOW		LOW-to-HIGH		
		Tpwl				
From	With Respect to	Setup	Hold	Setup	Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q (Note 1)
$\overline{WE}$ High	CP	15	Tpwl		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
I_{8765}	CP	12	–	20	0	Write into Q (Note 2)
$\overline{IEN}$ High	CP	24			0	Prevent Writing into Q
$\overline{IEN}$ Low	CP	Don't Care	Don't Care	21	0	Write into Q
I_{43210}	CP	18	–	32	0	Write into Q (Note 2)

Note 1: The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OEY}$ = 0).

Note 2: The set-up time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.

Note 3: For all other set up conditions not specified in this table, the set up time should be the delay to stable Y output, plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this set up condition ensures valid writing into the Q register and sign compare flip flop.

Note 4: $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE/MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.

Note 5: A and B addresses must be set-up prior to the clock HIGH-to-LOW transition to latch data at the RAM output.

Note 6: Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.

Note 7: Because I_{8765} controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.

Note 8: The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210} relative to the clock LOW-to-HIGH transition is the longer of (1) the set-up time prior to clock L →H, and (2) the sum of the set-up time prior to clock H →L and the clock LOW time.

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified.

II-2 STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

From	To: Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	70	58	52	78	68	67	28	–	–	47	71	84
DA, DB	60	52	40	66	55	58	–	–	–	35	61	74
Cn	35	19	–	41	31	29	–	–	–	23	33	40
I_{8-0}	72	69	56	80	71	69	–	36	26	58	75	89
CP	60	42	43	67	55	58	22	–	25	41	61	66
$SIO_{0,3}$	26	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	44	44	44

Notes: 1. A "–" means the delay path does not exist.

Standard Functions: See Table 2

Increment SF 4: F = S + 1 + Cn
Y → Z = 17($\overline{OEY}$ = H)
$\overline{IEN}$ → $\overline{WRITE}/\overline{MSS}$ = 20
EA → OUTPUT = DA → OUTPUT

II-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	72	58	–	–	68	67	28	–	–	47
	IS	72	58	52	–	–	–	28	–	–	47
	LSS	72	58	52	–	–	–	28	–	–	47
DA, DB	MSS	62	52	–	–	55	58	–	–	–	35
	IS	60	52	40	–	–	–	–	–	–	35
	LSS	60	52	40	–	–	–	–	–	–	35
Cn	MSS	40	19	–	–	31	29	–	–	–	23
	IS	35	19	–	–	–	–	–	–	–	23
	LSS	35	19	–	–	–	–	–	–	–	23
I_{8-0}	MSS	108	84	–	–	98	98	–	–	26	81
	IS	108	84	80	–	–	–	–	–	26	81
	LSS	108	84	80	33	–	–	–	36	26	81
CP	MSS	62	42	–	–	55	58	22	–	25	41
	IS	60	42	43	–	–	–	22	–	25	41
	LSS	104	80	74	29	–	–	22	–	25	77
Z	MSS	75	51	–	–	65	65	–	–	–	48
	IS	75	51	47	–	–	–	–	–	–	48
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

Unsigned Multiply

SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)
Y = Log. F/2
Q = Log. Q/2

Two's Complement Multiply

SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)
Y = Log. F/2
Q = Log. Q/2

Two's Complement Multiply Last Cycle

SF 6: F = S + Cn if Z = 0
F = S – R – 1 + Cn if Z = 1
$Y_3 = OVR \oplus F_3$ (MSS)
$Z = Q_0$ (LSS)
Y = Log. F/2
Q = Log. Q/2

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified.

II-4 DIVIDE INSTRUCTION (SF A, SF C, SF E)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	70	72/58	–	78/–	68	67	28	–	–	71
	IS	70	58	52	78/–	–	–	28	–	–	71
	LSS	70	58	52	78/–	–	–	28	–	–	71
DA, DB	MSS	60	66/52	–	66/–	55	58	–	–	–	61
	IS	60	52	40	66/–	–	–	–	–	–	61
	LSS	60	52	40	66/–	–	–	–	–	–	61
Cn	MSS	35	37/19	–	41/–	31	29	–	–	–	36
	IS	35	19	–	41/–	–	–	–	–	–	33
	LSS	35	19	–	41/–	–	–	–	–	–	33
I_{8-0}	MSS	72/96	89/79	–	80/33	71/91	69/91	–	–	26	76/98
	IS	72/96	69/79	56/79	80/–	–	–	–	–	26	75/98
	LSS	72/96	69/79	56/79	80/–	–	–	–	36	26	75/98
CP	MSS	60/91	51/74	–	67/28	55/74	58/74	22	–	25	61/93
	IS	60	42	43	67/–	–	–	22	–	25	61
	LSS	60	42	43	67/–	–	–	22	–	25	61
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
	LSS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
SIO_{0-3}	Any	26	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

Double Length Normalize and First Divide Op

SF A: $F = S + Cn$
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{F_0}\ \overline{F_1}\ \overline{F_2}\ \overline{F_3}$
Y = Log. F/2
Q = Log. Q/2

Two's Complement Divide

SF C: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
Y = Log. F/2
Q = Log. Q/2
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder

SF E: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
Y = F
Q = Log. Q/2
$Z = \overline{F_3} \oplus R_3$ (MSS) from previous cycle

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified.

II-5 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/$\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	95	–	49	106	106	28	–	–	125
	IS	70	58	52	–	–	–	28	–	–	84
	LSS	70	58	52	–	–	–	28	–	–	84
DA, DB	MSS	108	89	–	43	101	101	–	–	–	119
	IS	60	52	40	–	–	–	–	–	–	74
	LSS	60	52	40	–	–	–	–	–	–	74
Cn	MSS	36	19	–	–	35	29	–	–	–	40
	IS	35	19	–	–	–	–	–	–	–	40
	LSS	35	19	–	–	–	–	–	–	–	40
I_{8-0}	MSS	98	79	–	33	97	88	–	–	26	109
	IS	98	79	73	–	–	–	–	–	26	109
	LSS	98	79	73	–	–	–	–	36	26	109
CP	MSS	108	89	–	43	101	101	22	–	25	119
	IS	60	42	43	–	–	–	22	–	25	66
	LSS	60	42	43	–	–	–	22	–	25	66
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	65	46	40	–	–	–	–	–	–	76
	LSS	65	46	40	–	–	–	–	–	–	76
$\overline{IEN}$											
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

SF 5: F = S + Cn if Z = 0
F = $\overline{S}$ + Cn if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)
Y = F

Q = Q
N = F_3; Z = 0
N = $F_3 \oplus S_3$; Z = 1

II-6 SINGLE LENGTH NORMALIZATION (SF 8)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/$\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	70	–	–	–	–	–	28	–	–	71
	IS	70	58	52	–	–	–	28	–	–	71
	LSS	70	58	52	–	–	–	28	–	–	71
DA, DB	MSS	60	–	–	–	–	–	–	–	–	61
	IS	60	52	40	–	–	–	–	–	–	61
	LSS	60	52	40	–	–	–	–	–	–	61
Cn	MSS	35	–	–	–	–	–	–	–	–	33
	IS	35	19	–	–	–	–	–	–	–	33
	LSS	35	19	–	–	–	–	–	–	–	33
I_{8-0}	MSS	72	47	–	33	27	27	–	–	26	75
	IS	72	69	56	33	–	–	–	–	26	75
	LSS	72	69	56	33	–	–	–	–	26	75
CP	MSS	60	31	–	28	26	31	22	–	25	61
	IS	60	42	43	28	–	–	22	–	25	61
	LSS	60	42	43	28	–	–	22	–	25	61
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
$SIO_{0,3}$	Any	26	–	–	–	–	–	–	–	–	–

Notes: 1. A "–" means the delay path does not exist.

SF 8: F = S + Cn
N = Q_3 (MSS)
Y = F
Q = Log. Q/2

$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$

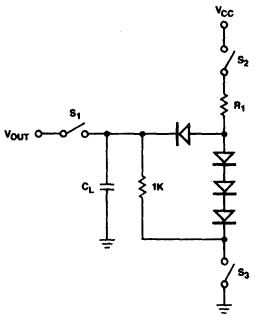
OVR = $Q_2 \oplus Q_1$ (MSS)

03579B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

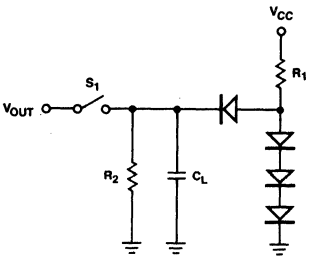
A. THREE-STATE OUTPUTS



TC001160

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS

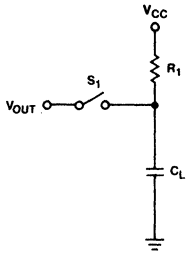


TC001150

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



TC001091

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2903A (DIP)

Pin #	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16-19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23-26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Am2904

Status and Shift Control Unit

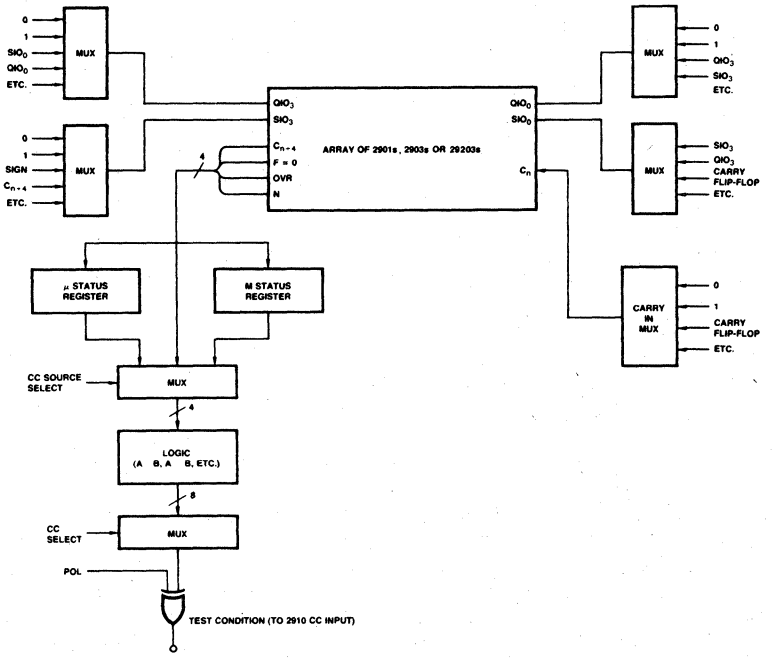
DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU –** including the Am2901, Am2903, Am29203 and MSI ALUs.
- **Generates Carry-in to the ALU –** Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers –** Connects to shift lines at the ends of an Am2901, Am2903, or Am29203 array to implement single and double length arithmetic and logical shifts and rotates – 32 different modes in all.
- **Contains two edge-triggered status registers –** Use for foreground/background registers in controllers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip –** Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

GENERAL DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the storage registers or directly from the ALU.

BLOCK DIAGRAM



BASIC FEATURES OF Am2904 BD001852

All the logic shown except the array of 2901s, 2903s, or 29203s is contained in the Am2904.

03582B

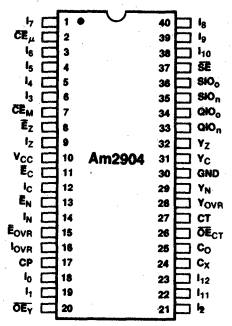
RELATED PRODUCTS

Part No.	Description
Am2901	4-Bit Microprocessor Slice
Am2903	Advanced 4-Bit Bipolar Microprocessor Slice
Am29203	4-Bit Bipolar Microprocessor Slice
Am2910	Microprogram Controller
Am29811	Next Address Control Unit for 2909A/11A

For additional applications refer to Chapter 4 of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

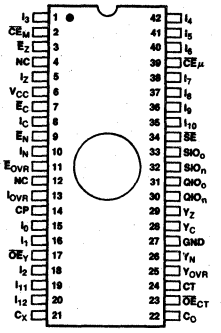
CONNECTION DIAGRAM
Top View

D-40



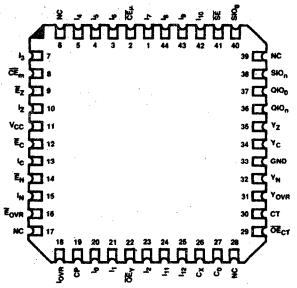
CD004130

F-42-1



CD004140

Chip-Pak™ L-44-1

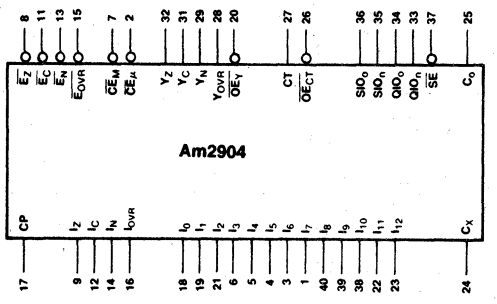


CD004150

Note: Pin 1 is marked for orientation

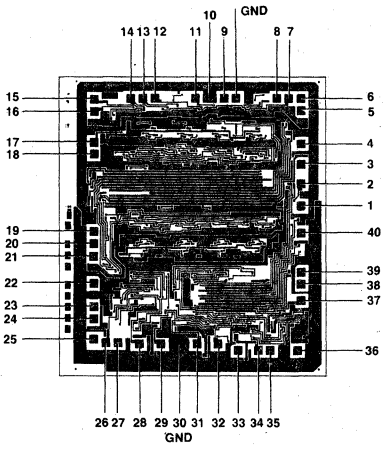
NC = No Connection.

LOGIC SYMBOL
(DIP)



LS000872

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.140″ x 0.161″
Pad Numbers correspond to DIP pinout

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2904 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 40-pin CERDIP
  - F – 42-pin flatpak
  - L – 44-pin leadless chip carrier
  - X – Dice
- **Am2904** — Device type
  - Status and Shift Control Unit

Valid Combinations	
Am2904	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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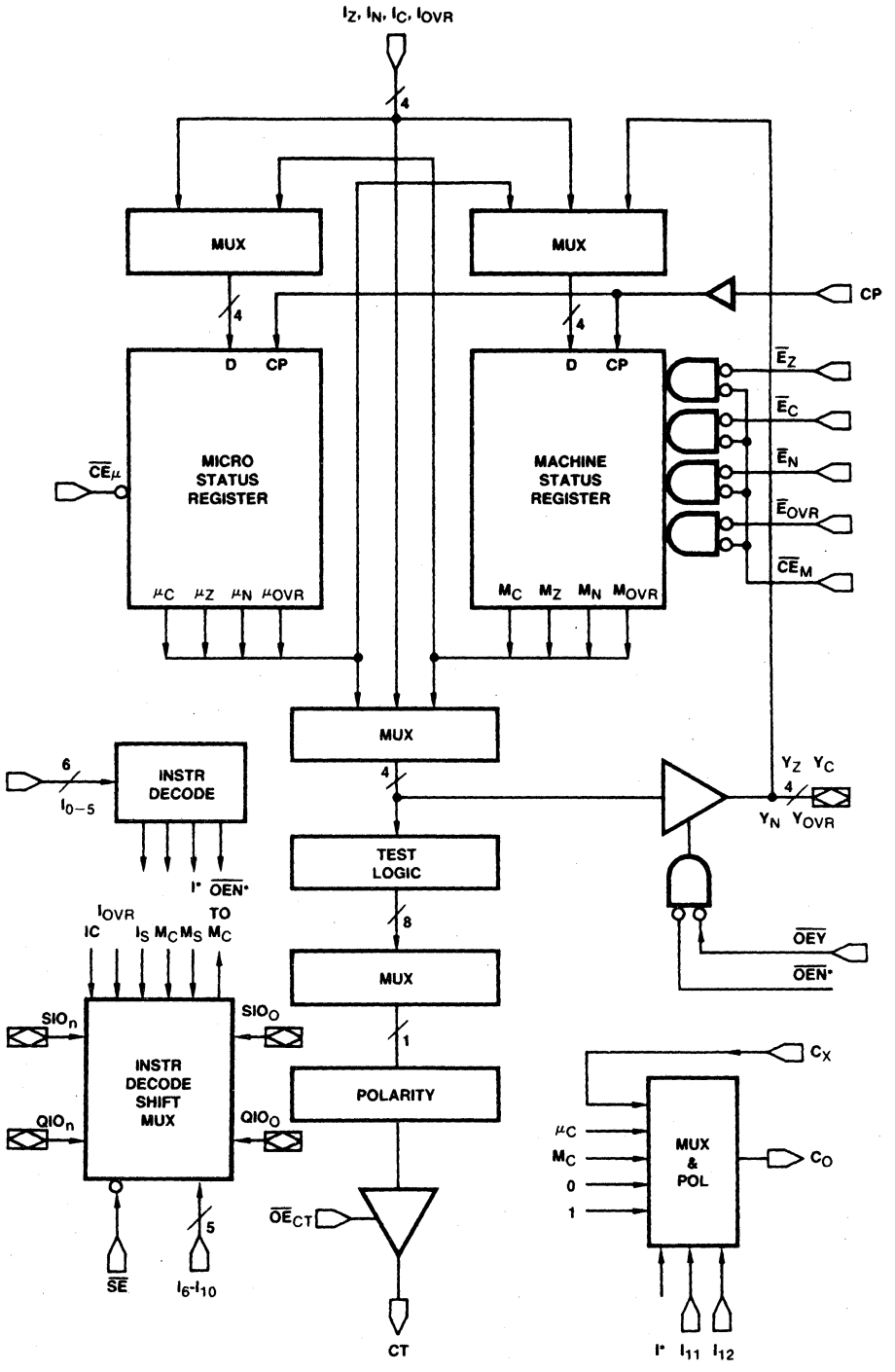
BLOCK DIAGRAM



*INTERNAL

BD001840

PIN DESCRIPTION

Pin No.	Name	I/O	Description
9	I_Z	I	Zero status input pin, intended for connection to the Z outputs of the Am2903 or the F = 0 outputs of the Am2901.
12	I_C	I	Carry status input pin, intended for connection to the C_{n+4} output of the most significant ALU slice.
14	I_N	I	Sign status input pin, intended for connection to the most significant ALU slice. The connection is to the N pin on the Am2903, and the F_3 pin on the Am2901.
16	I_{OVR}	I	Overflow status input pin, intended for connection to the OVR pin on the most significant ALU slice.
	I_{0-12}	I	The thirteen instruction pins which select the operation the Am2904 is to perform.
7	$\overline{CE_M}$	I	This pin, used in conjunction with $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ acts as the overall enable for the Machine Status Register. When the pin is LOW, MSR bits may be modified, according to the states of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$. When HIGH, the MSR will retain the present state, regardless of the state of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.
8, 11, 13, 15	$\overline{E_Z}$, $\overline{E_C}$ $\overline{E_N}$, $\overline{E_{OVR}}$	I	These pins, when LOW, enable the corresponding bits in the Machine Status Register. When HIGH, they will prevent the corresponding bits from changing state. By using these pins together with the $\overline{CE_M}$ pin, MSR bits can be selectively modified.
2	$\overline{CE_\mu}$	I	This pin, when LOW, enables all four bits of the Micro Status Register. When this pin is HIGH, the μSR will not change state.
32, 31, 29, 28	Y_Z, Y_C, Y_N, Y_{OVR}	I/O	These pins form a three-state bidirectional bus over which MSR and μSR status can be read out or the MSR can be loaded in parallel.
20	$\overline{OE_Y}$	I	When LOW, this pin enables the Y pins as outputs. When HIGH, the Y outputs are in the high impedance state.
27	CT	O	The conditional test output. The output of the Condition Code multiplexer appears here.
26	$\overline{OE_{CT}}$	I	When this pin is LOW, the CT pin is active. When HIGH the CT pin is in the high impedance state.
36, 35, 34, 33	SIO_0, SIO_n QIO_0 QIO_n	I/O	These pins complete the linking for the various shift and rotate conditions. SIO_0 is intended for connection to the SIO_0 pin of the least significant Am2903 slice (RAM_0 for Am2901). SIO_n connects to the SIO_3 pin of the most significant Am2903 slice, (RAM_3 for Am2901). QIO_0 connects to the QIO_0 pin of the least significant Am2903 slice (QIO_0 for Am2901) and QIO_n connects to the QIO_3 pin of the most significant Am2903 slice (Q_3 for Am2901).
37	$\overline{SE}$	I	This pin controls the state of the shift outputs. When LOW, the shift outputs are enabled. When HIGH, the shift outputs are in the high impedance state.
25	C_0	O	This pin is the output of the Carry-In Control Multiplexer. It connects to the C_n input of the least significant ALU slice, and the C_n input of the Am2902A.
24	C_X	I	This pin is used as an input to the Carry-In Control Multiplexer which can route it to the C_0 pin. The C_X pin is intended for connection to the Z output of the Am2903 to facilitate some of the Am2903 special instructions.
17	CP	I	The clock input to the device. The μSR and MSR are modified on the LOW to HIGH transition of the clock input. All other portions of the Am2904 are combinational and are unaffected by CP.

Am2904 ARCHITECTURE

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control. The architecture and instruction codes have been designed to complement the flexibility of the 2900 Family.

Status Register

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled. The registers use edge-triggered D-type flip-flops which change state on the LOW to HIGH transition of the Clock Input.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control ($I_{0\text{-}5}$). The bits in the μSR can also be individually set or reset under instruction control ($I_{0\text{-}5}$). When the $\overline{CE_\mu}$ input is HIGH, the μSR is inhibited from changing, independent of the $I_{0\text{-}5}$ inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR, and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control ($I_{0\text{-}5}$). The MSR can also be set, reset or complemented under instruction control ($I_{0\text{-}5}$). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E_Z}$, $\overline{E_N}$, $\overline{E_C}$, $\overline{E_{OVR}}$) and the $\overline{CE_M}$ input. A LOW on both the $\overline{CE_M}$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input prevents the corresponding bit changing in the MSR. A HIGH on $\overline{CE_M}$ prevents any bits changing in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allows the MSR to be loaded from the system data bus. This capability is used to save and restore the status registers during certain subroutines and when servicing interrupts.

Condition Code Multiplexer

The Condition Code Multiplexer output, CT, can be selected from 16 different functions. These include the true and complemented state of each of the status bits and combinations of these bits to detect such conditions as "greater than", "greater than or equal to", "less than" or "less than or equal to" for unsigned or two's complement numbers.

The Am2904 can perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910 and is provided with an output enable, $\overline{OE_{CT}}$ to make the addition of other condition inputs to this point easy.

Shift Linkage Multiplexer

The Shift Linkage Multiplexer generates the necessary linkages to allow the ALU to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates, with and without carry (M_C), are provided. When the $\overline{SE}$ input is HIGH, the four input/output pins (SIO_0, SIO_n, QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0, QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0 and Q_3 pins of the AM2901 or the SIO_0, SIO_3, QIO_0, QIO_3 pins of the Am2903.

Carry-In Control Multiplexer

The Carry-In Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu_C}$, $\overline{M_C}$). These functions allow easy implementation of both single length and double length addition and subtraction. The C_X input is intended to be connected to the Z output of the Am2903 to facilitate execution of some of the Am2903 special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901 or Am2903 and the C_n pin of the Am2902A.

Am2904 INSTRUCTION SET

The Am2904 is controlled by manipulating the 13 instruction lines, $I_{0\text{-}12}$, together with the nine enable lines, $\overline{CE_M}$, $\overline{CE_\mu}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, $\overline{SE}$. Most systems will save on microword bits by tying some of these lines to a fixed level or by connecting certain lines together, or by decoding microinstructions to generate appropriate Am2904 controls.

Status Registers

Instruction lines I_5, I_4, I_3, I_2, I_1, I_0 control the Status Registers. Below, these lines are referred to as two octal digits.

Micro Status Register (μSR)

The instruction codes for the Micro Status Register fall into three groups: Bit Operations, Register Operations and Load Operations (See Table 1 and Map 1). All operations require that $\overline{CE_\mu}$ be LOW to operate.

TABLE 1. MICRO STATUS REGISTER INSTRUCTION CODES.

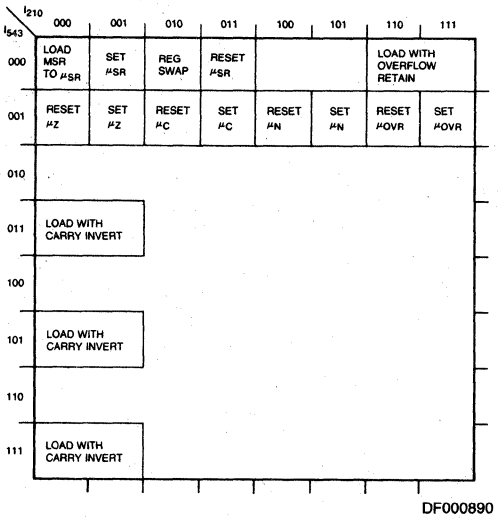
Bit Operations		
I_{543210} Octal	μSR Operation	Comments
10	$0 \rightarrow \mu_Z$	RESET ZERO BIT
11	$1 \rightarrow \mu_Z$	SET ZERO BIT
12	$0 \rightarrow \mu_C$	RESET CARRY BIT
13	$1 \rightarrow \mu_C$	SET CARRY BIT
14	$0 \rightarrow \mu_N$	RESET SIGN BIT
15	$1 \rightarrow \mu_N$	SET SIGN BIT
16	$0 \rightarrow \mu_{OVR}$	RESET OVERFLOW BIT
17	$1 \rightarrow \mu_{OVR}$	SET OVERFLOW BIT

Register Operations		
I_{543210} Octal	μSR Operation	Comments
00	$M_X \rightarrow \mu_X$	LOAD MSR TO μSR
01	$1 \rightarrow \mu_X$	SET μSR
02	$M_X \rightarrow \mu_X$	REGISTER SWAP
03	$0 \rightarrow \mu_X$	RESET μSR

Load Operations		
I_{543210} Octal	μSR Operation	Comments
06, 07	$I_Z \rightarrow \mu Z$ $I_C \rightarrow \mu C$ $I_N \rightarrow \mu N$ $I_{OVR} + \mu OVR \rightarrow \mu OVR$	LOAD WITH OVERFLOW RETAIN
30, 31 50, 51 70, 71	$\overline{I_Z} \rightarrow \mu Z$ $\overline{I_C} \rightarrow \mu C$ $I_N \rightarrow \mu N$ $I_{OVR} \rightarrow \mu OVR$	LOAD WITH CARRY INVERT
04, 05 20-27 32-47 52-67 72-77	$I_Z \rightarrow \mu Z$ $I_C \rightarrow \mu C$ $I_N \rightarrow \mu N$ $I_{OVR} \rightarrow \mu OVR$	LOAD DIRECTLY FROM I_Z, I_C, I_N, I_{OVR}

Note: The above tables assume $\overline{CE}\mu$ is LOW.

MAP 1. MICRO STATUS REGISTER INSTRUCTION CODES.



Notes: 1. All unmarked locations are a load direct from I_Z, I_C, I_N, I_{OVR}.

Instruction Codes 10_8 to 17_8 are BIT operations. These operations set or reset the individual bits in the μSR.

Instruction Codes 00_8 to 03_8 are REGISTER operations. These operations affect all bits in the μSR.

00_8 This instruction loads the μSR with the contents of the MSR while loading the MSR from the Y inputs and is further explained under "INTERRUPTS".

01_8 This instruction SETS all μSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all μSR bits.

All instruction codes except those mentioned in the above two sections cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

06_8, 07_8 When a series of arithmetic operations are being executed sometimes it is not necessary to test for an overflow condition after *each* operation, but rather it is sufficient simply to know that an overflow occurred during any one of the operations. Use of these instructions captures the overflow condition by loading the μSR overflow bit with the LOGICAL OR of its present state and I_{OVR}. Thus, once an overflow occurs, μOVR will remain set throughout the remaining operations.

30_8, 31_8, 50_8, 51_8, 70_8, 71_8 These instructions cause a load from the I inputs, but invert the carry bit. The reason for this is explained more fully under the "BORROW SAVE" section.

All others The remaining instructions load the μSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

Machine Status Register (MSR)

The instruction codes for the MSR fall into two groups; REGISTER Operations and LOAD Operations. All operations require that $\overline{CE}_M$ be LOW to operate (See Table 2 and Map 2). BIT operations are accomplished by the use of Register or Load Operations with the $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ inputs selectively set LOW.

Instruction codes 00_8-03_8 and 05_8 are REGISTER operations. They affect only those bits enabled by $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

00_8 This instruction loads the MSR from the Y inputs while transferring the present contents to the μSR. The use of this instruction is further explained under "INTERRUPTS".

01_8 This instruction SETS all enabled MSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all enabled MSR bits.

05_8 This instruction COMPLEMENTS all enabled MSR bits.

All instruction codes except those mentioned in the above section cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

04_8 The Am2904 Shift Linkage Multiplexer allows for shifts and rotates through the MSR CARRY bit. Some machines require a shift or rotate through the OVERFLOW bit. By using this code, which swaps the contents of the MSR CARRY bit (M_C) and OVERFLOW bit (M_{OVR}), the shift or rotate can be made to appear to take place through the OVERFLOW bit. The procedure is to swap the bits, shift or rotate (any number or positions) then swap the bits again.

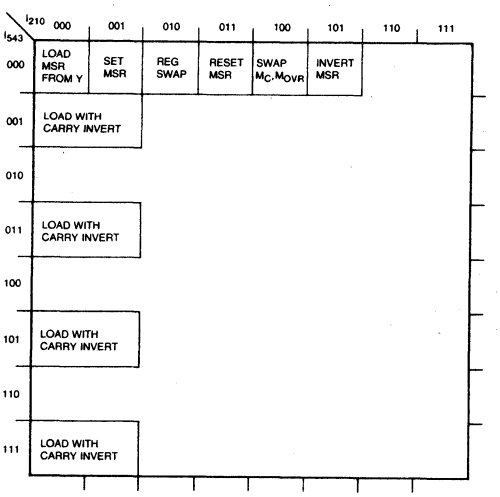
TABLE 2. MACHINE STATUS REGISTER INSTRUCTION CODES

Register Operations		
I_{543210} Octal	MSR Operation	Comments
00	$Y_X \rightarrow M_X$	LOAD Y_Z, Y_C, Y_N, Y_{OVR} TO MSR
01	$1 \rightarrow M_X$	SET MSR
02	$\mu_X \rightarrow M_X$	REGISTER SWAP
03	$0 \rightarrow M_X$	RESET MSR
05	$\overline{M_X} \rightarrow M_X$	INVERT MSR

Load Operations		
I_{543210} Octal	MSR Operation	Comments
04	$I_Z \rightarrow M_Z$ $M_{OVR} \rightarrow M_C$ $I_N \rightarrow M_N$ $M_C \rightarrow M_{OVR}$	LOAD FOR SHIFT THROUGH OVERFLOW OPERATION
10, 11 30, 31 50, 51 70, 71	$I_Z \rightarrow M_Z$ $\overline{I_C} \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD WITH CARRY INVERT
06, 07 12-27 32-47 52-67 72-77	$I_Z \rightarrow M_Z$ $I_C \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C I_N, I_{OVR}

Notes: 1. The above tables assume $\overline{CE_M}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ are LOW.
2. A shift-through-carry instruction loads M_C irrespective of I_5-I_0.

MAP 2. MACHINE STATUS REGISTER INSTRUCTION CODES.



DF000900

06_8, 07_8
12_8-27_8
32_8-47_8
52_8-67_8
72_8-77_8

These instructions load the MSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

10_8, 11_8
30_8, 31_8
50_8, 51_8
70_8, 71_8

These instructions cause a load from the I inputs but invert the CARRY bit. The reason for this is explained more fullu under the 'BORROW SAVE' section.

Condition Code Multiplexer

The two instruction lines I_4, I_5 select whether the μSR, the MSR or the direct inputs I_Z, I_C, I_N, I_{OVR} are used as the inputs to the Y output buffer and the CT output (see Tables 3 and 4).

The four instruction lines I_3, I_2, I_1, I_0 will select one of 16 possible operations to be carried out on the input bits, the result being routed to the Conditional Test Output (CT). Eight of the operations supply an individual status bit or its complement to the CT output. Another four do more complex operations while the remaining four are the complemented results of these (See Table 4).

The more complex operations are intended to follow the calculation A-B to give an indication of which is the larger (A, B unsigned) or more positive (A, B in 2's complement form). See Table 5.

Instruction codes 16_8 and 17_8 form the EXCLUSIVE – OR and the EXCLUSIVE – NOR functions of M_N and I_N. The use of these instructions is explained under "NORMALIZING".

TABLE 3. Y OUTPUT INSTRUCTION CODES.

$\overline{OE_Y}$	I_5	I_4	Y Output	Comment
H	X	X	Z	Output Off High Impedance
L	L	X	$\mu_i \rightarrow Y_i$	See Note 1
L	H	L	$M_i \rightarrow Y_i$	
L	H	H	$I_i \rightarrow Y_i$	

Notes: 1. For the conditions:
I_5, I_4, I_3, I_2, I_1, I_0 are LOW, Y is an input.
$\overline{OE_Y}$ is "Don't Care" for this condition.
2. X is "Don't Care" condition.

TABLE 4. CONDITION CODE OUTPUT (CT) INSTRUCTION CODES.

I_{3-0} HEX	I_3	I_2	I_1	I_0	$I_5 = I_4 = 0$	$I_5 = 0$, $I_4 = 1$	$I_5 = 1$, $I_4 = 0$	$I_5 = I_4 = 1$
0	0	0	0	0	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(M_N \oplus M_{OVR}) + M_Z$	$(I_N \oplus I_{OVR}) + I_Z$
1	0	0	0	1	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(M_N \odot M_{OVR}) \cdot \overline{M}_Z$	$(I_N \odot I_{OVR}) \cdot \overline{I}_Z$
2	0	0	1	0	$\mu_N \oplus \mu_{OVR}$	$\mu_N \oplus \mu_{OVR}$	$M_N \oplus M_{OVR}$	$I_N \oplus I_{OVR}$
3	0	0	1	1	$\mu_N \odot \mu_{OVR}$	$\mu_N \odot \mu_{OVR}$	$M_N \odot M_{OVR}$	$I_N \odot I_{OVR}$
4	0	1	0	0	μ_Z	μ_Z	M_Z	I_Z
5	0	1	0	1	$\overline{\mu}_Z$	$\overline{\mu}_Z$	$\overline{M}_Z$	$\overline{I}_Z$
6	0	1	1	0	μ_{OVR}	μ_{OVR}	M_{OVR}	I_{OVR}
7	0	1	1	1	$\overline{\mu}_{OVR}$	$\overline{\mu}_{OVR}$	$\overline{M}_{OVR}$	$\overline{I}_{OVR}$
8	1	0	0	0	$\mu_C + \mu_Z$	$\mu_C + \mu_Z$	$M_C + M_Z$	$\overline{I_C} + I_Z$(2)
9	1	0	0	1	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{M}_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$(2)
A	1	0	1	0	μ_C	μ_C	M_C	I_C
B	1	0	1	1	$\overline{\mu}_C$	$\overline{\mu}_C$	$\overline{M}_C$	$\overline{I_C}$
C	1	1	0	0	$\overline{\mu}_C + \mu_Z$	$\overline{\mu}_C + \mu_Z$	$\overline{M}_C + M_Z$	$\overline{I_C} + I_Z$
D	1	1	0	1	$\mu_C \cdot \overline{\mu}_Z$	$\mu_C \cdot \overline{\mu}_Z$	$M_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$
E	1	1	1	0	$I_N \oplus M_N$	μ_N	M_N	I_N
F	1	1	1	1	$I_N \odot M_N$	$\overline{\mu}_N$	$\overline{M}_N$	$\overline{I}_N$

NOTES: 1. ⊕ Represents EXCLUSIVE-OR
⊙ Represents EXCLUSIVE-NOR or coincidence.
2. Correct code as stated.

TABLE 5. CRITERIA FOR COMPARING TWO NUMBERS FOLLOWING "A MINUS B" OPERATION.

	For Unsigned Numbers			For 2's Complement Numbers		
		I_{3-0}			I_{3-0}	
Relation	Status	CT = H	CT = L	Status	CT = H	CT = L
A = B	Z = 1	4	5	Z = 1	4	5
A ≠ B	Z = 0	5	4	Z = 0	5	4
A ≥ B	C = 1	A	B	N⊙OVR = 1	3	2
A < B	C = 0	B	A	N⊕OVR = 1	2	3
A > B	$C \cdot \overline{Z} = 1$	D	C	$(N \odot OVR) \cdot \overline{Z} = 1$	1	0
A ≤ B	$\overline{C} + Z = 1$	C	D	(N⊕OVR) + Z = 1	0	1

⊕ = Exclusive OR H = HIGH
⊙ = Exclusive NOR L = LOW

Note: For Am2910, the CC input is active LOW, so use I_{3-0} code to produce CT = L for the desired test.

Shift Linkage Multiplexer

The five instruction lines I_{10}, I_9, I_8, I_7, I_6 control the SHIFT LINKAGE multiplexer. All instructions set up the linkages for both the ALU shifter (RAM shifter on the Am2901A) and the Q register.

UP and DOWN shifts are decided by I_{10} which should be connected to I_8 of the Am2903's instruction lines or I_7 of the Am2901's instruction lines. A wide range of input and output connections are provided, allowing for single or double length shifting or rotating with or without the use of the MSR CARRY or SIGN bits (See Table 6).

In the following discussion of some of the shifts the instruction codes are given as two octal digits AB; A represents I_{10}, I_9, B represents I_8, I_7, I_6.

When adding and down shifting on the same microcycle, (i.e. when doing multiplication or averaging) the shifter input must be the present CARRY, I_C, rather than the carry resulting from the last cycle (M_C). Instruction Code 13_8 accomplishes this for unsigned arithmetic. For 2's complement arithmetic, the required shifter input is: $I_N \oplus I_{OVR}$. This is provided by Instruction Code 16_8.

Instruction Codes 14_8, 15_8, 17_8 provide the RIGHT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

Instruction Codes 34_8, 35_8, 37_8 provide the LEFT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

The shift outputs are in the high impedance state unless $\overline{SE}$ is LOW.

Loading of the M_C bit by a shift operation overrides any loading or holding of the M_C bit by MSR Instructions (I_{0-5}, $\overline{CE_M}$ and $\overline{E_C}$).

"CARRY-IN" Control Multiplexer

The two instruction lines I_{12}, I_{11} control the source of the CARRY output (C_0).

When $I_{12} = 0$ $C_0 = I_{11}$

When $I_{12} = 1$ and $I_{11} = 0$, the external carry input C_X is presented to the carry output.

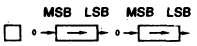
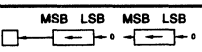
When $I_{12} = I_{11} = 1$ the carry output is selected from μ_C, $\overline{\mu_C}$, M_C or $\overline{M_C}$ as defined by I_5, I_3, I_2, I_1 (See Table 7).

APPLICATIONS INFORMATION

Borrow – Save

One of the capabilities of the Am2900 Family is the complete emulation of other processing machines. One requirement of an emulator is that, when a calculation is being performed, not only must the answer obtained from the Am2900 chips be the same as that from the machine being emulated, but after each machine level instruction, the status bits must be identical.

TABLE 6. SHIFTLINKAGE MULTIPLEXER INSTRUCTION CODES.

I_{10}	I_9	I_8	I_7	I_6	M_C RAM Q	SIO_0	SIO_n	QIO_0	QIO_n	Loaded into M_C
0	0	0	0	0		Z	0	Z	0	
0	0	0	0	1		Z	1	Z	1	
0	0	0	1	0		Z	0	Z	M_n	SIO_0
0	0	0	1	1		Z	1	Z	SIO_0	
0	0	1	0	0		Z	M_C	Z	SIO_0	
0	0	1	0	1		Z	M_N	Z	SIO_0	
0	0	1	1	0		Z	0	Z	SIO_0	
0	0	1	1	1		Z	0	Z	SIO_0	QIO_0
0	1	0	0	0		Z	SIO_0	Z	QIO_0	SIO_0
0	1	0	0	1		Z	M_C	Z	QIO_0	SIO_0
0	1	0	1	0		Z	SIO_0	Z	QIO_0	
0	1	0	1	1		Z	I_C	Z	SIO_0	
0	1	1	0	0		Z	M_C	Z	SIO_0	QIO_0
0	1	1	0	1		Z	QIO_0	Z	SIO_0	QIO_0
0	1	1	1	0		Z	$I_N \oplus I_{OVR}$	Z	SIO_0	
0	1	1	1	1		Z	QIO_0	Z	SIO_0	
1	0	0	0	0		0	Z	0	Z	SIO_n
1	0	0	0	1		1	Z	1	Z	SIO_n
1	0	0	1	0		0	Z	0	Z	
1	0	0	1	1		1	Z	1	Z	
1	0	1	0	0		QIO_n	Z	0	Z	SIO_n
1	0	1	0	1		QIO_n	Z	1	Z	SIO_n
1	0	1	1	0		QIO_n	Z	0	Z	
1	0	1	1	1		QIO_n	Z	1	Z	
1	1	0	0	0		SIO_n	Z	QIO_n	Z	SIO_n
1	1	0	0	1		M_C	Z	QIO_n	Z	SIO_n
1	1	0	1	0		SIO_n	Z	QIO_n	Z	
1	1	0	1	1		M_C	Z	0	Z	
1	1	1	0	0		QIO_n	Z	M_C	Z	SIO_n
1	1	1	0	1		QIO_n	Z	SIO_n	Z	SIO_n
1	1	1	1	0		QIO_n	Z	M_C	Z	
1	1	1	1	1		QIO_n	Z	SIO_n	Z	

Notes: 1. Z = High impedance (outputs off) state.
2. Outputs enabled and M_C loaded only if $\overline{SE}$ is LOW.
3. Loading of M_C from I_{10-6} overrides control from I_{5-0},$\overline{CE}_M$,$\overline{E}_C$.

TABLE 7. CARRY-IN CONTROL MULTIPLEXER INSTRUCTION CODES.

I_{12}	I_{11}	I_5	I_3	I_2	I_1	C_0
0	0	X	X	X	X	0
0	1	X	X	X	X	1
1	0	X	X	X	X	C_X
1	1	0	0	X	X	μ_C
1	1	0	X	1	X	μC
1	1	0	X	X	1	μ_C
1	1	0	1	0	0	$\overline{\mu}_C$
1	1	1	0	X	X	M_C
1	1	1	X	1	X	M_C
1	1	1	X	X	1	M_C
1	1	1	1	0	0	$\overline{M}_C$

There are alternative methods for subtracting in a digital machine and the state of the CARRY after the calculation depends on the method. For instance, the subtraction of 0100 from 1010 by the 2's complement add method generates a result of 0110 with a CARRY. Direct subtraction however, yields an answer of 0110 with no BORROW.

Many machines store the state of the CARRY for subtract operations, and this is the recommended method for maximum effective use of the Am2904, but, to allow those machines which store the BORROW to be efficiently emulated, the Am2904 has allocated special instructions. Using these codes causes the CARRY bit to be inverted before storage in the status registers and also re-inverts these status bits before using them as carry inputs. These codes are 10_8, 11_8, 30_8, 31_8, 50_8, 51_8, 70_8, 71_8 ($I_{5\text{-}0}$).

Notice that when these codes are used to load the inverted CARRY to either of the status registers, the CT output selected by the Condition Code Multiplexer assumes the CARRY is inverted and still defines whether $A > B$ or $A \leqslant B$ (See Table 4).

Similarly, when doing a compare on a machine which saves the BORROW, testing for $A > B$, $A \leqslant B$ forces the complement of the CARRY to be stored in the status registers (See Tables 1 and 2).

Normalizing

Normalizing is the process of stripping off all leading sign bits until the two most significant bits are complementary. The Am2904 facilitates both single and double length normalization in the Am2901 and the Am2903. When using the NORMALIZE special instructions with the Am2903, the EXCLUSIVE – OR of the most significant two bits is generated at the C_{n+4} pin of the most significant Am2903. The EXCLUSIVE – OR of the two bits next to the most significant bit is also generated at the OVR pin. The procedure for normalizing then is to loop on the normalize instruction with a branch condition on the C_{n+4} state or the OVR state, depending on the architecture employed. The C_{n+4} or OVR output is routed to the Am2910 CC input through the Am2904 Condition Code multiplexer. As the contents of the status registers always refer to the last cycle, not the present one, the last operation in normalizing is to downshift, bringing the sign bit (M_N) back into the most significant bit position. This is achieved using the shift operations 05_8 ($I_{10\text{-}6}$) for double length normalizing,and 02_8 for single length normalizing . For more details regarding normalizing with the Am2903 see the Am2903 data sheet.

The Am2901 does not have the EXCLUSIVE – OR gates to help with normalizing, so the Am2904 includes in the Condition Code multiplexer the EXCLUSIVE – OR and EXCLUSIVE – NOR functions of M_N (the sign bit resulting from the last operation) and I_N (the sign bit resulting from the present operation). Instruction codes 16_8 and 17_8 ($I_{5\text{-}0}$) form the EXCLUSIVE-OR and EXCLUSIVE-NOR functions of M_N and I_N.

Interrupts

Some machines allow interrupts only at the machine instruction level while others allow them at the microinstruction level. The Am2904 is designed to handle both cases.

When the machine is interrupted, it is necessary to store the contents of either the MSR (machine instruction level interrupts) or both the status registers (micro instruction level interrupts) into an external store. This transfer is intended to take place over the Y input/output pins (See Table 3).

After the interrupt has been serviced the registers must be restored to their pre-interrupt state. This is accomplished by two operations of instruction 00_8 ($I_{5\text{-}0}$) which loads the MSR from the Y inputs while loading the μSR from the MSR. Thus, the pre-interrupt contents of the μSR are first loaded to the MSR (first instruction 00_8), then this data is transferred to the μSR while the MSR is restored to its pre-interrupt state (second instruction 00_8).

In controllers and some other microprogrammed machines the applications program itself is often in the microprogram memory; that is, there is no macroinstruction set. These machines require only a microstatus register since there is no separate machine status. The MSR in the Am2904 can be used as a one-level stack on the microstatus register. When an interrupt occurs, the μSR and the MSR are simply swapped ($I_{5\text{-}0} = 02_8$).

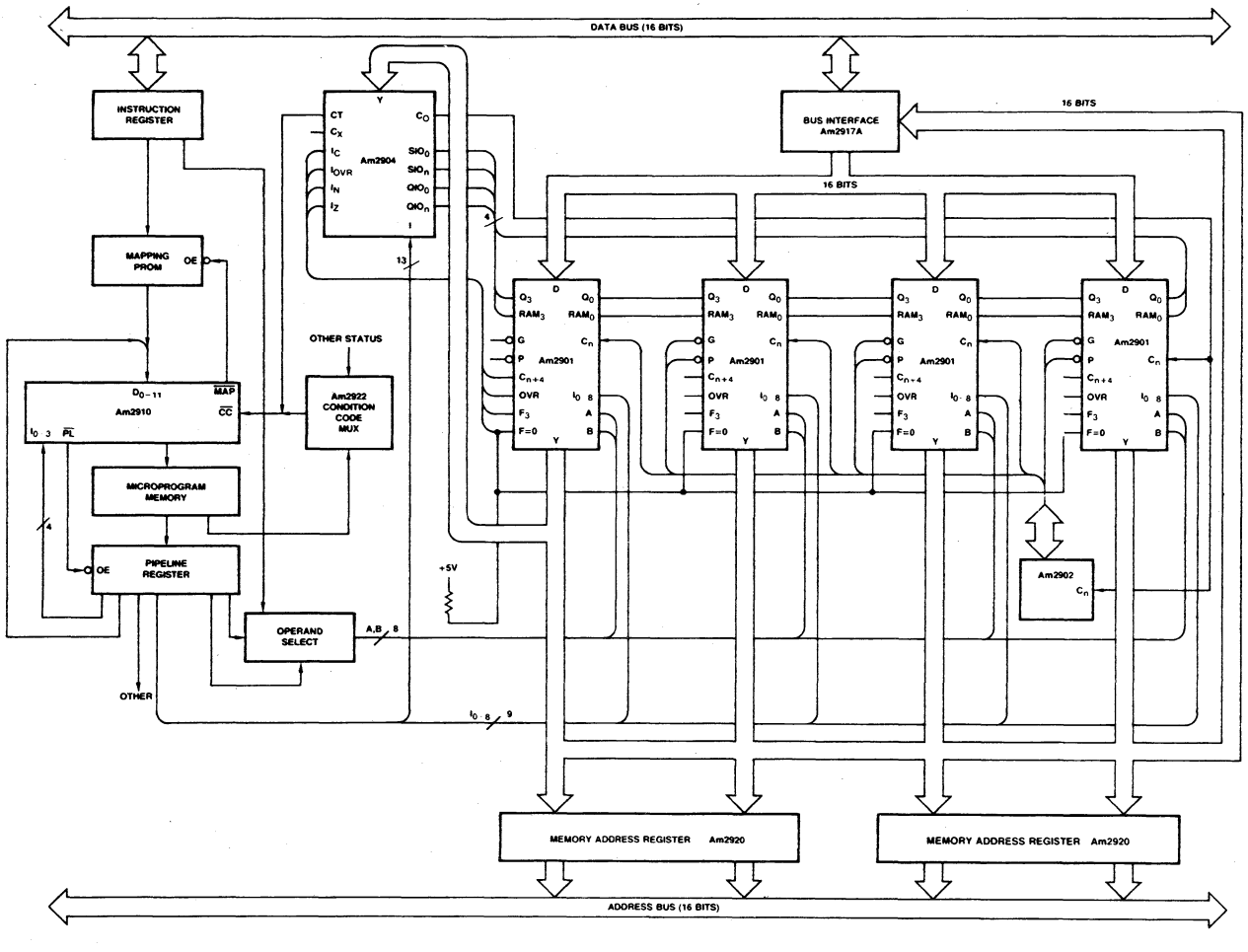


Figure 1. Typical Application of Am2904 with Am2901.

Refer to Page 13-1 for Essential Information on Military Devices

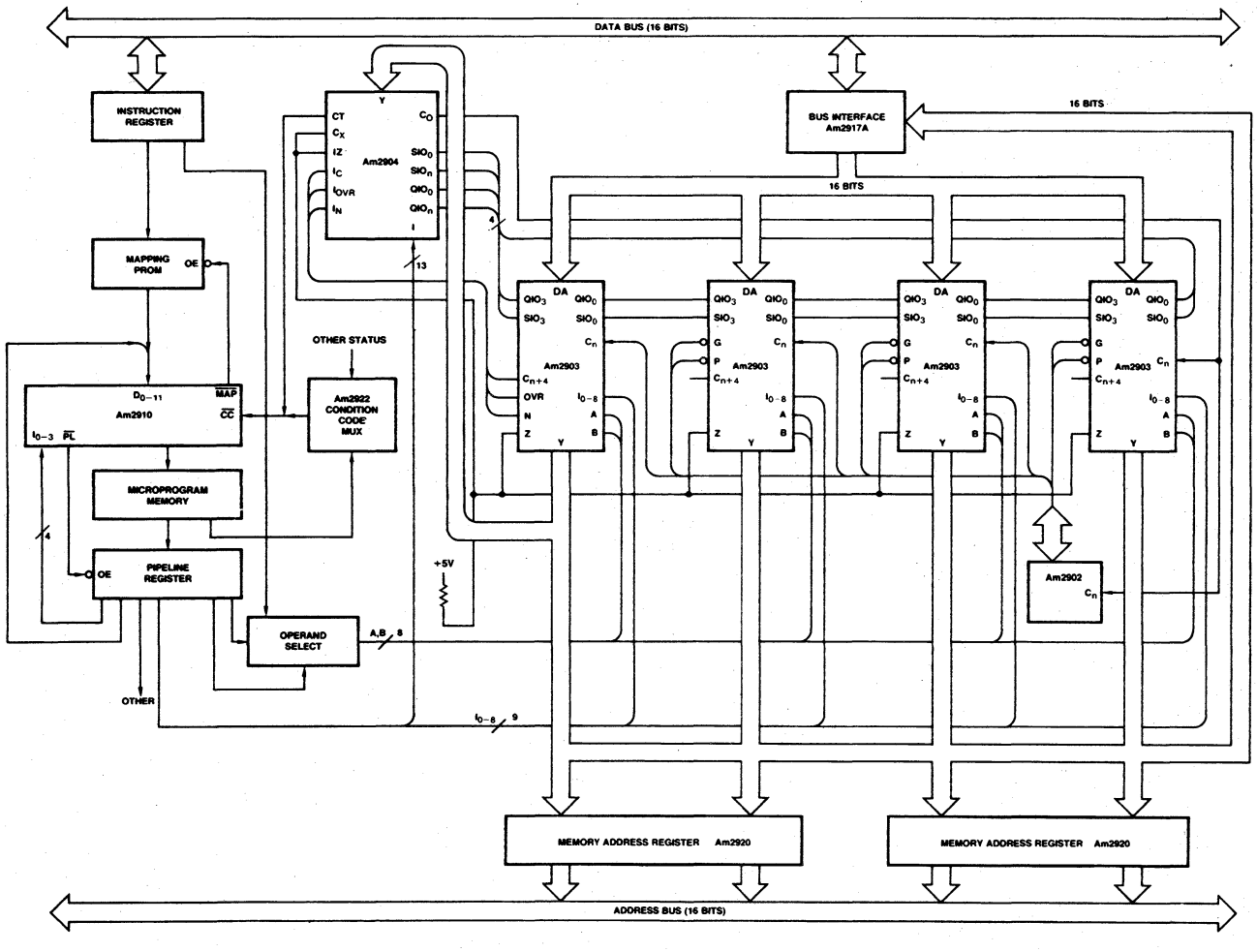


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Figure 2. Typical Application of Am2904 with Am2903.

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Case) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_Z, Y_C, Y_N, Y_{OVR}	2.4			Volts
				I_{OH} = −0.8mA SIO_O, SIO_n, QIO_O QIO_n, CT, CO	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_Z, Y_C Y_N, Y_{OVR}	I_{OL} = 24mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			SIO_O, QIO_O, CT, SIO_n, QIO_n, CO	I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		CP			−0.7	mA
				$\overline{CE_m}$, $\overline{CE_\mu}$			−1.8	
				I_Z, I_C, I_N, I_{OVR}			−1.2	
				I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$ $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X, Y_Z, Y_C, Y_N, Y_{OVR}			−0.45	
				$\overline{SE}$, SIO_O, SIO_n QIO_O, QIO_n			−1.35	
I_{IH}	Input HIGH Current	V_{CC} = MAX V_{IN} = 2.7V		CP, I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X			20	μA
				$\overline{CE_m}$, $\overline{CE_\mu}$			80	
				I_Z, I_C, I_N, I_{OVR}, $\overline{SE}$			60	
				SIO_O, SIO_n, QIO_O, QIO_n			110	
				Y_Z, Y_C, Y_N, Y_{OVR}			70	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX	CT	V_O = 2.4			50	μA
				V_O = 0.5			−50	
			SIO_O, SIO_n, QIO_O, QIO_n (Note 4)	V_O = 2.4			110	
				V_O = 0.5			−1350	
			Y_Z, Y_C, Y_N, Y_{OVR} (Note 4)	V_O = 2.4			70	
				V_O = 0.5			−450	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V, V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX	Am2904DC	T_A = 0°C to +70°C			318	mA
				T_A = +70°C			262	
			Am2904DM, FM	T_C = −55°C to +125°C			348	
				T_C = +125°C			222	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2904 XM, DM, FM, "COM'L" = Am2904 XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested.)

SWITCHING CHARACTERISTICS

The tables below define the Am2904 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to +5.25V, C_L = 50pF).

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	14	5
I_C (I_1 I_2 I_3 = 001)	27	5
I_C (I_1 I_2 I_3 ≠ 001)	14	5
$\overline{CE}_\mu$	18	3
$\overline{CE}_M$	23	3
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$	22	3
$I_0 - I_5$	41	1
$I_6 - I_{10}$	40	1
$\overline{SE}$	36	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	15	5
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z, I_C, I_N, I_{OVR}	Y_Z, Y_C, Y_N, Y_{OVR}	38
CP	Y_Z, Y_C, Y_N, Y_{OVR}	41
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	35
I_Z, I_C, I_N, I_{OVR}	CT	33
CP	CT	36
$I_0 - I_5$	CT	33
C_X	C_O	20
CP	C_O	27
$I_{1, 2, 3, 5, 11, 12}$	C_O	39
SIO_n, QIO_n	SIO_o	19
SIO_o, QIO_o	SIO_n	19
I_C, I_N, I_{OVR}	SIO_n	26
SIO_n, QIO_n	QIO_o	19
SIO_o, QIO_o	QIO_n	19
CP	SIO_o, SIO_n, QIO_o, QIO_n	30
I_6-I_{10}	SIO_o, SIO_n, QIO_o, QIO_n	26

C. Clock Requirements (ns)

Minimum Clock LOW Time	20
Minimum Clock HIGH Time	20

D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests measured to 0.5V change of output voltage level.

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	23	18
SE	SIO_o, SIO_n QIO_o, QIO_n	30	12
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	39	29
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	26	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	28	40

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to +5.5V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	15	5
I_C (I_1 I_2 I_3 = 001)	28	5
I_C (I_1 I_2 I_3 ≠ 001)	15	5
$\overline{CE}_\mu$	20	3
$\overline{CE}_M$	23	4
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$	23	4
$I_0 - I_5$	48	2
$I_6 - I_{10}$	44	2
$\overline{SE}$	40	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	16	6
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z, I_C, I_N, I_{OVR}	Y_Z, Y_C, Y_N, Y_{OVR}	40
CP	Y_Z, Y_C, Y_N, Y_{OVR}	45
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	38
I_Z, I_C, I_N, I_{OVR}	CT	44
CP	CT	40
$I_0 - I_5$	CT	41
C_X	C_O	22
CP	C_O	28
$I_{1, 2, 3, 5, 11, 12}$	C_O	42
SIO_n, QIO_n	SIO_o	20
SIO_o, QIO_o	SIO_n	20
I_C, I_N, I_{OVR}	SIO_n	29
SIO_n, QIO_n	QIO_o	20
SIO_o, QIO_o	QIO_n	20
CP	SIO_o SIO_n, QIO_o, QIO_n	32
I_6-I_{10}	SIO_o, SIO_n, QIO_o, QIO_n	31

C. Clock Requirements (ns)

Minimum Clock LOW Time	25
Minimum Clock HIGH Time	25

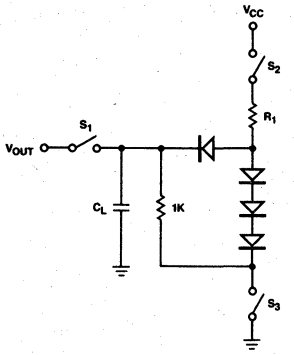
D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests
measured to 0.5V change of output voltage level.

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	25	18
SE	SIO_o, SIO_n QIO_o, QIO_n	35	16
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	43	32
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	28	23
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	30	41

SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



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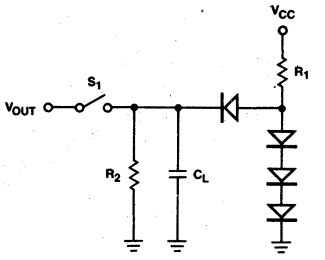
$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



TC001130

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. S_1, S_2, S_3 are closed during function all tests and AC tests except output enable tests.
3. S_1 and 3_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2904

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
25	C_0	B	470	3K
27	CT	A	430	1K
28	Y_{OVR}	A	220	1K
29	Y_N	A	220	1K
31	Y_C	A	220	1K
32	Y_Z	A	220	1K
33	QIO_N	A	430	1K
34	QIO_0	A	430	1K
35	SIO_N	A	430	1K
36	SIO_0	A	430	1K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Am2905

Quad Two-Input OC Bus Transceiver with Three-State Receiver

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver output can sink 100mA at 0.8V max
- Two-port input to D-type register on driver
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing

GENERAL DESCRIPTION

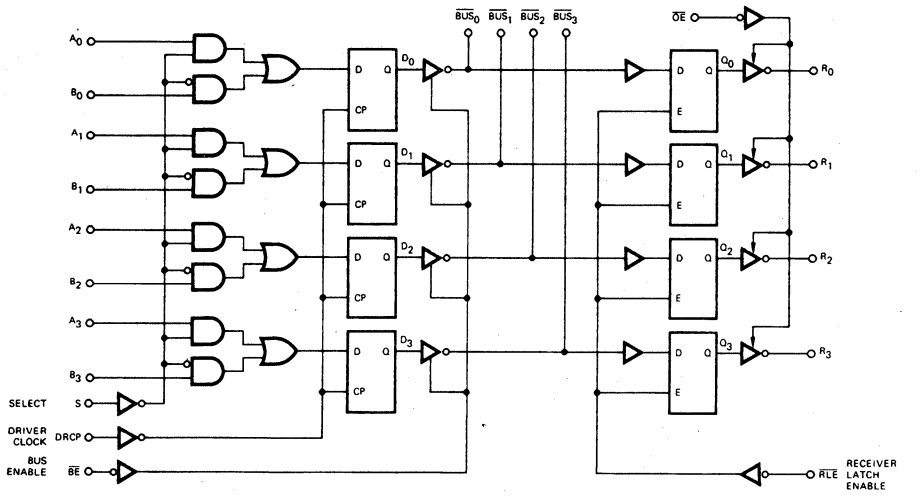
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

BLOCK DIAGRAM



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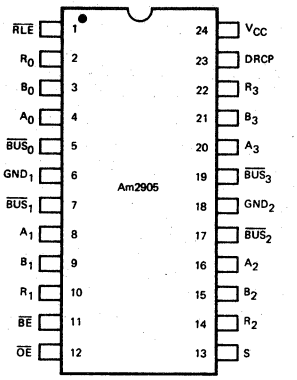
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

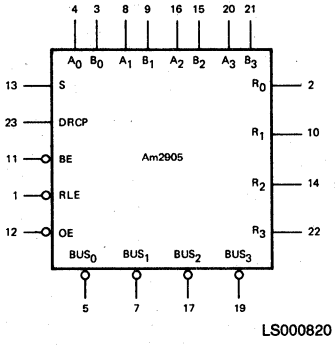
D-24-1



CD002090

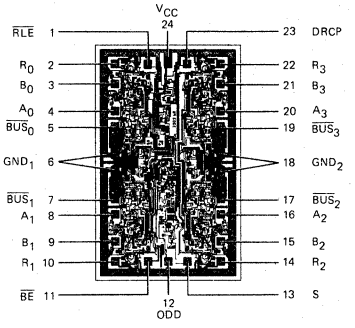
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000820

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2905 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - F– 24-pin flatpak
  - P– 24-pin plastic DIP
  - X– Dice
- **Am2905** — Device type
  - OC Bus Transceiver

Valid Combinations	
Am2905	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 8, 16, 20	A_0, A_1, A_2, A_3	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9, 15, 21	B_0, B_1, B_2, B_3	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
11	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
5 7 17, 19	$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 10 14, 22	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	$\overline{OE}$	I	Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	FUNCTION
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and
X	X	X	X	H	L	L	X	H	H	L	receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

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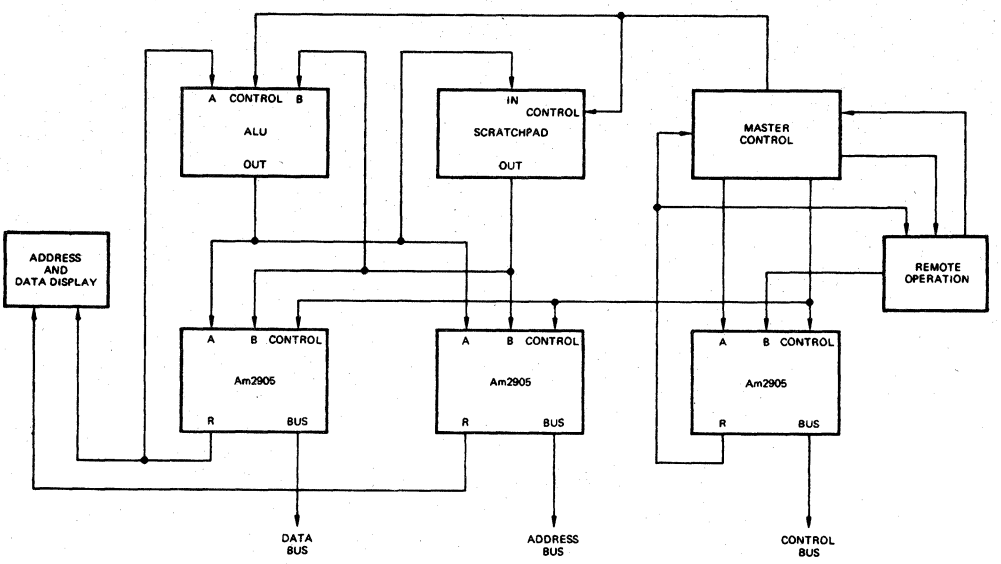
Refer to Page 13-1 for Essential Information on Military Devices

APPLICATIONS



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The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7V
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Output Current, Into Bus 200mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = V_{IN} = V_{IL} or V_{IH}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX, All inputs = GND			69	105	mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

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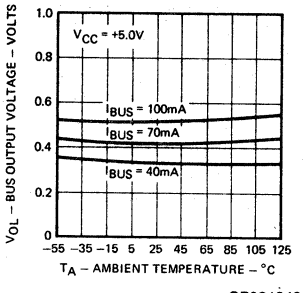
Refer to Page 13-1 for Essential Information on Military Devices

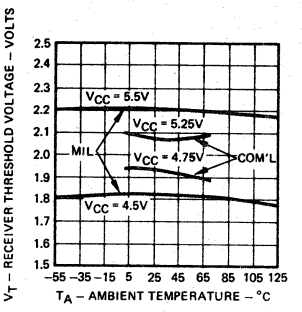
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



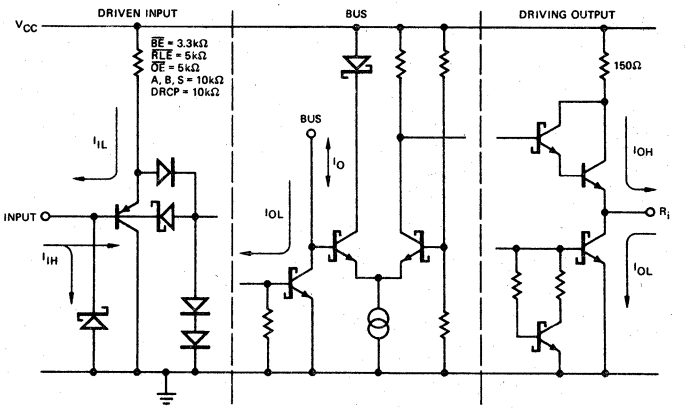
OP001340

Receiver Threshold Variation Versus Ambient Temperature



OP001330

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000390

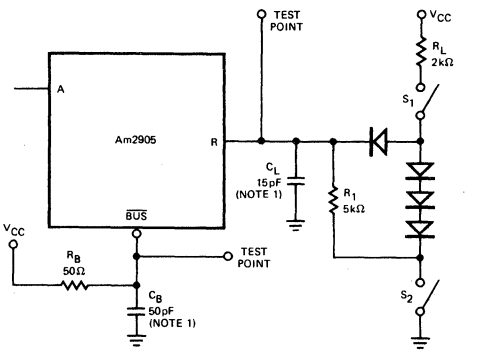
Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2905 Min	COMMERCIAL Am2905 Typ (Note 1)	COMMERCIAL Am2905 Max	MILITARY Am2905 Min	MILITARY Am2905 Typ (Note 1)	MILITARY Am2905 Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 50 Ω		21	36		21	40	ns
t_{PLH}				21	36		21	40	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{PLH}				13	23		13	26	
t_s	Data Inputs (A or B)	C_L = 15 pF, R_L = 2.0 kΩ	23			25			ns
t_h			7.0			8.0			
t_s	Select Input (S)		30			33			ns
t_h			7.0			8.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		25			28			ns
t_{PLH}	Bus to Receive Output (Latch Enable)			18	34		18	37	ns
t_{PHL}				18	34		18	37	
t_{PLH}	Latch Enable to Receiver Output			21	34		21	37	ns
t_{PHL}				21	34		21	37	
t_s	Bus to Latch Enable ($\overline{RLE}$)		18			21			ns
t_h			5.0			7.0			
t_{ZH}	Output Control to Receiver Output			14	25		14	28	ns
t_{ZL}				14	25		14	28	
t_{HZ}	Output Control to Receiver Output			14	25		14	28	ns
t_{LZ}				14	25		14	28	

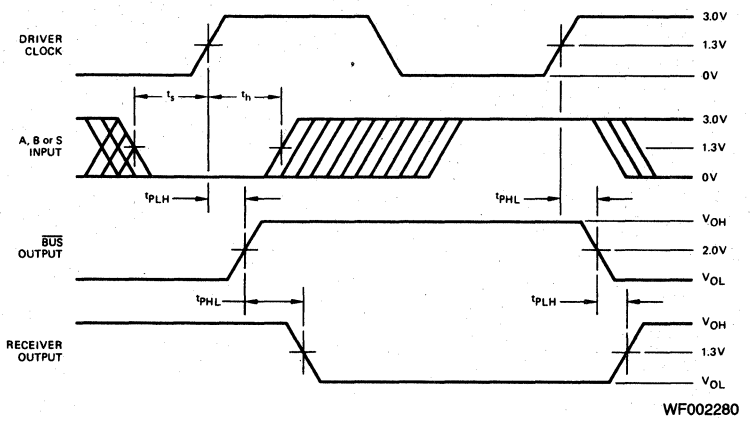
Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING TEST CIRCUIT



TC000870

SWITCHING WAVEFORMS



WF002280

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

Am2906

Quad Two-Input OC Bus Transceiver with Parity

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver output can sink 100mA at 0.8V max.
- Two-port input to D-type register on driver.
- Internal 4-bit odd parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.

GENERAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

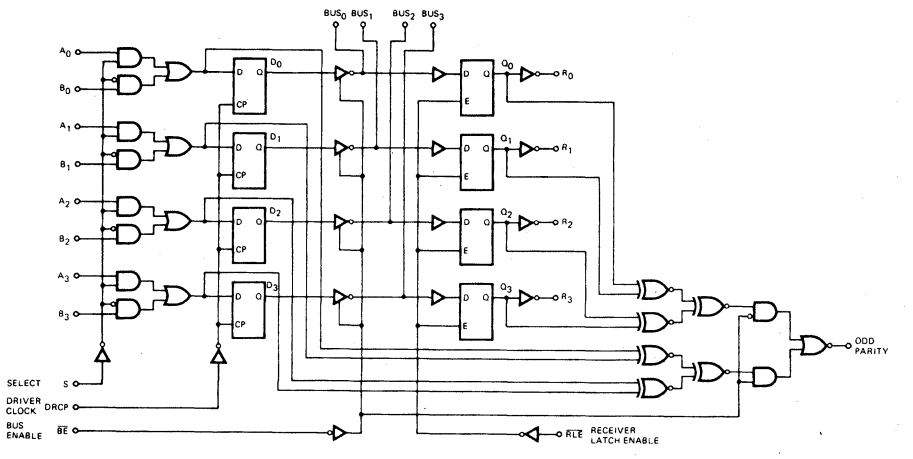
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

BLOCK DIAGRAM



BD001870

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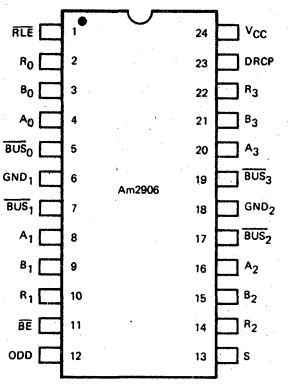
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

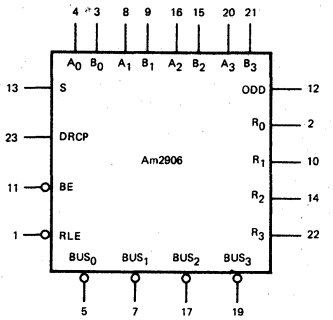
D-24-1



CD003000

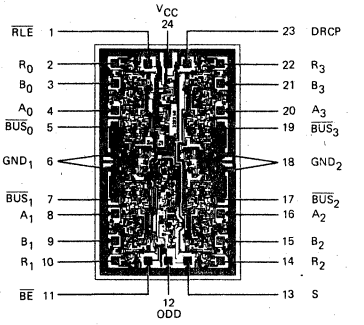
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000770

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2906 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - F– 24-pin flatpak
  - P– 24-pin plastic DIP
  - X– Dice
- **Am2906** — Device type
  - OC Bus Transceiver

Valid Combinations	
Am2906	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 8 16, 20	A_0, A_1, A_2, A_3	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9 15, 21	B_0, B_1, B_2, B_3	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP		Driver Clock Pulse. Clock pulse for the driver register.
11	$\overline{BE}$		Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
5 7 17, 19	$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$	O	The four driver outputs and receiver inputs (data is inverted).
2, 10 14, 22	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in high-impedance state.

FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUTS		
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	ODD	FUNCTION
X	X	X	X	H	X	X	X	Z	X	PQ	Driver output disable
X	X	X	X	L	X	X	X	X	X	PD	Driver output enable
X	X	X	X	H	L	X	L	L	H	H	Driver output disable and
X	X	X	X	H	L	X	H	H	L	H	receive data via Bus input
X	X	X	X	X	H	X	NC	X	NC	X	Latch received data
L	L	X	↑	X	X	L	X	X	X	X	Load driver register
L	H	X	↑	X	X	H	X	X	X	X	
H	X	L	↑	X	X	L	X	X	X	X	
H	X	H	↑	X	X	H	X	X	X	X	
X	X	X	L	X	X	NC	X	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	X	
X	X	X	X	L	X	L	X	H	X	H	Drive Bus
X	X	X	X	L	X	H	X	L	X	H	

H = HIGH
L = LOW
Z = HIGH Impedance

X = Don't care
i = 0, 1, 2, 3
↑ = LOW to HIGH transition

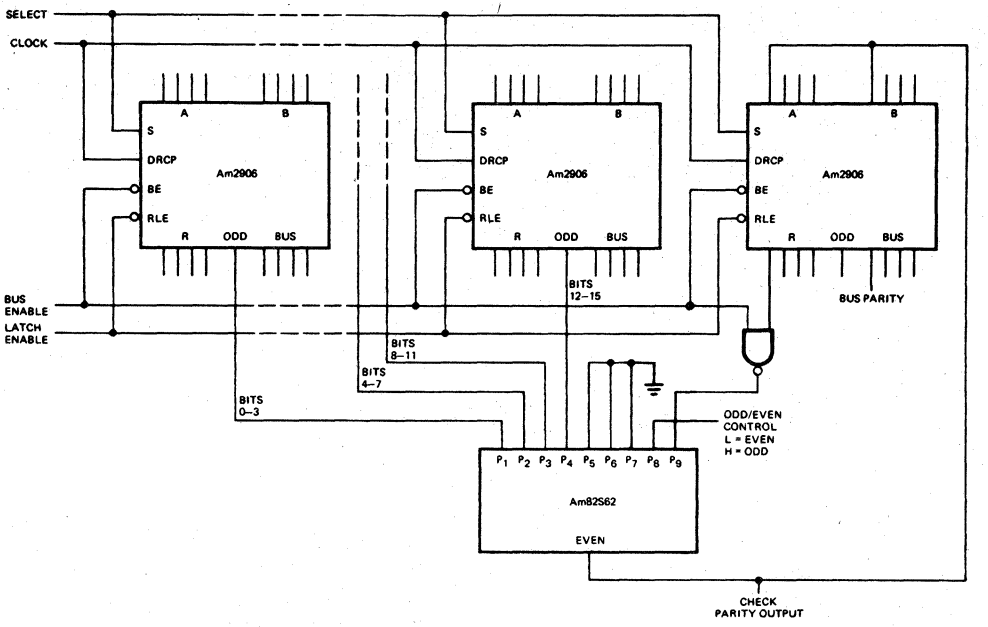
NC = No change
PD = Parity of D flip flops
PQ = Parity of Q latches

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	$ODD = I_0 \oplus I_1 \oplus I_2 \oplus I_3$
H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

I_i = Selected input A_i or B_i

APPLICATIONS



AF001040

Generating or checking parity for 16 data bits.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus 200mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL	I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L	I_{OH} = −2.6mA	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}		I_{OL} = 4mA		0.27	0.4	Volts
				I_{OL} = 8mA		0.32	0.45	
				I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus) (Note 3)	V_{CC} = MAX			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX, All inputs = GND				72	105	mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

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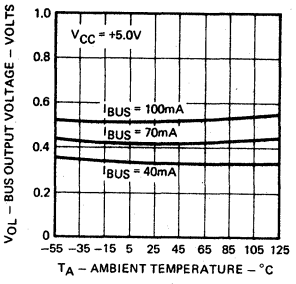
Refer to Page 13-1 for Essential Information on Military Devices

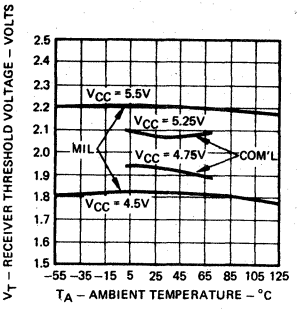
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



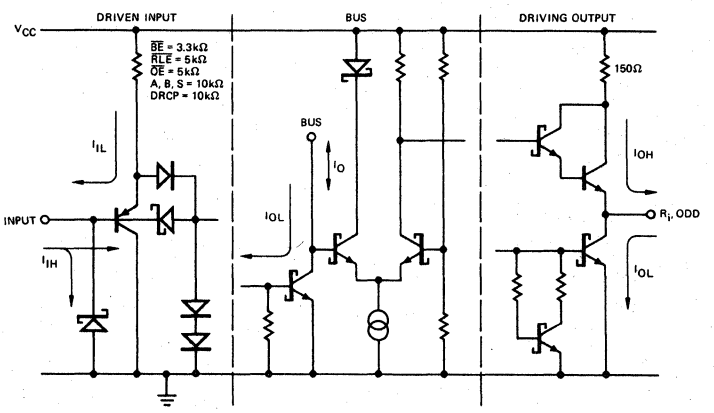
OP001340

Receiver Threshold Variation Versus Ambient Temperature



OP001330

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000340

Note: Actual current flow direction shown.

05398A

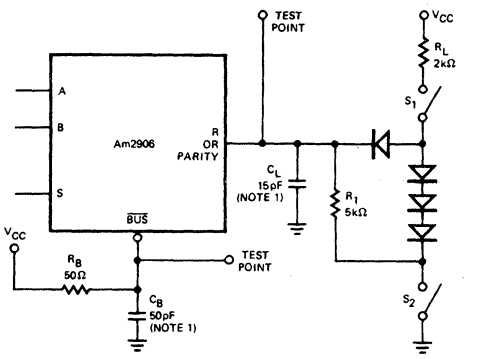
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2906 Min	COMMERCIAL Am2906 Typ (Note 1)	COMMERCIAL Am2906 Max	MILITARY Am2906 Min	MILITARY Am2906 Typ (Note 1)	MILITARY Am2906 Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 50 Ω		21	36		21	40	ns
t_{PLH}				21	36		21	40	
t_{PHL}	Bus Enable ($\overline{BE}$) to BUS			13	23		13	26	ns
t_{PLH}				13	23		13	26	
t_s	Data Inputs (A or B)	C_L = 15 pF, R_L = 2.0 kΩ	23			25			ns
t_h			7.0			8.0			
t_s	Select Inputs (S)		30			33			ns
t_h			7.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		25			28			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	34		18	37	ns
t_{PHL}				18	34		18	37	
t_{PLH}	Latch Enable to Receiver Output			21	34		21	37	ns
t_{PHL}				21	34		21	37	
t_s	Bus to Latch Enable ($\overline{RLE}$)		18			21			ns
t_h			5.0			7.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	40	ns
t_{PHL}				21	36		21	40	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING TEST CIRCUIT



TC000820

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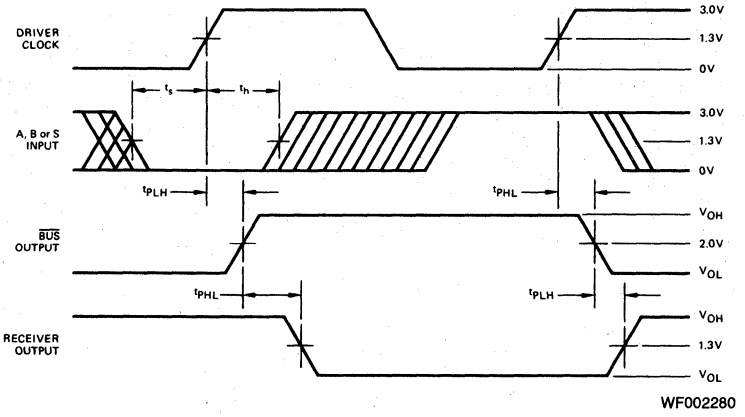
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



WF002280

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

Am2907/Am2908

Quad Bus Transceivers with Interface Logic

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- D-type driver register with open-collector bus driver output can sink 100mA at 0.8V max.
- Internal 4-bit odd parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Am2907 has 2.0V input receiver threshold; Am2908 is "DECQ or LSI-II bus compatible" with 1.5V receiver threshold

GENERAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

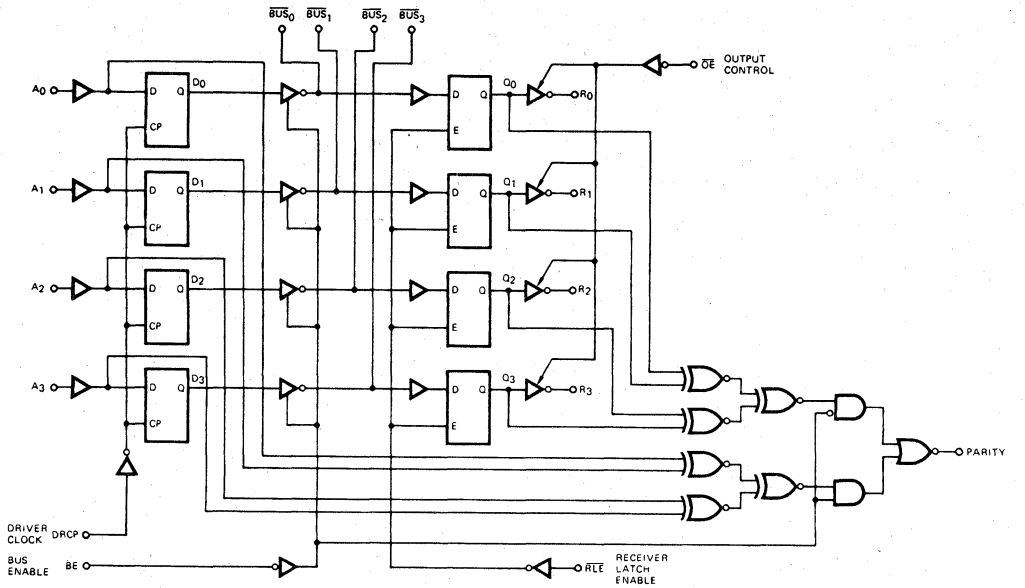
The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

05399A

Refer to Page 13-1 for Essential Information on Military Devices

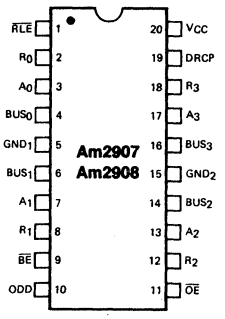
BLOCK DIAGRAM



BD001890

CONNECTION DIAGRAM
Top View

D-20-1

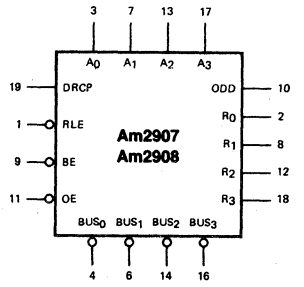


CD003060

Note: Pin 1 is marked for orientation

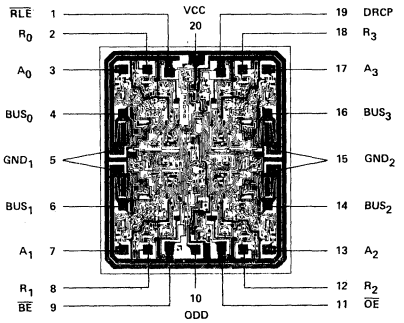
5

LOGIC SYMBOL



LS000840

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.088" x 0.103"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2907/ Am2908 **D C B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 20-pin CERDIP; F– 20-pin flatpak; P– 20-pin plastic DIP; X– Dice

Device type: Quad Bus Transceivers

Valid Combinations	
Am2907 Am2908	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7 13, 17	A_0, A_1 A_2, A_3	I	The four driver register inputs.
19	DRCP	I	Driver Clock Pulse: Clock pulse for the driver register.
9	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH. The four drivers are in the high impedance state.
4 6 14 16	$\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 8, 12, 18	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
10	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.
11	$\overline{OE}$	I	Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	FUNCTION
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X X	X X	H H	L L	L L	X X	L H	L H	H L	Driver output disable and receive data via Bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L H	↑ ↑	X X	X X	X X	L H	X X	X X	X X	Load driver register
X X	L H	X X	X X	X X	NC NC	X X	X X	X X	No driver clock restrictions
X	X	L	X	X	H	X	L	X	Drive Bus

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

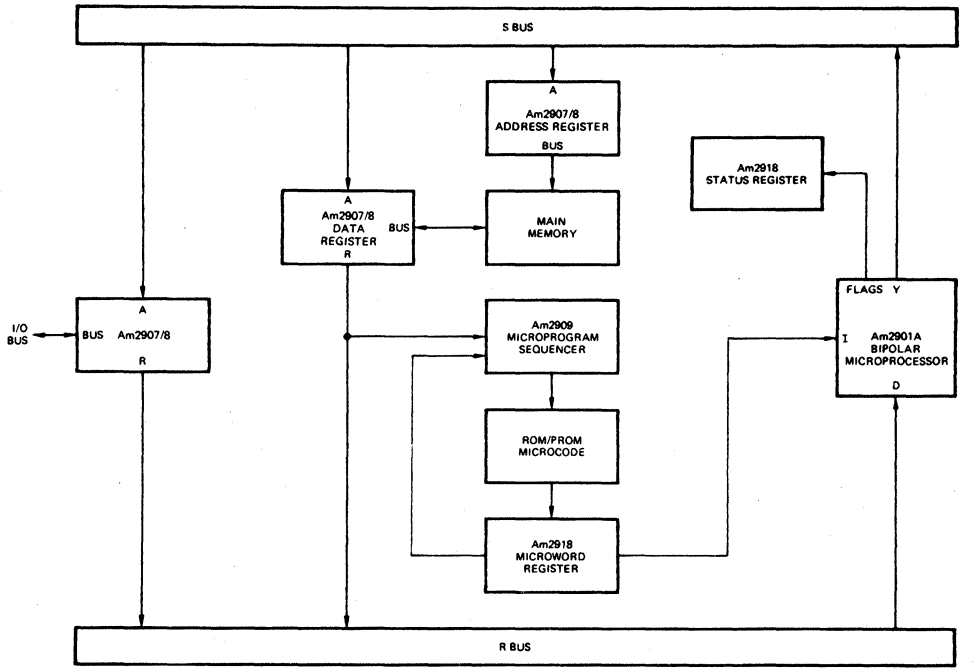
PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

05399A

Refer to Page 13-1 for Essential Information on Military Devices

APPLICATIONS



AF001000

The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus 200mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)(	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX, All inputs = GND	Am2907		75	110	mA
			Am2908		80	120	
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	

05399A

Refer to Page 13-1 for Essential Information on Military Devices

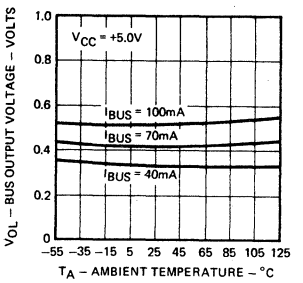
BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V	Am2907	MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
			Am2908	MIL	1.9	1.5		
				COM'L	1.7	1.5		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V	Am2907	MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	
			Am2908	MIL		1.5	1.1	
				COM'L		1.5	1.3	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts

5

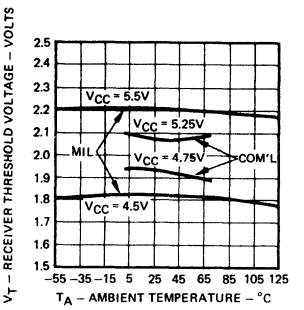
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



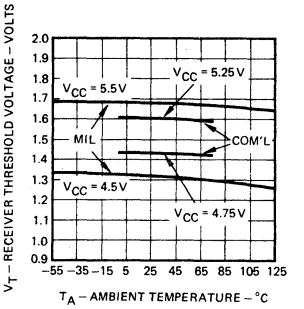
OP001340

Am2907 Receiver Threshold Variation Versus Ambient Temperature



OP001330

Am2908 Receiver Threshold Variation Versus Ambient Temperature

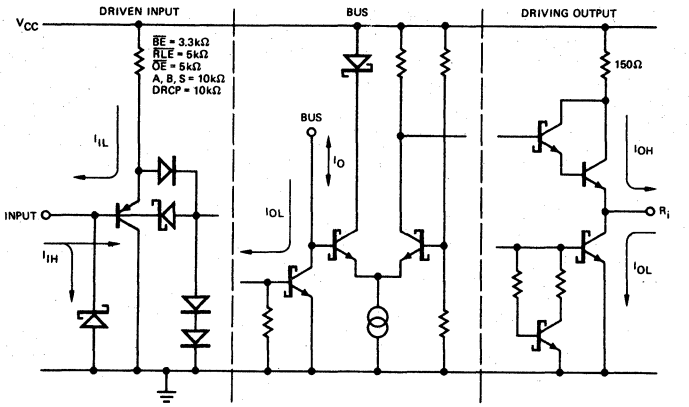


OP001420

05399A

Refer to Page 13-1 for Essential Information on Military Devices

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2907 Min	COMMERCIAL Am2907 Typ (Note 1)	COMMERCIAL Am2907 Max	MILITARY Am2907 Min	MILITARY Am2907 Typ (Note 1)	MILITARY Am2907 Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 50 Ω		21	36		21	40	ns
t_{PLH}				21	36		21	40	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{PLH}				13	23		13	26	
t_s	Data Inputs	C_L = 15 pF, R_L = 2.0 kΩ	15			18			ns
t_h			7.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		25			28			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	34		18	37	ns
t_{PHL}				18	34		18	37	
t_{PLH}	Latch Enable to Receiver Output			21	34		21	37	ns
t_{PHL}				21	34		21	37	
t_s	Bus to Latch Enable ($\overline{RLE}$)		18			21			ns
t_h			5.0			7.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{ZH}	Output Control to Output			14	25		14	28	ns
t_{ZL}				14	25		14	28	
t_{HZ}	Output Control to Output	C_L = 5.0 pF, R_L = 2.0 kΩ		14	25		14	28	ns
t_{LZ}				14	25		14	28	

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

05399A

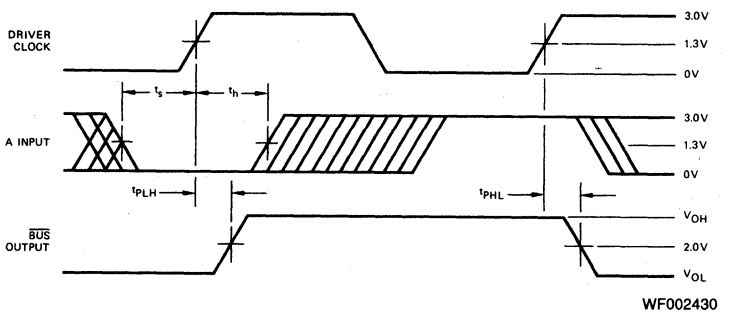
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2908 Min	COMMERCIAL Am2908 Typ (Note 1)	COMMERCIAL Am2908 Max	MILITARY Am2908 Min	MILITARY Am2908 Typ (Note 1)	MILITARY Am2908 Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF R_L (BUS): 91 Ω to V_{CC} 200 Ω to GND		21	36		21	40	ns
t_{PLH}				21	36		21	40	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{PLH}				13	23		13	26	
t_r	Bus Output Rise Time		7	10		5	10		ns
t_f	Bus Output Fall Time		4	6		3	6		
t_s	Data Inputs		15			18			ns
t_h			7.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		25			28			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 50 pF R_L = 2.0 kΩ		18	35		18	38	ns
t_{PHL}				18	35		18	38	
t_{PLH}	Latch Enable to Receiver Output			21	35		21	38	ns
t_{PHL}				21	35		21	38	
t_s	Bus to Latch Enable ($\overline{RLE}$)		18			21			ns
t_h			5.0			7.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)	C_L = 15 pF R_L = 2.0 kΩ		21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{ZH}	Output Control to Output			14	25		14	28	ns
t_{ZL}				14	25		14	28	
t_{HZ}	Output Control to Output	C_L = 5.0 pF R_L = 2.0 kΩ		14	25		14	28	ns
t_{LZ}				14	25		14	28	

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.

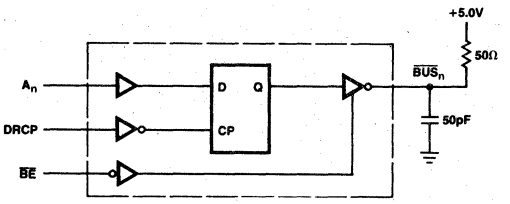
SWITCHING WAVEFORMS



WF002430

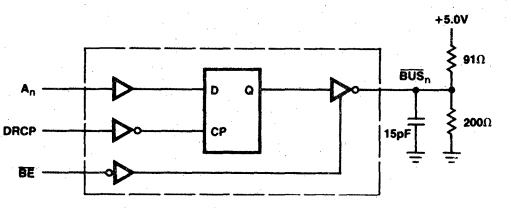
INPUT SET-UP AND HOLD TIMES.

SWITCHING TEST CIRCUIT



TC000950

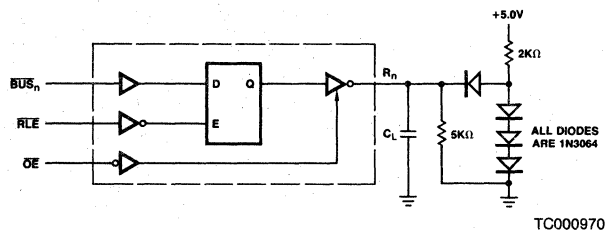
Am2907
DRIVER SWITCHING TEST CIRCUIT



TC000960

Am2908
DRIVER SWITCHING TEST CIRCUIT

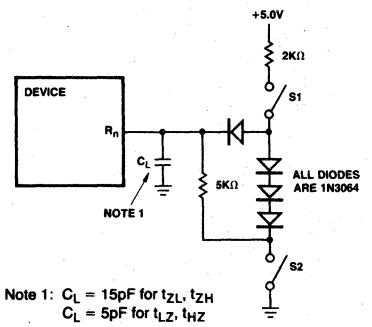
SWITCHING TEST CIRCUIT



TC000970

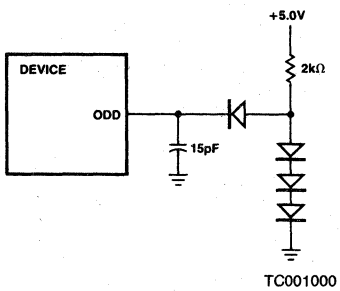
Note: C_L = 15pF for Am2907
C_L = 50pF for Am2908

Am2907/08 RECEIVER SWITCHING TEST CIRCUIT.



TC000990

LOAD FOR RECEIVER TRI-STATE TEST



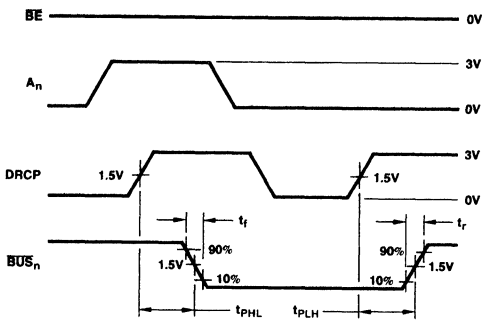
TC001000

LOAD FOR PARITY OUTPUT

05399A

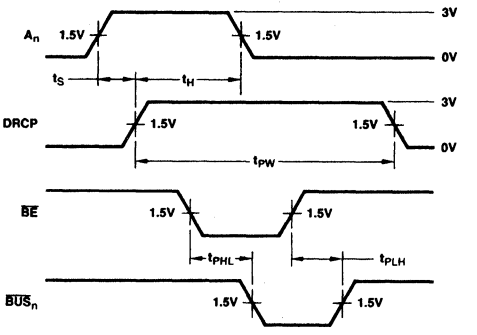
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



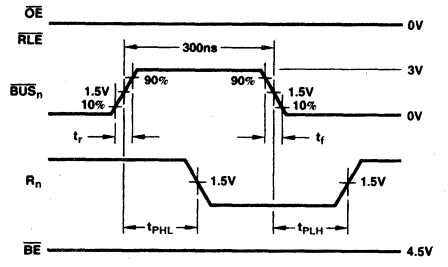
WF002340

DRIVER CLOCK (DRCP) TO BUS



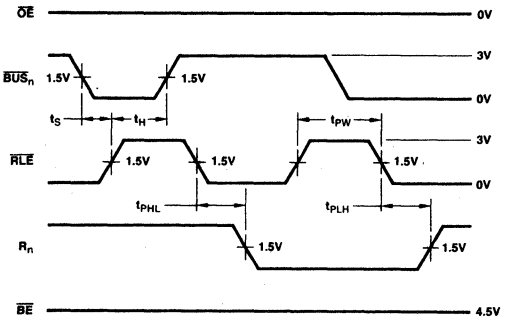
WF002330

BUS ENABLE ($\overline{BE}$) TO BUS



WF002370

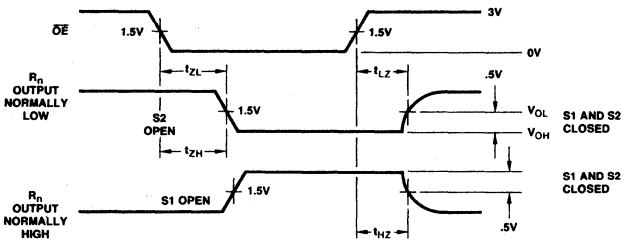
BUS TO RECEIVER OUTPUT (LATCH ENABLED)



WF002360

LATCH ENABLE TO RECEIVER OUTPUT

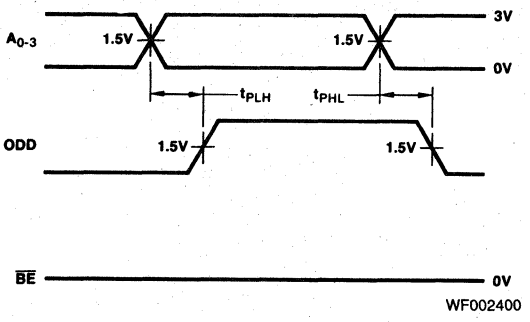
SWITCHING WAVEFORMS



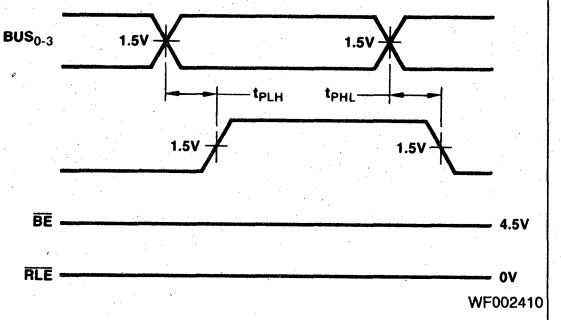
WF002420

RECEIVER TRI-STATE WAVEFORMS

05399A



A INPUT TO PARITY OUTPUT



BUS TO PARITY OUTPUT

Am2909A/Am2911A

Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to form longer word width
- Branch input for N-way branches
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only)
- Am2909 in 28-pin package & Am2911A in 20-pin package

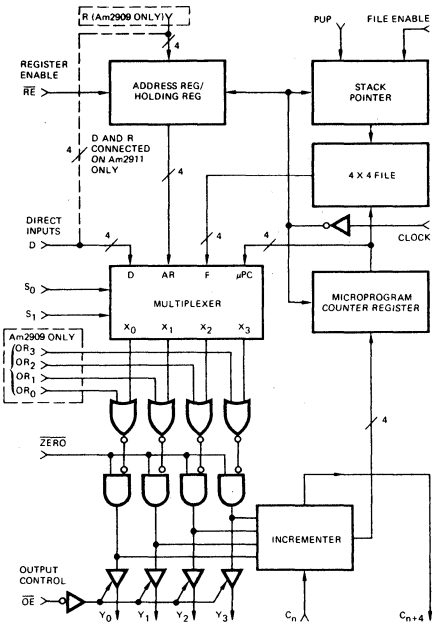
GENERAL DESCRIPTION

The Am2909A is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909As may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909A can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911A is an identical circuit to the Am2909A, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911A is in a 20-pin, 0.3″ centers package.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



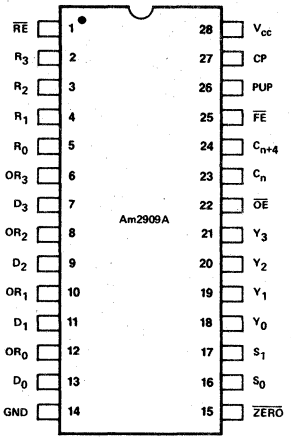
BD002171

03578B

Refer to Page 13-1 for Essential Information on Military Devices

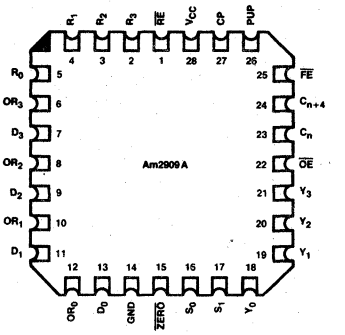
CONNECTION DIAGRAM
Top View

P-28, D-28



CD004332

CHIP-PAK™ L-28-1



CD004311

Note: Pin 1 is marked for orientation

RELATED PRODUCTS

Part No.	Description
Am2918	Pipeline Register
Am2922	Condition Code MUX
Am29803A	16-Way Branch Control Unit
Am29811A	Next Address Control
Am25LS163	4-Bit Counter
Am27S35	Registered PROM

For applications information, see Chapter 11 of **Bit Slice Microprocessor Design,** Mick & Brick, McGraw Hill Publications.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2909A
Am2911A

D — Package
D – 28-pin CERDIP
F – 28-pin flatpak
L – 28-pin leadless chip carrier
P – 28-pin plastic DIP
X – Dice

C — Temperature (See Operating Range)
C – Commercial (0°C to +70°C)
M – Military (–55°C to +125°C)

B — Screening Option
Blank – Standard processing
B – Burn-in

Device type
Microprogram Sequencers

Valid Combinations	
Am2909A Am2911A	PC DC, DCB, DMB FMB LC, LMB XC, XM

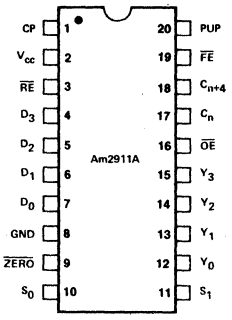
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a registered trademark of Advanced Micro Devices.

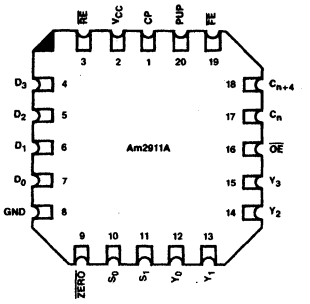
CONNECTION DIAGRAM
Top View

P-20,D-20



CD004321

CHIP PAK™ L-20-1

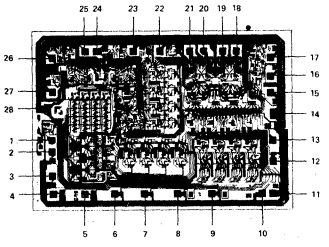


CD004301

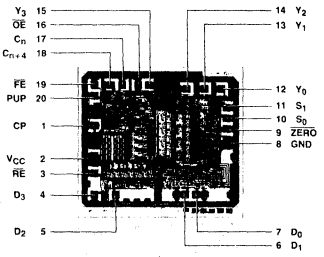
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

Am2909A

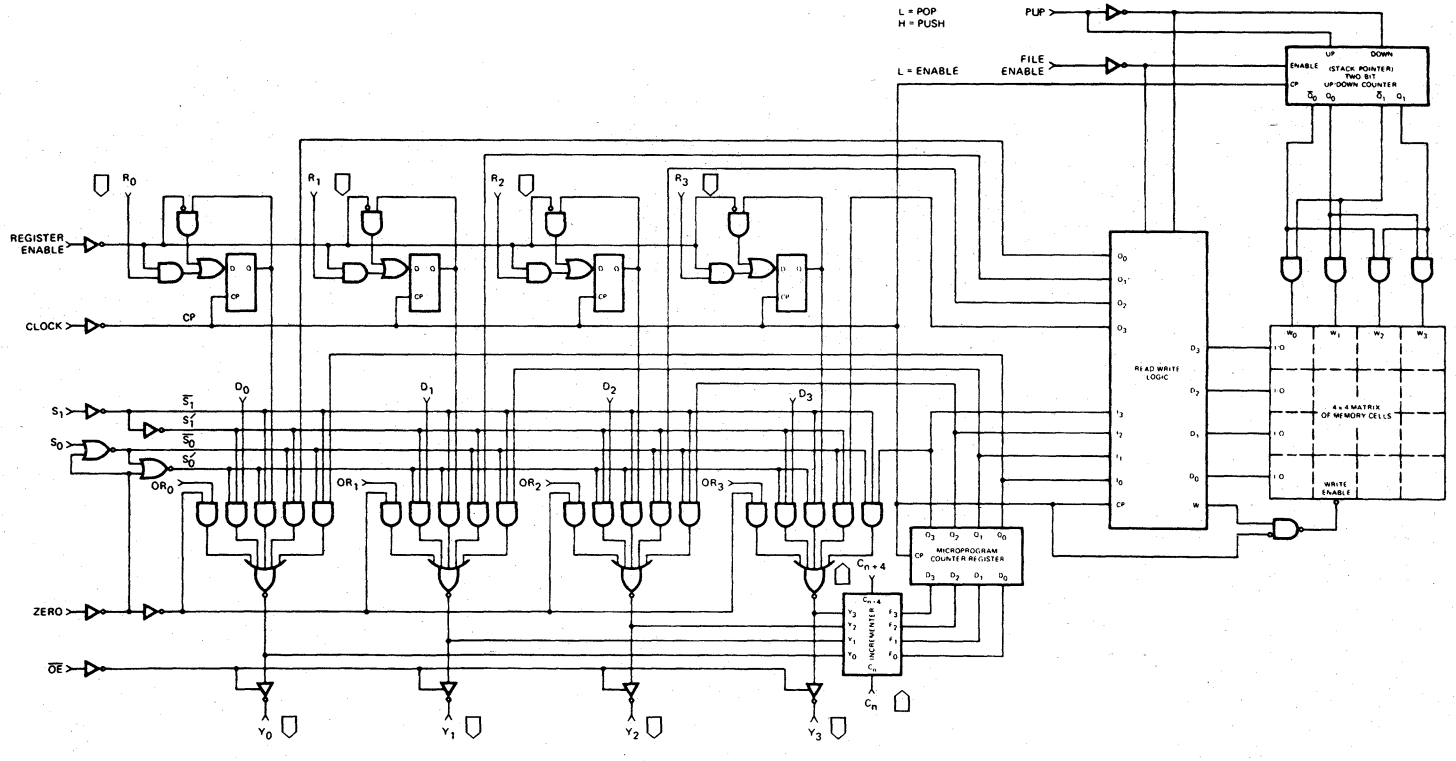


Am2911A



DIE SIZE 86 x 98 Mils

Chip-Pak is a register trademark of Advanced Micro Devices.



Note: R_i and D_i connected together on Am2911A and OR_i removed.

BD002092

Figure 1. Microprogram Sequencer Block Diagram.

USE ▷— FOR INPUT SIGNALS

USE —◁ FOR OUTPUT SIGNALS

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
17, 16/11, 10	S_1, S_0	I	Control lines for address source selection.
25, 26/19, 20	$\overline{FE}$, PUP	I	Control lines for push/pop stack.
1/3	$\overline{RE}$	I	Enable line for internal address register.
6, 8, 10, 12	OR_i	I	Logic OR inputs on each address output line. (2909A ONLY)
15/9	$\overline{ZERO}$	I	Logic AND input on the output lines.
22/16	$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance).
23/17	C_n	I	Carry-in to the incrementer.
2, 3, 4, 5	R_i	I	Inputs to the internal address register. (2909A ONLY)
7, 9, 11, 13/4-7	D_i	I	Direct inputs to the multiplexer.
27/1	CP	I	Clock input to the AR and μPC register and Push-Pop stack.
18-21/12-15	Y_i	O	Address outputs from Am2909A. (Address inputs to control memory.)
24/18	C_{n+4}	O	Carry out from the incrementer

ARCHITECTURE OF THE Am2909A/ Am2911A

The Am2909A/Am2911A are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 1.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911A, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909A/Am2911A contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out ($C_n + 4$) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage – the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909A/Am2911A feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/ PROM.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{CC} = MIN V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA, 2909A/11A				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL, 2909A/11A			0.7	Volts
				All others			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	C_n				40	μA
			Push/Pop, $\overline{OE}$				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 6V V_{OUT} = 0.5V		Y_0-Y_3	−30		−100	mA
				C_{n+4}	−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 4)	COM'L Only	T_A = 0 to +70°C			130	mA
			MIL Only	T_C = −55 to +125°C			140	
				T_C = +125°C			110	
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.7	Y_0-3	V_{OUT} = 0.4V			−20	μA
I_{OZH}				V_{OUT} = 2.7V			20	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2 and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. For the Am2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

Am2909A/Am2911A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II and III below define the timing characteristics of the Am2909A/Am2911A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

(all in ns, C_L = 50pF (except output disable tests))

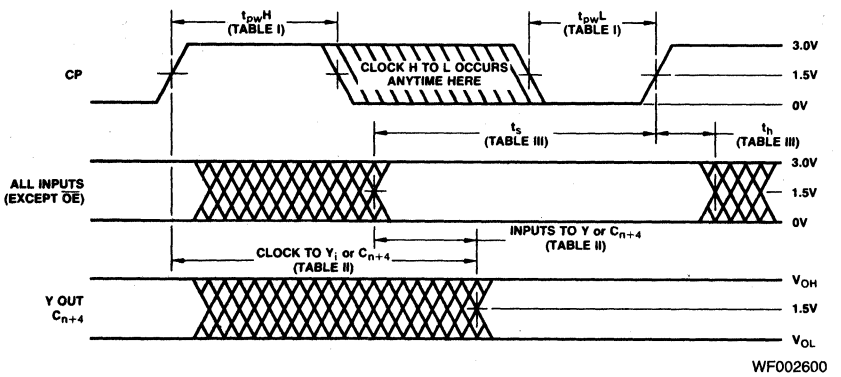
From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	22	20	25
S_0, S_1	29	34	29	34
OR_i	17	22	20	25
C_n	–	14	–	16
$\overline{ZERO}$	29	34	30	35
OE LOW (enable)	25	–	25	–
OE HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	39	44	45	50
Clock ↑ S_1S_0 = LL	39	44	45	50
Clock ↑ S_1S_0 = HL	44	49	53	58

*C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		19	4	19	5
R_i	2	10	4	12	5
PUP		25	4	27	5
$\overline{FE}$		25	4	27	5
C_n		18	4	18	5
D_I		25	0	25	0
OR_i		25	0	25	0
S_0, S_1		25	0	29	0
$\overline{ZERO}$		25	0	29	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911A, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



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Refer to Page 13-1 for Essential Information on Military Devices

OPERATION OF THE Am2909A/Am2911A

Figure 2 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 2 also shows the truth table for the output control and for the control of the push/pop stack. Figure 3 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909A. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
L	L	Microprogram Counter	μPC
L	H	Address/Holding Register	AR
H	L	Push-Pop stack	STK0
H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 2.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	L L L L	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End
N + 1	—	J + 1	K	Rb	Rc	Rd	Ra	—		Loop
N	L L L H	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up
N + 1	—	J + 1	K	J	Ra	Rb	Rc	—		Loop
N	L L H X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N + 1	—	J + 1	K	Ra	Rb	Rc	Rd	—		
N	L H L L	J	K	Ra	Rb	Rc	Rd	K	Pop Stack;	End
N + 1	—	K + 1	K	Rb	Rc	Rd	Ra	—	Use AR for Address	Loop
N	L H L H	J	K	Ra	Rb	Rc	Rd	K	Push μPC;	JSR AR
N + 1	—	K + 1	K	J	Ra	Rb	Rc	—	Jump to Address in AR	
N	L H H X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N + 1	—	K + 1	K	Ra	Rb	Rc	Rd	—		
N	H L L L	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	RTS
N + 1	—	Ra + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	H L L H	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	
N + 1	—	Ra + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	H L H X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref
N + 1	—	Ra + 1	K	Ra	Rb	Rc	Rd	—		(Loop)
N	H H L L	J	K	Ra	Rb	Rc	Rd	D	Pop Stack;	End
N + 1	—	D + 1	K	Rb	Rc	Rd	Ra	—	Jump to Address on D	Loop
N	H H L H	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	JSR D
N + 1	—	D + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	H H H X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N + 1	—	D + 1	K	Ra	Rb	Rc	Rd	—		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STKO is the location addressed by the stack pointer.

Figure 3. Output and Internal Next-Cycle Register States for Am2909A/Am2911A.

Figure 4 illustrates the execution of a subroutine using the Am2909A. The configuration of Figure 6 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also control (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909A at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909A inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. Figure 5 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J – 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_6	J + 3	–
T_7	J + 4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A + 1	–
T_5	A + 2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Am2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	–	–	–	J + 3	J + 3	J + 3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909A Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1	**JSR A**	I(A)	I(A + 1)	**RTS**	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**RTS**	I(J + 3)	I(J + 4)		

C_N = HIGH

Figure 4. Subroutine Execution.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J – 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_9	J + 3	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A + 1	–
T_5	A + 2	JSR B
T_7	A + 3	–
T_8	A + 4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Am2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	–	–	–	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	–
	STK1	–	–	–	–	–	–	J + 3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909A Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**JSR B**	**RTS**	I(A + 3)	**RTS**	I(J + 3)	I(J + 4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**JSR B**	**RTS**	I(A + 3)	**RTS**	I(J + 3)

C_N = HIGH

Figure 5. Two Nested Subroutines. Routine B is Only One Instruction.

USING THE Am2909A AND Am2911A

The Am2909A and Am2911A are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909A and Am2911A apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909A or Am2911A should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909A or Am2911A is shown in Figure 6. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909A or Am2911A. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

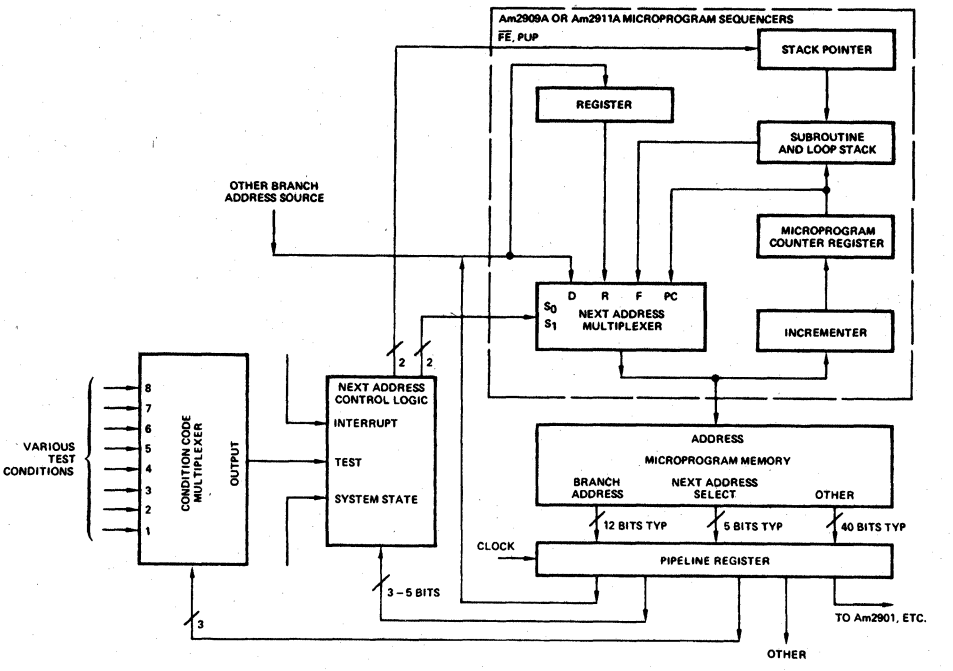


Figure 6. Recommended Computer Control Unit Architecture Using the Am2911A or Am2909A.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909A or an Am2911A. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 7 shows the CCU of Figure 6 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911A, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 8, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

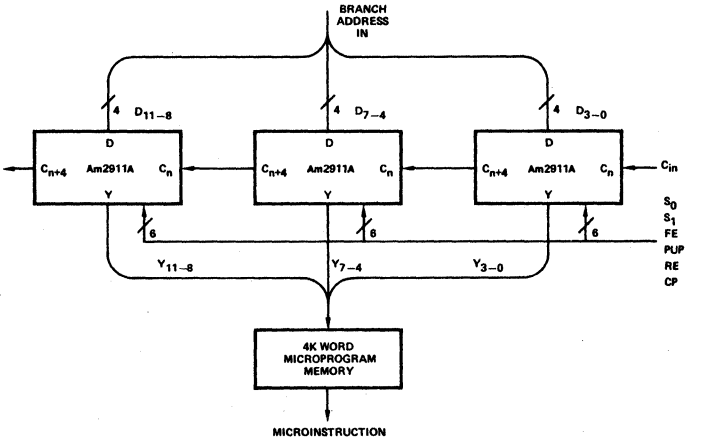


Figure 9. Twelve Bit Sequencer.

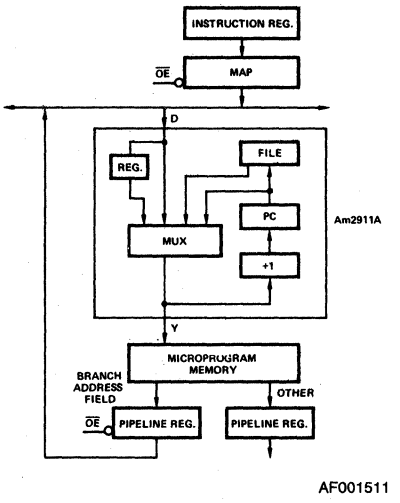


Figure 10. Branch Address Structures.

Expansion of the Am2909A or Am2911A

Figure 9 shows the interconnection of three Am2911A's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911A Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911A output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909A and Am2911A

The difference between the Am2909A and the Am2911A involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909A, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911A, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 10. Using the Am2909A, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911A, it is more common to connect the Am2911A's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 10 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER			
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	CON JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CVJ	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR # 0	H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR # 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

Figure 8. AM29811A TRUTH TABLE

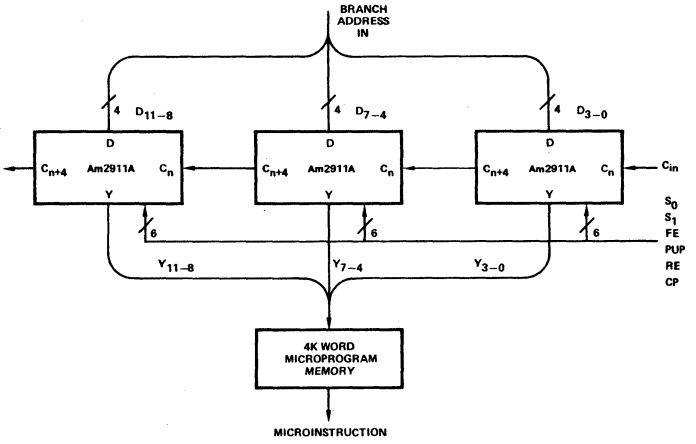


Figure 9. Twelve Bit Sequencer.

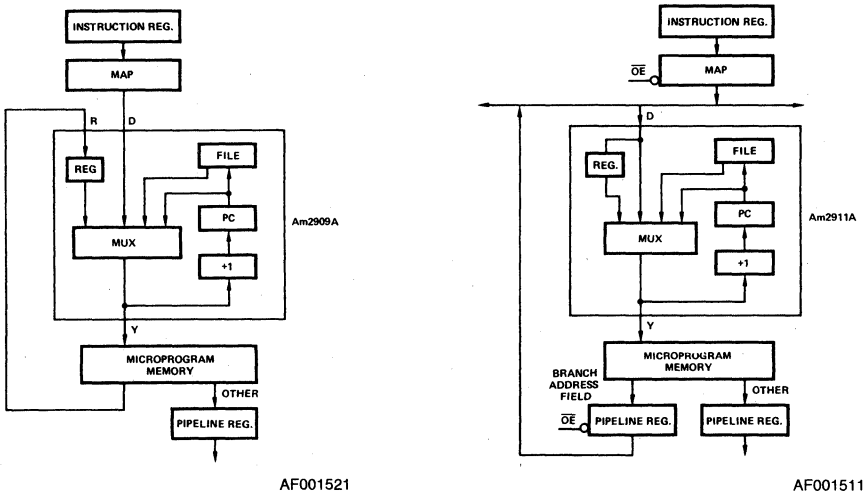
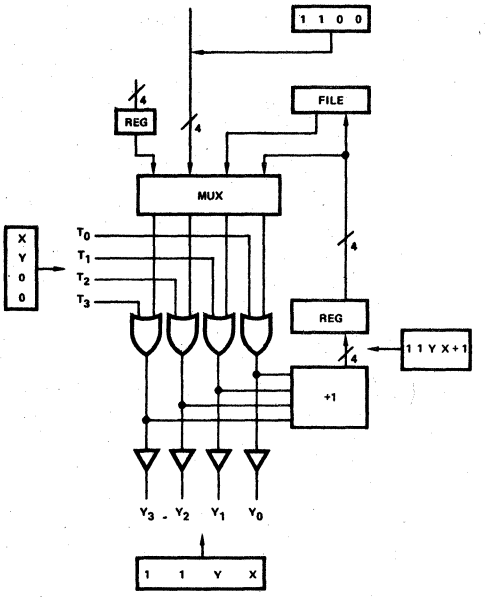


Figure 10. Branch Address Structures.

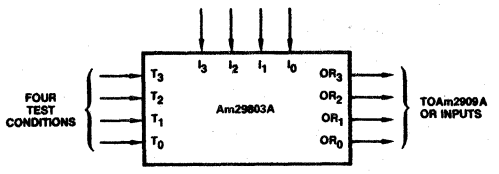
The second difference between the Am2909A and Am2911A is that the Am2909A has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 11. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 11, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.



AF001610

Figure 11. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909A. Figure 12 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909A for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911A's for the remainder of the bits. A detailed logic design for such a system is contained in "The Microprogramming Handbook."



AF001601

Figure 12.

How to Perform Some Common Functions with the Am2909A or Am2911A

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	H	L	L	H	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	H	H	H	H	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	H	H	H	L	H

Subroutine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	H	H	L	L	L

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803 FUNCTION TABLE

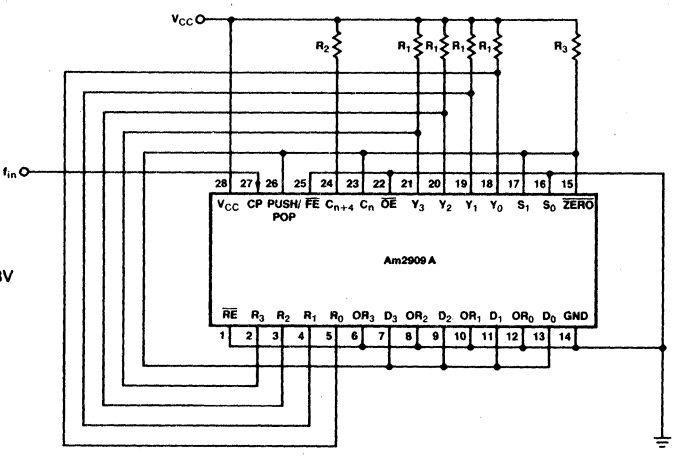
	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

Burn-In Circuit for Am2909A (Flatpack and CERDIP)

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



BC000011

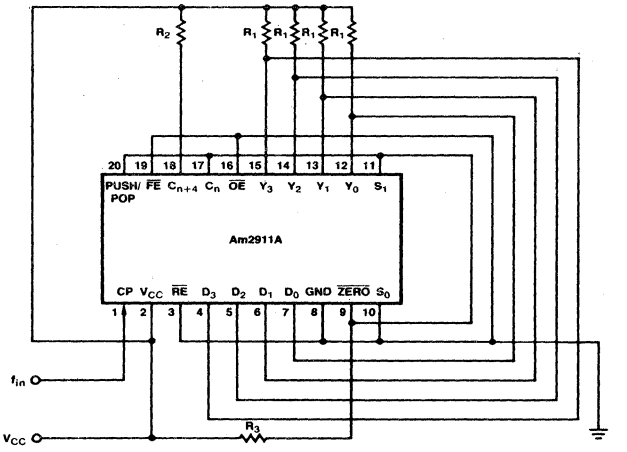
This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

Burn-in Circuit for Am2911A

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

From clock buffer on each board:
V_{CC} min. = 5.0V
V_{CC} max. = 5.1V

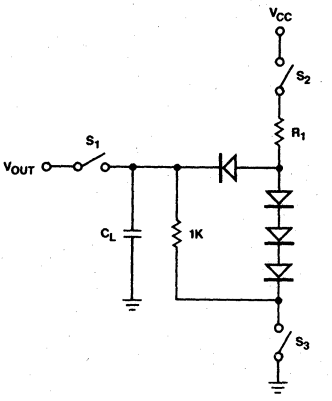


BC000021

This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

SWITCHING TEST CIRCUIT

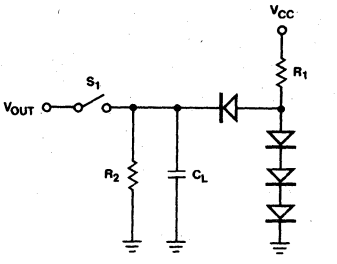
A. THREE-STATE OUTPUTS



TC001140

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



TC001150

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. S_1, S_2, S_3 are closed during function tests all and AC tests except output enable tests.
3. S_1 and 3_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS

			Am2909A	
Pin #	**Pin Label**	**Test Circuit**	**R_1**	**R_2**
18-21	Y_{0-3}	A	220	1K
24	C_{n+4}	B	220	2.4K

TEST OUTPUT LOADS

			Am2911A	
Pin #	**Pin Label**	**Test Circuit**	**R_1**	**R_2**
12-15	Y_{0-3}	A	220	1K
18	C_{n+4}	B	220	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2912

Quad Bus Transceiver

DISTINCTIVE CHARACTERISTICS

- Input to bus is inverting
- Quad high-speed open collector bus transceiver
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading

GENERAL DESCRIPTION

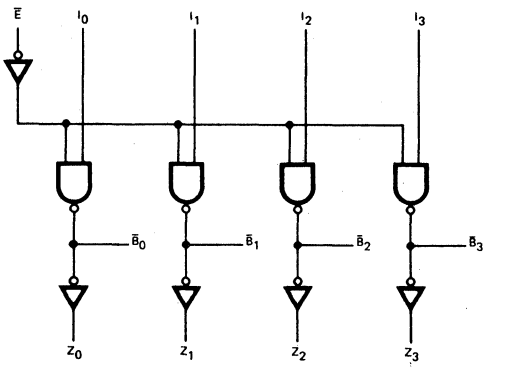
The Am2912 is a quad Bus Transceiver consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am2912 features advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

BLOCK DIAGRAM



BD002130

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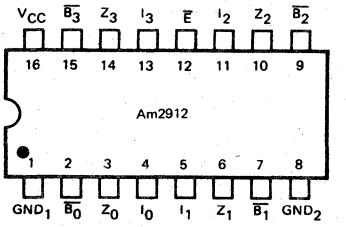
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

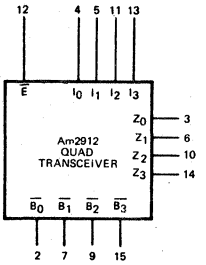
D-16-1



CD004260

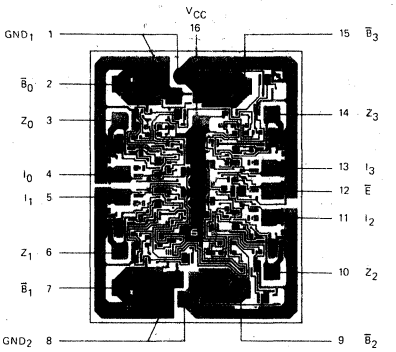
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000890

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.059″ x 0.075″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2912 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am2912** — Device type
  - Quad Bus Transceiver

Valid Combinations	
Am2912	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

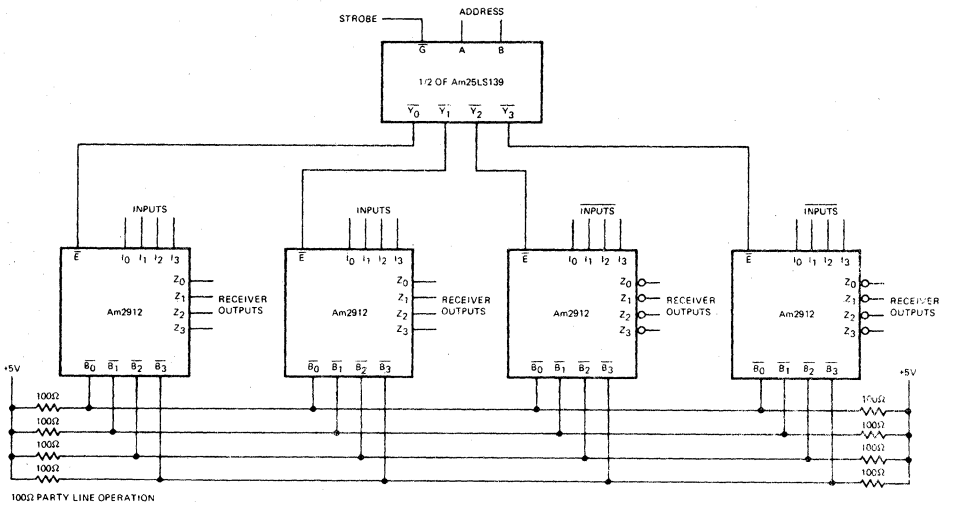
Pin No.	Name	I/O	Description
4, 5, 11, 13	I_0, I_1, I_2, I_3	I	The four driver inputs.
12	$\overline{E}$	I	Enable. When the Enable is HIGH, the four drivers are disabled.
2, 7, 9, 15	$\overline{B_0}$, $\overline{B_1}$, $\overline{B_2}$, $\overline{B_3}$	I/O	The four driver outputs and receiver inputs (data is inverted).
3, 6, 10, 14	Z_0, Z_1, Z_2, Z_3	O	The four receiver outputs. Data from the bus is inverted while data from the I inputs is non-inverted.

TRUTH TABLE

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

TYPICAL APPLICATION



AF001550

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus 200mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OH} = −1.0mA V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V	Enable			20	μA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX Enable = GND			45	70	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

05400A

Refer to Page 13-1 for Essential Information on Military Devices

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

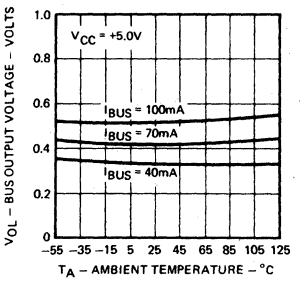
Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX		V_O = 0.8V			−50	
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	μA
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

5

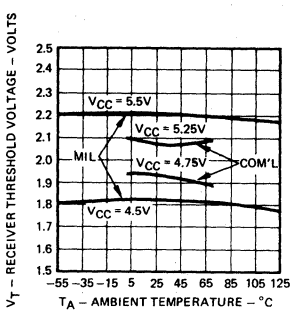
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



OP001460

Receiver Threshold Variation Versus Ambient Temperature



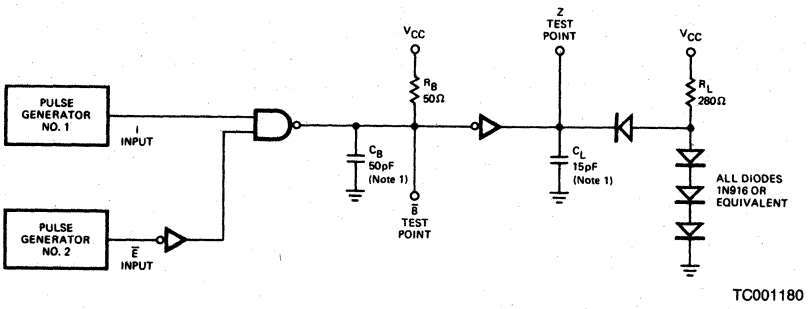
OP001470

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50 Ω, C_B = 50 pF (Note 1)		10	15	ns
t_{PHL}				10	15	
t_{PLH}	Enable Input to Bus			14	18	ns
t_{PHL}				13	18	
t_{PLH}	Bus to Receiver Out	R_B = 50 Ω, R_L = 280 Ω, C_B = 50 pF (Note 1), C_L = 15 pF		10	15	ns
t_{PHL}				10	15	
t_r	Bus	R_B = 50 Ω, C_B = 50 pF (Note 1)	4.0	10		ns
t_f	Bus		2.0	4.0		ns

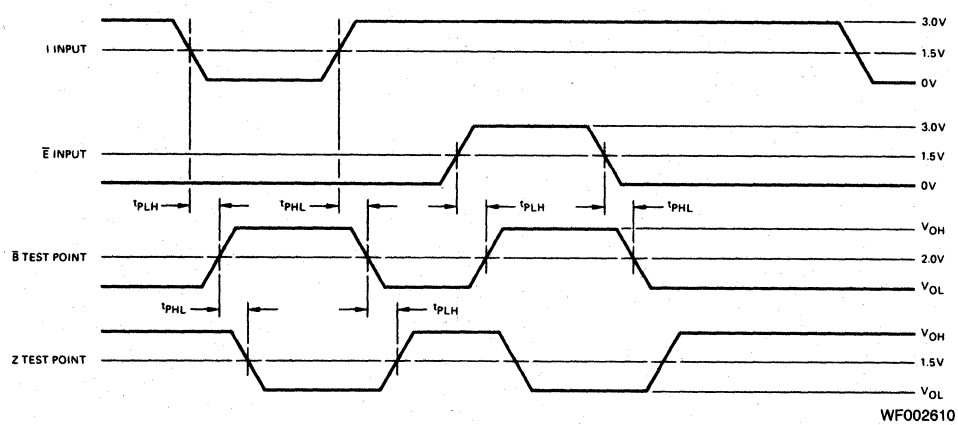
Note 1. Includes probe and jig capacitance.

SWITCHING TEST CIRCUIT



Note 1. Include Probe and Jig Capacitance.

SWITCHING WAVEFORMS



Am2913

Priority Interrupt Expander

DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148/2513
- Gated three-state output
- Advanced Low-Power Schottky processing

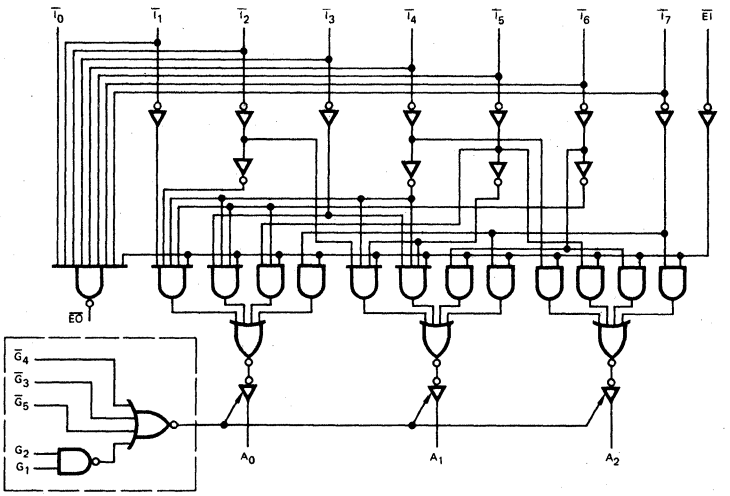
GENERAL DESCRIPTION

The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active $\overline{I}_7$ to $\overline{I}_0$. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input ($\overline{EI}$) and Enable Output ($\overline{EO}$).

One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

5

BLOCK DIAGRAM



BD001700

RELATED PRODUCTS

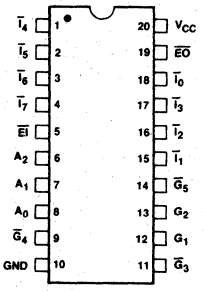
Part No.	Description
Am2914	Vectored Priority Interrupt Controller
Am25LS2513	8 to 3 Line Priority Encoder

03596A

Refer to Page 13-1 for Essential Information on Military Devices

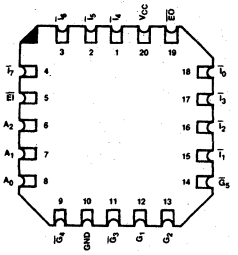
CONNECTION DIAGRAM
Top View

P-20, D-20



CD002030

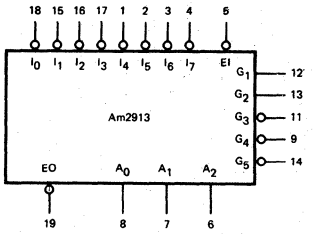
L-20-1



CD002020

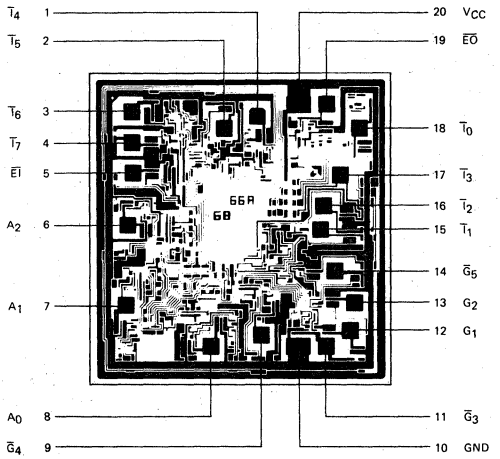
F-20 pin configuration identical to D-20, P-20.
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000760

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.082″ x 0.085″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2913 D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (−55°C to +125°C)
- D — Package: D – 20-pin CERDIP; F – 20-pin flatpak; L – 20-pin leadless chip carrier; P – 20-pin plastic DIP; X – Dice
- Am2913 — Device type: Priority Interrupt Expander

Valid Combinations	
Am2913	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

03596A

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
8, 7, 6	A0, A1, A2	O	Three-state, active high encoder outputs.
5	$\overline{EI}$	I	Enable input provided to allow cascaded operation.
19	$\overline{EO}$	O	Enable output provided to enable the next lower order priority chip.
12, 13	G_1, G_2	O	Active high three-state output controls.
11, 9, 14	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	O	Active low three-state output controls.
	$\overline{I}_{0-7}$	I	Active low encoder inputs.

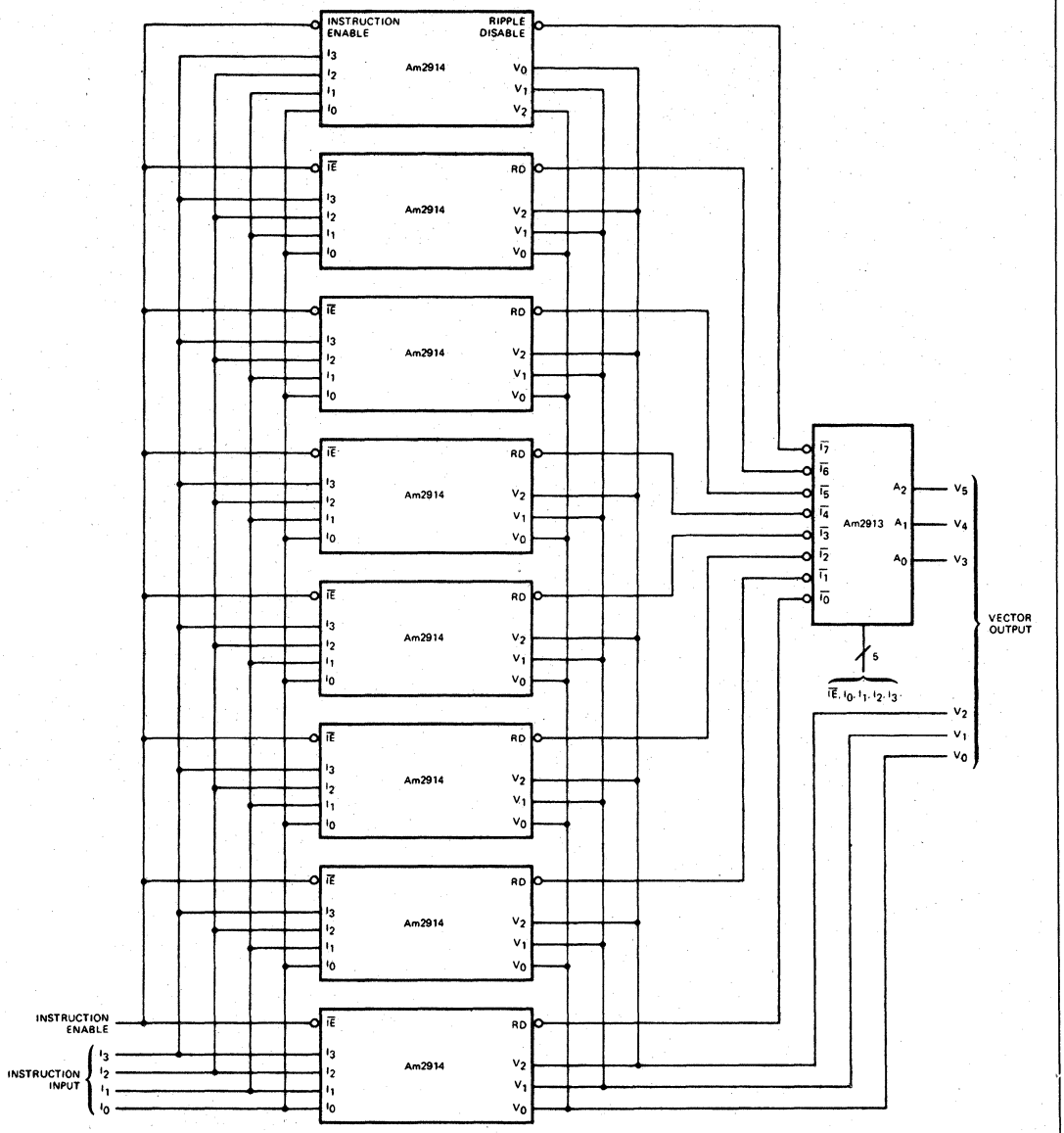
TRUTH TABLE

Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance



AF001300

Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

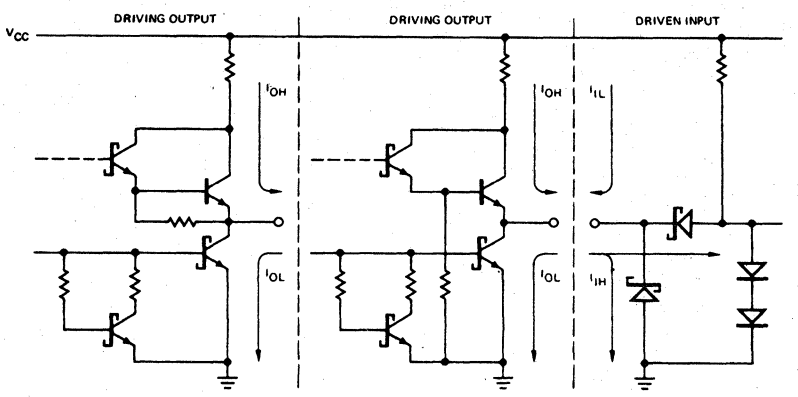
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA		2.4	3.2		
			$\overline{EO}$, I_{OH} = −440μA	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA(A_n Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH Voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{EI}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, $\overline{I}_0$				0.4	mA
			All others				0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{EI}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, $\overline{I}_0$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V	$\overline{EI}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, $\overline{I}_0$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX				15	24	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000710

Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)	$C_L = 15$ pF, $R_L = 2.0$ kΩ		17	25	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)			11	17	ns
t_{PHL}				12	18	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			7.0	11	ns
t_{PHL}				24	36	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			11	17	ns
t_{PHL}				23	34	
t_{PLH}	$\overline{EI}$ to A_n			12	18	ns
t_{PHL}				14	21	
t_{ZH}	G_1 or G_2 to A_n			23	40	ns
t_{ZL}				20	37	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			20	30	ns
t_{ZL}				18	27	
t_{HZ}	G_1 or G_2 to A_n	$C_L = 5.0$ pF, $R_L = 2.0$ kΩ		17	27	ns
t_{LZ}				19	28	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			16	24	ns
t_{LZ}				18	27	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am2913 Min	COMMERCIAL Am2913 Max	MILITARY Am2913 Min	MILITARY Am2913 Max	Units
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)	$C_L = 50$ pF, $R_L = 2.0$ kΩ		31		37	ns
t_{PHL}				30		34	
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)			22		27	ns
t_{PHL}				22		25	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			15		18	ns
t_{PHL}				48		60	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			19		21	ns
t_{PHL}				46		57	
t_{PLH}	$\overline{EI}$ to A_n			22		25	ns
t_{PHL}				27		32	
t_{ZH}	G_1 or G_2 to A_n			42		49	ns
t_{ZL}				43		49	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			36		43	ns
t_{ZL}				35		43	
t_{HZ}	G_1 or G_2 to A_n	$C_L = 5.0$ pF, $R_L = 2.0$ kΩ		34		40	ns
t_{LZ}				34		40	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			30		35	ns
t_{LZ}				31		35	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
Note: i = 0 to 7
n = 0 to 2

Am2914

Vectored Priority Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs –
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register –
  Six different operations can be performed on mask register
- Built-in status register –
  Status register holds code for lowest allowed interrupt
- Vectored output –
  Output is binary code for highest priority unmasked interrupt
- Expandable –
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable –
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming

GENERAL DESCRIPTION

The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the level-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

RELATED PRODUCTS

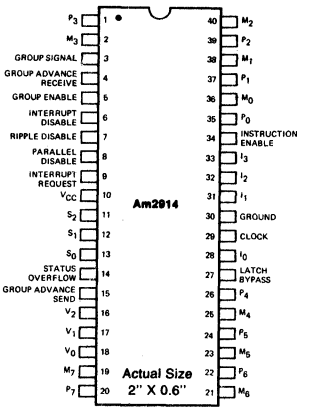
Part No.	Description
Am2902A	Carry Look-ahead Generator
Am2913	Priority Interrupt Expander
Am25LS138	3-to-8 Decoder
Am27S19	Mapping PROM

035768

Refer to Page 13-1 for Essential Information on Military Devices

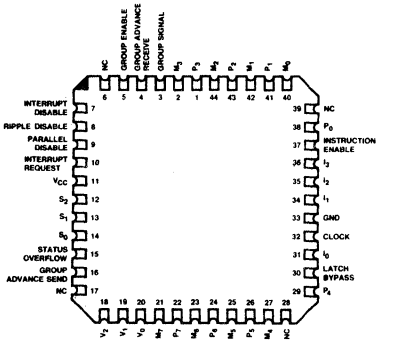
CONNECTION DIAGRAM
Top View

D-40-1



CD004210

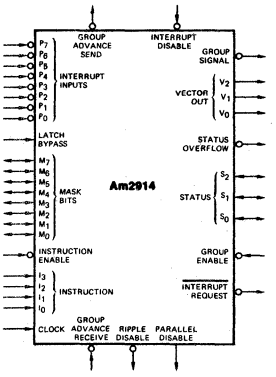
Chip Pak™ L-44-2



CD004220

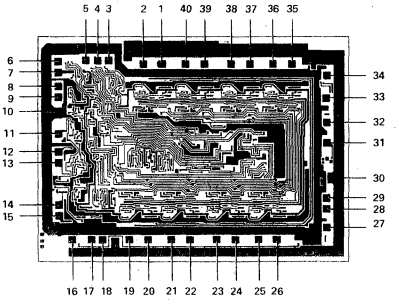
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000920

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.133″ x 0.187″

Numbers correspond to DIP pin-out.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2914 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 40-pin CERDIP
  - F – 42-pin flatpak*
  - L – 44-pin Chip Pak
  - X – Dice
- **Am2914** — Device type
  - Priority Interrupt Controller

*Note: Flatpak available for military only.

Valid Combinations	
Am2914	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip Pak is a registered trademark of Advanced Micro Devices.

BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded Interrupt Vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the Interrupt Vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

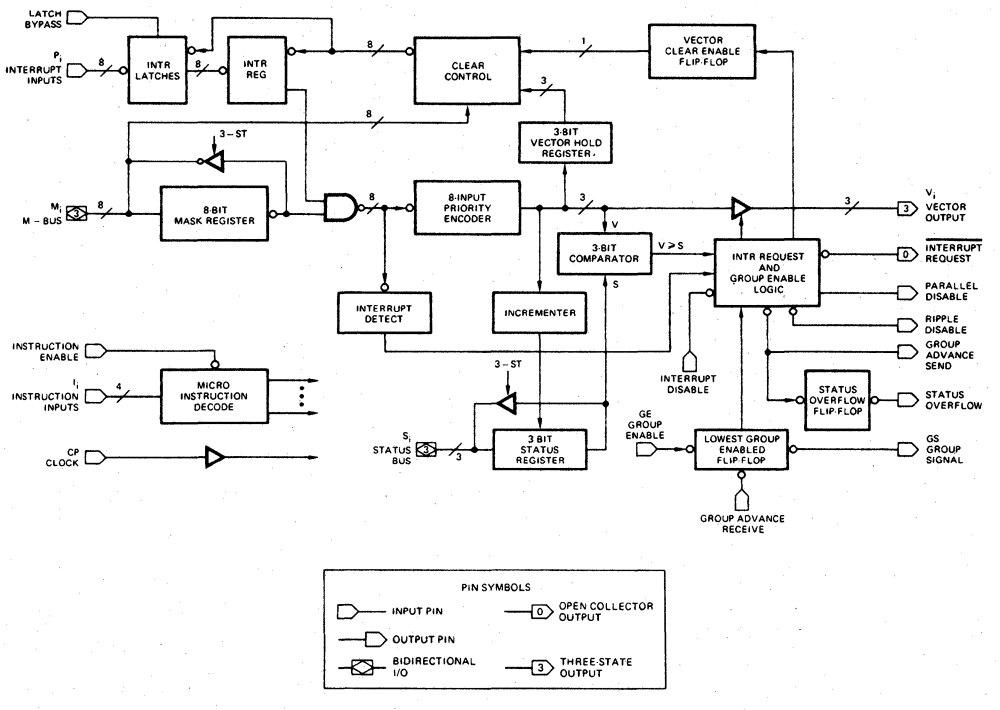
The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority Interrupt Vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

BLOCK DIAGRAM



BD001880

TABLE 1.

MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

$I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
1110	LDM	Load mask register from M bus
0111	RDM	Read mask register to M bus
1100	CLRM	Clear mask register (enables all priorities)
1000	SETM	Set mask register (inhibits all interrupts)
1010	BCLRM	Bit clear mask register from M bus
1011	BSETM	Bit set mask register from M bus
		Status Register Functions
1001	LDSTA	Load status register from S bus and LGE flip-flop from GE input
0110	RDSTA	Read status register to S bus
		Interrupt Request Control
1111	ENIN	Enable interrupt request
1101	DISIN	Disable interrupt request
		Vectored Output
0101	RDVC	Read vector output to V outputs, load V + 1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
0001	CLRIN	Clear all interrupts
0011	CLRMR	Clear interrupts from mask register data (uses the M bus)
0010	CLRMB	Clear interrupts from M bus data
0100	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0000	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

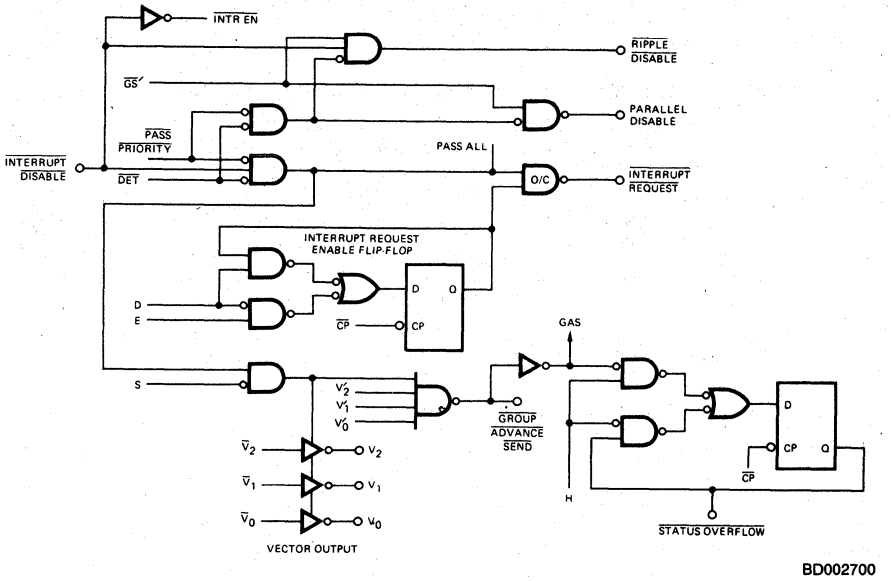


Figure 1. Interrupt Request Logic.

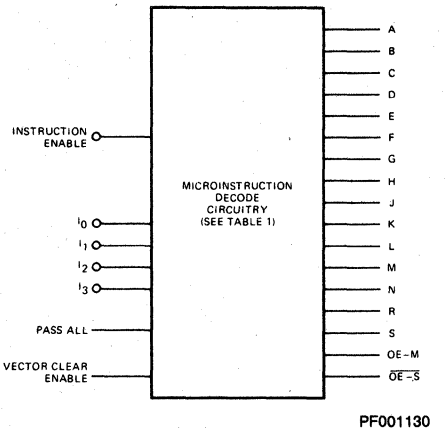


Figure 2.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +110°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN, V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I.\ D.}$				−2.0	
			$\overline{IE}$				−1.08	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{GE}$, $\overline{GAR}$				40	
			$\overline{IE}$				60	
			$\overline{I.\ D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = MAX	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
I_{OZH}			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = MAX	COM'L	0°C			305	mA
				70°C			250	
			MIL	−55°C			310	
				125°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

035768

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

(Group A, subgroup 10 and 11 tests and limits) All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0 and 3.0V. For Interrupt Request Output, $R_L = 390\Omega$, V_{LOAD} = 5.0V.

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE II. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	To Output											
	COMMERCIAL						MILITARY					
From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	SM Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE III. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

	COMMERCIAL							MILITARY						
Clock Path	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip–Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip–Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip–Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

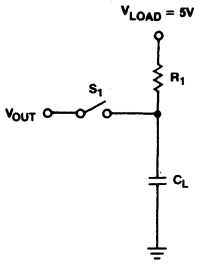
TABLE IV. SETUP AND HOLD TIME REQUIREMENTS (ns)
(All relative to clock LOW-to-HIGH transition)

	COMMERCIAL		MILITARY	
	Am2914		Am2914	
From Input	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
Irpt Disable	42	0	42	0
P_0-P_7 Hold Time Relative to LB	–	25	–	25

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

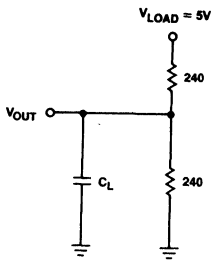
SWITCHING TEST CIRCUIT

C. OPEN-COLLECTOR OUTPUTS



TC001200

D. THREE-STATE OUTPUTS



TC001210

TEST OUTPUT LOAD FOR Am2914

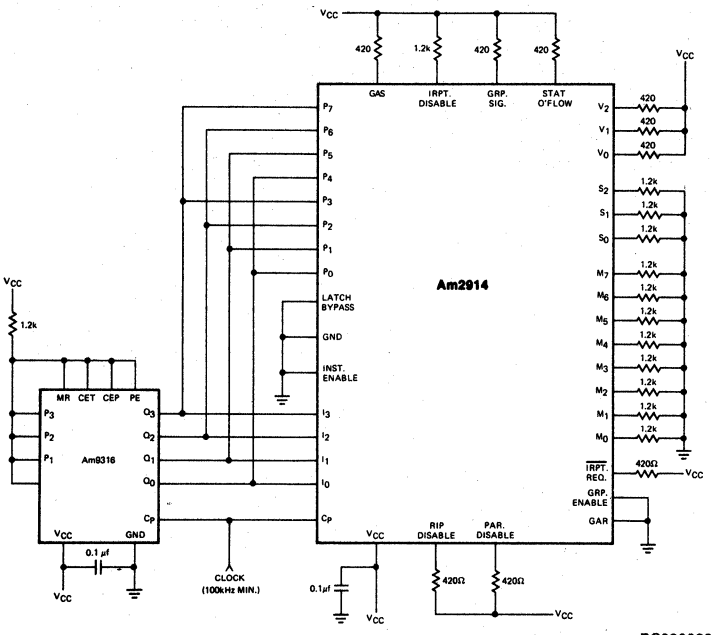
Pin #	Pin Label	Test Circuit	R_1	R_2
3	Group Signal	C	2K	–
4	Group Advance Receive	C	2K	–
7	Ripple Disable	C	2K	–
8	Parallel Disable	C	2K	–
9	Interrupt Request	C	390	–
13-11	S_{0-2}	D	240	240
14	Status Overflow	C	2K	–
18-16	V_{0-2}	D	240	240
–	M_{0-7}	D	240	240

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

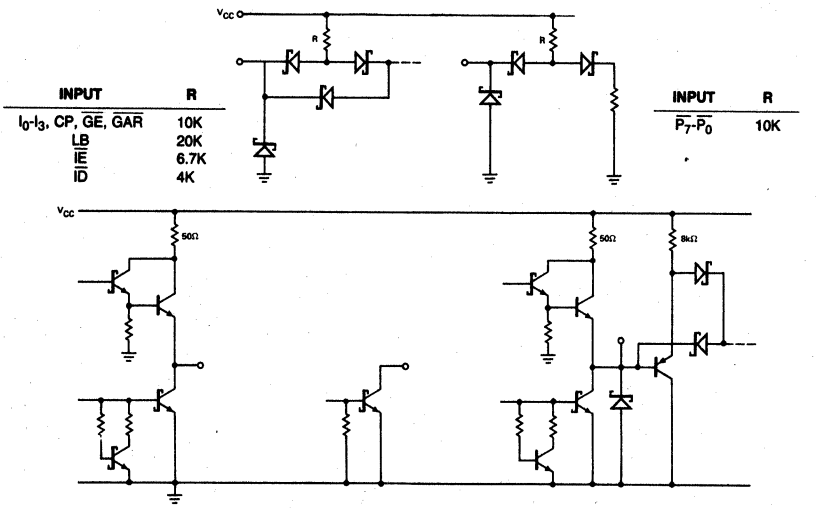
1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2914 Burn-in Circuit



BC000030

INPUT/OUTPUT CIRCUITS



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
LB	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K

OUTPUTS	
V_0-V_3	$\overline{SO}$
$\overline{GAS}$	PD
$\overline{GS}$	$\overline{RD}$

OUTPUT
$\overline{IR}$

OUTPUTS
M_0-M_7
S_0-S_3

IC000450

Am2915A

Quad Three-State Bus Transceiver with Interface Logic

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Three-state bus driver output can sink 48mA at 0.5V max.
- Two-port input to D-type register on driver
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

GENERAL DESCRIPTION

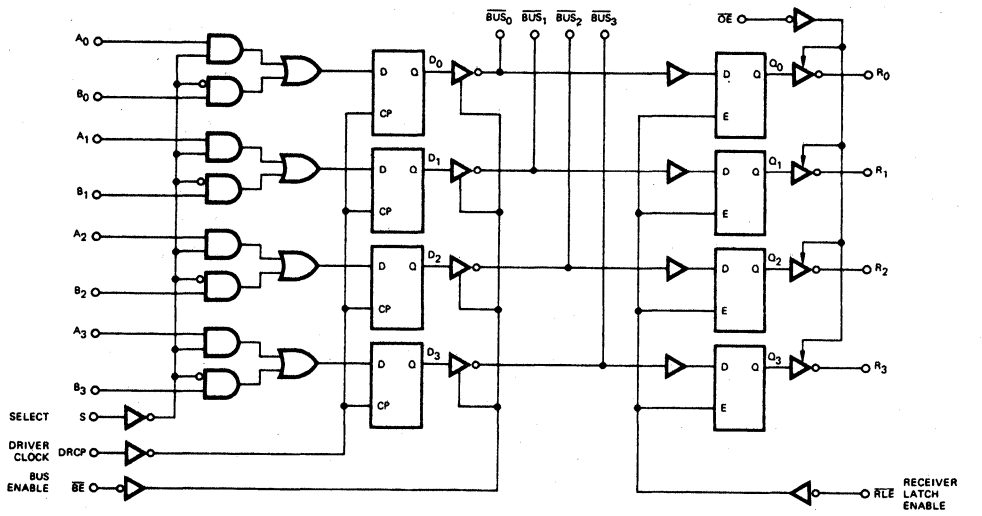
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input (BE) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and low-power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

BLOCK DIAGRAM



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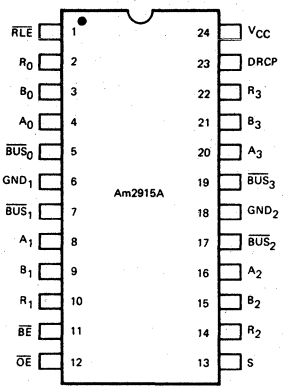
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

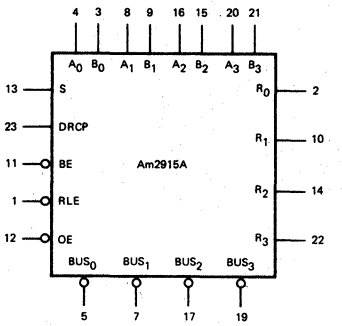
D-24-1



CD003010

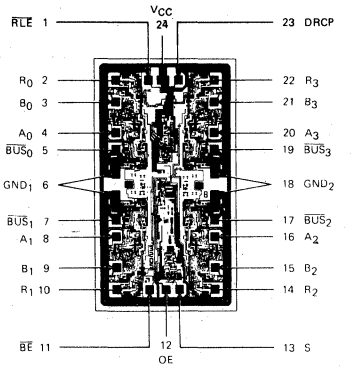
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000780

METALLIZATION AND PAD LAYOUT



DIE SIZE .074" x 0.130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2915A D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 24-pin CERDIP; F– 24-pin flatpak; P– 24-pin plastic DIP; X– Dice
- Am2915A — Device type: Quad 3-state Bus Transceiver

Valid Combinations	
Am2915A	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

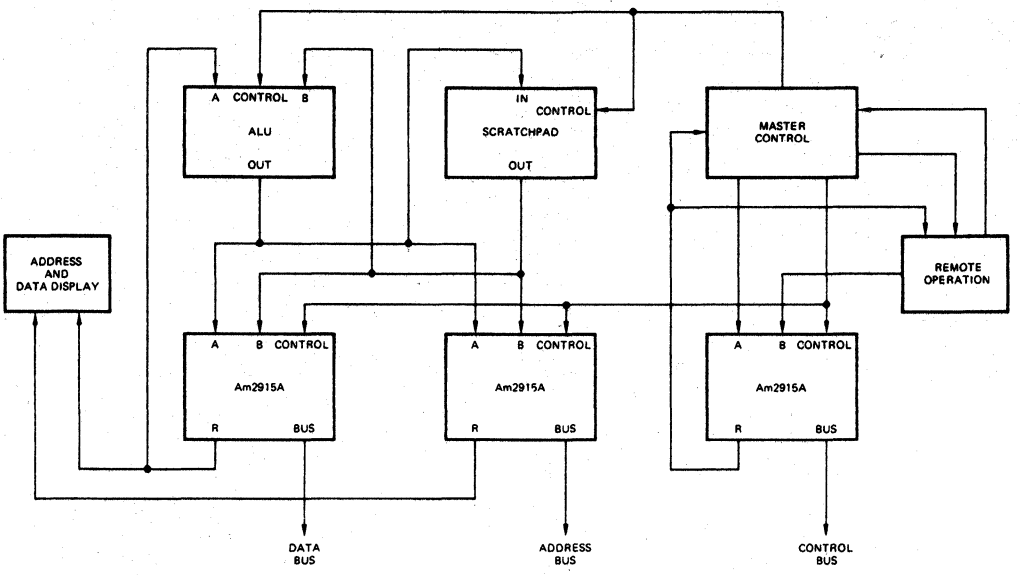
Pin No.	Name	I/O	Description
8, 16, 20	A_0, A_1, A_2, A_3	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9, 15, 21	B_0, B_1, B_2, B_3	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
11	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
5, 7, 17, 19	$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 10, 14, 22	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	$\overline{OE}$	O	Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	FUNCTION
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and
X	X	X	X	H	L	L	X	H	H	L	receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

APPLICATIONS



AF001010

The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7V
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Output Current, Into Bus 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100µA		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 7.0V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX	V_O = 2.4V			50	µA
			V_O = 0.4V			−50	

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

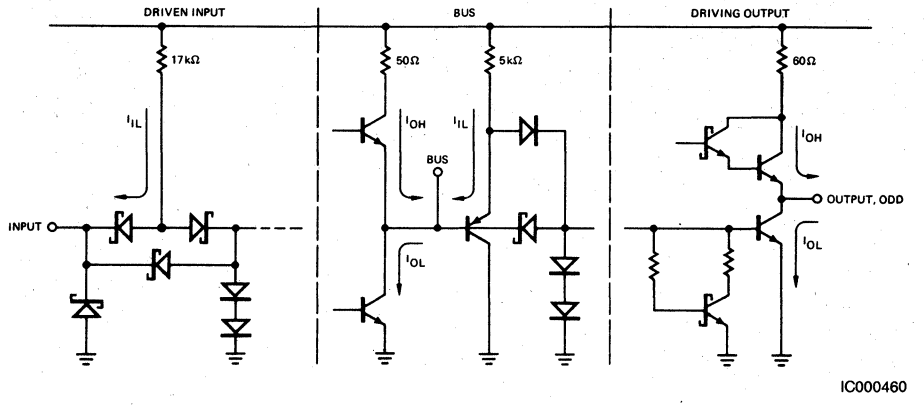
BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)		Min	Typ	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX, Bus enable = 2.4V	V_O = 0.4V			−200	µA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	µA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50	−120	−225	mA

05401A

Refer to Page 13-1 for Essential Information on Military Devices

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



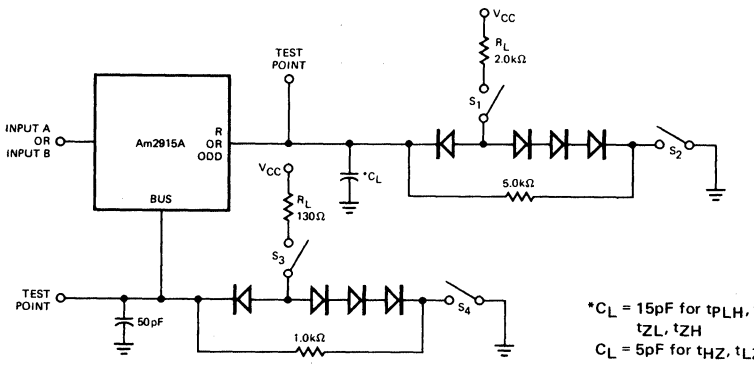
Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2915A Min	COMMERCIAL Am2915A Typ. (Note 1)	COMMERCIAL Am2915A Max	MILITARY Am2915A Min	MILITARY Am2915A Typ. (Note 1)	MILITARY Am2915A Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130 Ω		21	32		21	36	ns
t_{PLH}				21	32		21	36	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{HZ}, t_{LZ}				13	18		13	21	
t_s	Data Inputs (A or B)	C_L = 15 pF, R_L = 2.0 kΩ	12			15			ns
t_h			6.0			8.0			
t_s	Select Input (S)		25			28			ns
t_h			6.0			8.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		17			20			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	30		18	33	ns
t_{PHL}				18	27		18	30	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	33	ns
t_{PHL}				21	27		21	30	
t_s	Bus to Latch Enable ($\overline{RLE}$)		13			15			ns
t_h			4.0			6.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	23		14	26	ns
t_{HZ}, t_{LZ}		C_L = 5 pF, R_L = 2.0 kΩ		14	23		14	26	

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

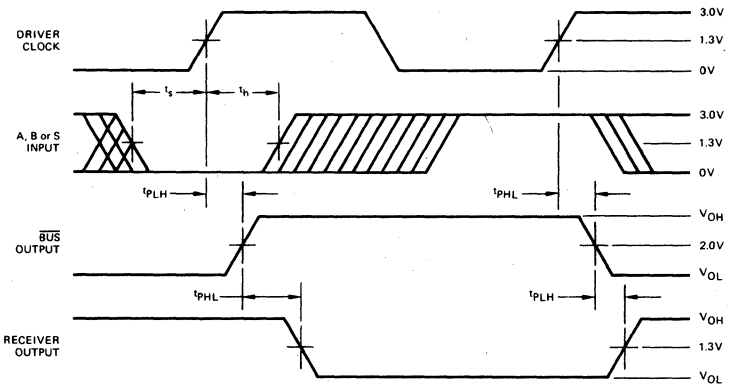
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

TC000880

SWITCHING WAVEFORMS



WF002280

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

Am2916A

Quad Three-State Bus Transceiver with Interface Logic

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Two-port input to D-type register on driver
- Three-state bus driver output can sink 48mA at 0.5V max.
- Internal 4-bit odd parity checker/generator
- Receiver output latch can sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

GENERAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

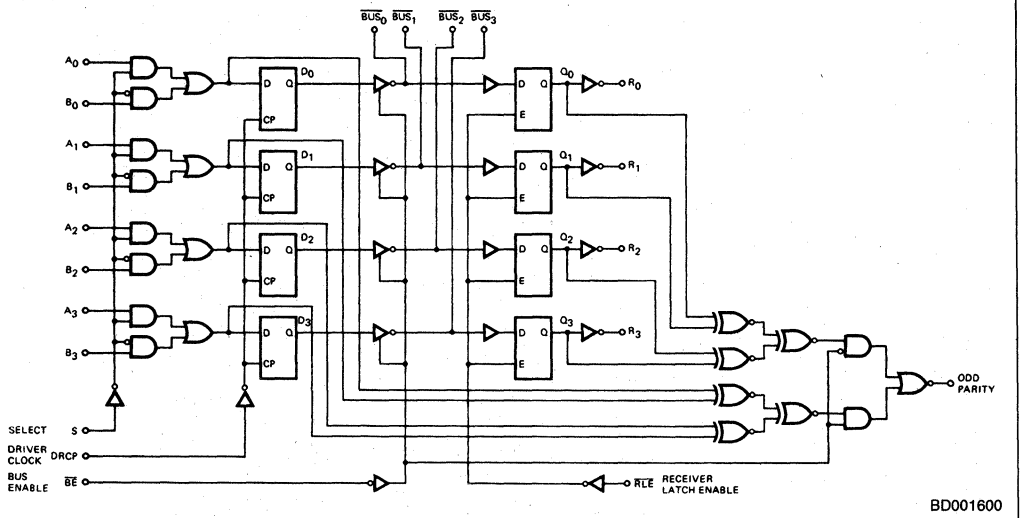
The input register consists of four D-type flip-flops with a buffered common clock and two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored.

The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

BLOCK DIAGRAM



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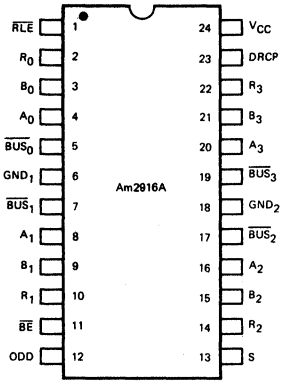
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

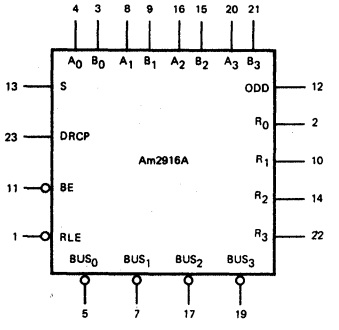
D-24-1



CD003020

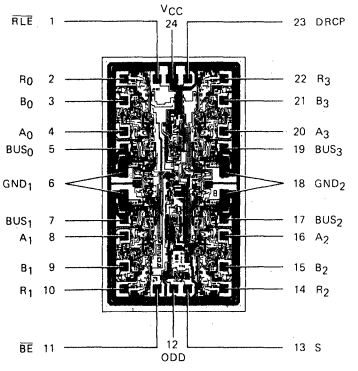
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000790

METALLIZATION AND PAD LAYOUT



DIE SIZE .074" x .130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2916A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - F– 24-pin flatpak
  - P– 24-pin plastic DIP
  - X– Dice
- **Am2916A** — Device type
  - Quad 3-state Bus Transceiver

Valid Combinations	
Am2916A	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

05402A

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 8, 16, 20	A_0, A_1, A_2, A_3	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9, 15, 21	B_0, B_1, B_2, B_3	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
11	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high-impedance state.
5, 7, 17, 19	$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 10, 14, 22	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUs inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUTS		
S	A_I	B_I	DRCP	$\overline{BE}$	$\overline{RLE}$	D_I	Q_I	$\overline{BUS}_I$	R_I	ODD	FUNCTION
X	X	X	X	H	X	X	X	Z	X	PQ	Driver output disable
X	X	X	X		X	X	X	X	X	PD	Driver output enable
X	X	X	X	H	L	X	L	L	H	H	Driver output disable and
X	X	X	X	H	L	X	H	H	L	H	receive data via Bus input
X	X	X	X	X	H	X	NC	X	NC	X	Latch received data
L	L	X	1	X	X	L	X	X	X	X	
L	H	X	1	X	X	H	X	X	X	X	Load driver register
H	X	L	1	X	X	L	X	X	X	X	
H	X	H	1	X	X	H	X	X	X	X	
X	X	X	L	X	X	NC	X	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	X	
X	X	X	X	L	X	L	X	H	X	H	Drive Bus
X	X	X	X	L	X	H	X	L	X	H	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition
PQ=Parity of Q latches
PD=Parity of D flip-flops

PARITY OUTPUT FUNCTION TABLE

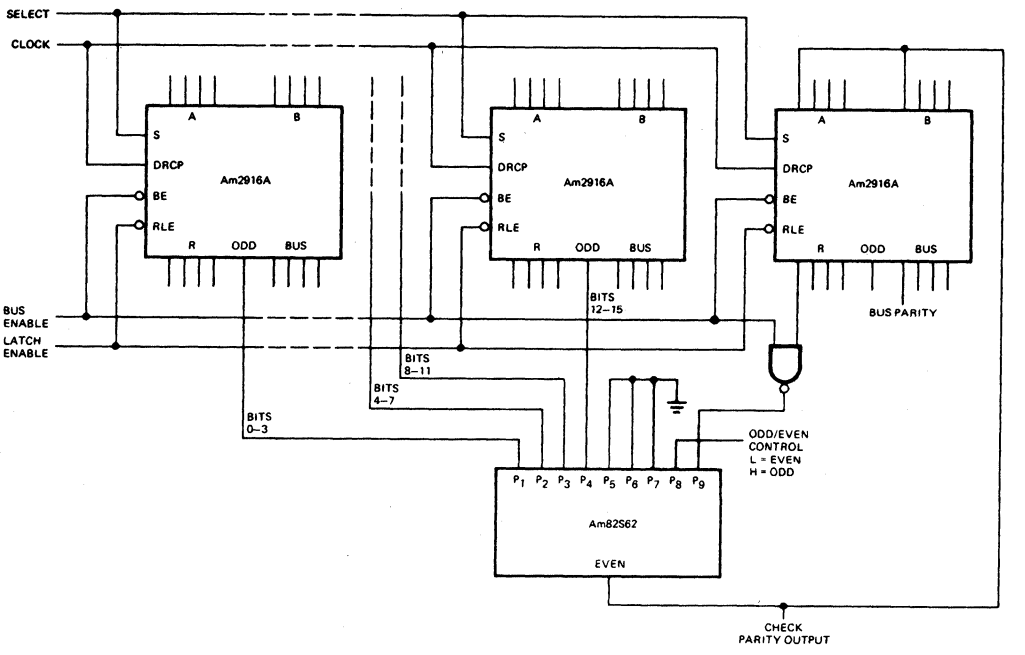
$\overline{BE}$	ODD PARITY OUTPUT
L	$ODD = I_0 \oplus I_1 \oplus I_2 \oplus I_3$
H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

I_i = Selected input A_i or B_i

05402A

Refer to Page 13-1 for Essential Information on Military Devices

APPLICATIONS



AF000990

Generating or checking parity for 16 data bits.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Output Current, Into Bus 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

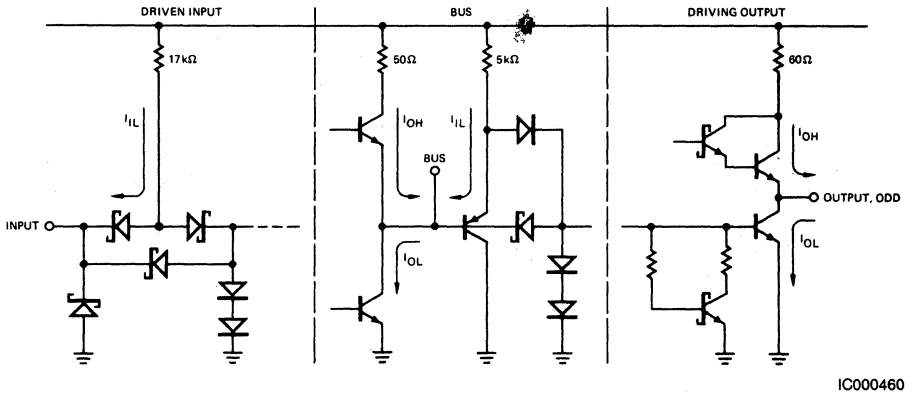
Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100μA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX, All inputs = GND			75	110	mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 1)		Min	Typ	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX V_O = 0V		−50	−120	−225	mA

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

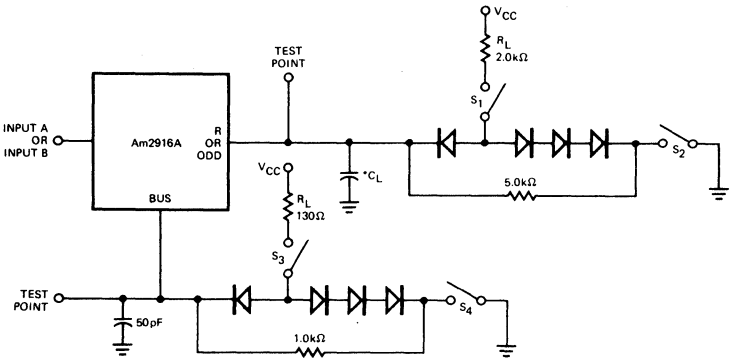
Parameters	Description	Test Conditions	COMMERCIAL Am2916A Min	COMMERCIAL Am2916A Typ (Note 1)	COMMERCIAL Am2916A Max	MILITARY Am2916A Min	MILITARY Am2916A Typ (Note 1)	MILITARY Am2916A Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130 Ω		21	32		21	36	ns
t_{PLH}				21	32		21	36	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{HZ}, t_{LZ}				13	18		13	21	
t_s	Data Inputs (A or B)	C_L = 15 pF, R_L = 2.0 kΩ	12			15			ns
t_h			6.0			8.0			
t_s	Select Inputs (S)		25			28			ns
t_h			6.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		17			20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	33	ns
t_{PHL}				18	27		18	30	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	33	ns
t_{PHL}				21	27		21	30	
t_s	Bus to Latch Enable ($\overline{RLE}$)		13			15			ns
t_h			4.0			6.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	42		32	46	ns
t_{PHL}				26	36		26	40	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	32		21	36	ns
t_{PHL}				21	32		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	32		21	36	ns
t_{PHL}				21	32		21	36	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

05402A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

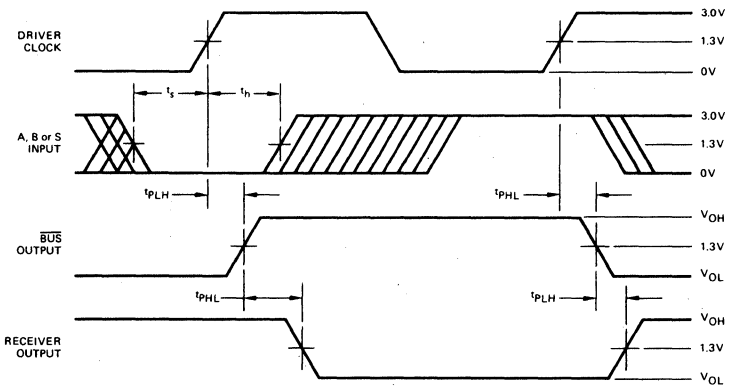


TC000890

*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

5

SWITCHING WAVEFORMS



WF002281

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

Am2917A

Quad Three-State Bus Transceiver with Interface Logic

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- D-type driver register with tri-state bus driver output can sink 48mA at 0.5V max.
- Internal 4-bit odd parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

GENERAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

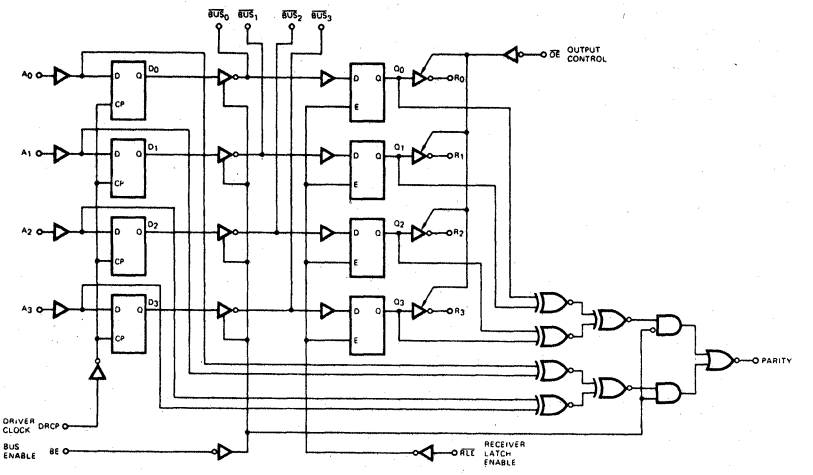
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

BLOCK DIAGRAM



BD001890

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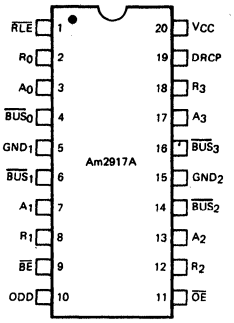
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-20-1

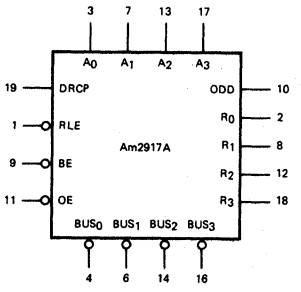


CD004160

Note: Pin 1 is marked for orientation

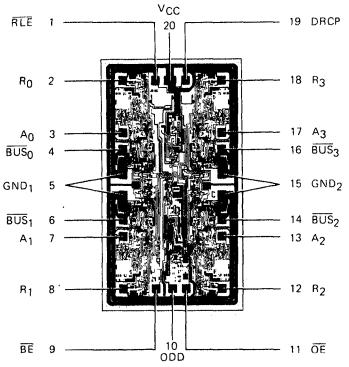
5

LOGIC SYMBOL



LS000880

METALLIZATION AND PAD LAYOUT



DIE SIZE .074" x .130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2917A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice
- **Am2917A** — Device type
  - Quad 3-state Bus Transceiver

Valid Combinations	
Am2917A	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7 13, 17	A_0, A_1, A_2, A_3	I	The four driver register inputs.
19	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
9	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
4, 6, 14, 16	BUS_0, BUS_1, BUS_2, BUS_3	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 8, 12, 18	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.
1	$\overline{RLE}$	I	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
10	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.
11	$\overline{OE}$	I	Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	FUNCTION
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X X	X X	H H	L L	L L	X X	L H	L H	H L	Driver output disable and receive data via Bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L H	↑ ↑	X X	X X	X X	L H	X X	X X	X X	Load driver register
X X	L H	X X	X X	X X	NC NC	X X	X X	X X	No driver clock restrictions
X X	X X	L L	X X	X X	L H	X X	H L	X X	Drive Bus

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

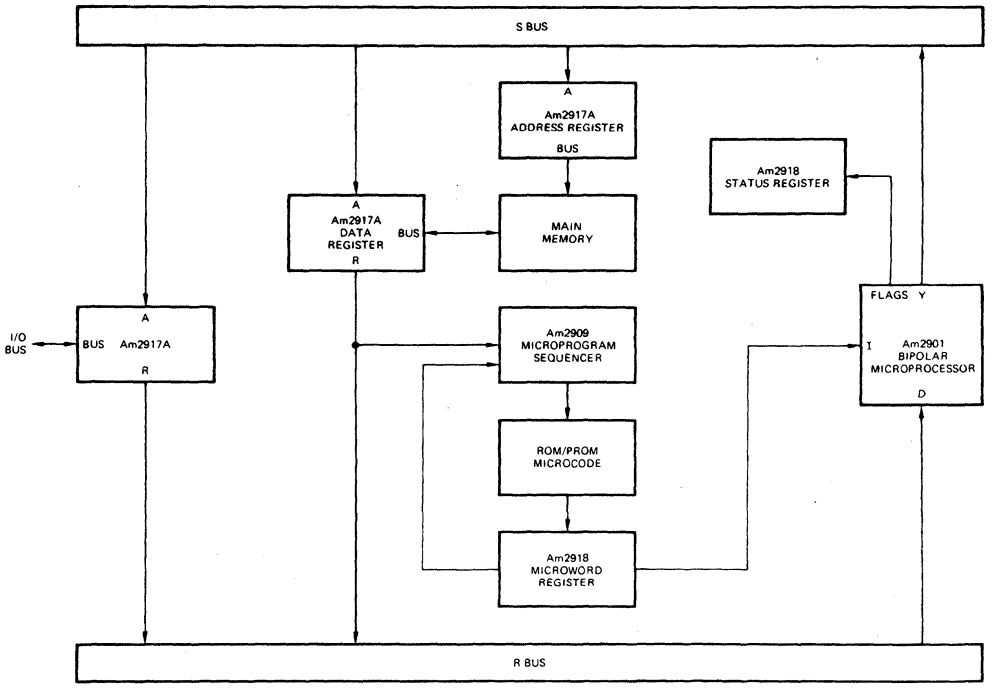
PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

05403A

Refer to Page 13-1 for Essential Information on Military Devices

APPLICATIONS



AF001380

The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max.
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Bus 100mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100μA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	

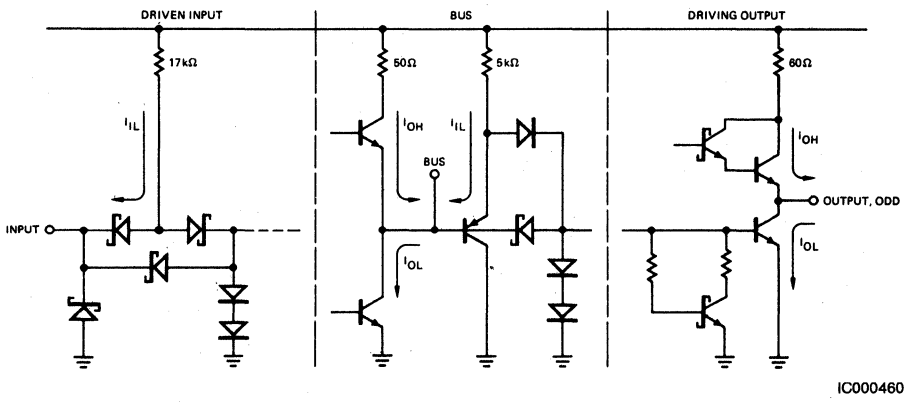
05403A

Refer to Page 13-1 for Essential Information on Military Devices

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)		Min	Typ	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX V_O = 0V		−50	−120	−225	mA

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

05403A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

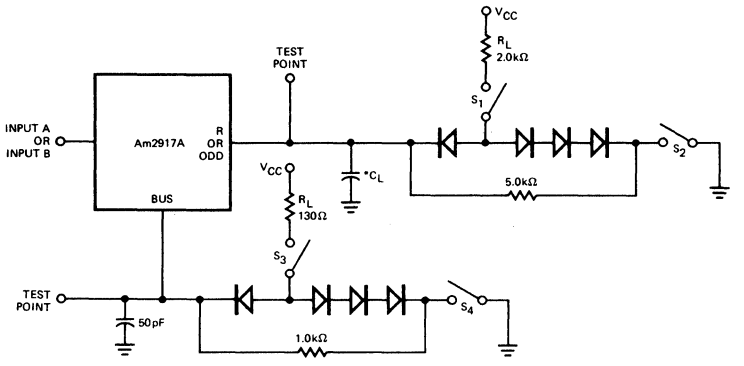
Parameters	Description	Test Conditions	COMMERCIAL Am2917A Min.	COMMERCIAL Am2917A Typ (Note 1)	COMMERCIAL Am2917A Max.	MILITARY Am2917A Min.	MILITARY Am2917A Typ (Note 1)	MILITARY Am2917A Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130 Ω		21	32		21	36	ns
t_{PLH}				21	32		21	36	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{HZ}, t_{LZ}				13	18		13	21	
t_s	A Data Inputs	C_L = 15 pF, R_L = 2.0 kΩ	12			15			ns
t_h			6.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		17			20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	33	ns
t_{PHL}				18	27		18	30	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	33	ns
t_{PHL}				21	27		21	30	
t_s	Bus to Latch Enable ($\overline{RLE}$)		13			15			ns
t_h			4.0			6.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	42		32	46	ns
t_{PHL}				26	36		26	40	
t_{PLH}	Bus to Odd Party Out (Driver Inhibit)			21	32		21	36	ns
t_{PHL}				21	32		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	32		21	36	ns
t_{PHL}				21	32		21	36	
t_{ZH}, t_{ZL}	Output Control to Output			14	23		14	26	ns
t_{HZ}, t_{LZ}		C_L = 5 pF, R_L = 2.0 kΩ		14	23		14	26	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

05403A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

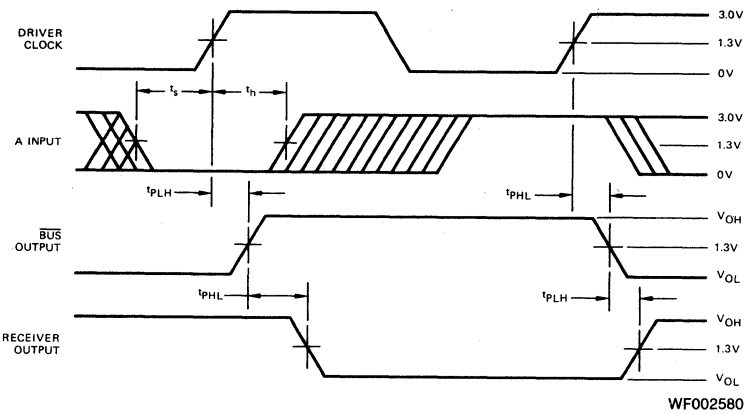


TC001170

*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

5

SWITCHING WAVEFORMS



WF002580

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

Am2918

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency

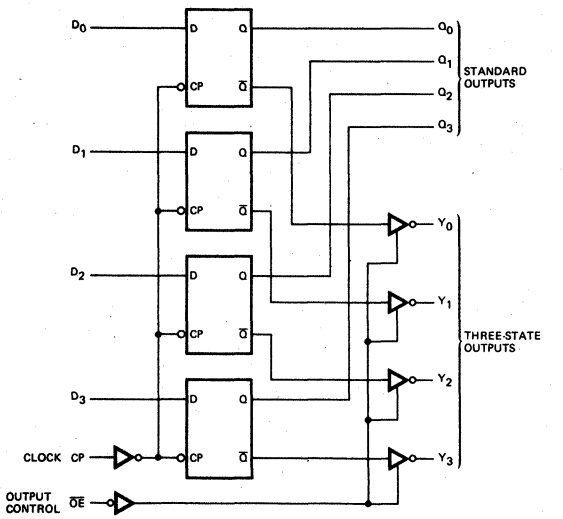
GENERAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration – especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem-pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

BLOCK DIAGRAM



BD002150

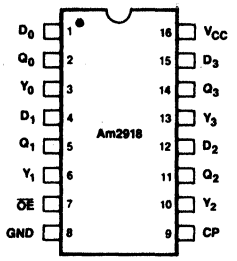
RELATED PRODUCTS

Part No.	Description
Am29LS18	Low Power Version
Am2919	Quad Register

03624B

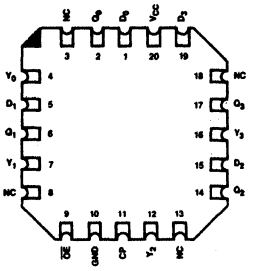
CONNECTION DIAGRAM
Top View

D-16-1



CD004250

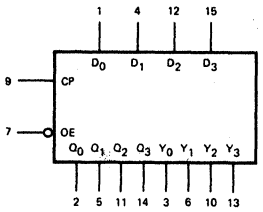
L-20-1



CD004240

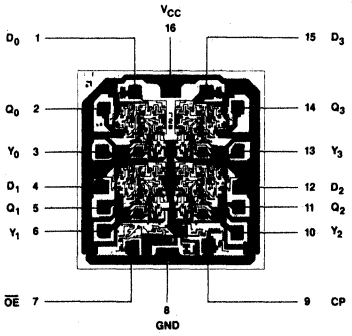
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000900

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.070" x 0.072"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2918 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 16-pin plastic DIP
  - X– Dice

Device type
Quad D Register

Valid Combinations	
Am2918	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP		CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$		$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

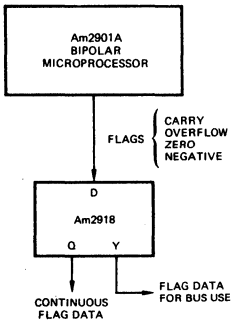
TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

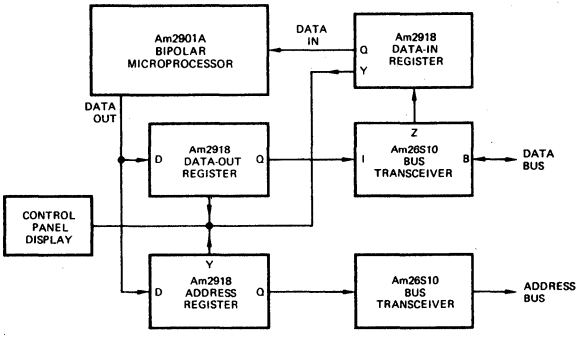
L = LOW
H = HIGH
X = Don't care
NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

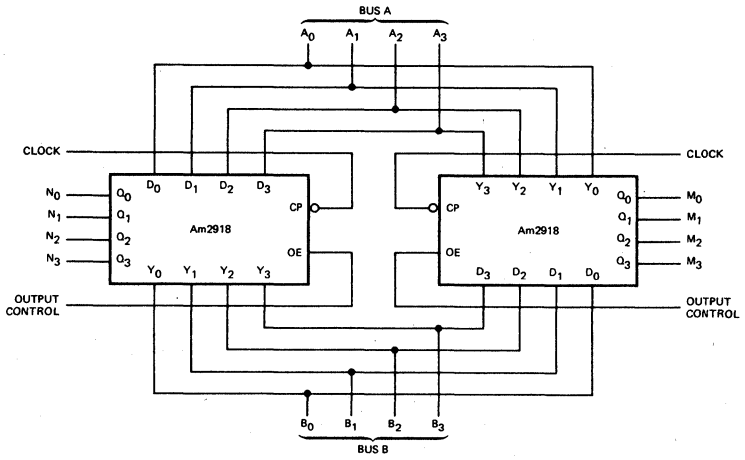
APPLICATIONS



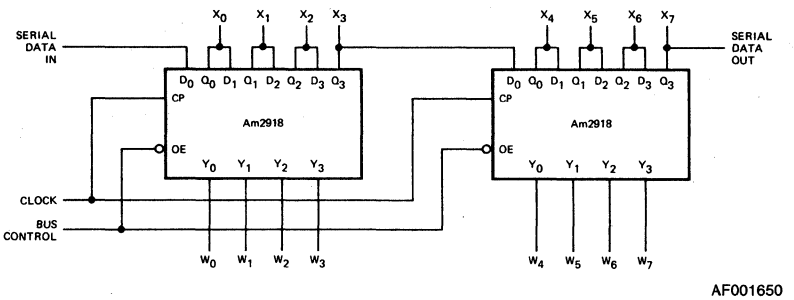
The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.



The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.



8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

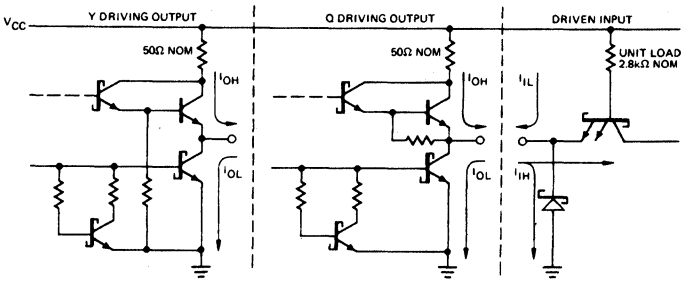
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q I_{OH} = −1mA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX	V_O = 2.4V				50	μA
			V_O = 0.4V				−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 5)				80	130	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000410

Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$, $R_L = 280\Omega$)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q Output		$C_L = 15$ pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		$C_L = 15$ pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			$C_L = 5.0$ pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		$C_L = 15$ pF	75	100		MHz

Am29LS18

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops

GENERAL DESCRIPTION

The Am29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

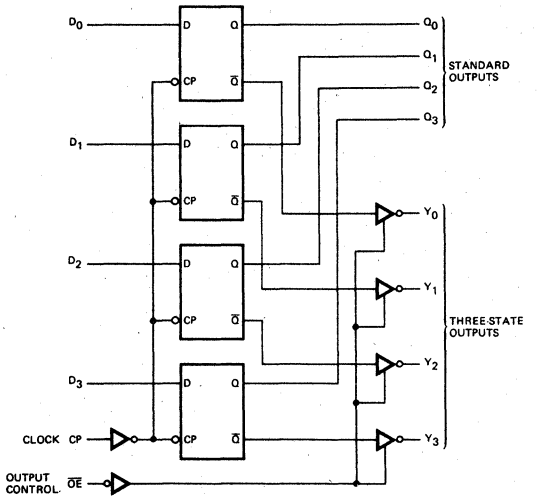
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

BLOCK DIAGRAM



BD002160

RELATED PRODUCTS

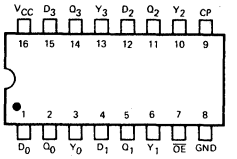
Part No.	Description
Am25S18	Quad D Register
Am25LS2518	Quad D Register
Am25LS2519	Quad Register

03623A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

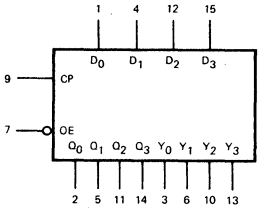
D-16-1



CD004270

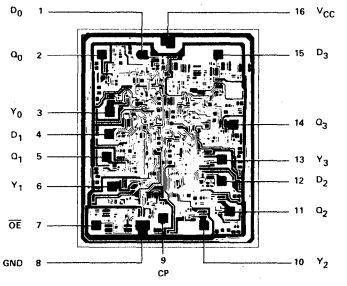
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000900

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083″ x 0.099″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29LS18 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am29LS18** — Device type: Quad D Register

Valid Combinations	
Am29LS18	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP		CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$		$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

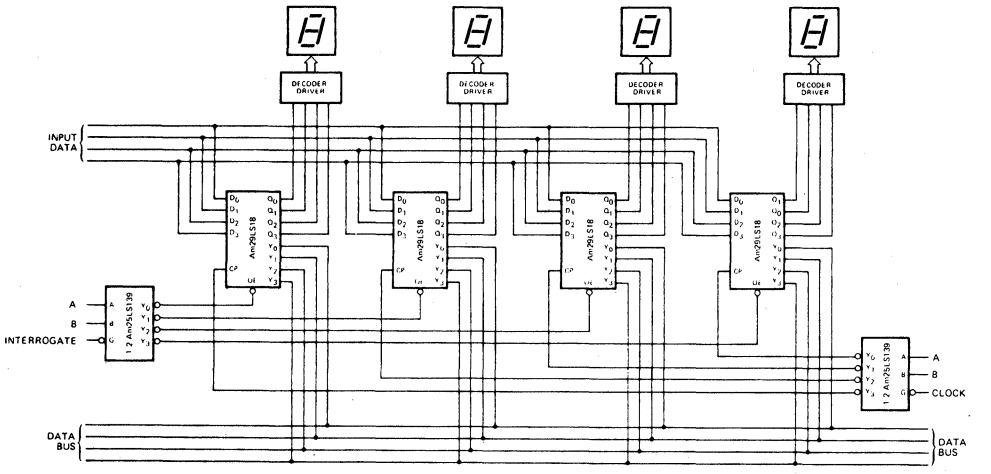
L = LOW
H = HIGH
X = Don't care
NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

03623A

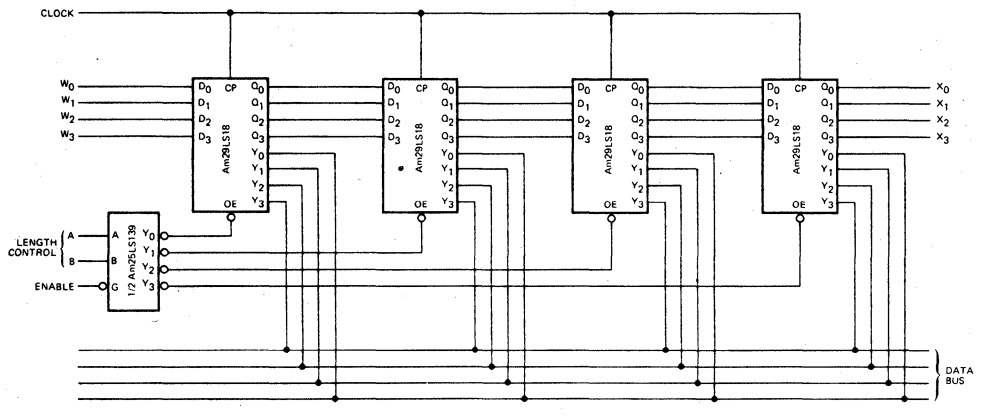
Refer to Page 13-1 for Essential Information on Military Devices

APPLICATIONS



AF001410

The Am29LS18 used as a display register with bus interrogate capability.



AF001400

The Am29LS18 as a variable length (1, 2, 3 or 4 word) shift register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

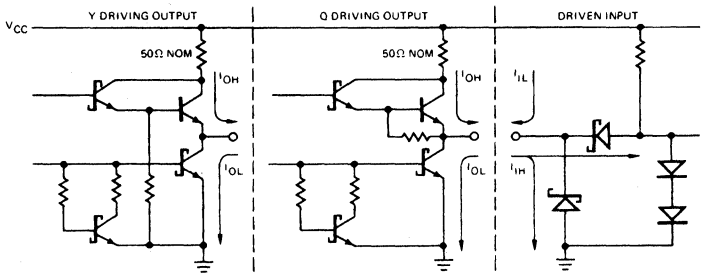
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q, I_{OH} = −660μA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, I_{OH} = −1.0mA	2.4	3.4		
				COM'L, I_{OH} = 2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX				17	28	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000420

Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q_i		C_L = 15 pF, R_L = 2.0 kΩ		18	27	ns
t_{PHL}					18	27	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				18	27	ns
t_{PHL}					18	27	
t_{pw}	Clock Pulse Width	LOW		18			ns
		HIGH		15			
t_s	Data			15			ns
t_h	Data			5.0			ns
t_{ZH}	$\overline{OE}$ to Y_i				7.0	11	ns
t_{ZL}					8	12	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0 pF, R_L = 2.0 kΩ		14	21	ns
t_{LZ}					12	18	
f_{max}	Maximum Clock Frequency (Note 1)			35	50		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am29LS18 Min	COMMERCIAL Am29LS18 Max	MILITARY Am29LS18 Min	MILITARY Am29LS18 Max	Units
t_{PLH}	Clock to Q_i		C_L = 50 pF, R_L = 2.0 kΩ		38		45	ns
t_{PHL}					38		45	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				35		40	ns
t_{PHL}					35		40	
t_{pw}	Clock Pulse Width	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			5.0		5.0		ns
t_{ZH}	$\overline{OE}$ to Y_i				15		17	ns
t_{ZL}					16		17	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 50 pF, R_L = 2.0 kΩ		27		30	ns
t_{LZ}					24		30	
f_{max}	Maximum Clock Frequency (Note 1)			30		25		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am2910A

Microprogram Controller

DISTINCTIVE CHARACTERISTICS

- **Twelve Bits Wide**
  Addresses up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- **Internal Loop Counter**
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- **Four Address Sources**
  Microprogram Address may be selected from microprogram counter, branch address bus, 9-level push/pop stack, or internal holding register.
- **Sixteen Powerful Microinstructions**
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- **Output Enable Controls for Three Branch Address Sources**
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- **Fast**
  The Am2910A supports 100ns cycle times and is 25 – 30% faster than the Am2910.

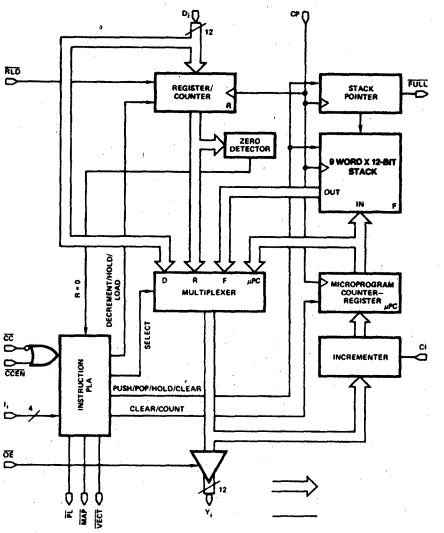
GENERAL DESCRIPTION

The Am2910A Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are nine levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a nine-deep last-in, first-out stack (F).

The Am2910A is a speed improved plug-in replacement of the Am2910 featuring AMD's ion-implanted micro-oxide (IMOX) processing and offering 25 – 30% speed improvement. The Am2910A also features a nine-word deep stack versus the five-deep stack of the Am2910.

BLOCK DIAGRAM



BDR02320

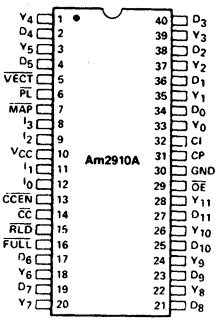
IMOX is a trademark of Advanced Micro Devices, Inc.

04522B

Refer to Page 13-1 for Essential Information on Military Devices

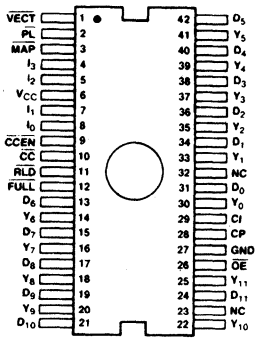
CONNECTION DIAGRAM
Top View

D-40,P-40



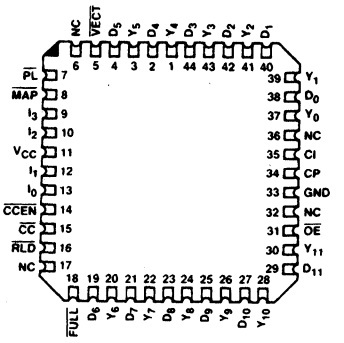
CD004670

F-42-1



CD004680

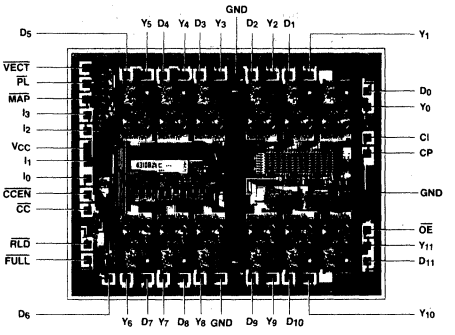
Chip-Pak™ L-44-1



CD004690

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



Die Size 0.170" x 0.194"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2910A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 40-pin CERDIP (D-40-1)
  - F– 42-pin flatpak (F-42-1)
  - L– 44-pin leadless chip carrier (L-44-1)
  - P– 40-pin plastic DIP (P-40-1)
  - X– Dice
- **Am2910A** — Device type
  - Microprogram Controller

Valid Combinations	
Am2910A	PC DC,DCB,DMB FMB LC,LMB XC,XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

04522B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.*	Name	I/O	Description
	D_i	I	Direct input to register/counter and multiplexer. D_0 is LSB.
	I_j	I	Selects one-of-sixteen instructions for the Am2910A.
14	$\overline{CC}$	I	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
13	$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
32	CI	I	Low order carry input to incrementer for microprogram counter.
15	$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
29	$\overline{OE}$	I	Three-state control of Y_i outputs.
31	CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
	Y_i	O	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB.
16	$\overline{FULL}$	O	Indicates that nine items are on the stack.
6	$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
7	$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
5	$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

*DIP only.

PRODUCT OVERVIEW

The Am2910A is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The Am2910A contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 9-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 1,4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

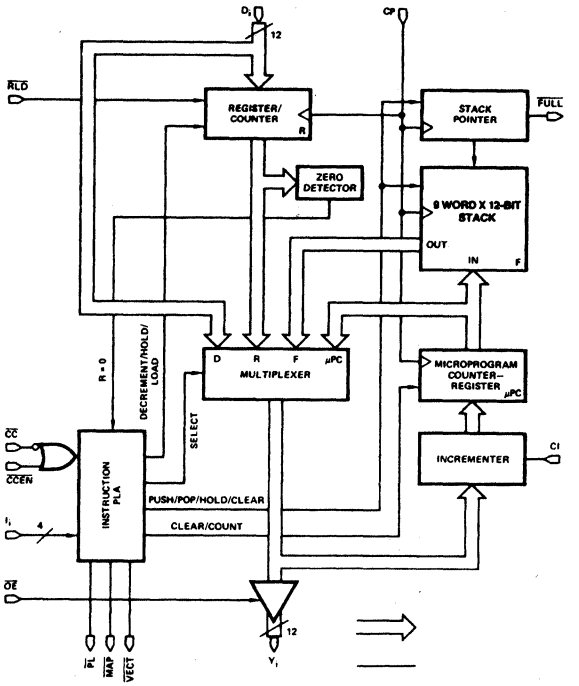
During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to nine. After a depth of nine is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place nonmeaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8,9,15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N + 1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

BLOCK DIAGRAM



BDR02320

OPERATION

The Table of Instructions shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs (see Functional Pin Description), can modify instruction execution. The combination $\overline{CC}$ HIGH and $\overline{CCEN}$ LOW is used as a test in 9 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove the Am2910A Y outputs from a three-state bus.

The stack, a nine-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack are undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (nine more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a ninth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

TABLE OF INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CONTENTS	FAIL $\overline{CCEN}$ = L and $\overline{CC}$ = H		PASS $\overline{CCEN}$ = H or $\overline{CC}$ = L		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load. H=HIGH L=LOW X = Don't Care

THE Am2910A INSTRUCTION SET

The Am2910A provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. In this discussion it is assumed the C_i is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying to the source of Am2910A instruction bit I_0, which leaves instructions 4, 6 and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the Am2910A is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, examples of all 16 instructions are included.

The examples given should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, simply means that the contents of microprogram memory word 50 are executed, then the contents of word 51 are executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

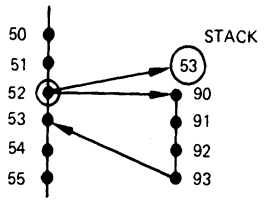
It might be appropriate at this time to mention that AMD has a microprogram assembler called AMDASM, which has the capability of using the Am2910A instructions in symbolic representation. AMDASM's Am2910A instruction symbolics (or mnemonics) are given in the examples, and again in the Table of Instructions.

0 JUMP ZERO (JZ)

PFR00830

Instruction 0, JZ (JUMP to ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

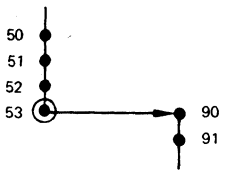
1 COND JSB PL (CJS)



PFR00950

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

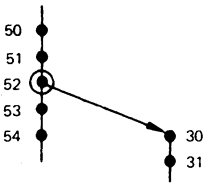
2 JUMP MAP (JMAP)



PFR00960

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52 and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

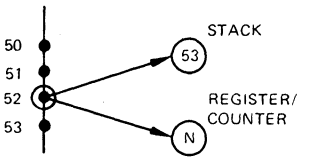
3 COND JUMP PL (CJP)



PFR00820

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value ($BR_0 - BR_{11}$). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. The example shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

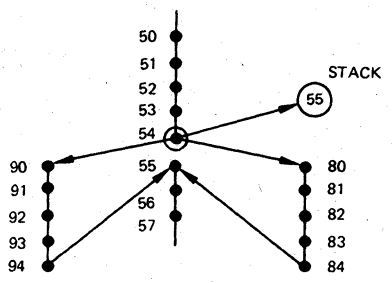
4 PUSH/COND LD CNTR (PUSH)



PFR00840

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In this example, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will describe how to use the pushed value and the register/counter for looping.

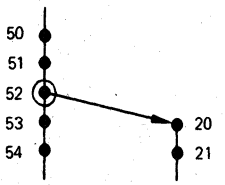
5 COND JSB R/PL (JSRP)



PFR00940

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter of the contents of the PIPELINE register. A PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A RETURN-FROM-SUBROUTINE (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the Am2910A register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

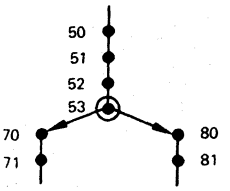
6 COND JUMP VECTOR (CJV)



PFR00920

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the Am2910A output $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

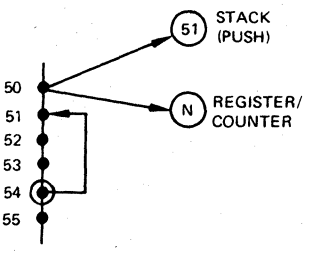
7 COND JUMP R/PL (JRP)



PFR00930

Instruction 7 is a CONDITIONAL JUMP via the contents of the Am2910A REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the CONDITIONAL JUMP-TO-SUBROUTINE via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. The example depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the Am2910A. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

8 REPEAT LOOP, CNTR ≠ 0 (RFCT)



PFR00910

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register/counter contains zero, the loop exit condition is occurring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

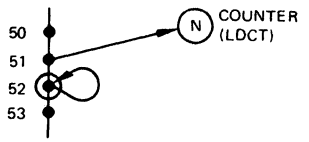
In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper

value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

9 REPEAT PL, CNTR ≠ 0 (RPCT)

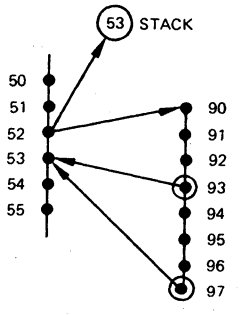


PFR00890

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested nine deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In this example, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

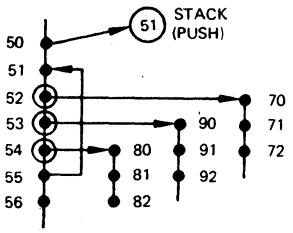
10 COND RETURN (CRTN)



PFR00900

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. This example depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a JUMP-TO-SUBROUTINE at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force $\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

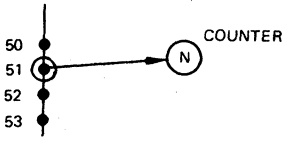
11 COND JUMP PL & POP (CJPP)



PFR00850

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

12 LD CNTR & CONTINUE (LDCT)

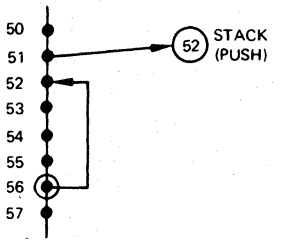


PFR00870

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a

branch address or a counter value depending upon the microinstruction being executed. Altogether there are three ways of loading the counter – the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

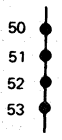
13 TEST END LOOP (LOOP)



PFR00860

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

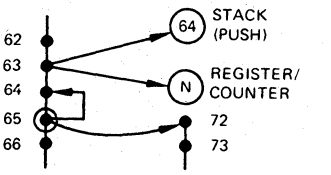
14 CONTINUE (CONT)



PFR00880

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

15 THREE-WAY BRANCH (TWB)



PFR00810

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

As one example, consider the case of a memory search instruction. As shown, the instruction at microprogram address 63 can be instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

ARCHITECTURES USING THE Am2910A

(Shading shows path(s) which usually limit speed)

One Level Pipeline Based (Recommended)

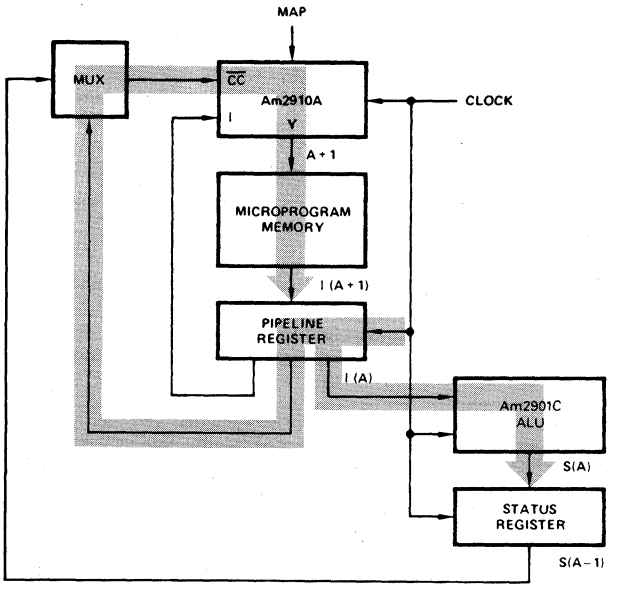
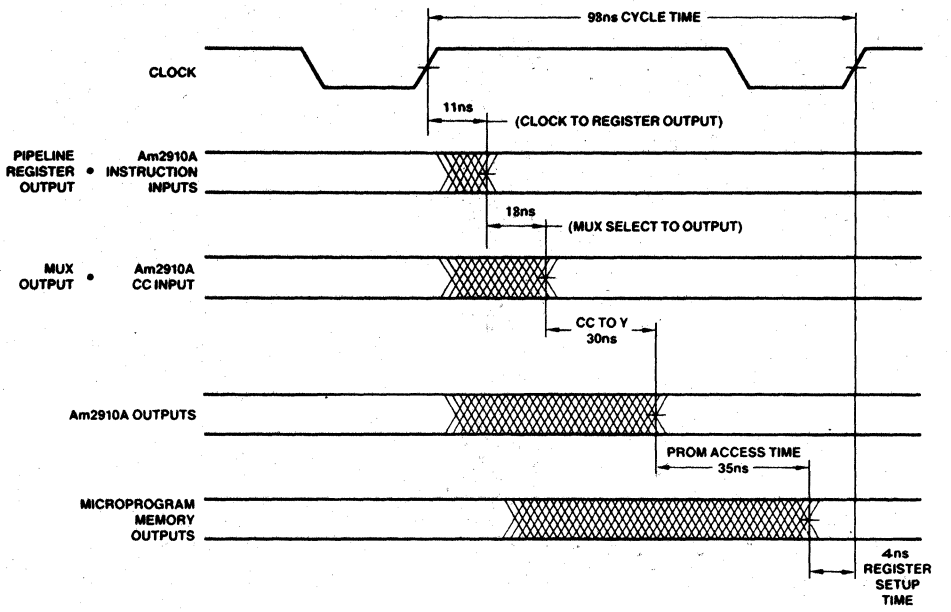


Figure 1.

One level pipeline provides better speed than most other architectures. The μProgram Memory and the Am2901 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs.

Typical CCU Cycle Timing Waveforms



WF003051

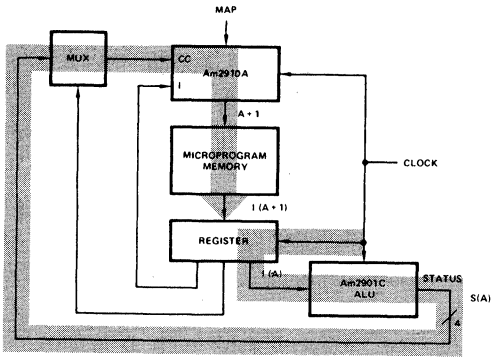
This drawing shows the timing relationships in the CCU illustrated above.

OTHER ARCHITECTURES USING THE Am2910A

(Shading shows path(s) which usually limit speed)

Figure 2.

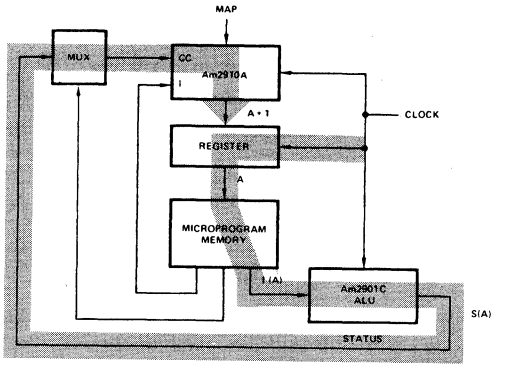
a. Instruction Based



PF001001

A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2901C delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

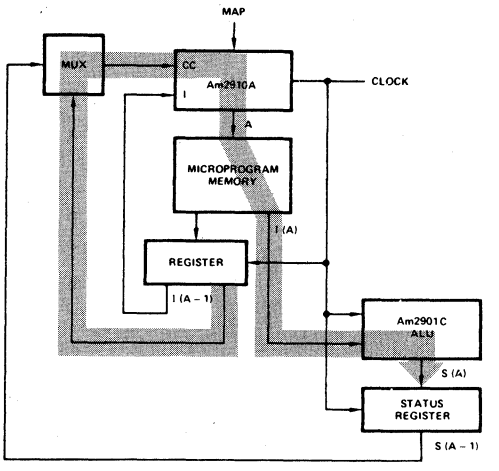
b. Addressed Based



PF001011

The Register at the Am2910A output contains the address of the microinstruction being executed. The Microprogram Memory and Am2901C are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10 – 12 bits) is stored instead of the instruction (typically 40 – 60 bits).

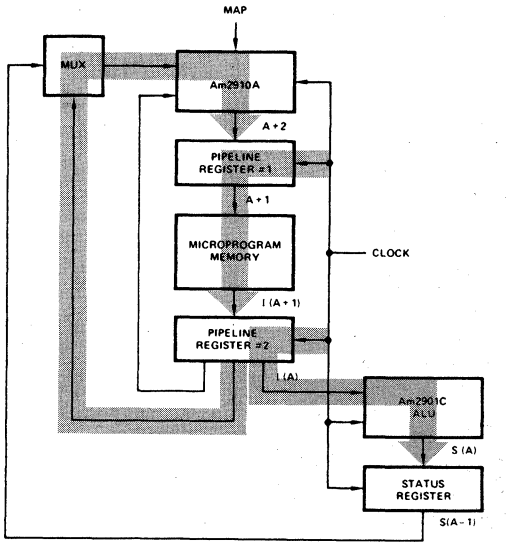
c. Data Based



PF001021

The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and Am2901C are in series in the critical paths.

d. Two Level Pipeline Based



PF001051

Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

Am2910A HIGH SPEED APPLICATION

Optimal Am2910A configurations can support high speed bit slice designs. When used with high speed registers and PROMs, the Am2910A can execute simple instructions in 100ns.

The following figure illustrates the usual critical path in the sequencer.

Timing on the critical paths becomes

Device	Path	Delay
Status Register	Clock →Output	11ns
Fast MUX	Select →Output	18ns
Am2910A	$\overline{CC}$→Y	30ns
Fast PROM	Addr →Output	35ns
Pipeline Register	Setup	4ns
		99ns

The following gives one suggested parts configuration to meet this design criterion.

Status Register	Am29825
MUX (8 to 1)	74S151
PROM	Am27S35
Pipeline Register	Am2918

One Level Pipeline Based (Recommended)

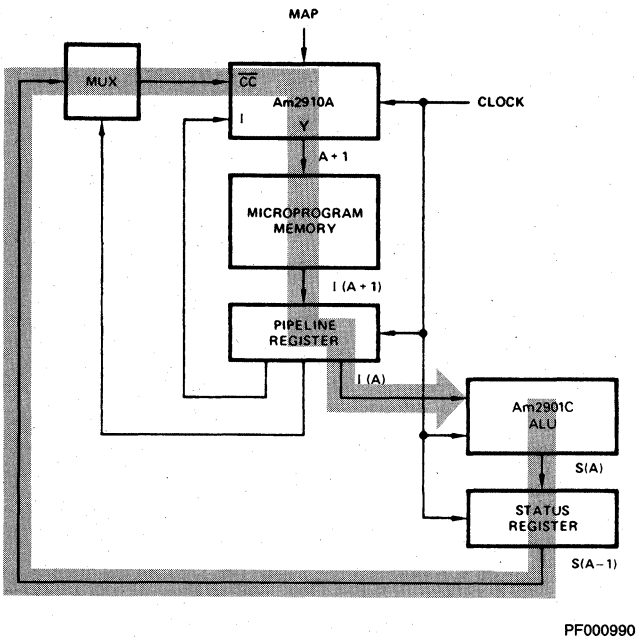


Figure 3.

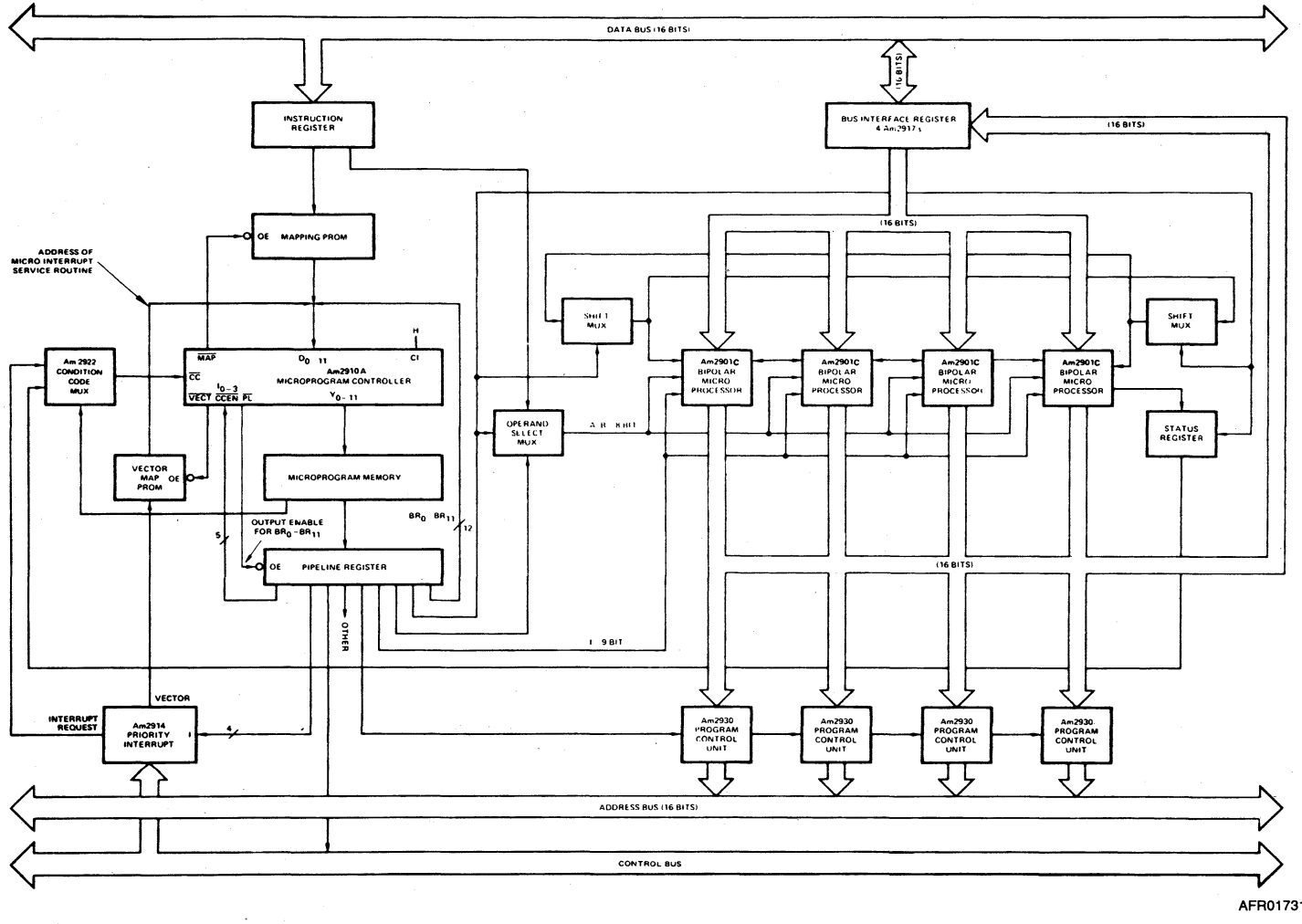


Figure 4. Typical Bipolar Microcomputer Using Am2910A

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Case Temperature with Power Applied .. −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus) 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage(V_{CC}) to ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage(V_{CC}) ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1.6mA, V_{IN} = V_{IH} or V_{IL}			2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA				0.5	
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA					
V_{IH}	Input HIGH Level (Note 4)	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs					0.8	
V_{CLMP}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-11}			−0.87	mA
				C1, $\overline{CCEN}$			−0.54	
				I_{0-3}, $\overline{OE}$,$\overline{RLD}$			−0.72	
				$\overline{CC}$			−1.31	
				CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-11}			80	μA
				C1, $\overline{CCEN}$			30	
				I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
				$\overline{CC}$			50	
				CP			100	
		V_{CC} = MAX, V_{IN} = 5.5V					1.0	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V		V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2910APC, DC	T_A = 0 to +70°C			344	mA
				T_A = +70°C			280	
			Am2910ADM, FM	T_C = −55 to +125°C			340	
				T_C = +125°C			280	

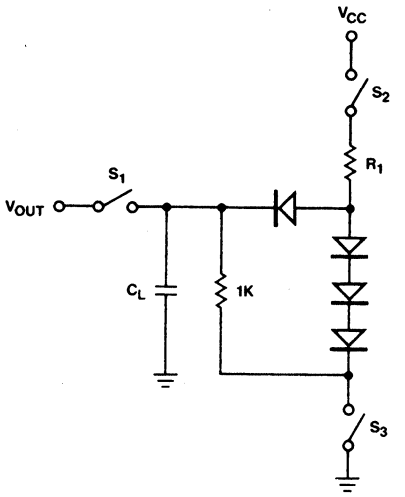
Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and a maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).

Notes on Testing

1. Insure the part is adequately decoupled at the test head. Large changes in supply current when the device switches may cause function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5 − 8ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide actual Sentry programs, under license from Sentry.

SWITCHING TEST CIRCUIT

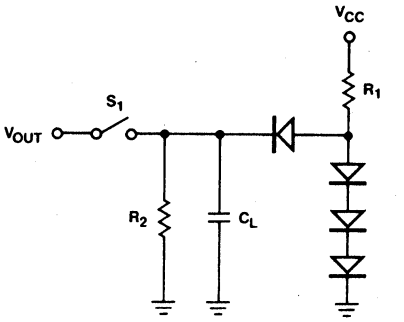
THREE-STATE OUTPUTS



TCR01350

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

NORMAL OUTPUTS



TCR01370

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacities without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2910A

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$Y_{0\text{-}11}$	A	300	1K
5	$\overline{VECT}$	B	470	1.5K
6	$\overline{PL}$	B	470	1.5K
7	$\overline{MAP}$	B	470	1.5K
16	$\overline{FULL}$	B	470	1.5K

Am2910A SWITCHING CHARACTERISTICS

The tables below define the Am2910A switching characteristics. Tables A are set up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE Am2910APC, DC

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	16	0
$D_i \rightarrow PC$	30	0
I_0-I_3	35	0
$\overline{CC}$	24	0
$\overline{CCEN}$	24	0
CI	18	0
$\overline{RLD}$	19	0

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	35	30	–
$\overline{CC}$	30	–	–
$\overline{CCEN}$	30	–	–
CP	40	–	31
$\overline{OE}$ (Note 1)	25/27	–	–

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	20	ns
Minimum Clock Period	50	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE Am2910ADM, FM

(T_C = −55 to +125°C, V+ = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	16	0
$D_i \rightarrow PC$	30	0
I_0-I_3	38	0
$\overline{CC}$	35	0
$\overline{CCEN}$	35	0
CI	18	0
$\overline{RLD}$	20	0

B. Combinational Delays

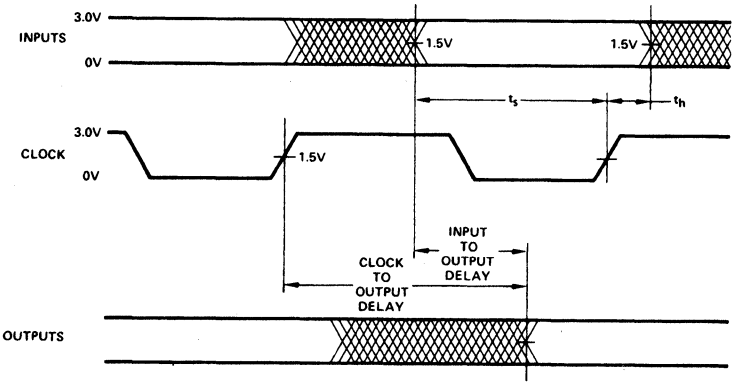
Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	40	35	–
$\overline{CC}$	36	–	–
$\overline{CCEN}$	36	–	–
CP	46	–	35
$\overline{OE}$ (Note 1)	25/30	–	–

C. Clock Requirements

Minimum Clock LOW Time	25	ns
Minimum Clock HIGH Time	25	ns
Minimum Clock Period	51	ns

Note 1. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

SWITCHING WAVEFORMS



WFR02990

RELATED PRODUCTS

Part No.	Description
Am2914	Vectored Interrupt Controller
Am2918	Pipeline Register
Am2922	Condition Code MUX
Am25LS377	Status Register
Am27S35	Registered PROM
Am29818	SSR Diagnostics/Pipeline Register

For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

Am2919

Quad Register with Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

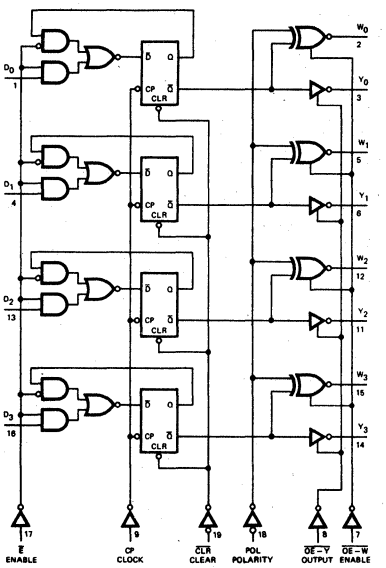
- Four D-type flip-flops
- Two sets of three-state outputs
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

GENERAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



BD002400

RELATED PRODUCTS

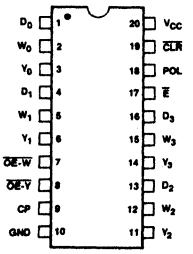
Part No.	Description
Am25LS2519	Quad Register
Am25LS2518	Quad D Register

03597B

Refer to Page 13-1 for Essential Information on Military Devices

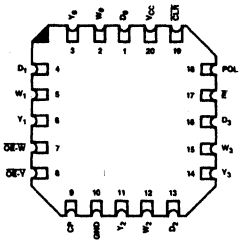
CONNECTION DIAGRAM
Top View

P-20
D-20
F-20*



CD004590

L-20-1



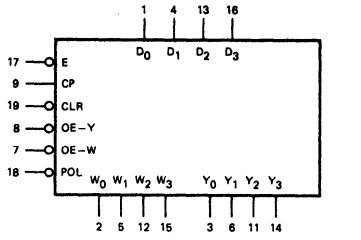
CD004600

*F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation

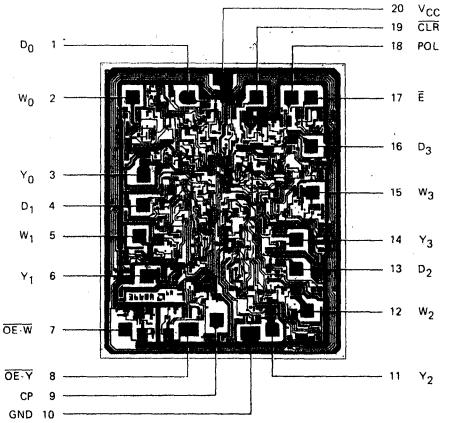
5

LOGIC SYMBOL



LS001000

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2919 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am2919** — Device type: Quad Register

Valid Combinations	
Am2912	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

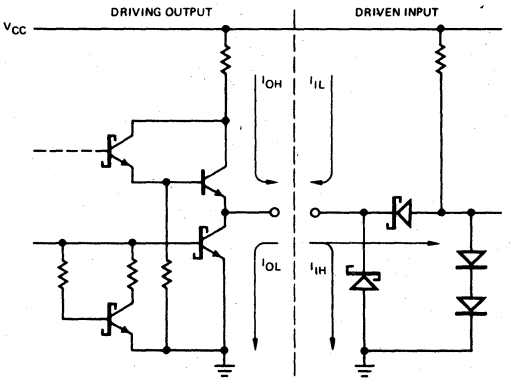
Pin No.	Name	I/O	Description
1, 4, 13, 16	D_i	I	Any of the four D flip-flop data lines.
17	$\overline{E}$	I	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
9	CP	I	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
7, 8	$\overline{OE}$-W, $\overline{OE}$-Y	I	Output Enable. When $\overline{OE}$ is LOW, the register is enabled to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set.
3, 6, 11, 14	Y_i	O	Any of the four non-inverting three-state output lines.
2, 5, 12, 15	W_i	O	Any of the four three-state outputs with polarity control.
18	POL	I	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
19	$\overline{CLR}$	I	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/ Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE}$-$\overline{W}$	1.0	–	–	–	–
8	$\overline{OE}$-$\overline{Y}$	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

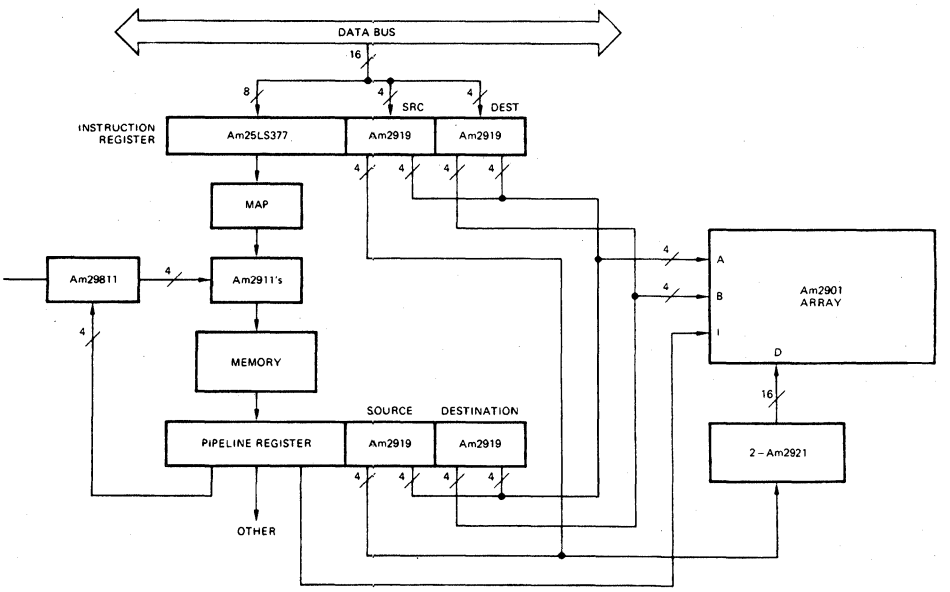
Note: Actual current flow direction shown.

FUNCTION TABLE

Function	Inputs							Internal	Outputs	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW
H = HIGH
Z = High Impedance
NC = No Change
X = Don't Care
↑ = LOW-to-HIGH Transition

APPLICATION



AF001850

The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_H or V_{IL}	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX		MIL		24	36	mA
				COM'L		24	39	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded: outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Clock to Y_i		C_L = 15pF R_L = 2.0kΩ		22	33	ns
t_{PHL}					20	30	
t_{PLH}	Clock to W_i (Either Polarity)				24	36	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y_i				29	43	ns
t_{PLH}	Clear to W_i				25	37	ns
t_{PHL}					30	45	
t_{PLH}	Polarity to W_i				23	34	ns
t_{PHL}					25	37	
t_{pw}	Clear			18			ns
t_{pw}	Clock Pulse Width	LOW		15			ns
		HIGH		18			
t_s	Data			15			ns
t_h	Data			5			ns
t_s	Data Enable			20			ns
t_h	Data Enable			0			ns
t_s	Set-up Time, Clear Recovery (Inactive) to Clock			20	15		ns
t_{ZH}	Output Enable to W or Y				11	17	ns
t_{ZL}					13	20	
t_{HZ}	Output Enable to W or Y		C_L = 5.0pF R_L = 2.0kΩ		13	20	ns
t_{LZ}					11	17	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 15pF R_L = 2.0kΩ	35	45		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

				Commercial		Military		
				Am2919		Am2919		
Parameters	**Description**		**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PLH}	Clock to Y_i		C_L = 50pF R_L = 2.0kΩ		39		42	ns
t_{PHL}					39		45	
t_{PLH}	Clock to W_i (Either Polarity)				41		43	ns
t_{PHL}					44		48	
t_{PHL}	Clear to Y_i				52		58	ns
t_{PLH}	Clear to W_i				42		43	ns
t_{PHL}					51		53	
t_{PLH}	Polarity to W_i				41		45	ns
t_{PHL}					42		44	
t_{pw}	Clear			20		20		ns
t_{pw}	Clock	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			10		10		ns
t_s	Data Enable			25		25		ns
t_h	Data Enable			0		0		ns
t_s	Set-up Time, Clear Recovery (Inactive) to Clock			23		24		ns
t_{ZH}	Output Enable to W_i or Y_i				24		27	ns
t_{ZL}					29		35	
t_{HZ}	Output Enable to W_i or Y_i		C_L = 5.0pF R_L = 2.0kΩ		33		45	ns
t_{LZ}					22		26	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 50pF R_L = 2.0kΩ	30		25		MHz

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am2920

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

GENERAL DESCRIPTION

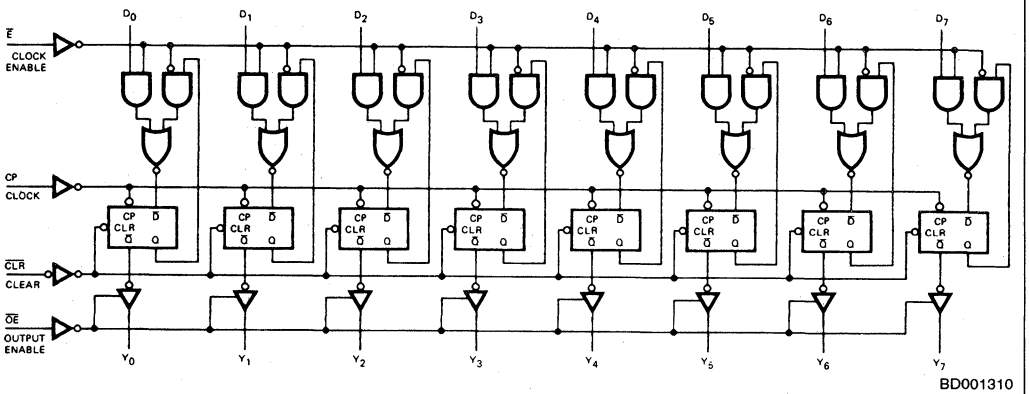
The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

BLOCK DIAGRAM



BD001310

RELATED PRODUCTS

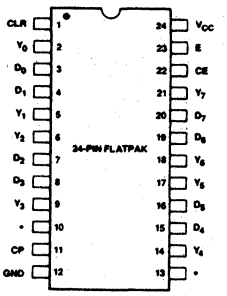
Part No.	Description
Am25LS2520	Octal D-type Flip-Flop
Am2918	Quad D-Registers
Am2954/55	Octal D-Registers
Am29821-26	8, 9, 10-Bit Registers

03598A

Refer to Page 13-1 for Essential Information on Military Devices

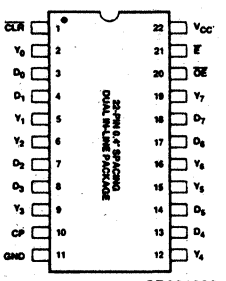
CONNECTION DIAGRAM
Top View

F-24



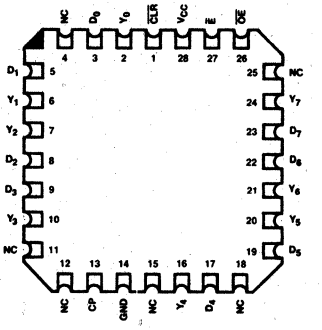
CD001910

P-22
D-22



CD001900

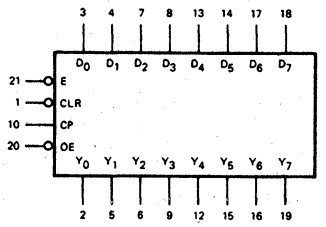
L-28-1



CD004900

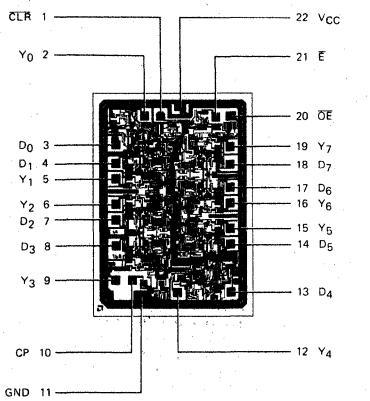
Note: Pin 1 is marked for orientation
*RESERVED — do not use.

LOGIC SYMBOL



LS000720

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.111"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2920 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 22-pin CERDIP
  - F– 24-pin flatpak
  - L– 28-pin leadless chip carrier
  - P– 22-pin plastic DIP
  - X– Dice
- **Am2920** — Device type
  - Octal D-Type Flip-Flop

Valid Combinations	
Am2920	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{CLR}$	I	When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.
10	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i	O	The register three-state outputs.
21	$\overline{E}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
20	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TT2 Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

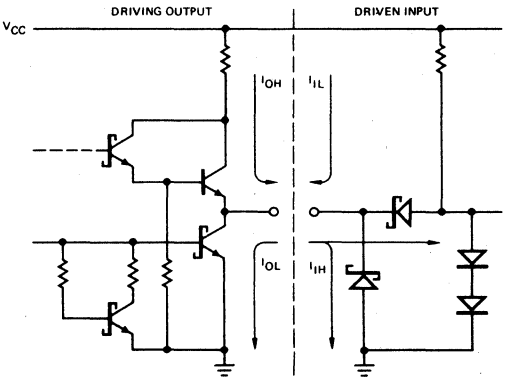
		Am2920				
			Output HIGH		Output LOW	
Pin No.'s	Input/ Output	Input Load	MIL	COM'L	MIL	COM'L
1	$\overline{CLR}$	1	–	–	–	–
2	Y_0	–	50	130	22	22
3	D_0	1	–	–	–	–
4	D_1	1	–	–	–	–
5	Y_1	–	50	130	22	22
6	Y_2	–	50	130	22	22
7	D_2	1	–	–	–	–
8	D_3	1	–	–	–	–
9	Y_3	–	50	130	22	22
10	CP	1	–	–	–	–
11	GND	–	–	–	–	–
12	Y_4	–	50	130	22	22
13	D_4	1	–	–	–	–
14	D_5	1	–	–	–	–
15	Y_5	–	50	130	22	22
16	Y_6	–	50	130	22	22
17	D_6	1	–	–	–	–
18	D_7	1	–	–	–	–
19	Y_7	–	50	130	22	22
20	$\overline{OE}$	1	–	–	–	–
21	$\overline{E}$	1	–	–	–	–
22	V_{CC}	–	–	–	–	–

FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH transition
Z = High-Impedance

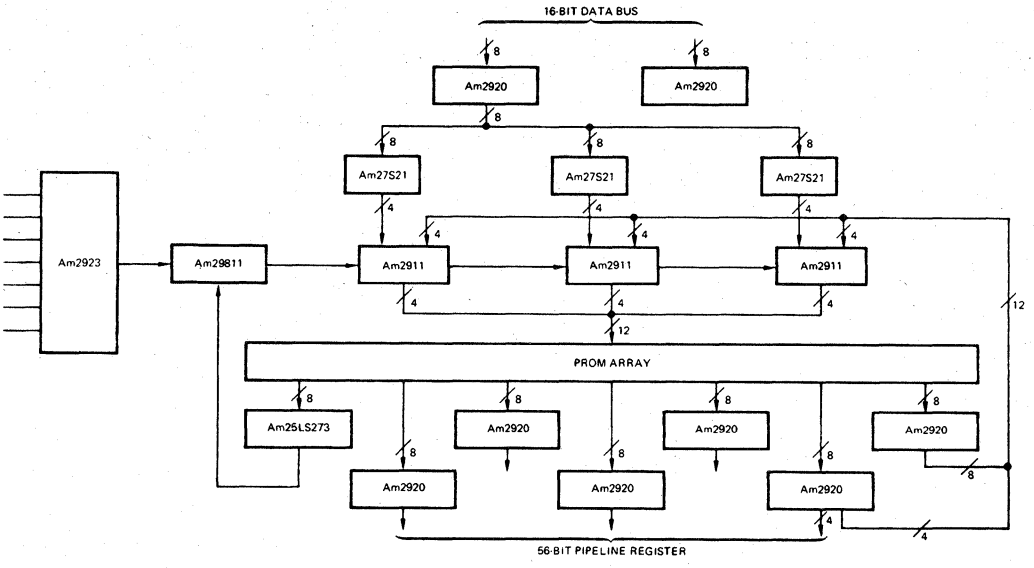
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

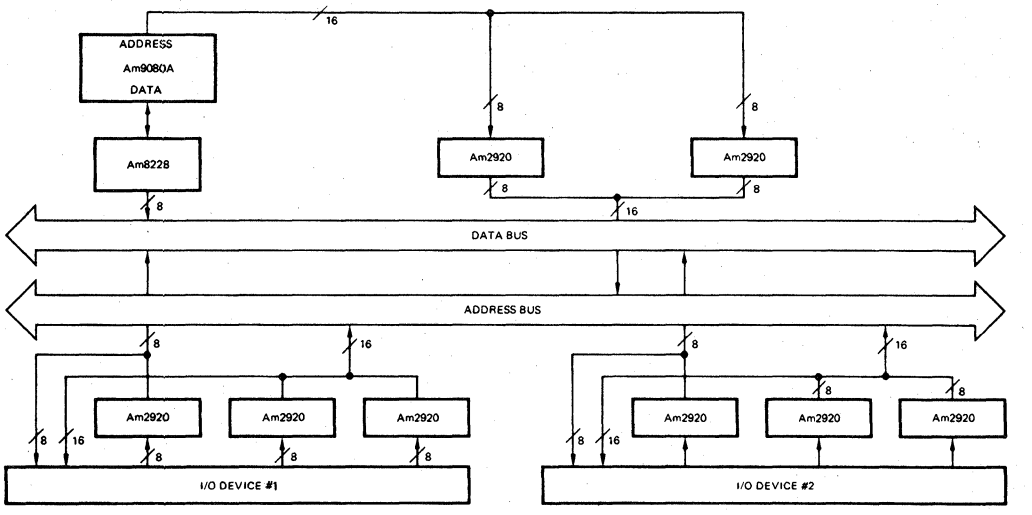
Note: Actual current flow direction shown.

APPLICATIONS



AF001940

A typical Computer Control Unit for a microprogrammed machine.



AF001930

The Am2920 is a useful device in interfacing with the Am9080A system buses.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current		V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			24	37	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, D_i inputs = CLR $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 15pF R_L = 2.0kΩ		18	27	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y				22	35	ns
t_s	Data (D_i)			10	3		ns
t_h	Data (D_i)			10	3		ns
t_s	Enable ($\overline{E}$)	Active		15	10		ns
		Inactive		20	12		
t_h	Enable ($\overline{E}$)			0	0		ns
t_s	Clear Recovery (In-Active) to Clock			11	7		ns
t_{pw}	Clock	HIGH		20	14		ns
		LOW		25	13		
t_{pw}	Clear			20	13		ns
t_{ZH}	$\overline{OE}$ to Y_i				9	13	ns
t_{ZL}					14	21	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		20	30	ns
t_{LZ}					24	36	
f_{max}	Maximum Clock Frequency (Note 1)				40		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no contraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am2920		MILITARY Am2920		Units
				Min	Max	Min	Max	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 50pF R_L = 2.0kΩ		33		39	ns
t_{PHL}					45		54	
t_{PHL}	Clear to Y				43		51	ns
t_s	Data (D_i)			12		15		ns
t_h	Data (D_i)			12		15		ns
t_s	Enable ($\overline{E}$)	Active		17		20		ns
		Inactive		20		23		
t_h	Enable ($\overline{E}$)			0		0		ns
t_s	Clear Recovery (In-Active) to Clock			13		15		ns
t_{pw}	Clock	HIGH		25		30		ns
		LOW		30		35		
t_{pw}	Clear			22		25		ns
t_{ZH}	$\overline{OE}$ to Y_i				19		25	ns
t_{ZL}					30		39	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0KΩ		35		40	ns
t_{LZ}					39		42	
f_{max}	Maximum Clock Frequency (Note 1)			25		20		MHz

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

03598A

Refer to Page 13-1 for Essential Information on Military Devices

Am2921

One-of-Eight Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- AC parameters specified over operating temperature and power supply ranges.

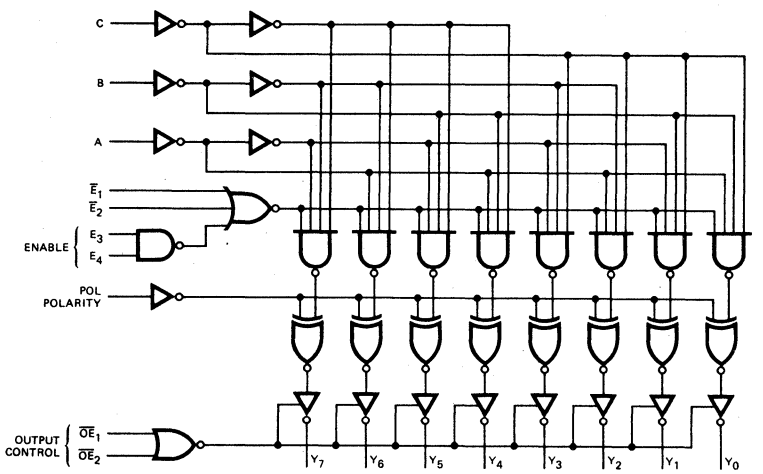
GENERAL DESCRIPTION

The Am2921 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B, and C, which are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



BD002550

RELATED PRODUCTS

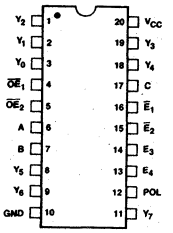
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am2924	3 to 8 Line Decoder/ Demultiplexer

03599B

Refer to Page 13-1 for Essential Information on Military Devices

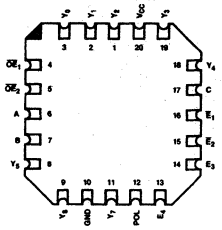
CONNECTION DIAGRAM
Top View

P-20
D-20
F-20*



CD004710

L-20-1



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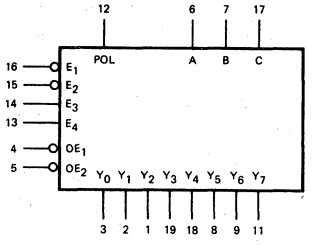
*F-20 pin configuration identical to D-20, P-20.

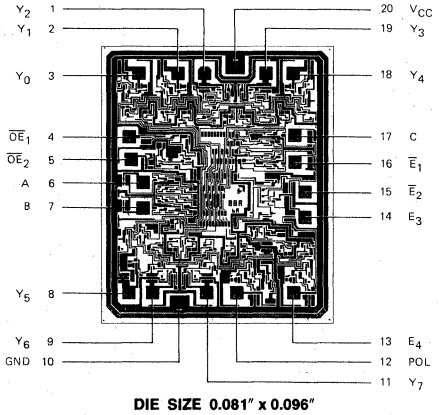
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS001070

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.081" x 0.096"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2921 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 20-pin plastic DIP
  - X– Dice
- **Am2921** — Device type
  - 1-of-8 Decoder

Valid Combinations	
Am2921	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

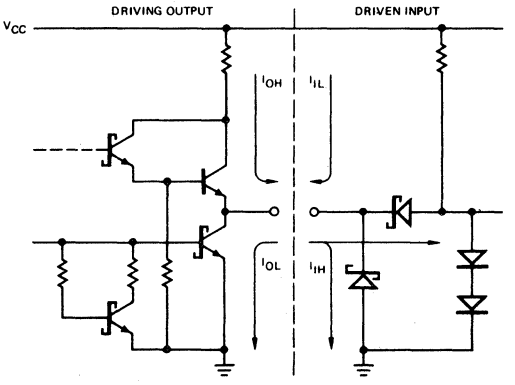
Pin No.	Name	I/O	Description
6, 7, 17	A, B, C	I	The three select inputs to the decoder/demultiplexer.
16, 15	$\overline{E}_1$, $\overline{E}_2$	I	The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.
14, 13	E_3, E_4	I	The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.
12	POL	I	Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.
4, 5	$\overline{OE}_1$, $\overline{OE}_2$	I	Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.
	Y_i	O	The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW

Pin No.'s	Input/ Ouput	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	–	50	130	33	33
2	Y_1	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	$\overline{OE}_1$	1.0	–	–	–	–
5	$\overline{OE}_2$	1.0	–	–	–	–
6	A	1.0	–	–	–	–
7	B	1.0	–	–	–	–
8	Y_5	–	50	130	33	33
9	Y_6	–	50	130	33	33
10	GND	–	–	–	–	–
11	Y_7	–	50	130	33	33
12	POL	1.0	–	–	–	–
13	E_4	1.0	–	–	–	–
14	E_3	1.0	–	–	–	–
15	$\overline{E}_2$	1.0	–	–	–	–
16	$\overline{E}_1$	1.0	–	–	–	–
17	C	1.0	–	–	–	–
18	Y_4	–	50	130	33	33
19	Y_3	–	50	130	33	33
20	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

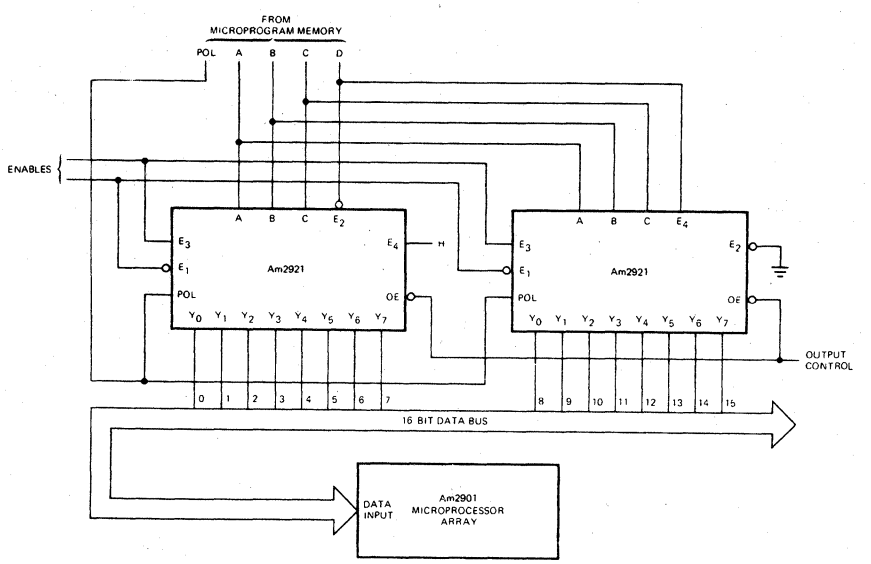
Note: Actual current flow direction shown.

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High-Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	H	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	H	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	H	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	H	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	H	H	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	H	L	L	L	L	L	L
	L	L	L	L	H	H	H	L	H	H	H	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	H	H	H	L	L	L	L	L
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L
	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	L	L	L
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	L
	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

APPLICATIONS



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Two Am2921's can be used to perform a bit set, bit clear, bit toggle or bit test on any of sixteen bits in a microprocessor system. Examples of the operations performed are as follows:

Microprogram Control					16-Bit Field From Am2921															Am2901 ALU Function	Bit Function Performed On Selected Register
D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	OR	BIT SET
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	AND	BIT TEST
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	AND	BIT CLEAR
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	EX NOR	BIT TOGGLE
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	EX OR	BIT TOGGLE

Note: Bit test is performed using F = 0 output of Am2901.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = 1.0mA (MIL)	2.4	3.4		Volts
			I_{OH} = −2.6mA (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			21	34	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E_1}$ = $\overline{E_2}$ = GND: E_3 = E_4 = POL = $\overline{OE_1}$ = $\overline{OE_2}$ = 4.5V.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, C to Y_i	C_L = 15pF, R_L = 2.0kΩ		20	30	ns
t_{PHL}				15	22	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i			19	28	ns
t_{PHL}				20	30	
t_{PLH}	E_3, E_4 to Y_i			21	31	ns
t_{PHL}				23	34	
t_{PLH}	POL to Y_i			16	24	ns
t_{PHL}				20	30	
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i			17	25	ns
t_{ZL}				14	21	
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		17	25	ns
t_{LZ}				20	30	

03599B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am2921 Min	COMMERCIAL Am2921 Max	MILITARY Am2921 Min	MILITARY Am2921 Max	Units
t_{PLH}	A, B, C to Y_i	C_L = 50pF, R_L = 2.0kΩ		36		42	ns
t_{PHL}				29		37	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i			34		39	ns
t_{PHL}				38		45	
t_{PLH}	E_3, E_4 to Y_i			38		45	ns
t_{PHL}				43		52	
t_{PLH}	POL to Y_i			29		34	ns
t_{PHL}				39		49	
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i			38		45	ns
t_{ZL}				23		25	
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		29		33	ns
t_{LZ}				33		36	

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am2922

Eight Input Multiplexer with Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Three-state output for expansion
- Common register enable, asynchronous register clear
- AC parameters specified over operating temperature and power supply ranges

GENERAL DESCRIPTION

The Am2922 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

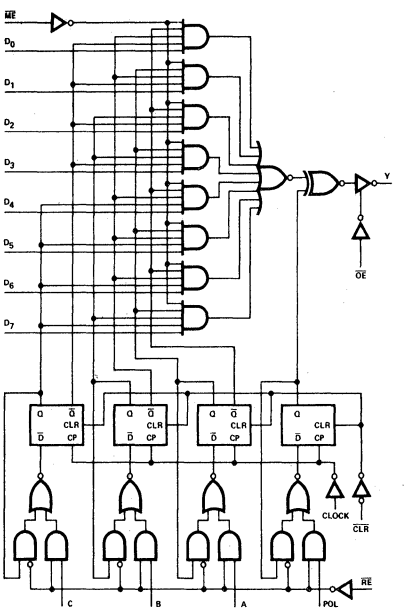
The Am2922 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (Polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am2922 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

BLOCK DIAGRAM



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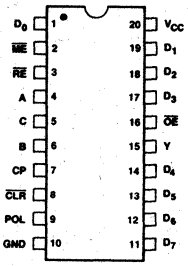
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

P-20
D-20



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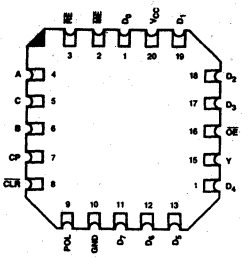
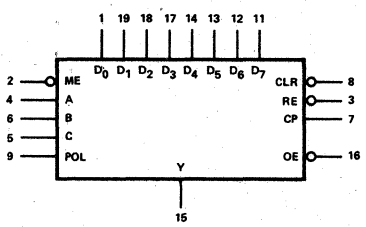
L-20-1



CD004720

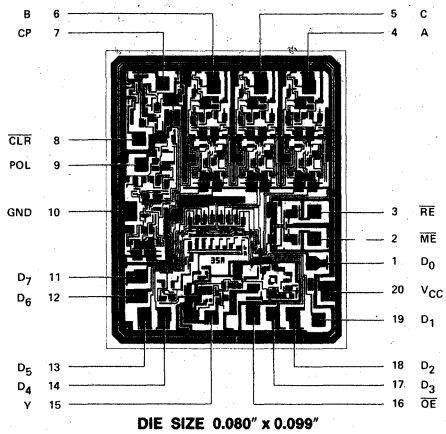
Note: Pin 1 is marked for orientation
F-20 pin configuration identical to D-20, P-20.

LOGIC SYMBOL



LS001010

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2922 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D– 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P– 20-pin plastic DIP
  - X– Dice
- Am2922 — Device type
  - 8-Input Multiplexer

Valid Combinations	
Am2922	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 6, 5	A, B, C	I	Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.
9	POL	I	Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.
2	$\overline{ME}$	I	Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.
3	$\overline{RE}$	I	Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.
8	$\overline{CLR}$	I	Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.
	D_1-D_8	I	Data Inputs to the 8-input multiplexer.
7	CP	I	Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.
16	$\overline{OE}$	I	Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.
15	Y	O	The chip output.

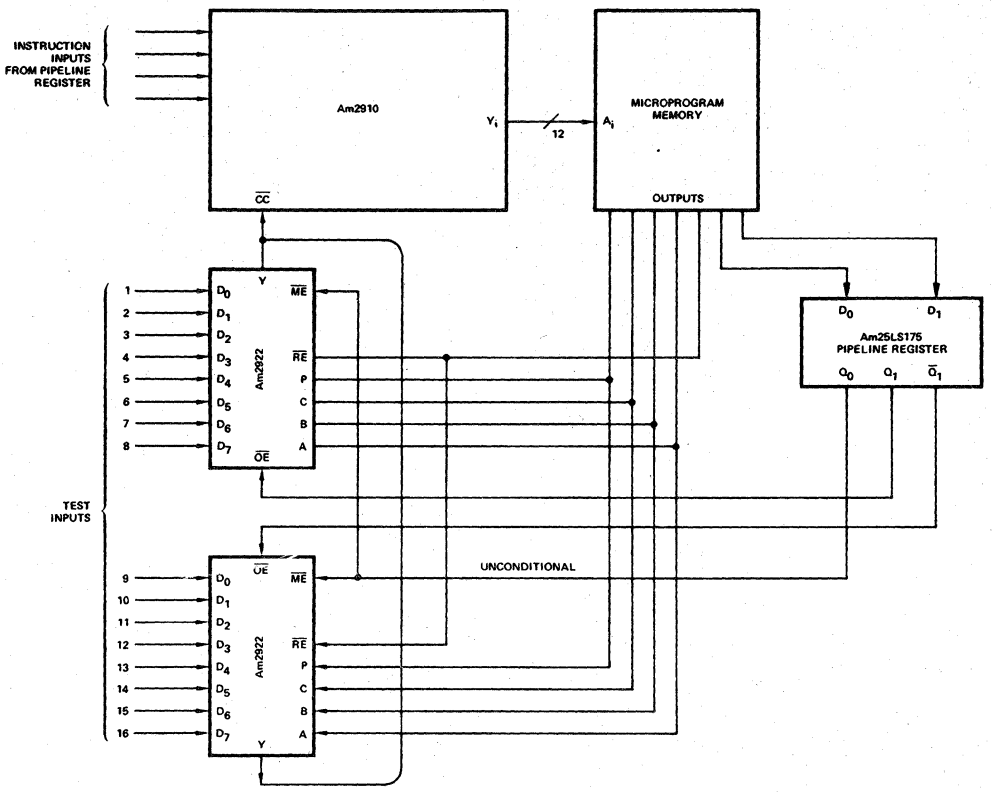
FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	$\overline{D}_i/D_i$ (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H					H	H	H				$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care
H = High
L = Low
↑ = Low-to-High Transition
Z = High-Impedance

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

APPLICATIONS



AF001840

A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 20mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L	0.8			
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			40	μ
			D_N, A, B, C, POL, CP, $\overline{CLR}$			50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			97	148	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_N, A, B, C, POL, $\overline{ME}$ at Gnd. All other inputs and outputs open. Measured after a momentary ground then 4.5V applied to clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

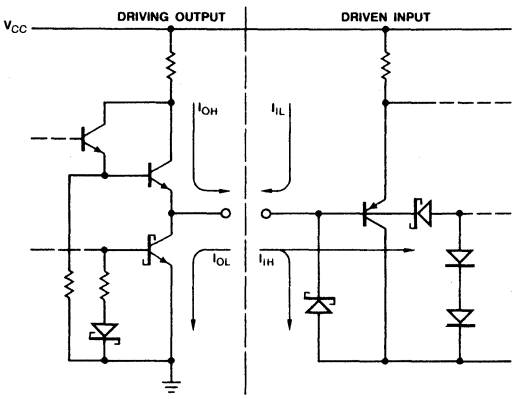
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Y POL – LOW	C_L = 15pF, R_L = 2.0kΩ		21	32	ns
t_{PHL}				19	29	
t_{PLH}	Clock to Y POL – HIGH			16	24	ns
t_{PHL}				19	29	
t_{PLH}	D_n to Y			10	16	ns
t_{PHL}				13	19	
t_{PLH}	CLR to Y			22	33	ns
t_{PHL}				22	33	
t_{PLH}	$\overline{ME}$ to Y			12	18	ns
t_{PHL}				12	18	
t_{ZL}	$\overline{OE}$ to Y			8	14	ns
t_{ZH}				8	14	
t_{LZ}		C_L = 5.0pF, R_L = 2.0kΩ		10	17	ns
t_{HZ}				10	17	
t_s	A, B, C, POL	C_L = 15pF, R_L = 2.0kΩ	10			ns
	CE		15			
t_s	CLR Recovery		5			ns
t_{pw}	Clock		10			ns
	Clear (LOW)		10			
t_h	A, B, C, POL, CE		0			ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am2922 Min	COMMERCIAL Am2922 Max	MILITARY Am2922 Min	MILITARY Am2922 Max	Units
t_{PLH}	Clock to Y POL – LOW	C_L = 50pF, R_L = 2.0kΩ		40		47	ns
t_{PHL}				34		38	
t_{PLH}	Clock to Y POL – HIGH			29		33	ns
t_{PHL}				35		41	
t_{PLH}	D_n to Y			19		21	ns
t_{PHL}				22		24	
t_{PLH}	CLR to Y			39		45	ns
t_{PHL}				39		45	
t_{PLH}	$\overline{ME}$ to Y			22		26	ns
t_{PHL}				19		20	
t_{ZL}	$\overline{OE}$ to Y			19		24	ns
t_{ZH}				22		29	
t_{LZ}		C_L = 5.0pF, R_L = 2.0kΩ		24		30	ns
t_{HZ}				24		30	
t_s	A, B, C, POL	C_L = 50pF, R_L = 2.0kΩ	11		12		ns
	CE		18		20		
t_s	CLR Recovery		6		7		ns
t_{pw}	Clock		11		12		ns
	Clear (LOW)		11		12		
t_h	A, B, C, POL, CE		3		3		ns

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000381

Note: Actual current flow direction shown.

RELATED PRODUCTS

Part No.	Description
Am25LS2535	8-Input Multiplexer
Am2923	8-Input Multiplexer

Am2923

Eight-Input Multiplexer

DISTINCTIVE CHARACTERISTICS

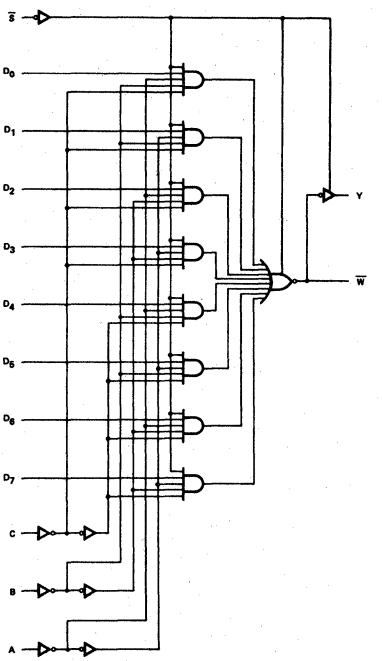
- Advanced Schottky technology
- 3-state output for bus organized systems
- Switches one of eight inputs to two complementary outputs

GENERAL DESCRIPTION

The Am2923 is an 8-input multiplexer that switches one of eight inputs onto the inverting and non-inverting outputs under the control of a 3-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am2923 features a 3-state output for data bus organization. The active-LOW strobe, or "output control", applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

BLOCK DIAGRAM



BD002360

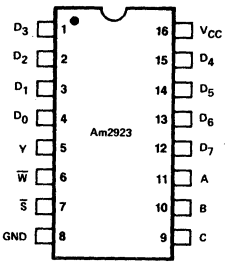
RELATED PRODUCTS

Part No.	Description
Am2922	8 Input MUX with Register Control
Am25LS2535	8 Input MUX with Register Control

03601B

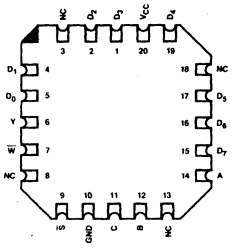
CONNECTION DIAGRAM
Top View

P-16
D-16
F-16*



CD004530

L-20-1

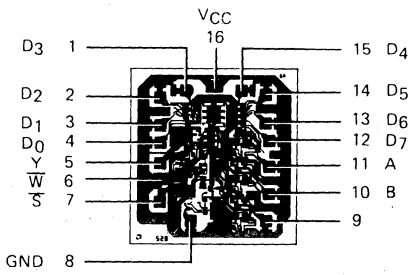


CD004540

Note: Pin 1 is marked for orientation
*F-16 pin configuration identical to D-16, P-16.

5

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.064" x 0.067"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2923 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 16-pin plastic DIP
  - X– Dice
- **Am2923** — Device type
  - 8-Input Multiplexer

Valid Combinations	
Am2923	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

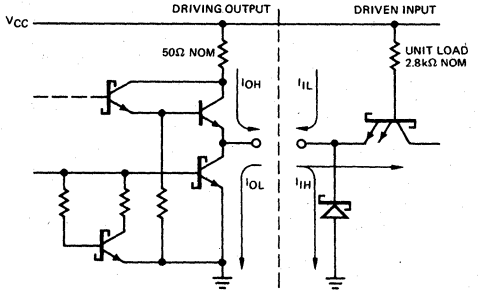
Pin No.	Name	I/O	Description
9, 10, 11	A,B,C	I	The three select inputs of the multiplexer.
	D_0,D_1 D_2,D_3, D_4,D_5 D_6,D_7	I	The eight data inputs of the multiplexer.
5	Y	O	The true multiplexer output.
6	$\overline{W}$	O	The complement multiplexer output.
7	$\overline{S}$	I	Output Control. HIGH on the output control (or strobe) forces both the $\overline{W}$ and Y outputs to the high-impedance (off) state.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			Output Control		
C	B	A	$\overline{S}$	Y	$\overline{W}$
X	X	X	H	Z	Z
L	L	L	L	D_0	D_0
L	L	H	L	D_1	D_1
L	H	L	L	D_2	D_2
L	H	H	L	D_3	D_3
H	L	L	L	D_4	D_4
H	L	H	L	D_5	D_5
H	H	L	L	D_6	D_6
H	H	H	L	D_7	D_7

H = HIGH X = Don't Care
L = LOW Z = High Impedance
D_0-D_7 = The output will follow the HIGH-level or LOW-level of the selected input.
$\overline{D_0}$-$\overline{D_7}$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000370

Note: Actual current flow direction shown.

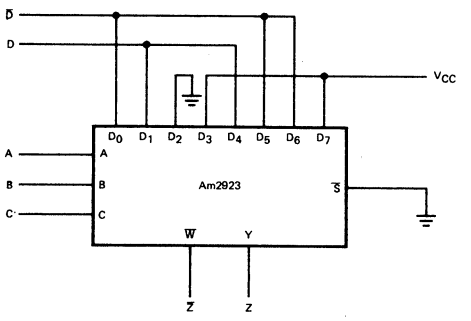
LOADING RULES (In Unit Loads)

Input/ Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_3	1	1	–	–
D_2	2	1	–	–
D_1	3	1	–	–
D_0	4	1	–	–
Y	5	–	20	10
$\overline{W}$	6	–	20	10
$\overline{S}$	7	1	–	–
GND	8	–	–	–
C	9	1	–	–
B	10	1	–	–
A	11	1	–	–
D_7	12	1	–	–
D_6	13	1	–	–
D_5	14	1	–	–
D_4	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

APPLICATIONS

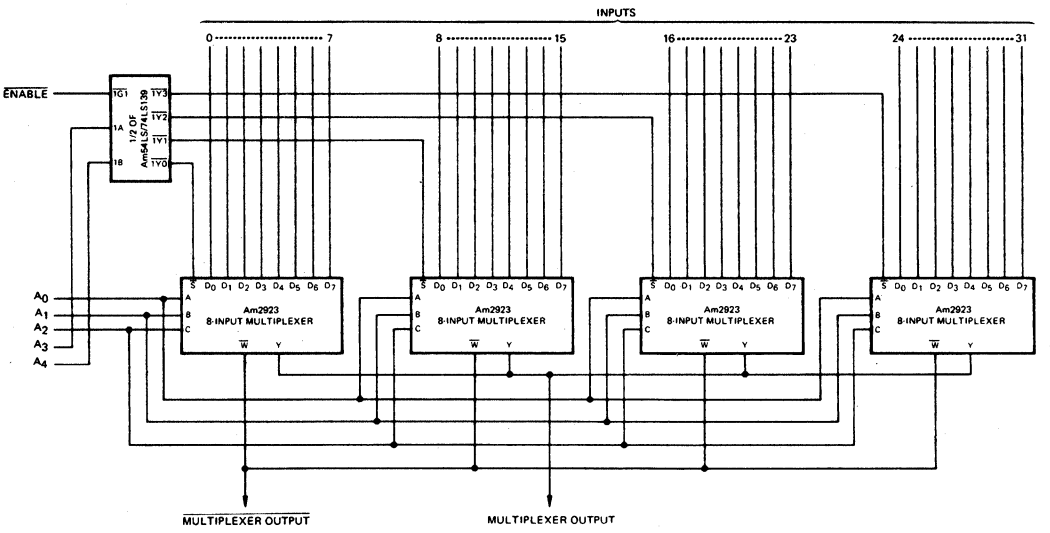
LOGIC FUNCTION GENERATION



AF002060

$Z = ABCD + \bar{A}\bar{B}CD + A\bar{C}D + \bar{A}B + AC\bar{D} + \bar{B}CD$

32-INPUT MULTIPLEXER



AF001690

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2mA	2.4	3.4		
			COM'L, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1	mA
$I_{O(off)}$	Off-State (High-Impedence) Output Current	V_{CC} = MAX, V_O = 2.4V V_{IN} = V_{IH} or V_{IL} V_O = 0.5V				50 −50	μA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 5)			55	85	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs at 4.5V.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, or C to Y; 4 Levels of Delay	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		12	18	ns
t_{PHL}				13	19.5	
t_{PLH}	A, B, or C to $\overline{W}$; 3 Levels of Delay			10	15	ns
t_{PHL}				9	13.5	
t_{PLH}	Any D to Y			8	12	ns
t_{PHL}				8	12	
t_{PLH}	Any D to $\overline{W}$			4.5	7	ns
t_{PHL}				4.5	7	
t_{ZH}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		13	19.5	ns
t_{ZL}				14	21	
t_{ZH}	Output Enable to $\overline{W}$			13	19.5	ns
t_{ZL}				14	21	
t_{HZ}	Output Enable to Y	V_{CC} = 5.0V, R_L=280Ω, C_L = 5pF		5.5	8.5	ns
t_{LZ}				9	14	
t_{HZ}	Output Enable to $\overline{W}$			5.5	8.5	ns
t_{LZ}				9	14	

03601B

Refer to Page 13-1 for Essential Information on Military Devices

Am2924

Three-Line to Eight-Line Decoder/Demultiplexer

DISTINCTIVE CHARACTERISTICS

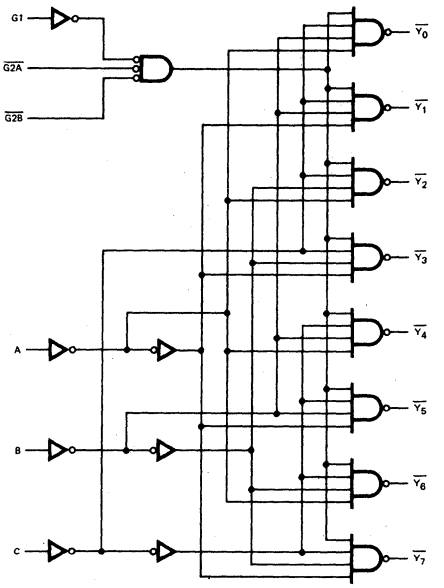
- Advanced Schottky technology
- Inverting and non-inverting enable inputs

GENERAL DESCRIPTION

The Am2924 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight $\overline{Y}$ outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight $\overline{Y}$ outputs are HIGH regardless of the A, B and C select inputs.

BLOCK DIAGRAM



BD002380

RELATED PRODUCTS

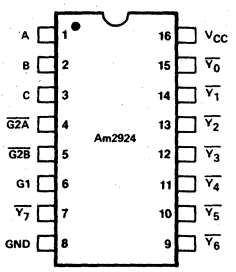
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder

03602B

Refer to Page 13-1 for Essential Information on Military Devices

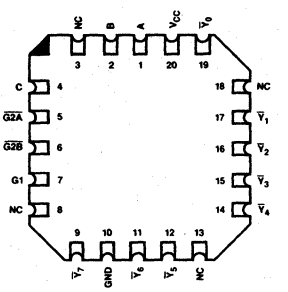
CONNECTION DIAGRAM
Top View

P-16
D-16
F-16*



CD004550

L-20-1

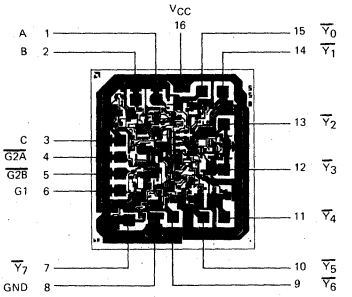


CD004560

*F-16 pin configuration identical to D-16, P-16.

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.065" x 0.070"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2924 **D** **C** **B**

- **B** — Screening Option: Blank – Standard processing; B – Burn-in
- **C** — Temperature (See Operating Range): C – Commercial (0 to +70°C); M – Military (–55 to +125°C)
- **D** — Package: D– 16-pin CERDIP; F– 16-pin flatpak; L– 20-pin leadless chip carrier; P– 16-pin plastic DIP; X– Dice
- **Am2924** — Device type: Decoder/Demultiplexer

Valid Combinations	
Am2924	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

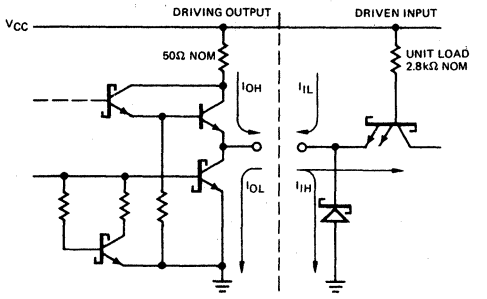
Pin No.	Name	I/O	Description
1, 2, 3	A, B, C	I	A, B, C Select. The three select inputs to the decoder.
6	G1	I	The active-HIGH enable input. A LOW on the G1 input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.
4,5	$\overline{G2A}$, $\overline{G2B}$	I	The active-LOW enable input. A HIGH on either the $\overline{G2A}$ or $\overline{G2B}$ input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.
15, 14, 13 12, 11, 10 9, 7	$\overline{Y_0}$, $\overline{Y_1}$, $\overline{Y_2}$, $\overline{Y_3}$, $\overline{Y_4}$, $\overline{Y_5}$, $\overline{Y_6}$, $\overline{Y_7}$	O	The eight decoder outputs.

FUNCTION TABLE

Inputs						Outputs							
Enable			Select										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000370

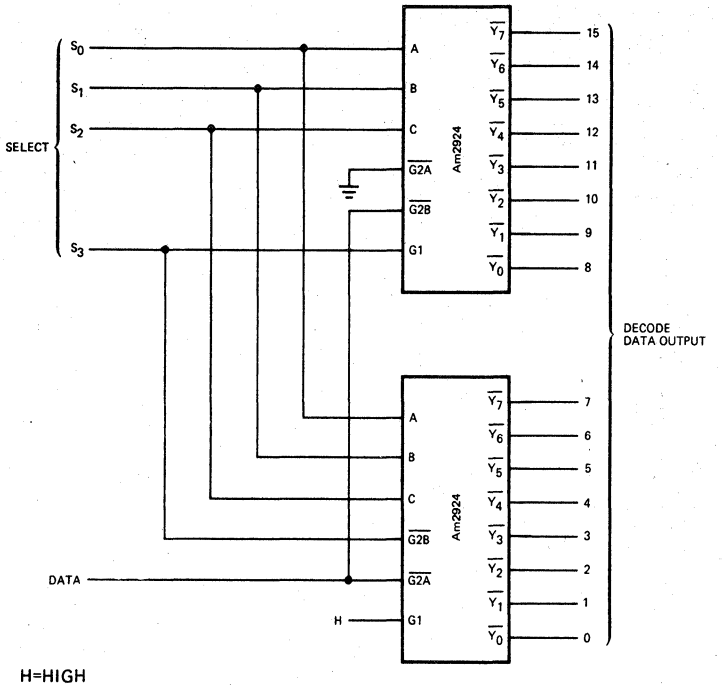
Note: Actual current flow direction shown.

LOADING RULES (In Unit Loads)

Input/ Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A	1	1	–	–
B	2	1	–	–
C	3	1	–	–
$\overline{G2A}$	4	1	–	–
$\overline{G2B}$	5	1	–	–
G1	6	1	–	–
$\overline{Y_7}$	7	–	20	10
GND	8	–	–	–
$\overline{Y_6}$	9	–	20	10
$\overline{Y_5}$	10	–	20	10
$\overline{Y_4}$	11	–	20	10
$\overline{Y_3}$	12	–	20	10
$\overline{Y_2}$	13	–	20	10
$\overline{Y_1}$	14	–	20	10
$\overline{Y_0}$	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

APPLICATIONS



AF002010

One-of-Sixteen Demultiplexer

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 5)			49	74	mA

Notes: 1. For conditions shown as MIN or MAX, use the the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output enabled and open.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Two Level Delay Select to Output	V_{CC} = 5V, C_L = 15pF, R_L=280Ω		4.5	7	ns
t_{PHL}				7	10.5	
t_{PLH}	Three Level Delay Select to Output			7.5	12	ns
t_{PHL}				8	12	
t_{PLH}	$\overline{G2A}$ or $\overline{G2B}$ to Output			5	8	ns
t_{PHL}				7	11	
t_{PLH}	G1 to Output			7	11	ns
t_{PHL}				7	11	

Am2925

Clock Generator and Microcycle Length Controller

DISTINCTIVE CHARACTERISTICS

- **Crystal controlled oscillator**
  Stable operation from 1MHz to over 31MHz
- **Four microcode controlled clock outputs**
  Allows clock cycle length control for 15–30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- **System controls for $\overline{\text{Run}}/\overline{\text{Halt}}$ and Single Step**
  Switch debounced inputs provide flexible halt controls
- **Slim 0.3″ 24-pin package**
  LSI complexity in minimum board area

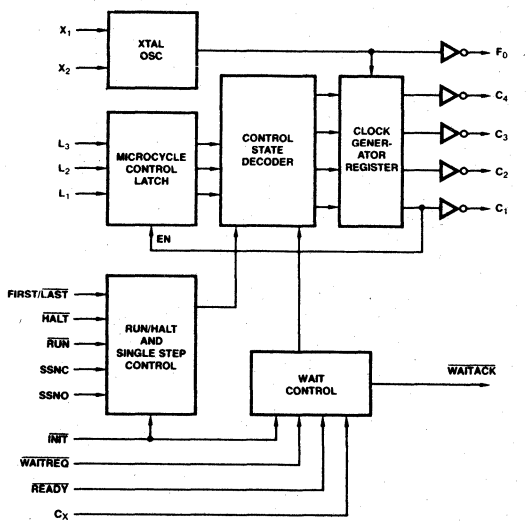
GENERAL DESCRIPTION

The Am2925 is a single-chip general purpose clock generator/driver. It is crystal controlled, and has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meet a variety of system speed requirements. The Am2925 generates four different simultaneous clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925 oscillator runs at frequencies to over 31MHz. A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

System control functions include Run, Halt, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/$\overline{\text{LAST}}$ input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. $\overline{\text{WAITACK}}$ indicates that the Am2925 is in a wait state.

BLOCK DIAGRAM



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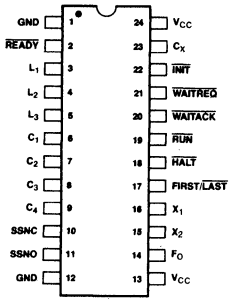
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-24-Slim



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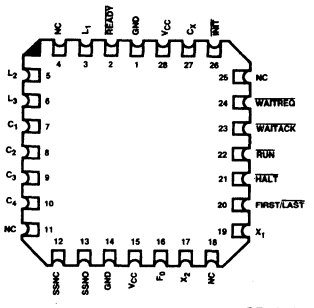
L-28-1



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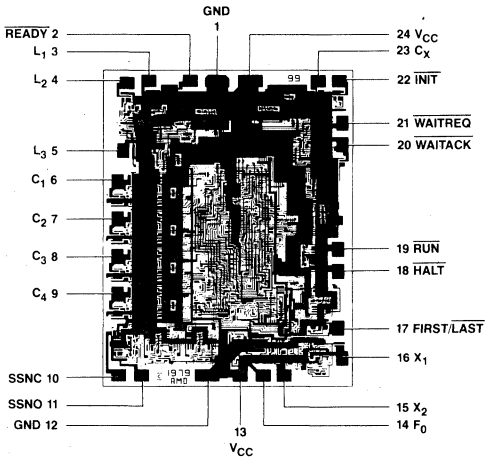
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.097″ x .122″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2925 **D** **C** **B**

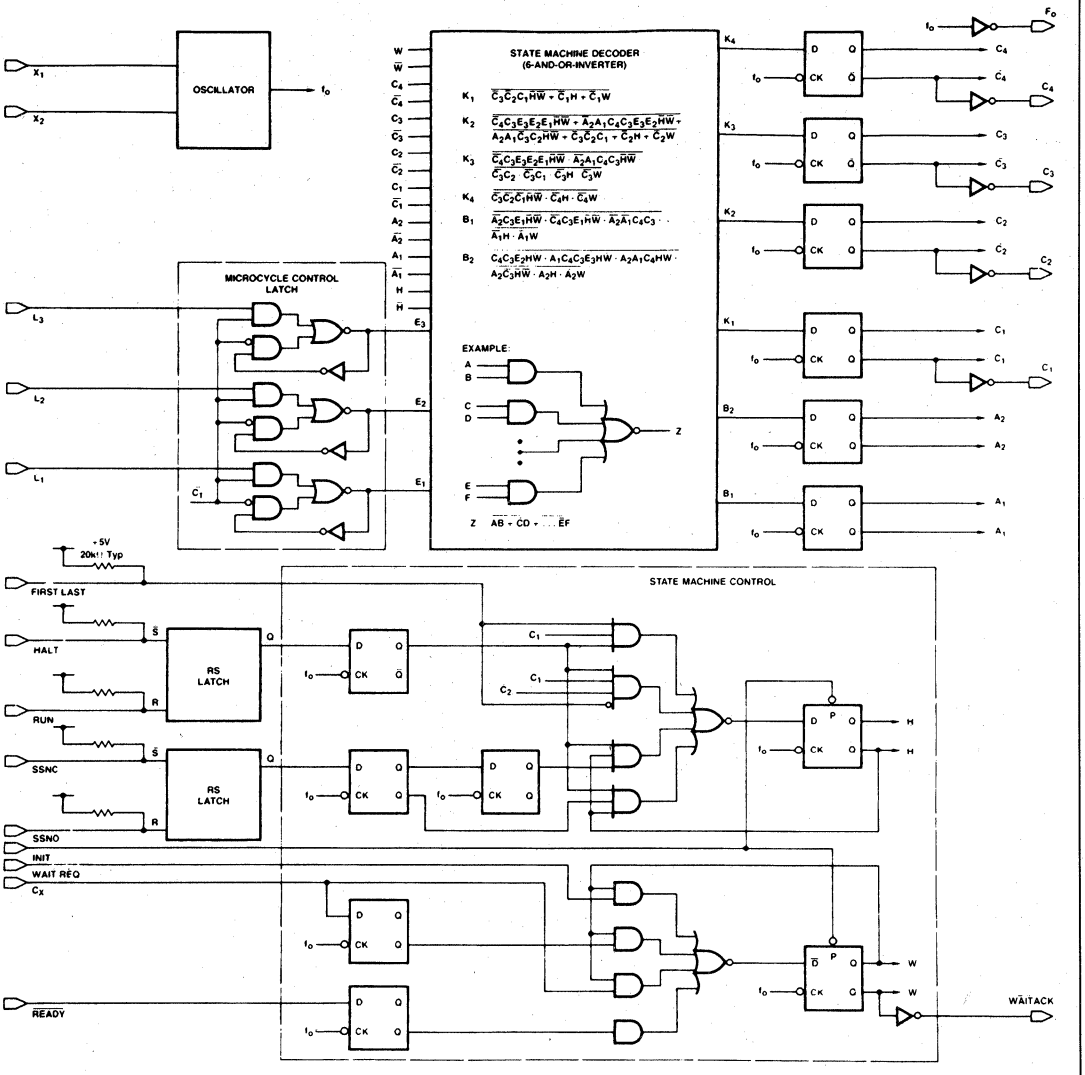
- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 24-pin SLIMDIP
  - L – 28-pin leadless chip carrier
  - X – Dice
- **Am2925** — Device type: Clock Generator

Valid Combinations	
Am2925	DC, DCB, DMB LC, LCB, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

LOGIC DIAGRAM



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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
6, 7, 8, 9	C_1, C_2 C_3, C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2, and L_3.
3, 4, 5	L_1, L_2, L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
14	F_0	O	The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
18, 19	$\overline{HALT}$ and $\overline{RUN}$	I	Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.
17	FIRST/$\overline{LAST}$	I	$\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
11, 10	SSNO and SSNC	I	Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.
21	$\overline{WAITREQ}$	I	The Wait Request active LOW input. When LOW this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.
23	C_X	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.
20	$\overline{WAITACK}$	O	The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
2	$\overline{READY}$	I	The $\overline{READY}$ active LOW input is used to continue normal clock output patterns after a wait stage.
22	$\overline{INIT}$	I	The Initialize active LOW input. This input is intended for use during power up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.
16, 15	X_1, X_2	I, O	External crystal connections. X_1 can also be driven by a TTL frequency source.

DETAILED DESCRIPTION

The Am2925 is a dynamically programmable general-purpose clock generator/driver. It can be logically separated into three parts. There is an oscillator, a state machine decoder and a state machine control section.

The oscillator is a linear inverting amplifier which may be configured with a minimum of external parts as a 1st harmonic* crystal oscillator, 3rd harmonic* crystal oscillator, L-C oscillator or used to buffer an external clock. The buffered, inverted output of this oscillator is available as F_0.

The state machine takes microcode information from the Microcycle Length "L" inputs L_1, L_2 and L_3 and counts the fundamental frequency of the internal oscillator, F_0, to create the clock outputs, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximately 50% duty cycle, and C_2 is HIGH for all but the last two periods.

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into a set of combinatorial logic to generate the next state. On each falling edge of the internal clock the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle (C_1 = C_2 = C_3 = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the Am2925 comprised of Run, Halt, Wait and Single Step.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The Am2925 allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

This application section will cover several aspects of the Am2925. The first topic to be covered is the oscillator section which is responsible for providing the basis of all system timing. Second will be how to operate the Am2925; last will be an example of an Am2925 in a 16-bit microprogrammed machine.

*It is understood that the terms "fundamental mode" and "3rd overtone" are generally regarded as more technically correct, but "1st harmonic" and "3rd harmonic" are used here because of their more generally accepted usage.

OSCILLATOR

The Am2925 contains an inverting, linear amplifier which is intended to form the basis of a crystal oscillator. In designing this oscillator it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am2925 is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO). For extreme temperature stability, an oven must be used or some other form of temperature compensation applied.

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32pF), or to specify the load when ordering a special crystal. It should then be possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20-25MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies and additional components are included in the oscillator circuit to prevent it oscillating at lower harmonics.

Where a high degree of accuracy or stability is not required, the amplifier may be configured as an L-C oscillator. It may also be driven from an external clock source if operation is required in synchronism with that source.

1st Harmonic (Fundamental) Oscillator

The circuit of a typical 1st harmonic oscillator is shown in Figure 1. The crystal load is comprised of the two 68pF capacitors in series. This 34pF approximates the standard 32pF crystal load. If a closer match is required then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range: 5–20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17—for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temp

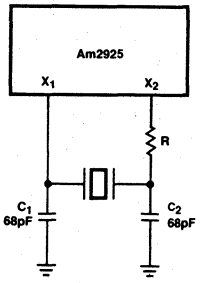

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Figure 1. Connections for 5–20 MHz.

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Note: At fundamental frequencies below 5MHz it is possible for the oscillator to operate at the 3rd harmonic. To prevent this a resistor should be added in series with the X_2 pin as shown in the circuit diagram.

The resistor value should match the impedance of C_2:

$$R = X_{C_2} = \frac{1}{2\pi f C_2}$$

3rd Harmonic Oscillator

At frequencies greater than 20MHz the crystal can be operated at its 3rd harmonic. A typical circuit is shown in Figure 2. Two additional components are included; an inductor, L_1, and a capacitor, C_3. The purpose of the capacitor is to block the d.c. path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large ($\geq$ 1000pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the 1st and 3rd harmonics of the crystal and is used to prevent the oscillator operating at the 1st harmonic. In the 1st harmonic oscillator (Figure 1), the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the 3rd harmonic oscillator, L_1 and C_1 are chosen such that at the 3rd harmonic the impedance of circuit is equivalent to that of the capacitor C_2 in the 1st harmonic oscillator (Figure 3b). Thus, the same π-network is formed (Figure 3c) and oscillation is possible. At the 1st harmonic the tuned circuit appears as an inductor (Figure 3a), the π-network is not formed and oscillation is not possible.

The following specification is typical for a crystal to be used in a 3rd harmonic oscillator.

Frequency Range: Above 20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 — for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change temp

Again it is good practice to ground the crystal case and keep connections short.

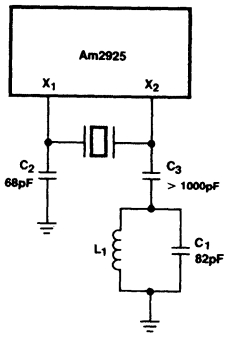

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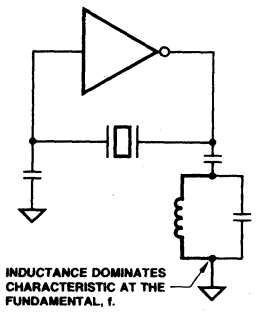
Figure 2. Connections for Frequencies above 20MHz.



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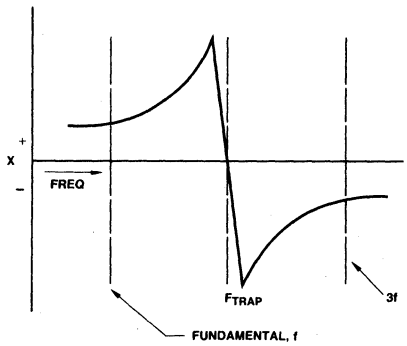
a) Fundamental Equivalent



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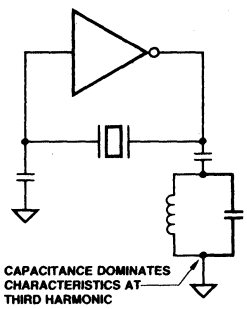
b) Trap Impedance



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c) 3rd Harmonic Equivalent

Figure 3. Forcing Third Harmonic Oscillation.

Design Procedure

(1) Assume C_1 = 82pF and C_2 = 68pF (this gives a sensible inductor value). L_1 is calculated according to the formula:

$$L_1 = \frac{1151}{f_o{}^2} \qquad f_o = \text{Operating frefquency in MHz}, \; L_1 \text{ in } \mu H$$

This sets the resonant frequency of the L-C combination at 0.52 f_o.

(2) Select the closest standard value inductor for L_1. Using this value calculate C_1 such that the resulting crystal load at the 3rd harmonic is 32pF.

$$C_1 = 60 + \frac{25330}{L_1 \cdot f_o{}^2} \qquad C_1 \text{ in pF.}$$

Choose the closest standard capacitor value to this.

Using standard values both the resonant frequency of the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible C_1 may be a fixed capacitor in parallel with a trimmer such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency. In either case the approximate inductor value will cause the resonant frequency to the L-C circuit to change. This frequency, f_r, may be computed and should remain approximately midway between the 1st and 3rd harmonic.

$$f_r = \frac{159}{\sqrt{L_1 C_1}} \qquad f_r \text{ in MHZ}, \; L_1 \text{ in } \mu H, \; C_1 \text{ in pF}$$

L-C Oscillator

The Am2925 can be operated as an L-C tuned oscillator (Figure 4) and will perform as a stable oscillator within the restrictions of the chosen frequency determining components (i.e., inductor and capacitors). The circuit chosen is a classical π-network with DC loop isolation. The Am2925 oscillator is a DC biased linear amplifier. This DC bias is necessary and therefore C_3 is included to block the DC path through the inductor. If a variable slug tuned inductor is used a moderate range of frequency adjustment tuneability (approximately 2:1) can be achieved. The range can be enhanced by switching the two resonant capacitors (C_1, C_2) to larger or smaller values. The specific frequency of operation can be determined by the formula:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(where C is } C_1 \text{ and } C_2 \text{ in series).}$$

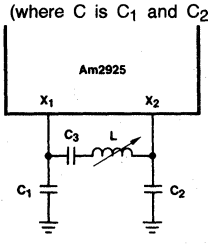

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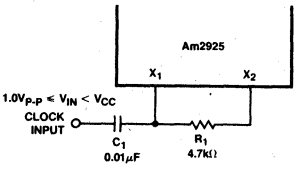
Figure 4. L-C Tuned Oscillator.

External Clock Drive

The Am2925 can be driven from an external clock source at a signal level of 1.0V P-P or greater. This is accomplished by reducing the gain of the amplifier and AC coupling the input signal (Figure 5). The gain is reduced by feeding the amplifier output back to the input through a 4.7kΩ resistor. AC coupling is provided by a 0.01μF capacitor. The controlled gain minimizes ringing caused by the fast rising edges of the driver. The AC coupling maintains oscillator output symmetry by preserving oscillator DC bias levels.

X_1 can be driven directly by TTL levels meeting the DC input requirements.



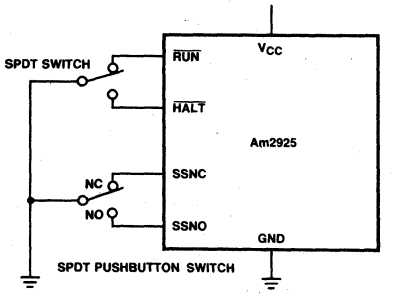
DF000880

Figure 5. External Clock Drive.

Am2925 Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch. The Microcycle Latch performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 6). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the Am2925 will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications the user wires this input HIGH or LOW depending on his design.



DF000860

Figure 6. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step.

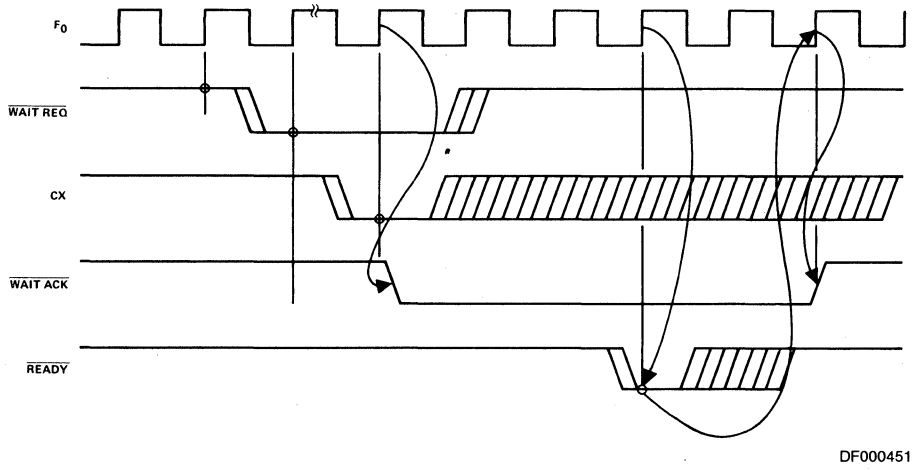


Figure 7. Am2925 WAIT/READY Timing.

When HALT is held low (RUN = HIGH) the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/LAST input. When RUN goes low (HALT = HIGH) the state machine will resume the run mode.

The WAITREQ, C_X, READY and WAITACK signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds in which case the peripheral pulls the WAITREQ line LOW. The C_X input lets the designer specify when the WAITREQ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 7). The READY line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The WAITACK line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after READY goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been low for one clock edge, the state machine will change to the run mode. The microcycle will end on the first or last state of the microcycle depending on the state of the FIRST/LAST.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the Am2925, the crystal oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference for set-up, hold and clock to output times. However for the Microcontrol Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcontrol Latch because in a typical application this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

Clock Outputs

There are four clock outputs provided for the user which have different duty cycles. The user must make a decision as to which one best fits his purposes. For example, in a three address architecture, with the Am2903 (Figure 8), the C_3 clock (approximately 50% duty cycle) could be used to drive the clock input while C_2 (always low last two oscillator cycles) drives Instruction Enable. This guarantees, for microcycle lengths greater than four, that the internal RAM data latches of the Am2903 are closed and the destination address is multiplexed onto the B address bus before the RAM begins the Write cycle (Figure 9).

16-BIT MACHINE WITH Am2925

The block diagram in Figure 10 shows a 16-bit microprogrammed machine which uses an Am2925 to generate system timing. The design decisions include oscillator frequency and clock pattern selections.

Selecting the Crystal

In order to pick the oscillator frequency, a detailed timing analysis of the machine must be done in order to determine the execution length of every operation to be performed. For each operation there will be several delay paths, which usually include the ALU and the microprogram control.

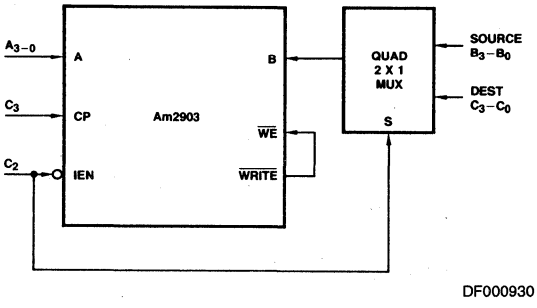


Figure 8. Am2903 Three Address Architecture.

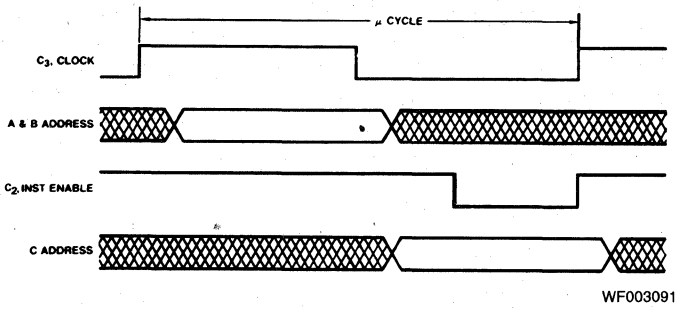


Figure 9. Am2903 Three Address Operation.

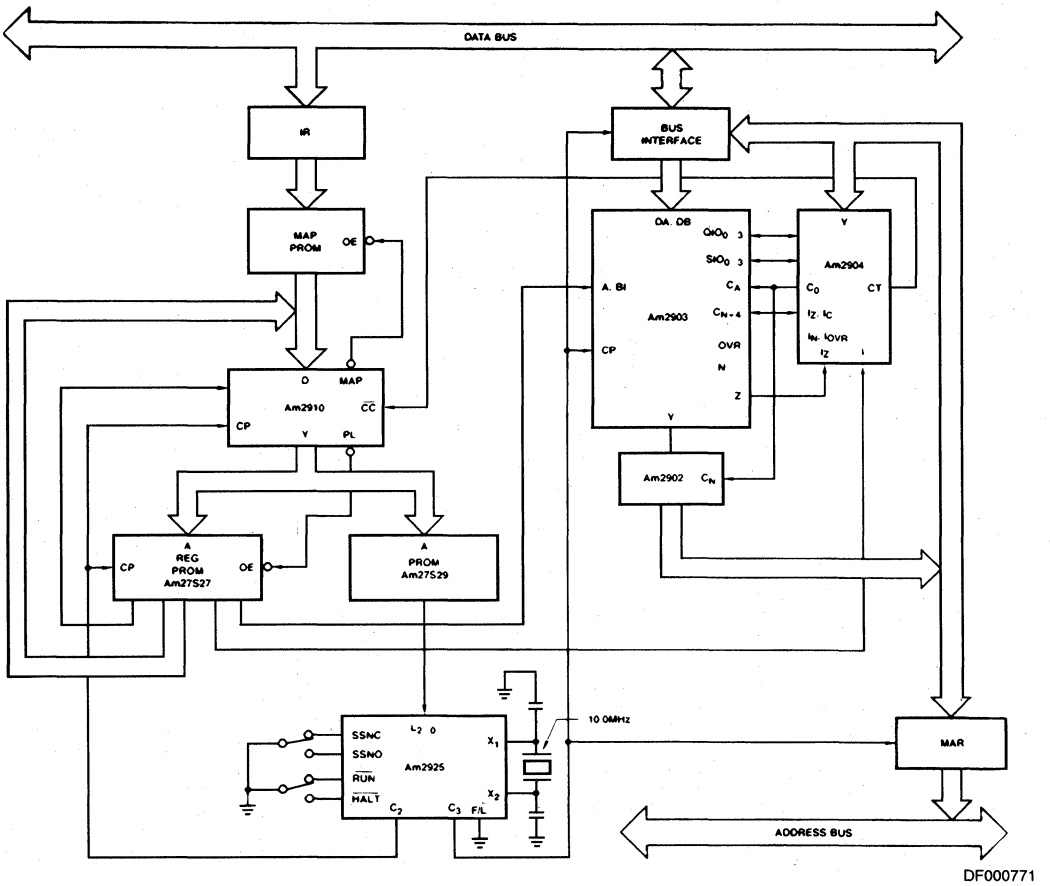


Figure 10. 16-Bit Microprogrammed Machine.

Table 1 is an example of two of these paths. PATH 1 is a path through the Am2910 (Figure 10) for a microprogram Conditional Jump Subroutine. PATH 2 is a data flow path through the Am2903 for an Add instruction. Therefore, if the operation were an Add with a Conditional Jump Subroutine the maximum delay would be 170ns. If there were a Program Control Unit also, then delays through it would have to be considered.

After the execution times all of the instruction types have been calculated, the oscillator frequency can be selected. It is desirable to minimize the difference between the most commonly used instructions and multiples of the oscillator period. In this way the most efficient use can be made of the variable microcycle scheme.

For example, in the hypothetical machine in Figure 10 there are five instruction types (most machines will have more). Table 2 is a table which lists each instruction type, corresponding execution time, and anticipated percentage of the typical instruction stream for each instruction. Several possible frequencies are shown which contain the next highest multiple of the corresponding oscillator period for each instruction. 20MHz is the best choice because it comes closest to matching instructions A and C which compose 90% of the typical instruction stream.

In this example, 20MHz was chosen. AT 20MHz there is a choice between fundamental or overtone crystals. Fundamental frequency crystals are commonly available up to 25MHz and 3rd harmonic crystals are available above 17MHz. A fundamental crystal was selected for the example machine because the component count for the oscillator design is lower than for the overtone design. However, if it had turned out that 30MHz was a better choice then overtone operation would be chosen since fundamental crystals above 25MHz are not generally available.

Fixed Bandwidth Buses

For those designs that require a data bus with fixed bandwidth and fixed time slots for each memory access, the designer should consider using cycle lengths which are a multiple of the shortest cycle length, i.e., cycle lengths 3, 6 and 9 or cycle lengths 4 and 8.

The design could further require that the bus be accessed only during the shortest cycle length. Therefore, by using multiple cycle lengths it can be predicted when the CPU will access the bus and for how long, thereby maintaining the fixed bandwidth.

Performance Comparison

Estimated performance can be calculated directly from Table 2. For a fixed microcycle machine the longest instruction execution time would have to be used for all instructions, yielding an average instruction time of 228ns. With a variable microcycle machine the average instruction time is the sum of the products for each instruction, of the percentage of the instruction stream and the next highest multiple. The average instruction for the example machine with a 20MHz crystal is:

(0.6 x 150 + .08 x 200 + .3 + 200 +
.01 x 200 + .01 + 250) = 170.5ns

This represents a 25% increase in system performance without requiring any other system speed-ups and without requiring faster devices.

Device No.	Device Path	Path 1	Path 2
Am27S27	CP – Q	27	27
Am2904	INST – CT	58	–
Am2903A	I/AB – GP	–	50
Am2910A	CC – Y	30	–
Am2902A	GP – CN + Z	–	7
Am27S27	TS	55	–
Am2903A	CN – Z	–	35
Am2904	TSZ	–	17
Total	ns	170	136

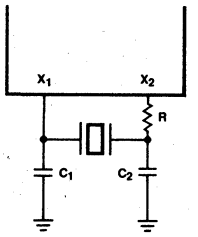
Table 1: Delay Path Totals for an Add and a Condition Jump Subroutine.

Instruction Type	A	B	C	D	E	Unit
Execution Time	143	180	184	200	228	ns
Percentage of Instruction Stream	60%	8%	30%	1%	1%	%
Closest Multiple Oscillator Period						
20MHz P = 50	150 (3P)	200 (4P)	200 (4P)	200 (4P)	250 (5P)	ns
25MHz P = 40	160 (4P)	200 (5P)	200 (5P)	200 (5P)	240 (6P)	ns
30MHz P = 33	167 (5P)	200 (6P)	200 (6P)	200 (6P)	233 (7P)	ns
33MHz P = 30	150 (5P)	180 (6P)	210 (7P)	210 (7P)	240 (8P)	ns

Table 2. Instruction Time Analysis.

Am2925 OSCILLATOR APPLICATIONS

EXTERNAL COMPONENT CALCULATIONS SUMMARY

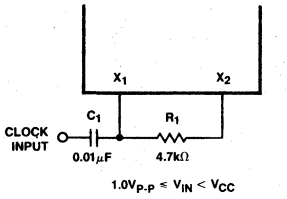


AF001770

$$R = X_{C_2} = \frac{1}{Tfc_2} \text{ for } 1-6\text{MHz}$$

$R = 0$ for $6-20$MHz

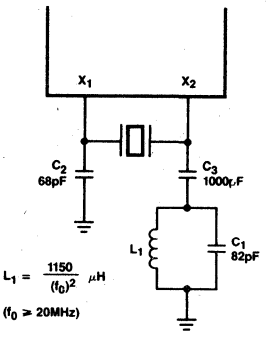
FUNDAMENTAL OSCILLATOR



$1.0V_{P\text{-}P} \leq V_{IN} < V_{CC}$

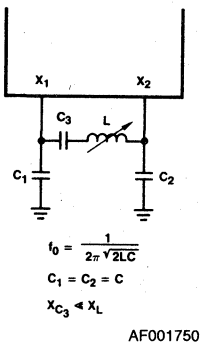
AF001760

EXTERNAL CLOCK DRIVE



AF001740

3rd HARMONIC OSCILLATOR



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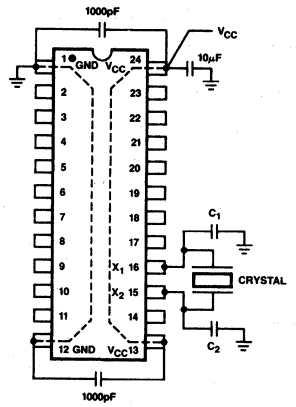
L-C OSCILLATOR

TYPICAL EXTERNAL CONNECTIONS



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DESIGN CONSIDERATIONS

1. Oscillator external connections should be less than 1″ long — wirewrap is not recommended.
2. V_{CC} and GND connections should be less than ½″ long to power plane.
3. Supply decoupling includes both high frequency and bulk storage elements.
4. The same considerations apply for 3rd overtone configurations.

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA		2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{WAITACK}$ C_i	I_{OL} = 4.0mA			0.4	Volts
				I_{OL} = 8.0mA			0.45	
				I_{OL} = 12mA			0.5	
			F_0	I_{OL} = 16mA			0.5	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Note 3)	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				−0.4	mA
			$\overline{WAITREQ}$, X_1 (See Figure 11)				−0.8	mA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−1.0	mA
			C_X				−1.2	mA
			FIRST/$\overline{LAST}$				−1.5	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				20	μA
			$\overline{WAITREQ}$				50	μA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−500	μA
			C_X				70	μA
			FIRST/$\overline{LAST}$				−750	μA
			X_1 (See Figure 11)				500	μA
I_I	Input HIGH Current	V_{CC} = MAX	V_{IN} = 5.5V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			100	μA
			V_{IN} = V_{CC}	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			100	μA
			V_{IN} = 5.5V	$\overline{WAITREQ}$, C_X			1.0	mA
			V_{IN} = V_{CC}	FIRST/$\overline{LAST}$			1.0	mA
			V_{IN} = 4.0V	X_1 (See Figure 11)			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX				85	120	mA

Notes: 1. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX use the appropriate value specified under Operating Ranges for the applicable device type.
3. Does not apply to X_1 and X_2.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} varies with temperature and oscillation frequency as shown in Figure 12. The parameters specified (worst case) applies to f_0 = 0, +25°C, C_1 = C_2 = C_3 = LOW, C_4 = HIGH, X_1 = 2.4V, X_2 = open and F_0 = LOW. The variations shown in Figure 12 apply to typical values.

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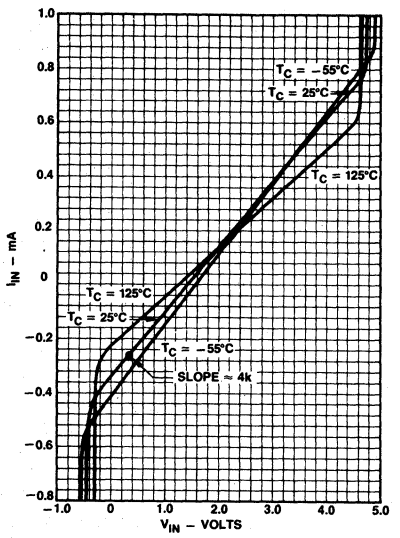
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

	Parameters	Description	Test Conditions	Min	Typ	Max	Units
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	C_L = 15pF, R_L = 280Ω	31			MHz
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)			42		
3	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)		0	5.0	7.5	ns
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)		3	11.5	16	ns
5	t_{SKEW}	C_1 (↓) to C_2 (↓)		0	0.5	2	ns
6	t_{SKEW}	C_1 (↓) to C_3 (↓)		0	0.5	2	ns
7	t_{SKEW}	C_1 (↓) to C_4 (↓) Opposite Transition		4	7	10	ns
8	t_S	L_1, L_2, L_3 to C_1 (↓)		5			ns
9	t_H	L_1, L_2, L_3 to C_1 (↓)		9			ns
10	t_S	C_X to F_0 (↓) (Note 7)		20	17		ns
11	t_H	C_X to F_0 (↓) (Note 7)		0	−10		ns
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	C_L = 50pF, R_L = 2.0kΩ	20	17		ns
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		0	−10		ns
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)		20	17		ns
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)		0	−10		ns
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↓) to F_0 (↓) (Notes 8, 9)		20	14		ns
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)		20	14		ns
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)		25	17		ns
19	t_S	$\overline{INIT}$ (↓) to F_0 (↓) (Note 8)		30			ns
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width		15	10		ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$			16	23	ns
22	t_{PLH}	Propagation Delay (Note 11)	C_L = 15pF, R_L = 280Ω		13	16	ns
23	t_{PHL}	X_1 to F_0			14	17	ns

Notes:
6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading
7. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW
8. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST normally wired HIGH or LOW.
11. Reference point of T offset has been moved forward which has increased T offsets.



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X_1 is not a TTL input. It is a crystal connection to an inverting linear oscillator amplifier, and is specified primarily for test convenience.

Figure 11. Am2925 X_1 Input Characteristics (Typical, V_{CC} = 5.0V).

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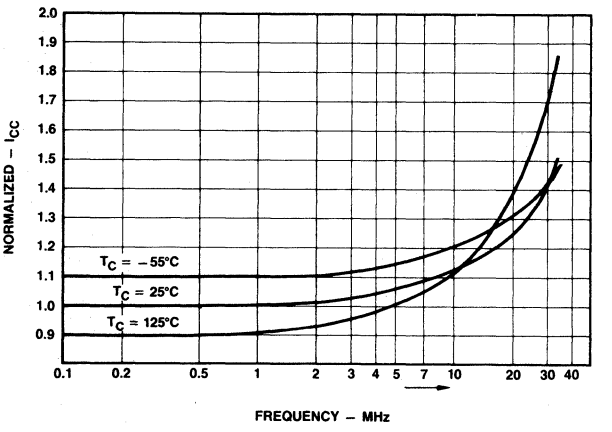
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

	Parameters	Description	Test Conditions	COMMERCIAL Am2925 Min	COMMERCIAL Am2925 Max	MILITARY Am2925 Min	MILITARY Am2925 Max	Units
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	C_L = 15pF, R_L = 280Ω	31		31		MHz
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)						
3	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)			8.5		8.5	ns
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)			17.0		18.0	ns
5	t_{SKEW}	C_1 (↓) to C_2 (↓)			2		2	ns
6	t_{SKEW}	C_1 (↓) to C_3 (↓)			2		2	ns
7	t_{SKEW}	C_1 (↓) to C_4 (↓) Opposite Transition			11		11	ns
8	t_S	L_1, L_2, L_3 to C_1 (↓)		6		7		ns
9	t_H	L_1, L_2, L_3 to C_1 (↓)		11		11		ns
10	t_S	C_X to F_0 (↓) (Note 7)		25		25		ns
11	t_H	C_X to F_0 (↓) (Note 7)	C_L = 50pF, R_L = 2.0kΩ	0		0		ns
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		25		25		ns
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		0		0		ns
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)		25		25		ns
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)		0		0		ns
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↓) to F_0 (↓) (Notes 8, 9)		25		25		ns
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)		25		25		ns
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)		30		35		ns
19	t_S	$\overline{INIT}$ (↓) to F_0 (↓) (Note 8)		33		35		ns
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width		20		25		ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$			25		27	ns
22	t_{PLH}	Propagation Delay (Note 11) X_1 to F_0	C_L = 15pF, R_L = 280Ω		23		26	ns
23	t_{PHL}				21		23	ns

Notes:
6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading
7. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW
8. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST normally wired HIGH or LOW.
11. Reference point of T offset has been moved forward which has increased T offsets.



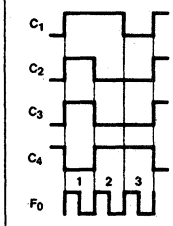
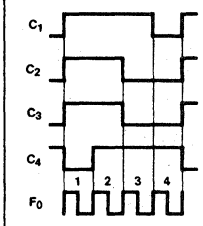
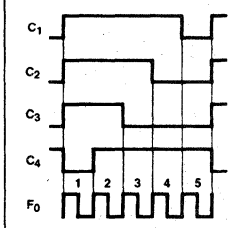
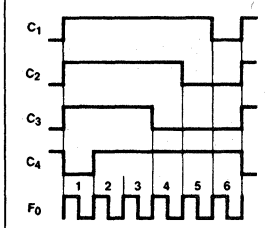
PF001090

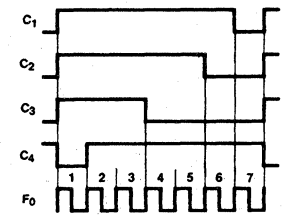
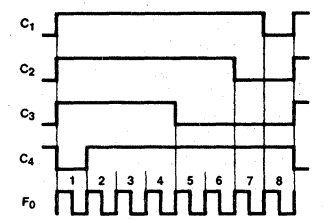
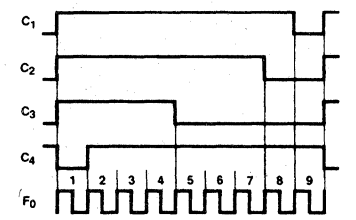
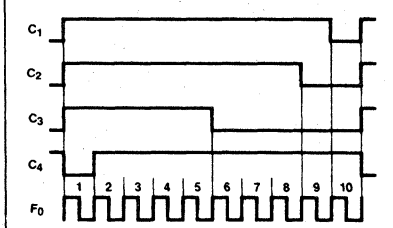
Figure 12. Am2925 I_{CC} Normalized vs Frequency (V_{CC} = 5.5V).

03367A

Refer to Page 13-1 for Essential Information on Military Devices

AM2925 CLOCK WAVEFORMS

PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_3 LLL	
F_4 LLH	
F_5 HLH	
F_6 HHH	

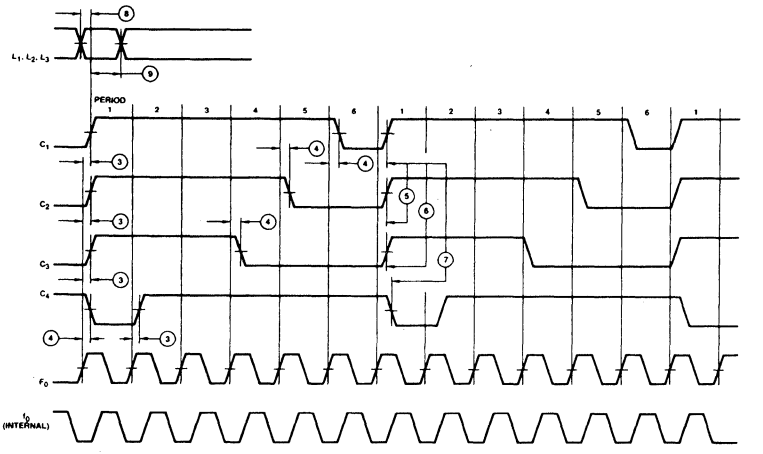
PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_7 LHH	
F_8 LHL	
F_9 HHL	
F_{10} HLL	

WF003080

03367A

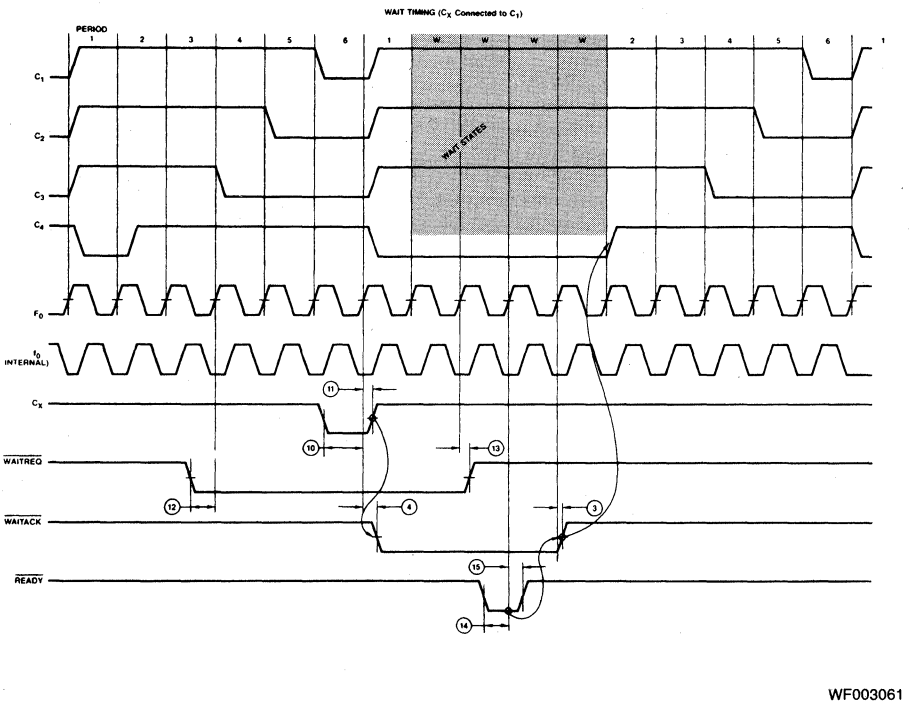
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



WF003070

NORMAL CYCLE WITHOUT WAIT STATES (Pattern F_6 Shown)



WF003061

WAIT TIMING (C_X Connected to C_1)

Am2927/Am2928

Quad Three-State Bus Transceivers With Clock Enable

DISTINCTIVE CHARACTERISTICS

- Three-state bus driver outputs can sink 48mA, and Three-state receiver outputs sink 24mA — both at 0.5V max.
- D-type register on drivers
- Latch output on Am2927; Registered output on Am2928
- Output data to input wrap around gating; Input register to output transfer gating with or without driving data bus
- Clock enabled registers
- 3.0V minimum V_{OH} for direct interface to MOS microprocessors

GENERAL DESCRIPTION

The Am2927 and Am2928 are high-performance, low-power Schottky, quad bus transceivers intended for use in bipolar or MOS microprocessor system applications.

Both devices feature register enable lines which function as clock enables without introducing gate delay in the clock inputs. The four transceivers share common enables, clock, select and three-state control lines.

The Am2927 consists of four D-type edge-triggered flip-flops. Each flip-flop output is connected to a three-state data bus driver and separately to the input of a corresponding receiver latch input. The receiver latch can select input from the driver or the data bus. The select line determines the source of input data for the bus driver choosing between input data or data recirculated from the receiver output. The receiver output also has a three-state output buffer.

The combination of the select input, S, the driver input enable, $\overline{ENDR}$, and the receiver latch enable, $\overline{RLE}$, provide seven different data path operating modes not available in other transceivers. For example, transmitted data can be stored in the receiver for subsequent retransmission. Also, received data can be output to the system and simultaneously fed back to the driver input.

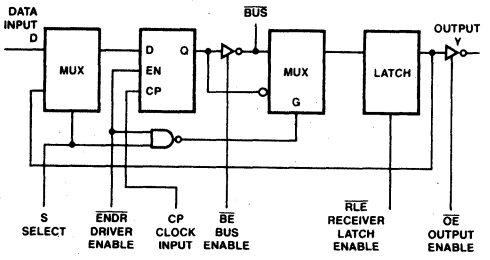
The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, $\overline{ENREC}$, which functions as a common clock enable.

Data from each D input is inverted at the bus output. Likewise, data at the bus input is inverted at the receiver output.

All three-state controls and enable lines are active low (the Am2927 receiver latch is transparent when $\overline{RLE}$ is LOW). The select input, S, determines whether the enabled driver input accepts data from the data input, D, or from the corresponding receiver output, Y. Similarly, the select line determines whether the receiver accepts input data from the data bus, or the driver output.

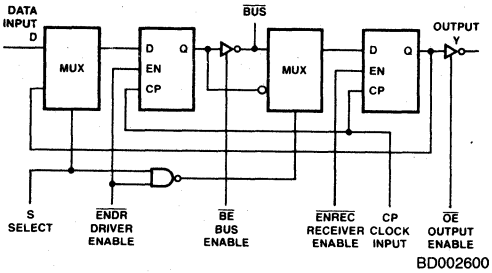
BLOCK DIAGRAM

Am2927



BD002610

Am2928



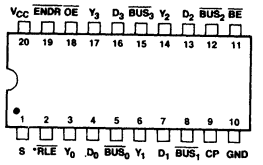
BD002600

01032B

Refer to Page 13-1 for Essential Information on Military Devices

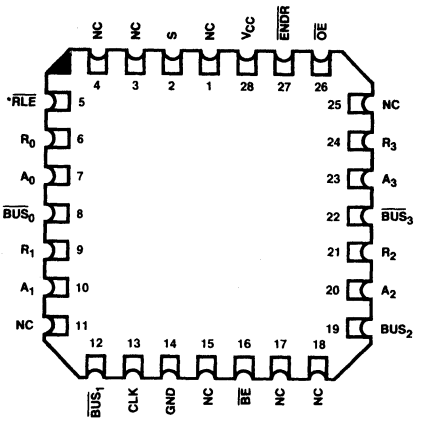
CONNECTION DIAGRAM
Top View

D-20-1



CD004831

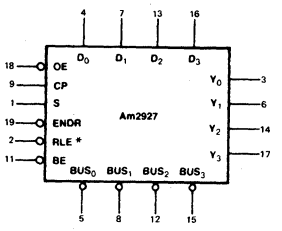
L-28-1



CD005060

Note: Pin 1 is marked for orientation
*ENREC for Am2928

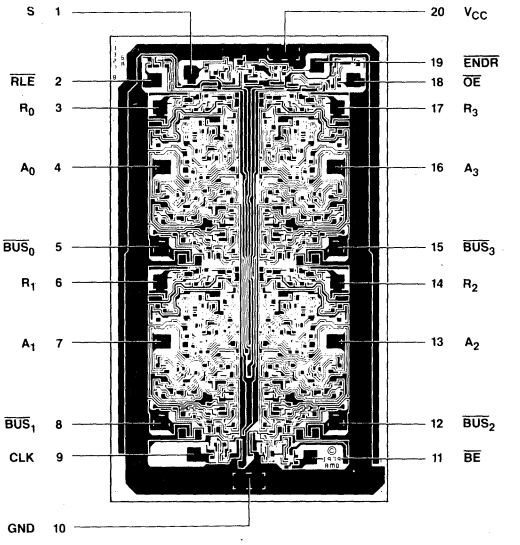
LOGIC SYMBOL



LS001101

*ENREC for Am2928

METALLIZATION AND PAD LAYOUT
Am2927*



DIE SIZE 0.087" x 0.144"

NOTE: The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, ENREC, which functions as a common clock enable.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2927/2928 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - L – 28-pin leadless chip carrier
  - X – Dice
- **Am2927/2928** — Device type
  - Quad 3-state Bus Transceivers

Valid Combinations	
Am2927 Am2928	DC, DM LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
9	CP	I	Clock Pulse to internal registers enters data on the LOW-to-HIGH transition.
11	$\overline{BE}$	I	Bus Enable. When Bus Enable is LOW the four drivers drive the $\overline{BUS}$ outputs.
5, 8, 12, 15	$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$	I/O	The four driver outputs and receiver inputs.
4, 7, 13, 16	D_0, D_1, D_2, D_3	I	The four driver data inputs inverting from D to $\overline{BUS}$.
3, 6, 14, 17	Y_0, Y_1, Y_2, Y_3,	O	The four receiver data outputs inverting from $\overline{BUS}$ to Y.
1	S	I	Select input controls data path modes in conjunction with $\overline{ENDR}$ and $\overline{RLE}$ (or $\overline{ENREC}$).
18	$\overline{OE}$	I	Output Enable. When Output Enable is LOW the four receiver outputs Y are active.
19	$\overline{ENDR}$	I	Driver Enable. Common clock enable for the input register. Allows the data on the D inputs to be loaded into the driver register on the clock LOW-to-High transition.
2	$\overline{RLE}$	I	Receiver Latch Enable (Am2927 only). When Receiver Latch Enable is LOW, the four receiver latches are transparent.The latches hold received data when $\overline{RLE}$ is HIGH.
2	$\overline{ENREC}$	I	Receiver Enable (Am2928 only). Common clock enable for the receiver register. Allows the $\overline{BUS}$ driver or previous receiver data to enter the receiver register on the rising edge of the clock.

Am2927 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	$\overline{RLE}$	Driver Register
H	X	X	Hold Previous Data
L	L	X	Load from D Input
L	H	L	Load from $\overline{BUS}$
L	H	H	Load Latched Receiver Data

Receiver Latch Control

$\overline{ENDR}$	S	$\overline{RLE}$	Receiver Output
X	X	H	Data Latched
H	H	L	Driver Register Output at Y output (Latch Transparent)
X	L	L	Bus Data at Y Output (Latch Transparent)
L	X	L	

Am2928 FUNCTION TABLES

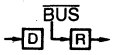
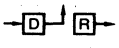
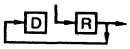
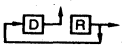
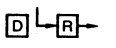
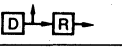
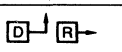
Driver Register Control

$\overline{ENDR}$	S	Driver Register
H	X	Hold Previous Data
L	L	Load from D input
L	H	Load from Receiver Register

Receiver Register Control

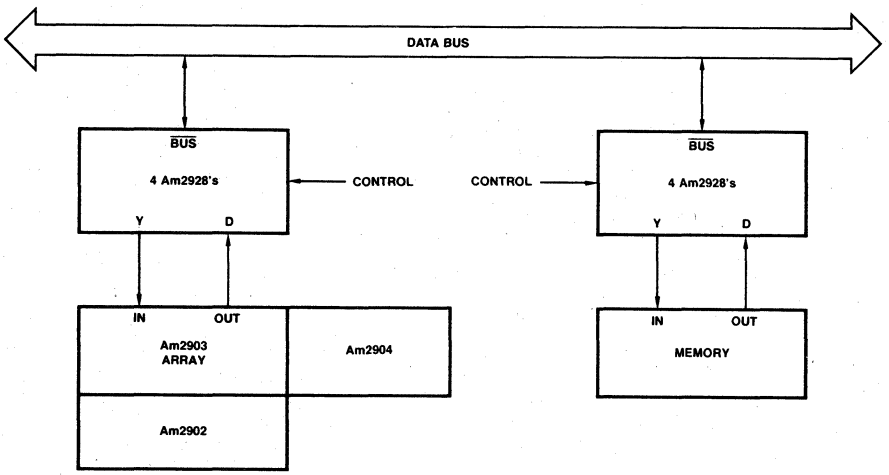
$\overline{ENDR}$	S	$\overline{ENREC}$	Receiver Output
X	X	H	Hold Previous Data
H	H	L	Load from Driver Register
X	L	L	Load from $\overline{BUS}$
L	X	L	

Am2927 AND Am2928 FUNCTION TABLE

Driver Input From	Receiver Input From	Control Input Condition			Signal Flow	$\overline{BE}$
		S	$\overline{ENDR}$	*		
D Input	BUS	L	L	L		H
	(No Load)	L	L	H		L
Receiver	BUS	H	L	L		H
	(No Load)	H	L	H		L
(No Load)	BUS	L	H	L		H
	Driver	H	H	L		X
	(No Load)	X	H	H		L

*$\overline{RLE}$ for Am2917 (asynchronous) or $\overline{ENREC}$ for Am2928 (⌋⌈).

APPLICATION



AF001800

The Am2927 and Am2928 can be used to provide Data Bus, Address Bus and Control Bus Interface in a high-speed bipolar microprocessor system.

01032B

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Output Current, Into Bus 100mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.4		
		V_{CC} = 5.0V	I_{OH} = −100μA	3.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 24mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	S, $\overline{ENDR}$			−2.8	mA
			All other inputs			−1.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	S, $\overline{ENDR}$			100	μA
			All other inputs			50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Off-State Output Current (Receiver Output)	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX	Receiver	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2927		150	185	mA
			Am2928		153	190	

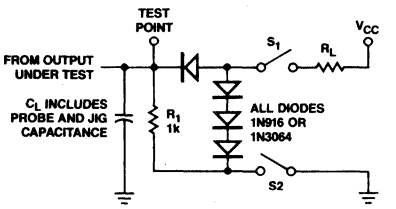
Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA	2.4			
V_{IH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus Enable = 2.4V				0.8	Volts
I_{OFF}	Bus Leakage Current (Power Off)	V_{CC} = 0V, V_O = 4.5V				100	μA
I_{OZL}	Bus Leakage Current (High-Impedance)	V_{CC} = MAX, BUS Enable = 2.4V	V_O = 0.4V			−1.4	mA
I_{OZH}			V_O = 2.5V			100	μA
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50		−255	mA
C_S	Bus Capacitance (Note 4)	V_{CC} = 0V			8		pF

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

SWITCHING TEST CIRCUIT



TC001470

Note: For standard totem-pole outputs, remove R_1; S_1 and S_2 closed.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified Am2927

Parameters	Description	Test Conditions (Note 2)	COMMERCIAL Am2927 Min	COMMERCIAL Am2927 Typ	COMMERCIAL Am2927 Max	MILITARY Am2927 Min	MILITARY Am2927 Typ	MILITARY Am2927 Max	Units
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L(BUS) = 130Ω		18	26		18	23	ns
t_{PHL}				18	26		18	23	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	26		14	23	ns
t_{HZ} • t_{LZ}		R_L = 130Ω, C_L = 5pF		12	18/30		12	16/23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18			15			ns
t_{PLH}	$\overline{BUS}$ to Receiver Output (Latch Enabled)	C_L = 50pF, R_L = 270Ω			23		16	20	ns
t_{PHL}					23		16	20	
t_{PLH}	Latch Enable, $\overline{RLE}$, to Receiver Output				26		18	23	ns
t_{PHL}					26		18	23	
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Output				23			21	ns
t_{HZ} • t_{LZ}		C_L = 5pF, R_L = 270Ω			21		14	18	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		10			9			ns
t_h			3			3			
t_s	Select S, to Clock ($\overline{RLE}$ = HIGH)		18			15			ns
t_h			3			2			
t_{PLH}	Select S, to Receiver Output	C_L = 50pF, R_L = 270Ω			26			23	ns
t_{PHL}					35			30	
t_s	Data Inputs D, to Clock		9			7			ns
t_h			5			4			
t_s	$\overline{BUS}$ to Latch Enable, $\overline{RLE}$		11			10			ns
t_h			4			3			

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2928

Parameters	Description	Test Conditions (Note 2)	COMMERCIAL Am2928 Min	COMMERCIAL Am2928 Typ (Note 1)	COMMERCIAL Am2928 Max	MILITARY Am2928 Min	MILITARY Am2928 Typ (Note 1)	MILITARY Am2928 Max	Units
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF		18	23			26	ns
t_{PHL}		R_L(BUS) = 130Ω		18	23			26	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	23			26	ns
t_{HZ} • t_{LZ}		R_L = 130Ω, C_L = 5pF		12	16/23			18/30	
t_{PLH}	Clock, CP, to Receiver Output	C_L = 50pF R_L = 270Ω		18	23			26	ns
t_{PHL}				18	23			26	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		15			18			ns
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Output			14	21			23	ns
t_{HZ} • t_{LZ}		C_L = 5pF, R_L = 270Ω		21	18			26	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		9			10			ns
t_h			3			3			
t_s	$\overline{BUS}$ to Clock (Receiver Register)		7			8			ns
t_h			4			5			
t_s	Receiver Enable, $\overline{ENMREC}$, to Clock		8			10			ns
t_h			4			5			
t_s	S to Clock		10			12			ns
t_h			4			5			
t_s	Data Inputs, D, to Clock (Driver Register)		7			9			ns
t_h			4			5			

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2930

Program Control Unit

DISTINCTIVE CHARACTERISTICS

- **Powerful, 4-bit slice address controller for memories**
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- **Executes 32 instructions**
  Capable of executing branch and subroutine call and return
- **Twelve different relative address instructions**
  Including JUMP-TO-SUBROUTINE relative and RETURN-FROM-SUBROUTINE relative
- **Built-in condition code input**
  Sixteen instructions are dependent on external condition control
- **Seventeen-level push/pop stack**
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- **Separate incrementer for program counter**
  A relative address may be computed and PC may be incremented by one on a single cycle

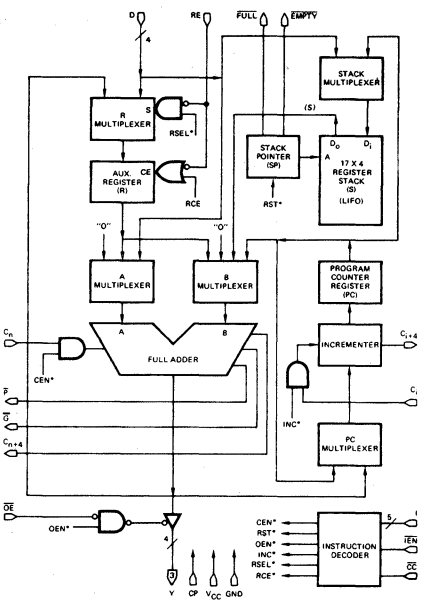
GENERAL DESCRIPTION

The Am2930 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2930's may be interconnected to generate a 16-bit address (64K words). The Am2930 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2930 performs five types of instructions. These are: 1) Unconditional Fetch; 2) Conditional Jump; 3) Conditional Jump-to-Subroutine; 4) Conditional Return-from-Subroutine; and 5) Miscellaneous Instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0–Y_3). These are: 1) the Program Counter (PC); 2) the Stack (S); 3) the auxiliary Register (R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0–I_4), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register. A condition code input is provided for conditional instructions.

BLOCK DIAGRAM



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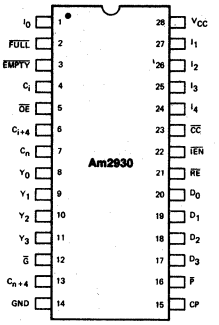
Refer to Page 13-1 for Essential Information on Military Devices

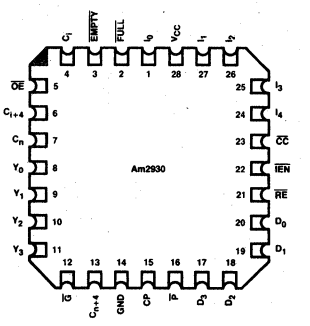
CONNECTION DIAGRAM
Top View

D-28
F-28*



CD004350

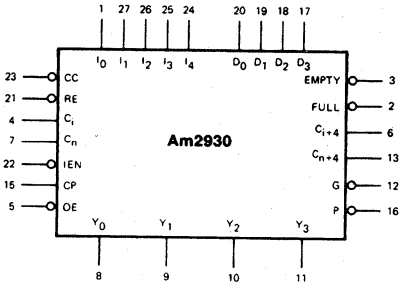
Chip-Pak™
L-28-1



CD004730

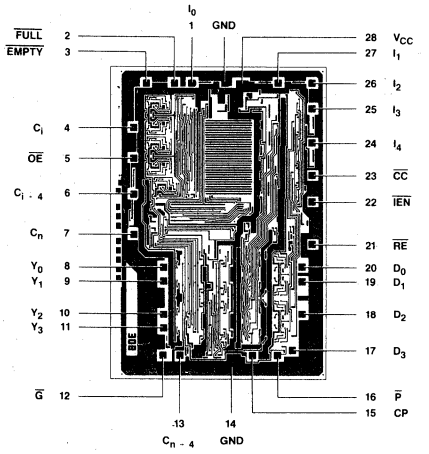
*F-28 pin configuration identical to D-28.
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS001050

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.133" x 0.200"
Pad numbers correspond to DIP pinout

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2930 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 28-pin CERDIP
  - F – 28-pin flatpak
  - L – 28-pin leadless chip carrier
  - X – Dice
- **Am2930** — Device type
  - Program Control Unit

Valid Combinations	
Am2930	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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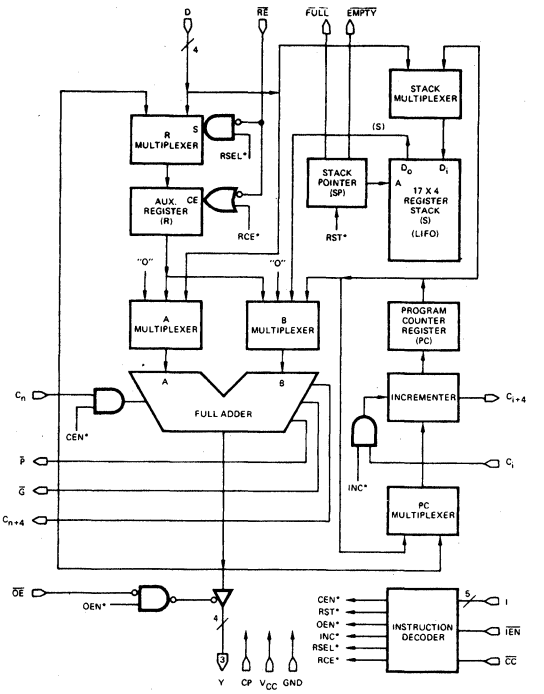
PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_{0-4}		The five Instruction control lines to the Am2930, used to establish data paths and enable internal registers.
22	$\overline{IEN}$	I	The Instruction Enable Input, used to enable and disable internal registers. When $\overline{IEN}$ is LOW, all internal registers are under control of the Instruction inputs. When $\overline{IEN}$ is HIGH, all internal registers except R are inhibited from changing state. R is controlled by the $\overline{RE}$ input. The $\overline{IEN}$ input does not affect the combinatorial data paths and the outputs established by the Instruction inputs.
23	$\overline{CC}$	I	The Condition Code input determines whether or not a conditional instruction (Instructions 16-31) is performed. If $\overline{CC}$ is LOW, the conditional instruction is executed. If $\overline{CC}$ is HIGH, Fetch PC (Instruction 1) is executed. The $\overline{CC}$ input may be either HIGH or LOW for unconditional instructions (Instructions 0-15).
21	$\overline{RE}$	I	The Register Enable input for the Auxiliary Register (R). A LOW on $\overline{RE}$ causes the Auxiliary Register (R) to be loaded from the D inputs unless Instruction 8 or 9 is being executed and $\overline{IEN}$ is LOW.
7	C_n	I	The carry-in to the Full Adder.
13	Cn + 4	O	The carry-out of the Full Adder.
16,12	$\overline{P}$, $\overline{G}$	O	The carry generate and propagate outputs of the Full Adder.
4	C_i	I	The carry-in to the program counter incrementer.
6	C_{i+4}	O	The carry-out of the program counter incrementer.
	Y_{0-3}	O	The four address outputs of the Am2930. These are three-state output lines. When enabled, they display the outputs of the Full Adder.
5	$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high-impedance); when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).
	D_{0-3}	I	The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.
3	$\overline{Empty}$	O	The Empty output is LOW when the Stack is empty.
2	$\overline{Full}$	O	The Full output is LOW when the LIFO stack is full – during and after the 17th push operation.
15	CP	I	The clock input to the Am2930. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

BLOCK DIAGRAM



BD002230

***INTERNAL**

ARCHITECTURE OF THE Am2930

The Am2930 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1. A full adder with input multiplexers
2. A Program Counter Register with an incrementer and an input multiplexer
3. A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4. An auxiliary register with an input multiplexer
5. An instruction decoder
6. Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition and provision is made for further lookahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During three instructions (unconditional Hold and conditional Hold and Suspend when the $\overline{CC}$ input is LOW), the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer if the $\overline{CC}$ input is LOW. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+ 1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Empty output ($\overline{EMPTY}$) is LOW when the stack is empty (after the Reset instruction and after the last word has been Popped from the stack); the active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Register Enable input ($\overline{RE}$) is LOW or if the Instruction inputs call for it to be loaded. When $\overline{RE}$ is LOW, R is loaded from the D inputs unless the Instruction dictates that R be loaded from the output of the Full Adder.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

For unconditional instructions, the $\overline{CC}$ input is not utilized; it may be either HIGH or LOW. For conditional instructions, if $\overline{CC}$ is LOW, the condition is met and the conditional operation is performed; if $\overline{CC}$ is HIGH, a Fetch PC is performed.

Output Buffers

The Address outputs (Y_0–Y_3) are three-state drivers which may be disabled either under Instruction control or by a HIGH on the Output Enable input ($\overline{OE}$). Disabling the Y outputs does not affect the execution of instructions inside the Am2930.

Instruction Enable

When HIGH, the Instruction Enable input ($\overline{IEN}$) forces PC and SP into the hold mode and disables the write circuitry to the RAM. The auxiliary register (R) is under control of the $\overline{RE}$ input when $\overline{IEN}$ is HIGH, independent of the state of the Instruction inputs. The $\overline{IEN}$ input does not affect the combinatorial data paths or Y outputs in the Am2930. The data paths are selected by the Instruction and $\overline{CC}$ inputs and are not affected by $\overline{IEN}$.

Am2930 INSTRUCTION SET

The Am2930 Instruction set can be divided into five types of instructions. These are:

- Unconditional Fetches
- Conditional Jumps
- Conditional Jumps-to-Subroutine
- Conditional Returns-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Unconditional Fetches

As can be seen from Table 1, there are nine unconditional Fetch instructions (Instructions 1–9). Under control of the Instruction inputs, the desired value is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instructions 1 through 7, the auxiliary register is under control of the RE input. For Instructions 8 and 9, R is loaded with PC and R + D, respectively. The RAM and Stack Pointer are not changed during a Fetch instruction.

Conditional Jumps

There are six conditional Jump instructions (Instructions 16 through 21). Under control of the Instruction inputs, the desired value is placed at the Y outputs. Additionally, the value is incremented if C_i of the least significant device is HIGH and loaded into PC. During these instructions, R is controlled by $\overline{RE}$. The RAM and Stack Pointer are not changed during these instructions. The above operations are performed if the $\overline{CC}$ input is LOW; if $\overline{CC}$ is HIGH, a Fetch PC operation is performed.

Conditional Jumps-to-Subroutine

There are six conditional Jump-to-Subroutine instructions (Instructions 22 through 27). Under control of the Instruction inputs, the desired value is placed on the Y outputs. On the rising edge of the clock the value is incremented* and loaded into PC; PC is loaded into the RAM at location SP + 1, and SP is incremented.

As with Conditional Jump Instructions, R is controlled by $\overline{RE}$ and whether the Jump-to-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Conditional Returns-from-Subroutine

There are two conditional Return-from-Subroutine instructions (Instructions 28 and 29). Under control of the instruction inputs, either S or S + D is placed at the Y outputs. Additionally, the selected value is incremented* and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

*If C_i of the least significant device is HIGH.

As with the Condition Jump and Jump-to-Subroutine Instructions, R is controlled by $\overline{RE}$ and whether the Return-from-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM is unchanged and R is controlled by $\overline{RE}$.

Load R (Instruction 10)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 11)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 12)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 13)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is controlled by $\overline{RE}$.

Pop PC (Instruction 14)

This instruction is the same as Fetch PC except SP is decremented at the end of the cycle, causing the data at the top of the stack to be lost.

Hold (Instruction 15)

This instruction places PC at the Y outputs and inhibits any change in PC, SP, and RAM. R is controlled by $\overline{RE}$.

Conditional Hold (Instruction 30)

This instruction is the same as Hold except $\overline{CC}$ must be LOW. If $\overline{CC}$ is HIGH, the Fetch PC instruction is performed.

Suspend (Instruction 31)

The Suspend instruction is the same as the Conditional Hold instruction except the Y outputs are forced into the high-impedance state if $\overline{CC}$ is LOW.

TABLE I – Am2930 INSTRUCTION SET

Mnemonic	Instruction Number	I_4	I_3	I_2	I_1	I_0	$\overline{CC}$	$\overline{IEN}$	Instruction	Y_0-Y_3	Next State (after CP ↓) (Note 3) PC	R $\overline{RE}$ = L	R $\overline{RE}$ = H	RAM	SP
		X	X	X	X	X	X	H	Instruction Disable	Note 1	–	D	–	–	–
PRST	0	L	L	L	L	L	X	L	RESET	"0"	"0" + C_i	D	–	–	Reset
FPC	1	L	L	L	L	H	X	L	FETCH PC	PC	PC + C_i	D	–	–	–
FR	2	L	L	L	H	L	X	L	FETCH R	R	PC + C_i	D	–	–	–
FD	3	L	L	L	H	H	X	L	FETCH D	D	PC + C_i	D	–	–	–
FRD	4	L	L	H	L	L	X	L	FETCH R + D	P + D + C_n	PC + C_i	D	–	–	–
FPD	5	L	L	H	L	H	X	L	FETCH PC + D	PC + D + C_n	PC + C_i	D	–	–	–
FPR	6	L	L	H	H	L	X	L	FETCH PC + R	PC + R + C_n	PC + C_i	D	–	–	–
FSD	7	L	L	H	H	H	X	L	FETCH S + D	S + D + C_n	PC + C_i	D	–	–	–
FPLR	8	L	H	L	L	L	X	L	FETCH PC → R	PC	PC + C_i	PC	PC	–	–
FRDR	9	L	H	L	L	H	X	L	FETCH R + D → R	R + D + C_n	PC + C_i	R + D + C_n	R + D + C_n	–	–
PLDR	10	L	H	L	H	L	X	L	LOAD R	PC	PC + C_i	D	D	–	–
PSHP	11	L	H	L	H	H	X	L	PUSH PC	PC	PC + C_i	D	–	PC→Loc SP + 1	SP + 1
PSHD	12	L	H	H	L	L	X	L	PUSH D	PC	PC + C_i	D	–	D→Loc SP + 1	SP + 1
POPS	13	L	H	H	L	H	X	L	POP S	S	PC+ C_i	D	–	–	SP–1
POPP	14	L	H	H	H	L	X	L	POP PC	PC	PC + C_i	D	–	–	SP–1
PHLD	15	L	H	H	H	H	X	L	HOLD	PC	–	D	–	–	–
	16-31	H	X	X	X	X	H	L	FAIL COND'L TEST (FETCH PC)	PC	PC + C_i	D	–	–	–
JMPR	16	H	L	L	L	L	L	L	JUMP R	R	R + C_i	D	–	–	–
JMPD	17	H	L	L	L	H	L	L	JUMP D	D	D + C_i	D	–	–	–
JMPZ	18	H	L	L	H	L	L	L	JUMP "O"	"O"	"O" + C_i	D	–	–	–
JPRD	19	H	L	L	H	H	L	L	JUMP R + D	R + D + C_n	R + D + C_n + C_i	D	–	–	–
JPPD	20	H	L	H	L	L	L	L	JUMP PC + D	PC + D + C_n	PC + D + C_n + C_i	D	–	–	–
JPPR	21	H	L	H	L	H	L	L	JUMP PC + R	PC + R + C_n	PC + R + C_n + C_i	D	–	–	–
JSBR	22	H	L	H	H	L	L	L	JSB R	R	R + C_i	D	–	PC→Loc SP + 1	SP + 1
JSBD	23	H	L	H	H	H	L	L	JSB D	D	D + C_i	D	–	PC→Loc SP + 1	SP + 1
JSBZ	24	H	H	L	L	L	L	L	JSB "O"	"O"	"O" + C_i	D	–	PC→Loc SP + 1	SP + 1
JSRD	25	H	H	L	L	H	L	L	JSB R + D	R + D + C_n	R + D + C_n + C_i	D	–	PC→Loc SP + 1	SP + 1
JSPD	26	H	H	L	H	L	L	L	JSB PC + D	PC + D + C_n	PC + D + C_n + C_i	D	–	PC→Loc SP + 1	SP + 3
JSPR	27	H	H	L	H	H	L	L	JSB PC + R	PC + R + C_n	PC + R + C_n + C_i	D	–	PC→Loc SP + 1	SP + 1
RTS	28	H	H	H	L	L	L	L	RETURN S	S	S + C_i	D	–	–	SP–1
RTSD	29	H	H	H	L	H	L	L	RETURN S + D	S + D + C_n	S + D + C_n + C_i	D	–	–	SP–1
CHLD	30	H	H	H	H	L	L	L	HOLD	PC	–	D	–	–	–
PSUS	31	H	H	H	H	H	L	L	SUSPEND	Z (Note 2)	–	D	–	–	–

PC – Program Counter
R – Auxiliary Register
SP – Stack Pointer
D – Direct Inputs
S – Stack Top

Notes: 1. When $\overline{IEN}$ is HIGH, the Y_0–Y_3 outputs contain the same data as when $\overline{IEN}$ is LOW, as determined by I_0–I_4 and $\overline{CC}$.
2. Z = High impedance state (outputs "OFF").
3. – = No change.

APPLICATIONS

The Am2930 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2930 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901's via a 16-bit register.

The Address outputs (Y) of the Am2930 are loaded into a 16-bit Memory Address Register (MAR). Although the MAR is shown as part of the CPU, in some applications it may be part of the memory.

An Am2902 High-Speed Lookahead Carry Generator is utilized to provide high-speed relative and indexed addressing. In slower systems, the C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The Condition Code input ($\overline{CC}$) is derived from the same condition code multiplexer which generates the condition code input for the microprogram sequencer.

The control inputs of the Am2930 (I_{0-4}, $\overline{IEN}$, $\overline{RE}$, $\overline{OE}$, and C_i and C_n of the least significant device) are shown originating at the Pipeline Register. Although it is not shown in Figure 1, it is possible to share the Pipeline Register outputs which go to these pins with another device. This can be accomplished if both the Am2930 and the other device do not operate on the same microcycle. Forcing the $\overline{IEN}$ input HIGH inhibits any changes in the Am2930 internal registers, independent of the state of these seven inputs. This allows the Am2930 to be placed in a hold mode while the other device is using the same Pipeline Register outputs as control signals.

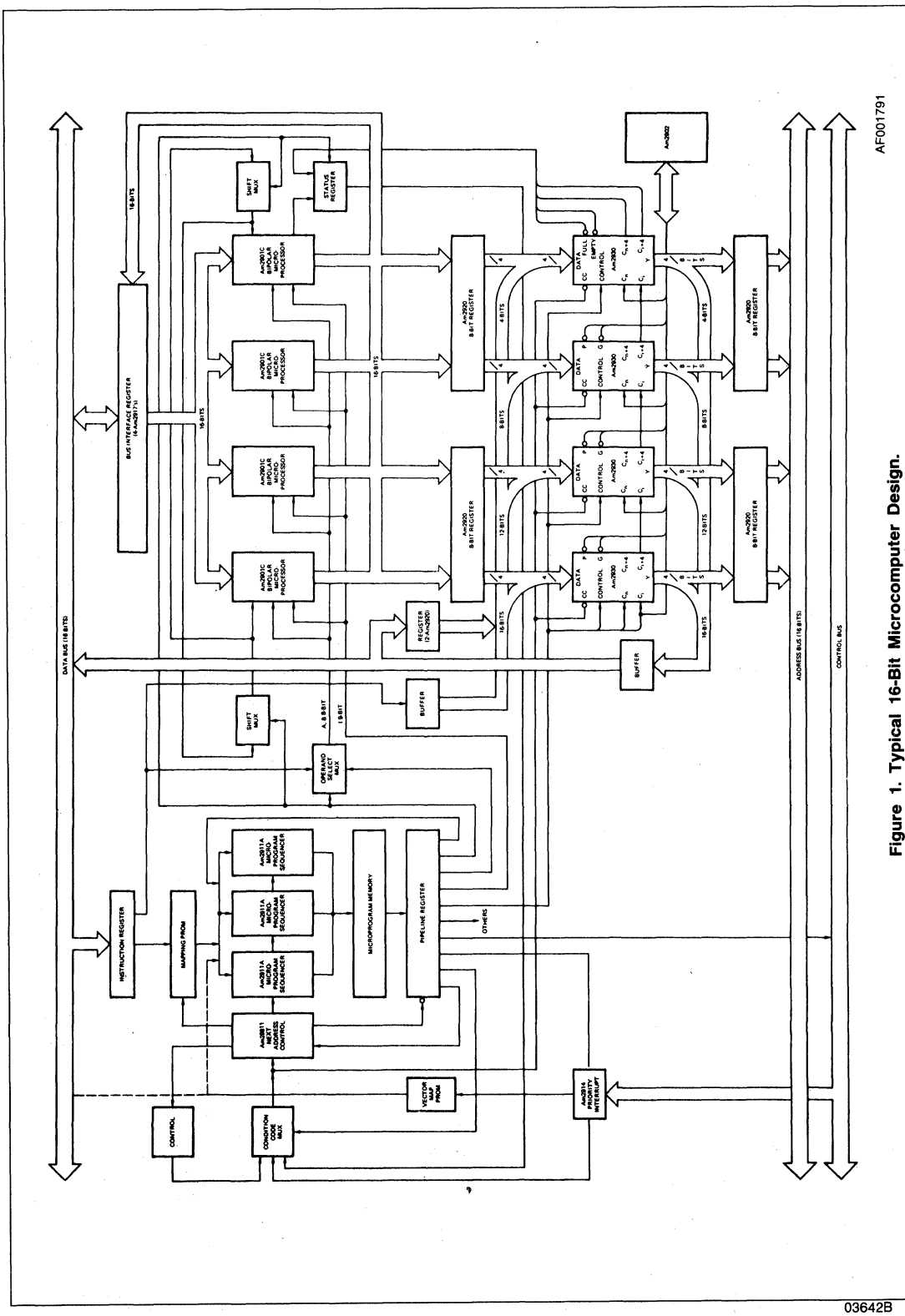


Figure 1. Typical 16-Bit Microcomputer Design.

03642B

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

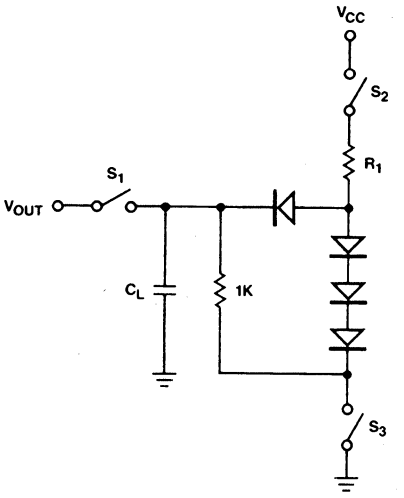
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	$\overline{Y_0}$, Y_1, Y_2, Y_3 $\overline{G}$, C_{n+4} C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, C_{n+4} C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{P}$, $\overline{FULL}$ $\overline{EMPTY}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				−.702	
			$\overline{CC}$				−.657	
			C_i				−2.31	
			C_n				−3.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX		T_C = −55 to +125°C			239	mA
				T_C = +125°C			170	
				T_A = 0 to 70°C			220	
				T_A = 70°C			185	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

SWITCHING TEST CIRCUIT

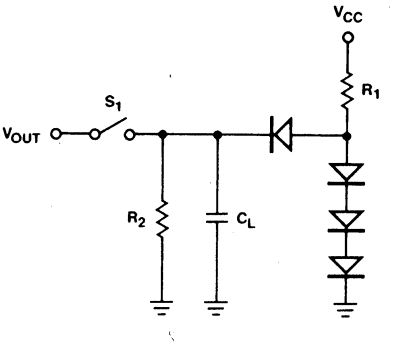
A. THREE STATE OUTPUTS



TCR01350

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



TCR01370

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L – 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2930

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
3	$\overline{EMPTY}$	B	300	2K
6	C_{i+4}	B	240	1.5K
8–11	Y_{0-3}	A	240	1K
12	$\overline{G}$	B	240	1.5K
13	C_{n+4}	B	240	1.5K
16	P	B	300	2K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Am2930 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2930. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. GUARANTEED PERFORMANCE OVER COMMERCIAL OPERATING RANGE

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	27	26
$\overline{CC}$ (Note 1)	Y	55	37
I_{4-0} (Note 1)	Y	80	55

Note 1: "Suspend" instruction.

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

	To Output						
From Input	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4 = L	C_{i+4} I_4 = H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	81	67	77	80	91	69	–
$\overline{CC}$	63	45	55	–	72	42	–
C_n	32	–	25	–	45	–	–
C_i	–	–	–	22	22	–	–
CP	69	53	61	43	78	55	55
D	49	33	40	–	59	–	–
$\overline{IEN}$	–	–	–	–	–	40	–

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	114	0
$\overline{CC}$	75	0
$\overline{IEN}$	55	0
C_n	43	0
C_i	32	5
D ($\overline{RE}$ = L I_{4-0} = 0-8 or 10-15)	25	2
$\overline{RE}$	24	4

II. GUARANTEED PERFORMANCE OVER MILITARY OPERATING RANGE

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	32	31
$\overline{CC}$ (Note 1)	Y	60	42
I_{4-0} (Note 1)	Y	85	60

Note 1: "Suspend" instruction.

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

	To Output						
From Input	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4 = L	C_{i+4} I_4 = H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	88	74	82	87	97	78	–
$\overline{CC}$	68	52	60	–	78	47	–
C_n	37	–	30	–	46	–	–
C_i	–	–	–	23	23	–	–
CP	74	58	66	48	84	60	60
D	55	38	45	–	65	–	–
$\overline{IEN}$	–	–	–	–	–	45	–

TABLE IID
Setup and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
I_{4-0}	124	0
$\overline{CC}$	80	0
$\overline{IEN}$	69	0
C_n	52	0
C_i	37	5
D ($\overline{RE}$ = L I_{4-0} = 0-8 or 10-15)	30	2
D (All other conditions)	72	2
$\overline{RE}$	29	4

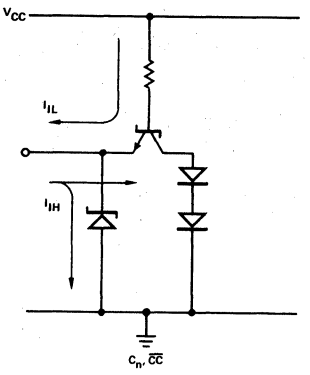
Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–3ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

Driven Inputs



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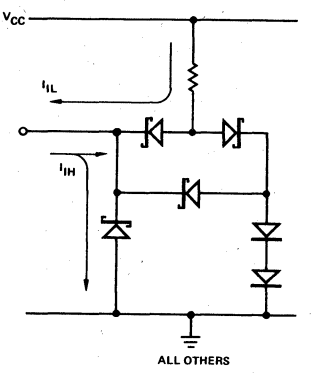
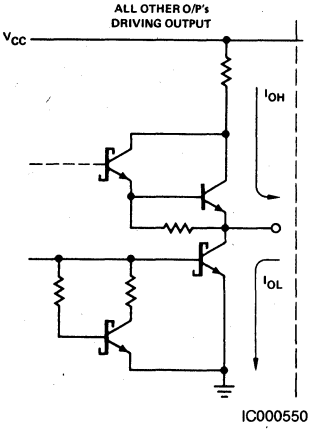


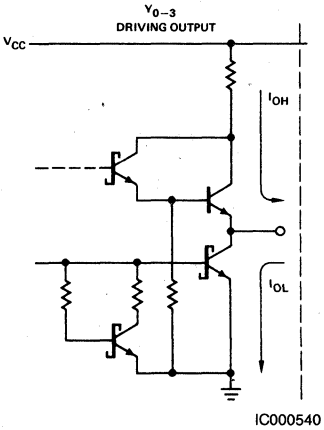
IC000560

Note: C_i input is connected to both configurations in parallel.

Driving Outputs



IC000550



IC000540

Note: Actual current flow direction shown.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2920	8-Bit Register
Am2922	Condition Code MUX

For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

Am2932

Program Control Unit/Push-Pop Stack

DISTINCTIVE CHARACTERISTICS

- **Powerful, 4-bit slice address controller for memories**
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- **Executes 16 instructions**
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- **Eight relative address instructions**
  Including Jump relative and Jump-to-Subroutine relative
- **Seventeen-level push/pop stack**
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- **Separate incrementer for program counter**
  A relative address may be computed and PC may be incremented by one on a single cycle

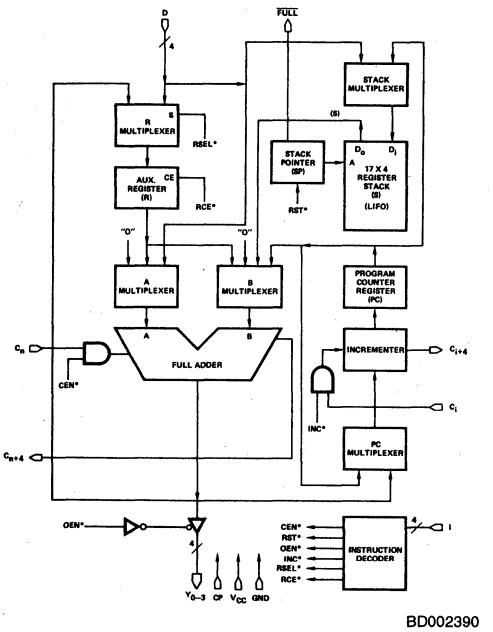
GENERAL DESCRIPTION

The Am2932 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2932s may be interconnected to generate a 16-bit address (64K words). The Am2932 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2932 performs five types of instructions. These are: 1. Fetch; 2. Jump; 3. Jump-to-Subroutine; 4. Return-from-Subroutine; and 5. Miscellaneous Instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1. the Program Counter (PC); 2. the Stack (S); 3. the auxiliary Register (R); and 4. the Direct inputs (D). Under control of the Instruction inputs (I_0-I_3), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register.

BLOCK DIAGRAM



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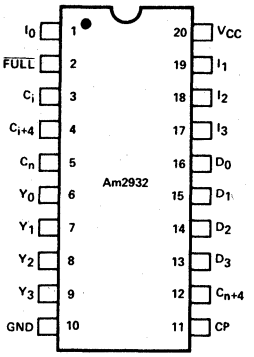
Refer to Page 13-1 for Essential Information on Military Devices

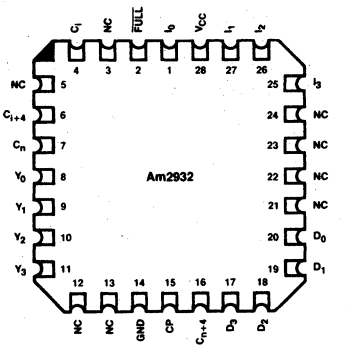
CONNECTION DIAGRAM
Top View

D-20



CD004510

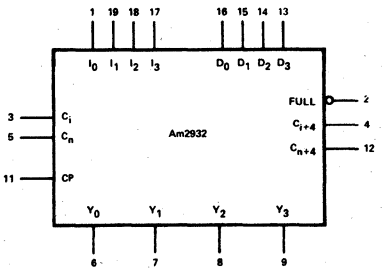
Chip-Pak™ L-28-1



CD004520

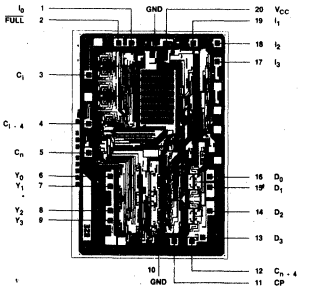
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
(DIP)



LS000950

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.134" x 0.200"

Pad numbers correspond to DIP pinout.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2932 D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 20-pin CERDIP; L– 28-pin leadless chip carrier; X– Dice
- Am2932 — Device type: Program Control Unit

Valid Combinations	
Am2932	DC, DCB, DMB LC, LMB XC, XM

Valid Combinations

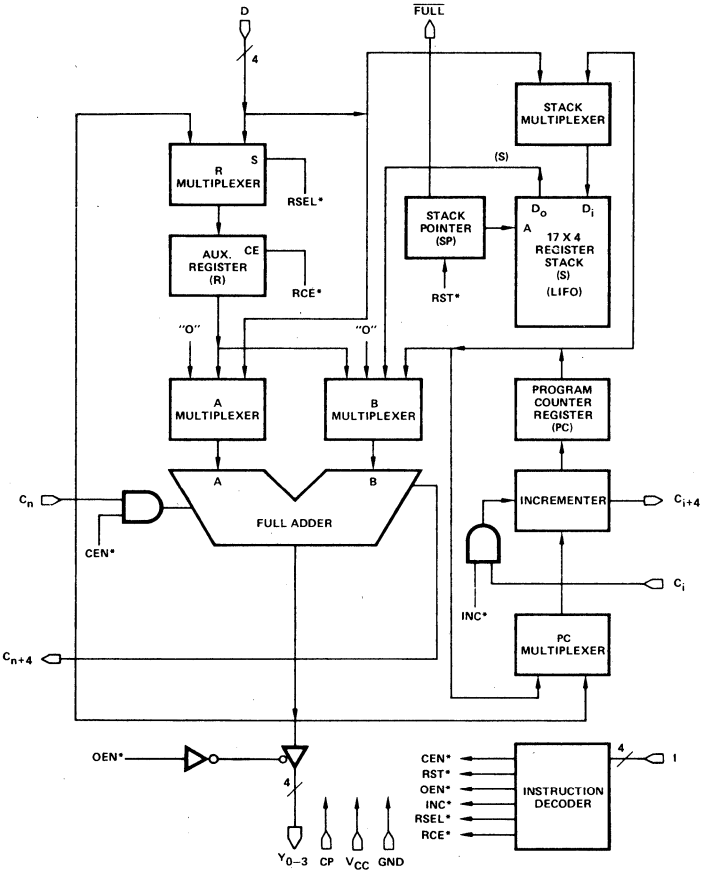
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_{0-3}	I	The four Instruction control lines to the Am2932, used to establish data paths and enable internal registers.
5	C_n	I	The carry-in to the Full Adder.
12	C_{n+4}	O	The carry-out of the Full Adder.
3	C_i	I	The carry-in to the program counter incrementer.
4	C_{i+4}	O	The carry-out of the program counter incrementer.
	Y_{0-3}	O	The four address outputs of the Am2932. These are three-state output lines. When enabled, they display the outputs of the Full Adder.
	D_{0-3}	I	The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.
2	$\overline{Full}$	O	The Full output is LOW when the LIFO stack is full - during and after the 17th push operation.
11	CP	I	The clock input to the Am2932. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

BLOCK DIAGRAM



BD002560

***INTERNAL**

ARCHITECTURE OF THE Am2932

The Am2932 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1. A full adder with input multiplexers
2. A Program Counter Register with an incrementer and an input multiplexer
3. A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4. An auxiliary register with an input multiplexer
5. An instruction decoder
6. Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition. The carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During the suspend instruction, the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP + 1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Instruction inputs call for it to be loaded.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled under Instruction control.

Am2932 INSTRUCTION SET

The Am2932 Instruction set can be divided into five types of instructions. These are:

- Fetches
- Jumps
- Jumps-to-Subroutine
- Return-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Fetches

As can be seen from Table I, there are four Fetch instructions (Instructions 4, 8, 9, 10). Under control of the Instructions inputs, the desired value is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instruction 10, R is loaded with PC. The RAM and Stack Pointer are not changed during a Fetch instruction.

Jumps

There are three Jump instructions (Instructions 5, 11, 12). Under control of the Instruction inputs, the desired value is placed at the Y outputs. Additionally, the value is incremented if C_i of the least significant device is HIGH and loaded into PC. The RAM, Stack Pointer and R are not changed during these instructions.

Jumps-to-Subroutine

There are two Jump-to-Subroutine instructions (Instructions 13 and 14). Under control of the Instruction inputs, the desired value is placed on the Y outputs. On the rising edge of the clock the value is incremented* and loaded into PC; PC is loaded into the RAM at location SP + 1; and SP is incremented.

During these instructions, R is not changed.

Return-from-Subroutine (Instruction 7)

Under control of the instruction inputs, S is placed at the Y outputs. Additionally, the value of S is incremented* and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock). During this instruction, R is not changed.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM and R are unchanged.

Load R (Instruction 15)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 6)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 2)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 3)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is not changed.

Suspend (Instruction 1)

The Suspend instruction inhibits any change in PC, SP, R and RAM and forces the Y outputs into the high impedance state.

TABLE I–Am2932 INSTRUCTION SET

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP ⎍) - Note 2			
								PC	R	RAM	SP
0	L	L	L	L	PRST	RESET	"0"	"0" + C_i	–	–	Reset
1	L	L	L	H	PSUS	SUSPEND	Z (Note 1)	–	–	–	–
2	L	L	H	L	PSHD	PUSH D	PC	PC + C_i	–	D→Loc SP + 1	SP + 1
3	L	L	H	H	POPS	POP S	S	PC + C_i	–	–	SP – 1
4	L	H	L	L	FPC	FETCH PC	PC	PC + C_i	–	–	–
5	L	H	L	H	JMPD	JUMP D	D	D + C_i	–	–	–
6	L	H	H	L	PSHP	PUSH PC	PC	PC + C_i	–	PC→Loc SP + 1	SP + 1
7	L	H	H	H	RTS	RETURN S	S	S + C_i	–	–	SP – 1
8	H	L	L	L	FR	FETCH R	R	PC + C_i	–	–	–
9	H	L	L	H	FPR	FETCH PC + R	PC + R + C_n	PC + C_i	–	–	–
10	H	L	H	L	FPLR	FETCH PC→R	PC	PC + C_i	PC	–	–
11	H	L	H	H	JMPR	JUMP R	R	R + C_i	–	–	–
12	H	H	L	L	JPPR	JUMP PC + R	PC + R + C_n	PC + R + C_n + C_i	–	–	–
13	H	H	L	H	JSBR	JSB R	R	R + C_i	–	PC→Loc SP + 1	SP + 1
14	H	H	H	L	JSPR	JSB PC + R	PC + R + C_n	PC + R + C_n + C_i	–	PC→Loc SP + 1	SP + 1
15	H	H	H	H	PLDR	LOAD R	PC	PC + C_i	D	–	–

Notes: 1. Z = High impedance state (outputs "OFF").
2. – = No change.

PC – Program Counter
R – Auxiliary Register
S – Stack Top
SP – Stack Pointer
D – Direct Inputs

*If C_i of the least significant device is HIGH.

APPLICATIONS

The Am2932 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2932 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901Cs via a 16-bit register.

The Address outputs (Y) of the Am2932 are passed to the address bus.

The C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The control inputs of the Am2932 ($I_{0\text{-}3}$, C_i and C_n of the least significant device) are shown originating at the Pipeline Register.

For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

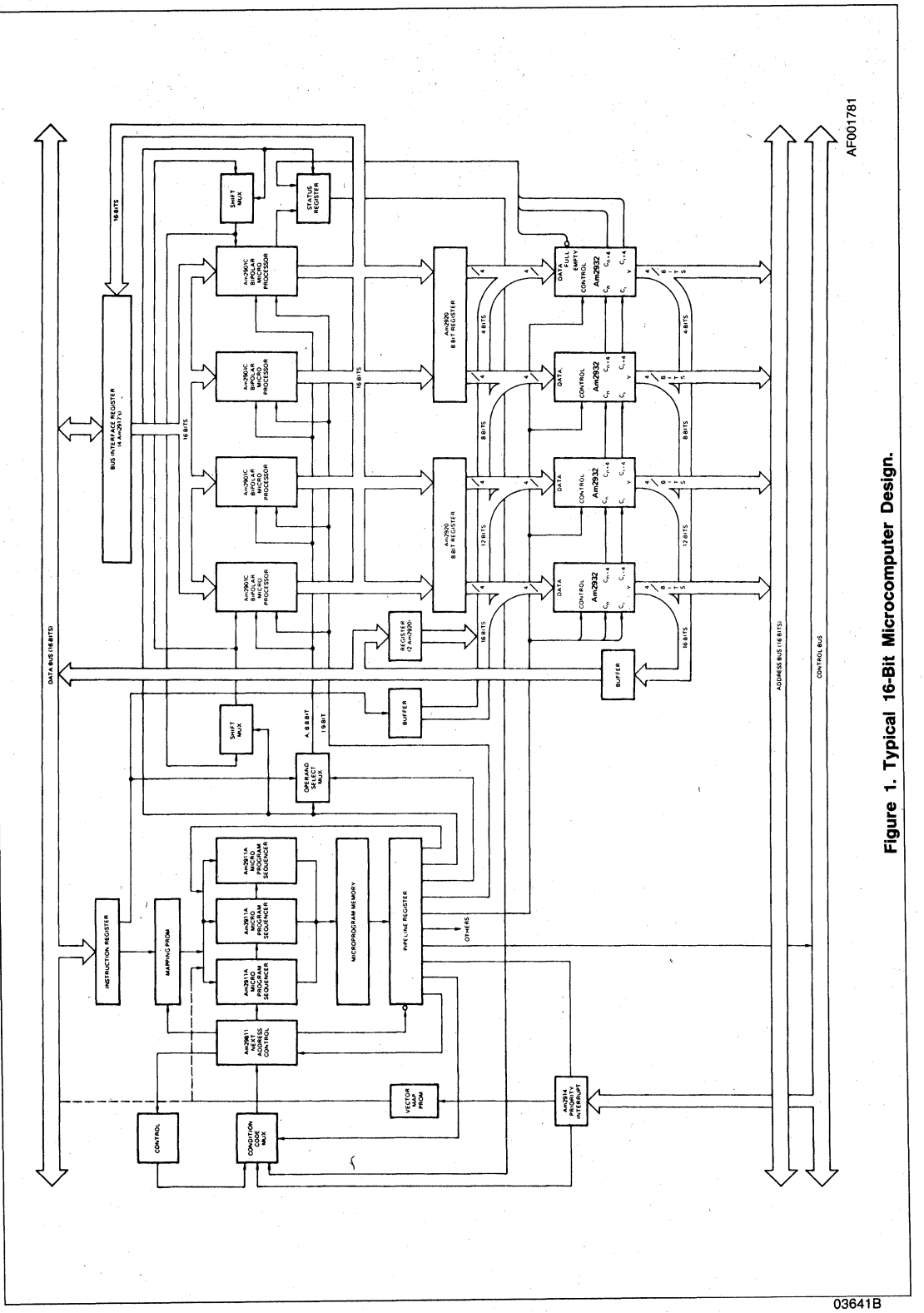


Figure 1. Typical 16-Bit Microcomputer Design.

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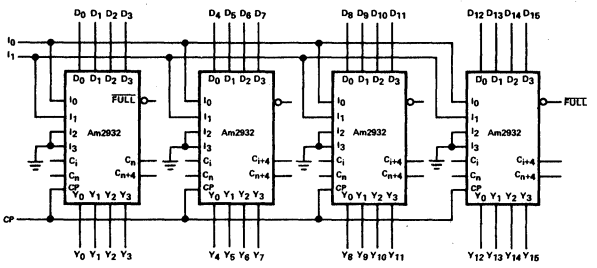
Refer to Page 13-1 for Essential Information on Military Devices



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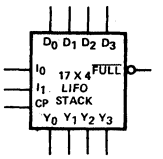
I_1	I_0	INSTRUCTION	Y OUTPUTS
L	L	RESET	"0"
L	H	SUSPEND	Z (HIGH IMPEDANCE)
H	L	PUSH D	SEE NOTE 1
H	H	POP S	TOP OF STACK



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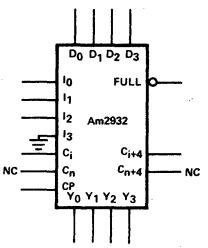
Equivalent Logic Symbol for AM2932 with I_2, I_3 Grounded

This figure shows the use of four Am2932s as a 17-word by 16-bit LIFO stack by grounding I_2 and I_3. The effect of grounding I_3 is shown in Figure 3.

Note 1. During this instruction, PC is placed on the Y outputs. If C_i is held LOW, the Y outputs will be LOW for this instruction after the device is initialized with a Reset instruction.

Figure 2. Application of Four Am2932s as a 17-Word by 16-Bit LIFO Stack.



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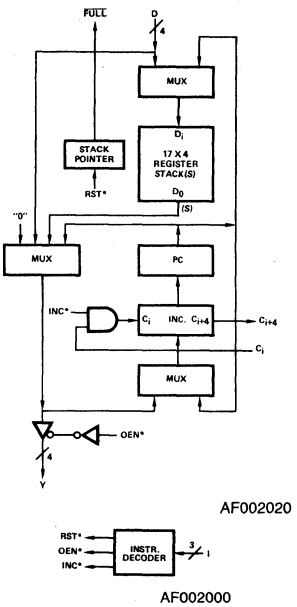
I_2	I_1	I_0	INSTRUCTION
L	L	L	RESET
L	L	H	SUSPEND
L	H	L	PUSH D
L	H	H	POP S
H	L	L	FETCH PC
H	L	H	JUMP D
H	H	L	PUSH PC
H	H	H	RETURN S



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AF002000

Figure 3. Equivalent Circuit of Am2932 with I_3 Grounded.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

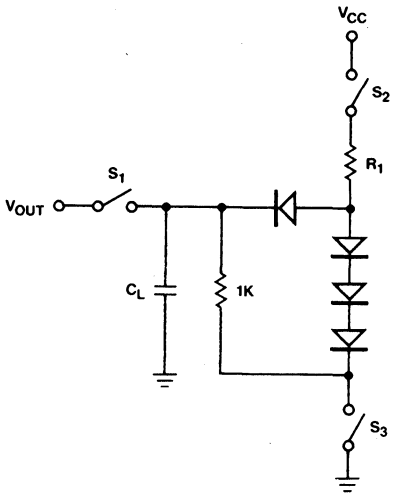
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 C_n+4 C_i+4	I_{OH} = −1.6mA	2.4			Volts
			$\overline{FULL}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			C_n+4, C_i+4	I_{OL} = 16mA			0.5	
			$\overline{FULL}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-3}			−.360	mA
				I_{0-3}, CP			−.702	
				C_i			−2.0	
				C_n			−3.69	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-3}			20	μA
				I_{0-3}, CP			40	
				C_i			90	
				C_n			250	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX		T_C = −55 to +125°C			210	mA
				T_C = +125°C			145	
				T_A = 0 to 70°C			190	
				T_A = 70°C			160	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

SWITCHING TEST CIRCUIT

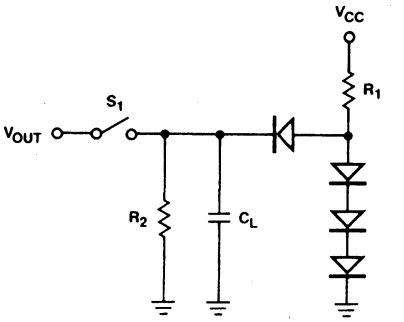
A. THREE STATE OUTPUTS



TCR01350

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TCR01370

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disabled tests.

TEST OUTPUT LOADS FOR Am2932

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
4	C_{i+4}	B	240	1.5K
6–9	Y_{0-3}	A	240	1K
12	C_{n+4}	B	240	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Am2932 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2932. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. GUARANTEED PERFORMANCE OVER COMMERCIAL OPERATING RANGE.

V_{CC} = 4.75 to 5.25V, T_A = 0 to +70°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	80	55

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

	To Output				
From Input	Y	C_{i+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	81	77	91	80	69
C_n	32	25	45	–	–
C_i	–	–	22	22	–
CP	69	61	78	43	55
D	39	–	50	–	–

TABLE ID
Set-up and Hold Times.
All in ns.
All relative to clock
LOW-to-HIGH transition.

	CP: ⎍	
Input	Set-up Time	Hold Time
C_n	43	0
C_i	32	5
D	52	2
I_{3-0}	114	0

Note: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

II. GUARANTEED PERFORMANCE OVER MILITARY OPERATING RANGE.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	85	60

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

	To Output				
From Input	**Y**	**C_{i+4}**	**C_{i+4} (Note 1)**	**C_{i+4} (Note 2)**	**$\overline{Full}$**
I_{3-0}	88	82	97	87	78
C_n	37	30	46	–	–
C_i	–	–	23	23	–
CP	74	66	84	45	60
D	44	–	55	–	–

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

	CP: ⎍	
Input	**Set-up Time**	**Hold Time**
C_n	52	0
C_i	37	5
D	60	2
I_{3-0}	124	0

Note: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2920	8-Bit Register
Am2922	Condition Code MUX

Am2940

DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- **DMA Address Generation**
  Generates memory address, word count and DONE signal for DMA transfer operation.
- **Expandable Eight-bit Slice**
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- **Repeat Data Transfer Capability**
  Initial memory address and word count are saved so that the data transfer can be repeated.
- **Programmable Control Modes**
  Provides four types of DMA transfer control plus memory address increment/decrement.
- **High Speed, Bipolar LSI**
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- **Microprogrammable**
  Executes 8 different instructions.

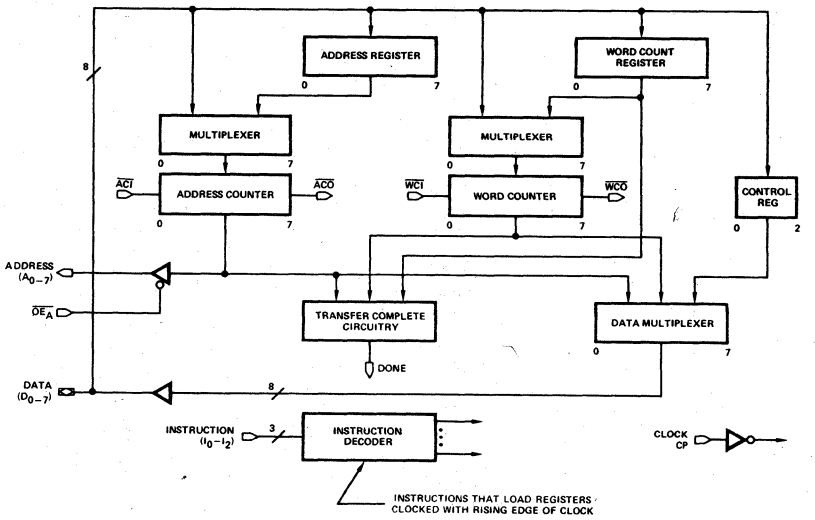
GENERAL DESCRIPTION

The Am2940, a 28-pin member of Advanced Micro Devices' Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

BLOCK DIAGRAM



Am2940 DMA Address Generator BD002450

For applications information see the last part of this data sheet and Chapter VII of *Bit Slice Microprocessor Design*, by Mick and Brick, McGraw-Hill Publishers.

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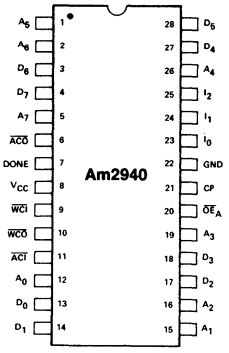
CONNECTION DIAGRAM
Top View

D-28



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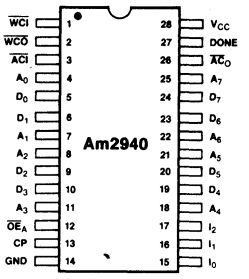
F-28



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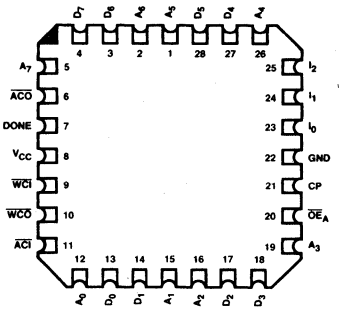
Chip-Pak™ L-28



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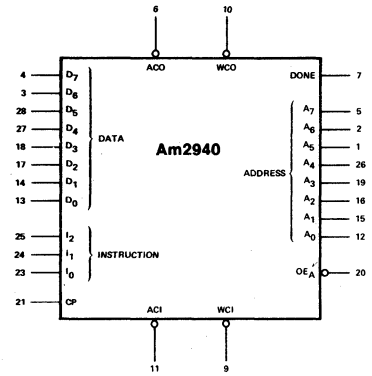
Note: Pin 1 is marked for orientation

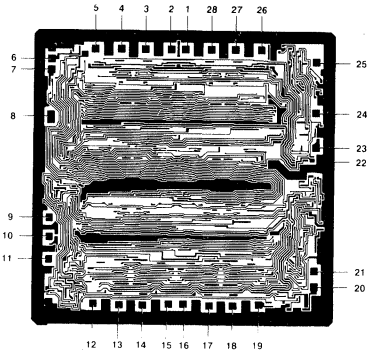
LOGIC SYMBOL



LS001021

METALLIZATION AND PAD LAYOUT

Note: Numbers refer to DIP pin connection.



DIE SIZE: 0.178″ x 0.181″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2940 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D– 28-pin CERDIP
  - F – 28-pin flatpak
  - L – 28-pin leadless chip carrier
  - X – Dice
- Am2940 — Device type
  - DMA Address Generator

Valid Combinations	
Am2940	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
23, 24, 25	I_{0-2}	I	Selects one of eight instructions.
11	$\overline{ACI}$	I	Carry-in to the address counter.
6	$\overline{ACO}$	O	Carry-out from the address counter.
9	$\overline{WCI}$	I	Carry-in to the word counter.
10	$\overline{WCO}$	O	Carry-out from the word counter.
	D_{0-7}	I/O	External data.
	A_{0-7}	O	Address outputs under control of Output Enable input, $\overline{OE}_A$.
20	$\overline{OE}_A$	I	Address output enable.
7	DONE	O	Transfer complete signal.
21	CP	I	Clock input. Registers and counters change on the LOW-to-HIGH transition.

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register
- An eight-bit Address Counter with input multiplexer
- An eight-bit Address Register
- An eight-bit Word Counter with input multiplexer
- An eight-bit Word Count Register
- Transfer complete circuitry
- An eight-bit wide data multiplexer with three-state output buffers
- Three-state address output buffers with external output enable control
- An instruction decoder

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry Input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW-to-HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is an open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data Output Buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The Address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits, CR_0-CR_1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW-to-HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

L = LOW
H = HIGH

Figure 1. Control Register Format Definition.

Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW-to-HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW-to-HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW-to-HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW-to-HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

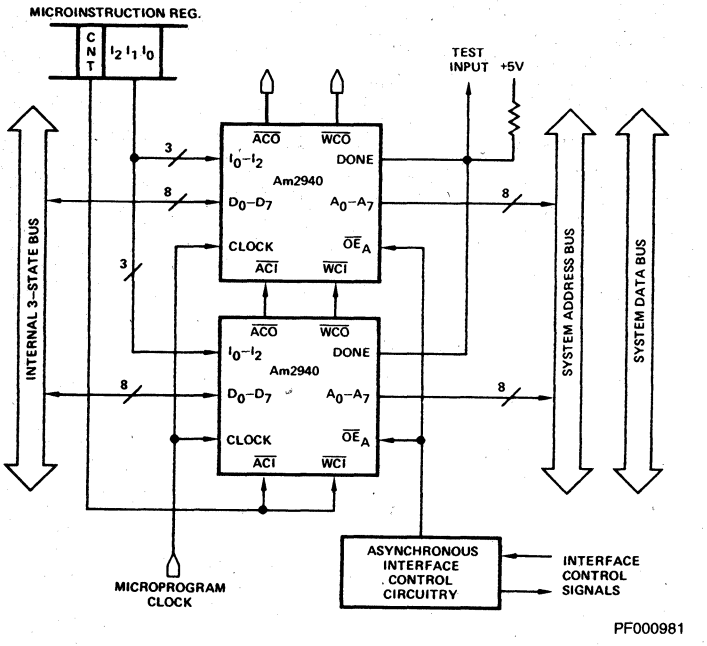


Figure 2. Am2940 Interconnections.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register; one instruction enables the Address and Word counters; and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW-to-HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2	I_1	I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0–D_7
L	L	L	0	WRITE CONTROL REGISTER	WRCR	0,1,2,3	HOLD	HOLD	HOLD	HOLD	D_0–$D_2 \rightarrow$ CR	INPUT
L	L	H	1	READ CONTROL REGISTER	RDCR	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	CR $\rightarrow$ D_0–D_2 (Note 1)
L	H	L	2	READ WORD COUNTER	RDWC	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	WC $\rightarrow$ D
L	H	H	3	READ ADDRESS COUNTER	RDAC	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	AC $\rightarrow$ D
H	L	L	4	REINITIALIZE COUNTERS	REIN	0,2,3	HOLD	WCR $\rightarrow$ WC	HOLD	AR $\rightarrow$ AC	HOLD	Z
						1	HOLD	ZERO $\rightarrow$ WC	HOLD	AR $\rightarrow$ AC	HOLD	Z
H	L	H	5	LOAD ADDRESS	LDAD	0,1,2,3	HOLD	HOLD	D $\rightarrow$ AR	D $\rightarrow$ AC	HOLD	INPUT
H	H	L	6	LDAD WORD COUNT	LDWC	0,2,3	D $\rightarrow$ WR	D $\rightarrow$ WC	HOLD	HOLD	HOLD	INPUT
						1	D $\rightarrow$ WR	ZERO $\rightarrow$ WC	HOLD	HOLD	HOLD	INPUT
H	H	H	7	ENABLE COUNTERS	ENCT	0,1,3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
						2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg. WCR = Word Count Reg. L = LOW
AR = Address Reg. WC = Word Counter H = HIGH
AC = Address Counter D = Data Z = High Impedance

Note 1: Data Bits D_3-D_7 are high during this instruction.

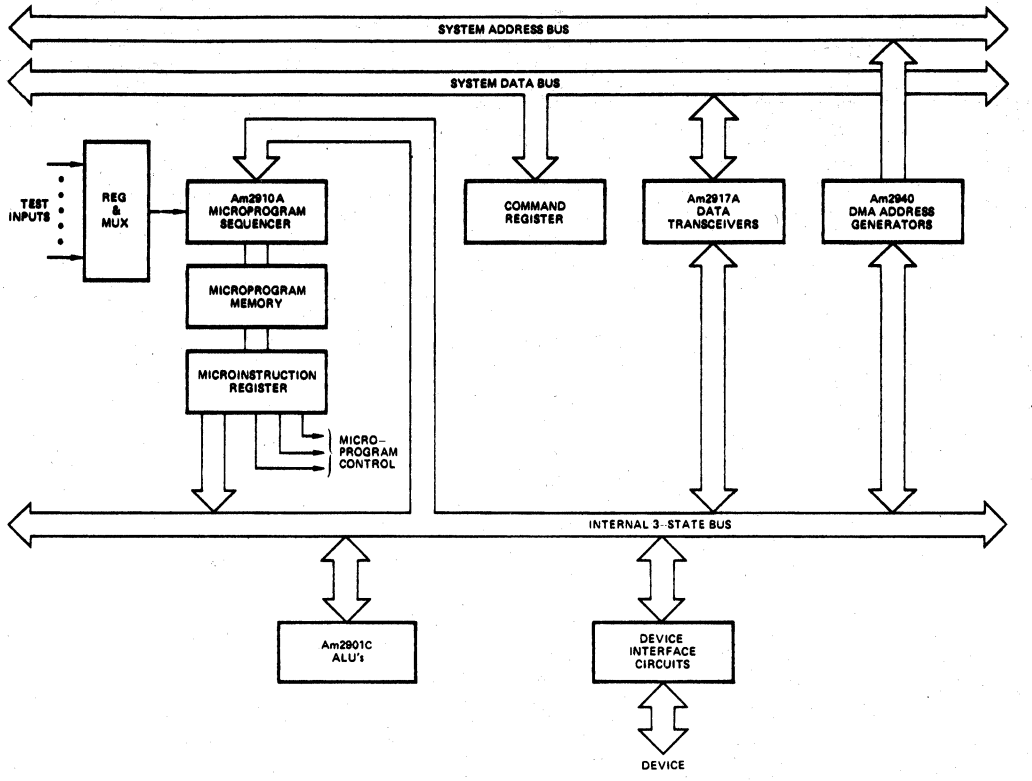
APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2910A Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901C Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 2. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910A Microprogram Sequencer.



BD002221

Figure 3. DMA Peripheral Controller Block Diagram.

03575B

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

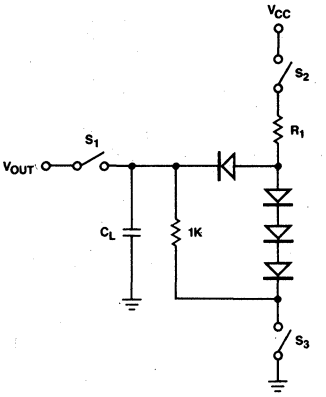
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −1.0mA		2.4			Volts
			COM'L I_{OH} = −2.6mA					
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} (Note 5)	$\overline{WCO}$, $\overline{ACO}$	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-7}			150	µA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX, V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7}			−50	µA
				D_{0-7}			−150	
I_{OZH}			V_{OUT} = 2.4	A_{0-7}			50	
				D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2940DC	T_A = 0°C to +70°C			290	mA
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.

SWITCHING TEST CIRCUIT

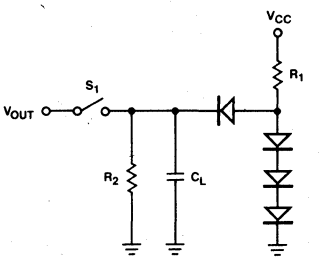
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS

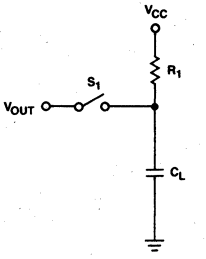


TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



TC001220

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, stray wiring and capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2940 (DIP)

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	D_{0-7}	A	220	1K
6	$\overline{ACO}$	B	470	2.4K
7	DONE	C	270	–
10	$\overline{WCO}$	B	470	2.4K

For additonal information on testing, see section "Guidelines on Testing Am2900 Family Devices."

SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified or a 5pF load.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2940DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	4
I_{012}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	-	-	-	-
$\overline{WCI}$ (Note 2)	-	20	-	46	-
I_{0-2}	-	-	-	-	37
CP (Note 3)	58	58	54	85	-

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2940DM, FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	-	-	-	-
$\overline{WCI}$ (Note 2)	-	21	-	54	-
I_0-I_2	-	-	-	-	41
CP (Note 3)	64	64	62	88	-

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	16	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes: 1. Control modes 0, 1, and 3 only.
2. $\overline{WCI}$ to DONE occurs only in control modes 0 and 1.
3. CP to DONE occurs only in control modes 0, 1, and 2.

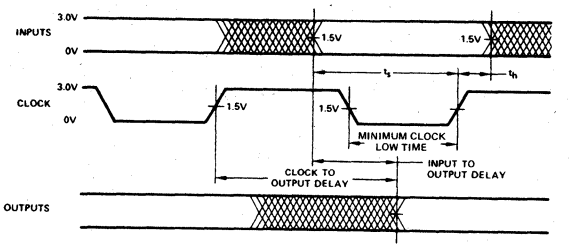


Figure 4. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2942

Programmable Timer/Counter DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- **Expandable eight-bit slice**
  - Any number of Am2942s can be cascaded. Three devices provide a 48-bit counter.
- **Reinitialize capability**
  - Counters can be reinitialized from on-chip registers.
- **Executes 16 instructions**
  - Eight DMA instructions plus eight Timer/Counter instructions.
- **Programmable control modes**
  - Provide four types of control.
- **Two independent programmable 8-bit up/down counters**
  - Counters can be cascaded to form single-chip 16-bit up/down counter.
- **High speed bipolar LSI**
  - Typical count frequency of 25MHz and 24mA output current sink capability.

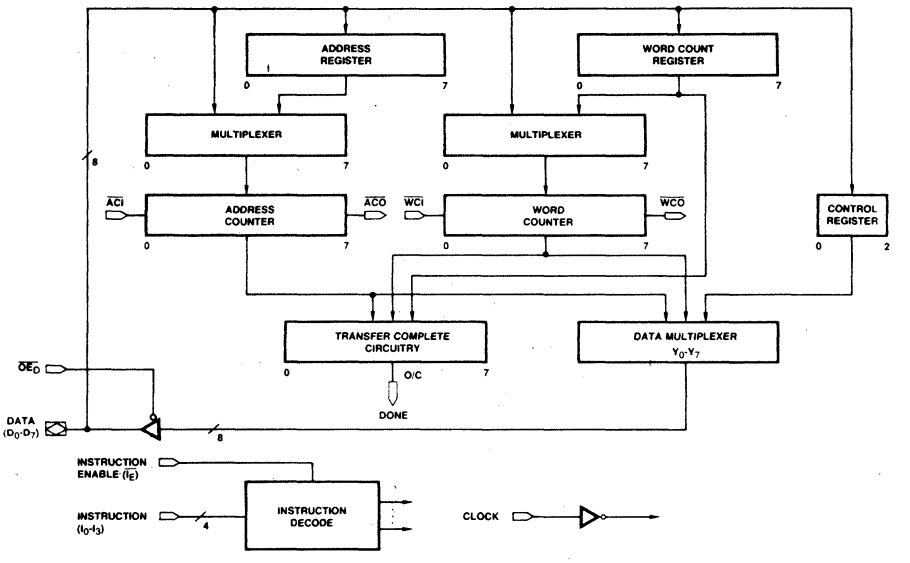
GENERAL DESCRIPTION

The Am2942, a 22-pin version of the Am2940, can be used as a high-speed DMA Address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2942 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2942 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2942 instruction field with other devices.

When used as a Timer/Counter, the Am2942 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2942s form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2942 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



BD002520

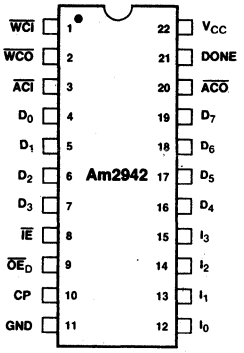
For applications information see the last part of this data sheet and Chapter VII of *Bit Slice Microprocessor Design*, by Mick and Brick, McGraw-Hill Publishers.

03574B

Refer to Page 13-1 for Essential Information on Military Devices

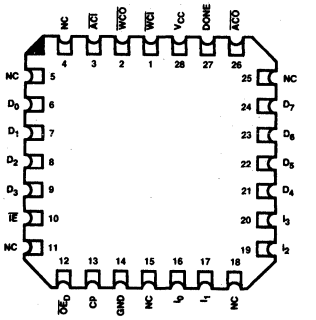
CONNECTION DIAGRAM
Top View

D-22
F-22*



CD004751

Chip-Pak™
L-28

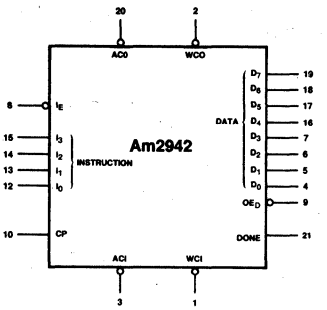


CD004851

*F-22 Pin Configuration identical to D-22

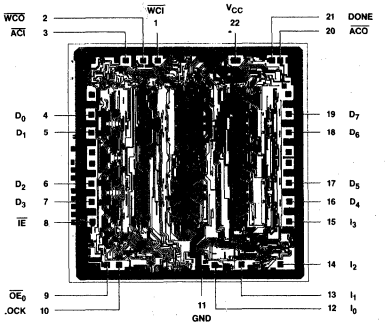
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000941

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.181″ x 0.178″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2942 D C B

- Screening Option
  - Blank – Standard processing
  - B – Burn-in
- Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 22-pin CERDIP
  - F – 22-pin flatpak
  - L – 28-pin leadless chip carrier
  - X – Dice
- Device type
  - DMA Address Generator

Valid Combinations	
Am2942	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
12, 13, 14, 15	I_{0-3}	I	Selects one of sixteen instructions.
3	$\overline{ACI}$	I	Carry-in to the address counter.
20	$\overline{ACO}$	O	Carry-out from the address counter.
1	$\overline{WCI}$	I	Carry-in to the word counter.
2	$\overline{WCO}$	O	Carry-out from the word counter.
	D_{0-7}	I/O	Bidirectional data bus.
9	$\overline{OE}_D$	I	Data bus output enable.
8	$\overline{IE}$	I	Instruction enable for I_{0-2}.
21	DONE	O	Transfer complete signal.
10	CP	I	Clock input. Registers and counters change on the LOW-to-HIGH transition.

Am2942 ARCHITECTURE

As shown in the Block Diagram, the Am2942 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

CONTROL REGISTER

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2942 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full lookahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW-to-HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0 and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_0-D_7 if and only if the Output Enable input, $\overline{OE}_D$, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3, Control Register bits, CR_0-CR_1, and the INSTRUCTION ENABLE input, $\overline{I_E}$.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW-to-HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

$\overline{OE_D}$	$D_0 - D_7$
L	DATA MULTIPLEXER OUTPUT, $Y_0 - Y_7$
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

Am2942 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW-to-HIGH transition of the CLOCK input, CP. Figure 1 specifies when the DONE signal is generated in this mode.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW-to-HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address.

When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW-to-HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW-to-HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2942 INSTRUCTIONS

The Am2942 instruction set consists of sixteen instructions. Eight are DMA Instructions and are similar to the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2942 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2942 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Multiplexer outputs Y_0-Y_2. Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW-to-HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. When I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2942 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction is identical to the REINITIALIZE COUNTERS instruction and provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that the Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2942 acts as a DMA circuit: When I_3 is tied HIGH, the Am2942 acts as a Timer/Counter circuit.
2. Am2942 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2942 Instructions.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0-2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD COUNT	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	-	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0-2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, T/C	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	-	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2942 Function Table.

APPLICATIONS

Figure 5 shows an Am2942 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910A Microprogram Sequencer provides an address to Am27S27 512 x 8 Registered PROMs. The on-chip PROM output register is used as the Microinstruction Register.

The Am2942 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 6 shows an Am2942 used as a single 16-bit programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 7 shows two Am2942s cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

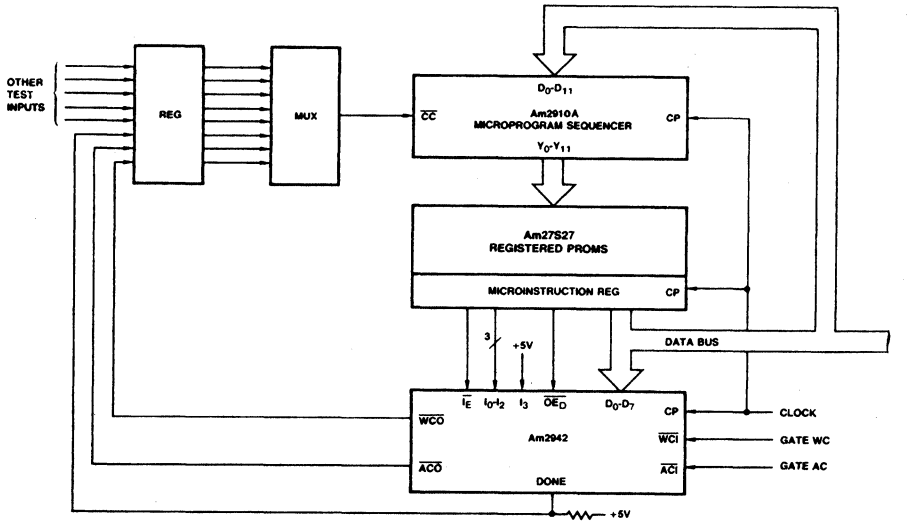

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Figure 5. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package.

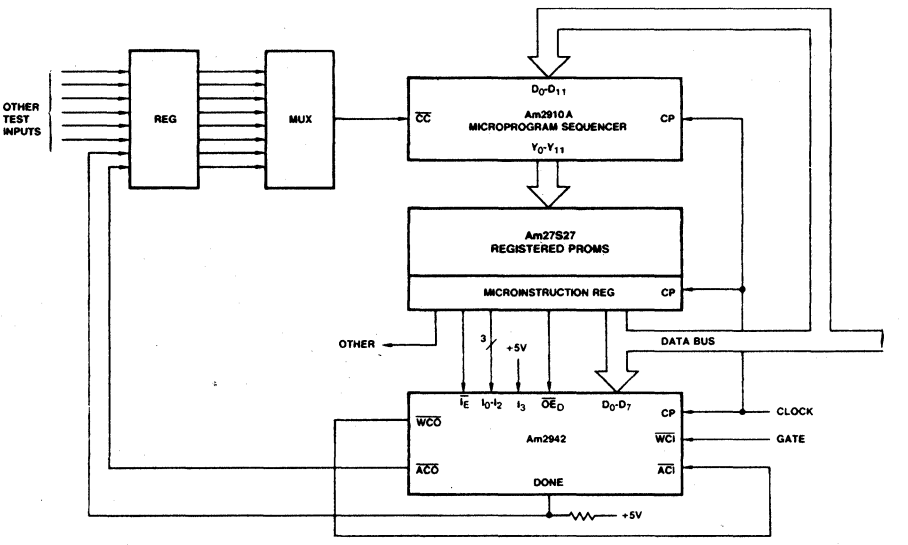

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Figure 6. 16-Bit Programmable Counter/Timer Using a Single Am2942.

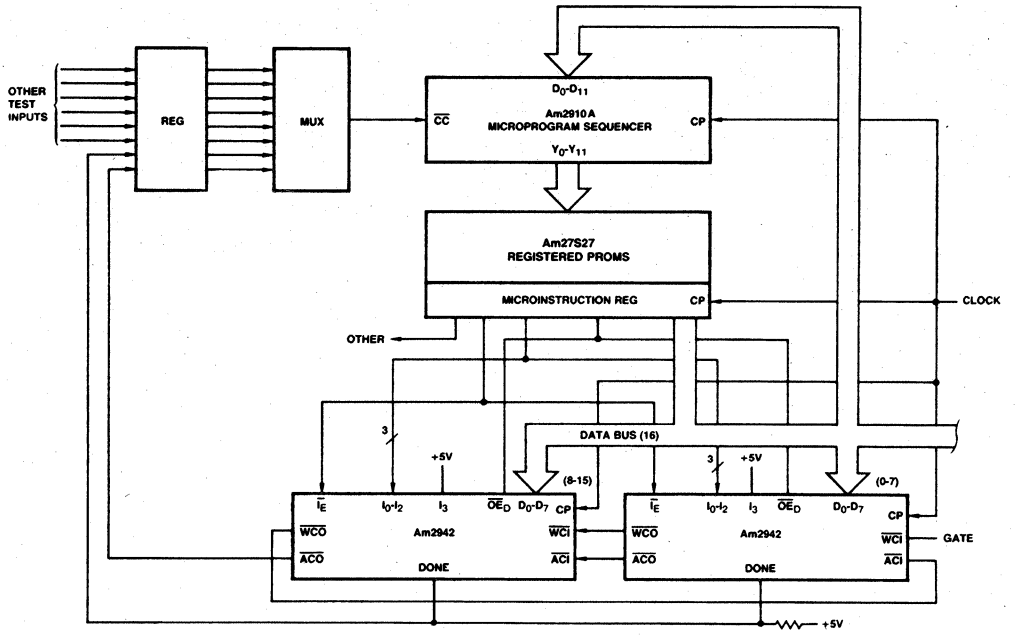

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Figure 7. 32-Bit Programmable Counter/Timer Using Two Am2942s.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

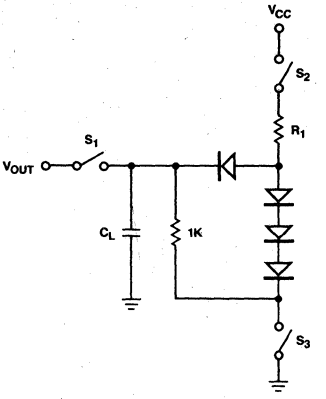
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −1.0mA		2.4			Volts
			COM'L I_{OH} = −2.6mA					
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{WCO}$, $\overline{ACO}$	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			D_{0-7}, DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input Logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-7}			150	µA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX, V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	D_{0-7}			−150	µA
I_{OZH}			V_{OUT} = 2.4	D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2942PC, DC	T_A = 0°C to +70°C			265	mA
				T_A = +70°C			220	
			Am2942DM, FM	T_C = −55°C to +125°C			285	
				T_C = +125°C			205	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).

SWITCHING TEST CIRCUIT

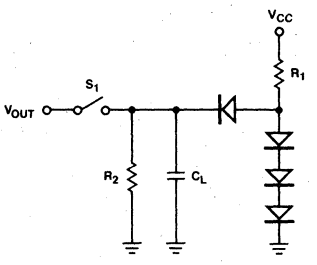
A. THREE STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS

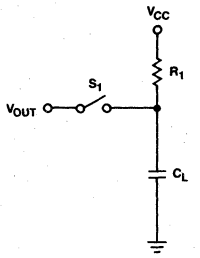


TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



TC001220

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2942 (DIP)

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
–	D_{0-7}	A	220	1K
20	$\overline{ACO}$	B	470	2.4K
21	DONE	C	270	–
2	$\overline{WCO}$	B	470	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

SWITCHING CHARACTERISTICS

The tables below define the Am2942 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times (I to D) which are specified for a 5pF load.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2942, DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	6
I_{0-3}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$	30	3
I_E	46	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	20	-	-	-
$\overline{WCI}$ (Note 1)	-	20	46	-
I_{0-3}	-	-	-	37
CP (Note 2)	58	58	85	59
I_E	-	-	-	37

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	25	25	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2942DM, FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	7
I_{0-3}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$	34	5
I_E	49	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	21	-	-	-
$\overline{WCI}$ (Note 1)	-	21	54	-
I_{0-3}	-	-	-	41
CP (Note 2)	64	64	88	68
I_E	-	-	-	41

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	30	30	ns

Notes: 1. $\overline{WCI}$ to DONE occurs only in control modes 0 and 1.
2. CP to DONE occurs only in control modes 0, 1, and 2.

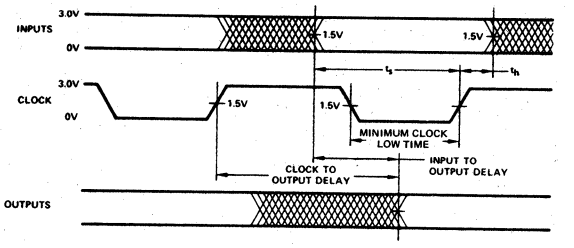


Figure 8. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2946/Am2947

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- V_{CC} – 1.15V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability; Low power – 8mA per bidirectional bit
- Am2946 inverting transceivers; Am2947 noninverting transceivers; Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- Bus port stays in hi-impedance state during power up/down

GENERAL DESCRIPTION

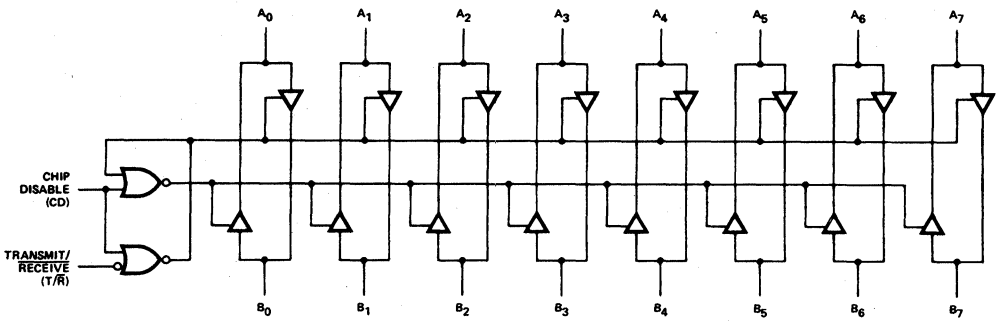
The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$, determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

BLOCK DIAGRAM

Am2947



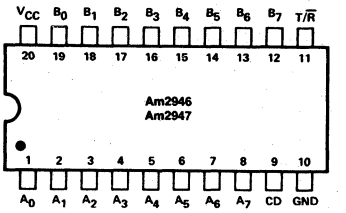
BD002530

Am2946 has inverting transceivers.

05406A

CONNECTION DIAGRAM
Top View

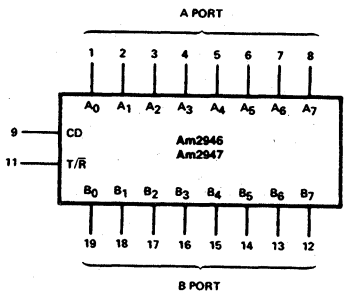
D-20-1



CD004760

Note: Pin 1 is marked for orientation

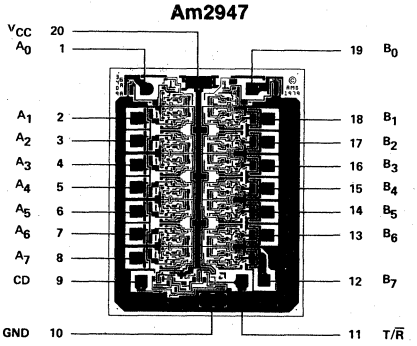
LOGIC SYMBOL



LS001060

METALLIZATION AND PAD LAYOUT

Am2947



DIE SIZE .069″ x .089″

Note: The Am2946 has inverting transceivers

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2946/2947 D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 20-pin CERDIP; X– Dice
- Am2946/2947 — Device type: Bidirectional Bus Transceivers

Valid Combinations	
Am2946 Am2947	PC DC, DCB, DM, DMB XC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_0-A_7	I/O	A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.
	B_0-B_7	I/O	B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.
9	CD	I	Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).
11	T/$\overline{R}$	I	Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

FUNCTION TABLE

Inputs	Conditions		
Chip Disable	L	L	H
Transmit/$\overline{Receive}$	L	H	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage 7.0V
Input Voltage 5.5V
Output Voltage 5.5V
Lead Temperature (Solder, 10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC} − 1.15	V_{CC} − 0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OL} = 12mA		0.3	0.4	Volts
			COM'L I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Minimum Input Voltage	CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{CO}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.1	−0.25	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	Am2946	CD = V_I = 2.0V, V_{CC} = MAX		70	100	mA
			CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am2947B	CD = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	
			CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

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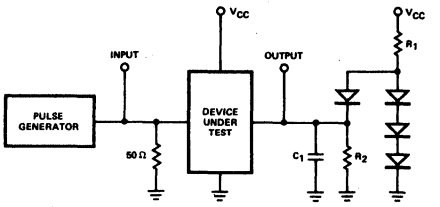
Refer to Page 13-1 for Essential Information on Military Devices

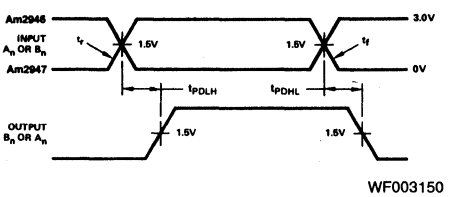
SWITCHING TEST CIRCUIT



TC001480

Note: C_1 includes test fixture capacitance.

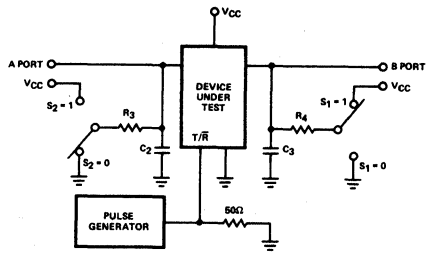
SWITCHING TIME WAVEFORM



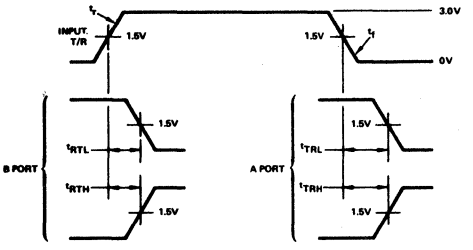
WF003150

$t_r = t_f < 10ns$ 10% to 90%

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



TC001390

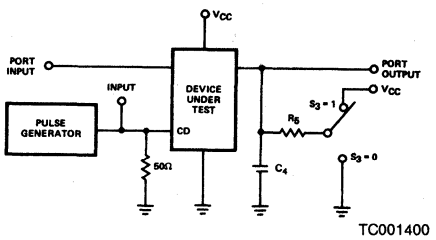


WF003110

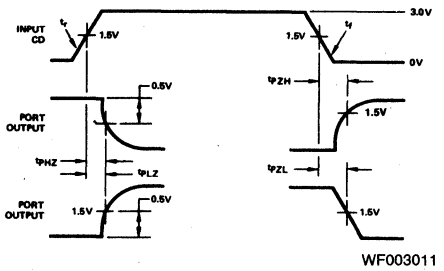
Note: C_2 and C_3 include test fixture capacitance.

$t_r = t_f < 10ns$ 10% to 90%

Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.



TC001400



WF003011

Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition.

$t_r = t_f < 10ns$ 10% to 90%

Figure 3. Propagation Delay from CD to A Port or B Port.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2946

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_1 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	22	35	ns
		S_3 = 0, R_5 = 5k, C_1 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	23	33	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	22	33	ns
t_{RTL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	26	35	ns
t_{RTH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	27	35	ns

Note: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2946

Parameter	Description	Test Conditions	COMMERCIAL Am2946 Max	MILITARY Am2946 Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	16	19	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	20	23	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	24	29	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	16	19	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	25	30	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V(Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V(Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	38	43	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	38	43	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	41	47	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	41	47	ns

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2947

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3, = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3, = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		R_3 = 1, R_5 = 667Ω, C_1 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	26	35	ns
		S_3 = 0, R_5 = 5k, C_1 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	28	38	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	28	38	ns
t_{RTL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	31	40	ns
t_{RTH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	31	40	ns

Note: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2947

Parameter	Description	Test Conditions	COMMERCIAL Am2947 Max	MILITARY Am2947 Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	42	48	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	42	48	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns

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Refer to Page 13-1 for Essential Information on Military Devices

Am2948/Am2949

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability; Low power – 8mA per bidirectional bit
- Am2948 has inverting transceivers; Am2949 has non-inverting transceivers — both have separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- Bus port stays in hi-impedance state during power up/down

GENERAL DESCRIPTION

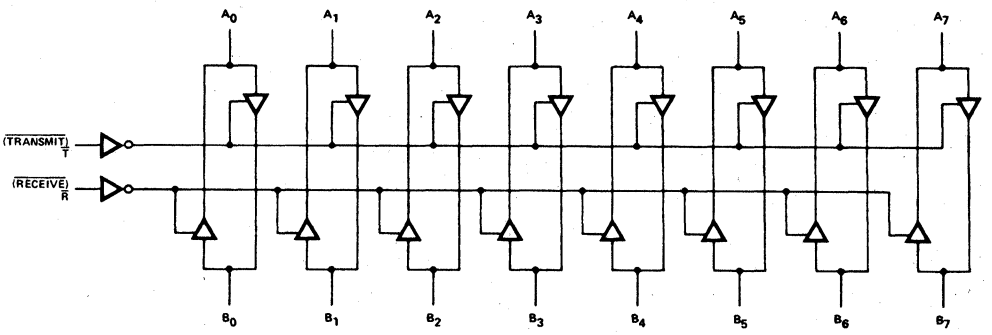
The Am2948 and Am2949 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

BLOCK DIAGRAM

Am2949



BD002500

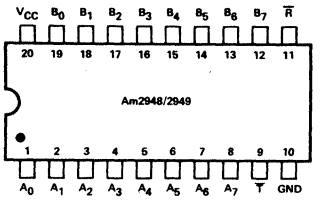
Am2948 has inverting transceivers.

05407A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

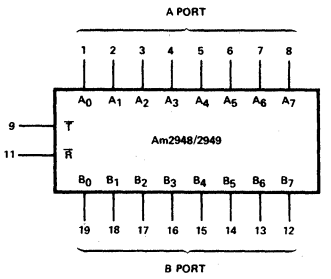
D-20-1



CD004770

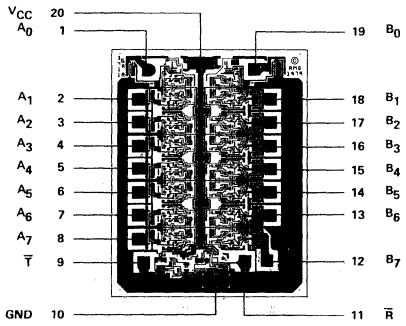
Note: Pin 1 is marked for orientation
Am2948 is inverting from Ai to Bi

LOGIC SYMBOL



LS000990

METALLIZATION AND PAD LAYOUT
Am2949



DIE SIZE .069" x .089"
Note: The Am2948 has inverting transceivers

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2948/2949 **D** **C** **B**

- **B** — Screening Option
  Blank – Standard processing
  B – Burn-in
- **C** — Temperature (See Operating Range)
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- **D** — Package
  D– 20-pin CERDIP
  P– 20-pin plastic DIP
  X– Dice
- **Am2948/2949** — Device type
  Bidirectional Bus Transceivers

Valid Combinations	
Am2948 Am2949	PC DC, DCB, DM, DMB XC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_0-A_7	I/O	A port inputs/.outputs are receiver output drivers when $\overline{\text{Receive}}$ is LOW and $\overline{\text{Transmit}}$ is HIGH, and are transmit inputs when $\overline{\text{Receive}}$ is HIGH and $\overline{\text{Transmit}}$ is LOW.
	B_0-B_7	I/O	B port inputs/outputs are transmit output drivers when $\overline{\text{Transmit}}$ is LOW and $\overline{\text{Receive}}$ is HIGH, and are receiver inputs when $\overline{\text{Transmit}}$ is HIGH and $\overline{\text{Receive}}$ is LOW.
9,11	$\overline{\text{Transmit}}$, $\overline{\text{Receive}}$	I	These controls determine whether A port and B port drivers are in 3-state. With both $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ HIGH both ports are in 3-state. $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{\text{Transmit}}$ HIGH and $\overline{\text{Receive}}$ LOW A port is the output and B port is the input. With $\overline{\text{Transmit}}$ LOW and $\overline{\text{Receive}}$ HIGH B port is the output and A port is the input.

FUNCTION TABLE

Control Inputs		Resulting Conditions	
Transmit	**Receive**	**A Port**	**B Port**
H	L	Out	In
L	H	In	Out
H	H	3-State	3-State
L	L	Both Active*	

*This is not an intended logic condition and may cause oscillations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage 7.0V
Input Voltage 5.5V
Output Voltage 5.5V
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ	Max	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "O" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC} − 1.15	V_{CC} − 0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical"0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 12mA		0.3	0.4	Volts
			COM'L I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX; Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC} − 1.15	V_{CC} − 0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.OV, $\overline{R}$ = 0.8V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	

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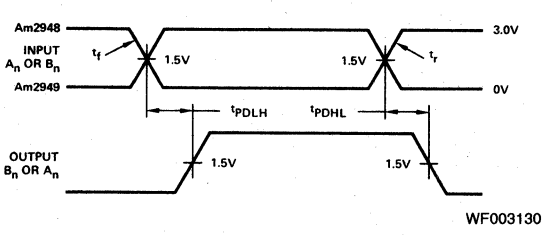
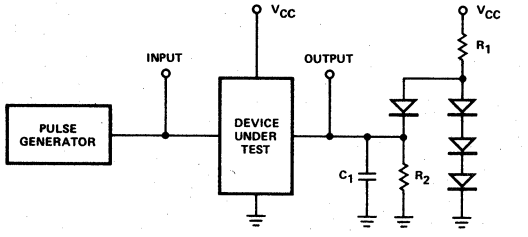
DC CHARACTERISTICS (Cont.)

CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	Am2948	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX		70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am2949	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

SWITCHING TEST WAVEFORM



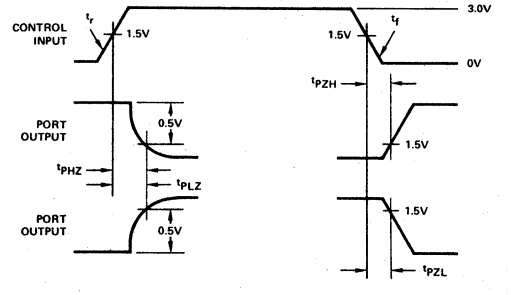
SWITCHING TEST CIRCUIT

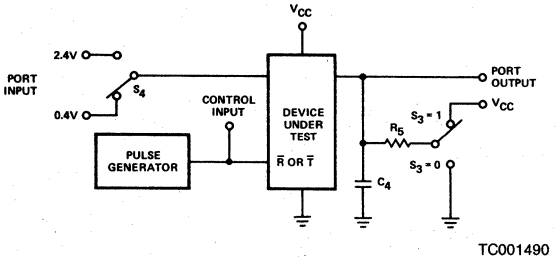


$t_r = t_f < 10ns$
10% to 90%

Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port.





$t_r = t_f < 10ns$
10% to 90%

Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2948

Parameter	Description	Test Conditions	Typ	Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 30pF	20	27	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)			
		R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)			
		R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B)			
		S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_1 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B)			
		S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2948

Parameter	Description	Test Conditions	COMMERCIAL Am2948 Max	MILITARY Am2948 Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	19	16	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	23	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	29	24	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	16	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	30	25	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	19	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2949

Parameter	Description	Test Conditions	Typ	Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 5k, C_4 = 30pF	20	27	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_1 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_1 = 45pF	17	25	ns

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2949

Parameter	Description	Test Conditions	COMMERCIAL Am2949 Max	MILITARY Am2949 Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 0.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

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Am2950-50A/Am2951-51A

Eight-Bit Bidirectional I/O Ports with Handshake

DISTINCTIVE CHARACTERISTICS

- **Eight-Bit, Bidirectional I/O Port with Handshake**– Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- **Register Full/Empty Flags**– On-chip flag flip-flops provide data transfer handshaking signals.
- **24mA Output Current Sink Capability.**
- **Separate Clock, Clock Enable and Three-State Output Enable for Each Register.**
- **Separate, Edge-Sensitive Clear Control for Each Flag Flip-Flop.**
- **Fast** – The Am2950A and Am2951A will be 25–30% faster than the Am2950 and Am2951.

GENERAL DESCRIPTION

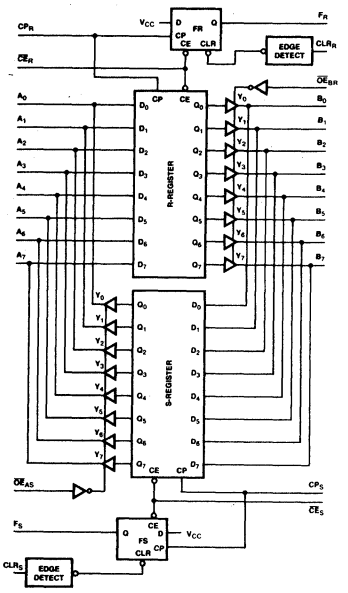
The Am2950 and Am2951, members of Advanced Micro Devices' Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2950/Am2951. Separate clock, Clock Enable and Three-State Output Enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

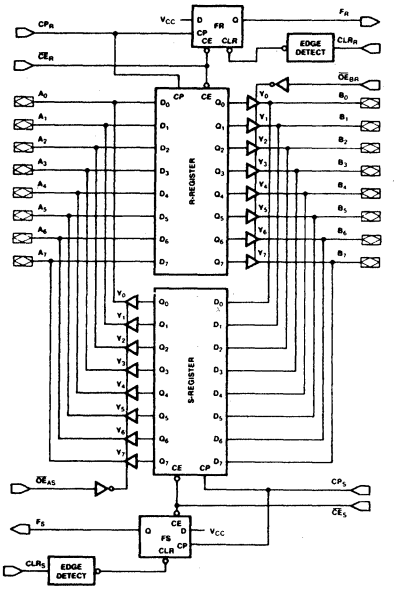
24mA output current sink capability, sufficient for most three-state busses, is provided by the Am2950/Am2951.

The Am2950A and Am2951A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2950 and Am2951 respectively but will be approximately 30% faster.

BLOCK DIAGRAM



BD002420



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Note: The Am2951 provides inverting data outputs (B_{0-7}).

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CONNECTION DIAGRAM
Top View

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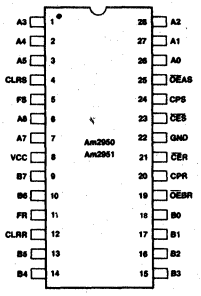

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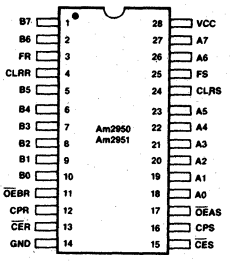
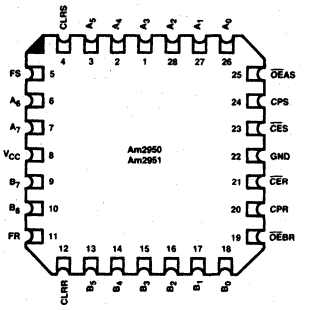


CD004660

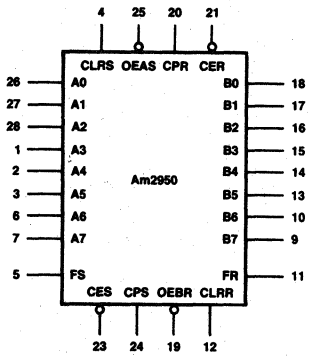
Chip-Pak™ L-28



CD004640

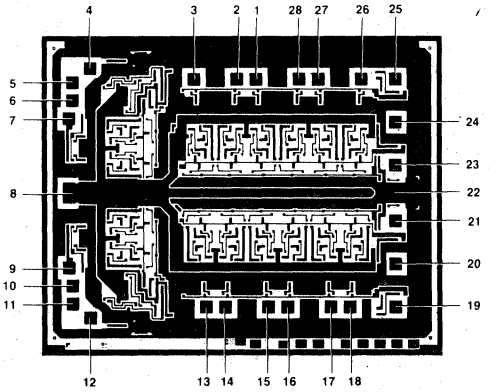
Note: Pin 1 is marked for orientation
Bi is inverted on Am2951.

LOGIC SYMBOL



LS001030

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.107″ x 0.138″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2950/50A
Am2951/51A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 28-pin CERDIP
  - F – 28-pin flatpak
  - L – 28-pin leadless chip carrier
  - X – Dice

Device type
8-Bit Bidirectional I/O Ports

Valid Combinations	
Am2950/50A Am2951/51A	DC, DCB, DMB FMB LC, LMB, XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A0-7	I/O	Eight bidirectional lines carrying the R Register inputs or S Register outputs.
	B0-7	I/O	Eight bidirectional lines carrying the S Register inputs or B Register outputs.
20	CPR	I	The clock for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW-to-HIGH transition of the CPR signal.
21	$\overline{CER}$	I	The Clock Enable for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW-to-HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, The R Register and FR Flip-Flop hold their contents, regardless of CPR signal transitions.
19	$\overline{OEBR}$	I	The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, the R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.
11	FR	O	The FR Flip-Flop output.
12	CLRR	I	The clear control for the FR Flip-Flop. The FR Flip-Flop is cleared on the LOW-to-HIGH transition of CLRR signal.
24	CPS	I	The clock for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW-to-HIGH transition of the CPS signal.
23	$\overline{CES}$	I	The clock enable for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW-to-HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register and FS Flip-Flop hold their contents, regardless of CPS signal transitions.
25	$\overline{OEAS}$	I	The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When $\overline{OEAS}$ is HIGH, the S Register outputs are in the high-impedance state.
5	FS	O	The FS Flip-Flop output.
4	CLRS	I	The clear control for the FS Flip-Flop. The FS Flip-Flop is cleared on the LOW-to-HIGH transition of CLRS signal.

5

REGISTER FUNCTION TABLE (Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

$\overline{OE}$	Internal Q	Y-Outputs		Function
		Am2950	Am2951	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

FLAG FLIP-FLOP FUNCTION TABLE (Applies to R or S Flag Flip-Flop)

Inputs			F-Output	Function
$\overline{CE}$	CP	CLR		
H	X	‡	NC	Hold Flag
X	X	↑	L	Clear Flag
L	↑	‡	H	Set Flag

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

NC = NO CHANGE
↑ = LOW-to-HIGH Transition
‡ = NO LOW-to-HIGH Transition

APPLICATIONS

The Am2950/Am2951 provides data transfer handshaking signals as well as eight-bit, bidirectional data storage. Its flexibility allows it to be used in any type of computer system, including Am2900, 8080, 8085, 8086, Z80, and Z8000 systems.

Figure 1 shows an Am2950 used to store data moving in both directions between a bidirectional system data bus and a bidirectional peripheral data bus. The on-chip Flag flip-flops provide the data in, data out handshaking signals required for data transfer and interrupt request generation.

Figure 2 shows a multiple I/O port system using Am2950's. Two Am2950's are used at each port to interface the 16-bit system data bus. The Am2950 flags are used to generate I/O interrupt requests.

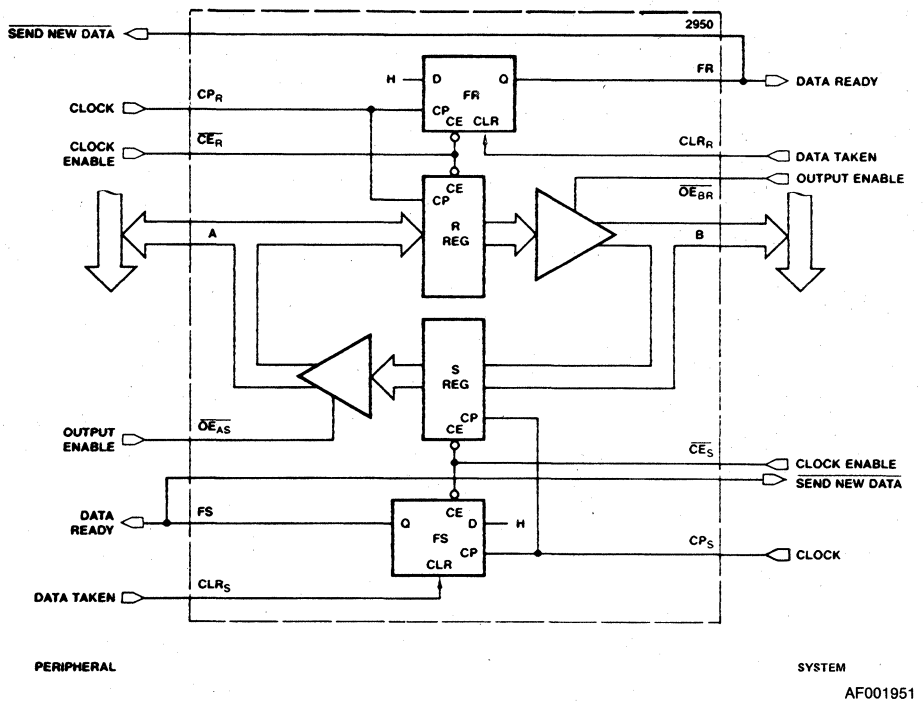


Figure 1. A Bidirectional I/O Port with Handshaking Using the Am2950.

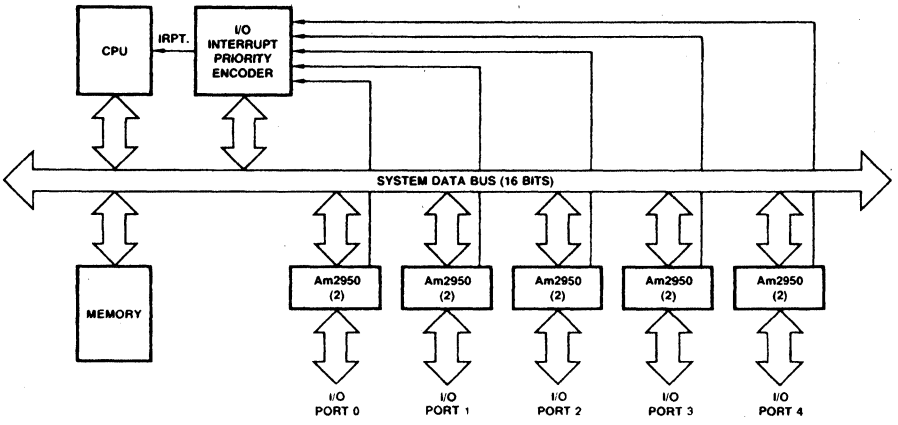


Figure 2. Multiple I/O Port System.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

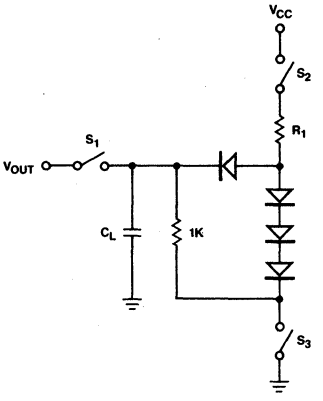
DC CHARACTERISTICS over operating range unless otherwise specified
Am2950/Am2951

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	FR, FS	I_{OH} = −1mA	2.4	3.4		Volts
			A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA	2.4	3.4		
				COM'L, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	FR,FS	I_{OL} = 12mA			0.5	Volts
			A_{0-7}, B_{0-7}	MIL I_{OL} = 16mA			0.5	
				COM'L, I_{OL} = 2.4mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}			−250	μA
				CLRR,CLRS			−2.0	mA
				Others			−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_{0-7}, B_{0-7}			70	μA
				CLRR, CLRS			100	
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V			70	μA
				V_O = 0.4V			−250	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Notes 4,5)	V_{CC} = MAX	COM'L	T_A = 0°C to +70°C			275	mA
				T_A = +70°C			228	
			MIL	T_C = −55°C to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.
5. Worst case I_{CC} is at minimum temperature.

SWITCHING TEST CIRCUIT

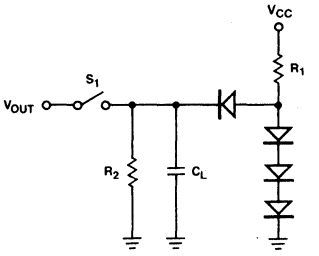
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2950/2951 (DIP)

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	B_{0-7}	A	220	1K
5	FS	B	300	2.4K
11	FR	B	300	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2950A/Am2951A SWITCHING CHARACTERISTICS

The tables below define the Am2950A/Am2951A switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↑		
B0-7	CPS ↑		
$\overline{CES}$	CPS ↑		
$\overline{CER}$	CPR ↑		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑				
CPR ↑				
CLRS ↑				
CLRR ↑				

C. Recovery Times

From	To	tREC
CLRS ↑	CPS ↑	
CLRR ↑	CPR ↑	

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↑		
B0-7	CPS ↑		
$\overline{CES}$	CPS ↑		
$\overline{CER}$	CPR ↑		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑				
CPR ↑				
CLRS ↑				
CLRR ↑				

C. Recovery Times

From	To	tREC
CLRS ⌐¯	CPS ⌐¯	
CLRR ⌐¯	CPR ⌐¯	

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

Am2950/Am2951 SWITCHING CHARACTERISTICS

The tables below define the Am2950/Am2951 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ⌐¯	7	5
B0-7	CPS ⌐¯	7	5
$\overline{CE}$S	CPS ⌐¯	*19/15	4
$\overline{CE}$R	CPR ⌐¯	*19/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ⌐¯	*30/26	–	20	–
CPR ⌐¯	–	*30/26	–	20
CLRS ⌐¯	–	–	22	–
CLRR ⌐¯	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ⌐¯	CPS ⌐¯	31
CLRR ⌐¯	CPR ⌐¯	31

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	22	27
$\overline{OE}$BR	B0-7	22	27

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓	11	8
B0-7	CPS ↓	11	8
$\overline{CES}$	CPS ↓	*20/15	4
$\overline{CER}$	CPR ↓	*20/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	*35/28	–	20	–
CPR ↓	–	*35/28	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	34
CLRR ↓	CPR ↓	34

D. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	24	28
$\overline{OE}$BR	B0-7	24	28

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec.

Am2952-52A/Am2953-53A

Eight-Bit Bidirectional I/O Ports with Handshake

DISTINCTIVE CHARACTERISTICS

- **Eight-Bit, Bidirectional I/O Port** – Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- **Separate Clock, Clock Enable and Three-State Output Enable for Each Register.**
- **24mA Output Current Sink Capability.**
- **Inverting and Non-Inverting Versions** – The Am2952 provides non-inverting data outputs. The Am2953 provides inverting data outputs.
- **24-pin Slim Package**
- **Fast** – The Am2952A and Am2953A will be 25–30% faster than the Am2952 and Am2953.

GENERAL DESCRIPTION

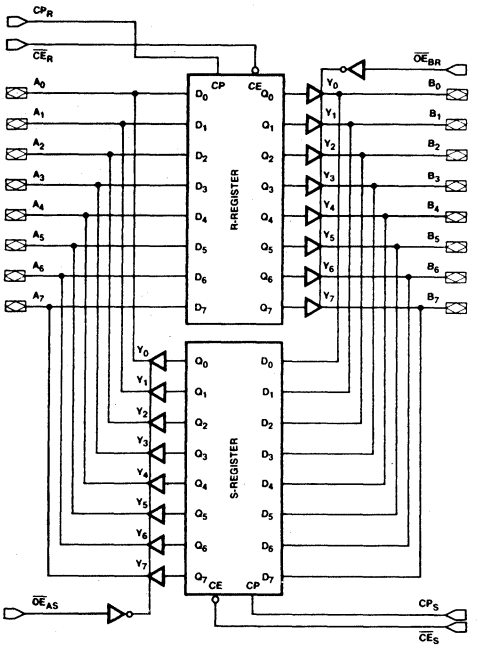
The Am2952 and Am2953, members of Advanced Micro Devices' Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2952/Am2953. Separate Clock, Clock Enable and Three-State Output Enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

24mA output current sink capability, sufficient for most three-state busses, is provided by the Am2952/Am2953.

The Am2952A and Am2953A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2952 and Am2953 respectively but will be approximately 30% faster.

BLOCK DIAGRAM



BD002371

Note: The Am2953 provides inverting data output

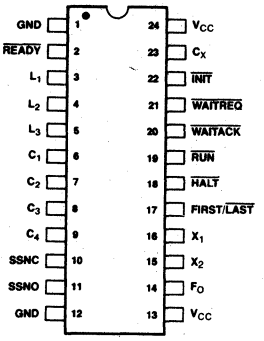
IMOX is a trademark of Advanced Micro Devices, Inc.

01402B

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

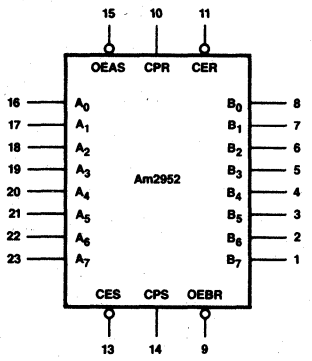
Am2952
D-24-SLIM



CD004820

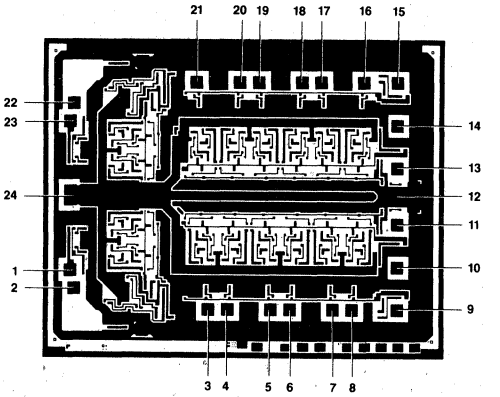
Note: Pin 1 is marked for orientation
B_i is inverted on Am2953

LOGIC SYMBOL
Am2952



LS001140

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.107" x 0.138"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2952/52A
Am2953/53A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin SLIMDIP
  - X– Dice
- **Am2952/52A / Am2953/53A** — Device type
  - 8-Bit Bidirectional I/O Ports

Valid Combinations	
Am2952/52A	DC, DCB, DMB
Am2953/53A	XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

01402B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A0-7	I/O	Eight bidirectional lines carrying the R Register inputs or S Register outputs.
	B0-7	I/O	Eight bidirectional lines carrying the S Register inputs or R Register outputs.
10	CPR	I	The clock for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal.
11	$\overline{CER}$	I	The Clock Enable for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, the R Register holds its contents, regardless of CPR signal transitions.
9	$\overline{OE}$BR	I	The Output Enable for the R Register. When $\overline{OE}$BR is LOW, the R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OE}$BR is HIGH, the R Register outputs are in the high-impedance state.
14	CPS	I	The clock for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal.
13	$\overline{CES}$	I	The clock enable for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register holds its contents, regardless of CPS signal transitions.
15	$\overline{OE}$AS	I	The output enable for the S Register. When $\overline{OE}$AS is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When $\overline{OE}$AS is HIGH, the S Register outputs are in the high-impedance state.

REGISTER FUNCTION TABLE (Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

$\overline{OE}$	Internal Q	Y-Outputs		Function
		Am2950	Am2951	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

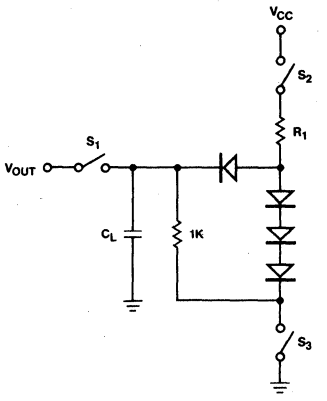
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA	2.4	3.4		Volts
				COM'L, I_{OL} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7} B_{0-7}	MIL, I_{OL} = 16mA			0.5	Volts
				COM'L, I_{OL} = 24mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}			−250	μA
				Others			−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_{0-7}, B_{0-7}			70	μA
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V			70	μA
				V_O = 0.4V			−250	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Notes 4, 5)	V_{CC} = MAX	COM'L	T_A = 0 to +70°C			275	mA
				T_A = +70°C			228	
			MIL	T_C = −55 to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.
5. Worst case I_{CC} is at minimum temperature.

SWITCHING TEST CIRCUIT

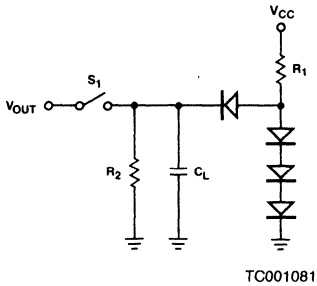
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2952/2953

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
16–23	A_{0-7}	A	220	1K
1–8	B_{0-7}	A	220	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2952A/Am2953A SWITCHING CHARACTERISTICS

The tables below define the Am2952/Am2953A switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with R_L on A_i and $B_i = 220\Omega$ and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7} ⌐¬	CPR		
B_{0-7} ⌐¬	CPS		
$\overline{CES}$ ⌐¬	CPS		
$\overline{CER}$ ⌐¬	CPR		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ⌐¬		
CPR ⌐¬		

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}		
$\overline{OE}BR$	B_{0-7}		

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	t_s	t_h
A_{0-7} ⌐¬	CPR		
B_{0-7} ⌐¬	CPS		
$\overline{CES}$ ⌐¬	CPS		
$\overline{CER}$ ⌐¬	CPR		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ⌐¬		
CPR ⌐¬		

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}		
$\overline{OE}BR$	B_{0-7}		

Am2952/Am2953 SWITCHING CHARACTERISTICS

The tables below define the Am2952/Am2953 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7} ⌐¬	CPR	7	5
B_{0-7} ⌐¬	CPS	7	5
$\overline{CES}$ ⌐¬	CPS	*19/15	4
$\overline{CER}$ ⌐¬	CPR	*19/15	4

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ⌐¬	*30/26	–
CPR ⌐¬	–	*30/26

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	22	27
$\overline{OE}BR$	B_{0-7}	22	27

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7} ⌐¬	CPR	11	8
B_{0-7} ⌐¬	CPS	11	8
$\overline{CES}$ ⌐¬	CPS	*20/15	4
$\overline{CER}$ ⌐¬	CPR	*20/15	4

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ⌐¬	*35/28	–
CPR ⌐¬	–	*35/28

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	24	28
$\overline{OE}BR$	B_{0-7}	24	28

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec.

Am2954/Am2955

Octal Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

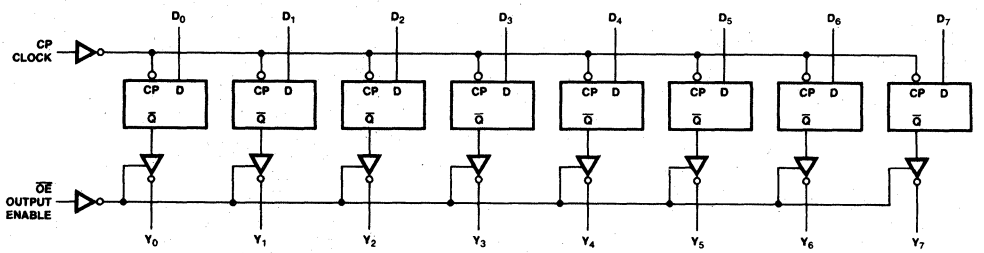
- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs; Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- High-speed — Clock to output 11 ns typical

GENERAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition. Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



BD002440

Inputs D_0 through D_7 are inverted on the Am2955.

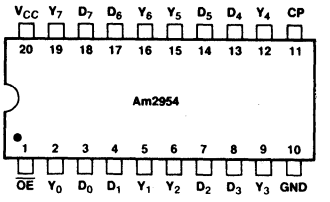
RELATED PRODUCTS

Part No.	Description
Am29821-26	8, 9, 10-Bit Registers
Am2918	Quad D-Register
Am2920	Quad D-Type Flip-Flop

03603B

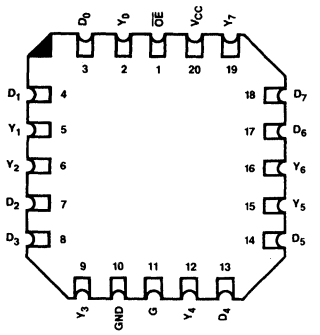
CONNECTION DIAGRAM
Top View

D-20, P-20, F-20*



CD004780

L-20-1

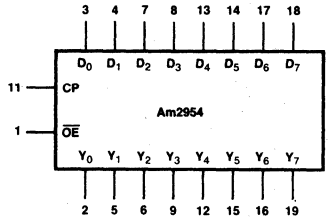


CD004580

Note: Pin 1 is marked for orientation

*F-20 pin configuration identical to D-20, P-20.

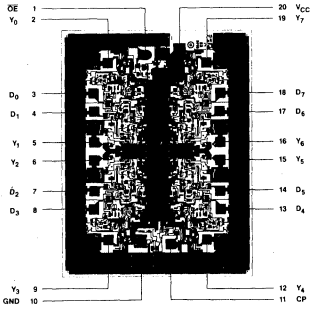
LOGIC SYMBOL



LS000970

Note: Inputs D_0 through D_7 are inverted on the Am2955

METALLIZATION AND PAD LAYOUT
Am2954



DIE SIZE 0.085″ x 0.110″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2954/2955 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 20-pin plastic DIP
  - X– Dice
- **Am2954/2955** — Device type: Octal Registers

Valid Combinations	
Am2954 Am2955	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

03603B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$D_i/\overline{D_i}$	I	The D flip-flop data inputs (Am2954, non-inverting/Am2955, inverting).
11	CP	I	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
	Yi	O	The register three-state outputs.
1	$\overline{OE}$	I	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

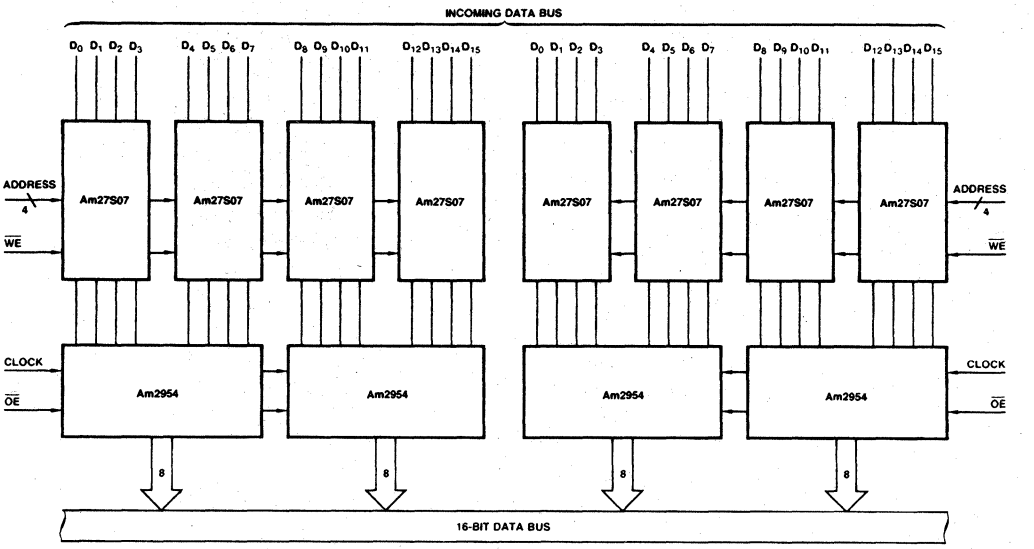
FUNCTION TABLE

Function	Inputs				Internal	Outputs
	$\overline{OE}$	Clock	Am2954 D_i	Am2955 D_i	Q_i	Y_i
H_i-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

APPLICATION



AF001870

Dual 16-word by 16-bit non-inverting high-speed data buffer.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL., I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IN}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IN}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

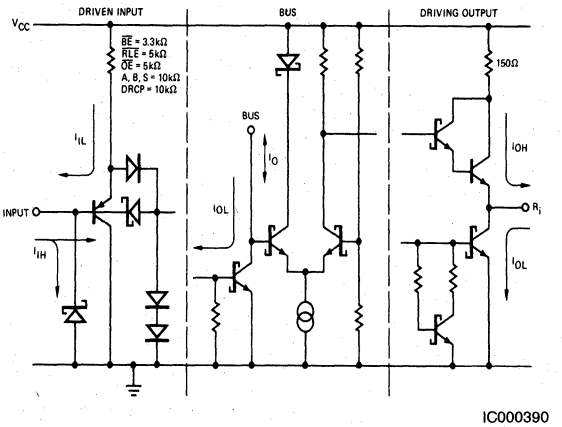
Notes: 1. For conditions shown as MIN or MAX use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH and all data inputs are LOW.
Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are $\overline{OE}$ = HIGH, and all data inputs are LOW.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Am2954 / Am2955 Min	Typ	Max	Units
t_{PLH}	Clock to Output, Y_i		C_L = 15pF R_L = 280Ω		8	15	ns
t_{PHL}					11	17	ns
t_{ZH}	$\overline{OE}$ to Y_i				8	15	ns
t_{ZL}					11	18	ns
t_{HZ}	$\overline{OE}$ to Y_i		C_L=5pF R_L = 280Ω		5	9	ns
t_{LZ}					7	12	ns
t_{PW}	Clock Pulse Width	HIGH	C_L = 15pF R_L = 280Ω	6			ns
		LOW		7.3			ns
t_S	Data to Clock			5			ns
t_H				2			ns
f_{max}	Maximum Clock Frequency (Note 1)			75	100		MHz

Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am2956/Am2957

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel latches
- Am2956 has non-inverting inputs
- Am2957 has inverting inputs
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- Hysteresis on latch enable input for improved noise margin
- 3-state outputs interface directly with bus organized systems

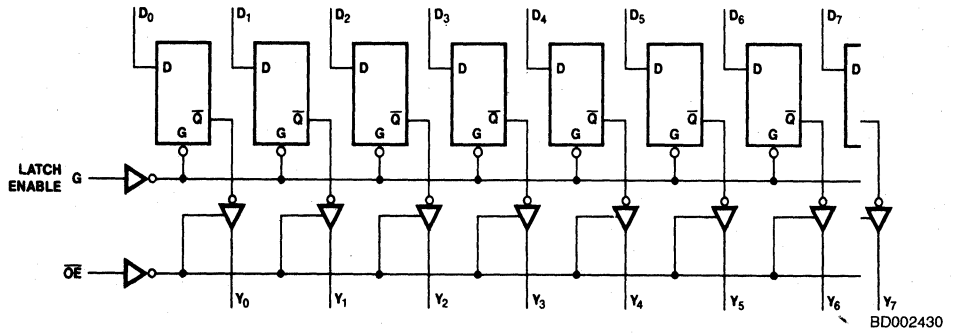
GENERAL DESCRIPTION

The Am2956 and Am2957 are octal latches with 3-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The Am2956 presents non-inverted data at the outputs while the Am2957 is inverting.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



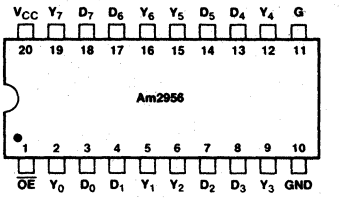
Inputs D_0 through D_7 are inverted on the Am2957.

RELATED PRODUCTS

Part No.	Description
Am29841-46	8, 9, 10-Bit Latches

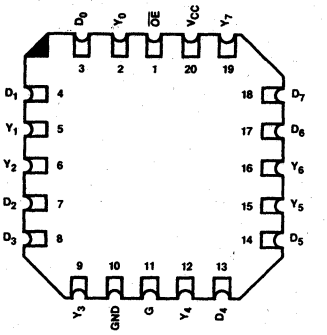
CONNECTION DIAGRAM
Top View

D-20, P-20



CD004570

L-20-1

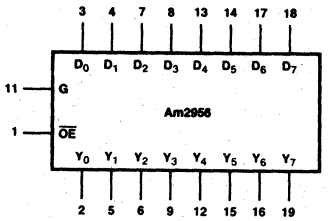


CD004580

Note: Pin 1 is marked for orientation

F-20 pin configuration identical to D-20, P-20.

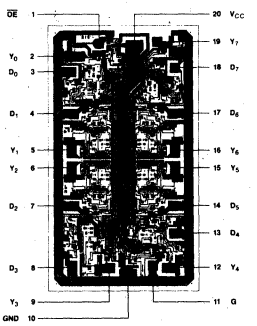
LOGIC SYMBOL



LS000980

Note: Inputs D_0 through D_7 are inverted on the Am2957

METALLIZATION AND PAD LAYOUT
Am2956



DIE SIZE 0.066″ x 0.119″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2956/2957 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am2956/2957** — Device type
  - Octal Latches with 3-State Outputs

Valid Combinations	
Am2956 Am2957	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$D_i/\overline{D_i}$	I	The latch data inputs (Am2956, non-inverting/Am2957, inverting).
11	G	I	The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Yi	O	The 3-state latch outputs.
1	$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

FUNCTION TABLES

Am2956

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

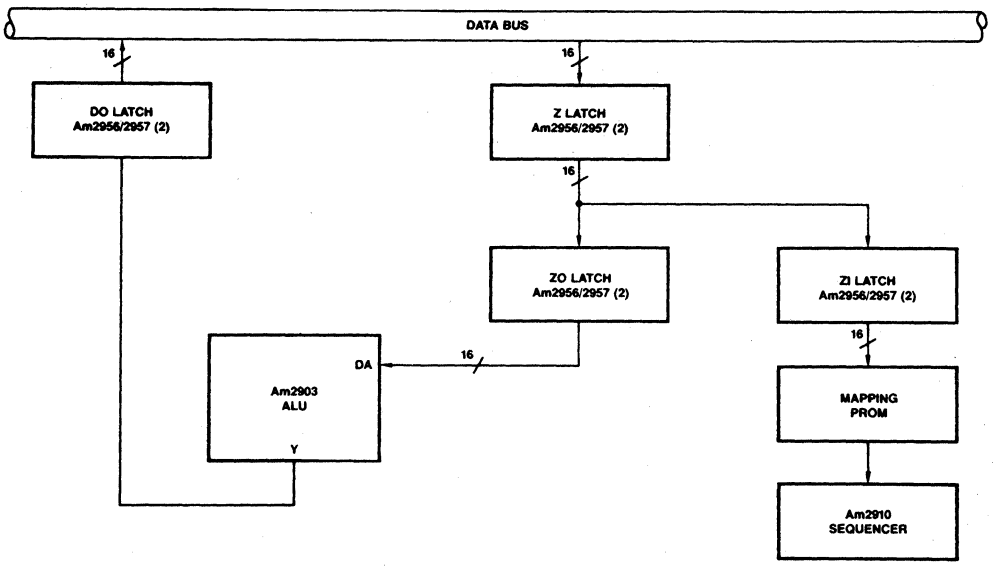
Am2957

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

APPLICATION



AF001880

Transparent Latches are used in high performance CPU designs. The Z Latch configuration shown provides overlapped fetch of machine instructions and operand data.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditons (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.46	Volts
				I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IN}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	2956	V_{CC} = MAX			105	160	mA
		2957				110	168	

Notes:1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX use the appropiate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V) Am2956

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Enable to Output	C_L = 15pF R_L = 280Ω		7	14	ns
t_{PHL}				12	18	ns
t_{PLH}	Data Input to Output			5	9	ns
t_{PHL}				9	13	ns
t_s(H)	HIGH Data to Enable		0			ns
t_s(L)	LOW Data to Enable		0			ns
t_h(H)	HIGH Data to Enable		10			ns
t_h(L)	LOW Data to Enable		10			ns
t_{pwH}	Enable Pulse Width		6			ns
t_{pwL}			7.3			ns
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns
t_{ZL}				11	18	ns
t_{HZ}	$\overline{OE}$ to Y_i	C_L = 5pF R_L = 280Ω		6	9	ns
t_{LZ}				8	12	ns

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

5

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V) Am2957

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Enable to Output	C_L = 15pF R_L = 280Ω		17	24	ns
t_{PHL}				19	26	ns
t_{PLH}	Data Input to Output			10	14	ns
t_{PHL}				14	20	ns
t_s(H)	HIGH Data to Enable		0			ns
t_s(L)	LOW Data to Enable		0			ns
t_h(H)	HIGH Data to Enable		10			ns
t_h(L)	LOW Data to Enable		10			ns
t_{pwH}	Enable Pulse Width		6			ns
t_{pwL}			7.3			ns
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns
t_{ZL}				11	18	ns
t_{HZ}	$\overline{OE}$ to Y_i	C_L = 5pF R_L = 280Ω		6	9	ns
t_{LZ}				8	10	ns

Am29203

Four-Bit Bipolar Microprocessor Slice

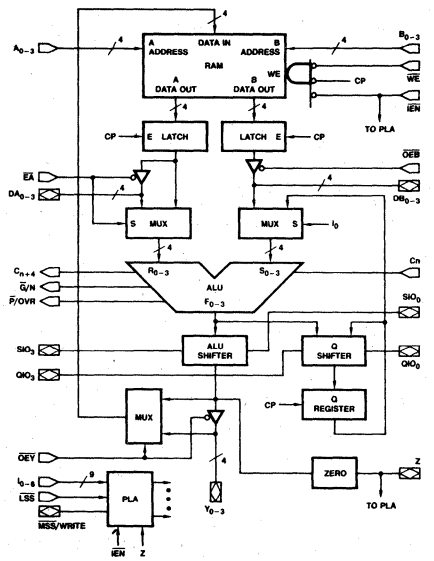
DISTINCTIVE CHARACTERISTICS

- **Expandable Register File –**
  The Am29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic –**
  Performing multiplication with the Am2901A requires a few external gates — these gates are contained on-chip in the Am29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- **Built-in Division Logic –**
  The Am29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic –**
  The mantissa and exponent of a floating-point number can be developed using a single microcycle per shift.
- **Built-in Parity Generation and Sign Extension Circuitry —**
  Can supply parity across the entire ALU outputs and provide sign-extension at any slice boundary.
- **BCD Arithmetic –**
  The Am29203 features automatic BCD add and subtract and conversion between binary and BCD.
- **Two Bidirectional Data Lines**
- **Improved I/O Capability –**
  Both the DA and DB data buses are bidirectional on the Am29203. In addition, the Y port is also bidirectional.

GENERAL DESCRIPTION

The Am29203 is a four-bit expandable bipolar microprocessor slice. The Am29203 performs all functions performed by the industry standard Am2901 and Am2903A, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am29203. In addition to its complete arithmetic and logic instruction set, the Am29203 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, BCD arithmetic and conversion, and other previously time-consuming operations. The Am29203 has three bidirectional ports and features AMD's ion-implanted micro-oxide (IMOX™) technology.

BLOCK DIAGRAM



BD002783

IMOX is a trademark of Advanced Micro Devices, Inc.

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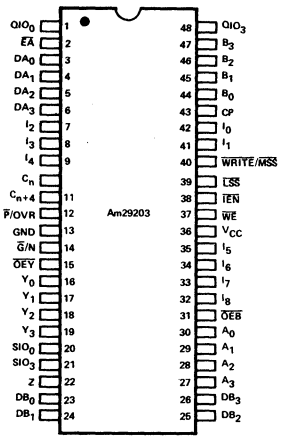
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-48



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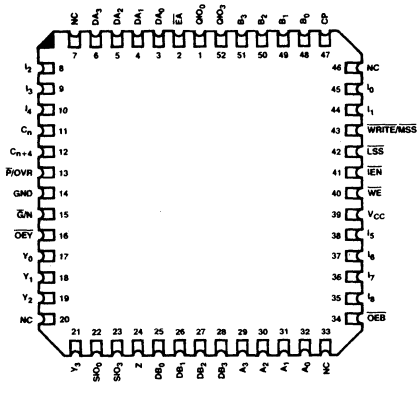
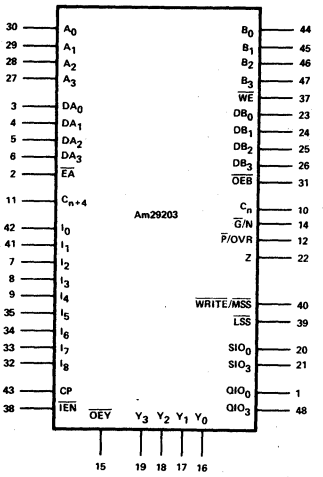
L-52-1



CD004501

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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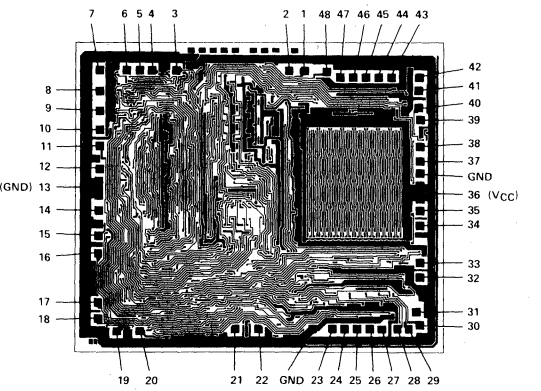
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163″ x 0.197″

Note: Pin numbers correspond to DIP package.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29203 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 48-pin CERDIP
  - F – 48-pin flatpak
  - L – 52-pin leadless chip carrier
  - X – Dice

Device type
Bipolar Microprocessor Slice

Valid Combinations	
Am29203	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917A	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am29707	Two-Port RAM
Am27S35	Registered PROM

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
	B_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
37	$\overline{WE}$	I	The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
	DA_{0-3}	I/O	A four-bit external data input which can be selected as one of the ALU operand sources; DA_0 is the least significant bit. On the AM29203, the DA path is bidirectional, operating as either an ALU source operand or as an external output for the RAM A-port.
2	$\overline{EA}$	I	A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
	DB_{0-3}	I/O	A four-bit external data input/output. Under control of the $\overline{OEB}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
31	$\overline{OEB}$	I	A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
10	C_n	I	The carry-in input to the AM29203 ALU.
	I_{0-8}	I	The nine instruction inputs used to select the Am29203 operation to be performed.
38	$\overline{IEN}$	I	The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am29203, $\overline{WRITE}$ is not affected by $\overline{IEN}$, but internally disables the RAM write enable.
11	Cn + 4	O	This output generally indicates the carry-out of the Am29203 ALU. Refer to Table 5 for an exact definition of this pin.
14	$\overline{G}$/N	O	A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
12	$\overline{P}$/OVR	O	A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
22	Z	I/O	An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
20, 21	SIO_0 SIO_3	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
1,48	QIO_0 QIO_3	I/O	Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.
39	$\overline{LSS}$	I	An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am29203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
40	$\overline{WRITE}$/ $\overline{MSS}$	I/O	When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
	Y_{0-3}	I/O	Four data inputs/outputs of the Am29203. Under control of the $\overline{OEY}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
15	$\overline{OEY}$	I	A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
43	CP	I	The clock input to the Am29203. The Q register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE Am29203

The Am29203 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am29203 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am29203 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OEB}$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port. On the Am29203, $\overline{EA}$ provides the same feature at the DA port.

External data at the Am29203 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto to Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am29203 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OEB}$ and I_0 inputs select RAM output port B, DB external data input, or the Q register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am29203 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the $\overline{EA}$, $\overline{OEB}$, and I_0 inputs.

TABLE 1. ALU OPERAND SOURCES

$\overline{EA}$	I_0	$\overline{OEB}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	Ram Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	Ram Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW
H = HIGH
X = Don't Care

TABLE 2. Am29203 ALU FUNCTIONS

I_4	I_3	I_2	I_1	I_0	ALU Functions
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	F = S Minus R Minus 1 Plus C_n
L	L	H	L	X	F = R Minus S Minus 1 Plus C_n
L	L	H	H	X	F = R Plus S Plus C_n
L	H	L	L	X	F = S Plus C_n
L	H	L	H	X	F = $\overline{S}$ Plus C_n
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	F = R Plus C_n
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	F = $\overline{R}$ Plus C_n
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	F_i = $\overline{R_i}$ AND S_i
H	L	H	L	X	F_i = R_i EXCLUSIVE NOR S_i
H	L	H	H	X	F_i = R_i EXCLUSIVE OR S_i
H	H	L	L	X	F_i = R_i AND S_i
H	H	L	H	X	F_i = R_i NOR S_i
H	H	H	L	X	F_i = R_i NAND S_i
H	H	H	H	X	F_i = R_i OR S_i

L = LOW
H = HIGH
i = 0 to 3
X = LOW or HIGH

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am29203 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am29203 executes instructions other than the 16 special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Am29203s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am29203s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, G, and carry propagate, P, signals required for a lookahead carry scheme are generated by the Am29203 and are available as outputs of the least significant and intermediate slices.

The Am29203 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am29203 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am29203 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am29203 applications section for a more detailed description of the Am29203 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am29203 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations;

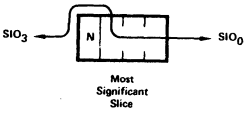
however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am29203. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q register.

The Q register and shifter are controlled by the instruction inputs. Table 4 defines the Am29203 special functions and the operations which the Q register and shifter perform for each. When the Am29203 executes instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the Q register and shifter operation as a function of these four bits.

Figure A.

Am29203 Arithmetic Shift Path



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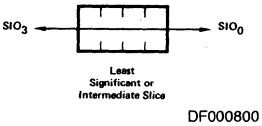

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Am29203 Logical Shift Path

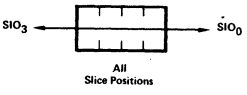

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TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, IEN = LOW

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{WRITE}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \nabla F_2 \nabla F_1 \nabla F_0 \nabla SIO_3$
∇ = Exclusive OR
L = LOW
H = HIGH
Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTONS (Note 7)

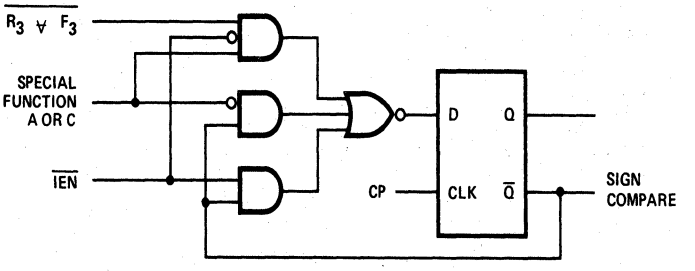
(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig/ Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function		QIO_3	QIO_0	$\overline{WRITE}$
0	L	0	Unsigned Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/ 2 → Q	Input		Q_0	L
1	L	0	BCD to Binary Conversion	(Note 4)	Log F/2 → Y	Input	Input	F_0	Log Q/ 2 → Q	Input		Q_0	L
1	H	0	Multiprecision BCD to Binary	(Note 4)	Log F/2 → Y	Input	Input	F_0	HOLD	Z		Q_0	L
2	L	0	Two's Complement Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/ 2 → Q	Input		Q_0	L
3	L	0	Decrement by One or Two	F = S − 2 + C_n	F → Y	Z	Z	Parity	Hold	Z		Z	L
4	L	0	Increment by One or Two	F = S + 1 + C_n	F → Y	Input	Input	Parity	Hold	Z		Z	L
5	L	0	Sign/Magnitude Two's Complement	F = S + C_n if Z = L F = $\overline{S}$ + C_n if Z = H	F → Y (Note 3)	Input	Input	Parity	Hold	Z		Z	L
6	L	0	Two's Complement Multiply, Last Cycle	F = S + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/ 2 → Q	Input		Q_0	L
7	L	0	BCD Divide by Two	(Note 4)	F → Y	Z	Z	Parity	Hold	Z		Z	L
8	L	0	Single Length Normalize	F = S + C_n	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3		Input	L
9	L	0	Binary to BCD Conversion	(Note 5)	Log 2F → Y	F_3	F_3	Input	Log 2Q → Q	Q_3		Input	L
9	H	0	Multiprecision Binary to BCD	(Note 5)	Log 2F → Y	F_3	F_3	Input	Hold	Z		Input	L
A	L	0	Double Length Normalize and First Divide Op	F = S + C_n	Log 2F → Y	$R_3 \nabla F_3$	F_3	Input	Log 2Q → Q	Q_3		Input	L
B	L	0	BCD Add	F = R + S + C_nBCD (Note 6)	F → Y	0	0	Z	Hold	Z		Z	L
C	L	0	Two's Complement Divide	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log 2F → Y	$\overline{R_3 \nabla F}$	F_3	Input	Log 2Q → Q	Q_3		Input	L
D	L	0	BCD Subtract	F = R − S − 1 + C_n BCD (Note 6)	F → Y	0	0	Z	Hold	Z		Z	L
E	L	0	Two's Complement Divide Correction and Remainder	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3		Input	L
F	L	0	BCD Subtract	F = S − R − 1 + C_n BCD (Note 6)	F → Y	0	0	Z	Hold	Z		Z	L

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \nabla$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \nabla F_3$ is generated at the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8 and F = S minus 3 if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5 and F = S plus 3 if magnitude of S_{0-3} is 5 or greater. Addition is module 16.
6. Additions and subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.

L = LOW
H = HIGH
X = Don't Care

Hi-Z = High Impedance
∇ = Exclusive OR
Parity = $SIO_3 \nabla F_3 \nabla F_2 \nabla F_1 \nabla F_0$

Figure B. Sign Compare Flip-Flop



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The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Output Buffers

The DB, DA, and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls.

The Y output buffers are enabled when the $\overline{OEY}$ input is LOW and are in the high impedance state when $\overline{OEY}$ is HIGH. The DB output buffers are enabled when the $\overline{OEB}$ input is LOW and the DA buffers are enabled when $\overline{EA}$ is LOW.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am29203 instructions. On the Am29203, the Z pin will be HIGH if $\overline{OEY}$ is HIGH, allowing zero detection on less than the full word.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}$/$\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am29203 instruction inputs.

On the Am29203, when $\overline{IEN}$ is HIGH, the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the Q register and Sign Compare Flip-Flop can be written according to the Am29203 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am29203 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am29203 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}$/$\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}$/$\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}$/$\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{W}$/$\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{W}$/$\overline{MSS}$ and $\overline{LSS}$ should not be connected together.

Am29203 SPECIAL FUNCTIONS

The Am29203 provides 16 Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD add, subtract, and divide by two.
- Single-and double-precision BCD to Binary and Binary to BCD conversion.

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am29203. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

The BCD arithmetic special functions can be used to add or subtract two BCD numbers and generate a valid BCD result in one microcycle. In addition a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions facilitate single- and double-precision algorithms to convert from BCD to Binary and from Binary to BCD.

Refer to Am29203 applications section for a more detailed description of these Special Functions.

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (I = 0 to 3)	Pi (I = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		X ($\overline{OEY}$ = L)		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig. Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	1	X	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	2	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	5	X	0	$\overline{S_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	7	X	0	$\overline{R_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	8	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	9	X	$\overline{R_i} \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	B	X	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	D	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
X	F	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C+4$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
1	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	(Note 7)	$G \vee PC_n$	$C_{n+3} \nabla C_{N+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \nabla C_{N+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
5	0	L	0	$\overline{S_j}$ if Z = L $\overline{S_i}$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \nabla S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$\overline{S_j}$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
8	0	L	0	S_i	(Note 3)	$Q_2 \nabla Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$
9	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$
9	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$	$\overline{Q_0}$ $\overline{Q_1}$ $\overline{Q_2}$ $\overline{Q_3}$
A	0	L	0	S_i	(Note 4)	$F_2 \nabla F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	(Note 8)	(Note 8)	(Note 9)	(Note 9)	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
C	0	L	$\overline{R_j} \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	$R_i \wedge \overline{S_i}$	$R_i \vee \overline{S_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$
E	0	L	$\overline{R_j} \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$	$\overline{Y_0}$ $\overline{Y_1}$ $\overline{Y_2}$ $\overline{Y_3}$

Notes:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \nabla Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \nabla F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{F_0}\ \overline{F_1}\ \overline{F_2}\ \overline{F_3}$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On all slices $\overline{P} = (\overline{P_0} + \overline{P_3})\ (\overline{P_0} + \overline{G_2})\ (\overline{P_0} + \overline{G_1} + \overline{P_2})$.
9. On all slices $\overline{G} = \overline{G_3}\ (\overline{G_0} + \overline{G_1} + \overline{P_2})\ (\overline{G_0} + \overline{G_1})\ (\overline{P_1} + \overline{G_2})\ (\overline{P_3} + \overline{P_1} \cdot \overline{P}_2 \cdot \overline{G_0})$.

L = LOW = 0
H = HIGH = 1
V = OR
$\wedge$ = AND
∇ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

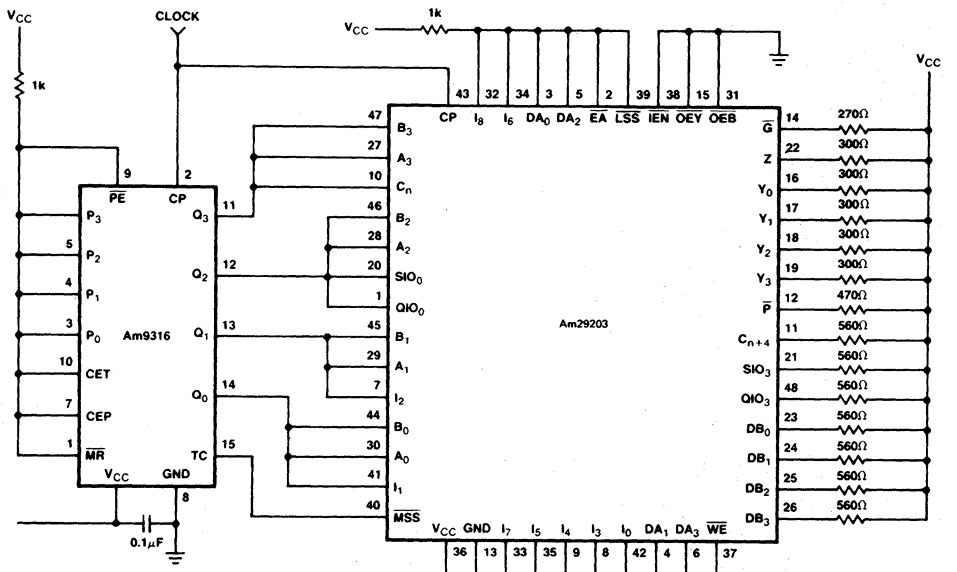
Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0-Y_3,$\overline{G}$/N	2.4			Volts
				I_{OH} = −800μA DB_{0-3},$\overline{P}$/OVR SIO_0,SIO_3,QIO_0,QIO_3, $\overline{WRITE}$, C_{n+4}	2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN, V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_0,Y_1,Y_2 Y_3,Z	I_{OL} = 20mA(COM'L)			0.5	Volts
				I_{OL} = 16mA(MIL)				
			DB_0,DB_1, DB_2,DB_3	I_{OL} = 12mA(COM'L)			0.5	
				I_{OL} = 8.0mA(MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4},$\overline{WRITE}$ SIO_3,QIO_0 QIO_3,SIO_0	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V (Note 4)		C_n			−3.6	mA
				Y_0,Y_1,Y_2,Y_3			−1.13	
				I_0,I_1,I_2,I_3,I_4 DA_0,DA_1,DA_2,DA_3			−0.72	
				SIO_0,SIO_3,QIO_0,$\overline{MSS}$ QIO_3,DB_0,DB_1, DB_2,DB_3			−0.77	
				All other inputs			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V (Note 4)		C_n			200	μA
				Y_0,Y_1,Y_2,Y_3			110	
				I_0-I_4,DA_0-DA_3			40	
				SIO_0,SIO_3,$\overline{MSS}$ QIO_3,DB_{0-3}, QIO_0			90	
				All other inputs			20	

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX, (Note 4)	$Y_0 - Y_3$	V_O = 2.4V			110	μA
				V_O = 0.5V			-1130	
			DB_{0-3},QIO_0,QIO_3 SIO_0,SIO_3,$\overline{WRITE}$/$\overline{MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			-770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			-30		-85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	COM'L	T_A = 0 to 70°C			350	mA
				T_A = 70°C			291	
			MIL	T_C = -55 to 125°C			395	
				T_C = 125°C			258	

Notes:

1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC}=5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$, and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worse case I_{CC} is at minimum temperature.
6. Three input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

Am29203 Burn-in and Life Test Circuit



V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am29203s.

TC001520

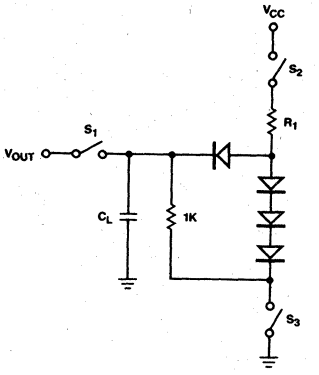
Notes on Testing

Incoming test procedures on this device should be carefully planned taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing AMD, offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

SWITCHING TEST CIRCUIT

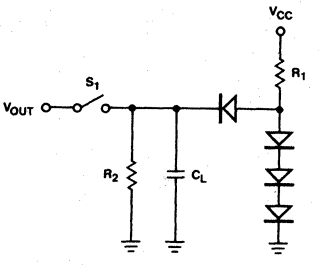
A. THREE-STATE OUTPUTS



TC001430

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS

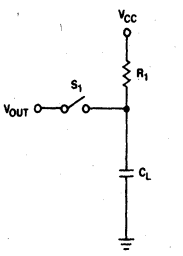


TC001380

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



TC001420

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function test and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am29203

Pin#	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16–19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23–26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Am290203 GUARANTEED COMMERCIAL RANGE PERFORMACE

The Am290203 switching characteristics are a function of the power supply voltage, the temperature, and the operating mode of the devices. The data has been condensed onto the tables below.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable To
A	Clock and Write Pulse	4.75 to 5.25V, 0 to 70°C	All Functions
B	Enable/Disable Times	4.75 to 5.25V, 0 to 70°C	All Functions
C	Setup and Hold Times	4.75 to 5.25V, 0 to 70°C	All Functions
I-2	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Standard and Increment/Decrement by 1 or 2
I-3	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Multiply Instructions
I-4	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Divide Instructions
I-5	Combinational Delays	4.75 to 5.25V, 0 to 70°C	BCD Instructions
I-6	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Sign Magnitude to Two's Complement Conversion
I-7	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Single Length Normalization

Am29203 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am29203 over the commercial operating range of 0 to + 70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE A. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Time CP and $\overline{WE}$ both LOW to Write	15ns

TABLE B. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
$\overline{OEY}$	Y	25	21
$\overline{OEB}$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
I_{8765}	QIO	38	38
I_{43210}	QIO	38	38
$\overline{LSS}$	$\overline{WR}$	25	21

Note: C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

COMBINATIONAL PROPAGATION DELAYS
C_L = 50pF
1-2 STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS

	To											
From	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA, DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	67	55	52	74	64	71	30	–	–	44	62	84
DA, DB	58	50	44	65	54	60	–	–	–	35	59	68
C_n	30	18	–	35	26	26	–	–	–	21	27	40
I_{8-0}	64	64	50	72	59	62	–	34	26	48	62	74
CK	58	42	43	61	54	60	21	–	21	35	54	65
$\overline{MSS}$	33	–	41	40	36	44	–	–	–	40	40	44
$SIO_{0,3}$	23	–	–	29	–	–	–	–	–	–	29	19

TABLE C. SET-UP AND HOLD TIMES ALL FUNCTIONS

		HIGH-to-LOW		LOW-to-HIGH		
		Tpwl				
From	**With Respect to**	**Set-up**	**Hold**	**Set-up**	**Hold**	**Comments**
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q
$\overline{WE}$ HIGH	CP	15	Tpwl		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
I_{8765}	CP	28	Tpwl		0	
$\overline{IEN}$ HIGH	CP	24	Tpwl		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
I_{43210}	CP	24	Tpwl		0	

Note: 1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OEY}$ = 0).

1-5 BCD INSTRUCTIONS (SF 1, SF 7, SF 9, SF B, SF D, SF F)

	To											
From	**Slice**	**Y**	**C_{n+4}**	**$\overline{G}$, $\overline{P}$**	**Z**	**N**	**OVR**	**DA DB**	**$\overline{WR}$**	**QIO**	**SIO_0**	**SIO_3**	**SIO Parity**
A, B Addr	MSS	77	55	–	72	68	68	30	–	–	44	62	84
	IS	77	55	61	72	–	–	30	–	–	44	62	84
	LSS	77	55	61	72	–	–	30	–	–	44	62	84
DA, DB	MSS	61	50	–	65	58	59	–	–	–	35	59	68
	IS	61	50	49	65	–	–	–	–	–	35	59	68
	LSS	61	50	49	65	–	–	–	–	–	35	59	68
C_n	MSS	36	23	–	35	33	33	–	–	–	29	34	40
	IS	36	23	–	35	–	–	–	–	–	29	34	40
	LSS	36	23	–	35	–	–	–	–	–	29	34	40
I_{8-0}	MSS	72	64	–	72	59	62	–	–	26	48	62	74
	IS	72	64	60	72	–	–	–	–	26	48	62	74
	LSS	72	64	60	72	–	–	–	34	26	48	62	74
CK	MSS	68	52	–	68/29[1]	64	60	21	–	21	35	54	65
	IS	68	52	55	68/29[1]	–	–	21	–	21	35	54	65
	LSS	68	52	55	68/29[1]	–	–	21	–	21	35	54	65
Z	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–	–

Note 1: Binary to BCD and multiprecision Binary to BCD Instructions only.

BCD to Binary conversion (SF 1)
BCD divide by two (SF 7)
Binary to BCD conversion (SF 9)
BCD add (SF B)
BCD substract (SF D, SF F)

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
1-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO_0	SIO_0	SIO Parity
A, B Addr	MSS	67	55	–	–	64	71	30	–	–	44	–
	IS	67	55	52	–	–	–	30	–	–	44	–
	LSS	67	55	52	–	–	–	30	–	–	44	–
DA, DB	MSS	59	50	–	–	54	60	–	–	–	35	–
	IS	58	50	44	–	–	–	–	–	–	35	–
	LSS	58	50	44	–	–	–	–	–	–	35	–
C_n	MSS	34	18	–	–	26	26	–	–	–	21	–
	IS	30	18	–	–	–	–	–	–	–	21	–
	LSS	30	18	–	–	–	–	–	–	–	21	–
I_{8-0}	MSS	104	76	–	–	90	96	–	–	26	68	–
	IS	91	76	74	–	–	–	–	–	26	68	–
	LSS	91	76	74	31	–	–	–	34	26	68	–
CK	MSS	62	42	–	–	54	60	21	–	21	35	–
	IS	58	42	43	–	–	–	21	–	21	35	–
	LSS	95	79	79	29	–	–	21	–	21	71	–
Z	MSS	72	50	–	–	64	64	–	–	–	42	–
	IS	66	50	50	–	–	–	–	–	–	42	–
	LSS	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–

Unsigned Multiply

SF 0: F = S + Cn if Z = L
F = S + R + Cn if Z = H
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply

SF 2: F = S + Cn if Z = L
F = R + S + Cn if Z = H
$Y_3 = F_3 \nabla$ OVR (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle

SF 6: F = S + Cn if Z = L
F = S – R – 1 + Cn if Z = H
Y_3 = OVR ∇ F_3 (MSS)
$Z = Q_0$ (LSS)

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
1-2 STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF 3 and SF 4)

From	To: Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA, DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	67	55	52	74	64	71	30	–	–	44	62	84
DA, DB	58	50	44	65	54	60	–	–	–	35	59	68
C_n	30	18	–	35	26	26	–	–	–	21	27	40
I_{8-0}	64	64	50	72	59	62	–	34	26	48	62	74
CK	58	42	43	61	54	60	21	–	21	35	54	65
$\overline{MSS}$	33	–	41	40	36	44	–	–	–	40	40	44
$SIO_{0,3}$	23	–	–	29	–	–	–	–	–	–	29	19

Decrement SF3: F = S – 2 + C_n Increment SF4: F = S + 1 + C_n

Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1-6 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

From	Slice	To: Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO	$\overline{SIO}$	SIO_0 Parity
A,B Addr	MSS	98	88	–	42	97	104	30	–	–	–	132
	IS	67	55	52	–	–	–	30	–	–	–	84
	LSS	67	55	52	–	–	–	30	–	–	–	84
DA, DB	MSS	93	83	–	37	92	99	–	–	–	–	127
	IS	58	50	44	–	–	–	–	–	–	–	68
	LSS	58	50	44	–	–	–	–	–	–	–	68
C_n	MSS	30	18	–	–	29	26	–	–	–	–	40
	IS	30	18	–	–	–	–	–	–	–	–	40
	LSS	30	18	–	–	–	–	–	–	–	–	40
I_{8-0}	MSS	89	73	–	28	91	84	–	–	–	–	118
	IS	86	73	72	–	–	–	–	–	–	–	96
	LSS	86	73	72	–	–	–	–	34	–	–	96
CK	MSS	96	82	–	36	89	98	21	–	–	–	126
	IS	58	42	43	–	–	–	21	–	–	–	65
	LSS	58	42	43	–	–	–	21	–	–	–	65
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	62	46	44	–	–	–	–	–	–	–	90
	LSS	62	46	44	–	–	–	–	–	–	–	90
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–	–

SF 5:
F = $\overline{S} + C_n$ if Z = L
F = $\overline{S} + C_n$ if Z = H
Y_3 = $S_3 \nabla F_3$ (MSS)
Z = S_3 (MSS)

03594B

Refer to Page 13-1 for Essential Information on Military Devices

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
1-7 SINGLE LENGTH NORMALIZATION (SF 8)

From	To: Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO_3	SIO_3	SIO Parity
A,B Addr	MSS	67	–	–	–	–	–	30	–	–	62	–
	IS	67	55	52	–	–	–	30	–	–	62	–
	LSS	67	55	52	–	–	–	30	–	–	62	–
DA, DB	MSS	58	–	–	–	–	–	–	–	–	59	–
	IS	58	50	44	–	–	–	–	–	–	59	–
	LSS	58	50	44	–	–	–	–	–	–	59	–
C_n	MSS	30	–	–	–	–	–	–	–	–	27	–
	IS	30	18	–	–	–	–	–	–	–	27	–
	LSS	30	18	–	–	–	–	–	–	–	27	–
I_{0-5}	MSS	55	46	–	29	24	25	–	–	26	60	–
	IS	52	50	30	29	–	–	–	–	26	54	–
	LSS	52	50	30	29	–	–	–	34	26	54	–
CK	MSS	58	26	–	29	23	27	21	–	21	54	–
	IS	58	42	43	29	–	–	21	–	21	54	–
	LSS	58	42	43	29	–	–	21	–	21	54	–
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–	–

SF 8:
F = $S + C_n$
N = Q_3(MSS)
C_{n+4} = $Q_3 \nabla Q_2$(MSS)
OVR = $Q_2 \nabla Q_1$(MSS)
Z = $\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$

Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1–4 DIVIDE INSTRUCTIONS (SF A, SF C, SF E)

From		To										
	Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_3	$\overline{WR}$	SIO Parity
A, B Addr	MSS	67	55/60[1]	–	74	64	71	30	–	–	62	–
	IS	67	55	52	74	–	–	30	–	–	62	–
	LSS	67	55	52	74	–	–	30	–	–	62	–
DA, DB	MSS	58	50/55[1]	–	65	54	60	–	–	–	59	–
	IS	58	50	44	65	–	–	–	–	–	59	–
	LSS	58	50	44	65	–	–	–	–	–	59	–
C_n	MSS	30	18/41[1]	–	35	26	26	–	–	–	30/27[1]	–
	IS	30	18	–	35	–	–	–	–	–	27	–
	LSS	30	18	–	35	–	–	–	–	–	27	–
I_{8-0}	MSS	80/55[1]	75	–	47[1]/31[2]	77	77	–	–	26	90/71[1]	–
	IS	80/55[1]	75	–	47[1]	–	–	–	–	26	85/52[1]	–
	LSS	80/55[1]	75	–	47[1]	–	–	–	34	26	85/52[1]	–
CK	MSS	58[1]/89[2]	50[1]/73[2]	–	61[1]/29[2]	54[1]/92[2]	60[1]/92[2]	21	–	21	87[2]/54[1]	–
	IS	58	42	43	61[1]	–	–	21	–	21	54	–
	LSS	58	42	43	61[1]	–	–	21	–	21	54	–
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	61	44	46	–	–	–	–	–	–	58	–
	LSS	61	44	46	–	–	–	–	–	–	58	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–

Notes:
1. Only 1st divide and normalization.
2. Only two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op

SF A:

$F = S + CN$
$N = F_3$ (MSS)
$SIO_3 = F_3 \nabla R_3$ (MSS)
$C_{n+4} = F_3 \nabla F_2$ (MSS),
$OVR = F_2 \nabla F_1$ (MSS)
$Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

Two's Complement Divide

SF C:

$F = R + S + Cn$ if $Z = L$
$F = S - R - 1 + Cn$ if $Z = H$
$SIO_3 = \overline{F_3 \nabla R_3}$ (MSS)
$Z = \overline{F_3 \nabla R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder

SF E:

$F = R + S + Cn$ if $Z = L$
$F = S - R - 1 + Cn$ if $Z = H$
$Z = \overline{F_3 \nabla R_3}$ (MSS) from previous cycle

Am29803A

16-Way Branch Control Unit

DISTINCTIVE CHARACTERISTICS

- 16 separate instructions – 2, 4, 8 or 16-way branch in one microprogram execution cycle
- Four individual test inputs
- Advanced Low-Power Schottky processing
- Four individual outputs for driving the four OR inputs on the Am2909A Microprogram Sequencer
- Provides maximum branch capability in a microprogram control unit using the Am2909

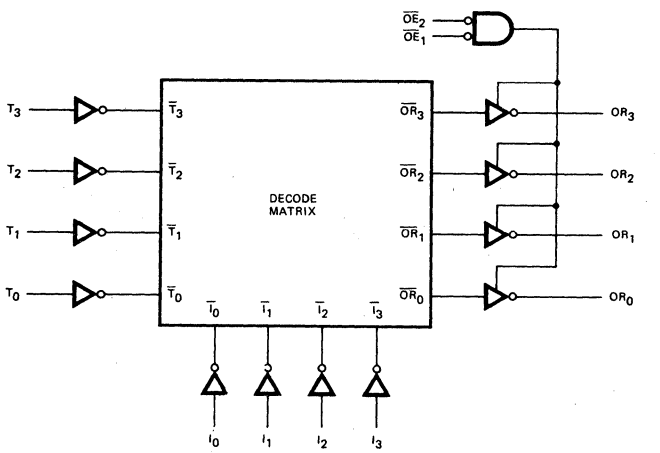
GENERAL DESCRIPTION

The Am29803A is a Low-Power Schottky processed device that provides 16-way branch control when used in conjunction with the Am2909A Microprogram Sequencer.

The device features 16 instructions that provide all combinations of simultaneous testing of four different inputs. The device has four outputs that are used to drive the four OR inputs of the Am2909A Microprogram Sequencer.

The "zero" instruction inhibits the testing of any of the four test (T) inputs. The remaining 15 instructions are used to test combinations of 1, 2, 3 or 4 of the T inputs simultaneously. If one T input is being tested, the Am29803A will select one of two possible addresses. If two T inputs are being tested, the device will select one of four possible addresses. If three T inputs are being tested, the device will select one of eight possible addresses. If all four T inputs are being tested, the device will select one of sixteen addresses as the field used to drive the OR inputs of the Am2909A.

BLOCK DIAGRAM



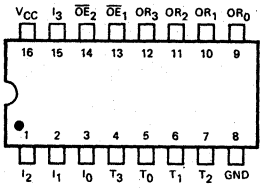
BD002570

03648A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D16
P16
F-16*

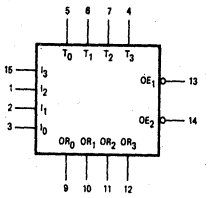


CD004790

*F-16 pin configuration identical to D-16, P16.

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS001080

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29803A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
- **Am29803A** — Device type
  - 16-Way Branch Control Unit

Valid Combinations	
Am29803A	PC DC, DCB, DMB FMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 2 1, 15	I_0, I_1, I_2, I_3	I	The four instruction inputs to the device.
5, 6 7, 4	T_0, T_1, T_2, T_3	I	The four test inputs for the device.
9, 10, 11, 12	OR_0, OR_1 OR_2, OR_3	O	The four outputs of the device that are connected to the four OR inputs of the Am2909.
13, 14	$\overline{OE}_1$, $\overline{OE}_2$	I	Output Enable. When either $\overline{OE}$ input is HIGH, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the OR outputs are enabled and the selected data will be present.

GUARANTEED LOADING RULES

OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/ Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	I_2	0.5	–	–	–
2	I_1	0.5	–	–	–
3	I_0	0.5	–	–	–
4	T_3	0.5	–	–	–
5	T_0	0.5	–	–	–
6	T_1	0.5	–	–	–
7	T_2	0.5	–	–	–
8	GND	–	–	–	–
9	OR_0	–	100	44	44
10	OR_1	–	100	44	44
11	OR_2	–	100	44	44
12	OR_3	–	100	44	44
13	$\overline{OE}_1$	0.5	–	–	–
14	$\overline{OE}_2$	0.5	–	–	–
15	I_3	0.5	–	–	–
16	V_{CC}	–	–	–	–

FUNCTION TABLE

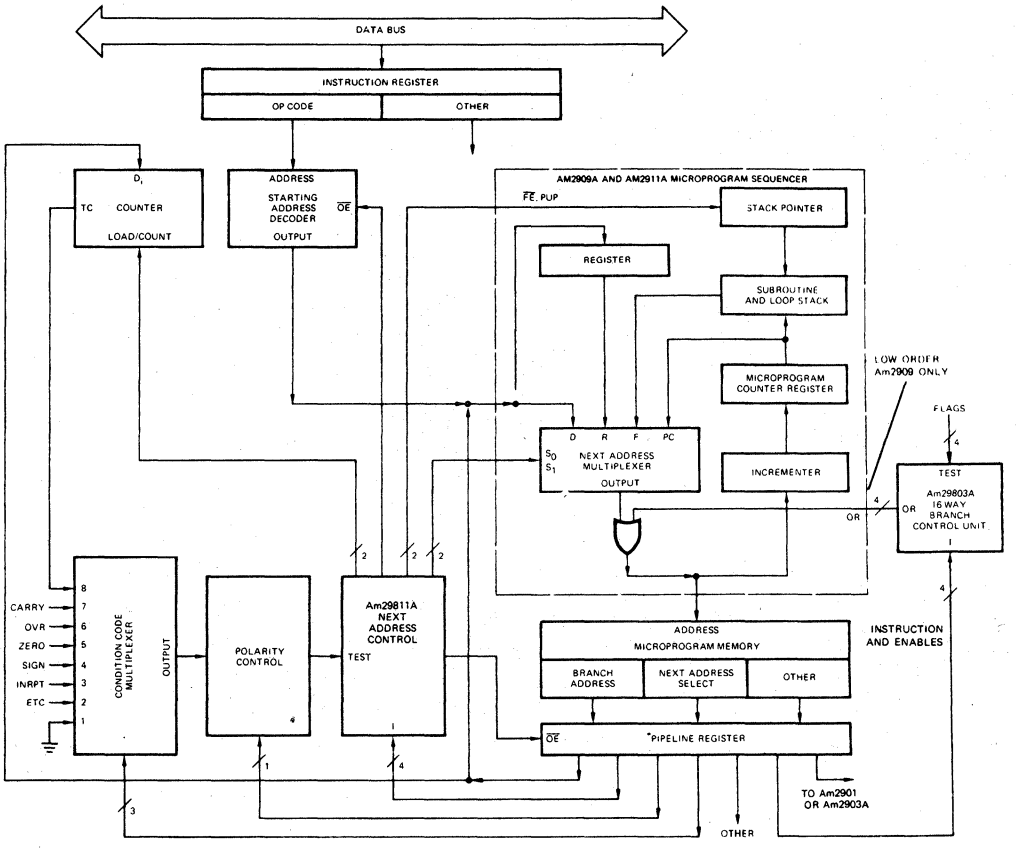
Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X	X	X	L	L	L	L	L
					X	X	X	H	L	L	L	H
Test T_1	L	L	H	L	X	X	L	X	L	L	L	L
					X	X	H	X	L	L	L	H
Test T_0 & T_1	L	L	H	H	X	X	L	L	L	L	L	L
					X	X	L	H	L	L	L	H
					X	X	H	L	L	L	H	L
					X	X	H	H	L	L	H	H
Test T_2	L	H	L	L	X	L	X	X	L	L	L	L
					X	H	X	X	L	L	L	H
Test T_0 & T_2	L	H	L	H	X	L	X	L	L	L	L	L
					X	L	X	H	L	L	L	H
					X	H	X	L	L	L	H	L
					X	H	X	H	L	L	H	H
Test T_1 & T_2	L	H	H	L	X	L	L	X	L	L	L	L
					X	L	H	X	L	L	L	H
					X	H	L	X	L	L	H	L
					X	H	H	X	L	L	H	H
Test T_0, T_1 & T_2	L	H	H	H	X	L	L	L	L	L	L	L
					X	L	L	H	L	L	L	H
					X	L	H	L	L	L	H	L
					X	L	H	H	L	L	H	H
					X	H	L	L	L	H	L	L
					X	H	L	H	L	H	L	H
					X	H	H	L	L	H	H	L
					X	H	H	H	L	H	H	H
Test T_3	H	L	L	L	L	X	X	X	L	L	L	L
					H	X	X	X	L	L	L	H
Test T_0 & T_3	H	L	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					H	X	X	L	L	L	H	L
					H	X	X	H	L	L	H	H
Test T_1 & T_3	H	L	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					H	X	L	X	L	L	H	L
					H	X	H	X	L	L	H	H
Test T_0, T_1 & T_3	H	L	H	H	L	X	L	L	L	L	L	L
					L	X	L	H	L	L	L	H
					L	X	H	L	L	L	H	L
					L	X	H	H	L	L	H	H
					H	X	L	L	L	H	L	L
					H	X	L	H	L	H	L	H
					H	X	H	L	L	H	H	L
					H	X	H	H	L	H	H	H
Test T_2 & T_3	H	H	L	L	L	L	X	X	L	L	L	L
					L	H	X	X	L	L	L	H
					H	L	X	X	L	L	H	L
					H	H	X	X	L	L	H	H
Test T_0, T_2 & T_3	H	H	L	H	L	L	X	L	L	L	L	L
					L	L	X	H	L	L	L	H
					L	H	X	L	L	L	H	L
					L	H	X	H	L	L	H	H
					H	L	X	L	L	H	L	L
					H	L	X	H	L	H	L	H
					H	H	X	L	L	H	H	L
					H	H	X	H	L	H	H	H
Test T_1, T_2 & T_3	H	H	H	L	L	L	L	X	L	L	L	L
					L	L	H	X	L	L	L	H
					L	H	L	X	L	L	H	L
					L	H	H	X	L	L	H	H
					H	L	L	X	L	H	L	L
					H	L	H	X	L	H	L	H
					H	H	L	X	L	H	H	L
					H	H	H	X	L	H	H	H

FUNCTION TABLE (Cont.)

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
Test T_0, T_1, T_2 & T_3	H	H	H	H	L	L	L	L	L	L	L	L
					L	L	L	H	L	L	L	H
					L	L	H	L	L	L	H	L
					L	L	H	H	L	L	H	H
					L	H	L	L	L	H	L	L
					L	H	L	H	L	H	L	H
					L	H	H	L	L	H	H	L
					L	H	H	H	L	H	H	H
					H	L	L	L	H	L	L	L
					H	L	L	H	H	L	L	H
					H	L	H	L	H	L	H	L
					H	L	H	H	H	L	H	H
					H	H	L	L	H	H	L	L
					H	H	L	H	H	H	L	H
					H	H	H	L	H	H	H	L
					H	H	H	H	H	H	H	H

H = HIGH
L = LOW
X = Don't care

APPLICATION



AF001831

A typical computer control unit using the Am2909, Am2911, Am29803A and Am29811A. Note that the least significant microprogram sequencer is an Am2909 and the more significant sequencers are Am2911's.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX			95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS1}}$ = 2.4V	V_O = 4.5V			40	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = MHz (Note 3)			8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH} t_{PHL}	I_i to OR_i	C_L = 15pF R_L = 2.0kΩ		25	35	ns
t_{PLH} t_{PHL}	T_i to OR_i			25	35	ns
t_{ZH} t_{ZL}	$\overline{OE}_i$ to OR_i			15	18	ns
t_{HZ} t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 5.0pF R_L = 2.0kΩ		15	18	ns

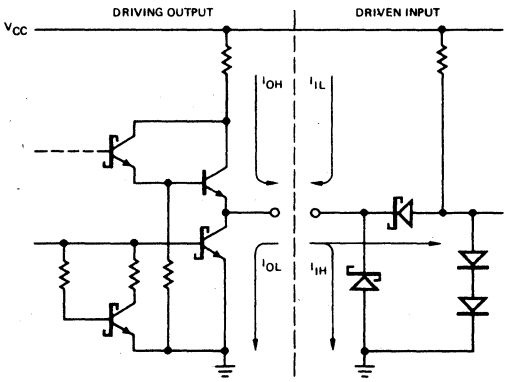
03648A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	I_i to OR_i	C_L = 15pF R_L = 2.0kΩ		45		60	ns
t_{PLH} t_{PHL}	T_j to OR_i			45		60	ns
t_{ZH} t_{ZL}	$\overline{OE}_i$ to OR_i			30		30	ns
t_{HZ} t_{LZ}	$\overline{OE}_i$ to OR_i			20		20	ns

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am29811A

Next Address Control Unit

DISTINCTIVE CHARACTERISTICS

- Next address control unit for the Am2911A Microprogram Sequencer
- 16 next address instructions
- Test input for conditional instructions
- Separate outputs to control the Am2911A, an independent event counter, and a mapping PROM/branch address interface
- Advanced Low-Power Schottky technology

GENERAL DESCRIPTION

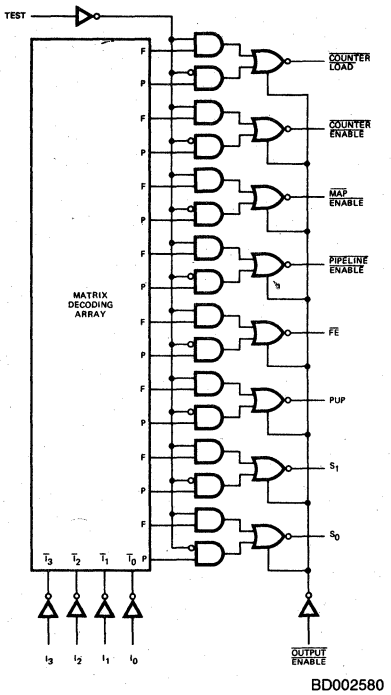
The Am29811A is a Low-Power Schottky device designed specifically for next address control of the Am2911A Microprogram Sequencer. The device contains all outputs required to control a high-performance computer control unit or a structured state machine design using microprogramming techniques.

Sixteen instructions are available by using a four-bit instruction field I_{0-3}. In addition, a test input is available such that conditional instructions can be performed based on a condition code test input.

The full instruction set consists of such functions as conditional jumps, conditional jump-to-subroutine, conditional return-from-subroutine, conditional repeat loops, conditional branch to starting address, and so forth.

One Am29811A can be used to control any number of Am2911A Microprogram Sequencers. The Am2911A Sequencer is a four-bit slice itself. Thus, one Am29811A Next Address Control Unit and three Am2911A Microprogram Sequencers can be used to build a powerful, microprogram sequencer capable of controlling 4k words of microprogram memory.

BLOCK DIAGRAM



BD002580

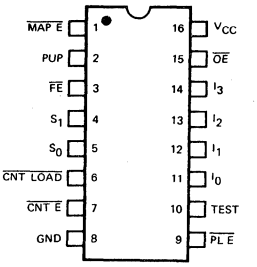
P = Pass
F = Fail

03649A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D16
P16
F-16*



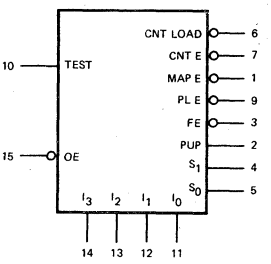
CD004800

*F-16 pin configuration identical to D-16, P-16.

Note: Pin 1 is marked for orientation

5

LOGIC SYMBOL



LS001090

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29811A **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 16-pin CERDIP; F– 16-pin flatpak; P– 16-pin plastic DIP
- Am29811A — Device type: Next Address Control Unit

Valid Combinations	
Am29811A	PC DC, DCB, DMB FMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
11, 12 13, 14	I_0, I_1 I_2,I_3	I	The four instruction inputs to the Am29811A.
10	TEST	I	The condition code input to the device. When the test input is LOW, the device assumes the test has failed. When the test input is HIGH, the device assumes the condition code required has been met; the test has passed.
6	$\overline{\text{Counter Load}}$	O	This output is used to drive the parallel load input of an Am25LS2569 up/down counter.
7	$\overline{\text{Counter Enable}}$	O	This output is used to drive the counter enable input of an Am25LS2569 up/down counter.
1	$\overline{\text{Map Enable}}$	O	This output is used to control the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.
9	$\overline{\text{Pipeline Enable}}$	O	This output is used to control the three-state output of the pipeline register (Am2918) containing the branch address for the computer control unit.
3	$\overline{\text{FE}}$ File Enable	O	This output is used to drive the file enable input of the Am2911. When the file enable output is LOW, a stack operation will take place.
2	PUP	O	Push/Pop. The PUP output is used to drive the push/pop input of the Am2911 Microprogram Sequencer. When the PUP output is HIGH, a push will take place when the file is enabled. When the PUP output is LOW, a pop will take place when the file is enabled.
5, 4	S_0, S_1	O	These two outputs are used to drive the S_0 and S_1 inputs to the Am2911 Microprogram Sequencer. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

GUARANTEED LOADING RULES

OVER OPERATING RANGE (In Unit Loads)

A Low–Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/ Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	$\overline{\text{MAP E}}$	–	100	44	44
2	PUP	–	100	44	44
3	$\overline{\text{FE}}$	–	100	44	44
4	S_1	–	100	44	44
5	S_0	–	100	44	44
6	$\overline{\text{CNT LOAD}}$	–	100	44	44
7	$\overline{\text{CNT E}}$	–	100	44	44
8	GND	–	–	–	–
9	$\overline{\text{PL E}}$	–	100	44	44
10	TEST	0.5	–	–	–
11	I_0	0.5	–	–	–
12	I_1	0.5	–	–	–
13	I_2	0.5	–	–	–
14	I_3	0.5		–	–
15	$\overline{\text{OE}}$	–	100	44	44
16	V_{CC}	–	–	–	–

INSTRUCTION TABLE

MNEMONIC	I_3	I_2	I_1	I_0	INSTRUCTION
JZ	L	L	L	L	Jump to Address Zero.
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L	L	H	L	Jump to Address at Mapping PROM Output.
CJP	L	L	H	H	Conditional Jump to Address in Pipeline Register.
PUSH	L	H	L	L	Push Stack and conditionally load counter.
JSRP	L	H	L	H	Jump-to-Subroutine with starting address conditionally selected from Am2911 R-Register or Pipeline Register.
CJV	L	H	H	L	Conditional Jump to Vector Address.
JRP	L	H	H	H	Jump to Address conditionally selected from Am2911 R-Register or Pipeline Register.
RFCT	H	L	L	L	Repeat Loop if counter is not equal to Zero.
RPCT	H	L	L	H	Repeat Pipeline Address if counter is not equal to Zero.
CRTN	H	L	H	L	Conditional Return-from-Subroutine.
CJPP	H	L	H	H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H	H	L	L	Load Counter and continue.
LOOP	H	H	L	H	Test end of Loop.
CONT	H	H	H	L	Continue to next address.
JP	H	H	H	H	Jump to Pipeline Register Address.

Am29811A FUNCTION TABLE

	INPUTS						OUTPUTS				
	INSTRUCTION										
MNEMONIC	I_3	I_2	I_1	I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L	L	L	L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L	L	L	H	COND JSB PL	L H	PC D	HOLD PUSH	HOLD HOLD	H H	L L
JMAP	L	L	H	L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L	L	H	H	COND JUMP PL	L H	PC D	HOLD HOLD	HOLD HOLD	H H	L L
PUSH	L	H	L	L	PUSH/COND LD CNTR	L H	PC PC	PUSH PUSH	HOLD LOAD	H H	L L
JSRP	L	H	L	H	COND JSB R/PL	L H	R D	PUSH PUSH	HOLD HOLD	H H	L L
CJV	L	H	H	L	COND JUMP VECTOR	L H	PC D	HOLD HOLD	HOLD HOLD	H H	H H
JRP	L	H	H	H	COND JUMP R/PL	L H	R D	HOLD HOLD	HOLD HOLD	H H	L L
RFCT	H	L	L	L	REPEAT LOOP,CNTR $\neq 0$	L H	F PC	HOLD POP	DEC HOLD	H H	L L
RPCT	H	L	L	H	REPEAT PL, CNTR $\neq 0$	L H	D PC	HOLD HOLD	DEC HOLD	H H	L L
CRTN	H	L	H	L	COND RTN	L H	PC F	HOLD POP	HOLD HOLD	H H	L L
CJPP	H	L	H	H	COND JUMP PL & POP	L H	PC D	HOLD POP	HOLD HOLD	H H	L L
LDCT	H	H	L	L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H	H	L	H	TEST END LOOP	L H	F PC	HOLD POP	HOLD HOLD	H H	L L
CONT	H	H	H	L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H	H	H	H	JUMP PL	X	D	HOLD	HOLD	H	L

H = HIGH
L = LOW
X = Don't Care

DEC = Decrement
*LL = Special Case

03649A

Refer to Page 13-1 for Essential Information on Military Devices

Am29811A TRUTH TABLE

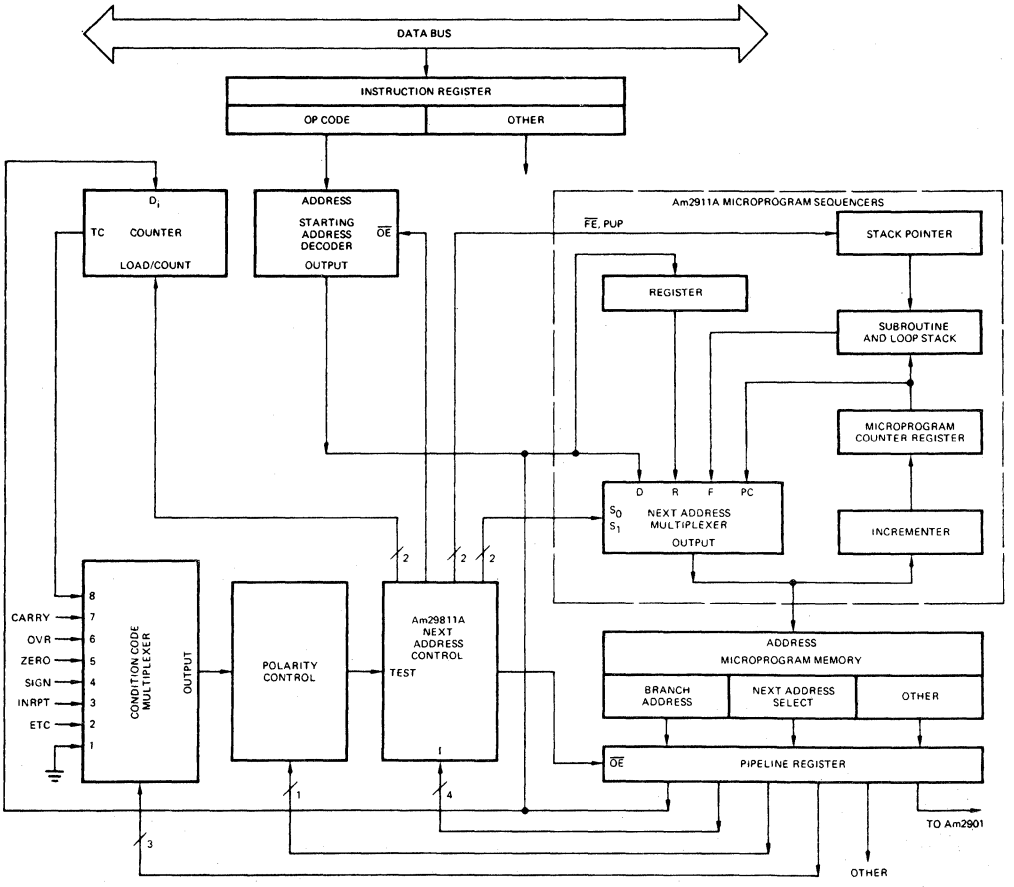
MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER			
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR = 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW

03649A

Refer to Page 13-1 for Essential Information on Military Devices

APPLICATION



AF001970

A Typical Computer Control Unit Using the Am2911 and Am29811A.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

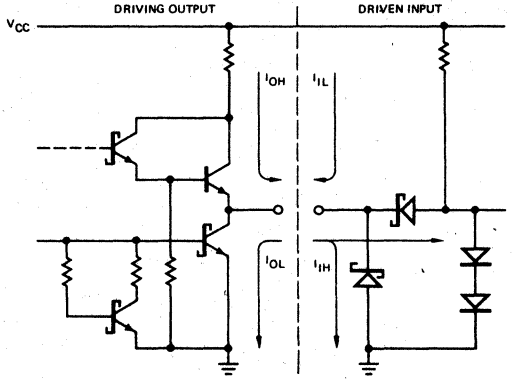
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX			90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $\overline{CS}$ = 2.4V	V_O = 4.5V			40	µA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = MHz (Note 3)			4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)			8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested but are periodically sampled.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH} t_{PHL}	I_i to Any Output	$C_L = 15pF$ $R_L = 2.0k\Omega$		25	35	ns
t_{PLH} t_{PHL}	Test to Any Output			25	35	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			15	20	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output	$C_L = 5.0pF$ $R_L = 2.0k\Omega$		15	20	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
t_{PLH} PHL	I_i to Any Output	$C_L = 15pF$ $R_L = 2.0k\Omega$		40		50	ns
t_{PLH} t_{PHL}	Test to Any Output			40		50	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			25		30	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output			25		30	ns

Am29100
Controller Family Products Index

Am29100 High-Performance Controller Products

Application Note

INTRODUCTION

MICROPROGRAMMING; BEST FOR COMPUTERS, BEST FOR CONTROLLERS

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high-speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low-speed applications, but when the demand for speed and intelligence goes up, they cannot keep pace. Controllers need something better: the 29100 Family.

The 29100 Family products have been designed from the ground up with peripheral control applications in mind. They are fast; they are optimized for bit-manipulation, character handling, data communication and long, sophisticated microprograms; and they are designed to work together in a system.

FAST LIKE YOU'VE NEVER HAD

The central element of our new high-speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a slice – it's a complete 16-bit processor, with three-input ALU, 32 scratchpad registers, an accumulator, data latch, barrel shifter, priority encoder and status register with conditional code generation logic. But the Am29116 is far more than a very fast number cruncher – it's been optimized for controller-oriented applications. Its instruction set has instructions often needed in controllers that are not available in any other processor.

A WHOLE FAMILY OF FAST LSI CONTROLLER PARTS

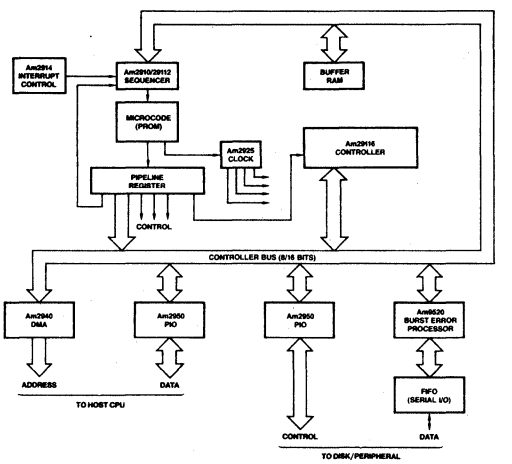
There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

TYPICAL CONFIGURATION USING THE 2900 CONTROLLER FAMILY

A typical intelligent controller configuration is shown below. The basic controller consists of the Am29116, a microprogram control unit and a high-speed buffer memory. Each microinstruction includes: a 16-bit instruction field to the Am29116, next-microinstruction selection bits, control for the buffer memory, control for the interface circuits and possibly an 8- or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.

HIGH-PERFORMANCE INTELLIGENT CONTROLLER



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Refer to Page 13-1 for Essential Information on Military Devices

Am29112

A High-Performance 8-Bit Slice Microprogram Sequencer

DISTINCTIVE CHARACTERISTICS

- **Expandable**
  8-bit Slice, cascadable up to 16-bits
- **Deep stack**
  A 33 deep on-chip stack is used for subroutine linkage, interrupt handling and loop control.
- **Hold feature**
  A hold pin facilitates multiple sequencer implementations.
- **Interruptible at the microprogram level**
  Two kinds of interrupts: maskable and unmaskable.
- **Powerful loop control**
  When cascaded, two counters can act as a single 16-bit counter or two independent 8-bit counters.
- **Powerful addressing modes**
  Features direct, multiway, multiway relative and program counter relative addressing.

GENERAL DESCRIPTION

The Am29112 is a high performance interruptible microprogram sequencer intended for use in very high speed microprogrammed machines and optimized for the new state-of-the-art ALU's and other processing components.

The Am29112 is designed to operate in 10MHz microprogrammed systems.

It has an instruction set featuring relative and multiway branching, a rich variety of looping constructs, and provision for loading and unloading the on-chip stack.

Interrupts are accepted at the microcycle level and serviced in a manner completely transparent to the interrupted microcode.

APPLICATION NOTES REFERENCE

- Microprogrammed CPU using Am29116
- An intelligent fast disk controller
- Am29116 architecture speeds pixel manipulation in interactive bit-mapped graphics

BLOCK DIAGRAM

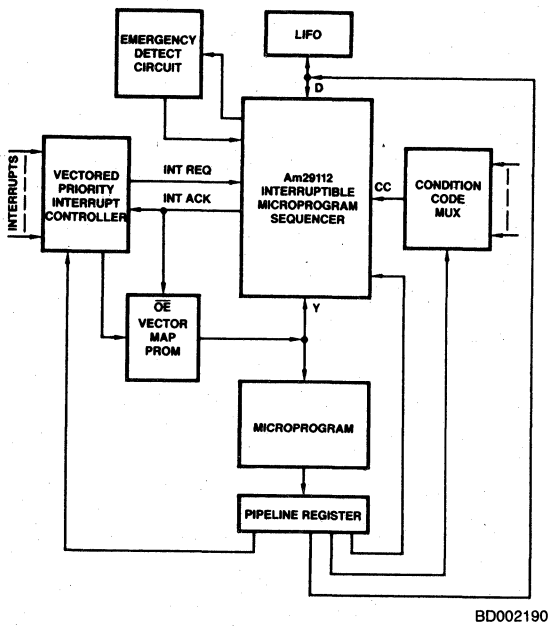

Figure 1. Am29112 in a Single Pipelined System.

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RELATED PRODUCTS

Part No.	Description
Am29116	A 16-Bit Bipolar Microprocessor
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am29114	Vectored Priority Interrupt Controller
Am2925	System Clock Generator and Driver
Am2940	DMA Address Generator
Am2942	Programmable Timer/Counter/DMA
Am2950/ 51/52/53	8-Bit Bidirectional I/O Port
Am29118	8-Bit Bidirectional I/O Port/Accumulator

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_0-D_7	I/O	Bidirectional data input for direct input to address multiplexer, counter and other control registers and stack output.
	Y_0-Y_7	I/O	Bidirectional microprogram address bus outputs microprogram address and inputs interrupt vector.
	M_0-M_3	I	Multiway input pins for up to 16-way branches.
	HOLD	I	When this signal is high, the Y bus is three-stated and the carry-in to the program counter incrementer is forced low. Also, the CMUX output is selected at the incrementer input.
	$\overline{CC}$	I	Test input for the sequencer. (See Table 2.)
	CCEN	I	Test enable for the sequencer. (See Table 2.)
	POL	I	Polarity input for test. (See Table 2.)
	I_0-I_4	I	Instruction input.
	I_5-I_6	I	Mode control input. Select one of three modes: normal, extended or forced continue. (See Table 1.)
	STKERR	O	Indicates stack overflow or underflow.
	$\overline{UINTR}$	I	Unmaskable interrupt request input.
	$\overline{MINTR}$	I	Maskable interrupt request input.
	INTD	I	Disable for maskable interrupts.
	$\overline{MINTA}$	O	Maskable interrupt acknowledge.
	LSS	I	Programs the least significant chip when high, most significant chip when low.
	RST	I	Reset input. Selects zero as the next microprogram address, resets the stack pointer and interrupt logic, and disables maskable interrupts.
	CP	I	Clock input.
	ACIO	I/O	Bidirectional adder I/O line for cascaded Am29112s.
	PCIO	I/O	Bidirectional program counter I/O line for cascaded Am29112s.
	CIO	I/O	Bidirectional counter I/O line for cascaded Am29112s.
	CZIO	I/O	Bidirectional counter zero I/O line for cascaded Am29112s.

PRODUCT OVERVIEW

The Am29112 is designed for use in single-level pipelined systems. A typical configuration is shown in Figure 2.

Branch addresses, constants for the various registers, and stack pointer values are supplied to the Am29112 through the D port which is bidirectional to allow the stack to be unloaded onto an external LIFO. The next address generated by the sequencer is output on the Y port and directly drives the microprogram memory. A single register at the output of the microprogram memory contains the microinstruction being executed, while the next is being fetched. External conditions are applied to the $\overline{CC}$ input of the Am29112 via the condition code MUX and also to the multiway inputs.

A vectored priority interrupt controller generates a prioritized interrupt request ($\overline{MINTR}$) to the Am29112, which acknowledges the request via the $\overline{MINTA}$ pin. Upon receiving the acknowledge, the priority interrupt control puts out the encoded priority of the interrupt, which is translated to a vector by the vector mapping PROM. The $\overline{MINTA}$ output of the Am29112 turns on the PROM output and simultaneously turns off the Y port, enabling the interrupt vector onto the microprogram address bus. In the Am29112, internal states are automatically saved on the stack while the interrupt vector is transmitted through the Y port and incremented to form the next microprogram address.

The emergency detect circuit generates an unmaskable interrupt request upon power failure or stack error. On receiving an unmaskable interrupt, the sequencer branches to the unmaskable interrupt routine; the address of this routine is stored on the Am29112 in the INTVECT register. Detailed interrupt handling is discussed in a later section.

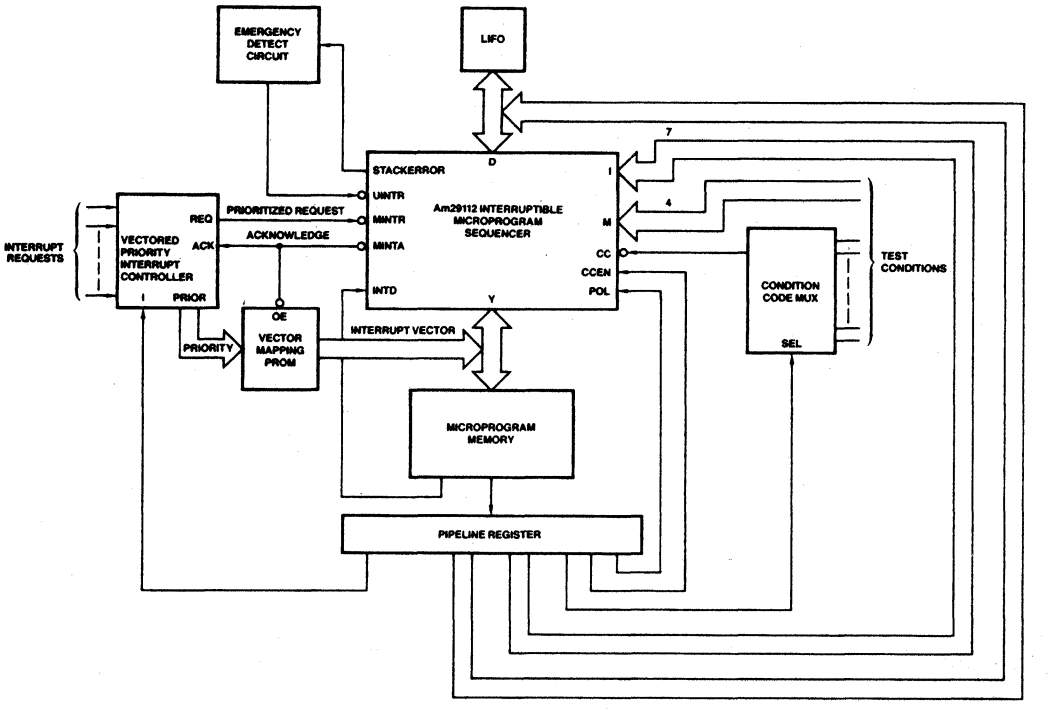

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Figure 2. Control Path in a Single Pipelined System Using the Am29112.

ARCHITECTURE OF THE Am29112

The internal organization of the Am29112 is shown in Figure 3. The most important control loop inside the sequencer consists of the CMUX, incrementer, and PC register. The CMUX selects the next microprogram address based on the instruction and condition code inputs. The next microprogram address is selected from the PC register for a continue, the D port for a branch, the adder for relative and multiway branches, the interrupt register for unmaskable interrupts, the stack for subroutine returns or loop repeats, or all zeros for the JUMP ZERO instruction.

The Am29112 has many registers other than the PC register and the interrupt register. There is an 8-bit counter used for loop control; the DWIDTH register is a 4-bit register which programs the number of least significant bits of the D port that are added to the PC in relative addressing modes; the stack pointer is a 6-bit counter/register that points to the top of stack element; the 3-bit command register is used to program the chip on power-up for compatibility with the external hardware configuration; finally, there is the INTRTN register which is used for saving the CMUX output on the stack when an interrupt occurs.

With the exception of the INTRTN register and the stack pointer, each of the above registers can be loaded directly from the D port of the Am29112.

The Am29112 features a high speed adder with full carry lookahead across 8-bits. The adder is used for PC relative addressing (branch address is PC + D), multiway relative addressing (branch address is D + M, where M is the 4-bit multiway input), and for testing the stack pointer against the D bus. In cascaded configurations, carry ripples from the LSS adder to the MSS adder over the CIO line.

The on-chip stack is 33 deep, and the Am29112 has instructions to save the D inputs, counter, multiway register, and PC-register on the stack. The stack output bus is connected via three-state buffers to the D port. It is possible to pop the stack to the D port.

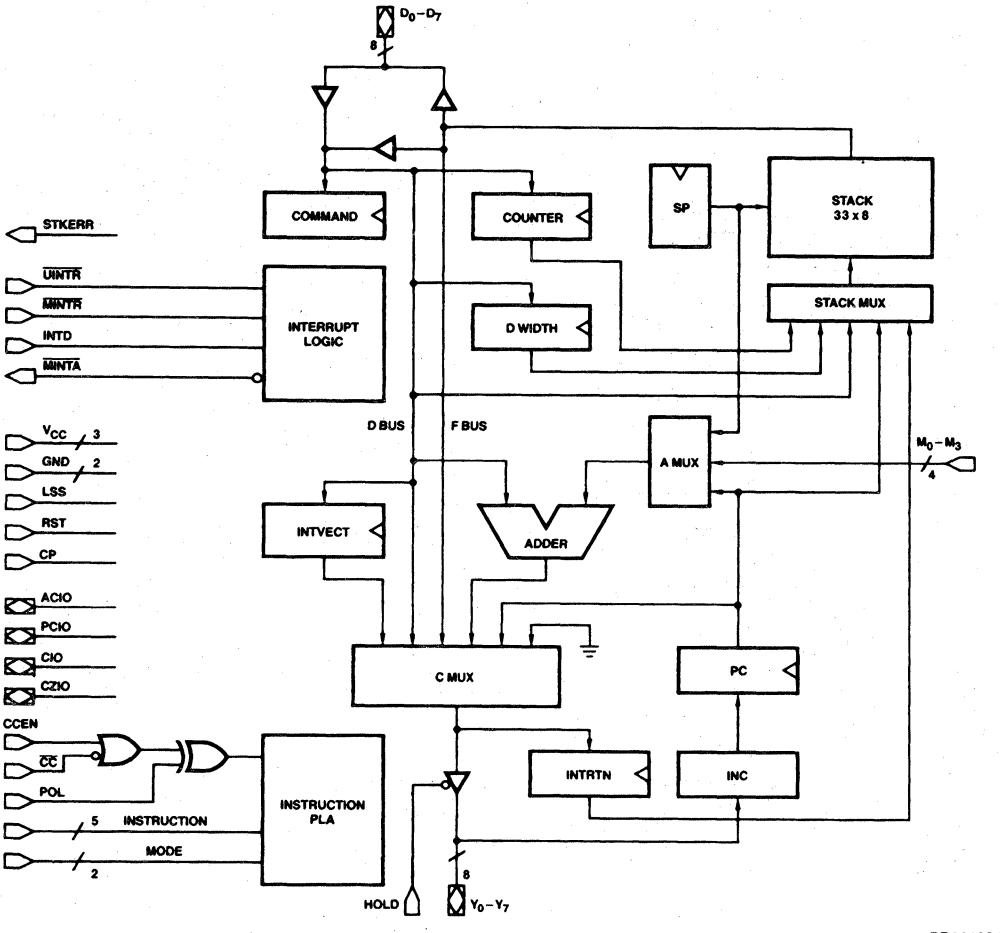

Figure 3. Am29112 48-Pin Package.

INSTRUCTION SET OF THE Am29112

MODE BITS ($I_{6,5}$)

The Am29112 is controlled by 5 instruction inputs, two mode inputs, and the condition code. In typical applications it is expected that the instruction inputs are driven directly from the pipeline, whereas the mode inputs are either permanently wired high or low to select the desired operating mode, or driven indirectly via external logic. (In some applications it might be justifiable to drive the mode bits directly from the pipeline.) The two mode bits select among three operating modes: normal (00), extended (01) and forced continue (10 and 11). In the normal mode, the entire instruction set of the Am29112 applies.

TABLE 1. MODE CONTROLS

$I_{6,5}$	Mode	Description
00	Normal	For cascaded Am29112s, two independent 8-bit counters
01	Extended	For cascaded Am29112s, one 16-bit counter
10	Forced Continue	The Am29112 executes a continue instruction regardless of instruction, condition code, and multiway inputs.
11		

EXTENDED MODE

The instruction set includes instructions that differentiate between upper and lower counters (when there are two cascaded Am29112s). In the normal mode, the two counters on cascaded Am29112s function independently, and it is possible to set up a doubly nested loop without having to save and restore counter values on the stack. In the extended mode, however, the counters on cascaded Am29112s behave like one 16-bit counter and instructions that differentiate between the counters degenerate into identical instructions. Hence in a system with only one Am29112 there is no use for the extended mode.

FORCED CONTINUE MODE

In the forced continue mode the Am29112 executes a continue in every cycle regardless of the instruction bits, condition code, and multiway inputs. The simplest application (if mode bits are driven directly from the pipeline) is to use forced continue for straight-line segments of code thereby permitting most of the sequencer control fields of the pipeline to be shared. The forced continue also has an important application in systems with a writeable control store where it is necessary to step through the addresses sequentially while loading the WCS.

The instructions of the Am29112 are classified into four groups:

- Branching and subroutine linkage
- Looping
- Stack and register
- Interrupt

The sequencer has an instruction repertoire of altogether 40 different instructions. In order to encode these instructions with only 5 instruction lines, the condition code is used in some cases to differentiate between two distinct instructions sharing the same opcode. This way of encoding is used for the stack and register, and interrupt groups of instructions. For these instructions, therefore, the condition code multiplexer is not used to select an external condition. However it is required to force the condition code to unconditional Pass or Fail. The condition code enable and polarity logic has been designed with this in mind. Using the enable and polarity, it is possible to generate both unconditional Pass and unconditional Fail (regardless of the condition code input). Hence the condition code for these instructions is like a sixth instruction line, and the condition code multiplexer field of the pipeline can be shared for these instructions (see Figure 4 and Table 2).

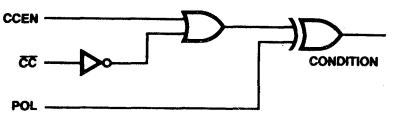

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Figure 4. Condition Code Circuit.

TABLE 2. CONDITION CODE TABLE

CCEN	$\overline{CC}$	POL	Condition
0	0	0	PASS
0	1	0	FAIL
0	0	1	FAIL
0	1	1	PASS
1	0	0	PASS
1	1	0	PASS
1	0	1	FAIL
1	1	1	FAIL

Am29112 Instruction Set

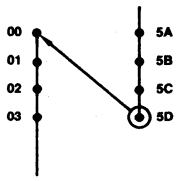
Opcode (I_{40})	Condition	Mnemonic	Description
0	X	JZ.U	UNCONDITIONAL JUMP ZERO
1	PASS	PUSHD.P	PUSH D (PASS)
1	FAIL	LDCMD.F	LOAD COMMAND REGISTER FROM D (FAIL)
2	COND	POP.C	POP; CONDITIONAL STACKOUT TO D
3	COND	CJD.C	CONDITIONAL JUMP D
4	COND	CJSD.C	CONDITIONAL JUMP SUBROUTINE D
5	COND	CJMW.C	CONDITIONAL JUMP MULTIWAY D
6	COND	CJSMW.C	CONDITIONAL JUMP SUBROUTINE MULTIWAY D
7	COND	CRTN.C	CONDITIONAL RETURN
8	COND	PUSHPL.C	PUSH PC; COND LOAD LOWER COUNTER
9	COND	LDLC.C	LOAD LOWER COUNTER; COND PUSH COUNTER
10	X	POPLC.U	POP TO LOWER COUNTER
11	PASS	RSTSP.P	RESET STACK POINTER (PASS)
11	FAIL	LDINTV.F	LOAD UNMASKABLE INTERRUPT VECTOR (FAIL)
12*	PASS	RFCTU.P	REPEAT LOOP, UPPER COUNTER = 0 (PASS)
12*	FAIL	RFCTL.F	REPEAT LOOP, LOWER COUNTER = 0 (FAIL)
13**	PASS	RPCTU.P	REPEAT PIPELINE, UPPER COUNTER = 0 (PASS)
13**	FAIL	RPCTL.F	REPEAT PIPELINE, LOWER COUNTER = 0 (FAIL)
14	COND	LOOP.C	TEST END LOOP
15	PASS	ENINT.P	ENABLE INTERRUPTS (PASS)
15	FAIL	DISINT.F	DISABLE INTERRUPTS (FAIL)
16***	COND	TWBL.C	THREE-WAY BRANCH, LOWER COUNTER
17***	COND	TWBU.C	THREE-WAY BRANCH, UPPER COUNTER
18	PASS	TSTSP.P	TEST SP WITH D (PASS)
18	FAIL	TSTMT.F	JUMP D IF STACK NOT EMPTY
19	COND	CJDF.C	COND JUMP D/STACK AND POP
20	COND	CJSDF.C	COND JUMP SUBROUTINE D/STACK AND POP
21	COND	CJMWR.C	COND JUMP MULTIWAY RELATIVE D
22	COND	CJSMWR.C	COND JUMP SUBROUTINE MULTIWAY RELATIVE D
23	COND	CJPP.C	COND JUMP PIPELINE AND POP
24	COND	PUSHPU.C	PUSH PC; COND LOAD UPPER COUNTER
25	COND	LDUC.C	LOAD UPPER COUNTER; COND PUSH COUNTER
26	PASS	POPUC.P	POP TO UPPER COUNTER (PASS)
26	FAIL	POPDW.F	POP TO DISPLACEMENT WIDTH (FAIL)
27	COND	LDDW.C	LOAD DISPLACEMENT WIDTH; COND PUSH DW
28	COND	CJR.C	COND JUMP D PC REL
29	COND	CJRN.C	COND JUMP D PC REL NEGATIVE
30	COND	CJSR.C	COND JUMP SUBROUTINE D PC REL
31	COND	CJSRN.C	COND JUMP SUBROUTINE D PC REL NEGATIVE

* These instructions are identical in the extended mode.
**These too.
***These too.

Extensions: U – unconditional; C – conditional; P – PASS condition; F – FAIL condition.
Note: PASS/FAIL condition can be produced as follows. P stands for polarity and I for input:

$\overline{CC}$	CCEN	POL	Condition
X	1	0	PASS
X	1	1	FAIL
I	0	P	COND

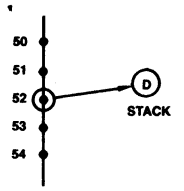
0 Jump Zero (JZ.U)



PF000600

UNCONDITIONAL

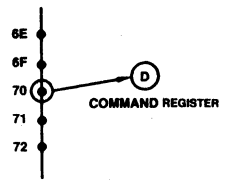
1 Push D (PUSHD.P)



PF000620

FORCED PASS

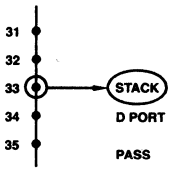
1 Load Command Register from D (LDCMD.F)



PF000611

FORCED FAIL

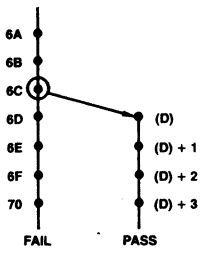
2 Pop and Conditional Stack-out to D (POP.C)



PF000571

CONDITIONAL

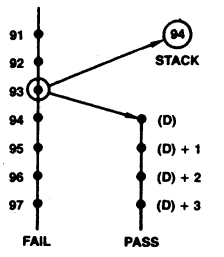
3 Conditional Jump D (CJD.C)



PF000580

CONDITIONAL

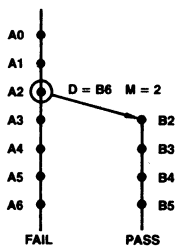
4 Conditional Jump Subroutine D (CJSD.C)



PF000590

CONDITIONAL

5 Conditional Jump Multiway D (CJMW.C)



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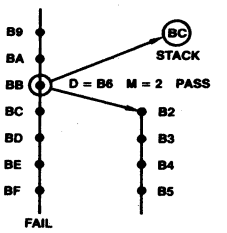
CONDITIONAL

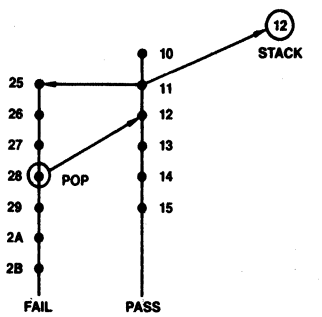
6 Conditional Jump Subroutine Multiway D (CJSMW.C)



PF000550

CONDITIONAL

7 Conditional Return (CRTN.C)

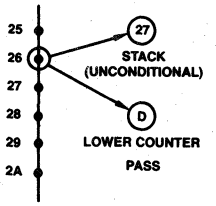


PF000540

CONDITIONAL

6

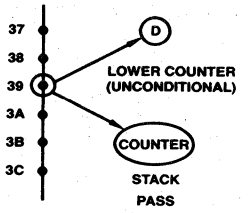
8 Push PC and Conditional Load Lower Counter (PUSHPL.C)



PF000511

CONDITIONAL

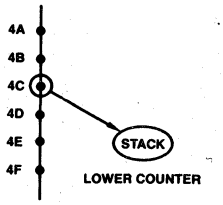
9 Load Lower Counter and Conditional Push Counter (LDLC.C)



PF000521

CONDITIONAL

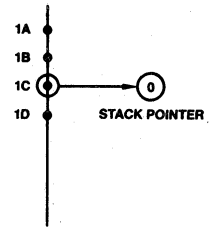
10 Pop to Lower Counter (POPLC.U)



PF000531

UNCONDITIONAL

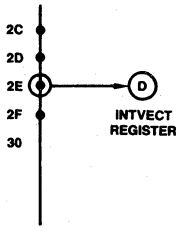
11 Reset Stack Pointer (RSTSP.P)



PF000460

FORCED PASS

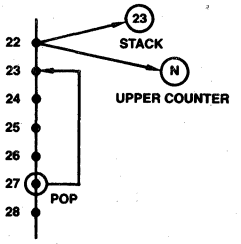
11 Load Unmaskable Interrupt Vector (LDINTV.F)



PF000470

FORCED FAIL

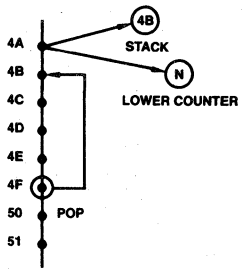
12 Repeat Loop, Upper Counter (RFCTU.P)



PF000790

FORCED PASS

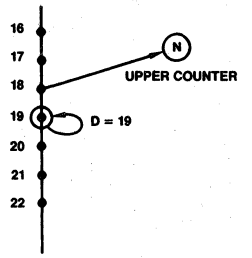
12 Repeat Loop, Lower Counter (RFCTL.F)



PF000440

FORCED FAIL

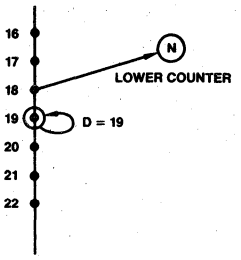
13 Repeat Pipeline, Upper Counter (RPCTU.P)



PF000451

FORCED PASS

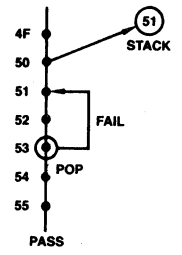
13 Repeat Pipeline, Lower Counter (RPCTL.F)



PF000781

FORCED FAIL

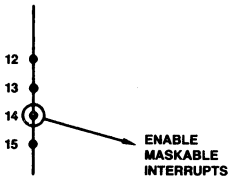
14 Test End Loop (LOOP.C)



PF000421

CONDITIONAL

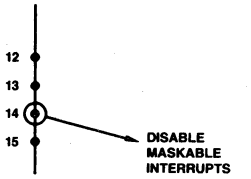
15 Enable Interrupts (ENINT.P)



PF000430

FORCED PASS

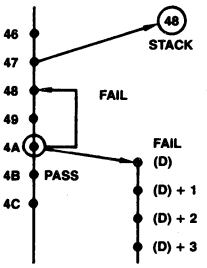
15 Disable Interrupts (DISINT.F)



PF000390

FORCED FAIL

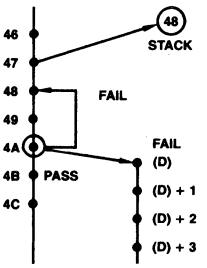
16 Three-Way Branch, Lower Counter (TWBL.C)



PF000411

CONDITIONAL

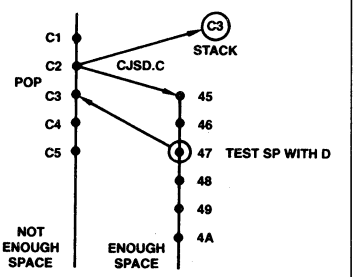
17 Three-Way Branch, Upper Counter (TWBU.C)



PF000411

CONDITIONAL

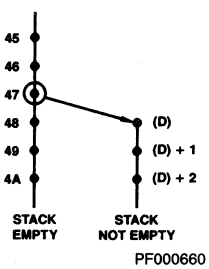
18 Test SP with D (TSTSP.P)



PF000400

FORCED PASS

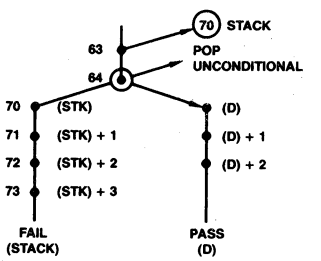
18 Jump D if Stack Not Empty (TSTMT.F)



PF000660

FORCED FAIL

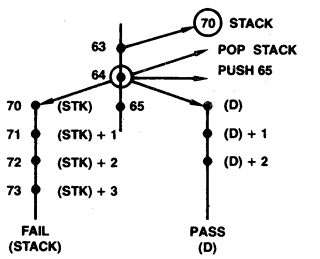
19 Conditional Jump D/Stack and Pop (CJDF.C)



PF000691

CONDITIONAL

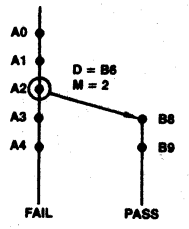
20 Conditional Jump Subroutine D/Stack and Pop (CJSDF.C)



PF000681

CONDITIONAL

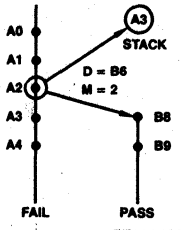
21 Conditional Jump Multiway Relative D (CJMWR.C)



PF000670

CONDITIONAL

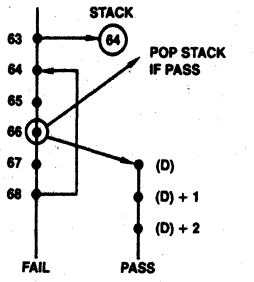
22 Conditional Jump Subroutine Multiway Relative D (CJSMWR.C)



PF000700

CONDITIONAL

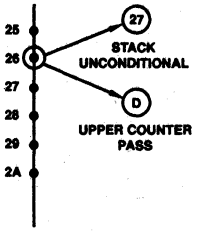
23 Conditional Jump Pipeline and Pop (CJPP.C)



PF000760

CONDITIONAL

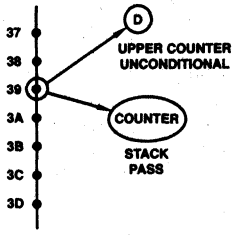
24 Push PC and Conditional Load Upper Counter (PUSHPU.C)



PF000730

CONDITIONAL

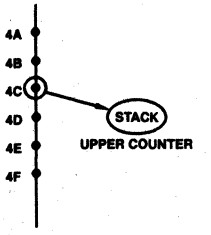
25 Load Upper Counter and Conditional Push Counter (LDUC.C)



PF000710

CONDITIONAL

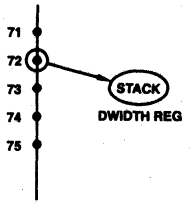
26 Pop to Upper Counter (POPUC.P)



PF000770

FORCED PASS

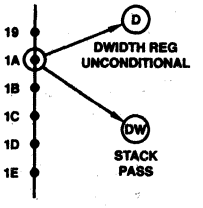
26 Pop to Displacement Width (POPDW.F)



PF000720

FORCED FAIL

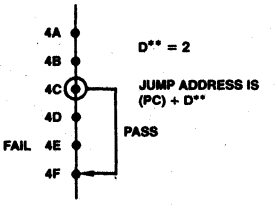
27 Load Displacement Width and Conditional Push DW (LDDW.C)



PF000740

CONDITIONAL

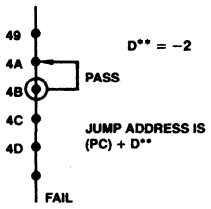
28 Conditional Jump D PC Relative (CJR.C)



PF000750

D** is displacement (see Note 1).
CONDITIONAL

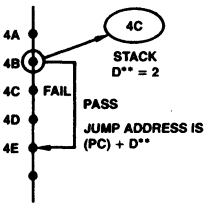
29 Conditional Jump D PC Relative Negative (CJRN.C)



PF000490

D** = −2, should be two's complement (see Note 2).
CONDITIONAL

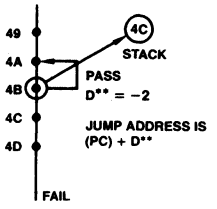
30 Conditional Jump Subroutine D PC Relative (CJSR.C)



PF000480

D**is displacement (see Note 1).
CONDITIONAL

31 Conditional Jump Subroutine D PC Relative Negative (CJSRN.C)



PF000500

D** = −2, should be two's complement (see Note 2).
CONDITIONAL

Notes: 1. The number of bits of D used as displacement is stored in DWIDTH register. The remaining high order bits are zero-extended.
2. The number of bits of D used as displacement is stored in DWIDTH register. The remaining high order bits are one-extended.

BRANCHING INSTRUCTIONS

Direct Branching

Instruction 0 is the unconditional jump to zero instruction. This instruction also resets the stack pointer and the interrupt logic as well as setting command register as follows: CR(0) = 1, CR(1) = LSS, CR(2) = 1.

Direct branching is implemented by instruction 3 (COND JUMP D) and 4 (COND JSB D). The branch address is input through the D port. If the condition is PASS, the branch is taken, otherwise the sequencer executes a continue. Two-way direct branching is implemented by instruction 19 (COND JMP D/STACK) and instruction 20 (COND JSB D/STACK). If the condition is Pass, the branch address is taken from the D input port, otherwise, the branch address is taken from the stack. In either case the stack is popped. This instruction assumes that the alternative address was pushed on the stack by a previous instruction. Jump to subroutine differs from JUMP in that the PC register is pushed on the stack. This enables the subroutine to use COND RETURN (7) to return to the point of call. Note that the two-way jump to subroutine (20) causes a simultaneous pop and push so that the stack pointer is unaffected but the top of stack element is replaced by the return address.

Relative Branching

In the relative branch instructions, a dynamically alterable subfield of the D inputs is added to the PC to form the branch address. The remaining most significant bits of the D inputs are ignored and internally converted to all 0's for forward branches and all 1's for backward branches. The displacement width (DWIDTH) register in the Am29112 holds the number of least significant bits of D that participate in the relative branch as the displacement, and can be loaded from the lower four bits of the D port. In cascaded systems, the displacement width has to be loaded consistently in the two chips. For example, for a displacement width of 9, the lower order chip gets a displacement width of 8 and the higher order chip gets a displacement width of 1. As another example, if the lower order chip has a displacement width of less than 8 bits, the higher order chip must have a displacement width of zero. If the displacement width register is loaded with any value greater than 8, it is exactly as if it were loaded with 8.

Instruction 28 (29) is the relative jump (jump back) instruction, and instruction 30 (31) is the relative jump to subroutine (jump back to subroutine) instruction. For backward relative branches, the displacement must be coded as a two's complement negative number. When the displacement width is the same as the microaddress width the forward and backward relative branch instructions are identical. When the displacement width is less than the microaddress width, the more significant bits of D outside the displacement are forced to all zeros for positive branches and to all ones for negative branches. This is effectively sign extension except that the sign information is contained in the instruction rather than the displacement, and there is no need for sign information to propagate between cascaded chips since it is assumed that the displacement width registers in the two chips have been consistently loaded.

The disadvantage of having the sign information in the instruction rather than the displacement can be overcome by a judicious choice of instruction format. The opcodes for forward and backward relative branch instructions have been chosen to differ in the least significant bit position only, with a '0' in that bit for forward branches and a '1' for backward branches. If the sequencer instruction field is contiguous with and on the more significant side of the displacement field in the pipeline register, then the least significant instruction bit is like the sign bit for the displacement for relative branch instructions. This permits the assembler to use the same opcode for forward and backward relative branch instructions, but *overlap* the displacement field (now declared to be one bit longer than the actual displacement field in the pipeline) with the sequencer instruction field by one bit. If the assembler now generates a negative displacement, the sequencer opcode formed is the backward branch; while if the displacement is positive, the sequencer opcode formed is forward branch.

When the instruction is executed, the PC already has been incremented and points to the next sequential instruction, hence a forward branch with a displacement of 0 causes the next sequential instruction to be executed.

Multiway Branching

Two variants of multiway branching are available on the Am29112 – multiway substitute D and multiway relative D. In multiway substitute D the 4 multiway inputs directly replace the 4 least significant bits of the branch address input at D.

Instruction 5 is a conditional multiway branch and instruction 6 a conditional multiway subroutine call. In these instructions, the least significant 4 bits of the D input port are not used by the sequencer, and may be shared, for instance to select among different sets of multiway inputs.

Multiway branching has the disadvantage that the jump table must be aligned on a 16 word boundary. This disadvantage is overcome in the Am29112 multiway relative branching instructions. In these instructions, the number input on the multiway pins is added to the branch address input at D. Instruction 21 is a conditional multiway relative branch and instruction 22 a conditional multiway relative subroutine call.

One of the advantages of multiway branching is that it enables a 16 way decision to be made in exactly one microcycle. However, the 16 target addresses are constrained to be contiguous in memory. Hence, if the target routines need more than one microword each, as is very likely, they are addressed indirectly through a table of 16 contiguous branch instructions. For very high speed applications, the extra microcycle needed to branch indirectly off the jump table may not be acceptable. This penalty is avoidable if the multiway bits are offset with respect to the D inputs. When two cascaded Am29112s are used, there are two sets of 4-bit multiway inputs. The least significant chip has a multiway input with no offset, while the most significant chip has a multiway input with an 8-bit offset. The Am29112 command register has a bit CR(1) that enables or disables multiway branching on the chip. In a system with two cascaded Am29112s, each chip has a command register bit. Multiway branching may be disabled in either chip by resetting the command register bit on that chip, or enabled by setting the command register bit. When multiway branching is disabled on a chip, for that chip both multiway and multiway relative branches are converted to direct branches, and the multiway inputs are a Don't Care. Multiway branching with an 8-bit offset is implemented by disabling multiway in the least significant slice and enabling it in the most significant slice. In this case, the 16 target addresses are dispersed in memory, separated by 256 locations each. Another useful configuration is obtained by enabling multiway on both chips. In this case, up to 16 sets of target addresses are dispersed in memory, separated by 256 locations each.

The Am29112 does not have an unconditional continue in its instruction set. This is not expected to be a drawback because the instruction set requires that both unconditional PASS and unconditional FAIL are programmable by the sequencer to select among different instructions sharing the same opcode. Hence, a continue is obtained by executing instruction 3 (COND JUMP D) with a forced FAIL condition.

LOOPING INSTRUCTIONS

The looping instructions on the Am29112 are of two kinds: conditional, which depend on an external condition to signal loop termination, and iterative, which decrement the Am29112 counter and check for a count of zero. There is also a three-way branch instruction that combines the check for external condition with the check for count of zero in a single instruction.

All the looping instructions are similar in two respects. Firstly, the check for the loop condition is done at the end of the loop. This implies that the loop body is always executed at least once. Secondly, in the case that the loop has to be repeated, a backward branch to the loop head is made by using the address on top of stack. This frees the D inputs for other use, but makes it necessary to push the address of the start of the loop on the stack before entering the loop. Also, if the loop is iterative, it is necessary to load a count value in the counter at the same time. Instructions 24 (PUSH PC; COND LOAD UPPER COUNTER) and 8 (PUSH PC; COND LOAD LOWER COUNTER) combine both these requirements.

Instruction 14 implements a simple conditional repeat loop. If the condition is FAIL the sequencer loops back using the top of stack address, and if the condition is PASS, the sequencer performs a continue to the next sequential address, and simultaneously pops the stack to remove the address of the loop head. The instruction may be described in Pascal-like syntax as:

repeat PUSH PC
LOOP BODY
until condition = TRUE;

Instruction 23 (COND LOOP EXIT) implements a loop exit that may be used with any of the Am29112 loop instructions. It is a conditional jump to D, which simultaneously pops the stack. If the condition is FAIL, it simply performs a continue.

As discussed earlier, the counters present in cascaded Am29112s may be used independently or cascaded as a single 16-bit counter under microprogram control. The mode bits select the cascaded configuration only in the extended mode. There are separate repeat and three-way branch instructions for upper and lower counters. In the case of the repeat instructions, the condition code is used to differentiate between the repeat on the upper and the repeat on lower counter (a condition of PASS selects the upper counter). In the case of the three-way branch, which needs the condition code input for the external condition, there are two separate opcodes for three-way branch on upper (opcode 17) and three-way branch on lower (opcode 16). When a single Am29112 is used only the repeat on lower counter instructions are useful; and when two Am29112s are cascaded but operated in the extended mode, the repeat instructions on upper and lower counter are identical in effect and both operate on the 16-bit cascaded counter.

Instruction 12 (REPEAT LOOP IF COUNTER NOT ZERO) is the iterative analog of instruction 14 (CONDITIONAL REPEAT LOOP). Instruction 8 (PUSH PC; COND LOAD COUNTER) is used with condition code as forced PASS and the desired count in the D field of pipeline. This causes the address of the loop head to be pushed on the stack, and the lower counter loaded with the count. At the end of the loop body, the repeat instruction checks if the count is zero. If it is not zero, it performs a loop back using the top of stack address and simultaneously decrements the counter; if it is zero, it pops the address of the loop head off the stack and simultaneously selects the next sequential address thereby exiting the loop. A repeat loop on the upper counter can be set up using instruction 24 instead of 8 to push PC and load upper counter and using instruction 14 to loop back with condition code as forced PASS. Note the potential off-by-one error: since the count is checked before it is decremented, a count of 1 causes two iterations: the first iteration finds a count of 1 and decrements; on the second iteration the count is found to be zero and the loop terminates. Hence, the value of count loaded should be *one less* than the desired number of iterations. In the example above, loading the counter with 7 resulted in 8 iterations.

The single instruction repeat (instruction 13) is provided for applications where the loop body is a single microinstruction, for example, an ALU shift. The loop is set up as before using instruction 9 or 25 (LOAD COUNTER AND COND PUSH COUNTER). The repeat instruction then presents its own address to the D inputs of the sequencer. As with the repeat loop instruction, the single instruction repeat checks for counter = 0. If the counter is equal to zero, it continues to the next sequential instruction; otherwise it repeats the address presented to the D inputs, which is its own address, and

decrements the count by one. Instruction 13 can also be used in place of instruction 12 where there is no stack location available to hold the address of the loop head.

Often it is necessary to repeat an action until either some external condition becomes true or a predetermined count is reached: for example, searching a character string for an occurrence of some character. The three-way branch instructions of the Am29112 combine the test for count and external condition in one cycle. At any loop iteration, if the condition becomes PASS when the three-way branch is executed, then the sequencer performs a continue to the next sequential instruction, and pops the stack. If the condition is FAIL when the three-way branch is 'xecuted, the sequencer tests the count. If the count is zero, then the search is unsuccessful and the sequencer performs a branch to the address input at the D port, simultaneously popping the stack. If the count is not zero, and the condition is FAIL, the sequencer performs a loop back via the stack. The instruction always decrements the counter by one if the counter is non-zero.

Since interrupts may occur at any point in the execution of microcode, it is necessary to be able to save counter values on the stack so that the interrupt routines can use the counter without interfering with the operation of the interrupted code. The sequencer provides instructions that permit arbitrary nesting of loops and subroutine calls. Instruction 9 (LOAD LOWER COUNTER; CONDITIONAL PUSH COUNTER) can be used to load the lower counter from the D port. If the condition is PASS, then the instruction also causes the old counter value to be pushed on the stack. To restore the counter from the stack, instruction 10 (POP TO LOWER COUNTER) can be used with a forced FAIL condition. Instructions 25 (LOAD UPPER COUNTER; CONDITIONAL PUSH COUNTER) and 26 (COND POP TO UPPER COUNTER/POP TO DISPLACEMENT WIDTH) are the counterparts for operating on the upper counter. Note that in cascaded systems, when the counter is pushed, regardless of whether instruction 25 or instruction 10 is executed, the entire counter is pushed to keep the stack balanced in the two Am29112s.

STACK AND REGISTER INSTRUCTIONS

In addition to all the instructions mentioned earlier that explicitly or implicitly alter the stack, the Am29112 has some specialized instructions for stack manipulation.

The stack on the Am29112 is 33 deep. Attempting to push when the stack is full or to pop when the stack is empty causes the STACK ERROR signal out of the Am29112 to be generated. The error is latched internally and persists until either the chip is reset or the stack is popped in case of overflow or pushed in case of underflow. When the stack overflows, the stack pointer does not wrap around, and all subsequent pushes on the full stack write over the top-of-stack location.

The stack on the Am29112 can be loaded through the D port using instruction 1 (COND PUSH D/LOAD COMMAND REGISTER) with condition as forced PASS and unloaded out of the D port using instruction 2 (POP; COND STACKOUT TO D) with a forced PASS condition. In the stackout instruction the D port becomes an output port. Care must be taken to avoid contention on the D bus when this instruction is executed. The D bus is output enabled while CP is low for this instruction. The ability to load and unload the stack is useful for implementing context switches. For fast unloading of the stack, a tight two-instruction loop can be set up using instruction 12 (POP; COND STACKOUT TO D) with a forced FAIL condition and instruction 18 (COND TEST SP/BRANCH STACK NOT EMPTY) also with a forced FAIL condition. The branch instruction performs a branch to D if the stack is not empty.

The stack nesting level in an interruptible sequencer varies dynamically. Hence, the Am29112 is provided with instructions for checking the available stack space: instruction 18 (COND TEST SP/BRANCH STACK NOT EMPTY). Two distinct instructions for testing the stack pointer have been packed into the same opcode and are differentiated by the condition code. A condition code of PASS selects the Test Stack Pointer instruction. In this instruction, the sequencer tests the stack to see if there is enough space, as determined by a constant input at the D port; if there is enough space, the sequencer performs a continue, whereas if there is not enough space, the sequencer performs a subroutine return. The number of stack locations required is input at the D port. In a system with only one Am29112, the least significant 6 bits of the D are used within the chip for this instruction. In a system with two cascaded Am29112s the determination is made *independently* in the two chips (since the stack pointer is at all times identical in the two chips). Hence, the same number must be presented to the two chips. The adders in the two Am29112s are not cascaded for this instruction but function independently. In both Am29112s only the 6 LSBs of the D port are actually used in the comparison.

INTERRUPT HANDLING

The Am29112 recognizes two kinds of interrupts: maskable and unmaskable. Maskable interrupts cause automatic saving of status on the internal stack and can be inhibited, either externally via the INTERRUPT DISABLE pin, or internally via instruction 15 (COND ENABLE/DISABLE INTERRUPT). In addition, maskable interrupts are disabled when there is not enough space on the stack to service the interrupt, though this internal inhibit can be overridden be clearing a bit in the command register. The unmaskable interrupt, on the other hand, cannot be disabled and does not cause saving of status on the internal stack. It is intended for handling abnormal and irrecoverable situations like power failure or stack overflow. When an unmaskable interrupt occurs, the sequencer branches to the address of the unmaskable interrupt routine stored in the INTVECT register. This address is stored on chip at system initialize time using instruction 11 (COND RESET SP/LOAD INTERRUPT REGISTER) with a condition of FAIL. If a maskable interrupt is being processed when the unmaskable interrupt occurs, the unmaskable interrupt may be delayed at most one cycle to prevent contention on the Y bus. In any case, the unmaskable interrupt request should persist for at least one clock edge.

The Am29112 contains an interrupt disable flip-flop on-chip. The flip-flop is set by the DISABLE INTERRUPT instruction (opcode 15 with forced FAIL) and reset by the ENABLE INTERRUPT instruction (opcode 15 with forced PASS). The flip-flop output performs the same function as the interrupt disable pin. On reset, or on receiving an unmaskable interrupt, the flip-flop is set thereby disabling maskable interrupts. Hence, at the end of initialization, the ENABLE INTERRUPT instruction will have to be executed to reset the flip-flop and enable maskable interrupts.

In the case of maskable interrupts, the interrupt return address is saved on the stack automatically using the INTRTN register. the INTRTN register is loaded with the CMUX output with every clock. When an interrupt is acknowledged, the Am29112 output is turned off and the vector applied externally. However, the sequencer executes the instruction which is in the pipeline register in that cycle. The result of executing the interrupted instruction, namely the next address, does not come out of the Am29112 Y bus because the Y bus is used to input the interrupt vector. It is clocked into the INTRTN register. On the first cycle of the interrupt routine, the sequencer pushes the return address on the stack so that the

interrupt routine returns by doing a COND RETURN, like any other subroutine.

THE INVISIBLE STACK PUSH THAT THE SEQUENCER EXECUTES WHEN IT IS INTERRUPTED OCCURS IN THE FIRST CYCLE OF THE INTERRUPT SERVICE ROUTINE. HENCE, THE FIRST INSTRUCTION OF THE INTERRUPT SERVICE ROUTINE MAY NOT BE ANY INSTRUCTION THAT USES THE STACK.

Before acknowledging an interrupt, the sequencer checks the stack to see if there is a minimum of five locations to handle the interrupt. If there is insufficient space on the stack, the acknowledge is not generated. This feature may be disabled by a bit in the command register.

CR(0) = 1 INHIBIT ACKNOWLEDGE ON STACK FULL (DEFAULT)

CR(0) = 0 GENERATE ACKNOWLEDGE ON STACK FULL

MASKABLE INTERRUPTS

The branch vector for maskable interrupts is applied externally to the Y port of the Am29112. This section discusses the system timing considerations and their impact on interrupt handling in the Am29112.

Figure 5(a) shows a general system configuration highlighting the interrupt portion of the circuitry and the control loop. A priority interrupt controller generates an interrupt request for the highest priority pending interrupt. This request is applied to the $\overline{\text{MINTR}}$ pin of the Am29112. If the request is not masked, the Am29112 puts out an acknowledge on the $\overline{\text{MINTA}}$ pin. The interrupt controller then puts out the encoded priority of the highest priority interrupt to the vector PROM, which maps the priority code into a vector.

The $\overline{\text{MINTA}}$ line turns on the vector PROM output at the same time as the Y port on the Am29112 is three-stated. Hence, the interrupt vector gets onto the micromemory address bus and is also input into the Am29112, and incremented to form the next address. The Am29112 saves the return address on the stack so that when the interrupt service routine does a subroutine return, control returns to the instruction following the interrupted instruction.

The maskable interrupt request is synchronized on the Am29112. If there is no disable, therefore, the acknowledge always is active in the cycle following the request. However, the acknowledge to Y bus three-stating delay is programmable: the Y bus three-stating signal can occur either in the same cycle as, or in the cycle following, the $\overline{\text{MINTA}}$ acknowledge, depending on a bit in the command latch of the Am29112.

The command register bit that programs the postdelay option is bit 2, the third least significant bit. The command register has 3 bits altogether and is loaded from the 3 LSBs of the D inputs using instruction 1 (COND PUSH D/LOAD COMMAND REGISTER) with a condition of PASS. Note that in a system with two cascaded Am29112s, the 0 and 2 bits of the command registers in the two chips must both be loaded with the same data on system initialization. The postdelay bit in the command register selects the postdelay option when it is zero.

Figure 5(b) shows the configuration without postdelay, including a simplified view of the acknowledge circuit. The acknowledge is granted at the same time the Y output of the Am29112 is three-stated and the vector PROM enabled by the MINTA signal out of the Am29112. The critical delay path in this case is clock to acknowledge (Am29112) + acknowledge to priority out (interrupt controller) + vector PROM access time + microprogram memory access time + pipeline setup time. Obviously, this delay will have a significant impact on overall cycle time. However, in slow systems or in systems where the vector is always available immediately with acknowledge, this configuration is acceptable. It is also acceptable if the vector mapping PROM is made part of the microprogram memory by dedicating the locations in low memory addressed by the priority to hold vectors to the corresponding interrupt routines.

Figure 5(c) shows a simplified view of the Am29112 configured with postdelay active. An external D-type flip-flop adds a one cycle delay to the $\overline{\text{MINTA}}$ signal before it switches the output enable on the vector register. The interrupt request to acknowledge delay is the same as in the circuit with postdelay inactive, but the Y bus three-stating signal occurs one cycle later than the acknowledge. The critical path has been broken into two with the register at the vector PROM output. In this case the critical delay path is cut short by the microprogram memory access time. While the vector PROM accesses the interrupt vector, the microprogram memory accesses the next sequential instruction. This implies that one more instruction of the interrupted code executes after the cycle in which the acknowledge is granted. (If that instruction happens to be a DISABLE INTERRUPT instruction, then even though no more interrupts will be accepted by the Am29112, the interrupt which has been acknowledged goes through and the corresponding interrupt service routine may enable interrupts again using the ENABLE INTERRUPT instruction.)

The command register bits are summarized below:

CR(0) : Interrupt acknowledge on stack full

- CR(0) = 1 : inhibit acknowledge on stack full (default)
- CR(0) = 0 : generate acknowledge on stack full

CR(1) : Multiway enable

- CR(1) = 1 : enable multiway branching (default for LSS)
- CR(1) = 0 : disable multiway branching (default for MSS)

CR(2) : Interrupt postdelay flip-flop

- CR(2) = 1 : no postdelay (default)
- CR(2) = 0 : postdelay

On reset & JZU: CR(0) = 1
CR(1) = LSS
CR(2) = 1

HOLD

The Am29112 is equipped with a HOLD pin for configurations utilizing more than one sequencer driving a common microprogram address bus. In such situations, it is necessary to cause the unselected sequencer to hold its internal state while some other sequencer executes, so that it can resume execution at the point where it was held. The HOLD pin, when asserted, three-states the Y bus, forces low the carry into the PC incrementer, and selects the internal CMUX output (instead of the Y bus) at the incrementer input. To complete the HOLD function, it is also necessary to disable interrupts and to put the sequencer into the forced continue mode. Under these conditions, the value of the PC is recirculated through the CMUX and the incrementer until the HOLD is released, and all the remaining state bits in the sequencer are not altered because of the forced continue.

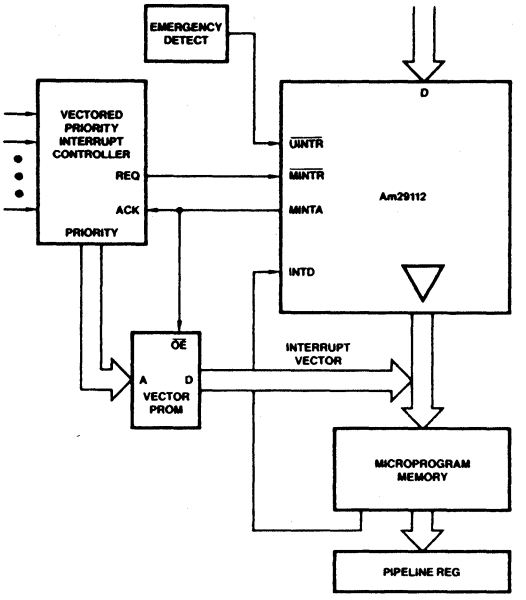


Figure 5a. Interrupt Control Loop.

Note: The INTD connection directly from microprogram memory.

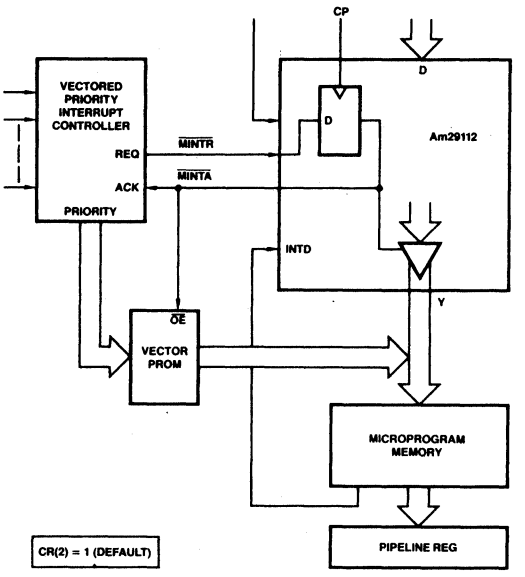


Figure 5b. No Postdelay.

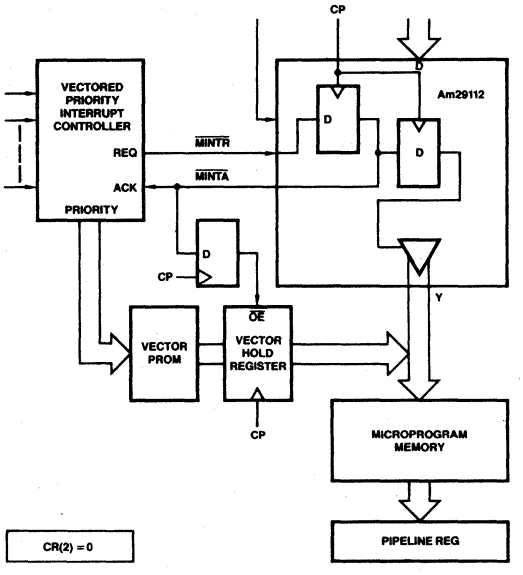


Figure 5c. With Postdelay.

Am29114

Real-Time Interrupt Controller

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Accepts 8 Interrupt Inputs**
  Interrupts may be pulses or levels and they are stored internally.
- **Supports Real-Time Interrupts**
  Interrupts are handled at microinstructions boundary.
- **Built-In Mask Register**
  Enables or disables individual interrupt inputs.
- **Built-In In-Service Register**
- **Vectored Output**
  Output is binary code for highest priority unmasked input.
- **Expandable**
  Any number of the Am29114's may be cascaded for larger interrupt systems.

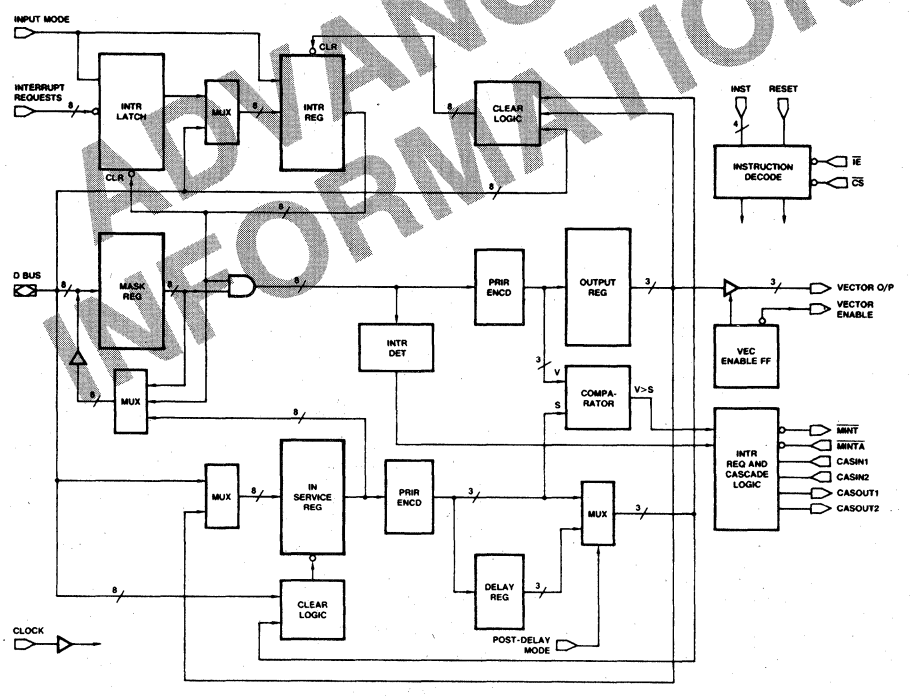
GENERAL DESCRIPTION

The Am29114 is a high-speed eight-bit priority interrupt controller that is cascadable to handle any number of interrupt request levels. Its interface specification is designed to make it suitable for use with the Am29112 microsequencer facilitating the handling of real-time micro-interrupts.

The Am29114 contains an interrupt register which is used to store requests until they are serviced, and an eight-bit in-service register which is used to store requests that are currently being serviced.

The contents of the in-service register are compared with the contents of the interrupt register. Interrupt requests having a lower or equal priority to the highest priority bit in the in-service register are disallowed, thus forming a fixed priority resolution scheme.

BLOCK DIAGRAM



BD001940

Am29114 – REAL-TIME INTERRUPT CONTROLLER

05190A

Refer to Page 13-1 for Essential Information on Military Devices

Am29116

A High-Performance 16-Bit Bipolar Microprocessor

PRELIMINARY

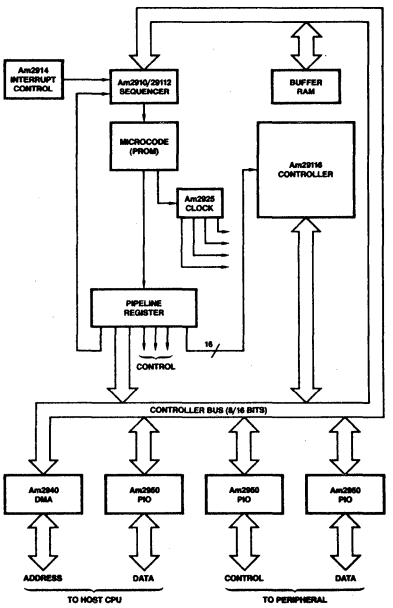
DISTINCTIVE CHARACTERISTICS

- **Optimized for High-Performance Controllers**
  Excellent solution for applications requiring speed and bit-manipulation power.
- **Fast**
  Supports 100ns microcycle time/10MHz data rate for all instructions.
- **16-Bit Barrel Shifter**
  Contains a 16-bit Barrel Shifter which can shift or rotate a word up to 15 positions in a single instruction cycle.
- **Immediate Instruction Capability**
  May be used for storing constants in microcode or for configuring a second data port.
- **Powerful Field Insertion/Extraction and Bit Manipulation Instructions**
  Rotate and Merge, Rotate and Compare and bit manipulation instructions provided for complex bit control.
- **32-Working Registers**
  Single port RAM may be configured to accept different source and destination addresses within single cycle.
- **52-Pin Hermetic DIP**

GENERAL DESCRIPTION

The Am29116 is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set is optimized for high performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applications, especially when combined with the Am29517 16 x 16 multiplier (65ns worst-case 16 x 16 multiply). In addition to its complete arithmetic and logic instruction set, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation.

BLOCK DIAGRAM



BD002200

Am29116 BASED HIGH PERFORMANCE PERIPHERAL CONTROLLER

02112C

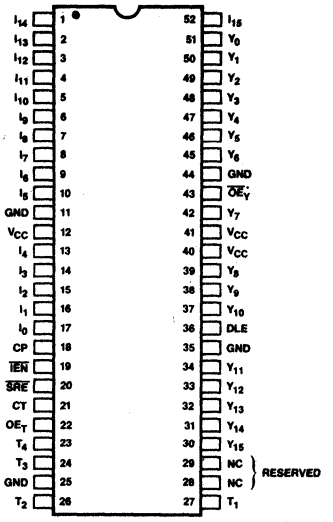
Refer to Page 13-1 for Essential Information on Military Devices

RELATED PRODUCTS

OTHER LITERATURE
• An Intelligent Fast Disk Controller using the Am29116 Application Note. • A Microprogrammed CPU Using the Am29116 Application Note.

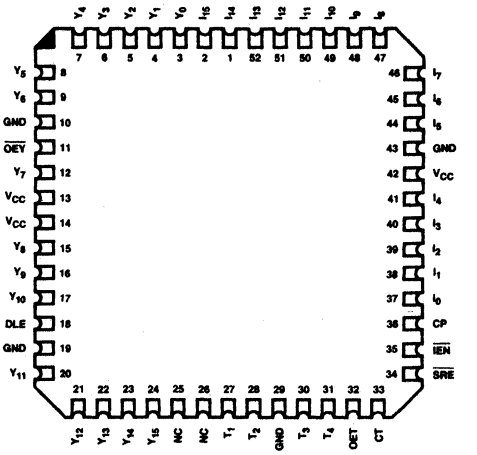
CONNECTION DIAGRAM
Top View

D-52-1



CD004190

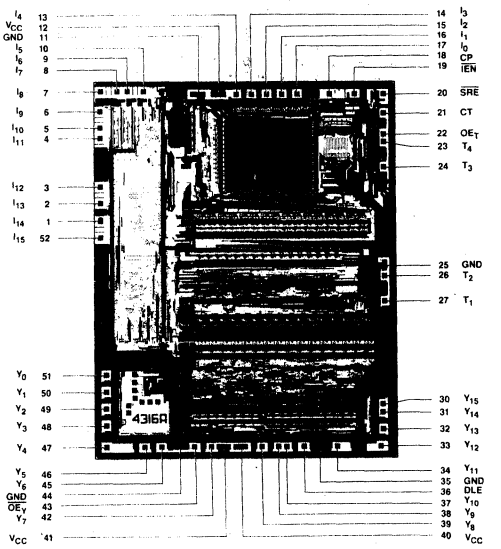
Chip-Pak™ L-52-1



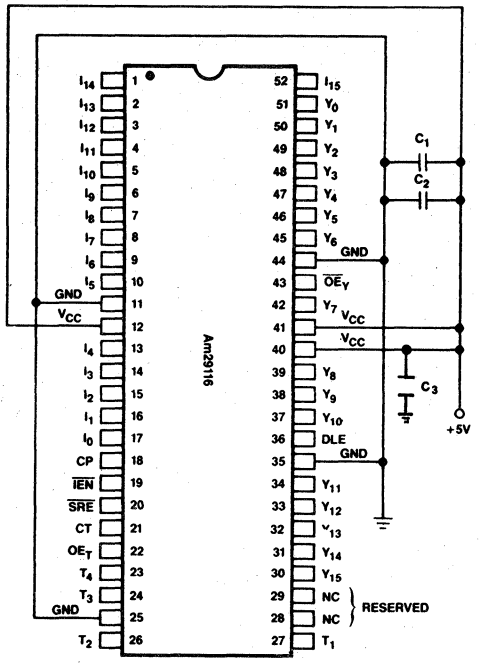
CD004180

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



V_{CC} AND GROUND PIN CONNECTIONS



CD004201

Notes: 1. All V_{CC} and all GND pins must be connected as shown. Offsets between any two V_{CC} pins or between any two GND pins should be avoided.
2. $C_1 = 1.0\mu F$, $C_2 = C_3 = 0.01\mu F$.

The C_1, C_2, and C_3 capacitors should be used to shunt low- and high-frequency noise from V_{CC}. Do not replace with one capacitor.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29116 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 52-pin CERDIP
  - L– 52-pin Chip-Pak
  - X– Dice
- **Am29116** — Device type
  - A High-Performance 16-Bit Bipolar Microprocessor

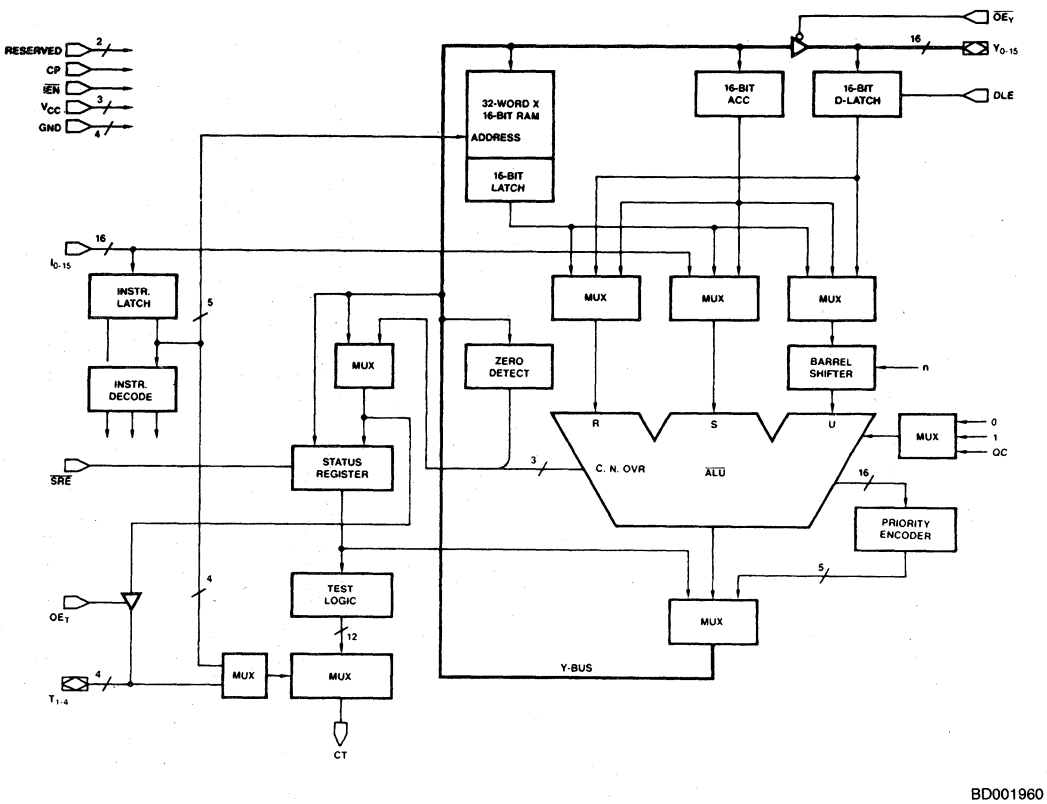
Valid Combinations	
Am29116	DC, DCB, DMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	Y_0-Y_{15}	I/O	Data Input/Output Lines. When $\overline{OE}_Y$ is HIGH, Y_0-Y_{15} are used as external data inputs which allow data to be directly loaded into the 16-bit data latch. Having $\overline{OE}_Y$ LOW allows the ALU data to be output on Y_0-Y_{15}.
36	DLE	I	Data Latch Enable. When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.
43	$\overline{OE}_Y$	I	Output Enable. When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high-impedance); when $\overline{OE}_Y$ is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).
	I_0-I_{15}	I	Sixteen Instruction Inputs. Used to select the operations to be performed in the Am29116. Also used as data inputs while performing immediate instructions.
19	$\overline{IEN}$	I	Instruction Enable. With $\overline{IEN}$ LOW, data can be written into the RAM when the clock is LOW. The Accumulator can accept data during the LOW-HIGH transition of the clock. Having $\overline{IEN}$ LOW, the Status Register can be updated when $\overline{SRE}$ is LOW. With $\overline{IEN}$ HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs. $\overline{IEN}$ should be LOW for the first half of the first cycle of an immediate instruction.
20	$\overline{SRE}$		Status Register Enable. When $\overline{SRE}$ and $\overline{IEN}$ are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either $\overline{SRE}$ or $\overline{IEN}$ HIGH will inhibit the Status Register from changing.
18	CP	I	Clock Pulse. The clock input to the Am29116. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the low period of the clock provided $\overline{IEN}$ is LOW and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-HIGH transition of the clock if $\overline{IEN}$ is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-HIGH transition of the clock.
27, 26, 24, 23	T_1-T_4	I/O	Input/Output Pin. Under the control of OE_T, the four lower status bits Z, C, N, OVR become outputs on T_1-T_4, respectively when OE_T goes HIGH. When OE_T is LOW, T_1- T_4 are used as inputs to generate the CT output.
22	OE_T	I	Output Enable. When OE_T is LOW, the 4-bit T outputs are disabled (high-impedance); when OE_T is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).
21	CT	O	Conditional Test. The condition code multiplexer selects one of the twelve condition code signals and places them on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.



BD001960

Figure 1. Detailed Am29116 Block Diagram.

ARCHITECTURE OF THE Am29116

The Am29116 is a high-performance, microprogrammable 16-bit bipolar microprocessor.

As shown in the Block Diagram, Figure 1, the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- ALU
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the $\overline{IEN}$ input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction. This two-address operation is not allowed for immediate instructions.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the $\overline{IEN}$ input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29116 on the bi-directional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29116 contains a 16-bit ALU with full carry lookahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge and rotate and compare with mask. All ALU operations can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 thru 15 do not participate. If none of bits 7 thru 0 are HIGH, the output is a binary zero. If bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable, ($\overline{SRE}$) input LOW and the $\overline{IEN}$ input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. $\overline{SRE}$ going HIGH or $\overline{IEN}$ going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry, (C) Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag 1, Flag 2, Flag 3).

With $\overline{SRE}$ LOW and $\overline{IEN}$ LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instructions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving the restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T bus. These four bits are available as outputs on the T_{1-4} outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The

multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different ways. One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, I_{0-4}, have priority over T_{1-4}, for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29116. One set controls the bidirectional, 16-bit Y bus. These outputs are enabled by placing a LOW on the $\overline{OE}$ input. A HIGH puts the Y outputs in the high-impedance state, allowing data to be input to the Data latch from an external source.

The second set of Three-State Output Buffers controls the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29116. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

INSTRUCTION SET

The instruction set of the Am29116 is very powerful. In addition to the single and two operand logical and arithmetic instructions, the Am29116 instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation. Complex instructions like rotate and merge, rotate and compare, and prioritize are executed in a single microcycle.

Three data types are supported by the Am29116.

- Bit
- Byte
- Word (16-bit)

In the byte mode data is written into the lower half of the word and the upper half is unchanged. The special case is when the status register is specified as the destination. In the byte mode the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions the CT output has the result and the Y-bus is undefined.

The Am29116 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Op

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labelled from 0 to 3. The quadrants were defined mainly for convenience in classification of the instruction set and addressing modes and can be used together with the OP CODES to distinguish the instructions.

The following pages describe each of the instruction types in detail. Throughout the description $\overline{OEy}$ is assumed to be LOW allowing ALU outputs on the Y-bus.

Table 1 illustrates operand source-destination combinations for each instruction type.

TABLE 1. OPERAND SOURCE DESTINATION COMBINATIONS

Instruction Type	Operand Combinations (Note 1)		
	Source (R/S)		Destination
Single Operand	RAM (Note 2) ACC D D(0E) D(SE) I 0		RAM ACC Y Bus Status ACC and Status
	Source (R)	Source (S)	Destination
Two Operand	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus Status ACC and Status
	Source (U)		Destination
Single Bit Shift	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
	Source (U)		Destination
Rotate n Bits	RAM ACC D		RAM ACC Y Bus
	Source (R/S)		Destination
Bit Oriented	RAM ACC D		RAM ACC Y Bus
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Merge	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Compare	D D D RAM	I I ACC I	 RAM RAM ACC

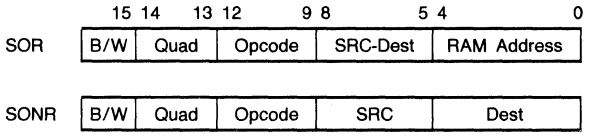
Instruction Type	Operand Combinations (Note 1)		
	Source (R)	Mask (S)	Destination
Prioritize (Note 3)	RAM ACC D	RAM ACC I 0	RAM ACC Y Bus
	Data In	Destination	Polynomial
Cyclic Redundancy Check	QLINK	RAM	ACC
No Operation	–		
	Bits Affected		
Set Reset Status	OVR, N, C, Z LINK Flag1 Flag2 Flag3		
	Source		Destination
Store Status	Status		RAM ACC Y Bus
	Source (R)	Source (S)	Destination
Status Load	D ACC D	ACC I I	Status Status and ACC
	Test Condition (CT)		
Test Status	(N⊕OVR) + Z N⊕OVR Z OVR Low C Z + $\overline{C}$ N LINK Flag 1 Flag 2 Flag 3		

Notes: 1. When there is no dividing line between the R&S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.
3. In the PRIORITIZE INSTRUCTION, OPERAND and MASK must be different sources.

SINGLE OPERAND INSTRUCTIONS

The Single Operand Instructions contain four indicators: byte or word mode, opcode, source and destination. They are further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. For a special case where 8-bit to 16-bit conversion is needed, the Am29116 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16-bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both ACC and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS



SINGLE OPERAND INSTRUCTION

I5 I4 I3 I2 9 8 5 4 0

Instruction[1]	B/W[2]	Quad[3]	Opcode			R/S[4]		Dest[4]	RAM Address		
SOR	0 = B 1 = W	10	1100	MOVE	SRC → Dest	0000	SORA	RAM	ACC	00000	R00	RAM Reg 00
			1101	COMP	$\overline{SRC}$ → Dest	0010	SORY	RAM	Y Bus	..	..	....
			1110	INC	SRC + 1 → Dest	0011	SORS	RAM	Status	11111	R31	RAM Reg 31
			1111	NEG	$\overline{SRC}$ + 1 → Dest	0100	SOAR	ACC	RAM			
						0110	SODR	D	RAM			
						0111	SOIR	I	RAM			
						1000	SOZR	0	RAM			
						1001	SOZER	D(0E)	RAM			
						1010	SOSER	D(SE)	RAM			
						1011	SORR	RAM	RAM			

Instruction	B/W	Quad	Opcode			R/S[4]			Destination	
SONR	0 = B 1 = W	11	1100	MOVE	SRC → Dest	0100	SOA	ACC	00000	NRY	Y Bus
			1101	COMP	$\overline{SRC}$ → Dest	0110	SOD	D	00001	NRA	ACC
			1110	INC	SRC + 1 → Dest	0111	SOI	I	00100	NRS	Status[5]
			1111	NEG	$\overline{SRC}$ + 1 → Dest	1000	SOZ	0	00101	NRAS	ACC, Status[5]
						1001	SOZE	D(0E)			
						1010	SOSE	D(SE)			

Notes:
1. The instruction mnemonic designates different instruction formats used in the Am29116. They are useful in assembly microcode with the System 29 AMDASM™ meta assembler.
2. B = Byte Mode, W = Word Mode.
3. See Instruction Set description.
4. R = Source; S = Source; Dest = Destination.
5. When status is destination,
   Status i ← Yi i = 0 to 3 (Byte mode)
   i = 0 to 7 (Word mode)

Y BUS AND STATUS – SINGLE OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y — Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR	MOVE	SRC → Dest	0 = B	Y ← SRC	NC	NC	NC	NC	0	U	0	U
SONR	COMP	$\overline{SRC}$ → Dest	1 = W	Y ← $\overline{SRC}$	NC	NC	NC	NC	0	U	0	U
	INC	SRC +1 → Dest		Y ← SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	$\overline{SRC}$ +1 → Dest		Y ← $\overline{SRC}$ +1	NC	NC	NC	NC	U	U	U	U

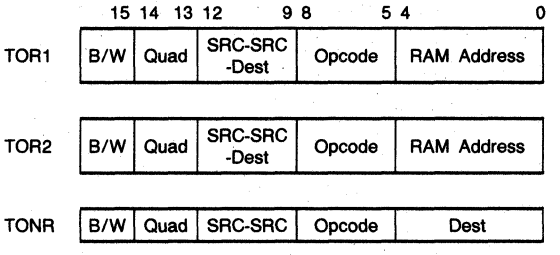
SRC = Source
U = Update
NC = No Change

0 = Reset
1 = Set
i = 0 to 15 when not specified

TWO OPERAND INSTRUCTIONS

The Two Operand Instructions contain five indicators: byte or word mode, opcode, R source, S source, and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS



TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
TOR1	0 = B 1 = W	00	0000 0010 0011 1000 1010 1011 1100 1110 1111	TORAA TORIA TODRA TORAY TORIY TODRY TORAR TORIR TODRR	RAM I D RAM I D RAM I D	ACC ACC RAM ACC I RAM ACC I RAM	ACC ACC ACC Y Bus Y Bus Y Bus RAM RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[2] SUBS SUBSC[2] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry $\overline{R \cdot S}$ $\overline{R \cdot S}$ $\overline{R \oplus S}$ $\overline{R + S}$ $\overline{R + S}$ $\overline{R \oplus S}$	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**			**R[1]**	**S[1]**	**Dest[1]**	**Opcode**			**RAM Address**		
TOR2	0 = B 1 = W	10	0001 0010 0101	TODAR TOAIR TODIR	D ACC D	ACC I I	RAM RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[2] SUBS SUBSC[2] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry $\overline{R \cdot S}$ $\overline{R \cdot S}$ $\overline{R \oplus S}$ $\overline{R + S}$ $\overline{R + S}$ $\overline{R \oplus S}$	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Note 1: R = Source
S = Source
Dest = Destination
Note 2: During subtraction the carry is interpreted as $\overline{\text{borrow}}$.

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad	R[1]	S[1]	Opcode			Destination		
TONR	0 = B 1 = W	11	0001 TODA D 0010 TOAI ACC 0101 TODI D	ACC I I	0000 SUBR S minus R 0001 SUBRC S minus R with carry 0010 SUBS R minus S 0011 SUBSC R minus S with carry 0100 ADD R plus S 0101 ADDC R plus S with carry 0110 AND $\underline{R \bullet S}$ 0111 NAND $\overline{R \bullet S}$ 1000 EXOR $\underline{R \oplus S}$ 1001 NOR $\overline{R + S}$ 1010 OR $\underline{R + S}$ 1011 EXNOR $\overline{R \oplus S}$			00000 NRY Y Bus 00001 NRA ACC 00100 NRS Status[2] 00101 NRAS ACC, Status[2]		

Notes 1: R = Source
S = Source
2: When status is destination,
Status $i \leftarrow Y_i$ i = 0 to 3 (Byte mode)
i = 0 to 7 (Word mode)
3: During subtraction the carry is interpreted as $\overline{\text{borrow}}$.

Y BUS AND STATUS CONTENTS – TWO OPERAND INSTRUCTIONS

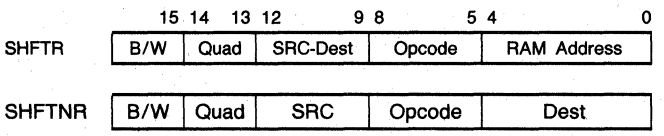
Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag 1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	SUBR	S minus R	0 = B	$Y \leftarrow S + \overline{R} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry	1 = w	$Y \leftarrow S + \overline{R} + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R + \overline{S} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} + QC$	NC	NC	NC	NC	U	U	U	U
	ADD	R plus S		$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \cdot S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	NAND	$\overline{R \cdot S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	0	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

SINGLE BIT SHIFT INSTRUCTIONS

The Single Bit Shift Instructions contain four indicators: byte or word mode, direction and shift linkage, source and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 2. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QN ⊕ QOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 3. The N and Z bits of the Status register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN ⊕ QOVR is useful for Two's Complement multiplication.

SINGLE BIT SHIFT FIELD DEFINITIONS:



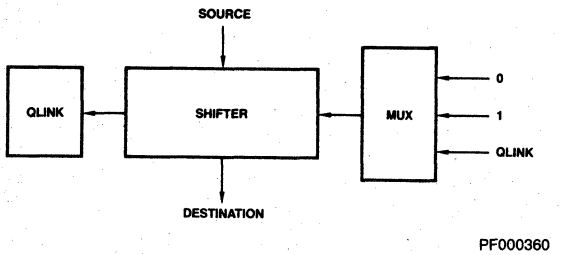


Figure 2. Shift Up Function.

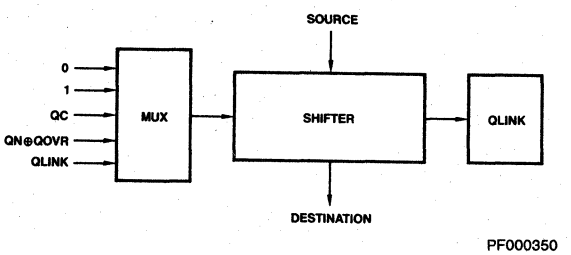


Figure 3. Shift Down Function.

SINGLE BIT SHIFT INSTRUCTIONS

SINGLE BIT SHIFT

Instruction	B/W	Quad	U[1]			Dest[1]	Opcode				RAM Address		
SHFTR	0 = B 1 = W	10	0110 0111	SHRR SHDR	RAM D	RAM RAM	0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Instruction	B/W	Quad	U[1]			Opcode				Destination		
SHFTNR	0 = B 1 = W	11	0110 0111	SHA SHD	ACC D	0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000 00001	NRY NRA	Y Bus ACC

Note 1. U = Source
Dest = Destination

Y BUS AND STATUS – SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
			0 = B	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-8}$ for i = 9 to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN⊕QOVR	1 = W	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 14; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
			0 = B	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 6; $Y_i \leftarrow SRC_{i-7}$, i = 8 to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

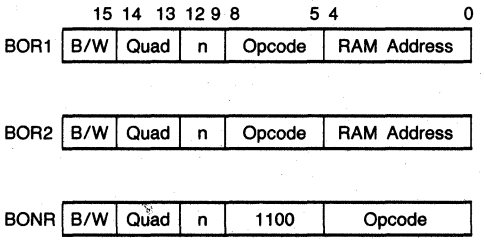
*Shifted Output is loaded into the QLINK.

6

BIT ORIENTED INSTRUCTIONS

The Bit Oriented Instructions contain four indicators: byte or word mode, operation, source/destination, and the bit position of the bit to be operated on (Bit 0 is the least significant bit). They are further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The operations which can be performed are: Set Bit n which forces the n^{th} bit to a ONE leaving other bits unchanged; Reset Bit n which forces the n^{th} bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2^n, which loads ONE in Bit position n and ZERO in all other bit positions; Load $\overline{2^n}$ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n which subtracts 2^n from the operand. For all the Load, Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status register is affected.

BIT ORIENTED FIELD DEFINITIONS



BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n	Opcode			RAM Address		
BOR1	0 = B 1 = W	11	0 to 15	1101 1110 1111	SETNR RSTNR TSTNR	Set RAM, bit n Reset RAM, bit n Test RAM, bit n	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**Opcode**			**RAM Address**		
BOR2	0 = B 1 = W	10	0 to 15	1100 1101 1110 1111	LD2NR LDC2NR A2NR S2NR	$2^n \rightarrow$RAM $\overline{2^n} \rightarrow$RAM RAM plus $2^n \rightarrow$RAM RAM minus $2^n \rightarrow$RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**				**Opcode**		
BONR	0 = B 1 = W	11	0 to 15	1100			00000 00001 00010 00100 00101 00110 00111 10000 10001 10010 10100 10101 10110 10111	TSTNA RSTNA SETNA A2NA S2NA LD2NA LDC2NA TSTND RSTND SETND A2NDY S2NDY LS2NY LDC2NY	Test ACC, bit n Reset ACC, bit n Set ACC, bit n ACC plus $2^n \rightarrow$ACC ACC minus $2^n \rightarrow$ACC $2^n \rightarrow$ACC $\overline{2^n} \rightarrow$ACC Test D, bit n Reset D, bit n Set D, bit n D plus $2^n \rightarrow$ Y BUS D minus $2^n \rightarrow$ Y Bus $2^n \rightarrow$ Y Bus $\overline{2^n} \rightarrow$ Y Bus

BIT ORIENTED INSTRUCTIONS

Y BUS AND STATUS – BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
BOR1	SETNR	Set RAM Bit n	0 = B	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	RSTNR	Reset RAM, Bit n	1 = W	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	TSTNR	Test Ram, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow SRC_n$	NC	NC	NC	NC	0	U	0	U
BOR2	LD2NR	$2^n \rightarrow$ RAM		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NR	$\overline{2^n} \rightarrow$ RAM		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	A2NR	RAM + $2^n \rightarrow$ RAM		$Y_i \leftarrow$ RAM + 2^n	NC	NC	NC	NC	U	U	U	U
	S2NR	RAM – $2^n \rightarrow$ RAM		$Y_i \leftarrow$ RAM – 2^n	NC	NC	NC	NC	U	U	U	U
BONR	TSTNA	Test ACC, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow ACC_n$	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	ACC + $2^n \rightarrow$ ACC		$Y_i \leftarrow$ ACC + 2^n	NC	NC	NC	NC	U	U	U	U
	S2NA	ACC – $2^n \rightarrow$ ACC		$Y_i \leftarrow$ ACC – 2^n	NC	NC	NC	NC	U	U	U	U
	LD2NA	$2^n \rightarrow$ ACC		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NA	$\overline{2^n} \rightarrow$ ACC		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	TSTND	Test D, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow D_n$	NC	NC	NC	NC	0	U	0	U
	RSTND	Reset D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	D + $2^n \rightarrow$ Y Bus		$Y \leftarrow D + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NDY	D – $2^n \rightarrow$ Y Bus		$Y \leftarrow D - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NY	$2^n \rightarrow$ Y Bus		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	$\overline{2^n} \rightarrow$ Y Bus		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D Latch but Y Bus.

ROTATE BY n BITS INSTRUCTIONS

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y-bus or both. An example of this instruction is given in Figure 4. In the Word mode, all 16-bits are rotated up while in the Byte mode, only lower 8-bits (0-7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

EXAMPLE: n = 4, Word Mode

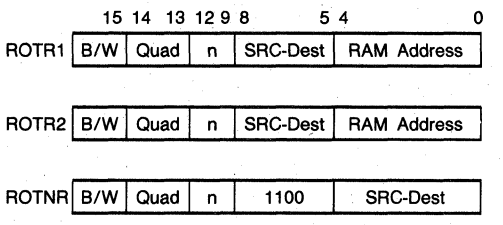
Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: n = 4, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 4. Rotate by n Example

ROTATE BY n BITS FIELD DEFINITIONS



ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	Dest[1]	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**	**n**			**U[1]**	**Dest[1]**	**RAM Address**		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**	**n**						**U[1]**	**Dest[1]**
ROTNR	0 = B 1 = W	11	0 to 15	1100				11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D D ACC ACC	Y Bus ACC Y Bus ACC

Note 1: U = Source
Dest = Destination

Y BUS AND STATUS – ROTATE BY n BITS INSTRUCTIONS

Instruction	Op-code	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n) \bmod 16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_{i+8} = SRC_{(i-n) \bmod 8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{8-n}	0	U

SRC = Source
U = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND MERGE INSTRUCTION

The Rotate and Merge Instructions contain five indicators: byte or word mode, rotated source, non-rotated source/destination, mask and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 5. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit by bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the i^{th} bit of the R input as the i^{th} output bit, while ONE in bit i will select the i^{th} rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 6.

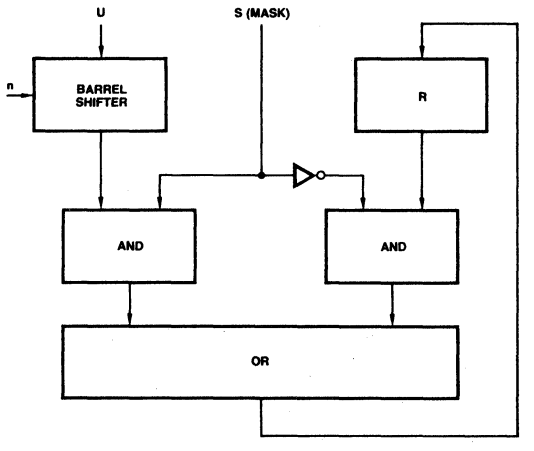
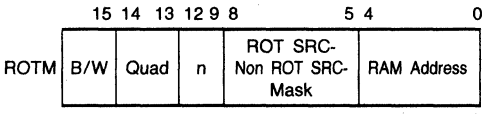


Figure 5. Rotate and Merge Function.

ROTATE AND MERGE FIELD DEFINITIONS:



EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 6. Rotate and Merge Example.

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n		U[1]	R/Dest[1]	S[1]	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111 MDAI 1000 MDAR 1001 MDRI 1010 MDRA 1100 MARI 1110 MRAI	D D D D ACC RAM	ACC ACC RAM RAM RAM ACC	I RAM I I ACC I I	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Note 1. U = Rotated Source
R/Dest = Non-Rotated Source and Destination
S = Mask

Y BUS AND STATUS – ROTATED MERGE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1=W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND COMPARE INSTRUCTIONS

The Rotate and Compare Instructions contain five indicators: byte or word mode, rotated source, non-rotated source, mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare instruction is illustrated in Figure 7. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 8.

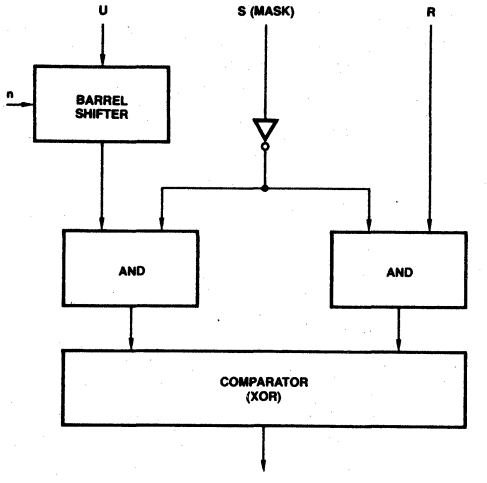
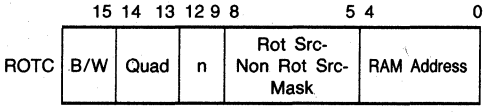


Figure 7. Rotate and Compare Function.

ROTATE AND COMPARE FIELD DEFINITIONS



EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111

Z (status) = 1

Figure 8. Rotate and Compare Examples.

ROTATE AND COMPARE INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	R[1]	S[1]	RAM Address		
ROTC	0=B 1=W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	I I ACC I	00000 .. 11111	R00 .. R31	RAM Reg 00 ... RAM Reg 31

Note 1. U = Rotated Source
R = Non-Rotated Source
S = Mask

Y BUS AND STATUS – ROTATE AND COMPARE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

PRIORITIZE INSTRUCTION

The Prioritize Instructions contain four indicators: byte or word mode, operand source (R), mask source (S) and destination. They are further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 9. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 10 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the status register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

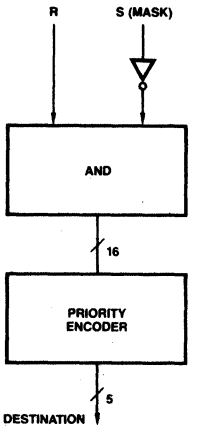


Figure 9. Prioritize Function.

PRIORITIZE INSTRUCTION FIELD DEFINITIONS

15	14	13 12	9 8	5 4	0
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (S)	
B/W	Quad	Mask (S)	Destination	RAM Address/ Source (R)	
B/W	Quad	Mask (S)	Source (R)	RAM Address/ Destination	
B/W	Quad	Mask (S)	Source (R)	Destination	

WORD MODE		BYTE MODE*	
Highest Priority Active Bit	**Encoder Output**	**Highest Priority Active Bit**	**Encoder Output**
None	0	None	0
15	1	7	1
14	2	6	2
.	.	.	.
.	.	.	.
1	15	1	7
0	16	0	8

*Bits 8 through 15 do not participate.

Figure 10.

PRIORITIZE INSTRUCTION

Instruction	B/W	Quad	Destination			Source (R)			RAM Address/Mask (S)		
PRT1	0 = B 1 = W	10	1000 1010 1011	PRIA PR1Y PR1R	ACC Y Bus RAM	0111 1001	RPT1A PR1D	ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Destination**			**RAM Address/Source (R)**		
PRT2	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	Acc 0 I	0000 0010	PR2A PR2Y	ACC Y Bus	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**RAM Address/Dest**		
PRT3	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0011 0100 0110	PR3R PR3A PR3D	RAM ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**Destination**		
PRTNR	0 = B 1 = W	11	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0100 0110	PRTA PRTD	ACC D	00000 00001	NRY NRA	Y Bus ACC

Y BUS AND STATUS - PRIORITIZE INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2		1 = W	$Y_i \leftarrow$ CODE ($SCR_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	$Y_i \leftarrow$ CODE ($SCR_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	U	0	U

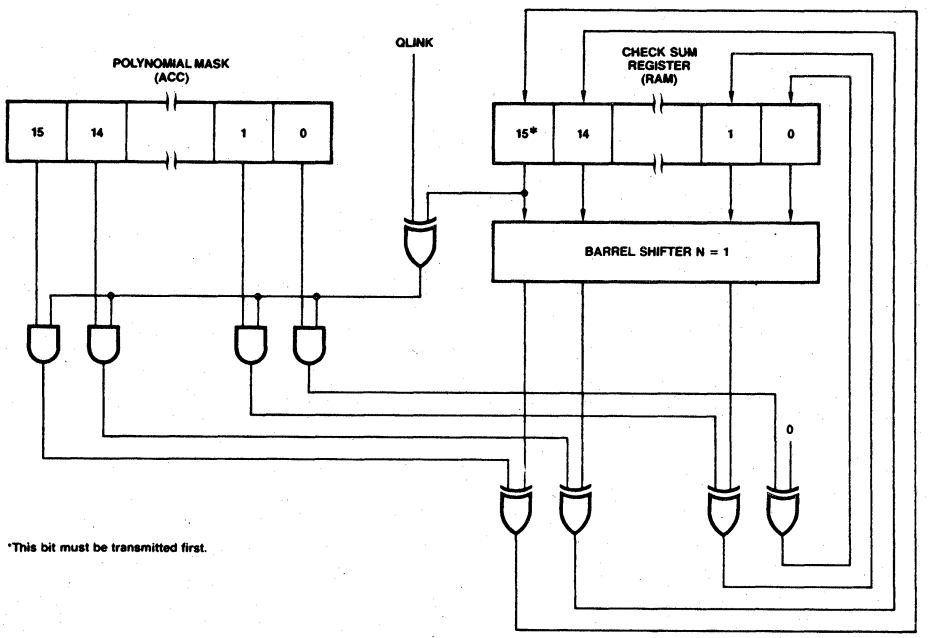
SRC = Source NC = No Change 1 = Set
U = Update 0 = Reset i = 0 to 15 when not specified

CRC INSTRUCTION

The CRC (Cyclic-Redundancy-Check) Instructions contain one indicator: address of a RAM register to use as the check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 11 illustrates the method used to generate these check bits for the CRC Forward function and Figure 12 illustrates method used for the 2CRC Reverse function. The ACC serves as a polynominal mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N and Z bits are affected and the OVR and C bits of the Status register are forced to ZERO.

CYCLIC-REDUNDANCY-CHECK DEFINITIONS:

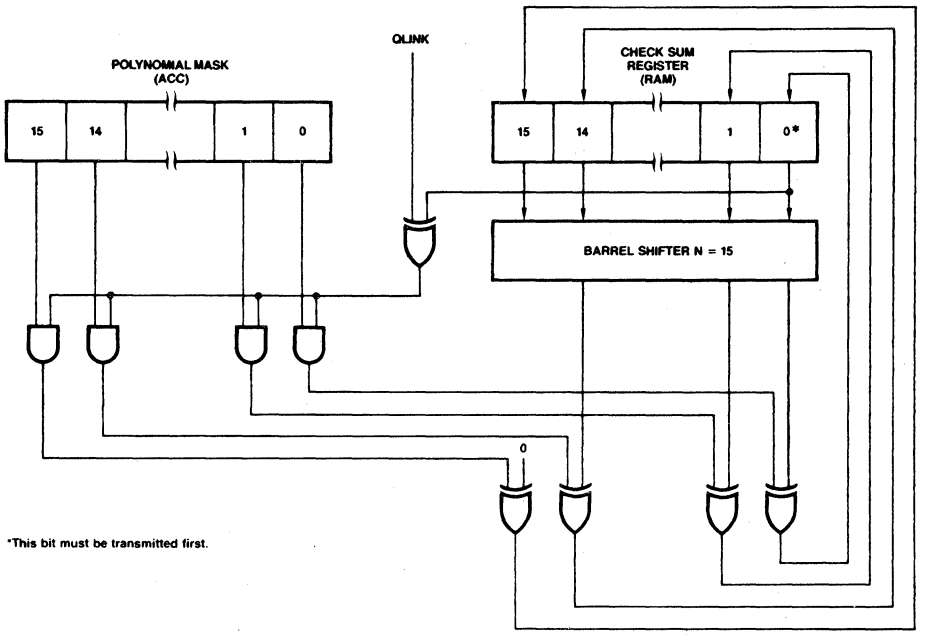
	15	14	13	12	9	8	5	4	0
CRCF	1	Quad	0110		0011		RAM Address		
CRCR	1	Quad	0110		1001		RAM Address		



PF000330

Figure 11. CRC Forward Function.

CRC INSTRUCTION



PF000320

Figure 12. CRC Reverse Function.

CYCLIC REDUNDANCY CHECK

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Y BUS AND STATUS – CYCLIC REDUNDANCY CHECK

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i] \oplus RAM_{i-1}$ for i = 15 to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i] \oplus RAM_{i+1}$ for i = 14 to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

*QLINK is loaded with the shifted out bit from the checksum register.

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

STATUS INSTRUCTIONS

Status Instructions – The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register (Figure 13), are to be set (forced to a ONE).

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	LINK	OVR	N	C	Z

MPR-775

Figure 13. Status Byte.

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register, are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; byte/word and a second indicator that specifies the destination of the status register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The status register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode the upper byte is unchanged or loaded with all ZEROs respectively.

The Load Status instructions are included in the single operand and two operand instruction types.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the Status register (QZ, QC, QN, QOVR, QLINK, QFlag1, QFlag 2, and QFlag3), four logical functions (QN ⊕ QOVR, (QN ⊕ QOVR) + QZ, QZ + $\overline{QC}$ and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The status register may also be tested via the bidirectional T bus. The code to test the status register via T bus is similar to the code used by instruction lines I_1 to I_4 as shown below. Instruction lines I_{0-4} have priority over T bus for testing the status register on CT output. See the discussion on the status register for a full description.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

STATUS

	15	14	13	12	9	8	5	4	0
SETST	0	Quad	1011	1010	Opcode				
RSTST	0	Quad	1010	1010	Opcode				
SVSTR	B/W	Quad	0111	1010	RAM Address/Dest				
SVSTNR	B/W	Quad	0111	1010	Destination				

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011	SONCZ	Set OVR, N, C, Z
					00101	SL	Set LINK
					00110	SF1	Set Flag1
					01001	SF2	Set Flag2
					01010	SF3	Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1011	1010	00011	RONCZ	Reset OVR, N, C, Z
					00101	RL	Reset LINK
					00110	RF1	Set Flag1
					01001	RF2	Set Flag2
					01010	RF3	Set Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Dest**		
SVSTR	0 = B 1 = W	10	0111	1010	00000	R00	RAM Reg 00
					...	...	....
					11111	R31	RAM Reg 31
					Destination		
SVSTNR	0 = B 1 = W	11	0111	1010	00000	NRY	Y Bus
					00001	NRA	ACC

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000	TNOZ	Test (N⊕OVR) + Z
					00010	TNO	Test N⊕OVR
					00100	TZ	Test Z
					00110	TOVR	Test OVR
					01000	TLOW	Test LOW
					01010	TC	Test C
					01100	TZC	Test Z + $\overline{C}$
					01110	TN	Test N
					10000	TL	Test LINK
					10010	TF1	Test Flag1
					10100	TF2	Test Flag2
					10110	TF3	Test Flag3

Note: $\overline{IEN}$ · test status instruction has priority over T_{1-4} instruction.

Y BUS AND STATUS – FOR STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow 1$ for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow 0$ for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status for i – 0 to 7; $Y_i \leftarrow 0$ for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC
Test	TNOZ	Test (N⊕OVR) + Z	0 = B	**	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test N⊕OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test Z + $\overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

**Y-Bus is Undefined.

NO-OP INSTRUCTION

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29116. It preserves the status register, RAM register and the ACC register.

NO OPERATION FIELD DEFINITION

	15	14	13	12	9	8	5	4	0
NOOP	0	11	1000		1010		00000		

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NOOP	0	11	1000	1010	00000

Y BUS AND STATUS – NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
NOOP		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified
*Y-Bus is undefined.

SUMMARY OF MNEMONICS

Instruction Type

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRT1	Prioritize RAM; Type 1
PRT2	Prioritize RAM; Type 2
PRT3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic Redundancy Check Forward
CRCR	Cyclic Redundancy Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D(0E) to RAM
SOSER	Single Operand D(SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D(0E)
SOSE	Single Operand D(SE)
NRY	Non-RAM Y Bus
NRA	Non-RAM ACC
NRS	Non-RAM Status
NRAS	Non-RAM ACC, Status

Two Operand

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y Bus
TORIY	Two Operand RAM, I to Y Bus
TODRY	Two Operand D, RAM to Y Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate n Bits

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask

CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM
PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition

ADD	Add without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y Bus

Subtraction

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y Bus

Logical Operations

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with LINK Insert
SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with LINK Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads

LD2NR	Load 2^n into RAM
LDC2NR	Load $\overline{2^n}$ into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load $\overline{2^n}$ into ACC
LD2NY	Place 2^n on Y Bus
LDC2NY	Place $\overline{2^n}$ on Y Bus

Bit Oriented

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set LINK Bit in Status Register
SF1	Set Flag1 Bit in Status Register
SF2	Set Flag2 Bit in Status Register
SF3	Set Flag3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset LINK Bit in Status Register
RF1	Reset Flag1 Bit in Status Register
RF2	Reset Flag2 Bit in Status Register
RF3	Reset Flag3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test

TNOZ	Test (N ⊕ OVR) + Z
TNO	Test N ⊕ OVR
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test Z + $\overline{C}$
TN	Test Negative Bit
TL	Test LINK Bit
TF1	Test Flag1 Bit
TF2	Test Flag2 Bit
TF3	Test Flag3 Bit

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Case) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_{0-5} T_{1-4} CT	I_{OH} = −1.6mA/−1.2mA (COM'L/MIL)	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_{0-15} T_{1-4} CT	I_{OL} = 16mA/12mA (COM'L/MIL)			0.5	Volts
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 6)		All Inputs		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 6)		All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN	All Inputs	I_{IN} = −18mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX V_{IN} = 0.5 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ DLE I_{0-4} I_{5-15} $\overline{OE_T}$ $\overline{OE_Y}$ CP T_{1-4} Y_{0-15}				−0.50 −0.50 −1.00 −1.00 −0.50 −0.50 −0.50 −1.50 −0.55 −0.55	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX V_{IN} = 2.4 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ DLE I_{0-4} I_{5-15} $\overline{OE_T}$ $\overline{OE_Y}$ CP T_{1-4} Y_{0-15}				50 50 100 100 50 50 50 150 100 100	µA
I_I	Input HIGH Current	V_{CC} = MAX V_{IN} = 5.5 Volts	All Inputs				1.0	mA
I_{OZH}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX V_O = 2.4 Volts (Note 4)	T_{1-4} Y_{0-15}				100	µA
I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX V_O = 0.5 Volts (Note 4)	T_{1-4} Y_{0-15}				−550	µA
I_{OS}	Output Short Circuit Current	V_{CC} = MAX + 0.5 Volts V_O = 0.5 Volts (Note 3)			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	COM'L	T_{AL} = 0 to 70°C (Note 7)			735	mA
				T_A = 70°C			535	
			MIL	T_C = −55 to 125°C (Note 7)			745	
				T_C = 125°C			485	

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-15}, T_{1-4} are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
7. Cold start.

SWITCHING CHARACTERISTICS

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to+70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
	I_{0-4} (ADDR)	79	84	–
	I_{0-15} (DATA)	79	84	–
	I_{0-15} (INSTR)	79	84	48
Input	DLE	58**	60	–
	T_{1-4}	–	–	39
	CP	56	62	36
	Y_{0-15}	62**	64*	–
	$\overline{IEN}$	–	–	43

*Y_{0-15} must be stored in the Data Latch and is source disabled before the delay to Y_{0-15} as an output can be measured.
**Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
(C_L = 5pF for disable only)

		Enable		Disable	
From Input	To Output	t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	20	20	20	20
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	20	30
DLE	–	15
$\overline{IEN}$	22	–

D. Setup and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	Do Not Change		(t_{h7}) 0	Two ADDR (Destination)
I_{0-5} (DATA)	CP	–	–	(t_{s8}) 65	(t_{h8}) 0	
I_{0-15} (INSTR)	CP	(t_{s3}) 38†	(t_{h3}) † 17	(t_{s9}) 65	(t_{h9}) 0	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 0	Disable
$\overline{IEN}$ LOW	CP	– (t_{s5}) 20	– (t_{h5})† 0	(t_{s11}) 22 –	(t_{h11})†† 0 –	Enable / Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 17	(t_{h12}) 0	
Y	CP	–	–	(t_{s13}) 44	(t_{h13}) 0	
Y	DLE	(t_{s6}) 10	(t_{h6}) 6	–	–	
DLE	CP	–	–	(t_{s14}) 42	(t_{h14}) 0	

†Timing for immediate instruction for first cycle.
†† Status register and accumulator destination only.

Notes on Testing

Incoming test procedures on this device should be carefull planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failure due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5—8ns. Inductance in the ground cable may allow may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

SWITCHING CHARACTERISTICS (Cont.)

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to+125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
	I_{0-4} (ADDR)	100	103	–
	I_{0-15} (DATA)	100	103	–
	I_{0-15} (INSTR)	100	103	50
Input	DLE	68	70	–
	T_{1-4}	–	–	46
	CP	70	73	43
	Y_{0-15}	70	72	–
	$\overline{IEN}$	–	–	50

*Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured.
**Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
(C_L = 5pF for disable only)

		Enable		Disable	
From Input	To Output	t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	25	25	25	25
OE_T	T_{1-4}	30	30	30	30

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	25	50
DLE	–	20
$\overline{IEN}$	26	–

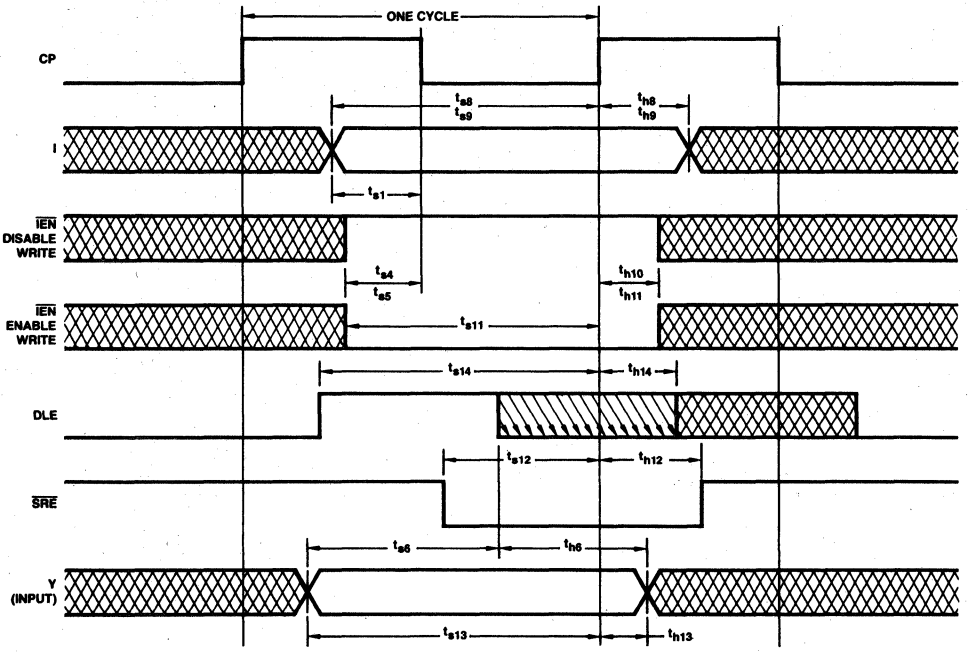
D. Set-up and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	Do Not Change		(t_{h7}) 0	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 76	(t_{h8}) 3	
I_{0-15} (INSTR)	CP	(t_{s3})† 57	(t_{h3})† 17	(t_{s9}) 76	(t_{h9}) 3	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 1	Disable
$\overline{IEN}$ LOW	CP	– (t_{s5}) 20	– (t_{h5})† 3	(t_{s11}) 28 –	(t_{h11})†† 1 –	Enable / Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 19	(t_{h12}) 0	
Y	CP	–	–	(t_{s13}) 50	(t_{h13}) 2	
Y	DLE	(t_{s6}) 11	(t_{h6}) 7	–	–	
DLE	CP	–	–	(t_{s14}) 50	(t_{h14}) 0	

†Timing for immediate instruction for first cycle.
†† Status register and accumulator destination only.

Am29116

SINGLE ADDRESS ACCESS TIMING



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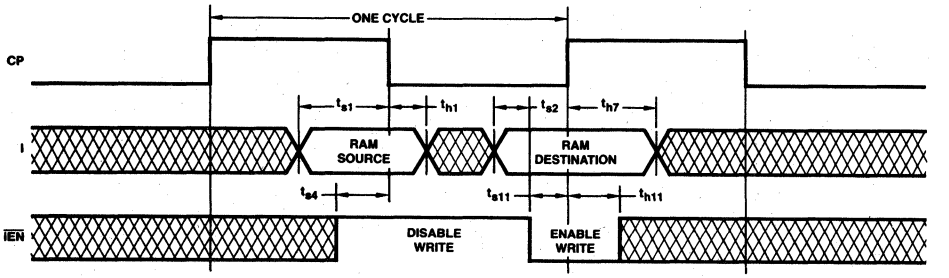
If t_{h6} is satisfied, t_{h13} need not be satisfied.

DOUBLE ADDRESS ACCESS TIMING



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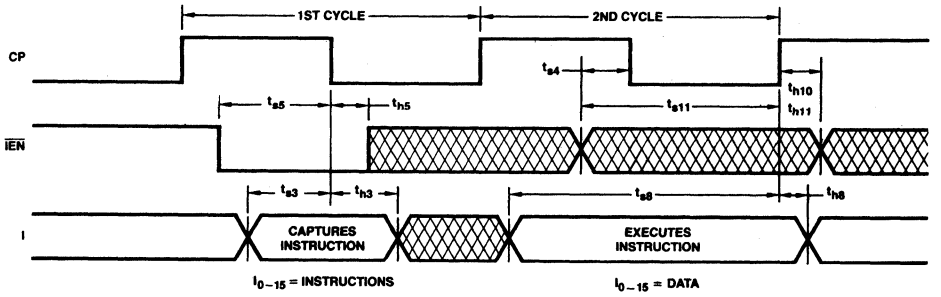
IMMEDIATE INSTRUCTION CYCLE TIMING



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Am29116A/29L116A

A High-Performance 16-Bit Bipolar Microprocessor

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

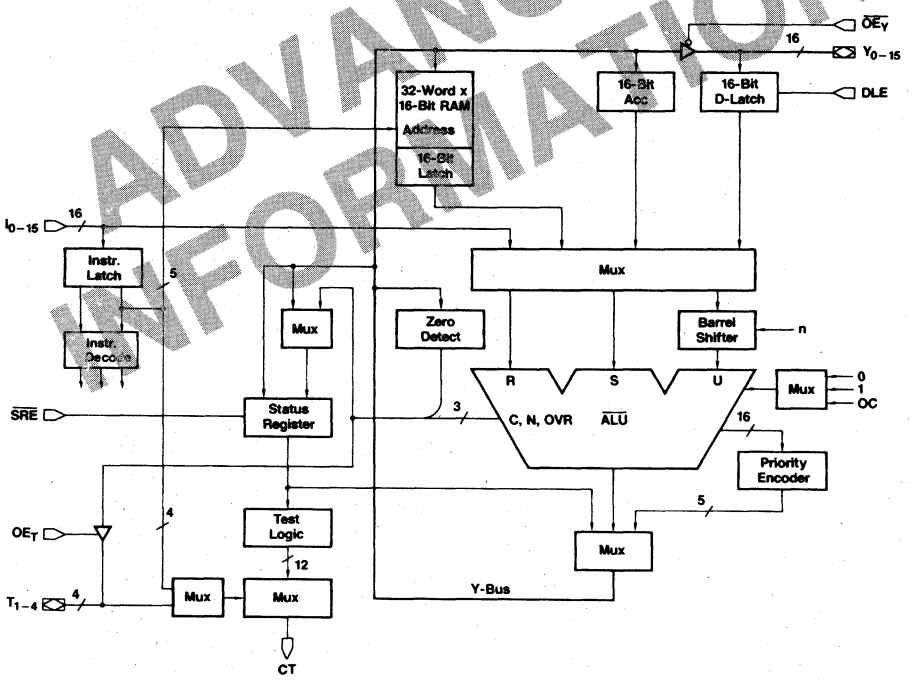
- **Second Generation of the Am29116 16-Bit Microprocessor**
  Internal ECL circuitry and second generation of Ion implanted Oxide-Isolated (IMOX™) process technology are combined to provide a faster version of the Am29116 and a lower power version of the 29116
- **Plug-In Replacement for the Am29116**
  The Am29116A and Am29L116A are pin-for-pin replacements for the Am29116
- **Improved Speed**
  The 29116A has 25 – 30% speed improvement on the critical paths relative to Am29116
- **Reduced Power**
  The 29L116A operates at reduced power requirements and compatible performace relative to the 29L116

GENERAL DESCRIPTION

The Am29116A/L116A microprogrammable 16-bit bipolar microprocessors were fabricated using the second generation of AMD's IMOX process technology. The architectures of the Am29116A/L116A are identical to the Am29116's, optimized for high-performance peripheral controllers such as graphics controllers, disk controllers, communication controllers, front-end concentrators and modems. The Am29116A is also extremely suitable for high-speed, general-purpose 16-bit CPU applications when combined with the Am29517A 16 x 16 multiplier.

BLOCK DIAGRAM

Am29116A



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IMOX is trademark of Advanced Micro Devices, Inc.

05761A

Refer to Page 13-1 for Essential Information on Military Devices

Am29117

A High-Performance 16-Bit Bipolar Microprocessor

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Optimized for High-Performance Controllers**
  Architecture and instruction set optimized for high-performance, intelligent controllers
- **Flow-Through Architecture**
  Separate input and output ports avoid bus turn-around for higher throughput
- **32 Working Registers**
  Contains 32 working registers with latched outputs
- **Fast**
  Supports 100ns microcycle time/10MHz data rate for all instructions
- **16-Bit Barrel Shifter**
  Contains a 16-bit Barrel Shifter which can shift or rotate a word up to 15 positions in a single instruction cycle
- **68-Pin Pin Grid Array Package**

GENERAL DESCRIPTION

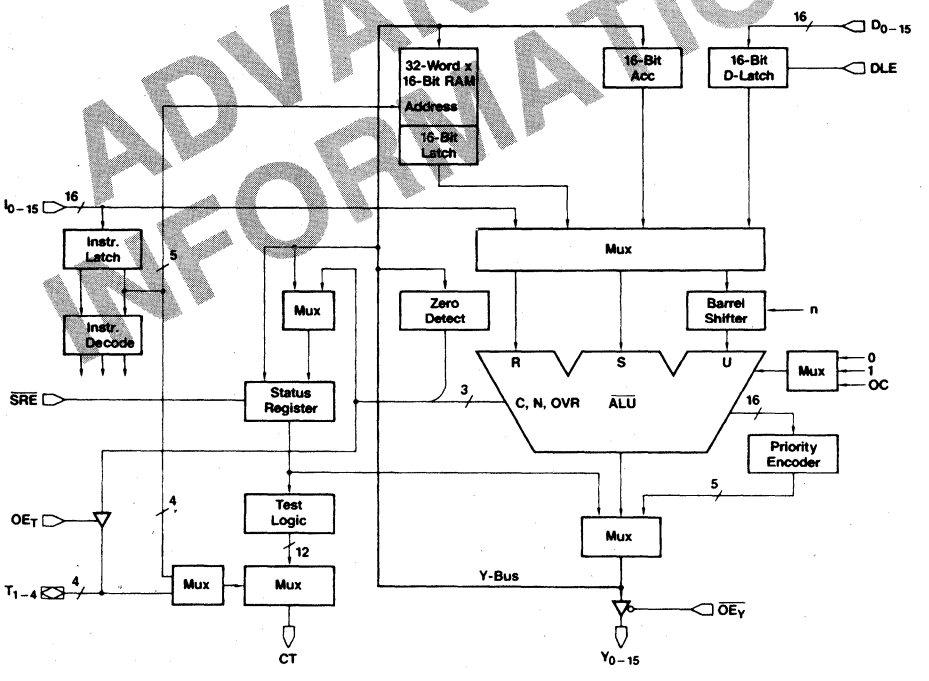
The Am29117 is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set are identical to the Am29116's except for the I/O bus structure. Since the device has separate input and output ports, designers can avoid quick bus turnaround requirements.

The architecture and instruction set are not only optimized for high-performance peripheral controllers, but also suitable for microprogrammed processor applications when combined with the Am29517A 16 x 16 multiplier.

The instruction set contains unique functions besides ordinary logic and arithmetic functions: bit manipulation instructions (set, reset and test), rotate merge/compare instructions, prioritize instruction and CRC instruction.

BLOCK DIAGRAM

Am29117



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Refer to Page 13-1 for Essential Information on Military Devices

Am29118

Eight-Bit Am29116 I/O Support

DISTINCTIVE CHARACTERISTICS

- Eight-bit bidirectional I/O port
- Reads both registers on A-port
- Separate clock, clock enable and three-state output enable to synchronize data between two bidirectional buses
- 24mA output current sink capability
- 24-pin slim package
- Additional accumulator to support certain Am29116 applications.

GENERAL DESCRIPTION

The Am29118 is an eight-bit wide bidirectional parallel data input/output port designed to provide an additional accumulator when used with the Am29116 or with any microprocessor with single bidirectional data port. In addition, it can be used as a parallel data input/output port, like the Am2952. The Am29118 is a metal mask option of the Am2952A, and so requires no additional pins to support the Am29116 input/output structure.

BLOCK DIAGRAM

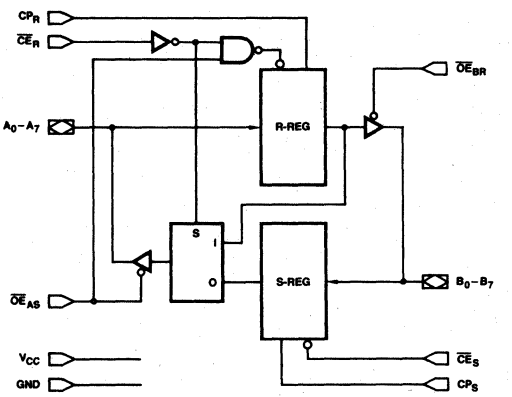

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Figure 1

RELATED PRODUCTS

Part No.	Description
Am29116	High Performance 16-Bit Bipolar Microprocessor
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2925	System Clock Generator and Driver
Am2940/2	DMA Address Generator
Am2950-3	8-Bit Bidirectional I/O Ports
Am29800 Family	High Performance Bus Interface

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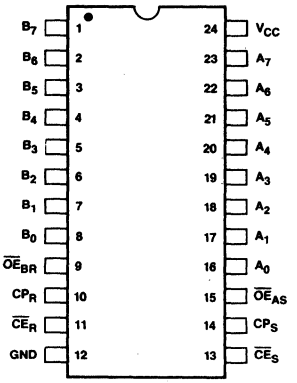
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-24-1



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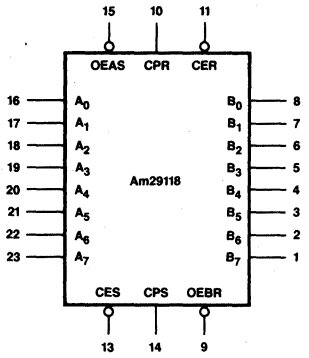
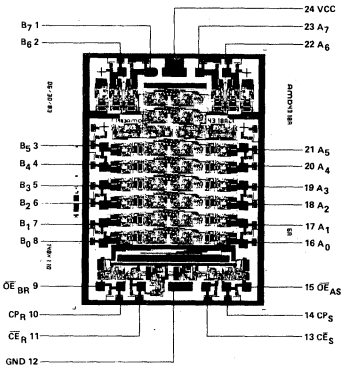
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000930

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.148' x 0.110'

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29118 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – 96 hour Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - X– Dice
- **Am29118** — Device type
  - 8-Bit Am29116 I/O Support

Valid Combinations	
Am29118	DC, DCB, DMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A0-7		Eight bidirectional lines carrying the R Register inputs or outputs or S Register outputs.
	B0-7		Eight bidirectional lines carrying the S Register inputs or R Resister outputs.
	CPR		The clock for the R Register. When $\overline{CER}$ is LOW and $\overline{OEAS}$ is HIGH data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal.
	$\overline{CER}$		The Clock Enable for the R Register. When $\overline{CER}$ is LOW and $\overline{OEAS}$ is HIGH data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, the R Register holds its contents, regardless of CPR signal transitions.
	$\overline{OEBR}$		The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, the R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.
	CPS		The clock for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal.
	$\overline{CES}$		The clock enable for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register holds its contents, regardless of CPS signal transitions.
	$\overline{OEAS}$		The output enable for the S Register. When $\overline{OEAS}$ is LOW, the R or S Register three-state outputs are enabled onto the A0-7 lines. When $\overline{OEAS}$ is HIGH, the S Register outputs are in the high-impedance state.

DETAILED DESCRIPTION

The Am29118 has two eight-bit wide registers (R-Register and S-Register) connected back to back for moving data in both directions between two buses. The R-Register serves the dual purpose of transmitting data from one bus (device's internal bus) to another (system bus), and serving as an additional accumulator for the Am29116.

The accumulator function is implemented by allowing the A-port to provide read and write data from the R-Register and read data from the S-Register; the B-port provides read data for the R-Register and write data for the S-Register (similar to the Am2952). This additional function in the Am29118 is implemented with a two-input multiplexer, as shown in Figure 1. Each register has an individual clock (CP_R and CP_S), a Clock Enable, ($\overline{CE}_R$ and $\overline{CE}_S$), and a three-state Output Enable ($\overline{OE}_{AS}$ and $\overline{OE}_{BR}$). The clock enable signal for the R-Register ($\overline{CE}_R$) and the Output Enable Signal for the S-Register ($\overline{OE}_{AS}$) are encoded to make the R-Register an accumulator, in addition to all the Am2952 functions as shown in Table 1. Recause of this encoding, transferring data from the S-Register to the R-Register is not permissible.

TABLE 1.

$\overline{OE}_{AS}$	$\overline{CE}_R$	Function
L	L	Read R, Disable CP_R
L	H	Read S, Disable CP_R
H	L	Enable CP_R
H	H	Disable CP_R

APPLICATIONS

In the Am29116 system, there is only one I/O port available for data communication with the ALU. In such a system, the Am29118 acts as an additional accumulator (temporary storage) to increase performance, and also provides capability of a bidirectional I/O port (like the Am2952).

Figure 2 shows the connections necessary for the Am29118 to be used as an accumulator as well as a bidirectional I/O port. The A-port is connected to the Y-bus (internal bus) of the Am29116, and B-port is connected to the system data bus. Four microcode are used for source and destination control for the Y-bus and the system data bus. Figure 3 shows the timing waveforms to modify an accumulator (R-Register) in two microcycles. During the first cycle, data is read from the R-Register, modified in the Am29116 and stored in one of the internal registers. A two-address architecture is required if the second operand to modify the R-Register is in one of the RAM registers, and the result has to be stored in another RAM register. For stable operation, data from the R-Register is latched in the D-Latch halfway through the clock during the first cycle. The instruction is executed and the result stored into a scratchpad register. In the second cycle, data is moved from the internal result register to the R-Register of the Am29118.

Figure 4 shows the timing waveforms to modify an accumulator (R-Register) in a single microcycle. In the first half of the cycle the source register is enabled on the Y-bus into the D-Latch of the Am29116. The D-Latch is transparent during the first half of the cycle. In the second half of the cycle, data is latched in the D-Latch and the bus source is disabled. During the second half of the cycle, the output buffer of the Am29116 is enabled to bring the result on the Y-bus to be loaded into the destination. These two techniques provide different advantages and disadvantages to modify the external accumulator using the Am29116. The first technique (Figure 3) takes two microcycles but allows a shorter microcycle time. The second technique (Figure 4) takes only one microcycle but needs a longer microcycle time.

There is also a requirement for the system bus to transfer data as input to the Am29116. The S-Register is used in this case to receive data from the system bus (like the Am2952).

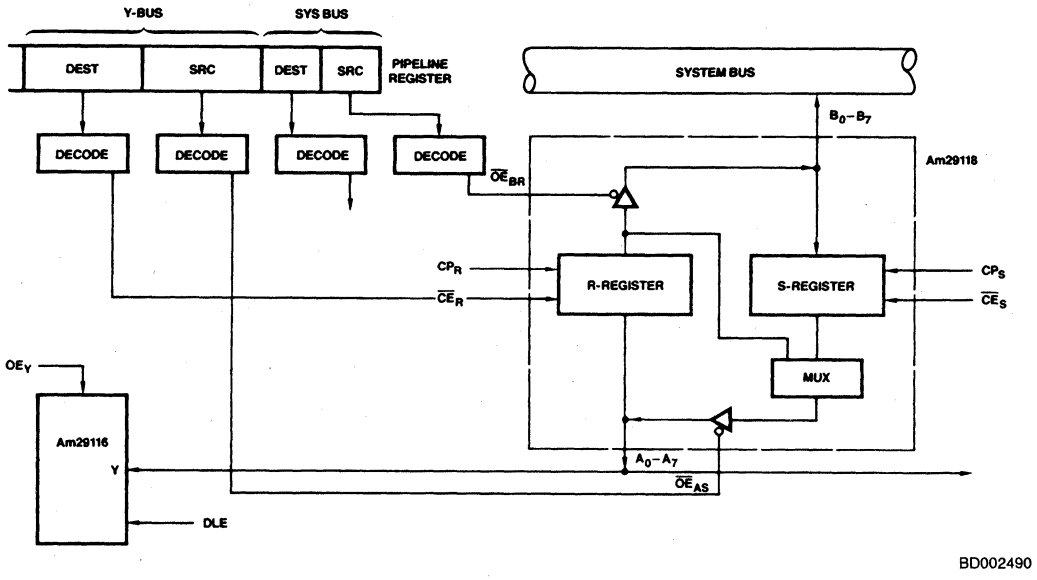


Figure 2. System Configuration.

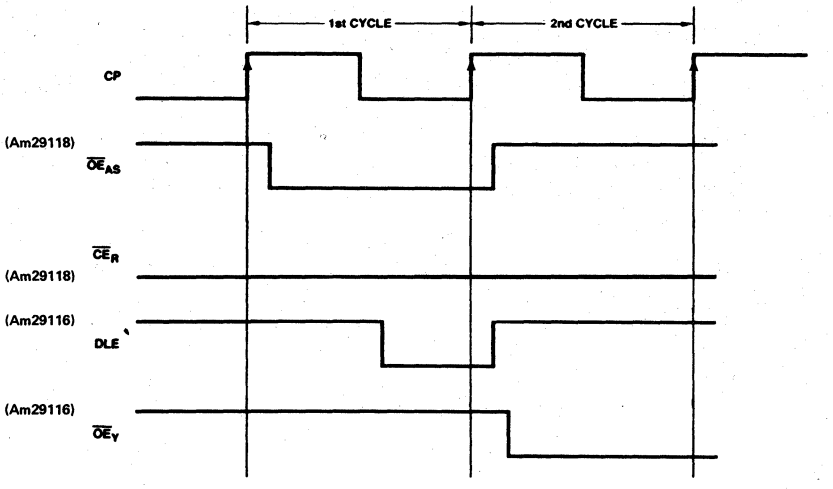


Figure 3. Timing Waveforms for Modifying R-Register in Two Microcycles using the Am29116.

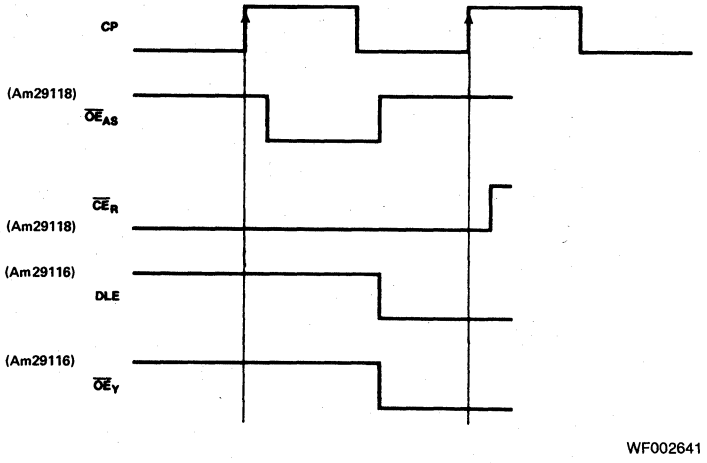


Figure 4. Timing Waveforms for Modifying R-Register using the Am29116.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature under Bias..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA	2.4	3.4		Volts
				COM'L, I_{OL} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OL} = 16mA			0.5	Volts
				COM'L, I_{OL} = 24mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−115	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}			−250	μA
				Others			−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN}=2.7V		A_{0-7},B_{0-7}			70	μA
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN}=5.5V					1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V			70	μA
				V_O = 0.4V			−250	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Notes 4, 5)	V_{CC} = MAX		T_A = 25°C		156	263	mA
			COM'L	T_A = 0 to +70°C			275	
				T_A = +70°C			228	
			MIL	T_C = −55 to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.
5. Worst case I_{CC} is at minimum temperature.

SWITCHING CHARACTERISTICS

PRELIMINARY

The tables below define the Am29118 switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0 or 3V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Setup and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7}	CPR ↓	7	5
B_{0-7}	CPS ↓	7	5
$\overline{CE}_S$	CPS ↓	7	4
$\overline{CE}_R$	CPR ↓	7	4

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	24	–
CPR ↓	–	24

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	20	20
CPR	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}_{AS}$	A_{0-7}	22	27
$\overline{OE}_{BR}$	B_{0-7}	22	27

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Setup and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7}	CPR ↓		
B_{0-7}	CPS ↓		
$\overline{CE}_S$	CPS ↓		
$\overline{CE}_R$	CPR ↓		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓		
CPR ↓		

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}_{AS}$	A_{0-7}		
$\overline{OE}_{BR}$	B_{0-7}		

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs under license.

Am29PL141

Fuse Programmable Controller (FPC)

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Implements complex fuse programmable state machines
- 64 words of 32-bit-wide microprogram memory
- Serial Shadow Register (SSR™) diagnostics on chip (programmable option)
- 20MHz clock rate, 28 pin DIP
- 29 high-level microinstructions
  - Conditional branching
  - Conditional looping
  - Conditional subroutine call
  - Multiway branch
- 16 outputs, 7 conditional inputs

GENERAL DESCRIPTION

The Am29PL141 is a single-chip Fuse Programmable Controller (FPC) which allows implementation of complex state machines and controllers by programming the appropriate sequence of microinstructions. A repertoire of jumps, loops, and subroutine calls, which can be conditionally executed based on the test inputs, provides the designer with powerful control flow primitives.

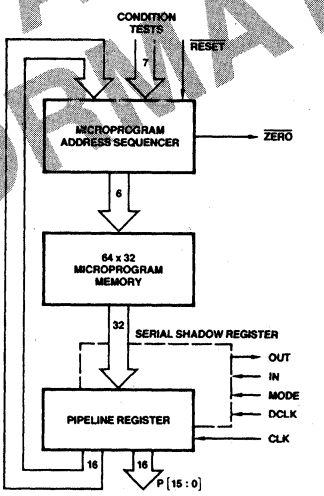
The Am29PL141 FPC also allows distribution of intelligent control throughout the system. It off-loads the central controller by distributing FPCs as the control for various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units.

A microprogram address sequencer is the heart of the FPC. It provides the microprogram address to an internal 64-word by 32-bit PROM. The fuse programming algorithm is almost identical to that used for AMD's Programmable Array Logic family.

As an option, the Am29PL141 may be programmed to have on chip SSR diagnostics capability. Microinstructions can be serially shifted in, executed, and the results shifted out to facilitate system diagnostics.

BLOCK DIAGRAM

Am29PL141 Block Diagram



BDR02340

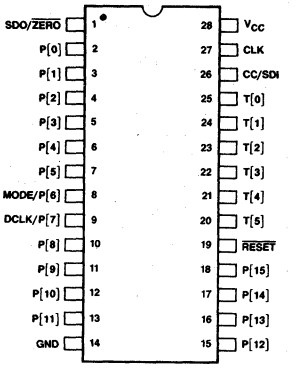
Figure 1.

SSR is a trademark of Advanced Micro Devices, Inc.

04179B

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View
D-28-1



CDR04480

Note: Pin 1 is marked for orientation

Figure 2.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
26	CC[SDI]	I	Condition code test input. When the TEST (P[24:22]) field of the executing microinstruction is set to 6 (binary 110), CC is selected to be the conditional input. (Note: In the SSR diagnostic configuration, CC is also the Serial Data Input SDI.)
27	CLK	I	Clock. The rising edge clocks the microprogram counter, count register, subroutine register, pipeline register, and EQ flag.
	P[15:8]	O	Upper eight, general-purpose microprogram control outputs. They are enabled by the OE signal from the microprogram pipeline register. When OE is High, P[15:8] are enabled, and when LOW, P[15:8] are three-stated.
	P[7:0] [DCLK, MODE]	O	Lower eight, general-purpose microprogram control outputs. They are permanently enabled. (Note: in the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK and P[6] becomes the diagnostic control input MODE.)
19	$\overline{\text{RESET}}$	I	Synchronous reset input. When it is Low, the output of the PC MUX is forced to the uppermost microprogram address (63). On the next rising clock edge, this address (63) is loaded into the microprogram counter; the microinstruction at location 63 is loaded into the pipeline register and the EQ flag is cleared.
	T[5:0]	I	Test inputs. In conditional microinstructions, the inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[5:0] inputs can also be used as a branch address when performing a microprogram branch, or as a count value.
1	$\overline{\text{ZERO}}$ [SDO]	O	Zero output. A Low state indicates that the CREG value is zero. (Note: In the SSR diagnostic configuration, $\overline{\text{ZERO}}$ becomes the Serial Data Output SDO. This change is only on the output pin; internally, the zero detect function is unchanged.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29PL141 **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – 96 Hour Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 28-pin CERDIP; X – Dice
- Am29PL141 — Device Type: Fuse Programmable Controller

Valid Combinations	
Am29PL141	DC, DMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

DETAILED DESCRIPTION

Figure 3, the block diagram of the Am29PL141 FPC, shows logic blocks and interconnecting buses. These allow parallel performance of different operations in a single microinstruction. The FPC consists of four main logic blocks: the microprogram memory, microaddress control logic, condition code selection logic, and microinstruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The microprogram memory contains the user-defined instruction flow and output sequence. The microaddress control logic addresses the microprogram memory. This control logic supports high-level microinstruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional microinstruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The microinstruction decode generates the control signals necessary to perform the microinstruction specified by the microinstruction part (P[31 : 16]) of the microword. The SSR enables in-system testing that allows isolation of problems down to the IC level.

MICROPROGRAM MEMORY

The FPC microprogram memory is a 64-word by 32-bit PROM with a 32-bit pipeline register at its output. The upper 16 bits (P[31 : 16]) of the pipeline register stay internal to the FPC and form the microinstruction to control address sequencing. The format for microinstructions is: a one-bit synchronous Output Enable OE, a five-bit OPCODE, a one-bit test polarity select POL, a three-bit TEST condition select field, and a six-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

The lower 16 bits (P[15 : 0]) of the pipeline register are brought out as user-defined, general purpose control outputs. The upper eight control outputs (P[15 : 8]) are three-stated when OE is programmed as a LOW. The lower eight control bits (P[7 : 0]) are always enabled. The microword and general microinstruction format are shown in Figure 4.

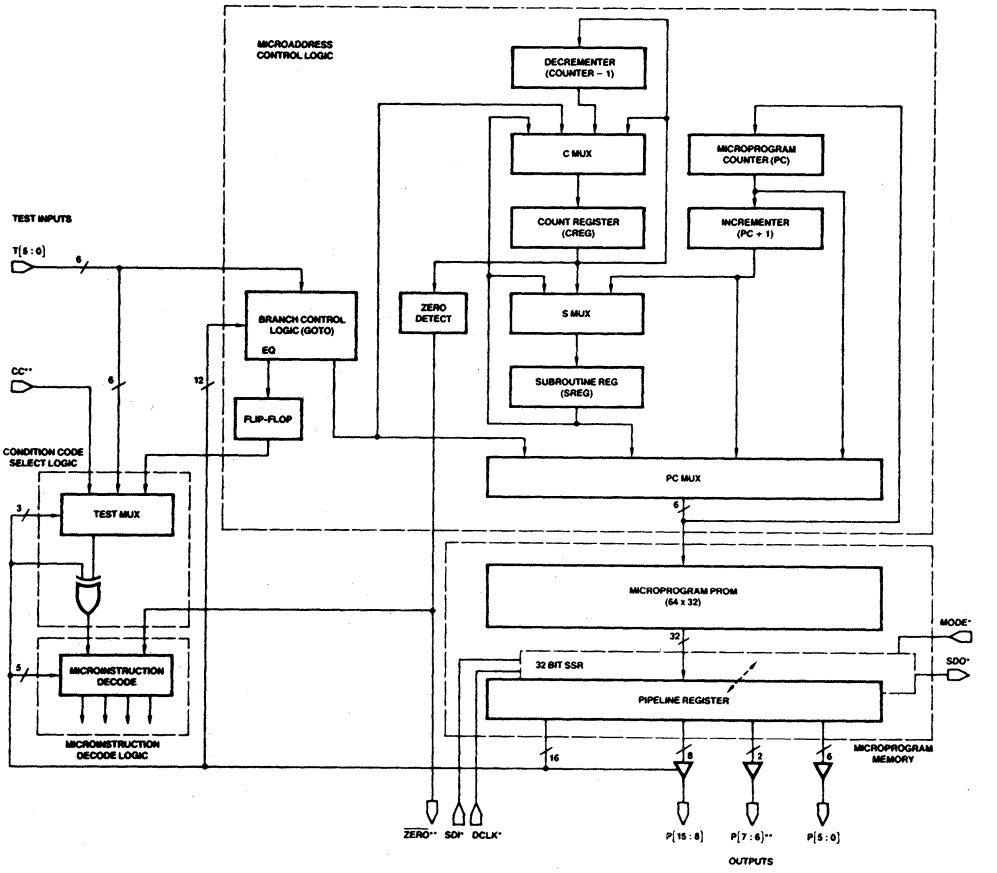
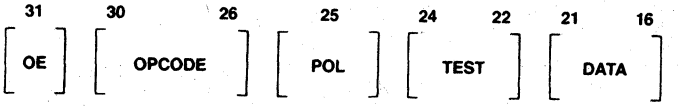


Figure 3. Am29PL141 Block Diagram.

*Note: These pins available only in SSR mode.
**Note: These pins available only in normal mode.

The general microinstruction format is shown below:

Am29PL141 General Microinstruction Format



DFR00730

WHERE:

OE = Synchronous Output Enable for P[15:8].

OPCODE = A five-bit opcode field for selecting one of the twenty-eight single data field microinstructions.

POL = A one-bit test condition polarity select.
0 = Test for true (HIGH) condition.
1 = Test for false (LOW) condition.

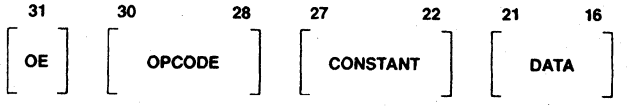
TEST = A three-bit test condition select.

TEST[2:0]	UNDER TEST
000	T[0]
001	T[1]
010	T[2]
011	T[3]
100	T[4]
101	T[5]
110	CC
111	EQ

DATA = A six-bit conditional branch microaddress, test input mask, or counter value field designated as PI in microinstruction mnemonics.

The special two data field comparison microinstruction format is shown below:

Am29PL141 Comparison Microinstruction Format



DFR00740

WHERE:

OE = Synchronous Output Enable for P[15:8].

OPCODE = Compare microinstruction (binary 100).

CONSTANT = A six-bit constant for equal to comparison with T*M.

DATA = A six-bit mask field for masking the incoming T[5:0] inputs.

Figure 4.

MICROADDRESS CONTROL LOGIC

The microaddress control logic consists of five smaller logic blocks. These are:

PC MUX – The microprogram counter multiplexer

P CNTR – Microprogram counter (PC) and incrementer (PC + 1)

SUBREG – Subroutine register (SREG) with subroutine mux (S MUX)

CNTR – Count register (CREG) with counter mux (C MUX), decrementer (COUNTER–1) and zero detect

GOTO – Specialized branch control logic

The PC MUX is a six-bit, four-to-one multiplexer. It selects either the PC, PC+1, SREG, or GOTO output as the next microaddress input to the microprogram memory and to the PC. The PC thus always contains the address of the microinstruction in the pipeline register. During a Reset, the PC MUX output is forced to all ones, selecting location 63 of the microprogram memory.

The P CNTR block consists of a six-bit register (PC) driving a six-bit combinatorial incrementer (PC+1). Either the present or the incremented values of PC can address the microprogram PROM. The incremented value of PC can be saved as a subroutine return address. The present PC value can address the microprogram PROM when waiting for a condition to become valid. PC+1 addresses the microprogram PROM for sequential microprogram flow, for unconditional microinstructions, and as a default for conditional microinstructions.

The SUBREG block consists of a six-bit, three-to-one multiplexer (S MUX) driving a six-bit register (SREG). The three possible SREG inputs are PC+1, CREG, and SREG. SREG normally operates as a one-deep stack to save subroutine return addresses. PC+1 is the input source when performing subroutine calls and PC MUX is the output destination when performing return from subroutine.

The CNTR block consists of a six-bit, four-to-one multiplexer (C MUX); driving a six-bit register (CREG); a six-bit, combinatorial decrementer (COUNTER-1); and a zero detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The SUBREG and CNTR can be considered as one logic block because of their unique interaction. To explain this interaction, notice that both have an additional input source and output destination not used in typical operation—each other. This allows the CREG to be an additional stack location when not used for counting, and the SREG to be a nested count location when not used as a stack location. Thus, the SREG and CREG can operate in three different modes:

1. As a separate one-deep stack and counter.
2. As a two-deep stack.
3. As a two-deep nested counter.

The GOTO logic block serves three functions:

1. It provides a six-bit count value from the DATA Field in the pipeline register (P[21 : 16]) or from the TEST inputs (T[5 : 0]) masked by the DATA Field (P[21 : 16]). (This is represented by T*M.)
2. It provides a branch address from the DATA Field in the pipeline register (P[21 : 16]) or from the TEST inputs (T[5 : 0]) masked by the DATA Field (P[21 : 16]). (This is represented by T*M.)
3. It compares the TEST inputs (T[5 : 0]) masked by the DATA Field (P[21 : 16]), called T*M, to the CONSTANT Field from the pipeline register (P[27 : 22]). If a match occurs, the EQ Flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to marked test bits must be ZERO.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to Sum-of-Products can be performed since a no match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

NOTE: A zero in the DATA Field blocks the corresponding bit in the TEST Field; a one activates the corresponding bit.

CONDITION CODE SELECTION LOGIC

The condition code selection logic consists of an eight-to-one multiplexer. The eight test conditon inputs are the device inputs (CC and T[5 : 0]) and the EQ flag. The TEST field P[24 : 22] selects one of the eight conditions to test.

The polarity bit POL in the microinstructions allows the user to test for either a true or false conditon. Refer to Table 2 for details.

MICROINSTRUCTION DECODE

The microinstruction decoder is a PLA that generates the control for 29 different microinstructions. The decoder's inputs include the OPCODE Field (P[30 : 26]), the zero detection output from the CNTR, and the selected test condition code from the conditional code selection logic.

Am29PL141 SSR DIAGNOSTICS OPTION

As a programmable option, the Am29PL141 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing that allows isolation of problems down to the IC level.

The SSR diagnostics configuration activates a 32-bit-wide, D-type register, called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the microprogram memory in normal operation or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. CC also functions as the Serial Data Input (SDI), $\overline{\text{ZERO}}$ becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in Table 1.

Serially loading a test microinstruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test microinstruction. The result of the test microinstruction can then be clocked into the pipeline register, as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

TABLE 1.

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
D	L	↑	H,L,↑	S_O	$S_{i-1} \leftarrow S_i$ $S_{31} \leftarrow D$	Hold	Serial Right Shift Register
X	L	H,L,↓	↑	S_O	Hold	$P_i \leftarrow PROM_i$	Normal Load Pipeline Register from PROM
L	H	↑	H,L,↓	L	$S_I \leftarrow P_i$	Hold	Load Shadow Register from Pipeline* Register
X	H	H,L,↓	↑	SDI	Hold	$P_I \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H,L,↓	H	Hold	Hold	Hold Shadow Register

*S7, S6 are undefined. S_{15} - S_8 load from the source driving pins P[15] - P[8]. If P[31] in the microword is a ONE, S_{15} - S_8 are loaded from the pipeline register. If P[31] in the microword is a ZERO, S_{15} - S_8 are loaded from an external source.

FUNCTION TABLE DEFINITIONS

INPUTS

H = HIGH X = Don't Care
L = LOW ↑ = LOW-to-HIGH transition
↓ = High-to-Low transition

TABLE 2.

Input Condition Being Tested	POL	Condition
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

PROGRAMMING AND VERIFICATION

The Am29PL141 FPC is programmed and verified using a simple algorithm that is almost identical to that used for AMD's Programmable Array Logic family. The internal programmable array of the Am29PL141 is organized as a 64 word by 32 bit (column) PROM. The fuse to be programmed is selected by its address (1 of 64), the byte at that address (1 of 4), and the bit in the byte (1 of 8). Control of programming and verifying is accomplished by applying a simple sequence of voltages on two control pins (CLK and CC).

The fuse address is selected using a full decode of the T[5 : 0] inputs, where T[5] is the MSB and T[0] the LSB. The one of four byte addressing is done on the P[7] (MSB) and P[6] (LSB) outputs. The bit selection is done one output at a time by applying the programming voltage (V_{OP}) to the output pin. The output pins that accept V_{OP} are P[15 : 8]. A graphical representation of the fuse array organization for programming, with fuse numbering compatible to the JEDEC standard programmable logic transfer format, is shown in Figure A.

The complete program and verify cycle timing is shown in Figure B. A programming sequence is initiated by raising the CLK pin to V_{HH}. This places the device in the program mode and disables the output pins so that they may be used as fuse addressing inputs. The next step is to address the fuse to be blown as previously stated. Note that bit selection, with V_{OP}, should follow address and byte selection. Raising the CC pin to V_{HH} initiates programming and lowering V_{OP} terminates programming. Lowering the CLK pin to a TTL LOW level places the device in the fuse verification mode by enabling the programming outputs, P[15 : 8]. Following a clock pulse the fuse may be verified on the same output as bit selection was performed. This scheme allows fuses to be verified in parallel as a byte if desired. The verification mode is terminated by lowering the CC pin back to a normal TTL level.

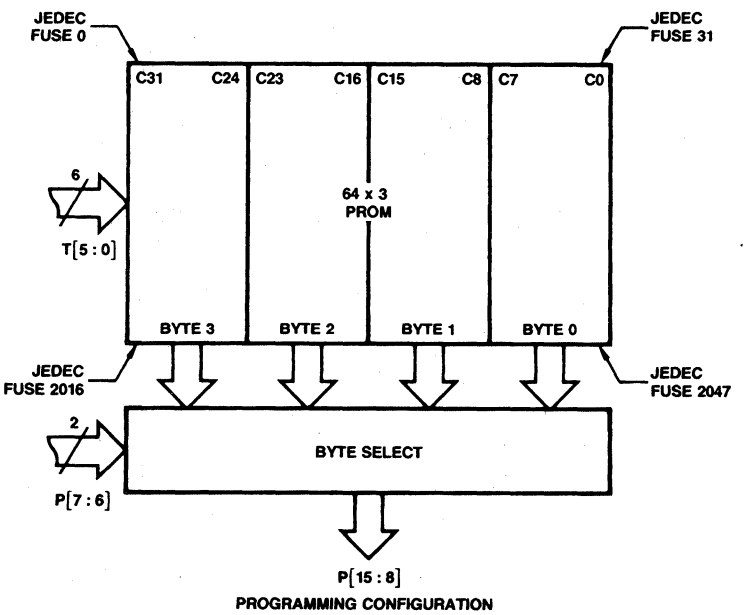
SSR DIAGNOSTICS CONFIGURATION PROGRAMMING

One additional fuse (#2048) is used to alter the configuration of the Am29PL141 to include on-chip SSR Diagnostics. This fuse is addressed by applying V_{HH} to the $\overline{RESET}$ and T[5], followed by V_{OP} on pin P[15]. To verify the diagnostic fuse, P[7] and P[6] must select byte #3, i.e., P[7] must be low and P[6] must be high.

PROGRAMMING YIELD

AMD programmable logic devices have been designed to insure extremely high programming yields (> 98%). To help insure that a part was correctly programmed, once the programming sequence is completed, the entire fuse array should be reverified at both low and high V_{CC} (V_{CCL} and V_{CCH}). Reverification can be accomplished in a verification only mode (CC at V_{HH}) by reading the outputs in parallel. This verification cycle checks that the array fuses have been blown correctly and can be sensed under varying conditions by the outputs.

AMD programmable logic devices contain many internal test features, including circuitry and extra fuses which allow AMD to test the ability of each part to perform programming before shipping, to assure high programming yields, and correct logical operation for a correctly programmed part. Programming yield losses are most likely due to poor programming socket contact, programming equipment that is out of calibration, or improper usage of said equipment.



PROGRAMMING CONFIGURATION

PFR00970

JEDEC FUSE NUMBER = 32 (FUSE ADDRESS) + 8(3 – BYTE) + (7 – BIT)

Figure A. Programming Configuration.

BYTE SELECT		
BYTE	**P[7]**	**P[6]**
0	H	L
1	H	H
2	L	L
3	L	H

BIT SELECT								
BIT	P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]
0	L	L	L	L	L	L	L	H
1	L	L	L	L	L	L	H	L
2	L	L	L	L	L	H	L	L
3	L	L	L	L	H	L	L	L
4	L	L	L	H	L	L	L	L
5	L	L	H	L	L	L	L	L
6	L	H	L	L	L	L	L	L
7	H	L	L	L	L	L	L	L

COLUMN DECODE				
0	C0	C8	C16	C24
1	C1	C9	C17	C25
2	C2	C10	C18	C26
3	C3	C11	C19	C27
4	C4	C12	C20	C28
5	C5	C13	C21	C29
6	C6	C14	C22	C30
7	C7	C15	C23	C31

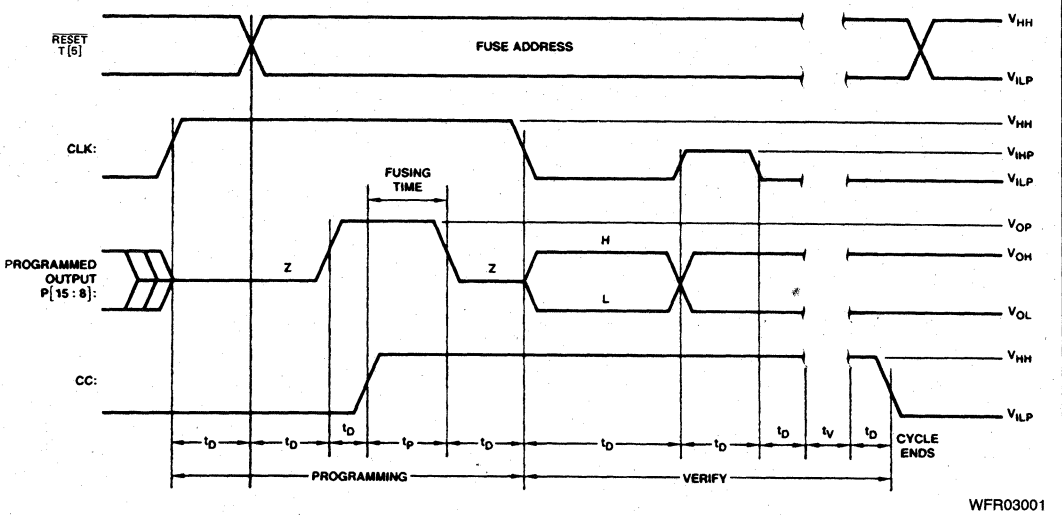
FUSE ADDRESS DECODE

FUSE ADDRESS	T[5]	T[4]	T[3]	T[2]	T[1]	T[0]
0	L	L	L	L	L	L
1	L	L	L	L	L	H
2	L	L	L	L	H	L
3	L	L	L	L	H	H
4	L	L	L	H	L	L
5	L	L	L	H	L	H
6	L	L	L	H	H	L
7	L	L	L	H	H	H
8	L	L	H	L	L	L
9	L	L	H	L	L	H
10	L	L	H	L	H	L
11	L	L	H	L	H	H
12	L	L	H	H	L	L
13	L	L	H	H	L	H
14	L	L	H	H	H	L
15	L	L	H	H	H	H
16	L	H	L	L	L	L
17	L	H	L	L	L	H
18	L	H	L	L	H	L
19	L	H	L	L	H	H
20	L	H	L	H	L	L
21	L	H	L	H	L	H
22	L	H	L	H	H	L
23	L	H	L	H	H	H
24	L	H	H	L	L	L
25	L	H	H	L	L	H
26	L	H	H	L	H	L
27	L	H	H	L	H	H
28	L	H	H	H	L	L
29	L	H	H	H	L	H
30	L	H	H	H	H	L
31	L	H	H	H	H	H
32	H	L	L	L	L	L
33	H	L	L	L	L	H
34	H	L	L	L	H	L
35	H	L	L	L	H	H
36	H	L	L	H	L	L
37	H	L	L	H	L	H
38	H	L	L	H	H	L
39	H	L	L	H	H	H
40	H	L	H	L	L	L
41	H	L	H	L	L	H
42	H	L	H	L	H	L
43	H	L	H	L	H	H
44	H	L	H	H	L	L
45	H	L	H	H	L	H
46	H	L	H	H	H	L
47	H	L	H	H	H	H
48	H	H	L	L	L	L
49	H	H	L	L	L	H
50	H	H	L	L	H	L
51	H	H	L	L	H	H
52	H	H	L	H	L	L
53	H	H	L	H	L	H
54	H	H	L	H	H	L
55	H	H	L	H	H	H
56	H	H	H	L	L	L
57	H	H	H	L	L	H
58	H	H	H	L	H	L
59	H	H	H	L	H	H
60	H	H	H	H	L	L
61	H	H	H	H	L	H
62	H	H	H	H	H	L
63	H	H	H	H	H	H

PROGRAMMING PARAMETERS T_A = 25°C

Parameters	Description		Min	Typ	Max	Units
V_{HH}	Control Pin Extra High Level	CC @ 10 – 40mA	19.5	20	20.5	Volts
		CLK@ 10 – 40mA	19.5	20	20.5	
V_{OP}	Program Voltage, P [15:8] @ 15 – 200mA		19.5	20	20.5	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50 – 200mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50 – 200mA		4.1	4.3	4.5	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50 – 200mA		5.4	5.7	6.0	Volts
V_{Blown}	Successful Blown Fuse Sense Level @ Output			0.3	0.5	Volts
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/µsec
dV_{FE}/dt	Rate of Fusing Enable Voltage Change (CC Rising Edge)		100		1000	V/µsec
tp	Fusing Time First Attempt		40	50	100	µsec
	Subsequent Attempts		4	5	10	msec
t_D	Delays Between Various Level Changes		100	200		ns
t_V	Period During which Output is Sensed for V_{Blown} Level		500			ns
V_{ONP}	Pull-Up Voltage on Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor on Outputs Not Being Programmed		1.9	2	2.1	KΩ

SSR DIAGNOSTICS CONFIGURATION PROGRAMMING WAVEFORMS



WFR03001

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 28 to Pin 14) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +V_{CC} max
DC Voltage Applied to Outputs
During Programming 21V
DC Output Current, Into Outputs During
Programming (Max Duration of 1 sec) 200mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	P[15:0], I_{OH} = − ZERO, I_{OH} = − SDO, I_{OH} = −	COM'L	2.4		Volts
			P[15:0], I_{OH} = − ZERO, I_{OH} = − SDO, I_{OH} = −	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	P[15.0], I_{OL} = ZERO, I_{OL} = SDO, I_{OL} =	COM'L		0.50	Volts
			P[15.0], I_{OL} = ZERO, I_{OL} = SDO, I_{OL} =	MIL			
V_{IH} (Note 1)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0		Volts
V_{IL} (Note 1)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V (Note2)					mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = MAX					mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{OZH}	Output Leakage Current (Note 3)	V_{CC} = MAX, V_{IL} = 0.8V V_{IH} = 2.0V	V_O = 2.7V			100	μA
I_{OZL}			V_O = 0.4V			−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0V@f = 1MHz (Note 4)					pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V@f = 1MHz (Note 4)					

Notes: 1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
4. Those parameters are not 100% tested, but are periodically sampled.

RELATED PRODUCTS

Part No.	Description
Am2914	Vectored Priority Interrupt Controller
Am29100	Controller Family Products

Am29500
Array Processing and
Digital Signal Processing Index

The Am29500 Family

A High-Performance Architecture
For Digital Signal/Array Processing

As new system designs continue to press for maximum performance, high-speed array processing is becoming an increasingly attractive alternative. Parallel processing and pipelined architectures implemented in the fastest technologies are requisites for maximum performance array and signal processing applications.

The Am29500 Family is designed specifically for maximum performance and flexibility. Key product features include:

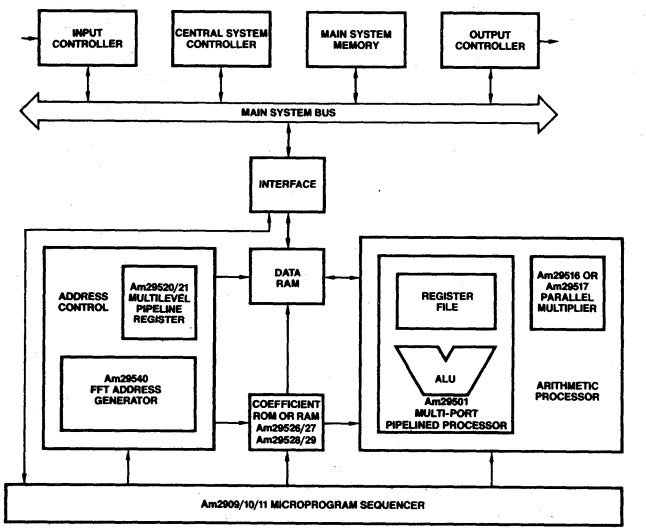
- Microprogrammable for maximum versatility
- Pipelined organization for efficient use of resources
- IMOX™ process and ECL internal-structures for maximum speed
- TTL I/O for ease of interface

The Am29500 family components are targeted for the efficient execution of Digital Signal Processing (DSP) and Array Processing algorithms, including Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) digital filters, Fast Fourier Transform (FFT) processors, graphics processors, etc.

The Am29500 family components include:

- **Am29501 Multi-Port Pipelined Processor**
  A specialized eight-bit wide parallel processor which executes multiple simultaneous data operations. Its Register/ALU structure provides the key functional element for a high-performance signal processing system.
- **Am29516/29517 High Speed 16 x 16-Bit Parallel Multipliers**
  Both are 16 x 16-bit Parallel Multipliers. The Am29516 is pin and functionally compatible with the MPY-16HJ, but with an added multiplexer to output the LSP at the MSP port. The Am29517 is the same function, but with clock enables for microprogrammed applications. Low power and speed enhanced versions are also available.
- **Am29520/29521 Multilevel Pipeline Registers**
  Both devices contain four 8-bit registers for dual two-stage or single four-stage data or address pipelining. Combined load-and-shift (Am29520) or separate load-and-shift (Am29521) control options are available.
- **Am29526/29527/29528/29529 High-Speed Sine/Cosine Function Generators**
  The sine and cosine functions are necessary for Fast Fourier Transforms (FFT). The Am29526/527 generate the most significant and least significant byte of the 16-bit sine function and the Am29528/529 generate the most significant and least significant byte of the 16-bit cosine function. The sine and cosine functions are generated to provide a range of θ for a half cycle, $0 \leqslant \theta \leqslant \pi$, in increments of $\pi/2048$.
- **Am29540 FFT Address Sequencer**
  This algorithm-specific VLSI chip generates data and coefficient addresses for the Fast Fourier Transform. It supports a wide variety of FFT algorithms in either radix-2 or radix-4.

HIGH PERFORMANCE SIGNAL PROCESSOR



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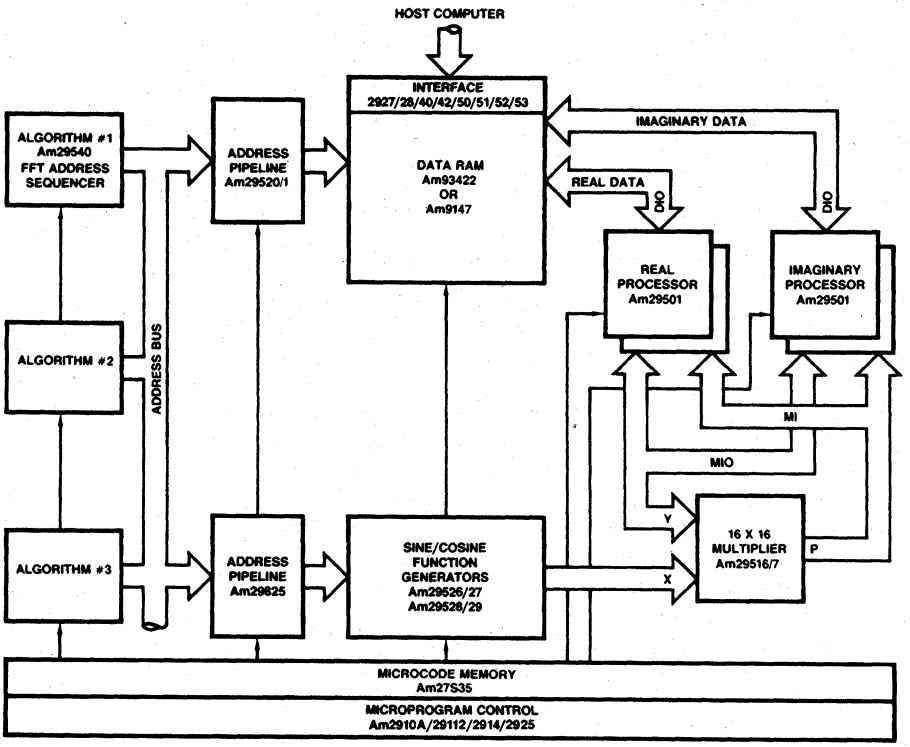
Refer to Page 13-1 for Essential Information on Military Devices

- **Am29509 and Am29510 Multiplier-Accumulators**
  These devices are 12 x 12 and 16 x 16 multipliers with built-in accumulators. They are often used in constructing digital filters. The Am29509 is pin- and function-compatible with the TDC1009 and the Am29510 is pin- and function-compatible with the TDC1010.
- **Am29325 Floating Point Processor**
  Support both IEEE and DEC 32-bit floating point formats, the Am29325 will perform a full parallel 32-bit floating point multiply in a single clock cycle. This device can replace more than a full circuit board of logic. 32-bit floating point is useful in filters for reducing errors and noise, and can be used to conveniently extend the number range in array processors.

A high-performance signal processor may be constructed as shown in the diagram. The processor is built entirely with Am29500 digital signal processing and Am2900 devices. Such a processor is attached as a slave to the main system bus to perform the multitude of arithmetic operations which prevail in DSP algorithms.

Am29500 ARRAY PROCESSOR



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Am29501

Multi-Port Pipelined Processor (Byte-Slice™)

DISTINCTIVE CHARACTERISTICS

- Expandable Byte-Slice™ Register-ALU
  - Sign extend input and output
  - Carry and $\overline{P}/\overline{G}$ expansion with force/inhibit/normal carry modes
- Eight instruction ALU
  - Four arithmetic operations
  - Four logic operations
- Ten internal data paths
  - Highly parallel architectures
  - Multiple simultaneous data manipulations
- Pipelining register file has six 8-bit registers
  - Multilevel pipelining
  - Multiple register-to-register moves
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- Three I/O ports for maximum system interconnect flexibility

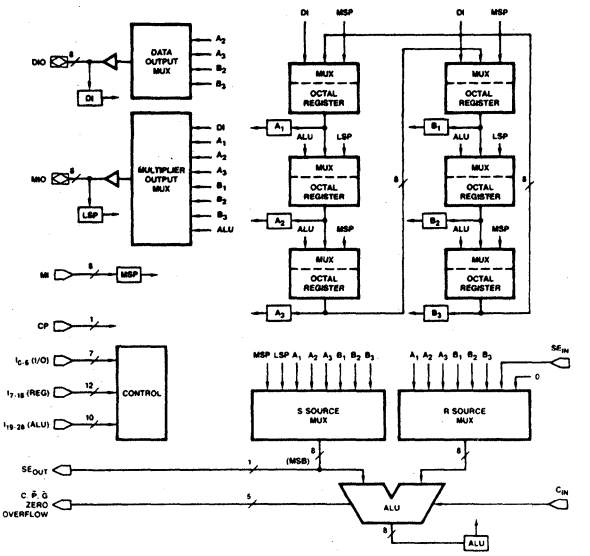
GENERAL DESCRIPTION

The Am29501 is an expandable Byte-Slice™ register-ALU designed to bring maximum speed to array processor and digital signal processor systems. It provides a flexible processor building block for implementing highly pipelined, highly parallel architectures where speed is achieved by a combination of optimized integrated circuit technology (IMOX™ process and internal ECL circuitry) and customized system architecture. I/O port flexibility and multiple concurrent data moves make it possible to construct processors capable of very high throughput. Parallel processors are especially efficient for array/vector operations or signal processing algorithms requiring complex number arithmetic (e.g. FFT, convolution, correlation, etc.).

The Am29501's Pipeline Register File provides data storage and pipelining flexibility. Any combination of register instructions, ALU instructions, and I/O instructions can be microprogrammed to occur in the same cycle. This allows overlap of external multiplication, ALU operations, and memory I/O.

Three I/O ports support a wide variety of parallel, pipelined architectures by providing separate I/O ports for the multiplier and the memory data bus. Either of two bidirectional I/O ports, DIO and MIO, can interface to the data bus or multiplier Y-input port, and a separate MI port connects to the multiplier output port.

BLOCK DIAGRAM



BDR02300

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Refer to Page 13-1 for Essential Information on Military Devices

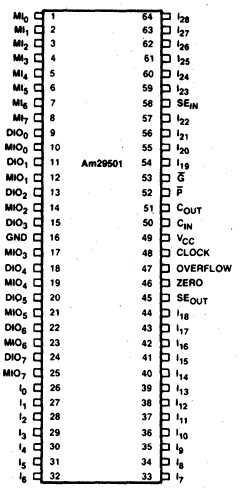
RELATED PRODUCTS

Part No.	Description
Am2902A	Carry look-ahead generator
Am29516/17	16 x 16-bit high speed multipliers
Am25S558	8 x 8-bit multiplier

CONNECTION DIAGRAM

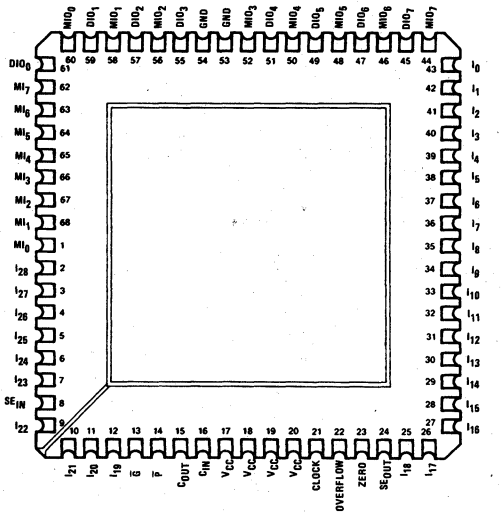
Top View

D-64-3



CDR04420

Leadless Chip Carrier



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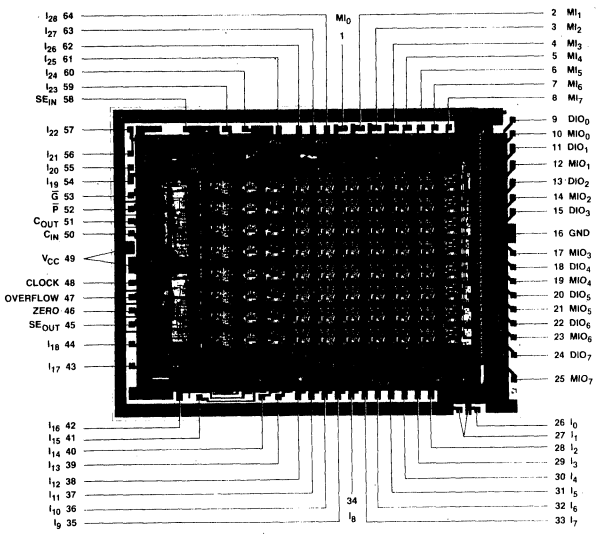
METALLIZATION AND PAD LAYOUT



Die Size: .289" x .222"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29501 **P** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in (Note 1)
- **C** — Temperature (see Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- **P** — Package
  - D – 64-pin CERDIP (D-64-3)
  - L – 68-TERMINAL Leadless Chip Carrier
- **Am29501** — Device type
  - Multi-port Pipelined Processor

Note 1: 160 Hour Burn-in
Heatsink Parts, $T_A = 125°C$
Non-Heatsink Parts, $T_A = 85°C$

Valid Combinations	
Am29501	DC, DCB, DMB, LC, LMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
50	C_{IN}	I	Carry-in input to the internal 8-bit ALU.
51	C_{OUT}	O	Carry-out output from the internal 8-bit ALU.
48	CP	I	Clock input for the internal pipeline register file. Data selected by I_7-I_{18}, meeting the set-up and hold time requirements of the respective register, is clocked into the register on the clock LOW-to-HIGH transition.
9, 11, 13, 15, 18, 20, 22, 24	DIO_0-DIO_7	I/O	Bidirectional data I/O port (see Note).
53, 52	$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902A for carry-lookahead.
26-44, 54-57, 59-64	I_0-I_{28}	I	Instruction inputs designed to be driven under microprogram control. All instruction inputs control multiplexers or drivers or the ALU directly. There is no instruction encoding. See Control Input Function Tables for operating modes.
1-8	MI_0-MI_7	I	Data Input port (Multiplier Input - see Note).
10, 12, 14, 17, 19, 21, 23, 25	MIO_0-MIO_7	I/O	Bidirectional data I/O port (Multiplier I/O - see Note).
47	OVR	O	Overflow This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
45	SE_{OUT}	O	The most significant bit of the S-operand. This is used in multiple precision arithmetic operations for sign extension of two's complement numbers.
58	SE_{IN}	I	A single-bit input which generates an 8-bit sign extension R-operand for multiple precision two's complement arithmetic operations.
46	ZERO	O	This is an open collector output which goes HIGH if the data on the ALU outputs are all LOW.

Note: This is a general purpose data port. The names are derived from the typical usage in a typical Am29500 system but are not restricted to this interconnection scheme.

*DIP Configuration

CONTROL INPUT FUNCTION TABLES

1. Data I/O Port (DIO) Output Select

I_3	I_2	I_0	Source
L	L	L	A_2
L	H	L	A_3
H	L	L	B_2
H	H	L	B_3
X	X	H	Output Disabled

2. Multiplier I/O Port (MIO) Output Select

I_6	I_5	I_4	I_1	Source
L	L	L	L	A_1
L	L	H	L	A_2
L	H	L	L	A_3
L	H	H	L	B_1
H	L	L	L	B_2
H	L	H	L	B_3
H	H	L	L	ALU
H	H	H	L	DI
X	X	X	H	Output Disabled

3. Register A_1 Data Source Select

I_8	I_7	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	B_3
H	H	A_1 (Hold)

4. Register A_2 Data Source Select

I_{10}	I_9	Source
L	L	LSP (MIO)
L	H	ALU
H	L	A_1
H	H	A_2 (Hold)

CONTROL INPUT FUNCTION TABLES (Cont.)

5. Register A_3 Data Source Select

I_{12}	I_{11}	Source
L	L	MSP (MI)
L	H	ALU
H	L	A_2
H	H	A_3 (Hold)

6. Register B_1 Data Source Select

I_{14}	I_{13}	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	A_3
H	H	B_1 (Hold)

7. Register B_2 Data Source Select

I_{16}	I_{15}	Source
L	L	LSP (MIO)
L	H	ALU
H	L	B_1
H	H	B_2 (Hold)

8. Register B_3 Data Source Select

I_{18}	I_{17}	Source
L	L	MSP (MI)
L	H	ALU
H	L	B_2
H	H	B_3 (Hold)

9. ALU Operating Instructions

I_{22}	I_{21}	I_{20}	I_{19}	OP	C_{OUT}	$\overline{P}$	$\overline{G}$	
L L H H	L H L H	L	L	$R+S+C_{IN}$ $R-S-C_{IN}$ $R+C_{IN}$ $-R+S-C_{IN}$	Carry	$\overline{P}$	$\overline{G}$	Normal Operating Mode**
L L H H	L H L H	L	H	$R+S+C_{IN}$ $R-S-C_{IN}$ $R+C_{IN}$ $-R+S-C_{IN}$	L	H	H	Inhibit Carry Mode
L L H H	L H L H	H	L	$R+S+C_{IN}$ $R-S-C_{IN}$ $R+C_{IN}$ $-R+S-C_{IN}$	H	$\overline{P}$	L	Force Carry Mode
L L H H	L H L H	H	H	R XOR S R AND S $\overline{R}$ R OR S	(L)*	(H)*	(H)*	Logic Operations

*C_{OUT}, $\overline{P}$ and $\overline{G}$ are not applicable to logic operation, Am29501 functions as shown.
**Carry is used for 16-bit expansion. $\overline{P}$ and $\overline{G}$ are used with an Am2902A for expansion to more than 16 bits.

10. ALU R Operand Selection

I_{25}	I_{24}	I_{23}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	Sign Extend Input Bussed to All Bits
H	H	H	Arithmetic Zero (All Inputs LOW)

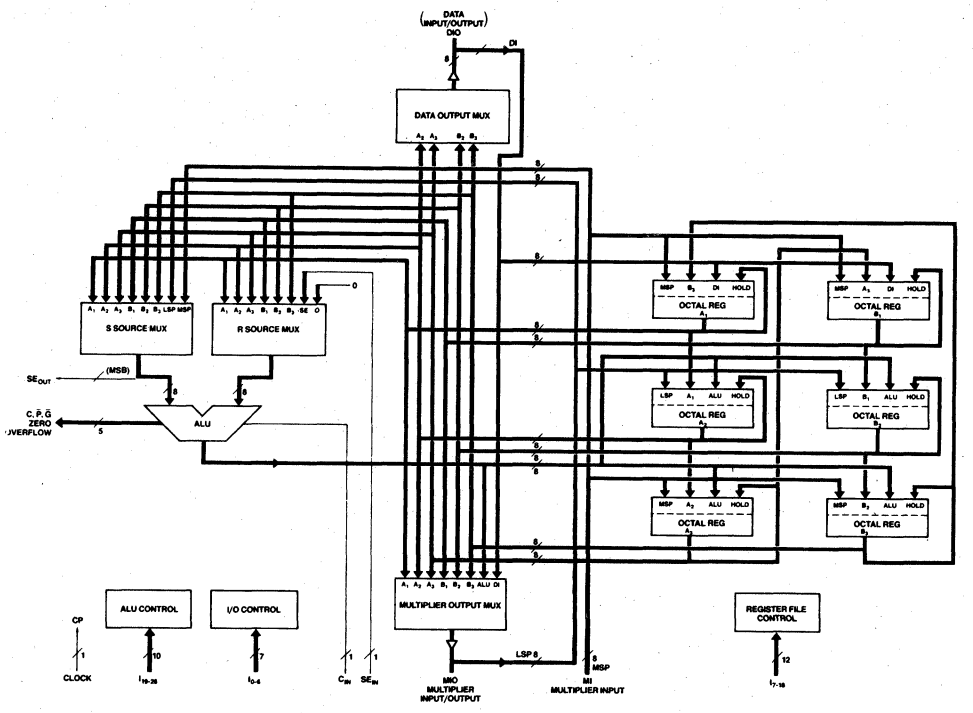
11. ALU S Operand Selection

I_{28}	I_{27}	I_{26}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	MSP (MI)
H	H	H	LSP (MIO)

DETAILED DESCRIPTION

Figure 1 contains a block diagram of the Am29501. It shows four major sections – an eight-bit cascadable ALU, a register file consisting of six eight-bit registers, three I/O ports, and a microcode control section.

DETAILED Am29501 BLOCK DIAGRAM



DFR00710

Figure 1.

ALU

The ALU performs arithmetic on an eight-bit Byte-Slice™ with full internal carry lookahead and carry input and output for cascading. The carry can ripple between byte-slices by connecting the C_{OUT} of one slice to C_{IN} of the next byte-slice. Carry generate ($\overline{G}$) and propagate ($\overline{P}$) outputs are also provided for faster operation when the ALU is used in conjunction with a carry lookahead generator such as the Am2902A.

There are three arithmetic modes – cascade, carry inhibit and forced carry. The cascade mode produces an output carry based on the results of the operation and is the normal mode. The carry inhibit mode produces no carry output and is used to decouple cascaded ALUs. A 16-bit ALU consisting of two Am29501s can operate as two 8-bit ALUs simultaneously by programming the carry inhibit mode. This mode could also be used with a second 16-bit ALU for double precision where the more significant slice is programmed in the carry inhibit mode for single precision and in the cascade mode for double precision. The less significant slices would be programmed in normal mode for either case. The forced carry mode is the converse and always produces a carry. All three modes treat the input carry in the same way. The Am29501 uses the input carry as a true borrow during subtraction as opposed to most two's complement ALUs which use borrow. The usual requirement is that input borrow be programmed HIGH (inactive) when doing a subtraction. Since the Am29501 has a true borrow, the input carry is programmed to be LOW for both addition and subtraction. This is consistent with the carry inhibit mode discussed previously.

In addition to arithmetic operations the ALU also does bitwise logic operations – OR, AND, exclusive OR, and invert. Carries are not applicable for these operations and are inactive. Codes to program the ALU function are contained in Control Input Function Table 9.

Each operand of the ALU has eight possible sources. Operand R can be any register in the register file or one of the I/O ports MI or MIO as shown in Table 10. Operand S can be any register, zero or a sign extension input (SE_{IN}) from another ALU (Table 11). The ALU result can be steered to registers A2, A3, B2, and B3 of the register file or the MIO I/O port.

Byte-Slice is a trademark of Advanced Micro Devices, Inc.

REGISTER FILE

The register file provides for fully independent use of the registers. Each register has a four-input mux which can be programmed so that the register holds its previous contents or is loaded from the ALU and I/O port or the "preceding" register. If all registers are programmed for the preceding register, a ring is formed and data circulates through all the registers. This facilitates constructing a pipelined data flow. Various combinations of I/O ports and the ALU make up the remaining inputs to each register. The sources for each register are shown in the Control Input Function Tables 3–8.

I/O PORTS

The Am29501 has two bidirectional ports (DIO and MIO) and one input port (MI). As an input the DIO port can be loaded into registers A1 and B1 and directed to the MIO output port. Output from the DIO comes from registers A2, A3, B2 or B3 using the codes from Control Input Function Table 1. This separation of input and output registers connected to the DIO port is in keeping with the pipelined organization of the part when the DIO port is used for data flow in and out of the processor.

Input through the MIO port can be directed to registers A2 and B2 in the register file and to the ALU. Output can come from any of the six registers, the DIO input port or from the ALU. This structure allows the user to direct operands to an auxiliary processor (such as a multiplier or barrel shifter) from any point in the pipeline. The MIO port could be connected to a processor with bidirectional data bus. The auxiliary processor would receive data and return its results to registers A2 and B2 through the MIO port.

The MI port provides another entry point for inserting data in the processing pipeline. An auxiliary processor with flow-through architecture could receive data from the MIO port and return data through the MI port which can be directed to registers A1, A3, B1 and B3 and to the ALU.

A potential use of the ports is connecting the bidirectional bus of an Am29116 microprocessor to the MIO port. An Am29516 would have its inputs connected to the same MIO port and its output to the MI port. This architecture could calculate magnitudes by computing the sum of the squares with the Am29516 and Am29501 and the square root with the Am29116.

CONTROL

The Am29501 is controlled by 29 microcode bits which select operations with no encoding. This provides the maximum flexibility for the independent control of parallel operations. Sources may be directed to multiple destinations simultaneously wherever data paths are provided.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0°C to +70°C
Chip Carriers ..... T_C = 0°C to 85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

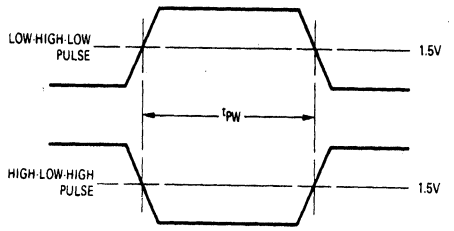
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −2.6mA (COM'L)	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 24mA DIO, MIO			0.5	Volts
				I_{OL} = 8mA Others			0.5	
			MIL	I_{OL} = 16mA DIO, MIO				
				I_{OL} = 8mA Others			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					0.1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 0.5V			−55	μA
I_{OZL}				V_O = 2.4V			100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−100	mA
I_{CC}	Power Supply Current	COM'L and MIL		T_A = 25°C		300		mA
		COM'L Only, V_{CC} = MAX		T_A = 0 to +70°C (Note 4)			400	
				T_A = +70°C (Note 4)			375	
		MIL Only, V_{CC} = MAX		T_C = −55 to +125°C				
				T_C = +125°C				

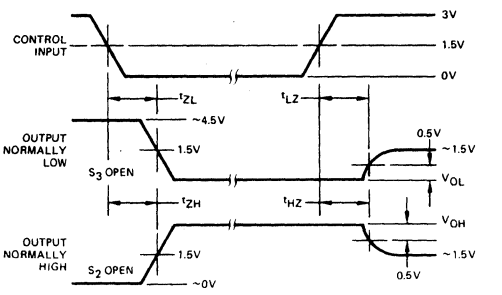
Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Chip Carriers: T_C = 85°C.

PULSE WIDTH



WFR02790

ENABLE AND DISABLE TIMES



WFR02660

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

NOTE: 1. Pulse generator for all pulses: Rate ≤ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SWITCHING CHARACTERISTICS AT ROOM TEMPERATURE

Typical Set-up/Hold Times and Propagation Delays
$V_{CC} = 5.0V$, $T_A = +25°C$, $C_L = 50pF$

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK			17	27	17	23	23	23	27	34	18	ns
DIO			12									ns
MIO						22	22	22	25	22	17	ns
MI				24		22	22	22	25	22	17	ns
C_{IN}				16		10			17	13		ns
SE_{IN}				23		19	19	16	22	19		ns
I_{2-3}(DIO)					14							ns
I_{4-6}(MIO)			15									ns
I_{7-18}(REG)												ns
I_{19-22}(ALU OP)			25			19	19	19	22	19		ns
I_{23-28}(ALU SEL)				31		20	20	20	25	22	14	ns

Am29501 Three-State Timing

Parameters	Description	Test Conditions	Typ $V_{CC} = 5V$, $T_A = 25°C$	Max $V_{CC} = 5V$, $T_A = 25°C$	Commercial Max	Military Max	Units
t_{LZ}	$I_0 \rightarrow DIO_{0-7}$	$C_L = 5pF$, $R_L = 667\Omega$	10		15		ns
	$I_1 \rightarrow MIO_{0-7}$						
t_{HZ}	$I_0 \rightarrow DIO_{0-7}$		10		15		ns
	$I_1 \rightarrow MIO_{0-7}$						
t_{ZL}	$I_0 \rightarrow DIO_{0-7}$	$C_L = 50pF$, $R_L = 667\Omega$	12		20		ns
	$I_1 \rightarrow MIO_{0-7}$						
t_{ZH}	$I_0 \rightarrow DIO_{0-7}$		12		20		ns
	$I_1 \rightarrow MIO_{0-4}$						

SWITCHING CHARACTERISTICS, COMMERCIAL

Minimum Set-up/Hold Times and Maximum Propagation Delays

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK			23	35	24	31	31	31	39	34	26	ns
DIO	10/5		17									ns
MIO	10/5	20/0				29	29	29	34	29	24	ns
MI	10/5	20/0		32		30	29	29	34	29	24	ns
C_{IN}		10/5		25		15			26	19		ns
SE_{IN}		20/0		29		27	27	22	32	27		ns
I_{2-3}(DIO)					21							ns
I_{4-6}(MIO)			22									ns
I_{7-18}(REG)	10/5											ns
I_{19-22}(ALU OP)		20/0	32			27	27	27	32	29		ns
I_{23-28}(ALU SEL)		20/0				29	29	29	35	32	22	ns

SWITCHING CHARACTERISTICS, MILITARY

Minimum Set-up/Hold Times and Maximum Propagation Delays

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK												ns
DIO												ns
MIO												ns
MI												ns
C_{IN}												ns
SE_{IN}												ns
I_{2-3}(DIO)												ns
I_{4-6}(MIO)												ns
I_{7-18}(REG)												ns
I_{19-22}(ALU OP)												ns
I_{23-28}(ALU SEL)												ns

Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in section 13 of this data book.

Am29501 Minimum Clock Pulse Widths

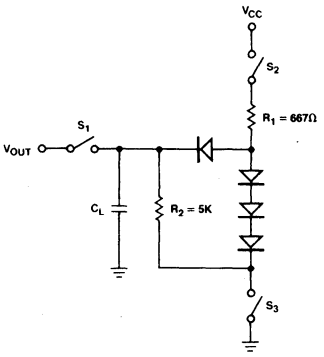
Parameter	Description		TYPICAL	COMMERCIAL	MILITARY	Units
t_{PW}	Clock Pulse Width	High		15		ns
		Low		15		ns

03564A

Refer to Page 13-1 for Essential Information on Military Devices

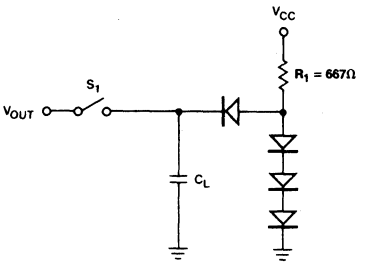
SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



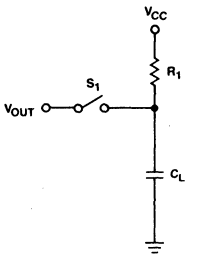
TCR01330

B. NORMAL OUTPUTS



TCR01340

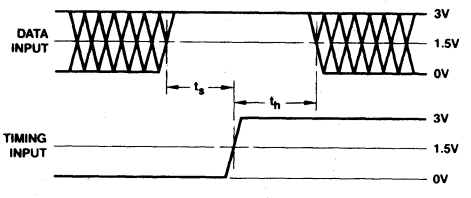
C. OPEN-COLLECTOR OUTPUTS



TC001420

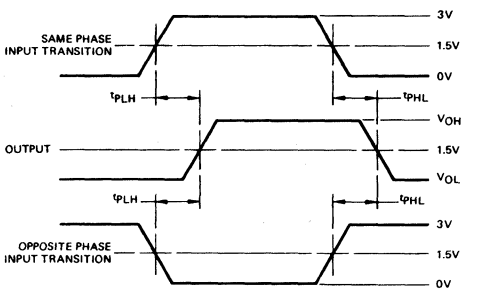
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

SET-UP, HOLD, AND RELEASE TIMES



WFR02970

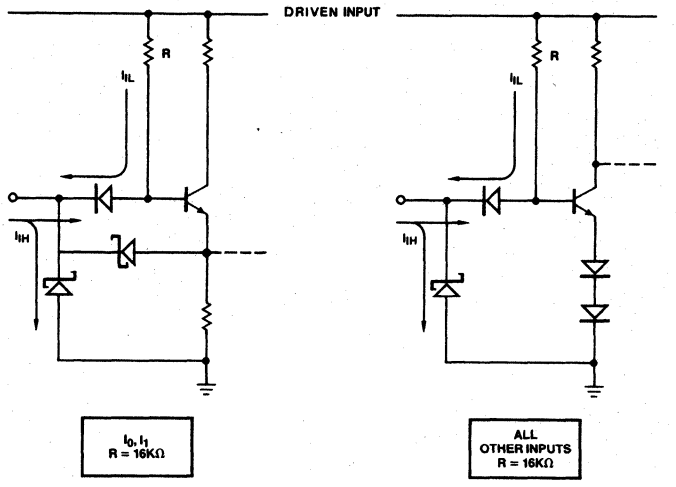
PROPAGATION DELAY



WFR02980

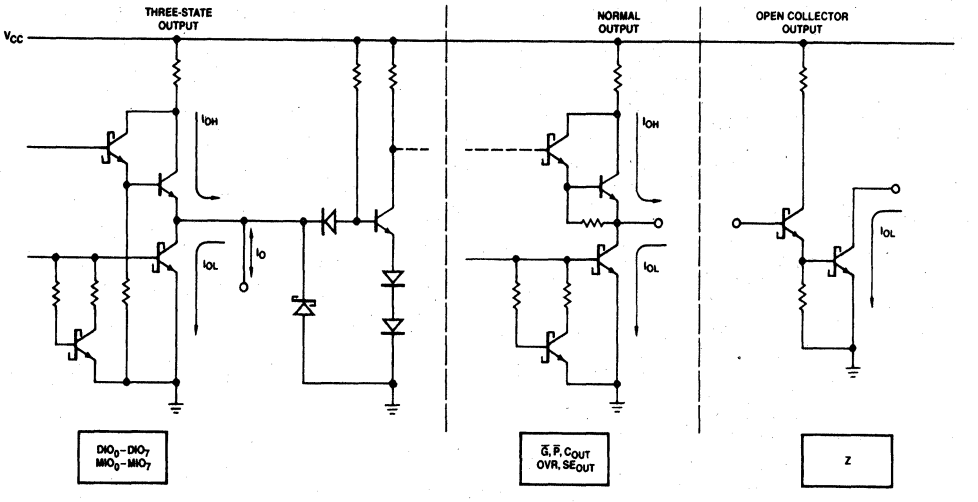
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00530

$C_I \cong 5.0pF$, all inputs



ICR00520

$C_O \cong 5.0pF$, all outputs
Note: Actual current flow direction shown.

Am29509/L509

12 x 12 Multiplier Accumulator

ADVANCED INFORMATION

- Uses two's complement or unsigned inputs and outputs
- Round control
- 27-bit product accumulation result
  - 24-bit product
  - 3-bit extended product
- Output register preload
- Three-state output control
- IMOX™ processing
  - ECL internal circuitry for speed
  - TTL I/O

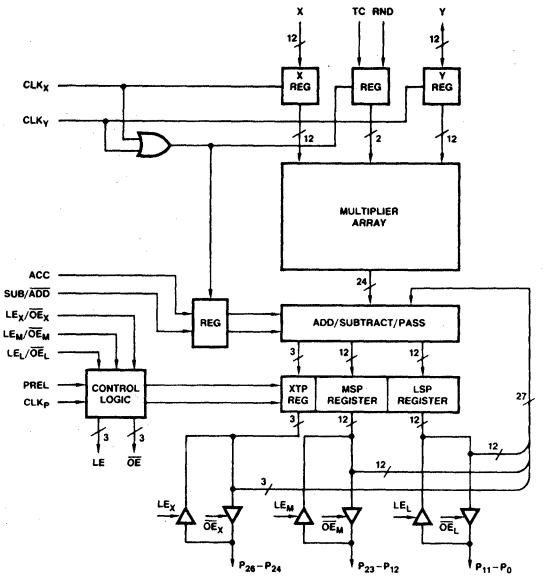
GENERAL DESCRIPTION

The Am29509 is a high-speed 12 x 12-bit multiplier/accumulator (MAC). The X and Y input registers accept 12-bit inputs in two's complement or unsigned magnitude format. A third register stores the Two's Complement (TC), Round (RND), Accumulate (ACC), and Subtraction SUB/$\overline{\text{ADD}}$ control bits. This register is clocked whenever the X or Y input registers are clocked.

The 27-bit accumulator/output register contains the full 24-bit multiplier output which is sign extended or zero-filled based on the TC control bit. The accumulator can also be preloaded from an external source through the bidirectional P-port. The operation of the accumulator is controlled by the signals ACC, SUB/$\overline{\text{ADD}}$, and PREL (Preload). Each of the input registers and output register has independent clocks.

The Am29L509 is a low-power version of the Am29509. The Am29L509 is expected to dissipate 50% less power than the high-speed Am29509.

BLOCK DIAGRAM



BD002830

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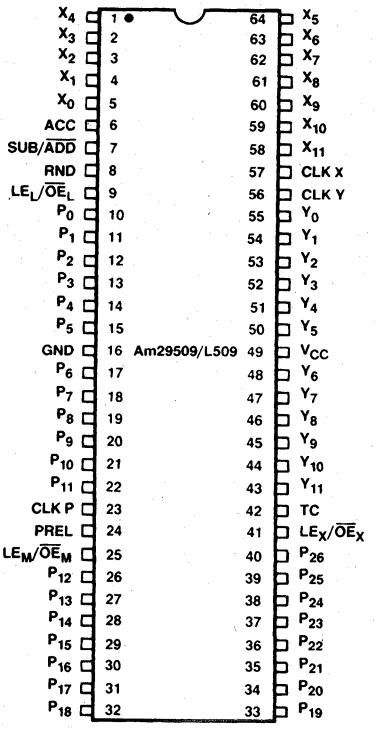
04986C

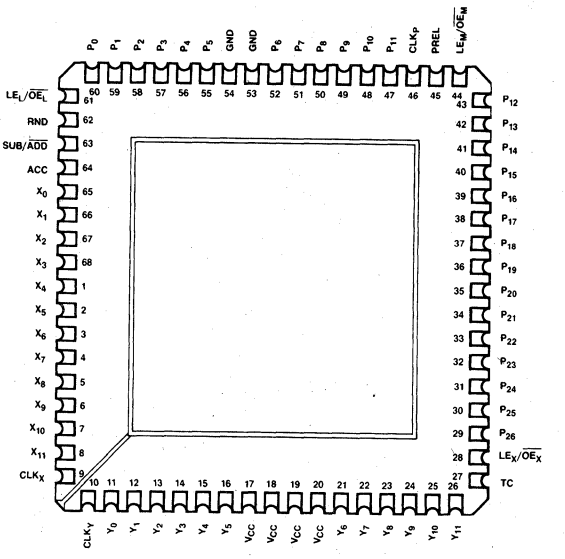
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



CDR04450

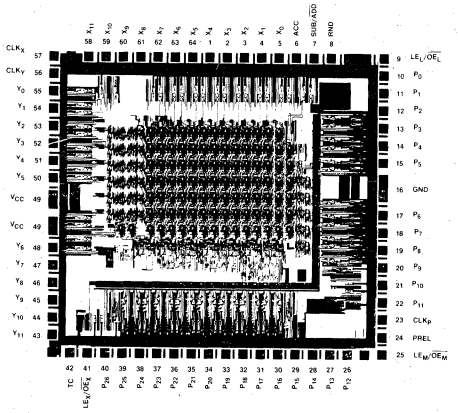
Leadless Chip Carrier



CDR04460

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

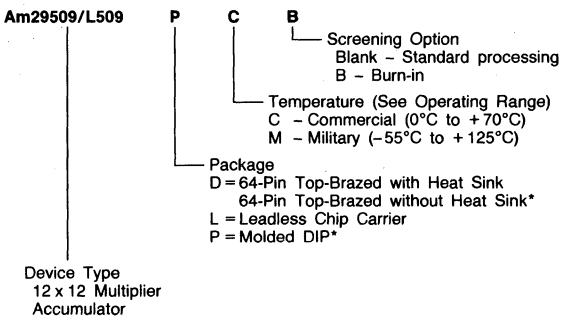


04986C

Refer to Page 13-1 for Essential Information on Military Devices

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



*For low-power version.

Note 1. 160-hour burn-in –
Heat sink parts: $T_A = 125°C$
Non-heat sink parts: $T_A = 85°C$

Valid Combinations	
Am29509	DC, DCB, DMB, LC, LMB
Am29L509	PC*, PCB*

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

*Pin No.	Name	I/O	Description
8	RND	I	Round When RND is High, a bit with a weight of P_{11} is added to the multiplier product. RND is loaded on the rising edge of CLK_X or CLK_Y.
42	TC	I	Two's Complement When High, the X and Y inputs are defined as two's complement data, or as unsigned data when Low. The TC control is loaded on the rising edge of CLK_X or CLK_Y.
24	PREL	I	Preload When High, data is preloaded into the specific output register when its respective Load Enable is High. When Low, the accumulator register is available at the P-port when the Output Enables are Low.
41	$LE_X/\overline{OE}_X$	I	Load Enable Extended/Output Enable Extended Active High Load Enable for the XTP port during preloading. Active Low three-state control for the XTP port during normal operation (see Preload Function). (TSX)**
25	$LE_M/\overline{OE}_M$	I	Load Enable Most/Output Enable Most Active High Load Enable for the MSP port during preloading. Active Low three-state control for the MSP port during normal operation (see Preload Function). (TSM)**
9	$LE_L/\overline{OE}_L$	I	Load Enable Least/Output Enable Least Active High Load Enable for the LSP port during preloading. Active Low three-state control for the LSP port during normal operation (see Preload Function). (TSL)**
57, 56	CLK_X, CLK_Y	I	CLOCKS Load X and Y data respectively and TC, RND, ACC and SUB/$\overline{ADD}$ on the rising edge.
23	CLK_P	I	CLOCK Loads data into the XTP, MSP and LSP registers on the rising edge.
1-5, 58-64	X_{11}-X_0	I	Multiplier Data Input Data is loaded into the X register on the rising edge of CLK_X.
43-48, 50-55	Y_{11}-Y_0	I	Multiplier Data Input Data is loaded into the Y register on the rising edge of CLK_Y.
38-40	P_{26}-P_{24}	I/O	Bidirectional Port Product output for Extended Product (XTP) and input to preload XTP register.
26-37	P_{23}-P_{12}	I/O	Bidirectional Port Product output for the Most Significant Product (MSP) and input to preload MSP register.
10-15, 17-22	P_{11}-P_0	I/O	Bidirectional Port Product output for the Least Significant Product (LSP) and input to preload the LSP register.
6	ACC	I	Accumulate When High, the multiplier product is accumulated in the accumulator. When Low, the multiplier product is written into the accumulator (see Accumulator Function Table). The ACC control is loaded on the rising edge of CLK_X or CLK_Y.
7	SUB/$\overline{ADD}$	I	Subtraction/Addition When High, the accumulator contents are subtracted from the multiplier product and the result written back into the accumulator. When Low, the multiplier product is added into the accumulator (see Accumulator Function Table). The SUB/$\overline{ADD}$ control is loaded on the rising edge of CLK_X or CLK_Y.

*DIP Configuration
**TRW TDC1009 PIN DESIGNATION

PRELOAD FUNCTION

PREL	$LE_X/\overline{OE}_X$	$LE_M/\overline{OE}_M$	$LE_L/\overline{OE}_L$	Output Register		
				XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = output buffers at High impedance (disabled).
Q = output buffers at Low impedance. Contents of output register available through output ports.
PL = output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKp.

ACCUMULATOR FUNCTION TABLE

PREL	ACC	SUB/$\overline{ADD}$	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

DETAILED DESCRIPTION

The Am29509 is a high-speed 12 x 12-bit multiplier/accumulator (MAC). It comprises a 12-bit parallel multiplier followed by a 27-bit accumulator. Two 12-bit input registers are provided for the X and Y operands. A third register stores two control bits, TC and RND. TC selects either a two's complement or an unsigned magnitude format for both data inputs. The RND control, when High, causes a bit to be added to the multiplier product with the weight of P_{11}. This causes the most significant 12-bits of the product to be rounded to the value nearest to the full 24-bit product. Using the RND control once during an accumulation causes the most significant 15-bits of the accumulator to be rounded to the value nearest the full 27-bit accumulation. The TC/RND register is clocked whenever the X or Y input registers are clocked.

The 24-bit multiplier output is zero-filled or sign-extended as appropriate to provide a 27-bit input to the accumulator. The accumulator has four functions: the product may be loaded into the accumulator, the product may be added into the accumulator value, the previous accumulator value may be subtracted from the product and the result stored in the accumulator or the accumulator may be preloaded from an external source. The operation of the accumulator is controlled by the signals ACC, SUB/$\overline{\text{ADD}}$ and PREL. ACC and SUB/$\overline{\text{ADD}}$ are stored in a register clocked whenever the X or Y registers are clocked. ACC in conjunction with SUB/$\overline{\text{ADD}}$ selects one of the first three accumulator functions (see Accumulator Function Table). For output and preloading purposes the accumulator is considered in three sections: Extended Product (XTP, P_{26}–P_{24}) controlled by $LE_X/\overline{OE}_X$, Most Significant Product (MSP, P_{23}–P_{12}) controlled by $LE_M/\overline{OE}_M$ and Least Significant Product (LSP, P_{11}–P_0) controlled by $LE_L/\overline{OE}_L$. When PREL is Low these controls are active-Low Output Enables for the three-state output buffers. When PREL is High the output buffers automatically become high impedance, and the controls operate as active High Load Enables to the three sections of the accumulator to permit preloading of data applied to the bidirectional P port. The P-port has 27-bits.

Am29509/L509
INPUT FORMATS

Fractional Two's Complement Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}
(Sign)											

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}
(Sign)											

Integer Two's Complement Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)											

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)											

Unsigned Fractional Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}

Unsigned Integer Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Am29509/L509
OUTPUT FORMATS
Two's Complement Fractional Output

XTP			MSP										LSP											
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}
(Sign)																										

Two's Complement Integer Output

XTP			MSP										LSP											
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)																										

Unsigned Fractional Output

XTP			MSP										LSP											
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Unsigned Integer Output

XTP			MSP										LSP											
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0 to +70°C
Chip Carriers ..... T_C = 0 to +85°C
Supply Voltage ..... 4.75V to 5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... 4.5V to 5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am29509/L509

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.4mA		2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs					.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					100	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	V_O = 2.4V			25	µA
I_{OZL}				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Product	V_O = 0V	−20		−85	mA
I_{CC}	Power Supply Current	COM'L and MIL	T_A = +25°C	STD Devices				mA
				L Devices				
		COM'L Devices V_{CC} = Max	T_A = 0 to +70°C (Note 4)	STD Devices				
				L Devices				
			T_A = 70°C (Note 4)	STD Devices				
				L Devices				
		MIL Devices V_{CC} = Max	T_C = −55 to +125°C	STD Devices				
				L Devices				
			T_C = +125°C	STD Devices				
				L Devices				

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Chip Carriers: T_C = 85°C.

7

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

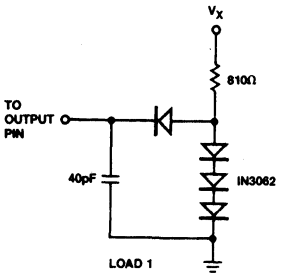
				COMMERCIAL		MILITARY		
				29509		29509		
Parameters	**Description**	**Test Conditions**	**Typ**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{MA}	Multiply Accumulate Time							ns
t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Set-up Time							ns
t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time							ns
t_S	PREL Set-up Time							ns
t_H	PREL Hold Time							ns
t_{PWH}	Clock Pulse Width High							ns
t_{PWL}	Clock Pulse Width Low							ns
t_{PDP}	Output Clock to P							ns
t_{PHZ}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$,	High to Z						ns
t_{PLZ}	$LE_L/\overline{OE}_L$ to P Disable Time	Low to Z						ns
t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$,	Z to High						ns
t_{PZL}	$LE_L/\overline{OE}_L$ to P Enable Time	Z to Low						ns
t_{HCL}	Relative Hold Time							ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

				COMMERCIAL		MILITARY		
				29L509		29L509		
Parameters	**Description**	**Test Conditions**	**Typ**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{MA}	Multiply Accumulate Time							ns
t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Set-up Time							ns
t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time							ns
t_S	PREL Set-up Time							ns
t_H	PREL Hold Time							ns
t_{PWH}	Clock Pulse Width High							ns
t_{PWL}	Clock Pulse Width Low							ns
t_{PDP}	Output Clock to P							ns
t_{PHZ}	$LE_X/\overline{OE}_X$,$LE_M/\overline{OE}_M$,	High to Z						ns
t_{PLZ}	$LE_L/\overline{OE}_L$ to P Disable Time	Low to Z						ns
t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$,	Z to High						ns
t_{PZL}	$LE_L/\overline{OE}_L$ to P Enable Time	Z to Low						ns
t_{HCL}	Relative Hold Time							ns

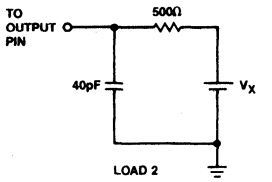
SWITCHING TEST CIRCUIT

Normal Load



TCR01290

Three-State Delay Load



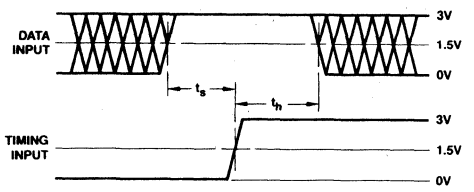
TCR01300

SWITCHING TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, .5V, 0.0V
t_{PZL}	2.6V	2.6V, .5V, V_{OL}

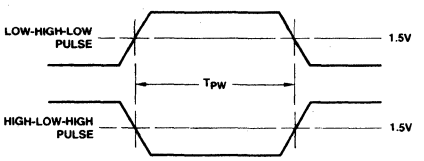
WFR02810

SET-UP AND HOLD TIME



WFR02970

PULSE WIDTH

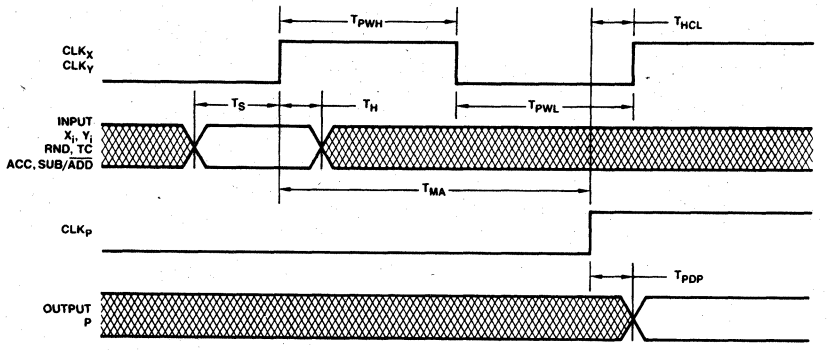


WFR02850

Notes: 1. Diagram shown for HIGH data only.
Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

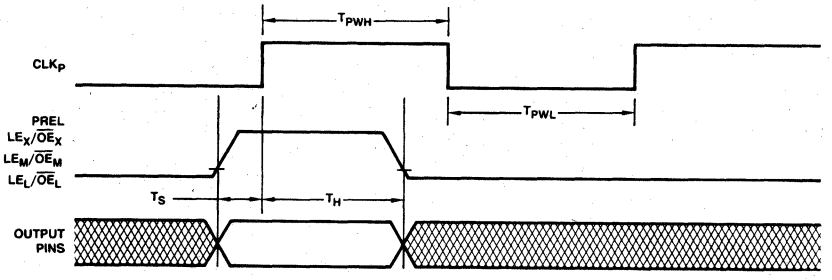
7

Am29509/L509
TIMING DIAGRAMS



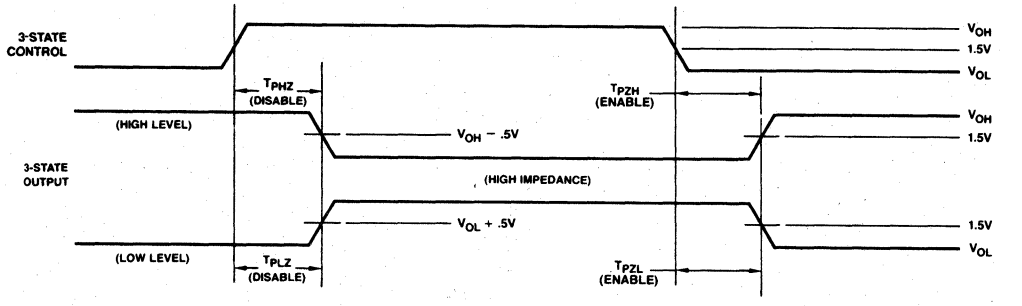
WFR02910

Am29509/L509
PRELOAD TIMING DIAGRAM



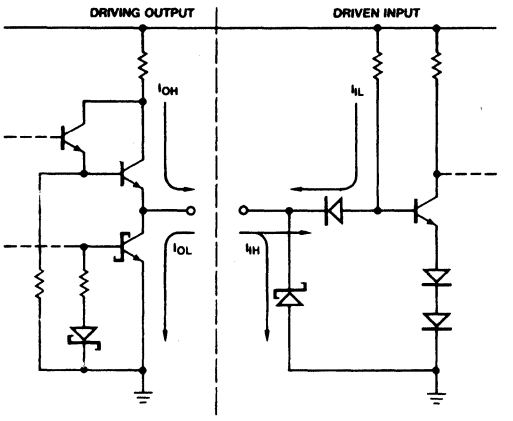
WFR02890

Am29509/L509
THREE-STATE
TIMING DIAGRAM



WFR02900

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00500

RELATED PRODUCTS

Part No.	Description
Am29526/527	High speed Sine function generator
Am29528/529	High speed Cosine function generator
Am29540	Programmable FFT address sequencer
Am29520/21	Multilevel pipeline registers

Am29510/L510

16 X 16 Multiplier Accumulator

DISTINCTIVE CHARACTERISTICS

- Uses two's complement or unsigned inputs and
- Round control
- Output register preload
- 35-bit product accumulator result
  - 32-bit product
  - 3-bit extended product
- IMOX™ processing
  - ECL internal circuitry for speed
  - TTL I/O, Single 5V Supply
- FAST
  - High speed version multiply accumulate time 80ns
  - Low power version multiply accumulate time 110ns

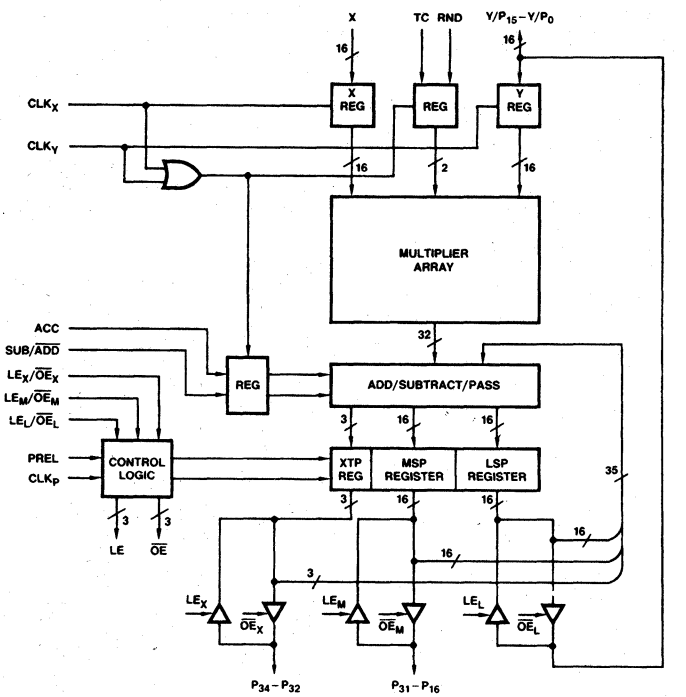
GENERAL DESCRIPTION

The Am29510 is a high-speed 16 x 16-bit multiplier/accumulator (MAC). The X and Y input registers accept 16-bit inputs in either two's complement or unsigned magnitude format. A third register stores the Two's Complement (TC), Round (RND), Accumulator (ACC), and Subtraction/Addition (SUB/$\overline{\text{ADD}}$) control bits. This register is clocked whenever the X or Y input registers are clocked.

The 35-bit accumulator/output register contains the full 32-bit multiplier output which is sign extended or zero-filled based on the TC control bit. The accumulator can also be preloaded from an external source through the bidirectional P port. The operation of the accumulator is controlled by the signals ACC, (Accumulator), SUB/$\overline{\text{ADD}}$ (Subtraction/Addition), and PREL (Preload). Each of the input registers and the output register has independent clocks.

The Am29L510 is a low-power version of the Am29510. The Am29L510 consumes only one-half the power of its standard power counterpart while maintaining nearly two-thirds the speed.

BLOCK DIAGRAM



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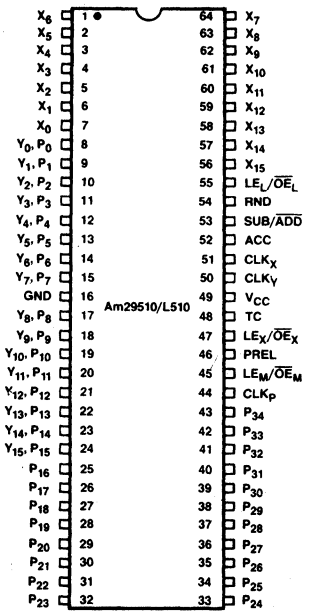
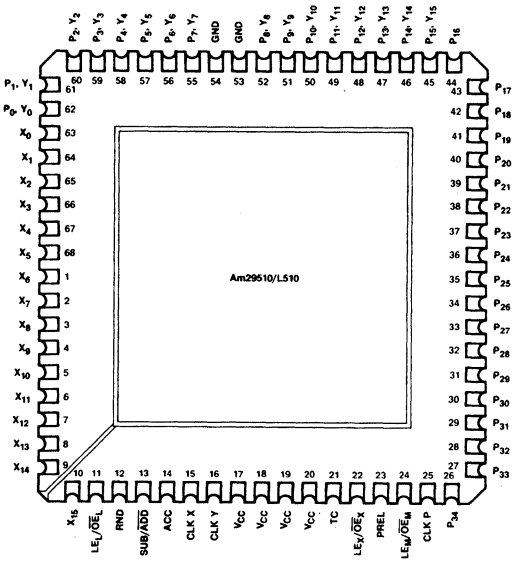
CONNECTION DIAGRAM
Top View

Dual In-Line



CDR04440

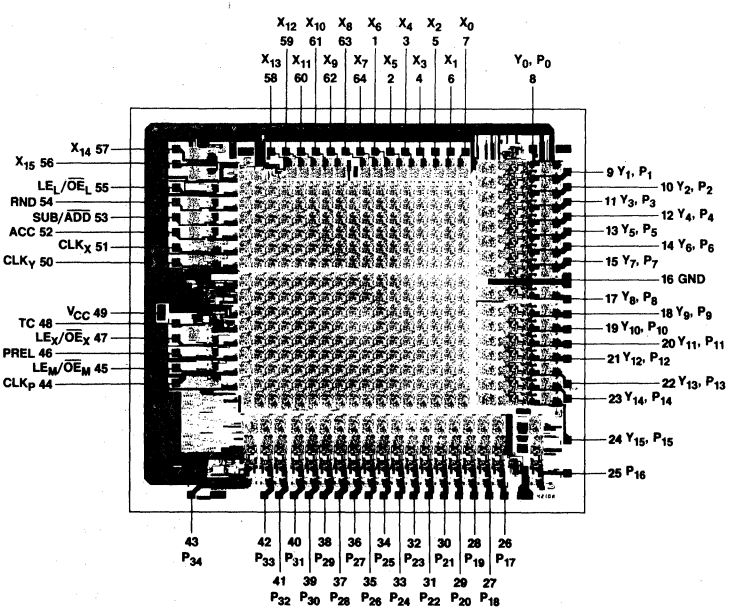
Leadless Chip Carrier



CDR04430

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE: .291" x .258"

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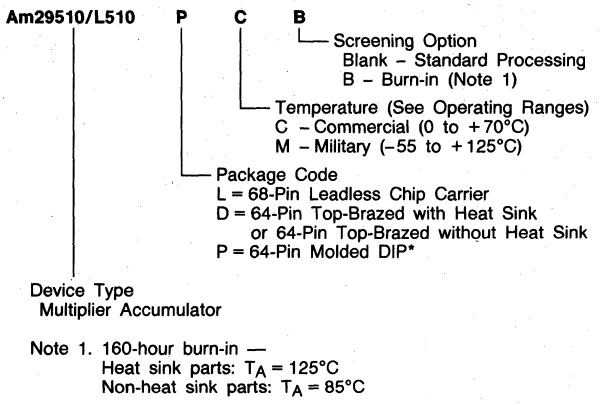
ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Note 1. 160-hour burn-in —
Heat sink parts: $T_A = 125°C$
Non-heat sink parts: $T_A = 85°C$

Valid Combinations	
Am29510	DC, DCB, DMB, LC, LMB, PC*, PCB*
Am29L510	

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
54	RND	I	Round When RND is High, a bit with a weight of P_{15} is added to the multiplier product. RND is loaded on the rising edge of CLK_X or CLK_Y.
48	TC	I	Two's Complement When High, the X and Y inputs are defined as two's complement data, or as unsigned data when Low. The TC control is loaded on the rising edge of CLK_X or CLK_Y.
46	PREL	I	Preload When High, data is preloaded into the specific output register when its respective Load Enable is High. When Low, the accumulator register is available at the P-port when the Output Enables are Low.
47	$LE_X/\overline{OE}_X$	I	Load Enable Extended/Output Enable Extended Active High Load Enable for the XTP port during preloading. Active Low three-state control for the XTP port during normal operation (see Preload Function). (TSX)**
45	$LE_M/\overline{OE}_M$	I	Load Enable Most/Output Enable Most Active High Load Enable for the MSP port during preloading. Active Low three-state control for the MSP port during normal operation (see Preload Function). (TSM)**
55	$LE_L/\overline{OE}_L$	I	Load Enable Least/Output Enable Least Active High Load Enable for the LSP port during preloading. Active Low three-state control for the LSP port during normal operation (see Preload Function). (TSL)**
51, 50	CLK_X, CLK_Y	I	CLOCKS Load X and Y data respectively and TC, RND, ACC and SUB/$\overline{ADD}$ on the rising edge.
44	CLK_P	I	CLOCK Loads data into the XTP, MSP and LSP registers on the rising edge.
1-7, 56-64	X_{15}-X_0	I	Multiplier Data Input Data is loaded into the X register on the rising edge of CLK_X.
8-15, 17-24	Y_{15}-Y_0 P_{15}-P_0	I/O	Bidirectional Port Data is loaded into the Y register on the rising edge of CLK_Y. Product output for Least Significant Product (LSP) and input to preload LSP register.
41-43	P_{34}-P_{32}	I/O	Bidirectional Port Product output for Extended Product (XTP) and input to preload XTP register.
25-40	P_{31}-P_{16}	I/O	Bidirectional Port Product output for the Most Significant Product (MSP) and input to preload MSP register.
52	ACC	I	Accumulate When High, the multiplier product is accumulated in the accumulator. When Low, the multiplier product is written into the accumulator (see Accumulator Function Table). The ACC control is loaded on the rising edge of CLK_X or CLK_Y.
53	SUB/$\overline{ADD}$	I	Subtraction/Addition When High, the accumulator contents are subtracted from the multiplier product and the result written back into the accumulator. When Low, the multiplier product is added into the accumulator (see Accumulator Function Table). The SUB/$\overline{ADD}$ control is loaded on the rising edge of CLK_X or CLK_Y.

*DIP Configuration
**TRW TDC1010 Pin Designation

PRELOAD FUNCTION

PREL	$LE_X/\overline{OE}_X$	$LE_M/\overline{OE}_M$	$LE_L/\overline{OE}_L$	Output Register XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = output buffers at High impedance (disabled).
Q = output buffers at Low impedance. Contents of output register available through output ports.
PL = output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKp.

ACCUMULATOR FUNCTION TABLE

PREL	ACC	SUB/$\overline{ADD}$	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

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Refer to Page 13-1 for Essential Information on Military Devices

DETAILED DESCRIPTION

The Am29510 is a high-speed 16 x 16-bit multiplier/accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. Two 16-bit input registers are provided for the X and Y operands. A third register stores two control bits, TC and RND. TC selects either a two's complement or an unsigned magnitude format for both data inputs. The RND control, when High, causes a bit to be added to the multiplier product with the weight of P_{15}. This causes the most significant 16-bits of the product to be rounded to the value nearest to the full 32-bit product. Using the RND control once during an accumulation causes the most significant 19-bits of the accumulator to be rounded to the value nearest the full 35-bit accumulation. The TC/RND register is clocked whenever the X or Y input registers are clocked.

The 32-bit multiplier output is zero-filled or sign-extended as appropriate to provide a 35-bit input to the accumulator. The accumulator has four functions: the product may be loaded into the accumulator, the product may be added into the accumulator value, the previous accumulator value may be subtracted from the product and the result stored in the accumulator or the accumulator may be preloaded from an external source. The operation of the accumulator is controlled by the signals ACC, SUB/$\overline{\text{ADD}}$ and PREL. ACC and SUB/$\overline{\text{ADD}}$ are stored in a register clocked whenever the X or Y registers are clocked. ACC in conjunction with SUB/$\overline{\text{ADD}}$ selects one of the first three accumulator functions (see Accumulator Function Table). For output and preloading purposes the accumulator is considered in three sections: Extended Product (XTP, P_{34}-P_{32}) controlled by $LE_X/\overline{OE}_X$, Most Significant Product (MSP, P_{31}-P_{16}) controlled by $LE_M/\overline{OE}_M$ and Least Significant Product (LSP, P_{15}-P_0) controlled by $LE_L/\overline{OE}_L$. When PREL is Low these controls are active-Low Output Enables for three-state output buffers. When PREL is High the output buffers automatically become high impedance, and the controls operate as active-High Load Enables to the three sections of the accumulator to permit preloading of data applied to the bidirectional P port. The P-port has 35 bits, the least significant 16 of which share pins with the Y input.

Am29510/L510 INPUT FORMATS

Fractional Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Integer Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)															

Unsigned Fractional Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

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Refer to Page 13-1 for Essential Information on Military Devices

Am29510/L510
OUTPUT FORMATS

Two's Complement Fractional Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)																																		

Two's Complement Integer Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)																																		

Unsigned Fractional Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0 to +70°C
Chip Carriers ..... T_C = 0 to +85°C
Supply Voltage ..... 4.75V to 5.25V

Military (M) Devices
Temperature ..... T_C = −55°C to +125°C
Supply Voltage ..... 4.5V to 5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am29510

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.4mA		2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs					.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					75	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Y, Product	V_O = 2.4V			25	µA
I_{OZL}				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Y, Product	V_O = 0V	−3		−30	mA
I_{CC}	Power Supply Current	COM'L and MIL		T_A = 25°C		750		mA
		COM'L Only V_{CC} = Max		T_A = 0 to +70°C (Note 4)			900	
				T_A = +70°C (Note 4)			725	
		MIL Only V_{CC} = Max		T_{CC} = −55 to +125°C			1000	
				T_{CC} = +125°C			750	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Chip Carriers: T_A = 85°C.

DC CHARACTERISTICS over operating range unless otherwise specified

Am29L510

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −0.4mA	2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA		.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					.8	Volts
				COM'L			.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					75	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	V_O = 2.4V			25	μA
I_{OZL}				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Y	V_O = 0V	−3		−30	mA
			Product	V_O = 0V	−3		−30	
I_{CC}	Power Supply Current	COM'L and MIL		T_A = 25°C		330		mA
		COM'L Only V_{CC} = Max		T_A = 0 to +70°C (Note 4)			450	
				T_A = +70°C (Note 4)			350	
		MIL Only V_{CC} = Max		T_{CC} = −55 to +125°C			535	
				T_{CC} = +125°C			375	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Chip Carriers, T_C = 85°C.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditions	Typ (Note 1)	COMMERCIAL 29510 Min	COMMERCIAL 29510 Max	MILITARY 29510 Min	MILITARY 29510 Max	Units
t_{MA}	Multiply Accumulate Time			50		80		90	ns
t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Set-up Time			12	25		30		ns
t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time			0	5		5		ns
t_S	PREL Setup Time			10	25		30		ns
t_H	PREL Hold Time			0	0		2		ns
t_{PWH}	Clock Pulse Width High			10	20		25		ns
t_{PWL}	Clock Pulse Width Low			10	20		25		ns
t_{PDP}	Output Clock to P			25		40		40	ns
t_{PDY}	Output Clock to Y			25		40		40	ns
t_{PHZ}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$ to P, $LE_L/\overline{OE}_L$ to Y Disable Time	High to Z		21		35		40	ns
t_{PLZ}		Low to Z		20		35		40	ns
t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$ to P, $LE_L/\overline{OE}_L$ to Y Enable Time	Z to High		28		40		40	ns
t_{PZL}		Z to Low		24		40		40	ns
t_{HCL}	Relative Hold Time				0		0		ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	Typ (Note 1)	COMMERCIAL 29L510 Min	COMMERCIAL 29L510 Max	MILITARY 29L510 Min	MILITARY 29L510 Max	Units
t_{MA}	Multiply Accumulate Time			70		110		120	ns
t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Set-up Time			20	40		45		ns
t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time			−3	0		0		ns
t_S	PREL Set-up Time			15	27		35		ns
t_H	PREL Hold Time			−5	0		0		ns
t_{PWH}	Clock Pulse Width High			15	25		30		ns
t_{PWL}	Clock Pulse Width Low			15	25		30		ns
t_{PDP}	Output Clock to P			35		45		50	ns
t_{PDY}	Output Clock to Y			35		45		50	ns
t_{PHZ}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$ to P, $LE_L/\overline{OE}_L$ to Y Disable Time	High to Z		24		35		40	ns
t_{PLZ}		Low to Z		25		35		40	ns
t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$ to P, $LE_L/\overline{OE}_L$ to Y Enable Time	Z to High		38		45		50	ns
t_{PZL}		Z to Low		32		40		45	ns
t_{HCL}	Relative Hold Time				0		0		ns

Note: 1. Typical limits are $V_{CC} = 5V$ and $T_A = 25°C$.

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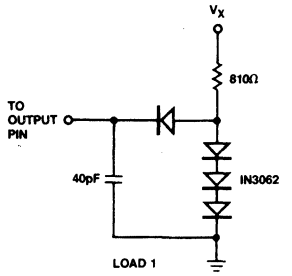
Refer to Page 13-1 for Essential Information on Military Devices

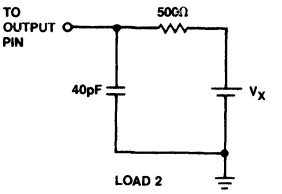
SWITCHING TEST CIRCUIT

Normal Load



TCR01270

Three-State Delay Load



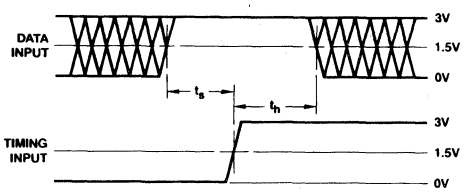
TCR01280

SWITCHING TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PDS}	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, V_{OL}, 0.5V
t_{PZH}	0.0V	V_{OH}, .5V, 0.0V
t_{PZL}	2.6V	2.6V, .5V, V_{OL}

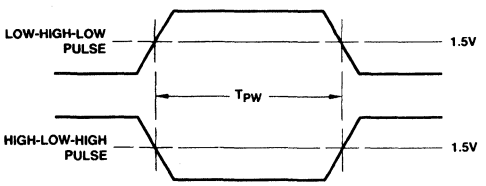
WFR02810

SET-UP AND HOLD TIME



WFR02970

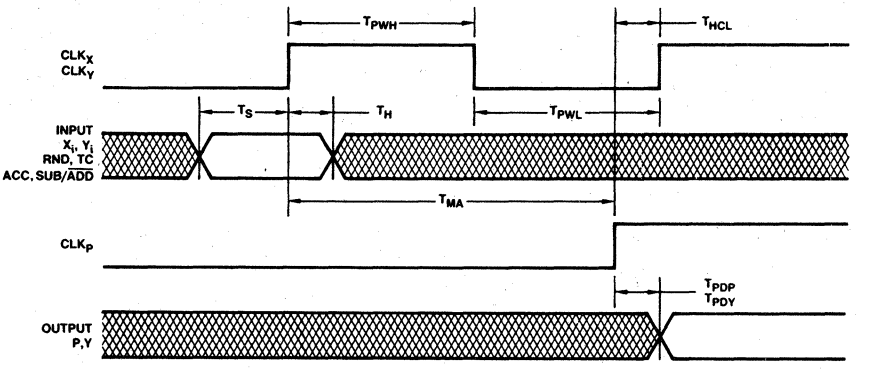
PULSE WIDTH



WFR02850

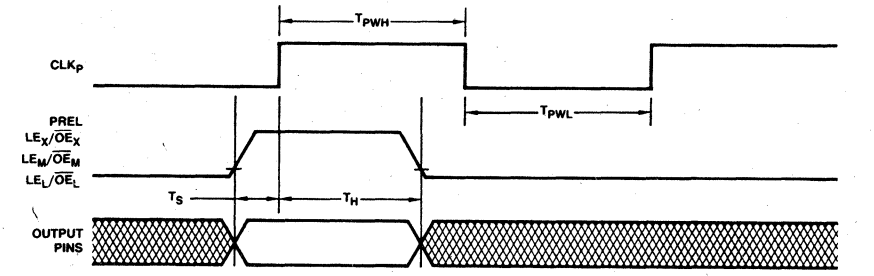
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Am29510/L510
TIMING DIAGRAMS



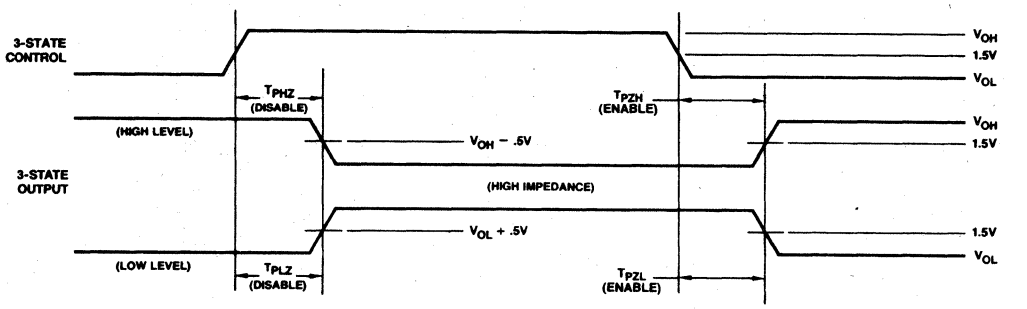
WFR02820

Am29510/L510
PRELOAD TIMING DIAGRAM



WFR02830

Am29510/L510
THREE-STATE
TIMING DIAGRAM

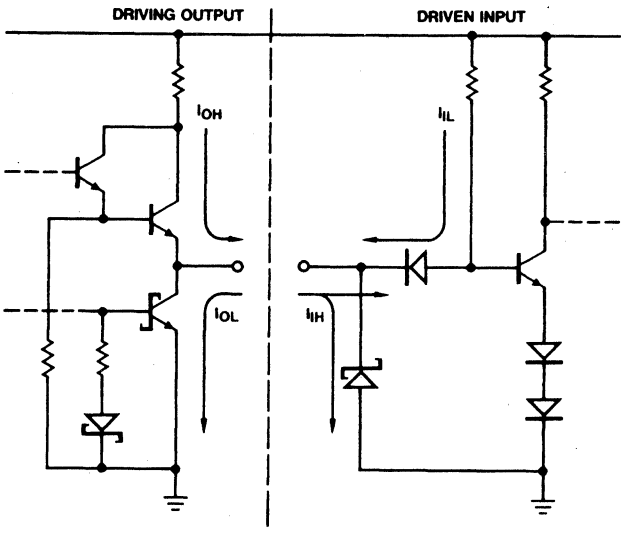


WFR02840

03563B

Refer to Page 13-1 for Essential Information on Military Devices

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00490

RELATED PRODUCTS

Part No.	Description
Am29526/527	High speed Sine function generator
Am29528/529	High Speed Cosine function generator
Am29540	Programmable FFT address sequencer
Am29520/21	Multilevel pipeline registers

Am29516/17 Family

16 x 16-Bit Parallel Multipliers

DISTINCTIVE CHARACTERISTICS

- High speed 16 x 16 multiplier
- Two's complement, unsigned or mixed operands
- Full product multiplexed at output
- Improved speed: 38ns clocked multiply (A devices) Reduced power dissipation: 2W (L devices)
- Am29516 pin and functionally compatible with TRW MPY-16HJ — Am29517 optimized for microprogramming, single clock with register enables
- TTL I/O-single +5V supply – 64-pin package

GENERAL DESCRIPTION

The Am29516 and Am29517 are high speed parallel 16 x 16-bit multipliers utilizing internal ECL logic to generate a 32-bit product. 17-bit input registers are provided for the X and Y operands and their associated mode controls X_M and Y_M. These mode controls are used to specify the operands as two's complement or unsigned numbers.

At the output of the multiplier array, a format adjust control (FA), allows the user to select either a full 32-bit product or a left-shifted 31-bit product suitable for two's complement only.

Two 16-bit output registers are provided to hold the most and least significant halves of the product (MSP and LSP) as defined by FA. For asynchronous output, these registers may be made transparent by taking the feedthrough control (FT) high. A round control (RND) allows the rounding of the MSP; this control is registered, and is entered whenever either input register is clocked.

The two halves of the product may be routed to a 16-bit 3-state output port (P) via a multiplexer, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

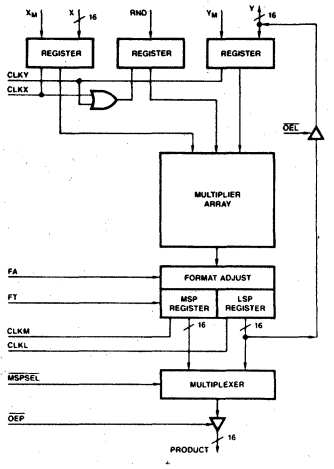
The Am29516 X, Y, MSP and LSP registers have independent clocks (CLKX, CLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY 16HJ. When this control is LOW the function is that of the MPY16HJ, thus allowing full compatibility.

The Am29517 differs in that it has a single clock input (CLK) and three register enables ($\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$) for the two input registers and the entire product, respectively. This facilitates the use of the part in microprogrammed systems. In both parts data is entered into the registers on the positive edge of the clock.

The Am29516A and Am29517A are higher speed versions of the Am29516 and Am29517, respectively, offering greater than 40% speed improvement while the Am29L516 and Am29L517 low-power versions consume only one-half the power of their standard power counterparts.

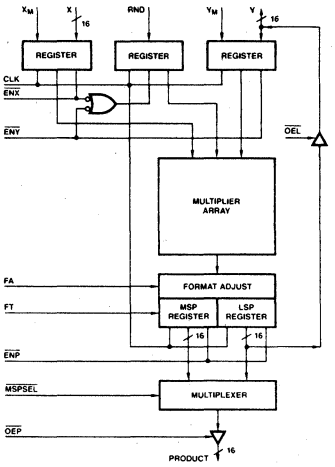
BLOCK DIAGRAM

Am29516/29516A/29L516



BD002840

Am29517/29517A/29L517



BD002850

03562C

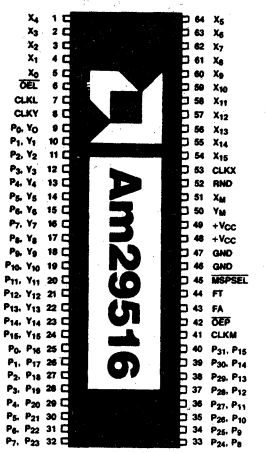
Refer to Page 13-1 for Essential Information on Military Devices

RELATED PRODUCTS

Part No.	Description
Am29501	Multi-port Pipelined Processor
Am29526/27	Sine Function Generator
Am29528/29	Cosine Function Generator
Am29520/21	Pipeline Register
Am29540	Address Generator

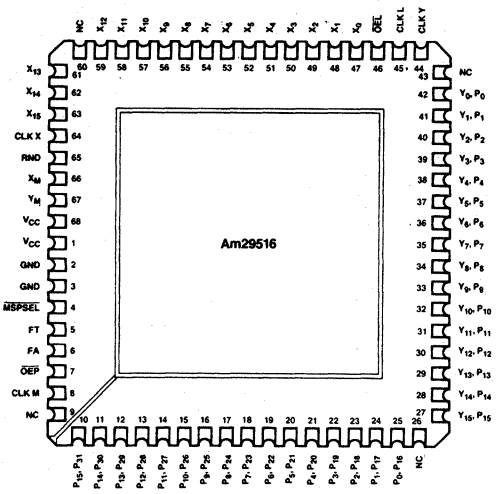
CONNECTION DIAGRAM
Top View

D-64-3



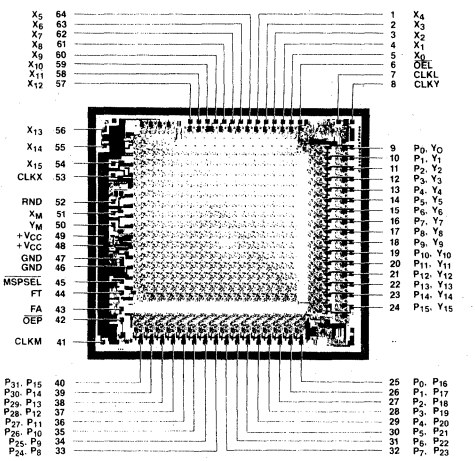
CDR04380

L-68-3



CDR04410

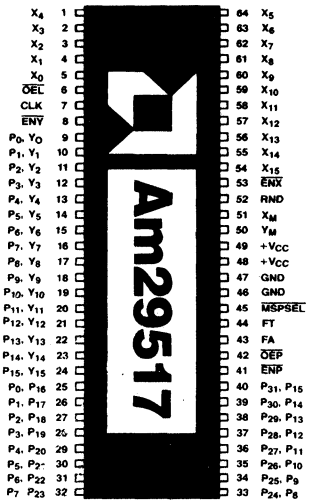
METALLIZATION AND PAD LAYOUT
Am29516A/29L516/29516



STANDARD DEVICE DIE SIZE: 250 X 222 MILS
'A' DEVICE DIE SIZE: 178 X 190 MILS
'L' DEVICE DIE SIZE: 250 X 222 MILS

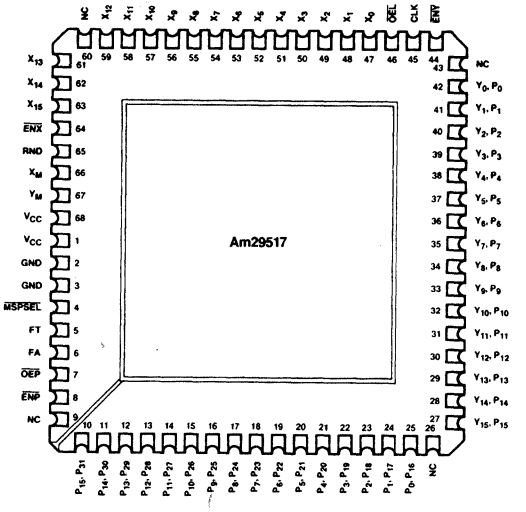
CONNECTION DIAGRAM
Top View

D-64-3



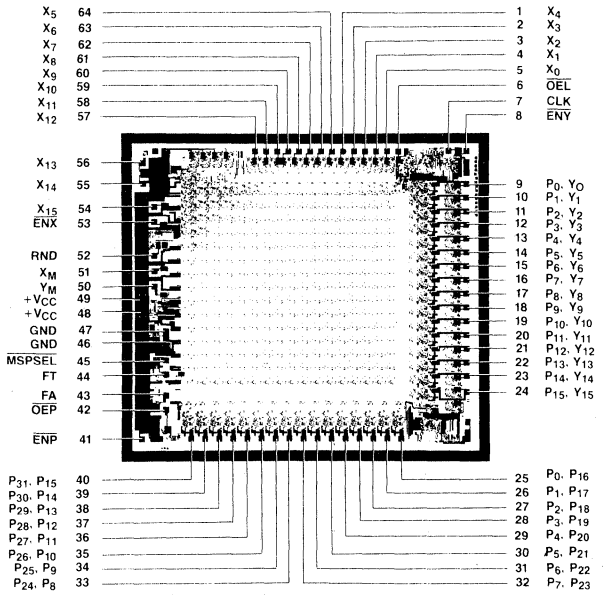
CDR04390

L-68-3



CDR04400

METALLIZATION AND PAD LAYOUT
Am29517A/29L517/29517

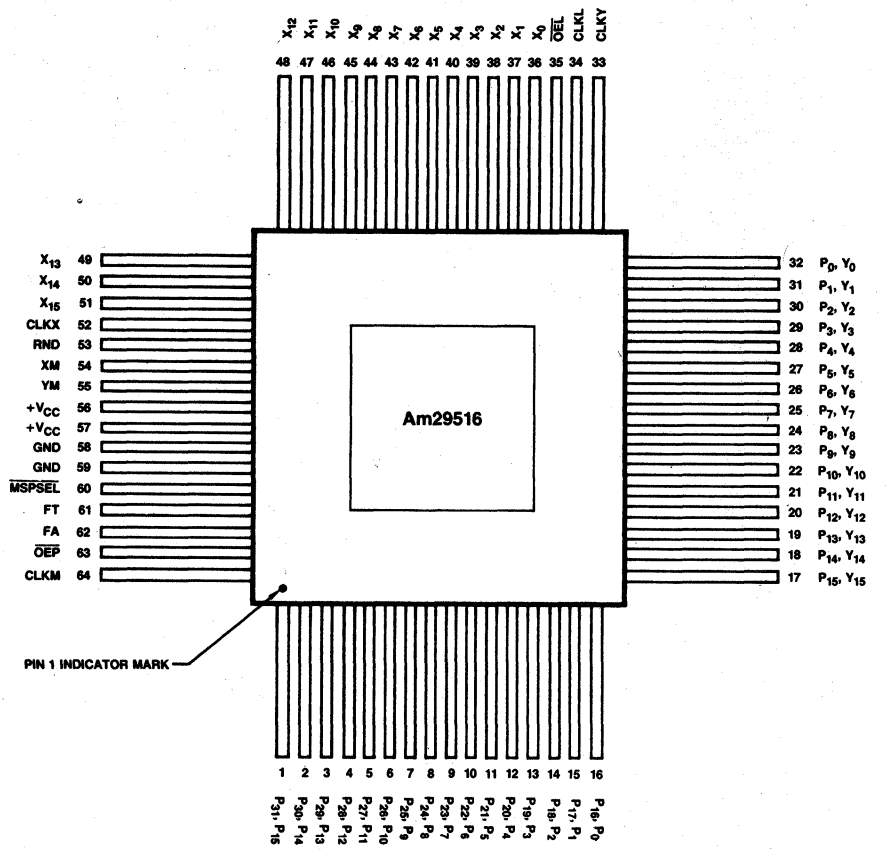


STANDARD DEVICE DIE SIZE: 250 X 222 MILS
'A' DEVICE DIE SIZE: 178 X 190 MILS
'L' DEVICE DIE SIZE: 250 X 222 MILS

03562C

Refer to Page 13-1 for Essential Information on Military Devices

F-64-3S



CDR04370

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29516 **P** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in (Note 1)
- **C** — Temperature (see Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- **P** — Package
  - D – TD-64-2 (64-pin CERDIP) – with heat sink*
  - F – F-64-35 (64-pin flatpak)
  - L = L-68-3 (68-TERMINAL Chip Carrier)
  - P = 64-pin Molded DIP
- Speed Select
  - 38ns = 29516A, 29517A
  - 65ns = 29516, 29517
  - 90ns = 29L516, 29L517
- Device Type
  - 29516, 29516A
  - 29517, 29517A
  - 29L516, 29L517

*TD-64-1 (64-pin CERDIP) without heat sink for Low-Power versions

Note 1. 160-hour burn-in –
Heat sink parts: $T_A = 125°C$
Non-heat sink parts: $T_A = 85°C$

Valid Combinations	
Am29516	DC, DCB, DMB – with heat sink FMB, LMB – without heat sink
Am29517 Am29516A Am29517A	DC, DCB, DMB – with heat sink LMB – without heat sink
Am29L516 Am29L517	PC, PCB, DC, DCB, DM, DMB, LMB without heat sink

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

7

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
1-5, 54-64	X_0-X_{15}	I	Multiplicand Data inputs.
9-24	Y_0-Y_{15}, P_0-P_{15}	I/O	Multiplier Data inputs or Least Significant Product (LSP) output.
25-40	P_{16}-P_{31}, P_0-P_{15}	O	MSP product port when $\overline{MSPSEL}$ is LOW. LSP product port when $\overline{MSPSEL}$ is HIGH.
51, 50	X_M,Y_M (TCX, TCY)**	I	Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data.
43	FA(RS)**	I	Format adjust control selects either a full 32-bit product (HIGH) or a left shifted 31-bit product with the sign bit replicated in the LSP (LOW). This control is normally high, except for certain fractional two's complement applications. (See Multiplier output formats table.)
44	FT	I	Feedthrough control (HIGH) makes both MSP and LSP registers transparent.
45	$\overline{MSPSEL}$	I	Selects either MSP (LOW) or LSP (HIGH) to be available at the product output port.
52	RND	I	Control for rounding the MSP. Adds a binary one to the most significant bit of the LSP for two's complement and unsigned numbers.
42	$\overline{OEP}$ (TRIM)**	I	Three-state enable for product output port.
6	$\overline{OEL}$ (TRIL)**	I	Three-state enable for routing LSP through Y input/output port.
Am29516 ONLY			
53, 8, 41, 7	CLKX CLKY CLKM CLKL	I	Register Clock, X_{15-0}, X_M, RND Register Clock, Y_{15-0}, Y_M, RND MSP Register Clock LSP Register Clock
Am29517 ONLY			
7, 53 8, 41	CLK $\overline{ENX}$ $\overline{ENY}$ $\overline{ENP}$	I	Clock, All Registers Register Enable, X_{15-0}, X_M, RND Register Enable, Y_{15-0}, Y_M, RND Register Enable MSP, LSP

*DIP Configuration
**TRW MPY 16HJ pin designation

INPUT FORMATS (All Devices)

Fractional Two's Complement Input Format

X_M, Y_M = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Integer Two's Complement Input Format

X_M, Y_M = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)															

Unsigned Fractional Input Format

X_M, Y_M = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input Format

X_M, Y_M = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

OUTPUT FORMATS
(All Devices)

Fractional 2's Complement (Shifted)* Output

FA = 0

MSP																LSP															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	-2^{0}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)																(Sign)															

Fractional 2's Complement Output

FA = 1

MSP																LSP															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)																															

Integer Two's Complement Output

FA = 1

MSP																LSP															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)																															

Unsigned Fractional Output

FA = 1

MSP																LSP															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

FA = 1

MSP																LSP															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

*In this format an overflow occurs in the attemped multiplication of the two's complement number 1.000...(−1) with itself, yielding a product of 1.000... or −1.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0°C to +70°C
Chip Carriers ..... T_C = 0°C to 85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am29516/29517

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.4mA		2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					75	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	V_O = 2.4V			25	μA
I_{OZL}				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 2)	V_{CC} = MAX	Y, Product	V_O = 0V	−3		−30	mA
I_{CC}	Power Supply Current (Note 3)		T_A = +25°C			600		mA
		COM'L Devices V_{CC} = MAX	T_A = 0 to +70°C (Note 4)				800	
			T_A = +70°C (Note 4)				750	
		MIL Devices V_{CC} = MAX	T_A = −55 to +125°C				900	
			T_A = +125°C				800	

Notes: 1. Typical limits are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. $\overline{OEP}$ and $\overline{OEL}$ LOW with all product (MSP and LSP) bits LOW.
4. Chip Carriers: T_C = 85°C.

DC CHARACTERISTICS over operating range unless otherwise specified
Am29516A/29L516/Am29517A/29L517

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.4mA		2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					75	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	V_O = 2.4V			25	μA
I_{OZL}				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 2)	V_{CC} = MAX	Y, Product	V_O = 0V	−3		−30	mA
I_{CC}	Power Supply Current (Note 3)	COM'L Devices V_{CC} = MAX	T_A = +25°C	A Devices		600		mA
				L Devices		300		
			T_A = 0 to +70°C (Note 4)	A Devices			800	
				L Devices			400	
			T_A = +70°C (Note 4)	A Devices			750	
				L Devices			350	
		MIL Devices V_{CC} = MAX	T_C = −55 to +125°C	A Devices			900	
				L Devices			440	
			T_{CC} = +125°C	A Devices			800	
				L Devices			350	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. $\overline{OEP}$ and $\overline{OEL}$ LOW with all product (MSP and LSP) bits LOW.
4. Chip Carriers: T_C = 85°C.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)
Am29516/29517

Parameters	Description		Test Conditions	Typ	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{MUC}	Unclocked Multiply Time		Load 1	50		85		95	ns
t_{MC}	Clocked Multiply Time			40		65		75	ns
t_S	X_i, Y_i, RND Set-up Time			10	20		25		ns
t_H	X_i, Y_i, RND Hold Time			0	3		3		ns
t_{PWH}	Clock Pulse Width High			10	15		15		ns
t_{PWL}	Clock Pulse Width Low			10	15		15		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out			20		30		35	ns
t_{PDP}	Output Clock to P			20		30		35	ns
t_{PDY}	Output Clock to Y			20		30		35	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	High to Z	Load 2	12		23		28	ns
t_{PLZ}		Low to Z		15		23		28	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to High		25		32		35	ns
t_{PZL}		Z to Low		25		32		35	ns
t_{PHZ}	$\overline{OEL}$ Disable Time	High to Z		12		23		28	ns
t_{PLZ}		Low to Z		15		23		28	ns
t_{PZH}	$\overline{OEL}$ Enable Time	Z to High		25		32		35	ns
t_{PZL}		Z to Low		25		32		35	ns
t_S	Clock Enable Set-up Time (Am29517 Only)		Load 1	5	10		15		ns
t_H	Clock Enable Hold Time (Am29517 Only)			0	3		3		ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (See Note 2) (Am29516 Only)			0	0		0		ns

Notes: 1. Switching Characteristics are measured and guaranteed for T_A as specified with 200 Lf/min flowing across the device.
2. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Am29L516/29L517

Parameters	Description		Test Conditions	Typ	COMMERCIAL Min	COMMERCIAL Max	MILITARY* Min	MILITARY* Max	Units
t_{MUC}	Unclocked Multiply Time		Load 1	90		120		135	ns
t_{MC}	Clocked Multiply Time			70		90		100	ns
t_S	X_i, Y_i, RND Set-up Time				25		25		ns
t_H	X_i, Y_i, Hold Time				0		0		ns
t_H	RND Hold Time				3		3		ns
t_{PWH}	Clock Pulse Width High				20		20		ns
t_{PWL}	Clock Pulse Width Low				20		20		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out			25		35		40	ns
t_{PDP}	Output Clock to P			25		35		40	ns
t_{PDY}	Output Clock to Y			25		35		40	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	High to Z	Load 2	20		30		35	ns
t_{PLZ}		Low to Z		20		30		35	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to High		25		35		40	ns
t_{PZL}		Z to Low		25		35		40	ns
t_{PHZ}	$\overline{OEL}$ Disable Time	High to Z		20		30		35	ns
t_{PLZ}		Low to Z		20		30		35	ns
t_{PZH}	$\overline{OEL}$ Enable Time	Z to High		25		35		40	ns
t_{PZL}		Z to Low		25		35		40	ns
t_S	Clock Enable Set-up Time (Am29L517 Only)		Load 1	10	15		20		ns
t_H	Clock Enable Hold Time (Am29L517 Only)				3		5		ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (See Note 2) (Am29L516 Only)				0		0		ns

Notes: 1. Switching Characteristics are measured and guaranteed for T_A as specified with 200 Lf/min flowing across the device.
2. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

*PRELIMINARY

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)
Am29516A/517A

Parameters	Description		Test Conditions	Typ	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{MUC}	Unclocked Multiply Time		Load 1	45		58		65	ns
t_{MC}	Clocked Multiply Time			30		38		42	ns
t_S	X_i, Y_i, Set-up Time			4	7		8		ns
t_H	X_i, Y_i, Hold Time			1	3		3		ns
t_S	RND Set-up Time			4	7		8		ns
t_H	RND Hold Time			1	3		3		ns
t_{PWH}	Clock Pulse Width High			7	7		8		ns
t_{PWL}	Clock Pulse Width Low			7	3		3		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out			13		18		21	ns
t_{PDP}	Output Clock to P			15		20		23	ns
t_{PDY}	Output Clock to Y			15		20		23	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	High to Z	Load 2	13		15		17	ns
t_{PLZ}		Low to Z		12		15		17	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to High		20		23		25	ns
t_{PZL}		Z to Low		15		23		25	ns
t_{PHZ}	$\overline{OEL}$ Disable Time	High to Z		13		15		17	ns
t_{PLZ}		Low to Z		12		15		17	ns
t_{PZH}	$\overline{OEL}$ Enable Time	Z to High		20		23		25	ns
t_{PZL}		Z to Low		15		23		25	ns
t_S	Clock Enable Set-up Time (Am29517A Only)		Load 1		10		15		ns
t_H	Clock Enable Hold Time (Am29517A Only)				3		3		ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (See Note 2) (Am29516A Only)			−1					ns

Notes: 1. Switching Characteristics are measured and guaranteed for T_A as specified with 200 Lf/min flowing across the device.
2. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

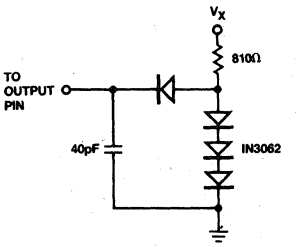
Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0.0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs under license.

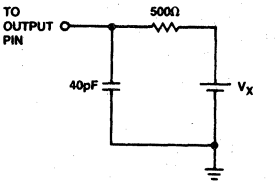
SWITCHING TEST CIRCUIT

Normal Load (Load 1)



TCR01250

Three-State Delay Load (Load 2)



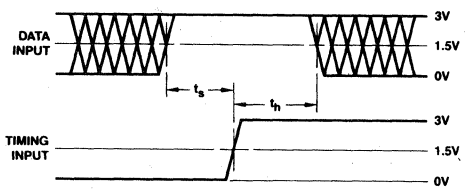
TCR01260

TEST WAVEFORMS
(All Devices)

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, 1.5V, 0.0V
t_{PZL}	2.6V	2.6V, 1.5V, V_{OL}

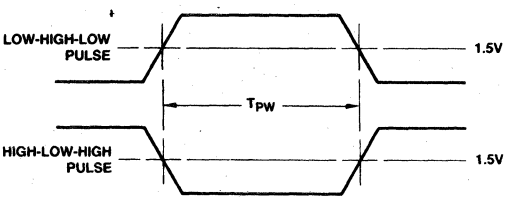
WFR02780

SETUP AND HOLD TIME
(All Devices)



WFR02970

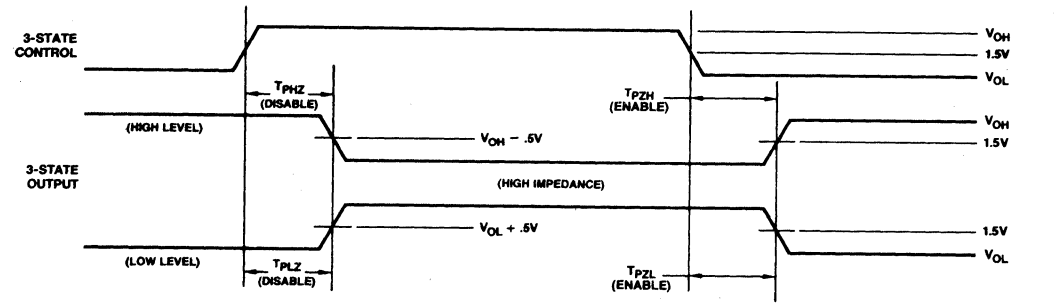
PULSE WIDTH
(All Devices)



WFR02850

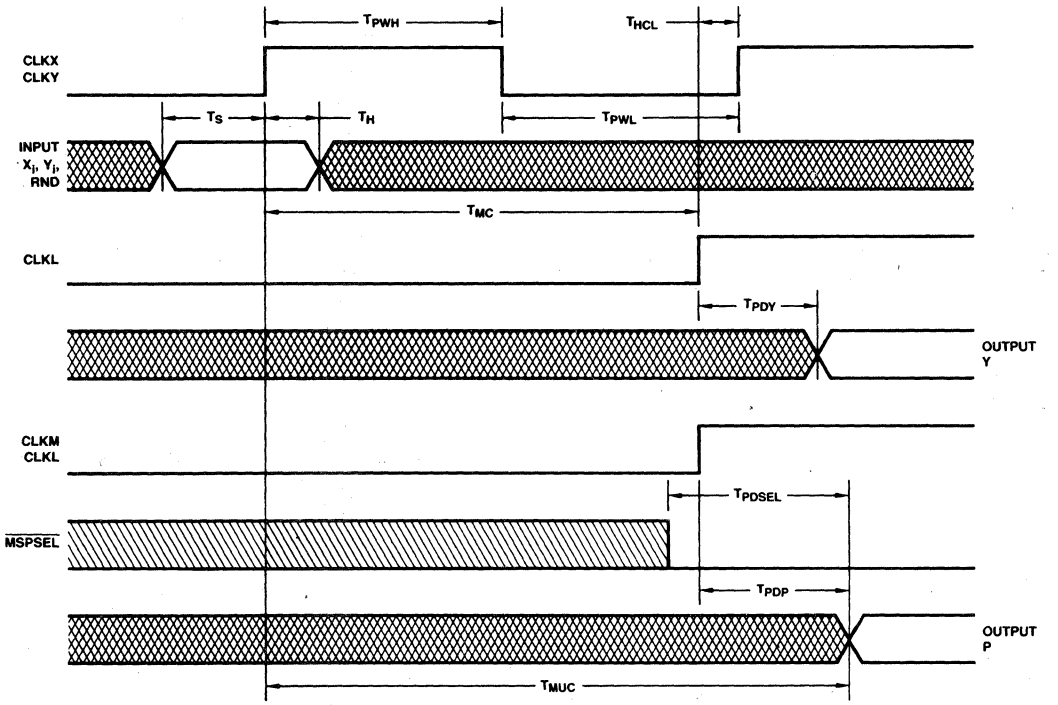
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

THREE-STATE TIMING DIAGRAM



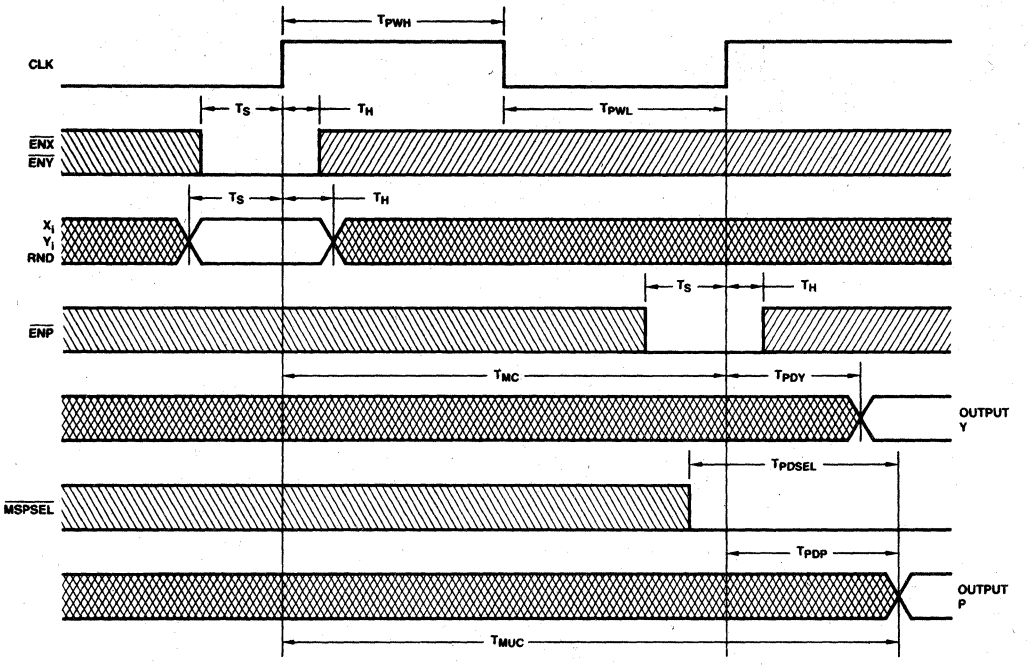
WFR02730

TIMING DIAGRAM
Am29516/29516A/29L516



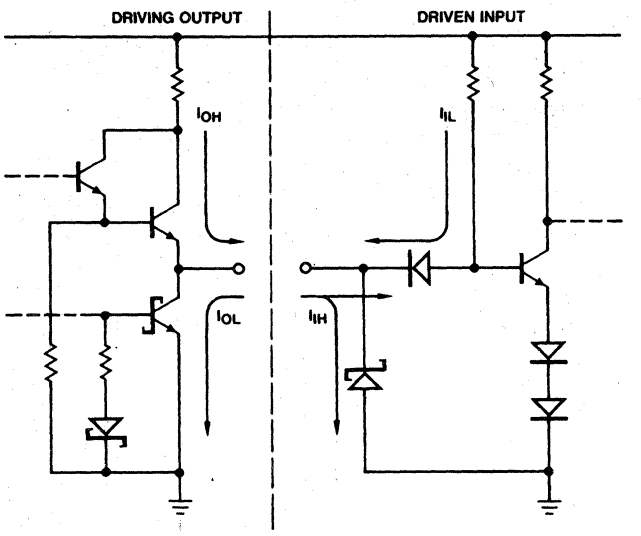
WFR02740

TIMING DIAGRAM
Am29517/29517A/29L517



WFR02750

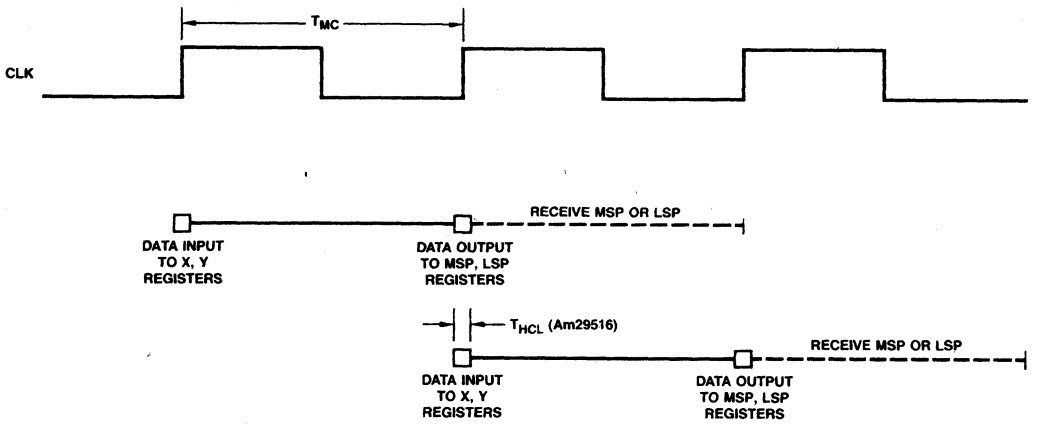
INPUT/OUPUT CURRENT INTERFACE CONDITIONS
(All Devices)



ICR00480

SIMPLIFIED TIMING DIAGRAM

TYPICAL APPLICATION



AFR01700

7

Am29520/Am29521

Multilevel Pipeline Registers

DISTINCTIVE CHARACTERISTICS

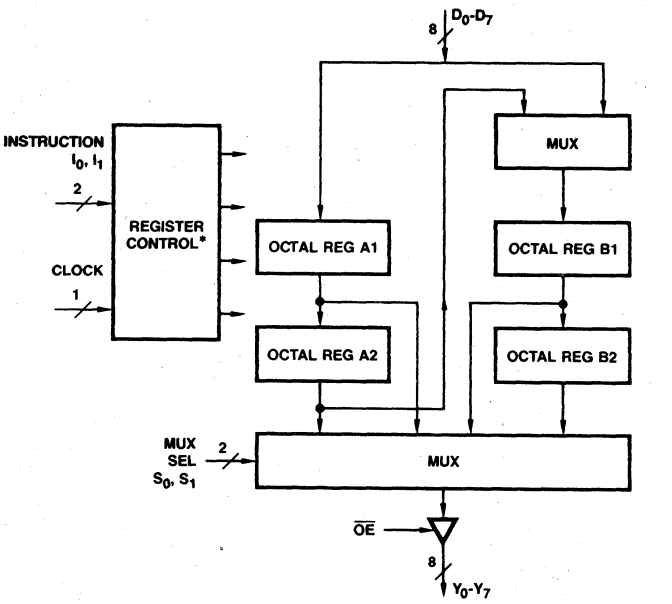
- Four 8-bit high speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- 24-pin 0.3″ package

GENERAL DESCRIPTION

The Am29520 and Am29521 each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level pipeline or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

The Am29520 and Am29521 differ only in the way data is loaded into and between the registers in dual 2-level operation. This difference is illustrated in Figure 1. In the Am29520 when data is entered into the first level (I – 2 or I – 1) the existing data in the first level is moved to the second level. In the Am29521 these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I = 3 is a HLD.

BLOCK DIAGRAM



BDR02270

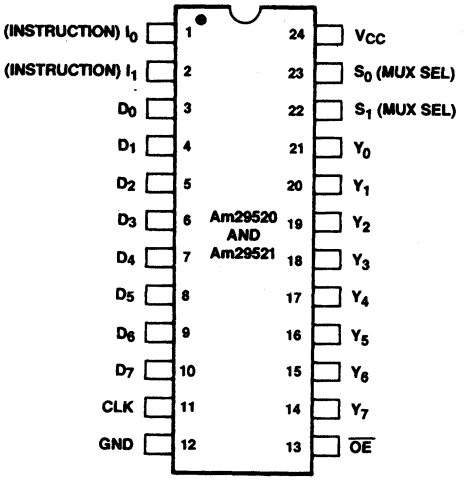
*Multilevel Pipeline Register

03569A

Refer to Page 13-1 for Essential Information on Military Devices

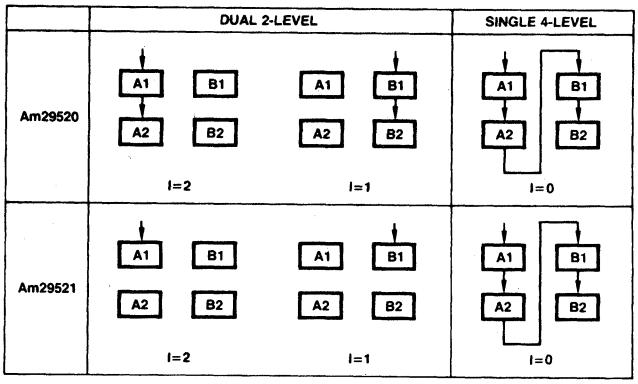
CONNECTION DIAGRAM
Top View

D-24-SLIM



CDR04470

Note: Pin 1 is marked for orientation



TB2

I = 3 HLD

Figure 1.

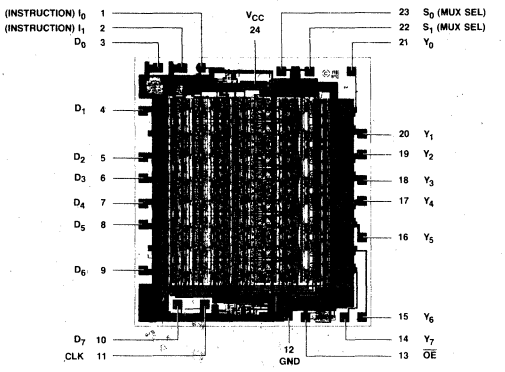
03569A

Refer to Page 13-1 for Essential Information on Military Devices

METALLIZATION AND PAD LAYOUT

CHIP TOPOGRAPHY

Am29520/21



DIE SIZE: 0.117" x 0.131"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29520/21 **P** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- **P** — Package
  - D– 24-pin SLIM
- **Am29520/21** — Device Type
  - Multilevel Pipeline Registers

Valid Combinations	
Am29520 Am29521	DC, DCB, DM, DMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
3-10	D_0-D_7	I	Register input port.
11	CLK	I	Clock input. Enter data into registers on LOW-to-HIGH transitions.
1, 2		I	Instruction inputs. See Figure 1 and Instruction Control Tables.
23, 22	S_0, S_1	I	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
13	$\overline{OE}$		Output enable for 3-state output port.
14-21	Y_0-Y_7	O	Register output port.

*DIP Configuration

APPLICATIONS

The IMOX™ Am29520 and Am29521 multilevel pipeline registers are specifically designed as a temporary address storing register for array processing and digital signal processing applications using the Am29500 Family.

In AP/DSP applications a single data address may be used a multiple number of times. The multilevel pipeline register allows saving addresses within its registers for use at a later time.

Below are a number of applications where the use of a multilevel pipeline register can be implemented.

CLOCK CONTROLLER, BYTE-WIDE DELAY LINE/SHIFT REGISTER

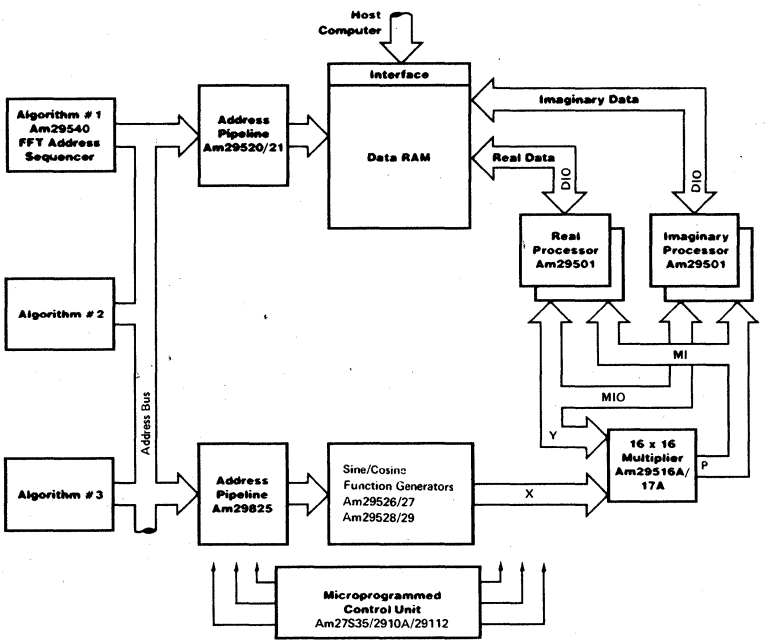
The Am29520/21 can be utilized as a byte-wide shift register capable of delaying a byte of data from one to four clock cycles. The number of delay cycles is controlled by the S_0, S_1 control inputs and can be changed by the user without interrupting the data flow.

ANALOG/DIGITAL BUFFER

In the example shown in Figure 2 the Am29520/21 acts as a 4-byte buffer between an A/D converter and a controller (or microprocessor). Four digitized samples are sequentially stored in the Am29520/21 from the A/D converter. This is accomplished by applying a READ control input to the clock input of the Am29520/21 as well as to the READ input of the A/D. Since I = 0, the data output from the A/D will be stored in the Am29520/21 as shown in Figure 3.

While the fifth sample is being acquired by the A/D, the controller will read all registers of the Am29520/21 by manipulating S_0, S_1. Note that the three-state output (controlled by OE) can be tied directly to a microprocessor bus and that the registers of the Am29520/21 can be easily memory mapped.

Am29500 PROCESSOR



BD002711

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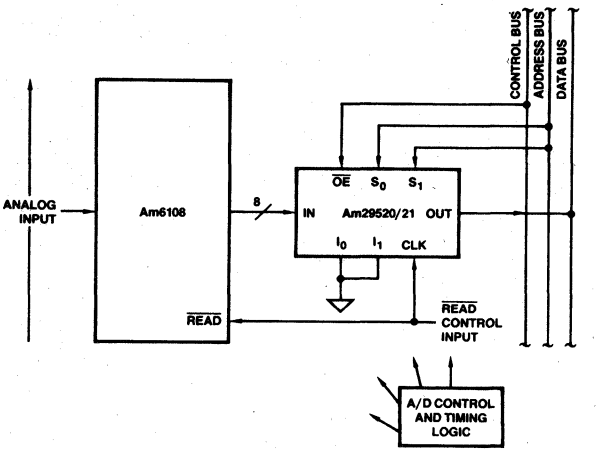
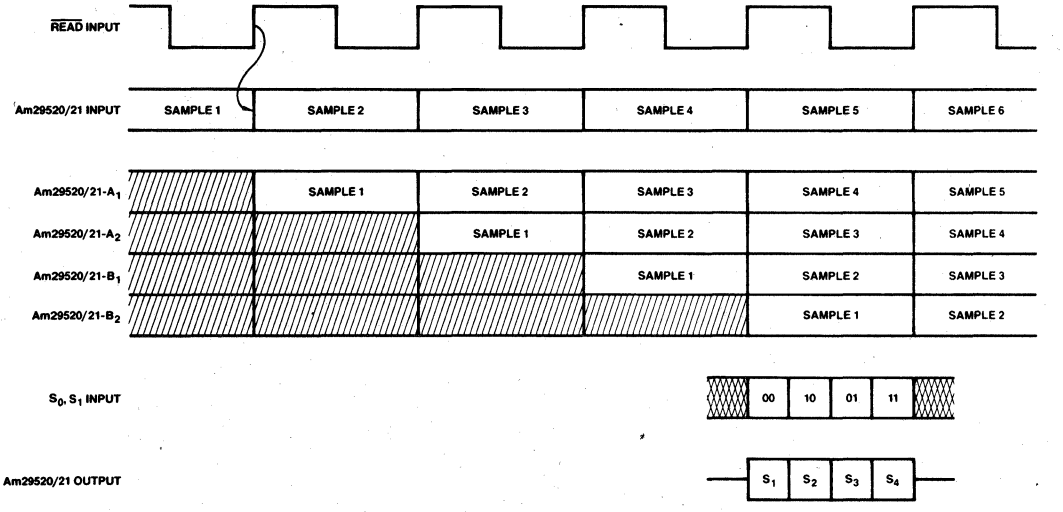
Refer to Page 13-1 for Essential Information on Military Devices

Figure 2. A/D Buffer



AFR01720

Figure 3. A/D Buffer Timing



AFR01710

The A/D will acquire four more samples before the Am29520/21 registers need to be read.

Note that the Am29520/21 can be simultaneously written and read. A two byte ping-pong memory is realizable by switching between I modes 1 and 2. While the A/D is writing registers B_1 and B_2, the microprocessor can be reading registers A_1 and A_2.

Also, note that the Am29520/21 is easily cascadable in width for applications involving 12-bit and 16-bit A/D converters.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... T_A = 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... T_C = −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

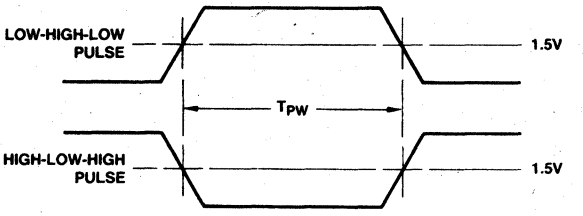
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5mA (COM'L)		2.4			Volts
			I_{OH} = −2.0mA (MIL)		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA				0.45	Volts
			I_{OL} = 20mA				0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		$\overline{OE}$			−2.0	mA
				Other Inputs			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 2.7V			50	μA
I_{OZL}				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−100	mA
I_{CC}	Power Supply Current (Note 4)	COM'L and MIL	T_A = 25°C			125		mA
		COM'L Only V_{CC} = MAX	T_A = 0 to +70°C				185	
			T_A = +70°C				155	
		MIL Only V_{CC} = MAX	T_C = −55 to +125°C				200	
			T_C = +125°C				150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs LOW.

PULSE WIDTH



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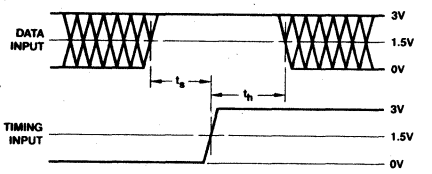
SET-UP AND HOLD TIME



WFR02970

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters		Description	Test Conditions	Min	Typ	Max	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	t_{PLH}	Clock to Data Output	$R_L = 280\Omega$ $C_L = 50pF$		12	18		21		24	ns
	t_{PHL}				12	20		22		24	
t_{PDSEL}	t_{PLH}	S_0, S_1 to Data Output			12	18		20		22	ns
	t_{PHL}				12	18		20		22	
t_S		Input Data to Clock		10			10		10		ns
t_H				3			3		3		
t_S		Instruction (Register Enable) to Clock		10			10		10		ns
t_H				3			3		3		
t_{PHZ}		$\overline{OE}$ to Output	$C_L = 5pF$		5	11		13		14	ns
t_{PLZ}		$\overline{OE}$ to Output	$C_L = 5pF$		6	13		15		16	ns
t_{PZH}		$\overline{OE}$ to Output	$R_L = 280\Omega$ $C_L = 50pF$		12	18		20		22	ns
t_{PZL}		$\overline{OE}$ to Output			13	20		21		22	ns
t_{PWH}		Clock Pulse Width HIGH		10			10		10		ns
t_{PWL}		Clock Pulse Width LOW		10			10		10		ns

Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in Section 13 of this data book.

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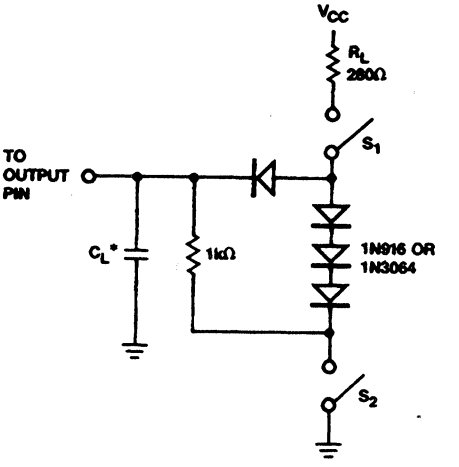
SWITCHING TEST CIRCUIT

SWITCHING TEST CIRCUITS FOR DELAY MEASUREMENTS



TCR01310

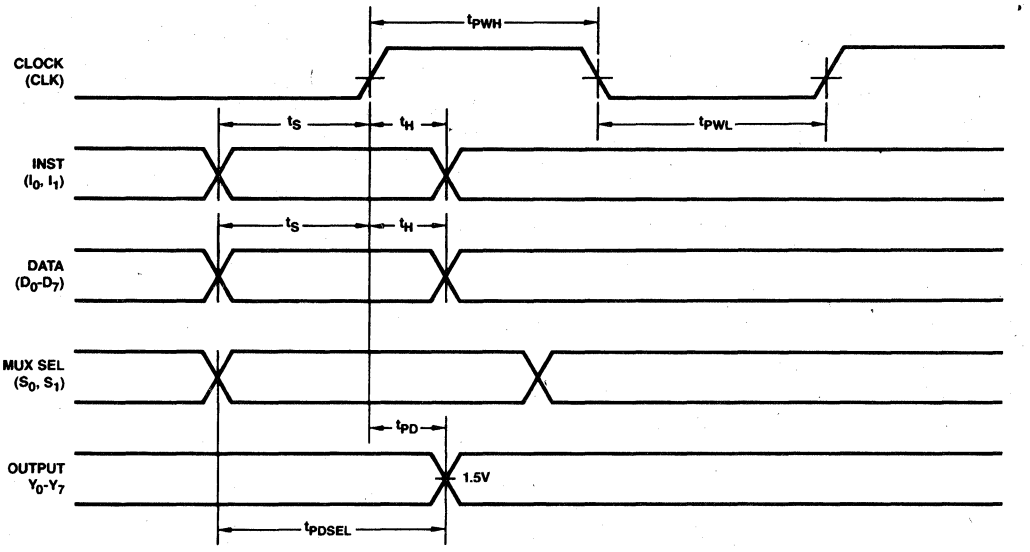
*C_L = 50pF for all t_{PD}, t_{ZH} and t_{ZL}
C_L = 5pF for t_{HZ} and t_{LZ}

TEST WAVEFORMS

Test	Output Waveform – Measurement Level	
All t_{PD}s	V_{OH} / V_{OL}, 1.5V	S_1 Closed S_2 Closed
t_{PHZ}	V_{OH}, 0.5V, ≈ 1.5V	S_1 Closed S_2 Closed
t_{PLZ}	≈ 1.5V, 0.5V, V_{OL}	S_1 Closed S_2 Closed
t_{PZH}	V_{OH}, 1.5V, 0.0V	S_1 Open S_2 Closed
t_{PZL}	V_{CC}, 1.5V, V_{OL}	S_1 Closed S_2 Open

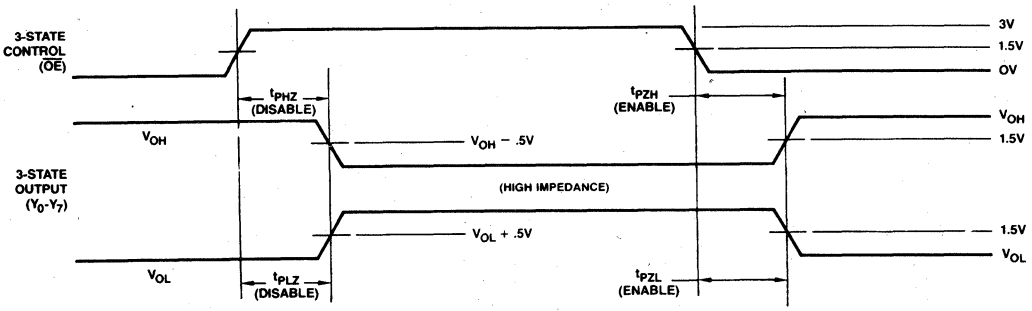
WFR02920

Am29520/21
TIMING DIAGRAM



WFR02930

Am29520/21
THREE-STATE TIMING



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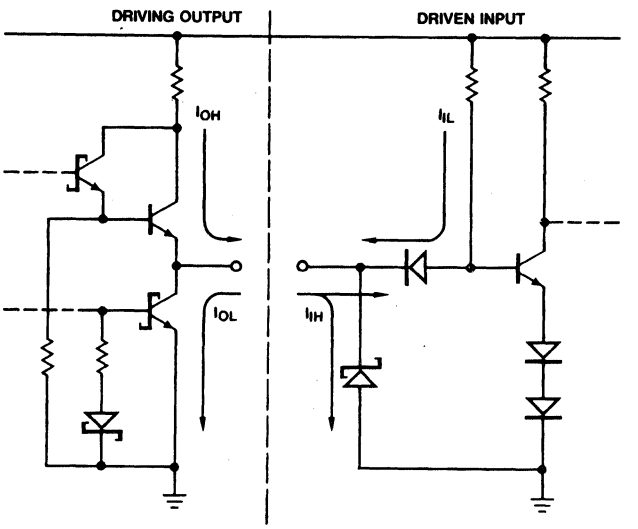
Refer to Page 13-1 for Essential Information on Military Devices

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00510

RELATED PRODUCTS

Part No.	Description
Am29540	FFT Address Sequencer
Am29116	16-bit Bipolar Microprocessor
Am2925	System Clock Generator and Driver
Am29517	16 x 16-bit High Speed Multiplier
Am29510	16 x 16-bit Multiplier Accumulator
Am6108	8-bit Microprocessor Compatible A/D Converter
Am9128-70	2K x 8 Static RAM
Am21L47-55	4K x 1 Static RAM

Am29526 • Am29527
Am29528 • Am29529

High Speed Sine, Cosine Generators

DISTINCTIVE CHARACTERISTICS

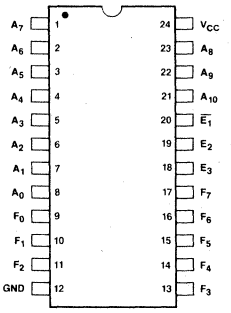
- Provides values for sine/cosine functions in $\pi/2048$ increments
- Outputs are 16-bit two's complement fractions
- Fast generation time of 50ns max Com'l
- S/LS compatible
- Three-state outputs
- IMOX™ processing

RELATED PRODUCTS

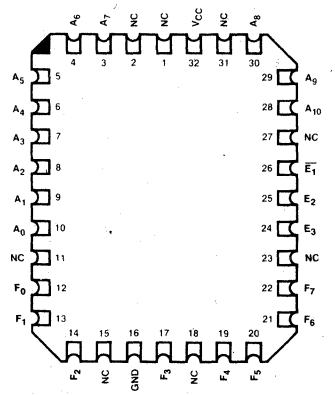
Part No.	Description
Am29516/17	16 x 16-Bit High Speed Multipliers
Am29510	16 x 16-Bit Multiply Accumulator
Am29540	FFT Address Sequencer
Am29825	High Performance 8-Bit Register

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™ ABL-006



ABL-007

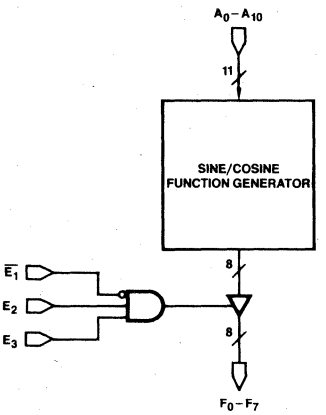
FUNCTIONAL DESCRIPTION

The Am29526/27 and Am29528/29 provide high speed generation of sine and cosine functions over the range $0 \leq \theta < \pi$ in increments of $\pi/2048$. θ is determined by an 11-bit input word. Each device provides an 8-bit output and two are used to give the full 16-bit value. The Am29526 and Am29527 generate the MS and LS bytes respectively for the sine function. Similarly, the Am29528 and Am29529 generate the cosine functions.

The outputs are fractional two's complement numbers with the radix point located immediately to the right of the sign bit (in between the bits weighted -2^0 and 2^{-1}). As this format does not allow for the representation of $+1$ the functions generated are $-\sin\theta$ and $-\cos\theta$. In this way the output values are restricted to the range $-1 \leq f(\theta) < +1$ which is representable. The outputs are three-state with one active Low enable and two active High enable.

While providing general purpose sine and cosine function capability, the Am29526/27/28/29 satisfy the requirements of the Am29540 FFT Address Sequencer.

BLOCK DIAGRAM



ABL-008

Am29526/27/28/29
ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	MIL	−15	−40	−90	mA
			COM'L	−20	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			115	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_{CS} = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = +25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

DEFINITION OF FUNCTIONAL TERMS

A_{10}–A_0 **Data Input Values**
Input, θ, corresponding to θ = 0 (000) to 2047π/2048 (3FF). A_{10} is MSB.

$\overline{E}_1$, E_2, E_3 **Output Enables**
When $\overline{E}_1$ is Low and E_2 and E_3 are High, the outputs F_0–F_7 are enabled. Otherwise the outputs are in the high impedance state or off.

F_7–F_0 **Data Output Values**
The outputs corresponding to −sinθ or −cosθ. F_7 is MSB.

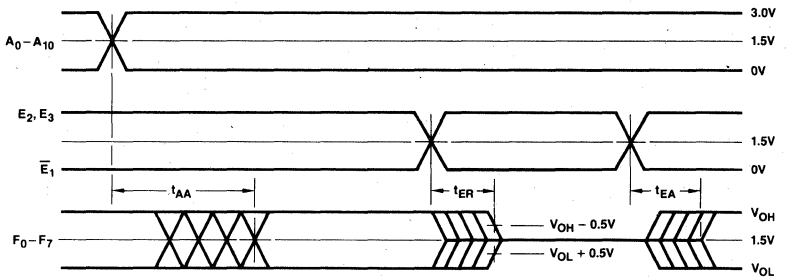
Refer to Page 13-1 for Essential Information on Military Devices

Am29526/27/28/29
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		$T_A = +25°C$, $V_{CC} = 5V$ Typ	COM'L: $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ Max	MIL: $T_C = -55$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ Max	Units	Test Conditions
t_{PLH}	Sin/Cos Generation Time A_i to F_i		30	50	65	ns	$R_L = 600\Omega$, $C_L = 30pF$ (Notes 1 and 2)
t_{PHL}			30	50	65	ns	
t_{PHZ}	$\overline{E}_1, E_2, E_3$ Disable Time	High to Z	10	25	30	ns	
t_{PLZ}		Low to Z	10	25	30	ns	
t_{PZH}	$\overline{E}_1, E_2, E_3$ Enable Time	Z to High	10	25	30	ns	
t_{PZL}		Z to Low	10	25	30	ns	

Notes: 1. t_{PLH} and t_{PHL} are tested with switch S_1 closed and $C_L = 30pF$.
2. For three-state outputs, the disables time is tested with $C_L = 30pF$ to the 1.5V level; S_1 is open for Z to High test and closed for Z to Low test. The enable time is tested with $C_L = 5pF$. High to Z tests are made to an output voltage to $V_{OH} - 0.5V$ with S_1 open; Low to Z tests are made to the $V_{OL} - 0.5V$ level with S_1 closed.

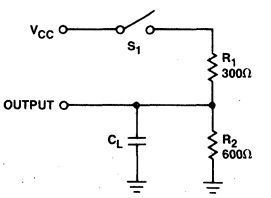
SWITCHING WAVEFORMS



Note: Level on output while chip is disabled is determined externally.

ABL-009

AC TEST LOAD



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Refer to Page 13-1 for Essential Information on Military Devices

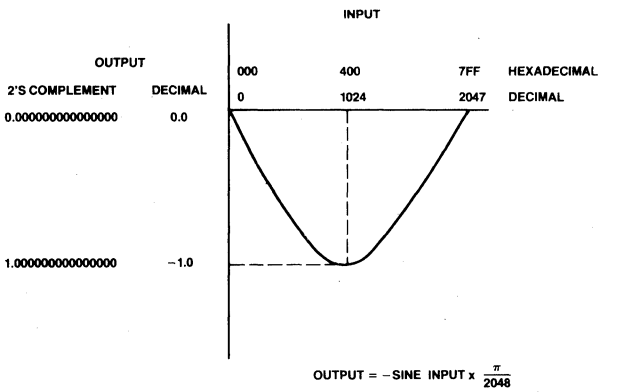
TABLE 1. $-COS(\theta)$ TABLE

Decimal Input	Actual Hexadecimal Input	Angle in Radians	Decimal Value of $-Cos(\theta)$	Hex Value of $-Cos(\theta)$	Am29526 MS Device	Am29527 LS Device
0	0	0	−1.000000	1000	10	00
512	200	$\pi/4$	−0.707107	A57E	A5	7E
1024	400	$\pi/2$	0.000000	0000	00	00
1536	600	$3\pi/4$	+0.707107	5A82	5A	82
2047	7FF	$2047\pi/2048$	+0.999999	7FFF	7F	FF

TABLE 2. $-SIN(\theta)$ TABLE

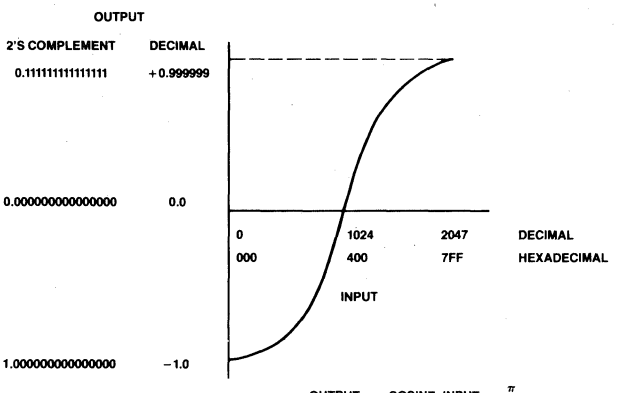
Decimal Input	Actual Hexadecimal Input	Angle in Radians	Decimal Value of $-Sin(\theta)$	Hex Value of $-Sin(\theta)$	Am29528 MS Device	Am29529 LS Device
0	000	0	0	0000	00	00
512	200	$\pi/4$	−0.707107	A57E	A5	7E
1024	400	$\pi/2$	−1.00000	8000	80	00
1536	600	$3\pi/4$	−0.707107	A57E	A5	7E
2047	7FF	$2047\pi/2048$	−0.001534	FFCE	FF	CE

Figure 1. The Minus Sine Function



ABL-011

Figure 2. The Minus Cosine Function



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Refer to Page 13-1 for Essential Information on Military Devices

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 3)	Screening Level (Note 2)
AM29526PC	P-24-1AA	C	C-1
AM29527PC	P-24-1AA	C	C-1
AM29528PC	P-24-1AA	C	C-1
AM29529PC	P-24-1AA	C	C-1
AM29526PC-B	P-24-1AA	C	B-1
AM29527PC-B	P-24-1AA	C	B-1
AM29528PC-B	P-24-1AA	C	B-1
AM29529PC-B	P-24-1AA	C	B-1
AM29526DC	D-24-1AA	C	C-1
AM29527DC	D-24-1AA	C	C-1
AM29528DC	D-24-1AA	C	C-1
AM29529DC	D-24-1AA	C	C-1
AM29526DC-B	D-24-1AA	C	B-1
AM29527DC-B	D-24-1AA	C	B-1
AM29528DC-B	D-24-1AA	C	B-1
AM29529DC-B	D-24-1AA	C	B-1
AM29526DM	D-24-1AA	M	C-3
AM29527DM	D-24-1AA	M	C-3
AM29528DM	D-24-1AA	M	C-3
AM29529DM	D-24-1AA	M	C-3
AM29526DM-B	D-24-1AA	M	B-3
AM29527DM-B	D-24-1AA	M	B-3
AM29528DM-B	D-24-1AA	M	B-3
AM29529DM-B	D-24-1AA	M	B-3
AM29526LC	L-32-2	C	C-1
AM29527LC	L-32-2	C	C-1
AM29528LC	L-32-2	C	C-1
AM29529LC	L-32-2	C	C-1
AM29526LM	L-32-2	M	C-3
AM29527LM	L-32-2	M	C-3
AM29528LM	L-32-2	M	C-3
AM29529LM	L-32-2	M	C-3
AM29526LM-B	L-32-2	M	B-3
AM29527LM-B	L-32-2	M	B-3
AM29528LM-B	L-32-2	M	B-3
AM29529LM-B	L-32-2	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.

2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

3. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.

Refer to Page 13-1 for Essential Information on Military Devices

Am29540

Programmable FFT Address Sequencer

DISTINCTIVE CHARACTERISTICS

- Generates data and coefficient addresses
- Programmable transform length 2 to 65,536 points
- Radix-2 or Radix-4
- In-place or non-in-place transformation
- Decimation in frequency (DIF) or decimation in time (DIT) FFT algorithms supported
- 40-pin DIP package, 5 volt single supply

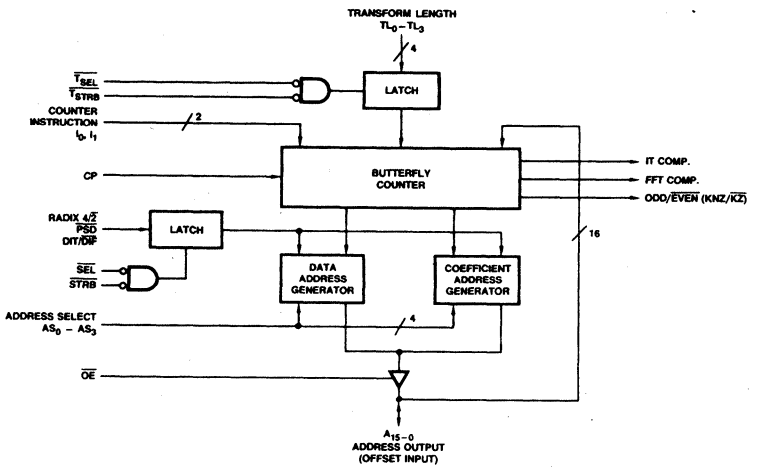
GENERAL DESCRIPTION

The Am29540 Fast Fourier Transform Address Sequencer generates all the data (RAM) and coefficient (ROM) addresses necessary to perform the repetitive butterfly operations of the FFT. Decimation in time and decimation in frequency algorithms are supported (control DIT/$\overline{\text{DIF}}$) in radix-2 or radix-4 (RADIX 4/$\overline{2}$). A radix-2 real valued input (RVI) transform is also supported. For radix-2 operation the transform length is programmable in powers of 2 from 2 to 65,536 points. In radix-4 the range is 4 to 65,536 in powers of 4.

Address sequences can be selected to be compatible with data which may or may not have been pre-scrambled ('bit-reversed'). If the data has been pre-scrambled the control $\overline{\text{PSD}}$ must be LOW to select the correct sequence. If the data is not pre-scrambled ($\overline{\text{PSD}}$ HIGH) and an in-place transform is performed, the output data will necessarily be in bit-reversed order. If this is not desirable, alternate addresses are available for a non-in-place, non-bit-reversing algorithm.

The butterfly counter operates on the positive clock edge and responds to four instructions. COUNT causes the counter to increment to the next butterfly. RESET causes the counter to initialize for the specified transform length. RESET/LOAD causes the counter to initialize and a data address offset to be loaded into the part via the bi-directional 3-state ADDRESS port. This offset is effectively OR-ed onto the higher significant bits of the address which are unused for the selected transform length. A HOLD instruction is also provided. Three status lines are provided. ODD/$\overline{\text{EVEN}}$ (KNZ/$\overline{\text{KZ}}$) controls the alternation of read and write memories for non-in-place transforms and determines the butterfly structure in the RVI transform. The flag has the function KNZ/$\overline{\text{KZ}}$ when RVI data addresses are selected (AS = 12 to 15). Iteration complete (IT COMP) flags the bottom of a "column" of butterflies and is used in conjunction with block floating point schemes. FFT COMP identifies the last butterfly of the transform.

BLOCK DIAGRAM



BDR02240

FFT Address Sequencer

03567C

Refer to Page 13-1 for Essential Information on Military Devices

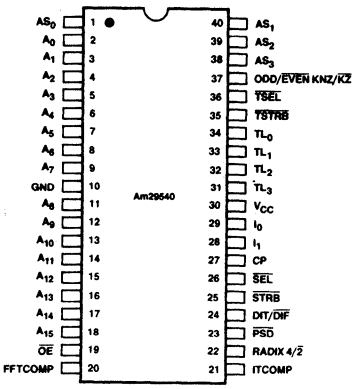
RELATED PRODUCTS

Part No.	Description
Am29501	Multi-port pipelined processor (Byte-slice™)
Am29516/17	16 x 16 parallel multiplier
Am29520/21	Multilevel pipeline register
Am29526/ 27/28/29	High speed sine/cosine generators
Am29825	High performance 8-bit register

Byte-Slice is a trademark of Advanced Micro Devices, Inc.

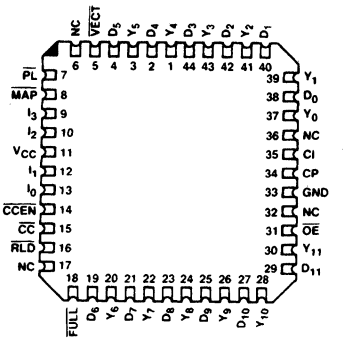
CONNECTION DIAGRAM
Top View

D-40-1



CDR04360

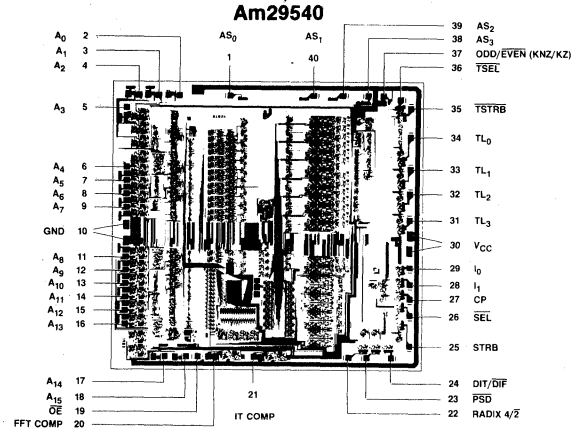
L-44-1



CD004690

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT
Am29540



DIE SIZE: 254 x 273 MILS

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29540 P C B

- B — Screening Option
  - Blank – Standard Processing
  - B – Burn-in
- C — Temperature (see Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- P — Package
  - D– 40 pin CERDIP
  - L – 44 pin Leadless Chip Carrier
  - X – Dice
- Am29540 — Device Type
  - Programmable FFT Address Sequencer

Valid Combinations	
Am29540	DC, DCB, DMB LC, LMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
31-34	TL_3, TL_2 TL_1, TL_0	I	Transform length control determines the number of points to be transformed. (See Figure 1.)
36, 35	$\overline{TSEL}$, $\overline{TSTRB}$	I	Transform length latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{TSEL}$ and $\overline{TSTRB}$ are LOW.
29, 28	I_0, I_1	I	Counter Instruction inputs determine one of four available butterfly counter instructions: Hold, Reset, Reset/Load and Count. (See Figure 2.)
27	CP	I	Butterfly counter clock (positive edge active).
22	Radix 4/$\overline{2}$	I	The Radix control determines whether addresses will be generated for Radix-4 (HIGH) for Radix-2 (LOW) transforms.
23	$\overline{PSD}$	I	The Pre-Scrambled Data, $\overline{PSD}$, input is used to select an appropriate transform for input data which has previously been digit reversed. Refer to individual transform flow charts for other cases.
24	DIT/$\overline{DIF}$	I	Control input for selection of the Decimation in Frequency algorithm (LOW) or Decimation In Time algorithm (HIGH).
26, 25	$\overline{SEL}$, $\overline{STRB}$	I	Transform type (Radix 4/$\overline{2}$, PSD, DIF/$\overline{T}$) latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{SEL}$ and $\overline{STRB}$ are LOW.
1, 38-40	AS_3, AS_2, AS_1, AS_0	I	Address Select control determines address selection. (See Figure 3.)
19	$\overline{OE}$	I	Three-state output enable. The 3-state output is controlled solely by $\overline{OE}$. The output does not automatically become high impedance during the Reset/Load instruction.
2-9, 11-18	A_{15}-A_0 Address Output (offset input)	I/O	Bidirectional 16-bit port to output selected addresses or to input an address offset.
37	ODD/$\overline{EVEN}$, (KNZ/$\overline{KZ}$)	O	For address select 0 to 11 the ODD/$\overline{EVEN}$ output controls the alternation of separate read and write memories for non-in-place transforms. For Address select 12 to 15 KNZ/$\overline{KZ}$ = (LOW) indicates that the rotational constant to be used in the RVI transform is W^0 and that an alternative butterfly must be implemented.
20	FFT COMP	O	FFT Complete = HIGH identifies the last butterfly (or end) of the transform. (See Figure 4.)
21	IT COMP	O	Iteration Complete = HIGH flags the bottom of a 'column' of butterflies. (See Figure 4.)

*DIP Configuration

DETAILED DESCRIPTION

The Am29540 can be pictured as consisting of sixteen 16-bit counters that output on a bidirectional three-state address port, A_{15}–A_0. These sixteen counters generate the data and coefficient addresses required to support the various FFT algorithms.

Decimation-In-Time (DIT) and Decimation-In-Frequency (DIF) algorithms are supported in Radix-2 and Radix-4. Two inputs, DIT/$\overline{DIF}$ and Radix4/$\overline{2}$, control these two parameters without encoding. A third microcode bit, $\overline{PSD}$, enables input data to be bit reversed. $\overline{PSD}$ must be LOW for all transforms with prescrambled (bit reversed) input data. For all in-place transforms with normally-ordered input data, $\overline{PSD}$ must be HIGH. For all non-in-place DIT transforms, $\overline{PSD}$ must be LOW, and for all non-in-place DIF transforms, $\overline{PSD}$ must be HIGH. These three microcode bits can be latched. $\overline{STRB}$ and $\overline{SEL}$ are the latch enables. They are ANDed so that the latch is transparent when both are LOW.

The transform length is latched via the TL_3–TL_0 inputs. $\overline{TSTRB}$ and $\overline{TSEL}$ are the latch enables. They are ANDed so that the latch is transparent when both are LOW. For Radix-4 operations, the transform length is programmable in powers of 4, from 4 to 65,536 points. In Radix-2, the range is 2 to 65,536 points in powers of 2. A Radix-2 Real Valued Input (RVI) algorithm is also supported for transform lengths from 2 to 65,536, in powers of 2. Codes to program the transform length are contained in Figure 1.

Two microcode bits, I_1–I_0, control the operation of the Am29540. The four possible instructions are:

1. HOLD. All counters hold their last values. This instruction is used at any time the counter values must remain constant and could be used during initialization of the part.
2. RESET. All counters are reset to the start of the transform. All unused address lines are set to zero. Control bits DIT/$\overline{DIF}$, Radix 4/$\overline{2}$ and $\overline{PSD}$ are unaffected.
3. RESET/LOAD. All counters are reset to the start of the transform. All unused address lines are set to the current value of the address port. This allows loading of an offset address via the bidirectional address port. This offset is effectively ORed onto the higher significant bits of the address which are unused for the transform length. Only data address counters are affected. Coefficient address counters are not affected.
4. COUNT. All counters are incremented to their next valid address.

Codes for all four instructions are contained in Figure 2.

Four address select controls, AS_3–AS_0, choose which of the sixteen counter outputs are available at the address port. Typically, these bits would come from the microcode. Data addresses are right-justified, A_{15} being the MSB. Coefficient addresses are left-justified: A_{15} is the MSB for Radix-4 operations; A_{14} is the MSB for Radix-2 operations. Codes for AS_3–AS_0 are contained in Figure 3.

Two output flags, ITCOMP and FFTCOMP, indicate counter status. When the bottom of a column of butterflies is reached, Iteration Complete (ITCOMP) goes HIGH. When the last butterfly (or end) of the transform is reached, FFT Complete (FFTCOMP) also goes HIGH. These two flags would typically be condition code inputs to the microprogram sequencer.

A third flag is used to indicate end of column for non-in-place transforms or one of two butterfly types for RVI transforms. For column indication, the flag is called ODD/$\overline{EVEN}$ and can be used to switch memory banks. The flag will be a HIGH for the last column of butterflies. In the RVI transform the flag is called KNZ/$\overline{KZ}$. The equations for the butterfly when the rotational constant is W^0 are different from when the rotational constant is not W^0. When KNZ/$\overline{KZ}$ is LOW, it indicates that the rotational constant to be used is W^0 and that the alternative butterfly equations must be executed. Typically there are two microcode segments. The KNZ/$\overline{KZ}$ flag would be a condition code input to the sequencer to select one of the two segments.

TL_3	TL_2	TL_1	TL_0	Transform Length		
				Radix-2	Radix-4	RVI
L	L	L	L	2	4	4
L	L	L	H	4	4	8
L	L	H	L	8	16	16
L	L	H	H	16	16	32
L	H	L	L	32	64	64
L	H	L	H	64	64	128
L	H	H	L	128	256	256
L	H	H	H	256	256	512
H	L	L	L	512	1024	1024
H	L	L	H	1024	1024	2048
H	L	H	L	2048	4096	4096
H	L	H	H	4096	4096	8192
H	H	L	L	8192	16384	16384
H	H	L	H	16384	16384	32768
H	H	H	L	32768	65536	65536
H	H	H	H	65536	65536	Not Used

Figure 1. Transform Length Control

I_1	I_0	Counter Function
L	L	Hold
L	H	Reset. Reset counter to start of transform with unused address outputs set to 0.
H	L	Reset/Load. Reset counter to start of transform with unused address outputs set to the current value of the address bus.
H	H	Count. Increment butterfly counter.

Figure 2. Counter Instruction Control

FFT Type	AS_3	AS_2
Complex Input	L X	X L
Real Valued Input (RVI)	H	H

Figure 2a. Offset Address Control

AS =	AS_3	AS_2	AS_1	AS_0	Description	Usage
0	L	L	L	L	Data Address 1	Radix 2/4
1	L	L	L	H	Data Address 2	Radix 2/4
2	L	L	H	L	Data Address 3	Radix 4
3	L	L	H	H	Data Address 4	Radix 4
4	L	H	L	L	Alt. Data Address 1	Radix 2/4
5	L	H	L	H	Alt. Data Address 2	Radix 2/4
6	L	H	H	L	Alt. Data Address 3	Radix 4
7	L	H	H	H	Alt. Data Address 4	Radix 4
8	H	L	L	L	Const Address 1	Radix 2/4, Shading
9	H	L	L	H	Const Address 2	Radix 4
10	H	L	H	L	Const Address 3	Radix 4
11	H	L	H	H	$\overline{\text{Const Address 1}}$	Shading
12	H	H	L	L	RVI Data Address 1	RVI
13	H	H	L	H	RVI Data Address 2	RVI
14	H	H	H	L	RVI Data Address 3	RVI
15	H	H	H	H	RVI Data Address 4	RVI

Figure 3. Address Select Control

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0°C to +70°C
Chip Carriers ..... T_C = 0°C to 85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... T_C = −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2.6mA, COM'L	2.4			Volts
			I_{OH} = −mA, MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V (See Note 5)				100	μA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_{IN} = 2.7V			20	μA
I_{OZL}			V_{IN} = 0.4V			0.4	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	COM'L and MIL	T_A=25°C		320	450	mA
		COM'L Only	T_A = 0 to +70°C (Note 6)			450	
		V_{CC} = MAX	T_A = +70°C (Note 6)			400	
		MIL Only	T_C = −55 to +125°C			470	
		V_{CC} = MAX	T_C = +125°C			350	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ LOW and all inputs LOW.
5. It is limited to 5.5V because A_0 to A_{15} inputs also connect to output transistors.
6. Chip Carriers: T_C = 0 to 85°C.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (T_A = 25°C, V_{CC} = 5.0V)

Parameters		Description		Test Conditions	Min	Typ	Max	Units
1	t_{PD}	CP to A_{0-15}(AS = 0)		C_L = 50pF See Test Circuits		21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 1)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 2)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 3)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 4)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 5)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 6)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 7)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 8)				25	32	ns
1	t_{PD}	CP to A_{0-15}(AS = 9)				25	32	ns
1	t_{PD}	CP to A_{0-15}(AS = 10)				30	40	ns
1	t_{PD}	CP to A_{0-15}(AS = 11)				21	40	ns
1	t_{PD}	CP to A_{0-15}(AS = 12)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 13)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 14)				21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 15)				21	30	ns
2	t_{PD}	Address Select to A_{0-15}	With A_2 LOW			30	40	ns
			With A_2 Active			45	60	ns
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time				20	30	ns
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time				20	35	ns
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time				18	30	ns
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time				16	25	ns
7	t_{PD}	CP to IT COMP				20	30	ns
8	t_{PD}	CP to FFT COMP				20	30	ns
9	t_{PD}	CP to ODD/$\overline{EVEN}$/ (KNZ/$\overline{KZ}$)				30	40	ns
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/ (KNZ/$\overline{KZ}$)				20	30	ns
11	t_S	Offset Address Input A_{0-15} to CP Set-up Time			10	4		ns
12	t_H	Offset Address Input A_{0-15} to CP Hold Time			0	−1		ns
13	t_S	Counter Instruction to CP Set-up Time			20	11		ns
14	t_H	Counter Instruction to CP Hold Time			0	0		ns
15	t_S	Transform Length Select to CP Set-up Time			40	25		ns
16	t_H	Transform Length Select to CP Hold Time			0	0		ns
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Set-up Time			8	4		ns
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time			5	3		ns
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Set-up Time			15	10		ns
20	t_H	$\overline{TSEL}$ to $\overline{TSTRB}$↑ Hold Time			15	10		ns
21	t_S	RADIX 4/$\overline{2}$ to CP Set-up Time			25	16		ns
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time			0	0		ns
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Set-up Time			8	5		ns
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time			0	0		ns
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑ Set-up Time			15	10		ns
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑ Hold Time			15	10		ns
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Set-up Time			45	30		ns
28	t_{PWSL}	Minimum Strobe Pulse Width LOW			15	10		ns
29	t_{PWH}	CP Pulse Width HIGH			15	10		ns
30	t_{PWL}	CP Pulse Width LOW			15	10		ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

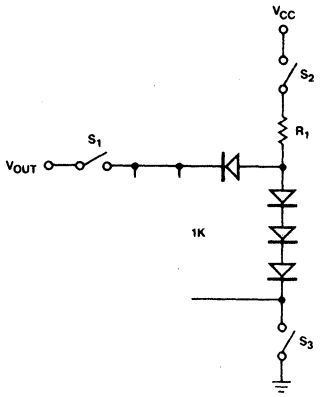
Parameters		Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
1	t_{PD}	CP to A_{0-15}(AS = 0)	C_L = 50pF See Test Circuits		35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 1)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 2)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 3)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 4)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 5)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 6)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 7)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 8)			42		50	ns
1	t_{PD}	CP to A_{0-15}(AS = 9)			42		50	ns
1	t_{PD}	CP to A_{0-15}(AS = 10)			53		60	ns
1	t_{PD}	CP to A_{0-15}(AS = 11)			53		60	ns
1	t_{PD}	CP to A_{0-15}(AS = 12)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 13)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 14)			35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 15)			35		40	ns
2	t_{PD}	Address Select to A_{0-15} With A_2 LOW			45		50	ns
		Address Select to A_{0-15} With A_2 Active			65		70	ns
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time			32		35	ns
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time			40		45	ns
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time			35		40	ns
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time			30		35	ns
7	t_{PD}	CP to IT COMP			40		50	ns
8	t_{PD}	CP to FFT COMP			40		50	ns
9	t_{PD}	CP to ODD/$\overline{EVEN}$/(KNZ/$\overline{KZ}$)			53		60	ns
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/(KNZ/$\overline{KZ}$)			38		45	ns
11	t_S	Offset Address Input A_{0-15} to CP Setup Time		11		12		ns
12	t_H	Offset Address Input A_{0-15} to CP Hold Time		1		2		ns
13	t_S	Counter Instruction to CP Setup Time		22		25		ns
14	t_H	Counter Instruction to CP Hold Time		0		0		ns
15	t_S	Transform Length Select to CP Setup Time		45		50		ns
16	t_H	Transform Length Select to CP Hold Time		0		0		ns
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Setup Time		9		10		ns
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time		7		8		ns
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Setup Time		18		20		ns
20	t_H	TSEL to$\overline{TSTRB}$ ↑ Hold Time		18		20		ns
21	t_S	RADIX 4/$\overline{2}$ to CP Setup Time		28		30		ns
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time		0		0		ns
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Setup Time		9		10		ns
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time		1		2		ns
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑ Setup Time		18		20		ns
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑ Hold Time		18		20		ns
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Setup Time		50		55		ns
28	t_{PWSL}	Minimum Strobe Pulse Width LOW		18		20		ns
29	t_{PWH}	CP Pulse Width HIGH		18		20		ns
30	t_{PWL}	CP Pulse Width LOW		18		20		ns

03567C

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

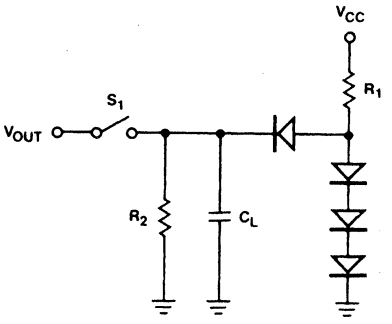
A. THREE-STATE OUTPUTS



TCR01230

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TCR01240

$$R_2 = \frac{2.4V}{I_{OH}} \qquad R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

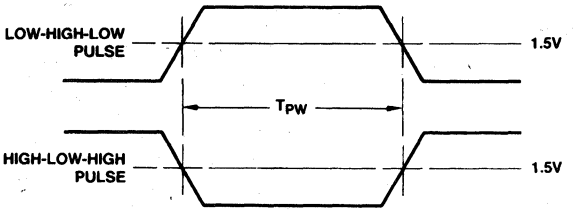
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

SWITCHING TEST WAVEFORMS

Test	Output Waveform – Measurement Level
All t_{PD}s	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	V_{OH}, 0.5V, 0.0V
t_{PLZ}	3V, 0.5V, V_{OL}
t_{PZH}	V_{OH}, 1.5V, 0.0V
t_{PZL}	3V, 1.5V, V_{OL}

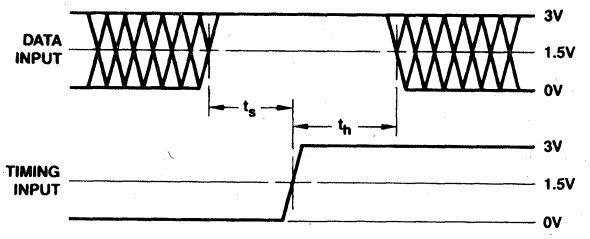
WFR02681

PULSE WIDTH



WFR02850

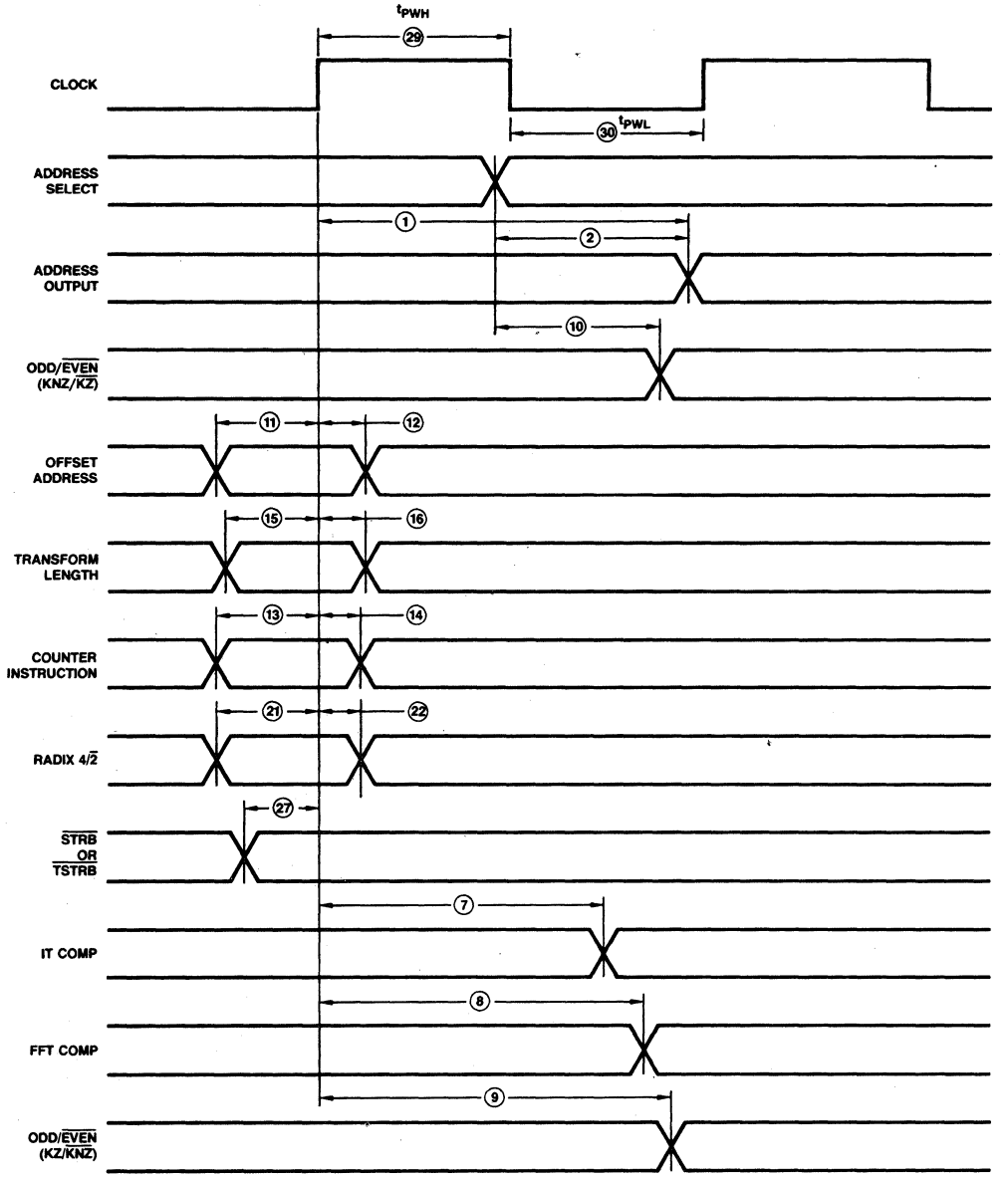
SET-UP AND HOLD TIME



WFR02970

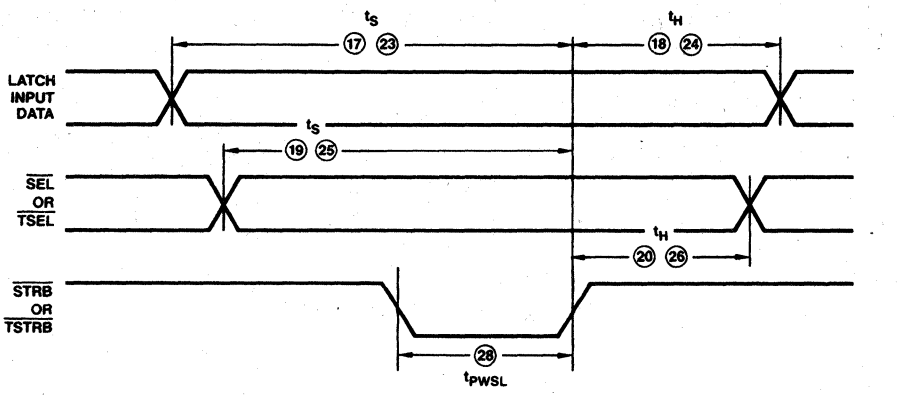
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

TIMING DIAGRAM



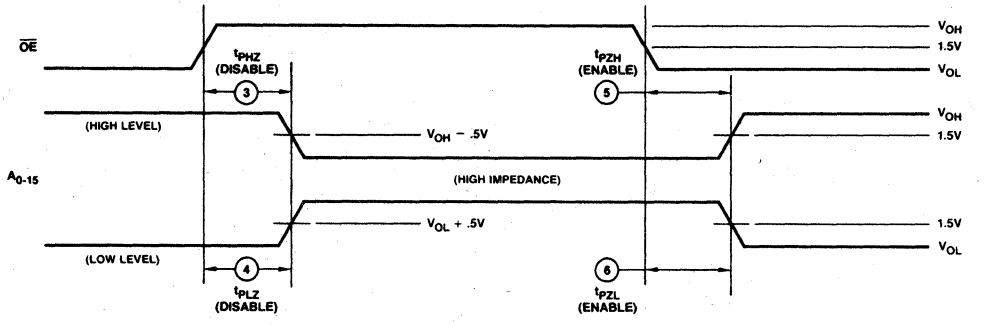
WFR02710

LATCH TIMING DIAGRAM



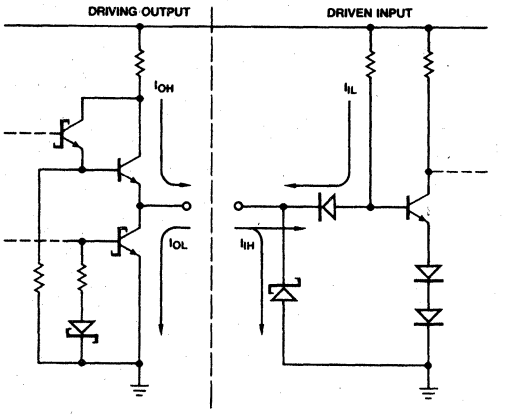
WFR02701

3-STATE TIMING DIAGRAM



WFR02720

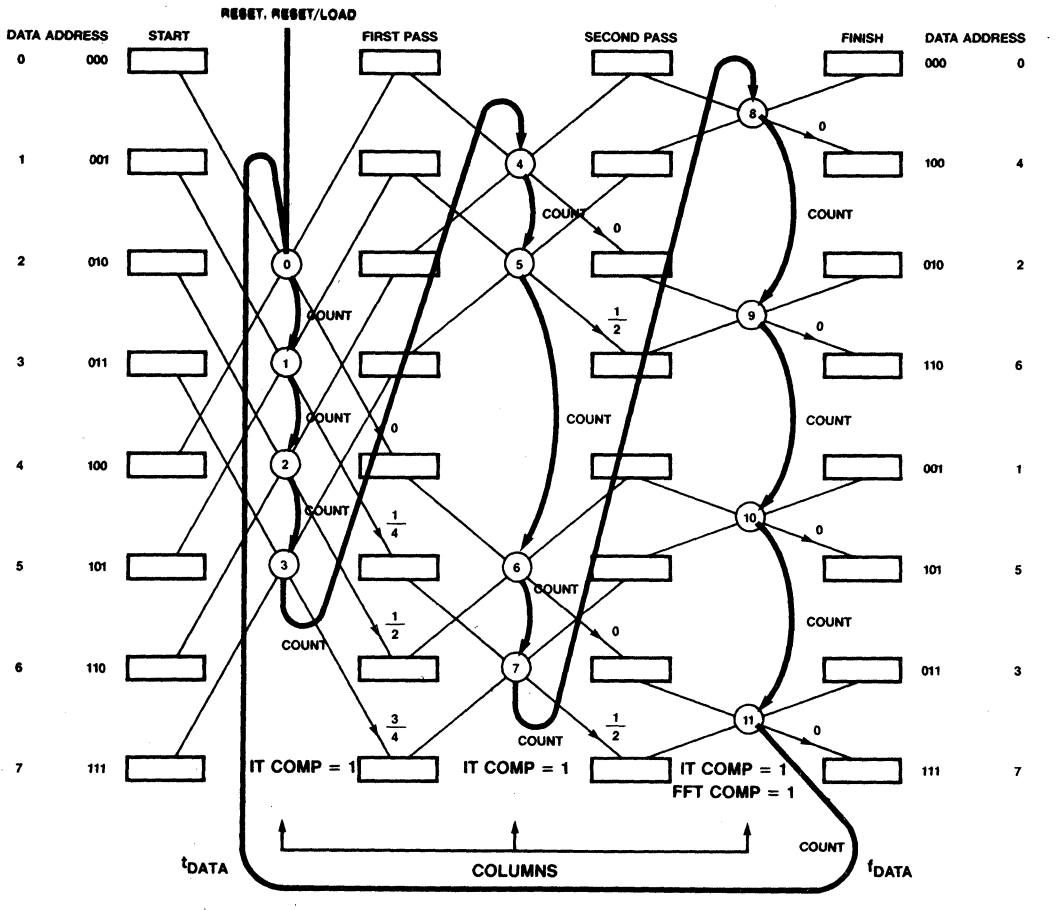
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00510

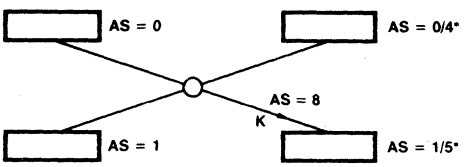
03567C

Refer to Page 13-1 for Essential Information on Military Devices



DFR00660

a. Sequence of Operations for Typical FFT



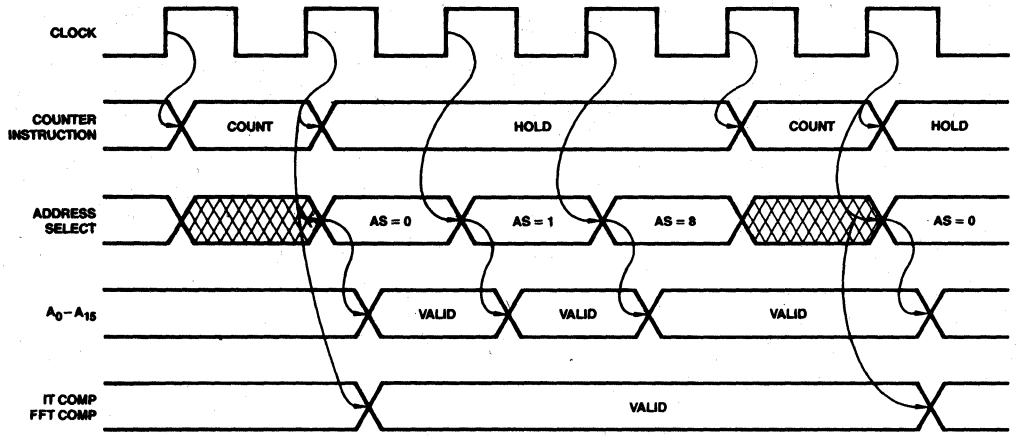
DFR00670

*Note: AS = 4 and AS = 5 are alternate addresses used in non-in-place transformations.

b. Single RADIX-2 Butterfly

Figure 4.

TYPICAL HIGH PERFORMANCE RADIX-2 ADDRESS GENERATION



DFR00690

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

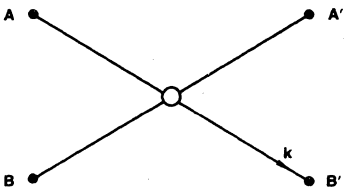
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

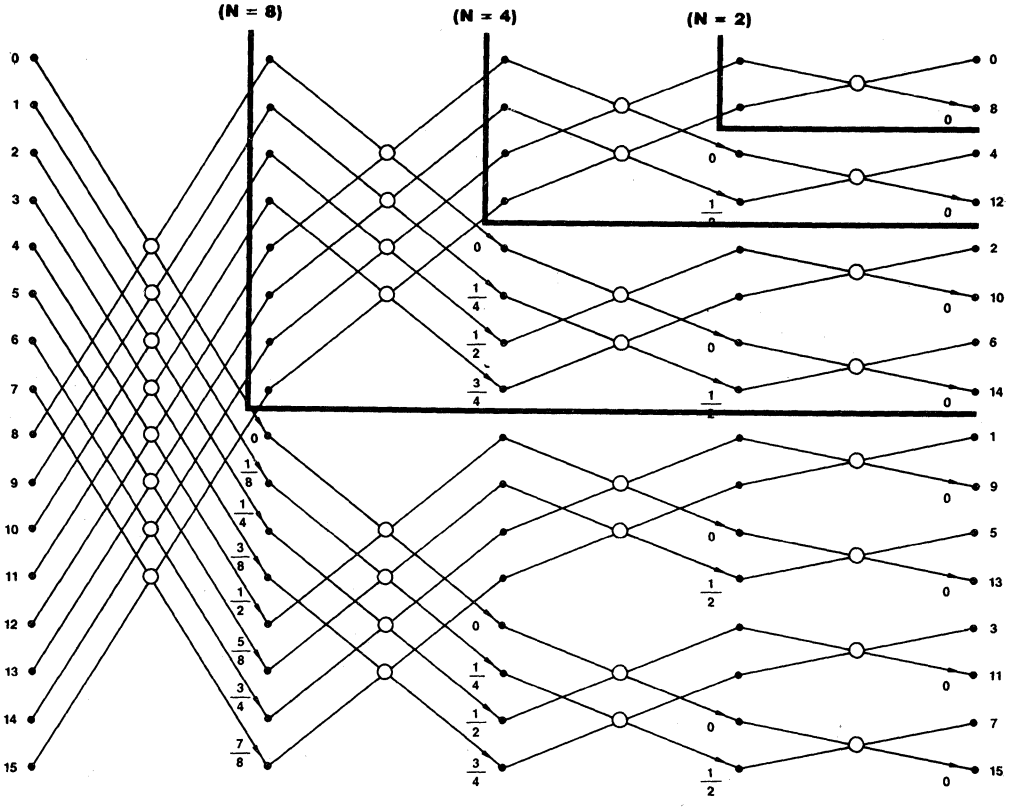
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00700

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

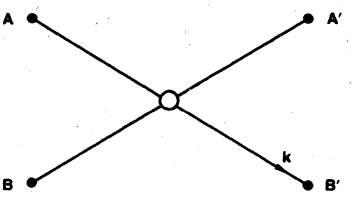
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

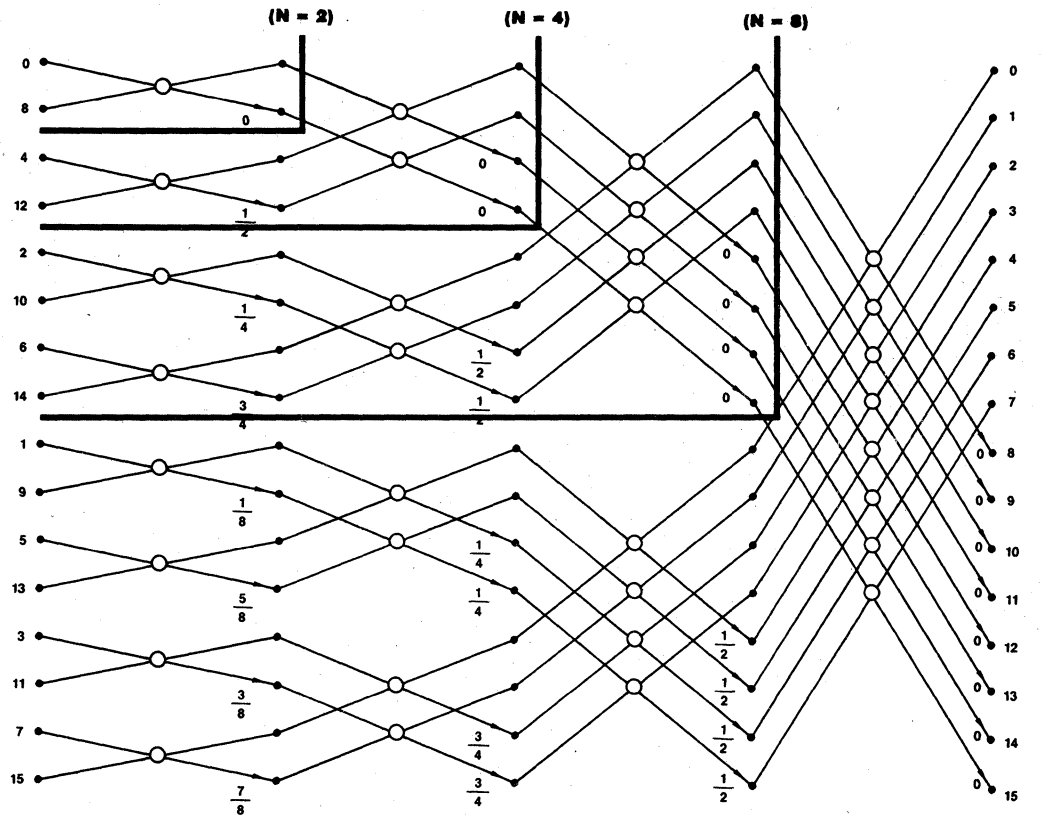
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00630

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	L	L

Address of	A	B	A'	B	W_K
AS =	0	1	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

FORWARD TRANSFORM

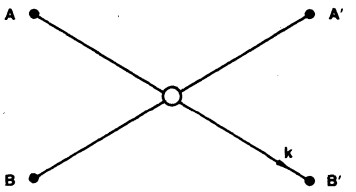
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

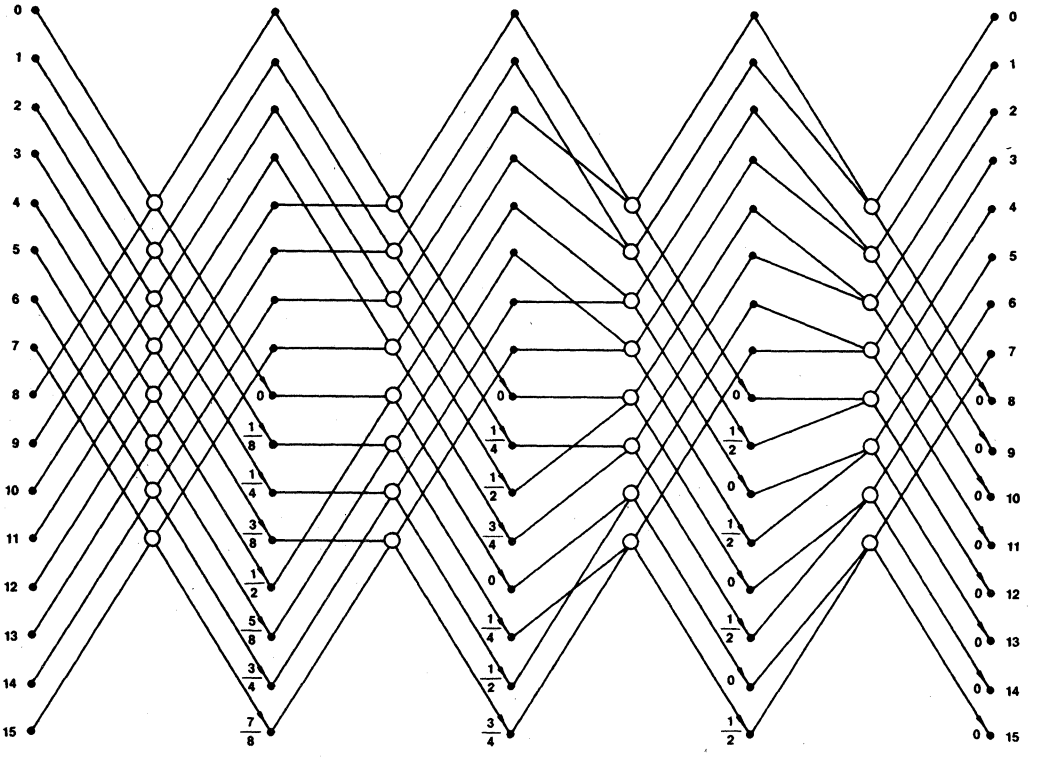
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00650

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/2
L	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	4	5	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

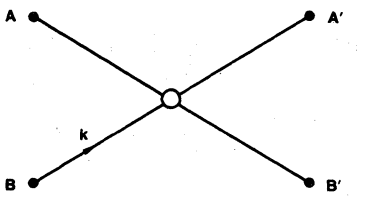
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

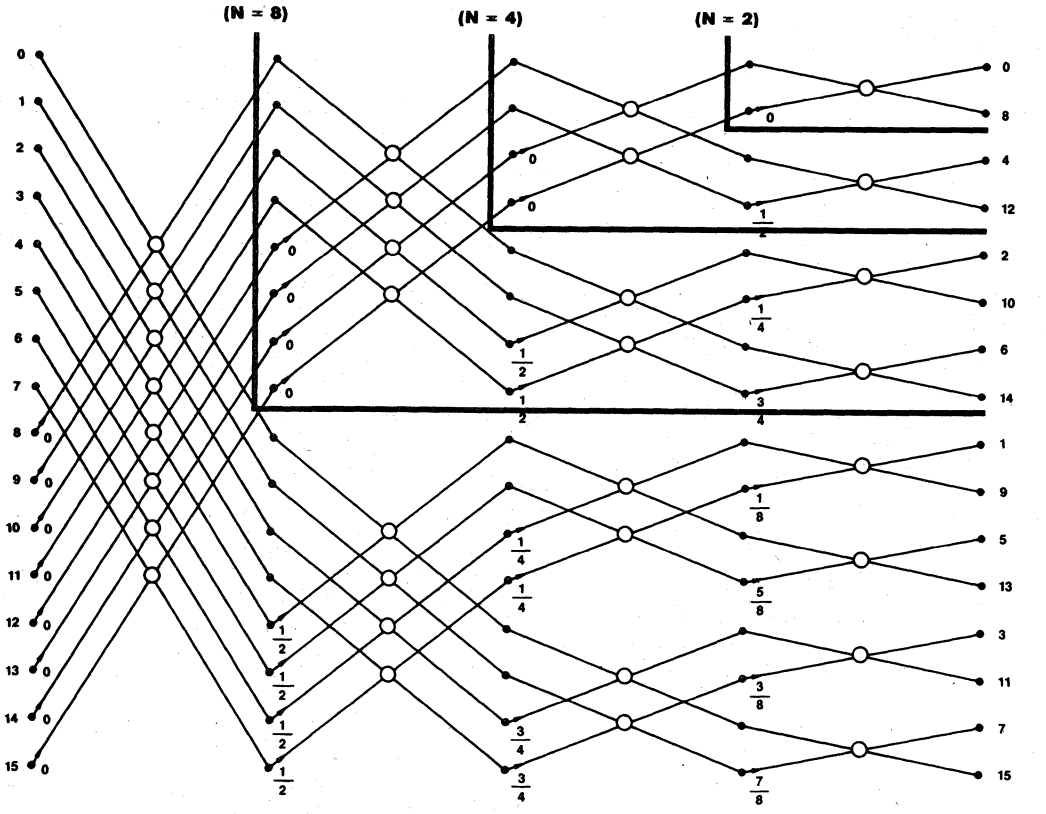
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-i\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00620

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

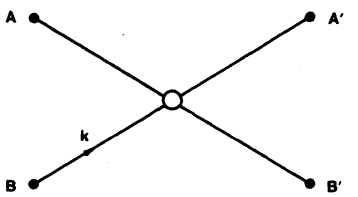
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

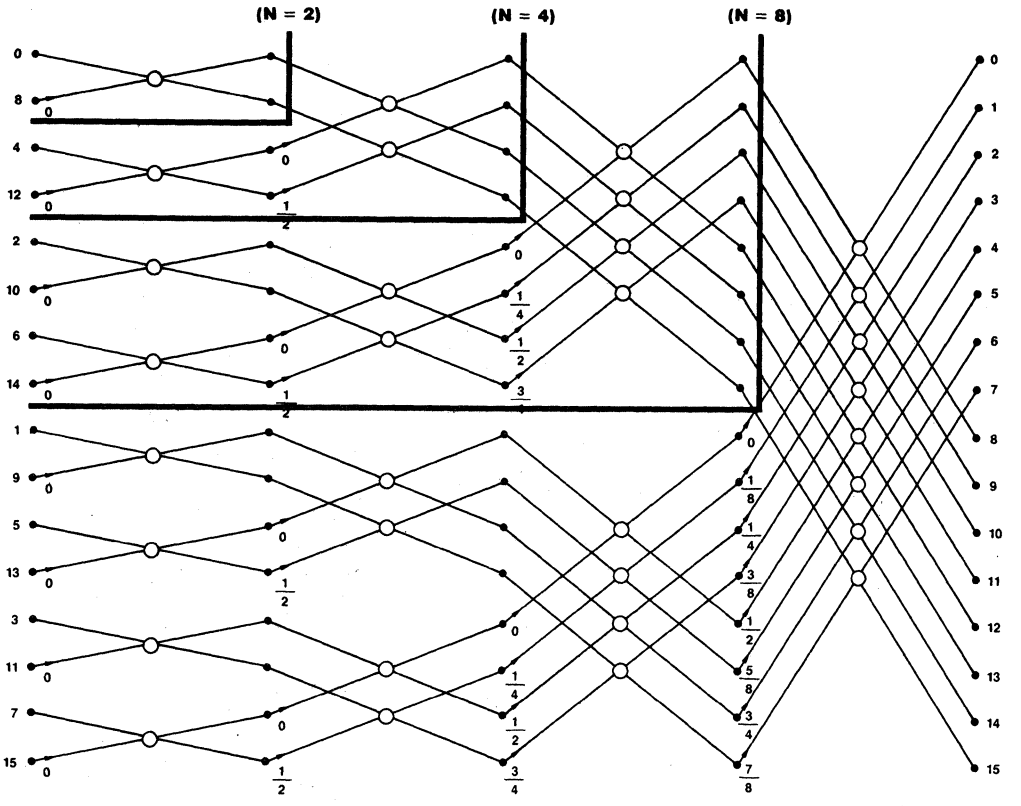
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00470

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	L	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

FORWARD TRANSFORM

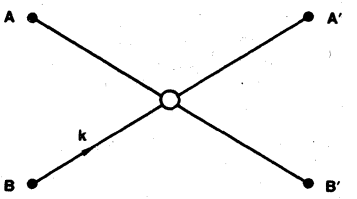
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

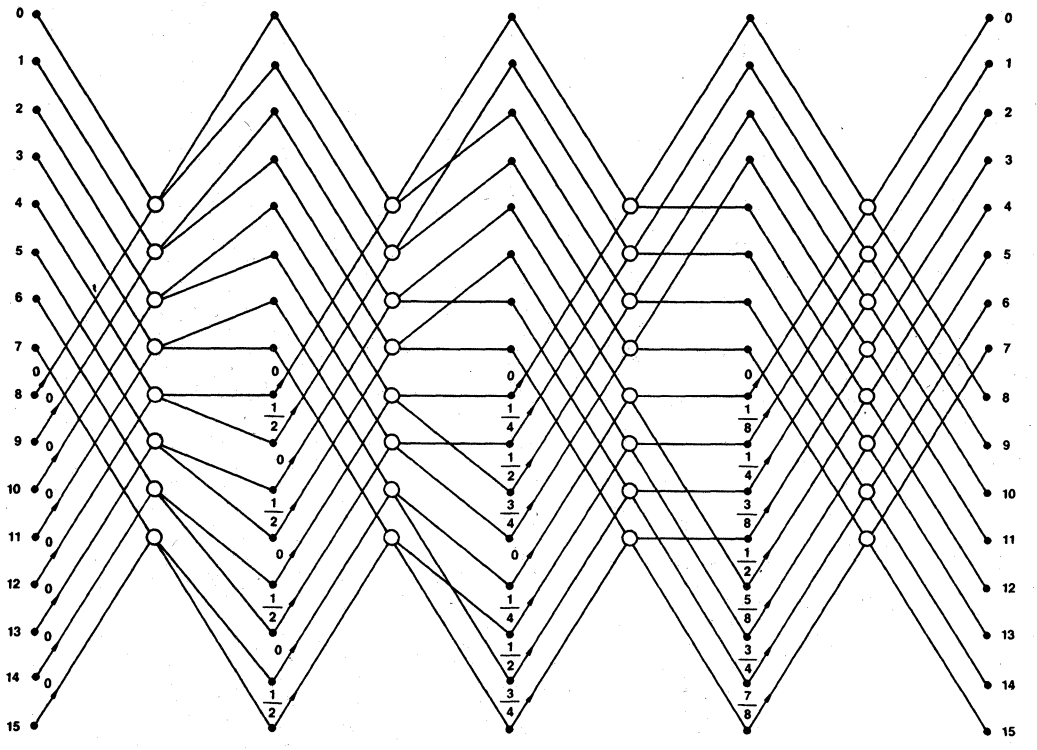
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00560

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	L	L

Address of	A	B	A'	B'	W^k
AS =	4	5	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input data (Digit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

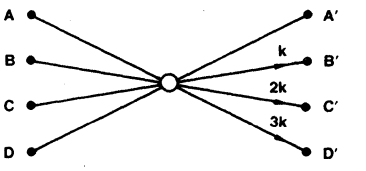
$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

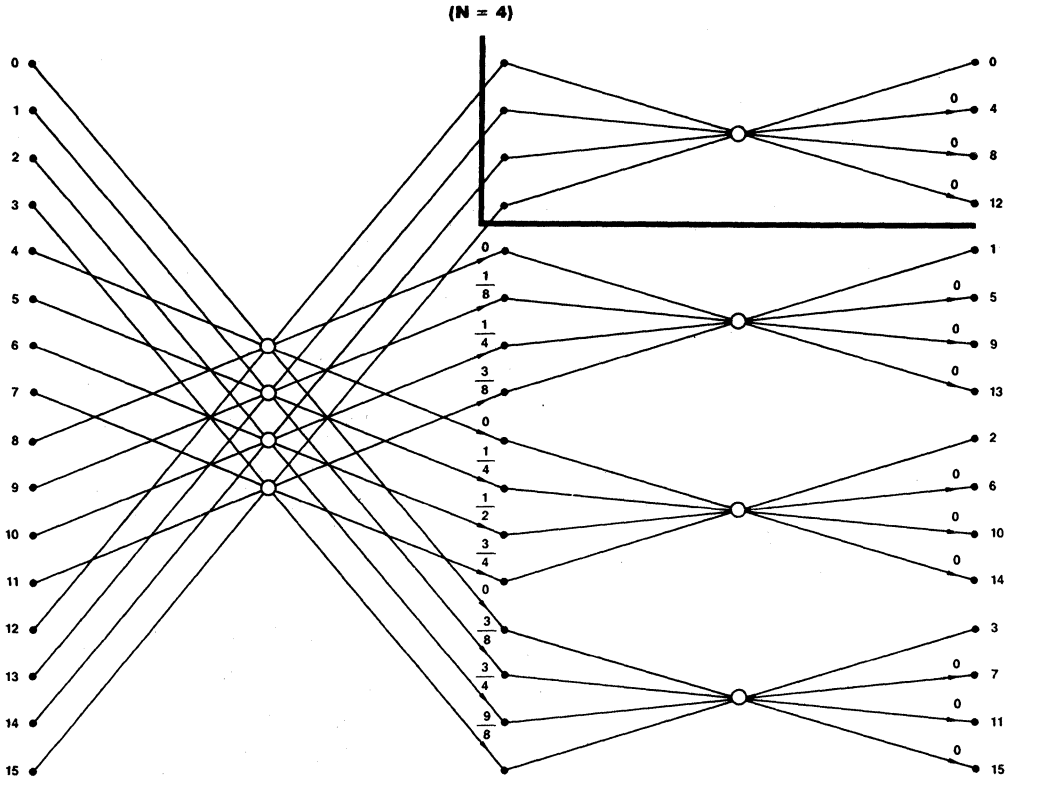
$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00510



DFR00570

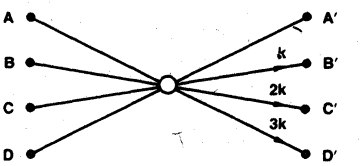
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00510

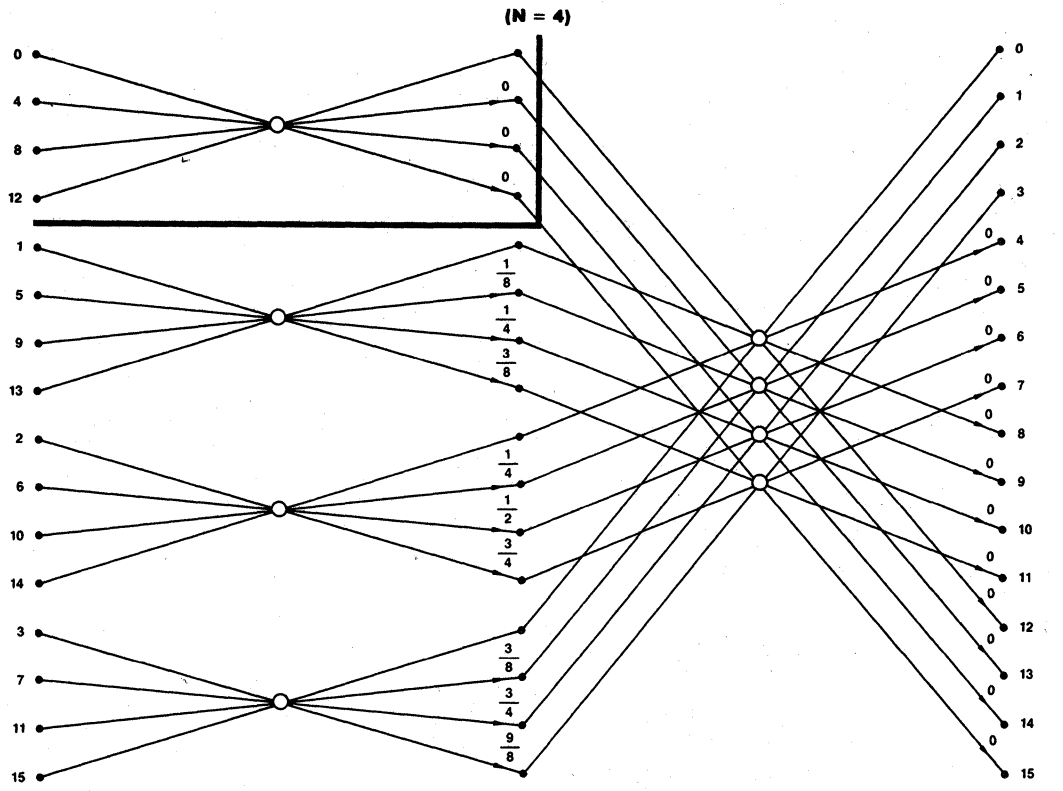
FORWARD TRANSFORM

$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$



DFR00500

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

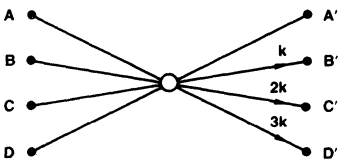
03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00510

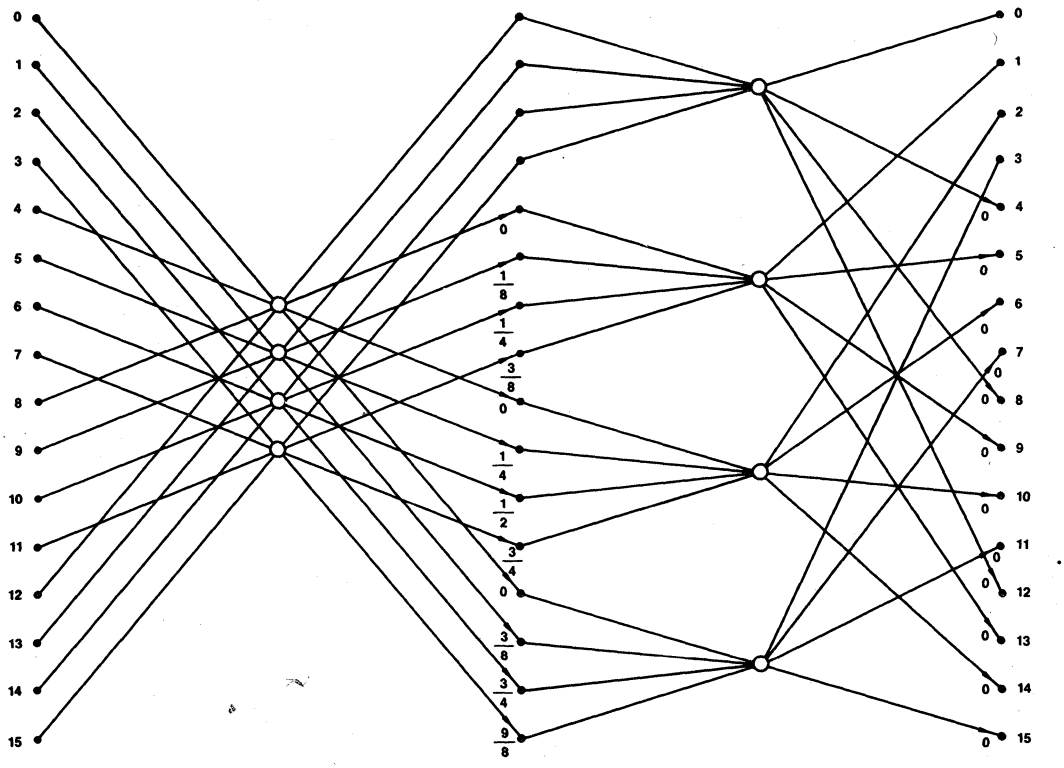
FORWARD TRANSFORM

$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$



DFR00580

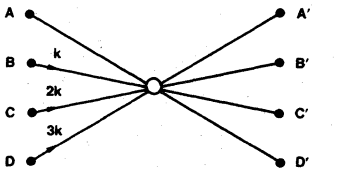
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	4	5	6	7	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input data (Digit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

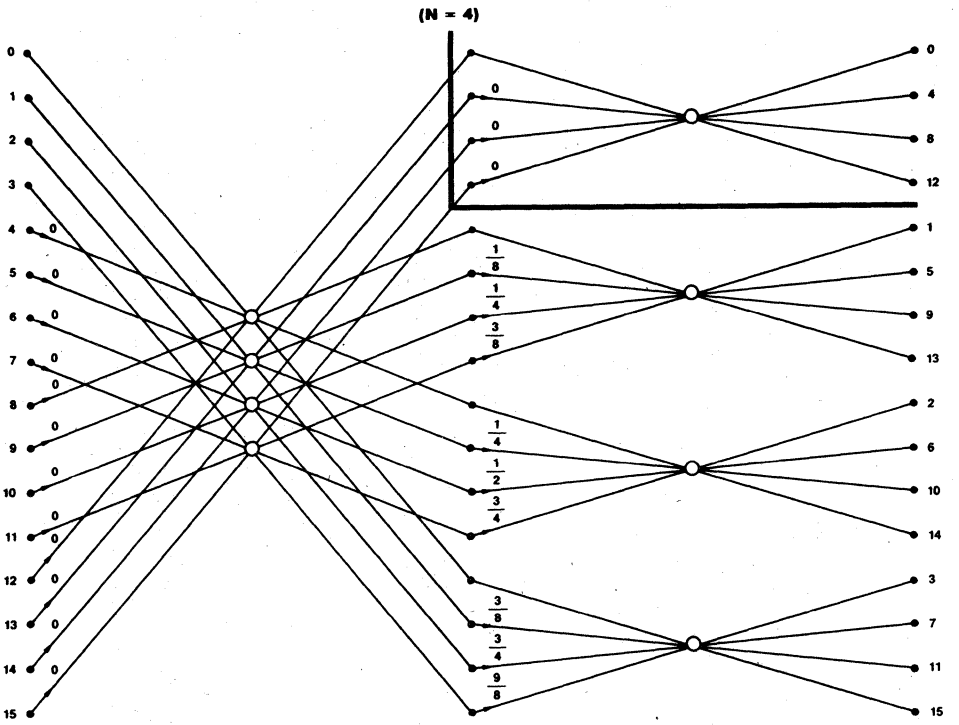
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00540

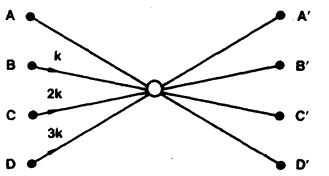
DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

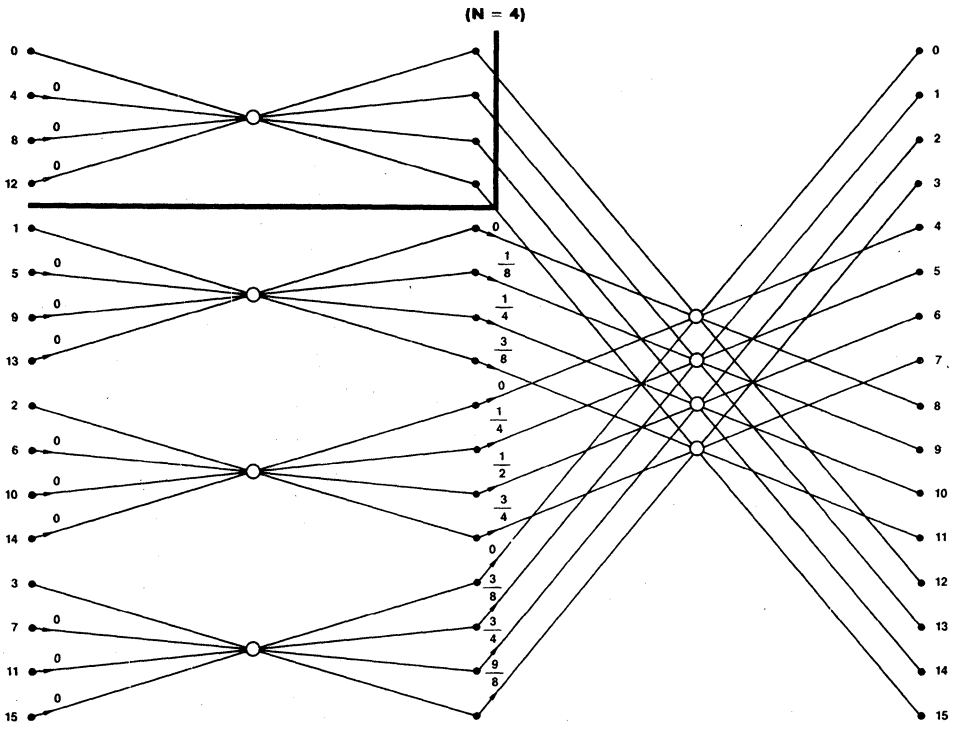
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00550

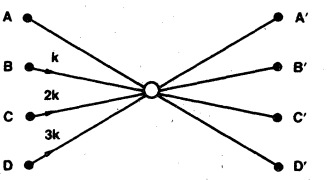
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/2
H	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

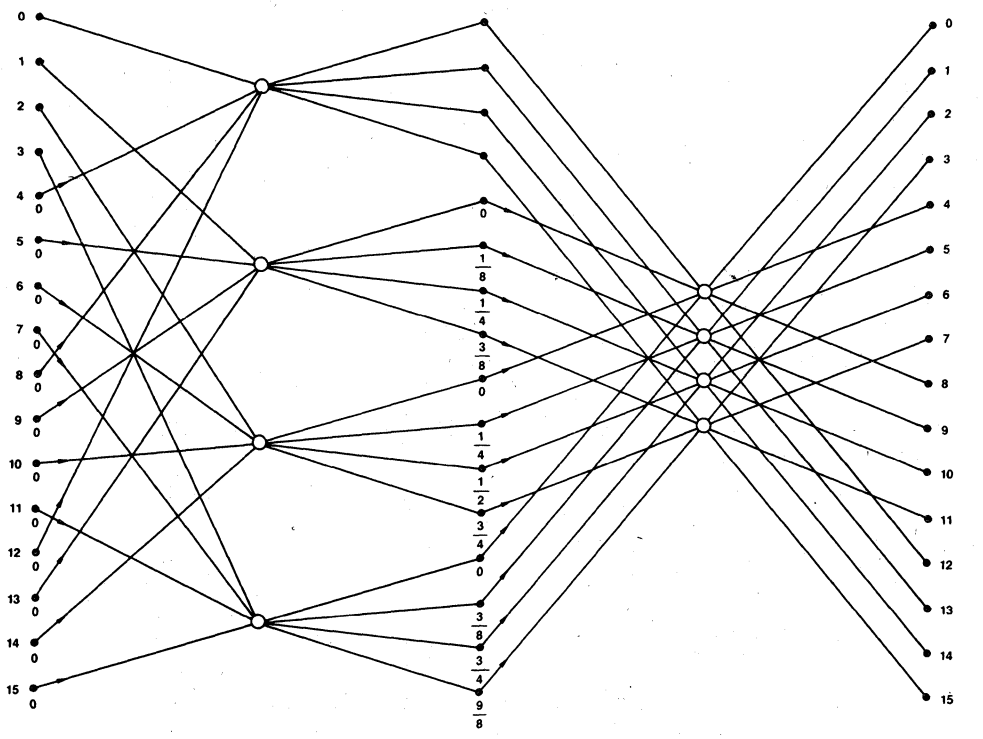
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00520

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/2
H	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	4	5	6	7	0	1	2	3	8	9	10

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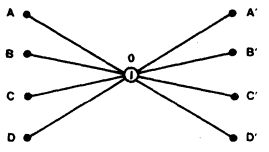
Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- Normally ordered output data (Unique input data order)
- DIF
- In-place
- Real valued output data
- Inverse Transform

TYPICAL BUTTERFLIES

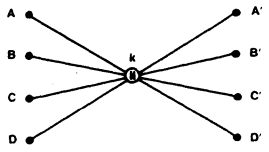
KNZ/$\overline{KZ}$ = LOW
(k = 0)



DFR00600

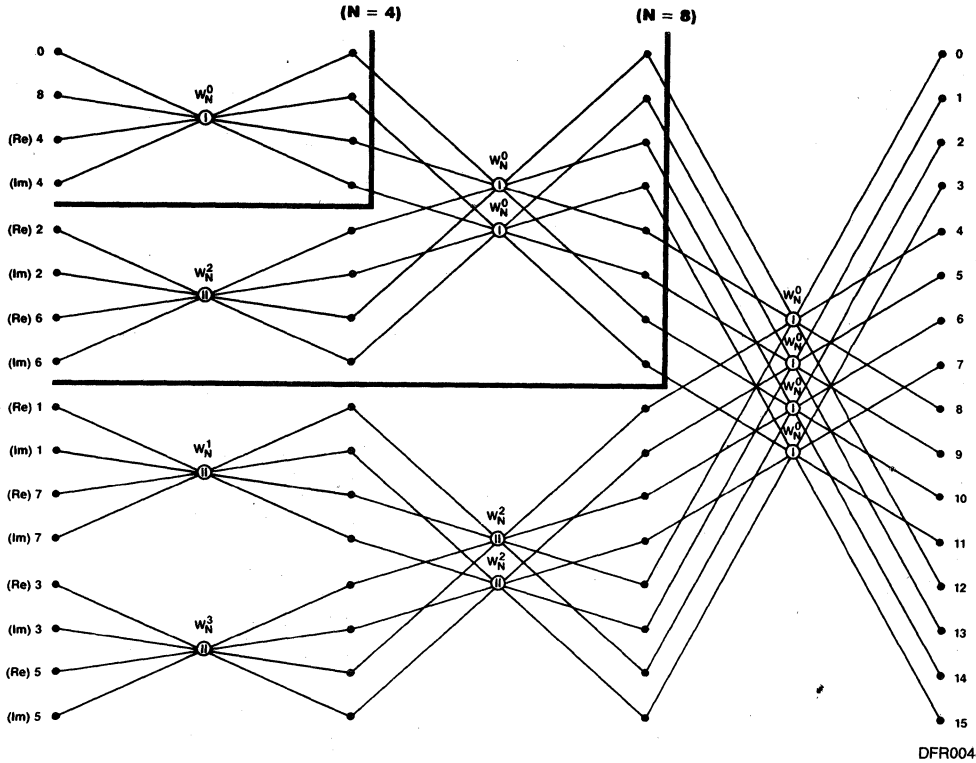
$A' = Re\ [A + jB + C - jD]$
$B' = Im\ [A + jB + C - jD]$
$C' = Re\ [(A + jB - C + jD)W_N^0]$
$D' = Im\ [(A + jB - C + jD)W_N^0]$
$W_N = ej^{2\pi/N}$

KNZ/$\overline{KZ}$ = HIGH
(k = 0)



DFR00610

$A' = Re\ [A + jB + C - jD]$
$B' = Re\ [(A + jB - C + jD)W_N^k]$
$C' = Im\ [A + jB + C - jD]$
$D' = Im\ [(A + jB - C + jD)W_N^k]$
$W_N = ej^{2\pi/N}$



DFR00480

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
L	L	L

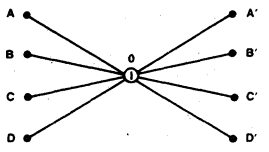
Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Unique output data order)
- In-place
- Real Valued Input (RVI) data
- Forward Transform

TYPICAL BUTTERFLIES

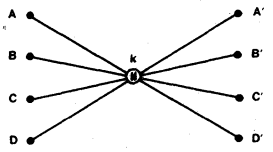
KNZ/$\overline{KZ}$ = LOW
(k = 0)



DFR00600

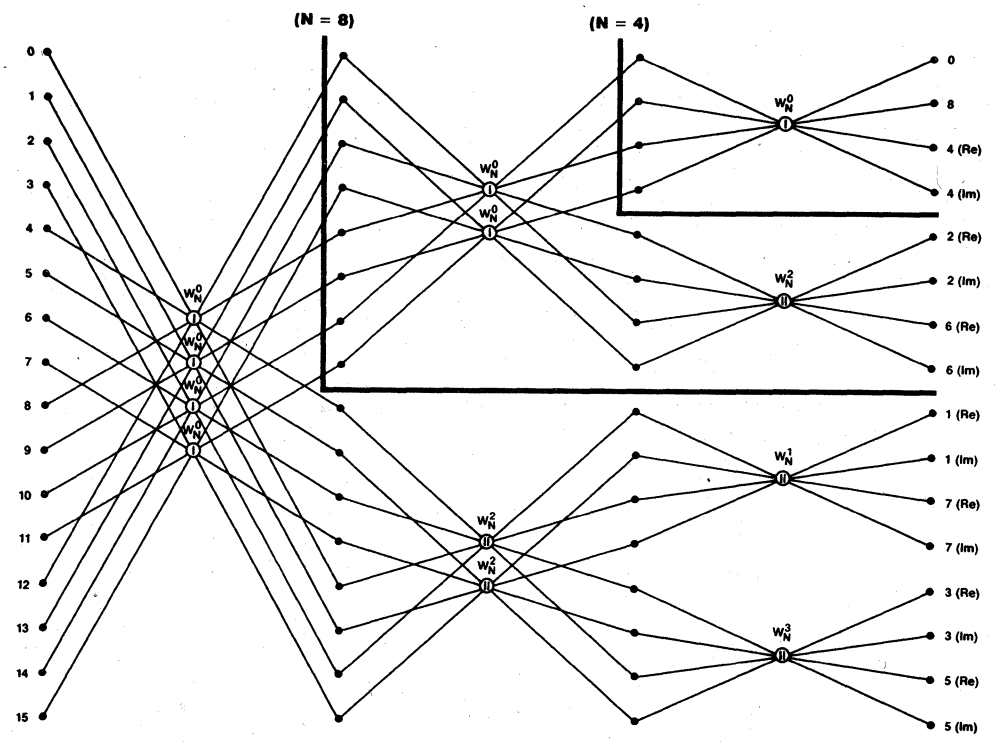
$A' = Re\ [A + jB + (C + jD)W_N^0]$
$B' = Im\ [A + jB + (C + jD)W_N^0]$
$C' = Re\ [A + jB - (C + jD)W_N^0]$
$D' = Im\ [-A - jB + (C - jD)W_N^0]$
$W_N = e^{\frac{-j2\pi}{N}}$

KNZ/$\overline{KZ}$ = HIGH
(k ≠ 0)



DFR00610

$A' = Re\ [A + jC + (B + jD)W_N^k]$
$B' = Im\ [A + jC + (B + jD)W_N^k]$
$C' = Re\ [A + jC - (B - jD)W_N^k]$
$D' = Im\ [-A - jC + (B + jD)W_N^k]$
$W_N = e^{\frac{-j2\pi}{N}}$



DFR00490

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	L

Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8

Am29800
High Performance Bus Interface and Logic Index

High Performance Bus Interface Family

David A. Laws and Peter Alfke
Advanced Micro Devices, Inc., Sunnyvale, CA

Standardizes Around Slim 24-Pin Package

Most IC designers tend to focus their attention on ever more complex VLSI solutions to improve the package count, cost, and reliability of microprocessor based systems. In many cases, however, greater impact could be achieved with much less effort by designing a more efficient bus interface. The last major innovation in this area was the advent of the popular 20-pin octal interface, which occurred not so coincidentally with the boom in 8-bit microprocessor sales.

The Octal Explosion

The 20-pin package was ideal for 8-bit interface elements as it allowed for eight input lines, eight output lines, two control inputs, power supply, and ground. Octal configurations of registers, latches and transceivers appeared in Schottky, low-power Schottky, and CMOS technologies from every major integrated circuit supplier, and as technology improved, a proliferation of polarity, pin rotation, high current drive, and low power options became available to meet every conceivable 8-bit need.

However, as the designers' world became more complex, it became apparent that modular sizes larger than 8 bits were needed. For example, systems that use a parity check scheme need 9 bits for each byte, and if a clock line is added, a 10-bit part is needed. The 10-bit part also fits nicely with the 20-bit addressing schemes used with many 16-bit microprocessors.

A 9- or 10-bit function previously required the one octal and one 4-bit part, which left the designer with two packages and potential problems. Clearly, the answer was a new approach.

The 24-Pin Solution

Two factors contributed to the 24-pin solution. First was the development of a more compact 24-pin package. Until recently the only package available for this pin count was a 600-mil wide DIP. Now a slimline, 24-pin 300-mil wide package, called Thin-DIP by AMD, is entering production at a number of package manufacturers. Second, advanced Schottky technologies made it possible to pack increased functional complexity onto chips small enough to fit into the narrow cavities of these new packages. AMD calls its version of this process IMOX™, an acronym which means ion-implanted and oxide-isolated.

The fabrication and packaging problems overcome, AMD proceeded to define a complete family of functions from the ground up. While the previous 20-pin octal interface devices had been a great improvement over their predecessors, the piecemeal approach to their conception had led to a bewildering array of inconsistent configurations. So before starting design on any one device, AMD applications engineers looked at all the essential interface functions required by a system. The result is the new Am29800 series.

The Am29800 Family includes registers, latches, buffers, and transceivers; most functions are supplied in 8- or 9- and 10-bit wide configurations. De facto standards have determined that most systems are noninverting internally, while most bus configurations are inverting. To meet all these needs, both inverting and noninverting versions of the Am29800 devices are available to the designer.

Now that two-layer metal interconnect is an established manufacturing process, it is possible to give careful consideration to the physical location of input and output pins. All inputs on the new Am29800 Family have been placed on one side of the package with corresponding outputs on the other, so data can flow in a direct physical path from the microprocessor CPU through the interface unit and onto the bus. This permits a much cleaner board layout. In addition, power supply, ground, and control function pins are always in the same position.

AMD also decided to standardize pinouts between logic functions. For example, all 10-bit elements, i.e., latches, registers, or transceivers, have the same input and output pin assignment, as do all 9- and 8-bit devices.

Electrical Performance

For many years, TTL devices, such as the 'S240 series, employed PNP inputs to achieve very low input current characteristics. Unfortunately, while the DC input current is indeed low, the dynamic performance of the device is severely downgraded because of the large capacitance associated with the PNPs. The Am29800 devices were designed with low capacitance loading at the inputs and outputs.

Most IC data sheets specify AC performance at 15pF test conditions only. While this is adequate for general purpose logic applications, a realistic bus structure will typically see much higher loading, and all Am29800 series devices are designed to provide optimum performance under more realistic system conditions. Specified sink currents of 48mA over the commercial temperature operating range (0 to 70°C) and 32mA over the military temperature range (−55 to +125°C) ensure adequate capacitance drive and fan-out for bus systems. And since drivers must charge load capacitance in both falling and rising directions, source current is also fully characterized at both 2.0 and 2.4V.

Critical AC specifications such as propagation delays and disable times for the three-state outputs are specified for 300pF load conditions both at 25°C and over the full operating temperature range and power supply tolerance; specific delays depend on the function being considered. Typical values for a D-type register at 50pF are 6 to 7ns, comparable to those achieved with AS or FAST devices under the same conditions and an improvement over higher power Schottky products. At 350pF, loading delays increase to the 12 to 14ns range. Simple buffers and inverters exhibit typical values of 4ns.

Registers

The Am29821-26 Bus Interface Registers are specifically designed to provide extra width for wide address or data paths and buses carrying parity.

05405A

Refer to Page 13-1 for Essential Information on Military Devices

The Am29821 is a 10-bit wide version of the popular '374 8-bit register. It has ten inputs, ten outputs, common buffered clock enable and three status Output Enable lines. The inverting version, Am29822, is comparable with the '534 8-bit device.

The 9-bit registers, Am29823 and Am 29824, give up one bit to gain two additional control lines which are used for Clock Enable ($\overline{EN}$), and Clear ($\overline{CLR}$). This combines '273, '374 and '377 functions in one single package. The extra pins available on the 8-bit parts, Am29825 and Am29826, provide gate output enable capability, which eliminates the need for external gate packages when used in DMA or Multibus* control applications. The Am29825 can also be used to implement high source/sink drive on the data port for the AmZ8000** or 8086 16-bit CPUs. The registers can be controlled from WR and CS, can be cleared and can be disabled for DMA operations. The two 24-pin parts replace four of the earlier octal devices plus one gate package, and system performance is improved up to three or four times because of the reduced number of gate delays and shorter wiring traces.

Other Functions

Other functions in the Am29800 Family include latches, buffers and transceivers, comparators, and special parity transceivers.

The Am29841 through Am29846 latches follow the pattern as the registers. The 10-bit device is similar in function to the popular 'S373 octal latch; control lines available are latch enable (LE) and three-state output enable (OE). The noninverting device is analogous to the '533 element. The 9-bit latches add preset (PRE) and clear (CLR) and the 8-bit options have added gated output enable controls.

Buffers and inverters, Am29827 and Am29828, are 10-bit wide high performance versions of the '240 and '244 devices, while the transceivers emulate the '245 and 8304B octal elements. For improved operation in a noisy bus environment, all data inputs have 200mV minimum input hysteresis.

The Metastable Problem

One problem faced by designers is the interfacing of asynchronous digital signals. Although most difficulties can be overcome somewhat easily, there is also a more fundamental problem that defies a perfect solution. The following is a general overview of the metastable problem.

Latches and flip-flops are normally considered bistable devices, since they have two unconditionally stable operating points, either HIGH or LOW. There is, however, a third operating point when the cross-coupled arrangement is exactly balanced. This operating point is stable only if there is no noise in the system and the system is perfectly balanced. The condition is called metastable (meta = Greek for "between"). A metastable condition will last only long enough for the circuit to fall into one of the two stable operating points. This time can be many microseconds, even milliseconds, for devices as fast as a 74S74 flip-flop. In other words, if a flip-flop has reached the balanced, metastable condition, it may remain in this state for an undetermined time, perhaps 1000 times longer than its normal response speed.

When Does This Cause A Problem?

In almost every digital system certain asynchronous events (key-strokes, incoming data, interrupts), must be synchronized to the computer clock. The textbook solution is a fast, clocked flip-flop, like the 74S74, in which the asynchronous signal is applied to the D input and clocked with the system clock. This results in a perfectly synchronized output (usually).

Let's analyze the timing more carefully: the data sheet specified a setup time requirement (for this device, t_S = 3ns). This means that any signal that arrives at least 3ns before the clock edge will achieve the intended result, i.e., an H will set, an L will reset the flip-flop. Great for synchronous systems. But what happens when the asynchronous input violates this setup time requirement and changes less than 3ns before the clock edge? Well, most of the time, nothing. The actual moment where the flip-flop samples the D input is somewhere in the guaranteed range, i.e., somewhere less than 3ns before the clock. So the flip-flop makes the decision. It either senses the change on the asynchronous input and therefore changes its Q output, or it ignores the change and doesn't change the Q output. So the only thing lost is one clock cycle. Unfortunately, that's not always true.

"Going metastable" here means that the synchronizer output is within a mid-level or oscillation range for an unpredictable time. Most occurrences will last less than 50ns, but may occasionally last much longer — perhaps many microseconds. This certainly can upset the timing chain.

A metastable latch or flip-flop has an unpredictable delay and will therefore change its output at a time that differs from the value obtained from the worst case timing analysis. In a slow system this usually doesn't matter, but in a fast system it can lead to a "crash."

In Conclusion:

The Am29800 Family registers provide an additional bonus; they recover extremely fast from a metastable condition.

The metastable condition occurs in all flip-flops any time the active clock edge interrogates the input at exactly the same time the input changes state. When this happens, the cross coupled latch at the output can reach a balanced, symmetrical condition which it will hold for some microseconds or even milliseconds before returning to its proper state. Previously, the designer of an asynchronous system had only one remedy for the metastable problem. Two or even three synchronizer flip-flops could be cascaded. This reduced probability of a metastable output but increased throughput delay.

The Am29800 registers, while not totally immune to this problem, are "metastable hardened" by means of a unique circuit design that reduces both the probability **and** the delay of any metastable condition under test. Artificially induced, a metastable condition failed to produce any output oscillations and increased the clock-to-input delay by a mere 6ns. This is an improvement of many orders of magnitude over previously available designs.

It is Now Necessary to Look Beyond the Data Sheet

If the D input changes exactly at the same moment that the flip-flop makes its decision, it might transfer exactly the amount of energy to kick the output latch into the metastable balanced condition, from which it will recover after an unpredictable delay (measured in nanoseconds, microseconds or even milliseconds).

In other words: any latch, flip-flop, or register has a "moment of truth" somewhere inside the guaranteed range of setup time where it actually makes up its mind, and if the input changes at that very moment, the output is no longer synchronous. This "moment of truth" is a very short window. For TTL flip-flops it is of the order of 10ps; for MOS devices it is more like 50ps to 100ps. For purposes of this discussion this timing window will be called "t."

How often does this happen?

*Multibus is a registered trademark of Intel Corporation.
**Z8000 is a trademark of Zilog, Inc.

Here are two extreme examples. In each case there is a need to synchronize asynchronous inputs that have **no phase or frequency relationship** with the computer clock.

- Date signal derived from a disk, roughly 6MHz with enough frequency modulation and jitter to make it totally asynchronous to the 10MHz computer clock. How often will the TTL synchronizer go metastable?

  The answer is: every time the Data Signal falls into the "window." The probability of hitting the window is t divided by the clock period, or even simpler: clock frequency times t.

  M = Metastable Rate $= f_D \cdot f_C \cdot t$
  f_D = Device Frequency = 6MHz • 10MHz • 10ps = 600Hz
  f_C = Clock Frequency

  The synchronizer goes metastable **600 times per second.**

- Keyboard entry: one keystroke per second synchronized with a 100KHz clock.

  M = Metastable Rate = 1Hz • 10^5Hz • 10ps = 10^{-6}Hz

The synchronizer goes metastable with a statistical probability of once per 10^6 sec, i.e., **once every six weeks** (assuming 5 eight-hour days/week).

29800 Design Guidelines

The 29800 Family offers short delay and setup times, high drive capability (fan-out), and low input capacitance—attractive features for modern high performance TTL systems.

As in any high speed bus interface ('S240 series, FAST or Advanced Schottky), high edge rates and high drive capability mean that a certain amount of care must be exercised in the design of both signal paths and the grounding system. Since every data path is really a transmission line, the relationships between loading, termination, noise margins and ringing must be given more than cursory consideration.

Similarly, the grounding network may require either heavier busing or a grid approach depending on the number of drivers in a given area. 48mA per bit, plus the AC impact of charging bus lines can cause large ground currents. Distributed supply decoupling is required to provide local charging current for bus drive.

Here are some general suggestions to minimize the potential for system induced grounding and noise problems. These suggestions, in conjunction with the designer's own practical experience handling similar problems with high performance S, AS or FAST logic families, will result in an optimum Am29800 design.

- **Minimize Crosstalk**

  Provide Tight Ground
  - Use topside links to create a ground "grid"
  - In multi-layer boards, use a ground plane
  - In flat cables, make every other wire a ground
  - Minimize spacing between signal lines and ground
  - Maximize spacing between signal lines

  For backplane or wire-wrap systems, use a twisted pair for sensitive functions – clock, asynchronous set/clear lines.

  Use of 4 layer boards is recommended.

- **Increase Decoupling**

  Distribute System Capacitance
  - Provide one bypass cap close to each buffer package
  - Provide one bypass cap for every two logic packages

  Use High Frequency Capacitors
  - Take care in the selection of decoupling capacitor materials. Good choices include high frequency tantalum and ceramic types.
  - Do not use low frequency capacitors or aluminum electrolytics

- **Be Sure All Lines Are Terminated**

Am29806/Am29809

6-Bit Chip Select Decoder
9-Bit Equal-to-Comparator

DISTINCTIVE CHARACTERISTICS

- High-speed, expandable, 9-bit "equal-to" comparator (Am29809)
- High-speed comparator with chip select decoder (Am29806)
- Multibus™ compatible, open-collector acknowledge output
- Internal pull-up resistors on all B inputs
- Acknowledge timing control input
- Fully TTL-compatible inputs and outputs

GENERAL DESCRIPTION

Am29809 9-Bit Comparator

The Am29809 is a 9-bit "equal-to" comparator. Its combinatorial, active LOW output, $\overline{E}_{OUT}$, responds to the combination of a LOW input on the enable input $\overline{G}$ and a match between input words A and B.

Am29806 Chip Select Decoder

The Am29806 combines a 6-bit "equal-to" comparator with a 2- to 4-line decoder to select one-of-four active LOW chip select outputs. The selected output becomes active in response to the select inputs S_0, S_1 and is enabled by an active LOW input on the enable input $\overline{G}$ and a match between comparator inputs A and B. The active LOW output, Any Enable ($\overline{ANYE}$), responds to a valid comparison of A and B and is intended for use as an output enable control for data path buffers associated with the selected peripheral or board.

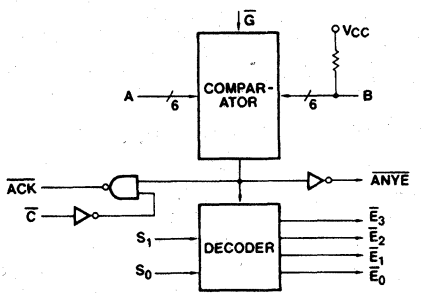
Both devices have open collector, active LOW acknowledge outputs with a conditional timing input $\overline{C}$ that may be driven by a timing circuit or wait state generator. The acknowledge output responds to a valid comparison, $\overline{G}$ = LOW and $\overline{C}$ = LOW.

Both devices have internal pull-up resistors on the comparator B-inputs for easy connection to SPST switches to ground selected input lines. The comparator function is described by:

$$\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\,(A_1 \cdot B_1)\,(A_2 \cdot B_2)\,\ldots\,(A_i \odot B_i)\,G}$$

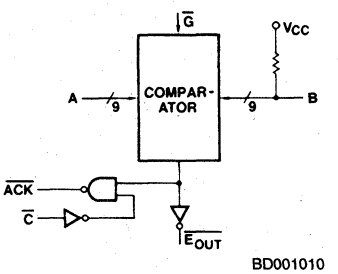
BLOCK DIAGRAM

Am29806 (6-Bit)



BD001000

Am29806 (9-Bit)



BD001010

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IMOX is a trademark of Advanced Micro Devices, Inc.

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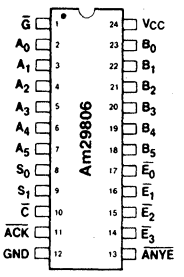
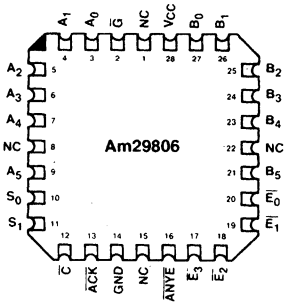
CONNECTION DIAGRAM
Top View

D-24-SLIM



CD001460

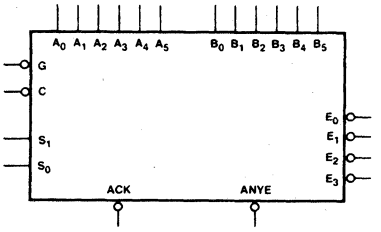
L-28-1



CD001480

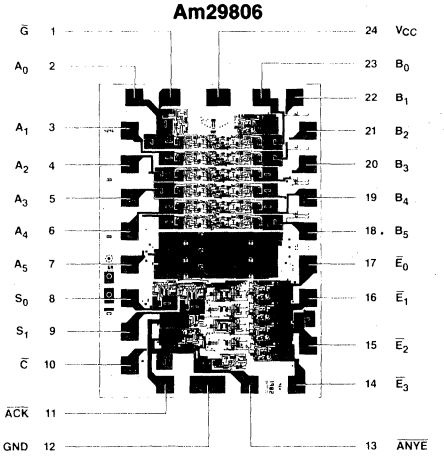
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am29806



LS000490

METALLIZATION AND PAD LAYOUT
Am29806



DIE SIZE:.066″ x .098″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29806 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D– 24-pin ceramic SLIMDIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X– Dice
- Am29806 — Device type
  - Am29806 – 6-Bit Chip Select Decoder
  - Am29809 – 9-Bit Equal-to-Comparator

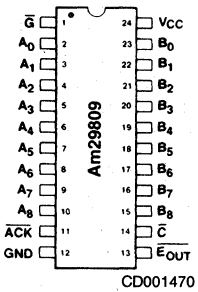
Valid Combinations	
Am29806 Am29809	DC, DCB, DM, DMB LC, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

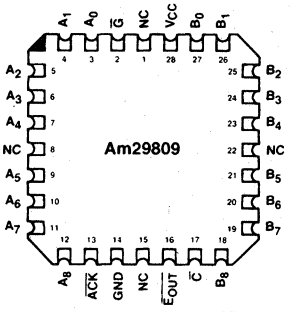
CONNECTION DIAGRAM
Top View

D-24-SLIM



CD001470

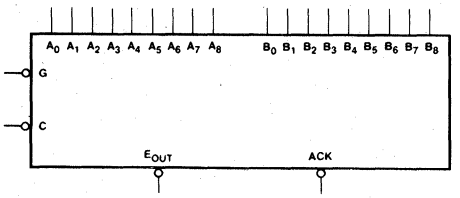
L-28-1



CD001490

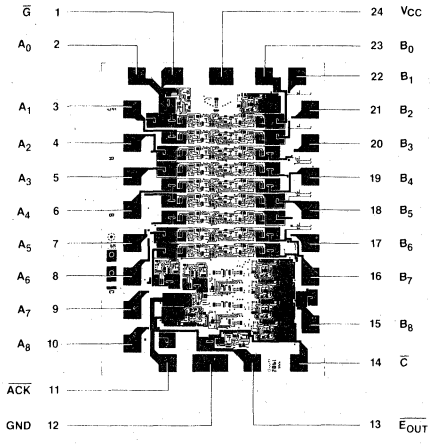
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am29809



LS000500

METALLIZATION AND PAD LAYOUT
Am29809



DIE SIZE:.066″ x .98″

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_i, B_i	I	Comparator data inputs. Each A_i is compared with each B_i on a bit basis. The comparator output is valid when all A_i bits match all B_i bits.
11	$\overline{ACK}$	O	Active LOW open collector acknowledge output. This output acknowledges memory of I/O transfers when A and B match and $\overline{C}$ and $\overline{G}$ are LOW.
13	$\overline{ANYE}$ (Am29806)	O	Active LOW output. Any Enable ($\overline{ANYE}$) is LOW when $\overline{G}$ = LOW and there is a match between A and B.
10	$\overline{C}$	I	Active LOW input. This input is used to control when $\overline{ACK}$ is active. It will normally be connected to GND when no wait states or timing delays need to be inserted. It may be connected to a wait state generator or timer.
13	$\overline{E_{OUT}}$ (Am29809)	O	Active LOW output. The comparator output is active for $\overline{G}$ = LOW and a match between A and B.
1	$\overline{G}$	I	Active LOW input. The comparator's input enable determines if the comparator's output is valid. $\overline{G}$ is normally used as an expansion input (connected to Am29809 $\overline{E_{OUT}}$).
Am29806 Only			
9,8	S_1, S_0	I	Decoder select inputs. These inputs are decoded to produce a 1-of-4 selection of the $\overline{E_i}$ outputs.
17–14	$\overline{E_0}$, $\overline{E_1}$, $\overline{E_2}$, $\overline{E_3}$	O	Active LOW outputs. 1-of-4 outputs is active as selected by S_1 and S_0.

FUNCTION TABLES

COMPARATOR FUNCTION TABLE

$\overline{G}$	A	B	$\overline{E_{OUT}}$ or $\overline{ANYE}$
H	X	X	H
L	A = B		L
	A ≠ B		H

ACKNOWLEDGE FUNCTION TABLE

$\overline{ANYE}$ or $\overline{E_{OUT}}$	$\overline{C}$	$\overline{ACK}$
H	X	H*
X	H	H*
L	L	L

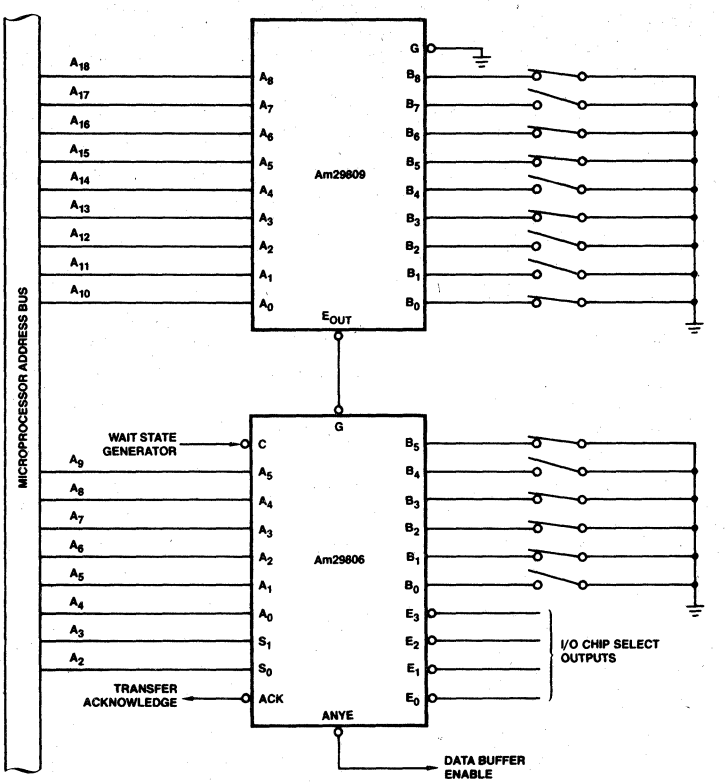
* Assumes pull-up resistor.

DECODER FUNCTION TABLE (Am29806)

$\overline{ANYE}$	S_1	S_0	$\overline{E_0}$	$\overline{E_1}$	$\overline{E_2}$	$\overline{E_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
	L	H	H	L	H	H
	H	L	H	H	L	H
	H	H	H	H	H	L

TYPICAL APPLICATION

MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER



AF000330

MAX $\overline{\text{ENABLE}}$ (HIGH - to - LOW) DELAY OVER 15 BITS

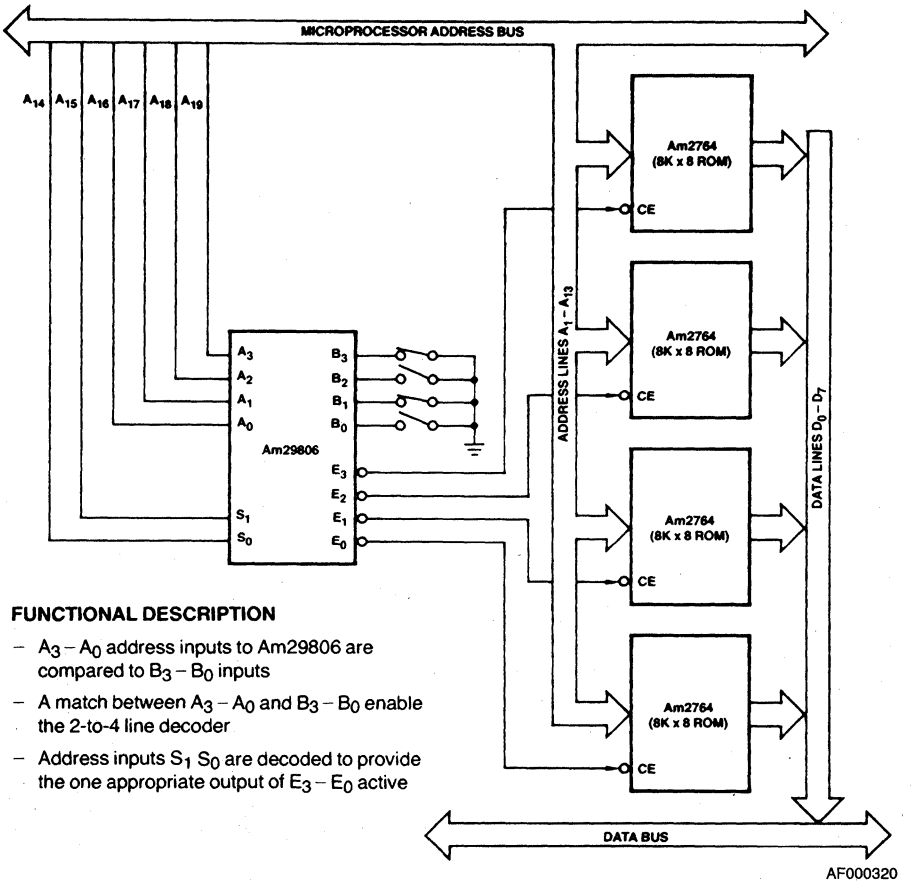
(Commercial Range)

t_{PHL}	A_i or B_i to $\overline{E_{OUT}}$	13
t_{PHL}	$\overline{G}$ to $\overline{ANYE}$	11
Total		24

TYPICAL APPLICATION

ADDRESS DECODING

Am29806 Decodes and Enables 1 of 4 Banks of Memory



AF000320

FUNCTIONAL DESCRIPTION

- $A_3 - A_0$ address inputs to Am29806 are compared to $B_3 - B_0$ inputs
- A match between $A_3 - A_0$ and $B_3 - B_0$ enable the 2-to-4 line decoder
- Address inputs S_1 S_0 are decoded to provide the one appropriate output of $E_3 - E_0$ active

8

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

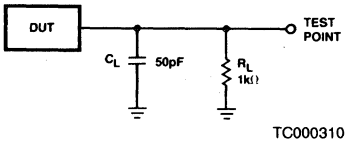
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage (Note 2)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{ACK}$ I_{OL} = 32mA			0.5	Volts
			All Others I_{OL} = .24mA				
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	A_i			−0.6	mA
			B_i			−1.0	
			All Others			−0.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V	A_i			20	μA
			B_i (Note 4)			−250	
			All Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	A_i			0.1	mA
			B_i			0.1	
			All Others			0.1	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	0 to 70°C		35	50	mA
			+70°C			45	
			−55 to +125°C		35	50	
			+125°C			40	

Notes: 1. Typical limits are T_A = 25°C V_{CC} = 5.0V
2. Except one-collector acknowledge output.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Due to internal pull-up resistor: 27kΩ nominal.

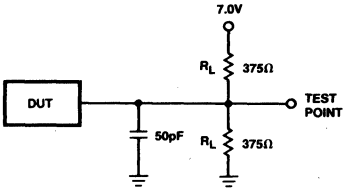
SWITCHING TEST CIRCUIT

Normal Output



TC000310

Open-Collector Output



TC000320

Note: C_L includes scope probe, wiring and stray capacitances without device in test fixture.

Figure 2.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions (See Figure 2)	Min	Typ	Max	Units
t_{PLH}	A_i or B_i to $\overline{E}_i$ and $\overline{ANYE}$	C_L = 50pF, R_L = 1kΩ		8	11	ns
t_{PHL}				8	11	
t_{PLH}	$\overline{G}$ to $\overline{E}_i$ and $\overline{ANYE}$			8	10	ns
t_{PHL}				8	10	
t_{PLH} (Note 1)	A_i or B_i to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω		9	12	ns
t_{PHL}				8	12	
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$			9	12	ns
t_{PHL}				7	11	
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$			9	12	ns
t_{PHL}				7	11	
t_{PLH}	S_i to $\overline{E}_i$	C_L = 50pf, R_L = 1kΩ		7	11	ns
t_{PHL}				7	11	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (See Figure 2)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	A_i or B_i to $\overline{E}_i$ and $\overline{ANYE}$	C_L = 50pF, R_L = 1kΩ		13		14	ns
t_{PHL}							
t_{PLH}	$\overline{G}$ to $\overline{E}_i$ and $\overline{ANYE}$			11		12	ns
t_{PHL}							
t_{PLH} (Note 1)	A_i or B_i to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω		14		15	ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$			13		14	ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$			13		14	ns
t_{PHL}							
t_{PLH}	S_i to $\overline{E}_i$	C_L = 50pF, R_L = 1kΩ		13		14	ns
t_{PHL}							

Note: 1. This propagation time is dependent on the RC time constant of the external load applied.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

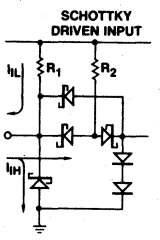
Parameters	Description	Test Conditions (See Figure 2)	Min	Typ	Max	Units
t_{PLH}	A_i or B_i to $\overline{E_{OUT}}$	C_L = 50pF, R_L = 1kΩ		8	11	ns
t_{PHL}				8	11	
t_{PLH}	$\overline{G}$ to $\overline{E_{OUT}}$			7	10	ns
t_{PHL}				7	10	
t_{PLH} (Note 1)	A_i or B_i to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω		9	12	ns
t_{PHL}				8	12	
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$			9	12	ns
t_{PHL}				7	11	
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$			7	12	ns
t_{PHL}				7	11	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

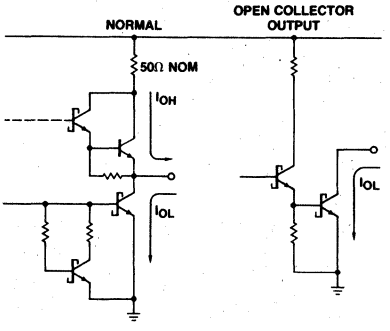
Parameters	Description	Test Conditions (See Figure 2)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	A_i or B_i to $\overline{E_{OUT}}$	C_L = 50pF, R_L = 1kΩ		13		14	ns
t_{PHL}							
t_{PLH}	$\overline{G}$ to $\overline{E_{OUT}}$			11		12	ns
t_{PHL}							
t_{PLH} (Note 1)	A_i or B_i to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω		14		15	ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$			13		14	ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$			13		14	ns
t_{PHL}							

Note 1. This propagation time is dependent on the RC time constant of the external load applied.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000020



IC000010

$C_i \approx 5.0$pF, all inputs
R_1* = 27k nominal
R_2 = 10k nominal
*Used only on B_i inputs.

Am29818

SSR™ Diagnostics/WCS Pipeline Register

DISTINCTIVE CHARACTERISTICS

- High-speed noninverting 8-bit parallel register for any data path or pipelining application
- WCS (Writable Control Store) pipeline register
  - Load WCS from serial register
  - Read WCS via serial scan
- Alternate sourced as SN54/74S818
- High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results

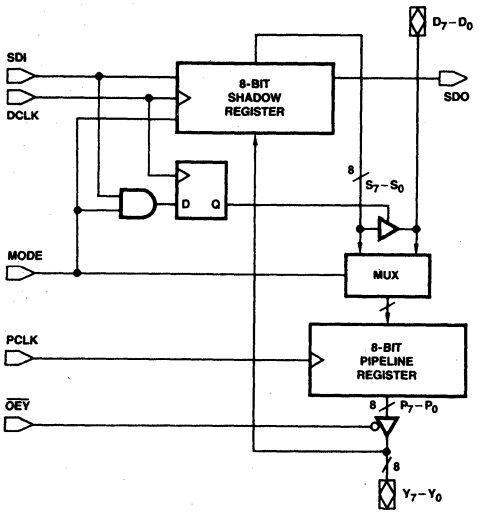
GENERAL DESCRIPTION

The Am29818 is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for *normal* system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a right-shift-only shift register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29818 Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM

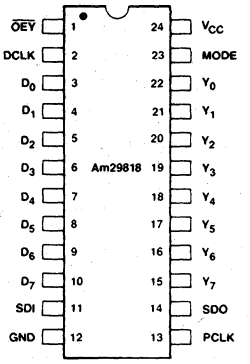


BD001020

03425C

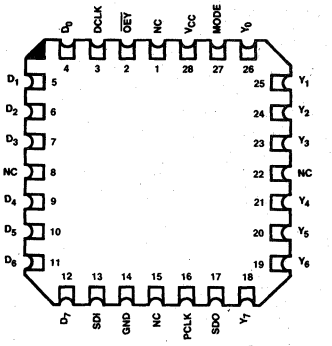
CONNECTION DIAGRAM
Top View

D-24-SLIM



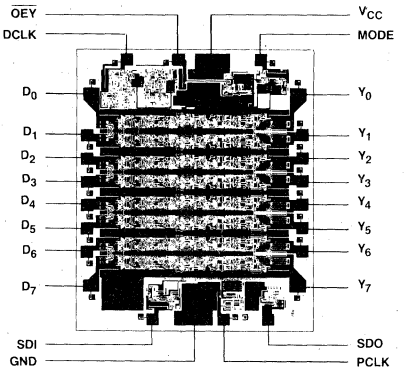
CD001100

CHIP PAK™ L-28-1



CD001160

METALLIZATION AND PAD LAYOUT
Am29818



DIE SIZE: .105 x .124

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29818 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 24-pin SLIMDIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X – Dice
- **Am29818** — Device type
  - SSR™ Diagnostics/WCS Pipeline Register

Valid Combinations	
Am29818	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip Pak is a trademark of Advanced Micro Devices, Inc.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
10 – 3	$D_7 - D_0$	I	Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).
2	DCLK	I	Diagnostics/WCS clock for loading shadow register (serial or parallel modes – see Function Table).
23	MODE	I	Control input for pipeline register multiplexer and shadow register control (see Function Table).
1	$\overline{OEY}$	I	Active LOW output enable for Y - port.
13	PCLK	I	Pipeline register clock input loads D - port or shadow register contents on LOW-to-HIGH transition.
11	SDI	I	Serial Data Input to shadow register. (See Function Table.)
14	SDO	O	Serial Data Output from shadow register.
15 – 22	$Y_7 - Y_0$	O	Data Outputs from the pipeline register and parallel inputs to the shadow register.

Am29818 FUNCTION TABLE DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no set-up or hold times are violated, this simultaneous operation is legal.

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$; $S_0 \leftarrow$ SDI	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	X	H	Hold*	NA	Hold Shadow Register; $S_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

FUNCTION TABLE DEFINITIONS

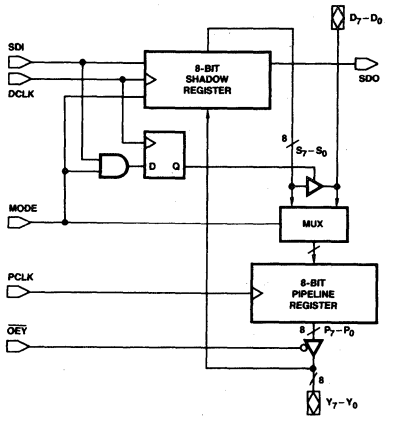
INPUTS

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition

OUTPUTS

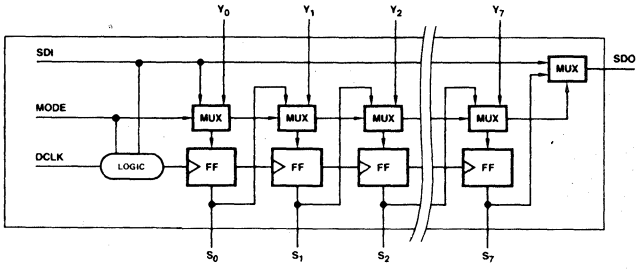
$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable output is not a function of the specified input combinations.

BLOCK DIAGRAM



BD001020

SHADOW REGISTER



DF000061

AN INTRODUCTION TO SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS

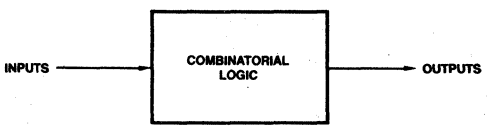
DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals - address, data, control and status - to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.

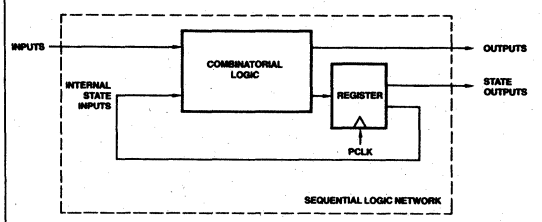
Figure 1.



DF000070

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

Figure 2.

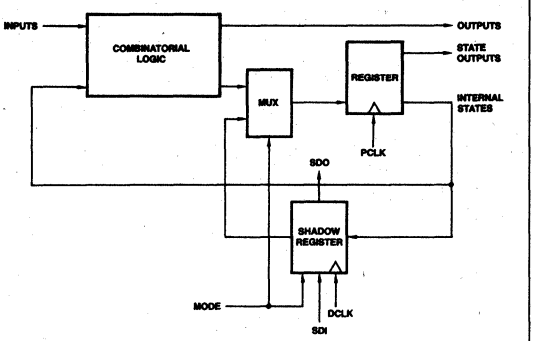


DF000080

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.

Figure 3.



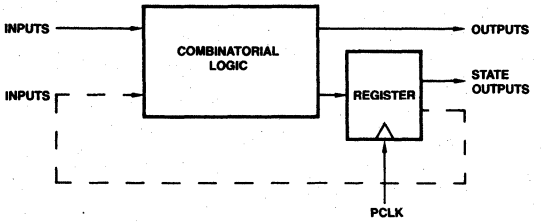
DF000040

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

Figure 4.



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Refer to Page 13-1 for Essential Information on Military Devices

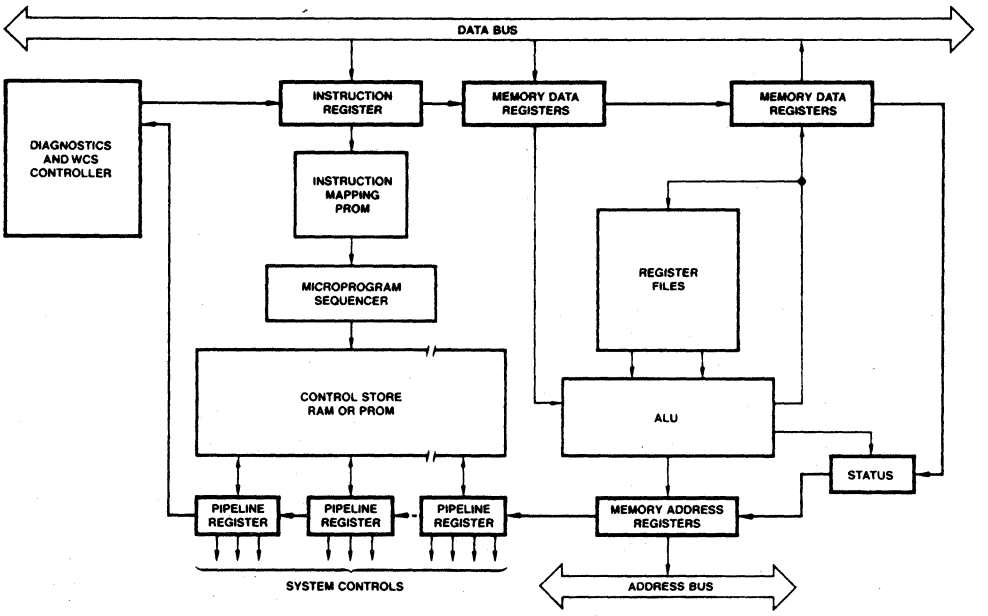
A TYPICAL COMPUTER ARCHITECTURE WITH SSR DIAGNOSTICS

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29818.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818s can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

Figure 5. Typical System Configuration



SSR DIAGNOSTICS/WCS PIPELINE REGISTERS
REPLACE NORMAL REGISTERS WITH DIAGNOSTICS LOOP

DF000030

USE OF THE Am29818 PIPELINE REGISTER IN WRITABLE CONTROL STORE (WCS) DESIGNS

The Am29818 SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29818 supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29818. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

CONCLUSION

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinational network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.

Figure 6. Am29818 Based WCS Application.

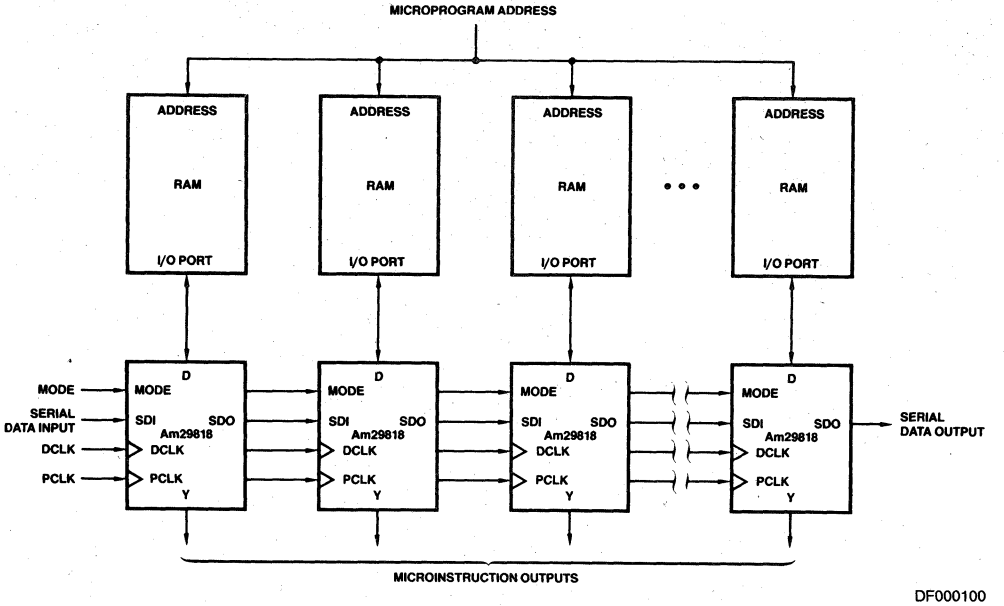


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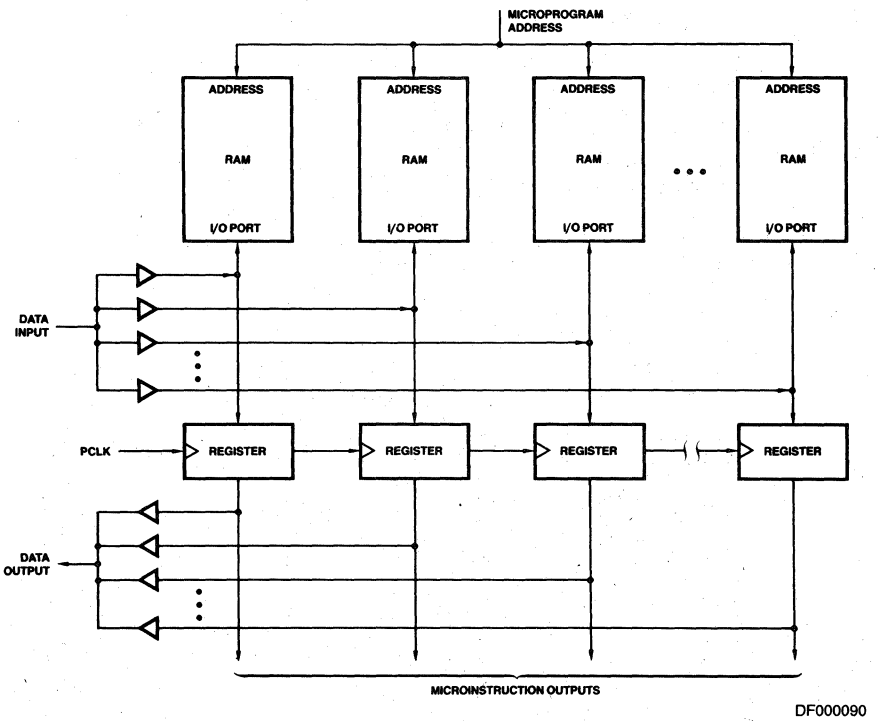
Figure 7. WCS Application without Am29818s.



DF000090

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 25mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

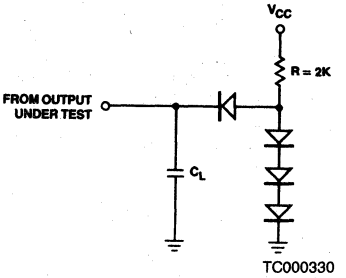
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$Y_0 - Y_7$: I_{OH} = −3mA $D_0 - D_7$, SDO: I_{OH} = −1mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$Y_0 - Y_7$: I_{OL} = 16mA (Mil) 24mA (Comm) $D_0 - D_7$, SDO: I_{OL} = 4mA (Mil), 8mA (Comm)			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs			2.0		
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	PCLK			−2.0	mA
			DCLK			−0.6	
			MODE, SDI, $\overline{OEY}$			−.45	
			$Y_0 - Y_7$, $D_0 - D_7$			−0.45	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V	DCLK, $\overline{OEY}$, MODE, SDI			50	µA
			PCLK, $Y_0 - Y_7$, $D_0 - D_7$			100	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−450	µA
			V_O = 2.4V			100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	$Y_0 - Y_7$	−30		−100	mA
			$D_0 - D_7$, SDO	−15		−50	
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	0 to +70°C		120	155	mA
			+70°C			140	
			−55 to +125°C		120	165	
			+125°C			130	

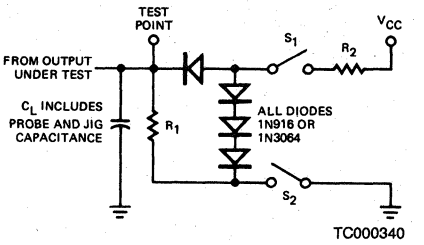
Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are TA = 25°C V_{CC} = 5.0V.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All three-state outputs are in the HIGH impedance state.

SWITCHING TEST CIRCUIT

SDO OUTPUT



THREE-STATE OUTPUTS



	R_1	R_2
$Y_0 - Y_7$	1K	280
$D_0 - D_7$	5K	2K

Note 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	PCLK → Y_X	See Test Output Load Conditions		13		18	ns
	MODE → SDO			16		18	ns
	SDI → SDO			16		18	ns
	DCLK → SDO			25		30	ns
t_S	D_X → PCLK		8		10		ns
	MODE → PCLK		15		15		ns
	Y_X → DCLK		5		5		ns
	MODE → DCLK		12		12		ns
	SDI → DCLK		10		12		ns
	DCLK → PCLK		15		15		ns
	DCLK → DCLK		40		45		ns
t_H	D_X → PCLK		2		2		ns
	MODE → PCLK		0		0		ns
	Y_X → DCLK		5		5		ns
	MODE → DCLK		2		5		ns
	SDI → DCLK		0		0		ns
t_{LZ}	$\overline{OEY}$ → Y_X			15		20	ns
	DCLK → D_X			45		45	ns
t_{HZ}	$\overline{OEY}$ → Y_X			25		30	ns
	DCLK → D_X			85		90	ns
t_{ZL}	$\overline{OEY}$ → Y_X			15		20	ns
	DCLK → D_X			30		35	ns
t_{ZH}	$\overline{OEY}$ → Y_X			15		20	ns
	DCLK → D_X			25		30	ns
t_{PW}	PCLK (HIGH and LOW)		15		15		ns
	DCLK (HIGH and LOW)		25		25		ns

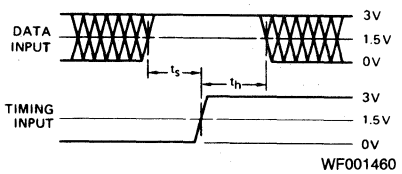
*AC performance over the operating range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PD}	PCLK → Y_X	See Test Output Load Conditions		10	12	ns
	MODE → SDO			10	14	ns
	SDI → SDO			10	14	ns
	DCLK → SDO			17	22	ns
t_S	D_X → PCLK		8			ns
	MODE → PCLK		12			ns
	Y_X → DCLK		5			ns
	MODE → DCLK		10			ns
	SDI → DCLK		10			ns
	DCLK → PCLK		12			ns
	DCLK → DCLK		35			ns
t_H	D_X → PCLK		0			ns
	MODE → PCLK		0			ns
	Y_X → DCLK		5			ns
	MODE → DCLK		0			ns
	SDI → DCLK		0			ns
t_{LZ}	$\overline{OEY}$ → Y_X				12	ns
	DCLK → D_X				37	ns
t_{HZ}	$\overline{OEY}$ → Y_X				22	ns
	DCLK → D_X				80	ns
t_{ZL}	$\overline{OEY}$ → Y_X				15	ns
	DCLK → D_X				25	ns
t_{ZH}	$\overline{OEY}$ → Y_X				15	ns
	DCLK → D_X				20	ns
t_{PW}	PCLK (HIGH and LOW)		15			ns
	DCLK (HIGH and LOW)		25			ns

SWITCHING WAVEFORMS

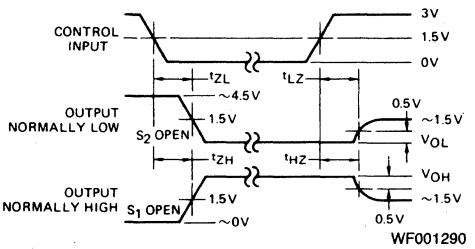
SET UP, HOLD, AND RELEASE TIMES



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

ENABLE AND DISABLE TIMES

Enable Disable

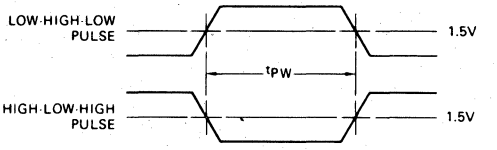


Notes: 1. Diagram shown for Input Control Enable-LOW and Input control Disable-HIGH.
2. S_1 and S_2 of load circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

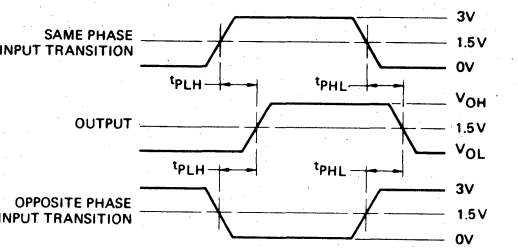
SWITCHING WAVEFORMS

PULSE WIDTH



WF001270

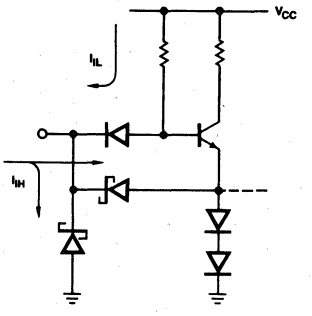
PROPAGATION DELAY



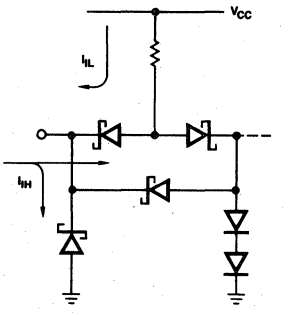
WF001420

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

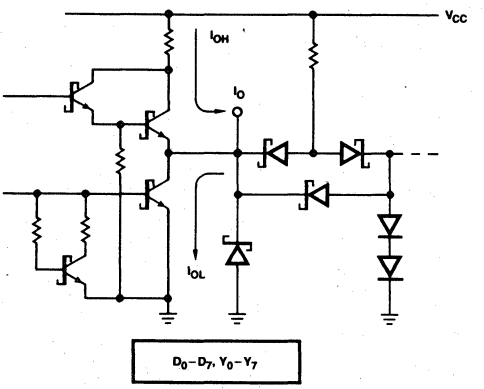
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



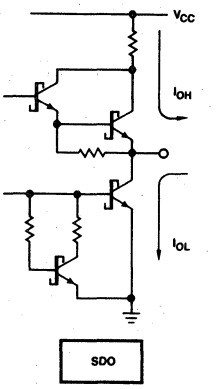
IC000030



IC000040



IC000050



IC000060

Am29821 – 26

High Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

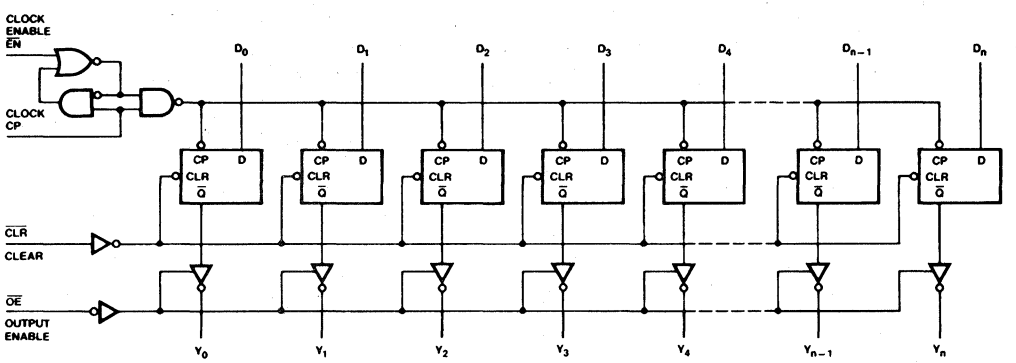
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Noninverting CP-Y t_{PD} = 7.5ns typ
  - Inverting CP-Y t_{PD} = 7.5ns typ
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down. Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- Metastable "Hardened" Registers

GENERAL DESCRIPTION

The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the AM29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM



BD001080

PRODUCT SELECTOR GUIDE

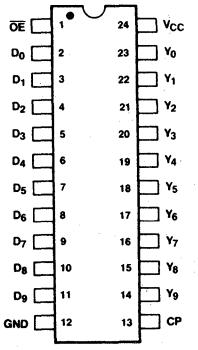
	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

01420C

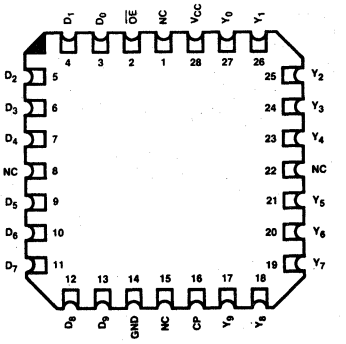
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

Am29821/Am29822 10-BIT REGISTERS

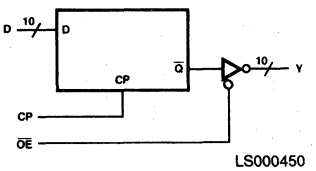


CD001360



CD001370

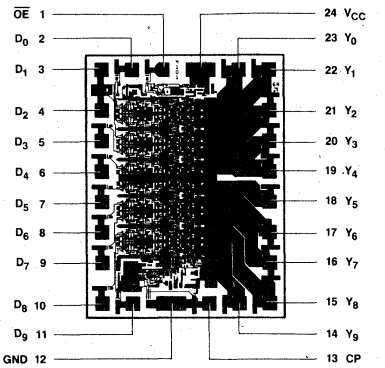
LOGIC SYMBOL



LS000450

METALLIZATION AND PAD LAYOUT

10-Bit Registers
Am29821*



DIE SIZE 0.084" x 0.064"
***Note: Am29822 is inverted**

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29821 – 26 D C B

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 24-pin SLIM DIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X – Dice
- **Am29821 – 26** — Device type
  - High Performance Bus Interface Registers

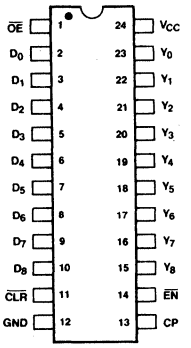
Valid Combinations	
Am29821 Am29822 Am29823 Am29824 Am29825 Am29826	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

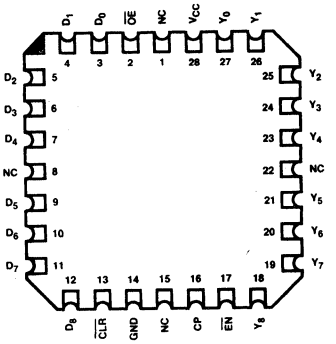
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CONNECTION DIAGRAM
Top View

Am29823/Am29824 9-BIT REGISTERS

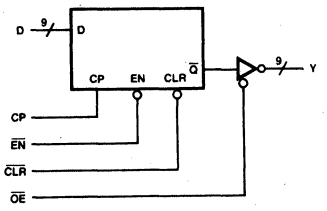


CD001220



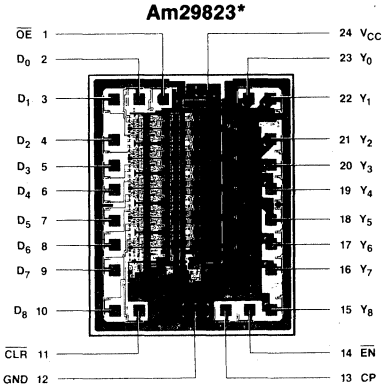
CD001230

LOGIC SYMBOL



LS000430

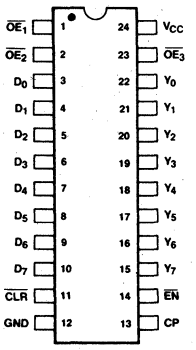
METALLIZATION AND PAD LAYOUT
9-Bit Registers
Am29823*



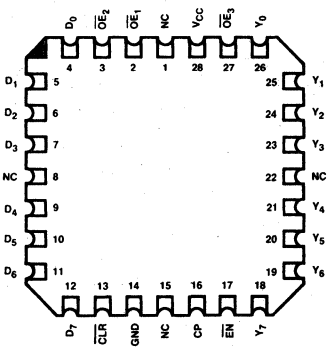
DIE SIZE 0.084" x 0.064"
***Note: Am29825 is inverted**

CONNECTION DIAGRAM
Top View

Am29825/Am29826 8-BIT REGISTERS

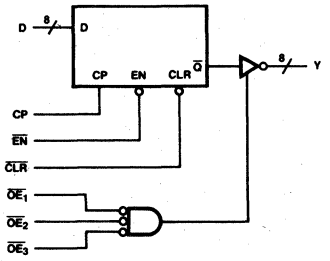


CD001200



CD001210

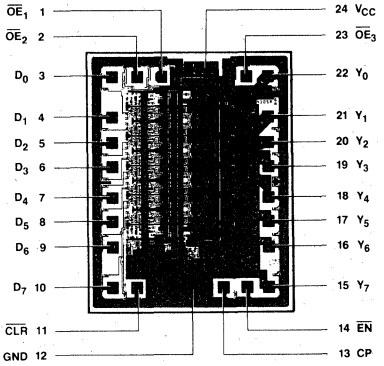
LOGIC SYMBOL



LS000420

METALLIZATION AND PAD LAYOUT

8-Bit Registers
Am29825*



DIE SIZE 0.084″ x 0.064″
***NOTE: m29826 is inverted**

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
11	$\overline{CLR}$	I	For both inverting and noninverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
13	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i, $\overline{Y_i}$	O	The register three-state outputs.
14	$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. (Note 5.)
	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

Note 5: The Am29823 thru Am29826 registers achieve short throughput delay and setup time and reduced power consumption by means of a clock gating and latching circuit. This circuit is sensitive to very short (< 3ns) HIGH-to-LOW-to-HIGH going spikes on $\overline{EN}$ while CP is HIGH. The designer should be aware of this and avoid the use of decoders or other potentially glitching devices in the $\overline{EN}$ logic.

FUNCTION TABLES

Am29821/29823/29825

Inputs					Internal Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	Function
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

Am29822/29824/29826

Inputs					Internal Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	$\overline{Y_i}$	Function
H	X	L	L	↑	H	Z	Hi-Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

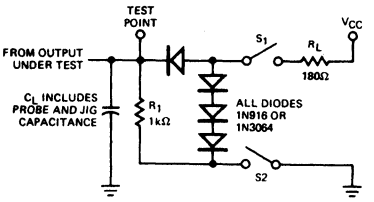
Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4	3.3		Volts
			I_{OH} = −24mA	2.0	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA		0.31	0.5	Volts
			COM'L, I_{OL} = 48mA		0.38	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−0.7	−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	Data, $\overline{CLR}$		−0.3	−1.0	mA
			$\overline{OE}$,$\overline{EN}$, CP		−1.2	−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Output Off-State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−75	−160	−250	mA
I_{CC}	Supply Current (Note 4)	V_{CC} = MAX, Outputs Open, $\overline{EN}$ = LOW	Over Temperature Range			140	mA
			+70°C			130	
			+125°C			120	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended Operating Range.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
4. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

01420C

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT



TC000350

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions (Note 4)	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF	3.5		8.5	ns
t_{PHL}				3.5		10.5	ns
t_{PLH}			C_L = 300pF			14	ns
t_{PHL}						18	ns
t_S	Data to $\overline{CP}$ Setup Time		C_L = 50pF	2.0	0		ns
t_H	Data to $\overline{CP}$ Hold Time			2.0	0.5		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time			3.0	1.5		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time			3.0	1.5		ns
t_H	Enable ($\overline{EN}$) Hold Time			0	−1.5		ns
t_{PHL}	Propagation Delay, Clear to Y_i				12.9	15.0	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time			5.0	1.1		ns
t_{PWH}	Clock Pulse Width	HIGH	C_L = 50pF	5.0	3.5		ns
t_{PWL}		LOW		5.0	3.0		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			5.0	4.0		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		C_L = 300pF			17	ns
t_{ZL}						21	ns
t_{ZH}			C_L = 50pF		11.5	12	ns
t_{ZL}					11.0	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌙ to Y_i		C_L = 50pF			9	ns
t_{LZ}						9	ns
t_{HZ}			C_L = 5pF		5.2	8	ns
t_{LZ}					5.5	8	ns

Note: 4. See test circuit and waveforms.

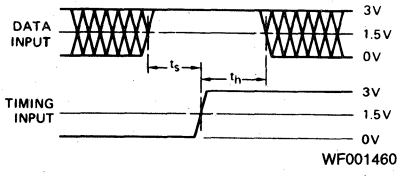
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditions (Note 4)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF	3.5	10	3.5	10	ns
t_{PHL}				3.5	12	3.5	12	ns
t_{PLH}			C_L = 300pF		16		16	ns
t_{PHL}					20		20	ns
t_S	Data to $\overline{CP}$ Setup Time		C_L = 50pF	4		4		ns
t_H	Data to $\overline{CP}$ Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ⎍) to CP Setup Time			4		4		ns
t_S	Enable ($\overline{EN}$ ⎎) to CP Setup Time			4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				20		20	ns
t_S	Clear Recovery ($\overline{CLR}$ ⎍) Time			7		7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		7		ns
t_{PWL}		LOW		7		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7		7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⎍ to Y_i		C_L = 300pF		20		22	ns
t_{ZL}					23		25	ns
t_{ZH}			C_L = 50pF		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⎎ to Y_i		C_L = 50pF		16		18	ns
t_{LZ}					12		12	ns
t_{HZ}			C_L = 5pF		9		10	ns
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

SWITCHING WAVEFORMS

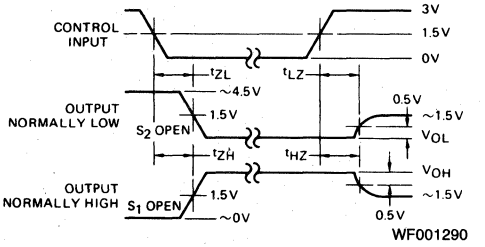
SET UP, HOLD, AND RELEASE TIMES



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

ENABLE AND DISABLE TIMES

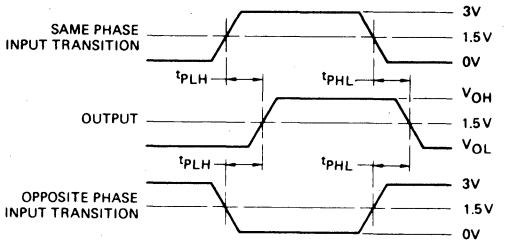
Enable **Disable**



Notes: 1. Diagram shown for input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

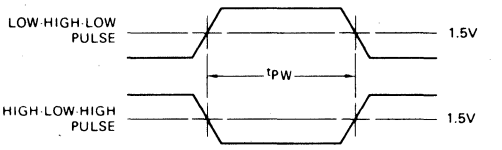
Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

PROPAGATION DELAY



WF001420

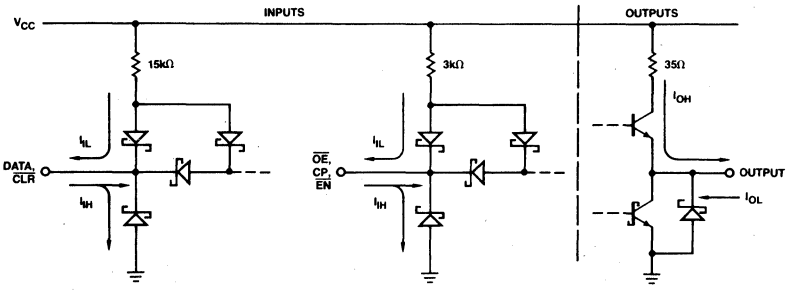
PULSE WIDTH



WF001270

Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000080

8

Am29827/Am29828

High Performance Buffers

DISTINCTIVE CHARACTERISTICS

- High-speed buffers and inverters
  - Noninverting t_{PD} = 5.0ns typ
  - Inverting t_{PD} = 4.5ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and -down. Outputs have Schottky clamp to ground
- 48mA commercial I_{OL}, 32mA military I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs

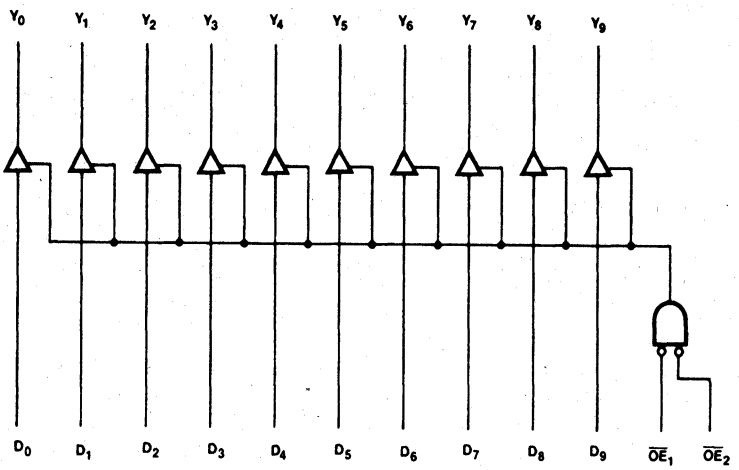
GENERAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

Am29827/Am29828 10-BIT BUFFERS



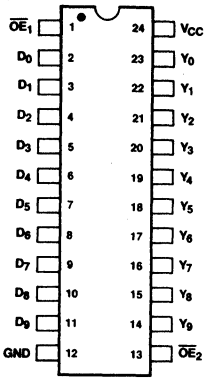
BD001090

IMOX is a trademark of Advanced Mirco Devices, Inc.

03371B

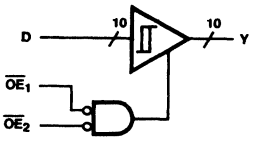
CONNECTION DIAGRAM
Top View

Am29827/Am29828 10-BIT BUS DRIVERS



CD001170

LOGIC SYMBOL



Am29827 (NONINVERTING)

LS000390

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29827
Am29828 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin SLIM DIP (D-24-SLIM)
  - L– 28-pin Leadless Chip Carrier (L-28-1)
  - X– Dice

Device type
High Performance Buffers

Valid Combinations	
Am29827 Am29828	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$\overline{OE}_i$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are HI-Z.
	D_i	I	10-bit data input.
	Y_i	O	10-bit data output.

FUNCTION TABLES

Am29827 (Noninverting)

Inputs		Outputs	
$\overline{OE}$	D_i	Y_i	Function
L	H	H	Transparent
L	L	L	Transparent
H	X	Z	HI-Z

Am29828 (Inverting)

Inputs		Outputs	
$\overline{OE}$	D_i	$\overline{Y}_i$	Function
L	H	L	Transparent
L	L	H	Transparent
H	X	Z	HI-Z

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −1.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
Output Current, into Outputs 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

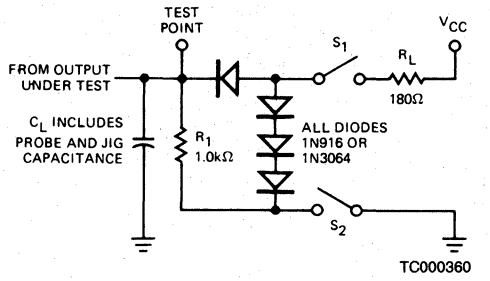
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4			V
			I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	V
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	V
V_{HYST}	Input Hysteresis	Output under test connected to Switching Test Circuit		200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX V_{IN} = 0.4V				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Output Off-State Output Current (HI-Z)	V_{CC} = MAX, V_O = 2.4V				50	μA
I_{OZL}	Output Off-State Output Current (HI-Z)	V_{CC} = MAX, V_O = 0.4V				−50	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX Outputs Open	Over Temperature Range			80	mA
			+70°C			75	
			+125°C			70	

Note: 1 Typical Units are V_{CC} = 5V, T_A = 25°C

8

SWITCHING TEST CIRCUIT



Note: Pulse Generator for All Pulses: Rate ≤ 10MHz;

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

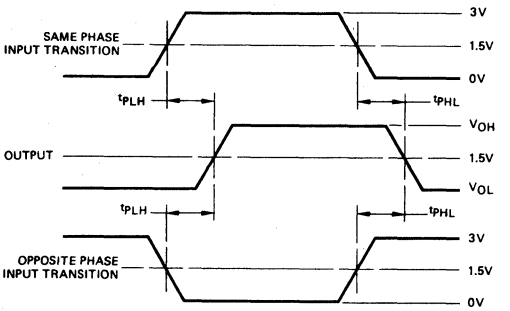
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	C_L = 50pF		4.8	6.0	ns
t_{PHL}				5.2	6.2	ns
t_{PLH}		C_L = 300pF		8.0	11	ns
t_{PHL}				10.8	13.2	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	C_L = 50pF		4.0	5.2	ns
t_{PHL}				4.9	5.9	ns
t_{PLH}		C_L = 300pF		7.3	10	ns
t_{PHL}				10.5	12.9	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	C_L = 50pF		6.5	12	ns
t_{ZL}				9.5	12	ns
t_{ZH}		C_L = 300pF		11	17	ns
t_{ZL}				18	21	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5pF		3.5	8.0	ns
t_{LZ}				3.5	8.0	ns
t_{HZ}		C_L = 50pF		11.2	16	ns
t_{LZ}				4.5	11	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	C_L = 50pF		8		10	ns
t_{PHL}				8		10	ns
t_{PLH}		C_L = 300pF		15		17	ns
t_{PHL}				15		17	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	C_L = 50pF		7.0		9.0	ns
t_{PHL}				7.5		9.5	ns
t_{PLH}		C_L = 300pF		14		16	ns
t_{PHL}				14		16	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	C_L = 50pF		15		17	ns
t_{ZL}				15		17	ns
t_{ZH}		C_L = 300pF		20		22	ns
t_{ZL}				23		25	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5pF		9		10	ns
t_{LZ}				9		10	ns
t_{HZ}		C_L = 50pF		17		19	ns
t_{LZ}				12		12	ns

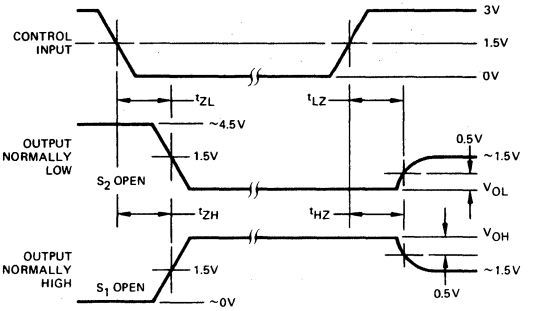
SWITCHING WAVEFORMS

PROPAGATION DELAY



ENABLE AND DISABLE TIMES

Enable Disable



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Am29833-34/Am29853-54

Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceiver for processor organized devices
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- Buffered direction three-state control
- Output short-circuit protected to V_{CC} limits
- 200mV minimum input hysteresis on input data ports
- High-capacitance drive capability
  48mA commercial I_{OL}
  32mA military I_{OL}

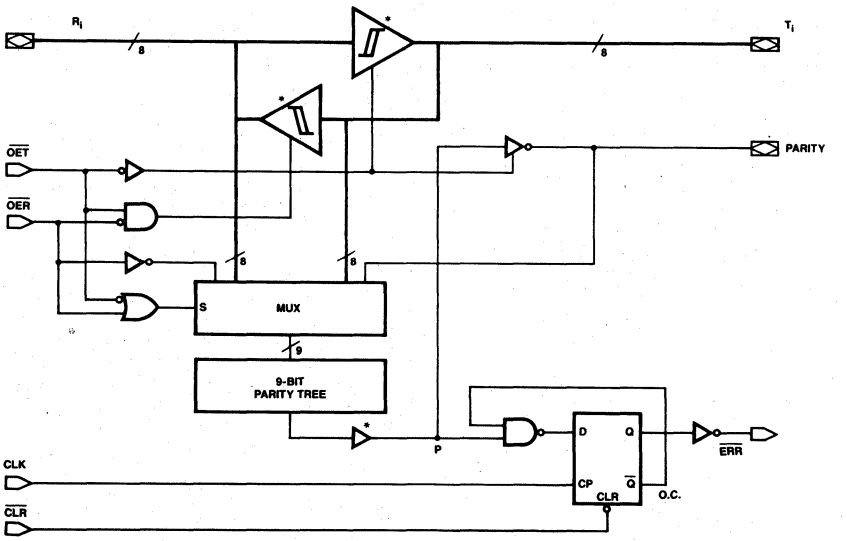
GENERAL DESCRIPTION

The Am29833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 9-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available. The Am29833/34 register option, and the Am29853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the open-collector $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

The output enables $\overline{OET}$ and $\overline{OER}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, the $\overline{OER}$ and $\overline{OET}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The Am29833 and Am29853 are noninverting, while the Am29834 and Am29854 present inverting data at the outputs. The devices are specified at 48mA output sink current over the commercial range and 32mA over the military range.

BLOCK DIAGRAM

Am29833
(Device Shown Noninverting)



BD001040

*Noninverting buffer for Am29833; inverting buffer for Am29834.

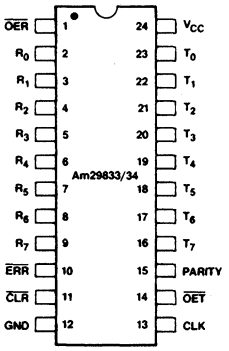
*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

00370B

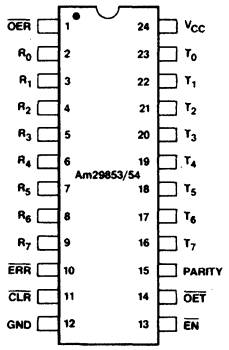
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

8-BIT TO 9-BIT PARITY TRANSCEIVERS



CD001120



CD001130

Leadless Chip Carrier

L-28-1

CD001110

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29833 – 34
Am29853 – 54 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin SLIM DIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X– Dice

Device type
Parity Bus Transceivers

Valid Combinations	
Am29833 Am29834 Am29853 Am29854	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

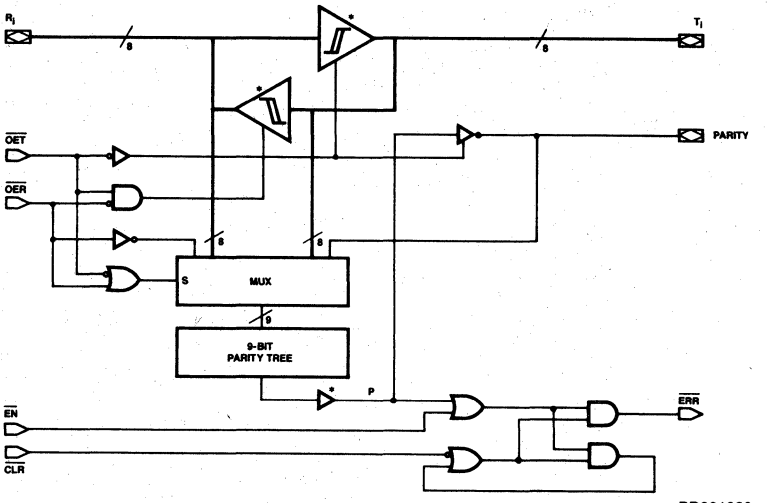
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29833 – 34			
1	$\overline{OER}$	I	RECEIVE enable input.
	R_i	O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains LOW until cleared.
11	$\overline{CLR}$	O	Clears the fault register output.
	T_i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	$\overline{OET}$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
Am29853/54			
1	$\overline{OER}$	I	RECEIVE enable input.
	R_i	O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared.
11	$\overline{CLR}$	O	Clears the fault latch output.
	T_i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	$\overline{OET}$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Enable latch input for fault flag.

BLOCK DIAGRAM
Am29853
(Device Shown Noninverting)



BD001030

*Noninverting buffer for Am29853; inverting buffer for Am29854.
*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

FUNCTION TABLES

Am29833 NONINVERTING OPTION

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of H's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port
L	H	–	–	H (Even)	NA	NA	H	H	NA	to T Port with parity,
L	H	–	–	L (Odd)	NA	NA	L	L	NA	receiving path is disabled
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port
H	L	H	↑	NA	H (Even)	H	NA	NA	L	to R Port with parity
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	test resulting in flag,
H	L	H	↑	NA	L (Even)	L	NA	NA	L	transmitting path is disabled
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and
H	H	L	–	–	–	Z	Z	Z	H	receiving paths are disabled.
H	H	H	↑	L (Odd)	–	Z	Z	Z	H	Parity logic defaults to
H	H	H	↑	H (Even)	–	Z	Z	Z	L	transmit mode
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29834 INVERTING OPTION*

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of L's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port
L	H	–	–	H (Even)	NA	NA	L	L	NA	to T Port with parity,
L	H	–	–	L (Odd)	NA	NA	H	H	NA	receiving path is disabled
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	H	Receive data from T Port
H	L	H	↑	NA	H (Even)	L	NA	NA	L	to R Port with parity
H	L	H	↑	NA	L (Odd)	H	NA	NA	H	test resulting in flag,
H	L	H	↑	NA	L (Even)	H	NA	NA	L	transmitting path is disabled
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and
H	H	L	–	–	–	Z	Z	Z	H	receiving paths are disabled.
H	H	H	↑	L (Odd)	–	Z	Z	Z	L	Parity logic defaults to
H	H	H	↑	L (Even)	–	Z	Z	Z	H	transmit mode
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
NC = No change
Z = High impedance
NA = Not applicable
– = Don't care or irrelevant
Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."
1. Output state assumes HIGH output pre-state.

ERROR FLAG OUTPUT TRUTH TABLE

Am29833 – Am29834 (REGISTER OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample*
H	↑	–	L	L	(1's
H	↑	L	–	L	Capture)
L	–	–	–	H	Clear

*Enable is used as strobe for the latch in sampled operation.

Am29853/Am29854 (LATCH OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample*
L	H	–	L	L	(1's
L	H	H	H	H	Capture)
H	L	–	–	H	Clear
H	H	–	L	L	Store*
H	H	–	H	H	

00370B

Refer to Page 13-1 for Essential Information on Military Devices

Am29853 NONINVERTING OPTION

Inputs						Outputs				Function
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of H's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	ERR_{n-1}	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29854 INVERTING OPTION*

Inputs						Outputs				Function
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of H's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	ERR_{n-1}	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	L (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance
NC = No change

NA = Not applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."
1. Output state assumes HIGH output pre-state.

00370B

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Output
for High Output State ..... −1.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage (Except ERR)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15mA	2.4			V
				I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN	ERR	I_{OL} = 48mA			0.5	V
			All Other Outputs V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL			0.5	
				I_{OL} = 48mA COM'L			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i	Output Connected to AC Test Load Circuit			200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		Data			−1.0	mA
				Control			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH}	Off-State Output Current (High Impedance)	V_{CC} = MAX		V_O = 2.4V			+100	μA
I_{OZL}				V_O = 0.4V			−1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX			75		250	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (All Outputs Are Open)		Over Temperature Range			195	mA
				+70°C			180	
				+125°C			170	

Note: 1 Typical units are TA = 25°C, V_{CC} = 5V.

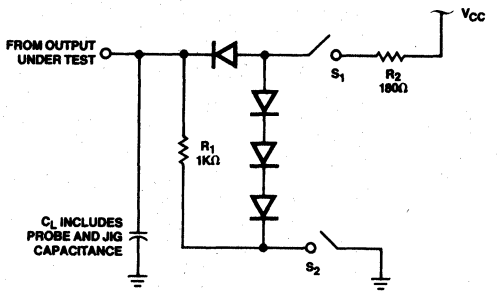
8

00370B

Refer to Page 13-1 for Essential Information on Military Devices

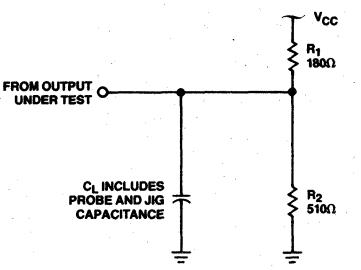
SWITCHING TEST CIRCUIT

CIRCUIT NO. 1



TC000380

CIRCUIT NO. 2



TC000370

Note: Test Circuit No. 1 is used with Propagation delay

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

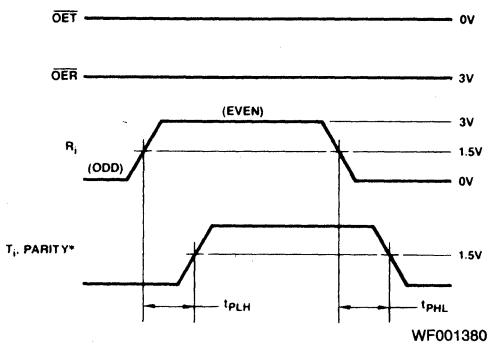
Parameters	Description		Test Conditions	Min	Type	Max	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		C_L = 50pF			12	ns
t_{PHL}						12	ns
t_{PLH}			C_L = 300pF			16	ns
t_{PHL}						16	ns
t_{PLH}	Propagation Delay R_i to PARITY		C_L = 50pF			15	ns
t_{PHL}						15	ns
t_{PLH}			C_L = 300pF			22	ns
t_{PHL}						22	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i		C_L = 50pF			15	ns
t_{ZL}						15	ns
t_{ZH}			C_L = 300pF			20	ns
t_{ZL}						23	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i		C_L = 5pF			9	ns
t_{LZ}						10	ns
t_{HZ}			C_L = 50pF			17	ns
t_{LZ}						12	ns
t_S	T_i, PARITY to CLK Setup Time*		C_L = 50pF	15			ns
t_H	T_i, PARITY to CLK Hold Time*			0			ns
t_S	Clear Recovery Time $\overline{CLR}$ to CLK**			15			ns
t_{PWH}	Clock Pulse Width*	HIGH		10			ns
t_{PWL}		LOW		10			ns
t_{PWL}	Clear Pulse Width	LOW		10			
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$*		C_L = 50pF			15	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		C_L = 50pF			15	ns
t_{PLH}	Propagation-Delay t_i, PARITY $\overline{ERR}$ (PASS Mode Only) Am29853/54		C_L = 50pF			22	ns
t_{PHL}						18	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity		C_L = 50pF Test Ckt #1			15	ns
t_{PHL}						15	ns
t_{PLH}			C_L = 300pFTest Ckt #1			22	ns
t_{PHL}						22	ns

*For Am29853/54 replace CLK with $\overline{EN}$.
**Note: Not applicable to Am29853/54.

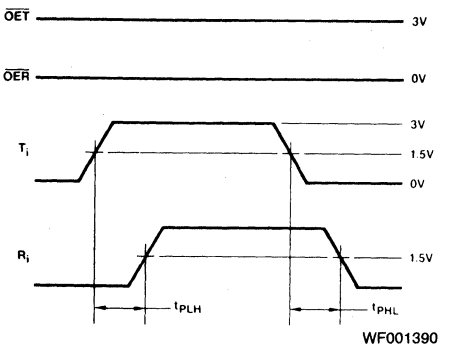
00370B

Refer to Page 13-1 for Essential Information on Military Devices

Am29833/53 SWITCHING WAVEFORMS (NONINVERTING OPTION)

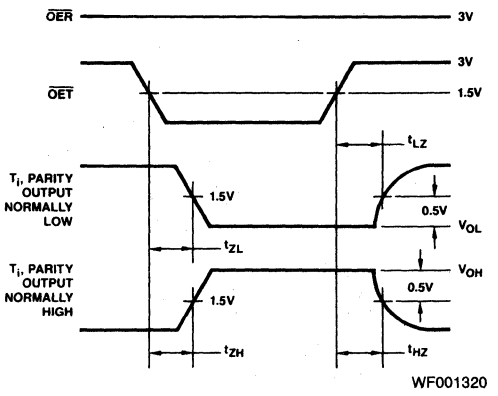


a. R_i to T_i, PARITY

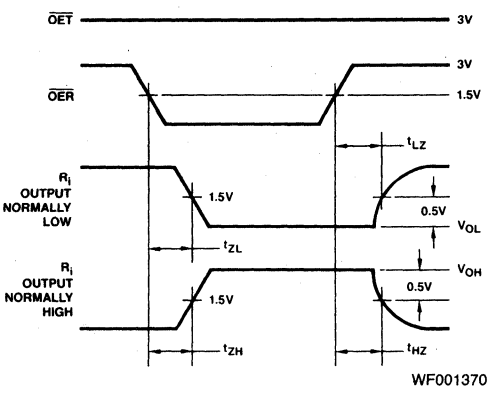


b. T_i to R_i

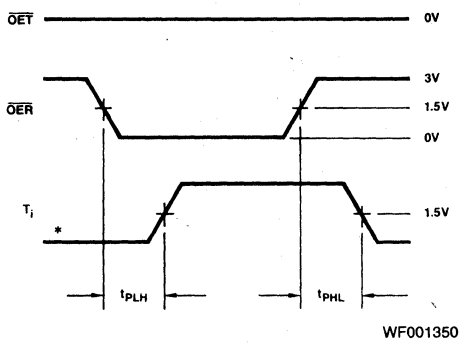
*Calculation must be done from last arriving signal.

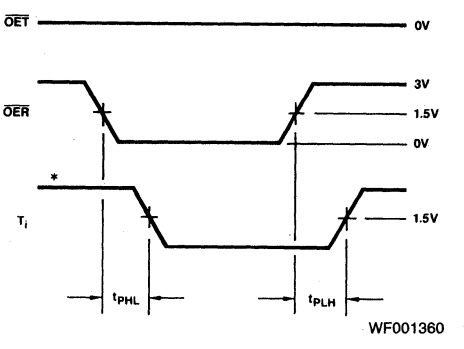


c. $\overline{OET}$ to T_i, PARITY



d. $\overline{OER}$ to R_i



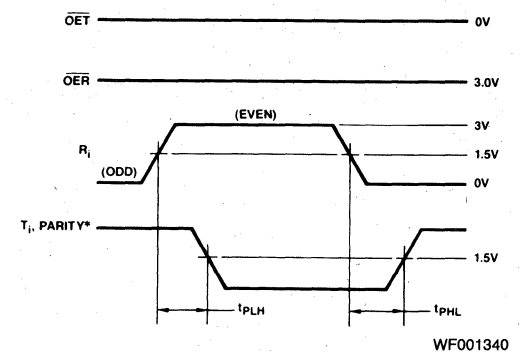


e. $\overline{OER}$ to PARITY

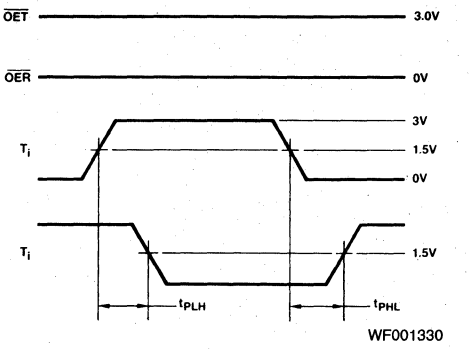
00370B

Refer to Page 13-1 for Essential Information on Military Devices

Am29834/54 SWITCHING WAVEFORMS (INVERTING OPTION)

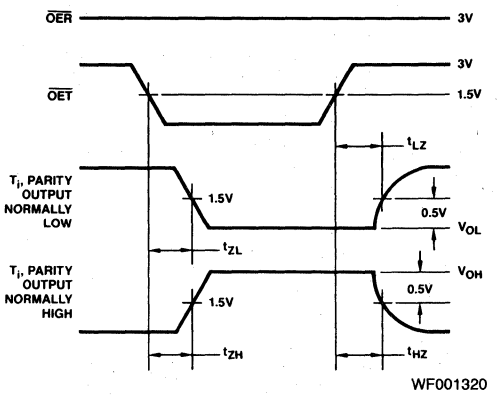


a. R_i to T_i, PARITY

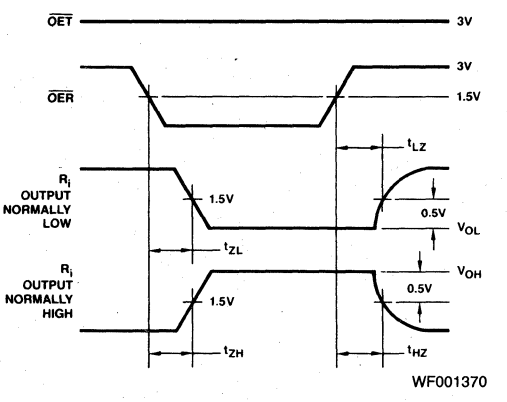


b. T_i to R_i

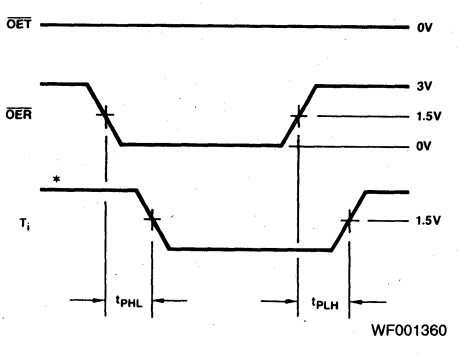
*Calculation must be done from last arriving signal.

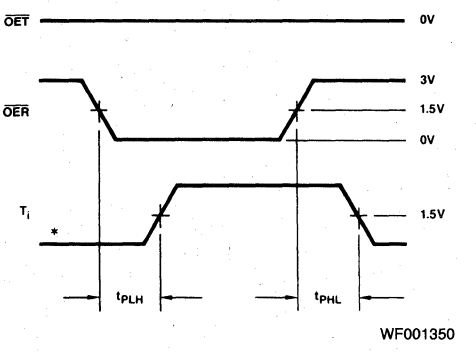


c. $\overline{OET}$ to T_i, PARITY



d. $\overline{OER}$ to R_i



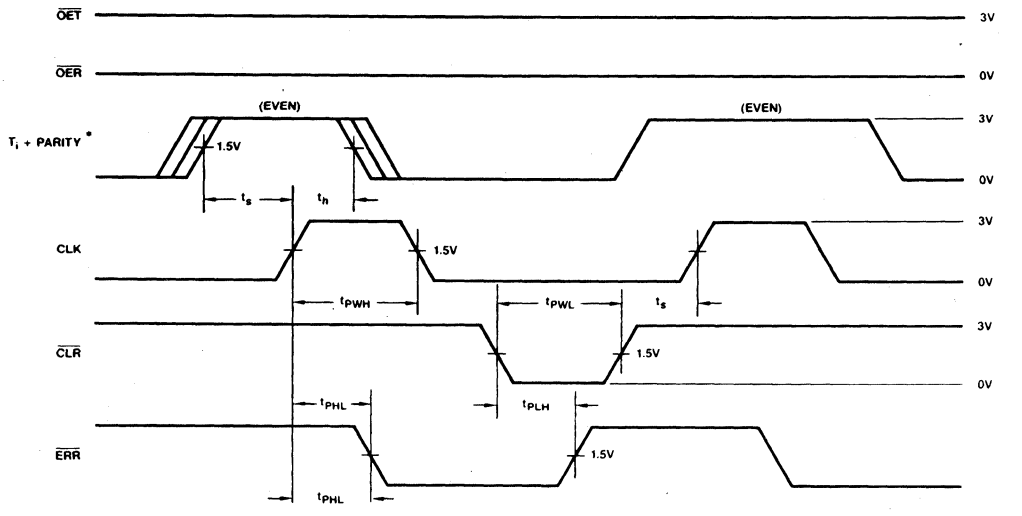


e. $\overline{OER}$ to PARITY

00370B

Refer to Page 13-1 for Essential Information on Military Devices

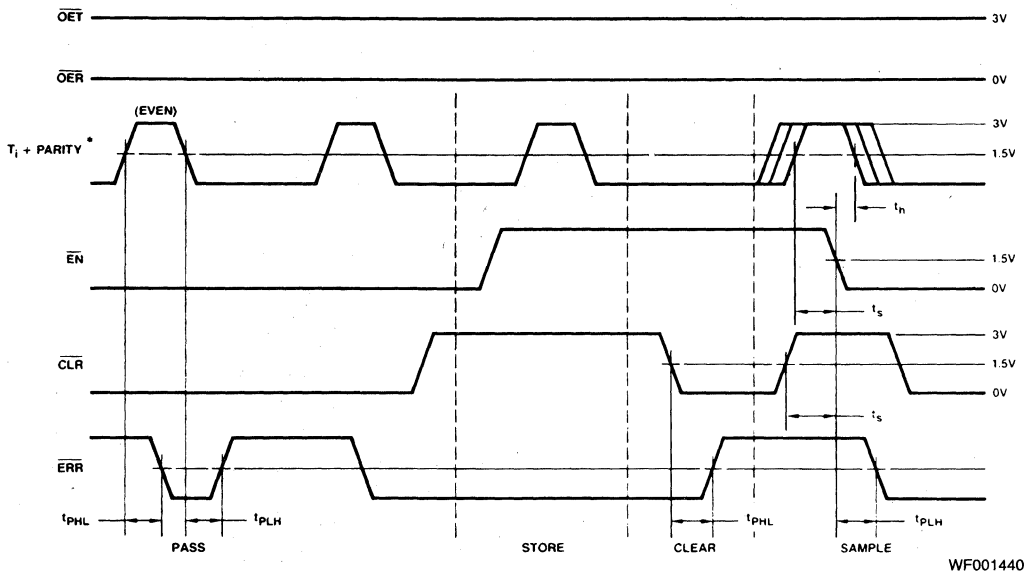
SWITCHING WAVEFORMS (REGISTER OPTION, Am29833/34)



WF001430

a. CLK, $\overline{CLR}$ to $\overline{ERR}$

SWITCHING WAVEFORMS (LATCH OPTION, Am29853/54)



WF001440

b. T_i, PARITY, $\overline{EN}$, $\overline{CLR}$ to $\overline{ERR}$

*Calculation must be done from last arriving signal.

00370B

Refer to Page 13-1 for Essential Information on Military Devices

Am29841 – 46

High Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 5.25ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- I_{OH} specified 2.0V and 2.4V

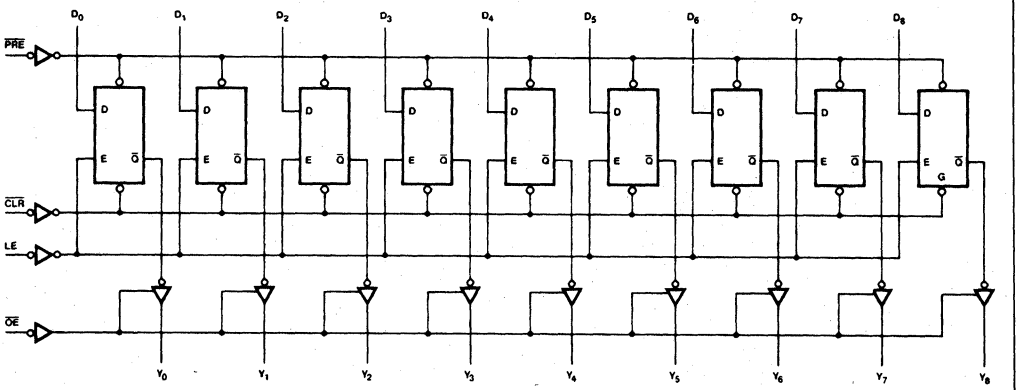
GENERAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide versions of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family products are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

Am29843



BD001050

PRODUCT SELECTOR GUIDE

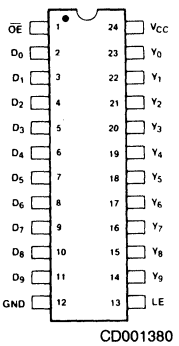
	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

01972C

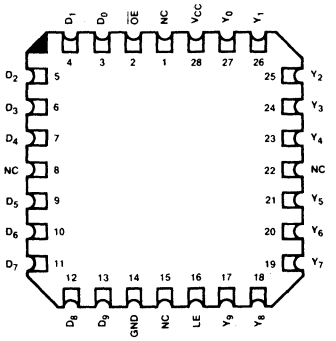
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

Am29841/Am29842 10-BIT LATCHES

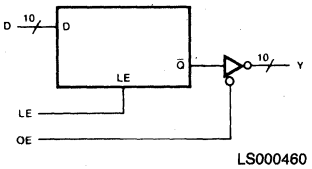


CD001380



CD001390

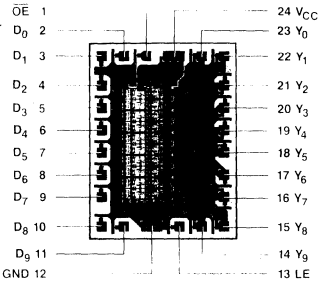
LOGIC SYMBOL



LS000460

METALLIZATION AND PAD LAYOUT

Am29841*
10-Bit Latches



DIE SIZE 0.084″ x 0.064″
Note: the Am29842 is inverted

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29841 – 46 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 24-pin SLIM DIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X – Dice
- Am29841 – 46 — Device type
  - High Performance Bus Interface Latches

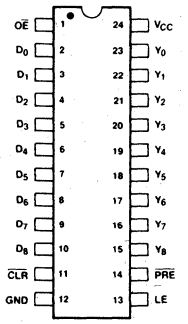
Valid Combinations	
Am29841 Am29842 Am29843 Am29844 Am29845 Am29846	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

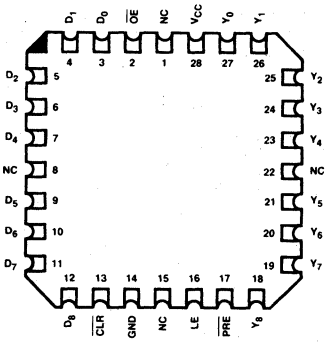
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CONNECTION DIAGRAM
Top View

Am29843/Am29844 9-BIT LATCHES

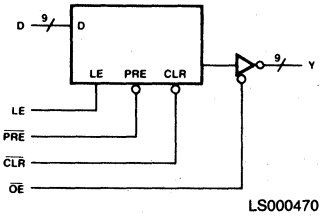


CD001400



CD001410

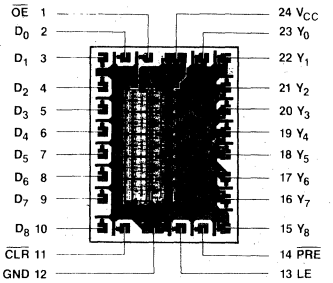
LOGIC SYMBOL



LS000470

METALLIZATION AND PAD LAYOUT

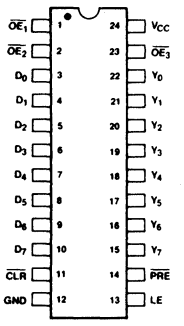
Am29843*
9-Bit Latches



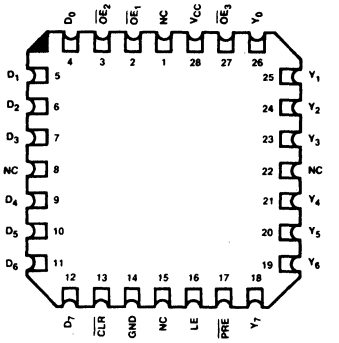
DIE SIZE 0.084" x 0.064"
Note: the Am29844 is inverted

CONNECTION DIAGRAM
Top View

Am29845/Am29846 8-BIT LATCHES

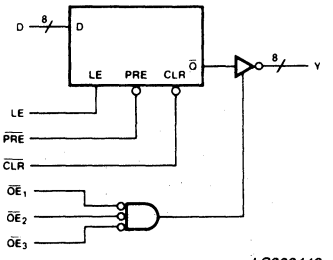


CD001340



CD001350

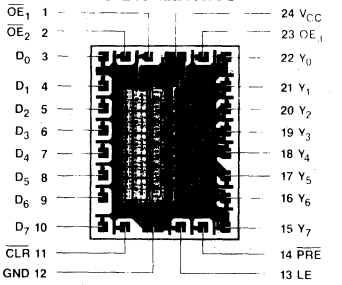
LOGIC SYMBOL



LS000440

METALLIZATION AND PAD LAYOUT

Am29845*
8-Bit Latches



DIE SIZE 0.084" x 0.064"
Note: the Am29846 is inverted

8

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29841/43/45 (Noninverting)			
11	$\overline{CLR}$	I	When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
	D_i	I	The latch data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y_i	O	The 3-state latch outputs.
1	$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.
14	$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
Am29842/44/46 (Inverting)			
11	$\overline{CLR}$	I	When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
	D_i	I	The latch inverting data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y_i	O	The 3-state latch outputs.
1	$\overline{OE}$	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.
14	$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

29841/43/45 (Noninverting)

Inputs					Internal Outputs		
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

29842/44/46 (Inverting)

Inputs					Internal Outputs		
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to V_{CC} max
DC input voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 100mA
DC input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

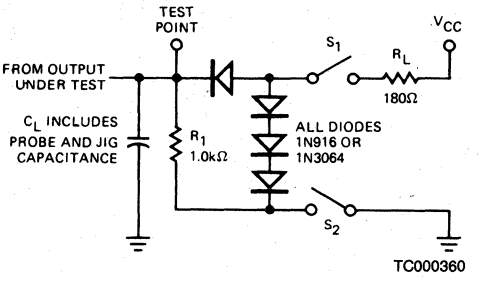
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4	3.3		Volts
			I_{OH} = −24mA	2.0	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	Volts
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−1.0.	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Output Off-State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current[3]	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs Open	Over Temperature Range			120	mA
			+70			110	
			+125°C			100	

Notes: 1. All typical values are T_A = 25°C, V_{CC} = 5.0V.
2. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING TEST CIRCUIT



SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditions (Note 4)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50pF	3.5	9.5	3.5	11	ns
t_{PHL}				3.5	9.5	3.5	11	ns
t_{PLH}			C_L = 300pF		12.5		14	ns
t_{PHL}					13		15	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		3		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\overline{Y_i}$) (LE = HIGH)		C_L = 50pF	3.5	10		12	ns
t_{PHL}				3.5	10		12	ns
t_{PLH}			C_L = 300pF		12.5		14	ns
t_{PHL}					13		15	ns
t_{PLH}	Data to LE Setup Time		C_L = 50pF	2.5		2.5		ns
t_{PHL}	Data to LE Hold Time			2.5		3		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50pF		12		16	ns
t_{PHL}					12		16	ns
t_{PLH}			C_L = 300pF		16		20	ns
t_{PHL}					16		20	ns
			C_L = 50pF					ns
								ns
t_{PLH}	Propagation Delay, Preset to Y_i				12		14	ns
t_S	Preset Recovery (PRE ↓) Time				14		17	ns
t_{PHL}	Propagation Delay, Clear to Y_i				21		23	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				14		17	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF	6		6		ns
t_{PWL}	Preset Pulse Width	LOW		8		9		ns
t_{PWL}	Clear Pulse Width	LOW		8		9		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		C_L = 300pF		20		22	ns
t_{ZL}					23		25	ns
t_{ZH}			C_L = 50pF		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		C_L = 50pF		15		15	ns
t_{LZ}					12		12	ns
t_{HZ}			C_L = 5pF		9		10	ns
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

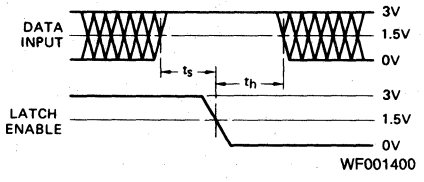
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions (Note 4)	Min	Typ	Max	Units
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50pF	3.5	5.7	8	ns
t_{PHL}				3.5	6.2	8	ns
t_{PLH}			C_L = 300pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.0	−0.2		ns
t_H	Data to LE Hold Time			2.5	0.7		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\overline{Y_i}$) (LE = HIGH)		C_L = 50pF	3.5	6.2	8.5	ns
t_{PHL}				3.5	6.5	8.5	ns
t_{PLH}			C_L = 300pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.5	0.3		ns
t_H	Data to LE Hold Time			2.5	0.2		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50pF		8	10.5	ns
t_{PHL}					7.5	10	ns
t_{PLH}			C_L = 300pF			15	ns
t_{PHL}						15	ns
			C_L = 50pF				ns
							ns
t_{PLH}	Propagation Delay, Preset to Y_i				6.5	9	ns
t_S	Preset Recovery ($\overline{PRE}$ ↑) Time				7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i				15	18	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				7.8	12	ns
t_{PWH}	LE Pulse Width.	HIGH	C_L = 50pF	4	2.5		ns
t_{PWL}	Preset Pulse Width	LOW		5			ns
t_{PWL}	Clear Pulse Width	LOW		6			ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		C_L = 300pF			17	ns
t_{ZL}						21	ns
t_{ZH}			C_L = 50pF		7.3	12	ns
t_{ZL}					9.7	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		C_L = 50pF		10.4	14	ns
t_{LZ}					4.7	11	ns
t_{HZ}			C_L = 5pF (Note 5)		3.4	8	ns
t_{LZ}					3.8	8	ns

Note: 4. See test circuit and waveforms.
5. Not tested.

SWITCHING WAVEFORMS

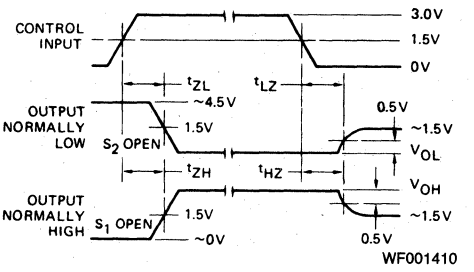
SET UP, HOLD, AND RELEASE TIMES



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

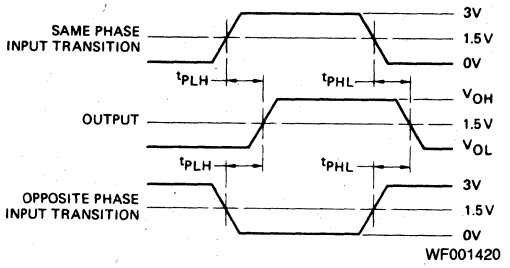
ENABLE AND DISABLE TIMES

Enable **Disable**

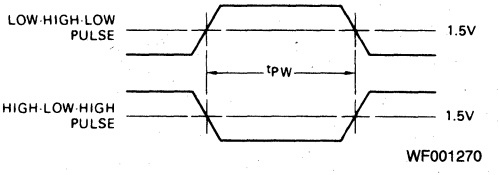


Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

PROPAGATION DELAY

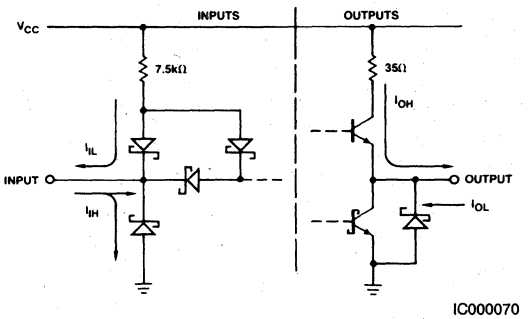


PULSE WIDTH



Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Am29861 - 64

High Performance Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed symmetrical bidirectional transceivers
  - Noninverting t_{PD} = 5.0ns typ
  - Inverting t_{PD} = 4.5ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- 48mA commercial I_{OL}, 32mA military I_{OL}
- Low input/output capacitance
- I_{OH} specified 2.0V and 2.4V

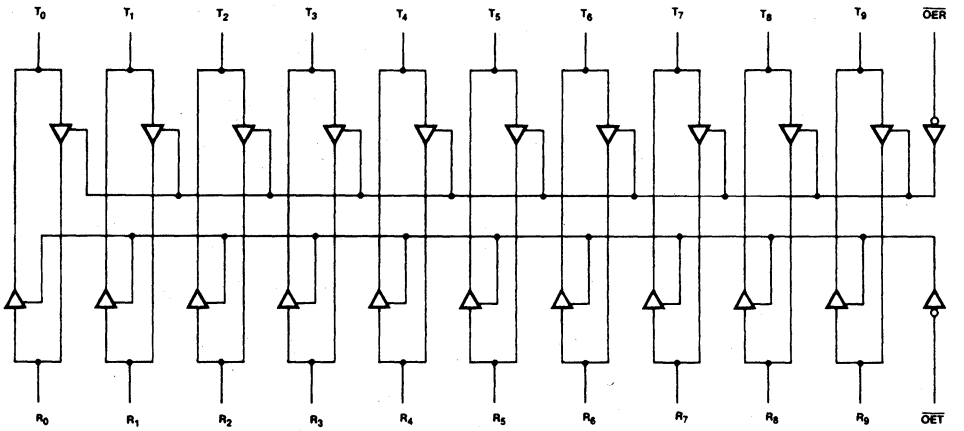
GENERAL DESCRIPTION

The Am29860 Series bus transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The Am29863/64 9-bit transceivers have NOR-ed output enables for maximum control flexibility. All transceiver data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

Am29861/Am29862 10-BIT TRANSCEIVERS



BD001060

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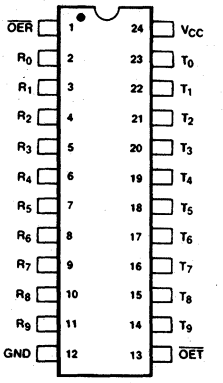
03369B

Refer to Page 13-1 for Essential Information on Military Devices

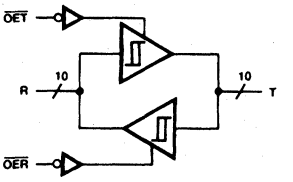
CONNECTION DIAGRAM
Top View

Am29861/Am29862 10-BIT TRANSCEIVERS



CD001150

LOGIC SYMBOL



Am29861 (NONINVERTING)

LS000370

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29861 - 64 D C B

- Screening Option
  - Blank – Standard processing
  - B – Burn-in
- Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 24-pin SLIM DIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X – Dice
- Device type
  - High Performance Bus Transceiver

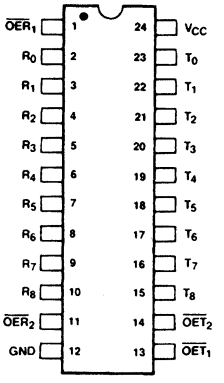
Valid Combinations	
Am29861 Am29862 Am29863 Am29864	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

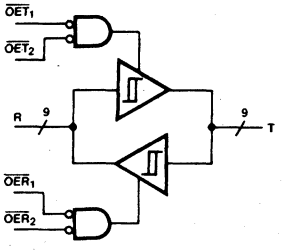
CONNECTION DIAGRAM
Top View

Am29863/Am29864 9-BIT TRANSCEIVERS



CD001140

LOGIC SYMBOL



Am29863 (NONINVERTING)

LS000380

8

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29861/Am29862			
1	$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
13	$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
	R_i	I/O	10-bit RECEIVE input/output.
	T_i	I/O	10-bit TRANSMIT input/output.
Am29863/Am29864			
	$\overline{OER_i}$	I	When both are LOW in conjunction with any $\overline{OET_i}$ HIGH indicates the RECEIVE mode.
	OET_i	I	When both are LOW in conjunction with any $\overline{OER_i}$ HIGH indicates the TRANSMIT mode.
	R_i	I/O	9-bit RECEIVE input/output.
	T_i	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES

Am29861/Am2983 (Noninverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

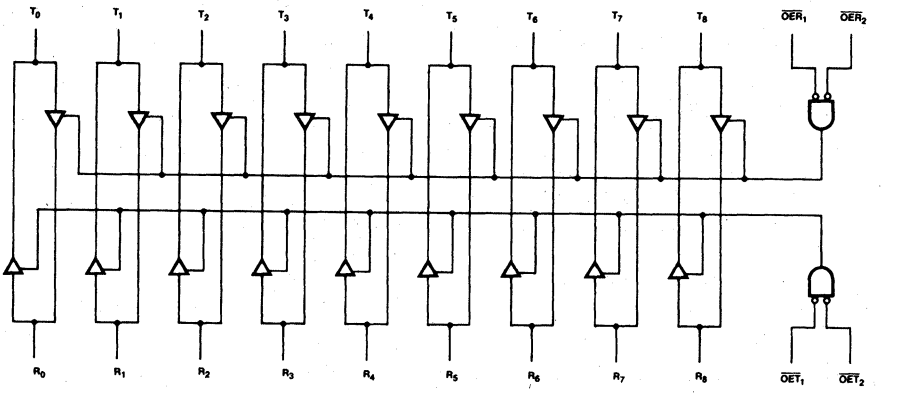
Am29862/Am29864 (Inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	$\overline{T_i}$	R_i	$\overline{T_i}$	Function
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance

X = Don't Care
N/A = Not Applicable

Am29863/Am29864
9-BIT TRANSCEIVERS



BD001070

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Output
for High Output State ..... −1.5V to V_{CC} max
DC Input voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

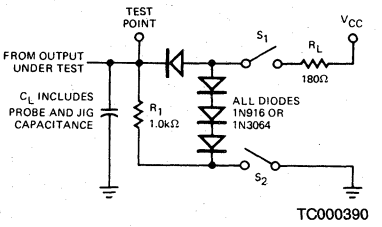
Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4			V
			I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	V
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	V
V_{HYST}	Input Hysteresis	Tested output is connected to AC load test circuit		200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−1.0.	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Output Off-State Output Current (HI-Z)	V_{CC} = MAX, V_O = 2.4V				50	μA
I_{OZL}	Output Off-State Output Current (HI-Z)	V_{CC} = MAX, V_O = 0.4V				−1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs Open	Over Temperature Range			160	mA
			+70°C			150	
			+125°C			140	

SWITCHING TEST CIRCUIT



Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861/Am29863 (Noninverting)	$C_L = 50pF$		4.8	6.0	ns
t_{PHL}				5.2	6.2	ns
t_{PLH}		$C_L = 300pF$		8	11	ns
t_{PHL}				11	14	ns
t_{PLH}	Propagation Delay from R_i to $\overline{T_i}$ or $\overline{T_i}$ to R_i Am29862/Am29864 (Inverting)	$C_L = 50pF$		4.0	5.2	ns
t_{PHL}				4.9	5.9	ns
t_{PLH}		$C_L = 300pF$		7.3	10	ns
t_{PHL}				10.5	12.9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i and $\overline{OER}$ to R_i	$C_L = 50pF$		6.5	12	ns
t_{ZL}				9.5	12	ns
t_{ZH}		$C_L = 300pF$		11	17	ns
t_{ZL}				17	21	ns
t_{HZ}	Output Disable Time OET to T_i and OER to R_i	$C_L = 5pF$		3.5	8.0	ns
t_{LZ}				3.5	8.0	ns
t_{HZ}		$C_L = 50pF$		11.2	16	ns
t_{LZ}				4.5	9.0	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

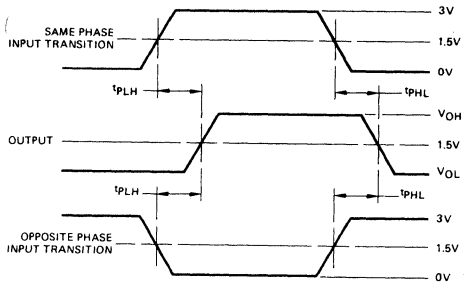
Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861/Am29863 (Noninverting)	$C_L = 50pF$		8		10	ns
t_{PHL}				8		10	ns
t_{PLH}		$C_L = 300pF$		15		17	ns
t_{PHL}				15		17	ns
t_{PLH}	Propagation Delay from R_i to $\overline{T_i}$ or $\overline{T_i}$ to R_i Am29862/Am29864 (Inverting)	$C_L = 50pF$		7.0		9.0	ns
t_{PHL}				7.5		9.5	ns
t_{PLH}		$C_L = 300pF$		14		16	ns
t_{PHL}				14		16	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	$C_L = 50pF$		15		17	ns
t_{ZL}				15		17	ns
t_{ZH}		$C_L = 300pF$		20		22	ns
t_{ZL}				23		25	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	$C_L = 5pF$		9		10	ns
t_{LZ}				9		10	ns
t_{HZ}		$C_L = 50pF$		17		19	ns
t_{LZ}				12		12	ns

03369B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS

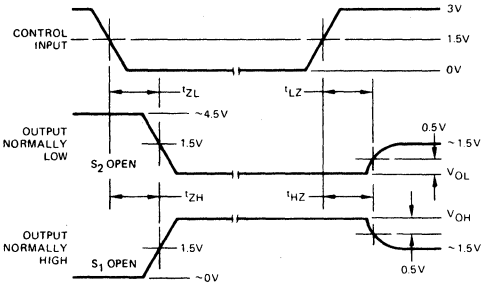
PROPAGATION DELAY



WF001470

ENABLE AND DISABLE TIMES

Enable **Disable**



WF001450

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

8

Am25S and Am25LS Logic Family Index

Am25S05

Four-Bit by Two-Bit Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.

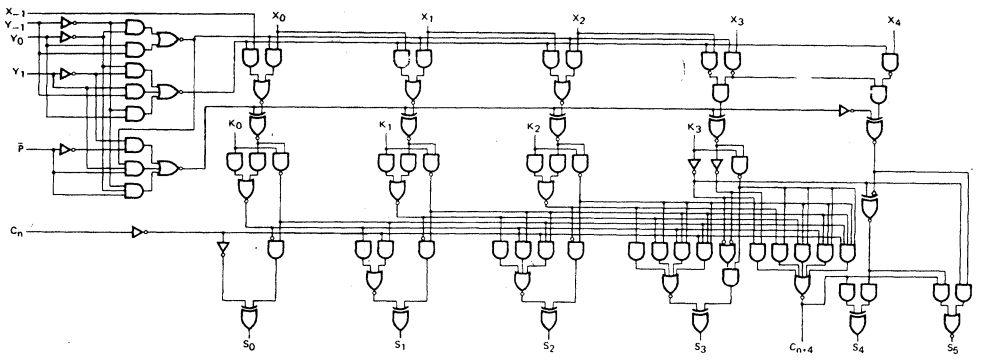
GENERAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m + n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

BLOCK DIAGRAM



BD001580

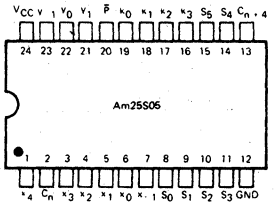
RELATED PRODUCTS

Part No.	Description
Am25LS14A	8-Bit Serial/Parallel Multiplier
Am25LS557/8	8-Bit by 8-Bit Multiplier
Am29516/7	16-Bit by 16-Bit Multiplier

03610B

Refer to Page 13-1 for Essential Information on Military Devices

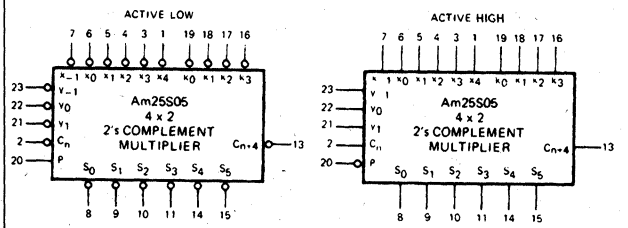
CONNECTION DIAGRAM
Top View



CD002010

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000700

METALLIZATION AND PAD LAYOUT

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S05 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 24-pin CERDIP
  - F – 24-pin flatpak
  - P – 24-pin plastic DIP
  - X – Dice
- **Am25S05** — Device type
  - 4-Bit by 2-Bit Multiplier

Valid Combinations	
Am25S05	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.
I Input.
L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.
O Output.

FUNCTIONAL TERMS:

C_n The carry input to the high-speed adder.
C_{n+4} The carry output from the high-speed adder.
K_i The constant field used for accumulating partial products. i = 0, 1, 2, 3. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.
$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.
S_i The product outputs. i = 0, 1, 2, 3, 4, 5.
x_i The multiplicand inputs. i = −1, 0, 1, 2, 3, 4. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.
Y_i The multiplier inputs. i = −1, 0, 1.
At the first row of the array Y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.
I_{OH} Output HIGH current, forced out of output in V_{OH} test.
I_{OL} Output LOW current, forced into the output in V_{OL} test.
I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.
I_{IH} Reverse input load current.
Negative Current Current flowing out of the device.
Positive Current Current flowing into the device.
V_{IH} Minimum logic HIGH input voltage.
V_{IL} Maximum logic LOW input voltage.
V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.
V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.
V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load	
	HIGH	LOW
Advanced Micro Devices 54/7400 Series	1.25	1.25
Advanced Micro Devices 9300/2500 Series	1.25	1.25
FSC Series 9300	1.25	1.25
TI Series 54/7400	1.25	1.25
Signetics Series 8200	2.5	2.5
National Series DM 75/85	1.25	1.25
DTL Series 930	15	1.25

OPERATION TABLE

Y Multiplier			Operation X Multiplicand
Y_{-1}	Y_0	Y_1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K − 2X
1	0	1	K − X
0	1	1	K − X
1	1	1	K − 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

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Am25S05 LOADING RULES IN UNIT LOADS

Input/Output	Pin Nos.	Input Unit Load		Fan-out	
		Input HIGH	Input LOW	Output HIGH	Output LOW
x_4	1	0.2	0.2	–	–
C_n	2	0.2	0.2	–	–
x_3	3	0.2	0.2	–	–
x_2	4	0.4	0.4	–	–
x_1	5	0.4	0.4	–	–
x_0	6	0.4	0.4	–	–
x_{-1}	7	0.2	0.2	–	–
S_0	8	–	–	20	10
S_1	9	–	–	20	10
S_2	10	–	–	20	10
S_3	11	–	–	20	10
GND	12	–	–	–	–
C_{n+4}	13	–	–	20	10
S_4	14	–	–	20	10
S_5	15	–	–	20	10
k_3	16	2	2	–	–
k_2	17	2	2	–	–
k_1	18	2	2	–	–
k_0	19	2	2	–	–
$\overline{P}$	20	1	1	–	–
y_1	21	0.6	0.6	–	–
y_0	22	0.6	0.6	–	–
y_{-1}	23	0.6	0.6	–	–
V_{CC}	24	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and −2.0mA at 0.5V at the LOW Logic Level.

USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the Y_i multiplier bit to the appropriate carry input terminal $i = 1, 3, 5...$
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number Representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s Y_s$ at K inputs
Unsigned (Magnitude)	Extended multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force k_s, y_s, $x_s = 0$.
Sign magnitude	$x_s = 0$, $y_s = 0$ None $x_s = 1$, $y_s = 0$ Form $[(XY)_2 + 2^{n-1}y]$ $x_s = 0$, $y_s = 1$ Form $[(XY)_2 + 2^{n-1}x]$ $x_s = 1$, $y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

CONNECTION SCHEMES

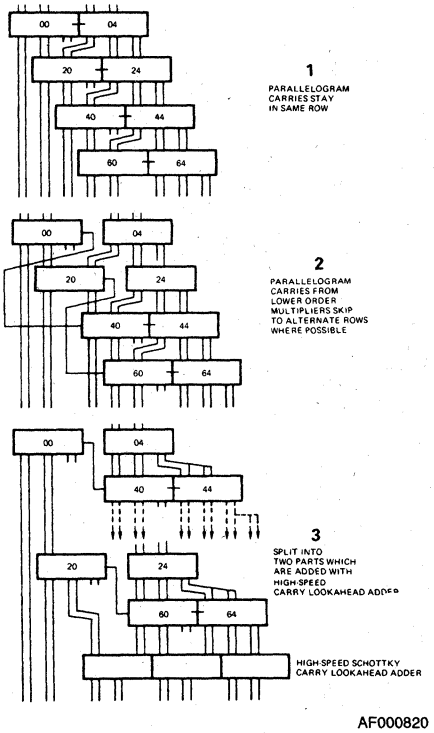


Figure 1

TYPICAL MULTIPLICATION TIMES

Array Size Bits	Total Multiplication Time (ns)	Package Count	
		Am25S05	Am54S/74S181
4 x 4	35	2	
8 x 8	75	8	
12 x 12	115	18	
12 x 12	82	18	5
16 x 16	155	32	
16 x 16	111	32	7
16 x 16	98	32	16
20 x 20	195	50	
20 x 20	130	50	9
24 x 24	235	72	
24 x 24	149	72	11
24 x 24	125	72	24
28 x 28	275	98	
28 x 28	168	98	13
32 x 32	315	128	
32 x 32	187	128	15
32 x 32	152	128	32

Am25S05

$Y = (y_{-1}\, y_0\, y_1)\, 2^A$
$X = (x_{-1}\, x_0\, x_1\, x_2\, x_3)\, 2^B$

AF001170

Figure 2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature(Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.3		Volts
			XC	2.7	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., Y_1 = .0V			120	175	mA

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor (See loading rules).

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 280Ω)

Parameters	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	4 4	8 9	12 14	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$		6 5	12 10	18 15	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$		7 6	15 13	22 20	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}		3 5	6.5 10	12 15	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$		6 4	13.5 9.5	20 14	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$		3 3	15.5 12.5	23 19	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}		8 9	17 18	26 27	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$		10 10	21 21	32 32	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$		6 5	23.5 21.5	35 32	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}		11 10	23 20	34 30	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$		11 11	23 23	34 34	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$		12 12	25 25	37 37	ns

Am25LS07/Am25LS08

Hex/Quad Parallel D Registers with Register Enable

DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit parallel registers
- Common Clock and Common Enable
- Positive edge triggered D flip flops
- Second sourced by TI as 54LS/74LS378 and 379
- Am25LS D.C. parameters including:
  V_{OL} = 0.45V at I_{OL} = 8mA
  Fan-out over military range = 22
  440μA source current

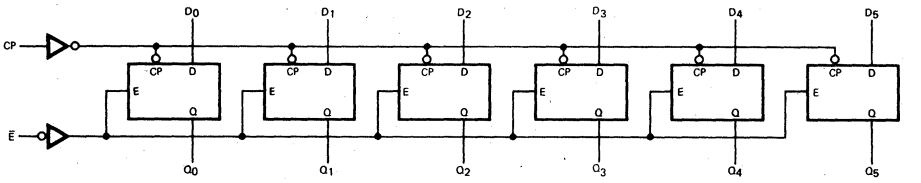
GENERAL DESCRIPTION

The Am25LS07 is a 6-bit Low Power Schottky register with a buffered common register enable. The Am25LS08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54LS/74LS174 and Am54LS/74LS175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

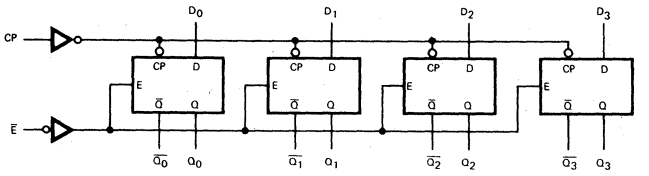
BLOCK DIAGRAM

Am25LS07



BD001450

Am25LS08



BD001520

RELATED PRODUCTS

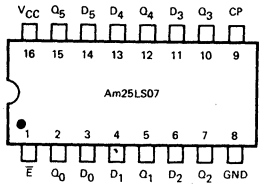
Part No.	Description
Am2918	Quad D Register
Am2919	Quad D Register

03699B

Refer to Page 13-1 for Essential Information on Military Devices

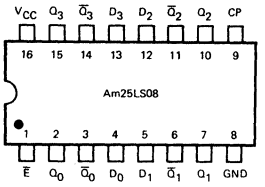
CONNECTION DIAGRAM
Top View

Am25LS07



CD001730

Am25LS08

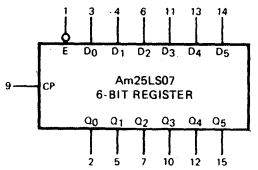


CD001720

Note: Pin 1 is marked for orientation

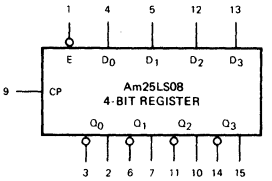
LOGIC SYMBOL

Am25LS07



LS000630

Am25LS08



LS000640

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS07/08 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25LS07/08** — Device type
  - Hex/Quad Parallel D Registers

Valid Combinations	
Am25LS07/08	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{E}$	I	Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.
9	CP	I	Clock. Pulse for the register. Enters data on the LOW-to-HIGH transition.
	Q_i	O	The TRUE register outputs.
	$\overline{Q}_i$	O	The complement register outputs.

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH NC = No Change ↑ = LOW-to-HIGH Transition
L = LOW X = Don't Care $\overline{Q_1}$ on Am25LS08 Only

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.8	Volts
			MIL			0.7	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Clock, $\overline{E}$			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	Clock, $\overline{E}$			20	μA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	LS07		16	22	mA
			LS08		11	18	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output	C_L = 15pF R_L = 2.0kΩ		13	20	ns
t_{PHL}	Clock to Output			13	20	ns
t_{pw}	Clock Pulse Width		17			ns
t_s	Data		20			ns
t_s	Enable		30			ns
t_h	Data		5.0			ns
t_h	Enable		5.0			ns
f_{max} (Note 1)	Maximum Clock Frequency		40	65		MHz

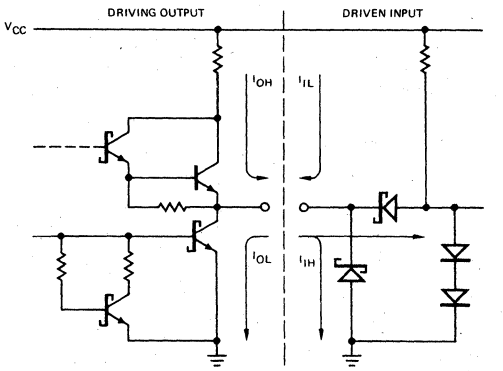
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS.		MILITARY Am25LS		Units
			Min	Max	Min	Max	
t_{PLH}	Clock to Output	C_L = 50pF R_L = 2.0kΩ		30		35	ns
t_{PHL}	Clock to Output			30		35	ns
t_{pw}	Clock Pulse Width		26		30		ns
t_s	Data		30		35		ns
t_s	Enable		43		50		ns
t_h	Data		11		12		ns
t_h	Enable		11		12		ns
f_{max} (Note 1)	Maximum Clock Frequency		30		25		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000180

Note: Actual current flow direction shown.

Am25S07/Am25S08

Hex/Quad Parallel D Registers with Register Enable

DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops

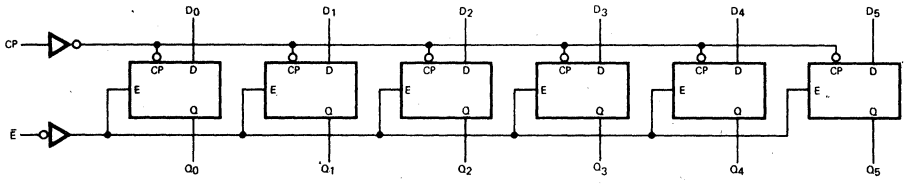
GENERAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

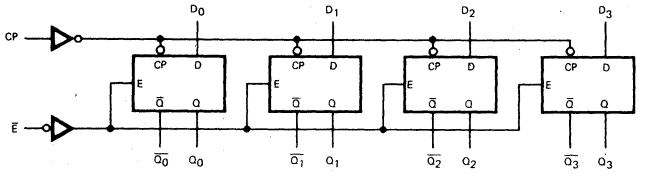
BLOCK DIAGRAM

Am25S07



BD001450

Am25S08



BD001520

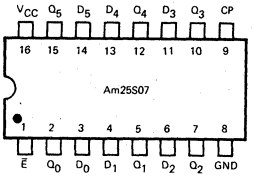
RELATED PRODUCTS

Part No.	Description
Am25LS07/08	Low Power Versions
Am2918	Quad D Register
Am2919	Quad Register
Am29821 – 26	8, 9, 10-Bit Register

03702B

CONNECTION DIAGRAM
Top View

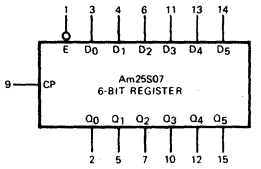
Am25S07



CD001680

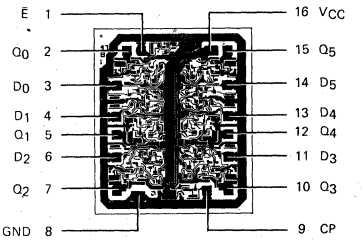
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am25S07



LS000590

METALLIZATION AND PAD LAYOUT
Am25S07



DIE SIZE: 0.070" x 0.083"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S07/08 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S07/08** — Device type
  - Hex/Quad D Registers

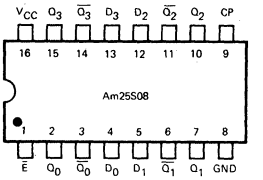
Valid Combinations	
Am25S07/08	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CONNECTION DIAGRAM
Top View

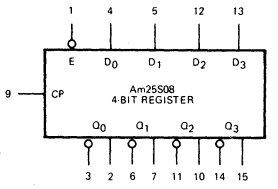
Am25S08



CD001690

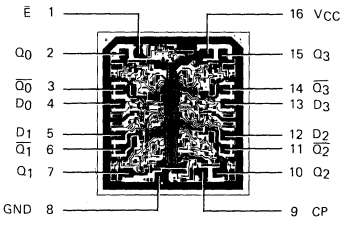
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am25S08



LS000600

METALLIZATION AND PAD LAYOUT
Am25S08



DIE SIZE: 0.067" x 0.073"

9

PIN DESCRIPTION

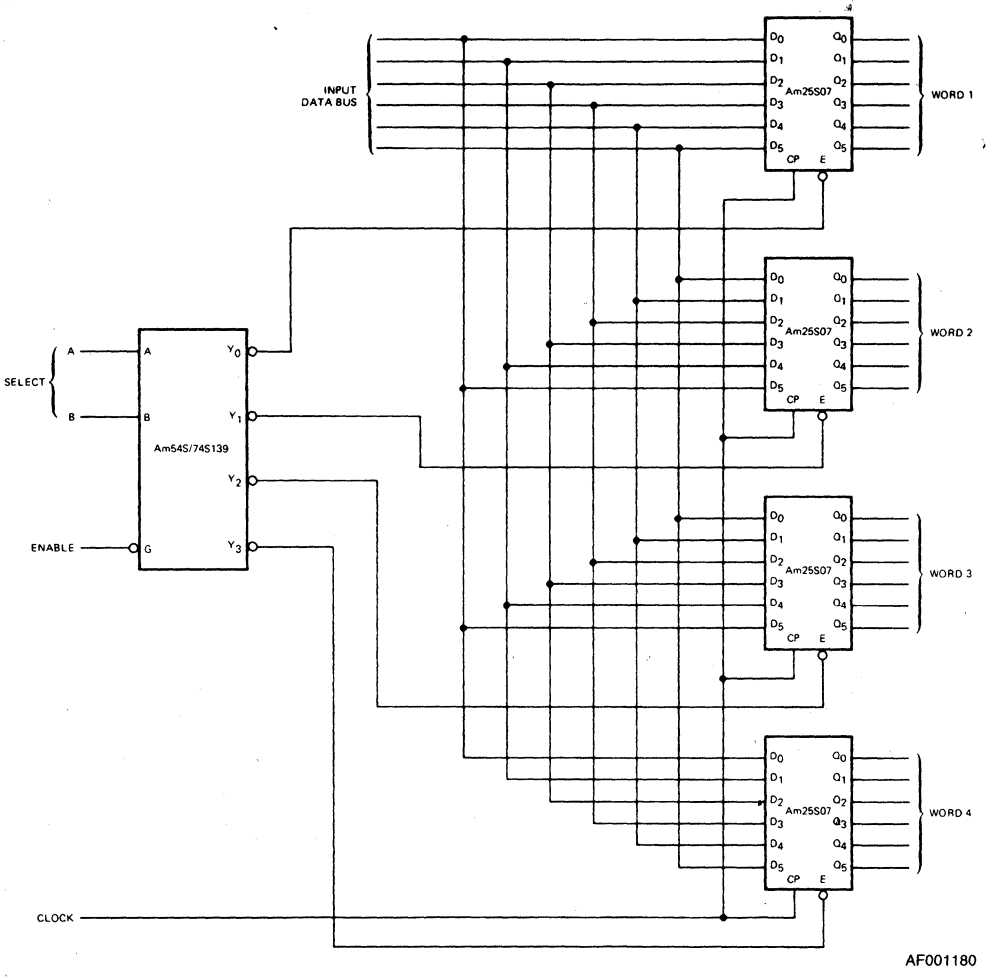
Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{E}$	I	Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.
9	CP	I	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
	Q_i	O	The TRUE register outputs.
	$\overline{Q}_i$	O	The complement register outputs.

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_I	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH Transition
NC = No Change
$\overline{Q}_i$ on Am25S08 Only

APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable		9			ns
t_h	Data		3			ns
t_h	Enable		3			ns

Am25S07 LOADING RULES (In STTL Unit Loads)

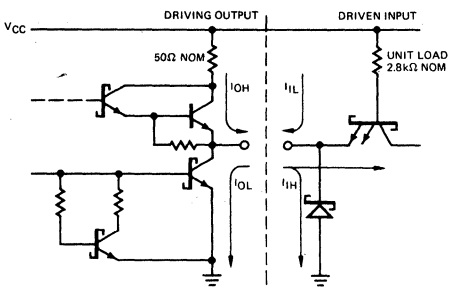
Input/Output	Pin Nos.	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000150

Note: Actual current flow direction shown.

9

Am25LS09

Quad Two-Input, High-Speed Register

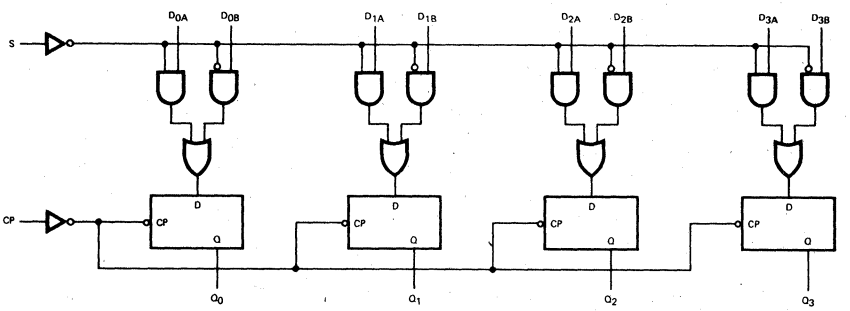
DISTINCTIVE CHARACTERISTICS

- 4-bit register accepts data from one-of-two 4-bit input fields
- Edge triggered clock action
- Second sourced by T.I. as 54LS/74LS399
- Am25LS D.C. parameters including:
  - V_{OL} = 0.45V at I_{OL} = 8mA
  - Fan-out over military range = 22
  - 440μA source current

GENERAL DESCRIPTION

The Am25LS09 is a dual port four-bit register using advanced Low Power Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

BLOCK DIAGRAM



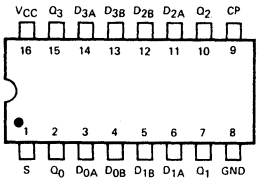
BD001460

RELATED PRODUCTS

Part No.	Description
Am25S09	High Speed Register
Am25S07/08	6/4-Bit Registers
Am25LS07/08	6/4-Bit Low Power Registers

03701B

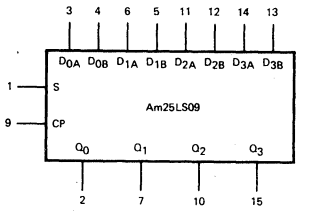
CONNECTION DIAGRAM
Top View



CD001740

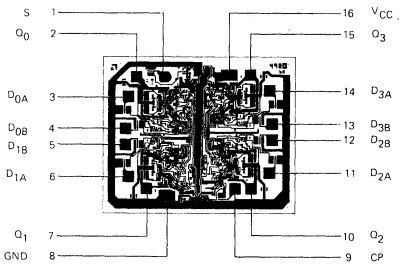
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000650

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.075" x 0.061"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS09 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25LS09** — Device type
  - Quad Two-Input, High-Speed Register

Valid Combinations	
Am25LS09	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

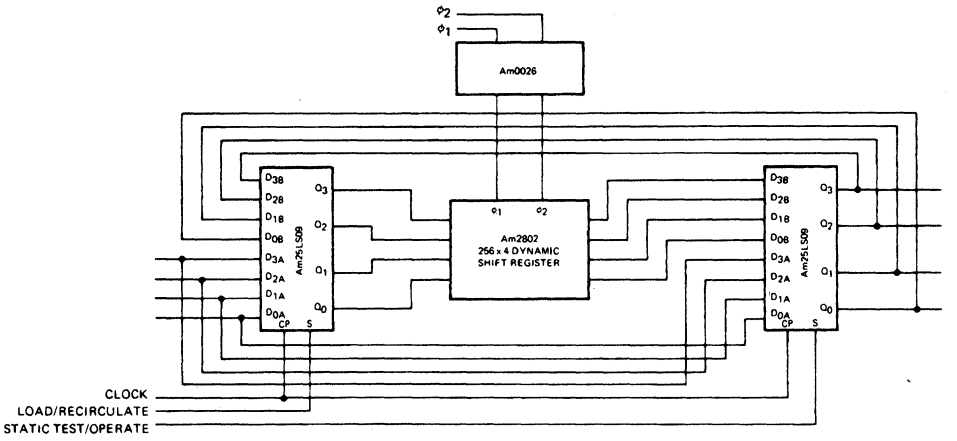
Pin No.	Name	I/O	Description
3, 6, 11, 14	D_{0A}, D_{1A}, D_{2A}, D_{3A}	I	The "A" word into the two-input multiplexer of the D flip-flops.
4, 5, 12, 13	D_{0B}, D_{1B}, D_{2B}, D_{3B}	I	The "B" word into the two-input multiplexer of the D flip-flops.
	Q_0, Q_1, Q_2, Q_3	O	The outputs of the four D-type flip-flops of the register.
1	S	I	Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.
9	CP	I	Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{IA}	INPUTS D_{IB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

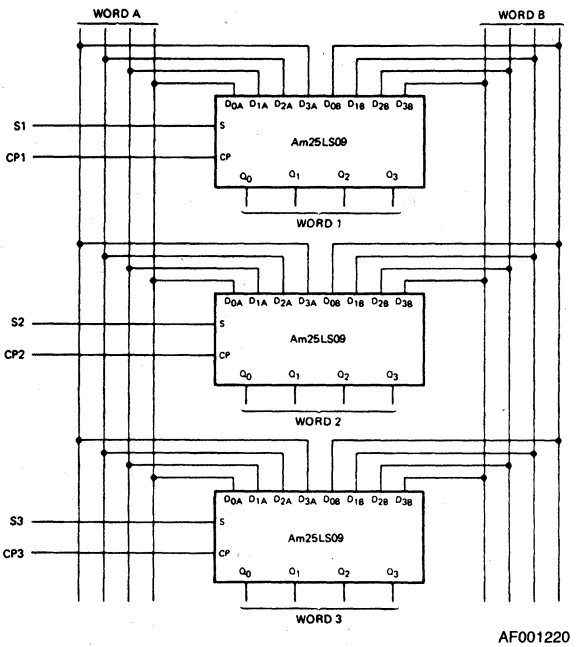
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
i = 0, 1, 2, or 3
↑ = LOW-to-HIGH Transition

APPLICATIONS



AF001210

Am25LS09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



AF001220

Am25LS09 used to store a word from either data bus A or data bus B.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 6 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Clock, S			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	Clock, S			20	μA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)			11	18	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q HIGH	C_L = 15pF, R_L = 2.0kΩ		13	20	ns
t_{PHL}	Clock to Q LOW			13	20	ns
t_{pw}	Clock Pulse Width		17			ns
t_s	Data Set-up Time		20			ns
t_s	Select Input Set-up Time		30			ns
t_h	Data Hold Time		5			ns
t_h	Select Input Hold Time		0			ns
f_{max} (Note 1)	Maximum Clock Frequency		40	65		MHz

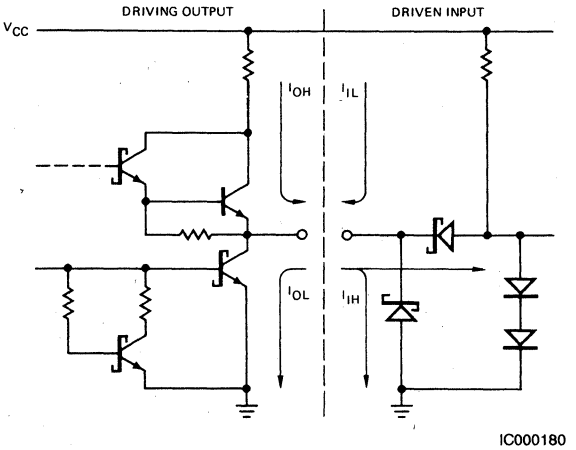
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to Q HIGH	C_L = 50pF, R_L = 2.0kΩ		30		35	ns
t_{PHL}	Clock to Q LOW			30		35	ns
t_{pw}	Clock Pulse Width		26		30		ns
t_s	Data Set-up Time		30		35		ns
t_s	Select Input Set-up Time		43		50		ns
t_h	Data Hold Time		11		12		ns
t_h	Select Input Hold Time		4		5		ns
f_{max} (Note 1)	Maximum Clock Frequency		30		25		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS · Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000180

Note: Actual current flow direction shown.

Am25S09

Quad Two-Input, High-Speed Register

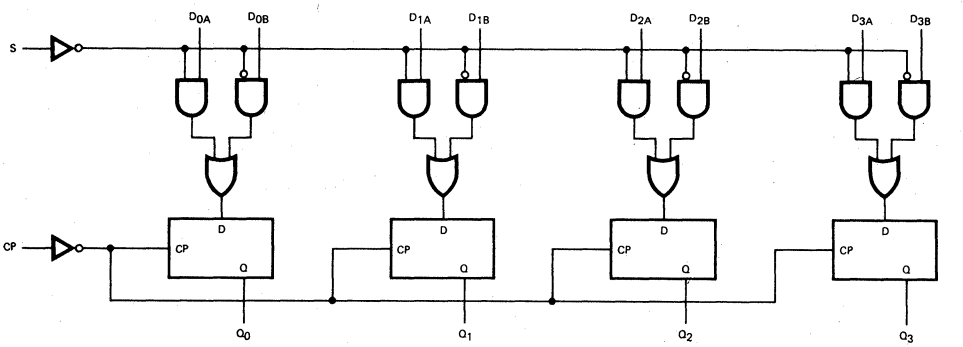
DISTINCTIVE CHARACTERISTICS

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge-triggered clock action
- High-speed Schottky technology.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

GENERAL DESCRIPTION

The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

BLOCK DIAGRAM



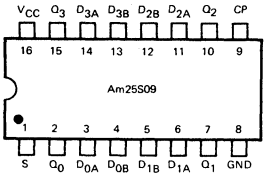
RELATED PRODUCTS

Part No.	Description
Am25LS09	Low Power Version
Am25S07/08	6/4-Bit Register
Am25LS07/08	6/4-Bit Low Power Register

03700B

Refer to Page 13-1 for Essential Information on Military Devices

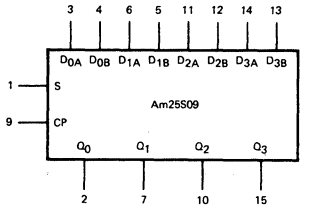
CONNECTION DIAGRAM
Top View



CD001700

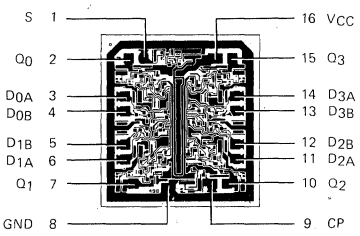
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000610

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.067″ x 0.073″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S09 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S09** — Device type
  - Quad Two-Input, High-Speed Register

Valid Combinations	
Am25S09	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

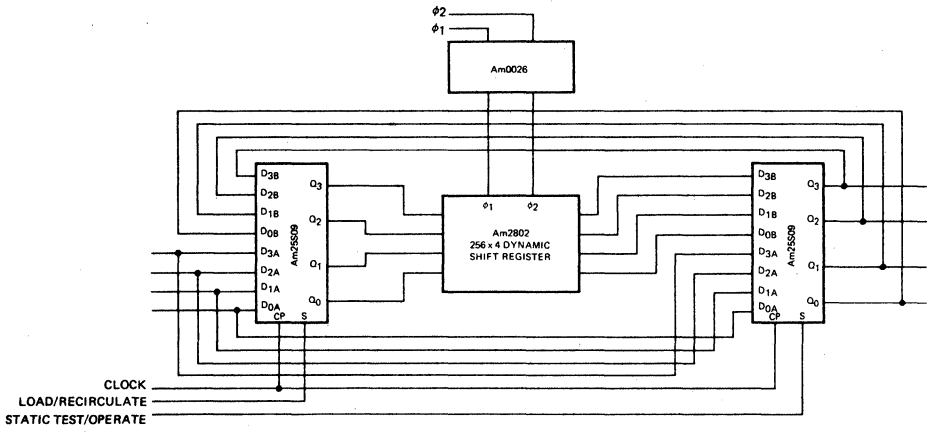
Pin No.	Name	I/O	Description
3 6 11 14	D_{0A}, D_{1A}, D_{2A}, D_{3A}	I	The "A" word into the two-input multiplexer of the D flip-flops.
4 5 12 13	D_{0B}, D_{1B}, D_{2B}, D_{3B}	I	The "B" word into the two-input multiplexer of the D flip-flops.
2,7 10,15	Q_0, Q_1, Q_2, Q_3	O	The outputs of the four D-type flip-flops of the register.
1	S	I	Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH, the B word is applied to the D inputs of the flip-flops.
9	CP	I	Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{IA}	INPUTS D_{IB}	OUTPUT Q_I
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

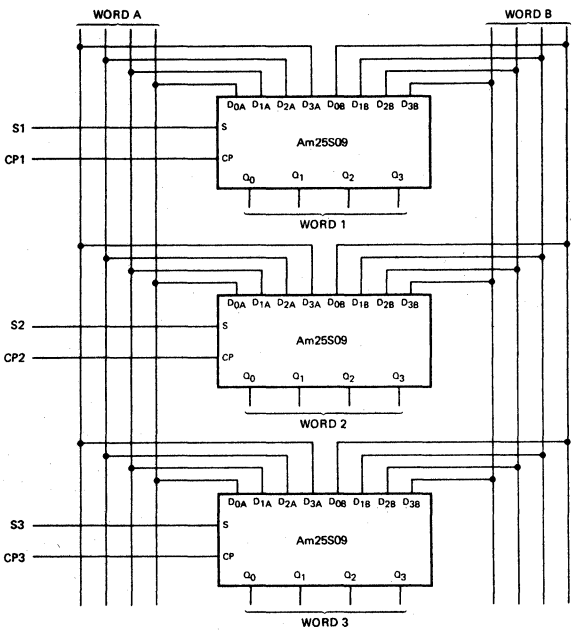
H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

APPLICATIONS



AF000760

Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



AF000770

Am25S09 used to store a word from either data bus A or data bus B.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH Voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input Load Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 5)			75	120	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C)

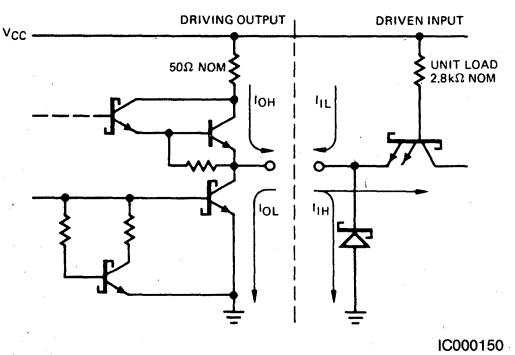
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q HIGH	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		8	12	ns
t_{PHL}	Clock to Q LOW			11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data Set-up Time		5.5			ns
t_s	Select Input Set-up Time		10			ns
t_h	Data Hold Time		3			ns
t_h	Select Input Hold Time		3			ns

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
S	1	1	–	–
Q_0	2	–	20	10
D_{0A}	3	1	–	–
D_{0B}	4	1	–	–
D_{1B}	5	1	–	–
D_{1A}	6	1	–	–
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
D_{2A}	11	1	–	–
Q_{2B}	1	1	–	–
D_{3B}	13	1	–	–
D_{3A}	14	1	–	–
Q_3	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

Am25S10

Four-Bit Shifter with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

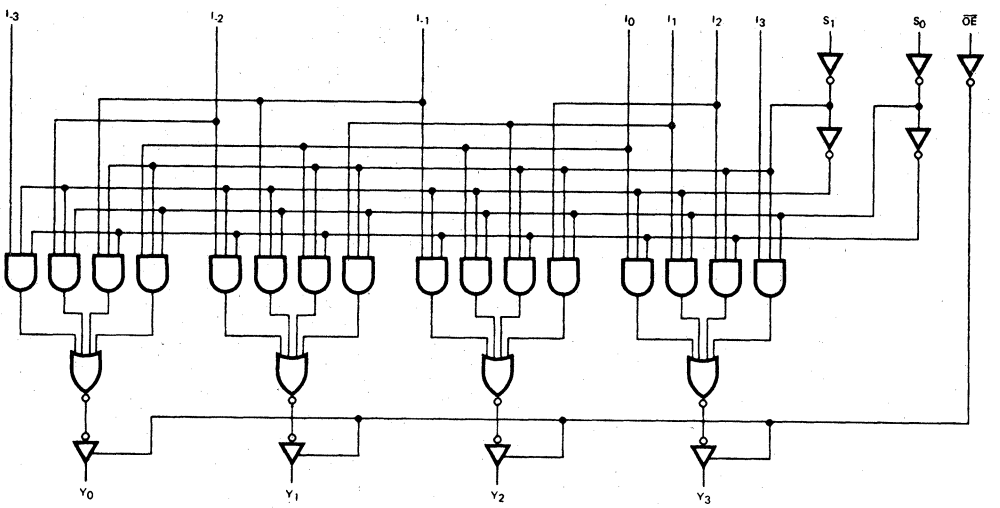
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay
- Alternate source is 54S/74S350

GENERAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

BLOCK DIAGRAM



BD002480

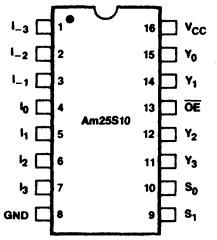
RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice ALU
Am2903	Superslice
Am29501	Multiport Pipeline Processor

03611B

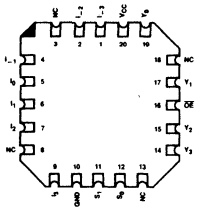
CONNECTION DIAGRAM
Top View

D-16, P-16



CD004060

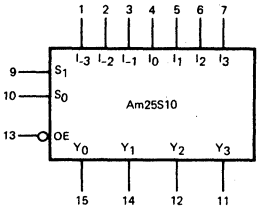
L-20-1



CD004050

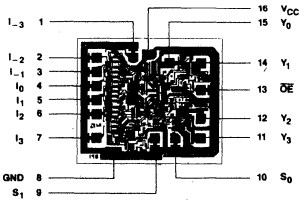
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000750

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.067" x 0.056"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S10 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S10** — Device type
  - 4-Bit Shifter with Three-State Outputs

Valid Combinations	
Am25S10	PC DC, DM LC, LM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_i	I	The seven data inputs of the shifter.
13	$\overline{OE}$		Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.
10, 9	S_0, S_1	I	Select inputs. Controls the number of places the inputs are shifted.
11, 12, 14, 15	Y_i	O	The four outputs of the shifter.

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load (Note 1)	Fan-out Output HIGH XM	Fan-out Output HIGH XC	Fan-out Output LOW
I-3	1	1	–	–	–
I-2	2	1.5	–	–	–
I-1	3	1.5	–	–	–
I_0	4	1.5	–	–	–
I_1	5	1.5	–	–	–
I_2	6	1.5	–	–	–
I_3	7	1	–	–	–
GND	8	–	–	–	–
S_1	9	1	–	–	–
S_0	10	1	–	–	–
Y_3	11	–	40	130	10
Y_2	12	–	40	130	10
$\overline{OE}$	13	1	–	–	–
Y_1	14	–	40	130	10
Y_0	15	–	40	130	10
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH and −2.0mA at 0.5V at the LOW.

Note 1. The fan-in on I_{-2}, I_{-1}, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at V_{IL} = 0.5V. As V_{IL} is decreased to a 0V, the input current I_{IL} MAX. increases to −4, −6, −8, −6 and −4mA respectively due to the decrease in current sharing with the internal select buffer outputs.

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0\overline{S}_1 I_0 + S_0\overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$Y_1 = \overline{S}_0\overline{S}_1 I_1 + S_0\overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$Y_2 = \overline{S}_0\overline{S}_1 I_2 + S_0\overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$

$$Y_3 = \overline{S}_0\overline{S}_1 I_3 + S_0\overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

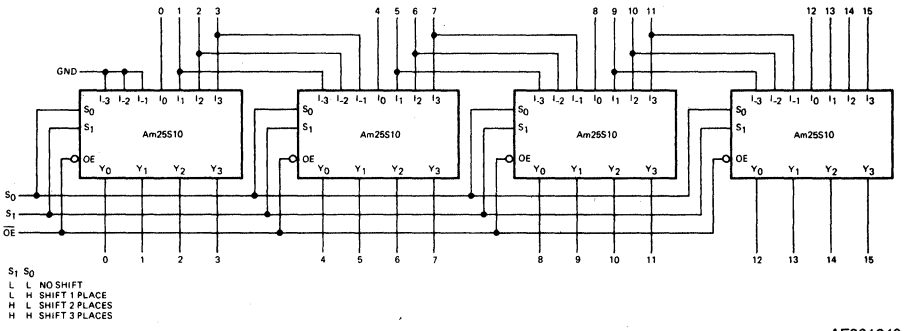
TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

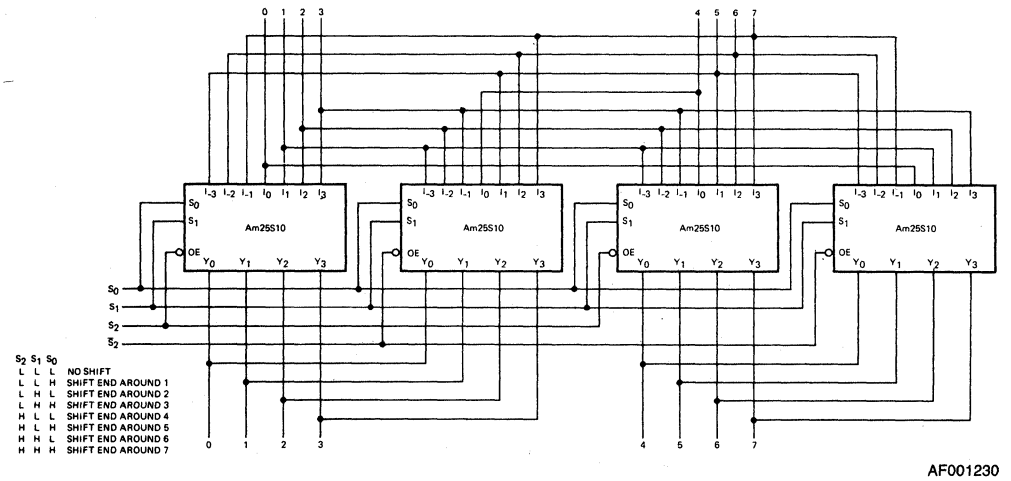
H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State

D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

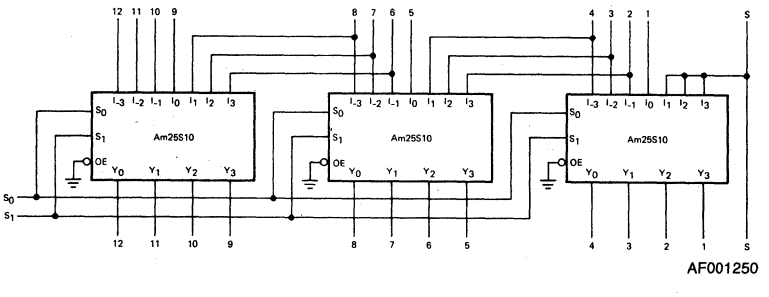
APPLICATIONS



16-Bit Shift-Up 0, 1, 2, or 3 Places.



8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



13-Bit 2's Complement Scaler

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

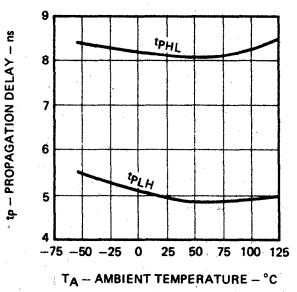
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	XM I_{OH} = −2mA	2.4	3.4		Volts
			XC I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4V			50	μA
			V_O = 0.5V			−50	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All outputs open, All inputs = GND			60	85	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

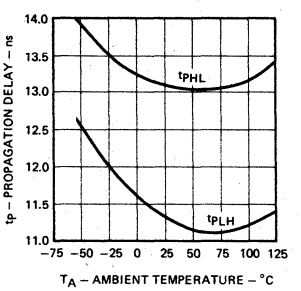
PERFORMANCE CURVES
SWITCHING CHARACTERISTICS

Data to Output (Typical)



OP001390

Select to Output (Typical)



OP001400

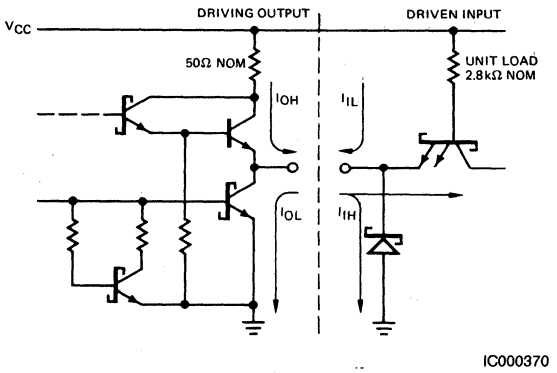
03611B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Output	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
t_{PHL}				8	12	
t_{PLH}	Select to Output			11	17	ns
t_{PHL}				13	20	
t_{ZH}	Output Control $\overline{OE}$ to Output				19.5	ns
t_{ZL}					21	
t_{HZ}	Output Control $\overline{OE}$ to Output	V_{CC} = 5V, C_L = 5pF, R_L = 280Ω		5	8	ns
t_{LZ}				10	15	

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25LS14A

8-Bit Serial/Parallel Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 50MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- IMOX™ process with ECL internal

GENERAL DESCRIPTION

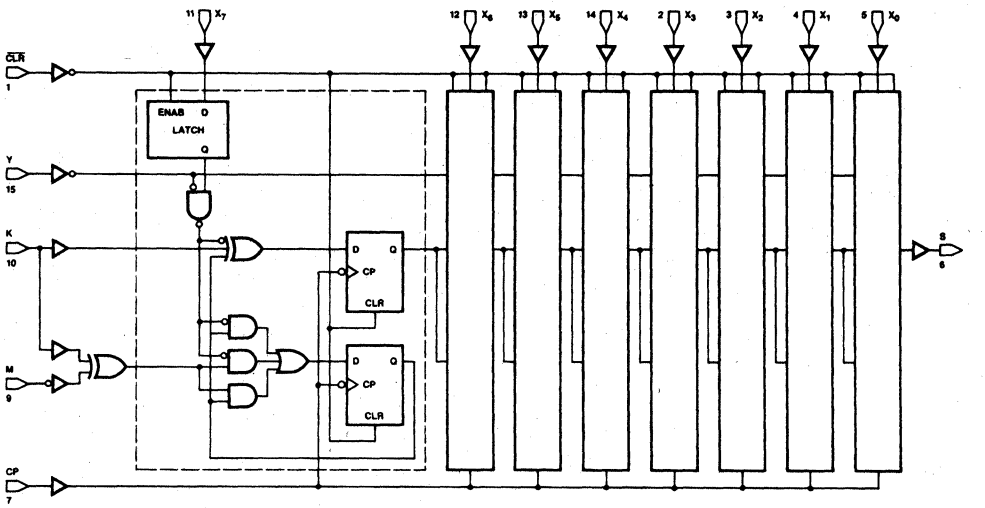
The Am25LS14A is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream – least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14A must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

BLOCK DIAGRAM

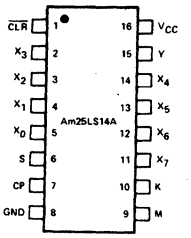


BD001650

IMOX is a trademark of Advanced Micro Devices.

01767C

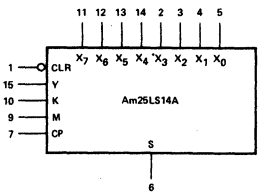
CONNECTION DIAGRAM
Top View



CD001800

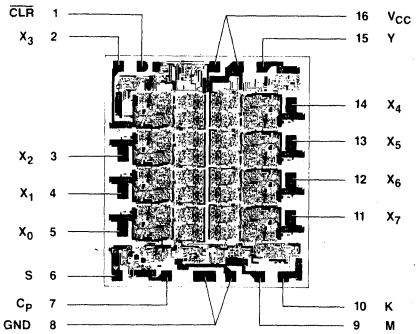
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000660

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.084" x 0.095"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS14A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25LS14A** — Device type
  - 8-Bit Multiplier

Valid Combinations	
Am25LS14A	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7	I	The eight data inputs for the multiplicand (X) data.
15	Y	I	The serial input for the multiplier (Y) data—least significant bit first.
6	S	O	The serial output for the product of X • Y—least significant bit first.
7	CP	I	Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.
1	CLR	I	Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.
10	K	I	The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.
9	M	I	The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	
CLR	CP	K	M	X_i	Y	Y_{-1}	S	FUNCTION
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

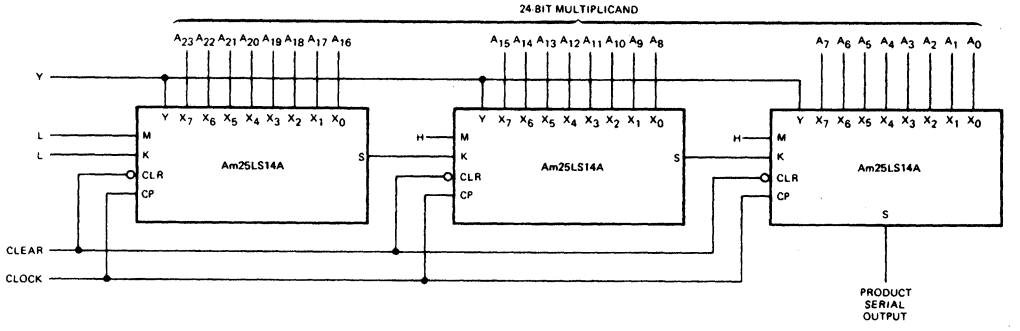
H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.
L LOW, applying to a LOW voltage level.
I Input.
O Output.
Negative Current Current flowing out of the device.
Positive Current Current flowing into the device.
I_{IL} LOW-level input current with a specified LOW-level voltage applied.
I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.
I_{OL} LOW-level output current.
I_{OH} HIGH-level output current.
I_{SC} Output short-circuit source current.
I_{CC} The supply current drawn by the device from the V_{CC} power supply.
V_{IL} Logic LOW input voltage.
V_{IH} Logic HIGH input voltage.
V_{OL} LOW-level output voltage with I_{OL} applied.
V_{OH} HIGH-level output voltage with I_{OH} applied.

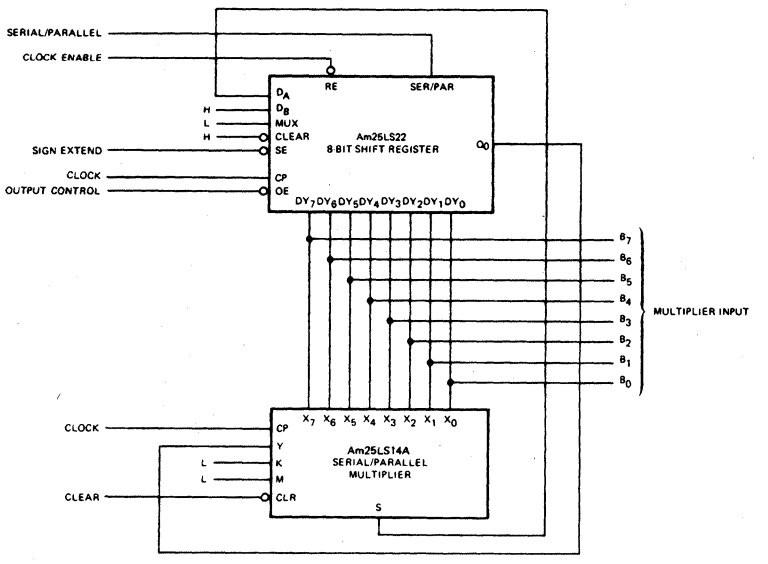
APPLICATIONS

See also Digital Signal Processing Applications Section for more information.



AF001120

Basic 24-Bit Serial/Parallel Connection



AF001130

8-Bit by 8-Bit Multiplier, Bus Organized,
with 8-Bit Truncated Product

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4	Volts
			I_{OL} = 12mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			−0.48	mA
			K, $\overline{CLR}$			−1.2	
			CP			−1.6	
			Y			−3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20	μA
			K, $\overline{CLR}$			30	
			CP			40	
			Y			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			45	65	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output	C_L = 15pF R_L = 2.0kΩ		8	14	ns
t_{PHL}				10	18	
t_{PHL}	Clear to Output			9	17	ns
t_s	Y to Clock		15			ns
t_h			0			
t_s	K to Clock		15			ns
t_h			0			
t_s	X_i to Clear		13			ns
t_h			0			
t_{pw}	Clock (HIGH)		10			ns
	Clock (LOW)		10			
t_{pw}	Clear Pulse Width		10			ns
t_s	Clear Recovery Time (Inactive State)		5			ns
f_{max} (Note 1)	Maximum Clock Frequency		50	60		MHz

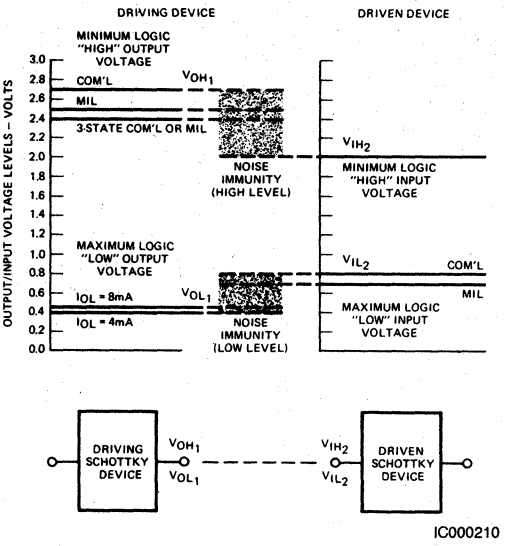
Note 1: Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	Am25LS COMMERCIAL		Am25LS MILITARY		Units
			Min	Max	Min	Max	
t_{PLH}	Clock to Output	C_L = 50pF R_L = 2.0kΩ		18		20	ns
t_{PHL}				22		25	
t_{PHL}	Clear to Output			22		25	ns
t_s	Y to Clock		22		25		ns
t_h			0		0		
t_s	K to Clock		20		22		ns
t_h			0		0		
t_s	X_i to Clear		20		22		ns
t_h			0		0		
t_{pw}	Clock (HIGH)		10		10		ns
	Clock (LOW)		10		10		
t_{pw}	Clear Pulse Width		10		10		ns
t_s	Clear Recovery Time (Inactive State)		5		5		ns
f_{max} (Note 1)	Maximum Clock Frequency		50		50		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

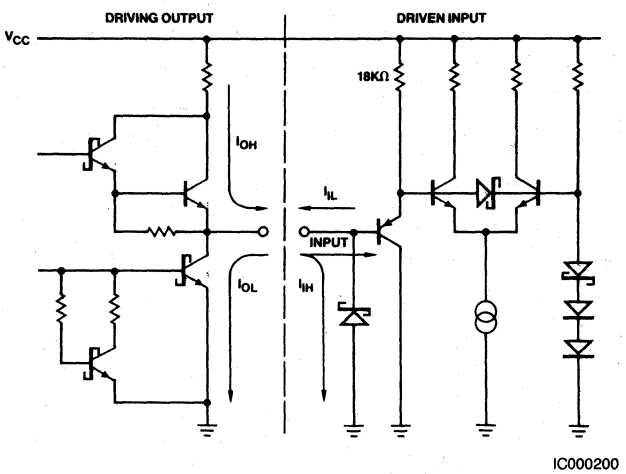
LOW CURRENT SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000210

Note: Refer to Electrical Characteristics for measure currents.

INPUT/OUTPUT INTERFACE CONDITIONS



IC000200

Note: Actual current flow direction shown.

Am25LS15

Quad Serial Adder/Subtractor

DISTINCTIVE CHARACTERISTICS

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Second sourced by T.I. as Am54LS/74LS385

GENERAL DESCRIPTION

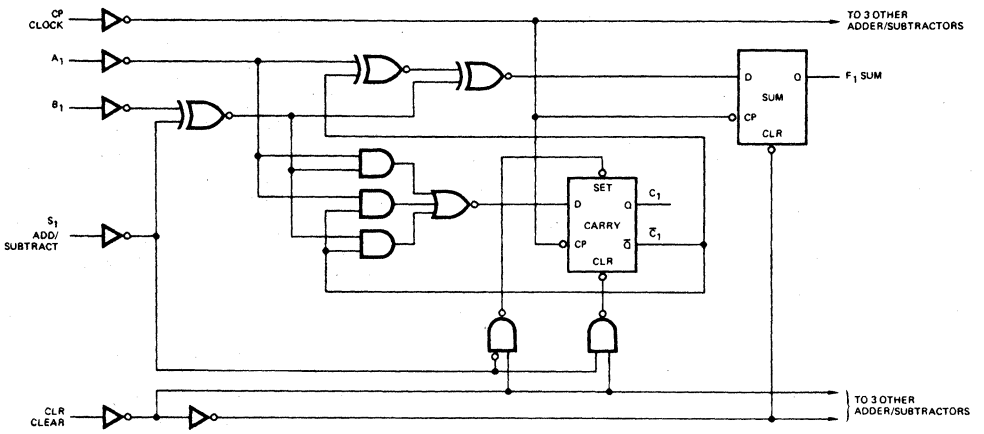
The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

BLOCK DIAGRAM

(One of Four Similar Functions)

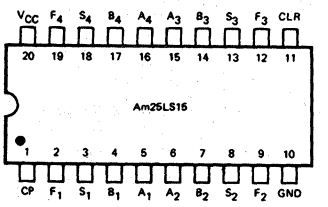


BD001670

03663B

Refer to Page 13-1 for Essential Information on Military Devices

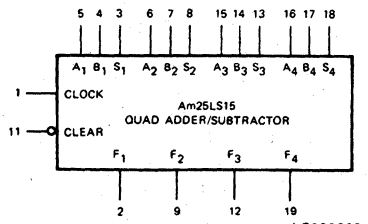
CONNECTION DIAGRAM
Top View



CD001790

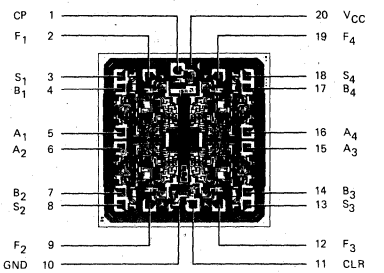
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000680

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.095" x 0.095"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS15 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - P– 20-pin plastic DIP
  - X– Dice
- **Am25LS15** — Device type
  - Quad Serial Adder/Subtractor

Valid Combinations	
Am25LS15	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
5,6,15,16	A_1, A_2, A_3, A_4	I	The "A" input into each adder/subtractor.
4,7,14,17	B_1, B_2, B_3, B_4	I	The "B" input into each adder/subtractor.
3,8,13,18	S_1, S_2, S_3, S_4	I	The add subtract control for each adder/subtractor. When S is LOW, the F function is A + B. When S is HIGH, the F function is A – B.
2,9,12,19	F_1, F_2, F_3, F_4	O	The four independent serial outputs of the adder/subtractor.
1	CP Clock	I	The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.
11	CLR Clear	I	When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

FUNCTION TABLE

External Inputs					Internal Point		Output	
CP	CLR	S	A	B	C	C_1	F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	Add
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	Subtract
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data in the Carry Flip-Flop Before the Clock Transition
C_l = Data in the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

$A = A_R + jA_I$

$B = B_R + jB_I$

$W = W_R + jW_I$

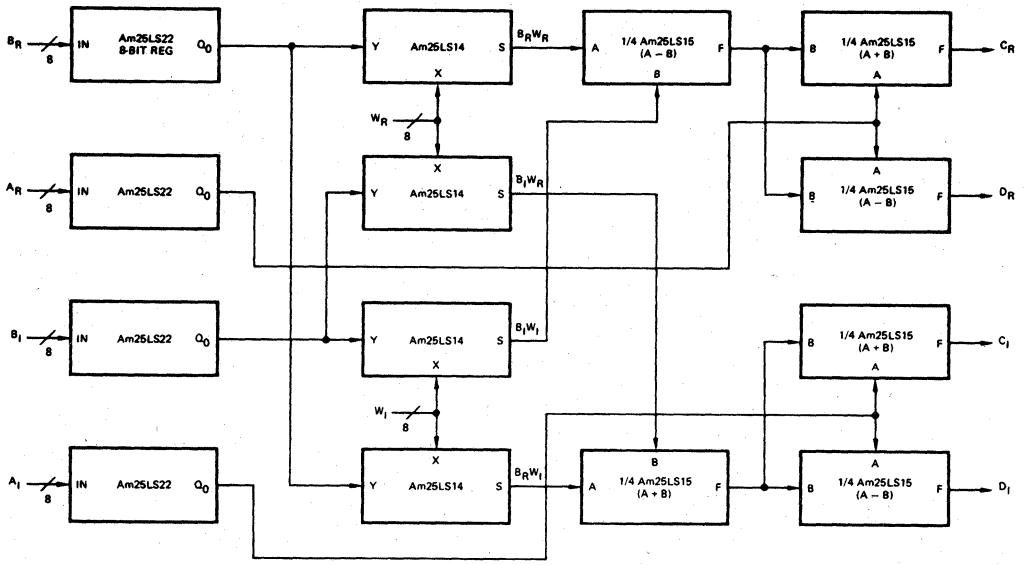
The outputs C and D are also complex numbers and are evaluated as:

$C = C_R + jC_I = (A_R + B_RW_R - B_IW_I) + j(A_I + B_RW_I + B_IW_R)$

$D = C_R + jD_I = (A_R - B_RW_R + B_IW_I) + j(A_I - B_RW_I - B_IW_R)$

The four multiplications can be implemented using four Am25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the Am25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

FAST FOURIER TRANSFORM (FFT) BUTTERFLY



AF001200

An FFT butterfly connection for complex arithmetic inputs and outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

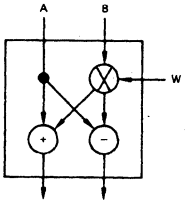
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC}=MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			48	75	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs HIGH, measured after a LOW-to-HIGH clock transmission.

Functional Diagram for FFT Butterfly Connection



AF001160

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output		C_L = 15pF R_L = 2.0kΩ		14	22	ns
t_{PHL}					14	22	
t_{PHL}	Clear to Output				20	30	ns
t_s	A, B, S			10			ns
t_h				0			
t_s	Clear Recovery			25			ns
t_h	Clear Hold Time			0			ns
t_{pw}	Clock	HIGH		17			ns
		LOW		17			
t_{pw}	Clear LOW			20			ns
f_{max} (Note 1)	Maximum Clock Frequency			30	40		MHz

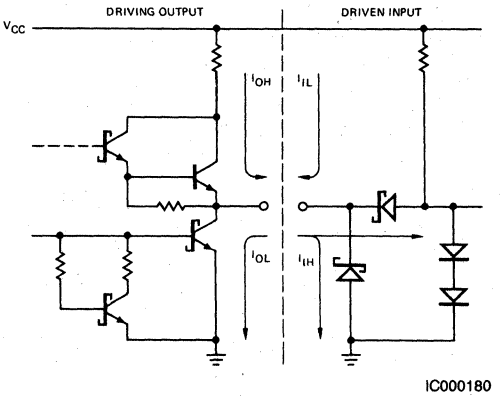
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on the t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS		MILITARY Am25LS		Units
				Min	Max	Min	Max	
t_{PLH}	Clock to Output		C_L = 50pF R_L = 2.0kΩ		33		38	ns
t_{PHL}					33		38	
t_{PHL}	Clear to Output				43		50	ns
t_s	A, B, S			17		20		ns
t_h				4		5		
t_s	Clear Recovery			37		42		ns
t_h	Clear Hold Time			4		5		ns
t_{pw}	Clock	HIGH		26		30		ns
		LOW		26		30		
t_{pw}	Clear LOW			30		35		ns
f_{max} (Note 1)	Maximum Clock Frequency			23		20		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000180

Note: Actual current flow direction shown.

Am25S18

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75MHz clock frequency

GENERAL DESCRIPTION

The Am25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

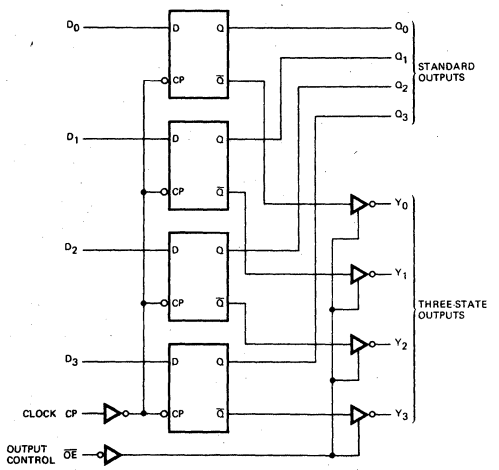
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25S18 is a 4-bit, high speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25S18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

BLOCK DIAGRAM



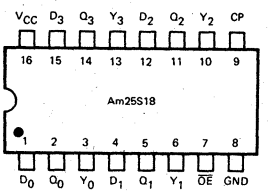
BD001510

RELATED PRODUCTS

Part No.	Description
Am25S07	Register
Am25S08	Register
Am25S09	Register
Am25S374	Register
Am29821-26	Register

03613B

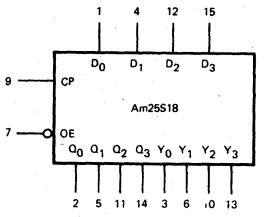
CONNECTION DIAGRAM
Top View



CD001710

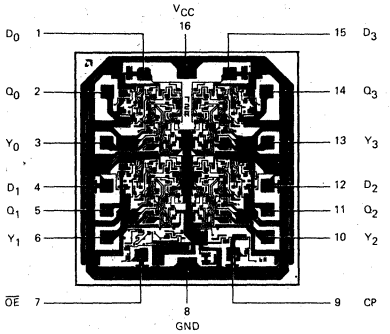
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000620

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.077″ x 0.079″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S18 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S18** — Device type
  - Quad D Register with Standard and Three-State Outputs

Valid Combinations	
Am25S18	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP	I	Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$	O	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW NC = No change
H = HIGH ↑ = LOW to HIGH transition
X = Don't care Z = High impedance
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

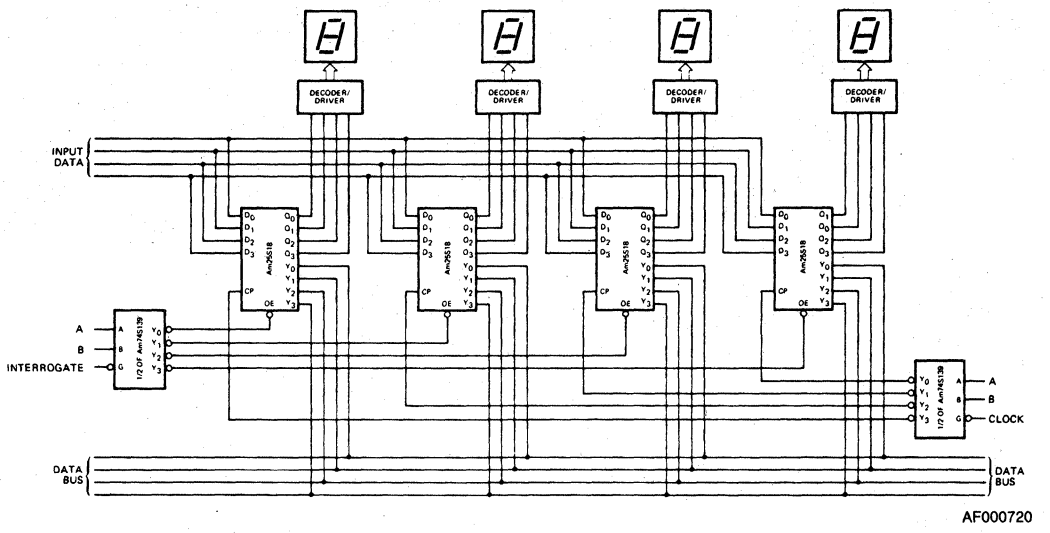
LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

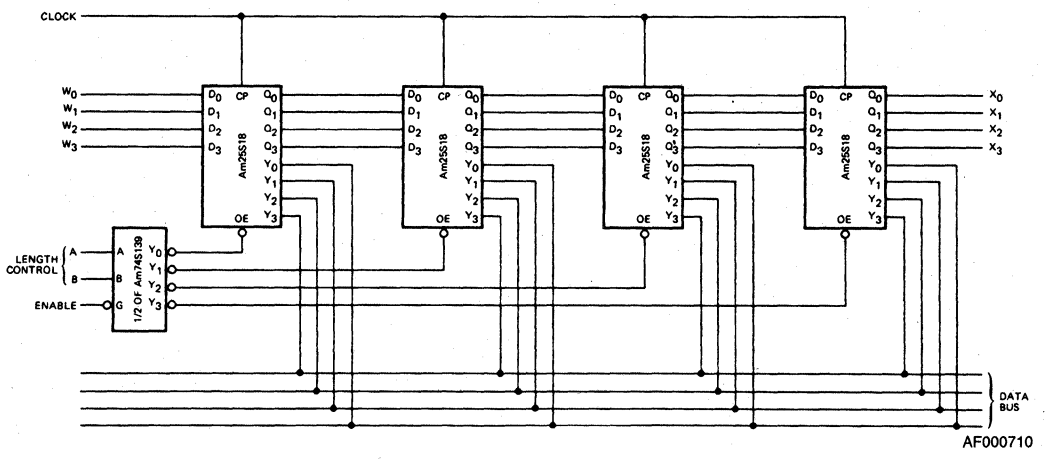
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for $i = 0, 1, 2, 3$.

APPLICATIONS



The Am25S18 Used As Display Register With Bus Interrogate Capability.



The Am25S18 As A Variable Length (1, 2, 3 or 4 Word) Shift Register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 18) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

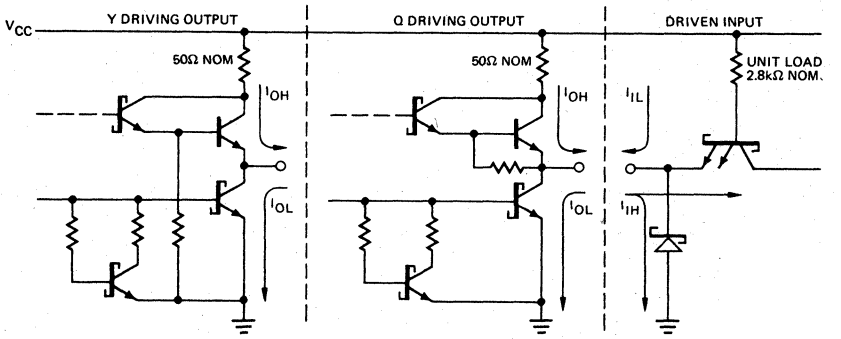
Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q I_{OH} = −1mA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	μA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V, R_L=280Ω)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output				6.0	9.0	ns
t_{PHL}	($\overline{OE}$ LOW)				8.5	13	
t_{ZH}	Output Control to Output		C_L = 15pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000170

Note: Actual current flow direction shown.

Am25LS22

8-Bit Serial/Parallel Register with Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322

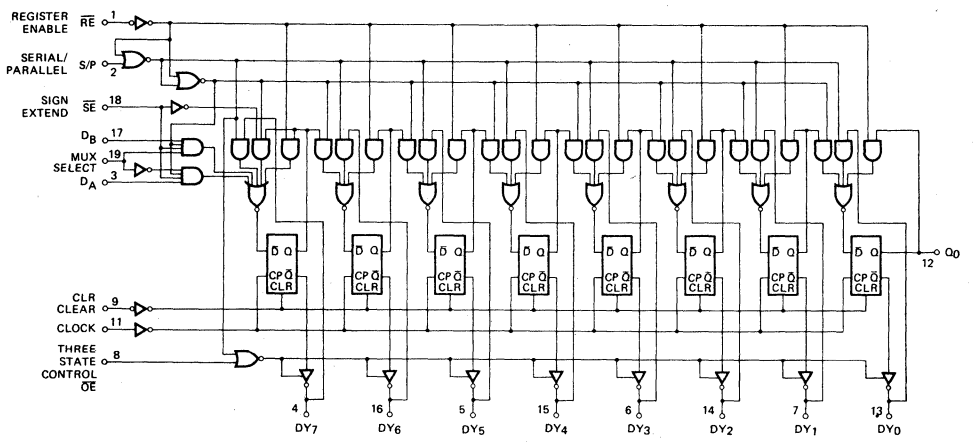
GENERAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0 is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extended function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

BLOCK DIAGRAM



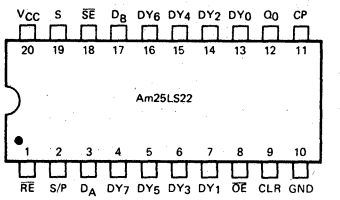
BD001470

RELATED PRODUCTS

Part No.	Description
Am25LS23	8-Bit Shift/Storage Register

03622B

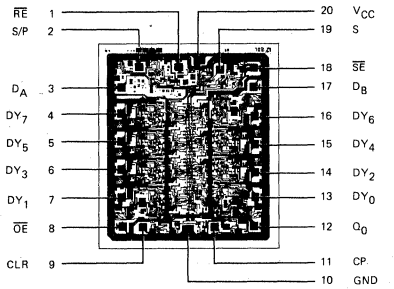
CONNECTION DIAGRAM
Top View



CD001750

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.096″ x 0.112″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS22 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - P– 20-pin plastic DIP
  - X– Dice
- **Am25LS22** — Device type
  - 8-Bit Serial/Parallel Register with Sign Extend

Valid Combinations	
Am25LS22	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	DY_i	I/O	The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.
12	Q_0	O	The continuous output from the Q_0 flip-flop of the register. This output is used for serial shifting.
1	$\overline{RE}$	I	Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited.
2	S/P	I	Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.
18	$\overline{SE}$	I	Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the Q_7 flip-flop will be repeated in the Q_7 flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer (D_A and D_B) is enabled to enter data during the serial shift right. The Q_7 flip-flop (DY_7) is normally considered the MSB of the register for arithmetic definitions.
3, 17	D_A, D_B	I	The serial inputs to the device.
19	S	I	Multiplexer Select. When S is LOW, the D_A serial input is selected. When S is HIGH, the D_B serial input is selected.
9	CLR	I	Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.
11	CP	I	Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.
8	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the eight DY_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

FUNCTION TABLE

Mode	Inputs							Outputs								
	Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	H	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	L	X	X	L	X	Z	Z	Z	Z	Z	Z	Z	Z	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
↑ = Clock LOW-to-HIGH Transition
X = Don't Care
H = HIGH
NC = No Change
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

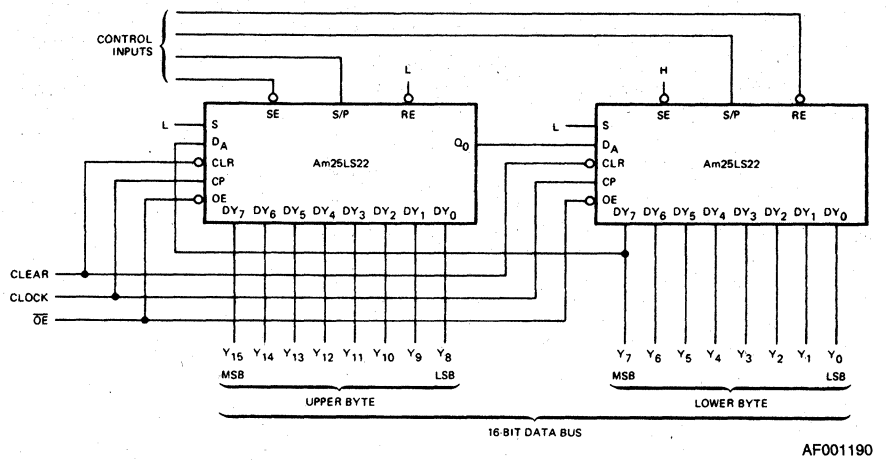
D_7, D_6...D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady-state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n}...Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

9

APPLICATION



AF001190

System Operation	Am25LS22 Upper Byte				Am25LS22 Lower Byte				Function
	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	Description
Load lower byte and extend lower byte sign to upper byte	H	H	L	X	X	L	L	X	Load from Bus
	L	H	L	H	X	X	H	H	7 clock cycles to extend sign
Load upper byte and extend upper byte sign while shifting value to lower byte position	X	L	L	X	X	X	X	X	Load from Bus
	H	H	L	H	H	H	L	H	8 clock cycles to extend upper byte sign and shift upper byte into lower byte position
Read 16-bit word to Bus	X	X	X	L	X	X	X	L	Unload

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State..... −0.5V to +V_{CC} max
DC Input Voltage ($\overline{OE}$, S/P, RE,
CP, CLR) ..... −0.5V to +7.0V
DC Input Voltage (Others) ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q_O, I_{OH} = −440µA	MIL	2.5			Volts
				COM'L	2.7			
			DY_i, I_{OH} = −1.0mA	MIL	2.4			
			DY_i, I_{OH} = −2.6mA	COM'L	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA			0.4	Volts
				I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{SE}$			−1.08	mA
				S			−0.72	
				Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V (Except DY_i)		$\overline{SE}$			60	µA
				S			40	
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, (Except DY_i)	V_{IN} = 7.0V	$\overline{OE}$,S/P,RE,CP,CLR			0.1	mA
			V_{IN} = 5.5V	$\overline{SE}$			0.3	
				S			0.2	
				Others			0.1	
I_{OZ}	Off state (High-Impedance) Output Current (DY_i)	V_{CC} = MAX		V_O = 2.4			40	mA
				V_O = 0.4V			−100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX				40	65	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN, or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to DY_i		R_L = 2.0kΩ, C_L = 15pF		16.5	24	ns
t_{PHL}					18	26	
t_{PHL}	Clear to DY_i				23	30	ns
t_{PLH}	Clock to Q_0				16.5	24	ns
t_{PHL}					18	26	
t_{PHL}	Clear to Q_0				23	30	ns
t_{ZH}	$\overline{OE}$ to DY_i				13	21	ns
t_{ZL}					18	26	
t_{HZ}			R_L = 2.0kΩ, C_L = 5pF		13	21	
t_{LZ}					18	26	
t_{ZH}	SER/PAR to DY_i		R_L = 2.0kΩ, C_L = 15pF		18	26	ns
t_{ZL}					23	32	
t_{HZ}			R_L = 2.0kΩ, C_L = 5pF		18	26	
t_{LZ}					23	32	
t_s	RE to Clock		R_L = 2.0kΩ, C_L = 15pF	20			ns
t_s	SE to Clock			10			
t_s	S to Clock			15			
t_s	D_A and D_B to Clock			15			
t_s	DY_i (Load) to Clock			15			
t_s	Clear Recovery to Clock			8.0			
t_s	S/P to Clock			15			ns
t_h	Any Input			0			
t_h	Clear Hold			0			ns
t_{pw}	Clock	HIGH		8.0			ns
		LOW		8.0			
t_{pw}	Clear			20			ns
f_{max} (Note 1)	Maximum Clock Frequency			35	50		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

03622B

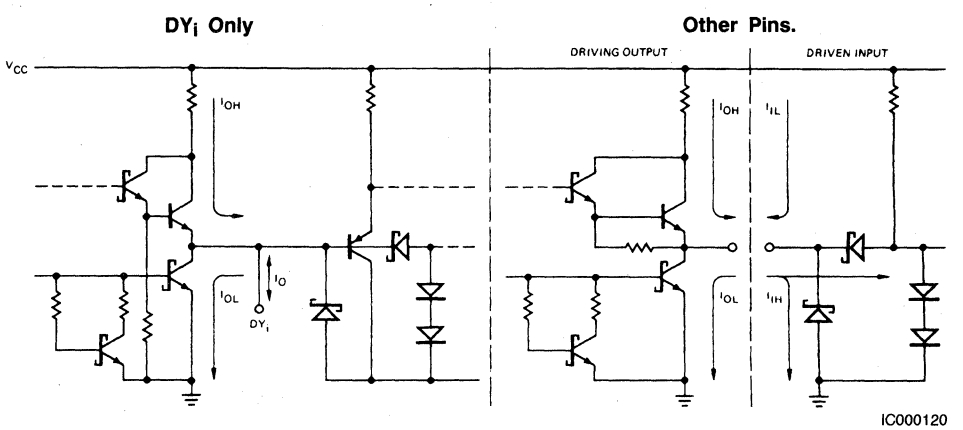
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to DY_i		C_L = 50pF, R_L = 2.0kΩ		35		41	ns
t_{PHL}					38		44	
t_{PHL}	Clear to DY_i				43		50	ns
t_{PLH}	Clock to Q_0				35		41	ns
t_{PHL}					38		44	
t_{PHL}	Clear to Q_0				43		50	ns
t_{ZH}	OE to DY_i				32		36	ns
t_{ZL}					38		44	
t_{HZ}			C_L = 5.0pF, R_L = 2.0kΩ		28		31	
t_{LZ}					34		39	
t_{ZH}	SER/PAR to DY_i		C_L = 50pF, R_L = 2.0kΩ		38		44	ns
t_{ZL}					46		53	
t_{HZ}			C_L = 5.0pF, R_L = 2.0kΩ		34		39	
t_{LZ}					42		48	
t_s	RE to Clock		C_L = 50pF, R_L = 2.0KΩ	30		35		
t_s	SE to Clock			17		20		
t_s	S to Clock			24		27		ns
t_s	D_A and D_B to Clock			24		27		
t_s	DY_i (Load) to Clock			24		27		
t_s	Clear Recovery to Clock			15		17		
t_s	S/P to Clock			24		27		ns
t_h	Any Input			4		5		
t_h	Clear Hold			4		5		ns
t_{pw}	Clock	HIGH		15		17		ns
		LOW		15		17		
t_{pw}	Clear			30		35		ns
f_{max} (Note 1)	Maximum Clock Frequency			26		23		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25LS23

8-Bit Shift/Storage Register with Synchronous Clear

DISTINCTIVE CHARACTERISTICS

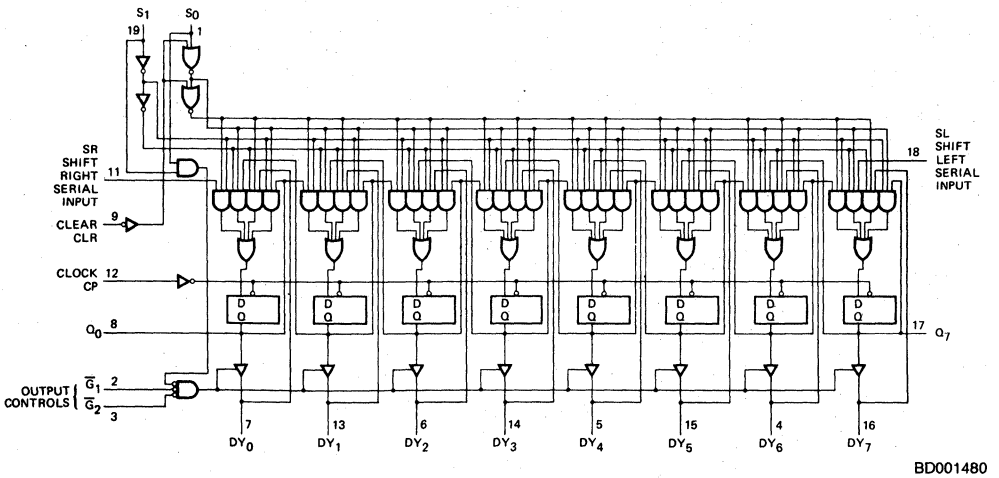
- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Second sourced by T.I. as 54LS/74LS323

GENERAL DESCRIPTION

The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops Q_0 and Q_7.

Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

BLOCK DIAGRAM



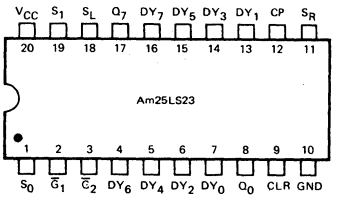
BD001480

RELATED PRODUCTS

Part No.	Description
Am25LS22	8-Bit Serial/Parallel Register

03661B

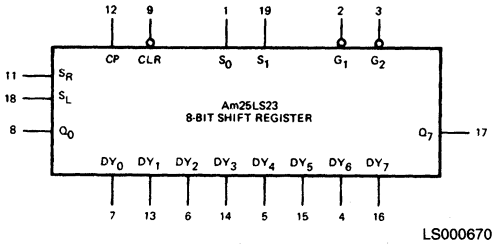
CONNECTION DIAGRAM
Top View



CD001760

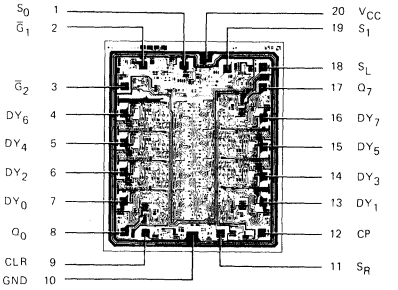
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000670

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.096″ x 0.112″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS23 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS23** — Device type
  - 8-Bit Shift Storage Register
  - With Synchronous Clear

Valid Combinations	
Am25LS23	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

Pin No.	Name	I/O	Description
11	S_R	I	Shift right data input to Q_7.
18	S_L	I	Shift left data input to Q_0.
9	Clear	I	Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled.
12	Clock	I	A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition.
1, 19	S_0, S_1	I	Mode selection control lines used to control input (output during load) conditions.
2, 3	$\overline{G}_1$, $\overline{G}_2$	I	Active LOW input to control three-state output in active LOW AND configuration.
8, 17	Q_0, Q_7	O	The only two direct outputs; used to cascade shift operations.
7, 13, 6, 14, 5, 15, 4, 16	$DY_0 - DY_7$	I/O	Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\overline{G}_1$, $\overline{G}_2$).

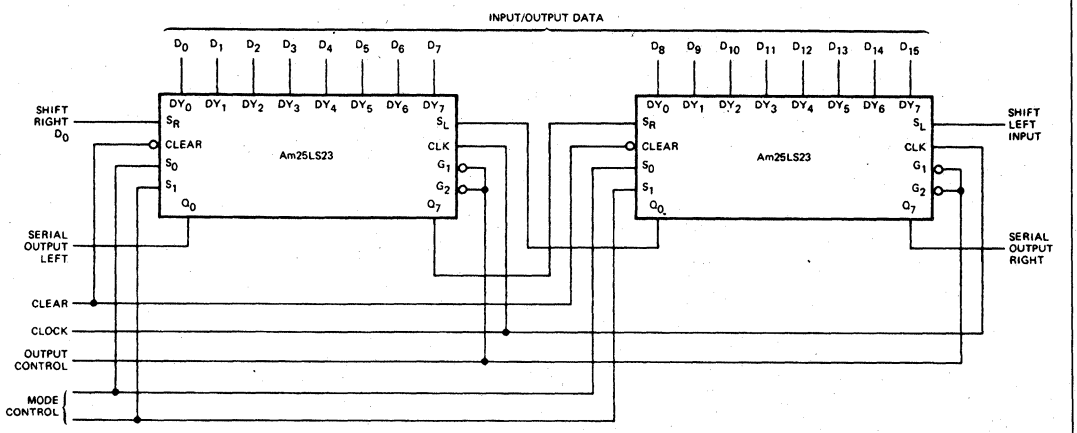
TRUTH TABLE

FUNCTION		INPUTS								OUTPUTS		INPUTS/OUTPUTS							
		S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$	$\overline{G}_2$	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	↑	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
M O D E	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Load (Note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedance ↑ = Transition LOW-to-HIGH
H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_1 are inputs.

APPLICATION



AF001110

16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State..... −0.5V to +V_{CC} max
DC Input Voltage S_0, S_1, $\overline{G}_1$, $\overline{G}_2$,
CLR, CP) ..... −0.5V to +7.0V
DC Input Voltage (Others) ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)				Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{OL}	Q_0, Q_7	I_{OH} = −440μA	MIL	2.5			Volts
					COM'L	2.7			
			DY_0-DY_7	MIL, I_{OH} = −1.0mA		2.4			
				COM'L, I_{OH} = −2.6mA		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA			0.25	0.4	Volts
				I_{OL} = 8.0mA			0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			S_0, S_1			−0.8	mA
					All others			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)			S_0, S_1			40	μA
					All others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	V_{IN} = 7V	S_0, S_1				0.2	mA
				$\overline{G}_1$, $\overline{G}_2$, CLR, CP				0.1	
			V_{IN} = 5.5V	Others				0.1	
I_{OZ}	Off-State (High Impedance) Output Current	V_{CC} = MAX.			V_O = 0.4V			−100	μA
					V_O = 2.4V			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)					38	60	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time.
4. I_{CC}-measured with clock input HIGH and output controls HIGH.

9

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q_0 or Q_7	C_L = 15pF, R_L = 2.0kΩ		18	26	ns
t_{PHL}				23	28	
t_{PLH}	Clock to DY_i			18	26	ns
t_{PHL}				21	28	
t_s	S_1, S_0 Set-up Prior to Clock		12			ns
t_s	DY_i or S_R, S_L Set-up Prior to Clock		12			ns
t_{PW}	Pulse Width (Clock)		15			ns
t_s	Clear to Clock		15			ns
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i			18	30	ns
t_{ZL}				20	30	
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$, to DY_i	C_L = 5.0pF, R_L = 2.0kΩ		22	33	ns
t_{HZ}				16	23	
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz

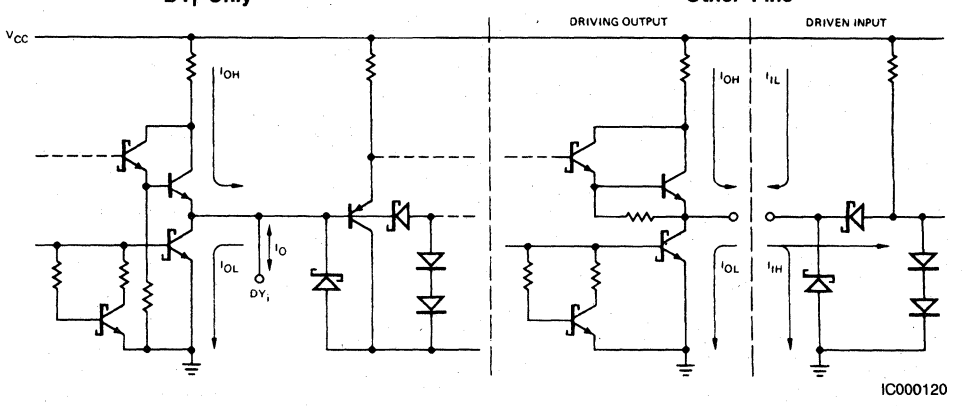
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to Q_0 or Q_7	C_L = 50pF, R_L = 2.0KΩ		38		44	ns
t_{PHL}				40		47	
t_{PLH}	Clock to DY_i			38		44	ns
t_{PHL}				40		47	
t_s	S_1, S_0 Set-up Prior to Clock		20		23		ns
t_s	DY_i, or S_R, S_L Set-up Prior to Clock		20		23		ns
t_{pw}	Pulse Width (Clock)		24		27		ns
t_s	Clear to Clock		24		27		ns
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i			43		50	ns
t_{ZL}				43		50	
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i	C_L = 5.0pF, R_L = 2.0KΩ		43		50	ns
t_{HZ}				30		35	
f_{max}	Maximum Clock Frequency (Note 1)		26		23		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25LS2513

Three-State Priority Encoder

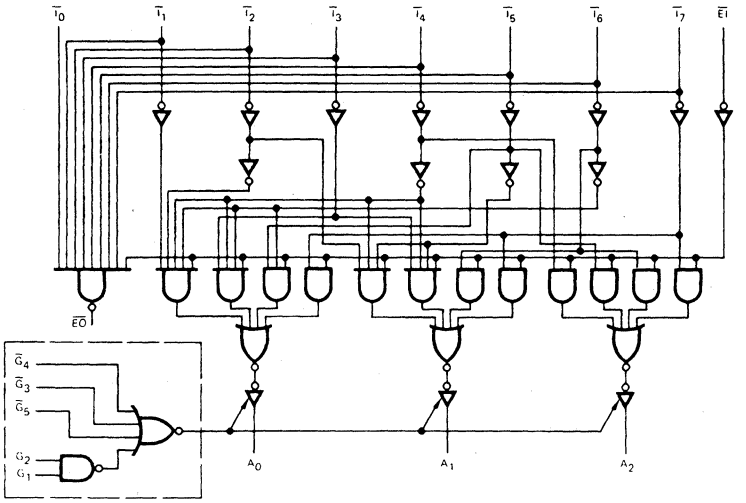
DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expandable
- Cascadable
- Three State inverted output version of Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing

GENERAL DESCRIPTION

The Am25LS2513 Low-Power Schottky Priority Encoder performs priority encoding of 8 inputs to provide a binary-weighted code of the priority order of the 3 tri-state active HIGH outputs A_0, A_1, A_2. Three active LOW and two active HIGH inputs in AND-OR configuration allow control of the tri-state outputs. The use of the input enable ($\overline{EI}$) combined with the enable output ($\overline{EO}$) permits cascading without additional circuitry. Enable input ($\overline{EI}$) HIGH will force all outputs LOW subject to the tri-state control. The enable output is LOW when all inputs $\overline{I_0}$ through $\overline{I_7}$ are HIGH and the enable input is LOW.

BLOCK DIAGRAM



BD001660

RELATED PRODUCTS

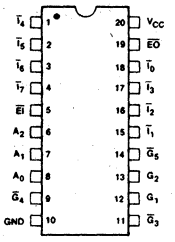
Part No.	Description
Am2913	Priority Interrupt Expander
Am2914	Vectored Priority Interrupt Controller

03609B

Refer to Page 13-1 for Essential Information on Military Devices

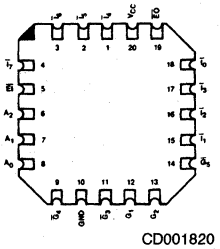
CONNECTION DIAGRAM
Top View

D-20-1



CD001810

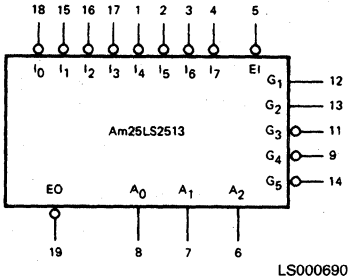
L-20-1



CD001820

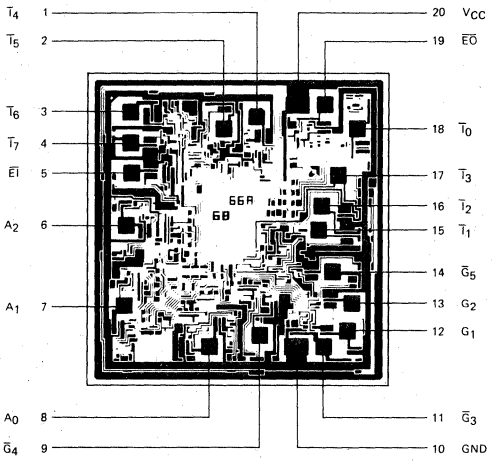
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000690

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.082 x 0.085

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2513 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2513** — Device type
  - 3-State Priority Encoder

Valid Combinations	
Am25LS2513	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
8, 7, 6	A0, A1, A2	O	Three-state, active high encoder outputs.
5	$\overline{EI}$	I	Enable input provided to allow cascaded operation.
19	$\overline{EO}$	O	Enable output provided to enable the next lower order priority chip.
12, 13	G_1, G_2	O	Active high three-state output controls.
11, 9, 14	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	O	Active low three-state output controls.
18,15,16, 17,1,2,3,4	$\overline{I}_{0-7}$	I	Active low encoder inputs.

TRUTH TABLES

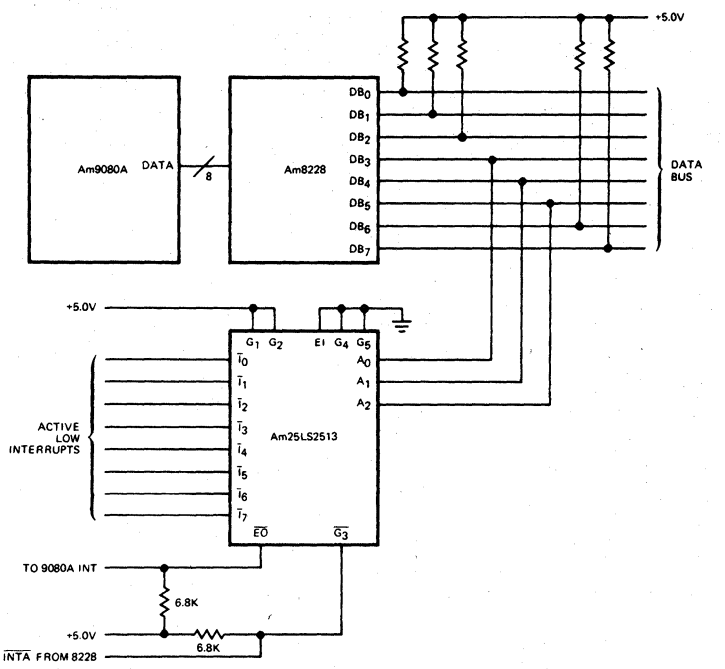
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

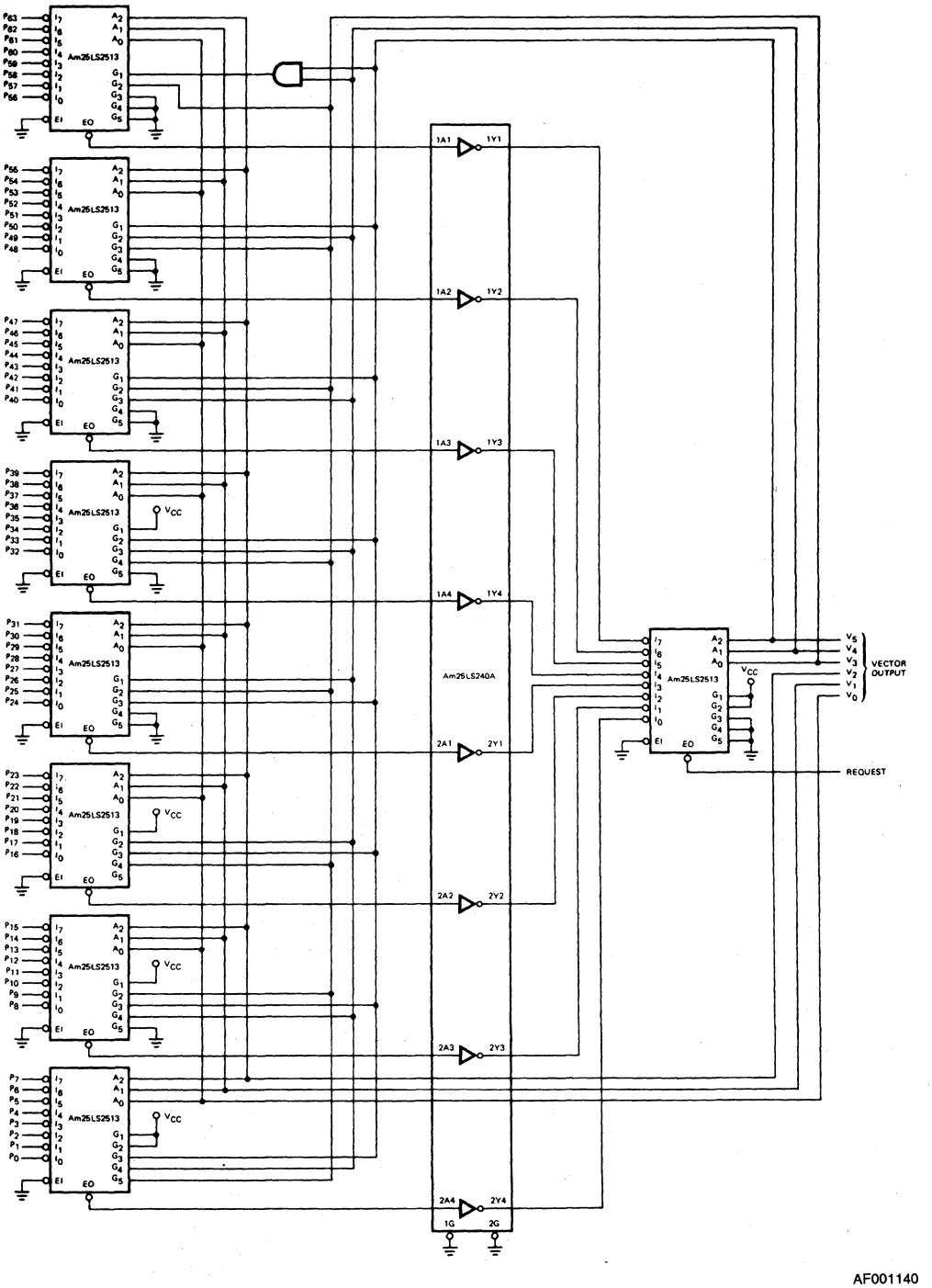
Z = HIGH Impedance

PRIORITY ENCODED RST INTERRUPT INSTRUCTION FOR THE Am9080A



AF001070

APPLICATION



64 Input Priority Encoder Connected for Parallel Enable

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	A_i	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −2.6mA	2.4	3.2		
			$\overline{EO}$, I_{OH} = −440μA	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA(A_n Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{E1}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, $\overline{I}_0$				−0.4	mA
			All others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	$\overline{E1}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, $\overline{I}_0$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	$\overline{E1}$, G_1, G_2, $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$, I_0				0.1	mA
			All others				0.2	
I_O	Off-State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)	$C_L = 15pF$ $R_L = 2.0k\Omega$		17	25	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)			11	17	ns
t_{PHL}				12	18	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			7.0	11	ns
t_{PHL}				24	36	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			11	17	ns
t_{PHL}				23	34	
t_{PLH}	$\overline{EI}$ to A_n			12	18	ns
t_{PHL}				14	21	
t_{ZH}	G_1 or G_2 to A_n			23	40	ns
t_{ZL}				20	37	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			20	30	ns
t_{ZL}				18	27	
t_{HZ}	G_1 or G_2 to A_n	$C_L = 5.0pF$ $R_L = 2.0k\Omega$		17	27	ns
t_{LZ}				19	28	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			16	24	ns
t_{LZ}				18	27	

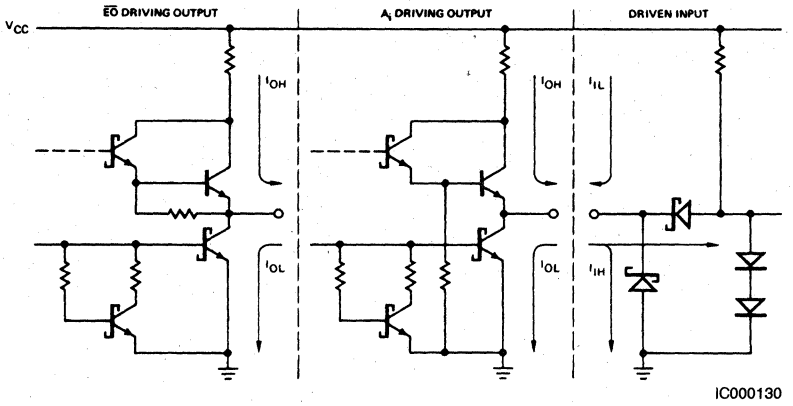
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	Am25LS COMMERCIAL		Am25LS MILITARY		Units
			Min	Max	Min	Max	
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)	$C_L = 50pF$ $R_L = 2.0k\Omega$		31		37	ns
t_{PHL}				30		34	
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)			22		27	ns
t_{PHL}				22		25	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			15		18	ns
t_{PHL}				48		60	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			19		21	ns
t_{PHL}				46		57	
t_{PLH}	$\overline{EI}$ to A_n			22		25	ns
t_{PHL}				27		32	
t_{ZH}	G_1 or G_2 to A_n			42		49	ns
t_{ZL}				43		49	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			36		43	ns
t_{ZL}				35		43	
t_{HZ}	G_1 or G_2 to A_n	$C_L = 5.0pF$ $R_L = 2.0k\Omega$		34		40	ns
t_{LZ}				34		40	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n			30		35	ns
t_{LZ}				31		35	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25LS381/Am54LS381/Am74LS381
Am25LS2517

Arithmetic Logic Unit/Function Generator Low-Power Schottky Integrated Circuits

DISTINCTIVE CHARACTERISTICS

- Three arithmetic functions
- Three logic functions
- Preset and clear functions
- Carry output (C_{n+4}) and overflow (OVR) outputs on Am25LS2517
- Generate and propagate outputs for full lookahead carry on Am25LS381
- 8mA sink current over the military temperature range on Am25LS
- 50mV Improved V_{OL} on Am25LS compared to Am54LS/74LS
- 440μA source current at HIGH output.

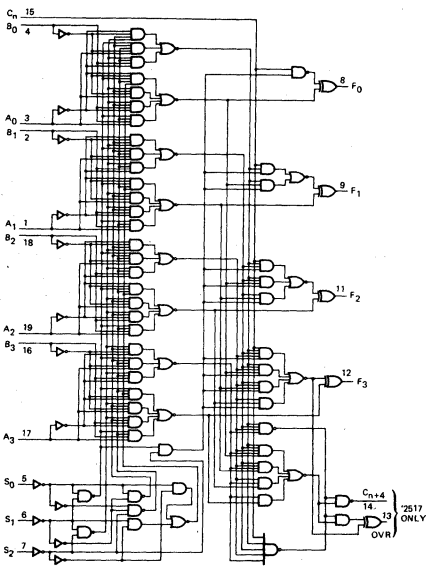
GENERAL DESCRIPTION

The Am25LS381 and Am54LS/74LS381 are arithmetic logic units (ALU)/function generators that perform three arithmetic operations and three logic operations on two 4-bit words. The device can also output forced 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry lookahead is used over the four-bit field within the device. When devices are cascaded, multi-level full carry lookahead is implemented using a '182 carry lookahead generator and the $\overline{G}$ and $\overline{P}$ outputs on the Am25LS381 or Am54LS/74LS381. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. If the C_{n+4} carry output function is required, the Am25LS2517 should be used.

The Am25LS381 is a high-performance version of the Am54LS/74LS381. Improvements include faster A.C. specifications, higher noise margin and twice the fan-out over the military temperature range.

The Am25LS2517 is an arithmetic logic unit (ALU)/function generator that performs three arithmetic operations and three logic operations on two 4-bit words. The device can also force output 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry lookahead is used over the four-bit field within the device. When devices are cascaded, the carry output (C_{n+4}) is connected to the carry input (C_n) of the next device. The Am25LS2517 can also detect two's complement overflow. The overflow output (OVR) is defined logically as $C_{n+3} \oplus C_{n+4}$.

BLOCK DIAGRAM



BD001790

03728B

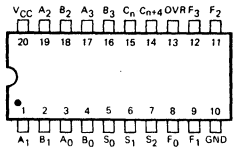
Refer to Page 13-1 for Essential Information on Military Devices

RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice
Am2903	Bit Slice
Am29203	Super Slice
Am29501	Multiport Pipeline Processor

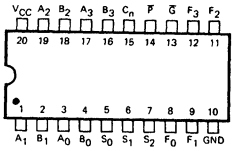
CONNECTION DIAGRAM
Top View

Am25LS2517



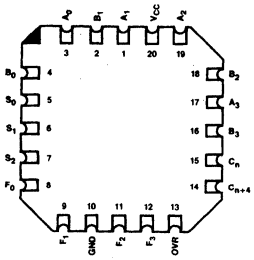
CD004040

Am25LS381
Am54LS/74LS381



CD004030

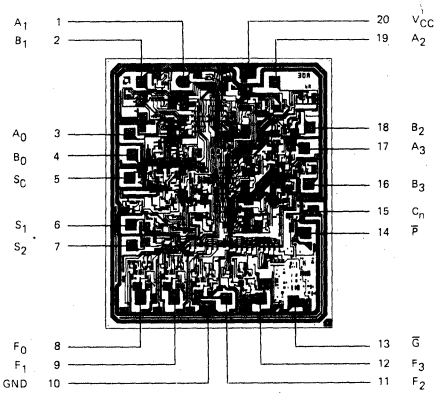
Leadless Chip Carriers
L-20-1



CD004020

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.091" x 0.108"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS381
Am25LS2517 **D** **C** **B**

- Screening Option
  - Blank – Standard processing
  - B – Burn-in
- Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless Chip-Pak
  - P – 20-pin plastic DIP
  - X – Dice
- Device type
  - ALU Function Generators

Valid Combinations	
Am25LS381	PC, PCB DC, DCB, DM, DMB FM, FMB XC, XM
Am25LS2517	PC, PCB DC, DCB, DM, DMB FM, FMB LC, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 1, 19, 17	A_0, A_1, A_2, A_3	I	The A data inputs.
4, 2, 18, 16	B_0, B_1, B_2, B_3	I	The B data inputs.
	S_0, S_1, S_2, S_3	I	The control inputs used to determine the arithmetic or logic function performed.
	F_0, F_1, F_2, F_3	O	The data outputs of the ALU.
16	C_n	I	The carry-in input of the ALU.
	C_{n+4}	O	The carry-lookahead output of the four-bit input field.
13	$\overline{G}$	O	The carry-generate output for use in multi-level lookahead schemes.
14	$\overline{P}$	O	The carry-propagate output for use in multi-level lookahead schemes.
13	OVR		Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

FUNCTION TABLE

Selection			Arithmetic/Logic Operation
S_2	S_1	S_0	
L	L	L	Clear
L	L	H	B Minus A
L	H	L	A Minus B
L	H	H	A Plus B
H	L	L	A⊕B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset

H = High Level, L = Low Level
See Truth Table for full description.

GUARANTEED LOADING RULES OVER OPERATING RANGE
(In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am25LS				Am54LS/74LS			
			Output HIGH	Output LOW			Output HIGH	Output LOW	
Pin Nos.	Input/Output	Input Load	−440μA	MIL	COM'L	Input Load	−440μA	MIL	COM'L
1	A_1	4.0	–	–	–	4.4	–	–	–
2	B_1	4.0	–	–	–	4.4	–	–	–
3	A_0	4.0	–	–	–	4.4	–	–	–
4	B_0	4.0	–	–	–	4.4	–	–	–
5	S_0	1.0	–	–	–	1.1	–	–	–
6	S_1	1.0	–	–	–	1.1	–	–	–
7	S_2	1.0	–	–	–	1.1	–	–	–
8	F_0	–	22	22	22	–	20	11	22
9	F_1	–	22	22	22	–	20	11	22
10	GND	–	–	–	–	–	–	–	–
11	F_2	–	22	22	22	–	20	11	22
12	F_3	–	22	22	22	–	20	11	22
13	$\overline{G}$ or OVR*	–	22	44	44	–	20	44	44
14	$\overline{P}$ or C_{n+4}	–	22	22	22	–	20	11	22
15	C_n	3.0**	–	–	–	4.4	–	–	–
16	B_3	4.0	–	–	–	4.4	–	–	–
17	A_3	4.0	–	–	–	4.4	–	–	–
18	B_2	4.0	–	–	–	4.4	–	–	–
19	A_2	4.0	–	–	–	4.4	–	–	–
20	V_{CC}	–	–	–	–	–	–	–	–

*OVR Drive is 22 Unit Loads.

**4.0 for Am25LS2517.

Am25LS/54LS/74LS381
TEST TABLE

Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5V	GND	4.5V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	All A's & B's	–	out-of-phase
C_n	F_i	1	0	0	–	B_i	A_i	All A's & B's	–	in-phase
A_i	$\overline{G}$	1	1	0	X	B_i	–	All B's	All A's	out-of-phase
B_i	$\overline{G}$	1	1	0	X	A_i	–	All B's	All A's	out-of-phase
A_i	$\overline{P}$	X	X	1	X	B_i	–	All A's & B's	–	out-of-phase
B_i	$\overline{P}$	1	1	0	X	–	A_i	All B's	All A's	out-of-phase
A_i	F_i	0	1	0	0	–	B_i	–	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	–	A's & B's	in-phase
B_i	F_i	0	1	0	0	–	A_i	–	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	–	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	–	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	$\overline{G}$	–	1	0	X	–	–	A's & B's	–	out-of-phase
S_0	$\overline{P}$	–	1	0	X	–	–	All B's	All A's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	$\overline{G}$	1	–	0	X	–	–	A's & B's	–	out-of-phase
S_1	$\overline{P}$	1	–	0	X	–	–	All A's	All B's	out-of-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	out-of-phase
S_2	$\overline{G}$	1	1	–	X	–	–	A's & B's	–	in-phase
S_2	$\overline{P}$	1	1	–	X	–	–	All A's	All B's	in-phase

X = Don't care

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Am25LS/54LS/74LS381
TRUTH TABLE

FUNCTION	INPUTS						OUTPUTS					
	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

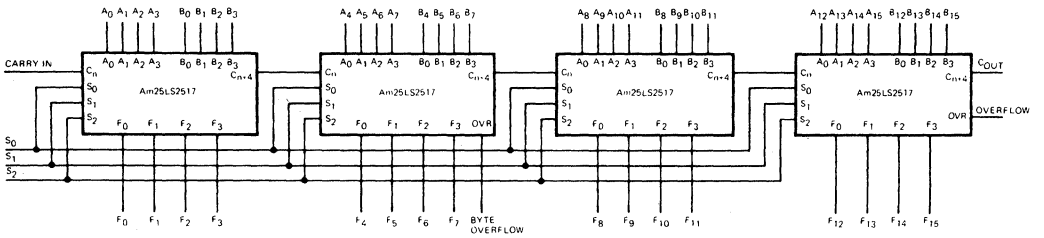
Am25LS2517
TEST TABLE

Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5V	GND	4.5V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	A's & B's	None	out-of-phase
C_n	F_i	1	0	0	–	B_i	A_i	A's & B's	None	in-phase
A_i	F_i	0	1	0	0	–	B_i	None	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	None	A's & B's	in-phase
A_i	OVRF	0	1	1	1	B_i	–	A's & B's	None	in-phase
A_i	C_{n+4}	0	1	1	1	B_i	–	A's & B's	None	in-phase
B_i	F_i	0	1	0	0	–	A_i	None	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
B_i	OVRF	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
B_i	C_{n+4}	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	None	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	None	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	OVRF	–	1	1	0	–	–	None	A's & B's	out-of-phase
S_0	C_{n+4}	–	1	1	0	–	–	None	A's & B's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	OVRF	0	–	1	X	–	–	None	A's & B's	in-phase
S_1	C_{n+4}	0	–	1	X	–	–	None	A's & B's	in-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	in-phase
S_2	OVRF	0	1	–	0	–	–	None	A's & B's	out-of-phase
S_2	C_{n+4}	0	1	–	0	–	–	None	A's & B's	in-phase

Am25LS2517
TRUTH TABLE

FUNCTION	INPUTS						OUTPUTS					
	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	0	0	0	1	1
				1	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	1	1
				1	1	1	0	0	0	0	1	1
A + B	1	0	1	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	0	0	0	0	0	0	0	1	1
				0	0	1	0	0	0	0	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	1	1
				1	0	1	0	0	0	0	0	0
				1	1	0	0	0	0	0	1	1
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	0	0	0	1	1	1	1	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	1	1	1	1	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

APPLICATIONS

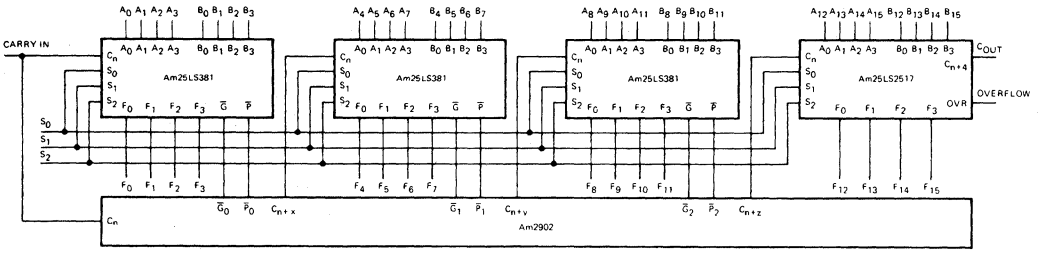


AF001430

TYPICAL SPEED CALCULATIONS

Path	Output	
	F	$C_n + 4$, OVR
A_i or B_i to C_{n+4}	24 ns	24 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to F_i	16 ns	–
C_n to C_{n+4}, OVR	–	15 ns
16-Bit Speed	70 ns	69 ns

The Am25LS2517 in a 16-Bit Ripple Carry ALU Connection.



AF001420

TYPICAL SPEED CALCULATIONS

Path	Output	
	F	$C_n + 4$, OVR
A_i or B_i to $\overline{G}$ or $\overline{P}$	20 ns*	20 ns*
$\overline{G}_i$ or $\overline{P}_i$ to C_{i+j} (Am2902)	8 ns	8 ns
C_n to F	16 ns	–
C_n to C_{n+4}, OVR	–	15 ns
16-Bit Speed	44 ns	43 ns

* Note that S_i to G or P may be longer path.

The Am25LS2517 and Am25LS381 in a 16-Bit Carry Lookahead ALU Connection.

USER NOTES

1. Throughout this data sheet, the active HIGH input and output terminology has been used.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in (C_n = HIGH) for the active HIGH case.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage (Except Am25LS2517,
C_N input = 5.5V) ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am25LS381 • Am25LS2517

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −440μA, V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			$\overline{G}$, I_{OL} = 16mA				0.55	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		Any S			−0.36	mA
				Any A or B			−1.44	
				'LS381, C_n			−1.08	
				'LS2517, C_n			−1.44	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		Any S			20	μA
				Any A or B			80	
				'LS381, C_n			60	
				'LS2517, C_n			80	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V		Any S			0.1	mA
				Any A or B			0.4	
				'LS381, C_n			0.3	
		V_{CC} = MAX, V_{IN} = 5.5V		'LS2517, C_n			0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	MIL	Am25LS381			40	mA
				Am25LS2517			43	
			COM'L	Am25LS381		25	43	
				Am25LS2517		27	47	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: S_0 = S_1 = S_2 = GND, all other inputs open.
LS2517: S_0 = C_n = open, all other inputs = GND.

DC CHARACTERISTICS over operating range unless otherwise specified

AM54LS/74LS381

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			74LS only, I_{OL} = 8mA			0.5	
			$\overline{P}$, I_{OL} = 8.0mA			0.5	
			$\overline{G}$, I_{OL} = 16mA			0.65	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current (Note 5)	V_{CC} = MAX, V_{IN} = 0.4V	Any S			−0.4	mA
			Others			−1.6	
I_{IH}	Input HIGH Current (Note 5)	V_{CC} = MAX, V_{IN} = 2.7V	Any S			20	μA
			Others			80	
I_I	Input HIGH Current (Note 5)	V_{CC} = MAX, V_{IN} = 7.0V	Any S			0.1	mA
			Others			0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			25	43	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: S_0 = S_1 = S_2 = GND, all other inputs open.
   LS2517: S_0 = C_n = open, all other inputs = GND.
5. Limits chosen by AMD based on SN545/74S381, T, I, LS data unavailable.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Am25LS Min	Am25LS Typ	Am25LS Max	Am54LS/74LS Min	Am54LS/74LS Typ	Am54LS/74LS Max	Units
t_{PLH}	C_n to F_i	C_L = 15pF, R_L = 2.0kΩ		14	21			26	ns
t_{PHL}				16	24			30	
t_{PLH}	A_i to B_i to F_i			16	24			30	ns
t_{PHL}				23	35			40	
t_{PLH}	S_i to F_i			20	30			35	ns
t_{PHL}				25	37			40	
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)			20	30			35	ns
t_{PHL}				15	23			30	
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)			17	26			34	ns
t_{PHL}				15	23			30	
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)			32	48			55	ns
t_{PHL}				23	35			42	
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)			23	34			–	ns
t_{PHL}				24	36			–	
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)			21	32			–	ns
t_{PHL}				24	36			–	
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)			27	41			–	ns
t_{PHL}				37	55			–	
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)			14	21			–	ns
t_{PHL}				15	22			–	
t_{PLH}	C_n to OVR ('LS2517 Only)			15	22			–	ns
t_{PHL}				15	22			–	

9

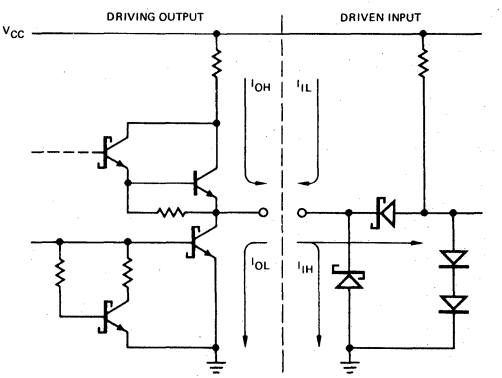
Am25LS only

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	C_n to F_i	C_L = 50pF, R_L = 2.0KΩ		27		30	ns
t_{PHL}				35		42	
t_{PLH}	A_i or B_i to F_i			32		36	ns
t_{PHL}				44		50	
t_{PLH}	S_i to F_i			38		42	ns
t_{PHL}				48		55	
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)			37		40	ns
t_{PHL}				31		36	
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)			34		39	ns
t_{PHL}				34		42	
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)			57		63	ns
t_{PHL}				47		55	
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)			41		45	ns
t_{PHL}				47		55	
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)			38		40	ns
t_{PHL}				46		52	
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)			52		60	ns
t_{PHL}				66		75	
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)			28		32	ns
t_{PHL}				28		30	
t_{PLH}	C_n to OVR ('LS2517 Only)			30		35	ns
t_{PHL}				28		30	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS/Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000180

Note: Actual current flow direction shown.

Am25LS2518

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-Power Schottky version of the popular Am2918 and Am25S18
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388

GENERAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

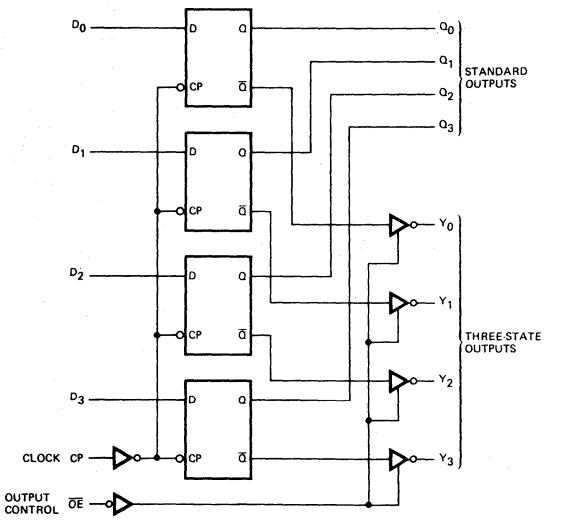
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

BLOCK DIAGRAM



BD001510

RELATED PRODUCTS

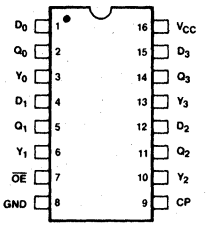
Part No.	Description
Am25S18	Quad D Register
Am2918	Quad D Register
Am29LS18	Quad D Low Power Register
Am29LS2519	Quad D Low Power Register

03618B

Refer to Page 13-1 for Essential Information on Military Devices

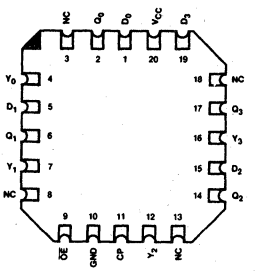
CONNECTION DIAGRAM
Top View

D-16, P-16



CD001670

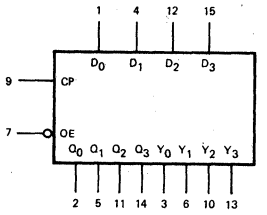
L-20-1



CD001660

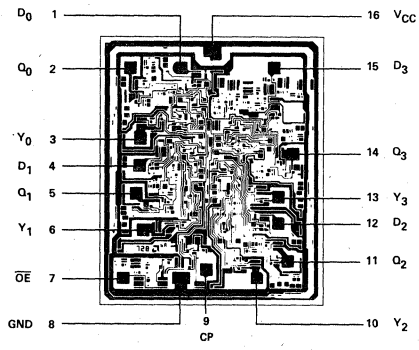
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000580

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083″ x 0.099″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2518 D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 16-pin CERDIP; F– 16-pin flatpak; L– 20-pin leadless chip carrier; P– 16-pin plastic DIP; X– Dice
- Am25LS2518 — Device type: Quad D Register

Valid Combinations	
Am25LS2518	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

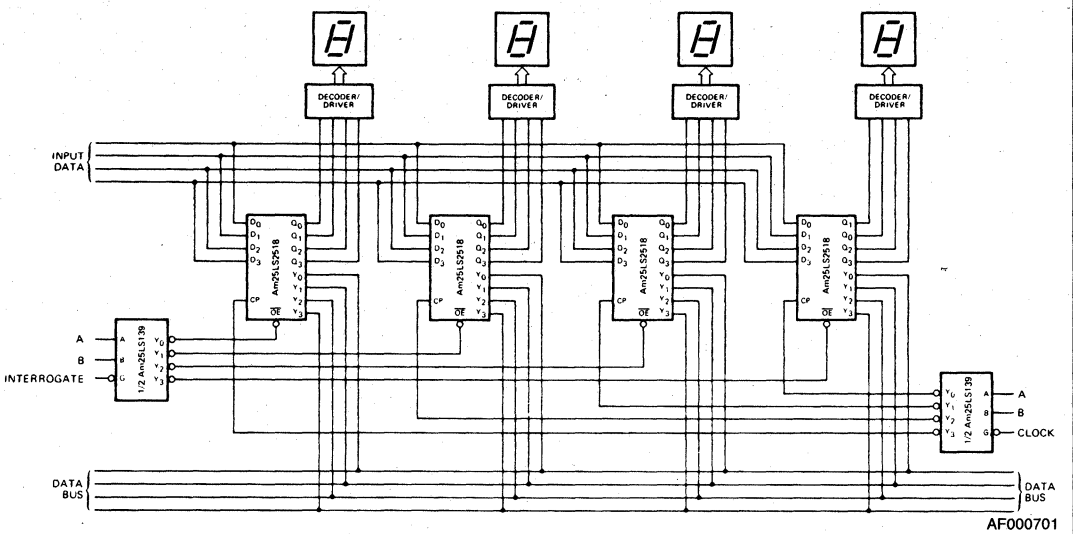
Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP	I	Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

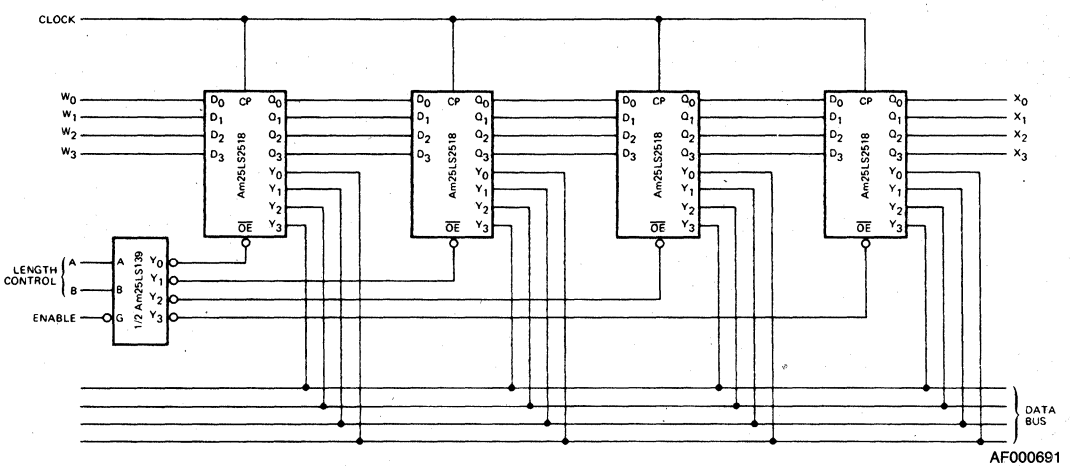
INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW NC = No change
H = HIGH ↑ = LOW-to-HIGH transition
X = Don't care Z = High-Impedance
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

APPLICATIONS



The Am25LS2518 used as display register with bus interrogate capability.



The Am25LS2518 as a variable length (1, 2, 3 or 4 word) shift register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q, I_{OH} = −660μA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, I_{OH} = −1.0mA	2.4	3.4		
				COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX				17	28	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q_i		$C_L = 15pF$ $R_L = 2.0k\Omega$		18	27	ns
t_{PHL}					18	27	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				18	27	ns
t_{PHL}					18	27	
t_{pw}	Clock Pulse Width	LOW		18			ns
		HIGH		15			
t_s	Data			15			ns
t_h	Data			5.0			ns
t_{ZH}	$\overline{OE}$ to Y_i				7.0	11	ns
t_{ZL}					8	12	
t_{HZ}	$\overline{OE}$ to Y_i		$C_L = 5.0pF$ $R_L = 2.0k\Omega$		14	21	ns
t_{LZ}					12	18	
f_{max}	Maximum Clock Frequency (Note 1)			35	50		MHz

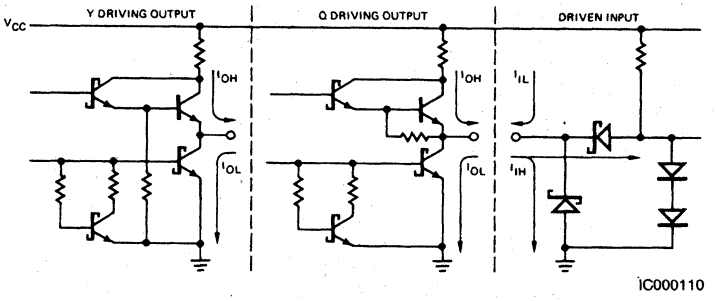
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS2518 Min	COMMERCIAL Am25LS2518 Max	MILITARY Am25LS2518 Min	MILITARY Am25LS2518 Max	Units
t_{PLH}	Clock to Q_i		$C_L = 50pF$ $R_L = 2.0k\Omega$		38		45	ns
t_{PHL}					38		45	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				35		40	ns
t_{PHL}					35		40	
t_{pw}	Clock Pulse Width	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			5.0		5.0		ns
t_{ZH}	$\overline{OE}$ to Y_i				15		17	ns
t_{ZL}					16		17	
t_{HZ}	$\overline{OE}$ to Y_i		$C_L = 5.0pF$ $R_L = 2.0k\Omega$		27		30	ns
t_{LZ}					24		30	
f_{max}	Maximum Clock Frequency (Note 1)			30		25		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2518
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25LS2519

Quad Register with Two Independently Controlled Three-State Outputs

DISTINCTIVE CHARACTERISTICS

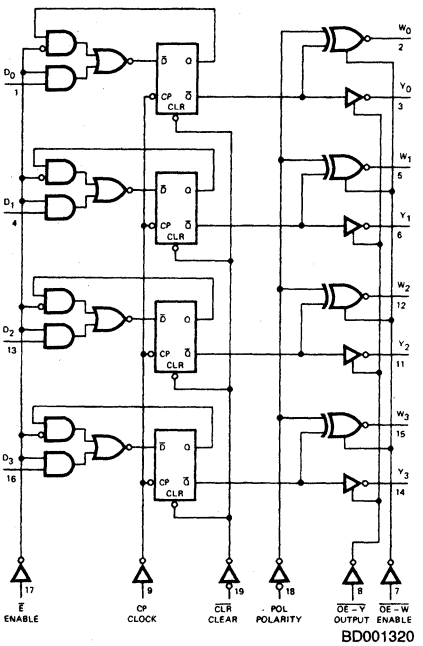
- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

GENERAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements on the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



BD001320

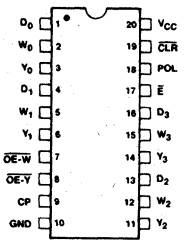
RELATED PRODUCTS

Part No.	Description
Am25S18, Am2918	Quad D Register
Am25LS2518	Quad D Register

03660B

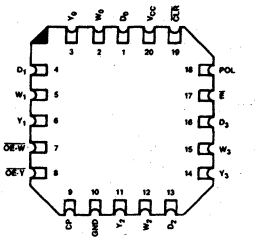
CONNECTION DIAGRAM
Top View

D-20-1



CD001870

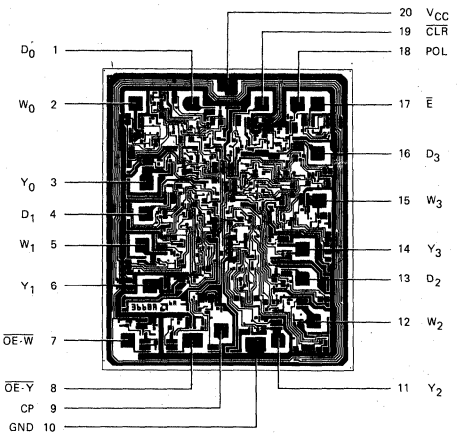
L-20-1



CD001880

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2519 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- Am25LS2519 — Device type: Quad D Register

Valid Combinations	
Am25LS2519	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	Any of the four D flip-flop data lines.
17	$\overline{E}$	I	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
9	CP	I	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
7, 8	$\overline{OE}$-W, $\overline{OE}$-Y	O	Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set.
	Y_i	O	Any of the four non-inverting three-state output lines.
	W_i	O	Any of the four three-state outputs with polarity control.
18	POL	O	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
19	$\overline{CLR}$	I	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

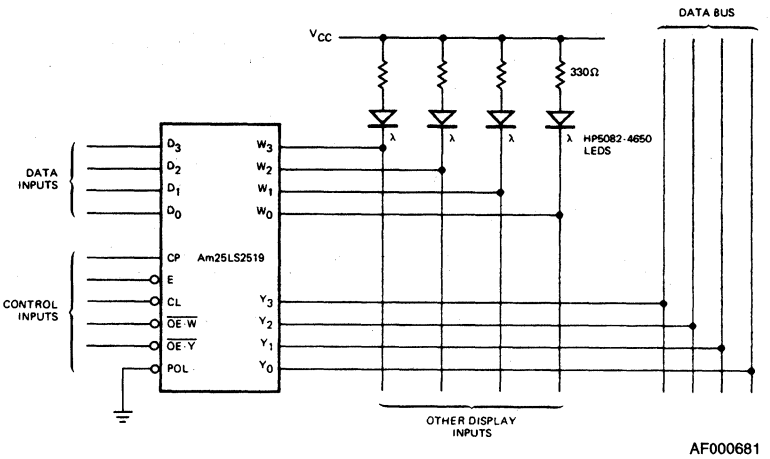
FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE}$-W	$\overline{OE}$-Y	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW
H = HIGH
Z = High-Impedance

X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

APPLICATION



AF000681

Convenient Register Content Monitor or Test Point

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	MIL		24	36	mA
			COM'L		24	39	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Clock to Y_i		C_L = 15pF R_L = 2.0kΩ		22	33	ns
t_{PHL}					20	30	
t_{PLH}	Clock to W_i (Either Polarity)				24	36	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y_i				29	43	ns
t_{PLH}	Clear to W_i				25	37	ns
t_{PHL}					30	45	
t_{PLH}	Polarity to W_i				23	34	ns
t_{PHL}					25	37	
t_{pw}	Clear			18			ns
t_{pw}	Clock Pulse Width	LOW		15			ns
		HIGH		18			
t_s	Data			15			ns
t_h	Data			5			ns
t_s	Data Enable			20			ns
t_h	Data Enable			0			ns
t_s	Set-up Time, Clear Recovery (Inactive) to clock			20	15		ns
t_{ZH}	Output Enable to W or Y				11	17	ns
t_{ZL}					13	20	
t_{HZ}	Output Enable to W or Y		C_L = 5.0pF R_L = 2.0kΩ		13	20	ns
t_{LZ}					11	17	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 15pF R_L = 2.0kΩ	35	45		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

				COMMERCIAL		MILITARY		
				Am25LS2519		Am25LS2519		
Parameters	Description		Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	Clock to Y_i		C_L = 50pF R_L = 2.0kΩ		39		42	ns
t_{PHL}					39		45	
t_{PLH}	Clock to W_i (Either Polarity)				41		43	ns
t_{PHL}					44		48	
t_{PHL}	Clear to Y_i				52		58	ns
t_{PLH}	Clear to W_i				42		43	ns
t_{PHL}					51		53	
t_{PLH}	Polarity to W_i				41		45	ns
t_{PHL}					42		44	
t_{pw}	Clear			20		20		ns
t_{pw}	Clock	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			10		10		ns
t_s	Data Enable			25		25		ns
t_h	Data Enable			0		0		ns
t_s	Set-up Time, Clear Recovery (Inactive) to Clock			23		24		ns
t_{ZH}	Output Enable to W_i or Y_i				24		27	
t_{ZL}					29		35	
t_{HZ}	Output Enable to W_i or Y_i		C_L = 5.0pF R_L = 2.0kΩ		33		45	ns
t_{LZ}					22		26	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 5.0pF R_L = 2.0kΩ	30		25		MHz

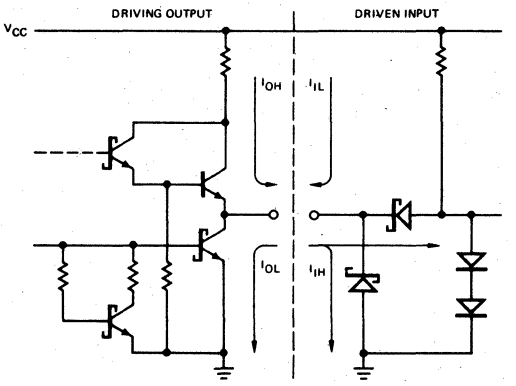
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

9

03660B

Refer to Page 13-1 for Essential Information on Military Devices

Am25LS2519
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am25LS2520

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- Am25LS Family offers improved sink current, source current and noise margin

GENERAL DESCRIPTION

The Am25LS2520 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

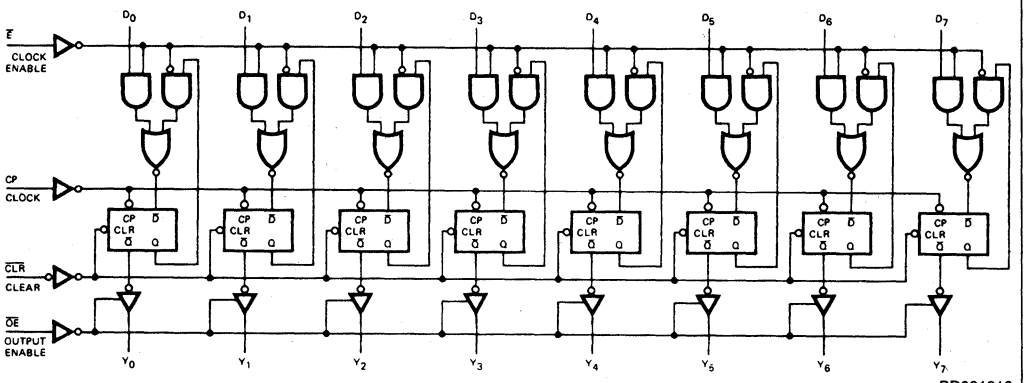
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package and in a 24-pin flatpack.

BLOCK DIAGRAM



BD001310

RELATED PRODUCTS

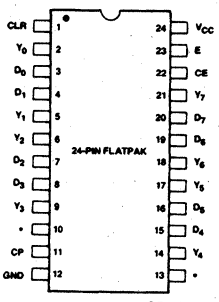
Part No.	Description
Am25S18	Quad D Register
Am2920	Octal D-Type Flip-flop
Am2954/5	Octal D Registers

03698B

Refer to Page 13-1 for Essential Information on Military Devices

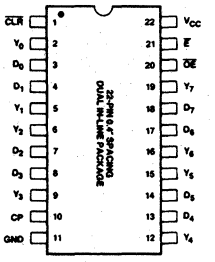
CONNECTION DIAGRAM
Top View

F-24



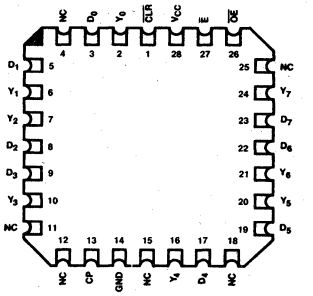
CD001910

D-22, P-22



CD001900

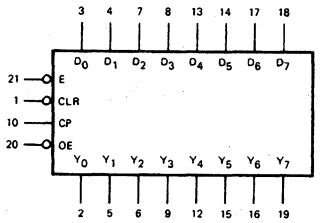
L-28-1



CD004900

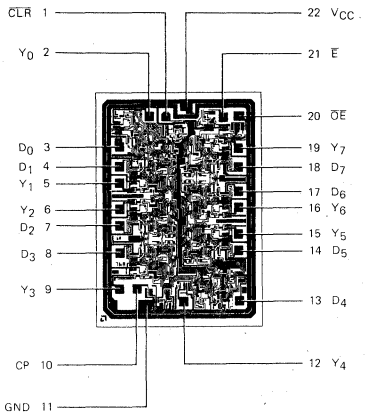
Note: Pin 1 is marked for orientation
*Reserved – do not use.

LOGIC SYMBOL



LS000720

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.111"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2520 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D– 22-pin CERDIP
  - F– 24-pin flatpak
  - L– 28-pin leadless chip carrier
  - P– 22-pin plastic DIP
  - X– Dice
- Am25LS2520 — Device type
  - Octal D-type Flip-Flop

Valid Combinations	
Am25LS2520	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{CLR}$	I	When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.
11	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i	O	The register three-state outputs.
21	$\overline{E}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
20	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

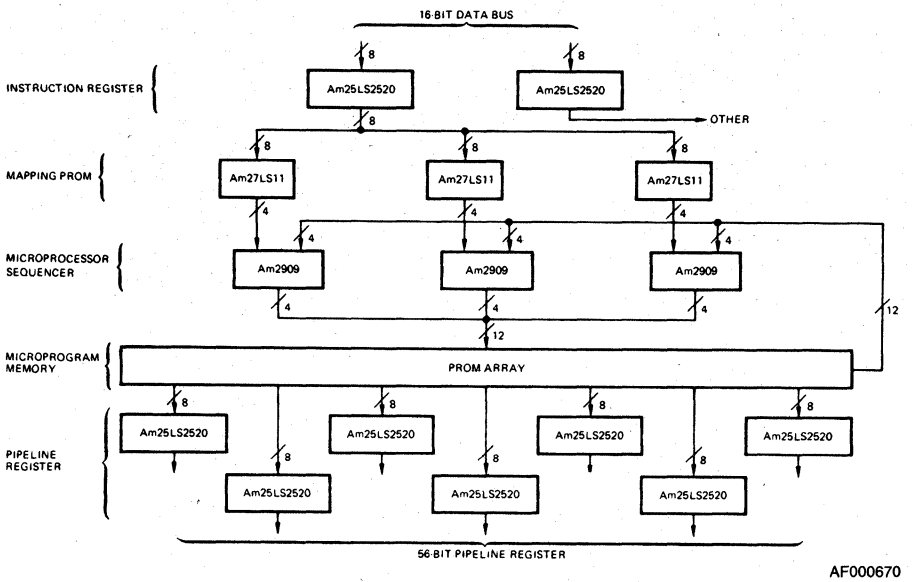
FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

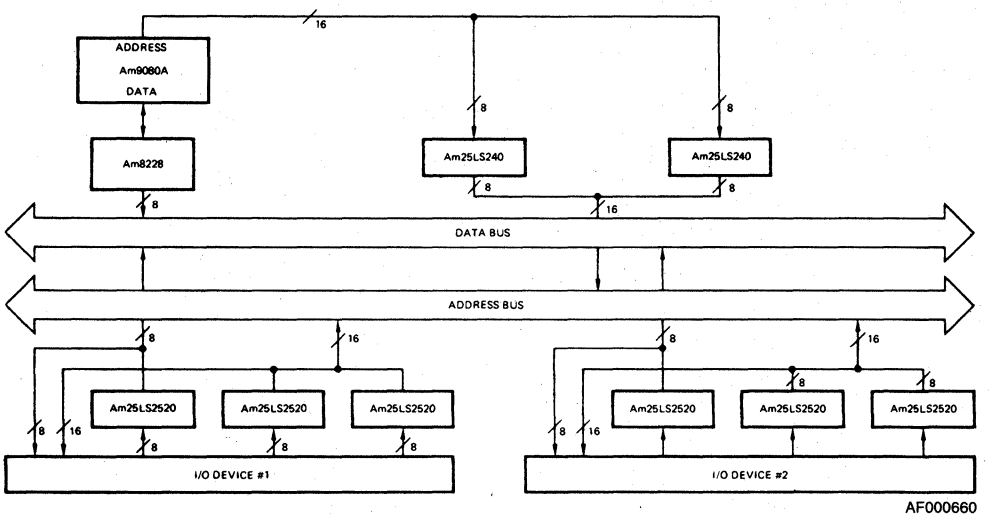
H = HIGH
L = LOW
NC = No change

↑ = LOW-to-HIGH Transition
X = Don't Care
Z = High-Impedance

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.



The Am25LS2520 is a useful device in interfacing with the Am9080A system buses.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			24	37	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 15pF R_L = 2.0kΩ		18	27	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y				22	35	ns
t_s	Data (D_i)			10	3		ns
t_h	Data (D_i)			10	3		ns
t_s	Enable ($\overline{E}$)	Active		15	10		ns
		Inactive		20	12		
t_h	Enable ($\overline{E}$)			0	0		ns
t_s	Clear Recovery (In-Active) to Clock			11	7		ns
t_w	Clock	HIGH		20	14		ns
		LOW		25	13		
t_{pw}	Clear			20	13		ns
t_{ZH}	$\overline{OE}$ to Y_i				9	13	ns
t_{ZL}					14	21	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		20	30	ns
t_{LZ}					24	36	
f_{max}	Maximum Clock Frequency (Note 1)				40		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

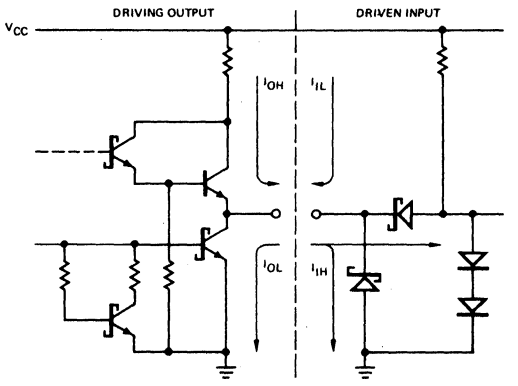
Parameters	Description		Test Conditions	COMMERCIAL Am25LS2520 Min	COMMERCIAL Am25LS2520 Max	MILITARY Am25LS2520 Min	MILITARY Am25LS2520 Max	Units
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 50pF R_L = 2.0kΩ		33		39	ns
t_{PHL}					45		54	
t_{PHL}	Clear to Y				43		51	ns
t_s	Data (D_i)			12		15		ns
t_h	Data (D_i)			12		15		ns
t_s	Enable ($\overline{E}$)	Active		17		20		ns
		Inactive		20		23		
t_h	Enable ($\overline{E}$)			0		0		ns
t_s	Clear Recovery (In-Active) to Clock			13		15		ns
t_{pw}	Clock	HIGH		25		30		ns
		LOW		30		35		
t_{pw}	Clear			22		25		ns
t_{ZH}	$\overline{OE}$ to Y_i				19		25	ns
t_{ZL}					30		39	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		35		40	ns
t_{LZ}					39		42	
f_{max}	Maximum Clock Frequency (Note 1)			25		20		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

03698B

Refer to Page 13-1 for Essential Information on Military Devices

Am25LS2520
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am25LS2521

Eight-Bit Equal-to Comparator

DISTINCTIVE CHARACTERISTICS

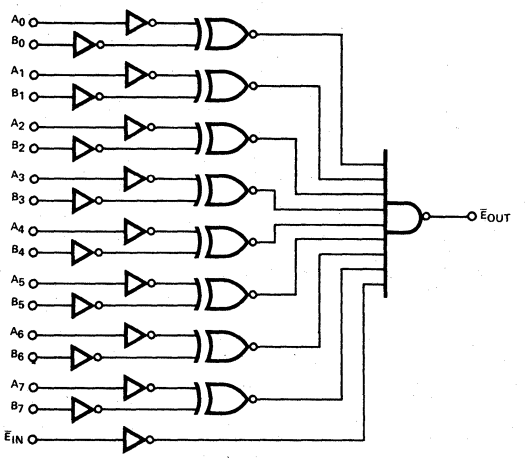
- 8-bit byte oriented equal comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- t_{pd} A · B to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package

GENERAL DESCRIPTION

The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ Y(A6 \odot B6)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. A_0 can be compared with B_0 at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

BLOCK DIAGRAM



BD001390

RELATED PRODUCTS

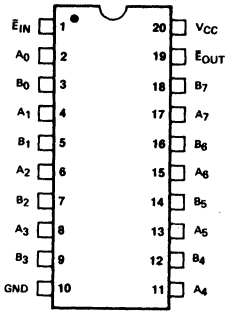
Part No.	Description
Am29806	Chip Select Decoder
Am29809	9-Bit Comparator

03619B

Refer to Page 13-1 for Essential Information on Military Devices

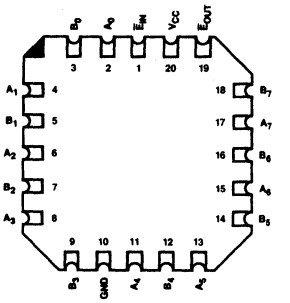
CONNECTION DIAGRAM
Top View

D-20-1



CD001610

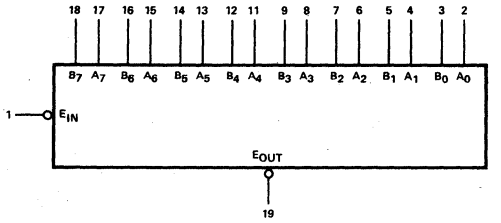
L-20-1



CD001600

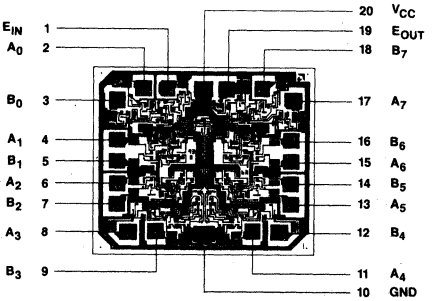
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000530

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.068″ x 0.058″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2521 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- Am25LS2521 — Device type
  - 8-Bit Equal-to-Comparator

Valid Combinations	
Am25LS2521	PC DC, DM FM LC, LM XC, XM

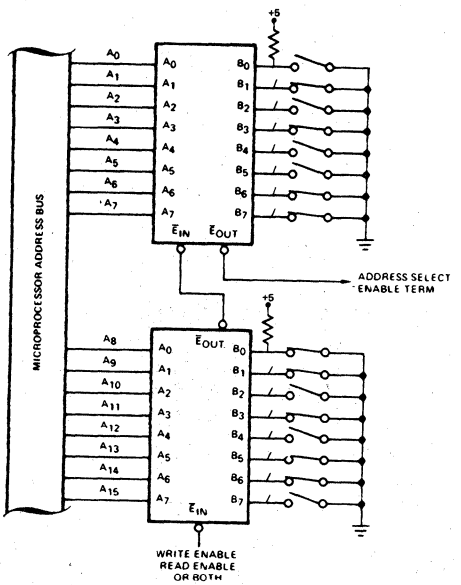
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_0-A_7	I	A input to comparator.
	B_0-B_7	I	B input to comparator.
1	$\overline{E}_{IN}$	I	Enable active LOW.
19	$\overline{E}_{OUT}$	O	$\overline{EQUAL}$ output active LOW.

APPLICATION



AF000651

MAX, $\overline{ENABLE}$ (HIGH-to-LOW) DELAY OVER 16-BITS
(Commercial Range)

t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$	19ns
t_{PHL}	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$	12.5ns
Total		31.5ns

Note: This part does not have internal pull up resistors. In this application external pull ups should be added to the 16 ports.

MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −440μA	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	A_i, B_i			−0.36	mA
			$\overline{E}$			−0.72	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	A_i, B_i			20	μA
			$\overline{E}$			40	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V	A_i, B_i			0.1	mA
			$\overline{E}$			0.2	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			27	40	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

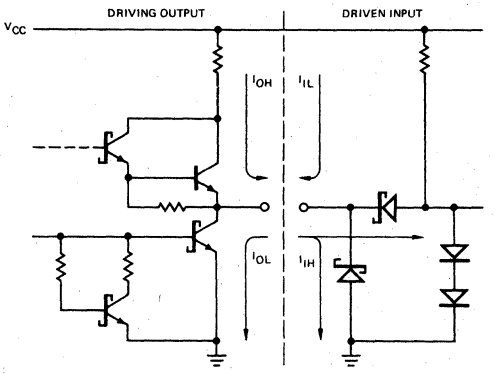
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A_i or B_i to $\overline{Equal}$	$C_L = 15pF$ $R_L = 2.0k\Omega$		9	15	ns
t_{PHL}				9	15	
t_{PLH}	$\overline{E}$ to $\overline{Equal}$			5	7	ns
t_{PHL}				6	8	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS2521 Min	COMMERCIAL Am25LS2521 Max	MILITARY Am25LS2521 Min	MILITARY Am25LS2521 Max	Units
t_{PLH}	A_i or B_i to	$C_L = 50pF$ $R_L = 2.0k\Omega$		20		22	ns
t_{PHL}	$\overline{Equal}$ Output			19		21	
t_{PLH}	$\overline{E}$ to $\overline{Equal}$ Output			10.5		12	ns
t_{PHL}				12.5		15	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2521
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000180

Note: Actual current flow direction shown.

Am25LS2535

Eight-Input Multiplexer with Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- Am25LS features improved noise margin, higher drive, and faster operation

GENERAL DESCRIPTION

The Am25LS2535 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

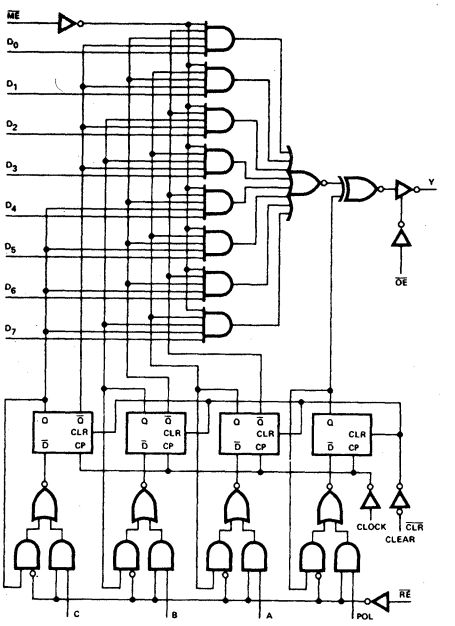
The Am25LS2535 contains an internal register which holds the A, B, and C multiplexer select lines as well as the POL (polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am25LS2535 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

BLOCK DIAGRAM

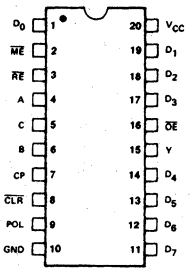


BD001620

03697B

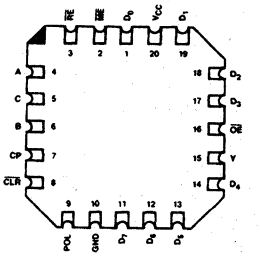
CONNECTION DIAGRAM
Top View

D-20-1



CD001860

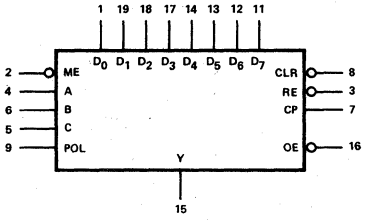
L-20-1



CD001920

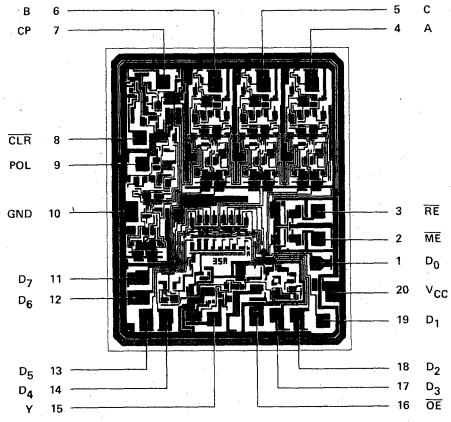
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000540

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080″ x 0.099″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2535 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 20-pin plastic DIP
  - X– Dice
- **Am25LS2535** — Device type
  - 8-Input Multiplexer

Valid Combinations	
Am25LS2535	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 6, 5	A, B, C	O	Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.
9	POL	O	Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.
2	$\overline{ME}$		Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.
3	$\overline{RE}$		Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.
8	$\overline{CLR}$		Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.
	D_1-D_8	I	Data Inputs to the 8-input multiplexer.
7	CP		Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.
16	$\overline{OE}$	O	Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high-impedance state.
15	Y	O	The chip output.

FUNCTION TABLE

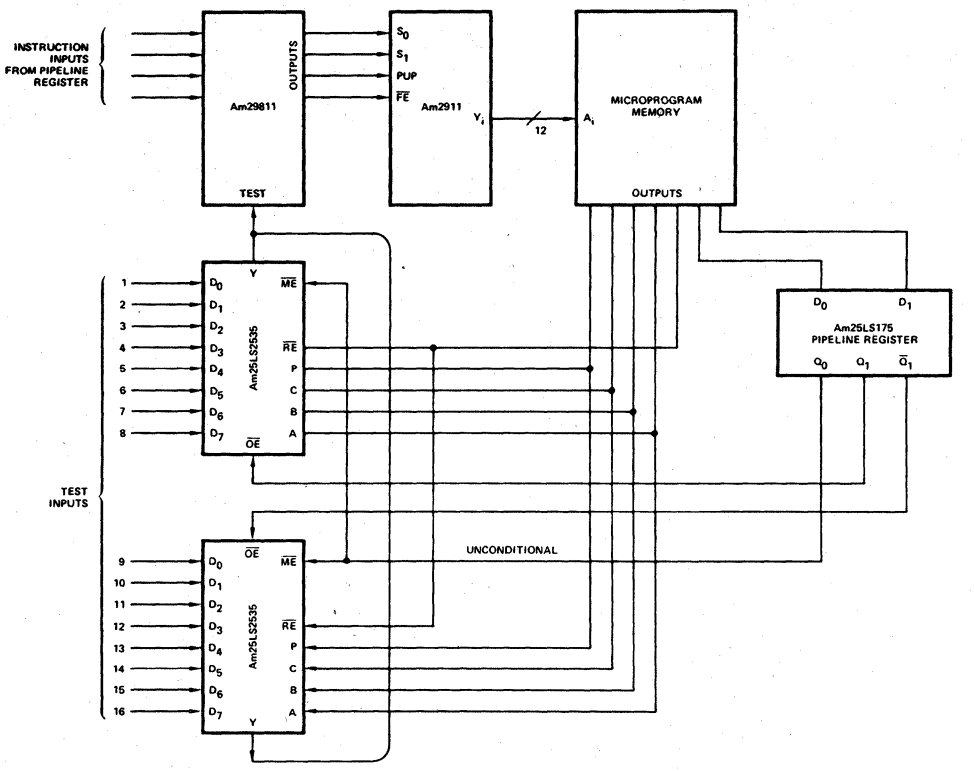
MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	D_i/D_i (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H					H	H	H				$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

9

APPLICATION



AF001980

A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA		2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA		2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 20mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−50	μA
			V_O = 2.4V				50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX				97	148	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_1–D_7, A, B, C, POL, $\overline{ME}$, CLR at GND. All other inputs and outputs open. Measured after a momentary ground then 4.5 V applied to clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

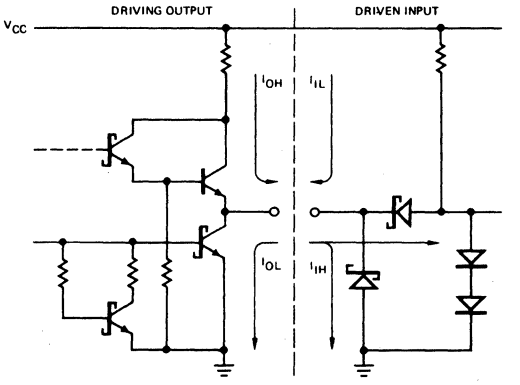
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Y POL – LOW	C_L = 15pF, R_L = 2.0kΩ		21	32	ns
t_{PHL}				19	29	
t_{PLH}	Clock to Y POL – HIGH			16	24	ns
t_{PHL}				19	29	
t_{PLH}	D_n to Y			10	16	ns
t_{PHL}				13	19	
t_{PLH}	$\overline{CLR}$ to Y			22	33	ns
t_{PHL}				22	33	
t_{PLH}	$\overline{ME}$ to Y			12	18	ns
t_{PHL}				12	18	
t_{ZL}	$\overline{OE}$ to Y			8	14	ns
t_{ZH}				8	14	
t_{LZ}		C_L = 5.0pF, R_L = 2.0kΩ		10	17	ns
t_{HZ}				10	17	
t_s	A, B, C, POL	C_L = 15pF, R_L = 2.0kΩ	10			ns
	$\overline{RE}$		15			
t_s	$\overline{CLR}$ Recovery		5			ns
t_{pw}	Clock		10			ns
	$\overline{Clear}$ (LOW)		10			
t_h	A, B, C, POL, $\overline{RE}$		0			ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

			COMMERCIAL		MILITARY		
			Am25LS2535		Am25LS2535		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	Clock to Y, POL-L	C_L = 50pF, R_L = 2.0kΩ		40		47	ns
t_{PHL}				34		38	
t_{PLH}	Clock to Y, POL-H			29		33	
t_{PHL}				35		41	
t_{PLH}	D_N to Y			19		21	ns
t_{PHL}				22		24	
t_{PLH}	$\overline{CLR}$ to Y			39		45	ns
t_{PHL}				39		45	
t_{PLH}	$\overline{ME}$ to Y			22		26	ns
t_{PHL}				19		20	
t_{ZL}	$\overline{OE}$ to Y			19		24	ns
t_{ZH}				22		29	
t_{LZ}	$\overline{OE}$ to Y	C_L = 5.0pF, R_L = 2.0kΩ		24		30	ns
t_{HZ}				24		30	
t_s	A, B, C POL	C_L = 50pF, R_L = 2.0kΩ	11		12		ns
	$\overline{RE}$		18		20		
t_s	$\overline{CLR}$ Recovery		6		7		ns
t_{pw}	Clock		11		12		ns
	$\overline{Clear}$ (LOW)		11		12		
t_h	A, B, C, POL, $\overline{RE}$		3		3		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2535
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

RELATED PRODUCTS

Part No.	Description
Am2922	8 Input Multiplexer
Am2923	8 Input Multiplexer

Am25LS2536

Eight-Bit Decoder with Control Storage

DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low-Power Schottky Process

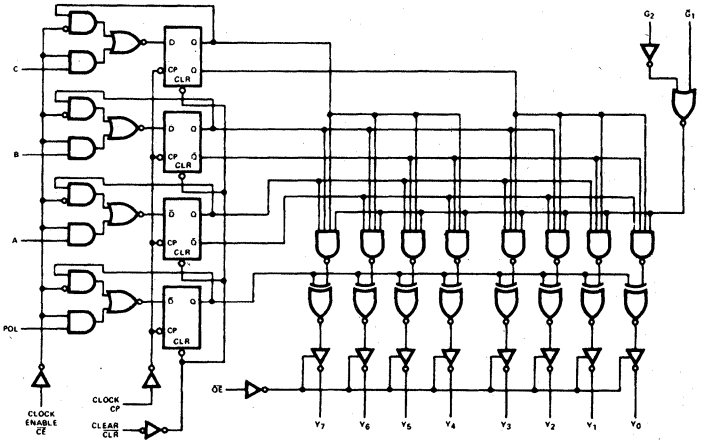
GENERAL DESCRIPTION

The Am25LS2536 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the exclusive "OR" gate allows for polarity control of the selected output. The 3-state outputs are enabled by a LOW on the ($\overline{OE}$) output enable.

The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have both Clear, Clock, and Clock Enable functions provided. The $\overline{G}_1$ and G_2 input provide either polarity for input control or data.

BLOCK DIAGRAM

8-Bit Decoder/Demultiplexer with Control Storage



BD001630

RELATED PRODUCTS

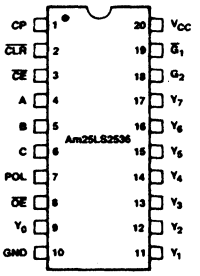
Part No.	Description
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

03666B

Refer to Page 13-1 for Essential Information on Military Devices

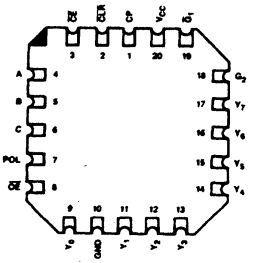
CONNECTION DIAGRAM
Top View

D-20-1



CD001930

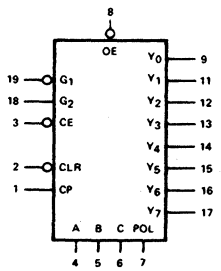
L-20-1



CD001940

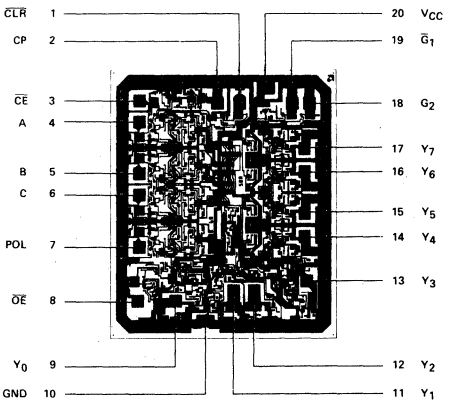
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000730

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.084" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2536 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2536** — Device type: 8-Bit Decoder

Valid Combinations	
Am25LS2536	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

Pin No.	Name	I/O	Description
2	$\overline{CLR}$	I	Clear. When the CLEAR input is LOW, the control register outputs (Q_A, Q_B, Q_C, Q_{POL}) are set LOW regardless of any other inputs.
1	CP	I	Clock. Enters data into the control register on the LOW-to-HIGH transition.
3	$\overline{CE}$	I	Clock Enable. Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the Q_i outputs do not change state, regardless of data or clock input transitions.
4, 5, 6	A, B, C	I	Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.
7	POL	I	Input to the control register bit used for determining the polarity of the selected output.
19	$\overline{G}_1$	I	Active LOW part of the expression $G = \overline{G}_1 \oplus G_2$ where G is either data input for the selected Y_n or is used as an input enable.
18	G_2	I	Active HIGH part of the expression $G = \overline{G}_1 G_2$.
	Y_n	O	The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.
8	$\overline{OE}$		Output Enable. When $\overline{OE}$ is HIGH the Y_n outputs are in the high impedance state; when $\overline{OE}$ is LOW the Y_n's are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the Y_n output buffers only and has no effect on the control register or any other logic.

FUNCTION TABLE

	Inputs									Internal Registers				Three-State Outputs							
Mode	C	B	A	POL	$\overline{CE}$	$\overline{CLR}$	G*	$\overline{OE}$	CP	Q_C	Q_B	Q_A	Q_{POL}	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
Clear	X	X	X	X	X	L	L	L	X	L	L	L	L	H	H	H	H	H	H	H	H
	X	X	X	X	X	L	H	L	X	L	L	L	L	L	H	H	H	H	H	H	H
Hold	X	X	X	X	H	H	NC	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
Select	L	L	L	H	L	H	H	L	↑	L	L	L	H	H	L	L	L	L	L	L	L
	L	L	H	H	L	H	H	L	↑	L	L	H	H	L	H	L	L	L	L	L	L
	L	H	L	H	L	H	H	L	↑	L	H	L	H	L	L	H	L	L	L	L	L
	L	H	H	H	L	H	H	L	↑	L	H	H	H	L	L	L	H	L	L	L	L
	H	L	L	H	L	H	H	L	↑	H	L	L	H	L	L	L	L	H	L	L	L
	H	L	H	H	L	H	H	L	↑	H	L	H	H	L	L	L	L	L	H	L	L
	H	H	L	H	L	H	H	L	↑	H	H	L	H	L	L	L	L	L	L	H	L
	H	H	H	H	L	H	H	L	↑	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	L	H	H	L	↑	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	L	↑	L	L	H	L	H	L	H	H	H	H	H	H
	L	H	L	L	L	H	H	L	↑	L	H	L	L	H	H	L	H	H	H	H	H
	L	H	H	L	L	H	H	L	↑	L	H	H	L	H	H	H	L	H	H	H	H
	H	L	L	L	L	H	H	L	↑	H	L	L	L	H	H	H	H	L	H	H	H
	H	L	H	L	L	H	H	L	↑	H	L	H	L	H	H	H	H	H	L	H	H
	H	H	L	L	L	H	H	L	↑	H	H	L	L	H	H	H	H	H	H	L	H
	H	H	H	L	L	H	H	L	↑	H	H	H	L	H	H	H	H	H	H	H	L
	X	X	X	H	L	H	L	L	↑	X	X	X	H	L	L	L	L	L	L	L	L
	X	X	X	L	L	H	L	L	↑	X	X	X	L	H	H	H	H	H	H	H	H
Output Disable	X	X	X	X	X	X	X	H	X	NC	NC	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z

NC = No Change X = Don't Care Z = High-Impedance ↑ = Low-to-High Transition

*

$\overline{G}_1$	G_2	G
L	L	L
L	H	H
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature
Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2.6mA, COM'L	2.4	3.2		Volts
			I_{OH} = −1.0mA, MIL	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA, COM'L		0.4	0.5	Volts
			I_{OL} = 12mA, MIL		0.35	0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			37	56	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions A = B = C = $\overline{G}_1$ = $\overline{OE}$ = $\overline{CE}$ = GND; CLK = $\overline{CLR}$ = POL = G_2 = 4.5V.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\overline{G}_1$ to Y_0 – Y_7	C_L = 45pF R_L = 667Ω		17	25	ns
t_{PLH}				23	34	
t_{PLH}	G_2 to Y_0 – Y_7			20	30	ns
t_{PHL}				26	39	
t_{PLH}	CP to Y_0 – Y_7			24	36	ns
t_{PHL}				30	45	
t_{PLH}	$\overline{CLR}$ to Y_0 – Y_7			24	36	ns
t_{PHL}				31	46	
t_s	Clock Enable to CP		25			ns
t_h			0			
t_s	A, B, C, POL to CP		15			ns
t_h			0			
t_{HZ}	$\overline{OE}$ to Y_0 – Y_7	C_L = 5pF R_L = 667Ω		9	14	ns
t_{LZ}				11	17	
t_{ZH}	$\overline{OE}$ to Y_0 – Y_7	C_L = 45pF R_L = 667Ω		15	22	ns
t_{ZL}				16	24	
t_s	Set-up Time, Clear Recovery to CP		20			ns
t_{pw}	Pulse Width — Clock		15			ns
	Pulse Width — Clear		15			

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS2536 Min	COMMERCIAL Am25LS2536 Max	MILITARY Am25LS2536 Min	MILITARY Am25LS2536 Max	Units
t_{PLH}	$\overline{G}_1$ to Y_0 – Y_7	C_L = 45pF R_L = 667Ω		29		31	ns
t_{PHL}				39		42	
t_{PLH}	G_2 to Y_0 – Y_7			34		37	ns
t_{PHL}				44		48	
t_{PLH}	CP to Y_0 – Y_7			40		42	ns
t_{PHL}					51		55
t_{PLH}	$\overline{CLR}$ to Y_0 – Y_7				47		54
t_{PHL}				58		66	ns
t_s	Clock Enable to CP		27		30		ns
t_h			0		0		
t_s	A, B, C, POL to CP		17		20		ns
t_h			0		0		
t_{HZ}	$\overline{OE}$ to Y_0 – Y_7	C_L = 5.0pF R_L = 667Ω		17		18	ns
t_{LZ}				27		34	
t_{ZH}	$\overline{OE}$ to Y_0 – Y_7	C_L = 5.0pF R_L = 667Ω		25		27	ns
t_{ZL}				28		30	
t_s	Set-up Time, Clear Recovery to CP		23		25		ns
t_{pw}	Pulse Width — Clock		17		20		ns
	Pulse Width — Clear		15		15		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2537

One-of-Ten Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Separate output polarity control
- Inverting and non-inverting enable inputs
- Does not respond to codes above nine
- A.C. parameters specified over operating temperature and power supply ranges

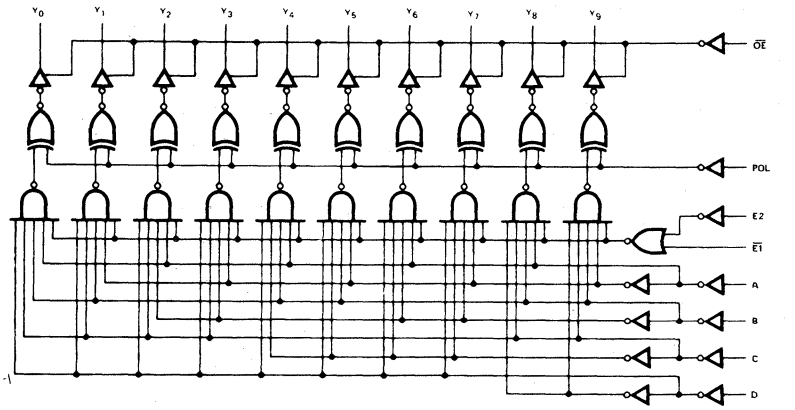
GENERAL DESCRIPTION

The Am25LS2537 is a demultiplexer/one-of-ten decoder that accepts four active high BCD inputs and selects one-of-ten mutually exclusive outputs. The device features three-state outputs as well as a buffered common polarity control such that the outputs are mutually exclusive active-low or mutually exclusive active-high. The logic design of the Am25LS2537 ensures that all outputs are unselected when the binary codes greater than nine are applied to the inputs. The inputs A, B, C, and D of the Am25LS2537 correspond to the respective binary weight of 1, 2, 4, and 8.

The output enable ($\overline{OE}$) input controls the three-state outputs. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the outputs are enabled. The polarity (POL) input is used to drive the Y outputs to either the active-HIGH state or the active-LOW state. When the POL input is LOW, the outputs are active-HIGH. When the POL input is HIGH, the Y outputs are active-LOW. The device features one active-HIGH and one active-LOW enable input which can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

The Am25LS2537 is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device also features Am25LS family faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

BLOCK DIAGRAM



BD001330

RELATED PRODUCTS

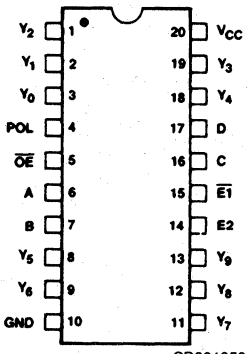
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2538	1-of-8 Decoder
Am25LS2539	Dual 1-of-4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1-of-8 Decoder
Am2924	3-to-8 Line Decoder/Demultiplexer

03665B

Refer to Page 13-1 for Essential Information on Military Devices

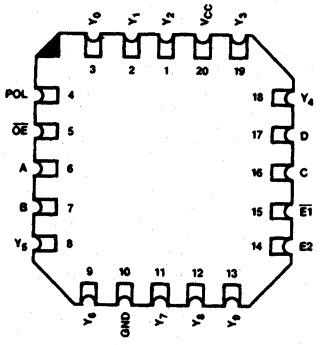
CONNECTION DIAGRAM
Top View

D-20-1



CD001950

L-20-1



CD001960

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2537 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - F– 20-pin flatpak
  - L– 20-pin leadless chip carrier
  - P– 20-pin plastic DIP
  - X– Dice
- **Am25LS2537** — Device type 1-of-10 Decoder

Valid Combinations	
Am25LS2537	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
6, 7, 16, 17	A, B, C, D	I	To select inputs to the decoder.
15	$\overline{E1}$	I	The active-LOW enable input. A HIGH on the $\overline{E1}$ input inhibits the decoder function regardless of any other inputs.
14	E2	I	The active-HIGH enable input. A LOW on the E2 input forces all the decoder functions to the inactive state regardless of any other inputs.
4	POL	I	The polarity control for the output function. When the polarity control is HIGH, the outputs are active-LOW. When the POL input is LOW, the outputs are active-HIGH.
5	$\overline{OE}$	O	Output Enable. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the output to the high-impedance (off) state.
	Y_i	O	Decoder outputs. The ten outputs of the decoder.

FUNCTION TABLE

FUNCTION	INPUTS								OUTPUTS									
	$\overline{OE}$	$\overline{E1}$	E2	POL	D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9
3-State	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	X	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
	L	X	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	X	L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	L	L	L	L	H	L	L	L
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	L	L	H	L	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L
Active-LOW Output	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
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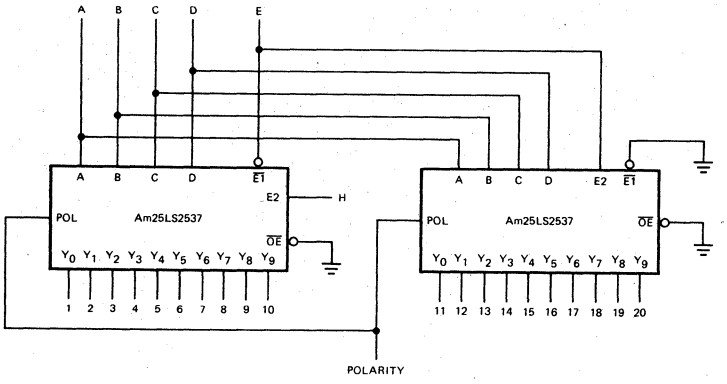
	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

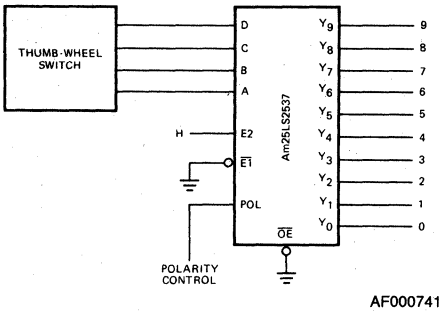
H = HIGH
L = LOW
X = Don't Care
Z = High-Impedance

9

APPLICATIONS



One-of-Twenty Decoder with Active-High or Active-Low Output Polarity.
Could be used for I/O Decoding in an Am9080A system.



BCD to Decimal (One-of-Ten) Decoder.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			25	40	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = D = $\overline{E1}$ = GND; E2 = POL = $\overline{OE}$ = 4.5V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max).

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, C, D to Y_i	C_L = 15pF, R_L = 2.0kΩ		22	33	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{E1}$ to Y_i			19	28	ns
t_{PHL}				21	31	
t_{PLH}	E2 to Y_i			21	31	ns
t_{PHL}				23	34	
t_{PLH}	POL to Y_i			18	27	ns
t_{PHL}				21	31	
t_{ZH}	$\overline{OE}$ Control to Y_i			22	33	ns
t_{ZL}				14	21	
t_{HZ}	$\overline{OE}$ Control to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		19	28	ns
t_{LZ}				23	34	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

			COMMERCIAL		MILITARY		
			Am25LS2537		Am25LS2537		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	A, B, C, D to Y_i	C_L = 50pF, R_L = 2.0kΩ		41		48	ns
t_{PHL}				32		39	
t_{PLH}	$\overline{E1}$ to Y_i			34		40	ns
t_{PHL}				38		45	
t_{PLH}	E2 to Y_i			38		45	ns
t_{PHL}				42		49	
t_{PLH}	POL to Y_i			32		37	ns
t_{PHL}				42		52	
t_{ZH}	$\overline{OE}$ Control to Y_i			44		55	ns
t_{ZL}				23		25	
t_{HZ}	$\overline{OE}$ Control to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		33		37	ns
t_{LZ}				38		42	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2538

One-of-Eight Decoder
with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- A. C. parameters specified over operating temperature and power supply ranges

GENERAL DESCRIPTION

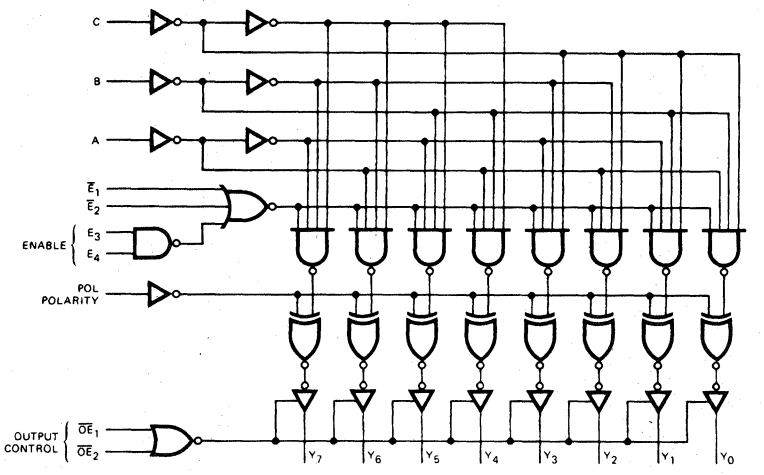
The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs–A, B, and C–that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high-impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

BLOCK DIAGRAM

One-of-Eight Decoder



BD002350

03664B

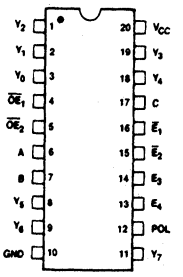
Refer to Page 13-1 for Essential Information on Military Devices

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1-of-10 Decoder
Am25LS2539	Dual 1-of-4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1-of-8 Decoder
Am2924	3-to-8 Line Decoder/Demultiplexer

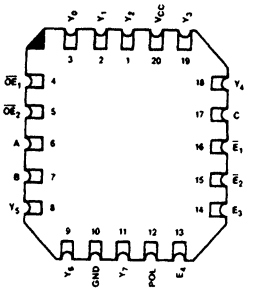
CONNECTION DIAGRAM
Top View

D-20-1



CD001970

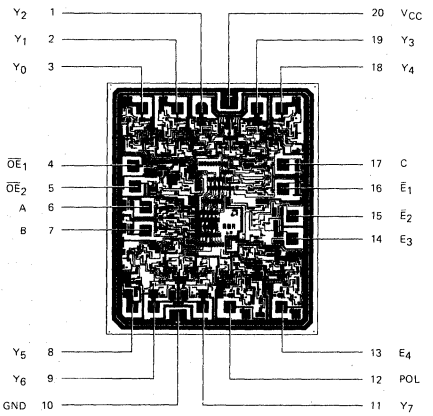
L-20-1



CD001980

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.081" x 0.096"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2538 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2538** — Device type
  - 1-of-8 Decoder

Valid Combinations	
Am25LS2538	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

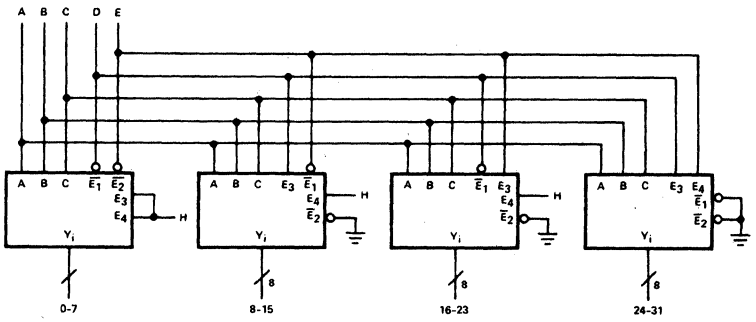
Pin No.	Name	I/O	Description
6, 7, 17	A, B, C	I	The three select inputs to the decoder/demultiplexer.
16, 15	$\overline{E}_1$, $\overline{E}_2$	I	The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.
14, 13	E_3, E_4	I	The active HIGH enable inputs. A LOW on either the E_3 or E_4 input forces all the decoded functions to be inhibited.
12	POL	I	Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.
4, 5	$\overline{OE}_1$, $\overline{OE}_2$	I	Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high-impedance state.
	Y_i	O	The eight outputs for the decoder/demultiplexer.

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High-Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

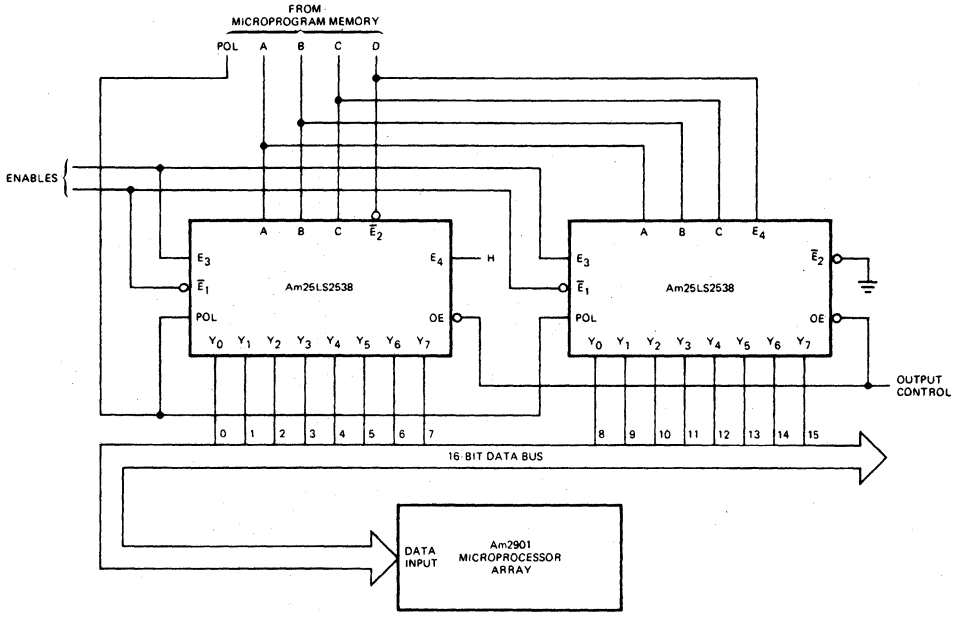
H = HIGH
L = LOW
X = Don't Care
Z = High-Impedance

APPLICATIONS



AF001091

One-of-thirty-two decoder without additional decoding devices.
Can be used for I/O decoding in an Am9080A system.



AF001081

Two Am25LS2538s can be used to perform a one-of-sixteen-bit mask function or a one-of-sixteen-bit select function to perform bit manipulation in a microprocessor system.

Examples:

D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Function
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Bit Select
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Bit Select
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	Bit Mask
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	Bit Mask

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA (MIL)	2.4	3.4		Volts
			I_{OH} = −2.6mA (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			21	34	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = D = $\overline{E}_1$ = $\overline{E}_2$ = GND: E3 = E_4 = POL = $\overline{OE}_1$ = $\overline{OE}_2$ = 4.5V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max).

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

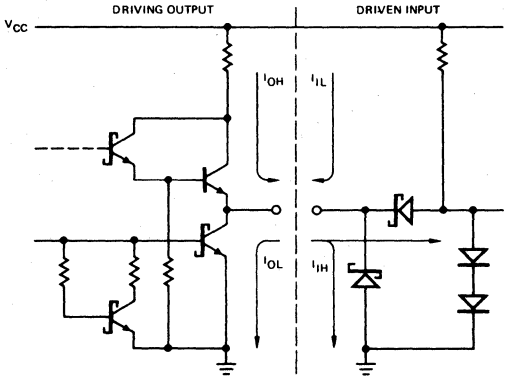
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, C to Y_i	C_L = 15pF, R_L = 2.0kΩ		20	30	ns
t_{PHL}				15	22	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to Y_i			19	28	ns
t_{PHL}				20	30	
t_{PLH}	E_3, E_4 to Y_i			21	31	ns
t_{PHL}				23	34	
t_{PLH}	POL to Y_i			16	24	ns
t_{PHL}				20	30	
t_{ZH}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i			17	25	ns
t_{ZL}				14	21	
t_{HZ}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		17	25	ns
t_{LZ}				20	30	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS2538 Min	COMMERCIAL Am25LS2538 Max	MILITARY Am25LS2538 Min	MILITARY Am25LS2538 Max	Units
t_{PLH}	A, B, C to Y_i	C_L = 50pF, R_L = 2.0kΩ		36		42	ns
t_{PHL}				29		37	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to Y_i			34		39	ns
t_{PHL}				38		45	
t_{PLH}	E_3, E_4 to Y_i			38		45	ns
t_{PHL}				43		52	
t_{PLH}	POL to Y_i			29		34	ns
t_{PHL}				39		49	
t_{ZH}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i			38		45	ns
t_{ZL}				23		25	
t_{HZ}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		29		33	ns
t_{LZ}				33		36	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2538
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am25LS2539

Dual One-of-Four Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

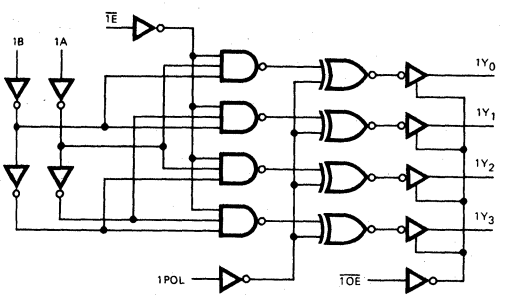
- Two independent decoders/demultiplexers
- Three-state outputs
- Buffered common polarity control
- A. C. parameters specified over operating temperature and power supply ranges

GENERAL DESCRIPTION

The Am25LS2539 is a dual two-line to four-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs – A and B which are decoded to one-of-four Y outputs. An enable input ($\overline{E}$) is used for gating or can be used as a data input for demultiplexing applications. When the enable input goes HIGH, all four decoder functions are inhibited.

An output enable ($\overline{OE}$) input is used to control the three-state outputs of the device. When the $\overline{OE}$ input is LOW, the outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance (off) state. The device also has separate buffered polarity (POL) inputs to force the outputs to either an active-HIGH state or an active-LOW state. When the POL input is LOW, the outputs are active-HIGH and when the POL input is HIGH, the outputs are active-LOW. The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device features Am25LS family improved switching specification, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

BLOCK DIAGRAM



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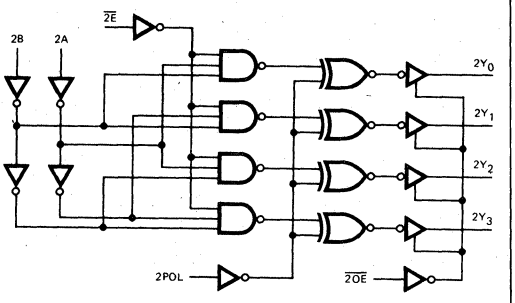


BD001410

RELATED PRODUCTS

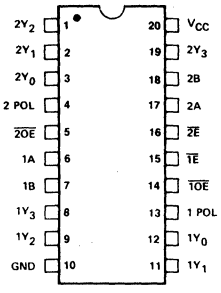
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1-of-10 Decoder
Am25LS2538	1-of-8 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1-of-8 Decoder
Am2924	3-to-8 Line Decoder/Demultiplexer

03620B

Refer to Page 13-1 for Essential Information on Military Devices

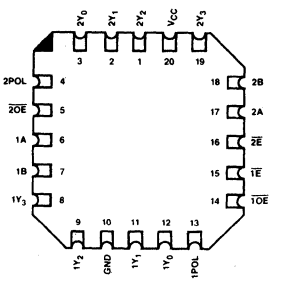
CONNECTION DIAGRAM
Top View

D-20-1



CD001630

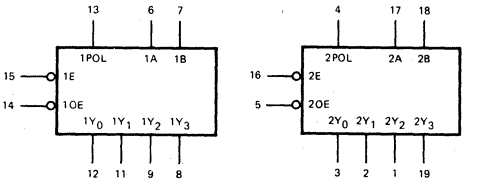
L-20-1



CD001620

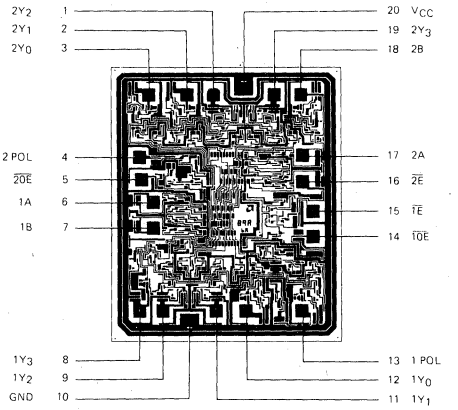
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000560 LS000550

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.081" x 0.096"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2539 **D** **C** **B**

- Screening Option
  - Blank – Standard processing
  - B – Burn-in
- Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- Device type
  - Dual 1-of-4 Decoder

Valid Combinations	
Am25LS2539	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A, B	I	Select the two select inputs to the decoder/demultiplexer.
15, 16	$\overline{E}$ Enable	I	The enable input to the decoder. A HIGH input forces the decoding functions to be inhibited regardless of the A and B inputs.
13, 4	POL	I	Polarity Input. The polarity input forces the outputs to either an active-HIGH state or an active-LOW state. A LOW on the polarity input forces the output active-HIGH. A HIGH on the polarity input forces the outputs active-LOW.
14, 5	$\overline{OE}$	I	Output Enable. A LOW on the $\overline{OE}$ input enables the outputs. A HIGH on the $\overline{OE}$ inputs forces the outputs to the high high-impedance (off) state.
	Y_0, Y_1, Y_2, Y_3	O	The four decoder/demultiplexer outputs.

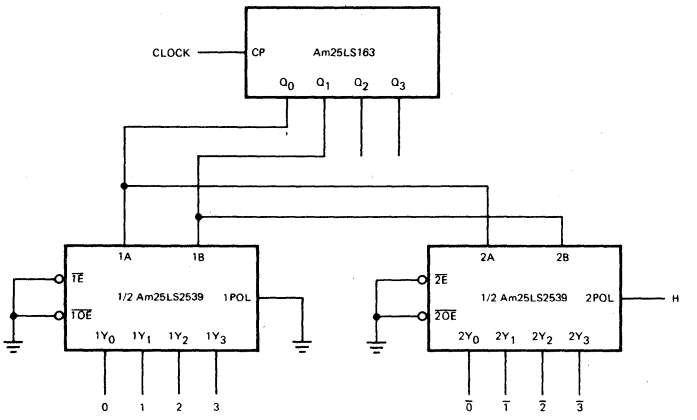
FUNCTION TABLE

Function	Inputs					Outputs			
	$\overline{OE}$	$\overline{E}$	POL	B	A	Y_0	Y_1	Y_2	Y_3
High-Impedance	H	X	X	X	X	Z	Z	Z	Z
Disable	L	H	L	X	X	L	L	L	L
	L	H	H	X	X	H	H	H	H
Active-High Output	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	L	H	L	L
	L	L	L	H	L	L	L	H	L
	L	L	L	H	H	L	L	L	H
Active-Low Output	L	L	H	L	L	L	H	H	H
	L	L	H	L	H	H	L	H	H
	L	L	H	H	L	H	H	L	H
	L	L	H	H	H	H	H	H	L

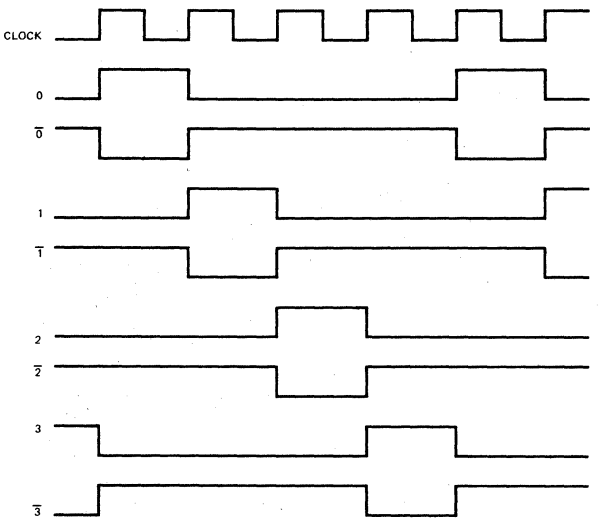
H = HIGH
L = LOW

X = Don't Care
Z = High-Impedance

APPLICATIONS



AF000831



AF000840

FOUR PHASE CLOCK GENERATOR

9

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			22	37	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = $\overline{E}$ = GND: POL = $\overline{OE}$ = 4.5V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max).

03620B

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

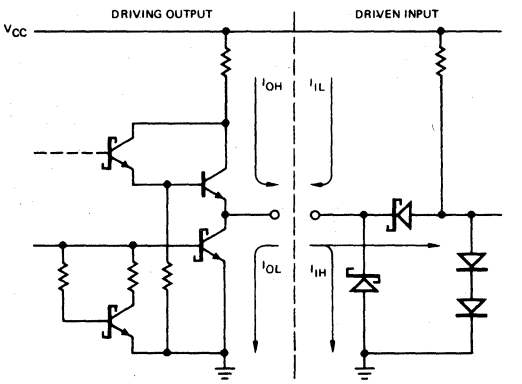
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B to Y_i	C_L = 15pF, R_L = 2.0 kΩ		22	33	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{E}$ to Y_i			19	28	ns
t_{PHL}				21	31	
t_{PLH}	POL to Y_i			16	24	ns
t_{PHL}				19	28	
t_{ZH}	$\overline{OE}$ to Y_i			15	23	ns
t_{ZL}				15	22	
t_{HZ}	$\overline{OE}$ to Y_i	C_L = 5.0 pF, R_L = 2.0kΩ		19	28	ns
t_{LZ}				23	34	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS2539 Min	COMMERCIAL Am25LS2539 Max	MILITARY Am25LS2539 Min	MILITARY Am25LS2539 Max	Units
t_{PLH}	A, B, to Y_i	C_L = 50pF, R_L = 2.0kΩ		41		48	ns
t_{PHL}				34		42	
t_{PLH}	$\overline{E}$ to Y_i			34		40	ns
t_{PHL}				38		45	
t_{PLH}	POL to Y_i			29		34	ns
t_{PHL}				39		49	
t_{ZH}	$\overline{OE}$ to Y_i			38		45	ns
t_{ZL}				24		25	
t_{HZ}	$\overline{OE}$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		33		37	ns
t_{LZ}				36		37	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2539 • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am25LS2548

Chip Select Address Decoder with Acknowledge

DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and read or write command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding

GENERAL DESCRIPTION

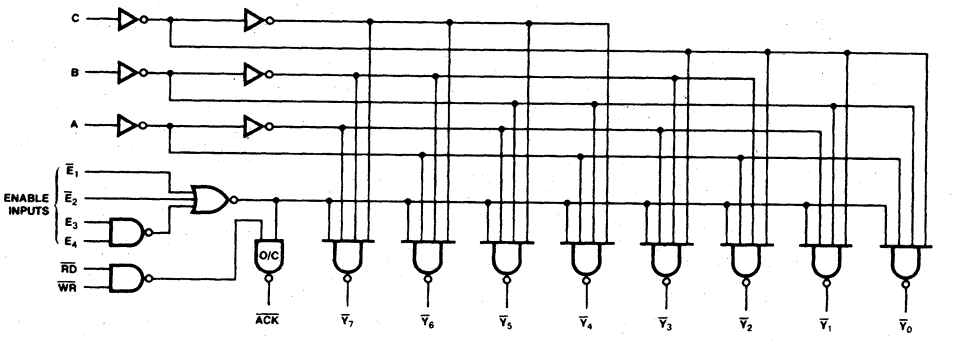
The Am25LS2548 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, $\overline{ACK}$, is active LOW and responds to the combination of all enables active and a read ($\overline{RD}$) or write ($\overline{WR}$) input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at inputs A, B, and C.

The Am25LS2548 is intended for chip select decoding in small, medium or large systems where multiple chip selects must be generated and address space must be allocated conservatively.

BLOCK DIAGRAM



BD001610

RELATED PRODUCTS

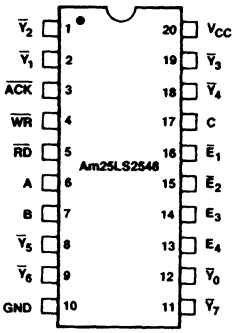
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1-of-10 Decoder
Am25LS2538	1-of-8 Decoder
Am25LS2539	Dual 1-of-4 Decoder
Am2921	1-of-8 Decoder
Am2924	3-to-8 Line Decoder/Demultiplexer

03621B

Refer to Page 13-1 for Essential Information on Military Devices

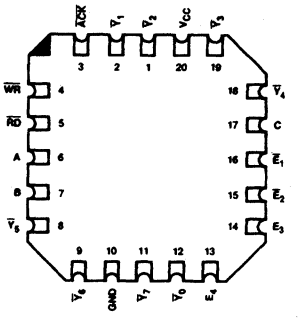
CONNECTION DIAGRAM
Top View

D-20-1



CD001990

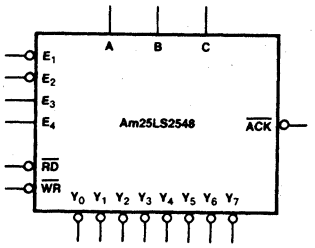
L-20-1



CD002000

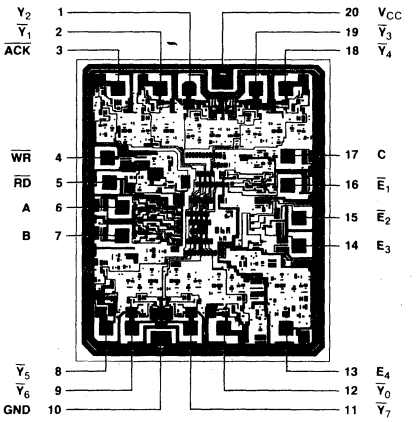
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000741

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.081" x 0.096"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2548 **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 20-pin CERDIP; F – 20-pin flatpak; L – 20-pin leadless chip carrier; P – 20-pin plastic DIP; X – Dice
- Am25LS2548 — Device type: Address Decoder

Valid Combinations	
Am25LS2548	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
6, 7, 17	A, B, C	I	Three-line to eight-line chip select decoder inputs.
16, 15	$\overline{E}_1$, $\overline{E}_2$	I	The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.
14, 13	E_3, E_4	I	The active HIGH enable inputs. A LOW on either the E_3 or E_4 input forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.
4, 5	$\overline{WR}$, $\overline{RD}$	I	The write input, $\overline{WR}$, and read input, $\overline{RD}$, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.
3	$\overline{ACK}$	O	The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, E_3 and E_4 are HIGH and $\overline{WR}$ or $\overline{RD}$ is LOW.
	$\overline{Y}_i$	O	The eight active LOW chip select outputs.

FUNCTION TABLES

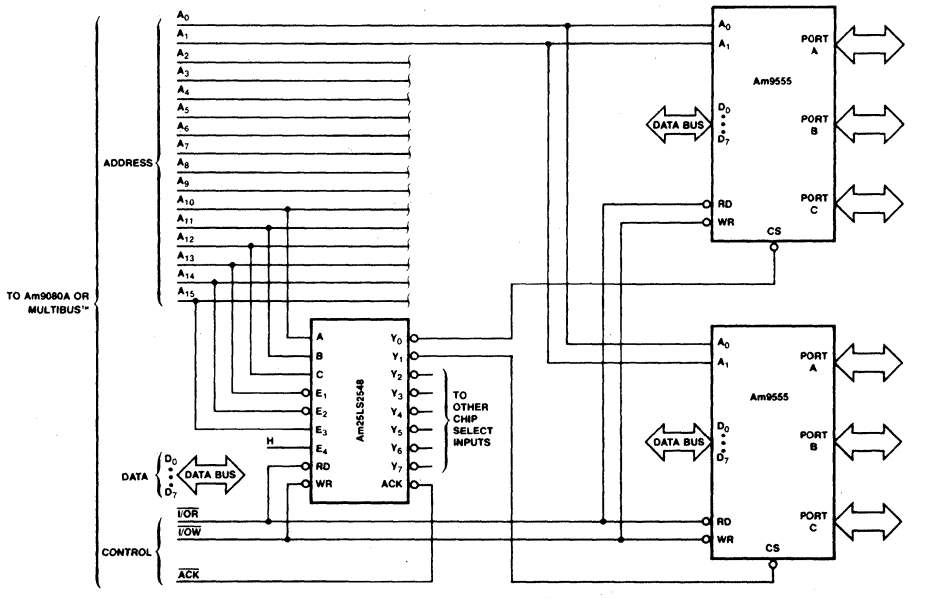
CHIP SELECT OUTPUTS Y_I

C	B	A	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H

ACKNOWLEDGE OUTPUT $\overline{ACK}$

$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

APPLICATIONS



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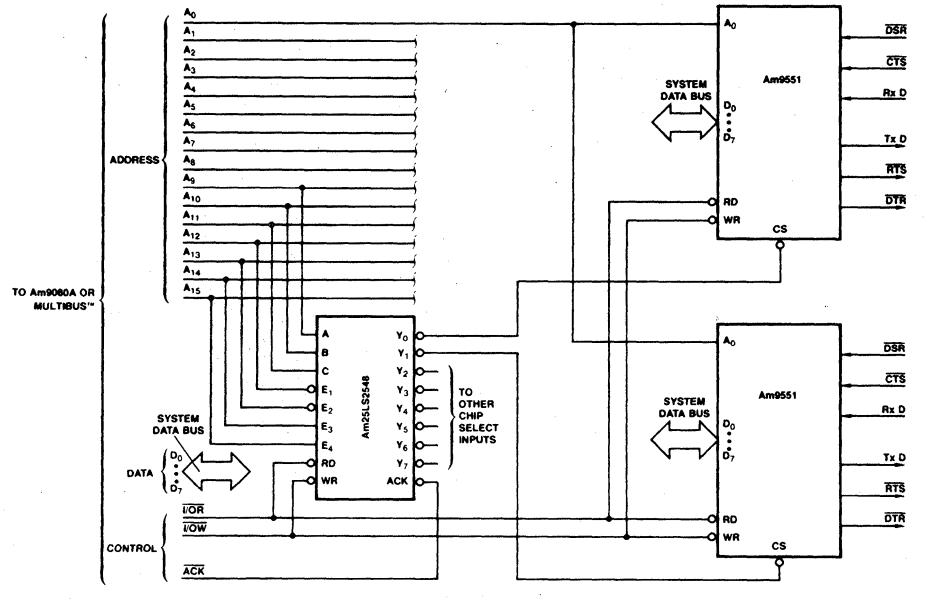


AF001060

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			15	20	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1$ = $\overline{E}_2$ = GND: RD = WR = E_3 = E_4 = 4.5V.

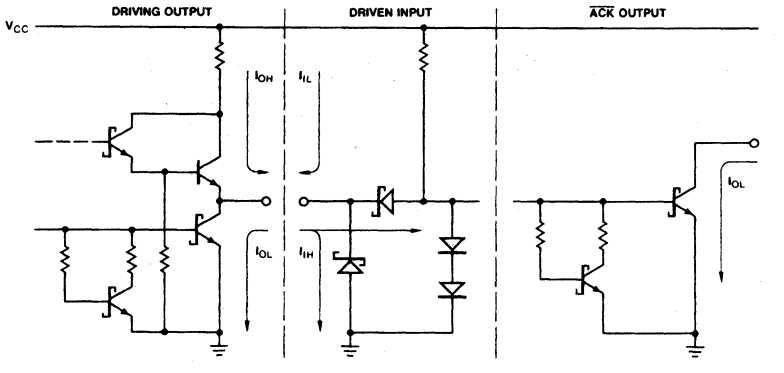
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C to $\overline{Y}_i$ (Three Level Delay)	C_L = 15pF, R_L = 2.0kΩ		14	20	ns
t_{PHL}				19	27	ns
t_{PLH}	A, B, or C to $\overline{Y}_i$ (Two Level Delay)			13	18	ns
t_{PHL}				15	21	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$			13	18	ns
t_{PHL}				16	23	ns
t_{PLH}	E_3, E_4 to $\overline{Y}_i$			15	21	ns
t_{PHL}				19	27	ns
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$			25	35	ns
t_{PHL}				16	22	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$			29	40	ns
t_{PHL}				25	35	ns
t_{PLH}	E_3, E_4 to $\overline{ACK}$			29	40	ns
t_{PHL}				25	35	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

			COMMERCIAL		MILITARY		
			Am25LS2548		Am25LS2548		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	A, B or C to Y_i (Three Level Delay)	C_L = 50pF, R_L = 2.0kΩ		27		30	ns
t_{PHL}				34		36	ns
t_{PLH}	A, B or C to Y_i (Two Level Delay)			23		25	ns
t_{PHL}				28		31	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$			23		25	ns
t_{PHL}				29		31	ns
t_{PLH}	E_3, E_4 to $\overline{Y}_i$			27		28	ns
t_{PHL}				34		36	ns
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$			45		45	ns
t_{PHL}				31		35	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$			45		45	ns
t_{PHL}				39		40	ns
t_{PLH}	E_3, E_4 to $\overline{ACK}$			45		45	ns
t_{PHL}				39		40	ns

Am25LS2548
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am25S557/Am25S558

Eight-Bit by Eight-Bit Combinatorial Multiplier

DISTINCTIVE CHARACTERISTICS

- Multiplies two 8-bit numbers – 16-bit output
- Combinatorial – no clocks required
- Full 8 x 8 multiply in 45ns typ.
- Cascades to 16 x 16 in 110ns typ.
- Expandable to multiples of 8 bits
- MSB and $\overline{MSB}$ outputs for easy expansion
- Unsigned, two's complement or mixed operands
- Implements common rounding algorithms with additional logic
- Three-state outputs
- Transparent 16-bit latch in Am25S557
- Industry standard pin-outs

GENERAL DESCRIPTION

The Am25S557 and Am25S558 are high-speed, combinatorial, 8 x 8-bit multipliers. Both use an array of full adders to form and add partial products in a single unclocked operation, resulting in a 16-bit parallel output product.

Mode control inputs X_M and Y_M allow the multiplier to accept either unsigned or two's complement numbers from either respective input to provide an unsigned or signed output. The mode control lines are held LOW for unsigned input words and HIGH for two's complement.

The Am25S557 and Am25S558 are easily expandable to longer work lengths. Both S_{15} and $\overline{S}_{15}$ are available to allow expansion in either signed or unsigned modes without external inverters. In the 16-bit by 16-bit configuration (32-bit output) the typical multiply time is 110ns.

Both configurations offer three-state output flexibility and the Am25S557 adds a 16-bit transparent latch between the multiplier array and the three-state output buffers (including $\overline{S}_{15}$).

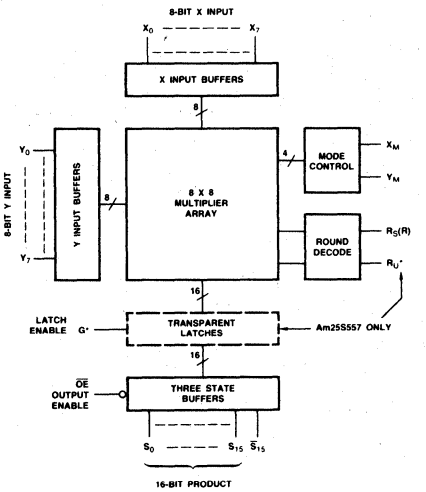
Rounding provisions for 8-bit truncated output configurations are particularly optimized for maximum flexibility. The Am25S557 internally develops proper rounding for either signed or unsigned numbers by combining rounding input R with X_M, Y_M, $\overline{X}_M$ and $\overline{Y}_M$ as follows:

$R_U = \overline{X}_M \bullet \overline{Y}_M \bullet R$ = Unsigned Rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\ R$ = Signed Rounding input to 2^6 adder.

Since the Am25S558 does not require the use of pin 9 for the latch enable input, (G), R_S and R_U are brought out separately.

BLOCK DIAGRAM



BD001780

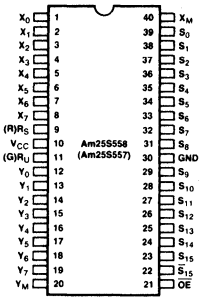
*Pin 11 is G for Am25S557 and R_U for Am25S558.

03614B

Refer to Page 13-1 for Essential Information on Military Devices

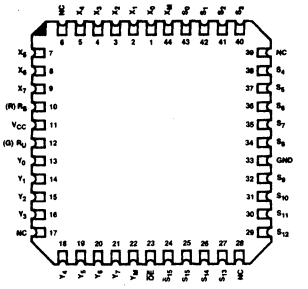
CONNECTION DIAGRAM
Top View

D-40-1



CD003030

L-44-1

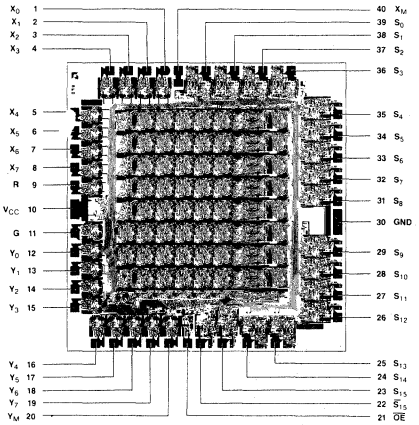


CD003040

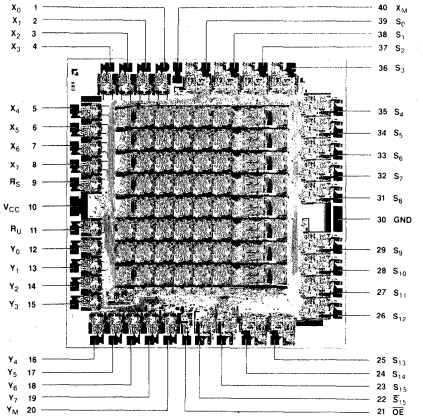
Pin assignments shown are for Am25S558. G and R shown in parentheses are pin assignments for Am25S557.

METALLIZATION AND PAD LAYOUT

Am25S557



Am25S558



DIE SIZE 0.171″ x 0.165″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S557
Am25S558 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 40-pin CERDIP
  - L – 44-pin leadless chip carrier
  - X – Dice
- **Am25S557 / Am25S558** — Device type
  - 8-Bit by 8-Bit Multiplier

Valid Combinations	
Am25S557	DC, DM LC, LM
Am25S558	DC, DM LC, LM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$X_0 - X_7$	I	Multiplicand 8-bit data inputs.
	$Y_0 - Y_7$	I	Multiplier 8-bit data inputs.
	X_M, Y_M	I	Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data.
	$S_0 - S_{15}$	O	Product 16-bit output.
23	$\overline{S}_{15}$		Inverted MSB for expansion.
9, 11	R_S, R_U	I	Rounding inputs for signed and unsigned data, respectively (Am25S558 only).
11	G		Transparent Latch Enable (Am25S557 only).
21	$\overline{OE}$	O	Three-state enable for S_0–S_{15} outputs.
9	R	I	Rounding input for signed or unsigned data (combined internally with X_M, Y_M in Am25S557 only).

MODE CONTROL INPUTS

Operating Mode	Input Data		Mode Control Inputs	
	$X_0 - X_7$	$Y_0 - Y_7$	X_M	Y_M
UNSIGNED	UNSIGNED	UNSIGNED	L	L
MIXED	UNSIGNED	2's COMP	L	H
	2's COMP	UNSIGNED	H	L
SIGNED	2's COMP	2's COMP	H	H

ROUNDING INPUTS
Am25S557

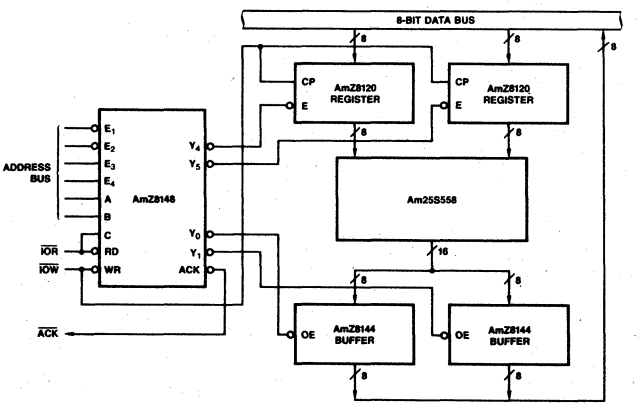
Inputs			Adds	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

Am25S558

Inputs		Adds		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	$X_M + Y_M = H$	
H	L	YES	NO	L	L
H	H	YES	YES	*	*

* Most rounding applications require a HIGH level for R_U or R_S, but not both.

I/O MAPPED INTERFACE WITH MOS MICROPROCESSOR



AF001270

APPLICATION

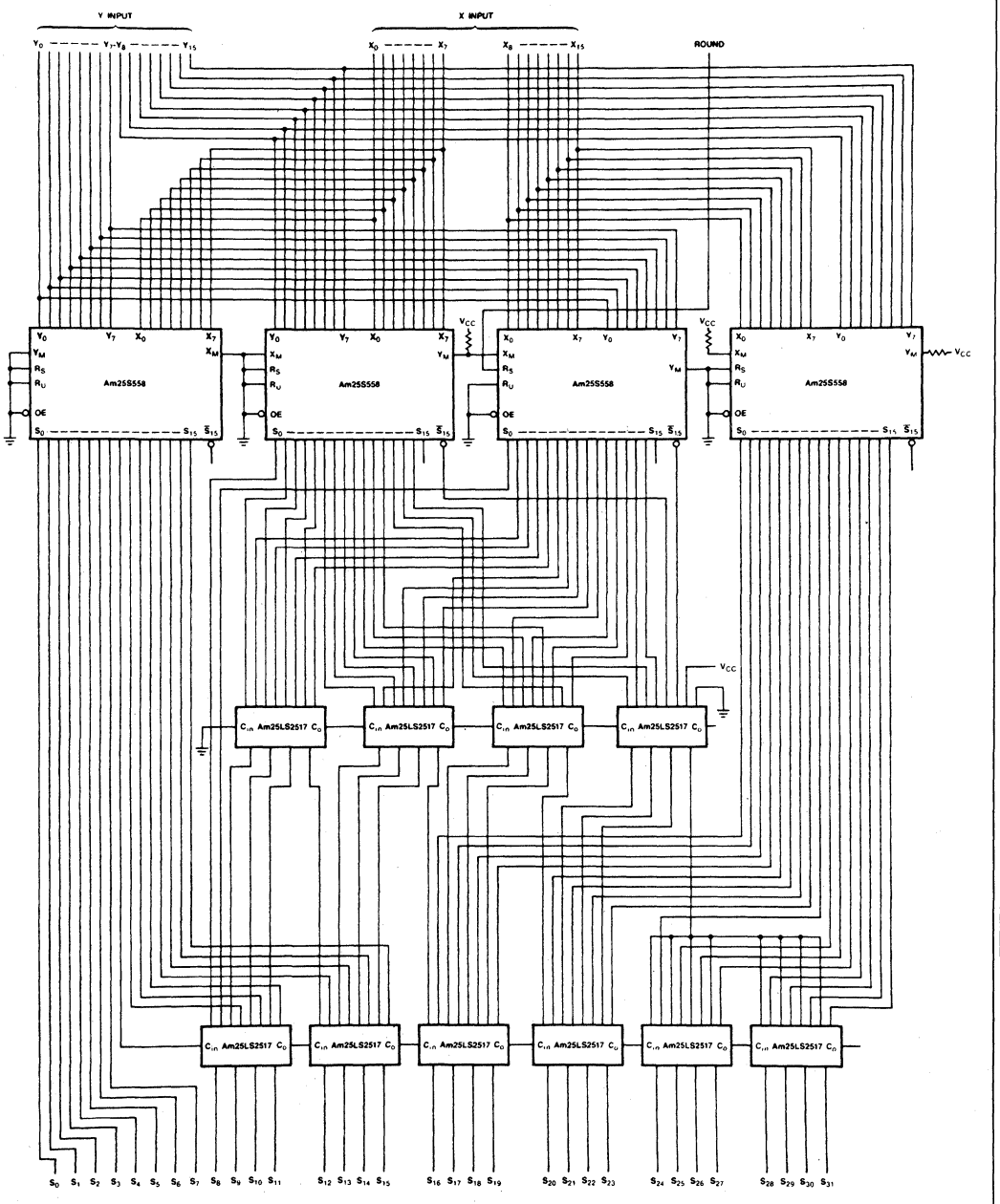


Figure 1. High-Speed 16 x 16 2's Complement Multiplication.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

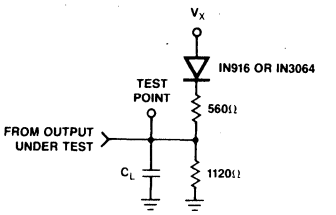
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OH} = −2.0mA	2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V, V_{IH} = 2.0V, I_{OL} = 8.0mA			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V					−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 0.5V			−100	μA
				V_O = 2.4V			+100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−20		−90	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX					280	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test with pin 21 at 4.5V, all other input pins at GND, all outputs open Am25S557 conditions the same except initialize with G (pin 11) at 4.5V, then GND.

SWITCHING TEST CIRCUIT



TC001460

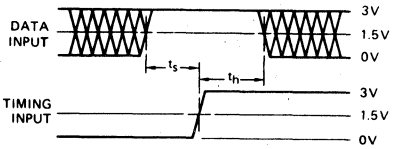
SWITCHING TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	5.0V	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 1.5V, 0.5V, 0.0V
t_{PLZ}	5.0V	2.8V, V_{OL}, 0.5V
t_{PZH}	0.0V	V_{OH}, 1.5V, 0.0V
t_{PZL}	5.0V	2.8V, 1.5V, V_{OL}

WF002350

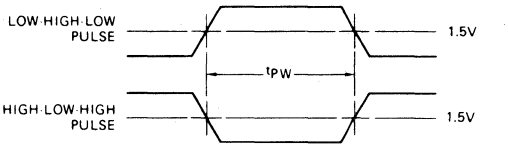
C_L Includes probe and jig capacitance.

SET-UP AND HOLD TIMES



WF001460

PULSE WIDTH



WF001270

Notes:1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25S557 Min	Typ	Max	MILITARY Am25S557 Min	Typ	Max	Units
t_{PD}	X_i, Y_i to S_0 to S_7	C_L = 30pF, R_L = 560Ω (See test figures)		45	60		55	70	ns
t_{PD}	X_i, Y_i to S_8 to S_{15} or $\overline{S}_{15}$			50	80		60	90	ns
t_s	X_i, Y_i to G Set-up Time		65			75			ns
t_h	X_i, Y_i to G Hold Time		−5			−5			ns
t_{PD}	G to S_1			30	45		30	50	ns
t_{PW}	Latch Enable Pulse Width		25	15		30	15		ns
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}			15	30		15	40	ns
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$			25	40		25	50	ns
t_{PLZ}	$\overline{OE}$ to S_1			15	30		15	40	ns
t_{PZH}	$\overline{OE}$ to S_1			20	35		20	40	ns
t_{PZL}	$\overline{OE}$ to S_1			20	35		20	40	ns

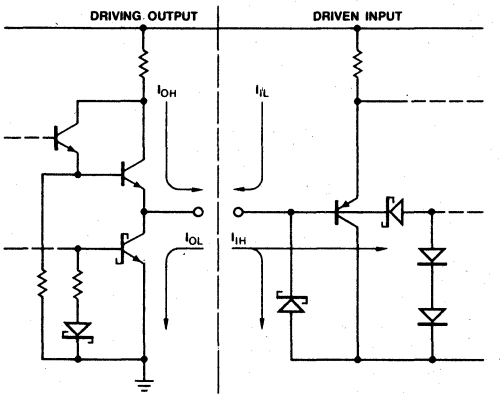
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25S558 Min	COMMERCIAL Am25S558 Typ	COMMERCIAL Am25S558 Max	MILITARY Am25S558 Min	MILITARY Am25S558 Typ	MILITARY Am25S558 Max	Units
t_{PD}	X_1, Y_1 to S_0 to S_7	C_L = 30pF, R_L = 580Ω (See test figures)		35	55		35	65	ns
t_{PD}	X_1, Y_1 to S_0 to S_{15} or $\overline{S}_{15}$			55	75		55	85	ns
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}			15	30		15	40	ns
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$			25	40		25	50	ns
t_{PLZ}	$\overline{OE}$ to S_1			15	30		15	40	ns
t_{PZH}	$\overline{OE}$ to S_1			20	35		20	40	ns
t_{PZL}	$\overline{OE}$ to S_1			20	35		20	40	ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25S557/Am25S558
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000380

RELATED PRODUCTS

Part No.	Description
Am29516/7	16 by 16-Bit Multiplier
Am25S05	4 by 2-Bit Multiplier
Am25LS14A	8-Bit Serial/Parallel Multiplier

Am25LS2568/Am25LS2569

Four-Bit Up/Down Counters with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced Low-Power Schottky technology

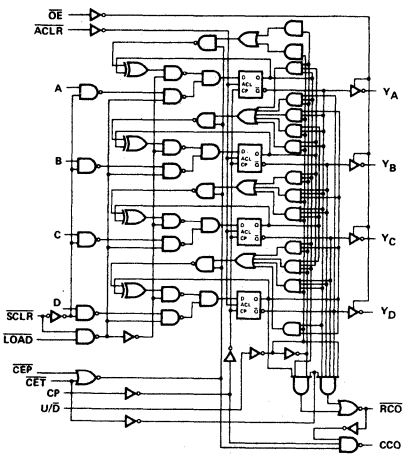
GENERAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input (U/$\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations require only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high-impedance state when HIGH and when LOW, the counter outputs are enabled.

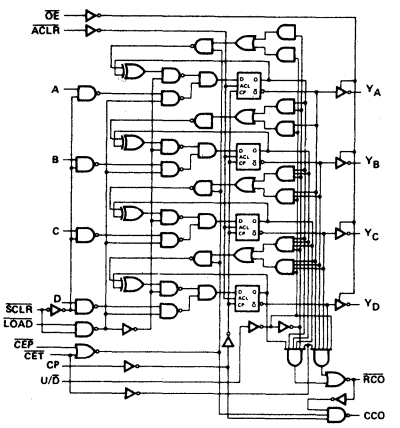
BLOCK DIAGRAM

Am25LS2568 (BCD)



BD001430

Am25LS2569 (BINARY)



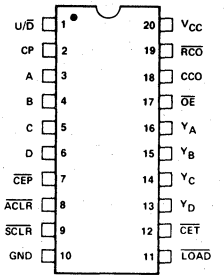
BD001420

03622B

Refer to Page 13-1 for Essential Information on Military Devices

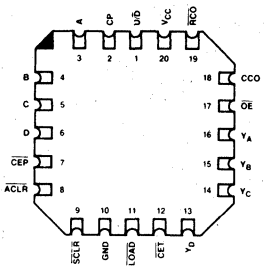
CONNECTION DIAGRAM
Top View

D-20-1



CD001640

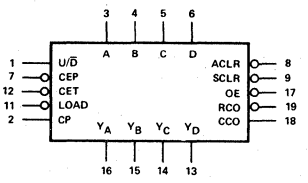
L-20-1



CD001650

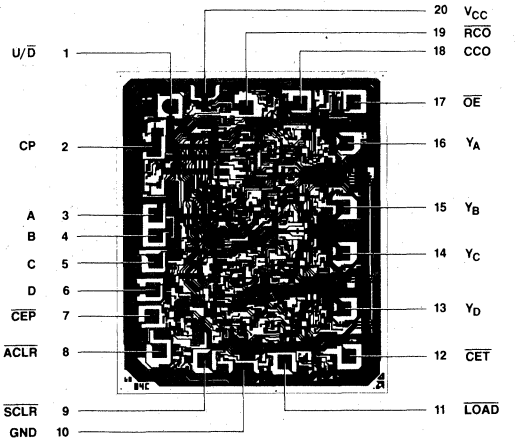
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000570

METALLIZATION AND PAD LAYOUT
Am25LS2568



DIE SIZE 0.087″ x 0.103″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2568/69 D C B

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2568/69** — Device type
  - BCD and Binary Counters

Valid Combinations	
Am25LS2568/ Am25LS2569	DC, DCB, DM, DMB FM, FMB LC, LM, LMB PC, PCB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 4, 5, 6	A, B, C, D	I	The four programmable data inputs.
7	$\overline{CEP}$	I	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count.
12	$\overline{CET}$	I	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
2	CP	I	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
11	$\overline{LOAD}$	I	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
1	$U/\overline{D}$	I	Up/Down Count Control. HIGH counts up and LOW counts down.
8	$\overline{ACLR}$	I	Asynchronous Clear. Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock.
9	$\overline{SCLR}$	I	Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW.
17	$\overline{OE}$	I	A HIGH on the output control sets the four counter outputs in the high-impedance, and a LOW enables the output.
16, 15 14, 13	Y_A, Y_B, Y_C, Y_D	O	The four counter outputs.
19	$\overline{RCO}$	O	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{RCO}$ is LOW at 0000.
18	CCO	O	Clock Carry Output. While counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Am25LS2568/2569
FUNCTION TABLE

	INPUTS												OUTPUTS					
MODE	LOAD	CEP	CET	U/$\overline{D}$	ASYNC CLEAR	SYNC CLEAR	$\overline{OE}$(1)	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	CLOCK CARRY
Clear (ASYNC)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	⊓⊔ (2)
Clear (SYNC)	X	X	X	1	1	0	0	X	X	X	X	↑	0	0	0	0	1	1
	X	X	X	0	1	0	0	X	X	X	X	↑	0	0	0	0	0	⊓⊔ (2)
Load	0	X	1	X	1	1	0	X	X	X	X	↑	$Q_n = D_n$				1	1
	0	X	0	0	1	1	0	0	0	0	0	↑	0	0	0	0	0	⊓⊔ (2)
	0	X	0	1	1	1	0	1	1	1	1(3)	↑	1	1	1	1(3)	0	⊓⊔ (2)
Count Up	1	0	0	1	1	1	0	X	X	X	X	↑	Q_{n+1}				(4)	(5)
Count Down	1	0	0	0	1	1	0	X	X	X	X	↑	Q_{n-1}				(6)	(5)
Inhibit	1	0	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	0	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
Output Disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	N.C.	N.C.

↑ = CLOCK LOW-to-HIGH transition
X = Don't Care
$D_n = D_0$ thru D_3 input level prior to clock transition

Q_{n+1} = Next higher count in binary sequence
Q_{n-1} = Next lower count in binary sequence
N.C. = No change

Notes:
1. Register performs all correct logic for any state of $\overline{OE}$, but $\overline{OE} = 0$ to view outputs.
2. Follows CLOCK if CET = CEP = 0, otherwise remains HIGH.
3. 1001 for LS68.
4. LOW for one full CLOCK cycle when maximum count is reached, otherwise remains HIGH.
5. Follows CLOCK when RC = 0.
6. LOW for one full CLOCK cycle when minimum count is reached, otherwise remains HIGH.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)				Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_i	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
				COM'L, I_{OH} = −2.6mA		2.4	3.2		
			$\overline{RCO}$, CCO	I_{OH} = −440μA	MIL	2.5	3.4		
					COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA				0.4	Volts
				I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{LOAD}$				−0.3	mA
				A, B, C, D, CP, $\overline{CEP}$				−0.4	
				$\overline{CET}$, $\overline{SCLR}$				−0.65	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V						20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V						0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX		V_O = 0.4V				−20	μA
				V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX				−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX					28	43	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ = HIGH, all other inputs = GND, all outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW		C_L = 15pF, R_L = 2.0kΩ		12	18	ns
t_{PHL}					14	21	
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH				12	18	ns
t_{PHL}					14	21	
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$				11	16	ns
t_{PHL}					6	10	
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$				15	23	ns
t_{PHL}					13	20	
t_{PLH}	Clock to $\overline{RCO}$				24	35	ns
t_{PHL}					18	26	
t_{PLH}	Clock to CCO				10	15	ns
t_{PHL}					10	15	
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO				10	15	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{ACLR}$ to Any Q				N.A.	N.A.	ns
t_{PHL}					17	26	
t_s	Set-up	A, B, C, D		22			ns
		$\overline{SCLR}$		20			
		$\overline{Load}$		30			
		U/$\overline{D}$		30			
		$\overline{CET}$, $\overline{CEP}$		25			
t_s	$\overline{SCLR}$ Recovery (inactive) to Clock			30			ns
t_h	Data Hold			0			ns
f_{max}	Maximum Clock Frequency (Note 1)			25	40		MHz
t_{pw}	Clock Pulse Width			25			ns
t_{PZH}	$\overline{OE}$ to Any Q; Enable					11	ns
t_{PZL}						19	
t_{PHZ}	$\overline{OE}$ to Any Q; Disable		C_L = 5.0pF, R_L = 2.0kΩ			18	ns
t_{PLZ}						24	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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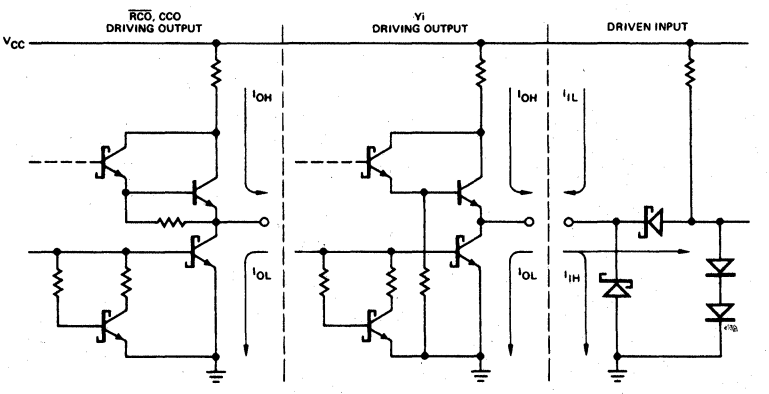
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW		C_L = 50pF R_L = 2.0KΩ		22		24	ns
t_{PHL}					29		35	
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH				22		24	ns
t_{PHL}					29		35	
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$				18		19	ns
t_{PHL}					17		21	
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$				26		28	ns
t_{PHL}					26		30	
t_{PLH}	Clock to $\overline{RCO}$				39		40	ns
t_{PHL}					34		39	
t_{PLH}	Clock to CCO				17		18	ns
t_{PHL}					22		27	
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO				16		17	ns
t_{PHL}					36		45	
t_{PLH}	$\overline{ACLR}$ to Any Q				N.A.		N.A.	ns
t_{PHL}					37		45	
t_s	Set-up	A, B, C, D		29		35		ns
		$\overline{SCLR}$		25		30		
		$\overline{Load}$		38		45		
		U/$\overline{D}$		38		45		
		$\overline{CET}$, $\overline{CEP}$		33		40		
t_s	SCLR Recovery (inactive) to Clock			39		50		ns
t_h	Data Hold			0		5		ns
f_{max}	Maximum Clock Frequency (Note 1)			20		18		MHz
t_{pw}	Clock Pulse Width			31		37		ns
t_{ZH}	$\overline{OE}$ to Any Q; Enable				16		20	ns
t_{ZL}					26		34	
t_{HZ}	$\overline{OE}$ to Any Q; Disable		C_L = 5.0pF R_L = 2.0KΩ		20		22	ns
t_{LZ}					30		36	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
N.A. not applicable.

Am25LS2568/2569
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000270

Note: Actual current flow direction shown.

Am26S and Am26LS Interface Family Index

Am26S02

Schottky Dual Retriggerable, Resettable Monostable Multivibrator

DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 28ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of only 1.0% over −55°C to + 125°C with R_X = 100kΩ
- Am26S02XC typical pulse width change of only 0.4% over 0°C to + 70°C with R_X = 100KΩ

GENERAL DESCRIPTION

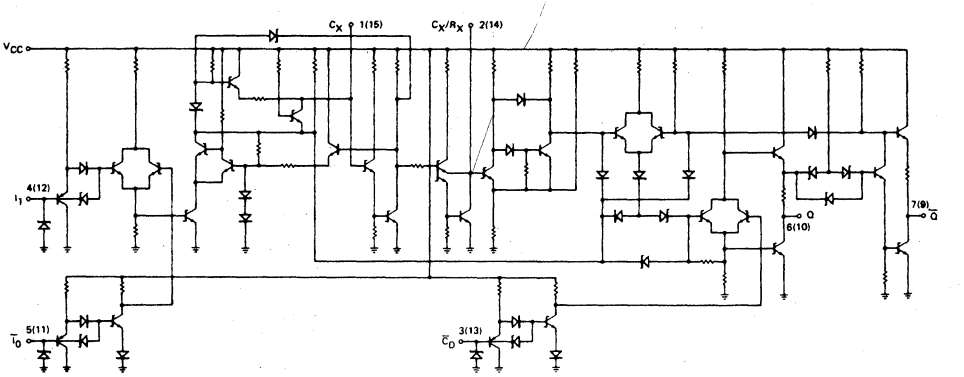
The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\overline{I}_0$ or $\overline{I}_1$ inputs.

The Am26S02XM has a typical pulse width change of only 1.0% over the full military −55°C to + 125°C temperature range and the Am26S02XC has a typical pulse width change of only 0.4% over the commerical 0°C to + 70°C temperature range with a R_X = 100kΩ.

SCHEMATIC DIAGRAM
(One Monostable Multivibrator Shown)

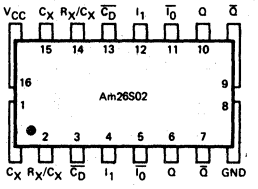


BD002140

04597A

Refer to Page 13-1 for Essential Information on Military Devices

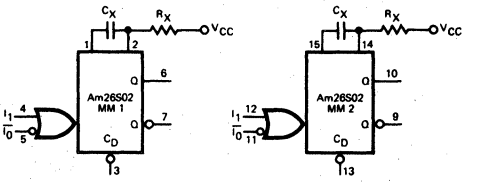
CONNECTION DIAGRAM
Top View



CD003050

Note: Pin 1 is marked for orientation

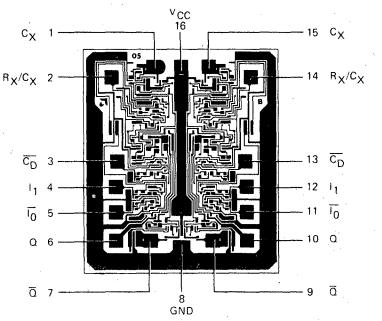
LOGIC SYMBOL



LS000830

V_{CC} = Pin 16
GND = Pin 8

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.062" x 0.071"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26S02 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - P – 16-pin plastic DIP
  - X – Dice
- **Am26S02** — Device type
  - Schottky Dual Multivibrator

Valid Combinations	
Am26S02	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
13	$\overline{C}_D$	I	Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.
11	$\overline{I}_0$	I	Active-LOW input. With I_1 LOW, a HIGH-to-LOW transition will trigger the monostable.
12	I_1	I	Active-HIGH input. With $\overline{I}_0$ HIGH, a LOW-to-HIGH transition will trigger the monostable.
10	Q	O	The TRUE monostable output.
9	$\overline{Q}$	O	The Complement monostable output.

FUNCTION TABLE

INPUTS			OUTPUTS	
OSC_D	I_1	I_1	$\overline{I}_0$	Q
L	X	X	L	H
H	H	X	L	H
H	L	↓	⎍	⎎
H	X	L	L	H
H	↑	H	⎍	⎎

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎎ = HIGH-LOW-HIGH Pulse
X = Don't Care

LOADING RULES (In Unit Loads)

Input/ Output	Pins	No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
C_X	Mono 1	1	–	–	–
R_X/C_X		2	–	–	–
$\overline{C}_D$		3	0.4	–	–
I_1		4	0.4	–	–
$\overline{I}_0$		5	0.4	–	–
Q		6	–	40	10
$\overline{Q}$	▼	7	–	40	10
GND		8	–	–	–
$\overline{Q}$	Mono 2	9	–	40	10
Q		10	–	40	10
$\overline{I}_0$		11	0.4	–	–
I_1		12	0.4	–	–
$\overline{C}_D$		13	0.4	–	–
R_X/C_X		14	–	–	–
C_X	▼	15	–	–	–
V_{CC}		16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

OPERATION RULES

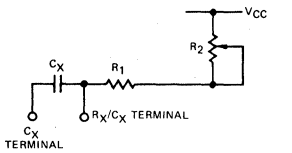
TIMING

1. Timing components C_X and R_X values.

Operating Temperature Range

	0°C to 70°C	−55°C to +125°C
R_X MIN	5kΩ	5kΩ
R_X MAX	100kΩ	50kΩ
C_X	any value	any value

2. Remote adjustment of timing.



TC001040

$R_1 + R_2 = R_x$
$R_1 \geq R_x MIN.$
$R_2 < R_x MAX. - R_1$

In the above arrangement, R_1 and C_x should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

10

OPERATION RULES (Cont.)

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly. Note that pulse width temperature stability improves as R_x increases.

4. Timing for $C_x \leqslant 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

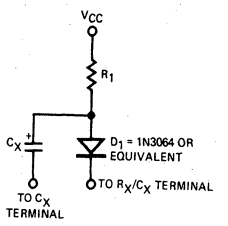
5. Timing for $C_x > 1000$ pF.

For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by:

$$t_{pw}Q = 0.30C_xR_x\left(1 + \frac{0.11}{R_x}\right)$$

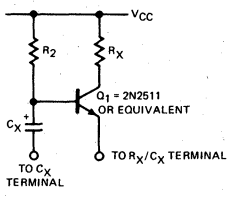
where

R_x is in kilohms
C_x is in picofarads
$t_{pw}Q$ is in nanoseconds



TC001030

$R_1 \leqslant 0.6 \times R_x$ MAX.



TC001020

$R_2 < 0.7 \times h_{FEQ1} \times R_x$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_x cannot withstand 1.0 volt reverse bias, one of the two circuit techniques shown below should be used to protect the electrolytic capacitor from the reverse voltage. The accuracy of the pulse width may be dependent on the diode (transistor) characteristics.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.26C_xR_x\left(1 + \frac{0.13}{R_x}\right)$$

The output pulse width for the transistor circuit is:

$$t_{pw}Q = 0.21C_xR_x\left(1 + \frac{0.16}{R_x}\right)$$

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_x MIN. $< R_x <$ R_xMAX. to obtain longer output pulse widths for a given C_x.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\overline{I}_0$ or input I_1 to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equations as follows:

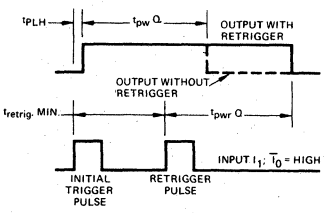
$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

where t_{PLH} is the propagation delay time from the $\overline{I}_0$ or I_1 input to the output. Note that t_{PLH} is typically 14ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is approximately:

t_{retrig}MIN. = $0.2C_x$
C is in picofarads
t is in nanoseconds



WF002460

CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the I_1 and $\overline{I}_0$ inputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

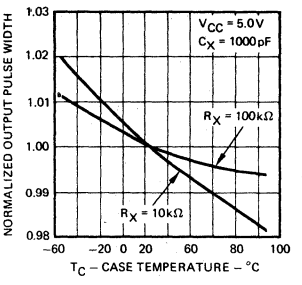
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}	2.5	2.8		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}		0.38	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA		−0.4	−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		−0.15	−0.4	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		0.1	20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX, V_{OUT} = 1.0V T_A = 25°C Only	−8	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = 5.0V, I_{IX} = 0.33mA (Notes 5 & 6)		48	69	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with pin 5 and 11 grounded and I_{IX} applied to pins 2 and 14.
6. I_{IX} is the current into the R_XC_X node to simulate R_X.

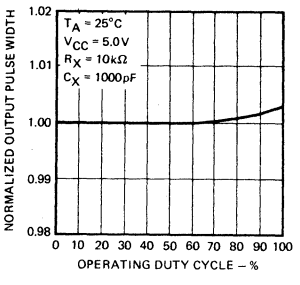
TYPICAL PERFORMANCE CURVES

Typical Normalized Output Pulse Width Versus Case Temperature



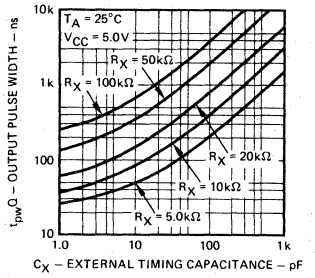
OP001280

Normalized Output Pulse Width Versus Operating Duty Cycle



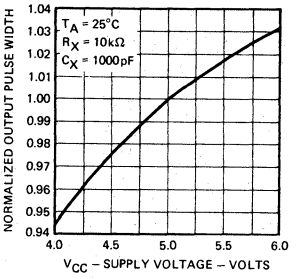
OP001320

Output Pulse Width Versus External Timing Capacitance



OP001260

Typical Normalized Output Pulse Width Versus Supply Voltage



OP001270

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	$\overline{I}_0$ to Q		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 5 kΩ, C_X = 0 pF		13	20	ns
t_{PHL}	$\overline{I}_0$ to $\overline{Q}$				15	23	ns
t_{PLH}	I_1 to Q				12	20	ns
t_{PHL}	I_1 to $\overline{Q}$				12	20	ns
t_{PLH}	Clear to $\overline{Q}$				21		ns
t_{PHL}	Clear to Q				9	13	ns
t_{pw}	Pulse Width	$\overline{I}_0$ HIGH or I_1 LOW		20	10		ns
		$\overline{I}_0$ LOW to I_1 HIGH		16	7		ns
		Clear LOW		24	16		ns
t_s	Clear Recovery (inactive) to Trigger			−10	−22		ns
$t_{pw}Q$ (Min)	Minimum Pulse Width Q Output		V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0 pF R_L = 1.0 kΩ	27	33	39	ns
$t_{pw}Q$	Pulse Width Q Output		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF (CK05 Type)	3.23	3.42	3.61	μs
R_X	Timing Resistor		0°C to 70°C	5		100	kΩ
			−55°C to +125°C	5		50	

Am26S10/Am26S11

Quad Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading

GENERAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

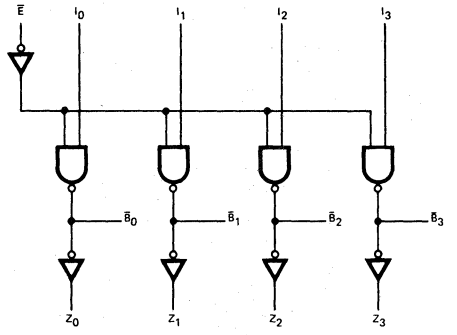
An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

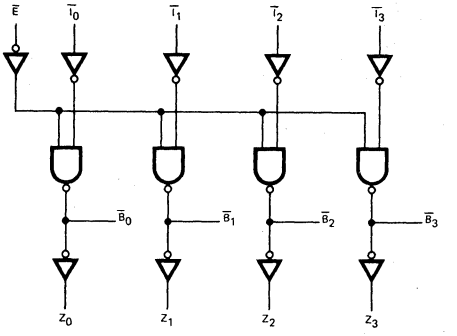
BLOCK DIAGRAM

Am26S10



BD001770

Am26S11



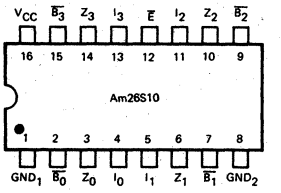
BD001760

RELATED PRODUCTS

Part No.	Description
26S12	Quad Bus Transceiver
26S12A	Quad Bus Transceiver
2915A	Quad Three-State Bus Transceiver with Interface Logic
2916A	Quad Three-State Bus Transceiver with Interface Logic
2917A	Quad Three-State Bus Transceiver with Interface Logic

04598A

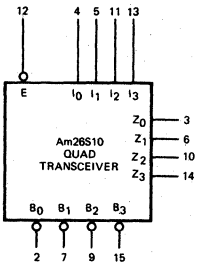
CONNECTION DIAGRAM
Top View



CD002080

Note: Pin 1 is marked for orientation

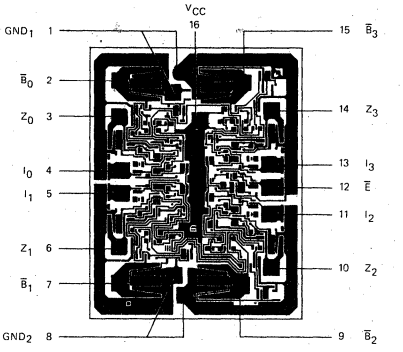
LOGIC SYMBOL



LS000810

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

METALLIZATION AND PAD LAYOUT
Am26S10



DIE SIZE 0.059" x 0.075"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26S10/11 **D** **C** **B**

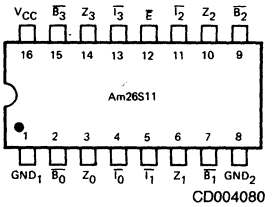
- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26S10/11** — Device type
  - Quad Bus Transceivers

Valid Combinations	
Am26S10 Am26S11	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

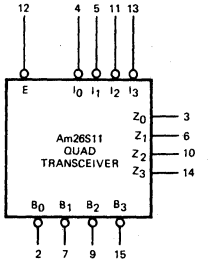
CONNECTION DIAGRAM
Top View



CD004080

Note: Pin 1 is marked for orientation

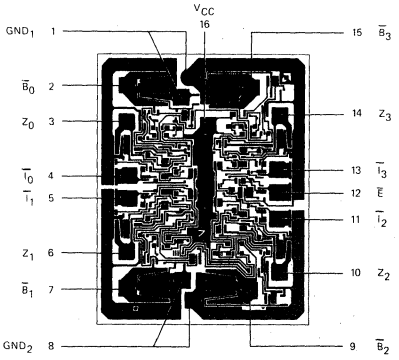
LOGIC SYMBOL



LS000800

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

METALLIZATION AND PAD LAYOUT
Am26S11



DIE SIZE 0.059" x 0.075"

TRUTH TABLES

Am26S10

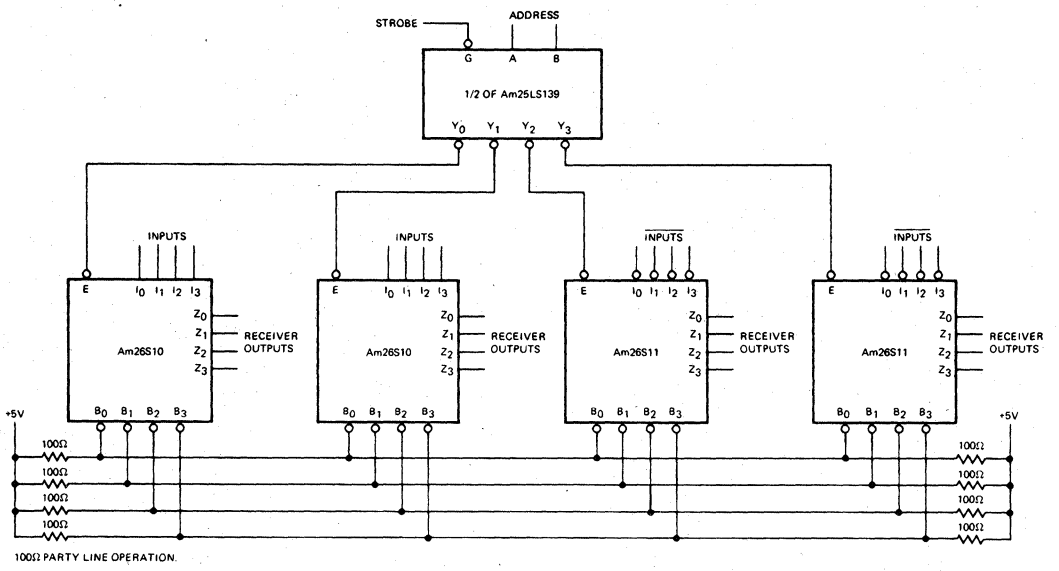
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

Am26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level X = Don't Care L = LOW Voltage Level
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

TYPICAL APPLICATION



AF001020

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus 200mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OH} = −1.0mA V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V	Enable			20	μA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX Enable = GND	Am26S10		45	70	mA
			Am26S11			80	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

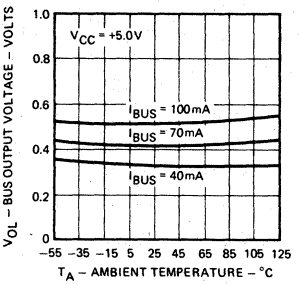
Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX		V_O = 0.8V			−50	μA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

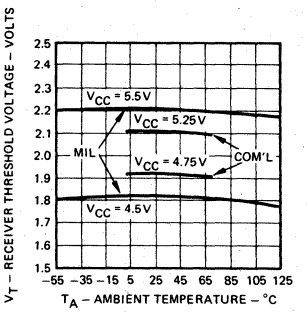
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



OP001370

Receiver Threshold Variation Versus Ambient Temperature



OP001380

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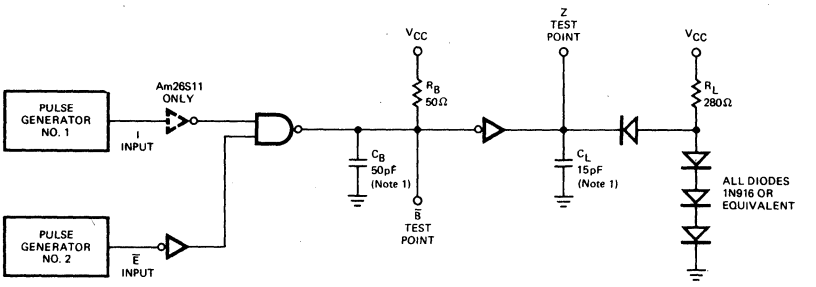
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT



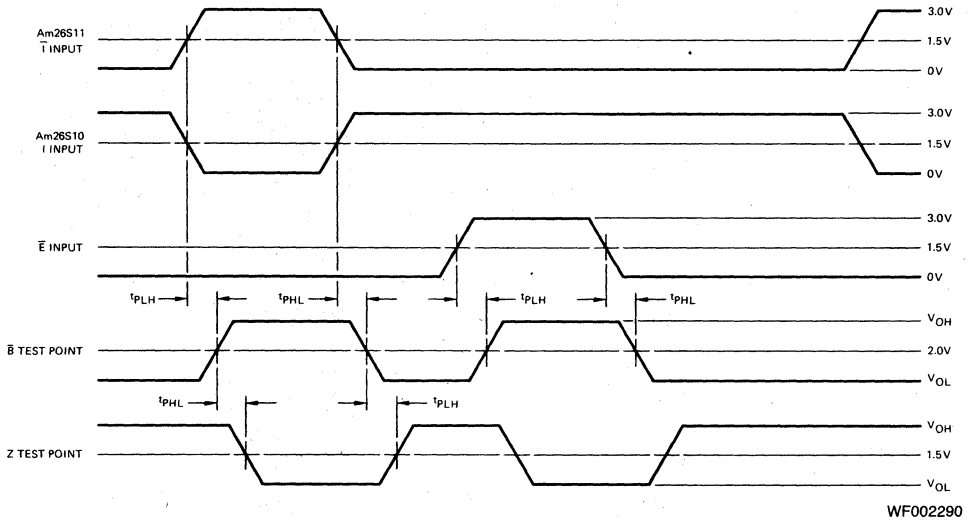
Note 1. Includes Probe and Jig Capacitance.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

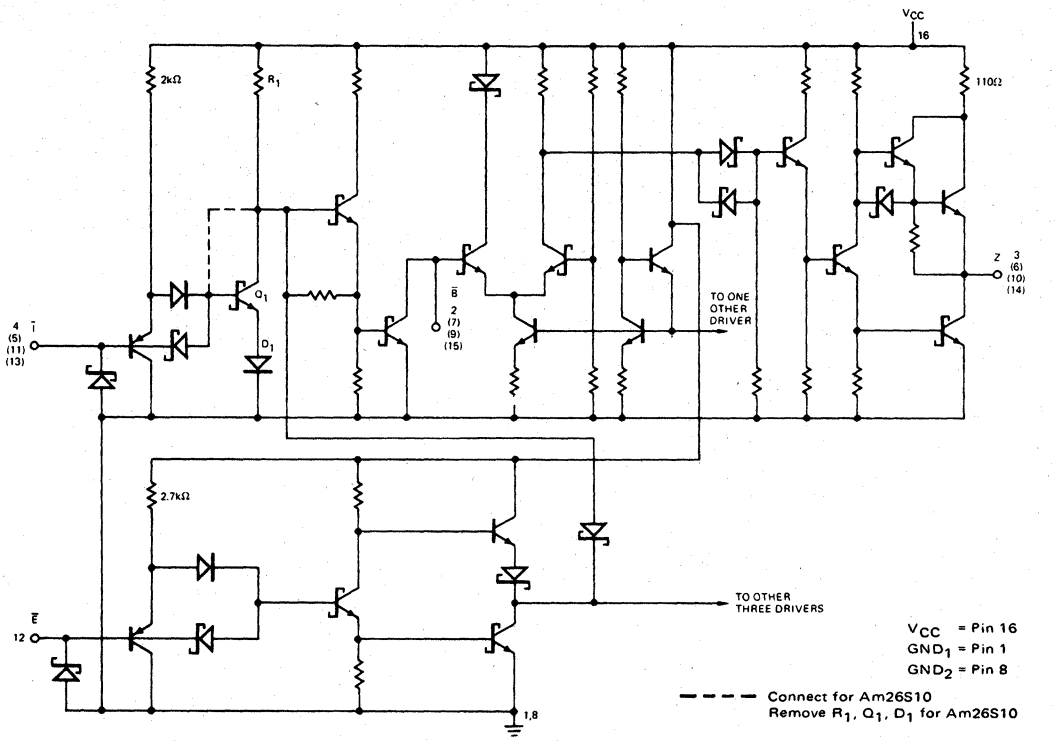
Parameters	Description		Test conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	Am26S10	R_B = 50 Ω C_B = 50 pF (Note 1)		10	15	ns
t_{PHL}					10	15	
t_{PLH}		Am26S11			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	Am26S10			14	18	ns
t_{PHL}					13	18	
t_{PLH}		Am26S11			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out		R_B = 50 Ω, R_L = 280 Ω C_B = 50 pF (Note 1) C_L = 15 pF		10	15	ns
t_{PHL}					10	15	
t_r	Bus		R_B = 50 Ω C_B = 50 pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

WAVEFORMS



Am26S10/Am26S11 SCHEMATIC DIAGRAM



IC000400

04598A

Refer to Page 13-1 for Essential Information on Military Devices

Am26S12/Am26S12A

Quad Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- Choice of receiver hysteresis characteristics

GENERAL DESCRIPTION

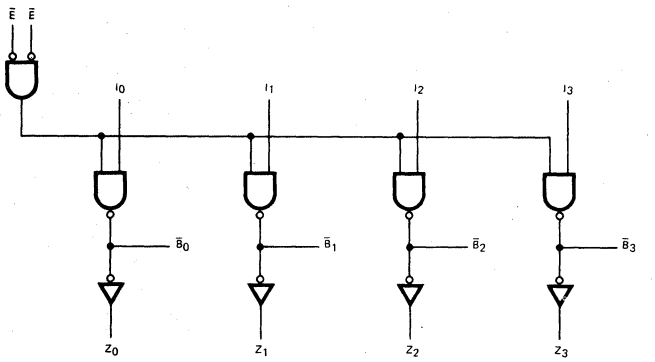
The Am26S12/Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL loads.

An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

BLOCK DIAGRAM



BD001800

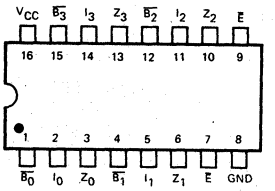
RELATED PRODUCTS

Part No.	Description
26S10	Quad Bus Transceiver
26S11	Quad Bus Transceiver
2915A	Quad Three-State Bus Transceiver with Interface Logic
2916A	Quad Three-State Bus Transceiver with Interface Logic
2917A	Quad Three-State Bus Transceiver with Interface Logic

05395A/05396A

Refer to Page 13-1 for Essential Information on Military Devices

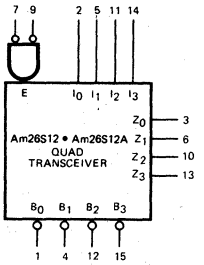
CONNECTION DIAGRAM
Top View



CD004070

Note: Pin 1 is marked for orientation

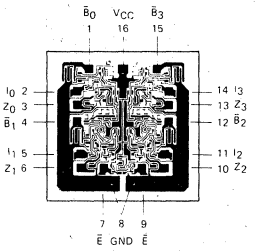
LOGIC SYMBOL



LS000860

V_{CC} = Pin 16
GND = Pin 8

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.071" x 0.072"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26S12/12A **D** **C** **B**

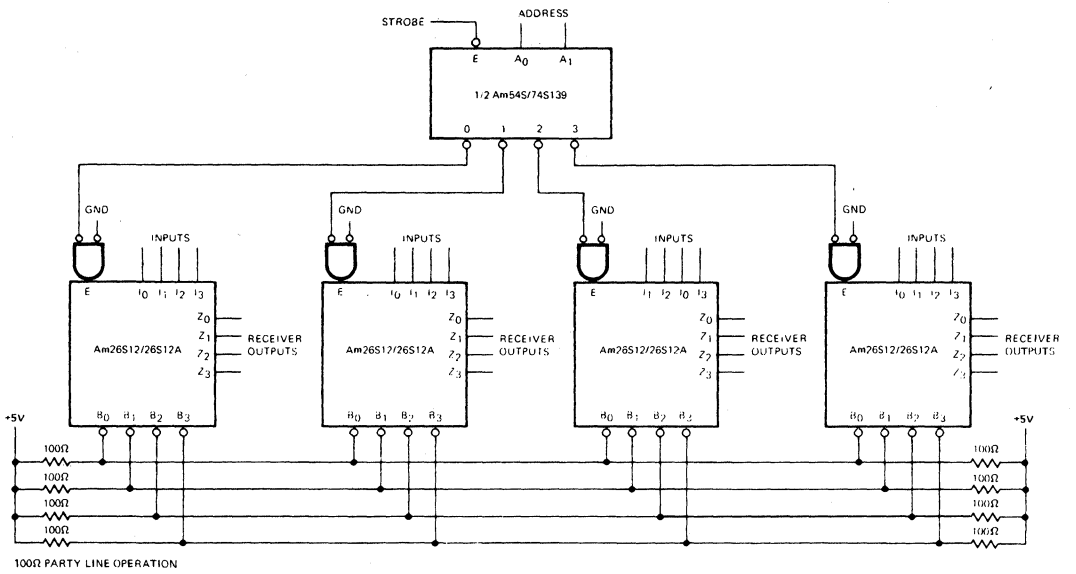
- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26S12/12A** — Device type
  - Quad Bus Transceivers

Valid Combinations	
Am26S12 Am26S12A	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Am26S12/26S12A APPLICATION



100Ω PARTY LINE OPERATION

AF001030

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into (Bus) 200mA
DC Output Current, Into Outputs
(Receiver) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
I_{CC}	Power Supply Current	V_{CC} = MAX				46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX or 0V; V_{BUS} = 4.0V; Driver in OFF State					100	µA
Driver Characteristics								
V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 100mA		0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX, V_I = 2.4V				1.0	40	µA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX, V_I = 0.4V				−0.4	−1.6	mA
Receiver Characteristics								
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −800µA, V_{IN} = V_{IL} (Receiver)			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA, V_{IN} = V_{IL} (Receiver)				0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12		1.8	2.0	2.2	Volts
			Am26S12A		2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12		1.2	1.4	1.6	Volts
			Am26S12A		1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H			0.4			Volts
I_{OS}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20		−55	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
3. Hysteresis characteristics data tested at 25°C only.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Conditions	Min	Typ	Max	Units
t_{PLH}	Turn Off Delay Input to Bus	C_{LB} = 15 pF, R_{LB} = 100 Ω		7	11	ns
t_{PHL}	Turn On Delay Input to Bus	C_{LB} = 300 pF, R_{LB} = 50 Ω		14	21	ns
t_{PLH}	Turn Off Delay Enable to Bus	C_{LB} = 15 pF, R_{LB} = 50 Ω		10	15	ns
t_{PHL}	Turn On Delay Enable to Bus	C_{LB} = 15 pF, R_{LB} = 50 Ω		10	15	ns
t_{PLH}	Turn Off Delay Bus to Output	C_L = 15 pF		18	26	ns
t_{PHL}	Turn On Delay Bus to Output	C_L = 15 pF		18	26	ns

Am26LS27/Am26LS28

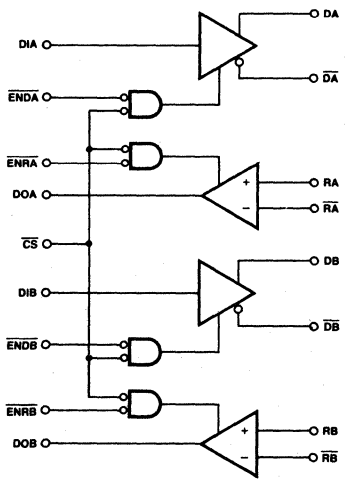
Dual EIA RS-485 Party Line Transceivers

DISTINCTIVE CHARACTERISTICS

- Dual EIA RS-aaa party line transceiver
- 5MHz max. baud rate
- Drives dual terminated twisted pair line with up to 32 transcievers on line
- Output short cicuit protected to V_{CM} limits
- High Z output at V_{CC} = max. and zero
- Separate enable gating for serial applications (27LS27)
- Three state receiver outputs with common enable (26LS28)

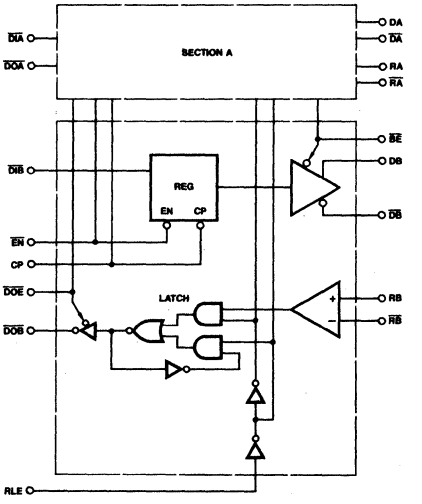
BLOCK DIAGRAM

Am26LS27



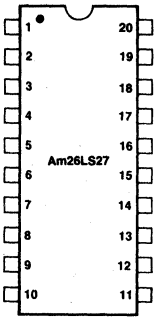
BD001720

Am26LS28

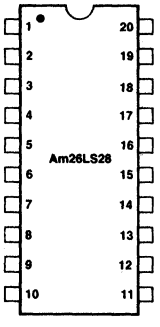


BD001710

CONNECTION DIAGRAM
Top View



CD002050



CD002040

Note: Pin 1 is marked for orientation

05390A/05391A

Am26LS29

Quad Three-State Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing

GENERAL DESCRIPTION

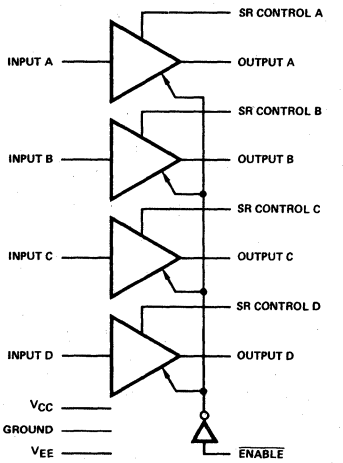
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

BLOCK DIAGRAM



BD001730

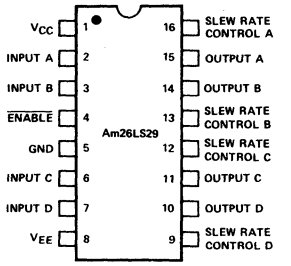
RELATED PRODUCTS

Part No.	Description
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

04599A

Refer to Page 13-1 for Essential Information on Military Devices

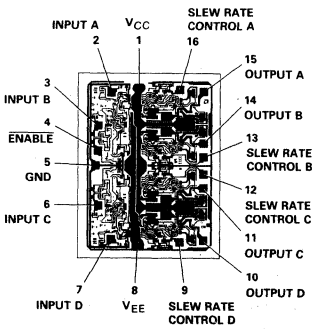
CONNECTION DIAGRAM
Top View



CD002060

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.070″ x 0.094″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS29 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26LS29** — Device type
  - Quad Single Line Driver

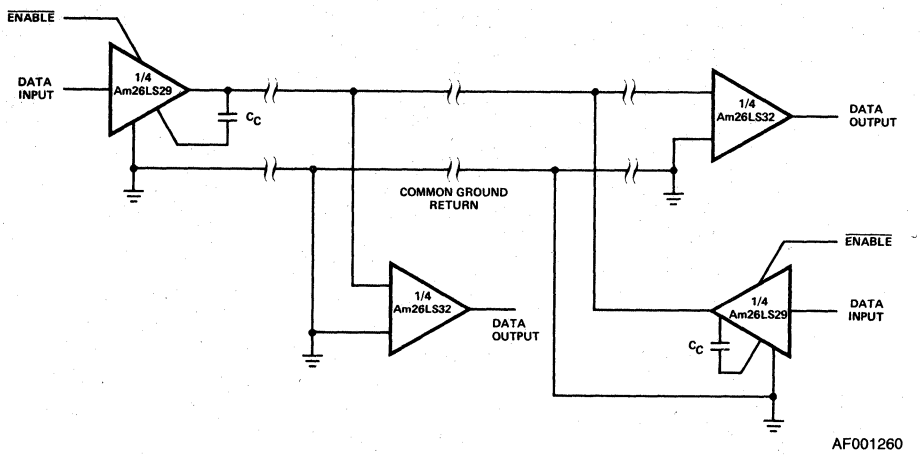
Valid Combinations	
Am26LS29	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

10

TYPICAL APPLICATION



AF001260

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage
V+ 7.0V
V− ..... −7.0V
Power Dissipation 600mW
Input Voltage ..... −0.5 to +15.0V
Output Voltage (Power Off) ..... ±15V
Lead Soldering Temperature (10) seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.75V to +5.25V
(V_{EE}) ..... −4.75V to −5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage (V_{CC}) ..... +4.5V to +5.5V
(V_{EE}) ..... −4.75 to −5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

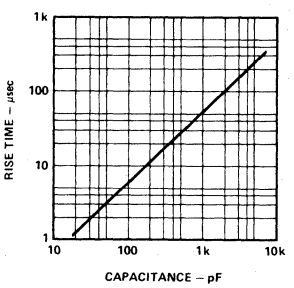
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_O	Output Voltage	$R_L = \infty$(Note 3)	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_X+	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 10V$		2.0	100	μA
I_X-			$V_O = -10V$		−2.0	−100	μA
I_S+	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−70	−150	mA
I_S-			$V_{IN} = 0.4V$		60	150	mA
I_{SLEW}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±110		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX	$V_O = 10V$		2.0	100	μA
			$V_O = -10V$		−2.0	−100	μA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9V minimum at −55°C.

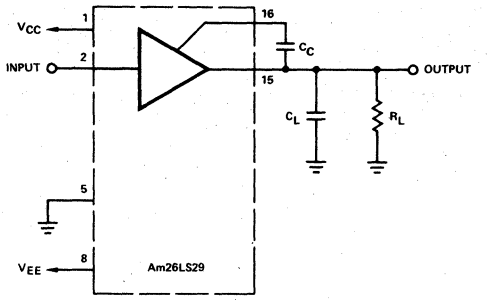
TYPICAL PERFORMANCE CURVES

Slew Rate (Rise or Fall Time) Versus External Capacitor



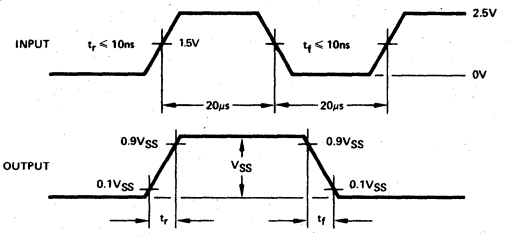
OP001290

SWITCHING TEST CIRCUIT



TC000850

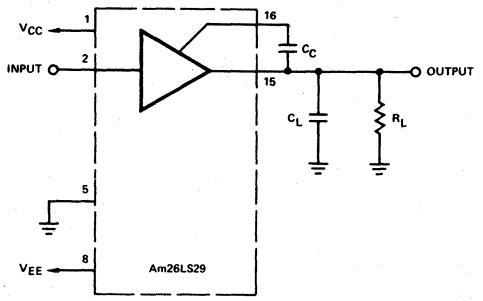
SWITCHING TEST WAVEFORM



WF002270

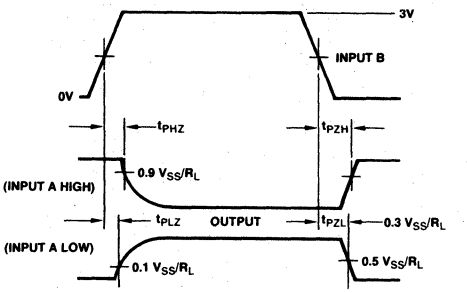
Figure 1. Rise Time Control.

SWITCHING TEST CIRCUIT



TC000860

SWITCHING TEST WAVEFORM



WF002260

Figure 2. Three State Delays

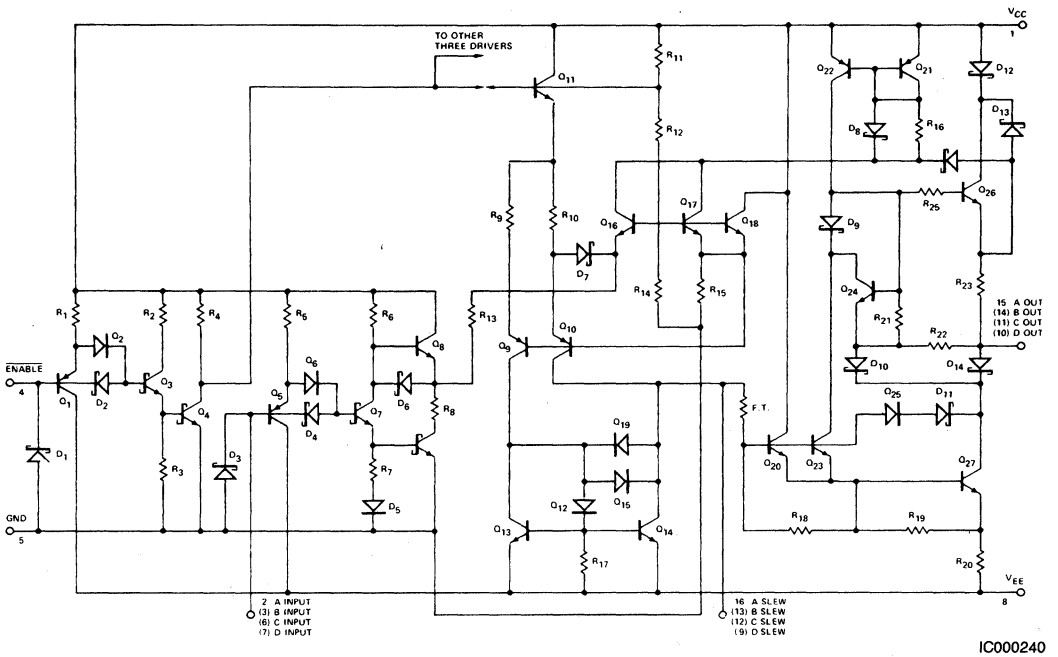
SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.0V$)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_r	Rise Time	$R_L = 450\ \Omega$, $C_L = 500$ pF, Fig. 1	$C_C = 50$ pF		3.0		μs
			$C_C = 0$ pF		120	300	ns
t_f	Fall Time	$R_L = 450\ \Omega$, $C_L = 500$ pF, Fig. 1	$C_C = 50$ pF		3.0		μs
			$C_C = 0$ pF		120	300	ns
Src	Slow Rate Coefficient	$R_L = 450\ \Omega$, $C_L = 500$ pF, Fig. 1			.06		μs/pF
t_{LZ}	Output Enable to Output	$R_L = 450\ \Omega$, $C_L = 500$ pF, $C_C = 0$ pF, Fig. 2			180	300	ns
t_{HZ}					250	350	
t_{ZL}		$R_L = 450\ \Omega$, $C_L = 500$ pF, $C_C = 0$ pF, Fig. 2.			250	350	
t_{ZH}					180	300	

04599A

Refer to Page 13-1 for Essential Information on Military Devices

Am26LS29EQUIVALENT CIRCUIT



IC000240

Am26LS30

Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing

GENERAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

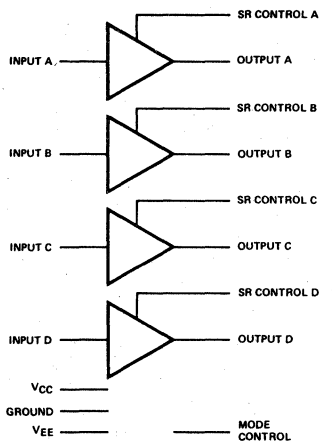
In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmissin line voltage of ±10V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

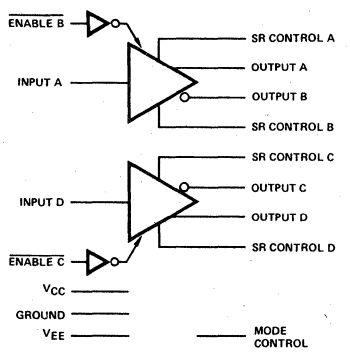
BLOCK DIAGRAM

Logic for Am26LS30 with Mode Control HIGH (RS-423)



BD001750

Logic for Am26LS30 with Mode Control LOW (RS-422)



BD001740

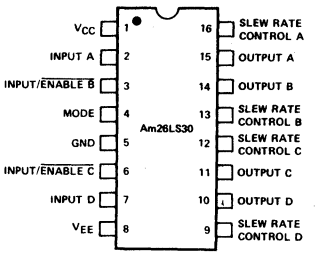
RELATED PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

04600A

Refer to Page 13-1 for Essential Information on Military Devices

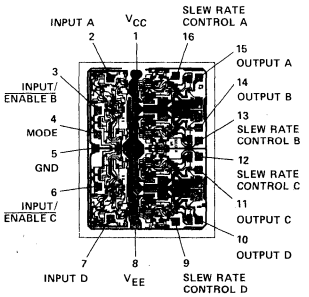
CONNECTION DIAGRAM
Top View



CD002070

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.070″ x 0.094″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS30 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - P – 16-pin plastic DIP
  - X – Dice
- **Am26LS30** — Device type
  - Dual Differential Line Driver

Valid Combinations	
Am26LS30	PC DC, DM FM XC, XM

Valid Combinations

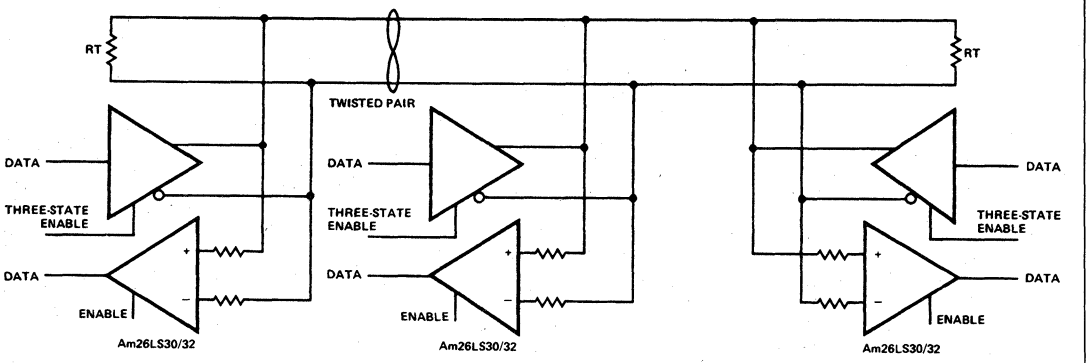
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

10

Am26LS30 FUNCTION TABLE

MODE	INPUTS		OUTPUTS	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

TYPICAL APPLICATION



AF001100

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage
V+ 7.0V
V− ..... −7.0V
Power Dissipation 600mW
Input Voltage ..... −0.5 to +15.0V
Output Voltage (Power Off) ..... ±15V
Lead Soldering Temperature (10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.75V to +5.25V
(V_{EE}) ..... GND

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage (V_{CC}) ..... +4.5V to +5.5V
(V_{EE}) ..... GND

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

EIA RS-422 Connection, Mode Voltage $\leq$ 0.8V

Parameters	Description	Test Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_O	Differential Output Voltage, $V_{A, B}$	$R_L = \infty$	V_{IN} = 2.0V		3.6	6.0	Volts
$\overline{V_O}$			V_{IN} = 0.8V		−3.6	−6.0	Volts
V_T	Differential Output Voltage, $V_{A, B}$	$R_L = 100\Omega$	V_{IN} = 2.0V	2.0	2.4		Volts
$\overline{V_T}$			V_{IN} = 0.8V	−2.0	−2.4		Volts
V_{OS}, $\overline{V_{OS}}$	Common Mode Offset Voltage	$R_L = 100\Omega$			2.5	3.0	Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common Mode Offset Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$		4.0	4.8		Volts
V_{CMR}	Output Voltage Common Mode Range	$V_{\overline{ENABLE}}$ = 2.4V		±10			Volts
I_{XA}	Output Leakage Current	V_{CC} = 0V	V_{CMR} = 10V			100	µA
I_{XB}			V_{CMR} = −10V			−100	µA
I_{OX}	Off State (High Impedance) Output Current	V_{CC} = MAX	$V_{CMR} \leq 10V$			100	µA
			$V_{CMR} \geq -10V$			−100	µA
I_{SA}, I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 6.0V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
		V_{IN} = 0.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6.0V		80	150	mA
I_{CC}	Supply Current				18	30	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1.0	40	µA
		$V_{IN} \leq 15V$			10	100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	µA
V_I	Input Clamp Voltage	I_{IN} = −12mA.				−1.5	Volts

DC CHARACTERISTICS over operating range unless otherwise specified

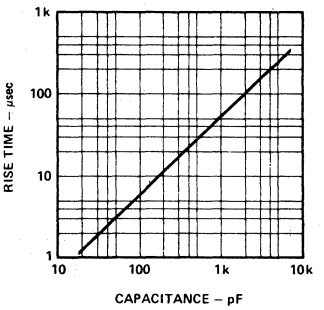
EIA RS-423 Connection, Mode Voltage ≥ 2.0V

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_O	Output Voltage	$R_L = \infty$(Note 3)	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_X+	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 6.0V$		2.0	100	μA
I_X-			$V_O = -6.0$		−2.0	−100	μA
I_S+	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
I_S-			$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±140		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9Vminimum at −55°C.

PERFORMANCE CURVE

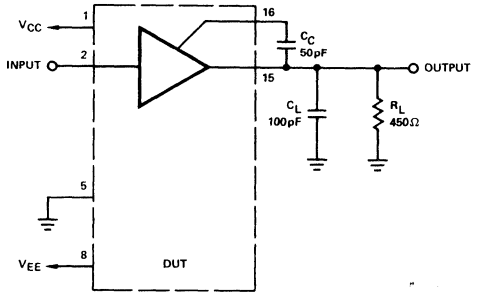
Slew Rate (Rise or Fall Time) Versus External Capacitor



OP001300

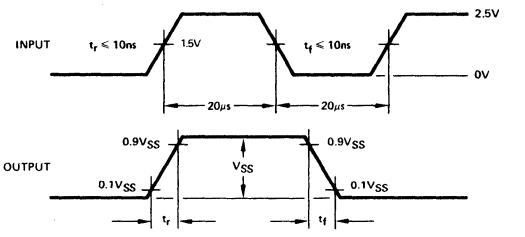
EIA RS-423 CONNECTION

SWITCHING TEST CIRCUIT



TC000940

SWITCHING TEST WAVEFORM

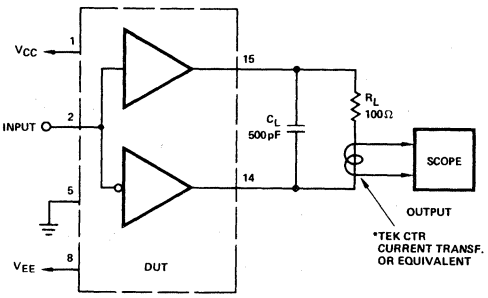


WF002270

Figure 1. Rise Time Control for RS-423.

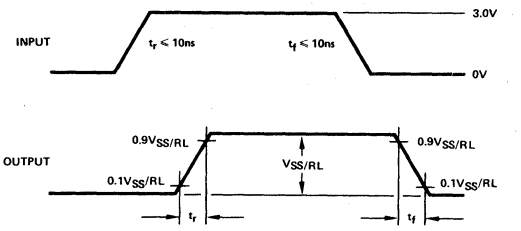
RS-422 CONNECTION

SWITCHING TEST CIRCUIT



TC000930

SWITCHING TEST WAVEFORM

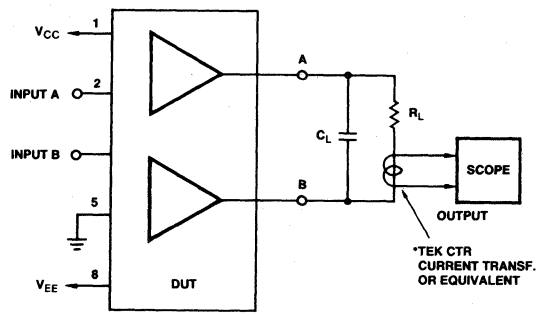


WF002310

*Current probe is the easiest way to display a differential waveform.

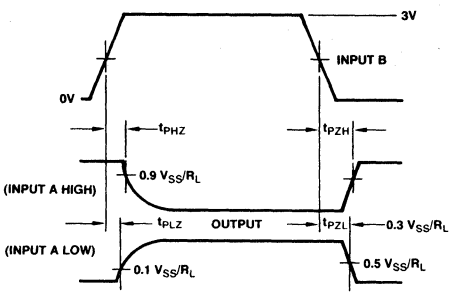
Figure 2.

SWITCHING TEST CIRCUIT



TC000920

SWITCHING TEST WAVEFORM



WF002260

Figure 3. Three State Delays.

SWITCHING CHARACTERISTICS

EIA RS-422 Connection, V_{CC} = 5.0V, V_{EE} = GND, Mode = 0.4V, T_A = 25°C

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_r	Differential Output Rise Time	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_f	Differential Output Fall Time	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{PDH}	Output Propagation Delay	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{PDL}	Output Propagation Delay	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{LZ}	Output Enable to Output	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 3		180	300	ns
t_{HZ}				250	350	
t_{ZL}		R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 3		250	350	
t_{ZH}				180	300	

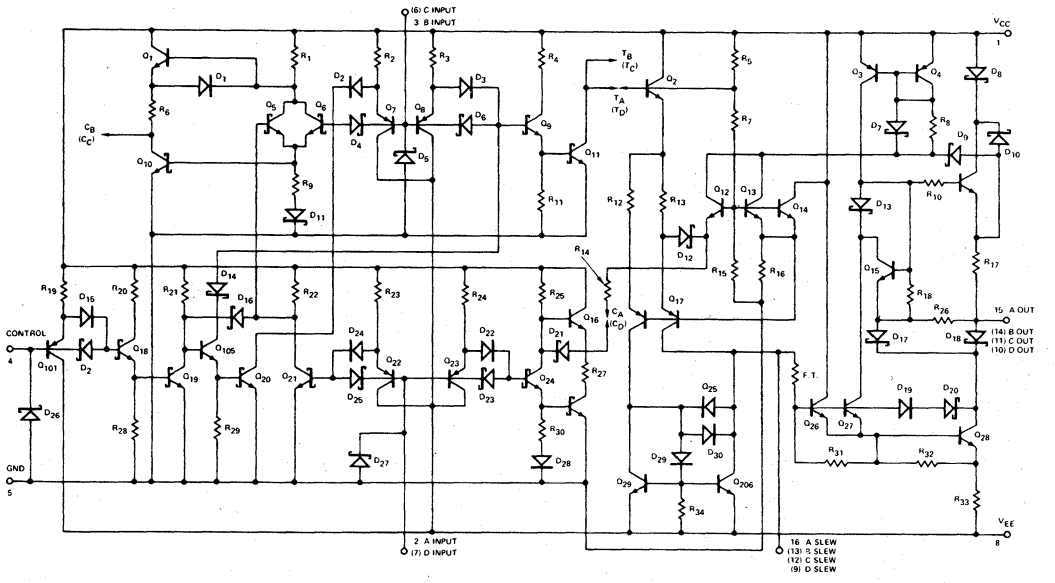
Notes: 1. Typical limits are at V_{CC} = 5.0 V, V_{EE} = GND, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

SWITCHING CHARACTERISTICS

RS-423 Connection, V_{CC} = 5.0V, V_{EE} = −5.0V, Mode = 2.4V, T_A = 25°C

Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_r	Rise Time	Fig. 1, R_L = 450 Ω, C_L = 500 pF	C_C = 50 pF		3.0		µs
			C_C = 0		120	300	ns
t_f	Fall Time	Fig. 1, R_L = 450 Ω, C_L = 500 pF	C_C = 50 pF		3.0		µs
			C_C = 0		120	300	ns
Src	Slow Rate Coefficient	Fig. 1, R_L = 450 Ω, C_L = 500 pF			.06		µs/pF
t_{PDH}	Output Propagation Delay	Fig. 1, R_L = 450 Ω, C_L = 500 pF, C_C = 0			180	300	ns
t_{PDL}	Output Propagation Delay	Fig. 1, R_L = 450 Ω, C_L = 500 pF, C_C = 0			180	300	ns

Am26LS30 EQUIVALENT CIRCUIT



IC000230

04600A

Refer to Page 13-1 for Essential Information on Military Devices

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing

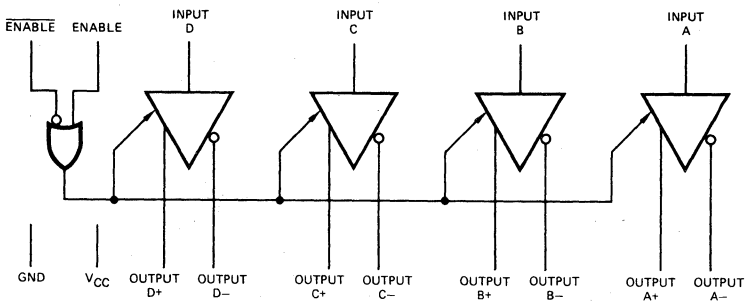
GENERAL DESCRIPTION

The Am26LS31 is a quad-differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

BLOCK DIAGRAM



BD001590

RELATED PRODUCTS

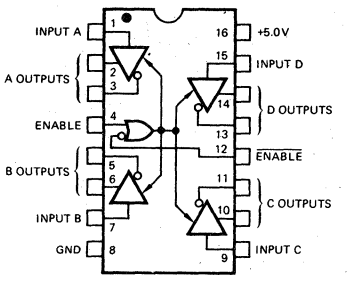
Part No.	Description
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

10

05392A

Refer to Page 13-1 for Essential Information on Military Devices

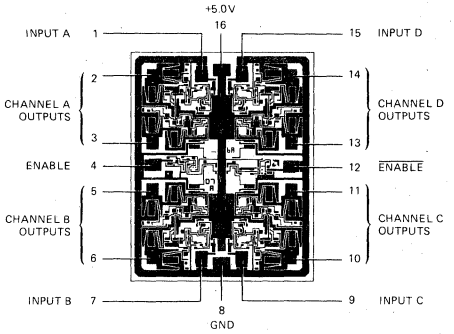
CONNECTION DIAGRAM
Top View



CD003070

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.067" x 0.084"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS31 **D** **C** **B**

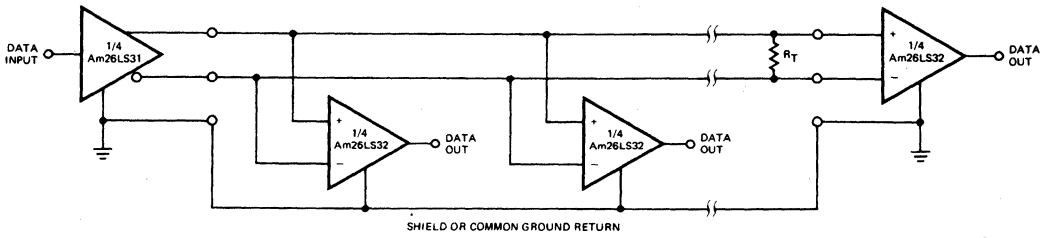
- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26LS31** — Device type
  - Quad Differential Line Driver

Valid Combinations	
Am26LS31	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

TYPICAL APPLICATION



BD002080

05392A

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range ..... −65°C to +150°C
Supply Voltage 7.0V
Input Voltage 7.0V
Output Voltage 5.5V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

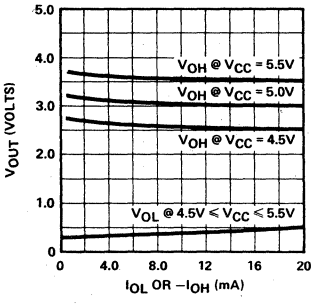
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −20mA		2.5	3.2		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 20mA			0.32	0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−0.20	−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 2.7V			0.5	20	μA
I_I	Input Reverse Current	V_{CC} = Max, V_{IN} = 7.0V			0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = MAX	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = 18mA			−0.8	−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max		−30	−60	−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max, all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

Notes: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

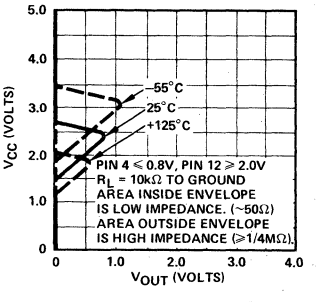
PERFORMANCE CURVES

Guaranteed V_{OH} and V_{OL} (T_A = −55°C to +125°C)



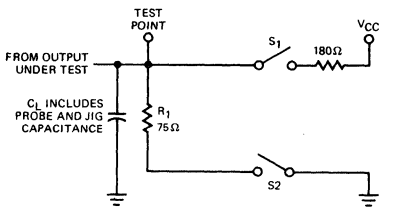
OP001440

V_{OUT} Versus V_{CC}



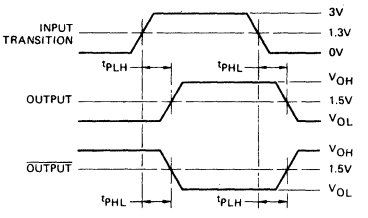
OP001310

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



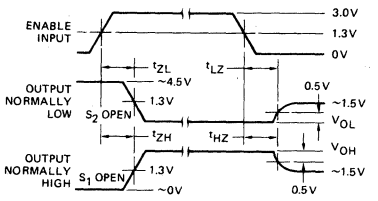
TC000980

PROPAGATION DELAY (Notes 1 and 3)



WF002390

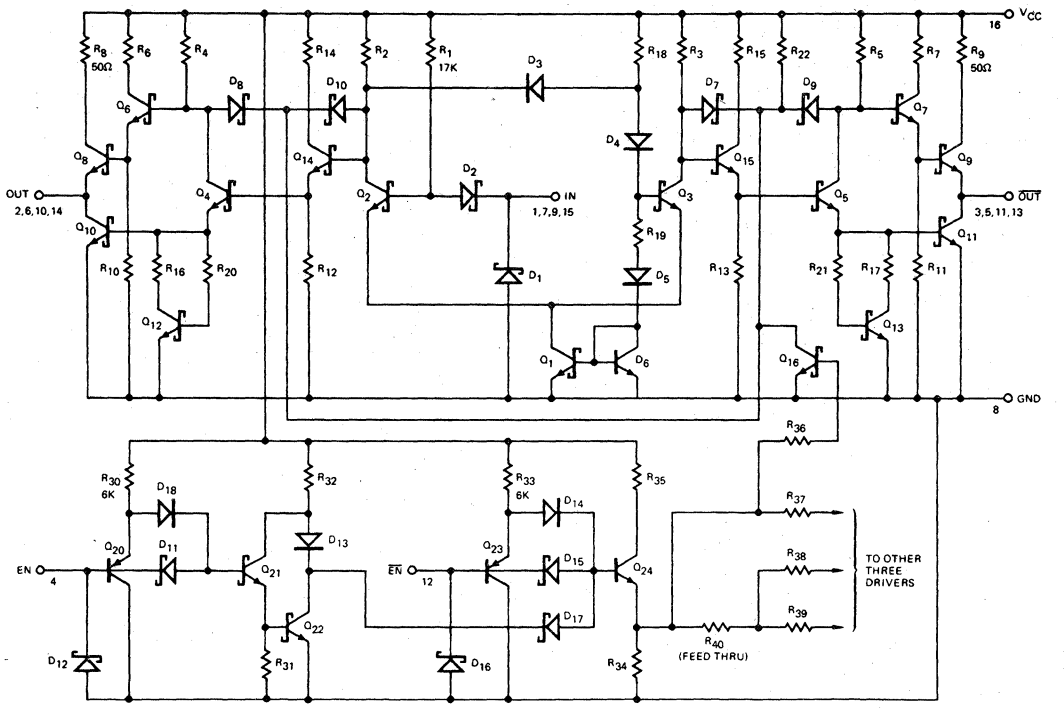
ENABLE AND DISABLE TIMES (Notes 2 and 3)



WF002380

Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 15$ns; $t_f \leq 6.0$ns.

EQUIVALENT CIRCUIT (1/4 Am26LS31)



IC000310

05392A

Refer to Page 13-1 for Essential Information on Military Devices

Am26LS32/Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
  - ±0.2V sensitivity over the input voltage range on Am26LS32;
  - ±0.5V sensitivity on Am26LS33
- 6k minimum input impedance with 30mV input hysteresis
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.

GENERAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

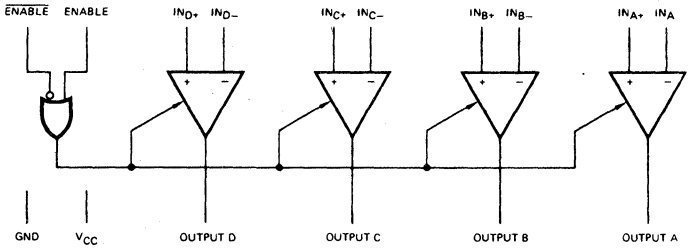
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

BLOCK DIAGRAM



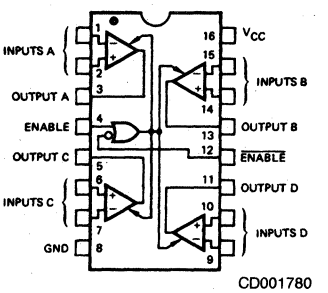
BD001640

RELATED PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS31	Quad High Speed Differential Line Receiver

05393A/05394A

CONNECTION DIAGRAM
Top View



CD001780

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS32/33 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26LS32/33** — Device type
  - Quad Line Receivers

Valid Combinations	
Am26LS32 Am26LS33	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7.0V
Commom Mode Range ..... ±25V
Differential Input Voltage ..... ±25V
Enable Voltage 7.0V
Output Sink Current 50mA
Storage Temperature Range ..... −65°C to +165°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

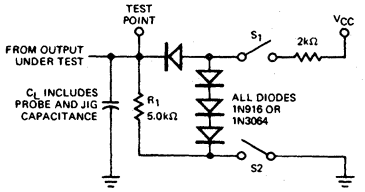
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, $-7V \leq V_{CM} \leq +7V$	−0.2	±0.06	+0.2	Volts
			Am26LS33, $-15V \leq V_{CM} \leq +15V$	−0.5	±0.12	+0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, $\Delta V_{IN} = +1.0V$, $\overline{V_{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min, $\Delta V_{IN} = -1.0V$, $\overline{V_{ENABLE}} = 0.8V$	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$			0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5V$			1	100	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = +1.0V$		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

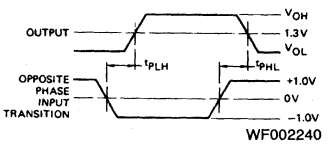
Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



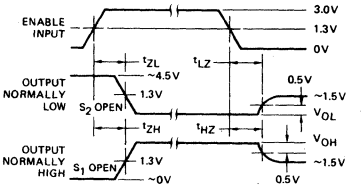
TC000841

PROPAGATION DELAY (Notes 1 and 3)



WF002240

ENABLE AND DISABLE TIMES (Notes 2 and 3)



WF002440

Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

Am26LS32B

Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- ±100mV sensitivity over V_{IN} range of 0V to 5V
- ±200mV sensitivity over V_{CM} range
- −7V to +12V input voltage range – differential or common mode
- Guaranteed input voltage hysteresis limits
  - 80mV minimum
  - 200mV maximum
- 3V maximum open circuit input voltage
- Three-state outputs disabled during power-up and power down
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over COM'L and MIL operating temperature ranges
- Single +5V supply
- Advanced low-power Schottky processing

GENERAL DESCRIPTION

The Am26LS32B is a quad line receiver designed to meet the requirements of RS-422 and RS-423, CCITT V.10 and V.11, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

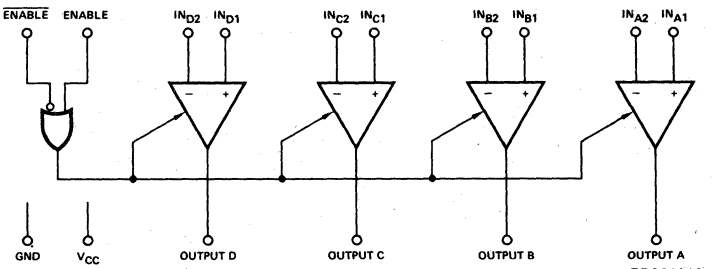
The Am26LS32B features an input sensitivity of 200mV over the common mode input voltage range of −7V to +12V.

The Am26LS32B is the first device in the Am26LS32 configuration to guarantee minimum hysteresis and propagation delay skew while maintaining better propagation delay guarantees than the Am26LS32. This allows a more critical analysis of performance in high noise environments and better performance in terms of signal quality, resulting in better system performance.

The Am26LS32B provides an enable and disable function common to all four receivers. It features three-state outputs with 24mA sink capability and incorporates a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32B is constructed using Advanced Low-Power Schottky processing.

BLOCK DIAGRAM



BD001810

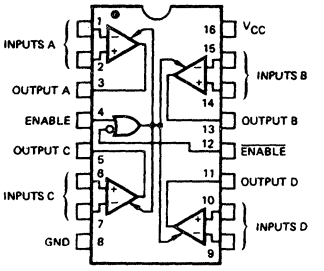
RELATED PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS33	Quad Differential Line Receiver

01024A

Refer to Page 13-1 for Essential Information on Military Devices

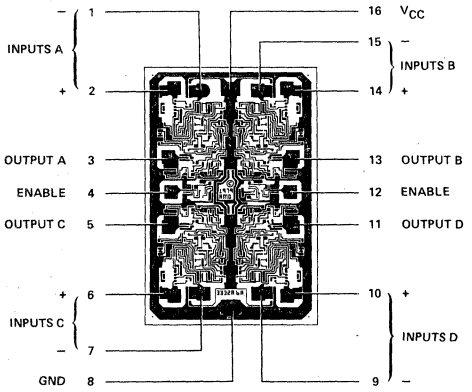
CONNECTION DIAGRAM
Top View



CD001780

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056″ x 0.084″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS32B **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26LS32B** — Device type
  - Quad Line Receiver

Valid Combinations	
Am26LS32B	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7.0V
Commom Mode Range ..... ±25V
Differential Input Voltage ..... ±25V
Enable Voltage 7.0V
Output Sink Current 50mA
Storage Temperature Range ..... −65°C to +165°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

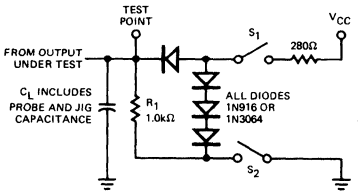
Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	$0 \leq V_{CM} \leq +5V$	−100	±60	100	mV
			$-7V \leq V_{CM} \leq +12V$	−200		200	
V_{HYST}	Input Hysteresis			80	120	200	mV
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	10		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, $\Delta V_{IN} = +1.0V$	$I_{OH} = -12mA$	2.0			Volts
		$V_{\overline{ENABLE}} = 0.8V$,	$I_{OH} = -1mA$	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min, $\Delta V_{IN} = -1.0V$	$I_{OL} = 16mA$			0.4	Volts
		$V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 24mA$			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			50	µA
			$V_O = 0.4V$			−50	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IH} = 2.7V$				20	µA
I_I	Enable HIGH Current	$V_{IN} = 5.5V$				100	µA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = +1.0V$		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

01024A

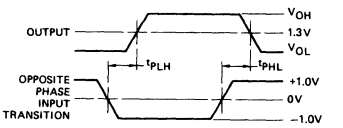
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



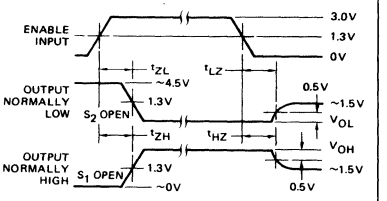
TC001010

PROPAGATION DELAY (Notes 1 and 3)



WF002450

ENABLE AND DISABLE TIMES (Notes 2 and 3)



WF002440

Notes: 1. Diagram shown for Enable LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay, Input to Output	$C_L = 50$ pF See test circuit		16	21	ns
t_{PHL}				17	21	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			1.5	3.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			16	22	ns
t_{ZH}				10	16	ns
t_{LZ}	Output Disable Time, ENABLE to Output	$C_L = 5$ pF See test circuit		11	18	ns
t_{HZ}				13	18	ns

SWITCHING CHARACTERISTICS* over operating range unless otherwise specified

Parameters	Descriptions	Test Conditions	COMMERCIAL Am26LS32B Min	COMMERCIAL Am26LS32B Max	MILITARY Am26LS32B Min	MILITARY Am26LS32B Max	Units
t_{PLH}	Propagation Delay, Input to Output	$C_L = 50$ pF See test circuits		26		26	ns
t_{PHL}				26		26	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			4.0		4.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			33		33	ns
t_{ZH}				22		22	ns
t_{LZ}	Output Disable Time, ENABLE to Output	$C_L = 5$ pF See test circuit		27		27	ns
t_{HZ}				27		27	ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

10

Am26LS34

Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- Meets all requirements of EIA Standards RS-422, RS-423, CCITT V.10 and V.11, and the new party line standard in development under EIA Project Number 1360.
- ±200mV sensitivity over input voltage range
- ±150mV sensitivity for $V_{CM} = 0$
- −7V to +12V common mode input voltage range
- 12kΩ minimum input impedance
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over MIL and COM'L temperature ranges
- Guaranteed input voltages hysteresis limits
  - 120mV minimum
  - 300mV maximum
- No internal failsafe
- Pin compatible with Am26LS32/32B/33

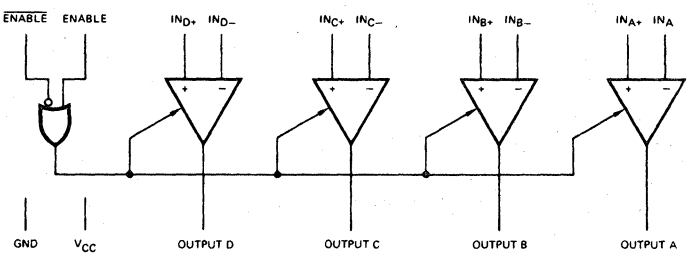
GENERAL DESCRIPTION

The Am26LS34 is a high performance, quad, differential line receiver. It has higher impedance and higher input voltage hysteresis than the similar Am26LS32B. The Am26LS34 also does not have internal fail-safe to allow greater user flexibility.

Input threshold sensitivty is specified for three different V_{CM} ranges. The improved sensitivity, guaranteed hysteresis and skew limits allow a more critical analysis of system performance in high noise environments and better system performance capability.

All performance parameters are guaranted over ±10% supplies and over the operating temperature range. In addition; I_{OL} is specified to 24mA for easy system bus interfacing.

BLOCK DIAGRAM



BD001640

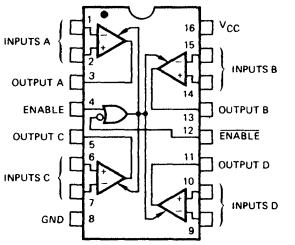
RELATED PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

01025A

Refer to Page 13-1 for Essential Information on Military Devices

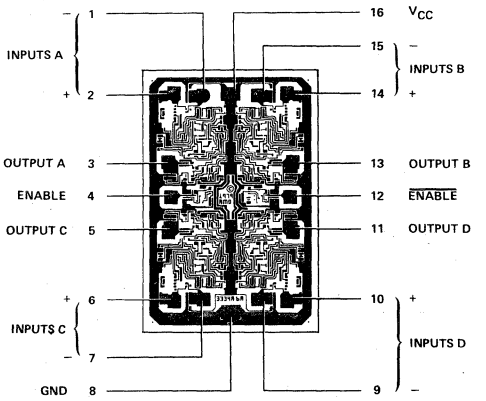
CONNECTION DIAGRAM
Top View



CD003090

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056″ x 0.084″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS34 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am26LS34** — Device type
  - Quad Line Receiver

Valid Combinations	
Am26LS34	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7.0V
Commom Mode Voltage ..... ±25V
Differential Input Voltage 30V
Enable Voltage 7.0V
Output Sink Current 50mA
Storage Temperature Range ..... −65°C to +165°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

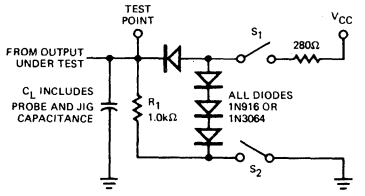
Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	$V_{CM} = 0V$	−150	±90	+150	mV
			$-7V \leq V_{CM} \leq +12V$	−200		+200	
			$-15V \leq V_{CM} \leq +15V$	−400		+400	
V_{HYST}	Input Hysteresis			120	180	300	mV
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		12k	20k	40k	Ω
I_{IN}	Input Current (Under Test)	$V_{IN} = +12V$			0.7	1.0	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -7V$			−0.5	−0.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, $\Delta V_{IN} = +1.0V$ $V_{ENABLE} = 0.8V$	−12mA	2.0			Volts
			−1mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{CC} = Min, $\Delta V_{IN} = -1.0V$ $V_{ENABLE} = 0.8V$	I_{OH} = 16mA			0.4	Volts
			I_{OL} = 24mA			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18mA$				−1.5	Volts
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			50	μA
			$V_O = 0.4V$			−50	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$			−0.03	−0.2	mA
I_{IH}	Enable HIGH Current	$V_{IH} = 2.7V$			0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5V$			1	100	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = +1.0V$		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

01025A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



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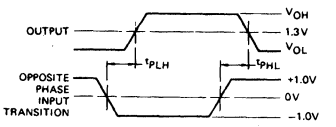
PROPAGATION DELAY (Notes 1 and 3)



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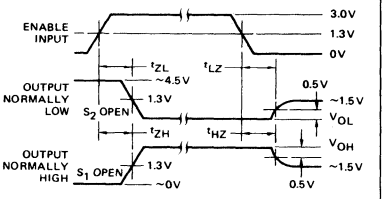
ENABLE AND DISABLE TIMES (Notes 2 and 3)



WF002440

Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator Rate ≤ 1.0MHz; $Z_o = 50\Omega$; t_r, $t_f \leq 2.5$ns.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay, Input to Output	$C_L = 50$ pF See test circuit		18	24	ns
t_{PHL}				20	24	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			2	4	ns
t_{ZL}	Output Enable Time, ENABLE to Output			16	22	ns
t_{ZH}				10	16	ns
t_{LZ}	Output Disable Time, ENABLE to Output	$C_L = 5$ pF See test circuit		11	18	ns
t_{HZ}				13	18	ns

SWITHCING CHARACTERISTICS* over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am26LS34 Min	COMMERCIAL Am26LS34 Max	MILITARY Am26LS34 Min	MILITARY Am26LS34 Max	Units
t_{PLH}	Propagation Delay, Input to Output	$C_L = 50$ pF See test circuit		30		30	ns
t_{PHL}				30		30	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			±5		±5	ns
t_{ZL}	Output Enable Time, ENABLE to Output			33		33	ns
t_{ZH}				22		22	ns
t_{LZ}	Output Disable Time, ENABLE to Output	$C_L = 5$ pF See test circuit		27		27	ns
t_{HZ}				27		27	ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am26LS38

Quad Differential Backplane Transceiver

PRELIMINARY

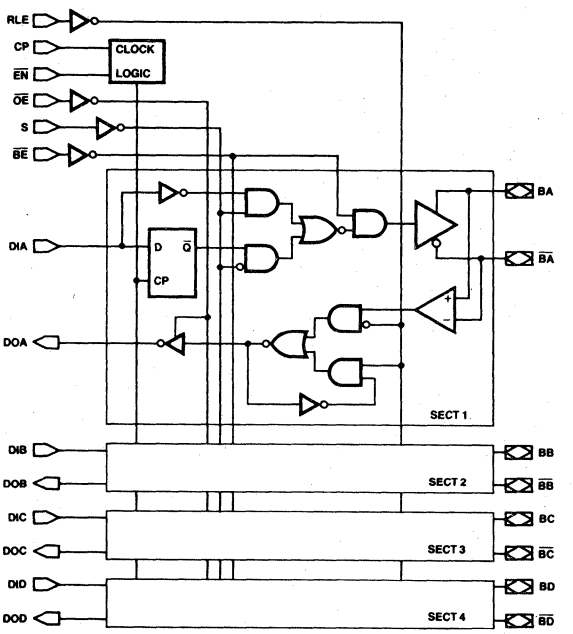
DISTINCTIVE CHARACTERISTICS

- 10Mb data rate
- 0.45V DC noise margin
- Biasing line terminations allow low voltage swing while maintaining high noise margin
- Pair delay 55ns maximum
- Controlled driver skew to minimize noise
- Driver register and receiver latch with register bypass mode
- Driver output short-circuit protected to V_{CC} limits
- Outputs disabled during power-up and down
- Three-state receiver outputs maintain Hi-Z during power-up and down and over V_{CC} range

GENERAL DESCRIPTION

The Am26LS38 is a high performance backplane transceiver designed to integrate Schottky TTL performance, high noise immunity and wired logic capability into a low cost differential backplane structure. The resulting backplane can have up to 24 receiver unit loads in a party-line, wired-OR logic configuration, with a guaranteed fail-safe state, and operates from a single 5V power supply.

BLOCK DIAGRAM



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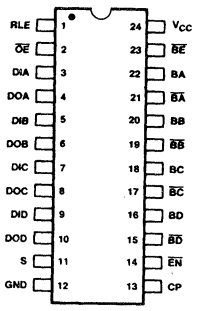
Refer to Page 13-1 for Essential Information on Military Devices

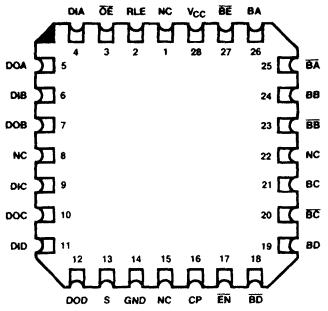
CONNECTION DIAGRAM
Top View

DIP



CD001830

Chip-Pak
L-28-1



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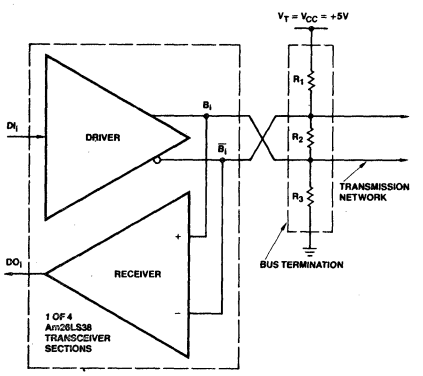
Note: Pin 1 is marked for orientation

SYSTEM CONNECTION DIAGRAM



CD001590

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am26LS38 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin SLIM DIP
  - L– 28-pin Chip-Pak
  - X– Dice
- **Am26LS38** — Device type
  - Quad Differential Backplane Transceiver

Valid Combinations	
Am26LS38	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	BA, BB, BC, BD (B_1), $\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$ (B_i)	I/O	Paired open emitter (B_i)/open collector ($\overline{B_i}$) driver outputs and receiver inputs. The driver outputs are either simultaneously active or simultaneously inactive. In the inactive state (DI_i = LOW) both drivers (B_i and $\overline{B_i}$) are turned off and the voltage differential representing the OFF state is determined by the line terminating resistor networks. In the active state (DI_i = HIGH), both drivers are driven on and act to reverse the voltage differential across the line to produce the ON state. The open-emitter/open-collector outputs are always connected in a wired-OR (or wired-AND) configuration. A driver is disabled by making its outputs inactive.
23	$\overline{BE}$	I	Bus Enable operates to enable or disable all output drivers by making them inactive when $\overline{BE}$ = HIGH and controlled by data input when $\overline{BE}$ = LOW.
13	CP	I	Clock Pulse input to the driver register enters data on the LOW-to-HIGH transition.
	DIA, DIB, DIC, DID (DI_i)	I	Data inputs to each driver's buffer or register. A HIGH input to DI_i will result in an active (ON) output. A LOW input will cause an inactive (OFF) output.
	DOA, DOB, DOC, DOD (DO_i)	O	Receiver data latch outputs. An inactive bus (OFF state) will produce a LOW DO_i output and an active bus (ON state) will produce a HIGH DO_i output.
14	$\overline{EN}$	I	Clock Enable for the driver registers. $\overline{EN}$ = LOW enables DI_i data to be clocked into the respective register. $\overline{EN}$ = HIGH acts to hold previous data in each register regardless of the state of CP.
2	$\overline{OE}$	I	Output Enable for the receiver latch output buffer. When $\overline{OE}$ is LOW the outputs are enabled. When $\overline{OE}$ is HIGH all receiver outputs are in the high impedance state.
1	RLE	I	Receiver Latch Enable for the receiver latches. When RLE is HIGH the latches are transparent. When RLE is LOW received data meeting the setup and hold requirements relative to the HIGH-to-LOW transition of RLE will be stored.
11	S	I	Select input control for the drivers. When S is HIGH driver data from the registers will be selected (Register Mode). When S is LOW (Buffer Mode) the drivers respond to the DI_i inputs directly, bypassing the driver registers.

FUNCTION TABLE

Inputs									Outputs			Function
RLE	CP	$\overline{EN}$	$\overline{OE}$	S	$\overline{BE}$	DI_i	B_i	$\overline{B_i}$	B_i	$\overline{B_i}$	DO_i	
H	X	X	L	L	L	L	NA	NA	L	H	L	Driver buffer mode (loop test)
H	X	X	L	L	L	H	NA	NA	H	L	H	
H	↑	L	L	H	L	L	NA	NA	L	H	L	Driver register mode
H	↑	L	L	H	L	H	NA	NA	H	L	H	
H	X	X	L	X	H	X	L	H	NA	NA	L	Receiver latch mode
H	X	X	L	X	H	X	H	L	NA	NA	H	
L	X	X	L	X	H	X	X	X	X	X	DO_{in-1}	Receiver in circulation
X	X	X	H	X	H	X	X	X	X	X	Z	Receiver output in high impedance state

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
DO_{in-1} = Previous state of DO_i
Z = High impedance
X = Don't care
NA = Not applicable

FUNCTIONAL DESCRIPTION

The Am26LS38 represents a new approach in backplane transceiver design. Its unipolar differential signalling scheme minimizes problems associated with crosstalk and the loss of noise immunity due to common mode voltage while providing high speed, party line and wired logic capabilities.

A good ground system and shielding are the best methods for limiting noise on the backplane. Ground planes can significantly reduce inductive ground voltage ringing. Where multilayer PC backplane are not a reasonable choice, a differential bus can be created using the Am26LS38 and twisted pair or any balanced transmission medium.

A backplane designed with an Am26LS38 has 3 main elements; 1) a driver section, 2) a receiver section, 3) and a controlled impedance differential line with a pre-biasing line termination. The scheme for driver, receiver, and termination resistors is shown in Figure A.

SYSTEM OPERATION

The system has two operational states.

1. Active – driver outputs on
2. Passive – driver outputs off

This 2-state (active/passive) operation makes passive or wired logic functions possible. In the passive state, the lines assume a known polarity and voltage (pre-biased bus). The passive bus state may be assigned either the false (wired-OR) or true (wired-AND) sense, potentially reducing the number of backplane signal lines.

The 2-state driver employs active pull-down (open collector) and active pull-up (open emitter) output stages (Figure A). When a driver is active, both output stages turn on. This impresses a 0.5V minimum voltage differential on the bus, reversing the voltage across R_2. In the passive mode both output stages are off. The voltage levels and polarities return to the conditions set by the pre-biasing resistive network. In either state the voltage across the differential lines are symmetrical about $V_{CC}/2$. The system achieves high speeds because the voltage levels required to change state are very close together.

The receiver is designed with a ±50mV threshold voltage. This low threshold level combined with a driver output greater than 500mV provides a high degree of tolerance to attenuation and reflection effects in the cable. Receiver hysteresis provides differential noise immunity. Without hysteresis, a small amount of noise around the switching threshold could cause errors.

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Refer to Page 13-1 for Essential Information on Military Devices

Propagation delay skew (t_{PHL}–t_{PLH}) is controlled. The system allows up to 1.5V of common mode voltage.

TERMINATING THE TRANSMISSION LINE OR BUS

Common mode reflections in the line can be reduced significantly by symmetrically terminating the bus. This increases the tolerance to common mode noise. Centering the network at $V_{CC}/2$ ($R_1 = R_3$) further improves the performance by causing all induced noise and reflections to appear as a common mode signal (Figure B).

Figure B. Object Circuit

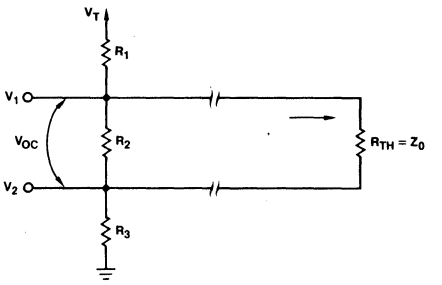

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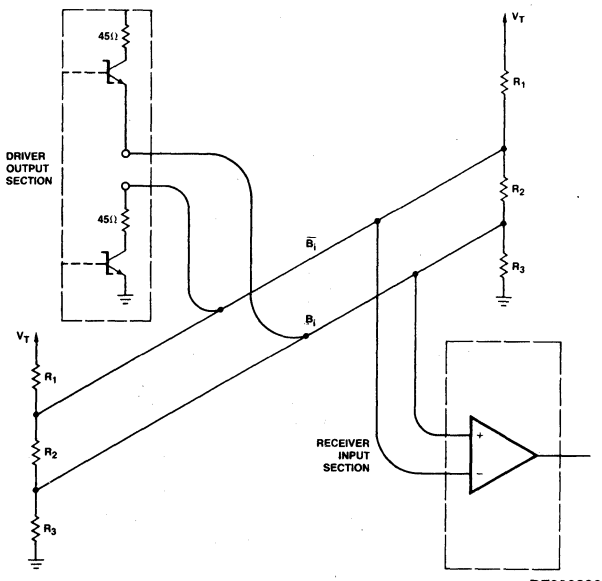
Figure A. The Scheme for Driver, Receiver, and Termination Resistors



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A first order approximation of resistor values may be developed by letting the ratio of R_1 to R_2 be 2:1, and the Thevenin equivalent resistance of the termination equal the characteristic impedance of the line (Z_0).

Then:

$$(1)\quad V_{OC} = V_T \frac{R_2}{R_2 + 2R_1}$$

$$(2)\quad R_{TH} = \frac{2R_1R_2}{2R_1 + R_2}$$

From equation (1) and (2),

$$(3)\quad R_1 = \frac{V_T R_{TH}}{2V_{OC}}$$

$$(4)\quad R_2 = \frac{V_T R_{TH}}{V_T - V_{OC}}$$

If $V_T = 5V$, $V_{OC} = 1.0V$, and $R_{TH} = 90\Omega = Z_0$, we can derive that $R_1 \sim 220\Omega$, $R_2 \sim 110\Omega$.

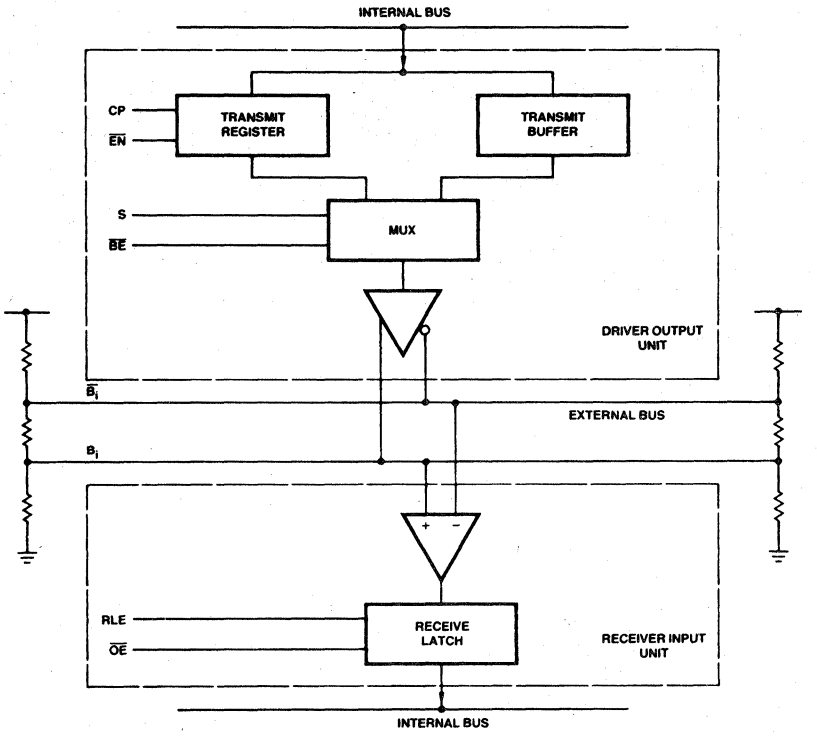
Second order adjustments require attention to unit loading factors (receiver differential input resistance is in parallel with R_2), transmission rates and a host of other factors.

DATA PATH

Figure C shows the data path from one driver to another receiver for one bit of the bus interface.

The transmit register or buffer and receiver latch are configured to provide two modes of operation. The register and latch can provide local storage for output and input data. In the non-storage mode the buffer input to the driver can be selected and the receiver can be wired transparent. Incorporating storage on-chip provides improved speed and lower package count without significant penalty in the non-storage mode.

Figure C. The Data Path for One Bit of the Bus Interface



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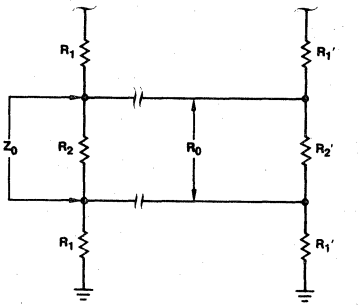
EQUIVALENT CIRCUIT
Recommended Termination



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Operating Temperature Range

Z_0	$R_1 = R_1'$	$R_2 = R_2'$
90Ω	220Ω	110Ω
120Ω	300Ω	150Ω

Minimum line V_O (differential voltage) = 0.5V

Equivalent Termination Versus DC Resistance

Z_0	R_0
88.0Ω	44.0Ω
120.0Ω	60.0Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7.0V
Common Mode Range ..... 0 to V_{CC}
Differential Mode Range (REC) ..... 0 to V_{CC}
Logic Inputs 5.5V
Storage Temperature Range ..... −65 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

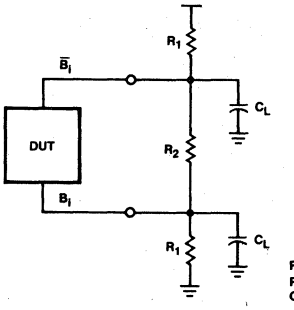
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ	Max	Units
Bus Driver Output							
V_O	Output Differential Voltage (Driver Active) V_{Bi}-$V_{\overline{Bi}}$	$\overline{BE}$ = LOW DI_i = HIGH Test Circuit #1		0.5			Volts
I_{SS}	Output Current	DI_i = HIGH Test Circuit #2 $\overline{BE}$ = LOW	Ia	−22.5	−55	−115	mA
			Ib	+22.5	+55	+115	
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5V		−75	−1	−250	mA
Bus Receiver Input							
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 to V_{CC} V_{OUT} = V_{OL} or V_{OH}		−50	±10	+50	mV
R_{IN}	Input Resistance to GND	$0 \leq V_{CC} \leq V_{CC}$ Max		4	5.7		kΩ
R_{IN}	Differential Input Resistance	$0 \leq V_{CC} \leq V_{CC}$ Max		8	11.4		kΩ
V_{OS}	Center Voltage	Test Circuit #3 Active and Passive		2.0	$V_{CC}/2$	3.0	Volts
$\lvert V_{OS}\rvert - \lvert V_{\overline{OS}}\rvert$	Center Voltage Difference (Active vs Passive)	Test Circuit #3			90	300	mV
Non-Bus Input and Outputs							
V_{OH}	Output HIGH Voltage	ΔV_{IN} = +0.1V	I_{OH} = −15mA	2.4	3.4		Volts
			I_{OH} = −24mA	2.0	3.3		
V_{OL}	Output LOW Voltage	ΔV_{IN} = −0.1V	MIL, I_{OL} = 32mA			0.5	Volts
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All inputs		2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{IN} = 0.4V	Data		−275	−400	μA
			Control		−0.65	−1.0	mA
			Clock		−0.65	−1.0	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.7V			0.1	+50	μA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5V		−75	−150	−250	mA
I_I	Input Leakage Current	V_{IN} = 5.5V				1	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA			−0.75	−1.2	Volts
I_{OZ}	Leakage Current Passive	V_O = 2.4V				+50	μA
		V_O = 0.4V				−50	
I_{CC}	Power Supply Current	$\overline{BE}$, $\overline{OE}$ = HIGH	T_A = 70°C			145	mA
			T_C = 125°C			130	
			−55 to +125°C		110	160	

SWITCHING TEST CIRCUIT

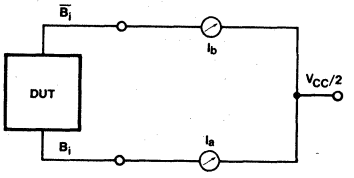
Test Circuit #1



$R_1 = 200\Omega$
$R_2 = 50\Omega$
$C_L = 50pF$

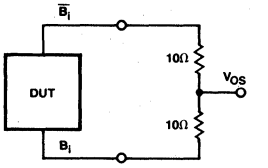
TC000710

Test Circuit #2



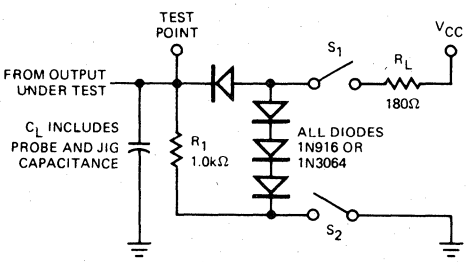
TC000740

Test Circuit #3



TC000730

Test Circuit #4



TC000360

Notes: 1. $C_L = 50pF$ unless otherwise specified.
2. S_1 and S_2 are closed except where shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

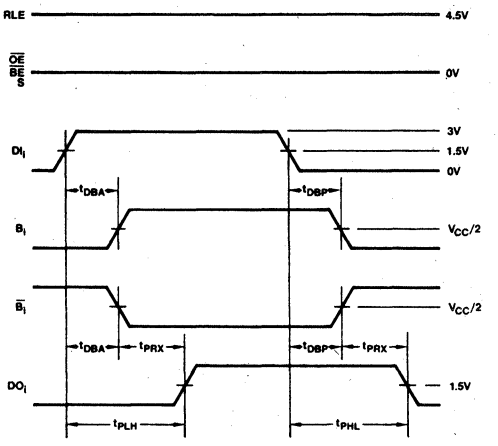
Parameters	Description		Test Conditions	COMMERCIAL C DEVICES $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$ Min	Max	MILITARY M DEVICES $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min	Max	Units
t_{DBA}	DI_i to B_i/ $\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = LOW, Test Circuit #1		12		16	ns
t_{DBP}		Passive			12		18	
t_{CBA}	CP to $B_i/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = HIGH, Test Circuit #1		20		24	ns
t_{CBP}		Passive			20		24	
t_{PA}	$\overline{BE}$ to $B_i/\overline{B}_i$ Propagation Delay	Active	DI_i = HIGH, S = LOW, Test Circuit #1		17		22	ns
t_{PP}		Passive			12		18	
t_S	DI_i to Clock Setup Time		$\overline{BE}$ = LOW	7		7		ns
t_H	DI_i to Clock Hold Time			3		4		
t_S	$\overline{EN}$ to Clock Setup Time			10		10		
t_H	$\overline{EN}$ to Clock Hold Time			0		0		
t_S	$B_i/\overline{B}_i$ to RLE Setup Time			7		7		
t_H	$B_i/\overline{B}_i$ to RLE Hold Time			3		3		
t_{PLZ}/t_{PHZ}	$\overline{OE}$ to DO_i Disable Time		C_L = 50 pF, Test Circuit #4		17		20	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF, Test Circuit #4		10		13	
t_{PZL}	$\overline{OE}$ to DO_i Enable Time		Test Circuit #4		15		17	ns
t_{PZH}					15		17	
t_{PLH}	RLE to DO_i		$\overline{OE}$ = LOW, Test Circuit #4		15		20	ns
t_{PHL}					20		24	
t_{PRX}	$B_i/\overline{B}_i$ to DO_i		RLE = HIGH, $\overline{OE}$ = LOW, Test Circuit #4		21		25	ns
t_{PLH}	$\overline{BE}$ to DO_i Propagation Delay		RLE = HIGH, $\overline{OE}$ = LOW, Test Circuits #1, #4		32		42	ns
t_{PHL}								
t_{PLH}	DI_i to DO_i (Buffer Mode)		S = LOW, RLE = HIGH, $\overline{OE}$ = LOW, Test circuits #1, #4		30		40	ns
t_{PHL}								
t_{PLH}	CP to DO_i (Register Mode)		S = HIGH, RLE = HIGH, $\overline{OE}$ = LOW, Test Circuits #1, #4		35		44	ns
t_{PHL}								
t_{PWL}	Clock Pulse Width	LOW		10		10		ns
t_{PWH}		HIGH		10		10		
t_{PWH}	RLE Pulse Width	HIGH		13		13		ns
t_{SKEW}	Propagation Delay Skew ($t_{PLH} - t_{PHL}$)		V_{CC} = 5 V, C_L = 50 pF, Measurement $V_{CC}/2$, Test Circuit #1		±7		±10	ns

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{DBA}	DI_i to $B_i/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = LOW, Test Circuit #1		7	10	ns
t_{DBP}		Passive			7	10	
t_{CBA}	CP to $B_i/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = HIGH, Test Circuit #1		10.5	16	ns
t_{CBP}		Passive			13	16	
t_{PA}	$\overline{BE}$ to $B_i/\overline{B}_i$ Propagation Delay	Active	DI_i = HIGH, S = LOW, Test Circuit #1		8.5	12	ns
t_{PP}		Passive			4	8	
t_S	DI_i to Clock Setup Time		$\overline{BE}$ = LOW	5	2.5		ns
t_H	DI_i to Clock Hold Time			2	0		
t_S	$\overline{EN}$ to Clock Setup Time			8	4		
t_H	$\overline{EN}$ to Clock Hold Time			0	−4		
t_S	$B_i/\overline{B}_i$ to RLE Setup Time			5	2.5		
t_H	$B_i/\overline{B}_i$ to RLE Hold Time			2	0.7		
t_{PLZ}/t_{PHZ}	$\overline{OE}$ to DO_i Disable Time		C_L = 50 pF, Test Circuit #4			20	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF, Test Circuit #4			13	
t_{PZL}	$\overline{OE}$ to DO_i Enable Time		Test Circuit #4			17	ns
t_{PZH}						17	
t_{PLH}	RLE to DO_i		$\overline{OE}$ = LOW, Test Circuit #4		11	13	ns
t_{PHL}					14	17	
t_{PRX}	$B_i/\overline{B}_i$ to DO_i		RLE = HIGH, $\overline{OE}$ = LOW, Test Circuit #4		12	17	ns
t_{PLH}	$\overline{BE}$ to DO_i Propagation Delay		RLE = HIGH, $\overline{OE}$ = LOW, Test Circuits #1, #4		15	25	ns
t_{PHL}							
t_{PLH}	DI_i to DO_i (Buffer Mode)		S = LOW, RLE = HIGH, $\overline{OE}$ = LOW, Test Circuit #1, #4		18	25	ns
t_{PHL}							
t_{PLH}	CP to DO_i (Register Mode)		S = HIGH, RLE = HIGH, $\overline{OE}$ = LOW, Test Circuits #1, #4		22	28	ns
t_{PHL}							
t_{PWL}	Clock Pulse Width	LOW		10	3		ns
t_{PWH}		HIGH		10	5		
t_{PWH}	RLE Pulse Width	HIGH		10	6		ns
t_{SKEW}	Propagation Delay Skew (t_{PLH}–t_{PHL})		V_{CC} = 5V, C_L = 50 pF, Measurement $V_{CC}/2$, Test Circuit #1		±1	±5	ns

SWITCHING WAVEFORMS

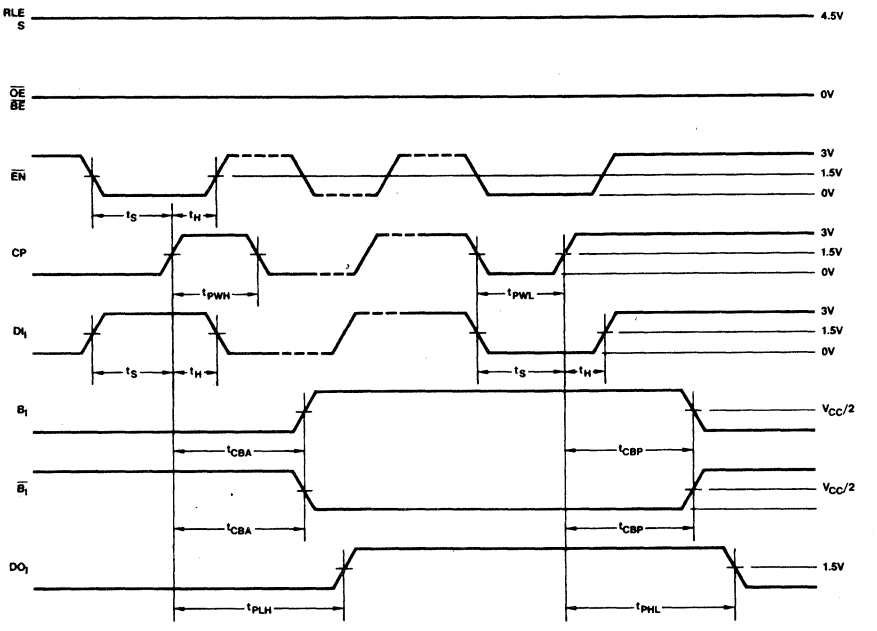
(1) DI_i to B_i,$\overline{B}_i$, DO_i (Buffer Mode)



WF002090

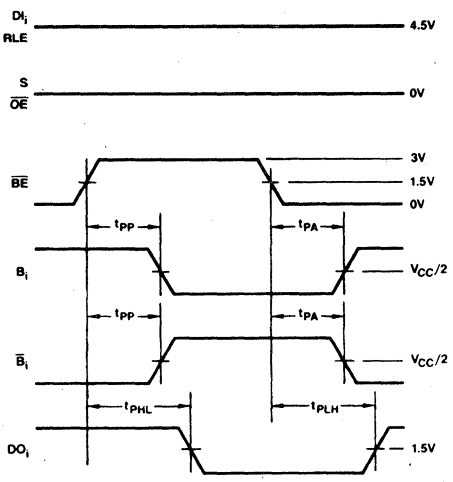
SWITCHING WAVEFORMS (Cont.)

(2) CP to B_i,$\overline{B}_i$, DO_i (Register Mode)



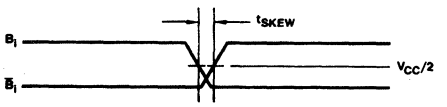
WF002100

(3) $\overline{BE}$ to B_i,$\overline{B}_i$, DO_i (Passive and Active)



WF002060

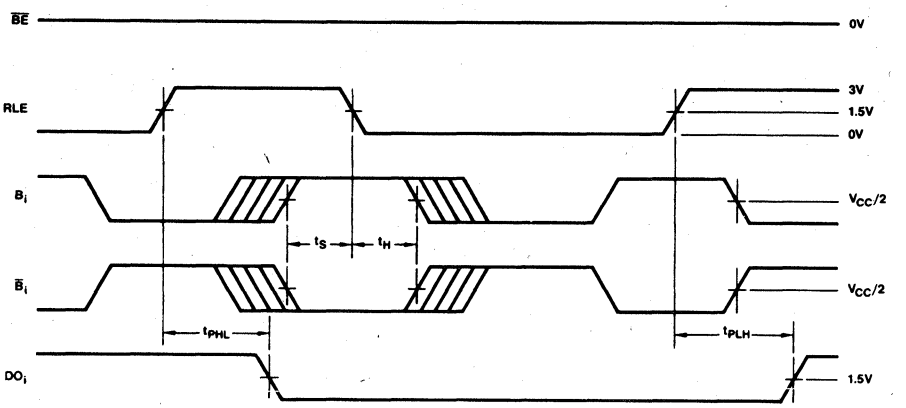
(4) Output to Output



WF002250

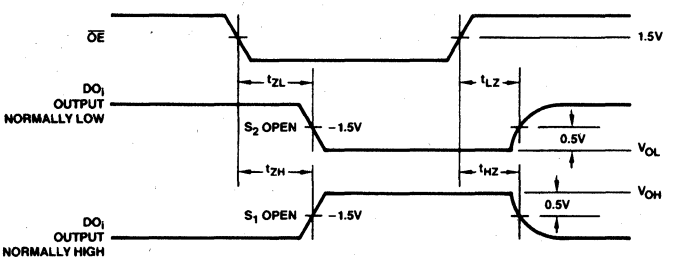
SWITCHING WAVEFORMS (Cont.)

(5) RLE to DO_i



WF002070

(6) $\overline{OE}$ to DO_i



WF002080

MOS Microprocessor Support Products

Am7960

Coded Data Transceiver

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Manchester encoder-decoder transceiver
- Matched filter receiver
- Frequency agile for data rates between 500Kbps and 3Mbps
- 32dB dynamic range (transmit to receive)
- "Modem-like" controller interface
- Transmit edge rate control
- High impedance interface to coupling transformer
- 2V differential output to 37.5Ω

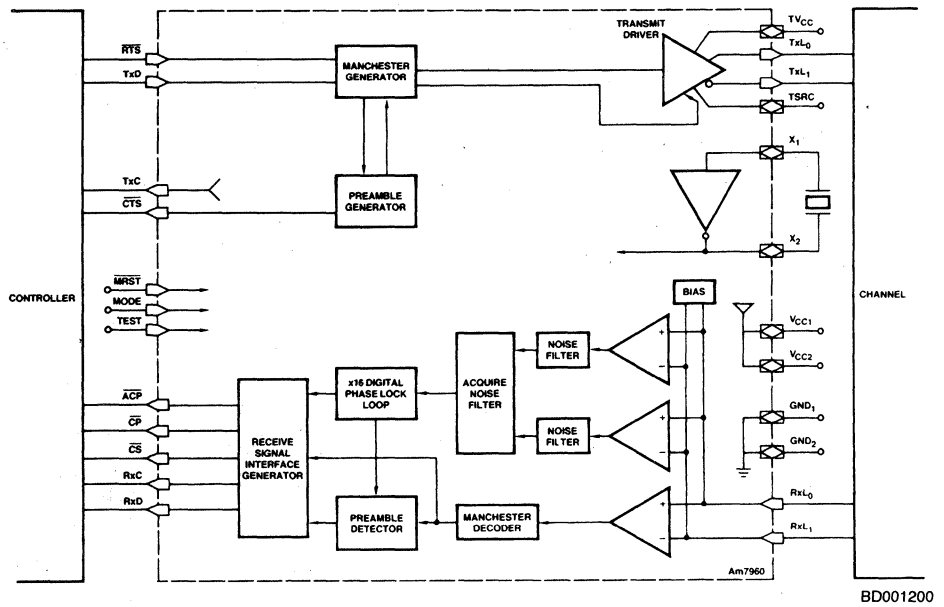
GENERAL DESCRIPTION

The Am7960 is a combination of a Manchester encoder/decoder and a transceiver. It is designed for use in synchronous communications systems which require common mode isolation in point-to-point or common bus architecture. It is frequency agile over the range of 0.5Mbps to 3Mbps. This 5V device provides 32dB of dynamic range, and guarantees 2V output into 37.5Ω. A single external component controls the slew rate of the transmitter, and a matched filter in the receiver minimizes false starts improving reliability.

The Am7960 has a modem-like controller interface which makes it compatible with nearly every existing synchronous communications controller (USARTs, SCCs, etc).

BLOCK DIAGRAM

Am7960



BD001200

RELATED PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller Par Ethernet
Am7991A	Serial Interface Adapter

04533A

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Controller Transmit Interface Signals			
	TxC	O	Transmit Clock. Transmit Clock is data transmit bit clock. All transmit interface signals are synchronized to this clock. This signal is always active.
	TxD	I	Transmit Data. Transmit Data is the serial transmit data.
	$\overline{RTS}$	I	Request to Send. The communication controller indicates that it wishes to transmit data by asserting Request to Send. Once started, only negating Request to Send can stop transmission.
	$\overline{CTS}$	O	Clear to Send. The Am7960 asserts Clear to Send when it can encode and transmit data on the channel.
Controller Receive Interface Signals			
	RxC	O	Receive Clock. Receive Clock is the data receive bit clock. All controller receive interface signals with the exception of Advance Carrier Presence are synchronized to this clock. When there is no carrier on the line, this signal is OFF.
	RxD	O	Receive Data. Receive Data is the serial receive data.
	$\overline{ACP}$	O	Advance Carrier Presence. Advance Carrier Presence is asserted whenever the receiver has detected line activity. It is negated after there has been no line activity for 2 bit times (quiet line). During transmission Advance Carrier Presence is internally negated. This signal is asynchronous with both Transmit Clock and Receive Clock.
	$\overline{CP}$	O	Carrier Presence. Carrier Presence is asserted after internal clock acquisition and immediately before asserting Receive Clock. It is negated after either end of message or quiet line.
	CS	O	Carrier Sense. Carrier Sense is asserted immediately before the first receive data bit and negated after either a Manchester coding violation or quiet line.
Channel Interface Signals			
	TxL_0 TxL_1	O	Transmit Outputs. The difference between these outputs (TxL_0 – TxL_1) is the channel transmit signal. There are provisions for controlling both the transmit slew rate and the short circuit current.
	TV_{CC}	I	Transmit Power Supply. The transmitter has a separate power supply input.
	TSRC	I/O	Slew Rate Control. This pin is used to control the transmit slew rate with external passive components.
	RxL_0 RxL_1	I	Receiver Inputs. The difference between these inputs (RxL_0 – RxL_1) is the channel receive signal.
Global Signals			
	$\overline{MRST}$	I	Master Reset. Master Reset is an asynchronous transceiver reset. When asserted, all interface signals will be inhibited with the exception of Transmit Clock. It has an internal pullup resistor, internal discharge clamp diode, and input hysteresis to provide power-on reset with a single external capacitor to ground.
	MODE	I	Mode Control. Mode Control determines if the Am7960 will internally generate and recognize line preamble. When LOW, the Mode Control is in Mode 0 and uses preamble. When HIGH, the Mode Control is in Mode 1 and is preamble transparent. This input has an internal pullup resistor.
	TEST	I	Test Control. Test Control is not a user function. This input is used to functionally test the device. It should always be LOW when active.
	X_1 X_2	I	Crystal Oscillator Connections. X_1 and X_2 are the Crystal Oscillator Connections. The Am7960 can be either operated from a crystal or driven from an external TTL clock.
	V_{CC1} V_{CC2}	I	Power Supply. V_{CC1} and V_{CC2} are 5.0 volt nominal power supply pins.
	GND_1 GND_2		Ground Pins.

DETAILED DESCRIPTION

The Am7960 has two operating modes: Mode 0 and Mode 1. When transmitting, Mode 0 inserts a 32-bit preamble, Manchester encodes the transmit data, and appends End Of Message. When receiving, Mode 0 identifies and removes preamble, decodes the Manchester line data, and removes End Of Message. Mode 1 is identical to Mode 0 except preamble is neither generated on transmit nor detected upon reception; the Coded Data Transceiver simply passes data (bit for bit) onto the media and recovers it at the destination. One of these two modes will interface to almost all existing synchronous controllers.

Manchester encoding is employed in the Am7960. A 1 bit is encoded as a 0 followed by a 1; a 0 bit is a 1 followed by a 0. Line end of message is two consecutive bits of 1s. In Mode 0, the preamble will be a Manchester 1 followed by 30 bits of alternating Manchester 0 and 1 bits followed by a final 1.

TRANSMIT

The Am7960 has a modem-like controller interface. Transmission is initiated by asserting Request To Send. Once started, only negating Request To Send can stop transmission. All receive signals are active with the exception of Advance Carrier Presence which will be off for the duration of the transmission. In either mode, Clear-To-Send is activated one transmit clock cycle before the Am7960 expects transmit data.

RECEIVE

The Receiver has three status lines: Advance Carrier Presence, Carrier Presence, and Carrier Sense. Advance Carrier Presence indicates that the receiver is detecting line activity. It is asynchronous with both Transmit Clock and Receive Clock. Advance Carrier Presence is asserted for line signals above the Positive Presence Level or below the Negative Presence Level for more than 40ns. Line signals between the presence levels or less than 16ns will be rejected. Once asserted, Advance Carrier Presence will remain active until line signal is absent for 2 bit times (quiet line).

After the Am7960 has detected an active line, it attempts to acquire Receive Clock. Clock qualification is achieved by sampling the presence levels. To qualify, a line signal must either be above the Positive Presence Level and then go below the Negative Presence Level or below the Negative Presence Level and then go above the Positive Presence Level in $\frac{3}{4}$ to $1\frac{1}{4}$ bit times. After this occurs, the next line data transition starts the internal clock recovery circuitry. If line becomes quiet or End Of Message detected, the clock will not

be reacquired until Advance Carrier Presence is OFF and then reasserted.

Active Carrier Presence indicates that the Am7960 has an internally acquired clock. Receive Clock will be active whenever Carrier Presence is active. Carrier Presence will remain active until either the line is quiet or End Of Message is detected.

Carrier Sense becomes active when the Am7960 intends to transmit Receive Data to the controller. Carrier Sense stays active until either the line is quiet or an invalid Manchester cell is detected. Receive Data is OFF until Carrier Sense becomes active and remains active until Carrier Presence becomes inactive.

The Am7960 decodes the line data by sampling the 1/4 and 3/4 bit intervals with respect to the start of the cell. If these samples are opposite, valid Manchester data has been decoded. If these samples are the same and the next 1/4 sample is the same, the receiver has detected End Of Message.

In Mode 0, valid preamble is defined as at least seven receive clocks, the last four as decoded Manchester 1 0 1 1. Until this criteria is met, the Am7960 will continue to hunt for preamble.

CHANNEL

The transmitter/receiver interface has been designed to provide a high impedance, low capacitance channel interface. There are provisions to externally control the transmit short circuit current as well as the slew rate of the transmit signals. Slew limiting the transmit signal decreases both the effect of channel intersymbol interference and the presence of undesired harmonic frequencies.

The receiver provides a high impedance input over the total input operating range. A common mode voltage reference minimizes the number of external components needed for use with coupling or isolation transformers. The receiver's high input sensitivity and large dynamic range allows reception of both large (near end) and small (far end) signals. Its range also allows for operation immediately adjacent to an active transmitter without overload damage.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature Under Bias ..... −55°C to +125°C
Supply Voltage Above Ground Potential .... −0.5V to +7.0V
Transmit Supply Current (Max) 250mA
Receiver Common Mode Voltage ..... −0.5V to +5.5V
Receiver Differential Input Voltage 4.5V
DC Output Current, Into Outputs (Logic Outputs) 30mA
DC Input Voltage (Logic Inputs) ..... −0.5V to +5.5V
DC Input Current (Logic Inputs) ..... −30mA to +5.0mA
Power Dissipation 1.0W
Lead Soldering Temperature (10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Name	Description		Test Conditions	Min	Typ	Max	Units
Controller Interface Signals							
V_{OH}	Output HIGH Voltage	Note 1	I_{OH} = −1mA	2.4			V
V_{OL}	Output LOW Voltage	Note 1	I_{OL} = =8mA			0.5	V
V_{OH}	Output MOS HIGH Voltage	Note 2	I_{OH} = −.4mA	3.9			V
V_{OL}	Output MOS LOW Voltage	Note 2	I_{OL} = 8mA			0.45	V
V_{IH}	Input HIGH Voltage	Notes 3, 4		2.0			V
V_{IL}	Input LOW Voltage	Notes 3, 4				0.8	V
V_{RIH}	Reset Input HIGH Voltage	Note 5	V_{CC} = Max		$V_{CC}/2$		V
V_{RIL}	Reset Input LOW Voltage	Note 5				0.8	V
V_{RH}	Reset Input Hysteresis	Note 5	V_{CC} = Min	0.20			V
V_I	Input Clamp Voltage	Notes 3, 4 and 5	I_{IN} = −18mA			−1.2	V
I_{IL}	Input LOW Current	Notes 3, 4	V_{IN} = 0.5V			−500	
		Note 5				−1000	
I_{IH}	Input HIGH Current	Notes 3, 4	V_{IN} = 2.4V			50	μA
		Note 5				50	
I_I	Input HIGH Current	Notes 3, 4 and 5	V_{CC} = Min, V_{IN} = 5.5V			1.0	mA
I_{SC}	Short Circuit Current	Notes 1, 6	V_{CC} = Max	−40		−120	mA
R_{RST}	Reset Resistor to V_{CC}	Note 5			20		kΩ
Transmit Channel Interface Signals							
V_T	Differential Transmit Output Voltage	Note 7	R_L = 37.5Ω	−2.0	−2.7	−3.5	V
V_T				2.0	2.7	3.5	
V_{OS}	Common Mode Transmit Output Voltage	Note 8	R_L = 37.5Ω	1.0		3.0	V
V_{OS}							
V_{TO}	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$ Difference in Differential Output Voltage	Note 7	R_L = 37.5Ω	−75		75	mV
V_{OSO}	$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$ Difference in Common Mode Output Voltage	Note 8	R_L = 37.5Ω	−75		75	mV
I_{TO}	$\lvert I_T \rvert - \lvert \overline{I_T} \rvert$ Difference in Output Currents	Note 9	R_L = 37.5Ω	−2		2	mA
I_{OSC}	Transmit Output Short Circuit Current		V_{CC} = Max			−250	mA
I_{OX}	Off State Leakage Currents		V_{CC} = Max V_{OX} = $V_{CC/2}$	−100		100	μA
C_T	Differential Transmit Input Capacitance		Transmit OFF			7	pF

Name	Description		Test Conditions	Min	Typ	Max	Units
Receive Channel Interface Signals							
V_{IN}	Differential Receiver Input Voltage	Note 10		V_TMax V_TMax			V
V_{TH}	Differential Receiver Offset Voltage	Note 11		−5		5	mV
V_{CM}	Common Mode Receiver Input Voltage	Note 12		1.0		3.0	V
V_{CPP}	Positive Static Carrier Presence Level	Note 10		20		35	mV
V_{CPN}	Negative Static Carrier Presence Level	Note 10		−20		−35	mV
R_R	Differential Receiver Input Resistance		$V_T < V_{IN} < V_T$ $0 < V_{CC} < Max$	20			kΩ
C_R	Differential Receiver Input Capacitance		$V_T < V_{IN} < V_T$			3	pF
Global Signals							
R_N	Differential Node Resistance	Note 13	$V_T < V_{IN} < V_T$ $0 < V_{CC} < Max$	20	30		kΩ
C_N	Differential Node Capacitance	Note 13	$V_T < V_{IN} < V_T$ $0 < V_{CC} < Max$			10	pF
I_{CC}	Power Supply Current		V_{CC} = Max			190	mA

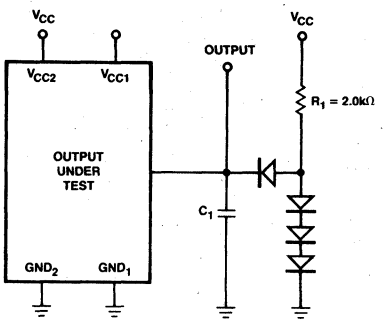
Notes:
1. Output signals $\overline{ACP}$, $\overline{CP}$, $\overline{CS}$ and $\overline{CTS}$.
2. Output signals TxC, RxC and RxD.
3. Inputs TxD and $\overline{RTS}$.
4. Inputs $\overline{TEST}$ and MODE.
5. Input $\overline{MRST}$ only.
6. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
7. V_T and $V_{\overline{T}}$ are the differential output signals TxL_0–TxL_1 depending upon signal polarity.
8. V_{OS} and $V_{\overline{OS}}$ are the average of TxL_0 and TxL_1 depending upon signal polarity.
9. I_T and $I_{\overline{T}}$ are the transmit output currents.
10. V_{IN} is the differential input signal RxL_0–RxL_1.
11. Offsets are for differential input signals (Figure 1).
12. V_{CM} is the average RxL_0 and RxL_1.
13. Node impedance is with transmitter and receiver connected.

04533A

Refer to Page 13-1 for Essential Information on Military Devices

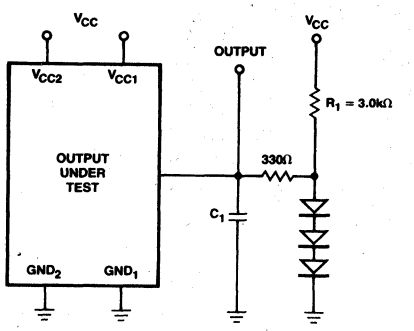
SWITCHING TEST CIRCUITS AND SWITCHING TEST WAVEFORMS

TEST CIRCUIT A. TTL OUTPUTS



TC000780

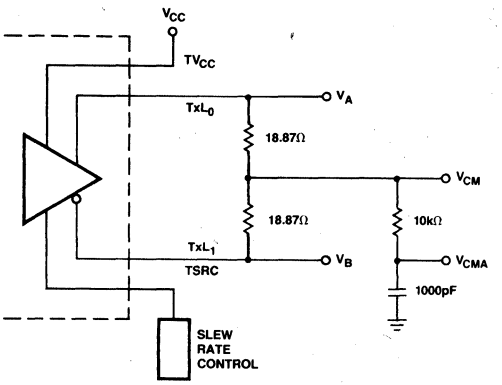
TEST CIRCUIT B. MOS OUTPUTS



TC000770

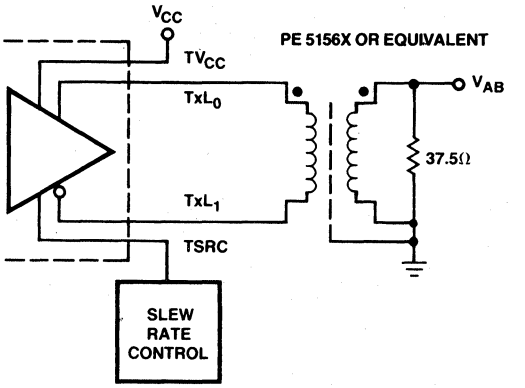
Note: C_1 includes test fixture capacitance.

TEST CIRCUIT C. TRANSMITTER OUTPUT



TC000760

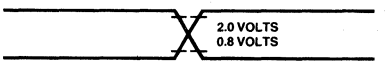
TEST CIRCUIT D. TRANSMITTER ASYMMETRY



TC000750

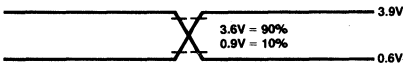
SWITCHING TEST WAVEFORMS

TEST CIRCUIT A. TTL OUTPUTS



WF002140

TEST CIRCUIT B. MOS OUTPUTS



WF002180

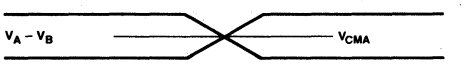
TEST CIRCUIT D. TRANSMITTER ASYMMETRY

WF002220

TEST CIRCUIT C. TRANSMITTER OUTPUT Rise and Fall Times

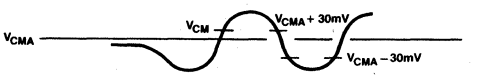
WF002150

Transmit Latency



WF002160

Common Mode Pulse Width



WF002170

04533A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Number	Description		Test Conditions	Min	Typ	Max	Units
Transmit Clock							
1	Transmit Clock Period	Note 2		330			ns
2	Transmit Clock Width LOW	Note 2		45%		55%	TxC
3	Transmit Clock Width HIGH	Note 2		45%		55%	TxC
4	Transmit Clock Rise Time	Note 2	C_L = 50pF			5	ns
5	Transmit Clock Fall Time	Note 2	C_L = 50pF			5	ns
Transmit Control							
6	Setup $\overline{RTS}$ to ↑ TxC	Notes 1 and 2		15			ns
7	Hold $\overline{RTS}$ to ↑ TxC	Notes 1 and 2		5			ns
8	Minimum Inter-Packet Delay				3		TxC
9	↑ TxC to $\overline{ACP}$ Inhibit	Notes 1 and 2		0.3		0.5	TxC
10	↑ TxC to $\overline{ACP}$ Enable	Notes 1 and 2		2.3			TxC
11	↑ TxC to $\overline{CTS}$ Enable	Notes 1 and 2				.35	TxC
12	↑ TxC to $\overline{CTS}$ Disable	Notes 1 and 2				.35	TxC
13	Setup TxD to ↑ TxC	Notes 1 and 2		15			ns
14	Hold TxD to ↑ TxC	Notes 1 and 2		5			ns
Transmit Latency							
15	↑ TxC to Encoded Data Line Clock Transition	Notes 3 and 4		0.75		1.0	TxC
16	↑ TxC to Transmitter Disable	Notes 3 and 5		2.25			TxC
Receive Clock and Data							
17	Receive Clock Period	Note 2		92%		108%	TxC
18	Receive Clock Width LOW	Note 2		42%		58%	TxC
19	Receive Clock Width HIGH	Note 2		42%		58%	TxC
20	Receive Clock Rise Time	Note 2	C_L = 50pF			5	ns
21	Receive Clock Fall Time	Note 2	C_L = 50pF			5	ns
22	↑ RxC to Valid RxD	Note 2		−5		20	ns
23	Receive Data Rise Time	Note 2	C_L = 50pF			10	ns
24	Receive Data Fall Time	Note 2	C_L = 50pF			10	ns
Receive Control							
25	Line Active to $\overline{ACP}$ Active	Notes 1 and 6		0.15		0.4	TxC
26	Line Quiet to $\overline{ACP}$ Inactive	Notes 1 and 7		2.15		2.4	TxC
27	$\overline{ACP}$ Width LOW	Note 1		0.1			TxC
28	$\overline{ACP}$ Width HIGH	Note 1		0.1			TxC
29	$\overline{ACP}$ Active to $\overline{CP}$ Active	Notes 1 and 9		1.5			TxC
30	$\overline{CP}$ Inactive to $\overline{ACP}$ Inactive	Note 1		0			ns
31	1st Line Data Transition to ↑ RxC	Notes 2 and 8		3.5			TxC
		Notes 2 and 9		1.0			
32	$\overline{CP}$ Active to ↑ RxC	Notes 1 and 2		60			ns
33	↓ RxC to Inactive $\overline{CP}$	Notes 1 and 2		0		0.1	TxC
34	$\overline{CS}$ Active to ↑ RxC	Notes 1, 2 and 8		60			ns
35	↓ RxC to $\overline{CS}$ Active	Notes 1, 2 and 9		0		0.1	TxC
36	↓ RxC to $\overline{CS}$ Inactive	Notes 1 and 2		0		0.1	TxC
37	$\overline{CP}$ Active to $\overline{CS}$ Active	Notes 1 and 9		7			RxC
Channel Transmit Signals							
38	Transmit Slew Rate Coefficient				TBD		
39	Transmit Rise Time	Notes 3 and 10		24%	30%	36%	TxC
40	Transmit Fall Time	Notes 3 and 10		24%	30%	36%	TxC
41	Transmit Common Mode Pulse Width	Notes 3 and 11			15	40	ns
42	Bit Cell Edge to Bit Cell Center	Note 12		48%		52%	TxC
43	Bit Cell Center to Bit Cell Center	Note 12		98%		102%	TxC
44	Bit Cell Center to Bit Cell Edge	Note 12		48%		52%	TxC
45	Transmit Waveform	Note 13		Monotonic			

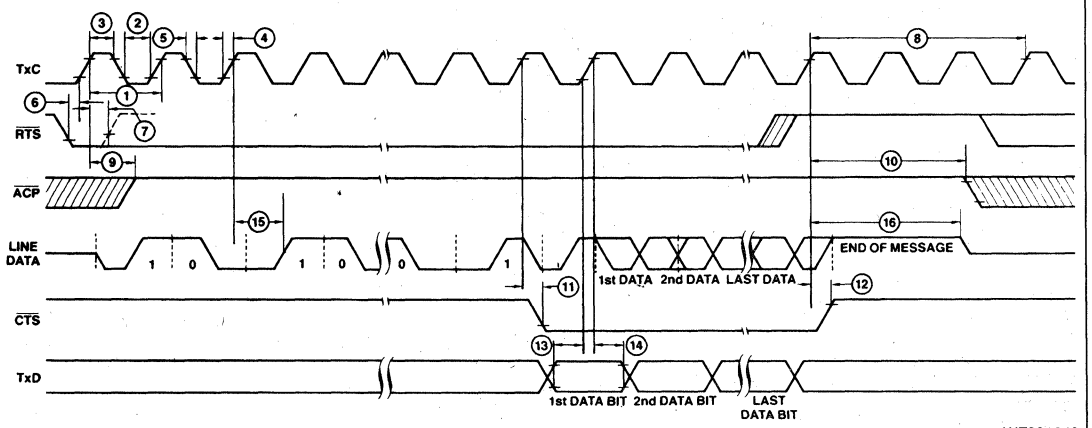
04533A

Refer to Page 13-1 for Essential Information on Military Devices

Number	Description		Test Conditions	Min	Typ	Max	Units
Channel Receive Signals							
46	Receiver Input Slew Rate			.2		TBD	V/TxC
47	Receiver Filtered Positive Line Pulse Width	Note 14				16	ns
48	Receiver Positive Line Active Pulse Width	Note 14		40			ns
49	Receiver Filter Negative Line Pulse Width	Note 14				16	ns
50	Receiver Negative Line Active Pulse Width	Note 14		40			ns
51	Receiver Timing Displacement Jitter Error	Note 15		−7		7	%TxC
52	Receiver Noise Jitter Error	Note 15		−5.5		5.5	%TxC
53	Receiver Total Jitter Error	Note 15		−12.5		12.5	%TxC
Global Signals							
54	Xtal Frequency					50	MHz
55	Transmit Frequency Tolerance			−0.1		0.1	%
56	Master Reset Pulse Width				TBD		μs
57	Initial Power-On Until Operation				TBD		μs

Notes:
1. TTL levels. (Test Circuit A).
2. MOS levels. (Test Circuit B).
3. Transmit slew rate set nominally at 30% TxC at 1MHz.
4. Measurements mode with TEST CIRCUIT C at $V_A - V_B = V_{CMA} \pm 5mV$.
5. Differential output starts to approach 0 volts.
6. Line active from differential receive signal has to meet minimum active width timing.
7. Line inactive is from the last differential signal to meet the minimum active width timing.
8. For Mode 1 only.
9. For Mode 0 only.
10. Transmit signals measured with TEST CIRCUIT C at $V_A - V_B = 10\%$ and 90%.
11. Transmit common mode pulse is measured with TEST CIRCUIT C at $V_{CM} - V_{CMA}$ above 30mV ±5mV or below −30mV ±5mV
12. Transmit Skew is measured with TEST CIRCUIT D at ±5mV.
13. Transmitter shall be monotonic for both rise and fall.
14. Differential receive signals less than the maximum filtered pulse width are guaranteed to be rejected by the receiver. Differential receive signal greater than the minimum active pulse width are guaranteed to turn on the receiver.
15. The Am7960 receiver jitter is defined as the percentage edge displacement from the ideal transmit signal at the transceiver data bit frequency over the period of the transceiver data bit frequency (Figure 2).The jitter has been divided into two areas: characteristic and random. Characteristic jitter is edge displacement due to asymmetry and intersymbol interference. Random jitter is gaussion edge displacement of mean 0 and sigma at 1/3 the maximum random deviation.

TRANSMIT MODE 0

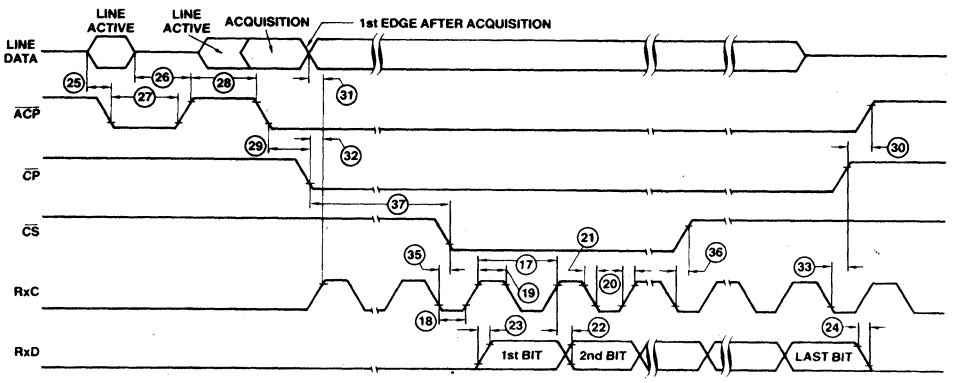


WF001640

04533A

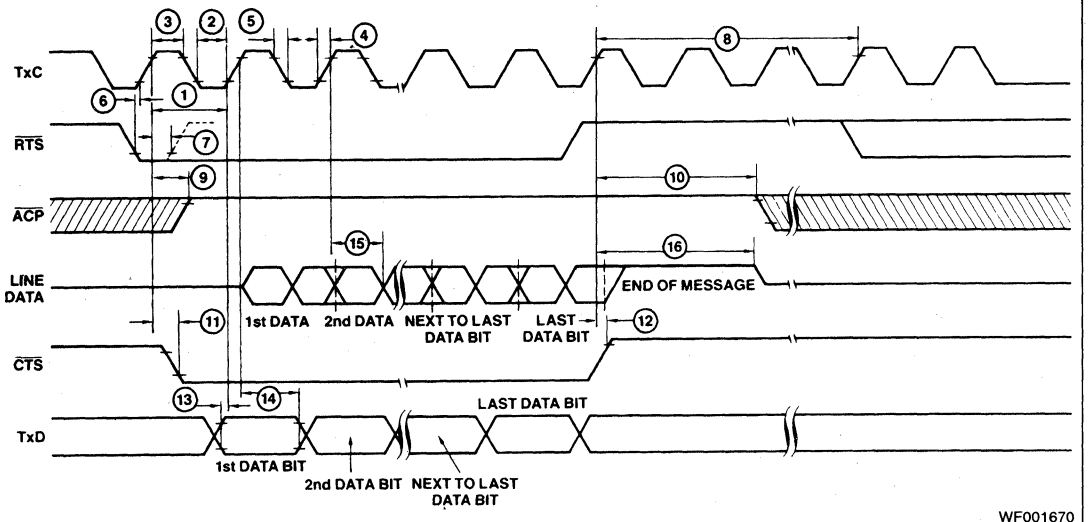
Refer to Page 13-1 for Essential Information on Military Devices

RECEIVE MODE 0



WF001650

TRANSMIT MODE 1

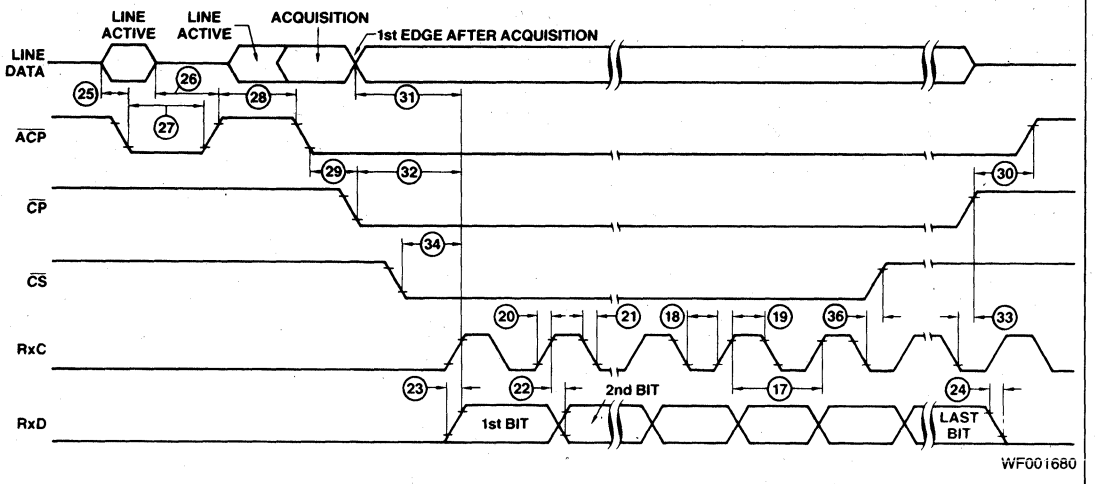


WF001670

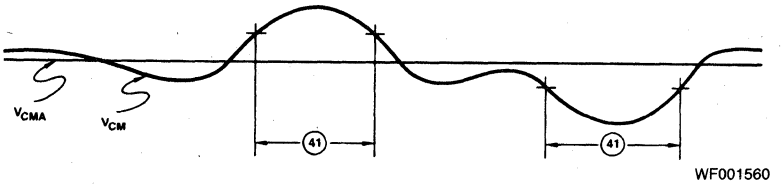
04533A

Refer to Page 13-1 for Essential Information on Military Devices

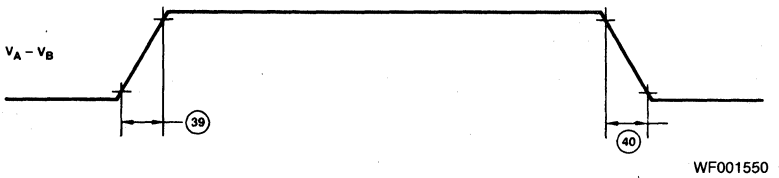
RECEIVE MODE 1



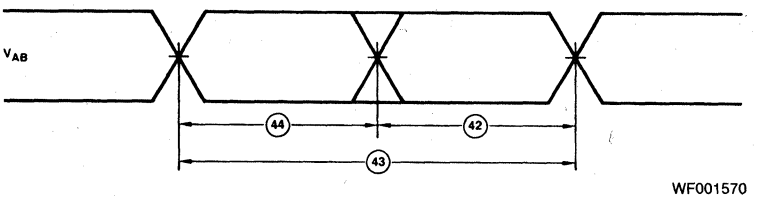
Common Mode Pulse Width



Transmit Rise/Fall Time



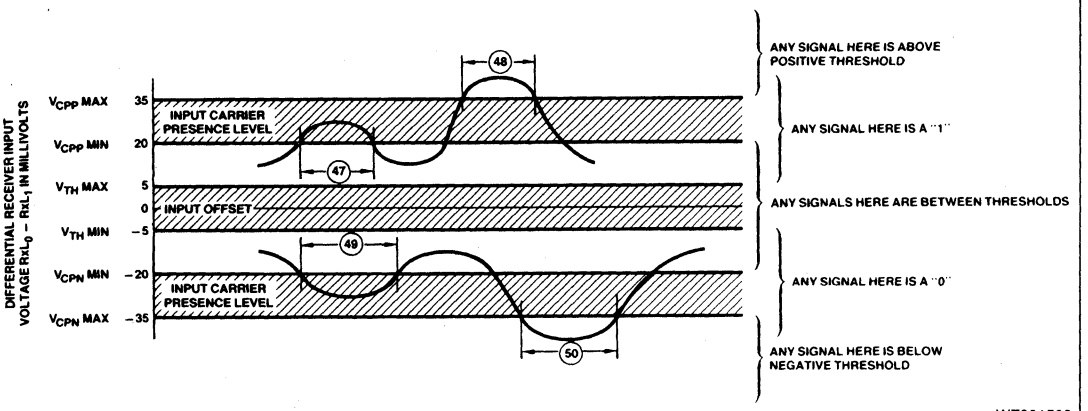
Transmit Latency



04533A

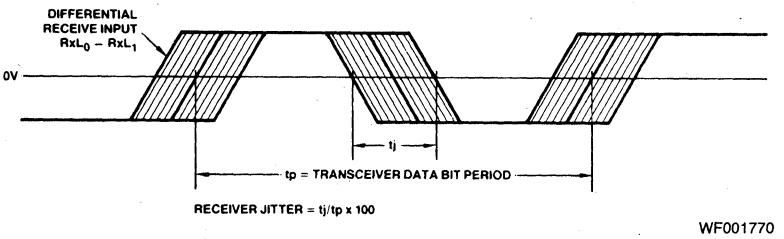
Refer to Page 13-1 for Essential Information on Military Devices

FIGURE 1. Receiver Thresholds



WF001580

Figure 2. Receiver Jitter



WF001770

Am7990*

Local Area Network Controller for Ethernet (LANCE)

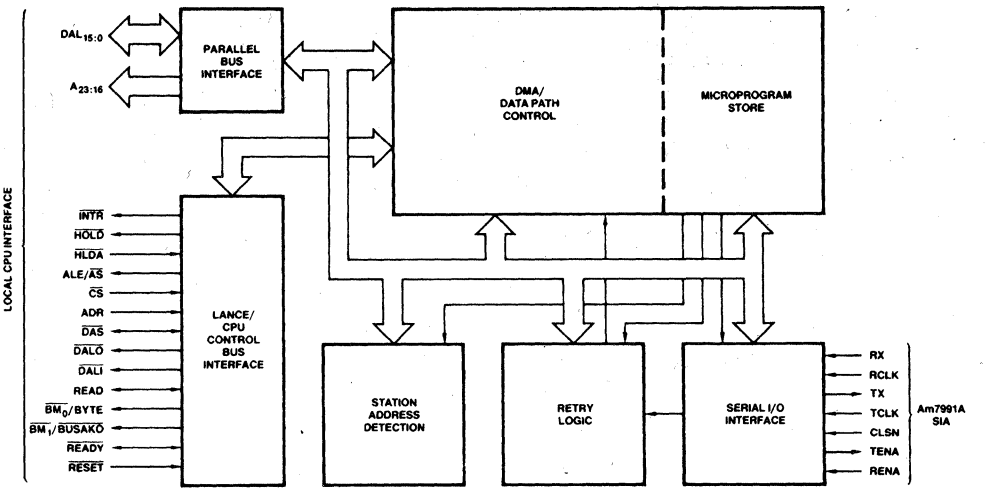
DISTINCTIVE CHARACTERISTICS

- Ethernet and IEEE 802.3 compatible
- Easily interfaced to 8086, 68000, Z8000, LSI-11 microprocessors
- On-board DMA and buffer management, 48 byte FIFO
- 24-bit wide linear addressing (Bus Master Mode)
- Network and packet error reporting
- Diagnostic Routines
  - Internal/external loop back
  - CRC logic check
  - Time domain reflectometer

GENERAL DESCRIPTION

The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48-pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an Ethernet Local Area Network. This chip, in conjunction with the Am7991A Serial Interface Adapter (SIA) and closely coupled local memory and microprocessor, is intended to provide the user with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N-Channel MOS technology and is compatible with a variety of microprocessors. On-board DMA, advanced buffer management and extensive error reporting and diagnostics facilitate design and improve system performance.

BLOCK DIAGRAM



BD002061

RELATED PRODUCTS

Part No.	Description
7960	Coded Data Transceiver
7991A	Serial Interface Adapter
7995	Ethernet Transceiver

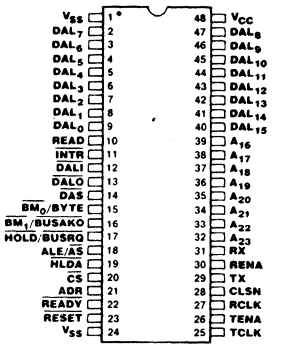
*December 1983 – See Valid Combinations Note Under Ordering Information

05698A

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

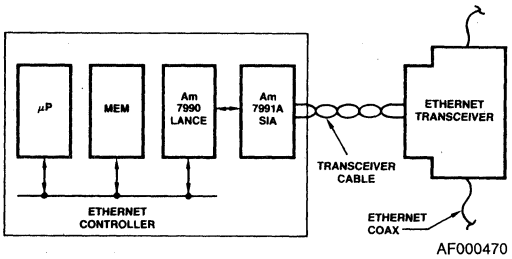
D-48-1



CD001450

Note: Pin 1 is marked for orientation

TYPICAL ETHERNET NODE



AF000470

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am7990 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 48-pin CERDIP (D–48–1)
- **Am7990** — Device type
  - LANCE

Valid Combinations	
Am7990	DC, DCB, DMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

11

PIN DESCRIPTION

DAL_{00} – DAL_{15} **Data/Address Lines (Input/Output 3-State)**
The time multiplexed Address/Data bus. During the address portion of a memory transfer, DAL_{00} – DAL_{15} contains the lower 16 bits of the memory address. The upper 8 bits of address are contained in A_{16} – A_{23}.

During the data portion of a memory transfer, DAL_{00} – DAL_{15} contains the read or write data, depending on the type of transfer.

The LANCE drives these lines as a Bus Master and as a Bus Slave.

A_{16} – A_{23} **High Order Address Bus (Output 3-State)**
The additional address bits necessary to extend the DAL lines to access a 24-bit address. These lines are driven as a Bus Master only.

READ **(Input/Output 3-State)**
Indicates the type of operation to be performed in the current bus cycle. This signal is an output when the LANCE is a Bus Master.

High – Data is taken off the DAL by the chip.

Low – Data is placed on the DAL by the chip.

The signal is an input when the LANCE is a Bus Slave.

High – Data is placed on the DAL by the chip.

Low – Data is taken off the DAL by the chip.

$\overline{BM_0}$/ BYTE $\overline{BM_1}$/ $\overline{BUSAKO}$
I/O pins 15 and 16 are programmable through bit (00) of CSR_3.

$\overline{BM_0}$, $\overline{BM_1}$

If CSR_3 (00) BCON = 0
I/O Pin 15 = $\overline{BM_0}$ (Output 3-state)
I/O PIN 16 = $\overline{BM_1}$ (Output 3-state)

$\overline{BM_0}$, $\overline{BM_1}$ (Byte Mask). This indicates the byte(s) on the DAL are to be read or written during this bus transaction. The LANCE drives these lines only as a Bus Master. It ignores the Byte Mask lines when it is a Bus Slave and assumes word transfers.

Byte selection using Byte Mask is done as described by the following table.

$\overline{BM_1}$	$\overline{BM_0}$	
LOW	LOW	Whole Word
LOW	HIGH	Upper Byte
HIGH	LOW	Lower Byte
HIGH	HIGH	None

BYTE, $\overline{BUSAKO}$

If CSR_3 (00) BCON = 1
I/O PIN 15 = BYTE (Output 3-state)
I/O PIN 16 = $\overline{BUSAKO}$ (Output)

Byte selection may also be done using the BYTE line and DAL_{00} line, latched during the address portion of the bus cycle. The LANCE drives BYTE only as a Bus Master and ignores it when a Bus Slave selection is done (similar to $\overline{BM_0}$, $\overline{BM_1}$).
Byte selection is done as outlined in the following table.

BYTE	DAL_{00}	
LOW	LOW	Whole Word
LOW	HIGH	Illegal Condition
HIGH	LOW	Lower Byte
HIGH	HIGH	Upper Byte

$\overline{BUSAKO}$ is a bus request daisy chain output. If the chip is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If the LANCE is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.

Byte Swapping

In an effort to be compatible with the variety of 16-bit microprocessors available to the designer, the LANCE may be programmed to swap the position of the upper and lower order bytes on data involved in transfers with the internal FIFO.

Byte swapping is done when BSWP = 1. The most significant byte of the word in this case will appear on DAL lines 7-0 and the least significant byte on DAL lines 15-8.

When BYTE = H (indicating a byte transfer) the table indicates on which part of the 16-bit data bus the actual data will appear.

Whenever byte swap is activated, the only data that is swapped is data traveling to and from the FIFO.

Signal Line	Mode Bits	
	BSWP = 0 and BCON = 1	**BSWP = 1 and BCON = 1**
BYTE = L and DAL_{00} = L	Word	Word
BYTE = L and DAL_{00} = H	Illegal	Illegal
BYTE = H and DAL_{00} = H	Upper Byte	Lower Byte
BYTE = H and DAL_{00} = L	Lower Byte	Upper Byte

$\overline{CS}$ **Chip Select (Input)**
Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle. $\overline{CS}$ must not be asserted when $\overline{HLDA}$ is LOW.

ADR — **Register Address Port Select (Input)**
When LANCE is slave, ADR indicates which of the two register ports is selected. ADR LOW selects register data port; ADR HIGH selects register address port, ADR must be valid throughout the data portion of the bus cycle and is only used by the LANCE when CS is low.

ALE/$\overline{AS}$ — **Address Latch Enable (Output 3-State)**
Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR_3.

As ALE (CSR_3 (01), ACON = 0), the signal transitions from a HIGH to a LOW during the address portion of the transfer and remains low during the data portion. ALE can be used by a Slave device to control a latch on the bus address lines. When ALE is high the latch is open and when ALE goes low the latch is closed.

As $\overline{AS}$ (CSR_3 (01), ACON = 1), the signal pulses LOW during the address portion of the bus transaction. The low to high transition of AS can be used by a slave device to strobe the address into a register.

The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master.

$\overline{DAS}$ — **Data Strobe (Input/Output 3-State)**
Defines the data portion of the bus transaction. $\overline{DAS}$ is high during the address portion of a bus transaction and low during the data portion. The low to high transition can be used by a Slave device to strobe bus data into a register. $\overline{DAS}$ is driven only as a Bus Master.

$\overline{DALO}$ — **Data/Address Line Out (Output 3-State)**
An external bus transceiver control line. $\overline{DALO}$ is asserted when the LANCE drives the DAL lines. $\overline{DALO}$ will be low only during the address portion if the transfer is a READ. It will be low for the entire transfer if the transfer is a WRITE. $\overline{DALO}$ is driven only when LANCE is a Bus Master.

$\overline{DALI}$ — **Data/Address Line in (Output 3-State)**
An external bus transceiver control line. $\overline{DALI}$ is asserted when the LANCE reads from the DAL lines. It will be low during the data portion of a READ transfer, and remain high for the entire transfer if it is a WRITE. $\overline{DALI}$ is driven only when LANCE is a Bus Master.

$\overline{HOLD}$/$\overline{BUSRQ}$ — **Bus Hold Request (Output Open Drain)**
Asserted by the LANCE when it requires access to memory. $\overline{HOLD}$ is held LOW for the entire ensuing bus transaction. The function of this pin is programmed through bit (00) of CSR_3. Bit (00) of CSR_3 is cleared when $\overline{RESET}$ is asserted.

When CSR_3 (00) BCON = 0

I/O pin 17 = $\overline{HOLD}$ (Output Open Drain)

When CSR_3 (00) BCON = 1

I/O pin 17 = $\overline{BUSRQ}$ (Output Open Drain)

$\overline{BUSRQ}$ will be asserted only if I/O pin 17 is high prior to assertion.

$\overline{HLDA}$ — **Bus Hold Acknowledge (Input)**
A response to $\overline{HOLD}$. When $\overline{HLDA}$ is low in response to the chip's assertion of $\overline{HOLD}$, the chip is the Bus Master. $\overline{HLDA}$ deasserts upon the deassertion of $\overline{HOLD}$.

$\overline{INTR}$ — **Interrupt (Output Open Drain)**
An attention signal that indicates, when active, that one or more of the following CSR_0 status flags is set: BABL, MERR, MISS, RINT, TINT or IDON. $\overline{INTR}$ is enabled by bit 06 of CSR_0 (INEA = 1). $\overline{INTR}$ remains asserted until the source of Interrupt is removed.

RX — **Receive (Input)**
Receive Input Bit Stream.

TX — **Transmit (Output)**
Transmit Output Bit Stream.

TENA — **Transmit Enable (Output)**
Transmit Output Bit Stream enable. A level asserted with the Transmit Output Bit Stream, TX, to enable the external transmit logic.

RCLK — **Receive Clock (Input)**
A 10MHz square wave synchronized to the Receive data and only active while receiving an Input Bit Stream.

CLSN — **Collision (Input)**
A logical input that indicates that a collision is occurring on the channel.

RENA — **Receive Enable (Input)**
A logical input that indicates the presence of carrier on the channel.

TCLK — **Transmit Clock (Input)**
10MHz clock.

$\overline{READY}$ — **(Input/Output Open Drain)**
When the LANCE is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that it will accept data in a WRITE cycle or that it has put data on the DAL lines in a READ cycle.

As a Bus Slave, the LANCE asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data off the DAL lines during a write cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and will return HIGH after $\overline{DAS}$ has gone HIGH. $\overline{READY}$ is an input when the LANCE is a Bus Master and an output when the LANCE is a Bus Slave.

$\overline{RESET}$ — **(Input)**
Bus Reset Signal. Causes the LANCE to cease operation, clears its internal logic, and enter an idle state. The stop bit in CSR_0 is also set.

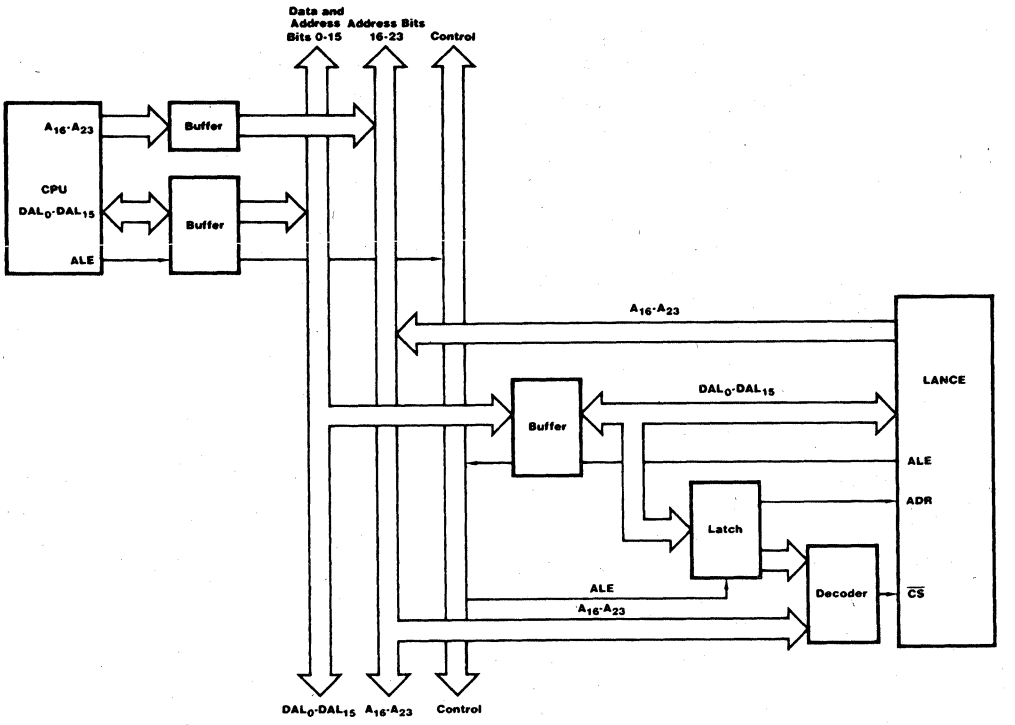
V_{CC} — Power supply pin +5 volts ±5%.

V_{SS} — Ground. Pins 1 and 24 should be connected together externally, as close to the chip as possible.

PRODUCT OVERVIEW

The parallel interface of the Local Area Network Controller for Ethernet (LANCE) has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: Z8000, 8086, 68000 and LSI-11. The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. A programmable mode of operation allows byte addressing in one of two ways: A Byte/Word control signal compatible with the 8086 and Z8000, or an Upper Data Strobe and Lower Data Strobe signal compatible with microprocessors such as the 68000. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

Figure 1. LANCE/CPU Interfacing
a. Multiplexed Bus



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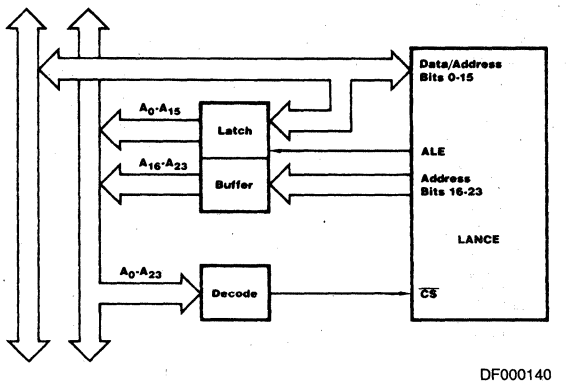
b. Demultiplexed Bus



DF000140

During initialization, the CPU loads the starting address of the initialization block into two internal control registers. The LANCE has four internal control and status registers ($CSR_{0, 1, 2, 3}$) which are used for various functions such as the loading of the initialization block address, different programming modes and status conditions. The host processor communicates with the LANCE during the initialization phase—for demand transmission and periodically to read the status bits following interrupts. All other transfers to and from the memory are handled as DMA under microword control.

Interrupts to the microprocessor are generated by the LANCE upon: 1) completion of its initialization routine, 2) the reception of a packet, 3) the transmission of a packet, 4) transmitter timeout error, 5) a missed packet and 6) memory error.

The cause of the interrupt is ascertained by reading CSR_0. Bit (06) of CSR_0, (INEA) enables or disables interrupts to the microprocessor. In systems where polling is used in place of interrupts, bit (07) of CSR_0 (INTR) indicates an interrupt condition.

The basic operation of the LANCE consists of two distinct modes: transmit and receive. In the transmit mode, the LANCE chip directly accesses data (in a transmit buffer) in memory. It prefaces the data with a preamble, sync pattern, and calculates and appends a 32-bit CRC. This packet is then ready for transmission to the Am7991A SIA. On transmission, the first byte of data loads into the 48-byte FIFO. The LANCE then begins to transmit preamble while simultaneously loading the rest of the packet into FIFO for transmission.

In the receive mode, packets are sent via the SIA to the LANCE. The packets are loaded into the 48-byte FIFO for preparation of automatic downloading into buffer memory. A CRC is calculated and compared with the CRC appended to the data packet. If the calculated CRC checksum doesn't agree with the packet CRC, an error bit is set.

DETAILED DESCRIPTION

ADDRESSING

Packets can be received using 3 different destination addressing schemes: physical, logical and promiscuous.

The first type is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address. One is group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. If any of these 64 groups have been preselected as the logical address, then the 48-bit address is stored in main memory. At this time, a look up is performed comparing the 48-bit incoming address with the pre-stored 48-bit logical address. The mode can be useful if sending packets to all of a particular type of device simultaneously (i.e., send a packet to all file servers or all printer servers). Additional details on logical addressing can be found in the INITIALIZATION section under "Logical Address Filter." The second logical address is a broadcast address where all nodes on the network receive the packet. The last receive mode of operation is the so-called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time, they will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit, detect the collision, then continue to transmit for a predetermined length of time to "jam" the network and ensure that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the Ethernet "truncated binary backoff" algorithm in order that the colliding nodes don't try to repeatedly access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before reporting back an error due to excessive collisions.

ERROR REPORTING AND DIAGNOSTICS

Extensive error reporting is provided by the LANCE. Error conditions reported relate either to the network as a whole or to data packets. Network-related errors are recorded as flags in the CSRs and are examined by the CPU following interrupt. Packet-related errors are written into descriptor entries corresponding to the packet.

System errors include:

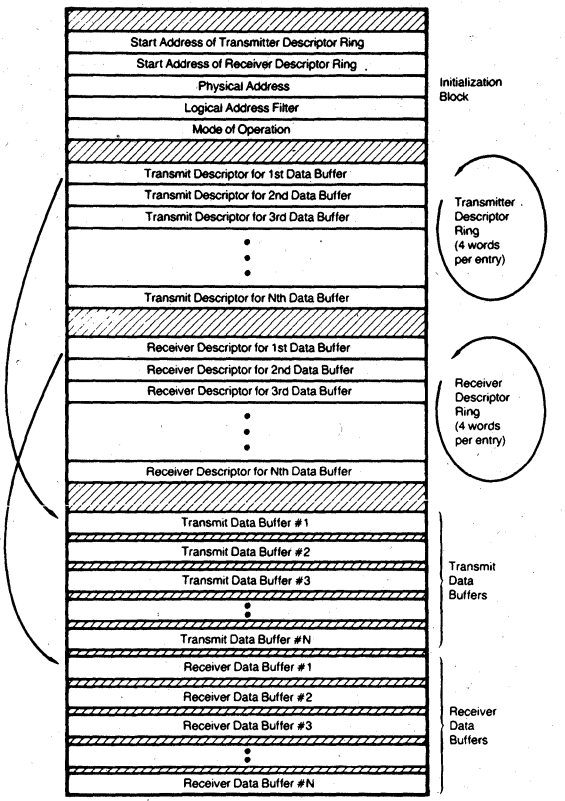
- Babbling Transmitter
  - Transmitter attempting to transmit more than 1518 data bytes.
- Collision
  - Collision detection circuitry nonfunctional
- Missed packet
  - Insufficient buffer space
- Memory timeout
  - Memory response failure

Packet-related errors:

- CRC
  - Invalid data
- Framing
  - Packet did not end on a byte boundary
- Overflow/Underflow
  - Indicates abnormal latency in servicing a DMA request
- Buffer
  - Insufficient buffer space available

The LANCE performs several diagnostic routines which enhance the reliability and integrity of the system. These include a CRC logic check and two loop back modes (internal/external). Errors may be introduced into the system to check error detection logic. A Time Domain Reflectometer is incorporated into the LANCE to aid system designers locate faults in the Ethernet cable. Shorts and opens manifest themselves in reflections which are sensed by the TDR.

Figure 2. LANCE/Processor Memory Interface



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BUFFER MANAGEMENT

A key feature of the LANCE and its on-board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 2. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, allowing the host processor to process the data in the buffer.

LANCE INTERFACE

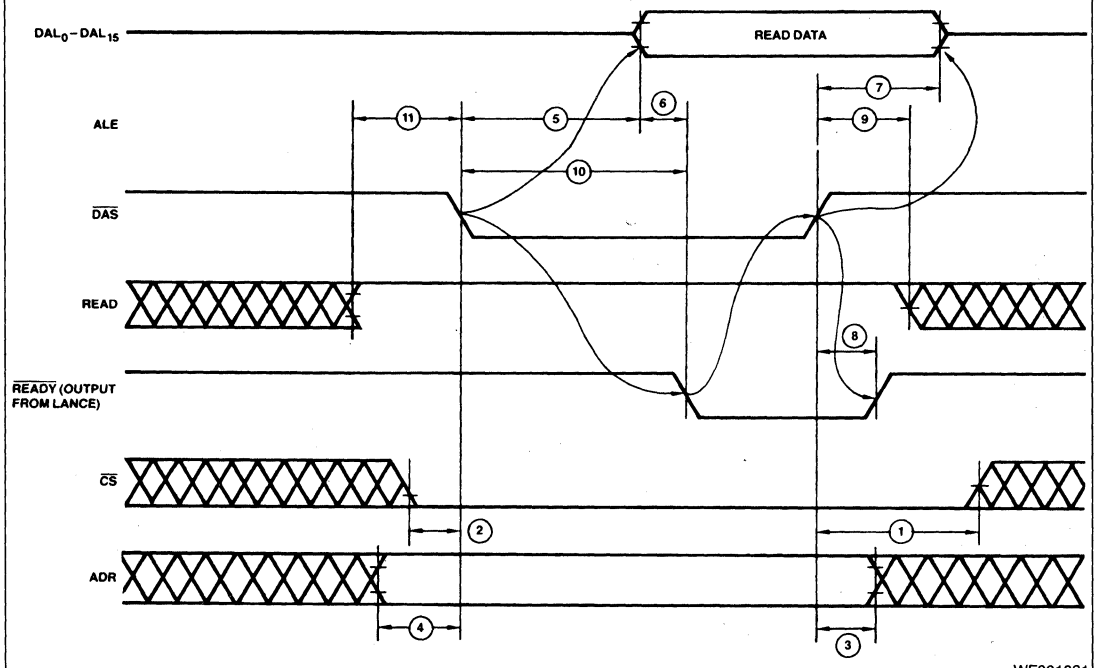
CSR bits such as ACON, BCON and BSWP are used for programming the pin functions used for different interfacing schemes. For example, ACON is used to program the polarity of the Address Strobe signal (ALE/$\overline{AS}$).

BCON is used for programming the pins, for handling either the BYTE/$\overline{WORD}$ method, for addressing word organized; byte addressable memories where the BYTE signal is decoded along with the least significant address bit to determine upper or lower byte, or an explicit scheme in which two signals labeled as BYTE MASK ($\overline{BM}_0$ and $\overline{BM}_1$) indicate which byte is addressed. When the BYTE scheme is chosen, the $\overline{BM}_1$ pin can be used for performing the function $\overline{BUSAKO}$.

BCON is also used to program pins for different DMA modes. In a daisy chain DMA scheme, 3 signals are used ($\overline{BUSRQ}$, $\overline{HLDA}$, $\overline{BUSAKO}$). In systems using a DMA controller for arbitration, only $\overline{HOLD}$ and $\overline{HLDA}$ are used.

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$, and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600ns in length and can be increased in 100ns increments.

BUS SLAVE READ TIMING



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Note: 1. There are two types of delays which depend on which internal register is accessed.
Type 1 refers to access of CSR_0, CSR_3 and RAP.
Type 2 refers to access of CSR_1 and CSR_2 which are longer than Type 1 delay.

READ SEQUENCE

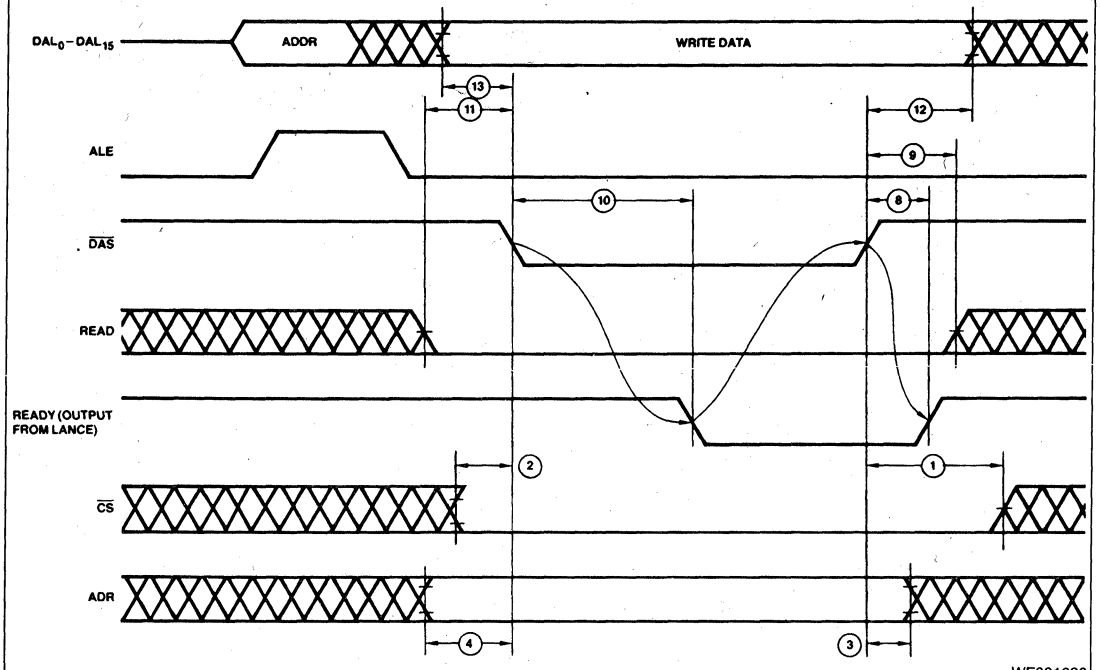
The read cycle is begun by valid addresses being placed on DAL_{00}–DAL_{15} and A_{16}–A_{23}. The BYTE MASK signals are placed valid to indicate a word, upper byte or lower byte memory reference. READ indicates the type of cycle. ALE or $\overline{AS}$ are pulsed, and the trailing edge of either can be used to latch addresses. DAL_{00}–DAL_{15} go into a 3-state mode and $\overline{DAS}$ falls low to signal the beginning of the memory access. The memory responds by placing $\overline{READY}$ low to indicate that the DAL lines have valid data. The LANCE then latches memory data on the rising edge of $\overline{DAS}$, which in turn ends the memory cycle and $\overline{READY}$ returns to high.

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE, and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ becomes active to avoid "spiking" of the bus transceivers.

WRITE SEQUENCE

The write cycle is very similar except that the DAL_{00}–DAL_{15} lines change from containing addresses to data after ALE or $\overline{AS}$ go inactive. After data is valid on the bus $\overline{DAS}$ goes active. Data to memory is held valid after $\overline{DAS}$ goes inactive.

BUS SLAVE WRITE TIMING



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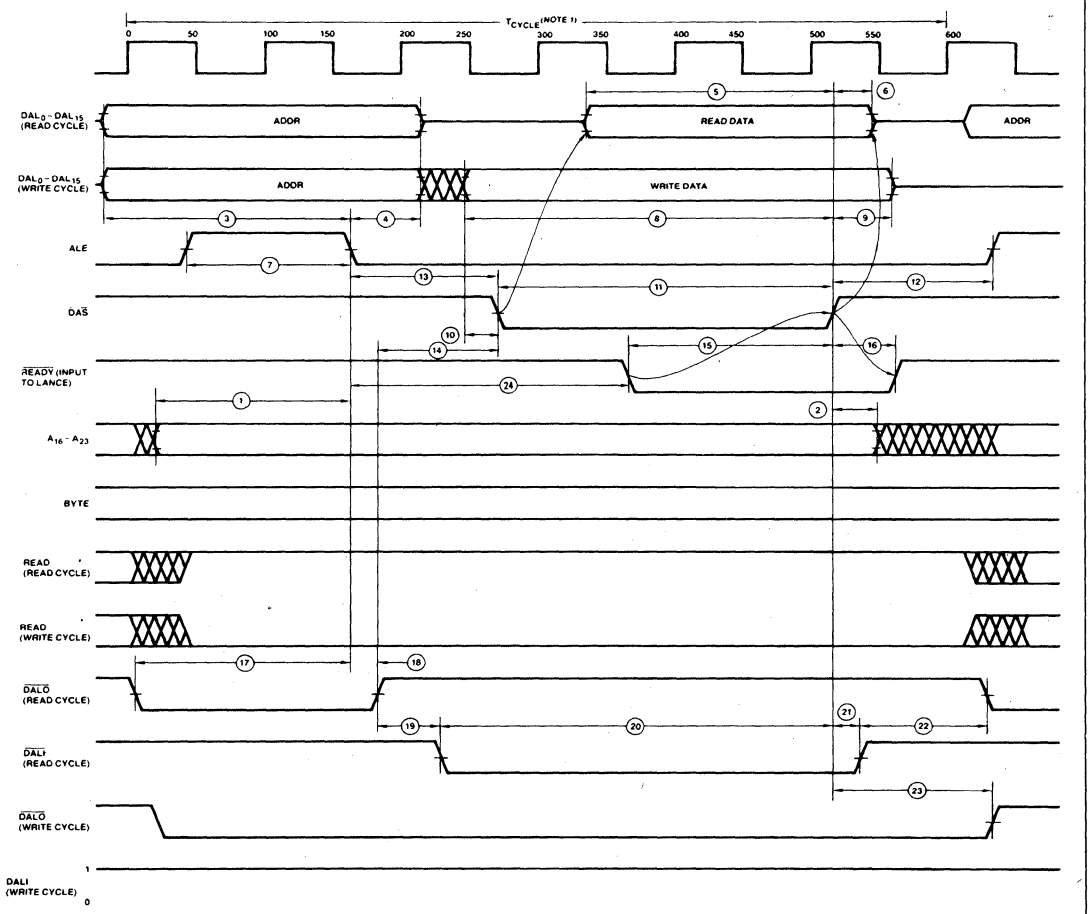
Refer to Page 13-1 for Essential Information on Military Devices

BUS MASTER TIMING



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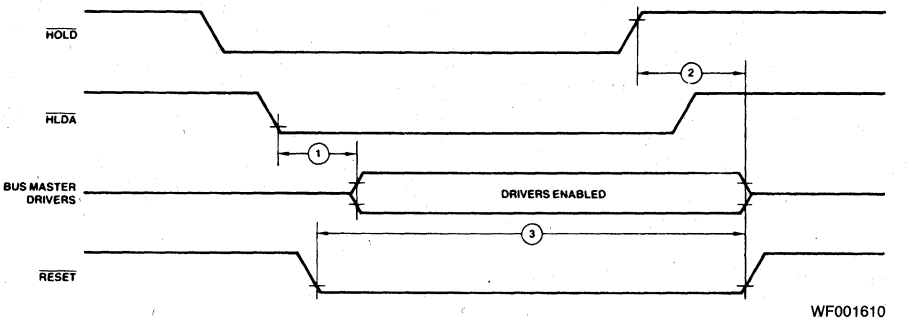
Notes: 1. T_{CYCLE} is the minimum transfer cycle and takes 600ns. Using $\overline{READY}$ it is possible to extend it in multiples of 100ns.

2. The $\overline{READY}$ setup time before negation of DAS is a function of the synchronization time of $\overline{READY}$. This is a critical parameter. The synchronization must occur within two internal clock ticks: 100ns. Therefore, the setup time will be 100ns plus the accumulated propagation delays, and the ready slips will occur on 100ns increments.

BUS ACQUISITION TIMING



Note: 1. $\overline{\text{RESET}}$ is an asynchronous input to the LANCE and is not part of the Bus Acquisition timing. When $\overline{\text{RESET}}$ is asserted, the LANCE becomes a Bus Slave.

DIFFERENCES BETWEEN ETHERNET VERSIONS 1 AND 2

a. Version 2 specifies that the collision detect of the transceiver must be activated during the interpacket gap time.

b. Version 2 specifies some network management functions, such as reporting the occurrence of collisions, retries and deferrals.

c. Version 2 specifies that when transmission is terminated, the differential transmit lines are driven OV diff. (half step).

DIFFERENCES BETWEEN IEEE 802.3 AND ETHERNET

a. 802 specifies a 2-byte length field rather than a type field. The length field (802) describes the actual amount of data in the frame.

b. 802 allows the use of a PAD field in the data section of a frame, while Ethernet specifies the minimum packet size at 64 bytes. The use of a PAD allows the user to send and receive packets which have less than 46 bytes of data.

Differences between Ethernet and 802 at the physical layer include the following:

	802	Ethernet
End of Transmission State	Half Step	High State (Rev 1) or Half Step
Common Mode Voltage	±5.5V	0 – +5V
Common Mode Current	Less than 1mA	1.6mA±40%
Input Threshold	±160mV	±175mV
Fault Protection	16V	0V

PROGRAMMING SPECIFICATION

This section defines the control and Status Registers and the memory data structures required to program the Am7990 (LANCE).

PROGRAMMING THE Am7990 (LANCE)

The Am7990 (LANCE) is designed to operate in an environment that includes close coupling with a local memory and a microprocessor (HOST). The Am7990 LANCE is programmed by a combination of registers and data structures resident within the chip and in memory. There are four Control and Status Registers (CSRs) within the chip which are programmed by the HOST device. Once enabled, the chip has the ability to access memory locations to acquire additional operating parameters.

The Am7990 has the ability to do independent buffer management as well as transfer data packets to and from the Ethernet. There are three memory structures accessed by the Chip:

1. Initialization Block – 12 words in contiguous memory starting on a word boundary. It also contains the operating parameters necessary for device operation. The initialization block is comprised of:
   - Mode of Operation
   - Physical Address
   - Logical Address Mask
   - Location to Receive and Transmit Descriptor Rings
   - Number of Entries in Receive and Transmit Descriptor Rings
2. Receive and Transmit Descriptor Rings – Two ring structures, one each for incoming and outgoing packets. Each entry in the rings is 4 words long and each entry must start on a quadword boundary. The Descriptor Rings are comprised of:
   - The address of a data buffer.
   - The length of that data buffer.
   - Status information associated with the buffer.
3. Data Buffers – Contiguous portions of memory reserved for packet buffering. Data buffers may begin on arbitrary byte boundaries.

In general, the programming sequence of the chip may be summarized as:

1. Programming the chip's CSRs by a host device to locate an initialization block in memory. The byte control, byte addressing, and address latch enable modes are defined here also.
2. The chip loads itself with the information contained within the initialization block.
3. The chip accesses the descriptor rings for packet handling.

CONTROL AND STATUS REGISTERS

There are four Control and Status Registers (CSRs) resident within the chip. The CSRs are accessed through two bus addressable ports, an address port (RAP) and a data port (RDP).

ACCESSING THE CONTROL AND STATUS REGISTERS

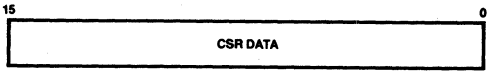
The CSRs are read (or written) in a two step operation. The address of the CSR to be accessed is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP.

Once written, the address in RAP remains unchanged until rewritten.

To distinguish the data port from the address port, a discrete I/O pin is provided.

ADR I/O Pin	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

Register Data Port (RDP)



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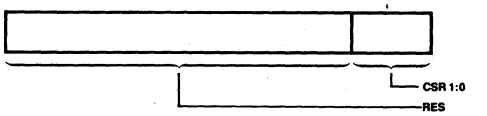
Bit	Name	Description
15:00	CSR Data	Writing data into RDP writes the data into the CSR selected in RAP. Reading the data from the RDP reads the data from the CSR selected in RAP. CSR_1, CSR_2 and CSR_3 are accessible only when the STOP bit of CSR_0 is set. If the STOP bit is not set while attempting to access CSR_1, CSR_2 or CSR_3, the chip will return READY, but a READ operation will return undefined data. WRITE operation is ignored.

Register Address Port (RAP)

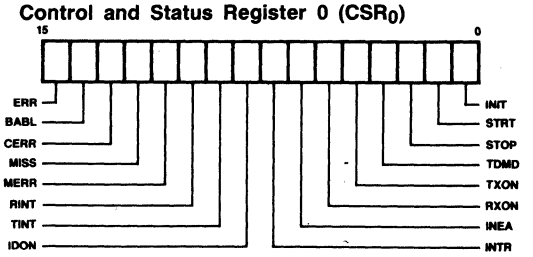


AF001490

Bit	Name	Description
15:02	RES	Reserved and read as zeroes.
01:00	CSR(1:0)	CSR address select. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR(1:0) — CSR 00 — CSR_0 01 — CSR_1 10 — CSR_2 11 — CSR_3

CONTROL AND STATUS REGISTER DEFINITION

Control and Status Register 0 (CSR_0)



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The LANCE updates CSR_0 by logical "ORING" the previous and present value of CSR_0.

Bit	Name	Description
15	ERR	ERROR summary is set by the "OR" of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only; writing it has no effect. It is cleared by Bus $\overline{\text{RESET}}$, by setting the STOP bit, or clearing the individual error flags.
14	BABL	BABBLE is a transmitter timeout error. It indicates that the transmitter has been on the channel longer than the time required to send the maximum length packet. BABL is a flag which indicates excessive length in the transmit buffer. It will be set after 1519 data bytes have been transmitted; the chip will continue to transmit until the whole packet is transmitted or there is a failure. When BABL error occurs, an interrupt will be generated if INEA = 1. BABL is READ/CLEAR ONLY and is set by the chip, and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

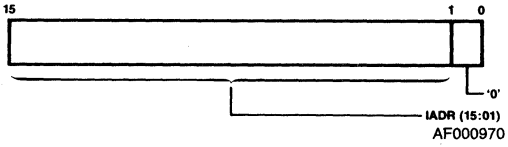
Bit	Name	Description
13	CERR	COLLISION ERROR indicates that the collision input to the chip failed to activate within 2μs after a chip-initiated transmission was completed. The collision after transmission is a transceiver test feature.This function is also known as heartbeat. CERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
12	MISS	MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer and the silo has overflowed, indicating loss of data. MISS is not valid in internal loopback mode. Silo overflow is not reported because there is no receive ring entry in which to write status. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY, and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
11	MERR	MEMORY ERROR is set when the chip is the Bus Master and has not received $\overline{\text{READY}}$ within 25.6μs after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY, and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
10	RINT	RECEIVER INTERRUPT is set when the chip updates an entry in the Receive Descriptor Ring for the last buffer received before fall of carrier. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY, and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
09	TINT	TRANSMITTER INTERRUPT is set when the chip updates an entry in the transmit descriptor ring for the last buffer sent before the end of transmission. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
08	IDON	INITIALIZATION DONE indicates that the chip has completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an interrupt is generated if INEA = 1. IDON is READ/CLEAR ONLY, and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
07	INTR	INTERRUPT FLAG is set by the "OR" of BABL, MISS, MERR, RINT, TINT and IDON. If INEA = 1 and INTR = 1, the INTR I/O pin will be low. INTR is READ ONLY; writing this bit has no effect. INTR is cleared by RESET, by setting the STOP bit, or by clearing the condition causing the interrupt.
06	INEA	INTERRUPT ENABLE allows the INTR I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1, the INTR I/O pin will be low. If INEA = 0, the INTR I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE and cleared by RESET or by setting the STOP bit.

Bit	Name	Description
05	RXON	RECEIVER ON indicates that the receiver is enabled. RXON is set when STRT is set if DRX = 0 in the MODE register in the initialization block and the initialization block has been read by the chip by setting the INIT bit. RXON is cleared when IDON is set from setting the INIT bit and DRX = 1 in the MODE register, or a memory error (MERR) has occurred. RXON is READ ONLY; writing this bit has no effect. RXON is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
04	TXON	TRANSMITTER ON indicates that the transmitter is enabled. TXON is set when STRT is set if DTX = 0 in the MODE register in the initialization block and the INIT bit has been set. TXON is cleared when IDON is set and DTX = 1 in the MODE register or an error, such as MERR, UFLO or BUFF, has occurred during transmission. TXON is READ ONLY; writing this bit has no effect. TXON is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
03	TDMD	TRANSMIT DEMAND—when set—causes the chip to access the Transmit Descriptor Ring without waiting for the polltime interval to elapse. TDMD need not be set to transmit a packet; it merely hastens the chip's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and is cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit. Writing a "0" in this bit has no effect.
02	STOP	STOP disables the chip from all external activity when set and clears the internal logic. Setting STOP is the equivalent of asserting $\overline{\text{RESET}}$. The chip remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set.
01	STRT	START enables the chip to send and receive packets, perform direct memory access, and do buffer management. STOP bit must be set prior to setting the STRT bit. Setting STRT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first. STRT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. STRT is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
00	INIT	INITIALIZE, when set, causes the chip to begin the initialization procedure and access the Initialization Block. STOP bit must be set prior to setting the INIT bit. Setting INIT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first. INIT is READ/WRITE WITH "1" ONLY. Writing a "0" into this bit has no effect. INIT is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

Control and Status Register 1 (CSR_1)

RAP = 1

READ/WRITE : Accessible only when the STOP bit of CSR_0 is a ONE. CSR_1 is unaffected by $\overline{\text{RESET}}$.



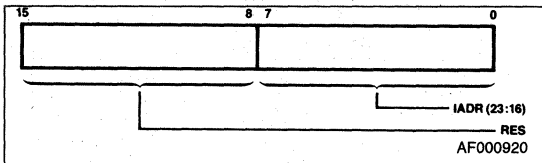
AF000970

Bit	Name	Description
15:01	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block.
00		Must be zero.

Control and Status Register 2 (CSR_2)

RAP = 2

READ/WRITE : Accessible only when the STOP bit of CSR_0 is a ONE. CSR_2 is unaffected by $\overline{\text{RESET}}$.



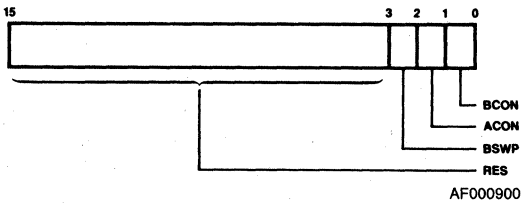
Bit	Name	Description
15:08	RES	Reserved.
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block.

Control and Status Register 3 (CSR_3)

CSR_3 allows redefinition of the Bus Master interface.

RAP = 3

READ/WRITE : Accessible only when the STOP bit of CSR_0 is ONE. CSR_3 is cleared by $\overline{RESET}$ or by setting the STOP bit in CSR_0.



Bit	Name	Description
15:03	RES	Reserved and read as "0".
02	BSWP	BYTE SWAP allows the chip to operate in systems that consider bits (15:08) to be the least significant byte and bits (07:00) to be the most significant byte. When BSWP = 1, the chip will swap the high and low bytes on DMA data transfers between the silo and bus memory. Only data from silo transfers is swapped; the Initialization Block data and the Descriptor Ring entries are NOT swapped. BSWP is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR_0.
01	ACON	ALE CONTROL defines the assertive state of ALE when the chip is a Bus Master. ACON is READ/WRITE and cleared by $\overline{RESET}$ and by setting the STOP bit in CSR_0. ACON — ALE 0 — Asserted High 1 — Asserted Low
00	BCON	BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR_0. BCON — I/O Pin 16 — I/O Pin 15 — I/O Pin 17 0 — $\overline{BM_1}$ — $\overline{BM_0}$ — $\overline{HOLD}$ 1 — $\overline{BUSAKO}$ — BYTE — $\overline{BUSRQ}$

All data transfers from the LANCE in the Bus Master mode are in words. However, the LANCE can handle odd address boundaries and/or packets with an odd number of bytes.

INITIALIZATION

INITIALIZATION BLOCK

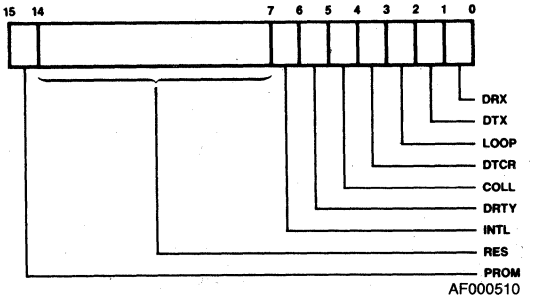
Chip initialization includes the reading of the initialization block in memory to obtain the operating parameters. The following is a definition of the Initialization Block.

The Initialization Block is read by the chip when the INIT bit in CSR_0 is set. The INIT bit should be set before or concurrent with the STRT bit to insure proper parameter initialization and chip operation. After the chip has read the Initialization Block, IDON is set in CSR_0 and an interrupt is generated if INEA = 1.

Higher Addresses	TLEN-TDRA (23:16)	IADR +22
	TDRA (15:00)	IADR +20
	RLEN-RDRA (23:16)	IADR +18
	RDRA (15:00)	IADR +6
	LADRF (63:48)	IADR +14
	LADRF (47:32)	IADR +12
	LADRF (31:16)	IADR +10
	LADRF (15:00)	IADR +08
	PADR (47:32)	IADR +06
	PADR (31:16)	IADR +04
	PADR (15:00)	IADR +02
Base Address of Block	MODE	IADR +00

Mode

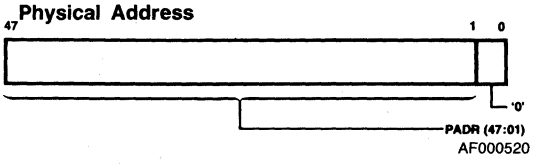
The Mode Register allows alteration of the chip's operating parameters. Normal operation is with the Mode Register clear.



Bit	Name	Description
15	PROM	PROMISCUOUS mode. When PROM = 1, all incoming packets are accepted.
14:07	RES	RESERVED

Bit	Name	Description
06	INTL	INTERNAL LOOPBACK is used with the LOOP bit to determine where the loopback is to be done. Internal loopback allows the chip to receive its own transmitted packet. Since this represents full duplex operation, the packet size is limited to 32 bytes. EXTERNAL LOOPBACK allows the LANCE to transmit a packet through the SIA transceiver cable out to the Ethernet coax. It is used to determine the operability of all circuitry and connections between the LANCE and the coaxial cable. INTL is only valid if LOOP = 1; otherwise it is ignored. LOOP INTL LOOPBACK 0 X No loopback, normal 1 0 External 1 1 Internal
05	DRTY	DISABLE RETRY. When DRTY = 1, the chip will attempt only one transmission of a packet. If there is a collision on the first transmission attempt, a Retry Error (RTRY) will be reported in Transmit Message Descriptor 3 (TMD_3).
04	COLL	FORCE COLLISION. This bit allows the collision logic to be tested. The chip must be in internal loopback mode for COLL to be valid. If COLL = 1, a collision will be forced during the subsequent transmission attempt. This will result in 16 total transmission attempts with a retry error reported in TMD_3.
03	DTCR	DISABLE TRANSMIT CRC. When DTCR = 0, the transmitter will generate and append a CRC to the transmitted packet. When DTCR = 1, the CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet. During loopback, DTCR = 0 will cause a CRC to be generated on the transmitted packet, but no CRC check will be done by the receiver since the CRC logic is shared and cannot generate and check CRC at the same time. The generated CRC will be written into memory with the data and can be checked by the host software.
		If DTCR = 1 during loopback, the host software must append a CRC value to the transmit data. The receiver will check the CRC on the received data and report any errors. Since the CRC generator is used to generate the hash filter, the multicast addressing cannot be used when DTCR = 1.
02	LOOP	LOOPBACK allows the chip to operate in full duplex mode for test purposes. The maximum packet size is 8–32 bytes.The received packet can be up to 36 bytes (32 + 4 bytes CRC) when DTCR=0. During loopback, runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet (64 bytes). LOOP = 1 allows simultaneous transmission and reception for a message constrained to fit within the silo. The chip waits until the entire message is in the silo before serial transmission begins. The incoming data stream fills the silo from behind as it is being emptied. Moving the received message out of the silo to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is possible if receive buffers are 32 bytes long to allow time for lookahead.
01	DTX	DISABLE THE TRANSMITTER causes the chip to not access the Transmitter Descriptor Ring and therefore no transmissions are attempted. DTX = 1 will clear the TXON bit in CSR_0 when initialization is complete.
00	DRX	DISABLE THE RECEIVER causes the chip to reject all incoming packets and not access the Receive Descriptor Ring. DRX = 1 will clear the RXON bit in the CSR_0 when initialization is complete.

Physical Address



AF000520

11

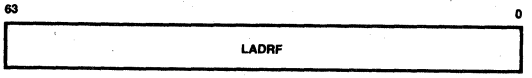
Bit	Name	Description
47:00	PADR	PHYSICAL ADDRESS is the unique 48-bit physical address assigned to the chip. PADR (0) must be zero.

Logical Address Filter

If the first bit of an incoming address is a "1" [PADR (0) = 1], the address is deemed logical and is passed through the logical address filter.

The logical address filter is a 64-bit mask that is used to accept incoming Logical Addresses. The incoming address is sent through the CRC circuit. After all 48 bits of the address have gone through the CRC circuit, the high order 6 bits of the resultant CRC are strobed into a register. This register is used to select one of the 64-bit positions in the Logical Address Filter. If the selected filter bit is a "1," the address is accepted and the packet will be put in memory. The logical address filter only assures that there is a possibility that the incoming logical address belongs to the node. To determine if it belongs to the node, the incoming logical address that is stored in main memory is compared by software to the physical address that was loaded through the initialization block.

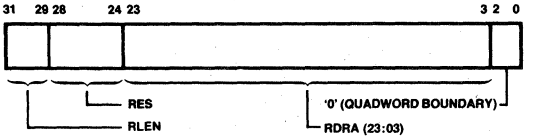
The Broadcast address, which is all ones, does not go through the Logical Address Filter and is always enabled. If the Logical Address Filter is loaded with all zeroes, all incoming logical addresses except broadcast will be rejected.



AF000500

Bit	Name	Description
63:00	LADRF	The 64-bit mask used by the chip to accept logical addresses.

Receive Descriptor Ring Pointer



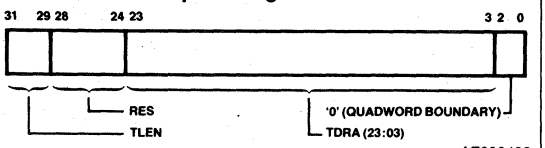
AF000490

Bit	Name	Description
15:13	RLEN	RECEIVE RING LENGTH is the number of entries in the receive ring expressed as a power of two.

RLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

12:08	RES	RESERVED
07:00 15:03	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Receive Descriptor Ring.
02:00		MUST BE ZEROES. These bits are RDRA (02:00) and must be zeroes because the Receive Rings are aligned on quadword boundaries.

Transmit Descriptor Ring Pointer



AF000480

Bit	Name	Description
15:13	TLEN	TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

12:08	RES	RESERVED
07:00 15:03	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring.
02:00		MUST BE ZEROES. These bits are TDRA (02:00) and must be zeroes because the Transmit Rings are aligned on quadword boundaries.

BUFFER MANAGEMENT

Buffer Management is accomplished through message descriptors organized in ring structures in memory. Each message descriptor entry is four words long. There are two rings allocated for the device: a Receive ring and a Transmit ring. The device is capable of polling each ring for buffers to either empty or fill with packets to or from the channel. The device is also capable of entering status information in the descriptor entry. Chip polling is limited to looking one ahead of the descriptor entry the chip is currently working with.

The location of the descriptor rings and their length are found in the initialization block, accessed during the initialization procedure by the chip. Writing a "ONE" into the STRT bit of CSR_0 will cause the chip to start accessing the descriptor rings and enable it to send and receive packets.

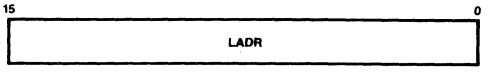
The chip communicates with a HOST device (probably a mircoprocessor) through the ring structures in memory. Each entry in the ring is either "owned" by the chip or the HOST. There is an ownership bit (OWN) in the message descriptor entry. Mutual exclusion is accomplished by a protocol which states that each device can only relinquish ownership of the descriptor entry to the other device; it can never take ownership, and no device can change the state of any field in any entry after it has relinquished ownership.

DESCRIPTOR RINGS

Each descriptor in a ring in memory is a 4-word entry. The following is the format of the receive and the transmit descriptors.

Receive Message Descriptor Entry

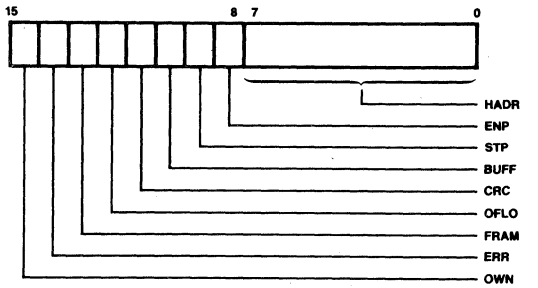
Receive Message Descriptor 0 (RMD_0)



AF000940

Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

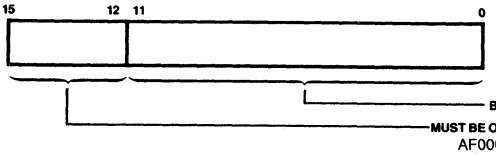
Receive Message Descriptor 1 (RMD_1)



AF000870

Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The chip clears the OWN bit after filling the buffer pointed to by the descriptor entry. The host sets the OWN bit after emptying the buffer. Once the chip or host has relinquished ownership of a buffer, it must not change any field in the four words that comprise the descriptor entry.
14	ERR	ERROR summary is the "OR" of FRAM, OFLO, CRC or BUFF. ERR is set by the chip and cleared by the host.
13	FRAM	FRAMMING ERROR indicates that the incoming packet contained a noninteger multiple of eight bits and there was a CRC error. If there was not a CRC error on the incoming packet, then FRAM will not be set even if there was a noninteger multiple of eight bits in the packet. FRAM is not valid in internal loopback mode. FRAM is set by the chip and cleared by the host.
12	OFLO	OVERFLOW error indicates that the receiver has lost all or part of the incoming packet due to an inability to store the packet in a memory buffer before the internal silo overflowed. OFLO is set by the chip and cleared by the host.
11	CRC	CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is set by the chip and cleared by the host.
10	BUFF	BUFFER ERROR is set any time the chip does not own the next buffer while data chaining a received packet. This can occur in either of two ways: 1) the OWN bit of the next buffer is zero, or 2) silo overflow occurred before the chip received the next STATUS. BUFF is set by the chip and cleared by the host. If a Buffer Error occurs, an Overflow Error may also occur internally in the SILO, but will not be reported in the descriptor status entry unless both BUFF and OFLO errors occur at the same time.
09	STP	START OF PACKET indicates that this is the first buffer used by the chip for this packet. It is used for data chaining buffers. STP is set by the chip and cleared by the host.
08	ENP	END OF PACKET indicates that this is the last buffer used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the chip and cleared by the host.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

Receive Message Descriptor 2 (RMD_2)

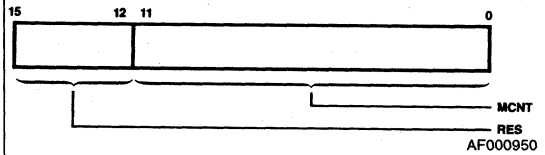


AF000930

11

Bit	Name	Description
15:12		MUST BE ONES. This field is written by the Host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the length of the buffer pointed to by this descriptor, expressed as a two's complement number. This field is written by the host and unchanged by the chip. Minimum buffer size is 64 bytes for the first buffer of packet.

Receive Message Descriptor 3 (RMD_3)

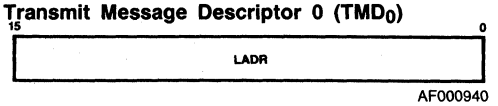


AF000950

Bit	Name	Description
15:12	RES	RESERVED and read as zeroes.
11:00	MCNT	MESSAGE BYTE COUNT is the length in bytes of the received message in Binary coded Decimal (BCD). MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the chip and cleared by the host.

Transmit Message Descriptor Entry

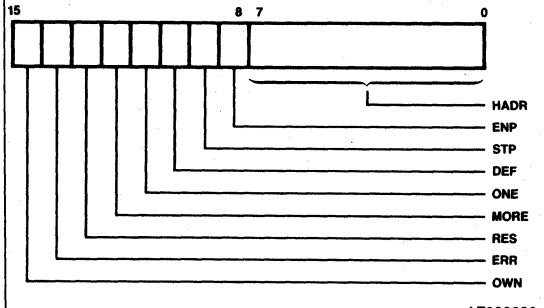
Transmit Message Descriptor 0 (TMD_0)



AF000940

Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

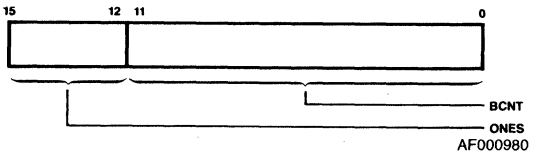
Transmit Message Descriptor 1 (TMD_1)



AF000880

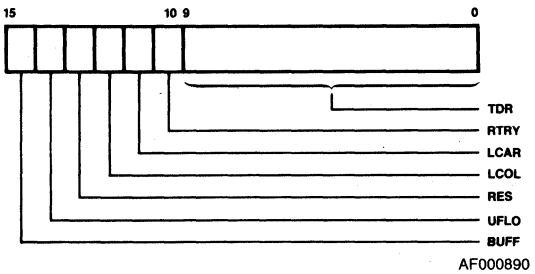
Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by this descriptor. The chip clears the OWN bit after transmitting the contents of the buffer. Both the host and the chip must not alter a descriptor entry after it has relinquished ownership.
14	ERR	ERROR summary is the "OR" of LCOL, LCAR, UFLO or RTRY. ERR is set by the chip and cleared by the host.
13	RES	RESERVED bit. The chip will write this bit with a "0."
12	MORE	MORE indicates that more than one retry was needed to transmit a packet. MORE is set by the chip and cleared by the host.
11	ONE	ONE indicates that exactly one retry was needed to transmit a packet. ONE is set by the chip and cleared by the host. One flag is not valid when LCOL is set.
10	DEF	DEFERRED indicates that the chip had to defer while trying to transmit a packet. This condition occurs if the channel is busy when the chip is ready to transmit. DEFER is set by the chip and cleared by the host.
09	STP	START OF PACKET indicates that this is the first buffer to be used by the chip for this packet. It is used for data chaining buffers. STP is set by the host and unchanged by the chip. The STP bit must be set in the first buffer of the packet or the LANCE will skip over this descriptor, poll the next descriptor(s) until the OWN and STP bit are set.
08	ENP	END OF PACKET indicates that this is the last buffer to be used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the host and unchanged by the chip.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

Transmit Message Descriptor 2 (TMD_2)

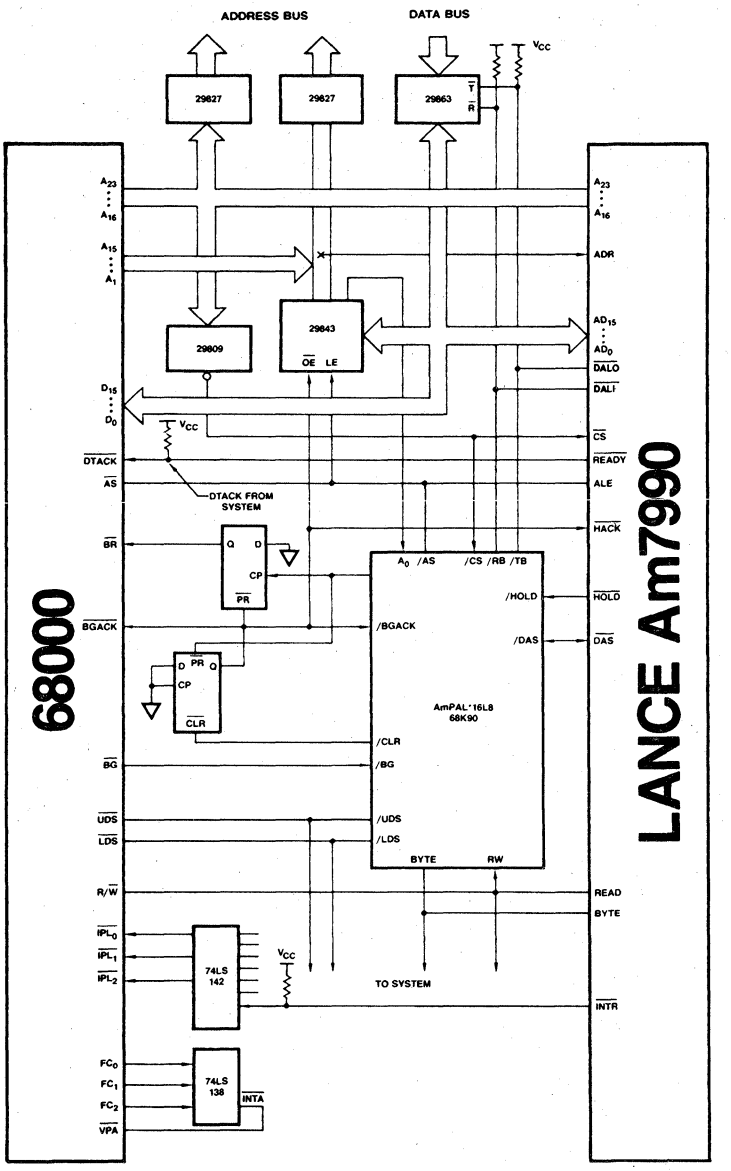


Bit	Name	Description
15:12	ONES	Must be ones. This field is set by the host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the usable length in bytes of the buffer pointed to by this descriptor expressed as a two's complement number. This is the number of bytes from this buffer that will be transmitted by the chip. This field is written by the host and unchanged by the chip. The first buffer of a packet has to be at least 100 bytes minimun when data chaining and 64 bytes when not data chaining.

Transmit Message Descriptor 3 (TMD_3)



Bit	Name	Description
15	BUFF	BUFFER ERROR is set by the chip during transmission when the chip does not find the ENP flag in the current buffer and does not own the next buffer. This can occur in either of two ways: either the OWN bit of the next buffer is zero, or silo underflow occurred before the chip received the next STATUS signal. BUFF is set by the chip and cleared by the host. BUFF error will disable the transmitter (CSR_0 = TXON = 0)
		If a Buffer Error occurs, an Underflow Error will also occur internally in the SILO. An underflow Error will not be reported in the descriptor status entry unless both BUFF and UFLO errors occur at the same time.
14	UFLO	UNDERFLOW ERROR indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that the silo has emptied before the end of the packet was reached. UFLO is set by the chip and cleared by the host.
13	RES	RESERVED bit. The chip will write this bit with a "0."
12	LCOL	LATE COLLISION indicates that a collision has occurred after the slot time of the channel has elapsed. The chip does not retry on late collisions. LCOL is set by the chip and cleared by the host.
11	LCAR	LOSS OF CARRIER is set when the carrier input (RENA) to the chip goes false during a chip-initiated transmission. The chip does not re-try upon loss of carrier. It will continue to transmit the whole packet LCAR until packet is finished. LCAR is not valid in INTERNAL LOOPBACK MODE. LCAR is set by the chip and cleared by the host.
10	RTRY	RETRY ERROR indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DRTY = 1 in the MODE register, RTRY will set after 1 failed transmission attempt. RTRY is set by the chip and cleared by the host.
09:00	TDR	TIME DOMAIN REFLECTOMETRY reflects the state of an internal chip counter that counts from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by the chip and is valid only if RTRY is set.



AF000371

68000 TO LANCE INTERFACE

The goal of this interface was to be compatible with 8MHz and faster 68000s while minimizing parts count. The Am22V10 could be used to eliminate the two flip-flops shown. Autovectoring is used since the Am7990 does not return a vector during interrupt acknowledge cycles. Note program BSWP, BCON to 1 and ACON to 0.

/AS RW BYTE/HOLD NC/BG AO NC/BGACK GND /CS/TB/ UDS/DAS/CLR BR NC/LDS/RB VCC

If (/BGACK) RB = CS*RW*UDS + CS*RW*LDS

If (/BGACK) TB = CS*/RW

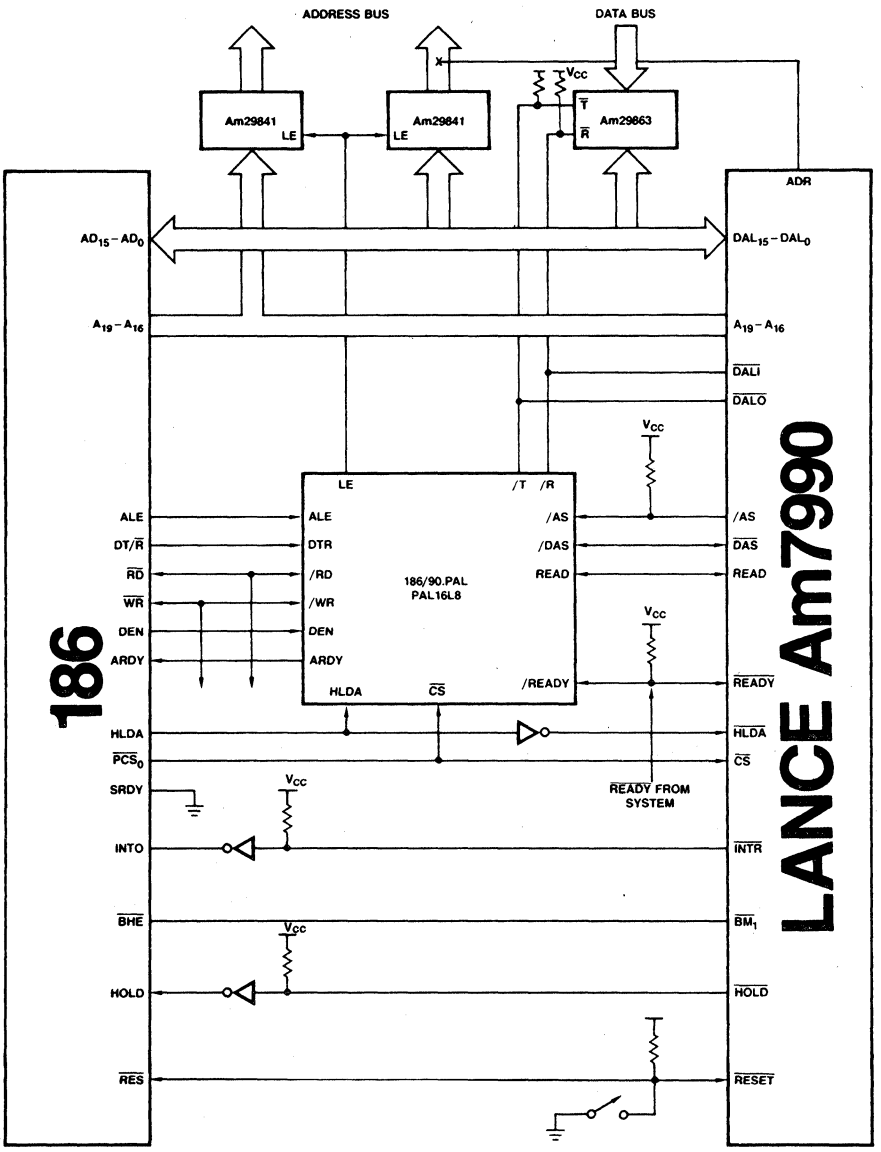
If (BGACK) UDS = DAS*/AO*BYTE + /BYTE*DAS

If (BGACK) LDS = DAS*AO*BYTE + /BYTE*DAS

If (/BGACK) DAS = UDS*LDS

CLR = /AS*BG

BR = /HOLD



AF000381

186 TO LANCE INTERFACE

This PAL design assumes that the 186 and LANCE are on the same board. The data bus buffer is only enabled if the LANCE is not selected. It seems natural to program the LANCE for ALE output. However, the PAL equations or indeed a discrete design is easier if/AS is used. This is because the LANCE tristates ALE; the 186 does not. Note data will be valid on the falling edge of/WR in min mode, meeting the apparent requirement of the LANCE in early data sheets. Data set up time is specified with respect to the rising edge of DAS in later data sheets; thus the designer has more flexibility. All transfers to or from the LANCE must be words. Program ACON to 1, BCON and BSWP to 0.

ALE/AS DTR NC NC DEN NC/READY HLDA GND /CS ARDY READ/R/T/DAS/WR/RD LE VCC

If (/HLDA) DAS = RD + WR

If (/HLDA)/READ = DTR

If (/HLDA) T = DTR*/CS

If (/HLDA) R = /DTR*DEN*/CS

If (HLDA) RD = READ*DAS

If (HLDA) WR = /READ*DAS

/LE = /ALE + /AS

/ARDY = /READY

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Applied Powers ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 20mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage		−0.5		0.8	Volts
V_{IH}	Input HIGH Voltage		2		V_{CC}+0.5V	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA			0.5	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −0.4mA	2.4			Volts
I_{IL}	Input Leakage	V_{IN} = 0.4V to V_{CC}			±10	μA

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters		Description	Test Conditions	Min	Typ	Max	Units
Bus Slave Timing							
1	t_{CSH}	Chip Select Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
2	t_{CSS}	Chip Select Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
3	t_{SAH}	ADR Hold Time following $\overline{DAS}$ LOW to HIGH		0			ns
4	t_{SAS}	ADR Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
5	t_{SDO1}	Data Delay following $\overline{DAS}$ HIGH to LOW	CSR_0, RAP, CSR_3		400		ns
	t_{SDO2}		CSR_1, CSR_2		1200		
6	t_{SRDS}	Read Data Setup Time before $\overline{READY}$ HIGH to LOW		75			ns
7	t_{SRDH}	Data Hold Time following $\overline{DAS}$ LOW to HIGH (Read Cycle)		0		35	ns
8	t_{SRYH}	$\overline{READY}$ Hold Time after $\overline{DAS}$ LOW to HIGH		0		35	ns
9	t_{SRH}	READ Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
10	t_{SRO1}	$\overline{READY}$ Driver Turn on Time after $\overline{DAS}$ HIGH to LOW	CSR_0, CSR_3, RAP		600		ns
	t_{SRO2}		CSR_1, CSR_2		1400		
11	t_{SRS}	READ Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
12	t_{SWDH}	Data Hold Time after $\overline{DAS}$ LOW to HIGH (Write Cycle)		0			ns
13	t_{SWDS}	Data Setup Time before $\overline{DAS}$ HIGH to LOW (Write Cycle)		0			ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters		Description	Test Conditions	Min	Typ	Max	Units
Bus Master Timing							
1	t_{XAS}	Extended Address Setup Time before ALE HIGH to LOW		75			ns
2	t_{XAH}	Extended Address Hold Time after $\overline{DAS}$ LOW to HIGH		35			ns
3	t_{AS}	Address Setup Time before ALE HIGH to LOW		75			ns
4	t_{AH}	Address Hold Time after ALE HIGH to LOW		35			ns
5	t_{RDAS}	READ Data Setup Time before $\overline{DAS}$ LOW to HIGH		50			ns
6	t_{RDAH}	READ Data Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
7	t_{ALEW}	ALE Width		130			ns
8	t_{WDS}	WRITE Data Setup Time before $\overline{DAS}$ LOW to HIGH		200			ns
9	t_{WDH}	WRITE Data Hold Time $\overline{DAS}$ LOW to HIGH		35			ns
10	t_{DDAS}	WRITE Data Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
11	t_{DSW}	$\overline{DAS}$ Width		200			ns
12	t_{DALE}	Delay from $\overline{DAS}$ LOW to HIGH to ALE LOW to HIGH		70			ns
13	t_{ADAS}	Delay from ALE HIGH to LOW to $\overline{DAS}$ HIGH to LOW		80			ns
14	t_{RIDF}	Delay from $\overline{DALO}$ LOW to HIGH to $\overline{DAS}$ HIGH to LOW (Read Cycle)		35			ns
15	t_{RDYS}	$\overline{READY}$ Setup Time before $\overline{DAS}$ LOW to HIGH (See Note)		75		250	ns
16	t_{RDYH}	$\overline{READY}$ Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
17	t_{OS}	$\overline{DALO}$ Setup Time before ALE HIGH to LOW		110			ns
18	t_{ROH}	$\overline{DALO}$ Hold Time after ALE HIGH to LOW (Read Cycle)		35			ns
19	t_{ROIF}	Delay from $\overline{DALO}$ LOW to HIGH to $\overline{DALI}$ HIGH to LOW (Read Cycle)		35			ns
20	t_{RIS}	$\overline{DALI}$ Setup Time before $\overline{DAS}$ LOW to HIGH (Read Cycle)		135			ns
21	t_{RIH}	$\overline{DALI}$ Hold Time after $\overline{DAS}$ LOW to HIGH (Read Cycle)		0			ns
22	t_{RIOF}	Delay from $\overline{DALI}$ LOW to HIGH to $\overline{DALO}$ HIGH to LOW (Read Cycle)		55			ns
23	t_{WDSI}	Delay from $\overline{DAS}$ LOW to HIGH to $\overline{DALO}$ LOW to HIGH (Write Cycle)		35			ns
24	t_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum Bus Cycle time (600ns).				80	ns

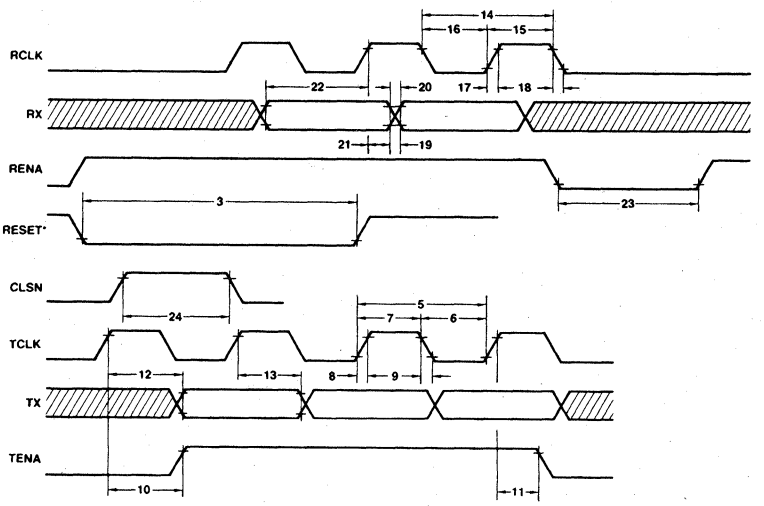
Note: The $\overline{READY}$ setup time before negation of $\overline{DAS}$ is a function of the synchronization time of $\overline{READY}$. The synchronization must occur within two clock ticks (100ns). Therefore, the setup time is 100ns plus any accumulated propagation delays. Ready slips occur on 100ns increments.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

	Parameters	Description	Test Conditions	Min	Typ	Max	Units
Bus Acquisition Timing							
1	t_{DON}	Bus Master Driver Enable Time after Assertion of $\overline{HLDA}$		0		250	ns
2	t_{DOFF}	Bus Master Driver Disable Time after Deassertion of HOLD		0		50	ns
3	t_{RW}	$\overline{RESET}$ Pulse Width (Note 1)		200			ns
4	t_{HHA}	HOLDA↓ to HOLD↓		0			
5	t_{TCT}	TCLK Period		99		101	ns
6	t_{TCL}	TCLK Low Time		45		55	ns
7	t_{TCH}	TCLK High Time		45		55	ns
8	t_{TCR}	Rise Time of TCLK		0		8	ns
9	t_{TCF}	Fall Time of TCLK		0		8	ns
10	t_{TEP}	TENA Propagation Delay after the Rising Edge of TCLK	C_L = 50pF			95	ns
11	t_{TEH}	TENA Hold Time after the Rising Edge of TCLK	C_L = 50pF	5			ns
12	t_{TDP}	TX Data Propagation Delay after the Rising Edge of TCLK	C_L = 50pF			95	ns
13	t_{TDH}	TX Data Hold Time after the Rising Edge of TCLK	C_L = 50pF	5			ns
14	t_{RCT}	RCLK Period		85		118	ns
15	t_{RCH}	RCLK High Time		38			ns
16	t_{RCL}	RCLK Low Time		38			ns
17	t_{RCR}	Rise Time of RCLK		0		8	ns
18	t_{RCF}	Fall Time of RCLK		0		8	ns
19	t_{RDR}	RX Data Rise Time		0		8	ns
20	t_{RDF}	RX Data Fall Time		0		8	ns
21	t_{RDH}	RX Data Hold Time (RCLK to RX Data Change)		5			ns
22	t_{RDS}	RX Data Setup Time (RX Data Stable to the Rising Edge of RCLK)		60			ns
23	t_{DPL}	RENA Low Time		120			ns
24	t_{CPH}	CLSN High Time		80			ns

Note: 1. $\overline{RESET}$ is an asynchronous input and does not occur as part of the Bus Acquisition cycle.

SERIAL LINK TIMING



WF001530

Note: 1.25ns offset from TCLK (¼ bit time and ¾ bit time from TCLK positive edge).

Timing measurements are made at the following voltages, unless otherwise specified:

	High	Low
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	V	0.5V

05698A

Refer to Page 13-1 for Essential Information on Military Devices

Am7991A/Am7992A*

Serial Interface Adapter (SIA)

DISTINCTIVE CHARACTERISTICS

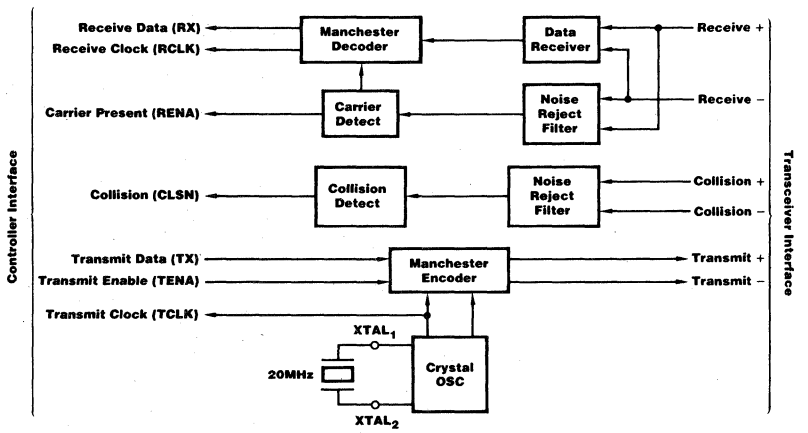
- Crystal controlled Manchester Encoder
- Manchester Decoder acquires clock and data within six bit times with an accuracy of ±3ns
  - Carrier/collision detected for greater than −300mV
  - No carrier/collision for less than −175mV
- Receiver decodes Manchester data with up to ±20ns clock jitter (at 10MHz)
- Input signal conditioning rejects transient noise
  - Transients < 10ns for collision detector inputs
  - Transients < 16ns for carrier detector inputs
- TTL compatible host interface
- Transmit accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

The Am7991A Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with both Ethernet and IEEE–802.3 specifications. In an Ethernet/IEEE-802.3 application the Am7991A interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable, acquires clock and data within 6 bit-times, and decodes Manchester data with up to ±20ns phase jitter at 10MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

BLOCK DIAGRAM

Serial Interface Adapter (SIA)



BD002070

RELATED PRODUCTS

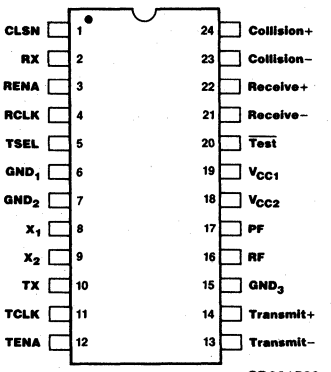
PART NO	DESCRIPTION
Am7990	Local Area Network Controller for Ethernet
Am7995	Ethernet Transceiver

*December 1983 – See Valid Combinations Note Under Ordering Information

03378C

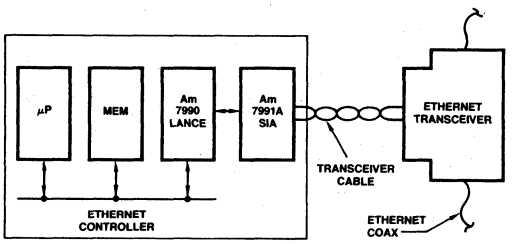
CONNECTION DIAGRAM
Top View

D-24-1



CD001520

TYPICAL ETHERNET NODE



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ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am7991A/92A **D** **C** **B**

- B: Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C: Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D: Package
  - D– 24-pin CERDIP *(D-24-1)
  - P– 24 pin plastic DIP (P-24-1)
- Am7991A/92A: Device type
  - Serial Interface Adapter (SIA)

Valid Combinations	
Am7991A	DC, DCB, DM, DMB
Am7992A	PC, DC, DCB, DM, DMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

* 7992A only available in D-24-SLIM.

PIN DESCRIPTION

CLSN **Collision (output)**
A TTL active high output. Signals at the Collision ±terminals meeting threshold and pulse width requirements will produce a logic high at CLSN output. When no signal is present at Collision ±, CLSN output will be low.

RX **Receive Data (output)**
A MOS/TTL output, recovered data. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RX is high. RX is actuated with RCLK and remains active until end of message. During reception, RX is synchronous with RCLK and changes after the rising edge of RCLK. When $\overline{\text{TEST}}$ is low, RX is enabled.

RENA **Receive Enable (output)**
A TTL active high output. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RENA is low. Signals meeting threshold and pulse width requirements will produce a logic high at RENA. When Receive ± becomes idle, RENA returns to the low state synchronous with the Manchester bit cell edge. For $\overline{\text{TEST}}$ low, RENA function is disabled.

RCLK **Receive Clock (output)**
A MOS/TTL output recovered clock. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RCLK is low. RCLK is activated after the third negative data transmission at Receive ±, and remains active until end of message. When $\overline{\text{TEST}}$ is low, RCLK is enabled independent of Receive ±.

TX **Transmit (Input)**
TTL compatible input. When TENA is high, signals at TX meeting setup and hold time to TCLK will be encoded as normal Manchester at Transmit + and Transmit –.

TX High: Transmit + is negative with respect to Transmit – for first half of data bit cell.

TX Low: Transmit + is positive with respect to Transmit – for first half of data bit cell.

TENA **Transmit Enable (Input)**
TTL compatible input. Active high data encoder enable. Signals meeting setup and hold time to TCLK will allow encoding of Manchester data from TX to Transmit + and Transmit –.

TCLK **Transmit Clock (output)**
MOS/TTL output. TCLK provides symmetrical high and low clock signals at data rate for reference timing of data to be encoded. It also provides clock signals for the controller chip (Am7990 – LANCE) and an internal timing reference for receive path voltage controlled oscillators.

Transmit +
Transmit – **Transmit (outputs)**
A differential line output. This line pair is intended to operate into terminated transmission lines. For signals meeting setup and hold time to TCLK at TENA and TX Manchester clock the data is outputted at Transmit + /Transmit –. When operating into a 78Ω terminated transmission line, signalling meets the required output levels and skew for both Ethernet and IEEE 802.3 drop cables.

Receive +
Receive – **Receiver (Inputs)**
A differential input. A pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the signal, and a data recovery receiver with no offset for Manchester data decoding.

Collision +
Collision – **Collision (Inputs)**
A differential input. An internally biased line receiver input with offset threshold and noise filtering. Signals at Collision ± have no effect on data path functions.

TSEL **Transmit Mode Select**
An open collector output and sense amplifier input.

TSEL Low: Idle transmit state Transmit + is positive with respect to Transmit –.

TSEL High: Idle transmit state Transmit + and Transmit – are equal, providing "zero" differential to operate transformer coupled loads.

When connected with an RC network, TSEL is held low during transmission. At the end of transmission the open collector output is disabled, allowing TSEL to rise and provide a smooth transmission from logic high to "zero" differential idle. Delay and output return to zero are externally controlled by the RC time constant TSEL.

X_1, X_2 **Biased Crystal Oscillator**
X_1 is the input and X_2 is the bypass port. When connected for crystal operation, the system clock which appears at TCLK is half the frequency of the crystal oscillator. X_1 may be driven from an external source of two times the data rate.

RF **Frequency Setting Voltage Controlled Oscillator (V_{CO}) Loop Filter**
This loop filter output is a reference voltage for the receive path phase detector. It also is a reference for timing noise immunity circuits in the collision and receive enable path. Nominal reference V_{CO} gain is 1.25 TCLK frequency MHz/V.

PF **Receive Path V_{CO} Phase Lock Loop Filter**
This loop filter input is the control for receive path loop damping. Frequency of the receive V_{CO} is internally limited to transmit frequency ±12%. Nominal receive V_{CO} gain is 0.25 reference V_{CO} gain MHz/V.

$\overline{TEST}$	**Test Control (Input)** A static input that is connected to V_{CC} for normal Am7991 operation and to ground for testing of receive path function. When $\overline{TEST}$ is grounded RCLK and RX are enabled so that receive path loop may be functionally tested.
GND_1	**High Current Ground**
GND_2	**Logic Ground**
GND_3	**Voltage Controlled Oscillator Ground**
V_{CC1}	**High Current and Logic Supply**
V_{CC2}	**Voltage Controlled Oscillator Supply**

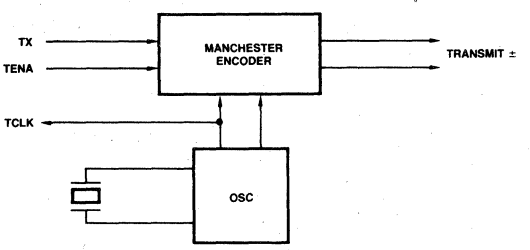
DETAILED DESCRIPTION

The Am7991A Serial Interface Adapter (SIA) has three basic functions. It is a Manchester Encoder/line driver in the transmit path, a Manchester Decoder with noise filtering and quick lock-on characteristics in the receive path, and a signal detect/converter (10MHz differential to TTL) in the collision path. In addition, the SIA provides the interface between the TTL logic environment of the Local Area Network Controller for Ethernet (LANCE) and the differential signaling environment in the transceiver cable.

TRANSMIT PATH

The transmit section encodes separate clock and NRZ data input signals meeting the set up and hold time to TCLK at TENA and TX, into a standard Manchester II serial bit stream. The transmit outputs (transmit + /transmit –) are designed to operate into terminated transmission lines. When operating into a 78Ω terminated transmission line, signaling meets the required output levels and skew for both Ethernet and IEEE–802.3

Figure 1. Transmit Section



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Transmitter Timing and Operation

A 20MHz fundamental mode crystal oscillator provides the basic timing reference in the SIA. It is divided by two to create the transmit clock reference (TCLK). Both 20MHz and 10MHz clocks are fed into the Manchester Encoder to generate the transitions in the encoded data stream. The 10MHz clock, TCLK, is used by the SIA to internally synchronize transmit data (TX) and transmit enable (TENA). TCLK is also used as a stable bit rate clock by the receive section of the SIA and by other devices in the system (the AM7990 LANCE used TCLK to drive its internal state machine). The oscillator may use an external .005% crystal or an external TTL level input as a reference. Transmit accuracy of .01% is achieved (no external adjustments are required).

TENA is activated when the first bit of data is made available on TX. As long as TENA remains High, signals at TX will be encoded as Manchester and will appear at transmit + and transmit –. When TENA goes Low, the differential transmit outputs go to one of two idle states:

- Mode 1 – (TSEL High) The idle state of transmit + /transmit – yields "zero" differential to operate transformer coupled loads.
- Mode 2 – (TSEL Low) in this idle state, transmit + is positive to transmit – (logical High). (Figure 11A)

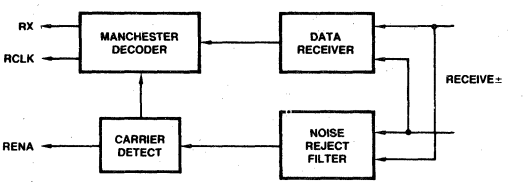
RECEIVE PATH

The principle function of the receiver is the separation of the Manchester encoded data stream into clock and NRZ data.

Input Signal Conditioning

Before the data and clock can be separated it must be determined whether there is "real" data or unwanted noise at the transceiver interface. The Am7991A SIA carrier detection receiver provides a static noise margin of –175mV to –300mV for received carrier detection. These DC thresholds assure that no signal more positive than –175mV is ever decoded and that signals more negative than –300mV are always decoded. Transient noise of less than 10ns duration in the collision path and 16ns duration in the data path are also rejected.

Figure 2. Receiver



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The stage prevents unwanted idle state noise on the transceiver cable from causing "false starts" in the receiver. This helps assure a valid response to "real" data.

The receiver section (Figure 3) consists of two data paths. The receive data path is designed to be a zero threshold, high bandwidth receiver. The carrier detection receiver is similar, but with an additional bias generator. Only data amplitudes larger than the bias level are interpreted as valid data. The noise rejection filter prevents noise transients < 16ns from enabling the data receiver output. The collision detector similarly rejects noise transients < 10ns.

Receiver Section Timing

Receive Enable (RENA) is the "carrier present" indication established when a signal of sufficient amplitude (V_{IDC}) and duration (t_{RPWR}) is present at the receive inputs. Receive Clock (RCLK) and Receive Data (RX) become available after the third negative data transition at receive+/receive – inputs, and stay active until end of packet. During reception, RX is synchronous with RCLK changing after the rising edge of RCLK.

The receiver detects the end of a packet when the normal transition on the differential inputs cease. After the last Low–to–High transition, RENA goes Low and RCLK completes

one last cycle, storing the last data bit. It then goes Low, and remains Low. (See Receive End of Packet Timing diagrams.) When $\overline{TEST}$ is Low, RCLK does not go Low and stay Low but continues to run.

Receive Clock Control

To ensure quick capture of incoming data the receiver phase–locked–loop is frequency locked to the transmit oscillator and it phase locks to incoming data edges.

Clock and data are available within 6 bit times (accurate to within ±3ns). The SIA will decode jittered data of up to ±20ns (Figure 4).

Differential 1/0 Terminations

The differential input for the Manchester data (receive ±) is externally terminated by two 40.2Ω ±1% resistors and one optional common mode bypass capacitor. The differential input impedance Z_{IDF} and the common mode input Z_{ICM} are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The collision ± differential input is terminated in exactly the same way as the receive input (See External Component diagram)

Collision Detection

The Ethernet Transceiver detects collisions on the Ethernet and generates a 10MHz signal on the transceiver cable (collision +/collision–). This collision signal passes through an input stage which assures signal levels and pulse duration. When the signal is detected by the SIA, the SIA sets the CLSN line High. This condition continues for approximately 190ns after the last Low-to-High transition on collision +/collision–.

Figure 3. Receiver Section Detail

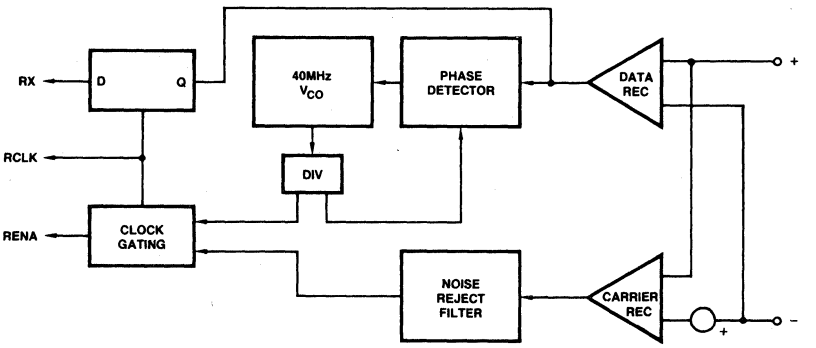
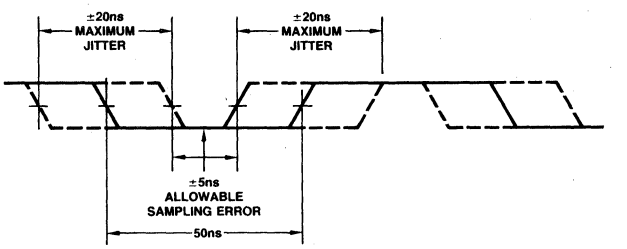
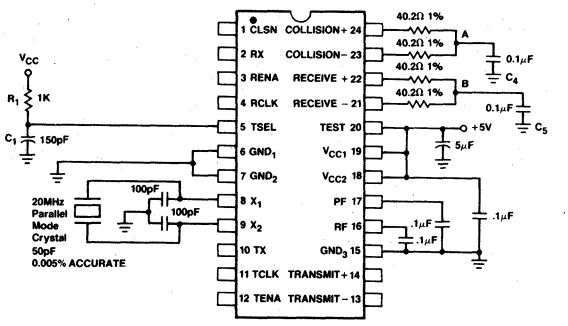


Figure 4. Maximum Jitter Impact on Sampling



Am7991A
External Component Diagram



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Notes: 1. Connect R_1, C_1, for 0 differential nontransmit. Connect to ground for logic 1 differential nontransmit.
2. Pin 20 shown for normal device operation.
3. Nodes A and B may be connected directly to ground for proper decoder operation, or to the common mode bypass C_4 and C_5. Some direct coupled transceivers require C_4 and C_5 to ground for proper operation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage (Logic Inputs) ..... +5.5V
DC Input Voltage (Rec Coll) ..... −6V to +6V
Transmit ±Output Current ..... −50mA to +5mA
DC Output Current, Into Outputs 100mA
DC Input Current (Logic Inputs) ..... ±30mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

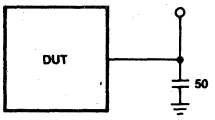
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage RXD, RENA, CLSN,TCLK	I_{OH} = −1.0mA	2.4	3.4		V
V_{OL}	Output Low Voltage RCLK, TCLK, RENA RXD, CLSN, TSEL	I_{OL} = 16mA			0.5	V
		I_{OL} = 1mA			0.4	
V_{OD}	Differential Output Voltage (Transmit+)−(Transmit−) V_O	RL = 78Ω	550		900	mV
	Differential Output Voltage (Transmit+)−(Transmit−) $\overline{V_O}$		−550		−900	
$V_{OD\ OFF}$	Transmit Differential Output Idle Voltage		−20	0.5	20	mV
$I_{OD\ OFF}$	Transmit Differential Output Idle Current		−0.5	±00.1	0.5	mA
V_{CMT}	Common Mode Output Transmit		0		5	V
V_{ODI}	Differential Output Voltage Imbalance (Transmit±) $\|\|V_O\|-\|\overline{V_O}\|\|$			5	20	mV
V_{IH}	Input High Voltage TTL		2.0			V
I_{IH}	Input High Current TTL	V_{CC} = MAX, V_{IN} = 2.7V			+50	μ
V_{IL}	Input Low Voltage TTL				0.8	V
I_{IL}	Input Low Current TTL	V_{CC} = MAX, V_{IN} = 0.4V			−400	μ
V_{IRD}	Differential Input Threshold (Rec Data)		−25	0	+25	mV
V_{IDC}	Differential Input Threshold (Carrier/Collision±)		−175	−225	−300	mV
I_{CC}	Power Supply Current	t_{OSC} = 50ns		100	180	mA
		t_{OSC} = 50ns, T_A = MAX			160	
I_I	Input Breakdown Current V_I = +5.5 (T_X, TENA)				1	mA
V_{IC}	I_{IN} = −18mA				−1.2	V
I_{SCO}	RXD, TCLK, CLSN, RENA Short Circuit Current		−40		−150	mA
R_{IDF}	Differential Input Resistance	V_{CC} = 0 to MAX	6k	8.4k	13k	Ω
R_{ICM}	Common Mode Input Resistance	V_{CC} = 0 to MAX	1.5k	2.1k	3.25k	Ω
V_{ICM}	Receive and Collision Input Voltage	I_{IN} = 0	2.5	3.5	4.2	V
I_{ILD}	Receive and Collision Input Low Current	V_{IN} = −1V	−0.32	−1.06	−1.64	mA
I_{IHD}	Receive and Collision Input High Current	V_{IN} = 6V	+0.14	+0.6	+1.10	mA
I_{IHZ}	Receive and Collision Input High Current	V_{CC} = 0, V_{IN} = +6V	0.4	1.28	1.86	mA

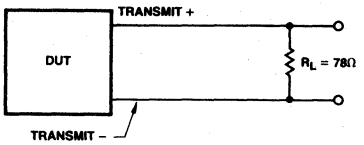
SWITCHING TEST CIRCUIT

Figure 5. Test Load for RX, RENA, RCLK, TCLK



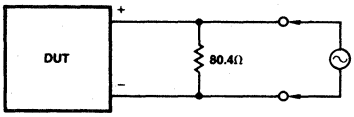
TC000470

Figure 6. Transmit ± Output Test Circuit



TC000461

Figure 7. Receive ±and Collision ±Input Test Circui t



TC000480

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Receiver Specification						
t_{RCT}	RCLK Cycle Time	t_{OSC} = 50ns	85		118	ns
t_{RCH}	RCLK High Time		38			ns
t_{RCL}	RCLK Low Time		38			ns
t_{RCR}	RCLK Rise Time	C_L = 50pF Figures 13 and 14 (Note 1)	0		8	ns
t_{RCF}	RCLK Fall Time		0		8	ns
t_{RDR}	RX Rise Time		0		8	ns
t_{RDF}	RX Fall Time		0		8	ns
t_{RDH}	RX Hold Time (RCLK to RX Change)		5			ns
t_{RDS}	RX Prop Delay (RCLK to RX Stable)				25	ns
t_{DPH}	RENA Turn-On Delay (V_{IDC} on Receive ± to $RENA_H$)	Figures 7 and 8			180	ns
t_{DPO}	RENA Turn-Off Delay (V_{IDH} on Receive ± to $RENA_L$)	Figures 7 and 9			160	ns
t_{DPL}	RENA Low Time	Figure 9	120			ns
t_{RPWR}	Receive ± Input Pulse Width to Reject (Input < V_{IDC})	Figures 7 and 14			16	ns
t_{RPWO}	Receive ± Input Pulse Width to Turn-On (Input < V_{IDC})	Figures 7 and 14	40			ns
t_{RLT}	Decoder Acquisition Time	Figure 8			600	ns
Collision Specification						
t_{CPWR}	Collision Input Pulse Width to Reject (Input < V_{IDC})	Figures 7 and 14			10	ns
t_{CPWO}	Collision Input Pulse Width to Turn-on (Collision ± Exceeds V_{IDC})	Figures 7, 12 and 14	26			ns
t_{CPWE}	Collision Input to Turn-Off CSLN (Input > V_{ILDO})	Figures 7 and 14	80			ns
t_{CPWN}	Collision Input to Not Turn-Off CLSN (Input > V_{IDC})				160	ns
t_{CPH}	CLSN Turn-On Delay (V_{IDC} on Collision ± to $CLSN_H$)	Figures 7, 12 and 13			180	ns
t_{CPO}	CLSN Turn-Off Delay (V_{IHD} on Collision ± to $CLSN_L$)				160	ns

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transmitter Specification						
t_{TCL}	TCLK Low Time	t_{OSC} = 50ns Figures 5 and 15	45		55	ns
t_{TCH}	TCLK High Time		45		55	ns
t_{TCR}	TCLK Rise Time		0		8	ns
t_{TCF}	TCLK Fall Time		0		8	ns
t_{TDS}, t_{ES}	TXD and TEN Setup Time	Figures 11 and 12	5			ns
t_{TDH}, t_{EH}	TXD and TEN Hold Time		5			ns
t_{TOCE}	Transmit ± Output, (Bit Cell Center to Edge)	Figures 6 and 11	49.5		50.5	ns
t_{OD}	TCLK High to Transmit ± Output				100	ns
t_{TOR}	Transmit ± Output Rise Time	20 – 80% Figure 11	1		5	ns
t_{TOF}	Transmit ± Output Fall Time		1		5	ns
V_{OD1}	Transmit Return to Zero Differential at End of Message Voltage at 1 Bit Time					mV
V_{OD2}	Transmit Return to Zero Differential at End of Message Voltage at 2 Bit Time					mV
V_{OD3}	Undershoot Voltage at Zero Differential Point on Transmit Return to Zero (End of Message)					mV

Note 1. Assumes equal capacitance loading on RCLK and RX.

Figure 8. Receiver Timing – Start of Packet

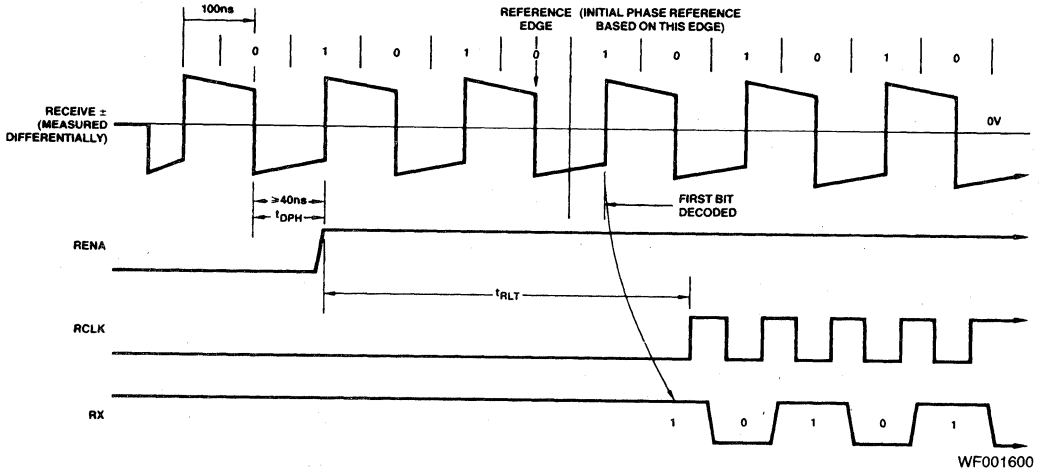


Figure 9. Receiver Timing – End of Packet (Last Bit = 0)

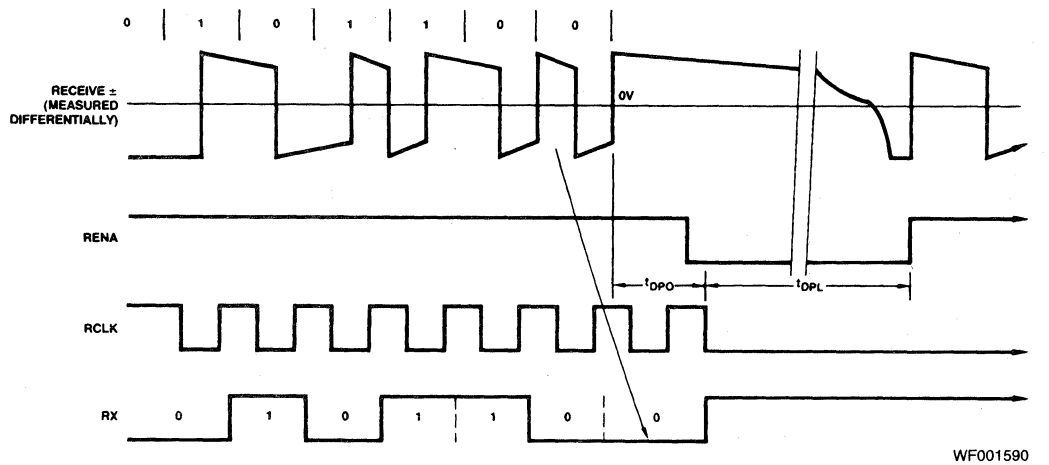


Figure 10. Receiver Timing – End of Packet (Last Bit = 1)

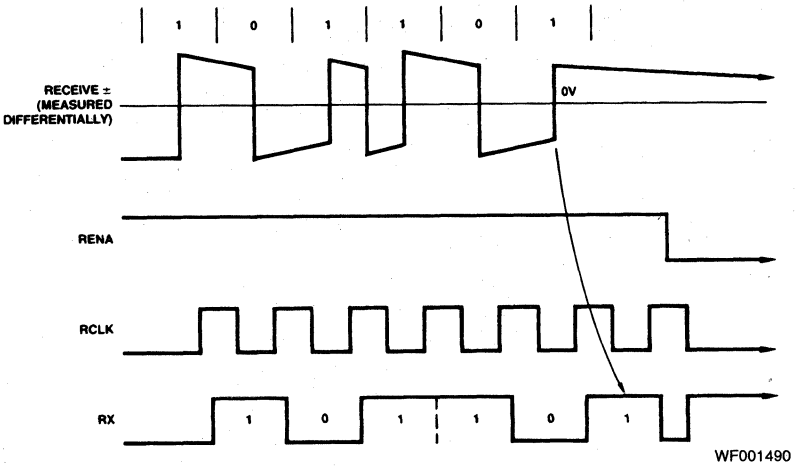


Figure 11A. Transmitter Timing – Start of Transmission

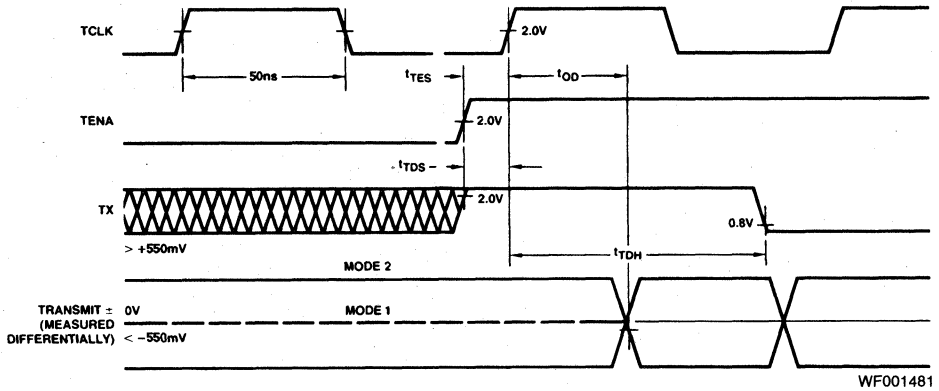
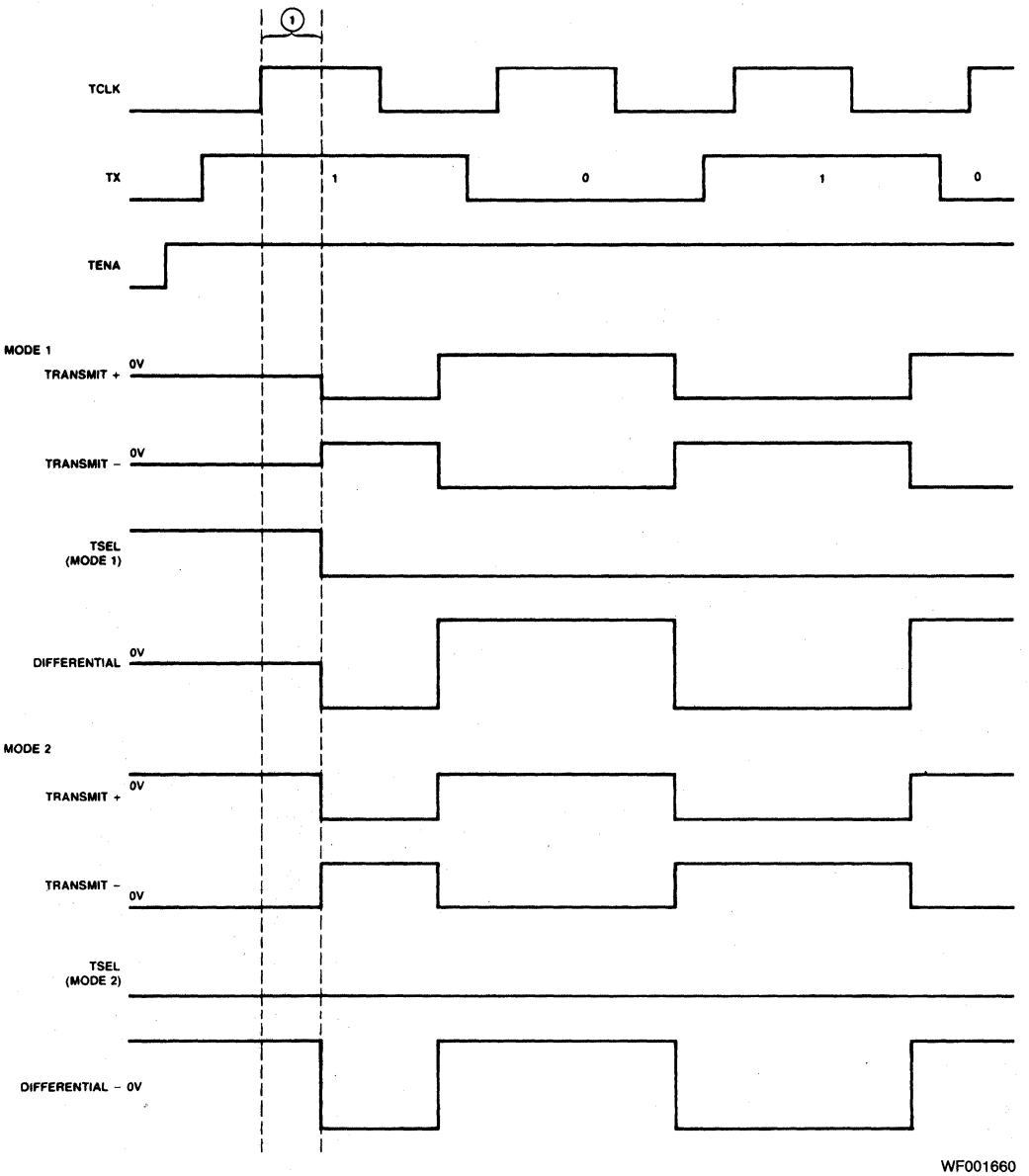


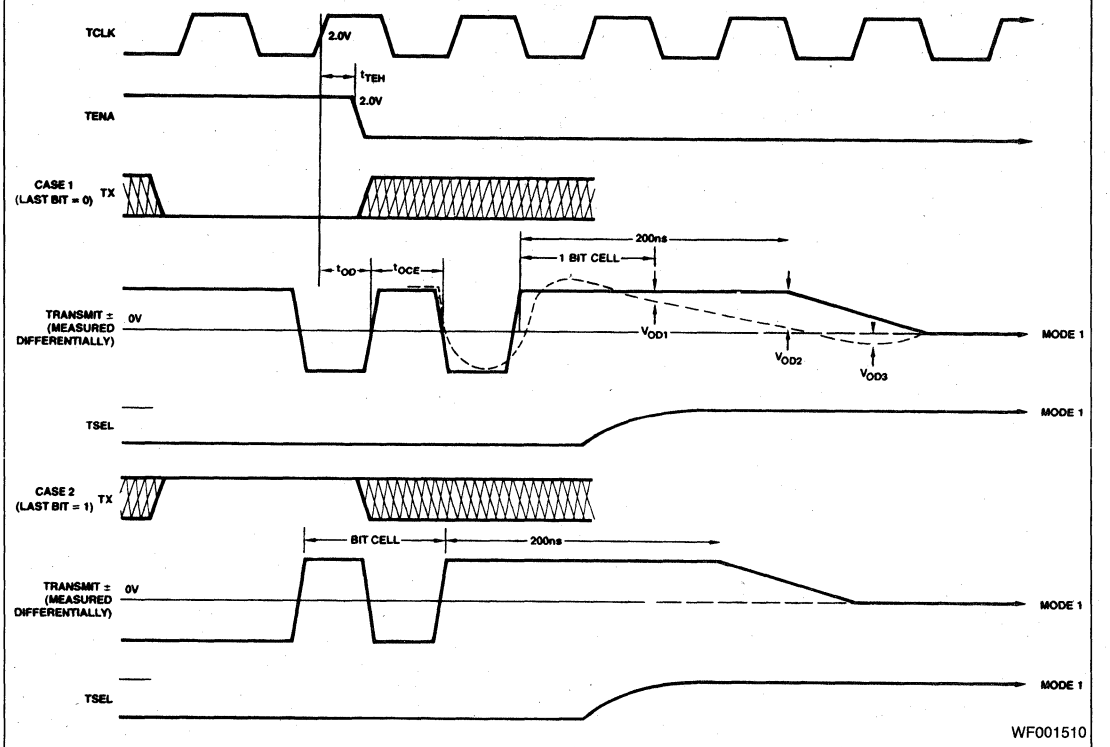
Figure 11b. Start of Transmit – Modes 1 and 2



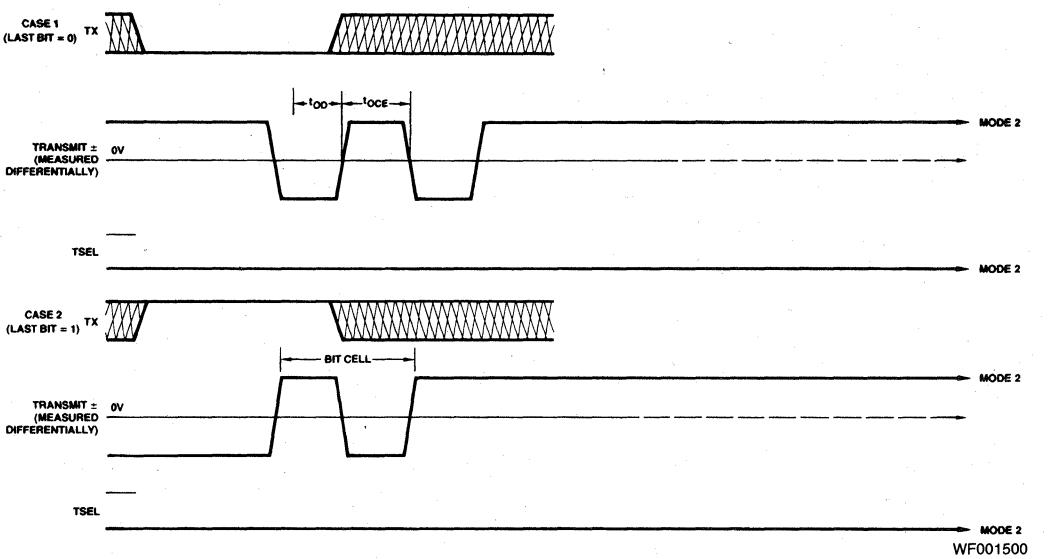
Note: 1. 25ns offset from TCLK (1/4 bit time and 3/4 bit time from TCLK position edge).

Figure 12. Transmitter Timing – End of Transmission

MODE 1

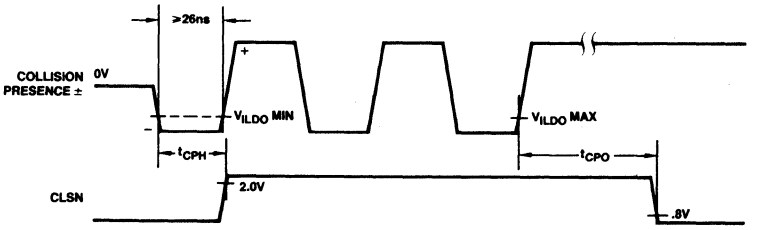


MODE 2



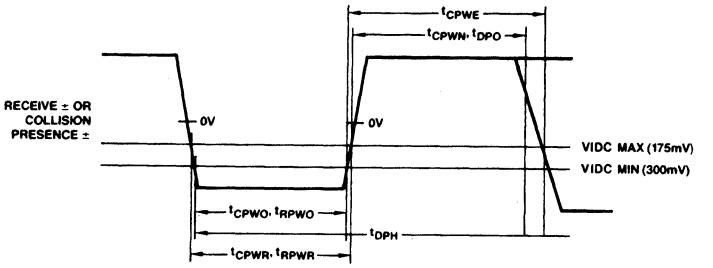
03378C

Figure 13. Collision Timing



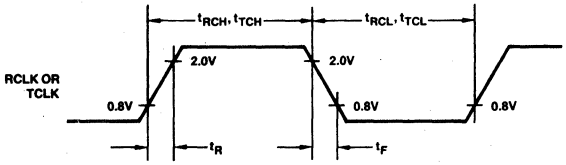
WF001720

Figure 14. Input Pulse Width Timing



WF001711

Figure 15. RCLK and TCLK Duty Cycle and Rise/Fall Time



WF002210

Am8120

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

GENERAL DESCRIPTION

The Am8120 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic $\bar{0}$ (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

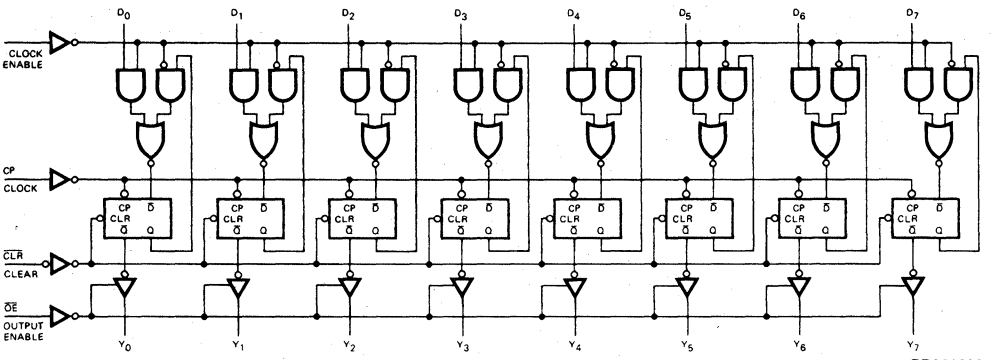
When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs.

When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a slim 24-pin package (0.3 inch row spacing).

BLOCK DIAGRAM



BD001280

RELATED PRODUCTS

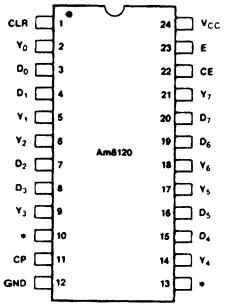
Part No.	Description
Am25S18	Quad D Register
Am2920	Octal D Type Flip-flop
Am2954/5	Octal D Registers

03696B

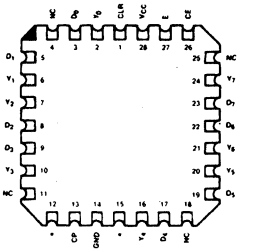
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

Leadless Chip Carrier
L-28-1



CD001560

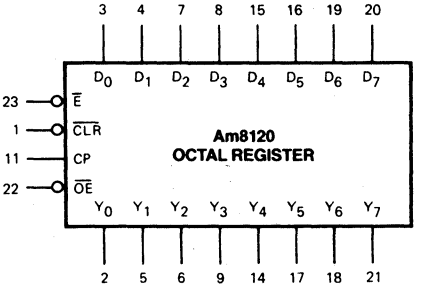


CD001570

Note: Pin 1 is marked for orientation

*Reserved – do not use.

LOGIC SYMBOL



LS000510

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am8120 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP (D-24-SLIM)
  - F– 24-pin ceramic flatpak (F-24-1)
  - L– 28-pin leadless chip carrier (L-28-1)
  - P– 24-pin plastic DIP (P-24-1)
  - X– Dice
- **Am8120** — Device type
  - Octal D-type Flip-flop

Valid Combinations	
Am8120	DC, DM FM LC, LM PC XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{CLR}$	I	When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.
11	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i	O	The register three-state outputs.
23	$\overline{E}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
22	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

Function Table

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i	Function
H	X	X	X	X	X	Z	Hi-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−20	μA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			24	37	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, D_i inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 15pF, R_L = 2.0kΩ		18	27	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y				22	35	ns
t_s	Data (D_i)			10	3		ns
t_h	Data (D_i)			10	3		ns
t_s	Enable ($\overline{E}$)	Active		15	10		ns
		Inactive		20	12		
t_h	Enable ($\overline{E}$)			0	0		ns
t_s	Clear Recovery (In-Active) to Clock			11	7		ns
t_{pw}	Clock	HIGH		20	14		ns
		LOW		25	13		
t_{pw}	Clear			20	13		ns
t_{ZH}	$\overline{OE}$ to Y_i				9	13	ns
t_{ZL}					14	21	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF, R_L = 2.0kΩ		20	30	ns
t_{LZ}					24	36	
f_{max}	Maximum Clock Frequency (Note 1)				40		MHz

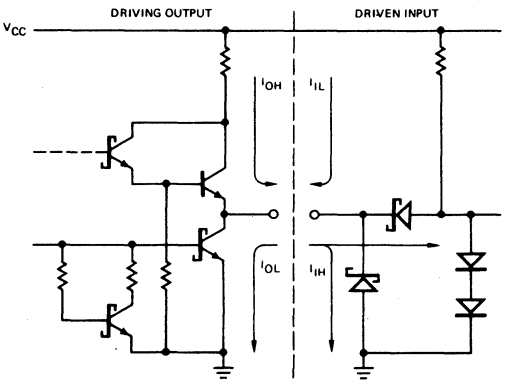
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)		C_L = 50pF, R_L = 2.0kΩ		33		39	ns
t_{PHL}					45		54	
t_{PHL}	Clear to Y				43		51	ns
t_s	Data (D_i)			12		15		ns
t_h	Data (D_i)			12		15		ns
t_s	Enable ($\overline{E}$)	Active		17		20		ns
		Inactive		20		23		
t_h	Enable ($\overline{E}$)			0		0		ns
t_s	Clear Recovery (In-Active) to Clock			13		15		ns
t_{pw}	Clock	HIGH		25		30		ns
		LOW		30		35		
t_{pw}	Clear			22		25		ns
t_{ZH}	$\overline{OE}$ to Y_i				19		25	ns
t_{ZL}					30		39	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF, R_L = 2.0kΩ		35		40	ns
t_{LZ}					39		42	
f_{max}	Maximum Clock Frequency (Note 1)			25		20		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

Am8127

AmZ8000 Clock Generator

DISTINCTIVE CHARACTERISTICS

- **High-drive high-level clock output**
  Special output provides clock signal matched to requirements of AmZ8000* CPU (4MHz and some 6MHz applications), MMU and DMA devices.
- **Synchronized $\overline{\text{WAIT}}$ state and time-out controls**
  On-chip logic generates $\overline{\text{WAIT}}$ signal under control of Halt, Single-step, Status and Ready signals. Automatic time-out of peripheral wait requests.
- **Four TTL-level clocks**
  Generates synchronized TTL compatible clocks at 16MHz, 2MHz and 1MHz to drive memory circuits and LSI peripheral devices. An additional TTL clock is synchronized with the CPU high-level clock for registers, latches and other peripherals.

GENERAL DESCRIPTION

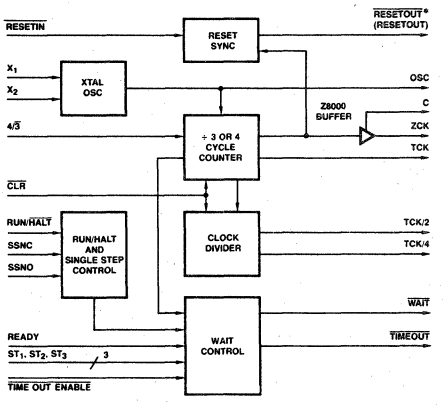
The Am8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001* and AmZ8002* CPUs, a standard buffered TTL 16MHz oscillator output is provided for a dynamic memory timing and control. In addition to 4MHz applications, the Am8127 will also function in some 6MHz Z8000 applications. The Am8127 forms an integral part of the dynamic memory support chip set including the Am8163 EDC and Refresh Controller, Am2964 Dynamic Memory Controller, Am2960 Error Detection and Correction Unit and Am2961/Am2962 EDC Bus Buffers. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The Am8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 4, 2 and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronization of the multiple clock outputs.

The controller functions include $\overline{\text{RESET}}$, RUN/$\overline{\text{HALT}}$, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's $\overline{\text{WAIT}}$ input is controlled by RUN/$\overline{\text{HALT}}$, Single-Step, Status and READY. When RUN/$\overline{\text{HALT}}$ is LOW the Am8127 drives the $\overline{\text{WAIT}}$ output LOW causing the CPU to add wait states (TW). The READY input is used by peripherals to request wait states. The active LOW input timeout enable, $\overline{\text{TOEN}}$, is used to force $\overline{\text{TIME-OUT}}$ LOW and WAIT HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST_1, ST_2 and ST_3 are decoded in the Am8127 to disable the $\overline{\text{TIMEOUT}}$ counter during CPU "Internal Operations" and during refresh.

The 4/3 input controls the clock duty cycle. An internal pull-up resistor pulls this input high for AmZ8000 CPUs. A LOW input causes the cycle counter to output a 33% duty cycle.

BLOCK DIAGRAM

CLOCK GENERATOR



BD001370

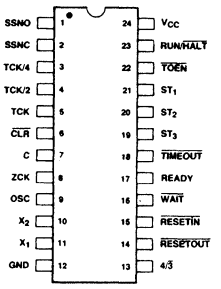
*$\overline{\text{RESETOUT}}$ is active LOW when 4/3 = HIGH

*Z8000, Z8001 and Z8002 are trademarks of Zilog, Inc.

03432C

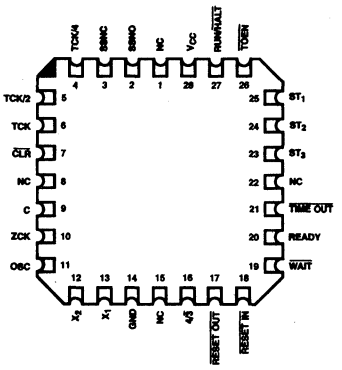
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



CD001850

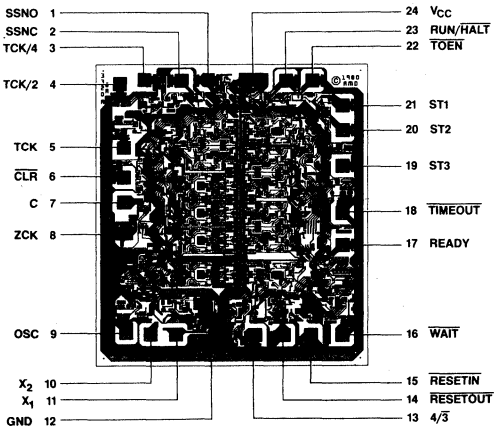
Leadless Chip Carrier



CD004890

24 Pin 0.3″ wide
Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.098″ x 0.088″

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am8127 **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 24-pin Ceramic SLIMDIP (D-24-SLIM); L – 28-pin Leadless Chip Carrier (L-28-1); X – Dice
- Am8127 — vice type: mZ8000 Clock Generator

Valid Combinations	
Am8127	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
8	ZCK	O	Buffered clock output for CPU and peripherals. This output has under/overshoot control and provides the high level output voltage required (V_{CC} – 0.4V). This output is capable of driving multiple CPU clock inputs (or DMA, MMU, etc).
7	C	I	Bootstrap input. The capacitor C_B is connected from the ZCK clock output to C to provide faster ZCK risetime.
5	TCK	O	TTL level buffered clock output. TCK is the same frequency as ZCK and is synchronized with ZCK. TCK is in phase with ZCK when the 4/$\overline{3}$ duty cycle control input is HIGH (50% duty cycle) and out of phase with ZCK when 4/$\overline{3}$ is LOW (33% ZCK duty cycle).
3, 4	TCK/2, TCK/4	O	TTL buffered clocks for peripherals. TCK/2 and TCK/4 are 1/2 and 1/4 the TCK frequency and are synchronized with the rising edge of TCK.
9	OSC	O	The clock oscillator TTL buffered output. This output provides a high speed clock for dynamic memory timing (e.g. AmZ8000 uses this output to generate $\overline{RAS}$/MUX-Select/$\overline{CAS}$ timing for dynamic RAMs) or other system application. The ZCK and TCK outputs are synchronized to the OSC rising edge.
13	4/$\overline{3}$	I	Clock duty cycle control for ZCK and TCK. A HIGH input (no connection – input has internal pull-up) will result in a 50% duty cycle for AmZ8000 application. A LOW input will cause a 33% duty cycle ZCK output.
6	$\overline{CLR}$	I	The clear active LOW input for internal counters. A LOW input meeting set-up and hold time requirements will clear the internal clock counters on the rising edge of OSC.
16	$\overline{WAIT}$	O	The $\overline{WAIT}$ output for connection to the CPU $\overline{WAIT}$ input. This latched output controls when the CPU enters wait states in response to the READY, ST_1, ST_2, ST_3, RUN/$\overline{HALT}$ and Single Step inputs.
17	READY	I	The active HIGH READY input is used by peripherals to request wait states. Ready inputs must meet the wait latch set-up and hold time requirements.
18	$\overline{TIMEOUT}$	O	The Timeout Counter active LOW output. The Timeout Counter counts ZCK/TCK clock cycles and is used to force $\overline{WAIT}$ HIGH 15 clock cycles after a peripheral has requested a wait but has failed to release the request. This output is normally used to interrupt the CPU.
22	$\overline{TOEN}$	I	The Timeout Enable active LOW input. A LOW input allows the Timeout Counter to count, causes the $\overline{TIMEOUT}$ output to go LOW for one ZCK/TCK clock period after 15 cycles and forces $\overline{WAIT}$ HIGH at the rising edge of the 16th cycle. A HIGH input disables the counter and allows $\overline{WAIT}$ to be controlled by the READY, RUN/$\overline{HALT}$ and Single Step inputs.
14	$\overline{RESET}$-$\overline{OUT}$ (RESET-OUT)	O	The Reset Output to the CPU. It is active LOW when the 4/$\overline{3}$ input is HIGH and active HIGH when the 4/$\overline{3}$ input is LOW.
15	$\overline{RESETIN}$	I	The active LOW Reset Input. A LOW input will cause $\overline{RESETOUT}$ to go LOW synchronous with ZCK ⌐¯. Pushbutton reset is implemented by momentarily grounding $\overline{RESETIN}$. Power-up reset is implemented by connecting a capacitor from $\overline{RESETIN}$ to ground. Capacitor values from 10μF to 22μF will provide a power-up of less than one second.
23	RUN/$\overline{HALT}$	I	A debounced input to allow halt and Single Step control modes. A HIGH input allows the CPU to run. A LOW input forces the $\overline{WAIT}$ output LOW causing the CPU to enter continuous wait states until the ZCK period after RUN/$\overline{HALT}$ is returned to HIGH.
1	SSNO, SSNC	I	Single Step control inputs. These debounced input allow the CPU to Single Step from one wait state to the next by momentarily disconnecting SSNC from ground and grounding SSNO. RUN/$\overline{HALT}$ must be LOW for Single Step operation.
19, 20, 21	ST_1, ST_2, ST_3	I	Status inputs from AmZ8000 CPU's and peripherals. Continuous LOW inputs indicate that the CPU is executing "internal operation" or "refresh." During this time the time out is disabled to avoid signaling an inappropriate interrupt. The status inputs are subject to the set-up and hold time requirements of the $\overline{WAIT}$ latch.
10, 11	X_1, X_2	I	External crystal connections (see application section). X_1 may be driven directly by a TTL input.

*$\overline{RESETOUT}$ is active LOW when 4/$\overline{3}$ = HIGH.

TYPICAL CRYSTAL SPEC

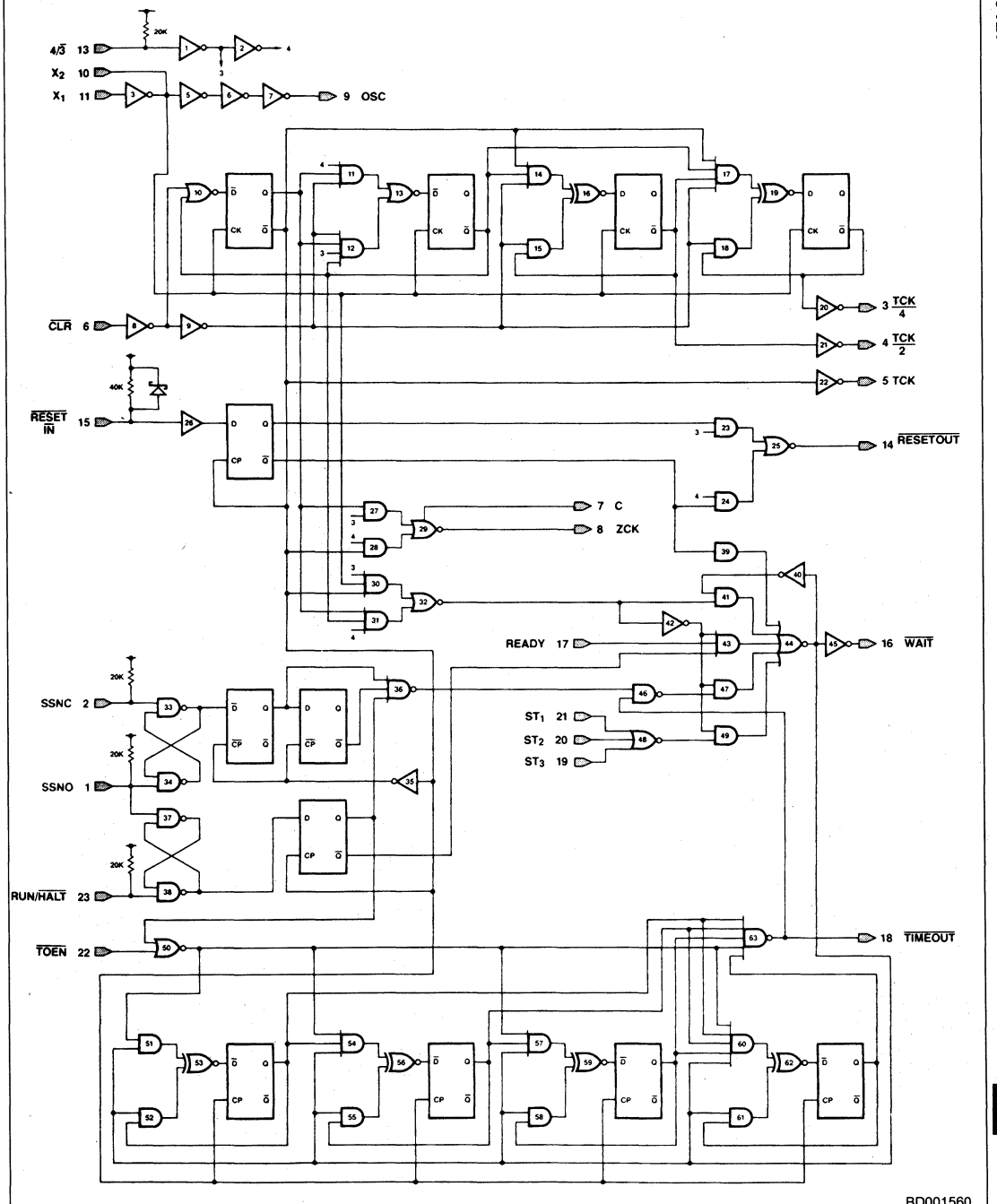
Mode	Fundamental AT cut
Resonance	Parallel or Series
Load	32pF (Net of 56pF C's shown + stray C)
Stability	±0.01% (or to user requirement)

$\overline{WAIT}$, $\overline{TIMEOUT}$ FUNCTION TABLE

RUN/$\overline{HALT}$	SSNC	ST_3	ST_2	ST_1	READY	$\overline{TOEN}$	$\overline{TIMEOUT}$ COUNTER	$\overline{TIMEOUT}$	$\overline{WAIT}$
H	X	L	L	L	H	X	Cleared	H	H
		L	L	L	L	X	Cleared	H	H
		Any ST_i = H			H	L	Cleared	H	H
					L	H	Hold	H	L
					L	L	Count +1 on ZCK ⌐¯	H until 16 clocks after ready ¯_, then LOW one ZCK period	L until 16 after ready \¯ HIGH one ZC
L	L	X			X	X	Hold	H	L
	H								HIGH c ZCK pe

Refer to Page 13-1 for Essential Informati

BLOCK DIAGRAM



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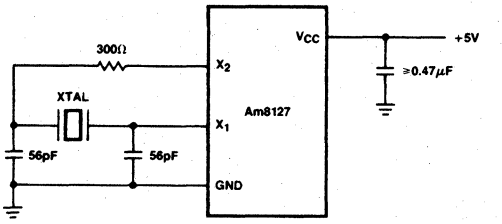
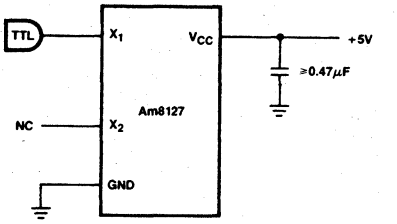
Refer to Page 13-1 for Essential Information on Military Devices

CRYSTAL CONTROLLED OSCILLATOR



DF000380

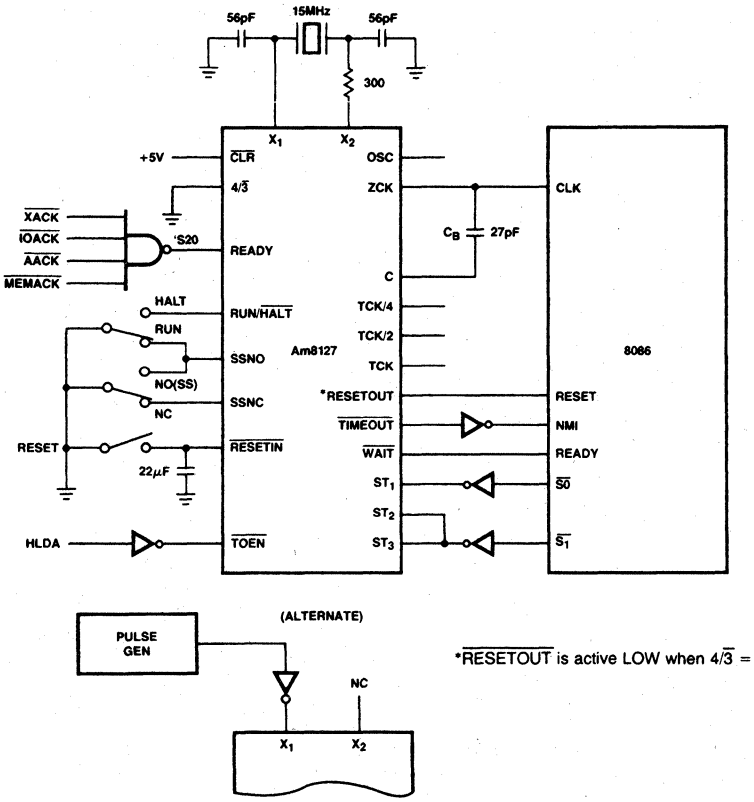
EXTERNAL CLOCK DRIVE



DF000370

AmZ8000 APPLICATION

(50% Duty Cycle ZCK)



*$\overline{\text{RESETOUT}}$ is active LOW when 4/$\overline{3}$ = HIGH

DF000350

The typical operating configuration for Am8127 is shown above. The component values shown provide a 4MHz clock output for the AmZ8002 CPU. The 27pF capacitor from C to ZCK is a bootstrap to ensure clock rise to V_{CC} −0.4V within the specified rise time. The 22μF reset capacitor is chosen to guarantee reset, plus adequate delay for reset during power-up with a slowly rising V_{CC} supply voltage. Ground SSNO if RUN/$\overline{\text{HALT}}$ or S-S isn't used.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage
X_1,4/$\overline{3}$, SSNO, SSNC, RUN/ $\overline{HALT}$ ..... −0.5V to V_{CC} +0.5V
Other Inputs ..... −0.5V to +5.5V
DC Voltage Applied to C ..... −0.5V to +8V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter	Description			Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN	ZCK	I_{OH} = −0.1mA		V_{CC}−0.4	V_{CC}−0.1		Volts
			TTL Outputs	I_{OH} = −1mA	MIL	2.4	3.4		Volts
				I_{OH} = −2.6mA	COM'L				
V_{OL}	Output LOW Voltage	V_{CC} = MIN		I_{OL} = 0.1mA, ZCK Output				0.4	Volts
				I_{OL} = 16mA, TTL Output				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input HIGH Voltage		$\overline{RESETIN}$		2.8	2.25		Volts
				$\overline{ST_1}$, $\overline{ST_2}$, $\overline{ST_3}$, $\overline{CLR}$, $\overline{TOEN}$, X_1, READY		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input LOW Voltage		$\overline{ST_1}$, $\overline{ST_2}$, $\overline{ST_3}$. CLR, $\overline{TOEN}$, X_1, READY				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA (Note 3)						−1.5	Volts
V_{IN}–V_{IL}	$\overline{RESETIN}$ Hysteresis	V_{CC} = MIN				400	650		mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		SSNO				−1.6	mA
				SSNC, 4/$\overline{3}$, RUN/$\overline{HALT}$, READY				−1.2	mA
				$\overline{TOEN}$, $\overline{CLR}$, X_1				−0.72	mA
				$\overline{RESETIN}$, $\overline{ST_1}$, $\overline{ST_2}$, $\overline{ST_3}$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		4/$\overline{3}$, SSNC, SSNO RUN/$\overline{HALT}$			(Note 4)	−300	µA
				$\overline{RESETIN}$			(Note 4)	−200	µA
				$\overline{CLR}$, READY, $\overline{TOEN}$ $\overline{ST_1}$, $\overline{ST_2}$, $\overline{ST_3}$				+50	µA
				X_1				+600	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{CLR}$, READY, $\overline{TOEN}$ $\overline{ST_1}$, $\overline{ST_2}$, $\overline{ST_3}$				+1.0	mA
I_{SC}	Output Short Circuit Current (Note 5)	V_{CC} = MAX		ZCK Output		−50		−240	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		X_1 = 2.4V, ZCK = TCK's = LOW			95	140	mA
				Operating, f_{OSC} ≤ 24MHz (Note 6)			120	180	

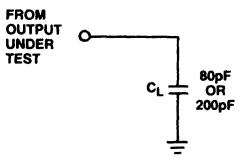
Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not applicable to X_1.
4. Specification is negative because of internal input pull-up resistors.
5. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
6. For oscillator frequencies up to 24MHz, outputs open.

STATIC INPUT ELECTRICAL CHARACTERISTICS

The static control inputs, SSNO, SSNC (Single Step), RUN/$\overline{\text{HALT}}$ and 4/$\overline{3}$ (clock duty cycle control), are Low-Power Schottky TTI compatible inputs with internal pull-up resistors to the +5V supply. They may be left open for a HIGH input (e.g., 4/$\overline{3}$ is left open for operation with AmZ8001/8002), or grounded for a LOW input. SSNO, SSNC and RUN/$\overline{\text{HALT}}$ are intended to be grounded or opened by switches. 4/$\overline{3}$ is normally left open for AmZ8001/8002. These inputs are specified at 0.4V/2.4V for test convenience.

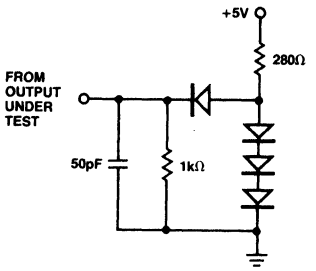
Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH input voltage	RUN $\overline{\text{HALT}}$, SSNO	2.4			Volts
V_{IL}	Input LOW Voltage	Guaranteed LOW input voltage	SSNC,4/$\overline{3}$			0.4	Volts

SWITCHING TEST CIRCUIT



TC000690

ZCK Output

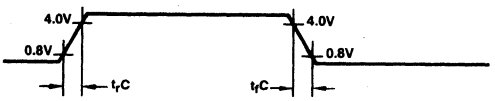


TC000700

TTL Outputs

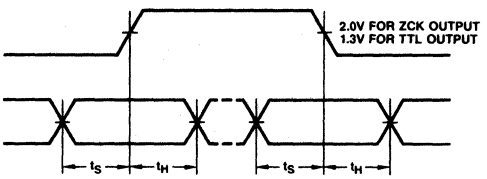
SWITCHING TEST WAVEFORMS

ZCK RISE AND FALL TIMES



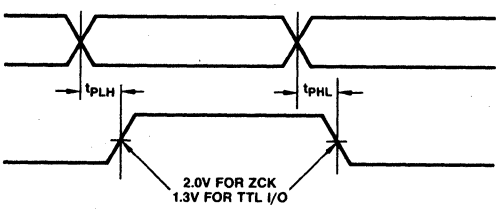
WF002190

SET-UP AND HOLD TIMES



WF001900

PROPAGATION DELAY TIMES



WF001890

SWITCHING CHARACTERISTICS —OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUT

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
f_{MAX}	Oscillator Frequency		See Test Circuits (Note 7)	24			MHz
t_{rC}	ZCK Rise Time	C_L = 80pF	ZCK C_L = 80pF (Note 8)		9	14	ns
t_{fC}	ZCK Fall Time				7.6	11	ns
t_{rC}	ZCK Rise Time	C_L = 200pF	ZCK C_L = 200pF (Note 8)		15.4	20	ns
t_{fC}	ZCK Fall time				14.0	20	ns
t_{PLH}	READY to $\overline{WAIT}$		See Test Circuits		8	14	ns
t_{PHL}					11.5	16	ns
t_{PLH}	Status ST_i to $\overline{WAIT}$				13	17	ns
t_{PHL}					17.2	21	ns
t_S	$\overline{CLR}$ to OSC (⎍) Setup Time				15	18	ns
t_H	$\overline{CLR}$ to OSC (⎍) Hold Time				−11	−6	ns

Notes: 7. Specification is based on fundamental mode crystal. See application section.
8. ZCK rise and fall times are based on a bootstrap capacitor value of 27pF.

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SWITCHING CHARACTERISTICS — 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_S	READY to ZCK Set-up Time	(Note 9)	See Test Circuits ZCK C_L = 80pF	T/4 + 10	T/4 + 4.5		ns
t_H	READY to ZCK Hold Time			T/4 + 2	T/4		ns
t_S	Status ST_i to ZCK Set-up Time			T/4 + 12	T/4 + 9.5		ns
t_H	Status ST_i to ZCK Hold Time			T/4 - 3	T/4 - 7.5		ns
t_S	$\overline{TOEN}$ to ZCK Set-up Time			30	22		ns
t_H	$\overline{TOEN}$ to ZCK Hold Time			-10	-16		ns
t_{SKEW}	ZCK to OSC			3	6	10	ns
t_{SKEW}	ZCK to TCK			0	4.0	7	ns
t_{PLH}	ZCK to $\overline{RESET\ OUT}$ Propagation Delay				9.0	13	ns
t_{PHL}					4	8	ns

Note: 9. T = ZCK period.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE — OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUTS*

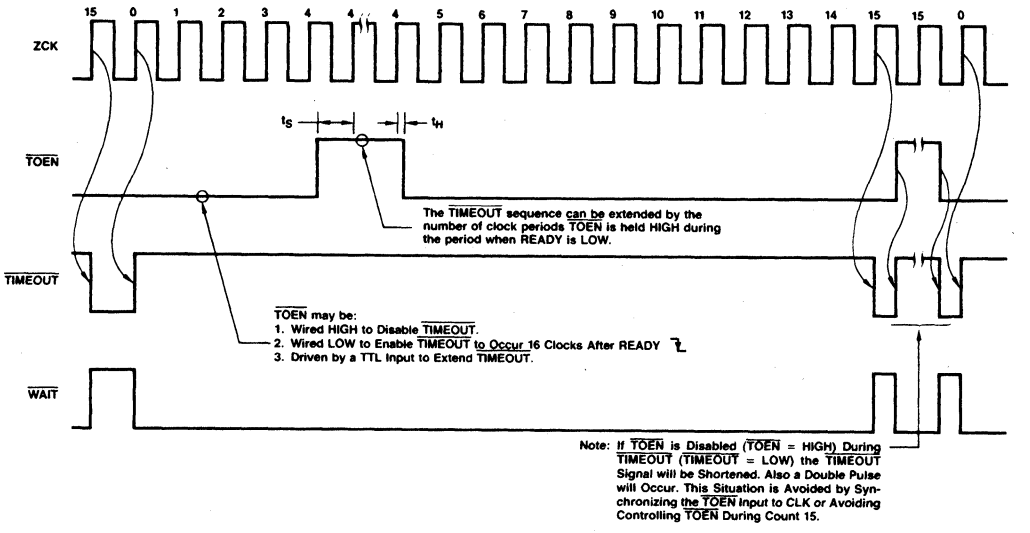
Parameters	Description		Test Conditions	COMMERCIAL Min	COMMERCIAL Max 0°C	COMMERCIAL Max 70°C	MILITARY Min	MILITARY Max -55°C	MILITARY Max 125°C	Units
t_{MAX}	Oscillator Frequency		(Note 7)	24			24			MHz
t_{rC}	ZCK Rise Time	C_L = 80pF	C_L = 80pF (Note 8)		15	15		20	15	ns
t_{fC}	ZCK Fall Time				14	14		20	14	ns
t_{rC}	ZCK Rise Time	C_L = 200pF	C_L = 200pF (Note 8)		25	20		32	20	ns
t_{fC}	ZCK Fall time				25	20		32	20	ns
t_{PLH}	READY to WAIT Propagation Delay		See Test Circuits		17	17		19	19	ns
t_{PHL}					19	19		19	19	ns
t_{PLH}	Status ST_i to $\overline{WAIT}$ Propagation Delay				20	20		22	22	ns
t_{PHL}					25	25		25	25	ns
t_S	$\overline{CLR}$ to OSC (↓) Setup Time			21			30			ns
t_H	$\overline{CLR}$ to OSC (↓) Hold Time			-3			0			ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE — 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

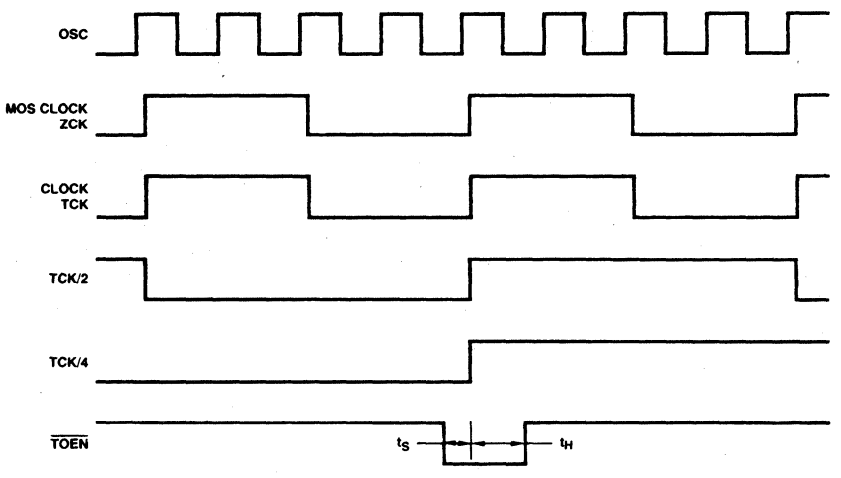
Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_S	READY to ZCK Setup Time	See Test Circuits ZCK, C_L = 80pF	T/4 + 14		T/4 + 17		ns
t_H	READY to ZCK Hold Time		T/4 + 5		T/4 + 5		ns
t_S	Status ST_i to ZCK Setup Time		T/4 + 15		T/4 + 20		ns
t_H	Status ST_i to ZCK Hold Time		T/4		T/4 + 5		ns
t_S	$\overline{TOEN}$ to ZCK Setup Time		35		40		ns
t_H	$\overline{TOEN}$ to ZCK Hold Time		-5		0		ns
t_{SKEW}	ZCK to OSC Skew		2	14	2	17	ns
t_{SKEW}	ZCK to TCK Skew		-2	10	-2	14	ns
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay			16		20	ns
t_{PHL}				16		20	ns

$\overline{\text{TIMEOUT}}$ COUNTER TIMING



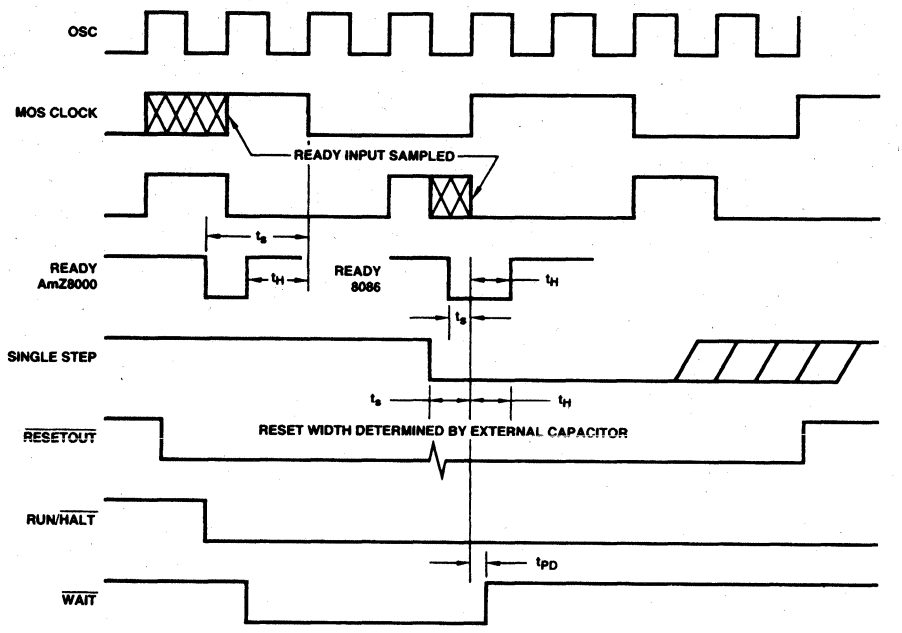
WF002020

Am8127 CLOCK OUTPUTS
DIVIDE BY 4 MODE (AmZ8000)



WF002030

Am8127 READY, WAIT, RESET, AND SINGLE STEP



WF002010

Am8152A/53A

Video System Controller (VSC)

DISTINCTIVE CHARACTERISTICS

- Proportional Spacing Support (2–17 dots)
- 9-bit dot data parallel input, with expansion capability to seventeen bits
- Trailing blanks (0–3 dots)
- Buffered and Synchronized Vertical and Horizontal Sync Outputs are Character Clock Outputs
- Attribute Support:
  - Character Blink
  - Underline
  - Overstrike
  - Reverse
  - Highlight
- Background color selection

GENERAL DESCRIPTION

The Am8152A/53A Video System Controller (VSC) provides interface between a CRT controller and a CRT monitor. The basic chip functions are:

- Support proportional and non-proportional character display
- Correctly synchronize and mix character attributes with video signals
- Output the video information in a four-level analog or digital format

The VSC consists of a parallel-to-serial converter which provides a video bit stream to on-chip attribute logic. This logic, under control of the attribute inputs, operates on the bit stream to generate grey scale video. Video outputs from the VSC are of two forms — analog and digital. The digitally encoded outputs implement four video levels: Blank, Black, Grey and White. Identical information is available in analog form via differential outputs (current driven) into a nominal 75Ω impedance.

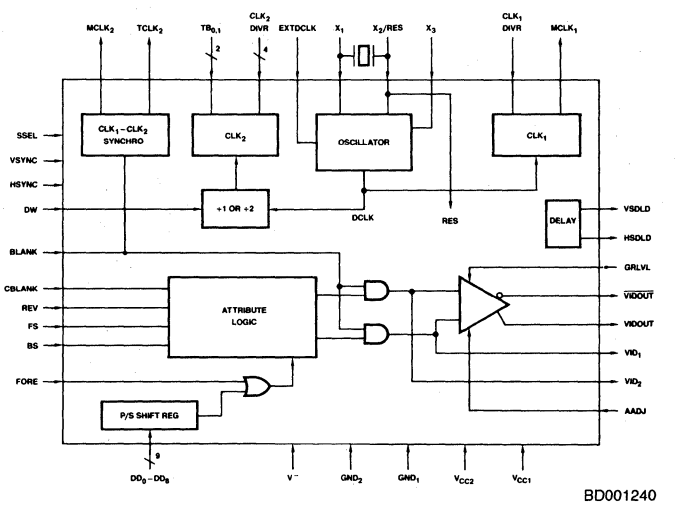
The Am8152A/53A also supports proportional spacing using a bit width programmable character clock. Character ROM pixel information is selectable from two to seventeen pixels per character. Up to three blank pixels can be appended to the character ROM input thereby facilitating right justification of text.

The difference between the Am8152A and the Am8153A is in the output scheme. The Am8152A has standard TTL outputs and operates in the 25 – 60MHz range, while the Am8153A has 10K ECL outputs and operates in the 40 – 100MHz range.

The Am8152A/53A is fabricated using AMD's advanced bipolar process with internal ECL logic. The device is available in conventional 48-pin dual in-line packages.

BLOCK DIAGRAM

Figure 1.



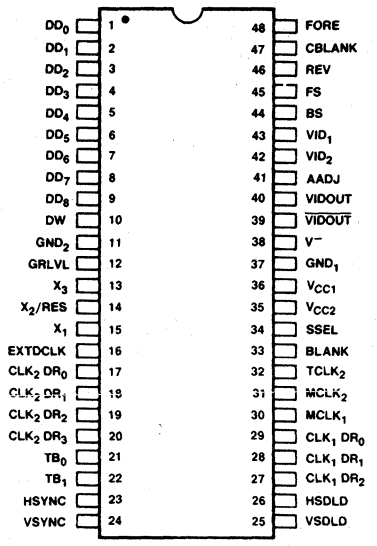
BD001240

Chip Pak is a trademark of Advanced Micro Devices, Inc.

03888C

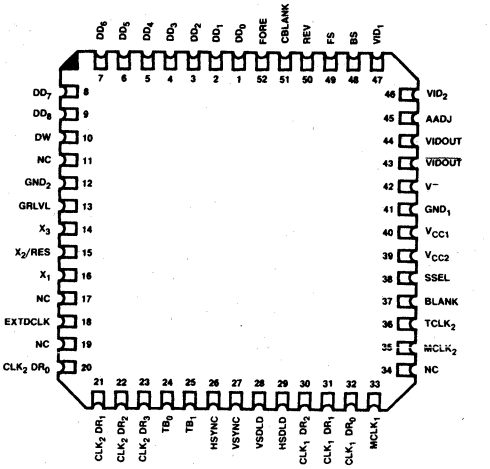
CONNECTION DIAGRAM
Top View

D-48-1



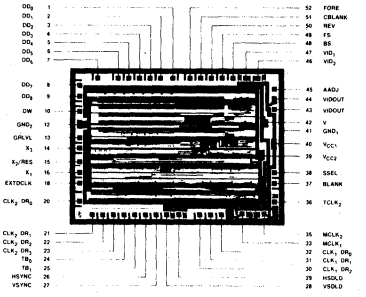
CD001510

Leadless Chip Carrier
L-52-1



CD004920

METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am8152A/53A P C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (−55°C to +125°C)
- P — Package
  - D – 48 pin CERDIP (D-48-1)
  - L – 52 Pin Leadless Chip Carrier (L-52-1)
  - X – Dice
- Am8152A/53A — Device type
  - Video System Controller

Valid Combinations	
Am8152A/53A	DC, DCB DM, DMB LC, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

$MCLK_1$ **$CLOCK_1$ (output, non-TTL compatible)**
$MCLK_1$ is a system clock. It is intended to drive the Am8052 horizontal and vertical timing circuitry as well as the DMA operations. $MCLK_1$ output is nominally a square wave divided down from the internal dot clock frequency according to the CLK_1 DR (CLK_1 Divide Ratio) input.

CLK_1 DR **CLK_1 DIVIDE RATIO (inputs (3))**
CLK_1 DR are three inputs which control the $MCLK_1$ divide ratio. The three inputs may be programmed to divide the $MCLK_1$ signal by two, four, six, ..., sixteen.

CLK_1 DR				
2	1	0	A(1)	B(1)
L	L	L	1	1
L	L	H	2	2
L	H	L	3	3
L	H	H	4	4
H	L	L	5	5
H	L	H	6	6
H	H	L	7	7
H	H	H	8	8

$MCLK_2$ **$CLOCK_2$ (output, non-TTL compatible)**
$MCLK_2$ is a character display clock. Its function is to control the character code and attribute data output rate from the appropriate Am8052 CRTC's ports.

CLK_2DR **$CLOCK_2$ DIVIDE RATIO (inputs (4))**
CLK_2 DR are four inputs which control an internal divider to divide the dot clock frequency by a value from two to seventeen.

CLK_2 DR					
3	2	1	0	C(1)	D(1)
L	L	L	L	1	1
L	L	L	H	1	2
L	L	H	L	2	2
L	L	H	H	2	3
L	H	L	L	3	3
L	H	L	H	3	4
L	H	H	L	4	4
L	H	H	H	4	5
H	L	L	L	5	5
H	L	L	H	5	6
H	L	H	L	6	6
H	L	H	H	6	7
H	H	L	L	7	7
H	H	L	H	7	8
H	H	H	L	8	8
H	H	H	H	8	9

Note 1: A, B, C, and D are measured in EXTDCLK periods.
(See Reset Timing on page 15).

$TCLK_2$ **TTL $CLOCK_2$ (output)**
$TCLK_2$ is a TTL compatible version of $MCLK_2$.

X_1, X_2/RES **X_1, X_2/RESET (inputs, X_2 is non-TTL compatible, reset is TTL compatible)**
X_1, X_2/RES are the external crystal inputs when the on-chip oscillator of the VSC is being used. The external crystal frequency is multiplied by five to produce the on-chip dot clock. If the external dot clock option is used, the X_1 should be tied LOW and X_2/RES may be used as a reset input, to synchronize multiple VSC's. Note that the reset signal should be synchronous to the external dot clock.

X_3 **X_3 (input, non-TTL compatible)**
X_3 is used as an input to the on-chip voltage-controlled oscillator. When the on-chip oscillator of the VSR is being used, X_3 should be connected to ground by an appropriate capacitor. If the external dot clock option is used, X_3 and X_1 should be tied LOW.

VSYNC **VERTICAL SYNC (input)**
VSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent on the SSEL input. If SSEL is HIGH, VSYNC must be synchronous to $MCLK_1$.

VSDLD **VERTICAL SYNC DELAYED (output)**
VSDLD is the delayed output of VSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending on the setting of SSEL.

HSYNC **HORIZONTAL SYNC DELAYED (input)**
HSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent upon the SSEL input. If SSEL is LOW, HSYNC must be synchronous to $MCLK_2$; if SSEL is HIGH, HSYNC must be synchronous to $MCLK_1$.

HSDLD **HORIZONTAL SYNC (output)**
HSDLD is the delayed output of HSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending upon the setting of SSEL.

SSEL **SYNC SELECT (input)**
The SSEL line determines if the VSYNC, HSYNC and BLANK are going to be synchronized to the $MCLK_1$ or $MCLK_2$ signals. A HIGH on SSEL also will resynchronize CLK_2 and CLK_1 during blanking.

CBLANK **CHARACTER BLANK (input)**
CBLANK forces video output levels (VID_1, VID_2, VIDOUT and VIDOUT) to switch to the background color level.

BLANK — **BLANK (input)**
BLANK is an input normally synchronous to $MCLK_1$, although it may be synchronous to $MCLK_2$ in non-proportional spacing applications. The active pulse width of BLANK will usually overlap the inactive-to-active waveforms of HSYNC and VSYNC, as well as the active-to-inactive portion of VSYNC. While BLANk is active $TCLK_2/MCLK_2$ may be forced to synchronize to the $MCLK_1$ clock. When BLANK goes inactive, the rising edges of $MCLK_1$ and $TCLK_2/MCLK_2$ must be synchronized in order to prevent "dot walk" in proportional spacing applications. BLANK active also forces the video output level to "blank" regardless of DD, FORE or other inputs.

FORE — **FOREGROUND VIDEO (input)**
The FORE video input is "OR'ed" with the dot data output by the parallel-to-serial shift register to switch to the foreground color level (e.g., to implement underlines).

$\overline{REV}$ — **REVERSE (input)**
The REV input causes the foreground color levels to be transposed with the background color level for the total character period (including any tracking blanks).

FS — **FOREGROUND SHIFT (input)**
The FS input causes the shift in the video output levels to produce a highlight effect. See Table 1.

TB_0, TB_1 — **TRAILING BLANKS (inputs (2))**
The TB inputs concatenate "blank" video dots to the tail end of the dot data contained in the parallel-to-serial shift register. TB can be specified to concatenate 0, 1, 2 or 3 dots. The TB value is also added to the CLK_2 DR value to obtain the total. The combination of all CLK_2DR inputs being High (17 dots) and both TB inputs being High (3 trailing blanks) is not allowed. The maximum CLK_2 period is 19 dot periods.

$DD_0 - DD_8$ — **DOT DATA (inputs (9))**
The DD inputs accept parallel character dot matrix information for serial conversion for video output. DD data is accepted at the $TCLK_2/MCLK_2$ clock rate. DD_0 is shifted out first.

BS — **BACKGROUND SELECT (input)**
The BS input specifies the color level of the background video. This input can be overridden by BLANK active.

VIDOUT, $\overline{VIDOUT}$ — **VIDEO OUTPUT**
(analog outputs (2), non-TTL compatible)
VIDOUT and $\overline{VIDOUT}$ outputs in a differential mode the composite blank, and video dot levels to a nominal 75Ω load impedance from switched current sources.

VID_1, VID_2 — **VIDEO DIGITAL**
(outputs (2), (8152A-TTL; 8153A-ECL)
VID_1 and VID_2 are digitally encoded outputs of the video out. VID_1 is the least significant bit. Encoding is as follows:

	VID_2 (VIDEO)	VID_1 (HIGHLIGHT)
Blank Level	0	0
Black	0	1
Grey	1	0
White	1	1

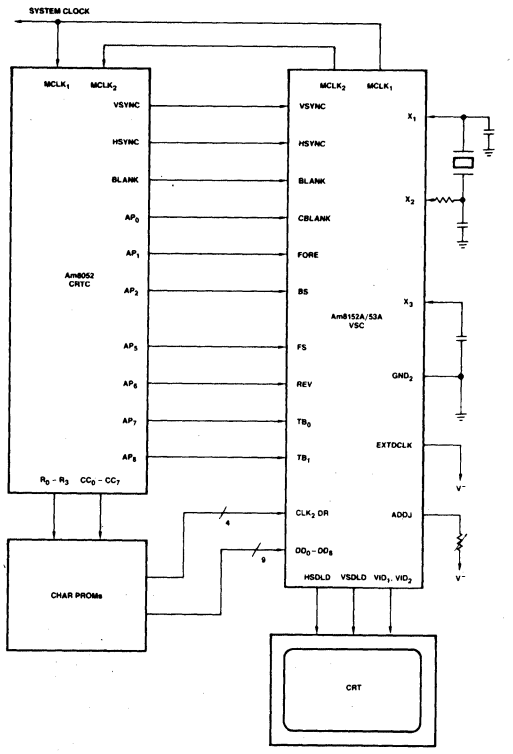
GRLVL — **GREY LEVEL (input)**
The GRLVL input adjusts the current level output, via the VIDOUT and $\overline{VIDOUT}$ outputs, of the grey video level. There are two pre-selected grey levels; for GRLVL HIGH grey is brighter, for LOW grey is darker.

DW — **DOUBLE WIDTH (inputs)**
The DW input, when active HIGH, causes the dot clock supplied to the $TCLK_2/MCLK_2$ clock divide to be divided by two. This function is used to facilitate doubling the width of a character cell matrix in the horizontal direction. The trailing blank information is also widened during a double width character.

EXTDCLK — **EXTERNAL DOT CLOCK**
(input, 8152A-TTL; 8153A-ECL)
EXTDCLK is an external, TTL or ECL compatible dot clock input for use in multiple Am8152A/53A configurations. This signal replaces the internal oscillator function. To enable EXTDCLK both X_1 and X_3 must be grounded.

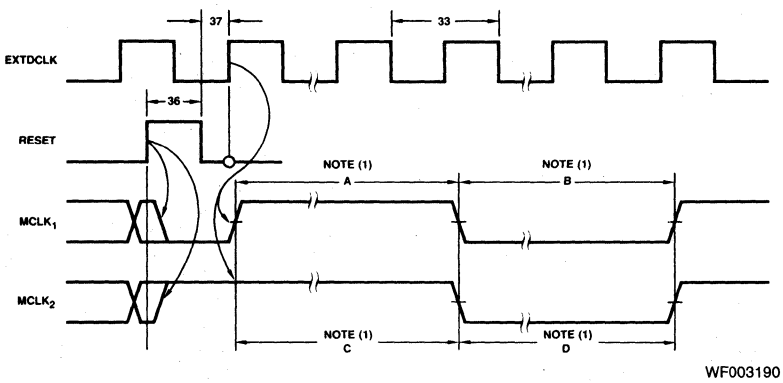
AADJ — **ANALOG OUTPUTS CURRENT ADJUST**
(input, non-TTL compatible)
Analog output current adjust is used for setting the analog video output current to 13.3mA. This is done by connecting AADJ to V^- via an applicable 1% resistor.

Figure 2. Am8152/53A Application with Am8052 CRT Controller



AF002100

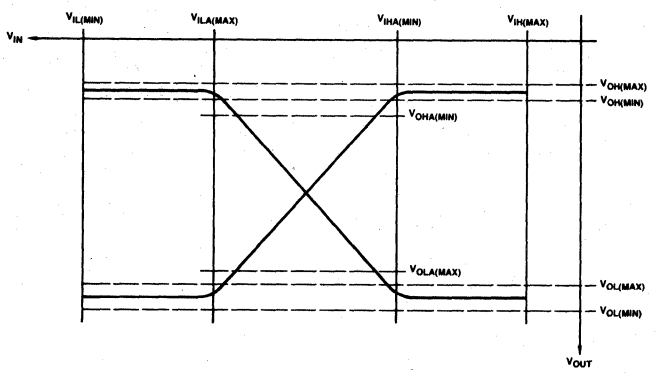
RESET TIMING FOR Am8152A/53A



WF003190

Note 1. See pin description

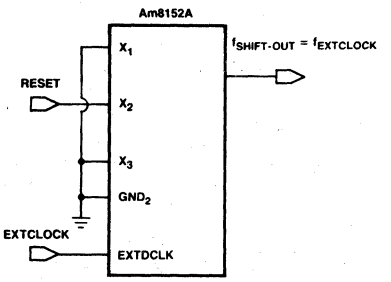
Am8153A 10K ECL SPECIFICATIONS



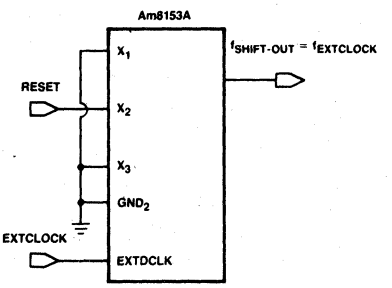
WF003200

DOTCLOCK GENERATION MODE

EXTERNAL CLOCK FLOW THROUGH MODE

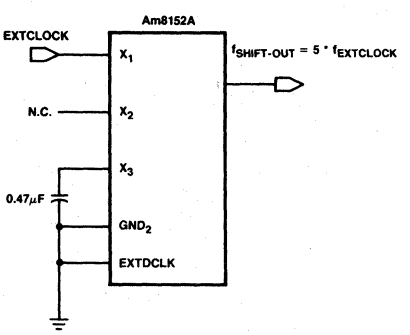


AF002140

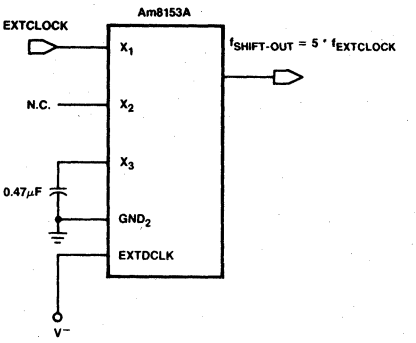


AF002110

EXTERNAL CLOCK MULTIPLIER MODE

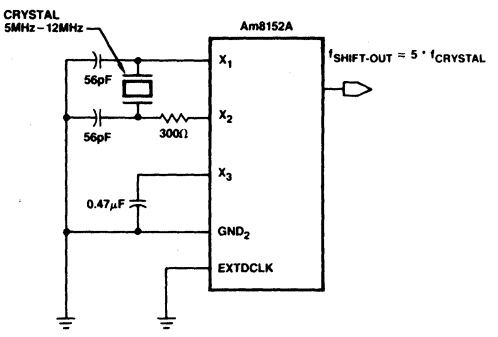


AF002150

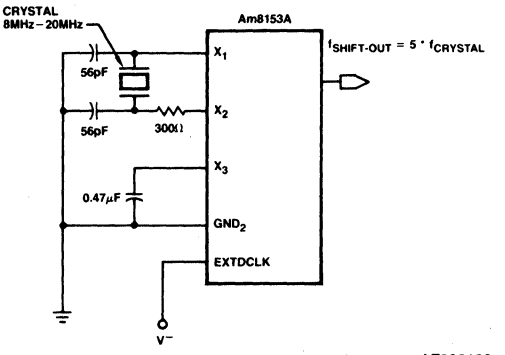


AF002120

CRYSTAL OSCILLATOR MULTIPLIER MODE



AF002160



AF002130

FUNCTIONAL DESCRIPTION

The Am8152A Video System Controller (VSC) supports both black and white and color video applications for CPUs, CRT controllers, and terminals. The essential functions of the VSC are to support proportional and non-proportional character display, to synchronize and mix character attributes with video, and to output the video in a four level analog or digital format.

PARALLEL PIXEL LOADING

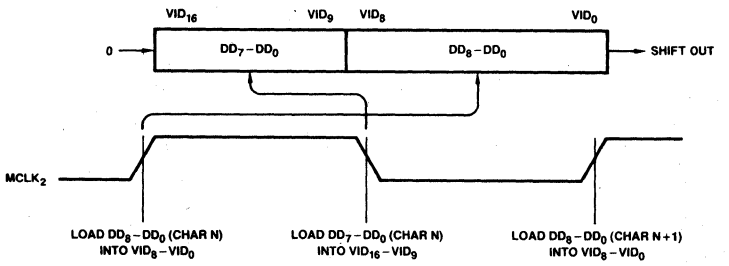
Pixel information that must be serialized for video transmission is loaded into the serial shift register via inputs $DD_0 - DD_8$. Information is loaded on both edges of the $MCLK_2$ character clock, as shown in Figure 3. The information set up on DD(0:7) prior to the falling edge of $MCLK_2$ is loaded into positions $VID_9 - VID_{16}$. Note that DD_8 information is ignored. Information set up on DD(0:8) prior to the rising edge of $MCLK_2$ is loaded into positions $VID_0 - VID_8$. Thus, up to 17 bits of pixel information can be loaded into the shift register. Note that if the character width is nine pixels or less the information captured on the falling edge of the $MCLK_2$ is not used. Any trailing blank insertion only occurs after the total number of pixels for the character have been transmitted. CLK_2DR (0:3) and TB (0:1) determine the divide ratio for the character clock. The sum of both values specifies the character clock period in dot clocks. During the trailing blank, the VSC shifts out what was loaded into the shift register. Therefore, it is the responsibility of the user to insure that the pixels output during the trailing blank dot period are set to the blank level.

VIDEO OPERATION

Parallel video data is obtained from the character ROM inputs; bits are shifted out serially and mixed with attribute information such as underline, shifted underline, and any other video sources. Video is internally encoded into one of four levels: White, Grey, Black and Blank. White is the highest analog current level, and Blank is the lowest. This information is then output through two ports (see Figure 5/6). One port provides a single current source output into a 75Ω impedance and the second port outputs either encoded TTL or ECL video on two pins.

There are two distinct blank inputs to the Am8152A/53A. BLANK is the CRTC's horizontal and vertical retrace period input which causes a blank output level to the display. CBLANK is an attribute input to selectively blank a character cell by forcing the video information for the particular character cell period to switch to the selected background color level.

Figure 3. Shift Register Loading



DF000940

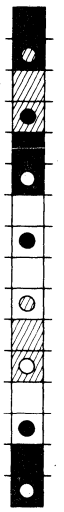
11

VIDEO INPUTS/OUTPUTS

Video information may be input in a number of different ways. Table 1 depicts all the combinations of video outputs achievable with each of the various inputs. The background color is determined by a separate pin input allowing either a black or white background. Using the REVERSE VIDEO (REV) input, a grey background can also be selected. The foreground then becomes black or white according to the signal on the foreground SHIFT line. Foreground and video sums can be modified depending on the combination of background, foreground shift, and reverse inputs. The user may apply any of his video inputs to the foreground to obtain a desired effect.

TABLE 1. Am8152A/53A VIDEO ATTRIBUTES

INPUTS				Am8152A/53A VIDEO ATTRIBUTES
BS	FS	REV	$\overline{\text{CBLANK}}$ (DD (0 : 8) + FORE)	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



TB4

SYSTEM TIMING

The CPU clock ($MCLK_1$) output is derived from an on-board oscillator by an externally programmable divide by two or three prescaler and a one to eight decoder. The internal oscillator is capable of operating a frequency of up to 100MHz and in a fundamental or third harmonic mode. Figure 4 shows the output waveform of $MCLK_1$ and $MCLK_2$.

The character clock ($MCLK_2$) output to the CRTC is frequency modulated according to the chosen number of dots per character cell. The duty cycle of $MCLK_2$ is 50% (±1 dot clock period) and is derived from an internal crystal driven oscillator whose divide ratio is set by the width of the character ROM plus the number of trailing blanks. A double width input further modifies $MCLK_2$ doubling the character width. During an active BLANK input $MCLK_2$ is internally re-synchronized to $MCLK_1$. This action aligns character cells at the left-end side of the display thereby eliminating "Dot Walk." The Vertical and Horizontal Sync (VSYNC, HSYNC) inputs from the CRT controller are buffered and delayed by a $MCLK_1$ or $MCLK_2$ clock period in order to phase correctly with the character video output.

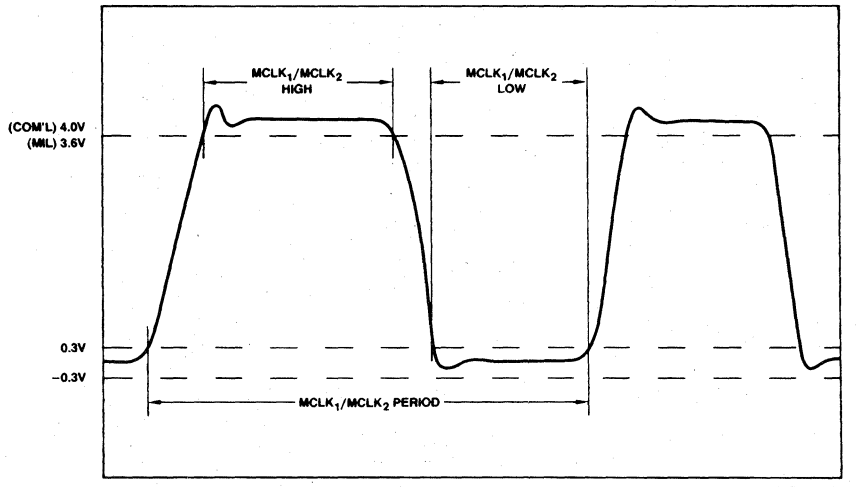
PROPORTIONAL/VARIABLE SPACING

Proportional spacing is achieved by programming on a character-by-character basis, a number of two to twenty dot clock periods per character. The character ROM pixel information is selectable from two to seventeen per character. Up to three trailing blank pixels can be concatenated to the character ROM input, making it easier to provide a straight right margin for right justification of text.

COLOR APPLICATION

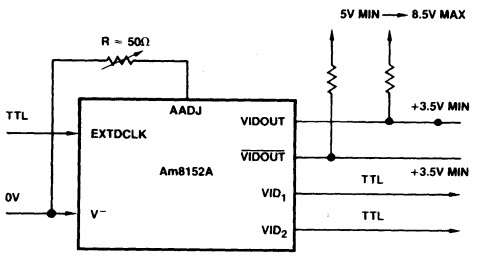
The Am8152A/53A may be used for many high-end color display applications. The foreground video and background information is mixed by the Am8152A/53A, and the encoded TTL video output can be used externally to select a color mix for the particular pixel being displayed. The horizontal and vertical synchronization, and video blank is output by the Am8152A/53A.

Figure 4. $MCLK_1/MCLK_2$ Output Waveform



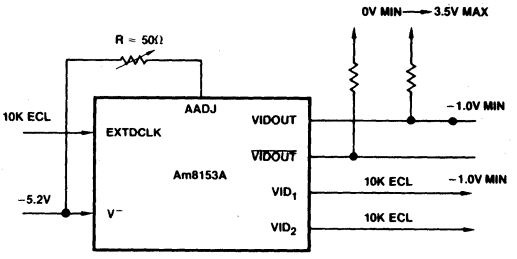
WF001730

Figure 5. Analog Video Outputs and Digital Video Outputs for Am8152A



DF000950

Figure 6. Analog Video Outputs and Digital Video Outputs for Am8153A



DF000960

ANALOG ELECTRICAL CHARACTERISTICS (see notes)

The following conditions apply unless otherwise specified:
COM'L $T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Min = 4.75V Max = 5.25V) Am8152A: $V^- = 0V$ Am8153A: $V^- = -5.2V \pm 5\%$
MIL $T_C = -55$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Min = 4.50V Max = 5.50V) $V^- = 0V$ $V^- = -5.2V \pm 10\%$

Grey Level	VID_2	VID_1		VIDOUT		$\overline{VIDOUT}$	
				Min (%)	Max (%)	Min (%)	Max (%)
X	I	I	I_{White}	0	0	100	100
I	I	O	I_{Grey1}	37	44	56	63
O	I	O	I_{Grey2}	45	53	47	55
X	O	I	I_{Black}	90.5	92.5	7.5	9.5
X	O	O	I_{Blank}	100	100	0	0

DRIFT OVER OPERATING CONDITIONS
(For particular part)

Grey Level	VID_2	VID_1		VIDOUT	$\overline{VIDOUT}$
X	I	I	I_{White}	0	0
I	I	O	I_{Grey1}	2% Max	2% Max
O	I	O	I_{Grey2}	2% Max	2% Max
X	O	I	I_{Black}	1% Max	1% Max
X	O	O	I_{Blank}	0	0

Notes:
1. Test Condition: Normal I_{White} for $\overline{VIDOUT}$ + 13.3mA.
2. Positive current flowing into VIDOUT/$\overline{VIDOUT}$.
3. t_R, t_F = 5ns Max.
4. $\overline{VIDOUT}$ output currents normalized to I_{White}. VIDOUT output currents normalized to I_{Blank}.
5. Min/Max values for VIDOUT and $\overline{VIDOUT}$ account for variation of different devices.
6. Am8152A
   V Pull-Up: $8.5V \geq V$ Pull-Up $\geq V_{CC}$
   VIDOUT/$\overline{VIDOUT}$: (V Pull-Up) $\geq$ VIDOUT/$\overline{VIDOUT} \geq (V_{CC} - 1V)$
7. Am8153A
   V Pull-Up: $3.5V \geq V$ Pull-Up $\geq 0V$
   VIDOUT/$\overline{VIDOUT}$: (V Pull-Up) $\geq$ VIDOUT/$\overline{VIDOUT} \geq -1.0V$

11

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
High Output State ..... −0.5V to +V_{CC}
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

Am8152A DC CHARACTERISTICS (See Note 4)

Parameters	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	$MCLK_1$ $MCLK_2$	I_{OH} = −0.1mA	MIL	3.6			Volts
			TTL Outputs	I_{OH} = −1mA	COM'L	4.0			Volts
				I_{OH} = −2.6mA	MIL	2.4	3.4		Volts
					COM'L	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min		I_{OL} = 0.1mA $MCLK_{1/2}$				0.3	Volts
				I_{OL} = 16mA TTL Outputs				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA						−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = 0.4V		All Inputs (Except RES, EXTDCLK)				−0.4	mA
				RES, EXTDCLK				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = 2.7V		All Inputs (Except RES)				+50	μA
				RES				+600	μA
I_I	Input HIGH Current at Max Input Voltage	V_{CC} = Max V_{IN} = 5.5V						+1.0	mA
I_{SC}	Output Short Current Current (Note 3)	V_{CC} = Max		$MCLK_1$, $MCLK_2$		−50		−250	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC1} = Max V_{CC2} = Max	Over Operating Range					415	mA
			@ T_A = 70°C					375	mA
			@ T_C = 125°C					350	mA

Notes: 1. For conditions shown as Min or Max use the appropriate value specified under DC Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Except : X_1, X_2, X_3, AADJ, VIDOUT, $\overline{\text{VIDOUT}}$.

Am8153A DC CHARACTERSTICS (See Note 4)

The following conditions apply unless otherwise specified:
COM'L $T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Min = 4.75V Max = 5.25V) $V^- = -5.2V \pm 5\%$ (Min = −4.94V Max = −5.46V)
MIL $T_C = -55$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Min = 4.50V Max = 5.50V) $V^- = -5.2V \pm 10\%$ (Min = −4.68V Max = −5.72V)

Parameters	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	$MCLK_1$ $MCLK_2$	$I_{OH} = -0.1mA$	MIL	3.6			Volts
					COM'L	4.0			Volts
			TTL Outputs	$I_{OH} = -1mA$ $I_{OH} = -2.6mA$	MIL	2.4	3.4		Volts
					COM'L	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min		$I_{OL} = 0.1mA$ $MCLK_{1/2}$				0.3	Volts
				$I_{OL} = 16mA$ TTL Outputs				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, $I_{IN} = -18mA$						−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max $V_{IN} = 0.4V$		All Inputs (Except RES)				−0.4	mA
				RES				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max $V_{IN} = 2.7V$		All Inputs (Except RES)				+50	μA
				RES				+600	μA
I_I	Input HIGH Current at Max Input Voltage	V_{CC} = Max $V_{IN} = 5.5V$						+1.0	mA
I_{SC}	Output Short Current Current (Note 3)	V_{CC} = Max		$MCLK_1$, $MCLK_2$		−50		−250	mA
				Others		−40		−130	mA
II<CC>	Power Supply Current	V_{CC1} = Max V_{CC2} = Max	Over Operating Range					410	mA
			@ $T_A = 70°C$					370	mA
			@ $T_C = 125°C$					345	mA
I^-	Power Supply Current	V^- = Max	Over Operating Range					40	mA
			@ $T_A = 70°C$					37	mA
			@ $T_C = 125°C$					35	mA

Notes: 1. For conditions shown as Min or Max use the appropriate value specified under DC Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Except: X_1, X_2, X_3, AADJ, VIDOUT, VIDOUT, VID_1, VID_2, EXTDCLK.

DC CHARACTERISTICS

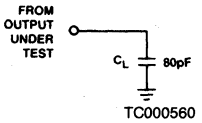
COM'L $T_A = 0$ to 70°C $V_{CC} = 5.0V \pm 5\%$ GND = 0V V– = −5.2V ±5% (Max = −5.46, Min = −4.94)
MIL $T_C = -55$ to 125°C $V_{CC} = 5.0V \pm 10\%$ GND = 0V V– = −5.2V ±10% (Max = −5.72, Min = −4.68)

	Parameters	Test Conditions	−55°C	0°C	25°C	70°C	125°C	Unit
10K ECL Outputs	V_{OH} (Max)	50Ω to −2V	−880	−840	−780	−720	−630	mV
	V_{OH} (Min)		−1080	−1000	−930	−900	−825	mV
	V_{OHA} (Min)		−1100	−1020	−950	−920	−845	mV
VID_1 and VID_2	V_{OLA} (Max)	50Ω to −2V	−1635	−1645	−1600	−1605	−1525	mV
	V_{OL} (Max)		−1655	−1665	−1620	−1625	−1545	mV
	V_{OL} (Min)		−1920	−1870	−1850	−1830	−1820	mV
10K ECL Input	V_{IH} (Max)		−880	−840	−780	−720	−630	mV
	V_{IHA} (Min)		−1255	−1145	−1105	−1045	−1000	mV
EXTDCLK	V_{ILA} (Max)		−1510	−1490	−1475	−1450	−1400	mV
	V_{IL} (Min)		−1920	−1870	−1850	−1830	−1820	mV
	I_{IH}	V^- = Max $V_{IN} = V_{IH}$ (Max)	200	200	200	200	200	μA
	I_{IL}	V^- = Max $V_{IN} = V_{IL}$ (Min)	150	150	150	150	150	μA

11

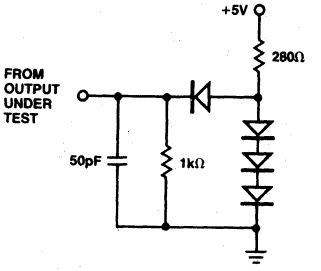
SWITCHING TEST CIRCUIT

$MCLK_1/MCLK_2$ OUTPUT



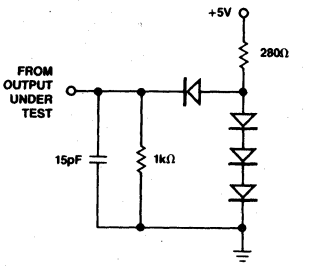
TC000560

TTL OUTPUTS EXCEPT $TCLK_2$



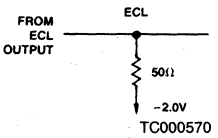
TC000700

$TCLK_2$ OUTPUT



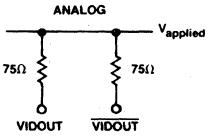
TC001530

ECL OUTPUTS



TC000570

ANALOG OUTPUTS



TC000550

Am8152A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

(T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V^- = 0V)

Number	Description		Min	Max	Units
1	$MCLK_1$ Period		100		ns
2	CLK_2 Period		70		ns
3	$MCLK_1$ HIGH (See Note 5)	4.0V	38		ns
4	$MCLK_1$ LOW (See Notes 3 and 5)	0.3V	38		ns
5	$MCLK_2$ HIGH (See Note 6)	4.0V	23		ns
6	$MCLK_2$ LOW (See Notes 3 and 6)	0.3V	23		ns
7	Data to $MCLK_2$/$TCLK_2$ RE (See Note 1)		20		ns
8	$MCLK_2$/$TCLK_2$ to Data Not Valid		0		ns
9	VSYNC/HSYNC to $MCLK_1$ RE Setup (SSEL = HIGH)		20		ns
10	VSYNC/HSYNC to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
11	$TCLK_2$ RE to $MCLK_2$ RE Delay			8	ns
12	$TCLK_2$ FE to $MCLK_2$ FE Delay			12	ns
13	$MCLK_1$ to VSLD, HSLD (SSEL = HIGH)			$6 + T_D$	ns
14	$TCLK_2$ to VSLD, HSLD (SSEL = LOW)			$6 + T_D$	ns
15	DD(0:7) to $TCLK_2$ FE		20		ns
16	$TCLK_2$ RE to VID_1 VID_2 VAL (See Note 2)			$6 + T_D$	ns
17	BLANK FE to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
18	BLANK FE to $MCLK_1$ FE Setup (SSEL = HIGH)		20		ns
19	BLANK RE to $MCLK_1$ RE Setup (SSEL = HIGH)		20		ns
20	BLANK RE to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
22	VID_1 to VID_2 Skew		−5	+5	ns
24	EXTDCLK to $MCLK_1$			20	ns
25	EXTDCLK to $TCLK_2$			13	ns
26	EXTDCLK to $MCLK_2$			23	ns
27	EXTDCLK to VID_1/VID_2			13	ns
28	EXTDCLK to HSDLD/VSDLD (SSEL HI)			13	ns
29	EXTDCLK to HSDLD/VSDLD (SSEL LO)			13	ns
30	EXTDCLK to Data in Setup		9		ns
31	EXTDCLK to Data Not Valid Hold		11		ns
32	EXTDCLK to H/V SYNC Setup		10		ns
33	EXTDCLK Period		16.6		ns
34	EXTDCLK LOW Cycle		5		ns
35	EXTDCLK HIGH Cycle		5.0		ns
36	Reset Pulse Width (High)		10.0		ns
37	Reset Low to EXTDCLK Setup		8.0		ns

Notes: 1. Data includes CBLANK, FORE, REV, FS, DD_0–DD_8, TB0, TB1, BS, CLK_1DR, CLK_2DR, DW.
2. First Pixel of character. T_D is pixel period as defined by oscillator frequency.
3. Max undershoot on these outputs is guaranteed to be −0.3V.
4. T_D is the dot clock period.
5. Guaranteed to 100ns $MCLK_1$ cycle time.
6. Guaranteed to 70ns $MCLK_2$ cycle time (even divide ratio only).

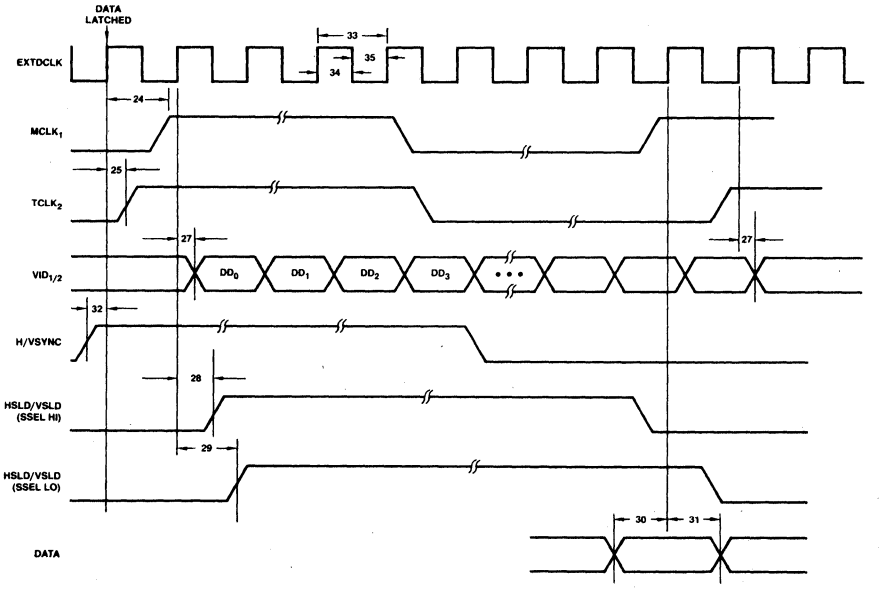
Am8153A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

(T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V^- = −5.2V ±5%)

Number	Description		Min	Max	Units
1	$MCLK_1$ Period		100		ns
2	CLK_2 Period		70		ns
3	$MCLK_1$ HIGH (See Note 5)	4.0V	38		ns
4	$MCLK_1$ LOW (See Notes 3 and 5)	0.3V	38		ns
5	$MCLK_2$ HIGH (See Note 6)	4.0V	23		ns
6	$MCLK_2$ LOW (See Notes 3 and 6)	0.3V	23		ns
7	Data to $MCLK_2$/$TCLK_2$ RE (See Note 1)		$20 + T_D$ (See Note 4)		ns
8	$MCLK_2$/$TCLK_2$ to Data Not Valid		0		ns
9	VSYNC/HSYNC to $MCLK_1$ RE Setup (SSEL = HIGH)		$20 + T_D$		ns
10	VSYNC/HSYNC to $MCLK_2$ RE Setup (SSEL = LOW)		$20 + T_D$		ns
11	$TCLK_2$ RE to $MCLK_2$ RE Delay			8	ns
12	$TCLK_2$ FE to $MCLK_2$ FE Delay			12	ns
13	$MCLK_1$ to VSLD, HSLD (SSEL = HIGH)			6	ns
14	$TCLK_2$ to VSLD, HSLD (SSEL = LOW)			6	ns
15	DD(0:7) to $TCLK_2$ FE		$20 + T_D$		ns
16	$TCLK_2$ RE to VID_1 VID_2 VAL (See Note 2)			6	ns
17	BLANK FE to $MCLK_2$ RE Setup (SSEL = LOW)		$20 + T_D$		ns
18	BLANK FE to $MCLK_1$ FE Setup (SSEL = HIGH)		$20 + T_D$		ns
19	BLANK RE to $MCLK_1$ RE Setup (SSEL = HIGH)		$20 + T_D$		ns
20	BLANK RE to $MCLK_2$ RE Setup (SSEL = LOW)		$20 + T_D$		ns
21	VID_1 to VID_2 Skew		−2	+2	ns
24	EXTDCLK to $MCLK_1$			20	ns
25	EXTDCLK to $TCLK_2$			10	ns
26	EXTDCLK to $MCLK_2$			23	ns
27	EXTDCLK to VID_1/VID_2			8	ns
28	EXTDCLK to HSDLD/VSDLD (SSEL HI)			10	ns
29	EXTDCLK to HSDLD/VSDLD (SSEL LO)			10	ns
30	EXTDCLK to Data in Setup		9		ns
31	EXTDCLK to Data Not Valid Hold		11		ns
32	EXTDCLK to H/V SYNC Setup		10		ns
33	EXTDCLK Period		10		ns
34	EXTDCLK LOW Cycle		5		ns
35	EXTDCLK HIGH Cycle		3.5		ns
36	Reset Pulse Width (High)		10.0		ns
37	Reset Low to EXTDCLK Setup		8.0		ns

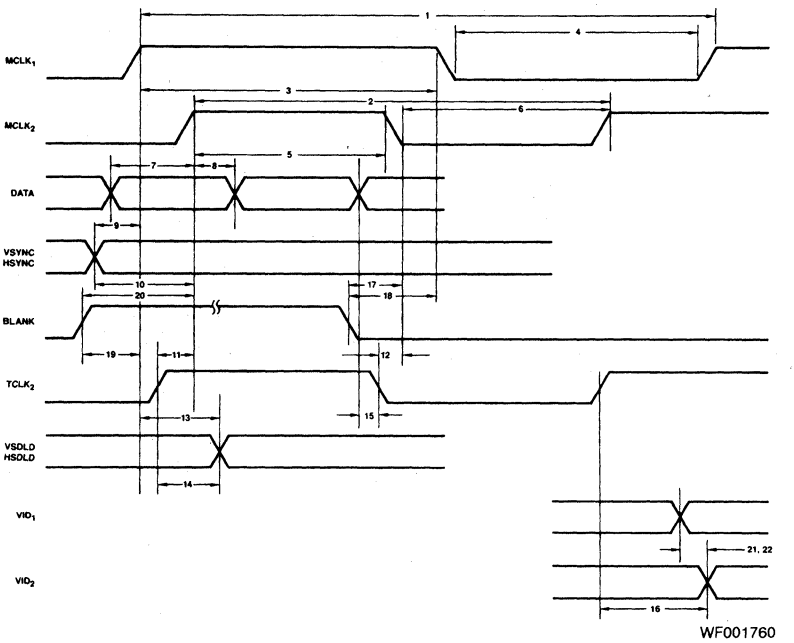
Notes: 1. Data includes CBLANK, FORE, REV, FS, DD_0–DD_8, TB0, TB1, BS, CLK_1DR, CLK_2DR, DW.
2. First Pixel of character. T_D is pixel period as defined by oscillator frequency.
3. Max undershoot on these outputs is guaranteed to be −0.3V.
4. T_D is the dot clock period.
5. Guaranteed to 100ns $MCLK_1$ cycle time.
6. Guaranteed to 70ns $MCLK_2$ cycle time (even divide ratio only).

Am8152A/53A TIMING
(PARAMETERS MEASURED WITH RESPECT TO EXTDCLK)



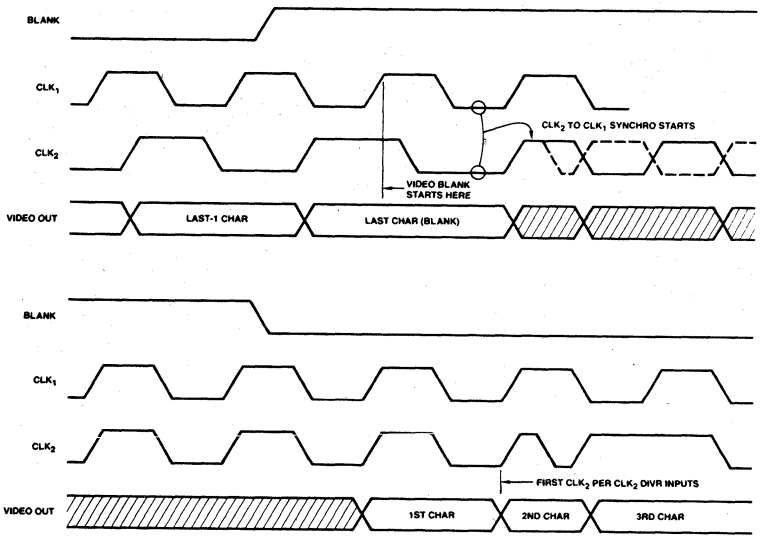
WF003210

AC TIMING DIAGRAM—MCLK$_1$/MCLK$_2$



WF001760

VSC CLK_2 SYNCHRONIZATION (ONLY OCCURS IF SSEL IS HIGH)



WF001750

8284A/8284A-1

Clock Generator and Driver for 8086, 8088 Processors

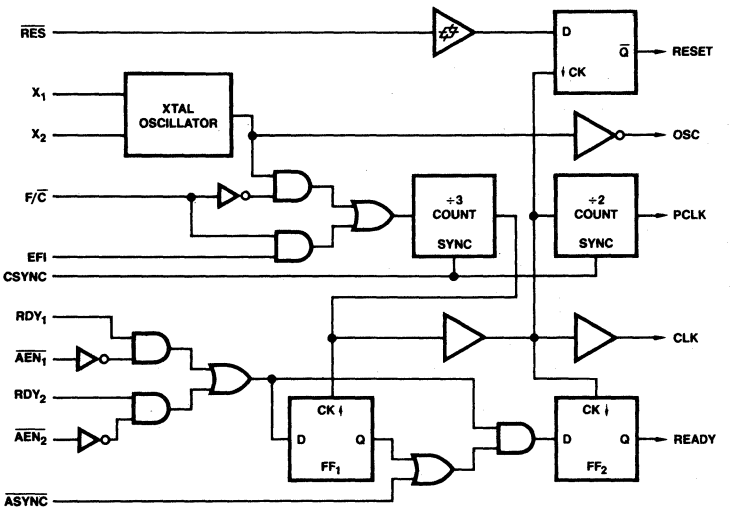
DISTINCTIVE CHARACTERISTICS

- Generates the System Clock for the 8086, 8088 Processors: 5MHz, 8MHz with 8284A; 10MHz with 8284A-1
- Uses a crystal or a TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- Generates system reset output from Schmitt trigger input
- Capable of clock synchronization with other 8284As

GENERAL DESCRIPTION

The 8284A is a single chip clock generator/driver for the 8086, 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic.

BLOCK DIAGRAM



BD001440

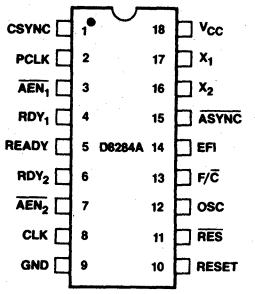
RELATED PRODUCTS

Part No.	Description
Am8086	16-Bit Microprocessor
8288	Bus Controller

Multibus is a registered trademark of Intel Corp.

03359C

CONNECTION DIAGRAM
Top View



CD001580

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

M D 8284 A B

- B — Screening Option
  - Blank-Standard processing
  - B-Burn-in
- A — Speed
  - 5MHz, 8MHz, 10MHz — CLOCK 5 Frequency
- 8284 — Device Type
  - Clock Generator and Driver
- D — Package
  - D – 18-pin CERDIP (D-18-1)
  - X – Dice
- M — Temperature Range
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)

Valid Combinations	
MD P D	8284A
MD D	8284AB
D	8284A-1 8284A-1B
Dice	8284AXM 8284AXC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7	$\overline{AEN_1}$, $\overline{AEN_2}$	I	Address Enable. The $\overline{AEN}$ signal is used to qualify the Bus Ready signal (RDY_1 or RDY_2). $\overline{AEN_1}$ validates RDY_1 while $\overline{AEN_2}$ validates RDY_2. It is possible for the processor to access two Multi-Master System Busses if you use both signals. Both signals are tied LOW in non Multi-Master Systems.
4, 6	RDY_1, RDY_2	I	Bus Ready. These signals are indications from a device located on the system bus that it is available or data has been received. RDY_1 and RDY_2 are qualified by $\overline{AEN_1}$ and $\overline{AEN_2}$ respectively.
15	$\overline{ASYNC}$	I	Ready Synchronous Select. The $\overline{ASYNC}$ signal defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is open (internal pull-up resistor is provided) or pulled HIGH, there is one stage of READY Synchronization. When $\overline{ASYNC}$ is LOW, there are two stages of READY Synchronization.
5	READY	O	Ready. READY is the synchronized RDY signal input. After the guaranteed hold time to the processor has been met, the READY signal is cleared.
7, 16	X_1,X_2	I	Crystal In. These are the input pins for the attached crystal. The crystal frequency is 3 times the desired process clock frequency.
13	F/$\overline{C}$	I	Frequency/$\overline{Crystal\ Select}$. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input. When strapped LOW, the F/$\overline{C}$ allows the processor clock to be generated by the crystal.
14	EFI	I	External Frequency. Used in conjunction with a HIGH signal on F/$\overline{C}$, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
8	CLK	O	Processor Clock. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (including bipolar support chips and other MOS devices). An output HIGH of 4.5V (V_{CC} = 5V) is provided on this pin to drive MOS devices. The output frequency of CLK is 1/3 of the crystal on EFI input frequency and a 1/3 duty cycle.
2	PCLK	O	Peripheral Clock. This signal is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
12	OSC	O	Oscillator Output. This signal is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
11	$\overline{RES}$	I	$\overline{Reset}$ In. This signal is used to generate a RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
10	RESET	O	Reset. This signal is used to reset the 8086 family processors.
1	CSYNC	I	Clock Synchronization. This signal is designed to allow multiple 8284As to be synchronized to provide clocks that are in phase. CSYNC HIGH will reset the internal counters, when CSYNC goes LOW the counters will resume counting. CSYNC needs to be externally synchronized to EFI. When used with the internal oscillator, CSYNC should be hard wired to ground.

DETAILED DESCRIPTION

OSCILLATOR

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X_1 and X_2 are the two crystal input crystal connections. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Two 510Ω series resistors are optional for systems which have a V_{CC} ramp time greater than (or equal to) 1V/ms and/or inherent board capacitance between X_1 or X_2 exceeding 10pF. This capacitance value should not include the 8284A's pin capacitance. By limiting the stray capacitance to less than 10pF on X_1 or X_2, the deviation from the desired fundamental frequency is minimized.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input, (CSYNC), allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A (see Figure 1). This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the EFI input or the crystal oscillator as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 or 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

Reset logic for the 8284A is provided by a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing.

The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY_1, RDY_2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN_1}$ and $\overline{AEN_2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

To assure RDY setup and hold times are met, synchronization is required for all asynchronous active going edges of either RDY input. Inactive-going edges of RDY (in normally ready systems) do not require synchronization, but must satisfy RDY setup and hold as a matter of proper system design.

The two modes of RDY synchronization operation are defined by the $\overline{ASYNC}$ input.

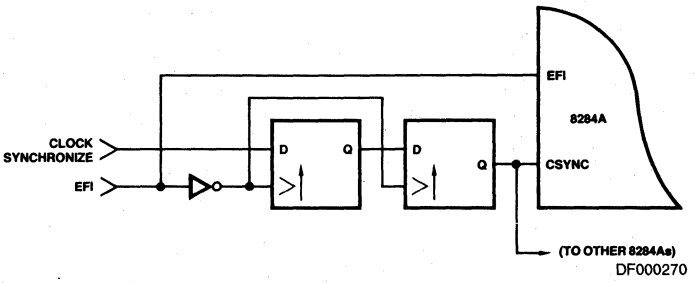
When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK; after which time the READY output will go active (HIGH). Negative-going asynchro-

nous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous, (normally not ready), devices in the system which cannot be guaranteed by design to meet the required RDY setup timing t_{R1VCL} on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

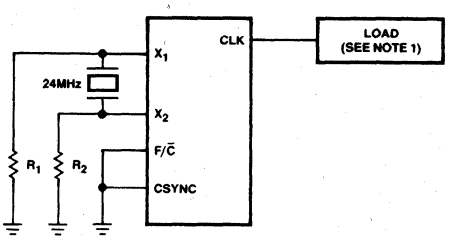
$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 1. CSYNC Synchronization



DF000270

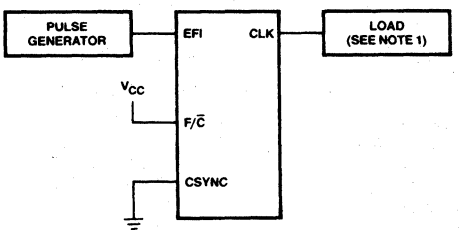
CLOCK HIGH AND LOW TIME (USING X_1, X_2)



AF000630

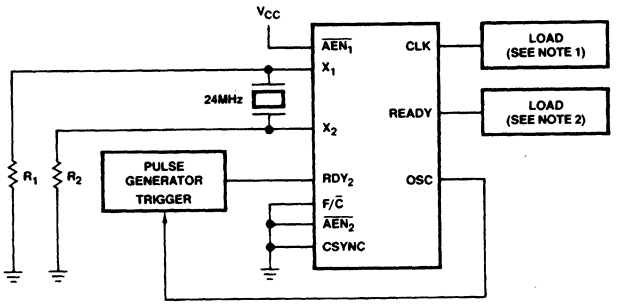
$R_1 = R_2 = 510\Omega$.

CLOCK HIGH AND LOW TIME (USING EFI)



AF000620

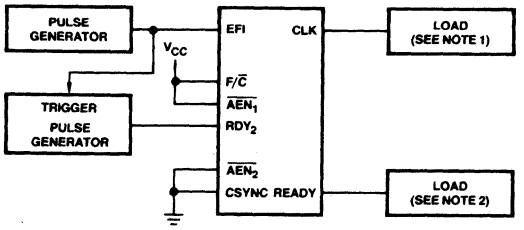
READY TO CLOCK (USING X_1, X_2)



AF000640

$R_1 = R_2 = 510\Omega$.

READY TO CLOCK (USING EFI)



AF000610

Notes: 1. $C_L = 100pF$
2. $C_L = 30pF$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Powers Applied
(COML, A-1) ..... 0°C to +70°C
(MIL) ..... −55°C to +125°C
All Output and Supply Voltages ..... −0.5V to +7.0V
All Input Voltage ..... −1.0V to +5.5V
Power Dissipation 1W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

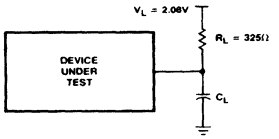
Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Max	Units
I_F	Forward Input Current ($\overline{ASYNC}$)	$V_F = 0.45V$		−1.3	mA
	Other Inputs	$V_F = 0.45V$		−0.5	
I_R	Reverse Input Current ($\overline{ASYNC}$)	$V_H = V_{CC}$		50	μA
	Other Inputs	$V_R = 5.25V$		50	
V_C	Input Forward Clamp Voltage	$I_C = -5mA$		−1.0	Volts
I_{CC}	Power Supply Current			162	mA
V_{IL}	Input LOW Voltage			0.8	Volts
V_{IH}	Input HIGH Voltage		2.0		Volts
V_{IHR}	Reset Input HIGH Voltage		2.6		Volts
V_{OL}	Output LOW Voltage	5mA		0.45	Volts
V_{OH}	Output HIGH Voltage CLK	−1mA	4.0	2.5	Volts
	Other Outputs	−1mA	2.4		
V_{IHR}–V_{ILR}	$\overline{RES}$ Input Hysteresis		0.25		Volts

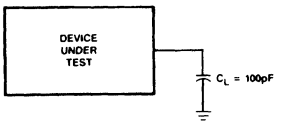
SWITCHING TESTING CIRCUIT (CLK, READY)



TC000670

C_L = 100pF for CLK
C_L = 30pF for READY

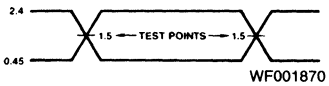
SWITCHING TESTING CIRCUIT (CLK, READY)



TC000680

C_L = 100pF

SWITCHING TESTING WAVEFORM (input, output)



WF001870

AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

TIMING REQUIREMENTS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{EHEL}	External Frequency HIGH Time	90% – 90%V_{IN}	13			ns
t_{ELEH}	External Frequency LOW Time	10% – 10%V_{IN}	13			ns
t_{ELEL}	EFI Period	MIL (Note 1)	$t_{EHEL} + t_{ELEH} + \delta$			ns
		COM'L, A-1	33			
	XTAL Frequency		12		25	MHz
t_{R1VCL}	RDY_1, RDY_2 Active Setup to CLK	$\overline{ASYNC}$ = HIGH	35			ns
t_{R1VCH}	RDY_1, RDY_2 Active Setup to CLK	$\overline{ASYNC}$ = LOW	35			ns
t_{R1VCL}	RDY_1, RDY_2 Inactive Setup to CLK		35			ns
t_{CLR1X}	RDY_1, RDY_2 Hold to CLK		0			ns
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK		50			ns
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK		0			ns
t_{A1VR1V}	$\overline{AEN_1}$, $\overline{AEN_2}$ Setup to RDY_1, RDY_2		15			ns
t_{CLA1X}	$\overline{AEN_1}$, $\overline{AEN_2}$ Hold to CLK		0			ns
t_{YHEH}	CSYNC Setup to EFI		20			ns
t_{EHYL}	CSYNC Hold to EFI	MIL	20			ns
		COM'L, A-1	10			
t_{YHYL}	CSYNC Width		$2 \cdot t_{ELEL}$			ns
t_{I1HCL}	$\overline{RES}$ Setup to CLK	(Note 2)	65			ns
t_{CLI1H}	$\overline{RES}$ Hold to CLK	(Note 2)	20			ns
t_{ILIH}	Input Rise Time	From 0.8V to 2.0V			20	ns
t_{ILIL}	Input Fall Time	From 2.0V to 0.8V			12	ns

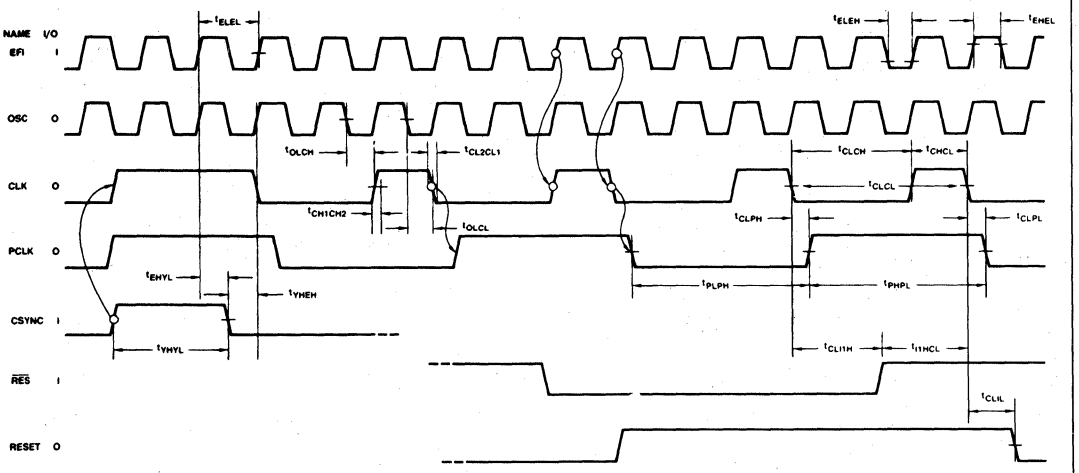
TIMING RESPONSES

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{CLCL}	CLK Cycle Period	MIL, COM'L	125			ns
		A-1	100			
t_{CHCL}	CLK HIGH Time	MIL, COM'L	(1/3 t_{CLCL}) + 2			ns
		A-1	39			
t_{CLCH}	CLK LOW Time	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CH1CH2} / t_{CL2CL1}	CLK Rise or Fall Time	1.0V to 3.5V			10	ns
t_{PHPL}	PCLK HIGH Time		t_{CLCL} - 20			ns
t_{PLPH}	PCLK LOW Time		t_{CLCL} - 20			ns
t_{RYLCL}	Ready Inactive to CLK (See Note 4)		-8			ns
t_{RYHCH}	Ready Active to CLK (See Note 3)	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CLIL}	CLK to Reset Delay				40	ns
t_{CLPH}	CLK to PCLK HIGH Delay				22	ns
t_{CLPL}	CLK to PCLK LOW Delay				22	ns
t_{OLCH}	OSC to CLK HIGH Delay		-5		22	ns
t_{OLCL}	OSC to CLK LOW Delay		2		35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8V to 2.0V			20	ns
t_{OHOL}	Output Fall Time (except CLK)	From 2.0V to 0.8V			12	ns

Notes:
1. δ = EFI rise (5ns max) + EFI fall (5ns max).
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 states.

SWITCHING WAVEFORMS

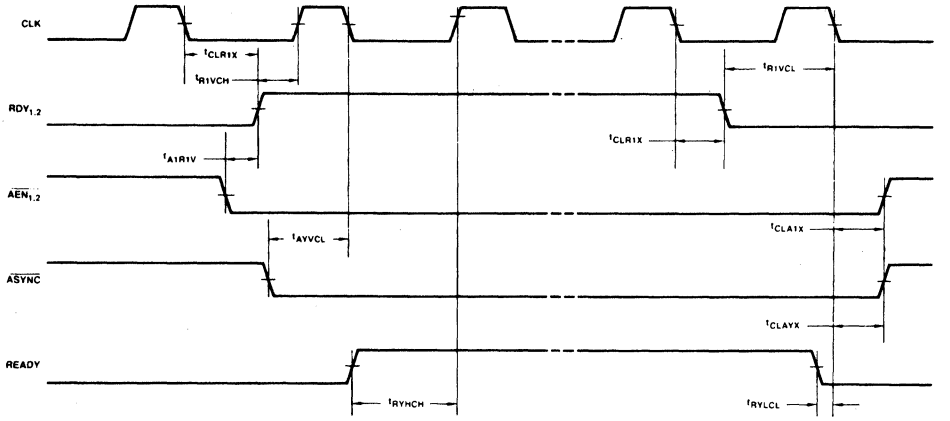
CLOCKS AND RESET SIGNALS



WF002530

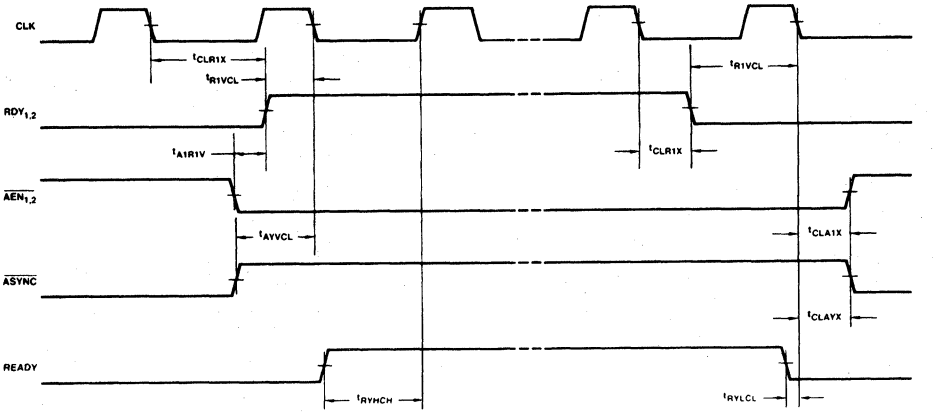
Note: All timing requirements are made at 1.5 volts, unless otherwise noted.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



WF002520

READY SIGNALS (FOR SYNCHRONOUS DEVICES)



WF002510

8286/8287

Octal Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- Data bus buffer/driver for 8086, 8088, 8080A, 8085A, and 8048 processors
- Fully parallel 8-bit transceivers: 8286 is noninverting
  8287 is inverting
- 3-state inputs/outputs for interfacing with bus-oriented systems
- Available in 20-pin, 0.3" center molded DIP or ceramic package
- Advanced bipolar Schottky processing
- Bus port stays in hi-impedance state during power up/down transition

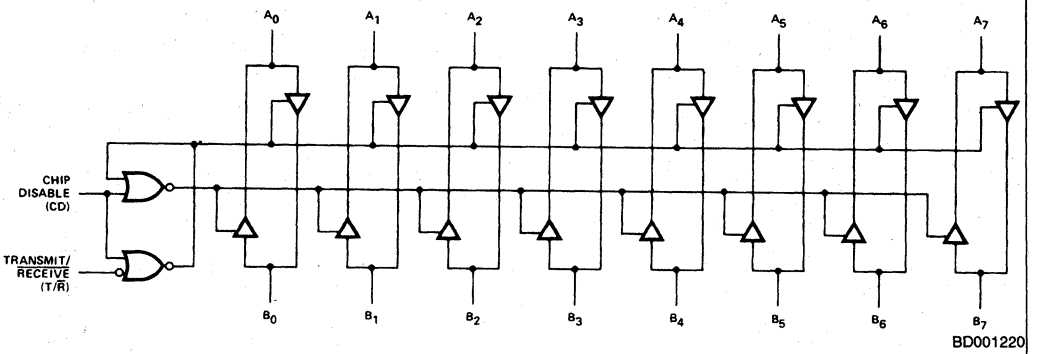
GENERAL DESCRIPTION

The 8286 and 8287 are 8-bit 3-state bipolar Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 32mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/Receive determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

BLOCK DIAGRAM

8286*



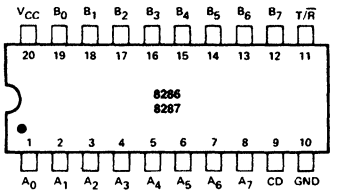
*8287 has inverting transceivers

RELATED PRODUCTS

PART NO	DESCRIPTION
2946/47	Octal Bus Transceivers
2948/49	Octal Bus Transceivers
8086	16-Bit Microprocessor

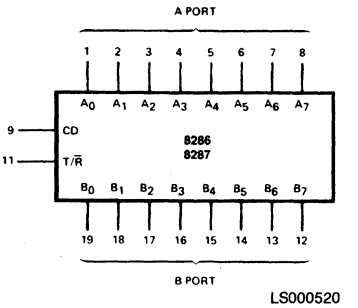
05699A

CONNECTION DIAGRAM
Top View



CD001500

LOGIC SYMBOL

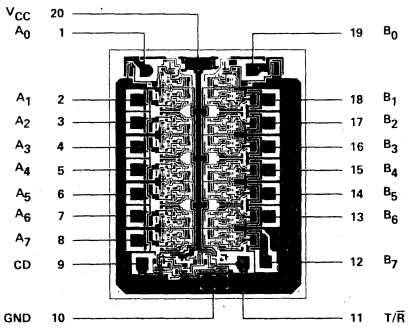


LS000520

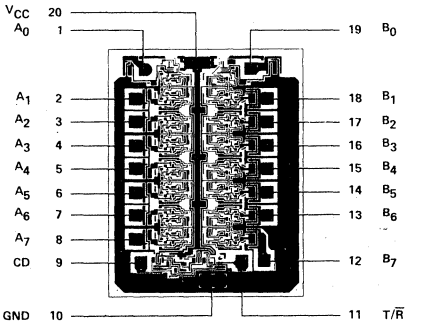
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

8286



8287



DIE SIZE .069" x .089"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

8286
M D 8287 B

- B — Screening Option
  - Blank-Standard processing
  - B-Burn-in
- 8287 — Device Type
  - Octal Bus Transceivers
- D — Package
  - D – 20-pin CERDIP (D-20-1)
  - P – 20-pin plastic DIP (P-20-1)
  - X – Dice
- M — Temperature Range
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)

Valid Combinations	
MD D P XM, XC	8286
MD D P	8286B
P XC	8287
P	8287B

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	$A_0 - A_7$	I/O	A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is Low and are transmit inputs when T/$\overline{R}$ is HIGH.
	$B_0 - B_7$	I/O	B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.
9	CD	I	Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).
11	T/$\overline{R}$	I	Transmit/$\overline{Receiver}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH, A port is the input and B port is the output. With T/$\overline{R}$ LOW, A port is the output and B port is the input.

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... +7.0V
Input Voltage ..... +5.5V
Output Voltage ..... +5.5V
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

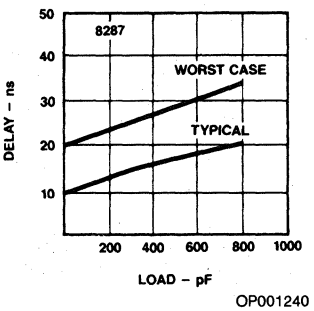
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

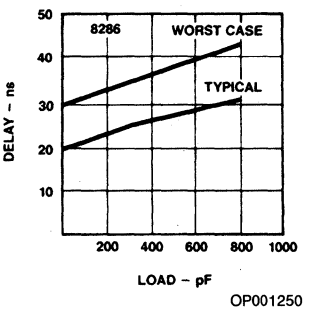
Parameters	Description		Test Conditions	Min	Max	Units
V_C	Input Clamp Voltage		$I_C = -5mA$		−1	Volts
I_{CC}	Power Supply Current	8287			130	mA
		8286			160	
I_F	Forward Input Current		$V_F = 0.45V$		−0.2	mA
I_R	Reverse Input Current		$V_R = 5.25V$		50	μA
V_{OL} (COM'L)	Output Low Voltage	B Outputs	$I_{OL} = 32mA$		.45	Volts
		A Outputs	$I_{OL} = 16mA$		.45	
V_{OL} (MIL)	Output Low Voltage	B Outputs	$I_{OL} = 20mA$		.45	Volts
		A Outputs	$I_{OL} = 10mA$		.45	
V_{OH}	Output High Voltage	B Outputs	$I_{OH} = -5mA$	2.4		Volts
		A Outputs	$I_{OH} = -1mA$	2.4		
I_{OFF}	Output Off Current		$V_{OFF} = 0.45V$		I_F	
			$V_{OFF} = 5.25V$		I_R	
V_{IL}	Input Low Voltage	A Port	$V_{CC} = 5.0V$ (See note 1)		0.8	Volts
		B Port	$V_{CC} = 5.0V$ (See note 1)		0.9	
V_{IH}	Input High Voltage		$V_{CC} = 5.0V$ (See note 1)	2.0		Volts
C_{IN}	Input Capacitance		F = 1MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$		12	pF

OPERATING CHARACTERISTICS

Output Delay versus Capacitance



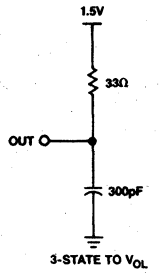
OP001240



OP001250

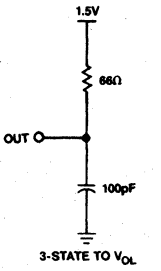
Refer to Page 13-1 for Essential Information on M

SWITCHING TEST CIRCUITS



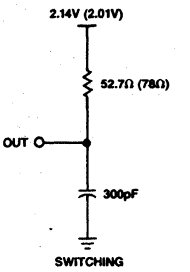
TC000610

B OUTPUT



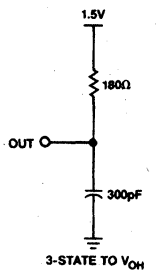
TC000620

A OUTPUT



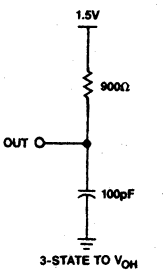
TC000630

B OUTPUT



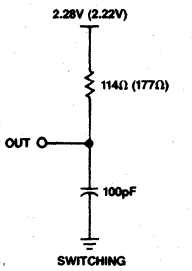
TC000580

B OUTPUT



TC000590

A OUTPUT



TC000600

A OUTPUT

Values in parenthesis reflect MIL temp. conditions.

SWITCHING CHARACTERISTICS (See Note 2)

Parameters	Description		Test Conditions (See Notes)	Min (COM'L)	Min (MIL)	Max	Units
TIVOV	Input to Output Delay	Inverting		5		22	ns
		Non-inverting		5		30	
TEHTV	Transmit/Receive Hold Time			5	TENHOZ		ns
TTVEL	Transmit/Receive Setup			10	30		ns
TEHOZ	Output Disable Time			3		18	ns
TELOV	Output Enable Time			10	10	30	ns
TILIH, TOLOH	Input, Output Rise Time		From 0.8 to 2.0V			20	ns
TIHIL, TOHOL	Input, Output Fall Time		From 2.0 to 0.8V			12	ns

Notes:
1. COM'L temperature loading conditions

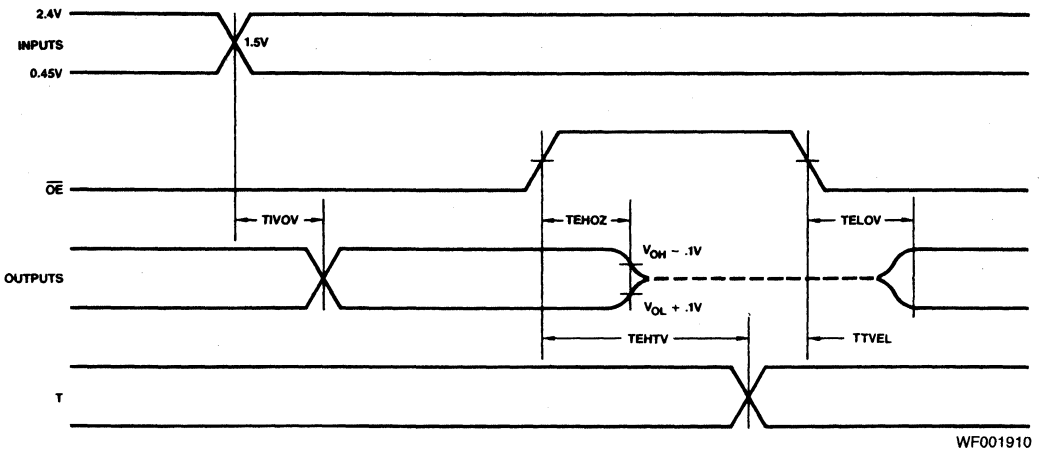
   MIL temperature loading conditions
2. Refer to waveforms and SWITCHING TEST CIRCUITS on following pages.

B outputs: I_{OL} = 32mA, I_{OH} = −5mA, C_L = 300pF
A outputs: I_{OL} = 16mA, I_{OH} = −1mA, C_L = 100pF
B outputs: I_L = 20mA, I_{OH} = −5mA, C_L = 300pF
A outputs: I_{OL} = 10mA, I_{OH} = −1mA, C_L = 100pF

05699A

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



WF001910

AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0"; timing measurements are made at 1.5V for both a logic "1" and "0."

8288

Bus Controller

DISTINCTIVE CHARACTERISTICS

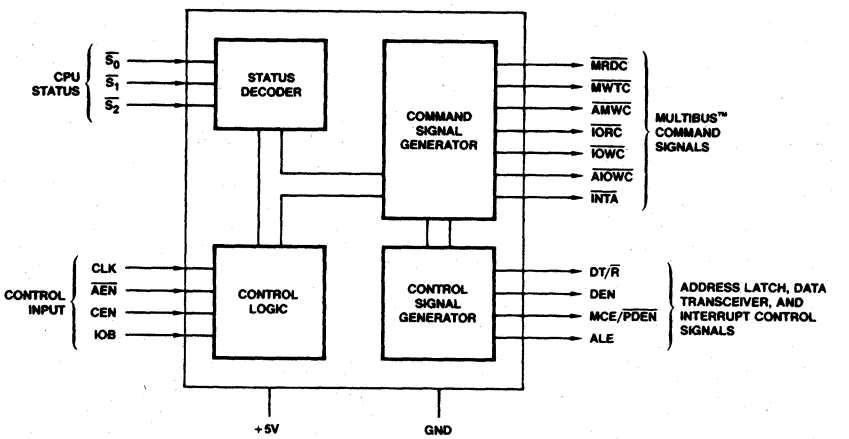
- Bipolar drive capability
- 3-state output drivers
- Multi-master or I/O bus interface
- Flexible system configurations

GENERAL DESCRIPTION

The 8288 optimizes 8086 or 8088 operations by providing command and control timing generation when the CPU is in maximum mode. It provides for highly flexible configurations for larger systems. It also adds powerful bipolar drive capability to the system.

The 8288 is implemented in bipolar technology in a 20-pin DIP.

BLOCK DIAGRAM

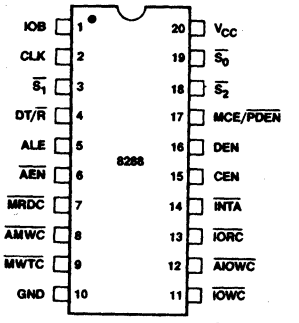


BD001570

03358B

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



CD001840

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

C D 8288 B

- B — Screening Option: Blank – Standard Processing; B – Burn-in
- 8288 — Device Type: Bus Controller
- D — Package: D– 20-pin CERDIP (D-20-1); X– Dice
- C — Temperature Range: C – Commercial (0°C to +70°C)

Valid Combinations	
D	8288 8288B

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
19, 3, 18	$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$	I	Status. These signals are the status input pins from the microprocessor. The 8288 decodes these inputs to generate command and control signals.
2	CLK	I	Clock. Clock signal from the clock generator.
5	ALE	O	Address Latch Enable. This signal strobes an address into the address latches. The latching occurs on the falling edge (HIGH to LOW) transition.
16	DEN	O	Data Enable. This signal enables the data transceivers onto the data bus (local or system).
4	DT/$\overline{R}$	O	Data Transmit/Receive. This signal determines the direction of data flow through the transceivers.
6	$\overline{AEN}$	I	Address Enable. This signal enables the 8288 command outputs at least 115ns after it becomes active LOW. When this pin goes inactive, it 3-states the command output drivers.
15	CEN	I	Command Enable. This signal, when LOW, enables all command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive states.
1	IOB	I	Input/Output Bus Mode. When strapped HIGH, the 8288 functions in the I/O Bus mode. When LOW, the 8288 functions in the System Bus mode.
12	$\overline{AIOWC}$	O	Advanced I/O Write Command. The $\overline{AIOWC}$ gives I/O devices early indication of a write instruction by issuing an I/O Write Command earlier in the machine cycle.
11	$\overline{IOWC}$	O	I/O Write. This signal tells an I/O device to read the data on the data bus.
13	$\overline{IORC}$	O	I/O Read. This signal tells an I/O device to drive its data onto the data bus.
8	$\overline{AMWC}$	O	Advanced Memory Write. The AMWC gives memory devices an early indication of a write instruction by issuing a memory write command earlier in the machine cycle.
9	$\overline{MWTC}$	O	Memory Write. This signal instructs the memory to record the data present on the data bus.
7	$\overline{MRDC}$	O	Memory Read. This signal instructs the memory to drive its data onto the data bus.
14	$\overline{INTA}$	O	Interrupt Acknowledge. This signal informs the interrupting device that its interrupt has been acknowledged and drives the vectoring information onto the data bus.
17	MCE/ $\overline{PDEN}$	O	Master Cascade Enable/ Peripheral Data Enable. Dual Function pin: MCE (IOB LOW): This signal occurs during an interrupt sequence. Its function is to read a Cascade Address from a master Priority Interrupt Controller onto the data bus. $\overline{PDEN}$ (IOB HIGH): This signal enables the data bus transceiver for the I/O Bus during I/O instructions. It performs the same function for the I/O Bus that DEN performs for the system bus.

DETAILED DESCRIPTION

COMMAND AND CONTROL LOGIC

The command logic decodes the three CPU status lines ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) to determine what command is to be issued.

This chart shows the meaning of each status "word."

$\overline{s}_2$	$\overline{s}_1$	$\overline{s}_0$	Processor State	8288 Command
0	0	1	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O BUS MODE

The 8288 is put into the I/O Bus mode by strapping the IOB pin HIGH. This mode allows one 8288 Bus Controller to handle two external buses. This allows the CPU to access the I/O Bus with no waiting involved. In the I/O Bus Mode, all I/O command lines ($\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$) are always enabled. When the processor initiates an I/O Command, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. There is no arbitration present in this system, so the I/O command lines should not be used to control the system bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. The IOB mode is recommended if I/O or peripherals dedicated to one processor exist in a multiprocessor based system.

SYSTEM BUS MODE

The 8288 is put into the System Bus mode by strapping the IOB pin LOW. This mode is used when only one bus exists. No command is issued until 115ns after the $\overline{AEN}$ line is activated. Bus arbitration is assumed, and this logic will inform the bus controller via the $\overline{AEN}$ line when the bus is free for use. Both I/O commands and memory wait for bus arbitration.

COMMAND OUTPUTS

To prevent the processor from entering unnecessary wait states, the advanced write commands initiate write procedures early in the machine cycle.

The command outputs are:
$\overline{MRDC}$ – Memory Read Command
$\overline{MWTC}$ – Memory Write Command
$\overline{IORC}$ – I/O Read Command
$\overline{IOWC}$ – I/O Write Command
$\overline{AMWC}$ – Advanced Memory Write Command
$\overline{AIOWC}$ – Advanced I/O Write Command
$\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$) are the control outputs of the 8288. The DEN signal determines when the external bus should be enabled onto the local bus while the DT/$\overline{R}$ determines the direction of the data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ function is determined by the IOB selection. When IOB is HIGH the $\overline{PDEN}$ serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the 8288 is in the System Bus mode (IOB Low). An interrupt sequence consists of two interrupt acknowledge cycles occurring back to back. No data or address transfers take place during the first cycle. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

The MCE signal is not used if the system only contains one PIC. If this is the case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) into a latch for halt state decoding.

COMMAND ENABLE

The Command Enable (CEN) input acts as a command qualifier for the 8288. If the CEN pin is HIGH the 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... 0°C to +70°C
All Output and Supply Voltages ..... −0.5V to +7.0V
All Input Voltage ..... −1.0V to +5.5V
Power Dissipation 1.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

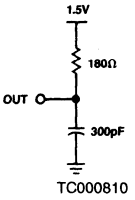
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Max	Units
V_C	Input Clamp Voltage	$I_C = -5mA$		−1	V
I_{CC}	Power Supply Current			230	mA
I_F	Forward Input Current	$V_F = 0.45V$		−0.7	mA
I_R	Reverse Input Current	$V_R = V_{CC}$		50	μA
V_{OL}	Output Low Voltage Command Outputs	$I_{OL} = 32mA$		0.5	V
	Control Outputs	$I_{OL} = 16mA$		0.5	V
V_{OH}	Output High Voltage Command Outputs	$I_{OH} = -5mA$	2.4		V
	Control Outputs	$I_{OH} = -1mA$	2.4		V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{OFF}	Three-State Leakage	$V_{OFF} = 0.4$ to 5.25V		100	μA

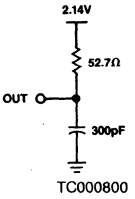
SWITCHING TEST CIRCUIT

3-State to High



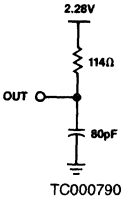
TC000810

Command Output Test Load



TC000800

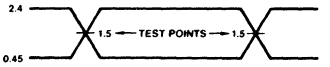
Control Output Test Load



TC000790

SWITCHING TEST INPUT, OUTPUT WAVEFORM

Input/Output



WF001870

AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0."

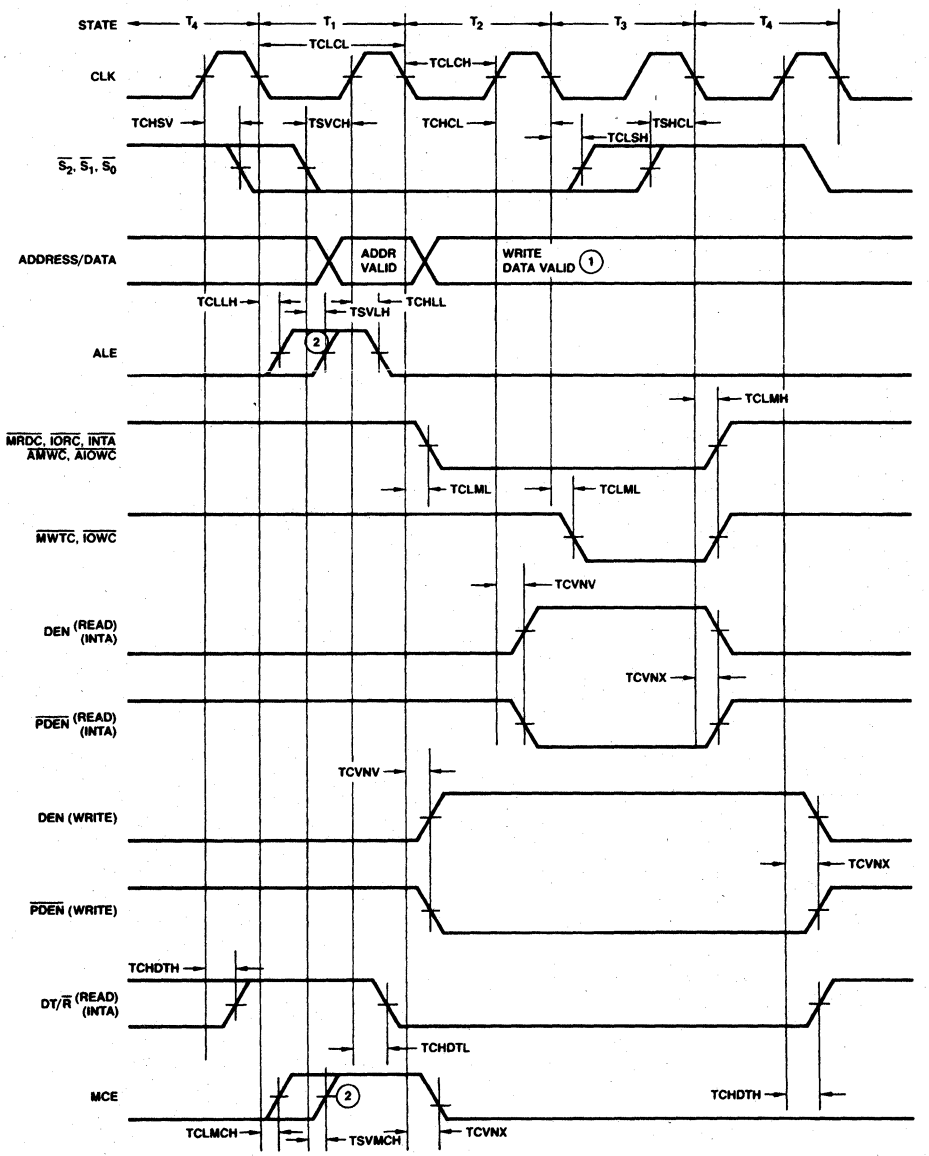
SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Max	Units
Timing Requirements					
TCLCL	CLK Cycle Period		100		ns
TCLCH	CLK Low Time		50		ns
TCHCL	CLK High Time		30		ns
TSVCH	Status Active Setup Time		35		ns
TCHSV	Status Active Hold Time		10		ns
TSHCL	Status Inactive Setup Time		35		ns
TCLSH	Status Inactive Hold Time		10		ns
TILIH	Input Rise Time	From 0.8V to 2.0V		20	ns
TIHIL	Input Fall Time	From 2.0V to 0.8V		12	ns
Timing Responses					
TCVNV	Control Active Delay		5.0	45	ns
TCVNX	Control Inactive Delay		10	45	ns
TCLLH TCMCH	ALE MCE Active Delay (from CLK)			20	ns
TSVLH TSVMCH	ALE MCE Active Delay (from Status)			20	ns
TCHLL	ALE Inactive Delay	$\overline{MRDC}$	4.0	15	ns
TCLML	Command Active Delay	$\overline{IORC}$	10	35	ns
TCLMH	Command Inactive Delay	$\overline{MWTC}$	10	35	ns
TCHDTL	Direction Control Active Delay	$\overline{IOWC}$		50	ns
TCHDTH	Direction Control Inactive Delay	$\overline{INTA}$		30	ns
TAELCH	Command Enable Time	$\overline{AMWC}$		40	ns
TAEHCZ	Command Disable Time	$\overline{AIOWC}$		40	ns
TAELCV	Enable Delay Time	Other	115	200	ns
TAEVNV	AEN to DEN			20	ns
TCEVNV	CEN to DEN, PDEN			25	ns
TCELRH	CEN to Command			TCLML	ns
TOLOH	Output Rise Time	From 0.8V to 2.0V		20	ns
TOHOL	Output Fall Time	From 2.0V to 0.8V		12	ns

For $\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: $I_{OL} = 32mA$, $I_{OH} = -5mA$, $C_L = 300pF$

For Other: $I_{OL} = 16mA$, $I_{OH} = -1.0mA$, $C_L = 80pF$

SWITCHING WAVEFORMS

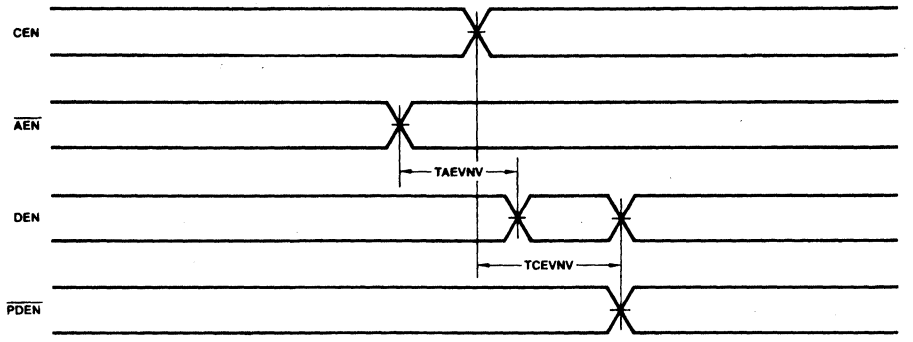


WF002110

Notes: 1. Address/data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3. All timing measurements are made at 1.5V unless specified otherwise.

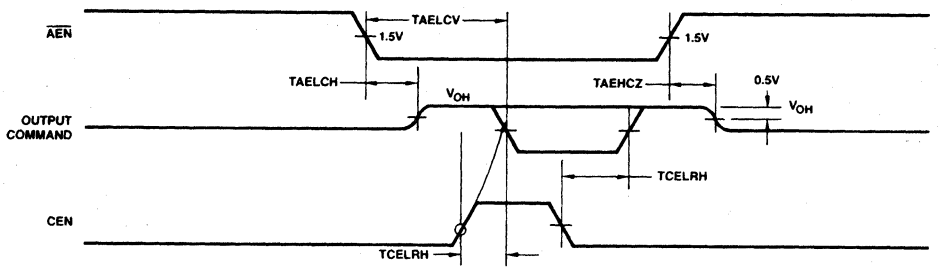
SWITCHING WAVEFORMS (Cont.)

DEN, PDEN QUALIFICATION TIMING



WF002040

ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



WF002050

Note: CEN must be low or valid prior to T_2 to prevent the command from being generated.

PALs, PROMs, MOS and Bipolar RAMs, MOS Peripherals, Analog and Data Acquisition

Bipolar PROM

Functional Index and Selection Guide

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments
Am27LS18[1]	32 x 8	50/65	80/80	OC	16	D,P,F,L	Low power
Am27LS19[1]	32 x 8	50/65	80/80	3S	16	D,P,F,L	
Am27S18	32 x 8	40/50	115/115	OC	16	D,P,F,L	
Am27S18A	32 x 8	25/35	115/115	OC	16	D,P,F,L	
Am27S19	32 x 8	40/50	115/115	3S	16	D,P,F,L	
Am27S19A	32 x 8	25/35	115/115	3S	16	D,P,F,L	
Am27S20	256 x 4	45/60	130/130	OC	16	D,P,F,L	
Am27S20A	256 x 4	30/40	130/130	OC	16	D,P,F,L	
Am27S21	256 x 4	45/60	130/130	3S	16	D,P,F,L	
Am27S21A	256 x 4	30/40	130/130	3S	16	D,P,F,L	
Am27S12	512 x 4	50/60	130/130	OC	16	D,P,F,L	
Am27S12A	512 x 4	30/40	130/130	OC	16	D,P,F,L	
Am27S13	512 x 4	50/60	130/130	3S	16	D,P,F,L	
Am27S13A	512 x 4	30/40	130/130	3S	16	D,P,F,L	
Am27S15	512 x 8	60/90	175/185	3S	24	D,P,F,L	
Am27S25	512 x 8	N.A.[2]/N.A.[2]	185/185	3S	24	D,P,F,L	Output registers, THINDIP Pkg[3]
Am27S25A	512 x 8	N.A.[4]/N.A.[4]	185/185	3S	24	D,P,F,L	Output registers, THINDIP Pkg[3]
Am27S27	512 x 8	N.A.[2]/N.A.[2]	185/185	3S	22	D,P,L	Output registers
Am27S28	512 x 8	55/70	160/160	OC	20	D,P,L	
Am27S28A	512 x 8	35/45	160/160	OC	20	D,P,L	
Am27S29	512 x 8	55/70	160/160	3S	20	D,P,L	
Am27S29A	512 x 8	35/45	160/160	3S	20	D,P,L	
Am27S30	512 x 8	55/70	175/175	OC	24	D,P,F,L	
Am27S30A	512 x 8	35/45	175/175	OC	24	D,P,F,L	
Am27S31	512 x 8	55/70	175/175	3S	24	D,P,F,L	
Am27S31A	512 x 8	35/45	175/175	3S	24	D,P,F,L	
Am27S32	1024 x 4	55/70	140/145	OC	18	D,P,F,L	
Am27S32A	1024 x 4	35/45	140/145	OC	18	D,P,F,L	Ultra fast
Am27S33	1024 x 4	55/70	140/145	3S	18	D,P,F,L	
Am27S33A	1024 x 4	35/45	140/145	3S	18	D,P,F,L	Ultra fast
Am27S35	1024 x 8	N.A.[2]/N.A.[2]	185	3S	24	D,P,F,L	Output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S35A	1024 x 8	N.A.[4]/N.A.[4]	185	3S	24	D,P,F,L	Ultra fast, output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S37	1024 x 8	N.A.[2]/N.A.[2]	185	3S	24	D,P,F,L	Output registers synchronous initialize, THINDIP Pkg[3]
Am27S37A	1024 x 8	N.A.[4]/N.A.[4]	185	3S	24	D,P,F,L	Ultra fast, output registers, synchronous initialize, THINDIP Pkg[3]
Am27S180	1024 x 8	60/80	185/185	OC	24	D,P,F,L	
Am27S180A	1024 x 8	35/50	185/185	OC	24	D,P,F,L	Ultra fast
Am27S181	1024 x 8	60/80	185/185	3S	24	D,P,F,L	
Am27S181A	1024 x 8	35/50	185/185	3S	24	D,P,F,L	Ultra fast
Am27PS181	1024 x 8	80/90	185/80[5]	3S	24	D,P,F,L	Power switched
Am27PS181A	1024 x 8	65/75	185/80[5]	3S	24	D,P,F,L	Power switched
Am27S280	1024 x 8	60/80	185/185	OC	24	D,P,F,L	THINDIP Pkg[3]
Am27S280A	1024 x 8	35/50	185/185	OC	24	D,P,F,L	Ultra fast, THINDIP Pkg[3]
Am27S281	1024 x 8	60/80	185/185	3S	24	D,P,F,L	THINDIP Pkg[3]

Refer to Page 13-1 for Essential Information on Military Devices

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments
Am27S281A	1024 x 8	35/50	185/185	3S	24	D,P,F,L	Ultra fast, THINDIP Pkg[3]
Am27PS281	1024 x 8	80/90	185/80[5]	3S	24	D,P,F,L	Power switched, THINDIP Pkg[3]
Am27PS281A	1024 x 8	65/75	185/80[5]	3S	24	D,P,F,L	Ultra fast, power switched, THINDIP Pkg[3]
Am27S184	2048 x 4	50/55	150/150	OC	18	D,P,F,L	
Am27S184A	2048 x 4	35/45	150/150	OC	18	D,P,F,L	Ultra fast
Am27S185	2048 x 4	50/55	150/150	3S	18	D,P,F,L	
Am27S185A	2048 x 4	35/45	150/150	3S	18	D,P,F,L	Ultra fast
Am27LS184	2048 x 4	60/65	120/125	OC	18	D,P,F,L	Low power
Am27LS185	2048 x 4	60/65	120/125	3S	18	D,P,F,L	Low power
Am27PS185	2048 x 4	60/65	150/75[5]	3S	18	D,P,F,L	Power switched
Am27S190	2048 x 8	50/65	185/185	OC	24	D,P,F,L	
Am27S190A	2048 x 8	35/50	185/185	OC	24	D,P,F,L	Ultra fast
Am27S191	2048 x 8	50/65	185/185	3S	24	D,P,F,L	
Am27S191A	2048 x 8	35/50	185/185	3S	24	D,P,F,L	Ultra fast
Am27PS191	2048 x 8	65/75	185/80[5]	3S	24	D,P,F,L	Power switched
Am27PS191A	2048 x 8	50/65	185/80[5]	3S	24	D,P,F,L	Ultra fast, power switched
Am27S290	2048 x 8	50/65	185/185	OC	24	D,P,F,L	THINDIP Pkg[3]
Am27S290A	2048 x 8	35/50	185/185	OC	24	D,P,F,L	Ultra fast, THINDIP Pkg[3]
Am27S291	2048 x 8	50/65	185/185	3S	24	D,P,F,L	THINDIP Pkg[3]
Am27S291A	2048 x 8	35/50	185/185	3S	24	D,P,F,L	Ultra fast, THINDIP Pkg[3]
Am27PS291	2048 x 8	65/75	185/80[5]	3S	24	D,P,F,L	Power switched, THINDIP Pkg[3]
Am27PS291A	2048 x 8	50/65	185/80[5]	3S	24	D,P,F,L	Ultra fast, power switched THINDIP Pkg[3]
Am27S40	4096 x 4	50/65	165/170	OC	20	D,P,L	
Am27S40A	4096 x 4	35/50	165/170	OC	20	D,P,L	Ultra fast
Am27S41	4096 x 4	50/65	165/170	3S	20	D,P,L	
Am27S41A	4096 x 4	35/50	165/170	3S	20	D,P,L	Ultra fast
Am27PS41	4096 x 4	50/65	170/85[5]	3S	20	D,P,L	Power switched
Am27S43	4096 x 8	55/65	185	3S	24	D,P,F,L	
Am27S43A	4096 x 8	40/55	185	3S	24	D,P,F,L	Ultra fast
Am27PS43	4096 x 8	N.A.	N.A.	3S	24	D,P,F,L	Power switched
Am27S45	2048 x 8	N.A.[2]	185/185	3S	24	D,P,L	Output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S45A	2048 x 8	N.A.[4]	185/185	3S	24	D,P,L	Ultra fast, output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S47	2048 x 8	N.A.[2]	185/185	3S	24	D,P,L	Output registers, synchronous initialize, THINDIP Pkg[3]
Am27S47A	2048 x 8	N.A.[4]	185/185	3S	24	D,P,L	Ultra fast, output registers, synchronous initialize, THINDIP Pkg[3]
Am27S65	1024 x 4	N.A.	185/185	3S	24	D,P	
Am27S65A	1024 x 4	N.A.	185/185	3S	24	D,P	
Am27S75	2048 x 4	N.A.	185/185	3S	24	D,P	
Am27S75A	2048 x 4	N.A.	185/185	3S	24	D,P	
Am27S85	4096 x 4	N.A.	185/185	3S	24	D,P	
Am27S85A	4096 x 4	N.A.	185/185	3S	24	D,P	
Am27S49	8192 x 8	55/65	190/190	3S	24	D,P,L	
Am27S49A	8192 x 8	40/55	190/190	3S	24	D,P,L	

Notes:
1. Replaces Am27LS08/09
2. Contains built-in pipeline registers: nominal address to clock setup time = 35ns (typ), clock to output = 20ns (typ).
3. 300-mil lateral pin spacing.
4. Contains built-in pipeline registers: nominal address to clock setup time = 25ns (typ), clock to output = 15ns (typ).
5. I_{CC} are power up and power down current limits respectively.

Refer to Page 13-1 for Essential Information on Military Devices

Bipolar Memory RAM

Functional Index and Selection Guide

BIPOLAR ECL RAM

Part Number	Organization	Access Time COM'L/MIL Max	I_{EE} COM'L/MIL Max	ECL Series	Number of Pins	Packages	Comments
Am10415SA	1024 x 1	15/20	-150/-165	10K	16	D,P,F,L	
Am10415A	1024 x 1	20/25	-150/-165	10K	16	D,P,F,L	
Am10415	1024 x 1	35/40	-150/-165	10K	16	D,P,F,L	
Am100415A	1024 x 1	15/-	-150/-	100K	16	D,P,F,L	
Am100415	1024 x 1	20/-	-150/-	100K	16	D,P,F,L	
Am10470SA	4096 x 1	15/20	-230/-255	10K	18	D,F[1],L	
Am10470A	4096 x 1	25/30	-200/-220	10K	18	D,F[1],L	
Am10470	4096 x 1	35/40	-200/-220	10K	18	D,F[1],L	
Am100470SA	4096 x 1	15/-	-230/-	100K	18	D,F[1],L	
Am100470A	4096 x 1	25/-	-195/-	100K	18	D,F[1],L	
Am100470	4096 x 1	35/-	-195/-	100K	18	D,F[1],L	
Am10474A	1024 x 4	15/20	-230/-255	10K	24	D,F,L	
Am10474	1024 x 4	25/30	-230/-220	10K	24	D,F,L	
Am100474A	1024 x 4	15/-	-230/-	100K	24	D,F,L	
Am100474	1024 x 4	25/-	-200/-	100K	24	D,F,L	
Am10480	16384 x 1	25/-	-200/-	10K	20	D,F,L	
Am10480A	16384 x 1	15/-	-230/-	10K	20	D,F,L	
Am100480	16384 x 1	25/-	-200/-	100K	20	D,F,L	
Am100480A	16384 x 1	15/-	-230/-	100K	20	D,F,L	

Note: 1. For Flat Package, Consult Factory.

Refer to Page 13-1 for Essential Information on Military Devices

BIPOLAR TTL RAM

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages (Note 1)	Comments
Am27S02A	16 x 4	25/30	100/105	OC	16	D,P,F,L	Ultra Fast
Am27S03A	16 x 4	25/30	100/105	3S	16	D,P,F,L	
Am27S02	16 x 4	35/50	105/105	OC	16	D,P,F,L	
Am27S03	16 x 4	35/50	125/125	3S	16	D,P,F,L	
Am27LS02	16 x 4	55/65	35/38	OC	16	D,P,F,L	Low Power
Am27LS03	16 x 4	55/65	35/38	3S	16	D,P,F,L	
Am74/54S289	16 x 4	35/50	105/105	OC	16	D,P,F,L	
Am74/54S189	16 x 4	35/50	125/125	3S	16	D,P,F,L	
Am27S06A	16 x 4	25/30	100/105	OC	16	D,P,F,L	Noninverting Outputs
Am27S07A	16 x 4	25/30	100/105	3S	16	D,P,F,L	
Am27S06	16 x 4	35/50	100/105	OC	16	D,P,F,L	
Am27S07	16 x 4	35/50	100/105	3S	16	D,P,F,L	
Am27LS06	16 x 4	55/65	35/38	OC	16	D,P,F,L	Noninverting Outputs, Low Power
Am27LS07	16 x 4	55/65	35/38	3S	16	D,P,F,L	
Am3101A	16 x 4	35/50	100/105	OC	16	D,P,F,L	
Am3101-1	16 x 4	35/50	100/105	OC	16	D,P,F,L	Write Transparent[2]
Am3101	16 x 4	50/60	100/105	OC	16	D,P,F,L	
Am31L01A	16 x 4	55/65	35/38	OC	16	D,P,F,L	Low Power Write Transparent[2]
Am31L01	16 x 4	80/90	35/38	OC	16	D,P,F,L	
Am74/5489-1	16 x 4	35/50	100/105	OC	16	D,P,F,L	Write Transparent[2]
Am74/5489	16 x 4	50/60	100/105	OC	16	D,P,F,L	
Am27LS00A	256 x 1	35/45	115/115	3S	16	D,P,F,L	Ultra Fast
Am27LS01A	256 x 1	35/45	115/115	OC	16	D,P,F,L	
Am29705A	16 x 4	28/30	210/210	3S	28	D,P,F,L	
Am29707	16 x 4	28/30	210/210	3S	28	D,P,F,L	
Am27LS00	256 x 1	45/55	70/70	3S	16	D,P,F,L	Fast, Low Power
Am27LS01	256 x 1	45/55	70/70	OC	16	D,P,F,L	
Am27LS00-1A	256 x 1	35/45	115/115	3S	16	D,P,F,L	Noninverting Outputs
Am27LS01-1A	256 x 1	35/45	115/115	OC	16	D,P,F,L	
Am27LS00-1	256 x 1	45/55	70/70	3S	16	D,P,F,L	
Am27LS01-1	256 x 1	45/55	70/70	OC	16	D,P,F,L	
Am93415A	1024 x 1	30/40	155/170	OC	16	D,P,F,L	Ultra Fast
Am93425A	1024 x 1	30/40	155/170	3S	16	D,P,F,L	
Am93415	1024 x 1	45/65	155/170	OC	16	D,P,F,L	
Am93425	1024 x 1	45/65	155/170	3S	16	D,P,F,L	
Am93412A	256 x 4	35/45	155/170	OC	22[3]	D,P,F,L	Ultra Fast
Am93422A	256 x 4	35/45	155/170	3S	22[3]	D,P,F,L	
Am93412	256 x 4	45/60	155/170	OC	22[3]	D,P,F,L	
Am93422	256 x 4	45/60	155/170	3S	22[3]	D,P,F,L	
Am93L412A	256 x 4	45/55	80/90	OC	22[3]	D,P,F,L	Low Power
Am93L422A	256 x 4	45/55	80/90	3S	22[3]	D,P,F,L	
Am93L412	256 x 4	60/75	80/90	OC	22[3]	D,P,F,L	
Am93L422	256 x 4	60/75	80/90	3S	22[3]	D,P,F,L	
Am93L425A	1024 x 1	45/55	65/75	3S	16	D,P,F,L	

Notes: 1. D = Hermetic DIP,P = Molded DIP,F = Cerpak,L = Chip-Pak™
2. Complement of data in is available on the outputs in the write mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Cerpak (F) is 24 pin.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

Refer to Page 13-1 for Essential Information on Military Devices

MOS Memory

Functional Index and Selection Guide

1K STATIC RAMS

Part Number	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package
			Standby	Active				
Am9122-25	256 x 4	25	–	660	22	5	C	D,P
Am9122-35	256 x 4	35	–	660	22	5	C,M	D,P
Am91L22-35	256 x 4	35	–	440	22	5	C	D,P
Am91L22-45	256 x 4	45	–	440	22	5	C,M	D,P
Am9122-60	256 x 4	60	–	248	22	5	C	D,P

4K STATIC RAMS

Part Number	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package
			Standby	Active				
Am2147-35	4096 x 1	35	165	990	18	5	C	D
Am2147-45	4096 x 1	45	165	990	18	5	M	D,L
Am2147-55	4096 x 1	55	165	990	18	5	C,M	D,L
Am2147-70	4096 x 1	70	110	880	18	5	C,M	D,L
Am21L47-45	4096 x 1	45	83	688	18	5	C	D
Am21L47-55	4096 x 1	55	83	688	18	5	C	D
Am2148-55	1024 x 4	55	165	990	18	5	C,M	D,L
Am2148-35	1024 x 4	35	165	990	18	5	C	D,L
Am2148-45	1024 x 4	45	165	990	18	5	C,M	D,L
Am2148-70	1024 x 4	70	165	990	18	5	C,M	D,L
Am2149-35	1024 x 4	35	N/A	990	18	5	C	D
Am21L48-45	1024 x 4	45	110	688	18	5	C	D,L
Am2149-45	1024 x 4	45	N/A	990	18	5	C,M	D
Am21L49-45	1024 x 4	45	N/A	688	18	5	C	D,L
Am21L48-55	1024 x 4	55	110	688	18	5	C	D,L
Am21L49-55	1024 x 4	55	N/A	688	18	5	C	D,L
Am21L48-70	1024 x 4	70	110	688	18	5	C	D,L
Am21L49-70	1024 x 4	70	N/A	688	18	5	C	D,L
Am9150-25	1024 x 4	25	N/A	990	24	5	C	D
Am9150-35	1024 x 4	35	N/A	990	24	5	C,M	D
Am9150-45	1024 x 4	45	N/A	990	24	5	C,M	D

16K STATIC RAMS

Part Number	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package
			Standby	Active				
Am9128-10	2048 x 8	100	165	660	24	5	C	D,P
Am9128-70	2048 x 8	70	165	770	24	5	C	D,P
Am9128-90	2048 x 8	90	165	990	24	5	M	D
Am2167-35	16384 x 1	35	165	660	20	5	C	D,P
Am2167-45	16384 x 1	45	83	660/880	20	5	C,M	D,P
Am2167-55	16384 x 1	55	83	660	20	5	C,M	D,P
Am2167-70	16384 x 1	70	165	660	20	5	C,M	D,P
Am2168-45	4096 x 4	45	165	550	20	5	C	D,P
Am2168-55	4096 x 4	55	165	550	20	5	C,M	D,P
Am2168-70	4096 x 4	70	165	550	20	5	C,M	D,P
Am2169-45	4096 x 4	45	NA	550	20	5	C	D,P
Am2169-55	4096 x 4	55	NA	550	20	5	C,M	D,P
Am2169-70	4096 x 4	70	NA	550	20	5	C,M	D,P

Refer to Page 13-1 for Essential Information on Military Devices

AMD 20-Pin PAL* Family

20-Pin IMOX™ Programmable Array Logic Elements

DISTINCTIVE CHARACTERISTICS

- **Fast**
  - High speed "A" versions (t_{pd} = 25ns, t_s = 20ns, t_{co} = 15ns, max)
  - Standard speed versions (t_{pd} = 35ns, t_s = 30ns, t_{co} = 25ns, max)
- **Flexible**
  - User programmability allows customized designs
  - Eases design updates in prototype or product
- **Low Cost**
  - Reduces board space/chip count
  - Reduces design time
  - Reduces inventory cost
- **Reliable**
  - Proven Platinum-Silicide fuse technology
  - Fully AC and DC tested
  - Preload of output registers allows full logical testing

GENERAL DESCRIPTION

AMD PALs are high speed electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely.

Initially the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate. An AND gate with all fuses blown will assume the logical true state. The outputs of the AND gates are connected to fixed OR gates. The only limitations imposed are the number of inputs to the AND gates (up to 16) and the number of AND gates per OR (up to 8).

The part types in the AMD PAL family are differentiated by the allocation of registered (with internal feedback) and combinatorial (bi-directional and dedicated) outputs. All combinatorial AMD PALs are available in both active HIGH (AND-OR) and active LOW (AND-OR-INVERT) versions.

AMD PAL FAMILY CHARACTERISTICS

All members of the AMD PAL family have common electrical characteristics and programming procedures. All parts in this family are produced with a fusible link at each input to the AND gate array. Connections may be selectively removed by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link programmable logic.

The AMD PAL family is manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AMD PAL family also incorporates the unique capability of preloading the output registers during testing to any desired value. Preload is invaluable when testing the logical functionality of a programmed AMD PAL.

AMD PAL FAMILY TABLE

Part Number	Array Inputs	Logic	OE	Outputs	t_{pd} (MAX) STD	t_{pd} (MAX) A	t_s (MAX) STD	t_s (MAX) A	t_{co} (MAX) STD	t_{co} (MAX) A	
AmPAL16R8	(8) Dedicated (8) Feedback	(8) 8-Wide AND-OR	Dedicated	Registered Inverting	–	–	30	20	25	15	ns
AmPAL16R6	(8) Dedicated (6) Feedback (2) Bidirectional	(6) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	ns
		(2) 7-Wide AND-OR-INVERT	Programmable	Bidirectional							
AmPAL16R4	(8) Dedicated (4) Feedback (4) Bidirectional	(4) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	n
		(4) 7-Wide AND-OR-INVERT	Programmable	Bidirectional							
AmPAL16L8	(10) Dedicated (6) Bidirectional	(8) 7-Wide-AND-OR-INVERT	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–		
AmPAL16H8	(10) Dedicated (6) Bidirectional	(8) 7-Wide AND-OR	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–	–	
AmPAL16LD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR-INVERT	–	Dedicated	35	25	–	–	–		
AmPAL16HD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR	–	Dedicated	35	25	–	–	–		

*PAL is a registered trademark of Monolithic Memories, Inc.
IMOX is a trademark of Advanced Micro Devices, Inc.

Refer to Page 13-1 for Essential Information on Milita

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 20 to Pin 10) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs (Except
During Programming) ..... −0.5V to +V_{CC} max
DC Voltage Applied to Outputs
During Programming 21V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) 200mA
DC Input Voltage ..... −0.5 to +5.5mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

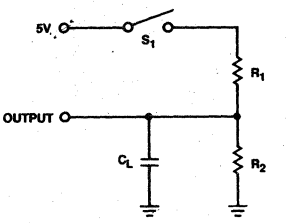
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2mA	COM'L	2.4	3.5		Volts
			I_{OH} = −2mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	COM'L			0.5	Volts
			I_{OL} = 12mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−20	−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V (Note 3)			−30	−60	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	16L8, 16H8, 16HD8, 16LD8 16L8A, 16H8A, 16HD8A, 16LD8A			110	155	mA
			16R8, 16R6, 16R4 16R8A, 16R6A, 16R4A			120	180	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = MAX, V_{IL} = 0.8V V_{IH} = 2.0V	V_O = 2.7V				100	μA
I_{OZL}			V_O = 0.4V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @f = 1MHz (Note 5)				6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @f = 1MHz (Note 5)				9		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

Refer to Page 13-1 for Essential Information on Military Devices

AC TEST LOAD



TC001190

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
HIGH SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A, 16LD8A, 16H8A, 16HD8A	COM'L $R_1 = 200$ $R_2 = 390$	12		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		8		15		20	ns
t_S	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A	MIL $R_1 = 390$ $R_2 = 750$	10	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A		-10	0		0		ns
t_P	Clock Period			35		45		ns
t_W	Clock Width			15		20		ns
t_{MAX}	Maximum Frequency				28.5		22	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

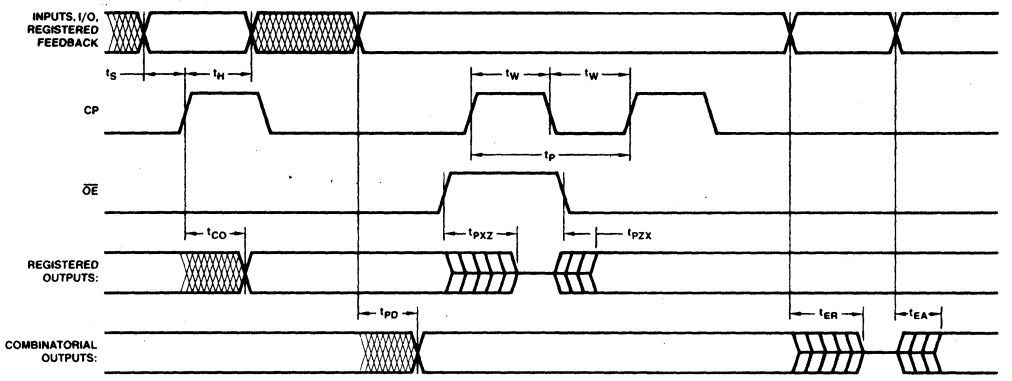
SWITCHING CHARACTERISTICS over operating range unless otherwise specified
STANDARD SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	COM'L $R_1 = 200$ $R_2 = 390$	17		35		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		12		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		12		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		12		25		25	ns
t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	MIL $R_1 = 390$ $R_2 = 750$	15	30		35		ns
t_H	Hold Time 16R8, 16R6, 16R4		-10	0		0		ns
t_P	Clock Period			55		60		ns
t_W	Clock Width			20		25		ns
f_{MAX}	Maximum Frequency				18		16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



WF002570

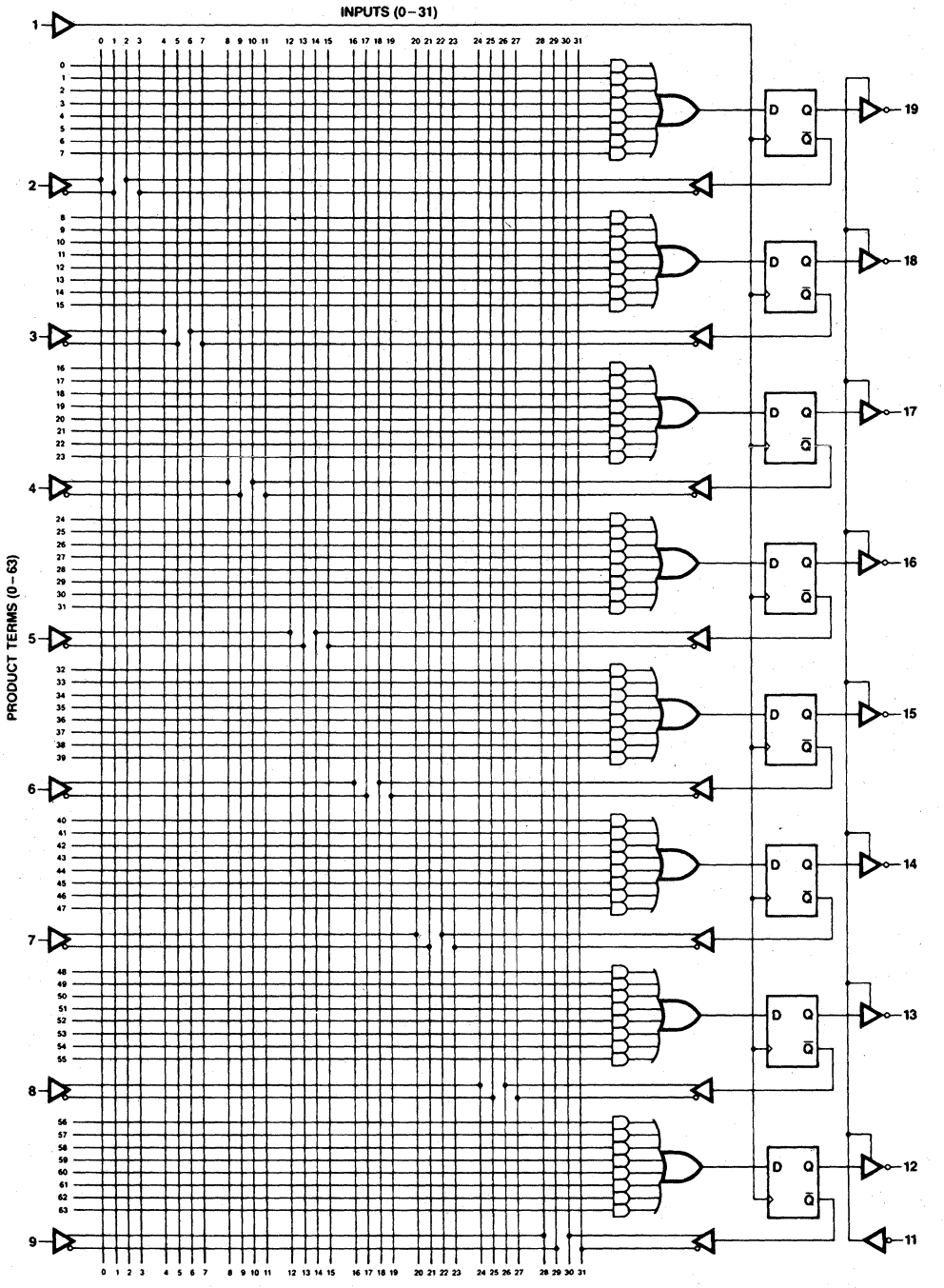
KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

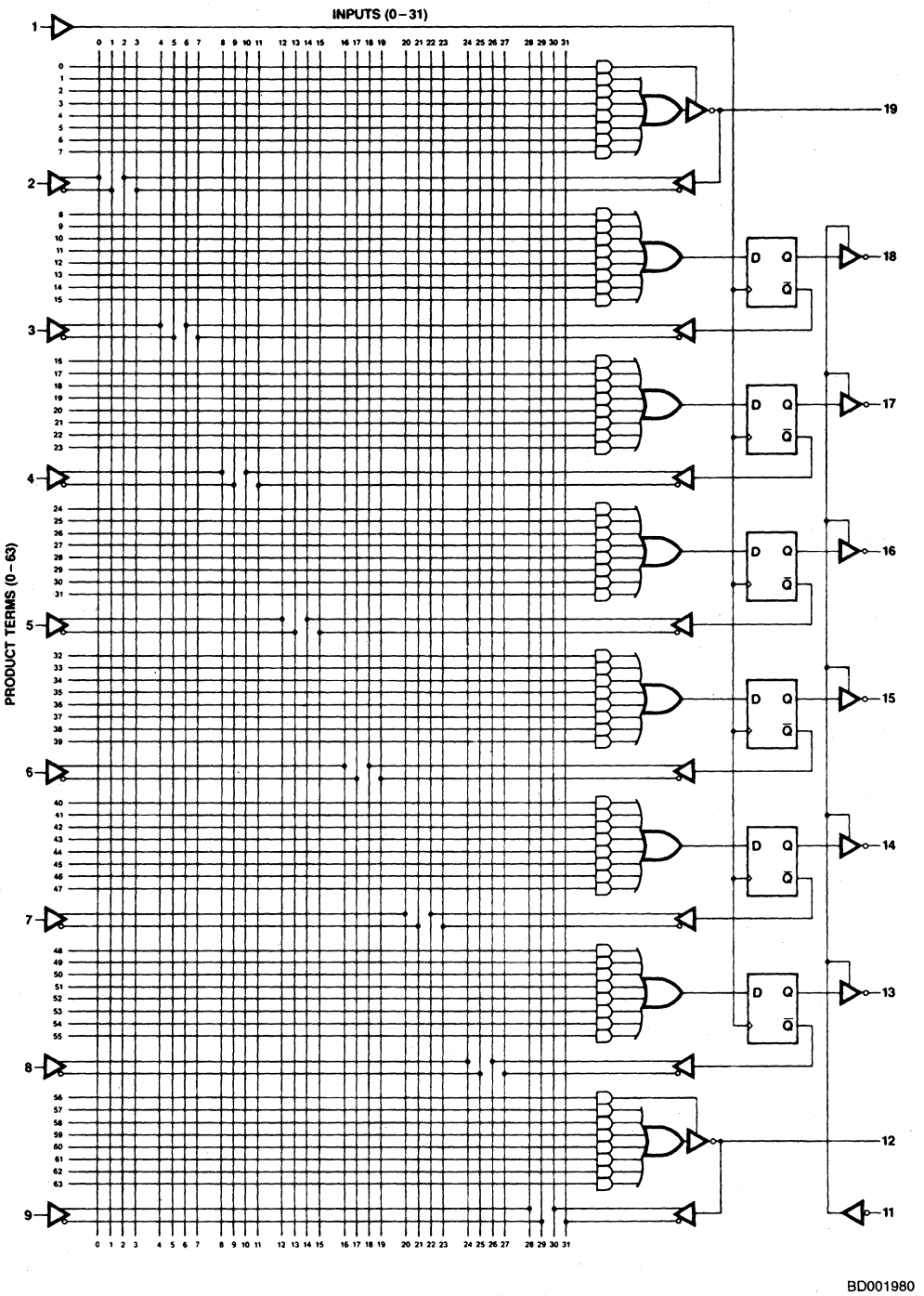
KS000010

Refer to Page 13-1 for Essential Information on Military Devices

BLOCK DIAGRAM AmPAL16R8/AmPAL16R8A

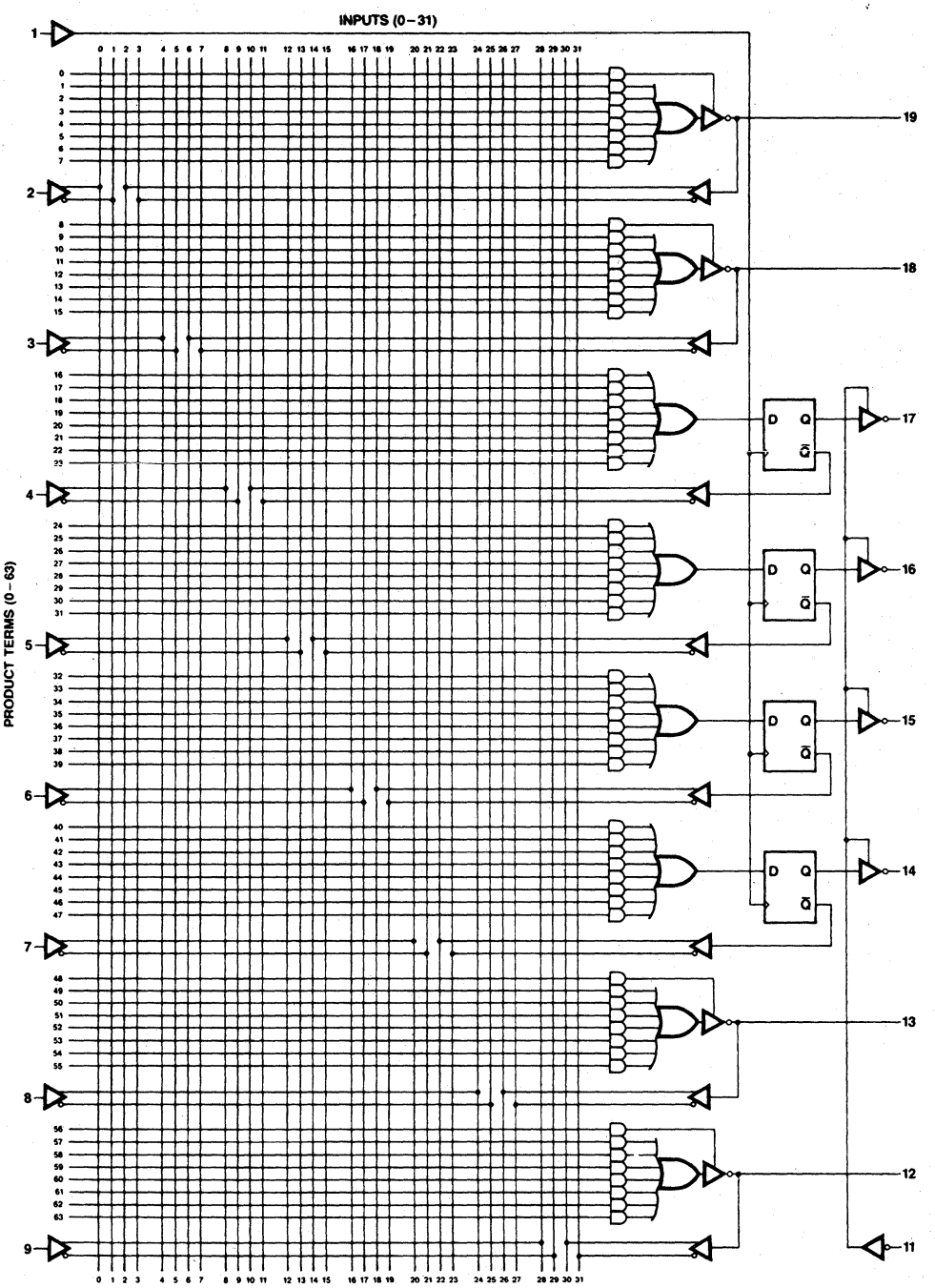


BLOCK DIAGRAM AmPAL16R6/AmPAL16R6A



Refer to Page 13-1 for Essential Information on Military Devices

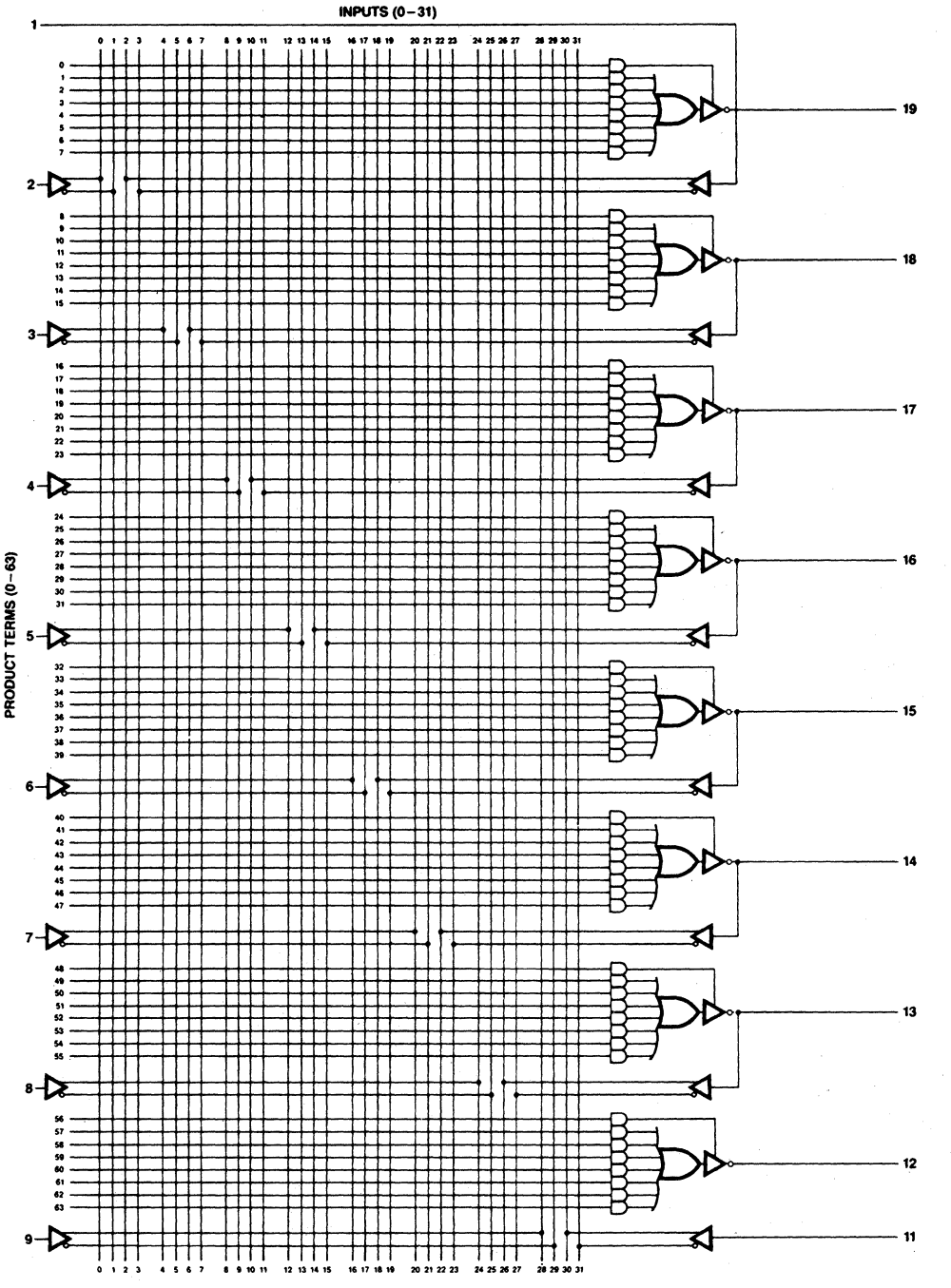
BLOCK DIAGRAM AmPAL16R4/AmPAL16R4A



BD001990

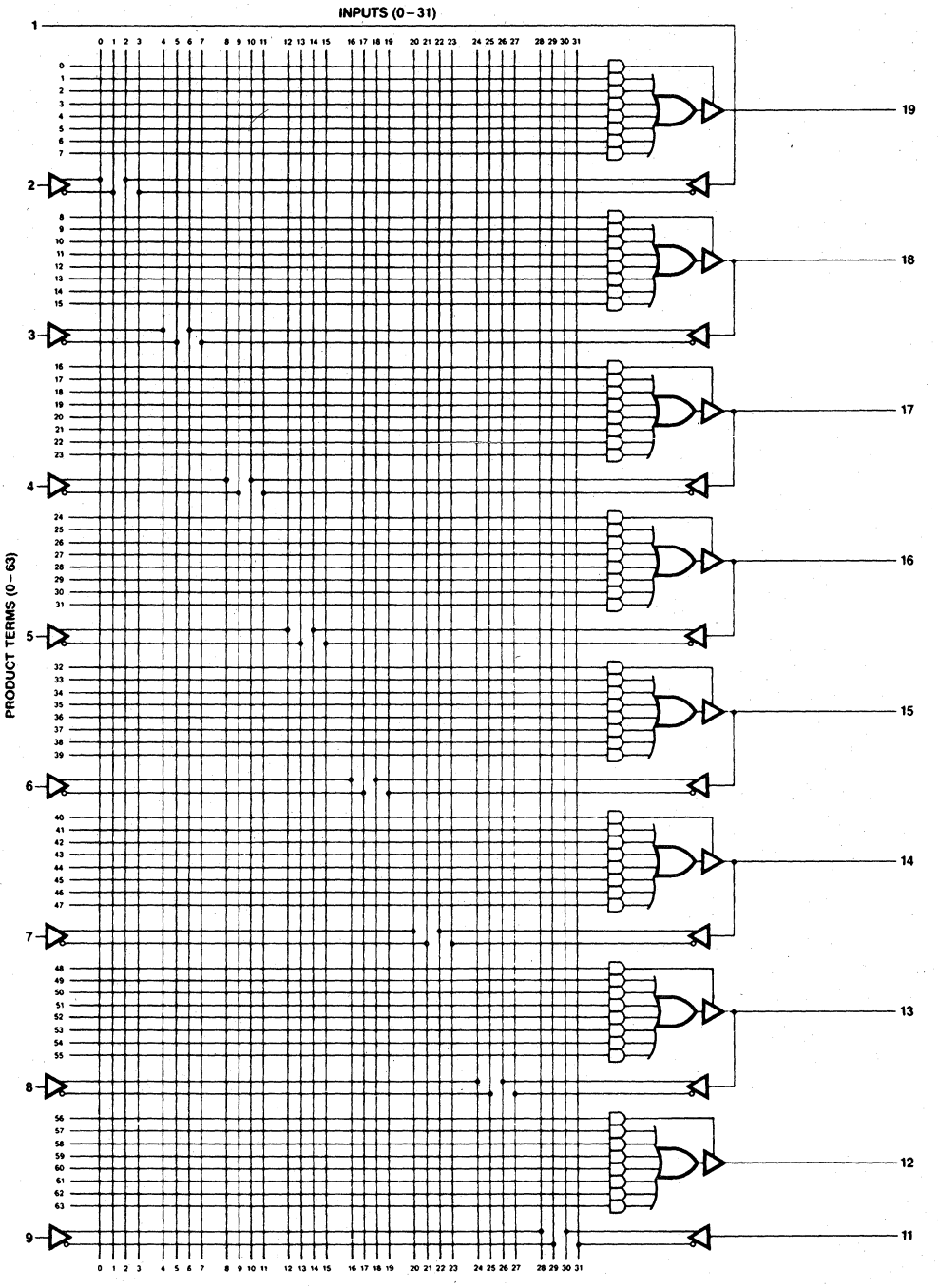
Refer to Page 13-1 for Essential Information on Military Devices

BLOCK DIAGRAM AmPAL16L8/AmPAL16L8A



BD002020

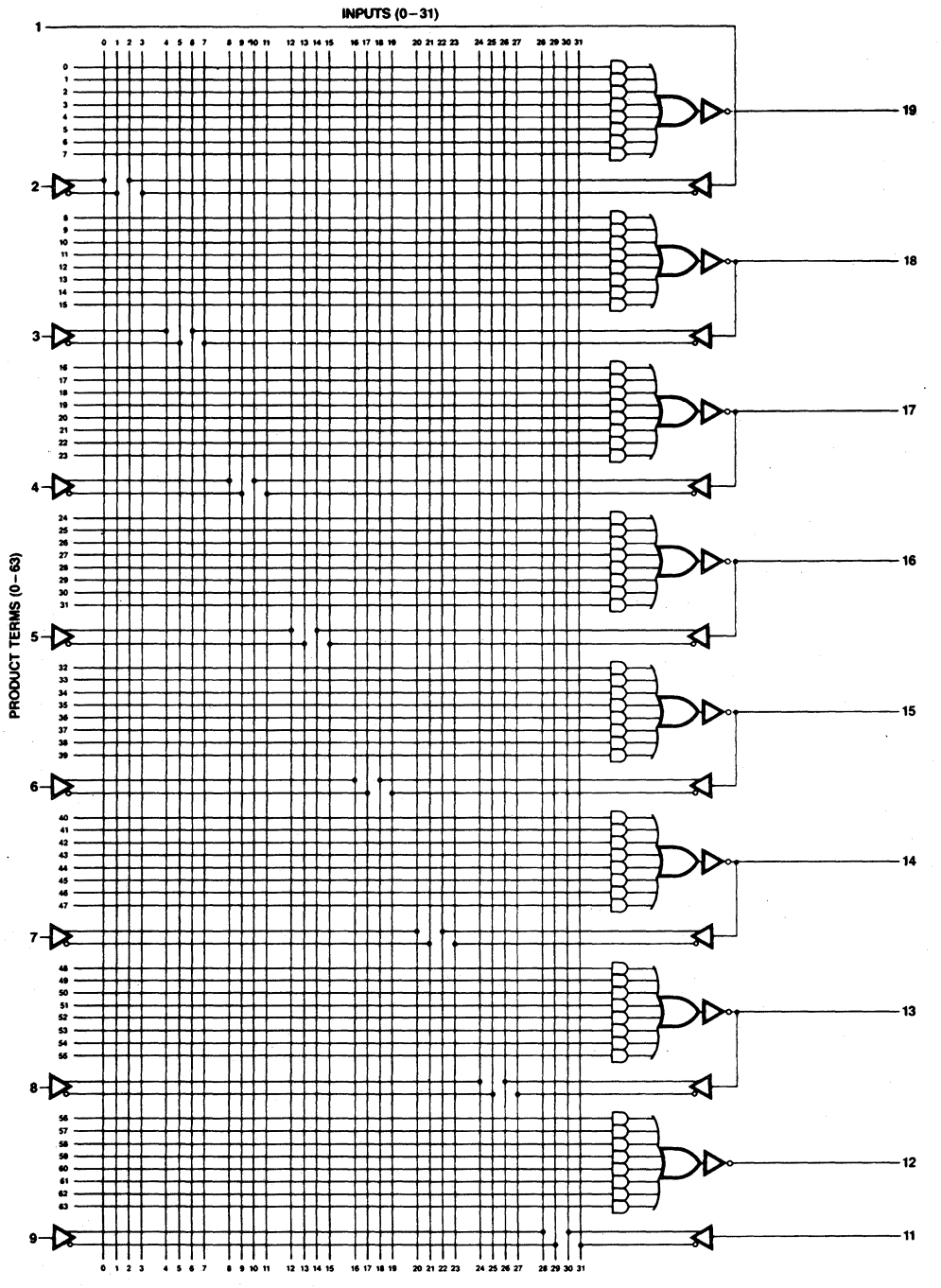
BLOCK DIAGRAM AmPAL16H8/AmPAL16H8A



BD002030

Refer to Page 13-1 for Essential Information on Military Devices

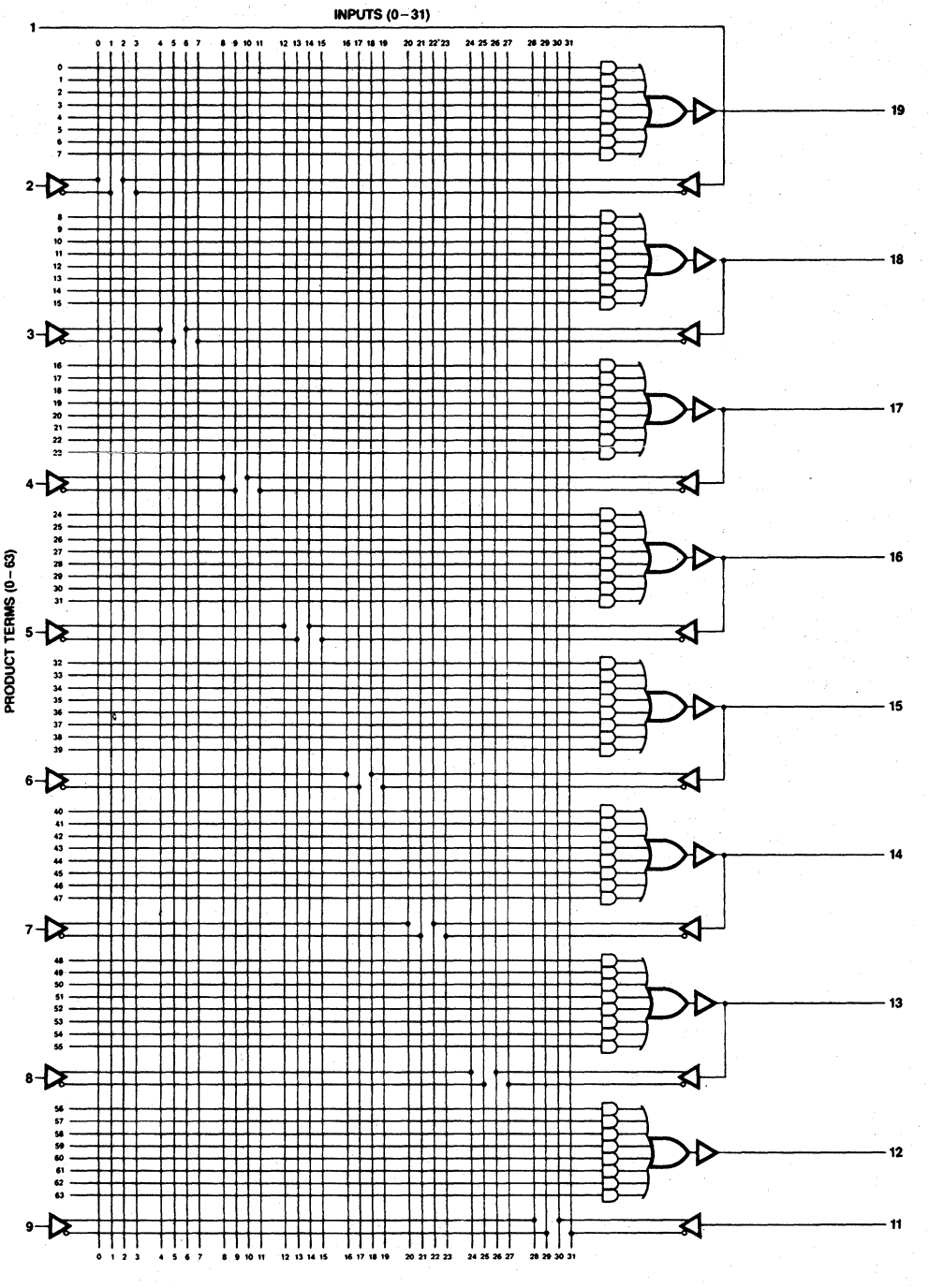
BLOCK DIAGRAM AmPAL16LD8/AmPAL16LD8A



BD002040

Refer to Page 13-1 for Essential Information on Military Devices

BLOCK DIAGRAM AmPAL16HD8/AmPAL16HD8A



BD002010

Refer to Page 13-1 for Essential Information on Military Devices

PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and a programming voltage pulse applied to the output under programming. Addressing of the 2048 element fuse array is accomplished with normal TTL levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle – no extra high levels are required.

The necessary sequence of levels for programming any fuse is shown in the Programming Timing Diagram. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table below.

The 16L8, 16R8, 16R6, 16R4, 16H8, 16LD8 and 16HD8 use identical programming conditions and sequences.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PALs have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:
1. Power up part to V_{CCP}
2. Raise Pin 5 to V_{HH}.
3. Pulse Pin 11 from ground to V_{OP} for a 50μsec duration.
4. Perform a normal end-of-programming verify cycle at V_{CCL} and V_{CCH}. All fuse locations should be sensed as blown if the security fuse has been successfully blown.

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PALs normally have high programming yields (> 98%). Programming yield losses are frequently due to poor socket contact, equipment out of calibration or improperly used.

PROGRAMMING PARAMETERS T_A = 25°C

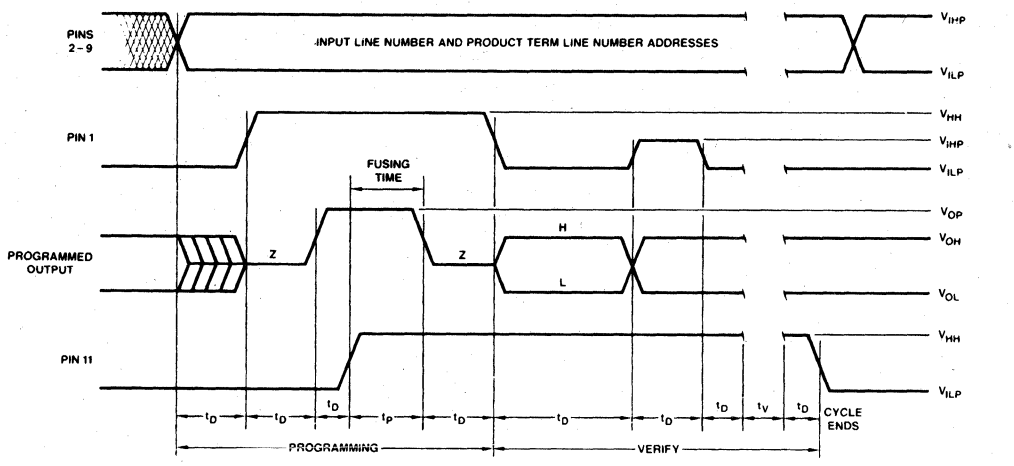
Parameters	Description		Min	Typ	Max	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 10-40mA	10	11	12	Volts
		Pin 11 @ 10-40mA	10	11	12	
V_{OP}	Program Voltage Pins 12-19 @ 15-200mA		18	20	22	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50-200mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50-200mA		4.1	4.3	4.5	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50-200mA		5.4	5.7	6.0	Volts
V_{Blown}	Successful Blown Fuse Sense Level @ Output	16L8, 16R8, 16R6, 16R4, 16LD8 16L8A, 16R8A, 16R6A, 16R4A, 16LD8A		0.3	0.5	Volts
		16H8, 16HD8, 16H8A, 16HD6A	2.4	3		
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/μsec
dV_{11}/dt	Rate of Fusing Enable Voltage Change (Pin 11 Rising Edge)		100		1000	V/μsec
t_p	Fusing Time First Attempt		40	50	100	μsec
	Subsequent Attempts		4	5	10	msec
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	KΩ

AMD PAL PROGRAMMING EQUIPMENT INFORMATION

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Kontron Electronics, Inc. 630 Price Avenue Redwood City, CA 94063	Stag Microsystems 528-5 Weddel Drive Sunnyvale, CA 94086
Programmer Model(s)	Model-100, 29, 19 or 17	Model-MPP-80S or EPP80	Model-PPX
AMD PAL Personality Module	Logicpak 950-1942-001	MOD-33	PPM2200
Socket Adapter	715-1947-003	SA37	Am202S

Refer to Page 13-1 for Essential Information on Military Devices

PROGRAMMING WAVEFORMS



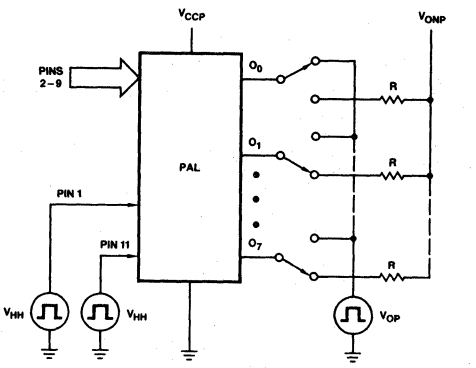
PF001100

TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States				
	9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

$L = V_{ILP}$
$H = V_{IHP}$

SIMPLIFIED PROGRAMMING DIAGRAM



PF000380

TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin		
								4	3	2
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12			
Programming Access and Verify Pin										

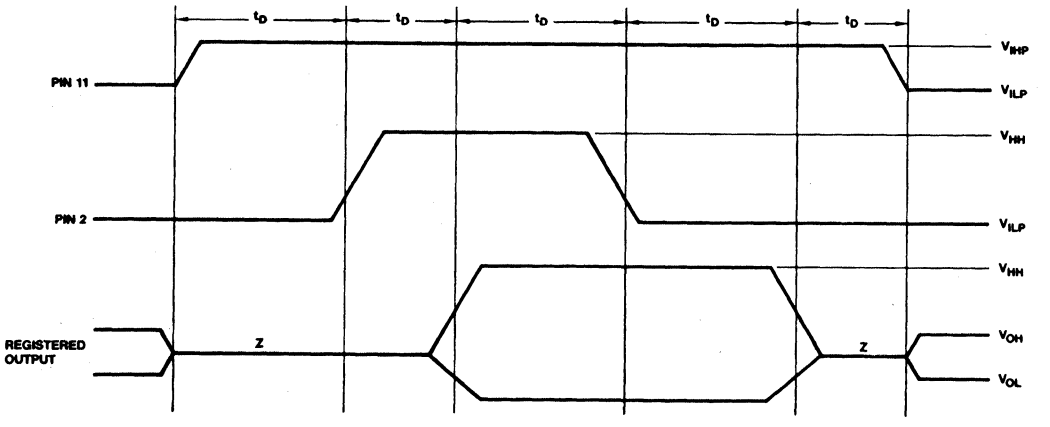
$L = V_{ILP}$
$H = V_{IHP}$

Refer to Page 13-1 for Essential Information on Military Devices

PRELOAD OF REGISTERED OUTPUTS

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



PF001160

Level forced on registered output pin during preload cycle	Output state at the output pin after cycle
V_{HH}	HIGH
0 V to V_{CCH} or OPEN	LOW

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

AmPAL XXXXX X X X X

- Screening
  - C = 883C Basic Flow
  - B = 883B (Burn-in)
- Temperature Range
  - C = Commercial
  - M = Military
- Package
  - P = Molded DIP (Commercial Only)
  - D = Hermetic DIP
  - L = Chip-Pak™
- Speed Selection
  - = Standard
  - A = High Speed
- Basic Device
  - 16R8
  - 16R6
  - 16R4
  - 16L8
  - 16H8
  - 16LD8
  - 16HD8

*Chip-Paks are rated a maxium case temperature only.

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Chip-pak is a trade mark of Advanced Micro Devices, Inc.

Refer to Page 13-1 for Essential Information on Military Devices

MOS Microprocessor

Family Selector Guide

	8086/88	8085A	8085A-2	8080A	Z8001/2†	Z8001/2-A
Clock Period	200ns	320ns	200ns	480ns	250ns	165ns
Clock Generator	8284A	On-Chip	On-Chip	8224	8127	8127
Arithmetic Processing Unit	8087	9511A-1 9512-1	9511A-4 9512-1	9511A 9512	9511A-4 9512-1	9511A-4 9512-1
Interrupt Controller	8259A-5	9519A 8259A	9519A-4 8259A-5	9519A 8259A	9519A-1	9519A-1
DMA Controller	8089 9516A 9517A-5	9517A-4	9517A-5	9517A	8016 9517A-4	8016A
Dynamic Memory Controller	2964B 2968	2964B 2968	2964B 2968	2964B 2968	2964B 2968	2964B 2968
Serial I/O	8251A 8530A 8030A	8251A 8530	8251A 8530A	8251A	8030	8030A
Parallel I/O	8255A-5 8036A	8255A-5	8255A-5	8255A	8036	8036A
Counter Timer I/O	9513 8036A 8073	9513 8253-5	9513 8253-5	9513 8253	8073	8073
FIFO I/O	8038	8038	8038	8038	8038	8038
Data Ciphering Processor	8068	8068	8068	9518	8068	8068
Error Detection and Correction	2960	2960	2960	2960	2960	2960
Burst Error Processor	8065 9520	8065 9520	8065 9520	8065 9520	8065 9520	8065 9520
CRT Controller	8275 8052	8275	8275	8275	8052	8052A
I/O Processor	8089	N/A	N/A	N/A	N/A	N/A
RAM I/O	N/A	8155/6	8155/6-2	N/A	N/A	N/A
Memory Management Unit	N/A	N/A	N/A	N/A	8010	8010A
Bus Control/ Arbiter	8288	N/A	N/A	N/A	N/A	N/A
Bus Latches	29841-6	29841-6	29841-6	29841-6	29841-6	29841-6
Bus Buffers	29827/28	2958/9	2958/9	2958/9	2958/9	2958/9
Bus Transceivers	29861-4	29861-4	29861-4	29861-4	29861-4	29861-4
EDC Buffers	2961/2	2961/2	2961/2	2961/2	2961/2	2961/2
RAM Drivers	2965/6	2965/6	2965/6	2965/6	2965/6	2965/6

†Z8000 is a trademark of Zilog, Inc.

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Microprocessor Components

Part Number	Description
SINGLE-CHIP MICROCOMPUTERS	
8031	8-Bit Microcomputer
8051	8-Bit Microcomputer with On-Board ROM
PERIPHERALS ADVANCED SYSTEM COMPONENTS	
Am9511A	Arithmetic Processor
Am9512	Arithmetic Processor
Am9513/A	System Timing Controller
Am9516	Data Transfer Controller
Am9517A	DMA Controller
Am9518/68	Data Ciphering Processor
Am9519A	Universal Interrupt Controller
Am9520	Burst Error Processor
Am9521	32-, 35-Bit Burst Error Processor
Am9551	Serial I/O USART
DISPLAY PRODUCTS	
Am8052	CRT Controller
Am8152	Video System Controller
Am8153	Video System Controller
iAPX86 FAMILY SYSTEM COMPONENTS	
8231A/9511A	Arithmetic Processor
8232/9512	Arithmetic Processor
8237A/9517A	DMA Controller
8251	Serial I/O USART
8251A	Serial I/O USART
8253	Counter/Timer
8255A	Programmable Peripheral Interface
8259A	Interrupt Controller
8284A	Clock Generator
8286	Octal Transceiver
8287	Octal Transceiver
8288	Bus Controller
AmZ8530	Serial Communications Controller
8155/H	RAM with I/O Ports
8156/H	RAM with I/O Ports
AmZ8536	Counter Timer and Parallel I/O Unit
Z8001/2 FAMILY SYSTEM COMPONENTS	
AmZ8016	Data Transfer Controller
Z8030	Serial Communication Controller
Z8031	Asynchronous Serial Communications Controller
Z8036	Counter I/O
Z8038	FIFO I/O Interface

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Part Number	Description
AmZ8065	Burst Error Processor
AmZ8068	Data Ciphering Processor
AmZ8073	System Timing Controller
Z8121	Octal Comparator
Z8127	Clock Generator & Controller
Z8163	Refresh & EDC Controller (16MHz)
Z8167	Refresh & EDC Controller (22 MHz)
NETWORKING FAMILY	
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7991	Serial Interface Adaptor (SIA)
CPU's	
Z8001	16-Bit CPU
28002	16-Bit CPU
8080A/9080A	8-Bit CPU
8086	16-Bit CPU
8088	8-Bit CPU
8085A	8-Bit CPU
Z8001/2 Family System Components	
8010	Memory Management Unit
8016	Data Transfer Controller
8030	Serial Communications Controller
8036	Counter I/O
8038	FIFO I/O Interface
8052	CRT Controller
8060	FIFO Buffer/FIO Expander
8065	Burst Error Processor
8068	Data Ciphering Processor
8073	System Timing Controller
26861-4	High Performance Bus Transceivers
8121	Octal Comparator
8127	Clock Generator and Controller
29827/28	High Performance Bus Buffers
8163	Refresh and EDC Controller (16 MHz)
8167	Refresh and EDC Controller (22 MHz)
29821-6	High Performance Bus Registers
29841-6	High Performance Bus Latches

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Part Number	Description
Bipolar Support Circuits	
25LS244	Octal Buffer
25LS2521	Octal Comparator
25LS2536	Octal Address Decoder
25LS2548	Octal Decoder with ACK
29821-6	High Performance Bus Registers
2925	Clock Generator
29861-4	High Performance Bus Transceiver
2948/49	Octal Bus Transceiver
2960	16-Bit Error Detection and Correction
2961/62	EDC Buffers
2964B	Dynamic Memory Controller
2965/66	RAM Drivers
29841-6	High Performance Bus Latches

Refer to Page 13-1 for Essential Information on Military Devices

Analog Data Acquisition Product Guide and Cross Reference

Part Number	Description
DIGITAL-TO-ANALOG CONVERTERS	
GENERAL PURPOSE 8-BIT	
DAC-08	Industry Standard 8-Bit Multiplying D/A
Am1508/1408	Multiplying D/A
SSS1508A/1408A	Multiplying D/A
MICROPROCESSOR COMPATIBLE 8-BIT	
Am6080	Contains 8-Bit Data Latch with Write, Chip Select and Data Enable Logic On-Chip
Am6081	Same as Am6080 Plus On-Chip Multiplexer
GENERAL PURPOSE 12-BIT	
Am6012	Low Cost, 250ns Setting Time, Multiplying 12-Bit D/A
Am6022*	High-Speed Version of Am6012, 75ns Setting Time
MICROPROCESSOR COMPATIBLE 12-BIT	
Am6082*	Contains Reference, Double Buffered Latch, Control Logic and High-Speed Op Amp. 150ns Current or 400ns Voltage Setting Time
GENERAL PURPOSE 14-BIT	
Am6014*	14-Bit Plus Sign Multiplying D/A, 500ns Setting Time
COMPANDING	
Am6070	8-Bit, 72dB of Dynamic Range for Control Systems
Am6072	8-Bit, μ-Law for PCM Communication Systems
ANALOG-TO-DIGITAL CONVERTERS	
HIGH SPEED 4-BIT	
Am6688	100MHz Sampling Rate, 8-Bit Accuracy, Flash Converter
HIGH SPEED 6-BIT	
Am6606*	100MHz Sampling Rate, 8-Bit Accuracy, Flash Converter
HIGH-SPEED MICROPROCESSOR COMPATIBLE 8-Bit	
Am6108/6148**	1μs Conversion Time, Contains Reference, DAC, Comparator, SAR, Scale Resistors, 3-State Buffers and Control Logic
HIGH-SPEED MICROPROCESSOR COMPATIBLE 12-Bit	
Am6112	3μs Conversion Time, Contains Reference, DAC, Comparator, SAR, Scale Resistors, 3-State Buffers and Control Logic
SAMPLE AND HOLD AMPLIFIERS	
GENERAL PURPOSE	
LF198/398	Less than 10μs Acquisition Time, Industry Standard Sample and Hold
HIGH-SPEED	
Am6420*	500ns Acquisition Time, 10ns Aperture Delay, 0.01% Linearity Error

*In development.
**Am6148 is the slim 24-pin, 0.3" version of the Am6108.

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VOLTAGE COMPARATORS

Am685	5ns Propagation Delay, ECL Output
Am686	12ns Propagation Delay, TTL Output
Am687	8ns Propagation Delay, Dual 685, ECL Output
Am1500/ LH2111	Dual Precision
LM111/311	High Accuracy, Low Cost
LM119	Dual High Speed, ±5V to ±15V Supply
LM139	Quad, Low Power, High Accuracy

OPERATIONAL AMPLIFIERS

LF155/156	FET-Input, High Slew Rate and Fast Setting Time
LM108	Low Power, ±2V to ±20V Supply
LM118	High Speed, 15MHz Bandwidth
LM148	Quad, Low Power 741

CROSS REFERENCE

AMD	National	Fairchild	Signetics	PMI	Motorola	Raytheon	Analog Devices
DAC-08AQ DAC-08HQ DAC-08HN	DAC0800LAJ DAC0802LCJ DAC0802LCN	µA0801ADM µA0801HDC µA0801HPC	SE5009F NE5009F NE5009N	DAC-08AQ DAC-08HQ DAC-08HP	DAC-08AQ DAC-08HQ DAC-08HP	DAC-08ADM DAC-08HDM DAC-08HBM	ADDAC-08AD ADDAC-08HD –
DAC-08Q DAC-08EQ DAC-08EN	DAC0800LJ DAC0800LCJ DAC0800LCN	µA0801DM µA0801EDC µA0801EPC	SE5008F NE5008F NE5008N	DAC-08Q DAC-08EQ DAC-08EP	DAC-08Q DAC-08EQ DAC-08EP	DAC-08DM DAC-08EDM DAC-08EBM	ADDAC-08D ADDAC-08ED –
DAC-08CQ DAC-08CN	DAC0801LCJ DAC0801LCN	µA0801CDC µA0801CPC	NE5007F NE5007N	DAC-08CQ DAC-08CP	DAC-08CQ DAC-08CP	DAC-08CDM DAC-08CBM	ADDAC-08CD –
AM1508L8 AM1408L8 AM1408N8	DAC0808LJ DAC0808LCJ DAC0808LCN	µA0802DM µA0802ADC µA0802APC	MC1508-8F MC1408-8F MC1408-8N	– – –	MC1508L8 MC1408L8 MC1408P8	– – –	AD1508-8D AD1408-8D –
AM1408L7 AM1408N7	DAC0807LCJ DAC0807LCN	µA0802BDC µA0802BPC	MC1408-7F MC1408-7N	– –	MC1408L7 MC1408P7	– –	AD1408-7D –
AM1408L6 AM1408N6	DAC0806LCJ DAC0806LCN	µA0802CDC µA0802CPC	MC1408-6F MC1408-6N	– –	MC1408L6 MC1408P6	– –	– –
SSS1508A-8Q SSS1408A-8Q SSS1408A-7Q SSS1408A-6Q	– – – –	– – – –	– – – –	SSS1508A-8Q SSS1408A-8Q SSS1408A-7Q SSS1408A-6Q	– – – –	– – – –	– – – –
AM6012ADM AM6012ADC AM6012APC AM6012DM AM6012DC AM6012PC	– – – – – –	– – – – – –	– – – – – –	– – – DAC312BR DAC312FR –	– – – – – –	– – – – – –	– – – – – –
AM6070ADM AM6070ADC AM6070DM AM6070DC	– – – –	– – – –	– – – –	DAC-76BX DAC-76EX DAC-76X DAC-76CX	– – – –	– – – –	– – – –
AM6072DM AM6072DC	– –	– –	– –	– DAC-86EX	– –	– –	– –
AM6080 AM6081	DAC0830/1/2† –	– –	NE5018/19† –	DAC-808/888† –	– –	– –	AD558† –
AM6688	–	–	–	–	MC6108	–	–
AM6108	ADC0820†	–	–	–	–	–	AD570† AND AD7574†
AM6148	ADC0820†	–	–	–	–	–	
LF198	LF198	µAF198	NE5537	–	–	–	–

†Functional equivalent only

General Information Index

INFORMATION ON MILITARY DEVICES

Advanced Micro Devices is currently updating its parts listing to identify those devices which are fully compliant with MIL–STD–883, Revision C, Notice 2. For further information, including a current listing of military flows, and to answer questions regarding specific AMD parts, please contact your local AMD sales representative.

Guidelines on Testing Am2900 Family Devices

I. INTRODUCTION

The Am2900 Family represents a major step forward in bipolar technology, in that each device contains a number of MSI-type functions interconnected on one chip. The gate counts in the parts comprising the Am2900 Family are around 10-100 times the gate count of MSI functions. While this produces a number of advantages for manufacturing, such as reduced component count and lower costs, it complicates the incoming-inspection problem because test programs tend to be long and complex and must be carefully designed to insure that *all bad parts are rejected and most good parts are accepted.* While stating these two criteria is simple, reducing them to practice is not. LSI devices are not as "forgiving" of simplifications in test patterns and assumptions about forcing functions and noise levels, as their simpler counterparts. These notes are intended to point out some common areas of difficulty and their solutions.

II. THE PURPOSE OF TESTING

Testing is performed at most facilities during an inspection of purchased material. The reason, of course, is that it is much less expensive to screen parts then, than it is to troubleshoot and repair completed boards. Ideally, all the parts passed by incoming inspection will work in the system. This is insured through a specification which defines the way the part must behave in the system, and the incoming test should confirm that devices received meet the specification. The incoming test should not reject devices which meet the specification. When test programs are too tight or test for conditions not contained in the specification, delays in shipments occur and significant costs are incurred by both the vendor and the buyer trying to resolve "correlation problems."

III. GUARANTEEING THAT THE PARTS WORK

One step in testing devices is to perform DC parametric tests: I_{CC}, V_{OH}, V_{OL} and the like. These tests on bipolar LSI are not really different from those performed on simpler TTL devices, except that the number of pins involved is greater, and more complex set-ups may be required to put outputs in the proper state for testing. Another step is functional testing, and for bipolar LSI, function tests are significantly different than for MSI. The function tests must first insure that the device is capable of working, i.e., it's hooked up correctly inside. These kinds of tests can be described as "stuck-at-one, stuck-at-zero" tests, because they are designed to exercise each gate in the part. Even for a part as complex as the Am2901, the "stuck-at" tests can be performed quickly. Less than 400 test patterns must be applied to the part to exercise every gate.

But, "stuck-at" tests make an assumption: if a gate works, then it works regardless of the state of other gates in the circuit. Each gate is treated independently, but, in the integrated circuit, no gate is an island. The performance of one gate can, in fact, depend on the states of surrounding gates, because they share common inputs or common ground lines.

These possible faults are often not tested by "stuck-at" tests, because they are not independent of the state of surrounding logic. These potential faults depend on the physical and logical construction of the circuit. They are usually called "pattern sensitivities." Pattern-sensitive faults, like the two described above, are not something new. All digital products exhibit pattern sensitivities – even SSI. But, on simpler parts, either traditional "stuck-at" tests happen to find most of them, or the parts are easy enough to test that all possible data patterns are generated during testing. Neither of these circumstances is true for bipolar LSI. A special effort must be made to apply many data patterns to the devices to check for pattern-sensitive faults. This has been done for years with RAM patterns such as GALPAT. It must now be done with logic functions as well.

In the devices in the Am2900 Family, as with RAMs, testing all possible data patterns is not practical, but, the various MSI kinds of functions in the devices (register, ALU, multiplexer, etc.) can generally be logically isolated, and each of those functions should be checked independently for all possible data patterns. This principle works because (1) as a rule, it is possible to control the MSI functions in a 2900 part with some degree of independence, and (2) the MSI functions are usually physically separated on the die, so that a data pattern within one MSI block will not exhibit pattern sensitivity dependent on the data in another MSI block.

In the Am2901, for example, ALU tests using the two RAM ports as data sources are unlikely to be affected by the state of the data inputs or the Q register. The shift multiplexer at the input of the RAM is unlikely to be affected by the Q register or the ALU source-select multiplexers. The control logic for the ALU source multiplexers should not be affected by anything in the ALU. By applying these kinds of principles intelligently, function tests can be constrained to a few thousand tests which provide a very high confidence level that the part is not subject to pattern-sensitive faults within its operating range.

As an example of the test philosophy used on these parts, the function tests for the Am2901 are described below.

Am2901 FUNCTION TEST DESCRIPTION

The following describes the function tests performed on the Am2901. The $\overline{OE}$ pin is low during the entire function tests and each test gets one clock pulse.

A-Port GALPAT via ALU

These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the same as the A-address and OP code 337 is used for a write operation, while OP code 134 is used for a read operation. The four shift-operation pins, Q_0, Q_3 RAM_0 and RAM_3, are ignored.

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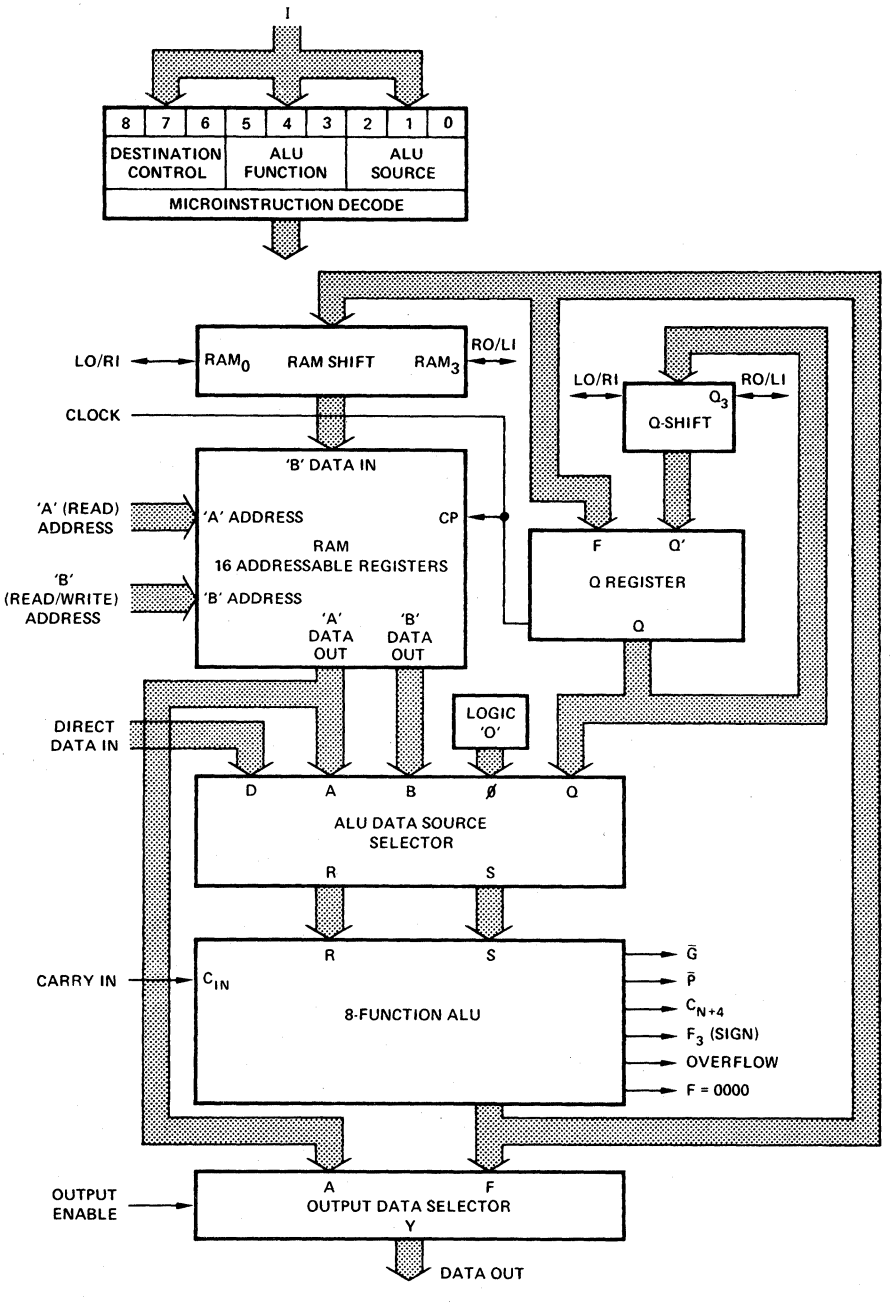

AF001680

THE Am2901 4-BIT MICROPROCESSOR SLICE

B-Port GALPAT via ALU

These are tests in which the B-address of the 2-port RAM is tested for Galloping "ones" in a field of "zero." During these tests, the A-address is the inverse of the B-address and OP code 337 is used for a write operation while OP code 133 is used for a read operation. The four shift-operation pins, Q_0, Q_3 RAM_0 and RAM_3, are ignored.

A-Port GALPAT Bypass ALU

These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the inverse of the A-address and OP code 337 is used for a write operation while OP code 233 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

Repeat 1 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat item 2 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat item 3 above by inverting Data and Y output information on D_{3-0} and Y_{3-0}. All the other outputs are ignored. This is Galloping "zeros" in a field of "ones" for A-Port bypass ALU.

ALU Source Code

During these tests, the A- and B-addresses are at word locations preloaded with known values. The Q register is also preloaded. Then, with the ALU destination OP code = 1 (No-OP) and the ALU function code = 6 (exclusive OR), the source code is cycled through from 0-7. The function code is then modified to 7 (exclusive NOR) and the source code sequence is cycled through once more.

ALU Function Code

During these tests, the memory is preloaded with content equal to the address. In other words, word 0 is loaded with 0, word 1 with 1, and so on. Then, with A-address = B-address, a destination OP code of 1 (No OP), and a source OP code of 1 (A&B Port selected), the ALU function code is cycled through the sequence of 7, 5, 4, 0, 1, 3, 2, 6 for every set of A&B address. This whole sequence is then repeated with A-address equal to the inverse of the B-address.

Arithmetic Operation & Carry Generation

During these tests, the memory is preloaded with content address. With OP code 105, whereby D input is added to the A-Port of the memory, the tester cycles through every possible D input added to every word in memory with carry in being both one and zero.

Q Register Operation

During these tests, the Q register is first loaded with all zeros. Then, with Cn = LOW and with OP code 006, whereby Q register is loaded with the sum of data input and Q-register content on every clock cycle, the device is clocked through all possible data inputs. The Cn input is then changed to a HIGH, and with OP code 016 whereby Q register is loaded with the difference of Q-D. The device is clocked through all possible data input again. This checks both the add and subtract modes of the ALU, the internal-carry-lookahead circuitry and the Q-register operation.

Q Register Shifting

During these tests, a unique string of data (11100001 010011011110) is shifted into the appropriate shift inputs. OP codes used in this group of tests are 432 for shift left, 532 for no shift, 632 for shift right and 732 for no shift.

RAM Shifting

During these tests, A- and B-addresses are at word 0. A string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used are 434 and 533 for left shift, 634 and 733 for right shift.

IV. AVOIDING THE REJECTION OF GOOD DEVICES

Discrepancies in testing results between the vendor and the buyer result in much irritation and substantial costs for both. Some of the common sources of these discrepancies are discussed below.

Testing for Unspecified or "don't care" Conditions

The data sheet (or purchase specification) defines the characteristics of the part. It is hard enough to test for everything specified without adding additional tests for unspecified parameters. If the state of an output is not specified under certain conditions, then it should not be tested.

Noise

Many testing problems result from noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path, is the source of these problems.

When the inputs to the device are changed there is a sequence of rapid changes in the device's ground current as signals propagate through internal gates to the outputs. These appear as changes in the voltage drop across the device ground lead. This voltage drop can be as much as 2 volts across a few inches of wire. Rise times are on the order of 1nsec and pulse widths range from 2 to 10nsec. Output transient current during switching may be 50 to 100mA. The test systems input and output reference voltages are set with respect to tester ground and are not affected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt.

This must be considered in selecting levels for V_{IL} and V_{IH}. The device data sheet says V_{IL} must be less than 0.8V and V_{IH} more than 2.0V. But this is as measured at the device package pins, between input and ground. This means that if the ground varies ±0.5 volt the input levels must be $V_{IL} \leqslant 0.3V$ and $V_{IH} \leqslant 2.5V$. If this is not done, a noise pulse could, for example, make the clock input effectively go high in the middle of the clock low time, causing an extra clock pulse. A similar situation exists at the device outputs, requiring V_{OL} to be set higher, and V_{OH} lower, than the data sheet numbers. AMD uses $V_{IL} = 0V$, $V_{IH} = 3V$, $V_{OL} = 1V$, $V_{OH} = 2V$ for functional tests.

Proper observations are important to the understanding and control of these problems. Small changes in timing, bypass capacitors, etc. will have large effects on the noise. An oscilloscope of 200 MHz or greater bandwidth is essential. Noise voltage should be measured at the device ground pin (at the device package edge, not the bottom of the test socket). Connect the probe ground to the tester chassis. In order to see the peak noise voltage, cycle the tester through a long

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pattern. Trigger the scope internally from the noise waveform. Turn the trigger level slowly up until the trace is almost lost. The peak noise voltage will appear at the left side of the screen. Sweep speed should be about 10nsec/div. Repeat for the peak of the opposite polarity.

Another useful technique is to identify a particular test pattern location which causes significant noise. Sync the oscilloscope to this test cycle. Using a two channel scope, connect one channel to an input pin and the other channel to the device ground pin. Invert the channel on the ground pin and add the two channels. The waveform will show the effective input levels.

An additional problem is introduced by I/O pins. When output load circuits are connected to these pins the tester must drive the load and the device when the pins are inputs. If the tester has a driver impedance of 50 ohms and the load supplies 16mA into V_{OL}, the input level produced will be 0.8V too high. This must be compensated by further reducing the programmed V_{IL} for only the I/O pins. Some devices are sensitive to input voltages below ground.

Guidelines

If the tester does not provide suitable alternate driver supplies, it may be necessary to provide resistor pullups for input-only pins.

The same ground lead inductance problems causes difficulties in DC testing. Many DC tests require some functional sequence to produce the correct device state. The input levels must be such to avoid false clocks, etc. DC tests may be used to verify input threshold levels. To do this, an output test such as V_{OL} or V_{OH} is selected where the outputs combinatorally depend on the inputs. Using non-threshold levels the appropriate input conditions are applied. The input levels are then reprogrammed to threshold levels. The outputs are then measured for V_{OL} or V_{OH}. It is not possible to do the functional set-up with threshold levels, even if it is only a single line, as oscillations may occur. Switching between alternate driven supplies also may generate sufficient noise to cause problems.

AC Testing

Many modern testers allow switching tests to be performed during the application of complex test sequences. The switching and function tests can then occur together. Unfortunately, this blurs the distinction between functional failure and switching-speed failure when a device is rejected, so, it is a good idea to do some preliminary function testing with "loose" AC limits before trying to do everything at once. When function and AC testing are combined, it is important to consider the *driving conditions* under which the AC parameters are tested. Switching measurements on Bipolar ICs are usually made with input levels switching between 0V and 3.0V (sometimes 0.4V and 2.4V are used). The output transition is measured at 1.5V (sometimes at 1.3V).

They are never specified at threshold levels (0.8V and 2.0V) because of noise problems.

Realistic AC tests require sequencing through many lines of test patterns to include a variety of data patterns. Unfortunately the AC accuracy of most modern logic testers is not as good as memory testers. There are often significant differences between different waveform formats. The position of an edge may depend on whether adjacent pins are switching and whether they are going up or down. This limits the accuracy of testing, especially for such parameters as hold times, where tester error usually exceeds the difference between device typical and data sheet maximum. This may be observed on an oscilloscope by cycling the tester and synchronizing the scope to a repetitive pulse, such as the device clock pin.* Do not trigger the scope on any particular tester cycle. Observing a device input on the second scope channel will show many overlapping transitions, positive and negative. The width of this band must be added to other error sources to determine tester accuracy.

Temperature Testing

Integrated circuits are specified to operate over either the commercial range of 0°C to +70°C or the military range of −55°C to +125°C. Standard screening procedures (from MIL-STD-883) call for 100% testing at 25°C followed by sample testing at the high and low temperature. Many users duplicate this test sequence in their incoming inspection, and some test 100% at temperature.

Testing problems are rarely encountered at low temperatures, if care is taken to prevent ice formation on the test socket. At high temperature, difficulties may arise because of the difficulty in creating a test environment which is representative of the thermal conditions found in the system.

High temperature testing with a controlled ambient temperature is very difficult because the thermal coefficient between the package and the surrounding environment depends on humidity, rate of air flow, package color, connections to package pins, and position of surrounding devices. For testing purposes, only the case temperature can really be controlled. (Most systems' thermal engineering is also designed to control case temperatures.)

V. INCOMING INSPECTION AND TESTING SUPPORT PRODUCTS

AMD provides several products to assist in the development of incoming inspection testing for most Am2900 LSI devices. See the table on the following page for specifics by device.

Sentry Test Programs

These are complete data sheet function, DC and AC parameter programs. They run on a Fairchild Sentry VII with low voltage test heads, 4K local memory and SPM. Complete load board documentation is included. Programs are supplied on magnetic tape in TDX format. Source files in ASCII code on magnetic tape can be provided for those who wish to generate test programs for other testers. *Test programs require a licensing agreement.*

Correlation Kit

This consists of two devices and datalog from AMD's characterization program.

ORDERING INFORMATION

Order Code	Description
AM29XX – SEN	Sentry Test Program
AM29XX – KIT	Correlation Kit

*Use a sweep speed of 1nsec/div.

IMOX™ Reliability Report

Advanced Micro Devices

SUMMARY

This report is a comprehensive summary of reliability test data accumulated on AMD's IMOX process. IMOX is an acronym for ion-IMplanted/micro-OXide isolation. AMD presently uses this wafer fabrication process on all new Bipolar products, including Bipolar Memory, Interface, Logic and Microprocessor devices. We present not only the statistical data, but also discuss the process itself, typical failure mechanisms, and the test methodology behind the data. The results show experimental and statistical proof that the AMD IMOX process ensures system designers of long life and highly reliable Bipolar devices.

In line with Advanced Micro Devices' commitment to provide customers with high quality, high performance devices, we will continue to evaluate devices for reliability through ongoing HTOL (high temperature operating life) testing. This report will be updated at regular intervals as new reliability data is accumulated.

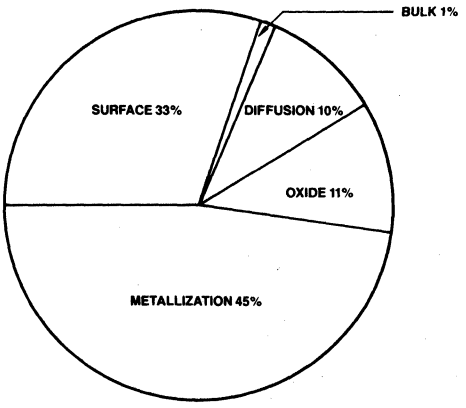
PROCESS

The IMOX process utilizes ion-implanted transistors, oxide isolation and dual-layer metal to create fast, high performance Bipolar devices that consume less power as well.

IMOX processing allows for reduction of transistor geometries and the amount of unused space surrounding a transistor, which means that individual transistors can be built significantly smaller and closer together. Since decreased geometries are obtained without a reduction in photolithographic line width, no increase in the process sensitivity occurs. Speed is one of the most vital characteristics of a Bipolar device. With the tighter layout and reduced capacitances of IMOX processing, we have improved the speed on many devices by as much as 25–30%. Tighter layouts have also allowed us to utilize previously unavailable die space for increased complexity. This is represented in two new AMD Bipolar VLSI devices, the Bipolar Microprocessor, Am29116 and the 16 x 16 Parallel Multiplier, Am29517.

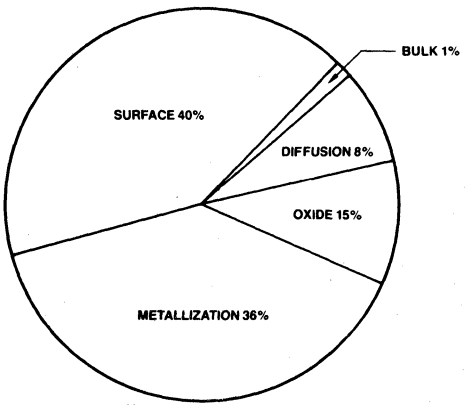
FAILURE MECHANISMS

Failures in integrated circuits are frequently categorized by the phase of manufacturing or the component of the part's structure that is associated with the determined failure mechanism. Failure distributions often are presented as pie charts with slices of the pie named for these categories (see Figures 1 and 2). The failure category distribution percentages are roughly those expected for Bipolar IMOX devices. Each of these categories may contain several distinct failure mechanisms–the basic physical or chemical process that results in a failure. The external indicators of a failure (the failure mode) are generally electrical in nature: opens, shorts, non-functional or parametric anomalies. There may be different mechanisms indicated by a single failure mode. The following is a discussion of the commonly observed failure mechanisms in integrated circuits.



Key: Failure type distribution for STTL/LSI Integrated Circuits (data derived from Reliability Analysis Center study, 'Microcircuit Screening Effectiveness,' 1978-Order No. TRS-1, 78). Data based on field failure information available to RAC, not life test data.

Figure 1. Normalized Distributions of STTL/LSI Malfunctions



Key: Failure percentages are averages based on past failure analysis studies performed by engineers at AMD.

Figure 2. AMD Observed Distributions of STTL/LSI Malfunctions

DIFFUSION

Diffusion-related mechanisms generally cause marginal device parameters which affect the performance of the device in certain operationally extreme situations. Electrical stresses induced during operation at elevated temperatures are effective in screening marginal diffusion problems. The activation energy associated with this general mechanism is difficult to assign without knowing more about the exact process, but it can be assumed to be 1.0eV for other than the dielectric breakdown.

OXIDE

Oxide-related faults can be found in the thermally grown oxide regions or in the deposited passivation layers. Defects in the latter sometimes lead to chemical attack of the underlying layers if corrosive elements are present. Activation energies for these types of defects are very large (> 1.0eV). Metal-to-metal or metal-to-semiconductor breakdown can also occur. These are often caused by pinholes, contaminants in the oxide or with photolithographic defects. Though the time dependence for oxide failure is more voltage than temperature related, life-tests are effective in electrically stressing oxide imperfections.

BULK

Bulk (silicon) defects are those associated with the silicon wafer or die itself, such as crystal imperfections, resistivity gradients, expitaxial layer defects, damage to the die, and foreign material precipitates. These defects in themselves do not change with time at even the highest die operating temperatures, but they can become part of the active region of the device when built-in charge changes occur. This failure mode is very rare. Of the total failure rate percentage, this type of failure occurs less than 1% of the time.

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SURFACE

Ionic-contamination-induced inversion and channeling are the most frequently detected surface related mechanisms. At elevated temperatures, ions become mobile in or on the oxide covering the die. If the device is powered, the ions will be attracted to high field regions that exist near reverse biased junctions. This accumulation of charge can induce a surface layer (channel) of a conduction type opposite to that of the adjacent region (inversion), i.e., an N-type channel on a P-type region. Additional modes of failure are altered parasitic device characteristics, parasitic capacitance and "leaky" bipolar junction characteristics. The effects of built-in charge may be very slow in appearing, showing up only after many hours under bias at elevated temperatures. The activation energy associated with charge migration in silicon dioxide has been found to be 0.5 to 1.0eV.

METALLIZATION

A familiar mechanism of metallization-related failures is metal migration. When high current densities on the order of hundreds of thousands of amps per square centimeter occur at elevated temperatures, the metal (aluminum) atoms are carried along by the electron flow, causing migration of the metallization opposite to the direction of current flow which results in wear out. This may be in the form of disconnects, breaks, metal lead opens, etc. AMD's design rules for a metallization stripe cross section provide for a maximum current density of 200,000 amperes per square centimeter, well within the MIL-M-38510 maximum allowable current density for glassivated aluminum conductors. The activation energy of electromigration has been determined to be 0.5 to 1.0eV.

Open metallization detected in failed devices may be due to metal migration. The high current condition required to cause metal migration is often found to be the result of a defective circuit element. Photolithographic or masking defects sometimes result in reduction of metallization cross-section which is sufficient to allow metal migration to occur. The mechanism by which a severely scratch-damaged metal stripe opens in a very localized area is probably metal migration. Open or short conditions will be easily detected during internal visual inspection. Subtle defects, such as reduced cross-sectional area, can be detected by a dynamic life test at high temperature.

INTERCONNECT, WIREBOND AND PACKAGE SEAL/LEAD DEFECTS

The interconnect category includes failures that result from the "flying" lead being damaged by nicking, by work-stressing during bonding and by handling subsequent to the wirebond operation. The wirebond category includes all types of bond failures, including intermetallic formation. The package seal/lead defect category includes hermeticity failures and hermeticity-related failures such as corrosion. None of these failure types are found in a life-test program. They are controlled by material selection, receiving inspection, and extensive control of the assembly process. The success at these controls is verified by examining the results of quality conformance testing for military and "Hi-Rel" customers, specifically, the group B and group D tests (MIL-STD-883, method 5005). The group B test (lot acceptance test) includes a wirebond strength test. The group D test is a pure-package quality conformance test and includes tests for lead integrity, resistance to thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration, centrifuge, and salt atmosphere exposure. Group B and D testing is periodically performed by AMD and is available for inspection.

ACCELERATED TESTING

Semiconductor devices fail as a consequence of certain physical, metallurgical and chemical processes, all of which have temperature-dependent rates. The rates may also be potential or current dependent, but these dependencies are generally second-order effects. Users of electronic components are aware of the thermal effect and have frequently borrowed the organic chemist's rule of thumb, that reaction rates double for a 10°C temperature rise, to estimate the effects of high temperature life testing. This procedure does not provide the proper acceleration factor if applied for more than a decade or two of temperature and is quite inaccurate in estimating a 70°C equivalence for a 125°C life test.

For most processes causing semiconductor failures, the Arrhenius equation enables us to determine realistic failure rates. Temperature variations and their corresponding reaction rates can also be calculated for semiconductor devices. The following equation can be used over the entire temperature range:

$$\lambda(T) = C_1 \exp(-E_a/KT)$$

where:

- $\lambda(T)$ = device failure rate (temperature-dependent)
- T = absolute temperature (°K)
- K = Boltzmann's constant (8.62×10^{-5} eV/°K)
- E_a = activation energy of the individual device failure mechanisms (eV)
- C_1 = a constant

The temperatures used are junction temperatures, and the ability to use higher temperatures to achieve acceleration is constrained by the maximum permissible junction temperature under bias. Junction temperatures can be computed using power dissipation and package thermal characteristics. The following equation shows how those temperatures were derived:

$$T_J = T_A + \theta_{JA}\left[(I_{CC_{max}})\ (V_{CC_{max}})\right]$$

To determine the acceleration factor for temperature, T_2, with reference to another temperature, T_1, simply divide the failure rate equations for the two temperatures:

$$\text{A.F.} = \frac{\lambda(T_1)}{\lambda(T_2)} = \exp\left[\frac{E_a}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

where:

- A.F. = acceleration factor
- $\lambda(T_1)/\lambda(T_2)$ = ratio of reaction rates (failure)

This equation contains one constant whose value is not known from physical theory: the activation energy, E_a. Activation energy reflects the temperature dependence of a particular failure mechanism or group of mechanisms. It has been determined experimentally for some specific processes. Various investigators disagree as to the exact value of E_a because such experiments are difficult to conduct and spurious failures occur to cloud the results. Table 1 shows the range of these values as determined by experimentation.

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TABLE 1.
ACTIVATION ENERGIES FOR CERTAIN PROCESSES

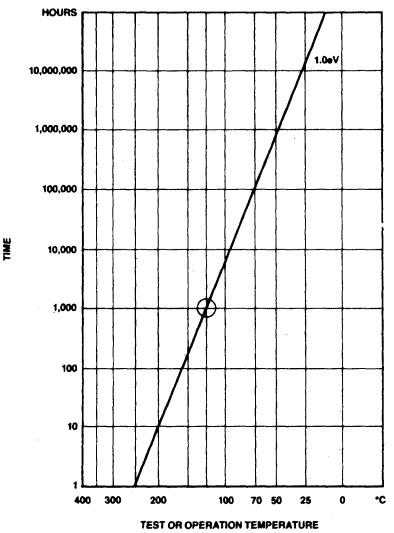
Surface Contamination	1.2–1.40 eV
Electromigration	0.5–1.00 eV
Oxide Defects (dielectric breakdown)	0.3–0.40 eV
Corrosion	0.3–0.60 eV
Intermetallic Growth (gold aluminum)	1.0–1.05 eV
Slow Trapping	1.30 eV

RELIABILITY TEST STUDY

The approach used in this report for evaluating reliability involves the concept of failure rates as a function of time. Life expectancy of devices can be categorized into three distinct intervals:

a. Infant Mortality
b. Operating Range
c. Old Age Mortality

An example of this distribution is shown in Figure 4. The results of this study are from long-term life tests. These tests are performed for 1000 hours or more without an initial burn-in. Therefore, "Infant Mortalities" are included in the failure rates of the units tested. With the inclusion of a burn-in process, the failure rates of the IMOX devices are expected to be less than the failure rates calculated in this report.



RF000220

An Arrhenius plot may be used to predict the effect of temperature shift for a particular population at a given average activation energy. This plot has been set up around a 1000-hour test at 125°C for two activation energies, 1.0eV and 0.466eV. Equivalent test times of other temperatures may be determined for either a 1.0eV or a 0.466eV process. For example, an equivalent test time for 0.466eV at any temperature may be determined by simply picking an appropriate temperature and reading the number of hours corresponding to the intersection of the temperature and the 0.466eV line.

Figure 3. Arrhenius Plot

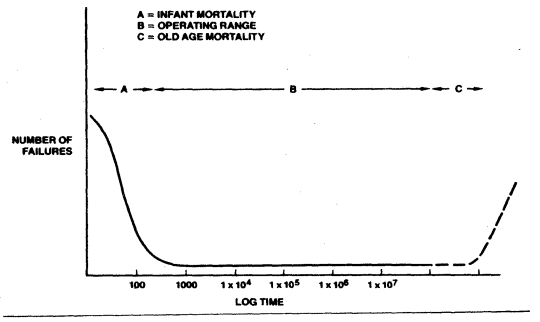


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Figure 4. Life Expectancy of Devices

Table 2 shows that units were subjected to HTOL (High Temperature Operating Life) testing at 125°C and 150°C per MIL-STD-883, method 1005 and 1015, conditions C and D. For an example of an HTOL circuit, see Figure 5. Data was collected on the SN54LS374A and the Am27S184/185 (cerdip and plastic) devices. The testing yielded 10,864,000 device hours worth of data. In total, 20 failures were recorded indicating a failure rate range (at 60% confidence level) of 0.183–0.50 per 1000 hours at 125°C using the chi-squared distribution.

This table also includes corresponding calculated failure rates at lower temperatures using an activation energy level of 1.0eV. The failure rate for the IMOX processed SN54LS374A is less than .0025% per Khr at 70°C (cerdip) and less than .0045 per Khr at 70°C (plastic). The failure rate for the Am27S184/185 is less than .0120 per khr. The lower temperatures (70°C and 25°C) are chosen to give users reliability predictions at the high end of the commercial operating temperature range and at the average "room temperature" operating temperature of a commercial system.

Other IMOX Bipolar devices which are presently undergoing HTOL testing are: Am2901C, Am29116 and Am29516. After recently completing 1000 cumulative hours of dynamic life testing (condition D) at 125°C, the 94-piece lot of Am2901C's resulted in a zero reject rate. Preliminary data has been gathered on each device type. At this time, statistically calculated rates would not accurately reflect the products' failure rate. After further testing is complete, failure rates will be calculated for each product and supplied in an addendum to this report.

TABLE 2. IMOX RELIABILITY OPERATING LIFE TEST DATA SUMMARY

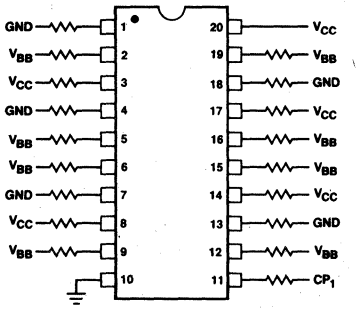
Device	Number of Units	Device Khrs	Number of Rejects	%Fall Per Khr	λ 125°C	λ 70°C	λ 25°C	Fits 70°C	Fits 25°C
54LS374A									
Cerdip	1435	6856	11	0.160	0.183	0.002	.00001	17	0.1
Plastic	1110	3825	9	0.235	0.274	0.003	.000015	26	0.15
27S184/185	263	183	0	0	0.50	0.0046	.000028	46	0.28
29116	Life Test in Progress								
29516	THE DATA FROM 29116 CAN BE APPLIED.								
IMOX Total	2808	10864	20	0.184	0.20	0.0018	.0000114	18	0.114

Notes: 1. All calculated failure rates and Fits Nos. used the Arrhenius Equation with 1.0 VeV activation energy.
2. Fits = Failure in 10^9 hrs at 70°C and 25°C using a 60% confidence level.

SUMMARY

This report summarizes the actual reliability testing of AMD's proprietary process, IMOX. The statistical data and charts are presented to provide accurate comparative information. The demonstrated failure rates of the devices at 70°C reflect the high reliability of IMOX processed products. The design rules for IMOX processing are the same for all Bipolar products. Therefore, similar testing performed on other Bipolar devices, i.e., Am29116, would also result in very low failure rates as seen in this study.

Analysis of the various failures have shown that the device failures were of a random mode and their degree of occurrence was inconsistent. No inherent process failure mechanism has been found in the IMOX process. In conclusion, IMOX is the superior method for Bipolar wafer fabrication and for building high reliability into AMD devices.



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POWER SUPPLY SETTINGS

Supply No.	Signal	Voltage
1	V_{BB}	+5.0 V±
2	V_{CC}	+5.0 V±

Conditions:
1. Pin 10: Device Ground
2. Pin 11: CP_1 – 100 KHz ± 10%
   High levels: +3.0 V to +5.0 V
   Low levels: −0.2 V to 1.2 V

MIL-STD-883 Method 1015 Condition C
C – Steady state, power and reverse bias.
Inputs reverse biased.
This circuit was used for testing the SN54LS374A.

Figure 5. HTOL Circuit Configuration

References

IMOX Reliability Report by Beverly Henry. In preparation of this report, Chris King, Wisty Olsson, Ann Rosser, Chris Schmidt and Pauline Seales provided valuable assistance.

Gate Counts and Die Sizes by Device

The following data is useful for hybrid design and for MIL-STD reliability calculations. The gate counts are only an approximation for LSI devices because the circuit implementation often uses multi-level gates and unique logic structures, not just NAND and NOR gates.

Am25S/25LS

Part Number	Equivalent Number of Gates (Approximate)	Die Area In Mils^2 = .001 x .001 in.)	Die Dimensions (In Mils = .001 in.)
Am25S05	86	9680	88 x 110
Am25LS07	26	6300	75 x 84
Am25S07	26	5810	70 x 83
Am25LS08	18	4575	75 x 61
Am25S08	18	4891	67 x 73
Am25LS09	30	4575	75 x 61
Am25S09	30	4891	67 x 73
Am25S10	29	3696	56 x 66
Am25LS14	Replaced by Am25LS14A		
Am25LS14A	167	7980	84 x 95
Am25LS15	92	9025	95 x 95
Am25S18	30	6083	77 x 79
Am25LS22	82	10,752	96 x 112
Am25LS23	88	10,752	96 x 112
Am25S557	1115	28,215	171 x 165
Am25S558	1115	28,215	171 x 165
Am25LS2513	33	6970	82 x 85
Am25LS2517	89	9828	91 x 108
Am25LS2518	30	8217	83 x 99
Am25LS2519	59	8217	83 x 99
Am25LS2520	84	8880	80 x 111
Am25LS2521	26	4662	63 x 74
Am25LS2535	52	7920	80 x 99
Am25LS2536	66	8316	84 x 99
Am25LS2537	42	7776	81 x 96
Am25LS2538	34	7776	81 x 96
Am25LS2539	38	7776	81 x 96
Am25LS2548	18	7776	81 x 96
Am25LS2568	87	8549	87 x 103
Am25LS2569	79	8549	87 x 103

Am26S/26LS

Part Number	Equivalent Number of Gates (Approximate)	Die Area (In Mils² = .001 x .001 in.)	Die Dimensions (In Mils = .001 in.)
Am26S02	N/A	4402	62 x 71
Am26S10	9	4425	59 x 75
Am26S11	13	4425	59 x 75
Am26S12	9	5112	71 x 72
Am26S12A	9	5112	71 x 72
Am26LS27	In development		
Am26LS28	In development		
Am26LS29	6	6580	70 x 94
Am26LS30	6	6580	70 x 94
Am26LS31	10	5628	67 x 84
Am26LS32	6	4704	56 x 84
Am26LS32B	6	4704	56 x 84
Am26LS33	6	4704	56 x 84
Am26LS34	6	4704	56 x 84
Am26LS38	72	6208	64 x 97

Am2900

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils² = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
Am2901	Replaced by Am2901B and Am2901C		
Am2901A	Replaced by Am2901B and Am2901C		
Am2901B	538	14,976	117 x 128
Am2901C	550	15,990	130 x 123
Am2902	Replaced by Am2902A		
Am2902A	19	4154	62 x 67
Am2903	630	32,111	163 x 197
Am2903A	752	36,808	172 x 214
Am2904	283	22,540	140 x 161
Am2905	49	10,400	80 x 130
Am2906	56	10,400	80 x 130
Am2907	52	9064	88 x 103
Am2908	52	9064	88 x 103
Am2909	Replaced by Am2909A		
Am2909A	225	6831	69 x 99
Am2910	736	32,980	170 x 194
Am2910A	In development		
Am2911	Replaced by Am2911A		
Am2911A	221	6664	68 x 98
Am2912	9	4425	59 x 75
Am2913	33	6970	82 x 85
Am2914	335	24,871	133 x 187
Am2915A	49	9620	74 x 130
Am2916A	56	9620	74 x 130
Am2917A	52	9620	74 x 130
Am2918	30	6083	77 x 79
Am29LS18	30	8217	83 x 99
Am2919	59	8217	83 x 99
Am2920	84	8880	80 x 111
Am2921	34	7776	81 x 96
Am2922	52	7920	80 x 99
Am2923	18	4288	64 x 67
Am2924	17	4550	65 x 70
Am2925	120	11,834	97 x 122
Am2926	10	5278	58 x 91
Am2927	72	12,096	87 x 144
Am2928	95	12,096	87 x 144
Am2929	10	5278	58 x 91

Refer to Page 13-1 for Essential Information on Military Devices

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
Am2930	548	26,600	133 x 200
Am2932	521	26,600	133 x 200
Am2940	415	32,037	177 x 181
Am2942	415	32,037	177 x 181
Am2946	18	6141	69 x 89
Am2947	18	6141	69 x 89
Am2948	18	6141	69 x 89
Am2949	18	6141	69 x 89
Am2950	175	14,766	107 x 138
Am2950A	In development		
Am2951	175	14,766	107 x 138
Am2951A	In development		
Am2952	102	14,873	107 x 139
Am2952A	In development		
Am2953	102	14,873	107 x 139
Am2953A	In development		
Am2954	50	7968	96 x 83
Am2955	50	7968	96 x 83
Am2956	50	7854	66 x 119
Am2957	50	7854	66 x 119
Am2958	10	5369	59 x 91
Am2959	10	5369	59 x 91
Am2960	450	13,056	102 x 128
Am2960A	In development		
Am2961	82	8874	102 x 87
Am2962	74	8874	102 x 87
Am2964B	170	22,308	156 x 143
Am2965	10	5640	94 x 60
Am2966	10	5640	94 x 60
Am2968	In development		
Am2969	In development		
Am2970	In development		
Am29112	In development		
Am29116	2500	78,061	251 x 311
Am29116A	In development		
Am29203	752	36,808	172 x 214
Am29501	1000	64,158	289 x 222
Am29510	In development		
Am29516	2100	55,500	250 x 222
Am29516A	In development		
Am29517	2100	55,500	250 x 222
Am29517A	In development		
Am29520	362	15,327	117 x 131
Am29521	362	15,327	117 x 131
Am29526	N/A	N/A	N/A
Am29527	N/A	N/A	N/A
Am29528	N/A	N/A	N/A
Am29529	N/A	N/A	N/A
Am29540	1125	N/A	N/A
Am29705	258	13,056	102 x 128
Am29705A	206	9984	104 x 96
Am29707	207	9984	104 x 96
Am29803A	N/A	N/A	N/A
Am29806	42	6468	66 x 98
Am29809	42	6468	66 x 98
Am29811A	N/A	N/A	N/A
Am29818	152	11,328	96 x 118
Am29821	72	5376	64 x 84

Refer to Page 13-1 for Essential Information on Military Devices

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
Am29822	72	5376	64 x 84
Am29823	68	5376	64 x 84
Am29824	68	5376	64 x 84
Am29825	61	5376	64 x 84
Am29826	61	5376	64 x 84
Am29827	11	N/A	N/A
Am29828	11	N/A	N/A
Am29833	In development		
Am29834	In development		
Am29841	52	5376	84 x 64
Am29842	52	5376	84 x 64
Am29843	49	5376	84 x 64
Am29844	49	5376	84 x 64
Am29845	44	5376	84 x 64
Am29846	44	5376	84 x 64
Am29853	In development		
Am29854	In development		
Am29861	22	N/A	N/A
Am29862	22	N/A	N/A
Am29863	20	N/A	N/A
Am29864	20	N/A	N/A

8XXX MOS MPU Support

Part Number	Equivalent Number of Gates (Approximate)	Die Area (In Mils^2 = .001 x .001 in.)	Die Dimensions (In Mils = .001 in.)
Am8120	84	8880	80 x 111
Am8127	135	8624	98 x 88
Am8163	350	28,860	185 x 156
Am8167	350	28,860	185 x 156
Am8212	N/A	10,192	91 x 112
Am8216	10	5940	66 x 90
Am8224	47	7140	85 x 84
Am8226	10	5940	66 x 90
Am8228	N/A	14,960	110 x 136
Am8238	N/A	14,960	110 x 136

Package Material Configurations

	Multilayer Ceramic			Ceramic			
	Brazed Packages		Chip Carrier	Cerdip		Plastic	
Package Body Material	90% Alumina (Min)		90% Alumina (Min)	90% Alumina (Min)		Novolac Epoxy	
Die Attach Pad Metallization	Gold		Gold	Gold	Silver Palladium	Gold	Silver
Die Attach Material	Gold/Silicon		Gold/Silicon	Gold/ Silicon	Gold	Gold/ Silicon	Silver Epoxy
Die Attach Temperature	440°C Max		440°C Max	440°C Max		440°C Max	200°C (Curing Temp)
Bond Finger Metallization	Gold		Gold	Aluminum		Gold or Silver	
Bonding Wire	Aluminum/1% Silicon		Aluminum/1% Silicon	Aluminum/1% Silicon		Gold	
Bonding Method	Ultrasonic		Ultrasonic	Ultrasonic		Ball-bonding	
Seal Ring Metallization	Gold		Gold	None		N/A	
Seal Material	Gold/Tin	Lead/Tin/ Silver	Gold/Tin	Vitreous Glass		N/A	
Lid Material	Alloy 42 (Gold Plated)	Alloy 42 (Tin Plated)	Alloy 42 (Gold Plated)	90% Alumina (Min)		N/A	
Seal Temperature	370°C Max		370°C Max	470°C Max		175°C Max (Mold Temperature)	
Seal Ambient	Nitrogen		Nitrogen	Air		N/A	
Lead Material	Alloy 42		N/A	Alloy 42		Alloy 42	Copper
Lead Finish	Gold	Tin	N/A	Tin		Solder	

Refer to Page 13-1 for Essential Information on Military Devices

Thermal Characterization of Packaged Devices

APPLICATION NOTE
by J.L. Hayward

DEFINITION OF THERMAL RESISTANCE

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_j = T_X + P_d R_{\theta JX} \qquad (1)$$

where: T_j = junction temperature
T_X = reference temperature
P_d = power dissipation
$R_{\theta JX}$ = thermal resistance
X = some defined test condition

In general, one of three conditions is defined for measurement of thermal resistance:

- $R_{\theta JC}$ – thermal resistance measured with respect to the temperature at some specified point on the package surface.
- $R_{\theta JA}$ (still air) – thermal resistance measured with respect to the temperature of a specified volume of still air.
- $R_{\theta JA}$ (moving air) – thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between $R_{\theta JC}$ and $R_{\theta CA}$ is

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where $R_{\theta CA}$ is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques. $R_{\theta JC}$ is dependent solely on material properties and package geometry; $R_{\theta JA}$ includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$R_\theta = \frac{L}{K(T)A} \qquad (2)$$

where: L = length of the heat flow path
A = cross sectional area of the heat flow path
K(T) = thermal conductivity as a function of temperature·

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$R_\theta = \Sigma R_{\theta n} = \Sigma \frac{L}{K_n A}$$

But since the heat flow path through a component is influenced by the materials surrounding it, determination of L and A is not always straightforward.

A second factor that affects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{R_{\theta JX}}(T_j - T_X) = \frac{1}{\Sigma R_{\theta n}}(T_j - T_X) \qquad (3)$$

the relationship between P_d and T_j can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry, T_j must increase and, since the individual $R_{\theta n}$ will also increase with temperature, the increase in T_j will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

EXPERIMENTAL METHOD

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a

convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to insure that the results of the measurement are truly representative of the thermal state of the device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For those MOS devices for which no useful parameter is available, simulation is accomplished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into multiple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1mA current level at two different temperatures. The diode calibration factor is then:

$$K_f = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \qquad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. (See Figure 1.) The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of < 100Hz. During the brief OFF states the device is reverse-biased with a 1mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

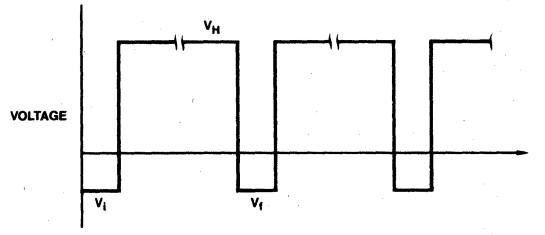
$$R_{\theta JX} = \frac{K_f(V_f - V_i)}{V_H I_H} = \frac{K_f \Delta V}{P_d} \qquad (5)$$

where: K_f = calibration factor
V_i = initial forward voltage value
V_f = current forward voltage value
V_H = heating voltage
I_H = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is $R_{\theta JA}$ (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For $R_{\theta JC}$ measurements the device is attached to a large metal heatsink. This insures that the reference point on the device surface is maintained at a constant temperature. Through the use of heaters attached to the metal fixture, the "case" temperature may be maintained at any specified value above ambient. The requirements for measurement of $R_{\theta JA}$ (moving air) are rather more complex. They involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

Figure 1. Waveforms for Pulsed Thermal Resistance Test



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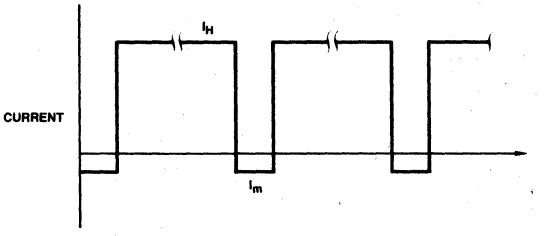


AF001530

Refer to Page 13-1 for Essential Information on Military Devices

THERMAL CHARACTERIZATION DATA FOR CERDIPS[1]

Lead Count	Width (Inches)	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	0.300	66–89	22
20	0.300	68–78	N/A
24	0.300	55–57	13–14
24	0.600	49	11
28	0.600	29	N/A
40	0.600	36–37	7–9

THERMAL CHARACTERIZATION DATA FOR SIDE-BRAZE AND TOP-BRAZE PACKAGES[1]

Lead Count	Type	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
40	Side-Braze	27–35	6–7
48	Side-Braze	37	10
52	Top-Braze with Heat-Spreader	19	4
64	Top-Braze with Heat-Spreader	20	7

THERMAL CHARACTERIZATION DATA FOR PLASTIC DIPs[1]

Lead Count	Width (Inches)	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	0.300	110*	N/A
20	0.300	81–123*	32*
24	0.600	99–115*	43–57*
28	0.600	85*	N/A
40	0.600	62–73*	27–34*

*In 1983 AMD introduced copper-lead-frame versions of all plastic packages. The copper-lead-frame versions have better thermal characteristics than the current plastic packages measured above.

THERMAL CHARACTERIZATION DATA FOR LEADLESS CHIP CARRIERS (JEDEC TYPE C)[1]

Lead Count	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
20	66–72*	N/A
28	69*	N/A
44	52–57*	N/A
52	44*	N/A

*The $R_{\theta JA}$ values listed for leadless chip carriers were measured with the chip carriers mounted in the appropriate burn-in sockets. This restricts convection of heat from the package and results in θ values higher than might be expected in actual use.

THERMAL CHARACTERIZATION DATA FOR CERPAKS AND FLATPACKS[1]

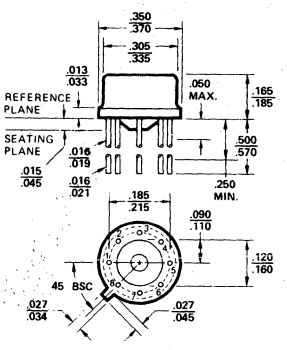
Lead Count	Type	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	Cerpak	113–159	10–17
20	Cerpak	119	N/A
24	Cerpak	99	8
42	Brazed Flatpack	63	8

Note 1. This data, while derived from actual measurements done on specific packaged devices, is only approximate and cannot be guaranteed because of the wide variation of die sizes and device power levels.

Package Outlines

METAL CAN PACKAGES

H-8-1



PO000780

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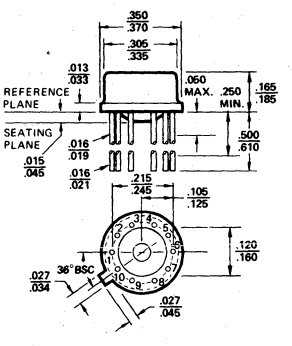

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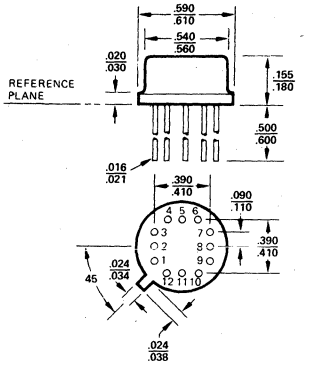
G-12-1

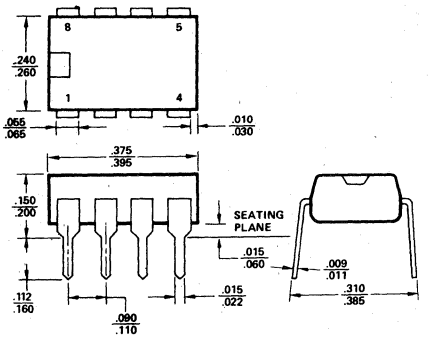


PO000770

Note. Standard lead finish is bright acid tin plate or gold plate.

MOLDED DUAL IN-LINE PACKAGES

P-8-1



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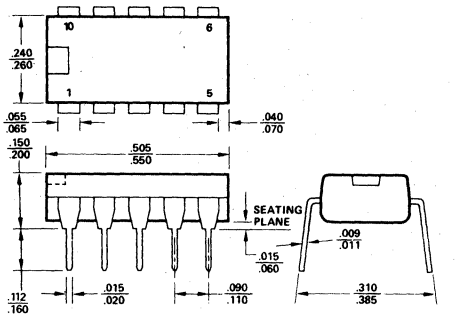

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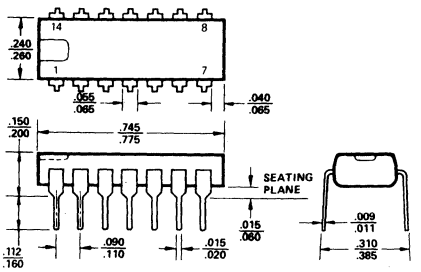

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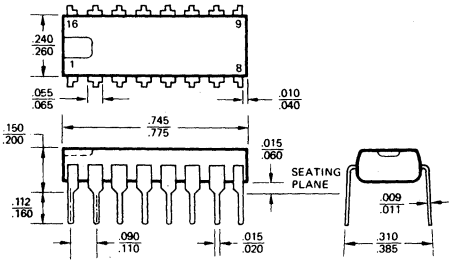

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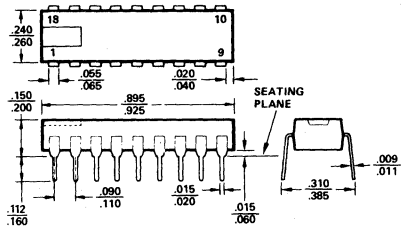

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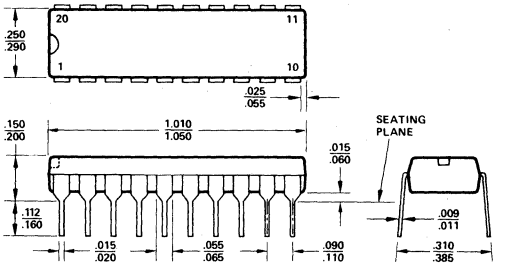

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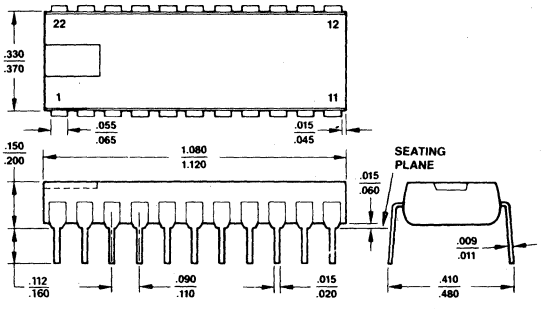

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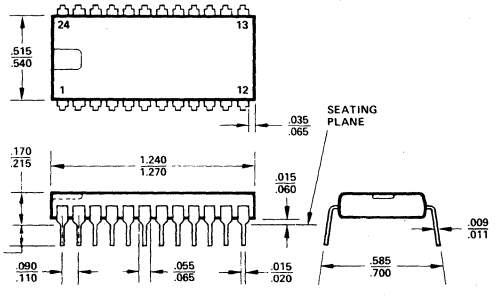

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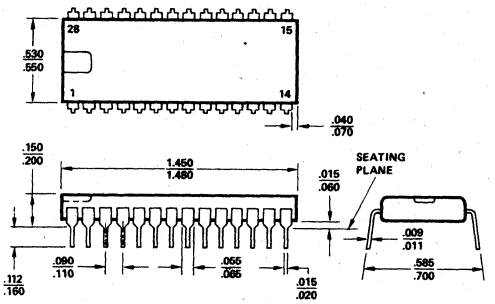

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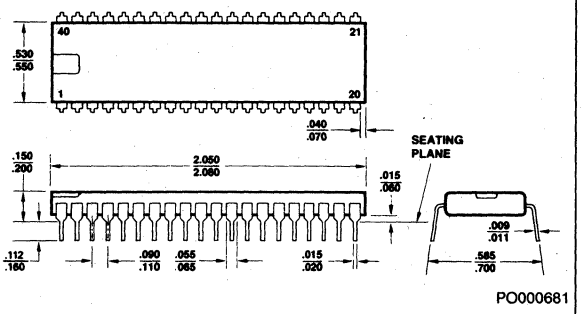
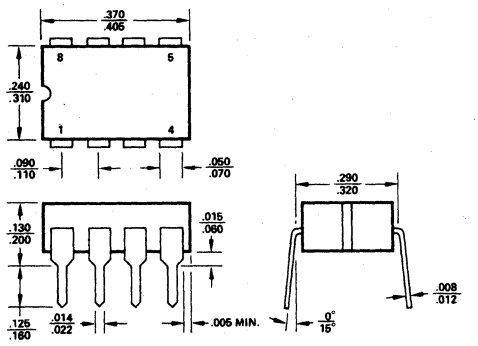


PO000681

Note. Standard lead finish is tin plate or solder dip.

HERMETIC DUAL IN-LINE PACKAGES

D-8-1



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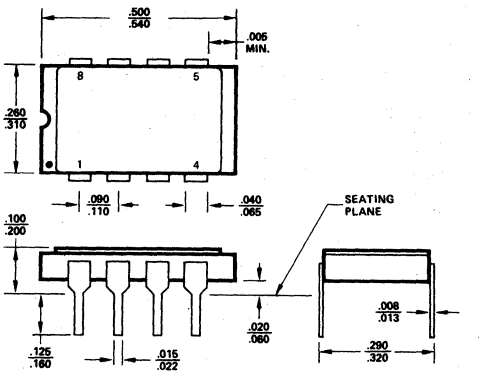

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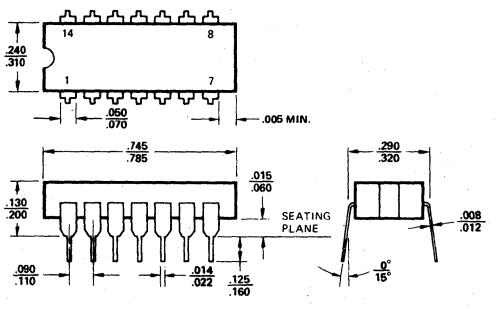

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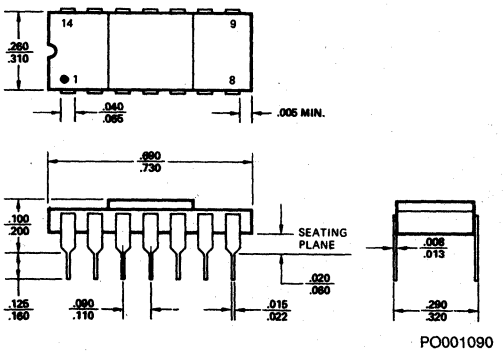

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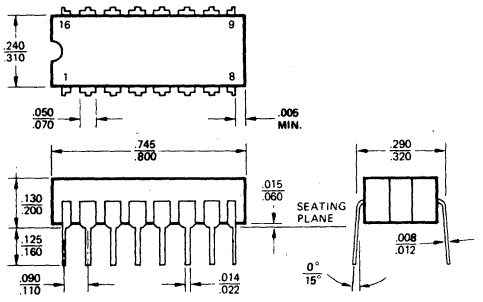

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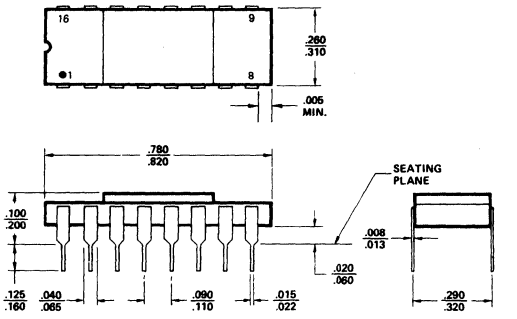

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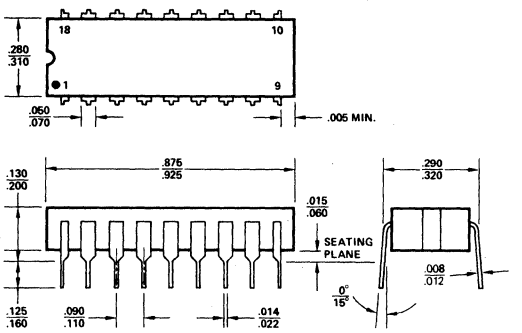

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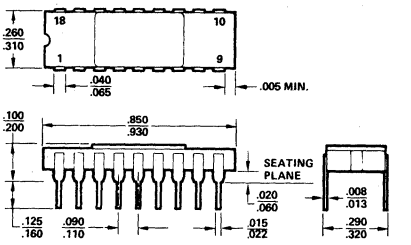

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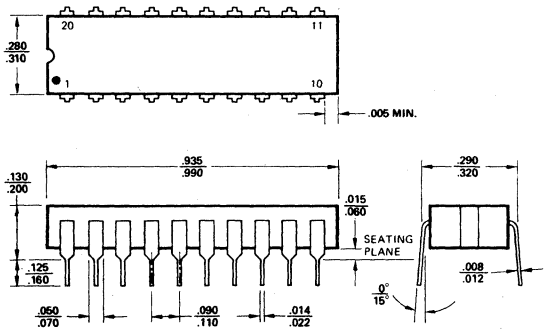

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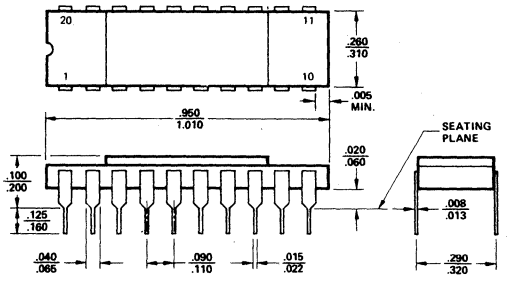

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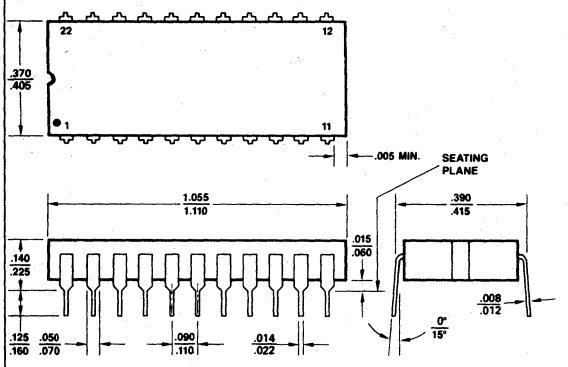

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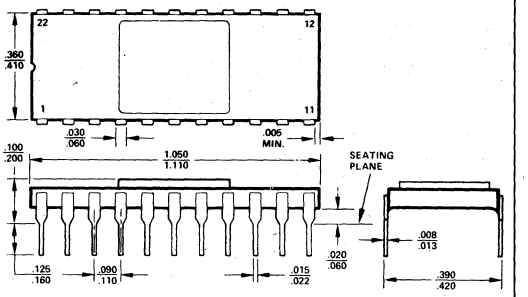

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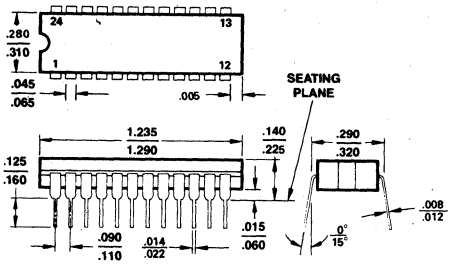
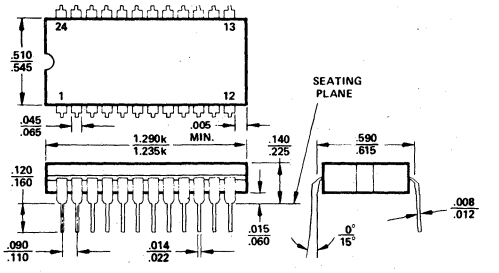
D-24-SLIM



PO001271

D-24-1 and D-24-4



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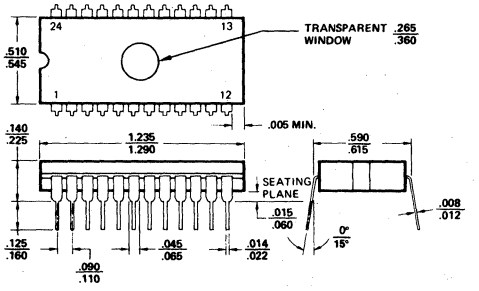

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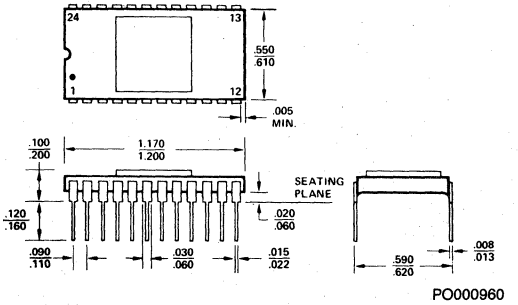
D-24-2



PO000960

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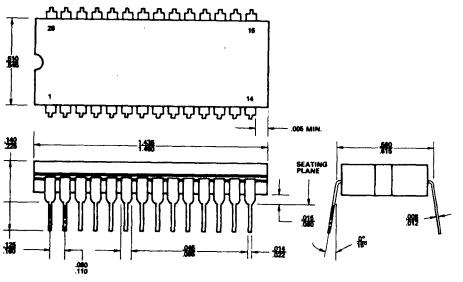

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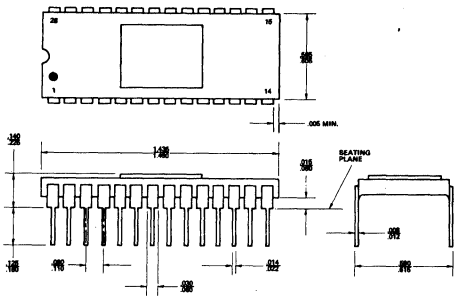

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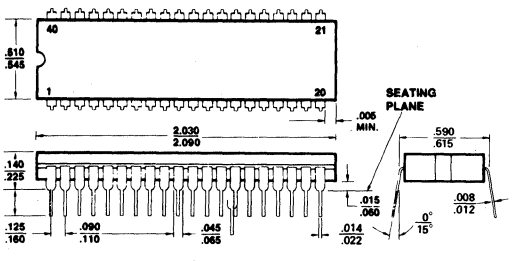
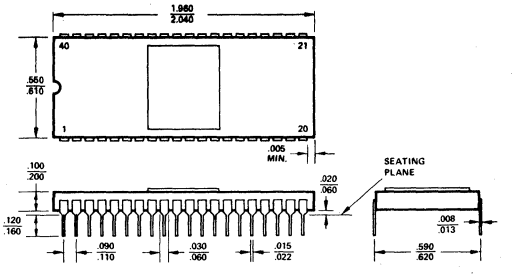


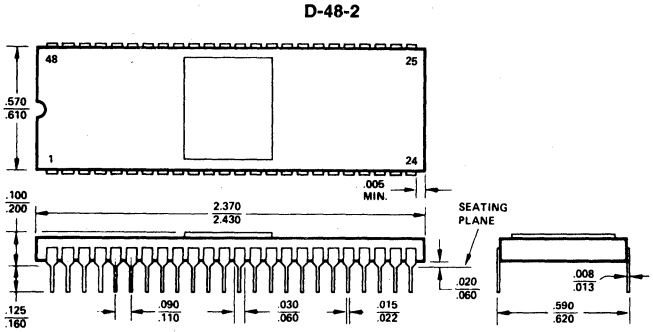
PO001191

D-40-2



PO001200

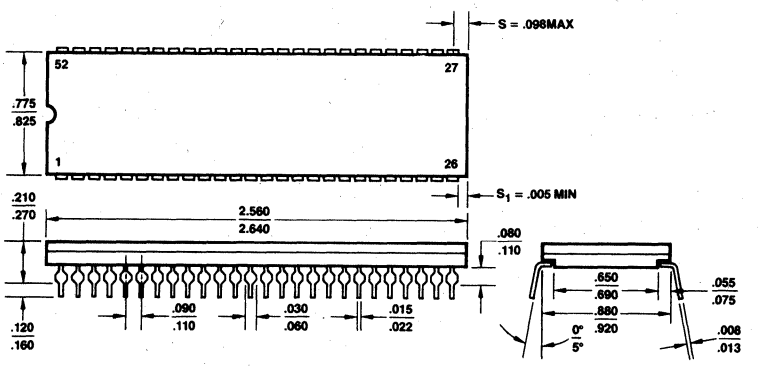
D-48-2



PO001210

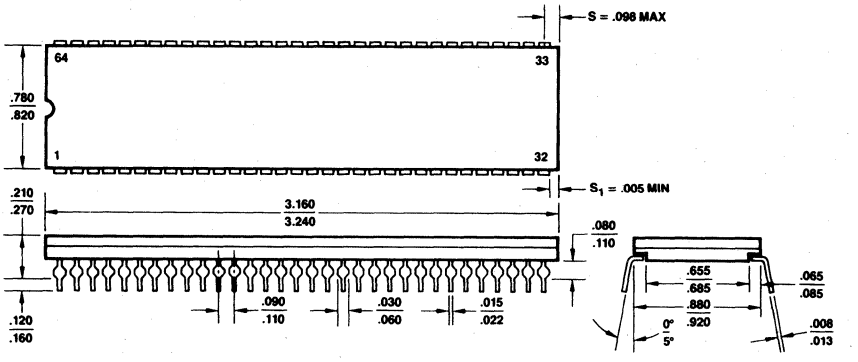
HERMETIC DUAL IN-LINE PACKAGES (Cont.)

D-52-3



PO001250

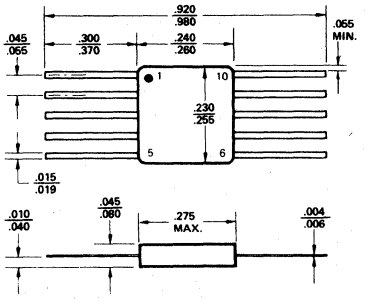
D-64-3



PO001240

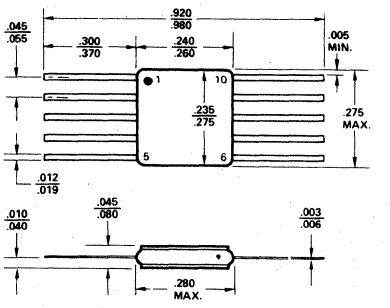
FLAT PACKAGES

F-10-1



PO000950

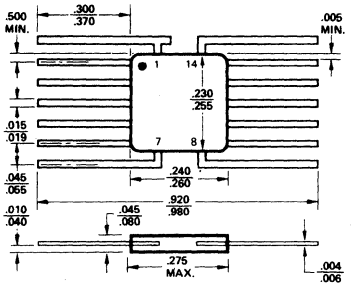
F-10-2



PO000940

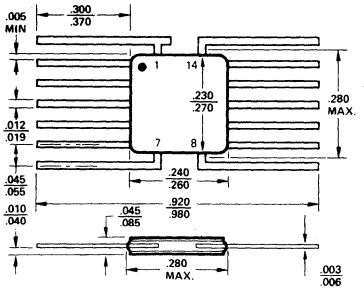
FLAT PACKAGES (Cont.)

F-14-1



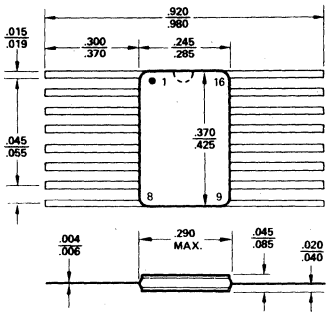
PO000930

F-14-2



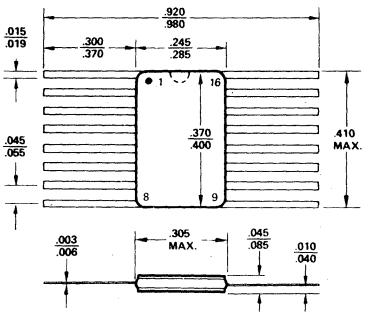
PO000920

F-16-1



PO000910

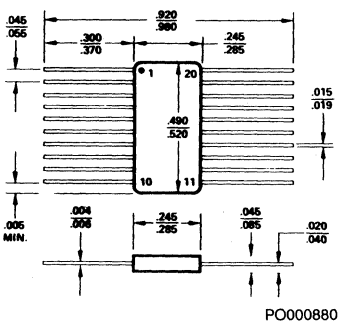
F-16-2



PO000900

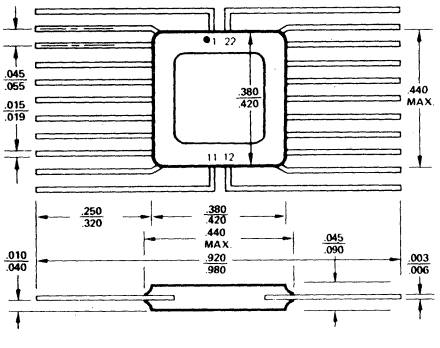
Note: Notch is pin 1 index on cerpack.

F-20-1



PO000880

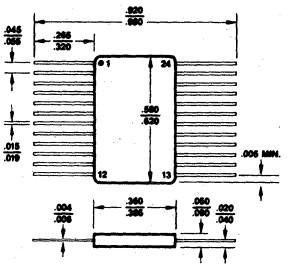
F-22-1



PO000890

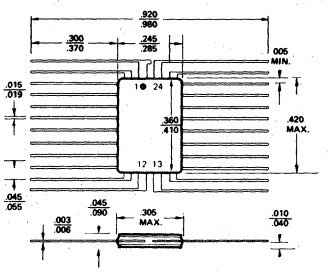
FLAT PACKAGES (Cont.)

F-24-1



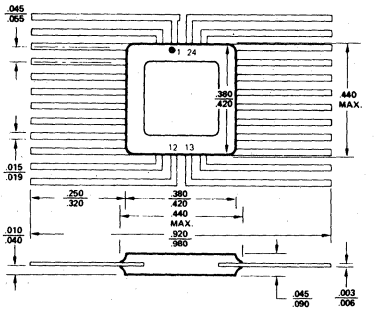
PO000850

F-24-2



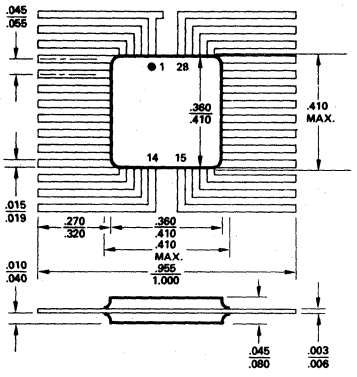
PO000840

F-24-3



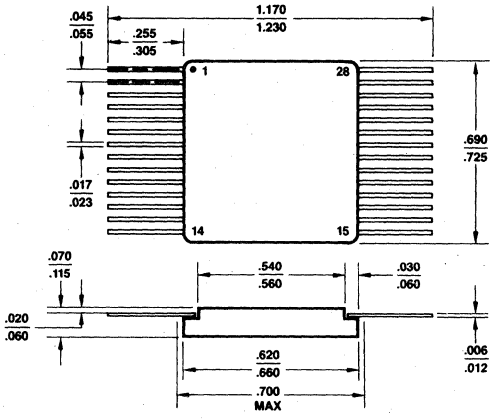
PO000870

F-28-1



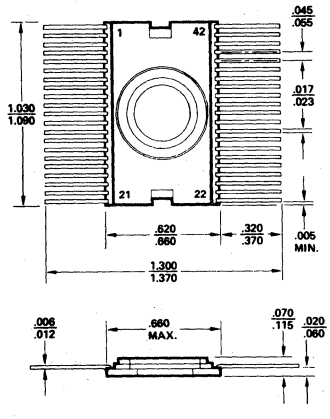
PO000820

F-28-2 and F-28-3



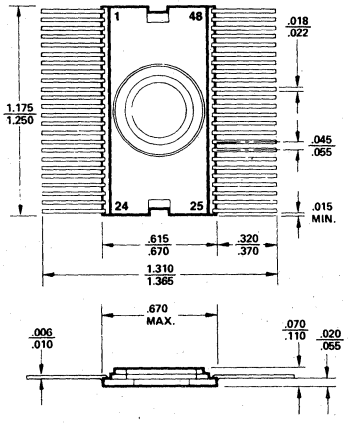
PO000810

F-42-1



PO000860

F-48-2

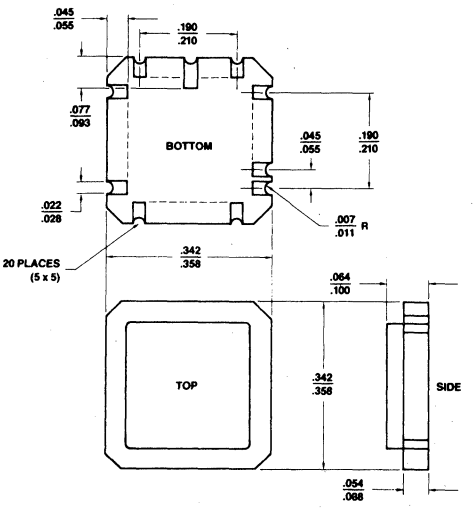


PO000830

Refer to Page 13-1 for Essential Information on Military Devices

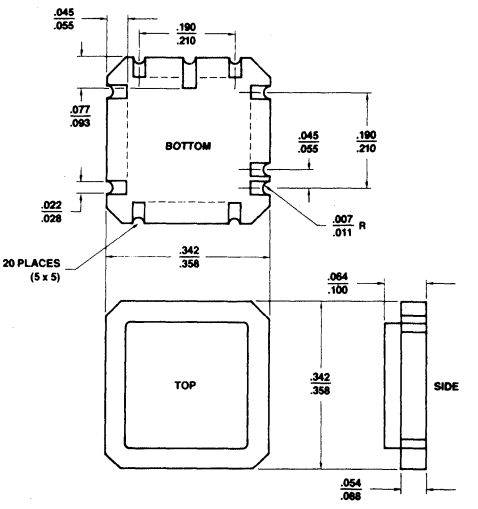
SQUARE CHIP CARRIER FAMILY

L-20-1



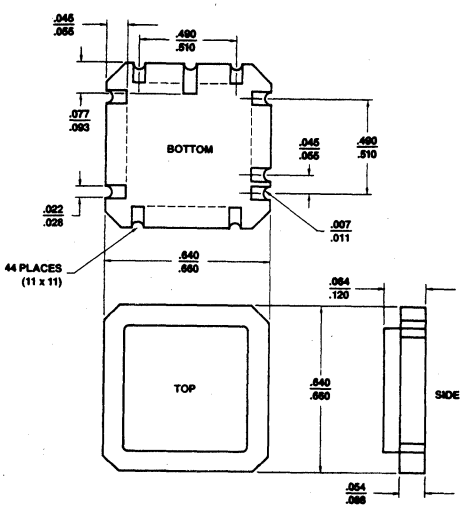
PO001120

L-28-1



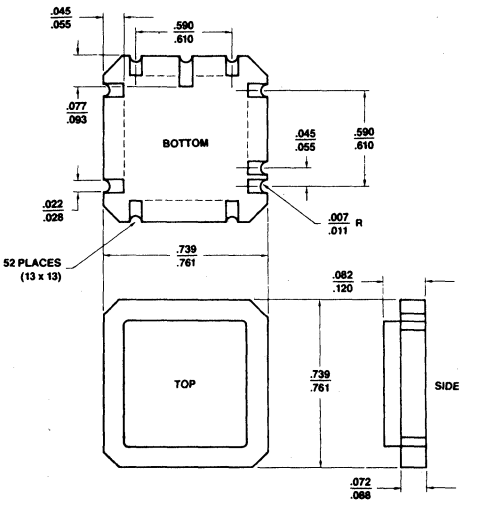
PO001130

L-44-1



PO001140

L-52-1



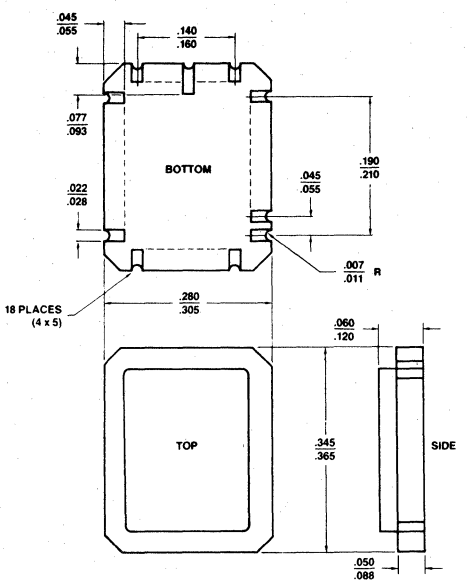
PO001150

13

Refer to Page 13-1 for Essential Information on Military Devices

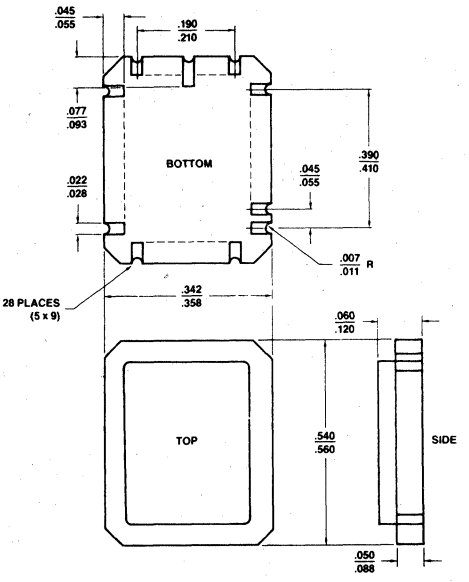
RECTANGULAR CHIP CARRIER FAMILY

L-18-2



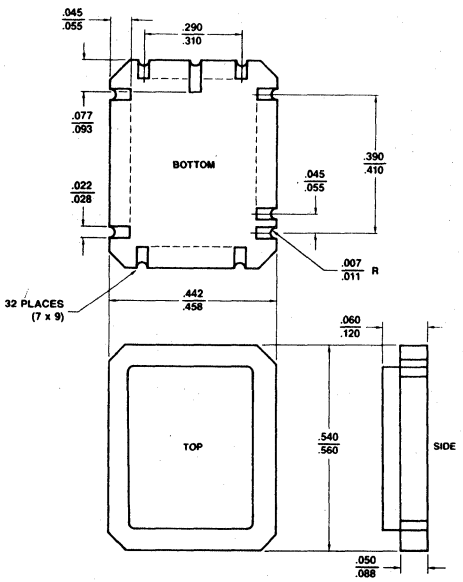
PO001160

L-28-2



PO001180

L-32-2



PO001170

Ordering Information

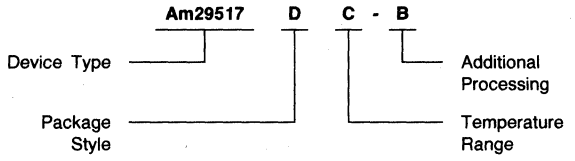
All Advanced Micro Devices' products listed are stocked locally and distributed nationally by Franchised Distributors. See back of this book for the location nearest you. Please consult them for the latest price revisions. For direct factory orders, call local AMD Sales Office or Sales Representative. See the back of this book for the location nearest you.

Minimum Order

The minimum direct factory order is $100.00 for a standard product. The minimum direct factory order for burn-in product is $250.00.

Proprietary Product Ordering, Package and Temperature Range Codes

The following scheme is used to identify Advanced Micro Devices' proprietary products.

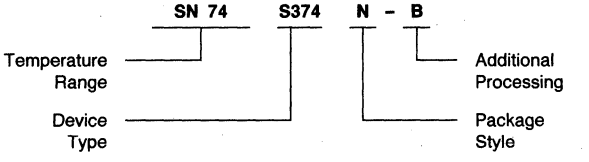


Package Style	Temperature Range	Additional Procedures
D – Hermetic DIP	C – Commercial 0°C to +70°C	Blank – Standard processing
F – Flat Package	M – Military −55°C to +125°C	B – Burn-in
P – Molded DIP		
L – Leadless Chip Carrier		
X – Dice		

Second Source Product Ordering, Package and Temperature Range Codes

An order number and marking system identical to the original manufacturer's is used for the Advanced Micro Devices' pin-for-pin and electrically equivalent circuit.

The following example is the ordering scheme for Advanced Micro Devices' second source to Texas Instruments' products.



Package Style	Temperature Range	Additional Processing
J – Hermetic DIP	C – Commercial 0°C to +70°C	B – Burn-in
N – Molded DIP	M – Military −55°C to +125°C	
W – Flat Package		
X – Dice		

Refer to Page 13-1 for Essential Information on Military Devices

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Silic 314, Immeuble Helsinki
74, rue d'Arcueil
F-94588 Rungis Cedex
Tél: (01) 687.36.66
TELEX: 202053
FAX: 686.21.85

GERMANY
Advanced Micro Devices GmbH
Rosenheimer Strasse 143B
8000 Munchen 80,
West Germany
Tel: 49 89 41140
TELEX: 05-23883
FAX: 406 490

GERMANY
Advanced Micro Devices GmbH
Feuerseeplatz 4/5
D-7000 Stuttgart 1
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Zur Worth 6
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Tel: (05143) 53 62
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HONG KONG
Advanced Micro Devices
Room 1602 World Finance Centre
South Tower
Harbour City
17 Canton Road
Tsimshatsui, Kowloon
Tel: (852) 3 695377
TELEX: 50426
FAX: (852) 123 4276

ITALY
Advanced Micro Devices S.R.L.
Centro Direzionale
Via Novara, 570
I-20153 Milano
Tel: (02) 3533241
TELEX: 315286
FAX: (39) 349 8000

JAPAN
Advanced Micro Devices, K.K.
Shinjuku Kokusai Building
6-6-2 Nishi-Shinjuku
Shinjuku-ku, Tokyo 160
Tel: (03) 345-8241
TELEX: 24064
FAX: 03 342-5196

SWEDEN
Advanced Micro Devices AB
Box 7013
Rissneleden 144, 5tr
S-172 07 Sundbyberg
Tel: (08) 7330350
TELEX: 11602
FAX: 7332285

UNITED KINGDOM
Advanced Micro Devices (U.K.) Ltd.
A.M.D. House,
Goldsworth Road,
Woking,
Surrey GU21 1JT
Tel: Woking (04862) 22121
TELEX: 859103
FAX: 22179

Advanced Micro Devices (U.K.) Ltd.
The Genesis Centre
Garrett Field
Science Park South
Birchwood
Warrington WA3 7BH
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ADVANCED MICRO DEVICES, INC.
901 Thompson Place
P.O. Box 3453
Sunnyvale,
California 94088
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306
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