Am9580A/Am9590

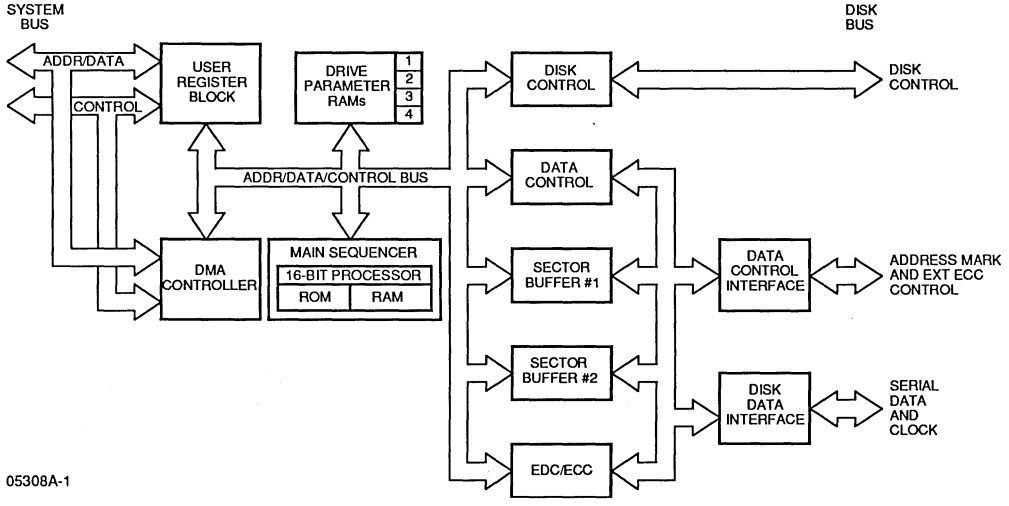
Hard Disk Controllers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- **Am9580A supports ST506/412 and IBM double-density floppy formats**
- **Am9590 supports ESDI, ST506/412, and IBM double-density floppy formats**
- **Supports hard- and soft-sectored formats**
- **Controls up to four drives in any mix of hard and flexible formats**
- **Two on-chip 512-byte sector buffers support zero-sector interleaving**
- **Supports error checking algorithms including:**
  - CRC/CCITT
  - Single-Burst Reed-Solomon
  - Double-Burst Reed-Solomon
  - External ECC (user-definable Error Correcting Codes)
- **Linked-list command and data structures**
- **On-chip DMA controller supports 32-bit addressing and 8/16 bit data**
- **Am9590 supports data rates up to 15 Mbit/second**

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am9580A and the Am9590 are single-chip solutions to the problems encountered in designing data formatters and disk system controllers. A companion part is also offered, the Am9582 Disk Data Separator, which when combined with one of the above disk controllers provides all of the functions which until now have been found only on sophisticated board-level products.

Both of these highly integrated disk controllers are flexible enough to cope with the differing requirements of today's broad marketplace, while using the advanced technology and innovative features that tomorrow's market will demand.

These disk controllers support both rigid and flexible disk drives and their respective data formats. Four drives of any mix (hard and flexible) can be controlled with these devices, with individual drive characteristics easily user-programmable.

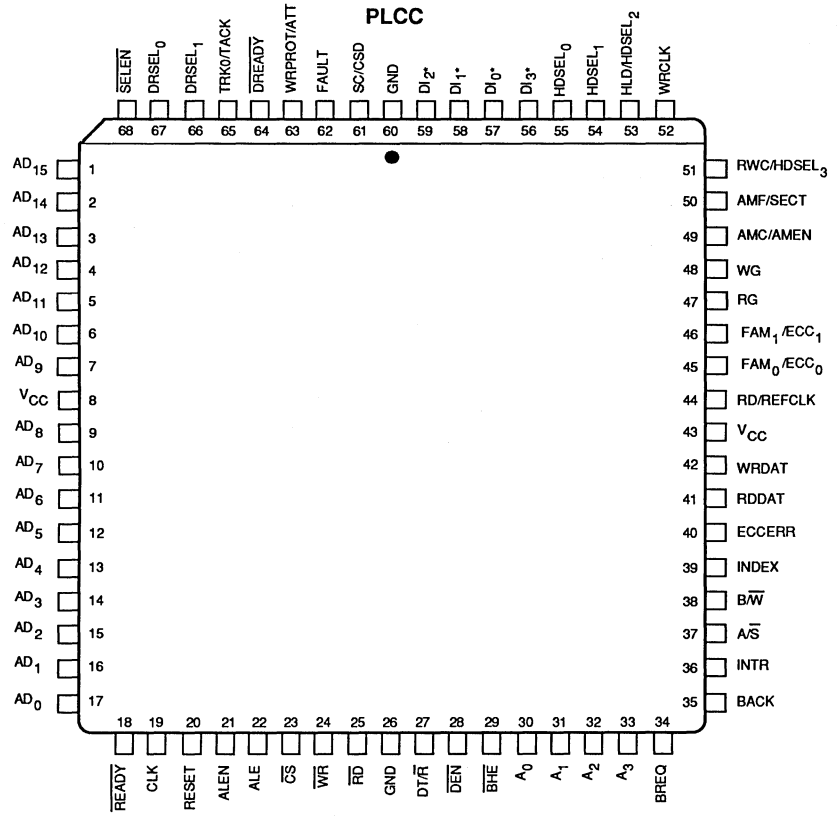
A sophisticated on-chip DMA controller fetches commands, writes status information, fetches data to be written on disk, and writes data that has been read from the disk. The DMA operation is programmable to adjust the bus occupancy, data bus width (8 or 16 bits), and wait state insertion. Two sector buffers allow zero-sector interleaving to access data on physically adjacent sectors, improving both file access time and system throughput. Sector sizes of 128, 256, and 512 bytes are programmable.

Both controllers ensure data integrity by selecting either an error-detecting code (CRC-CCITT), or one of two error-correcting codes (Single- or Double-Burst Reed-Solomon). Additionally, the Hard Disk Controller (HDC) provides handshake signals to control external Error-Correcting Codes (ECC) circuitry to implement any user-definable ECC algorithm.

The ESDI and ST506/412 interfaces are completely supported by the Am9590. Users interested only in the ST506/412 standard can use the Am9580A. Both of these controllers provide all of the required signals.

CONNECTION DIAGRAMS

Top View



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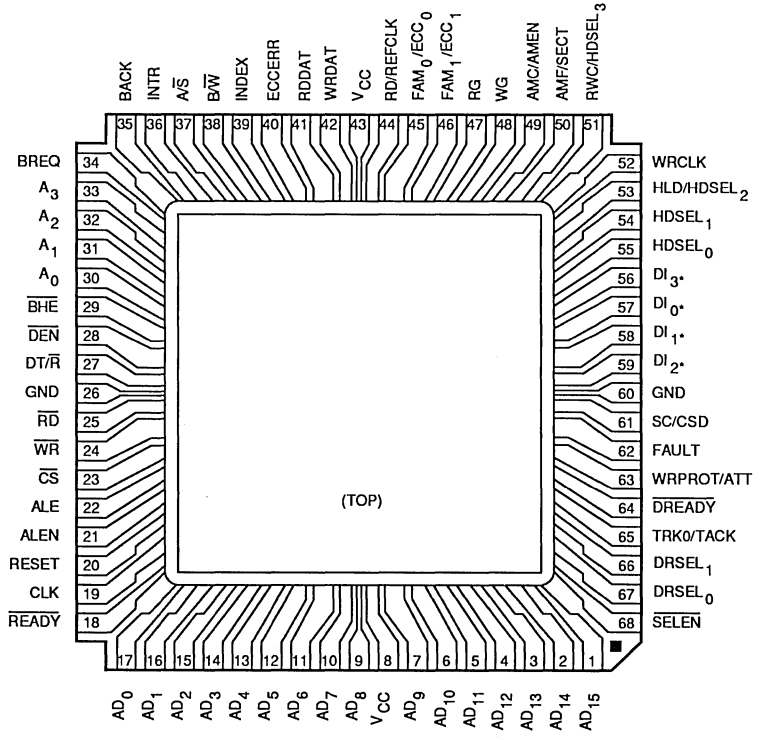
*Refer to Pin Description section for options.

CONNECTION DIAGRAMS (Cont'd.)

Top View

LCC



* Refer to Pin Description section for options.

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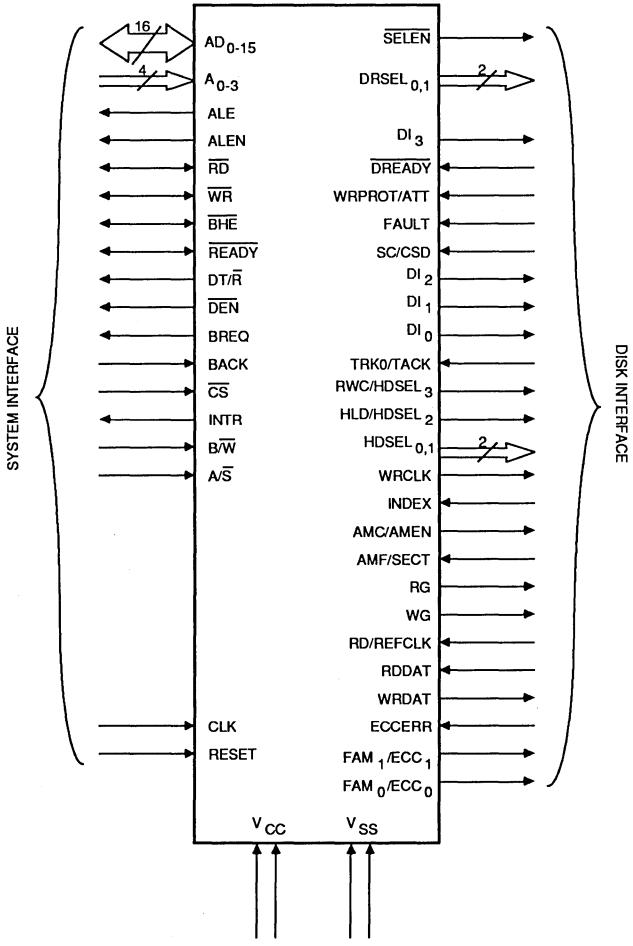
LOGIC SYMBOL



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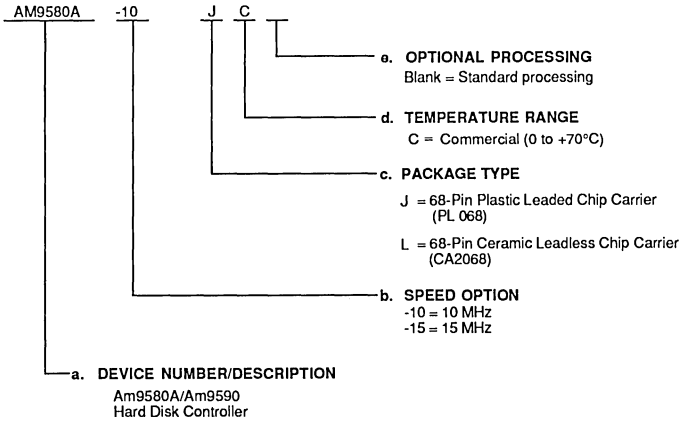
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM9580A-10	JC, LC
Am9590-15	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Interface Signals

GND_1, GND_2 Ground

Ground (both lines must be connected).

V_{CC1}, V_{CC2} Power Supply

+5 V Power supply (both lines must be connected).

System Interface Lines

A_0 Address Line 0 (Input; Active HIGH)

When the HDC is in Slave Mode, a HIGH on this address line selects the upper byte of internal registers, and a LOW selects the lower byte of internal registers. For word accesses, this line must be LOW. A_0–A_3 must be valid through the read or write cycle. In Master Mode, this line is ignored.

A_1–A_3 Address Lines 1-3 (Inputs; Active HIGH)

When the HDC is in Slave Mode, these lines select one of the internal registers (see Figure 1). In Master Mode, these lines are ignored.

AD_0–AD_{15} Address/Data Bus (Input/Output; Active HIGH, Three State)

The Address/Data Bus (AD Bus) is a time-multiplexed, bidirectional, three-state, 16-bit bus used for all system transactions. A HIGH represents a "1" on the bus and a LOW represents a "0". AD_0 is the least-significant bit. The presence of an address is indicated by either ALE or ALEN. When ALE is HIGH, the bus contains lower address bits (A_0–A_{15}). When ALEN is HIGH, the bus contains upper address bits (A_{16}–A_{31}). The 32-bit address allows the HDC to directly access a linear (non-segmented) memory address space of up to 4 Gigabytes.

The presence of data is indicated by the $\overline{RD}$, $\overline{WR}$, and $\overline{READY}$ signals. The HDC drives data out onto the AD Bus (lines are configured as outputs) when $\overline{RD}$ is asserted in Slave Mode, or when $\overline{WR}$ is asserted in Master Mode. The HDC reads data in from the AD Bus (lines are configured as inputs) when $\overline{WR}$ is asserted in Slave Mode, or when $\overline{RD}$ is asserted in Master Mode.

Mode	$\overline{RD}$	$\overline{WR}$	AD_{0-15}
Slave	L	H	Output
Slave	H	L	Input
Master	L	H	Input
Master	H	L	Output

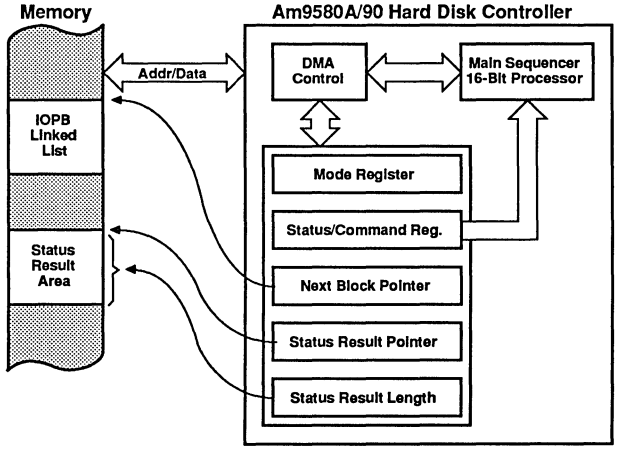
ALE Address Latch Enable (Output; Active HIGH)

ALE latches the lower address word (A_0–A_{15}) onto the external address latch. This output is never floating.

ALEN Upper Address Latch Enable (Output; Active HIGH)

ALEN latches the upper address word (A_{16}–A_{31}) onto the external address latch. This signal is active whenever the upper address is to be updated. The upper address is not updated at the beginning of each DMA burst; therefore, the upper address latch must not be shared with the CPU or other DMA devices. This output is never floating. (See also "System Interface" Section.)

Software Interface



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A/$\overline{S}$ Asynchronous/$\overline{\text{Synchronous}}$ (Input)

This input selects the $\overline{\text{READY}}$ input to be synchronous or asynchronous to the system clock (CLK). When A/$\overline{S}$ is HIGH, the HDC internally synchronizes the $\overline{\text{READY}}$ input. When A/$\overline{S}$ is LOW, $\overline{\text{READY}}$ must be synchronized externally. This input may only change state while the HDC is in the IDLE state. A/$\overline{S}$ is normally tied to +5 V or GND.

BACK Bus Acknowledge (Input; Active HIGH)

BACK acknowledges the HDC bus request, indicating that the CPU has relinquished the system bus to the HDC. Since BACK is internally synchronized, transitions on BACK do not have to be synchronous with the system clock (CLK). BACK may be removed, at any time, to make the HDC release the bus (bus preemption). If the HDC DMA is preempted by removing BACK, the HDC completes the current bus transaction and releases BREQ for the programmed dwell time so that external devices may gain system bus mastership. BACK must be active for at least one clock.

$\overline{\text{BHE}}$ $\overline{\text{Byte High Enable}}$ (Input/Output; Active LOW)

$\overline{\text{BHE}}$ enables data on the most-significant byte of the Address/Data Bus (AD_8–AD_{15}). The data bus is allocated as follows:

$\overline{\text{BHE}}$	A0	Data Lines	Type
0	0	AD_0–AD_{15}	Word transfer
0	1	AD_8–AD_{15}	Byte transfer on upper byte
1	0	AD_0–AD_7	Byte transfer on lower byte
1	1	—	None (reserved)

When the HDC is the bus master, this pin is an output. When the HDC is the bus slave, it is an input and must be stable for the entire cycle. $\overline{\text{BHE}}$ is ignored in Slave Mode, and is HIGH in Master Mode when the HDC is strapped to a byte interface.

BREQ Bus Request (Output; Active HIGH)

The HDC activates BREQ to request control of the system bus. BREQ timing is specified by the DMA Burst Length and DMA Dwell Time Parameters in the Mode Register.

B/$\overline{W}$ Byte/$\overline{\text{Word}}$ Strap (Input)

This pin selects either a byte (8 bits) (B/$\overline{W}$ HIGH) or word (16 bits) (B/$\overline{W}$ LOW) interface. When a byte interface is selected, only AD_0–AD_7 are used for data transfers, making all operations byte operations. When word interface is selected, AD_0–AD_{15} are used for data transfers. The HDC always uses a 32-bit address. This input may be altered only while the HDC is in the IDLE state.

HIGH = byte interface

LOW = word interface

CLK System Clock (Input)

CLK is a TTL-compatible clock input used to time DMA transfers and disk-control operations (e.g., seeks). The system clock drives all except the Disk Data Section of the HDC .

$\overline{\text{CS}}$ $\overline{\text{Chip Select}}$ (Input; Active LOW)

The host processor activates $\overline{\text{CS}}$ to enable a Slave Mode access to read or write HDC internal registers. $\overline{\text{CS}}$ may be asynchronous to the system clock (CLK). This pin is ignored when the HDC is in Master Mode.

$\overline{\text{DEN}}$ $\overline{\text{Data Enable}}$ (Output; Active LOW, Three State)

When the HDC is bus master, a LOW on this output enables an external data bus transceiver (DT/$\overline{R}$ specifies the direction). $\overline{\text{DEN}}$ is active when data is driven onto the Address/Data Bus (master write cycle), or the bus is three-stated when receiving the data (master read cycle). This output is three-stated when the HDC is not in control of the system bus.

DT/$\overline{R}$ Data Transmit/$\overline{\text{Receive}}$ (Output; Three State)

In Master Mode, this output indicates the direction of data flow. A HIGH indicates that the data is being transmitted from the HDC to memory (master write cycle). A LOW indicates that the data is being transferred from memory to the HDC (master read cycle). This output is floating when the HDC is not in control of the system bus.

INTR Interrupt Request (Output; Active HIGH)

INTR is activated when the HDC requires CPU service. Interrupt Request is reset whenever the upper byte (Status Byte) of the Status/Command Register (SCR) is accessed. The HDC asserts INTR after a hardware or software reset to indicate that the internal reset process has been completed. This interrupt cannot be disabled. Further interrupts are issued whenever the HDC enters the IDLE state (e.g., terminating a command chain). These interrupts may be disabled by resetting the Interrupt Mask in the Mode Register. The INTR output is never floating.

$\overline{\text{RD}}$ $\overline{\text{Read}}$ (Input/Output; Active LOW)

A LOW on this line indicates that the CPU or HDC is performing an I/O or memory read cycle. When the HDC is in Slave Mode, this is an input signal used by the CPU to read the internal registers of the HDC (slave access). When the HDC is the bus master, this signal is an HDC output to access data from memory.

In Slave Mode, the transfer control signals, $\overline{\text{RD}}$ and $\overline{\text{WR}}$, must not be active simultaneously, but may be asynchronous to the clock. In Master Mode, the HDC drives this line synchronously by using a 4-clock-cycle transfer.

$\overline{\text{READY}}$ $\overline{\text{Ready}}$ (Input/Output; Active LOW, Open Drain)

When the HDC is in control of the system bus, this is an input to allow slow memories and peripheral devices to extend the bus cycle. When the HDC is in Slave Mode, this is an output indicating that the HDC is ready to complete the current bus transfer. The CPU $\overline{\text{READY/WAIT}}$ input must be connected to the $\overline{\text{READY}}$ output of the Am9590 (in Slave Mode), because slave cycle length varies between 1 and 16 system clocks.

RESET Reset (Input; Active HIGH)

When RESET is active, all output lines are inactive, all three-state outputs are floating, and all inputs other then RESET are ignored. With the falling edge of RESET, the chip enters the initialization procedure. A RESET pulse is required after power-up. On completion of initialization, an interrupt request will be issued and INTR will go HIGH. If the user attempts to read from or write to the HDC prior to completion of initialization, the $\overline{\text{READY}}$ output will remain inactive until initialization has been completed; this causes the CPU to wait. After an initial hardware reset, a software reset (loading the Command Status field of the Status/Command Register with RESET) is equivalent to a hardware reset (pulse on the RESET input).

Power-up reset must be active after V_{cc} has been stable for a certain period. This can be achieved by a long reset pulse generated by an RC circuit during power-up, or by a short pulse after power-up. RESET must be HIGH for at least two system clock cycles.

$\overline{\text{WR}}$ $\overline{\text{Write}}$ (Input/Output; Active LOW)

A LOW on this line indicates that the CPU or HDC is performing an I/O or a memory write cycle. When the HDC is in Slave Mode, it is an input signal used by the CPU to load the internal registers of the HDC. When the HDC is the bus master, this signal is an HDC output to write data to the system memory. In Slave Mode, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ must not be active simultaneously.

Disk Interface Lines

Some of the pins described in this section have different functions, depending on the type of interface selected. The cross-reference list at the end of this section shows the relationship between interface and pin functions.

AMC/AMEN Address Mark Control/Address Mark Enable (Output; Active HIGH)

(AMC) Address Mark Control — The HDC asserts AMC in conjunction with Read Gate (RG) or Write Gate (WG), to command the external data separator to generate address marks (write operation), or to search for address marks (read operation). In either operation, the data separator acknowledges the completion of the requested operation by asserting Address Mark Found (AMF). In write cycles, this signal indicates that the address mark has been generated. The type and length of the address mark is completely transparent to the HDC. The data separator may therefore generate any address mark. In read cycles, AMF indicates that an address mark has been found.

9590 only

(AMEN) Address Mark Enable — For ESDI interface, this pin causes the ESDI drive to either write an address mark (in conjunction with WG) or to search for an address mark (no RG activated).

AMF/SECT Address Mark Found/Sector (Input; Active HIGH)

(AMF) Address Mark Found — In ST506/412 or Floppy Modes, the data separator asserts AMF in response to AMC to acknowledge that an address mark has been generated (write cycle) or found (read cycle). In ESDI mode (soft-sectored), the disk drive generates AMF. The AMF signal must be asserted in the Read/Reference Clock (RD/REFCLK) cycle after the data separator has put out the last address mark bit (write cycle), or in the RD/REFCLK cycle when the data separator provides the first data bit after the address mark (read cycle).

9590 only

(SECT) Sector — For hard-sectored ESDI drives, this signal indicates to the Am9590 the start of a new sector.

DI_0 Disk Interface Control 0 (Input; Output, Active HIGH)

(RTZ) Return To Zero — In Hard-Disk Mode, a pulse on the RTZ output should re-calibrate the head to Track 0 (TRK0). The HDC may also re-calibrate the drive by issuing STEP pulses until Track 0 is reached (TRK0 becomes active). The RTZ pulse has the same width as the STEP pulse. The drive should assert SC (Seek Complete) as an indication of the completion of the requested re-calibration. If the drive asserts SC (LOW), and TRK0 is LOW, the Am9590 will assume that re-calibration has failed. In this case, the HDC continues to re-calibrate the drive by issuing STEP pulses until Track 0 is reached (TRK0 becomes HIGH).

(MON) Motor On — In Floppy Mode, this output provides Motor On signals for the floppy-disk drive. Whenever a floppy-disk drive is selected and MON is asserted HIGH, it turns on the spindle motor of the selected drive(s). The HDC waits for a programmed period before attempting any read or write access to the drive (see Drive Parameter Block description).

9590 only

Command Complete — In ESDI Mode, this input indicates to the HDC whether the drive has completed a command or if a new command may be issued. Command Complete goes inactive upon the reception of the first Command Data bit. It stays inactive until the command has been executed. Command Complete is also monitored after a head change during disk-data transfers. This allows the drive to have any head-settle time that is required.

($HDSEL_4$) Head Select 4 — For Special interface, this is the second most significant bit of the head number.

DI_1 Disk Interface Control 1 (Output; Active HIGH)

(DIRIN) Direction In — DIRIN indicates the direction the head should move on STEP pulses. When HIGH, the head should move towards higher track numbers (in or towards the disk spindle). When LOW, it should move towards lower track numbers (out). DIRIN will be asserted at least four clock cycles before any seek pulses are issued. It remains stable during the entire stepping operation until at least four clock cycles after the last STEP pulse.

9590 only

Command Data — For the ESDI interface, the Am9590 uses this pin to send serial ESDI command words, plus parity, to the disk drive.

($HDSEL_3$) Head Select 5 — For the Special interface, this is the most significant bit of the head number.

DI_2 Disk Interface Control 2 (Output; Active HIGH)

STEP — The HDC pulses the STEP line to move the head from one track to the next. The width and spacing of pulses are programmable, allowing an easy upgrade path to higher performance drives. The disk drive should initiate the head movement with the rising edge of STEP. SC (Seek Complete) must go inactive after the HDC has issued the first STEP pulse.

9590 only

(TRQ) Transfer Request — For ESDI interface, the HDC uses this pin to request a data transfer (one bit at a time) to or from the drive. If data is transferred to the drive, the pin is activated when a command bit is present on the Command/Data line. It is de-asserted after the ESDI disk drive responds with Transfer Acknowledge (TACK). If data is received from the drive, TRQ indicates that the HDC is ready to receive a bit from the drive. Again, TRQ is de-asserted with the reception of TACK.

(TDATA) Track Data — In Restricted Seek Mode and Special Mode, TDATA provides the current track number (16 bits) each time the track number needs to be updated. A shift clock is available on the DI_3 output.

DI_3 Disk Interface Control 3 (Output; Active HIGH)

(PCEN) Precompensation Enable — This output indicates whether the data write encoder should initiate precompensation on the encoded disk-write data pulse stream. PCEN will be valid for at least four system clocks prior to any disk-write operation (WG LOW), and will remain valid for at least four system clocks after the disk-write operation (WG HIGH). PCEN is asserted if the current track number is greater than or equal to the Precompensation Track Parameter specified in the Drive Parameter Block for the selected drive. No other internal processing takes place.

HIGH — Precompensation enabled
LOW — Precompensation disabled

PCEN should be connected to PCEN/S($\overline{D}$) of the Am9582, even if precompensation is not used. When $\overline{SELEN}$ is asserted, this output is pulsed LOW to select Double-Density Floppy Mode.

(TCLK) Track # Clock — In Restricted Seek and Special Modes, this output provides the shift clock for the serial track information provided on Track Data (TDATA). See the following description on Disk Interface Control 2 (DI_2).

$\overline{DREADY}$ $\overline{Drive\ Ready}$ (Input; Active LOW)

Drive Ready indicates that the currently selected drive is ready to read, write, or seek. This signal should be connected to the $\overline{DRSELECTED}$ signal of the drive. It must become LOW within 100,000 system clocks after $\overline{SELEN}$ is asserted by the HDC (see Motor On description for Floppy Mode). Once asserted by the selected drive, any negation of this line causes the current IOPB to be aborted. $\overline{DREADY}$ is ignored while $\overline{SELEN}$ is HIGH. $\overline{DREADY}$ must be de-asserted before re-accessing the drive.

$DRSEL_{0,1}$ Drive Select 0,1 (Outputs; Active HIGH)

$DRSEL_{0,1}$ designates which of the four possible drives is expected to respond to the assertion of $\overline{SELEN}$.

$DRSEL_1$	$DRSEL_0$	Drive Selected
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

$DRSEL_0$ and $DRSEL_1$ are the two least-significant bits of the drive number specified in the Input/Output Parameter Block (IOPB).

ECCERR External ECC Error (Input; Active HIGH)

When using the external ECC option, this input is asserted when the external ECC logic finds an error. During a read operation, the Am9590 samples ECCERR at the end of Postamble 2 to determine if an error has been detected by the external ECC logic. This input should always be grounded except for a data-field read operation.

FAM_0 /ECC_0 Floppy Address Mark 0/External ECC Control 0 (Output; Active HIGH)

FAM_1 /ECC_1 Floppy Address Mark 1/External ECC Control 1 (Output; Active HIGH)

The external ECC option, in conjunction with the outputs ECC_0 and ECC_1, provide status control for the external ECC logic. These dual-function lines either control external ECC (hard-disk format, external ECC enabled) or

indicate the type of address mark to be used (double-density floppy format, AMC HIGH). The four states are encoded as follows:

ECC CONTROLS

ECC_1, ECC_0	State	Comment
00_B	Idle	No operation in the external ECC.
01_B	Reset	External ECC should reset and prepare itself for an operation.
11_B	Generate	Whether reading or writing, the external ECC should strobe data in and generate a check-sum.
10_B	Check	When reading, this state indicates that the ECC should accept the check-sum from the disk. When writing, it should gate the check sum to the disk.

These states always proceed in the Gray code progression shown above, i.e., 00-01-11-10-00, which can be decoded without glitches. The nominal state of these lines is 00 (Idle).

Double-Density Floppy Mode, in conjunction with Floppy Address Mark outputs (FAM_0, FAM_1), tell the data separator to generate an Index Address Mark (IXAM) rather than a normal address mark. The two states that can be encoded are as follows:

00 = Index Address Mark (IXAM)

10 = Data Field or Header Address Mark (DAM, IDAM)

In ST506/412 and ESDI, these will be 10.

FAULT Fault (Input; Active HIGH)

For ST506/412, floppy, and SMD operations, this indicates a fault in the selection of the current drive, or a fault within the selected drive. For normal operations, FAULT must be inactive (LOW) as long as $\overline{\text{DREADY}}$ is active (LOW). FAULT is considered valid after $\overline{\text{DREADY}}$ is asserted. If it is asserted by the selected drive, the HDC will immediately abort the current IOPB and deselect the drive. This signal should be connected to the $\overline{\text{READY}}$ pin of the drive.

9590 only

For ESDI interface, this pin must to be inactive during a read, write, or seek operation. If it is asserted during a read, write, or seek, the HDC will immediately abort the current IOPB and deselect the drive. It is disregarded during a serial communication.

$HDSEL_{0,1}$ Head Select 0, 1 (Output; Active HIGH)

These are the two lower-order bits of the head number selected.

HLD/$HDSEL_2$ Head Load/Head Select 2 (Output; Active HIGH)

(HLD) Head Load — For floppy drives, this pin provides the Head Load signal. SC (Seek Complete) is sampled eight clocks after the assertion of HLD. If SC is LOW, the HDC waits for it to go HIGH. If SC is HIGH, the HDC assumes that the heads are already loaded.

($HDSEL_2$) Head Select 2 — For hard-disk drives, this pin provides Bit 2 of the head number.

INDEX Index (Input; Active HIGH)

INDEX marks each revolution of the disk. INDEX should be valid as long as $\overline{\text{DREADY}}$ is asserted. The HDC uses INDEX to keep track of the number of complete disk revolutions encountered during disk I/O operations, and/or to indicate the physical beginning of the track. Only the leading (rising) edge of INDEX is significant. Depending on the drive parameters programmed, the first sector might begin before INDEX has gone inactive (LOW).

RDDAT Read Data (Input; Active HIGH)

RDDAT is the NRZ (Not Return to Zero) disk-data input. The HDC samples RDDAT with the rising edges of RD/REFCLK.

RD/REFCLK Read/Reference Clock (Input)

RD/REFCLK is a TTL-compatible clock input that controls the operation of the data section of the HDC. This clock samples the read data (Read Clock) and strobes out write data (Reference Clock). It is assumed to be valid 16 system clocks (CLK) after a drive-selection acknowledge ($\overline{\text{DREADY}}$) is received, and must remain valid until $\overline{\text{SELEN}}$ is de-asserted. While valid, this clock should be free from any glitches (the specified clock HIGH and LOW widths must not be violated).

RG Read Gate (Output; Active HIGH)

RG indicates that a disk-read operation is in progress. It commands the Phase-Locked Loop (PLL) of the data separator to lock the RD/REFCLK to the serial-read data from disk. This output changes synchronously with RD/REFCLK.

RWC/$HDSEL_3$ Reduced Write Current/Head Select 3 (Output; Active HIGH)

(RWC) Reduced Write Current — RWC indicates that the head is over an inner track where the write current should be reduced. RWC is activated whenever the current track number is greater than or equal to the RWC track parameter, specified in the Drive Parameter Block for each drive. No internal processing of RWC takes place in the HDC. RWC operation is similar to that of Precompensation Enable (PCEN). If RWC is used to control the write current, the write current should be reduced when RWC goes active (HIGH). A programmable option bit within the Drive Parameter Block configures this output.

($HDSEL_3$) Head Select 3 — This pin provides Bit 3 of the head number.

SC/CSD Seek Complete/Configuration Status Data (Input; Active HIGH)

(SC) Seek Complete — The drive asserts SC to indicate to the HDC that the head is loaded (only for Floppy Mode) and the drive is ready for another seek operation. This line is sampled and verified HIGH before starting any seek operation.

(CSD) Configuration Status Data — If the ESDI interface (Serial Mode) is selected, this line is the serial data input for configuration/status information from the drive.

$\overline{\text{SELEN}}$ $\overline{\text{Select Enable}}$ (Output; Active LOW)

$\overline{\text{SELEN}}$ = LOW enables the drive specified by $DRSEL_{0,1}$. When $\overline{\text{SELEN}}$ = HIGH, no drive is selected. The disk drive must respond to $\overline{\text{SELEN}}$ LOW by bringing $\overline{\text{DREADY}}$ LOW. See $\overline{\text{DREADY}}$ and MON descriptions.

TRK0/TACK Track 0/Transfer Acknowledge (Input; Active HIGH)

(TRK0) Track 0 — The selected drive must assert TRK0 whenever the head is positioned over the outermost track (Track 0). This is the only hardware indicator that the head is positioned over a specific track. This input is sampled only when the HDC is performing a drive restore operation. Here, the HDC provides single STEP pulses (DIRIN LOW), waits for SC to go inactive (LOW), returns to active (HIGH), and then samples TRK0. Whenever TRK0 is asserted, the HDC assumes that the heads have restored to Track 0.

9590 only

(TACK) Transfer Acknowledge — For the ESDI interface, this pin, with Transfer Request (TRQ), handles the asynchronous handshake for the serial command transfer between the Am9590 and the ESDI hard-disk drive.

WG Write Gate (Output; Active HIGH)

WG indicates that a disk-write operation is in progress. It commands the data separator to lock the RD/REFCLK to a constant frequency source (e.g., a crystal oscillator) to provide a stable reference clock for the write operation. This output changes synchronously with RD/REFCLK.

WRCLK Write Clock (Output; Active LOW)

This is the Reference Clock output for ESDI write operations. It is inverted from, and synchronous to, the Reference Clock input (RD/REFCLK). WRCLK must not be connected to the Am9582 Write Clock input.

WRDAT Write Data (Output; Active HIGH)

WRDAT is the NRZ disk-data output. Transitions occur on the rising edge of RD/REFCLK.

WRPROT/ATT Write Protected/Attention (Input; Active HIGH)

(WRPROT) Write Protected — Before the HDC attempts to write data to the currently selected drive, the HDC samples WRPROT to determine whether the drive is write protected (WRPROT HIGH). If it is, the current IOPB is immediately aborted. Typically, in Hard-Disk Mode, this input should be tied LOW (inactive), and considered valid after $\overline{\text{DREADY}}$ is asserted. It is ignored during "read-only" types of commands. When $\overline{\text{SELEN}}$ is inactive (HIGH), this input is also ignored.

9590 only

(ATT) Attention — For ESDI interface, this line has to be valid after $\overline{\text{DREADY}}$ becomes active. With this signal, an ESDI drive indicates to the controller that status information can be read from the drive (usually this is an error condition). If ATT becomes active when the HDC attempts a read or write operation, the HDC will abort immediately and deselect the drive.

TABLE 1. DRIVE INTERFACE PIN CROSS-REFERENCES

Pin Name	Pin #	Floppy	ST506/412	9590 only ESDI (Serial)	9590 only Special
$\overline{\text{SELEN}}$	68	$\overline{\text{SELEN}}$	$\overline{\text{SELEN}}$	$\overline{\text{SELEN}}$	$\overline{\text{SELEN}}$
$DRSEL_1$	66	$DRSEL_1$	$DRSEL_1$	$DRSEL_1$	$DRSEL_1$
$DRSEL_0$	67	$DRSEL_0$	$DRSEL_0$	$DRSEL_0$	$DRSEL_0$
$\overline{\text{DREADY}}$	64	$\overline{\text{DREADY}}$	$\overline{\text{DREADY}}$	$\overline{\text{DREADY}}$	$\overline{\text{DREADY}}$
WRPROT/ATT	63	WRPROT	WRPROT	ATT	WRPROT
FAULT	62	FAULT	FAULT	FAULT	FAULT
SC/CSD	61	SC	SC	CSD	SC
TRK0/TACK	65	TRK0	TRK0	TACK	—
DI_3	56	PCEN	PCEN	TCLK	TCLK
DI_2	59	STEP	STEP	TRQ	TDATA
DI_1	58	DIRIN	DIRIN	Command Data	$HDSEL_5$
DI_0	57	MON	RTZ	Command Complete	$HDSEL_4$
$RWC/HDSEL_3$	51	RWC	$RWC/HDSEL_3$	$HDSEL_3$	$HDSEL_3$
$HLD/HDSEL_2$	53	HLD	$HDSEL_2$	$HDSEL_2$	$HDSEL_2$
$HDSEL_1$	54	—	$HDSEL_1$	$HDSEL_1$	$HDSEL_1$
$HDSEL_0$	55	SIDE	$HDSEL_0$	$HDSEL_0$	$HDSEL_0$
INDEX	39	INDEX	INDEX	INDEX	INDEX
AMC/AMEN	49	AMC	AMC	AMEN	AMC/AMEN
AMF/SECT	50	AMF	AMF	AMF/SECT	AMF/SECT
RG	47	RG	RG	RG	RG
WG	48	WG	WG	WG	WG
RD/REFCLK	44	RD/REFCLK	RD/REFCLK	RD/REFCLK	RD/REFCLK
WRCLK	52	—	—	WRCLK	WRCLK
WRDAT	42	WRDAT	WRDAT	WRDAT	WRDAT
RDDAT	41	RDDAT	RDDAT	RDDAT	RDDAT
ECCERR	40	—	ECCERR	ECCERR	ECCERR
FAM_1/ECC_1	46	FAM_1	FAM_1/ECC_1	ECC_1	ECC_1
FAM_0/ECC_0	45	FAM_0	ECC_0	ECC_0	ECC_0

FUNCTIONAL DESCRIPTION

The HDC supports two interfaces as shown in the block diagram. The system interface (see Figure 1) communicates with the host CPU and system memory. The disk interface controls the data separator and the disk drives.

System Interface

The HDC is designed for easy interfacing to most 8-bit or 16-bit, multiplexed or demultiplexed, synchronous or asynchronous, microprocessor buses. A strap pin programs the system interface for either byte (8 bits) or word (16 bits) mode. In Slave Mode, the host CPU can access the internal registers of the HDC. In Master Mode, the on-chip DMA controller controls the system bus.

DMA Controller

The on-chip DMA controller provides the HDC with the ability to execute complex disk I/O operations without host CPU intervention. The DMA controller scans the command chain stored in system memory, updates the Status Result Area when errors occur, and transfers the data between the internal sector buffers and system memory. Data may be stored in non-contiguous memory; for example, to support linked-list data storage in word processing systems.

The DMA controller generates 32-bit linear addresses to directly access up to 4 Gigabytes of system memory. For multi-bus-master systems, DMA transfers can be throttled to dedicate only a certain share of the system bus bandwidth to the HDC. The Mode Register (Figure 9) specifies DMA burst length and dwell. DMA bursts can be preempted by removing Bus Acknowledge (BACK). The HDC can insert a programmable number of software wait states into DMA bus cycles. Additionally, hardware wait states can be added via the $\overline{\text{READY}}$ input. The HDC updates the upper address word (A_{16}–A_{31}) when there is a carry-out of the lower 16 address bits.

User Registers

The Mode Register defines the operation of the DMA controller. The Status/Command Register controls the basic operation of the HDC itself. The Next Block Pointer (NBP) Register links to the first Input/Output Parameter Block (IOPB) of the command chain. The Status Result Pointer Register and the Status Result Length Register define the Status Result Area where the HDC stores the status for each IOPB.

Main Sequencer

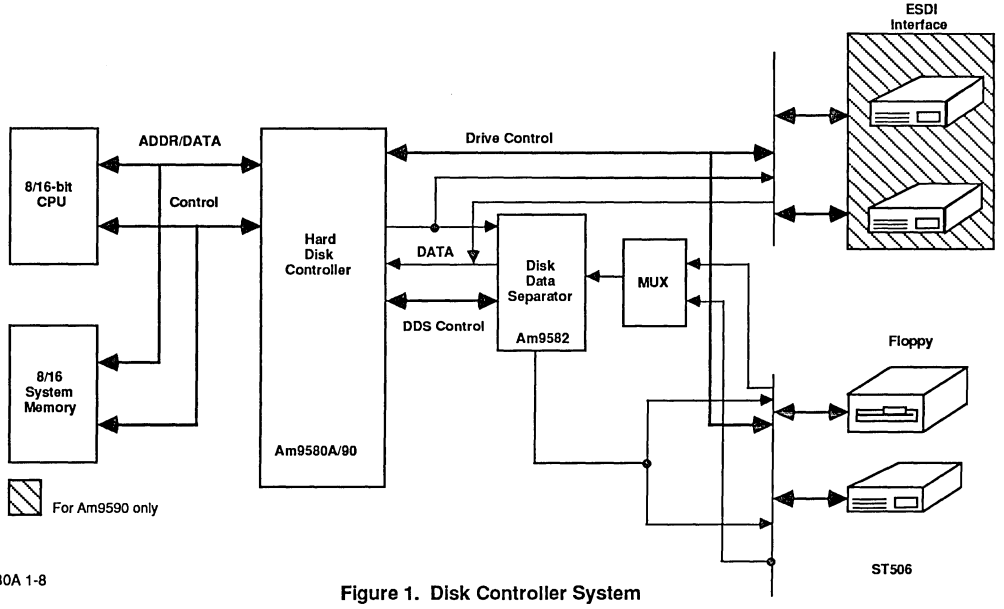
The Main Sequencer translates the high-level system commands into the control signals for the various independent functional sections of the HDC. This 16-bit processor relieves the system CPU of complex data manipulations.

Drive Parameter RAMs

The Drive Parameter RAMs store the specification parameters for drives that adapt the HDC to any combination of disk recording schemes. The contents can be altered any time with a single IOPB. Once loaded, these parameters allow disk commands to be independent of the drive type or track format. For example, the write command is the same whether it is for a double-density floppy-disk drive or a Winchester hard-disk drive.

Error Checking

The HDC features two powerful Reed-Solomon error-correcting codes, as well as the industry-standard error detection code, CRC-CCITT. It also supports a user-definable, external error correction scheme. Along with programmable retry and correction attempt policy, the HDC allows maximum control of data integrity.



09480A 1-8

Figure 1. Disk Controller System

Sector Buffers

The HDC transfers data to or from disk without adding time constraints on the system bus bandwidth. The two internal sector buffers (Figure 2) can be filled or emptied, at any speed, without interfering with data transfer between sector buffers and the disk. The two internal sector buffers are toggled for zero-sector interleave disk-data operations.

While one sector buffer is filled with data from disk, the other buffer is emptied by the DMA controller. Physically, contiguous sectors on a track can thus be read or written "on the fly" (during one revolution of the disk).

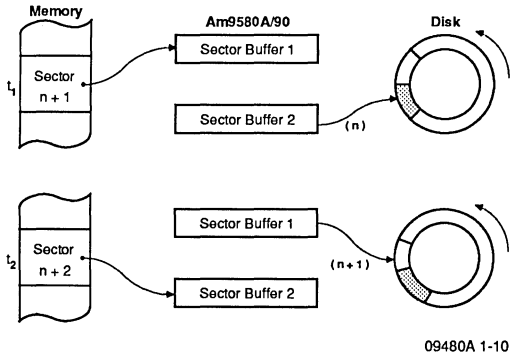


Figure 2. Dual On-Chip Sector Buffers

Disk Control Interface

Am9580A Only

The Am9580A has a disk control interface which provides all the control lines to directly handle the ST506/412 and double-density floppy-disk interfaces. Other drive interface standards can be supported using external circuitry. The controller can support any combination of floppy-disk and hard-disk drives. The drive parameters can be individually specified in one out of four Drive Parameter Blocks.

Am9590 Only

The Am9590 has a disk control interface which provides all the control lines to directly handle the ESDI, ST506/412, and double-density floppy-disk interfaces. Other drive interface standards can be supported using external circuitry. By using the ST506/412 and floppy options, the Am9590 issues STEP pulses to position the heads to the desired cylinder. STEP width and dwell times, as well as head-settling times, are programmable. If the ESDI interface is selected, the HDC will automatically generate seek and restore commands to the ESDI drive using the serial communication link (Figure 3). Other ESDI commands, such as REQUEST STATUS and REQUEST CONFIGURATION, can be issued by the CPU using the ESDI Channel IOPB of the Am9590. The controller can support any combination of floppy-disk, ESDI, and ST506/412 hard-disk drives. The drive parameters can be individually specified in one out of four Drive Parameter Blocks.

The HDC can perform implied and overlapped seeks. When the implied seek option is selected, the HDC automatically causes the appropriate seeks when issuing a read or write command. If this option is disabled, the seek operation has to be performed externally.

When the overlapped seek option is selected, several drives can seek in parallel, thus minimizing the seek overhead in multiple disk-drive systems. After the HDC has issued a seek command to one drive, and while this drive performs the seek, the HDC scans subsequent IOPBs for commands requiring seeks on other drives. If the HDC finds such commands, it issues seek commands to these drives to make them seek in parallel. After the first drive has finished the seek operation, the HDC resumes execution of the command chain.

Disk Data Interface

Am9580A Only

The Disk Data Interface of the Am9580A handles the serial data input and output to the disk drive. It controls the Address Mark handshake with the data separator, as well as the optional external ECC logic. Operating asynchronously to the

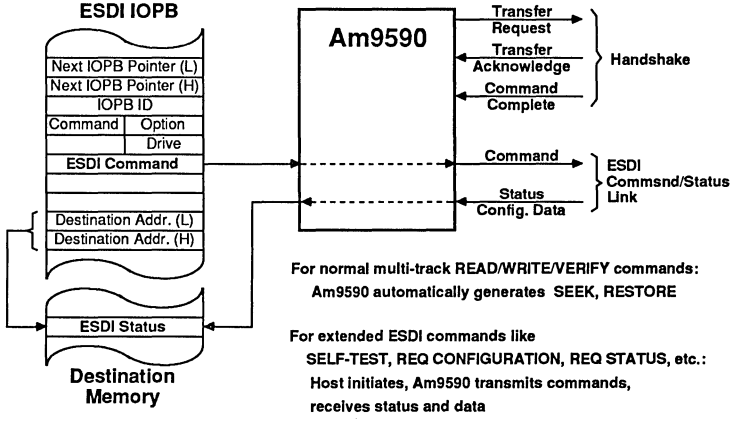


Figure 3. ESDI Serial Command/Status Communications

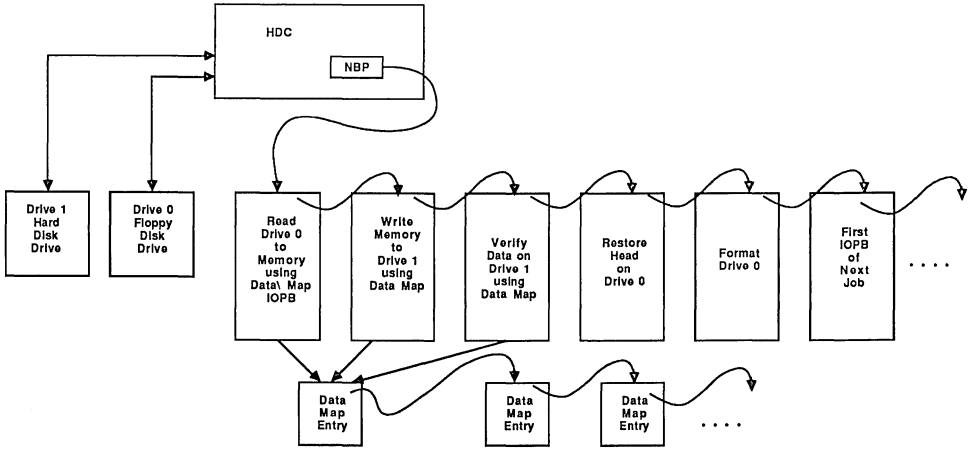
other blocks of the device, the Disk Data Interface is driven by the Read/Reference Clock (RD/REFCLK) generated by the data separator. The Disk Data Interface converts the data stored in the sector buffer into a serial bit-stream for the disk, or it de-serializes the incoming bit-stream to be loaded into one of the sector buffers. Non-data information, such as the header (sector ID field), pads, gaps, preambles, and postambles, is conditioned according to the parameters stored in the Drive Parameter RAMs to meet the defined recording standard.

Am9590 Only

The Disk Data Interface of the Am9590 handles the serial data input and output to the disk drive. It controls the Address Mark handshake for soft-sectored ESDI drives as well as hard-sectored drives. In ST506/412 and Double-Density Floppy Mode it also controls the data separator. Operating asynchronously to the other blocks of the device, the Disk Data Interface is driven by the Read/Reference Clock (RD/REFCLK). This clock is either driven by the disk drive (ESDI) or by the data separator (ST506/412, Floppy Disk). In ESDI mode, the device provides a synchronous Write Clock output. The Disk Data Interface converts the data stored in the sector buffer into a serial bit-stream for the disk, or it de-serializes the incoming bit-stream to be loaded into one of the sector buffers. Non-data information, such as the header (sector ID field), pads, gaps, preambles, and postambles, is conditioned according to the parameters stored in the Drive Parameter RAMs to meet the defined recording standard.

IOPB Command Structure

The HDC features a high-level data and command structure (Figure 4). The basic unit of this command structure is the Input/Output Parameter Block (IOPB). The host CPU creates IOPBs in system memory to pass control and status information to the HDC. The HDC fetches these IOPBs by using the on-chip DMA controller. Each IOPB specifies one disk com-



09480A 1-12

Figure 4. Command Chaining Example

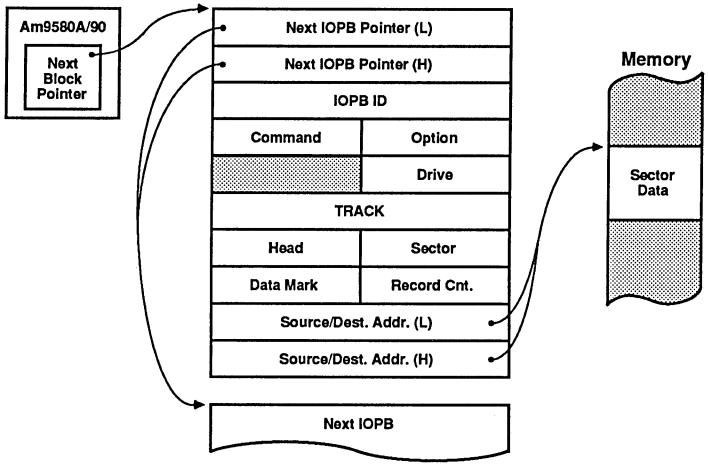


Figure 5. IOPB Address Sequence

09480A 1-13

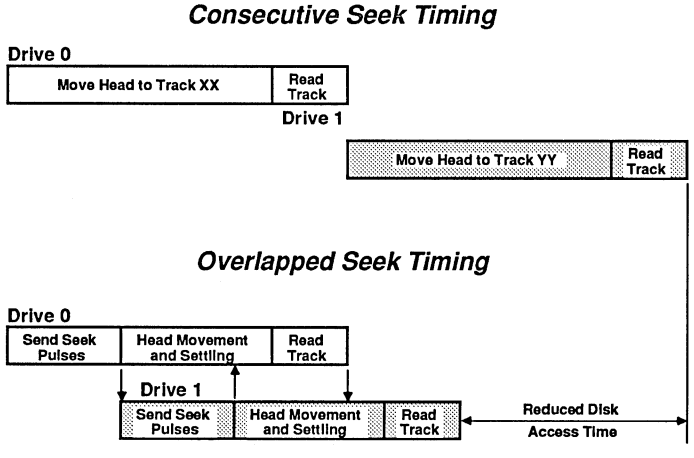


Figure 6. Seek Modes

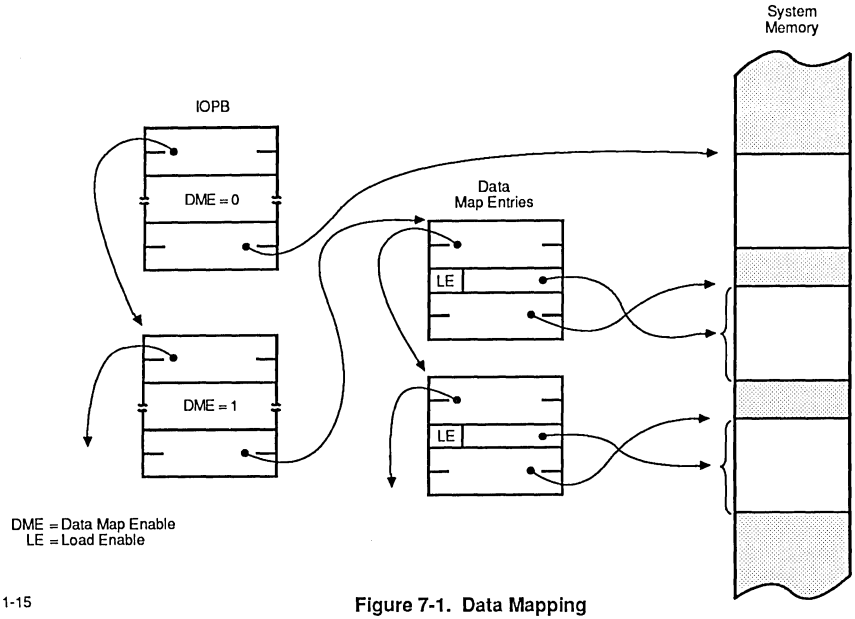
09480A 1-14

mand, and contains all parameters needed to execute it (Figure 5). To start execution of an IOPB, the host CPU loads the address of the IOPB into the Next Block Pointer Register and writes the "Start Chain" command by programming the Status/Command Register. After the IOPB is executed, the HDC reports the status information and waits for further instructions. The host CPU can examine the Status/Command Register for information about the command termination. The CPU can also get status from the Status Result Block in memory if an error occurs.

As an option, IOPBs may be put together in a linked-list format that the HDC can interpret sequentially. With this structure, a complex list of disk commands can be set up and then executed by the HDC without CPU intervention. The CPU is then totally free from any disk control processing. For example, the host CPU might set up a list of commands for the HDC to copy an entire floppy disk to a hard disk and verify that the data has been copied correctly. Upon verification, the HDC reformats the floppy disk, all without host CPU intervention.

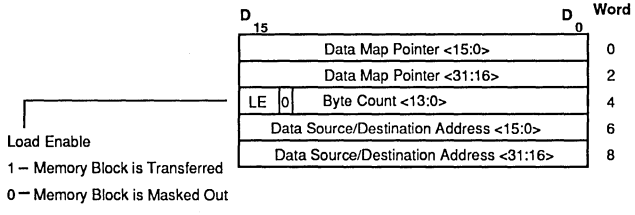
An IOPB command chain is basically a queue of jobs waiting for HDC execution. This offers a predefined and efficient structure for the operating system to handle its disk I/O. The ID field of the IOPB provides the linkage between a particular disk command and the user process that made the disk request. The jobs can thus be placed in the HDC job queue and then ignored by the operating system unless an error occurs. All the information required to retrace an error is provided by the HDC Status Result Block.

Since the HDC manages the disk job queue, it can look ahead in the queue to overlap several time-consuming operations. Head movement (seeking) can require a major portion of the disk access. Since the HDC controls up to four drives, it can perform an IOPB operation on one drive while it is executing seeks for future IOPBs on the other drives. This eliminates the seek-time overhead when those subsequent IOPBs are finally executed (Figure 6).



09480A 1-15

Figure 7-1. Data Mapping



09480A 1-26

Figure 7-2. Data Map Entry

Data Mapping

Sector data to be transferred to or from the disk may be stored in non-contiguous system memory using the data mapping option (Figure 7-1.). Definable portions of a disk file can be written or read from separate areas of memory on a byte-by-byte basis. The data map defines the linked-list data structure. The data map option is processed by the HDC, while the disk is in operation, so that data maps can be handled without affecting the data transfer rate. Virtual memory systems can employ this feature to arrange memory pages directly with the HDC and eliminate the time-consuming task of moving data blocks to the appropriate locations.

Status Result Blocks

When the HDC finds that an IOPB has caused an error, it writes a Status Result Block (SRB). Errors might be caused by invalid command codes, disk read and write errors, and seek or memory time-outs. Since the SRB contains the ID number for the IOPB that caused the error, the operating system can determine which disk I/O job caused the error and report this to the user. Depending on the type of error and what policy has been selected, the HDC may continue with the IOPB chain automatically, or wait for the host processor to tell it whether to start over or continue. The SRBs contain all the specific information required to find the exact location of the error and to make recovery as complete as possible.

Registers

When the IOPB command chain has been set up, the Next Block Pointer Register of the HDC is set to point to the first IOPB in the chain. Writing a Start Chain command to the Status/Command Register (Figure 8) causes the HDC to copy the first IOPB into its internal memory. The Next Block Pointer always points to the current command in the IOPB chain. The Status/Command Register also reports HDC error and status codes (such as memory time-outs, IOPB option results, and other information related to the internal operation of the HDC).

The Status Result Pointer points to an area of contiguous memory (Status Result Area) reserved for Status Result Blocks (SRBs). The length of this memory block is defined by the Status Result Length Register which specifies the number of SRBs (each SRB is 10 bytes). The error-handling scheme of the operating system can manipulate this as needed to coordinate disk use.

The Mode Register (Figure 9) controls how much of the system bus bandwidth is allocated to the HDC, and how much is left to meet other system requirements. For more information, refer to the Technical Manual.

TABLE 2. REGISTER ADDRESSES

$\overline{CS}$	A_3	A_2	A_1	Register Accessed
L	L	L	L	Status/Command Register
L	L	L	H	Mode Register
L	L	H	L	Next Block Pointer (low word)
L	L	H	H	Next Block Pointer (high word)
L	H	L	L	Status Result Pointer (low word)
L	H	L	H	Status Result Pointer (high word)
L	H	H	L	Status Result Length
L	H	H	H	Reserved
H	X	X	X	No Register Accessed

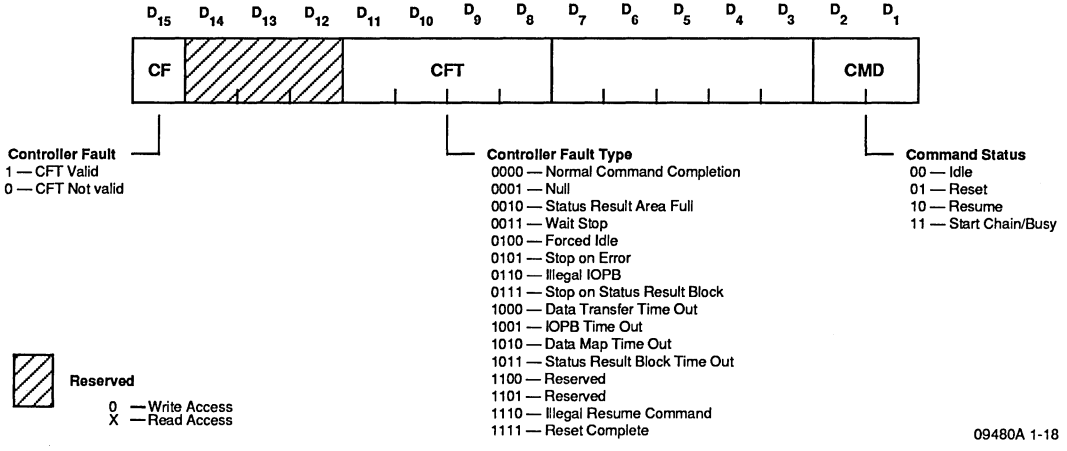


Figure 8. Status/Command Register

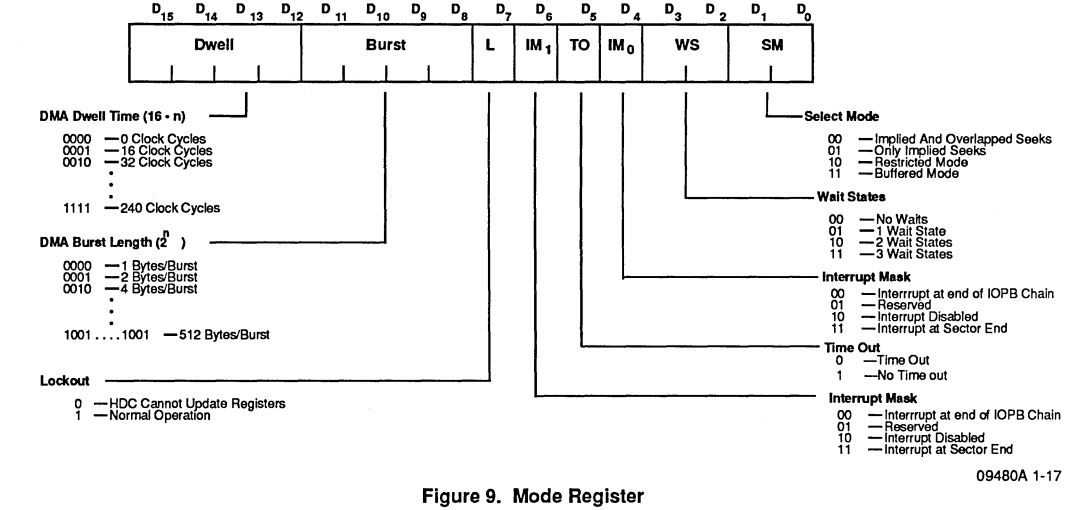


Figure 9. Mode Register

COMMAND DESCRIPTION

All operations of the HDC result from commands which are set up in system memory in IOPBs (I/O Parameter Blocks). The HDC starts interpreting the command list after receiving the "Resume Chain" or "Start Chain" command from the host CPU (see Status/Command Register description). Errors and warnings on command execution are reported by adding Status Result Blocks (SRB) to the Status Result Area. Table 3 cross-references the error types (SRBs) and commands (IOPBs).

Each IOPB consists of ten 16-bit words which reside in system memory (Figure 10). The HDC always fetches all ten IOPB words sequentially; it does not skip "don't care" fields. For Seek-Look-Ahead fetches only the first six words are read.

Read

This command reads single or multiple sectors from disk and loads the data into the destination memory location. The operation can cross head as well as track boundaries.

Write

This command writes single or multiple sectors to disk and load the data from the source memory location. The operation can cross head as well as track boundaries.

Verify

This command reads single or multiple sectors from disk and compares the data to the source memory location specified. The operation can cross head as well as track boundaries.

Format

This command formats single or multiple tracks. It writes sector headers and data fields with a user-definable pattern. The operation can cross head as well as track boundaries.

Relocate Track

This command marks a specified track as relocated. It also writes the relocation vector into each sector data field.

Load Drive Parameter Block

This command loads the Drive Parameter Block from the specified source memory location into the Internal Drive Parameter RAM of the specified drive number.

Dump Drive Parameter Block

This command dumps the Drive Parameter Block from the Internal Drive Parameter RAM of the specified drive number to the specified destination memory location.

Read Physical Sector

This is a recovery command for marginal data on the disk. It allows reading of a sector data field, disregarding the header information. This command is a single-sector command.

Read ID

This command allows reading of the sector header information.

Load Buffer

This command loads an internal sector buffer from the specified source memory location.

Dump Buffer

This command dumps an internal sector buffer to the specified destination memory location.

Load Syndrome

This command loads the ECC Syndrome RAM with a given pattern located at the source memory location

Dump Syndrome

This command dumps the ECC Syndrome RAM to the destination memory location.

Correct Buffer

After loading the Syndrome RAM, this command allows correction of a data buffer, using the pattern loaded. It can be used if the internal ECC logic is not capable of correcting an error.

Seek

This command will cause the HDC to seek the drive head(s) to a specified cylinder.

Restore

This command will cause the HDC to seek the drive head(s) to cylinder "0". It must always be issued after a RESET.

ESDI Channel

This command sends ESDI command words (bytes 10 and 11) to the ESDI drive and receives status information from the drive. Status information will be dumped into the destination memory location. The command generates and checks the parity bit automatically.

Move Data

The Move Data command allows the HDC to double as a "general-purpose" DMA controller. It is not truly general purpose because it only allows you to move blocks equal to a sector size (128, 256, or 512 bytes) or multiples of a sector size. It does allow you to do Move Data from one area in memory to another. This is very useful when doing disk caching or when just another DMA channel is needed.

TABLE 3. STATUS RESULT BLOCKS

STATUS RESULT BLOCK	Byte 1	Byte 0	Byte 3	Byte 2	Byte 5	Byte 4	Byte 7	Byte 6	Byte 9	Byte 8
Index Error	ID			00_H	Track			Head		
No IDs Found on Track	ID			01_H	Track			Head		
Seek Error	ID			02_H	Current Track		Desired Track		Current Head	Desired Head
Data Recovered with ECC	ID		Retry Count	03_H	Track			Head		Sector
Data Sync Fault	ID			04_H	Track			Head		Sector
Relocated Track Found	ID			05_H	Current Track		Relocated Track		Current Head	Relocated Head
Relocated Track, No Vector Recovered	ID			06_H	Track			Head		
Record Not Found with ID Errors	ID			07_H	Track			Head		Sector
Fatal Seek Error	ID			08_H	Current Track		Desired Track		Current Head	Desired Head
Record Not Found	ID			09_H	Track			Head		Sector
Data Recovered with Retries	ID		Retry Count	$0A_H$	Track			Head		Sector
Data Non-Verify	ID			$0B_H$	Track			Head		Sector
Data Time-Out	ID			$0C_H$	Byte Count		Block Address <15:0>		Block Address <31:16>	
Multi-Record Overflow	ID			$0D_H$	Track			Head		Sector
Data Mark Error	ID		Current Data Mark	$0E_H$	Track			Head		Sector
Sector Size Mismatch	ID		Actual Size	$0F_H$	Track			Head		Sector
ECC Not Selected	ID			10_H						
Drive Selection Fault	ID		Status	11_H						
Fault While Seeking	ID		Status	12_H	Track					
Fault While Head Select	ID		Status	13_H				Head		
Drive Trap Status	ID		Status	14_H						
End of Data Map	ID			15_H						
Restore Fault	ID		Status	16_H	Track					
Data Not Recovered	ID			17_H	Track			Head		Sector
Multi Record Command Terminated	ID			18_H	Track			Head		Sector
ID CRC Error	ID			19_H						
ESDI Channel Error	ID		Status	$1A_H$		Bit Count				
ESDI ID Flag Mismatch	ID		Actual Flag	$1B_H$	Track			Head		Sector
Data Not Corrected	ID			$1D_H$						
Drive Deselect Fault	ID		Status	$1E_H$						

09480A 1-31

Byte D	Byte H	
0	0	Next IOPB P. <7:07>
1	1	Next IOPB P. <15:1>
2	2	Next IOPB P. <23:16>
3	3	Next IOPB P. <31:24>
4	4	ID <7:0>
5	5	ID <15:8>
6	6	Option
7	7	Command Code (1)
8	8	Byte 8
9	9	Byte 9
10	A	Byte 10
11	B	Byte 11
12	C	Byte 12
13	D	Byte 13
14	E	Byte 14
15	F	Byte 15
16	10	Byte 16
17	11	Byte 17
18	12	Byte 18
19	13	Byte 19

Word D	Word H		
0	0	Next IOPB Pointer <15:0>	
2	2	Next IOPB Pointer <31:16>	
4	4	ID	
6	6	Command Code (1)	Option
8	8	Byte 9	Byte 8
10	A	Byte 11	Byte 10
12	C	Byte 13	Byte 12
14	E	Byte 15	Byte 14
16	10	Byte 17	Byte 16
18	12	Byte 19	Byte 18

09480A 1-19

(1) see IOPB parameter table

Figure 10. IOPB Structure

TABLE 4. IOPB PARAMETERS

Command	Code	Options 7	6	5	4	3	2	1	0	Byte 9	Byte 8	Byte 11	Byte 10	Byte 13	Byte 12	Byte 15	Byte 14	Byte 17	Byte 16	Byte 19	Byte 18
Read	0C	W	SE	SSRB	0	DME	DM	*	RD	Flag	Drive	Track		Head	Sector	Data Mark	Record Count	Destination <15 • • • 0>		Destination <31 • • • 16>	
Write	0D	W	SE	SSRB	FW	DME	DM	*	RD	Flag	Drive	Track		Head	Sector	Data Mark	Record Count	Source <15 • • • 0>		Source <31 • • • 16>	
Verify	0F	W	SE	SSRB	0	DME	DM	0	RD	Flag	Drive	Track		Head	Sector	Data Mark	Record Count	Source <15 • • • 0>		Source <31 • • • 16>	
Format	07	W	SE	SSRB	0	DME	0	0	0	00	Drive	Track		Head	Pattern	Track Count		Map Pointer <15 • • • 0>		Map Pointer <31 • • • 16>	
Relocate Track	0B	W	SE	SSRB	0	0	0	0	0	00	Drive	Track		Head	00	Alternate Track		Alternate Head	00	0000	
Load Driver Para Block	00	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Source <15 • • • 0>		Source <31 • • • 16>	
Dump Drive Para Block	03	W	SE	SSRB	0	0	0	0	0	0	Drive	0000		00	00	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Read Physical Sector	0A	W	SE	SSRB	0	TV	DM	0	0	00	Drive	Track		Head	Physical Sector	Data Mark	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Read ID	09	W	SE	SSRB	0	AS	0	0	0	00	Drive	Track		Head	Physical Sector	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Load Buffer	01	W	SE	SSRB	0	DME	0	0	TB	00	Drive	0000		00	00	00	00	Source <15 • • • 0>		Source <31 • • • 16>	
Dump Buffer	02	W	SE	SSRB	0	DME	0	0	TB	00	Drive	0000		00	00	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Load Syndrome	04	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Source <15 • • • 0>		Source <31 • • • 16>	
Dump Syndrome	05	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Correct Buffer	06	W	SE	SSRB	0	LD	0	0	0	00	Drive	0000		00	00	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Seek	0E	W	SE	SSRB	0	TV	0	0	0	00	Drive	Track		Head	00	00	00	0000		0000	
Restore	08	W	SE	SSRB	0	TV	0	0	HP	00	Drive	0000		00	00	00	00	0000		0000	
ESDI Channel	10	W	SE	SSRB	0	0	0	SR	WCC	00	Drive	Command		00	00	00	00	Destination <15 • • • 0>		Destination <31 • • • 16>	
Move Data	01	W	SE	SSRB	0	DME	DM	0	TB	00	Drive	# of Set		Destination <15 • • • 0>		Destination < 31 • • • 16 >		Source <15 • • • 0>		Source < 31 • • • 16 >	

* R/WL: 0 = Normal Read/ Write
1 = Read Long/Write Long

09480A 1-20

Option Bits

One byte in each IOPB contains a set of options applicable to a particular command. Any combination of options may be set.

W — Wait

0 = Disabled: After execution of the current IOPB, the HDC continues with the next IOPB.

1 = Enabled: After execution of the current IOPB, the HDC terminates IOPB chain execution. It flags the termination by a "Wait Stop" Controller Fault (see Status/Command Register description). Seek-look-ahead operations will not be performed past any IOPB with this option bit set. A stop on this option is resumable.

SE — Stop on Error

0 = Disabled: After execution of the current IOPB, the HDC continues with the next IOPB.

1 = Enabled: The HDC stops the execution of the current IOPB chain if the current IOPB terminates with a fatal error (e.g., Fatal Seek Error, Record Not Found, or Drive Selection Fault). A stop on this option is not resumable.

SSRB — Stop on Status Result Block

0 = Disabled: After execution of the current IOPB, the HDC continues with the next IOPB.

1 = Enabled: The HDC stops the execution of the current IOPB chain if the current IOPB causes a Status Result Block (of any kind) to be written. SSRB is a superset of SE. This means the HDC will also stop for all cases that it would stop for if SE were set. So, the stop is only resumable if the SRB was caused by a non-fatal error. The HDC terminates the command chain immediately after issuing the SRB (this may be in the middle of executing the current IOPB).

DME — Data Map Enable

0 = Data Mapping Disabled: The Source/Destination Pointer links directly to the data block in system memory. This block is addressed in a linear manner.

1 = Data Mapping Enabled: The Source/Destination Pointer links to the first Data Map Entry. The data block is pointed to by the pointer contained in the Data Map Entry. The data may be stored in non-contiguous memory.

DM — Data Mark

0 = Disabled: The HDC uses the default data mark, which is F8H for Hard-Disk Mode and FBH for Floppy-Disk Mode. The FORMAT command writes the default data mark. The HDC cannot ignore data marks.

1 = Enabled: Any type of Data Mark may be used. The Data Mark is specified in the data mark field of the IOPB. This function is available only for normal disk I/O commands (read, write, and verify) and Read Physical Sector.

TV — Track Verify

0 = Disabled: The HDC does not attempt to read a sector ID field to verify whether the heads are positioned correctly.

1 = Enabled: The HDC attempts to read a sector ID field to verify that the heads are positioned correctly. If it detects that the heads are mis-positioned, it issues a Seek Error SRB. However, it does not restore and re-seek the heads automatically. The normal disk I/O commands perform an implied Track Verify. These commands always verify the track before any read or write access to the drive is attempted.

TB — Toggle Buffer

0 = Disabled

1 = The HDC toggles to the other sector buffer after the current sector buffer has been completely loaded or dumped.

RD — Relocate Disabled

0 = Bit is reset and the Auto Relocate Bit in the Drive Parameter Block is set, the HDC will automatically handle relocated tracks.

1 = Bit is set, auto-relocating is switched off. Therefore, the HDC does not check for a relocated track when starting to read or write. This feature allows higher performance by decreasing the sector skew at the beginning of each track to One.

FW — Floppy Wait

0 = Floppy Wait Disabled

1 = After writing the last physical sector to a track, the HDC waits for 1 ms before it attempts any seek operations.

AS — Arbitrary Sector

0 = Disabled

1 = Enabled (see Read ID command description)

LD — Locator Dump

0 = Disabled

1 = Enabled (see Correct Buffer command description)

HP — Head Park

0 = The Am9590 will try to restore the heads, starting at the current track.

1 = The Am9590 will step in five tracks before attempting to restore. Therefore, even if the heads are parked at a track number lower than 0, the RESTORE command will work properly. The method to move the head to the park position is drive-dependent.

9590 Only

WCC — Wait for COMMAND COMPLETE

0 = When sending an ESDI command (ESDI channel IOPB) to the drive, the HDC will not wait for COMMAND COMPLETE to go active before executing the next command.

1 = The Am9590 will wait for COMMAND COMPLETE after sending an ESDI command (ESDI channel IOPB) before it executes the next IOPB.

SR — Status Returned

0 = If an ESDI command is being sent with this bit reset, the HDC will not expect status information to be returned by the disk drive.

1 = The Am9590 will wait for status information to be returned by the disk drive. The status information will be transferred into the memory location indicated by the Destination Pointer of the IOPB.

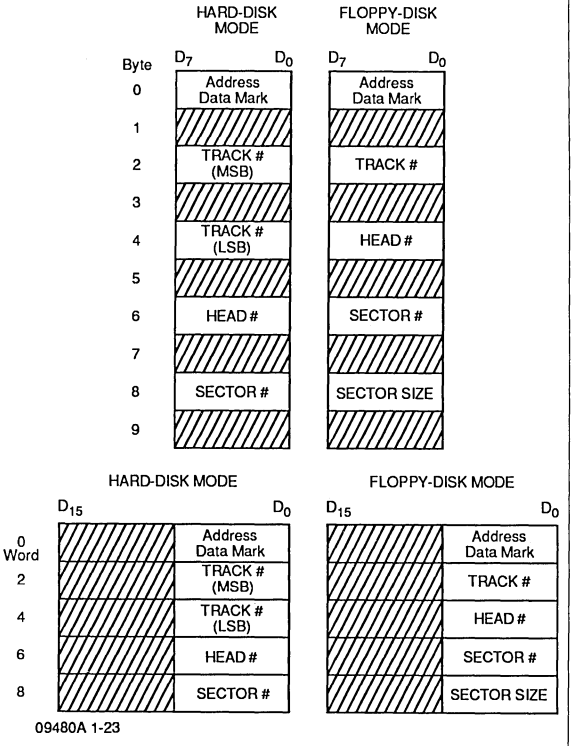


Figure 11. Sector ID Dumped by the Read ID Command

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... – 65 to + 150°C
Supply Voltage
with Respect to Ground ..... – 0.5 to + 7.0 V
Voltage on Any Pin
with Respect to Ground ..... – 0.5 to + 7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to + 70°C
Supply Voltage (V_{CC}) ..... + 4.75 to + 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		– 0.5*	0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = – 250 µA	2.4		V
I_I	Input Leakage Current	$V_{SS} + 0.4 \leq V_I \leq V_{CC}$		±10	µA
I_O	Output Leakage Current	$V_{SS} + 0.4 \leq V_O \leq V_{CC}$		±10	µA
I_{CC}	Supply Current	T_A = 0°C, V_{CC} = 5.25 V		500	mA
C_{IN}	Input Capacitance	Unmeasured Pins Returned to Ground f = 1 MHz		20*	pF
C_{OUT}	Output Capacitance			20*	pF
$C_{I/O}$	Bidirectional Capacitance			20*	pF

*Not tested.

SWITCHING CHARACTERISTICS over operating range

No.	Parameter Symbol	Parameter Description		Min.	Max.	Unit
1	t_{CPH}	System Clock HIGH Time		38		ns
2	t_{CPL}	System Clock LOW Time		38		ns
3	t_{CPC}	System Clock Cycle Time		100	500	ns
6	t_{DCPH}	Disk Clock HIGH Time	15 MHz	28		ns
			10 MHz	38		
7	t_{DCPL}	Disk Clock LOW Time	15 MHz	28		ns
			10 MHz	38		
8	t_{DCPC}	Disk Clock Cycle Time	15 MHz	63	10,000 (Note 1)	ns
			10 MHz	100	10,000 (Note 1)	
21	t_{DRGA}	RD/REFCLK to RG Active			50	ns
22	t_{DRGI}	RD/REFCLK to RG Inactive			50	ns
23	t_{RGDW}	RG Dwell		8 t_{DCPC} (Note 2)		ns
24	t_{AMCRG}	RG to AMC		8 t_{DCPC} (Note 2)		ns
25	t_{DAMCA}	RD/REFCLK to AMC Active			50	ns
26	t_{DAMCI}	RD/REFCLK to AMC Inactive			50	ns
27	t_{AMCAMF}	AMC Active to AMF Active		4 t_{DCPC} (Note 2)		ns
28	t_{SUAMF}	AMF Setup to RD/REFCLK		30		ns
29	$t_{DAMCAMF}$	AMC Inactive to AMF Inactive			16 t_{DCPC} (Note 2)	ns
30	t_{DATSCC}	Data Setup to RD/REFCLK (Note 3)	15 MHz	50		ns
			10 MHz	60		
31	t_{DATHD}	Data Hold to RD/REFCLK		0		ns
32	t_{SUFAM}	$FAM_{0,1}$ Setup to AMC Active		30		ns
33	t_{HDFAM}	$FAM_{0,1}$ Hold to RD/REFCLK		0		ns
36	t_{AMCDW}	AMC Dwell		8 t_{DCPC} (Note 2)		ns
40	t_{DWG}	RD/REFCLK to WG Active			50	ns
41	t_{WGDW}	WG Dwell		8 t_{DCPC} (Note 2)		ns

SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
42	t_{DWGAMC}	WG Active to AMC Active	40 t_{DCPC} (Note 2)		ns
44	t_{HDDW}	RD/REFCLK to WRDAT Delay		50	ns
45	t_{SUFAM}	$FAM_{0,1}$ Setup to AMC	8 t_{DCPC} (Note 2)		ns
46	t_{HDFAM}	$FAM_{0,1}$ Hold to RD/REFCLK	0		ns
47	t_{INDWG}	Index to WG/RG	13 t_{DCPC} (Note 2)		ns
48	t_{AMC}	AMC Active	24 t_{DCPC} (Note 2)		ns
49	t_{REFWG}	RD/REFCLK to WG Inactive		50	ns
55	t_{DECC}	RD/REFCLK to $ECC_{0,1}$	0	50	ns
57	t_{ERRSV}	ECCERR Setup to Last RD/REFCLK (In Post 2)	8 t_{DCPC} (Note 2)		ns
58	t_{ERRHD}	ECCERR Hold to Last RD/REFCLK (In Post 2)	0		ns
60	t_{DRSU}	$DRSEL_{0,1}$ Setup to $\overline{SELEN}$ Active	5 t_{CPC} (Note 2)		ns
61	t_{PCSU}	PCEN Setup to $\overline{SELEN}$ Active	5 t_{CPC} (Note 2)		ns
62	$t_{SELDRDY}$	$\overline{SELEN}$ Active to $\overline{DREADY}$ Active		12.8	ms
63	t_{FLTSU}	Fault to $\overline{DREADY}$ Setup	0		ns
64	t_{WPSU}	WRITEPROT to $\overline{DREADY}$ Setup	0		ns
65	t_{DSHD}	$\overline{SELEN}$ Inactive to $DRSEL_{0,1}$	5 t_{CPC} (Note 2)		ns
66	t_{DRDYHD}	$\overline{SELEN}$ Inactive to $\overline{DREADY}$ Hold	0		ns
67	t_{FLTHD}	$\overline{SELEN}$ Inactive FAULT Hold	0		ns
68	t_{WPHD}	$\overline{SELEN}$ Inactive to WRPROT Hold	0		ns
69	t_{PCHD}	PCEN Hold	5 t_{CPC} (Note 2)		ns
75	t_{DIRSU}	DIRIN Setup	5 t_{CPC} (Note 2)		ns
76	t_{STPWD}	STEP HIGH Width	User Programmable		ns
77	t_{STLW}	STEP LOW Width	User Programmable		ns
78	t_{SKSU}	SC Setup to STEP	5 t_{CPC} (Note 2)		ns
79	t_{STPSK}	STEP LOW to SC LOW		10	ms

SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
80	t_{TRKSK}	TRK0 to SC Setup	0		ns
81	t_{SKDIRI}	SC to DIRIN Inactive Hold	5 t_{CPC} (Note 2)		ns
82	t_{RTZSK}	RTZ LOW to SC LOW		10	ms
84	t_{RTZWD}	RTZ Pulse Width	User Programmable		ns
85	t_{SELSKI}	$\overline{SELEN}$ Invalid to SC Invalid	0		ns
86	$t_{SELTRKI}$	$\overline{SELEN}$ Invalid to TRK0 Invalid	0		ns
100	t_{HHRW}	$\overline{BHE}$ to $\overline{RD}$, $\overline{WR}$ Hold	0		ns
101	t_{HADD}	Address Hold	0		ns
102	t_{HCS}	$\overline{CS}$ Hold Time	0		ns
103	t_{TSUADD}	Address Setup	0		ns
104	t_{NRDY}	$\overline{READY}$ Negate Time		50	ns
105	t_{CSRD}	$\overline{CS}$, $\overline{BHE}$ to $\overline{RD}$ Setup	0		ns
106	t_{RRDY}	$\overline{READY}$ Response Time	2 t_{CPC} (Note 2)	16 t_{CPC} (Note 2)	ns
107	t_{HSTB}	Strobe Hold	0		ns
108	t_{RRCV}	$\overline{READY}$ Recover	t_{CPC} + 10		ns
109	t_{DATON}	Data Turn On	t_{CPC} (Note 2)	15 t_{CPC} (Note 2)	ns
110	t_{SUDAT}	Data Setup	t_{CPC} – 50		ns
111	t_{DATOFF}	Data Turn Off		60	ns
112	t_{CSWR}	$\overline{CS}$, $\overline{BHE}$ to $\overline{WR}$ Setup	0		ns
114	t_{WRCV}	Write Recovery	t_{CPC} + 10		ns
115	t_{SUDATW}	Data Write Setup	40		ns
116	t_{HDDATW}	Data Write Hold	0		ns
117	t_{CLDV}	Clock to Data Valid		50	ns
118	t_{DCLRD}	Clock to $\overline{READY}$ LOW		70	ns
120	t_{DALE}	CLK to ALE Active		50	ns
121	t_{WALE}	ALE Pulse Width	t_{CPH} – 10		ns
122	t_{ADDHD}	AD_{0-15} Hold Time	t_{CPL} – 20		ns
123	t_{DADD}	CLK to AD_{0-15} Valid		50	ns
124	t_{SUADD}	AD_{0-15} Setup	t_{CPH} – 20		ns

SWITCHING CHARACTERISTICS (Cont'd.)

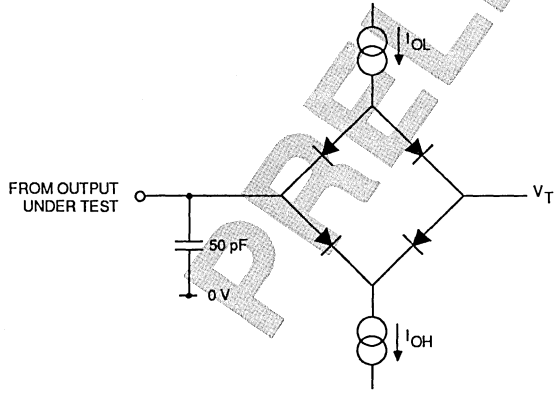
No.	Parameter Symbol	Parameter Description		Min.	Max.	Unit
125	t_{IADD}	CLK to AD_{0-15} Invalid			60	ns
126	t_{DRD}	CLK to $\overline{RD}$ Active			50	ns
127	t_{VCNTL}	CLK to $\overline{BHE}$, DT/$\overline{R}$ Valid			60	ns
128	t_{DDEN}	CLK to $\overline{DEN}$ Active			60	ns
129	t_{IDEN}	CLK to $\overline{DEN}$ Negate	Read Cycle	10	60	ns
			Write Cycle	—		
130	t_{SUDAT}	Data In Setup		20		ns
131	t_{HDDAT}	Data In Hold		10		ns
132	t_{IRD}	CLK to $\overline{RD}$ Negate		10	60	ns
133	t_{ICNTL}	$\overline{BHE}$, DT/$\overline{R}$ Negate (if changing)			60	ns
134	t_{SURBY}	$\overline{READY}$ Setup (Sync)		15		ns
135	t_{HDRDY}	$\overline{READY}$ Hold (Sync)		12		ns
136	t_{IDO}	Data Out Invalid			100	ns
137	t_{SUDT}	Data Out Setup		$t_{CPH} - 20$		ns
138	t_{DWR}	CLK to $\overline{WR}$ Active			50	ns
139	t_{HDWR}	CLK to $\overline{WR}$ Inactive			60	ns
140	t_{ARSU}	$\overline{READY}$ Setup to CLK LOW (Async)		15		ns
141	t_{ARHD}	$\overline{READY}$ Hold to CLK LOW (Async)		12		ns
150	t_{DBR}	CLK to BREQ Active			70	ns
151	t_{DBA}	BACK to CLK Setup**		20		ns
152	t_{DDTR}	CLK to DT/$\overline{R}$ Valid			100	ns
153	t_{DCNTL}	CLK to $\overline{BHE}$, $\overline{RD}$ and $\overline{DEN}$			100	ns
154	t_{DWR}	CLK to $\overline{WR}$ Valid			100	ns
155	t_{IBREQ}	CLK to BREQ Inactive			70	ns
156	t_{IDTR}	CLK to DT/$\overline{R}$ Invalid			70	ns
157	t_{ICNTL}	CLK to $\overline{BHE}$, $\overline{RD}$ and $\overline{DEN}$ Invalid			70	ns
158	t_{IWR}	CLK to $\overline{WR}$ Invalid			70	ns
159	t_{SBA}	BACK to CLK Setup**		20		ns
166	t_{HBA}	CLK to BACK Hold**		20		ns
160	t_{DALEN}	CLK to ALEN Active			50	ns
161	t_{WALEN}	ALEN Pulse Width		$t_{CPH} - 10$		ns

SWITCHING CHARACTERISTICS (Cont'd.)

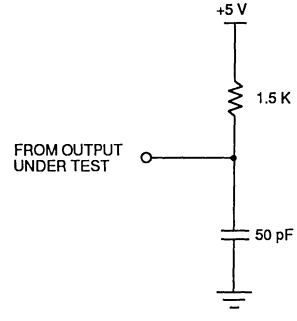
No.	Parameter Symbol	Parameter Description		Min.	Max.	Unit
162	t_{DADDH}	AD_{0-15} Hold Time		$t_{CPL} - 20$		ns
163	t_{DADD}	CLK to AD_{0-15} Valid			60	ns
164	t_{SUADD}	AD_{0-15} Setup Time		$t_{CPH} - 20$		ns
165	t_{IADD}	CLK to AD_{0-15} Invalid			100	ns
167	t_{SRES}	RESET to CLK Setup**		20		ns
168	t_{HRES}	CLK to RESET Hold**		20		ns
169	t_{ICNTBR}	Control Inactive to BREQ Inactive		0		ns
170	t_{IADBR}	AD_{0-15} to BREQ Inactive		0		ns
50	t_S	WRDAT Setup to WRCLK Rising Edge	10 MHz	30		ns
			15 MHz	20		
51	t_H	WRDAT Hold from WRCLK Rising Edge	10 MHz	30		ns
			15 MHz	20		

* Not tested.
** For test reference only.
Notes: 1. Can be static if no drive selected.
2. Nominal times may vary due to propagation delay from clock edge.
3. RD/REFCLK from drive should be inverted to meet this parameter.

SWITCHING TEST CIRCUITS



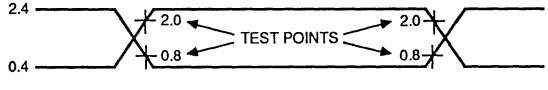
A. Standard Test Load



B. Open-Drain Test Load

09853A-21

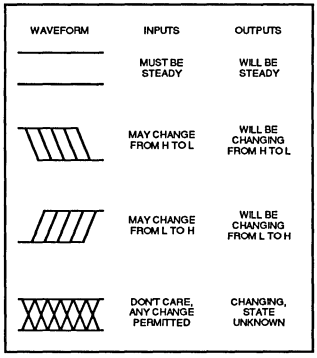
SWITCHING TEST WAVEFORM



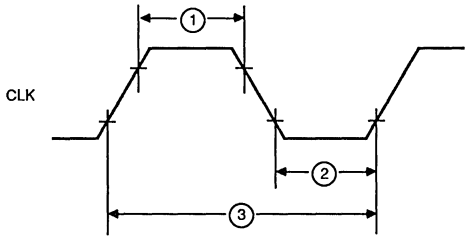
09853A-22

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

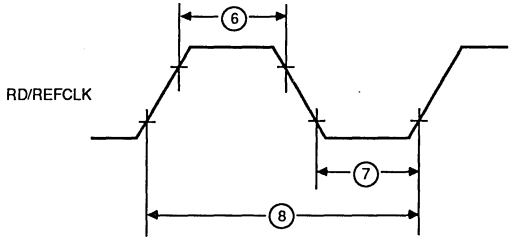


KS000010



09853A-1

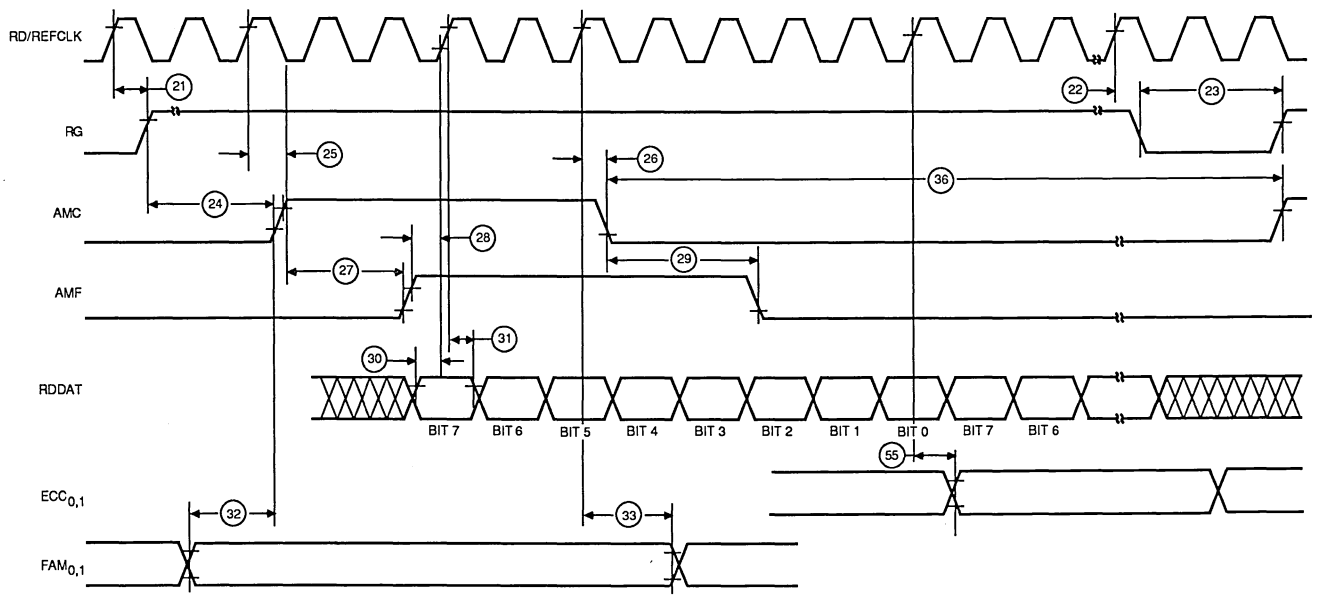
Clock Timing



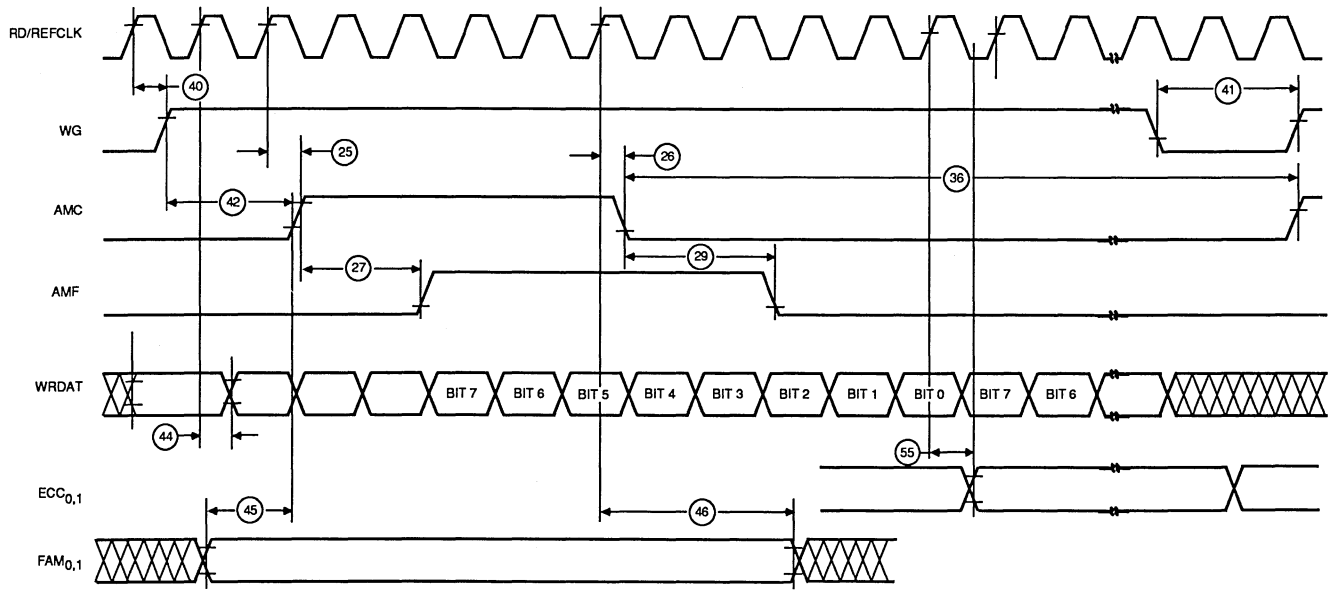
09853A-2

RD/REFCLK Timing

SWITCHING WAVEFORMS (Cont'd.)

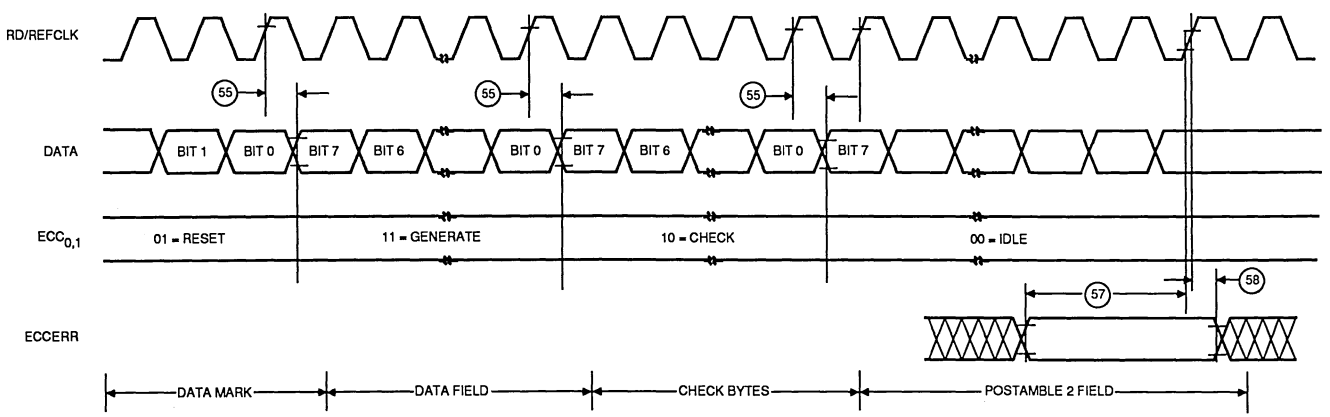


Disk Data Read Timing



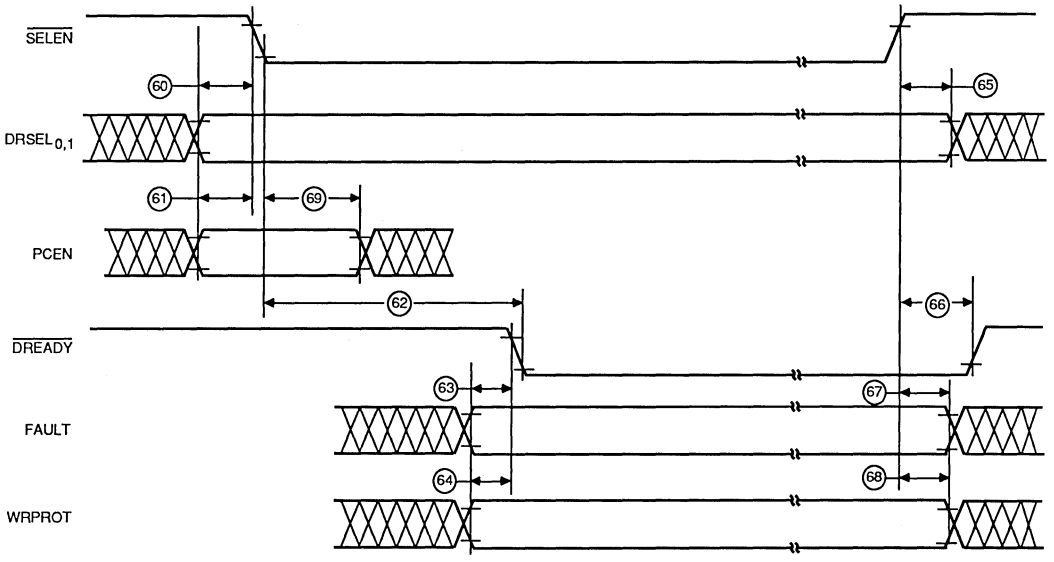
Disk Data Write Timing

SWITCHING WAVEFORMS (Cont'd.)



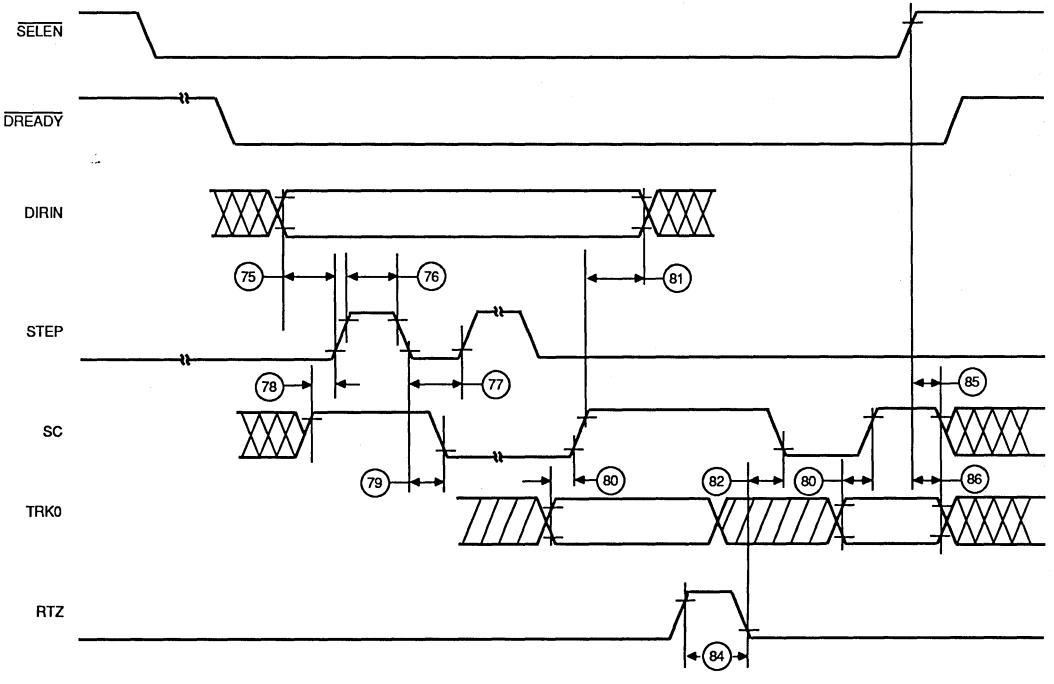
External ECC Interface Timing

SWITCHING WAVEFORMS (Cont'd.)



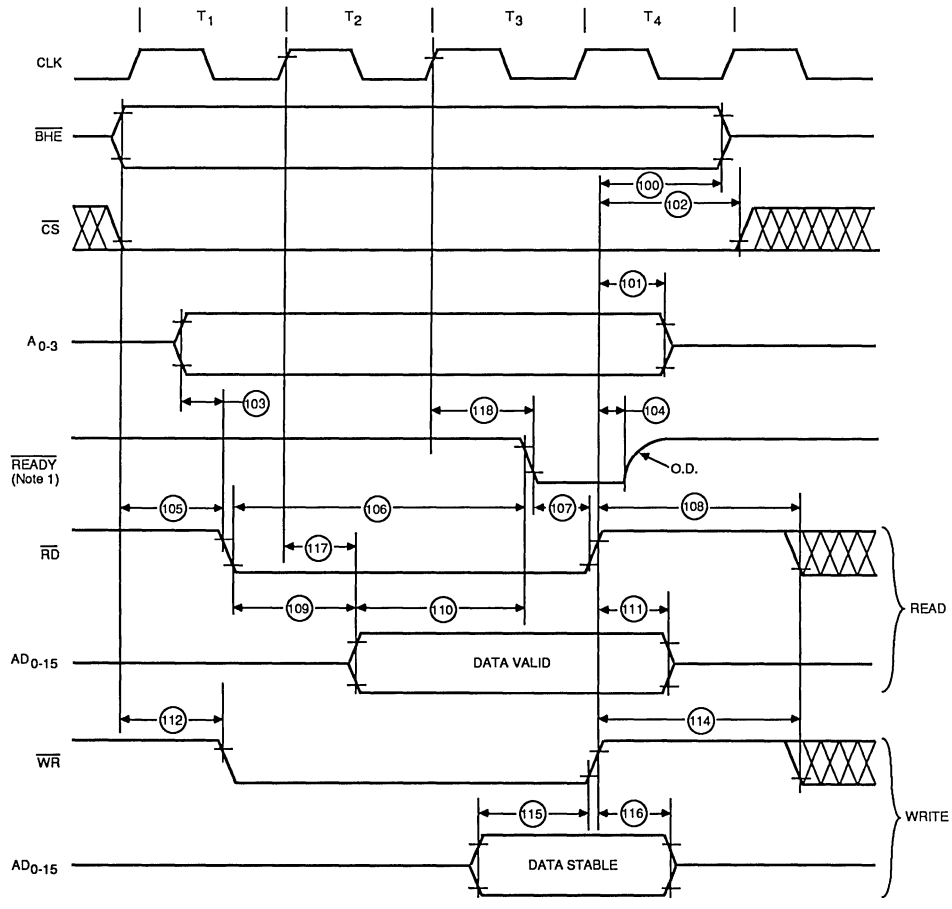
Disk Interface Timing 1

09853A-6



09853A-7

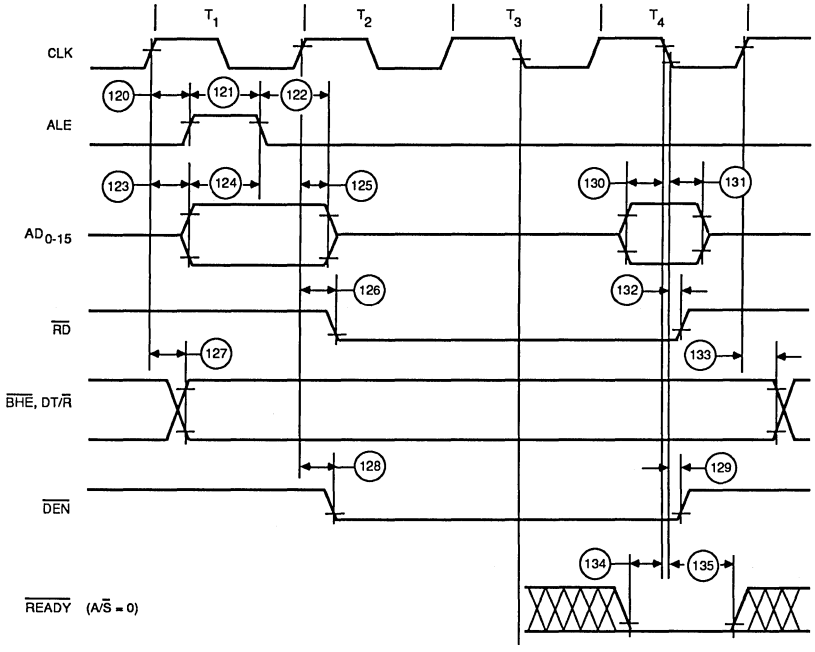
Disk Interface Timing 2



Note 1: READY pin open-drain output pulled HIGH by external load.

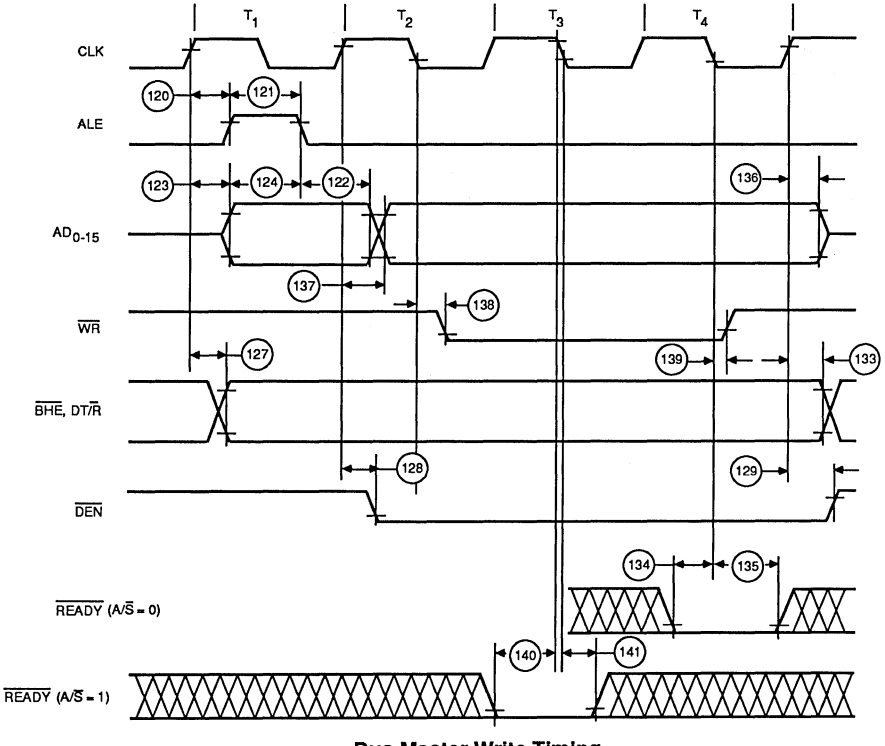
Bus Slave/Read/Write Timing

SWITCHING WAVEFORMS (Cont'd.)



09853A-9

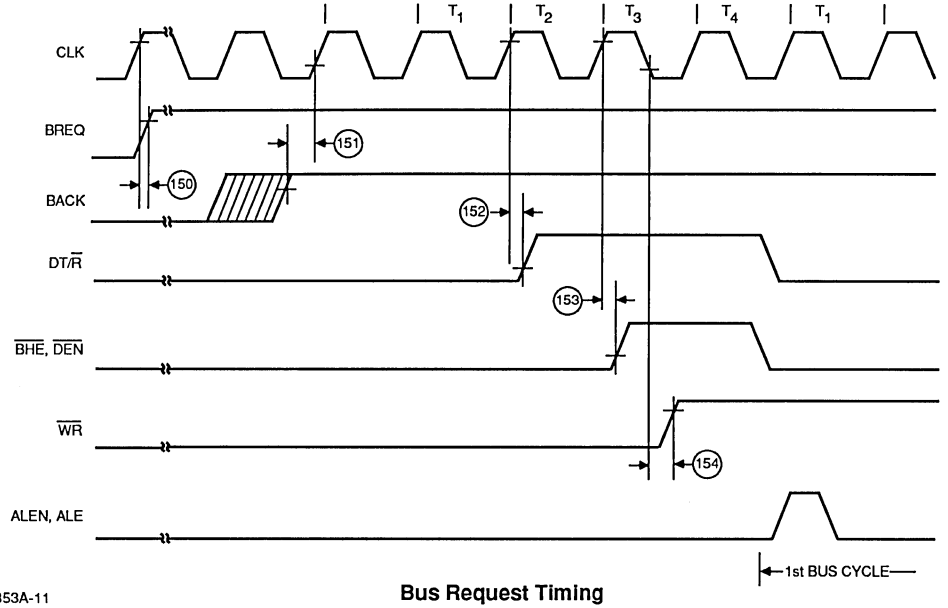
Bus Master Read Timing



09853A-10

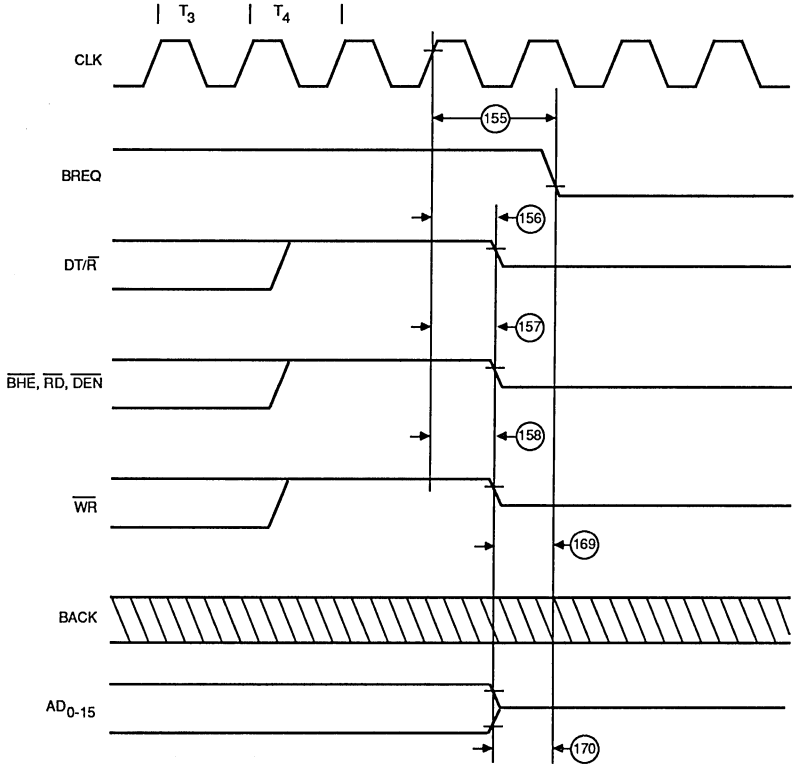
Bus Master Write Timing

SWITCHING WAVEFORMS (Cont'd.)



09853A-11

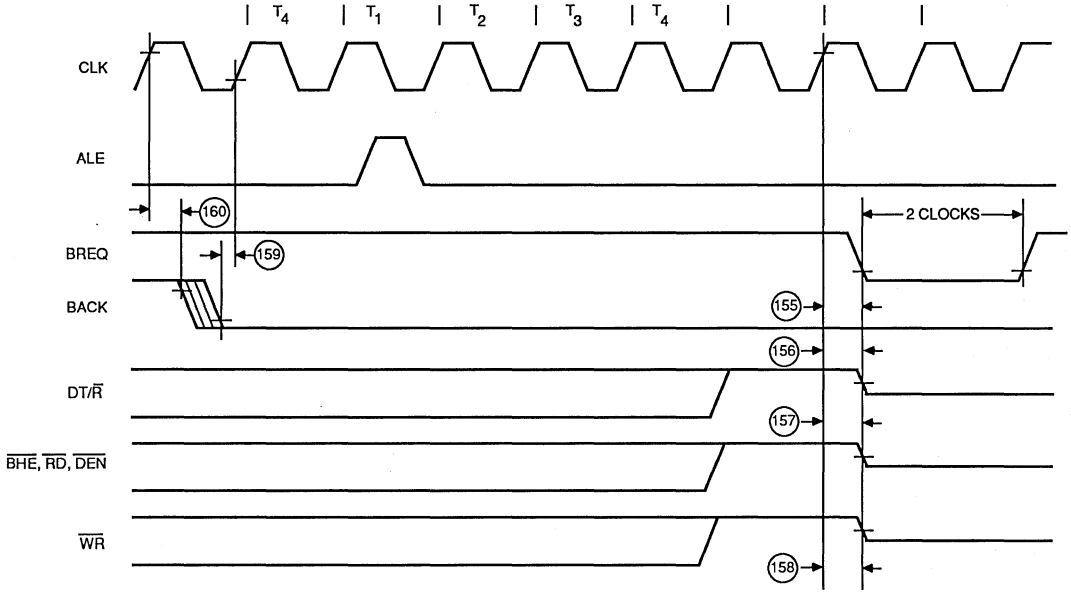
Bus Request Timing



09853A-12

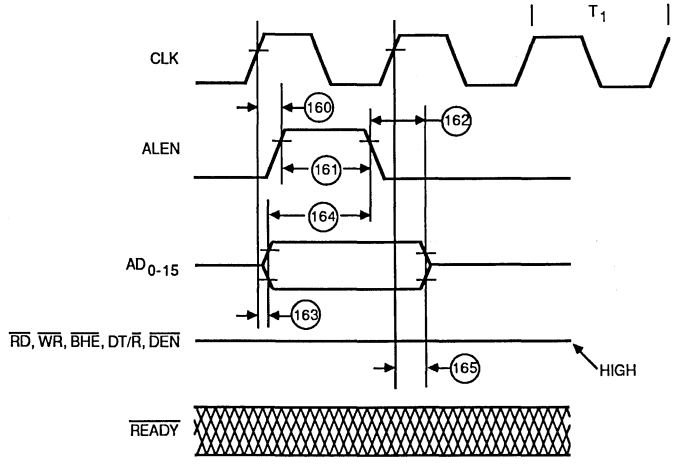
Bus Release Timing

SWITCHING WAVEFORMS (Cont'd.)



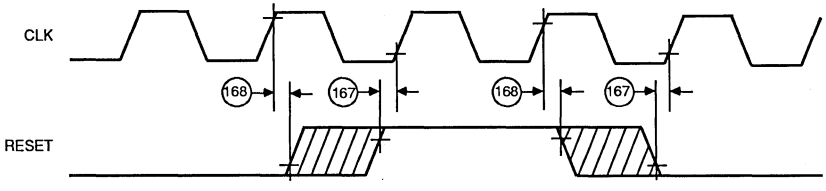
Pre-Emptive Bus Release Timing

09853A-13



09853A-14

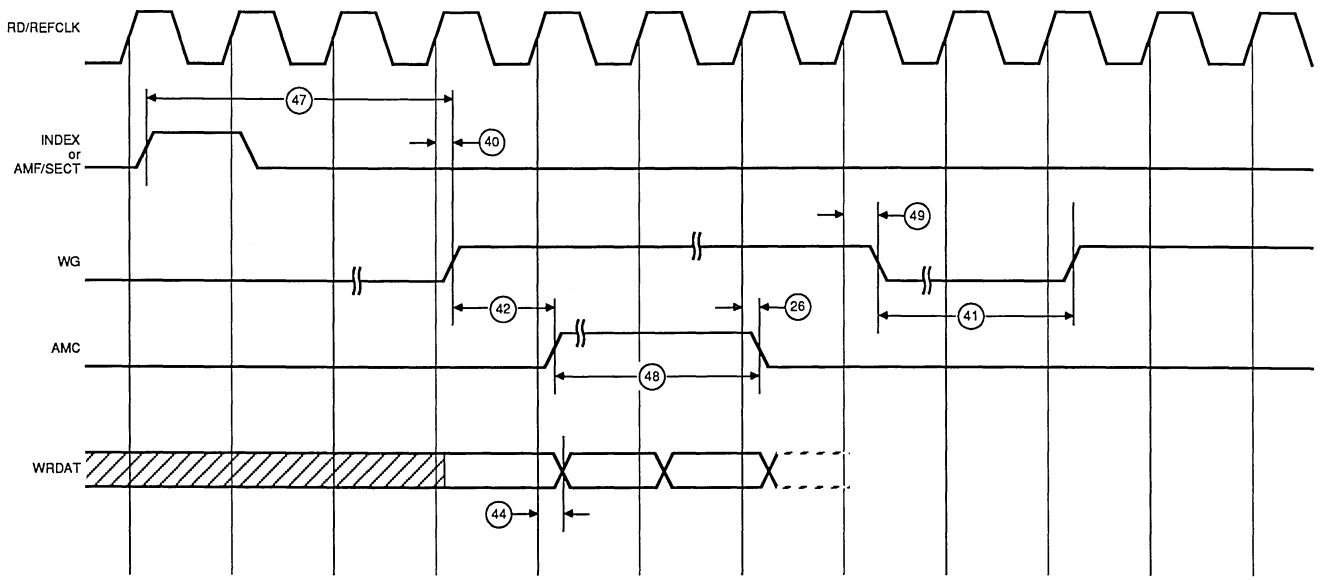
Upper Address Latch Timing



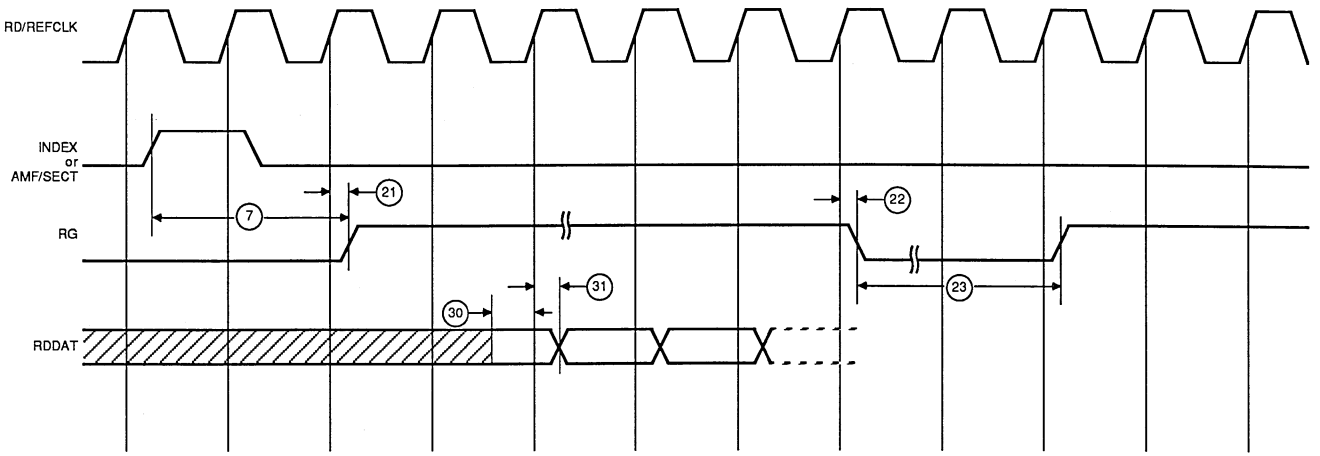
09853A-15

RESET Timing

SWITCHING WAVEFORMS (Cont'd.)

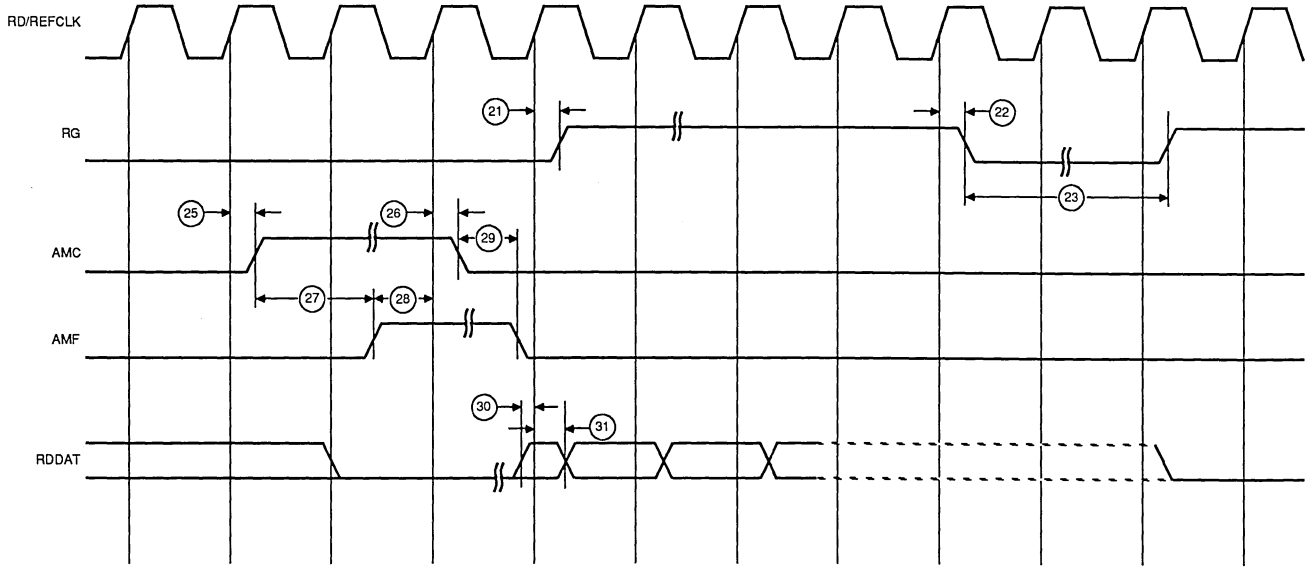


ESDI Soft-Sectored Format Timing



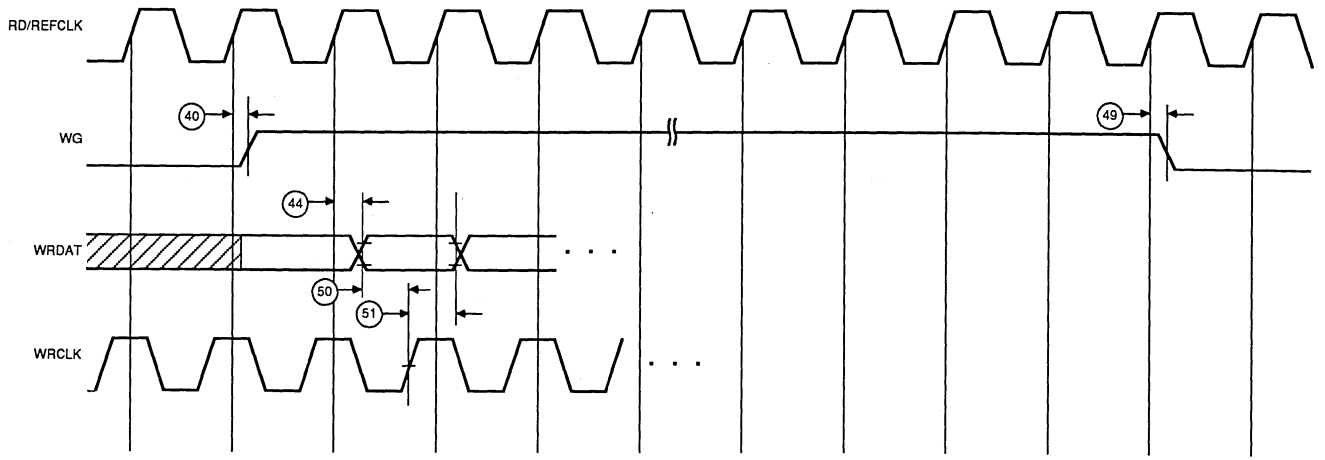
ESDI Hard-Sectored Read Timing

SWITCHING WAVEFORMS (Cont'd.)



ESDI Soft-Sectored Read Timing

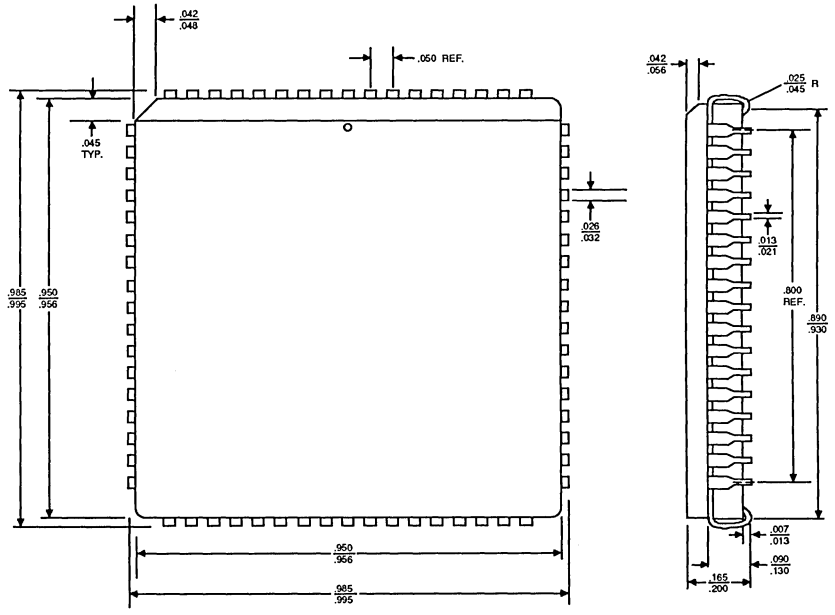
SWITCHING WAVEFORMS (Cont'd.)



ESDI Write Timing

PHYSICAL DIMENSIONS*

PL 068

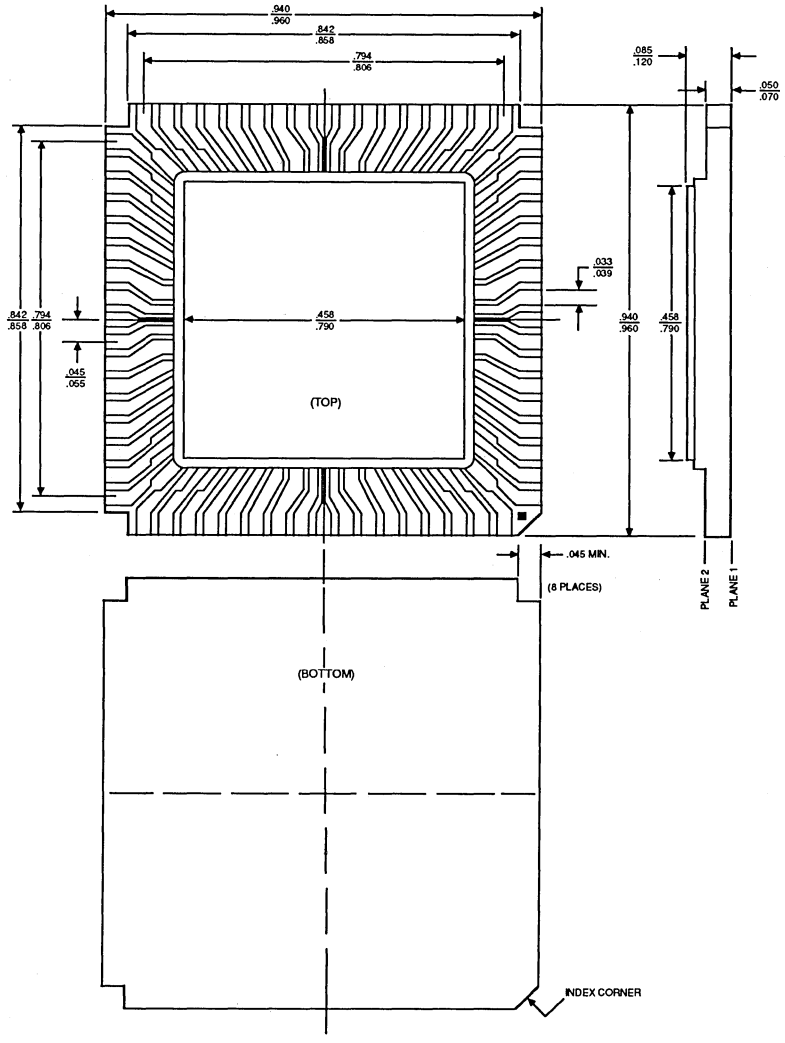


* For reference only.

PID # 067531

PHYSICAL DIMENSIONS (Cont'd.)

CA2068



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