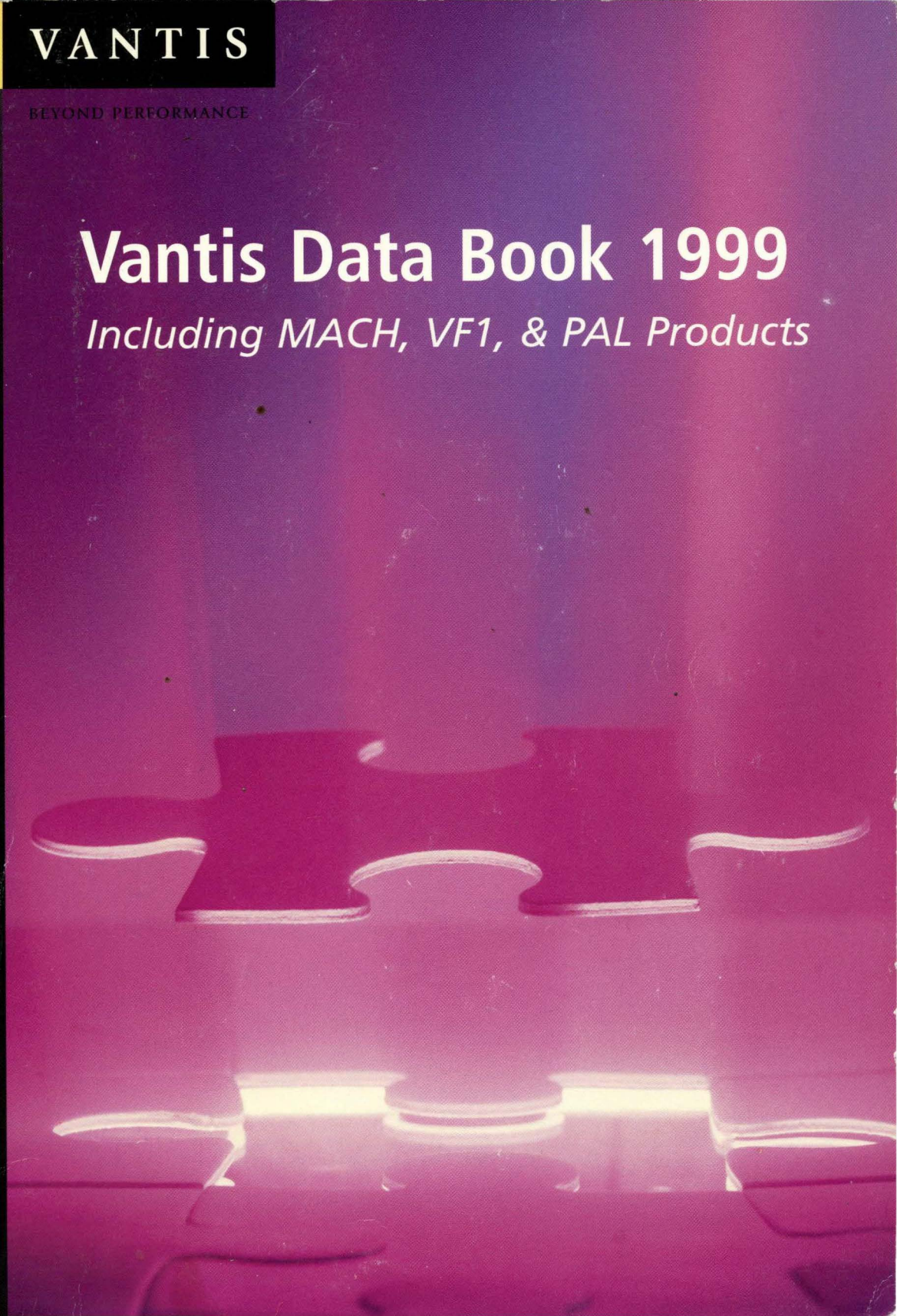
VANTIS

BEYOND PERFORMANCE

Vantis Data Book 1999

Including MACH, VF1, & PAL Products



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Including CPLD, FPGA, & PAL Products

BEYOND PERFORMANCE

Vantis Data Book 1999

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Welcome to Vantis! We are proud to introduce our new 1999 Data Book. It's not just MACH® anymore! Now featuring our entire line of programmable logic products, this is our most comprehensive and easy-to-use data book to date.

Vantis brings unmatched emphasis and depth to the industry with our high-density MACH (Macro Array CMOS High Density) CPLD family, our newly-announced FPGA (field programmable gate array) family, VF1™, as well as our SPLD product, the PAL®. In addition, our current software offerings have been expanded to include the DesignDirect™ tool suite, establishing software as a much stronger part of the Vantis solution.

Vantis' MACH 4 and MACH 5 families represent the most comprehensive CPLD offering in the industry. Currently the leader in 3.3-Volt offerings, the MACH family has recently been expanded with the MACH 4A and MACH 5A product lines offering even greater density solutions while still maintaining the exceptional performance MACH devices are known for.

The VF1 family marks Vantis' entry into the FPGA market. These new devices are designed to effectively double system performance by providing 50-100 percent faster system speed than any other FPGA vendor.

Innovation and dedicated focus are at the heart of everything we do here at Vantis. From the development of ground-breaking architectures and advanced process technologies to our industry-renown customer service. At Vantis, programmable logic performance is not measured in nanoseconds alone. By combining software performance with proven quality and reliability and the best on-time-delivery in the business, Vantis is committed to taking our customers Beyond Performance.

Cheers,

Andy Robin

Vice President of Marketing

Contents

Vantis Overview

VANTIS
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Introduction

Formed in 1996, Vantis is an AMD company that exists solely to better serve the specialized requirements of programmable logic customers. Vantis brings expertise to the industry from almost two decades of innovation and excellence as one of the top PLD suppliers.

TOTAL PROGRAMMABLE LOGIC LEADERSHIP

Today's leading-edge electronic systems require programmable logic devices (PLDs) to provide a variety of benefits including quick time-to-market and design flexibility. Vantis is one of the only PLD suppliers that offers a complete portfolio of programmable logic solutions: SPLDs (Simple PLDs), CPLDs (Complex PLDs) and FPGAs (Field Programmable Gate Arrays). This complete portfolio ensures the optimal solution for each system need. In addition, Vantis PLDs are recognized as the industry's highest performance devices.

Vantis is more than just the speed performance leader. Vantis ships more PLD components than any other supplier. Becoming the PLD volume leader required paying close attention to our customers' needs. These needs include accelerating system performance, simplifying PLD integration and delivering results with outstanding product quality that exceed our customers' expectations. At Vantis, we refer to this total product commitment as "Beyond Performance".

Accelerating System Performance

As the PLD performance leader, Vantis strives to enhance every aspect of our products to provide superior benefits to the designer. There are three basic components that affect performance in PLD devices: process technology, architecture and circuit design techniques. Vantis excels in all three.

Process Technology: Vantis utilizes leading-edge process technologies to drive system performance. In addition, Vantis has an experienced process technologies group that specializes in defining next-generation processes and improving existing processes. These technical experts also work closely with Vantis circuit designers to exploit process features to the fullest for superior speed performance while optimizing for other important device attributes such as low-power operation and 5-Volt tolerant I/Os in 2.5-Volt processes.

Architecture Design: The basic device concept, or architecture, can greatly affect how fast the PLD device will run. Vantis has proven its performance leadership by designing and shipping faster programmable logic solutions. The original 22V10 architecture, the MACH® CPLD architectures and the innovative VF1™ FPGA architecture are examples of high-performance architecture leadership. All were specified and designed to provide better performing solutions. For example, the MACH products are SpeedLocked™ to ensure guaranteed timing regardless of usage, a capability that no other supplier offers. And, VF1 FPGAs offer a unique Variable-Grain-Architecture™ that adapts to the designer's logic to achieve faster performance.

Circuit Design: Circuit design affects every aspect of PLD performance. Special attention is paid to minimize data setup time and clock-to-output time, resulting in faster external system bus speeds. Analog phase-locked-loops are designed to offer clock multiplication, doubling and tripling internal frequencies. On-chip drivers are scaled for optimal interconnect performance

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improving overall chip speed. In addition, logic and memory blocks are carefully planned to yield maximum speed and versatility. All of these are accomplished while minimizing power dissipation and with minimal silicon overhead.

The focus Vantis places on PLD performance in process, architecture and circuit design translates into accelerated system speeds and shorter design cycles for the customer. Vantis is the PLD performance leader.

Simplifying System Integration

The time-to-market advantage of PLD technology allows system designers to complete the design of programmable logic devices long after many other components on the printed circuit board (PCB) have been finalized. This implies that the PLD must seamlessly integrate into a pre-defined system environment. System integration issues may include power dissipation limitations, In-System Programming (ISP) requirements and I/O interoperability. Vantis believes that simplifying system integration is key to the success of Vantis and our customers.

To enable fast and easy integration into leading-edge electronic systems, Vantis provides 3.3-Volt safe 5-Volt devices, 5-Volt tolerant 3.3-Volt devices and a roadmap to 2.5-Volt operation. PCI compliance, hot-socketing, programmable slew rate, and programmable Bus-Friendly™ or pull-up operation are additional Vantis capabilities that aid in system integration. Power management capabilities allow the users of Vantis devices to trade speed in non-critical portions of their designs for lower power consumption. This feature, combined with the industry's most robust offering of 3.3-Volt devices, allows users to reduce their overall power consumption. Testability and programming are supported through the use of industry-standard JTAG interfacing. The use of the JTAG industry standard, not universal among PLD suppliers, further simplifies the integration of Vantis PLDs into the customer's overall system. Also, the availability of industrial and commercial temperature range devices allows designers to use these capabilities over a wide range of operating conditions. Most importantly, Vantis PLDs simplify system integration *without* compromising speed.

Delivering Results

Programmable logic's key value proposition to electronic system designers is time-to-market. Yet time-to-market is often achieved at the expense of system performance. Vantis ensures that designers can quickly access the performance that they seek while exploiting the time-to-market value provided by PLDs. Vantis takes the first step in delivering this capability many months before producing the first silicon of a new product family. Device architects, software tool designers and silicon engineers work in concert to ensure that new Vantis architectures easily support capabilities such as First-Time-Fit™, Fast-Fit-Time™, pin-locking, SpeedLocking™, and greater logic flexibility. Vantis DesignDirect™ software enables system designers to easily access these features. DesignDirect software is available either as a fully-integrated tool providing all design steps from capture to device programming or as a stand-alone silicon implementation tool that interfaces seamlessly with the industry's most popular third-party design capture, synthesis and simulation tools. DesignDirect software provides a rapid design environment that facilitates design changes while delivering superior speed performance to the customer. Vantis is *committed* to delivering superior results to our customers.

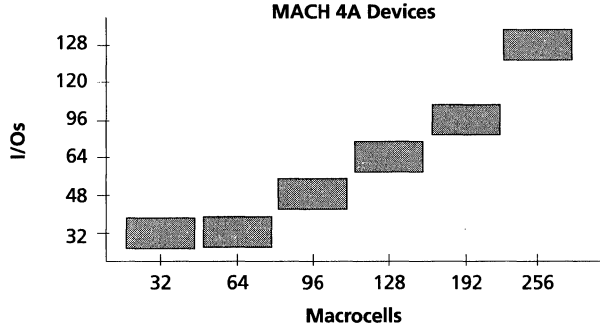
VANTIS PRODUCTS

MACH CPLDs

Addressing the need for speed in networking, telecommunications, and computing, Vantis' MACH 1, 2, 4 and 5 families offer the industry's highest performance CPLDs. Devices are available in speeds as fast as 5ns t_{PD} and in densities ranging from 32 to 512 macrocells. The MACH families are PCI-compliant and support JTAG-ISP, a critical customer requirement providing flexibility in the manufacturing environment. They also include other features such as SpeedLocking architecture for guaranteed fixed timing, Bus-Friendly inputs and I/Os, and programmable power-down modes for extra power savings.

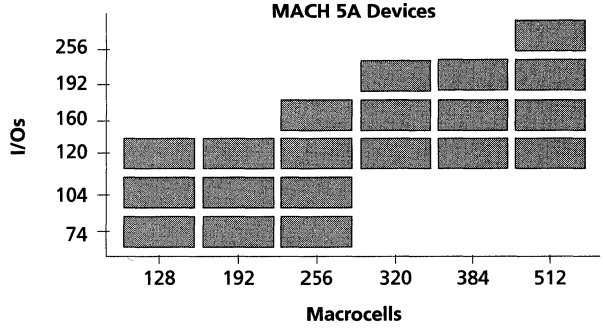
MACH 4 Family

Vantis' MACH 4 family is the most flexible CPLD solution on the market today, providing designers with high-speed, SpeedLocked solutions for both 5-Volt and 3.3-Volt applications. With the architecture of multiplexer-based central switch matrices, MACH 4 delivers First-Time-Fit, Fast-Fit-Time, and easy system integration with 100% pin-out retention after any design change and refit. Other features include synchronous and asynchronous modes available for each macrocell, and input registers for extra design flexibility.



MACH 5 Family

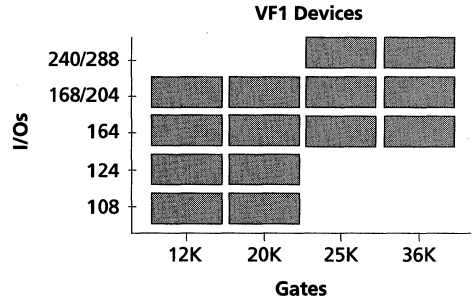
The MACH 5 family from Vantis offers high-performance CPLDs with speeds as fast as 5.5ns and densities ranging from 128 to 512 macrocells. All MACH 5 family members deliver fast fit and easy system integration with excellent pin-out retention. The MACH 5 family is the industry's fastest high-density CPLD family enabling significantly higher speeds at higher densities than ever achieved before.



VF1 FPGAs

Vantis' VF1 family is designed to provide "best in class" performance with a combined synergy of software and architecture that delivers unmatched Ease-of-Success™ to customers. Providing the industry's most cost-effective FPGA solutions for high-performance, low-power systems, products from the Vantis VF1 family are designed to provide 50 to 100 percent faster system speed than any other FPGA vendor, effectively doubling system performance.

The VF1 family is based on a proprietary innovative and synthesis-friendly Variable-Grain-Architecture design, unique Variable-Length-Interconnect™ hierarchy, and high-performance embedded memory. The VF1 architecture provides the ability to vary FPGA block configuration to adapt to a large variety of possible applications and design styles. The VF1 chip is designed with embedded, dual-port, 5-ns memory. Strategically located in vertical channels on the device, the memory provides maximum connectivity for the surrounding logic. At the core of the VF1 family architecture is Variable-Grain-Block™ (VGB™) logic. Each VGB is capable of implementing fine-grained three-input functions to coarse-grained 16-input functions, all providing extremely high performance. In addition, adjacent VGBs can be combined to create fast 32-input functions.



PAL SPLDs

As the SPLD leader, Vantis continues to provide a broad range of products including all the fundamental SPLD architectures. We offer key PAL devices in speed grades as fast as 5ns, along with low-power options, 3.3-Volt versions, industrial temperature range devices, and a wide range of packages.

Vantis Software

Vantis offers a suite of world-class software including DesignDirect software, MACHXL® software, and MACH-Synario software.

Vantis now offers internally-developed software targeted at FPGA, CPLD and SPLD devices. The DesignDirect software tool suite supports flexible top-down design methodologies optimized for high-density PLD design, thus allowing users to realize the benefits of designing in HDLs without sacrificing design performance and utilization.

MACHXL software is the design implementation software for Vantis MACH and PAL devices that allows designers to use their own third-party design tools.

MACH-Synario software is a complete development system for MACH and PAL devices, providing a highly productive, low-cost environment for the design, implementation and simulation of VHDL, ABEL-HDL, and schematic-based designs on the PC.

BEYOND PERFORMANCE

To Vantis, Beyond Performance means providing our customers with more than what the competition offers. It means providing easy-to-use, high-performance devices that will help our customers get their products to market quicker. It means allowing them to breathe easy, knowing they can get top-notch customer support, day or night. It also means easy-to-use software that allows customers to design at the push of a button, and a proven 98 percent on-time delivery rate. Vantis knows how important it is to go beyond providing our customers with just the performance they desire. Vantis is committed to helping our customers succeed in the marketplace.

That's why Vantis takes you Beyond Performance.

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Vantis Device Selector Guide

MACH® 4 FAMILY

Table 1. MACH 4 Devices[1]

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/NO speed adder)	Flip-Flops	JTAG-ISP	Commercial		Ind'l [2]				
									t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS} [3] ns	t_{CO} [4] ns	I_{CC} mA (Static)
M4(LV)-32/32-7	44PLCC, 44TQFP, 48TQFP	32 (1,250)	32	2	32	Up to 20	32	Yes	7.5	111.1	10	5.5	5.5	25
M4(LV)-32/32-10									10	95.2	12	6	6.5	
M4(LV)-32/32-12									12	76.9	14	7	8	
M4(LV)-32/32-15									15	55.6	18	10	10	
M4(LV)-64/32-7	44PLCC, 44TQFP, 48TQFP	64 (2,500)	32	2	32	Up to 20	96	Yes	7.5	111.1	10	5.5	5.5	25
M4(LV)-64/32-10									10	95.2	12	6	6.5	
M4(LV)-64/32-12									12	76.9	14	7	8	
M4(LV)-64/32-15									15	55.6	18	10	10	
M4(LV)-96/48-7	100TQFP	96 (3,750)	48	8	48	Up to 20	144	Yes	7.5	111.1	10	5.5	5.5	50
M4(LV)-96/48-10									10	95.2	12	6	6.5	
M4(LV)-96/48-12									12	76.9	14	7	8	
M4(LV)-96/48-15									15	55.6	18	10	10	
M4(LV)-128N/64-7	84PLCC	128 (5,000)	64	6	64	Up to 20	192	No	7.5	111.1	10	5.5	5.5	70
M4(LV)-128N/64-10									10	95.2	12	6	6.5	
M4(LV)-128N/64-12									12	76.9	14	7	8	
M4(LV)-128N/64-15									15	55.6	18	10	10	
M4(LV)-128/64-7	100PQFP, 100TQFP	128 (5,000)	64	6	64	Up to 20	192	Yes	7.5	111.1	10	5.5	5.5	70
M4(LV)-128/64-10									10	95.2	12	6	6.5	
M4(LV)-128/64-12									12	76.9	14	7	8	
M4(LV)-128/64-15									15	55.6	18	10	10	
M4(LV)-192/96-7	144TQFP	192 (7,500)	96	16	96	Up to 20	288	Yes	7.5	111.1	10	5.5	5.5	85
M4(LV)-192/96-10									10	95.2	12	6	6.5	
M4(LV)-192/96-12									12	76.9	14	7	8	
M4(LV)-192/96-15									15	55.6	18	10	10	
M4(LV)-256/128-7	208PQFP 256BGA	256 (10,000)	128	14	128	Up to 20	384	Yes	7.5	111.1	10	5.5	5.5	100
M4(LV)-256/128-10									10	95.2	12	6	6.5	
M4(LV)-256/128-12									12	76.9	14	7	8	
M4(LV)-256/128-15									15	55.6	18	10	10	

Notes:

1. *M4 devices reflect a new nomenclature. A brief cross reference is provided below:*

OLD OPN	NEW M4 OPN	OLD OPN	NEW M4 OPN
MACH355--->	M4-96/96	MACH446--->	M4-128/64
MACH436--->	M4-128N/64	MACH466--->	M4-256/128

2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

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Table 2. MACH 4A Devices[1]

Device	Package	Macrocells	I/Os	Dedicated inputs	Output Enables	PT per Output	Flip Flops	JTAG-ISP	Commercial		Ind'l [2]		
									t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M4A(3,5)-32/32-50	44PLCC, 44TQFP, 48TQFP	32	32	2	32	Up to 20	32	Yes	5	182	7.5	3	4
M4A(3,5)-32/32-60									6	154	10	4	4.5
M4A(3,5)-32/32-7									7.5	125	10	5.5	5
M4A(3,5)-32/32-10									10	118	12	6	5.5
M4A(3,5)-32/32-12									12	95	14	7	6.5
M4A(3,5)-64/32-50	44PLCC 44TQFP 48TQFP	64	32	2	32	Up to 20	96	Yes	5	182	7.5	3	4
M4A(3,5)-64/32-60									6	154	10	4	4.5
M4A(3,5)-64/32-7									7.5	125	10	5.5	5
M4A(3,5)-64/32-10									10	118	12	6	5.5
M4A(3,5)-64/32-12									12	95	14	7	6.5
M4A(3,5)-96/48-50	100TQFP	96	48	8	48	Up to 20	144	Yes	5	182	7.5	3	4
M4A(3,5)-96/48-60									6	154	10	4	4.5
M4A(3,5)-96/48-7									7.5	125	10	5.5	5
M4A(3,5)-96/48-10									10	118	12	6	5.5
M4A(3,5)-96/48-12									12	95	14	7	6.5
M4A(3,5)-128/64-50	100TQFP, 100PQFP	128	64	6	64	Up to 20	192	Yes	5	182	7.5	3	4
M4A(3,5)-128/64-60									6	154	10	4	4.5
M4A(3,5)-128/64-7									7.5	125	10	5.5	5
M4A(3,5)-128/64-10									10	118	12	6	5.5
M4A(3,5)-128/64-12									12	95	14	7	6.5
M4A(3,5)-192/96-50	144TQFP	192	96	16	96	Up to 20	288	Yes	5	182	7.5	3	4
M4A(3,5)-192/96-60									6	154	10	4	4.5
M4A(3,5)-192/96-7									7.5	125	10	5.5	5
M4A(3,5)-192/96-10									10	118	12	6	5.5
M4A(3,5)-192/96-12									12	95	14	7	6.5
M4A(3,5)-256/128-50	208PQFP 256BGA	256	128	14	128	Up to 20	384	Yes	5	182	7.5	3	4
M4A(3,5)-256/128-60									6	154	10	4	4.5
M4A(3,5)-256/128-7									7.5	125	10	5.5	5
M4A(3,5)-256/128-10									10	118	12	6	5.5
M4A(3,5)-256/128-12									12	95	14	7	6.5

Notes:

1. *Advance Information*
2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

MACH 5 FAMILY

Table 3. MACH 5 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]		t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns				
M5LV-128/68-5	100PQFP, 100TQFP	128 (5,000)	68	4	16	Up to 32	Yes	5.5	181.8	7.5		3	4.5	35
M5(LV)-128/68-7								7.5	125	10		4	6	
M5(LV)-128/68-10								10	100	12		5	7	
M5(LV)-128/68-12								12	83.3	15		6	8	
M5-128/68-15								15	62.5	20		8	10	
M5LV-128/74-5	100TQFP	128 (5,000)	74	4	16	Up to 32	Yes	5.5	181.8	7.5		3	4.5	35
M5LV-128/74-7								7.5	125	10		4	6	
M5LV-128/74-10								10	100	12		5	7	
M5LV-128/74-12								12	83.3	15		6	8	
M5LV-128/104-5	144PQFP, 144TQFP	128 (5,000)	104	4	16	Up to 32	Yes	5.5	181.8	7.5		3	4.5	35
M5(LV)-128/104-7								7.5	125	10		4	6	
M5(LV)-128/104-10								10	100	12		5	7	
M5(LV)-128/104-12								12	83.3	15		6	8	
M5-128/104-15								15	62.5	20		8	10	
M5LV-128/120-5	160PQFP	128 (5,000)	120	4	16	Up to 32	Yes	5.5	181.8	7.5		3	4.5	35
M5(LV)-128/120-7								7.5	125	10		4	6	
M5(LV)-128/120-10								10	100	12		5	7	
M5(LV)-128/120-12								12	83.3	15		6	8	
M5-128/120-15								15	62.5	20		8	10	
M5-192/68-7	100PQFP, 100TQFP	192 (7,500)	68	4	24	Up to 32	Yes	7.5	125	10		4	6	45
M5-192/68-10								10	100	12		5	7	
M5-192/68-12								12	83.3	15		6	8	
M5-192/68-15								15	62.5	20		8	10	
M5-192/104-7	144PQFP	192 (7,500)	104	4	24	Up to 32	Yes	7.5	125	10		4	6	45
M5-192/104-10								10	100	12		5	7	
M5-192/104-12								12	83.3	15		6	8	
M5-192/104-15								15	62.5	20		8	10	
M5-192/120-7	160PQFP	192 (7,500)	120	4	24	Up to 32	Yes	7.5	125	10		4	6	45
M5-192/120-10								10	100	12		5	7	
M5-192/120-12								12	83.3	15		6	8	
M5-192/120-15								15	62.5	20		8	10	
M5-192/160-7	208PQFP	192 (7,500)	160	4	24	Up to 32	Yes	7.5	125	10		4	6	45
M5-192/160-10								10	100	12		5	7	
M5-192/160-12								12	83.3	15		6	8	
M5-192/160-15								15	62.5	20		8	10	

Table 3. MACH 5 Devices (Continued)

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]			I_{CC} mA (Static)
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	
M5LV-256/68-5	100PQFP, 100TQFP	256 (10,000)	68	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/68-7								7.5	125	10	4	6	
M5(LV)-256/68-10								10	100	12	5	7	
M5(LV)-256/68-12								12	83.3	15	6	8	
M5-256/68-15								15	62.5	20	8	10	
M5LV-256/74-5	100TQFP	256 (10,000)	74	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5LV-256/74-7								7.5	125	10	4	6	
M5LV-256/74-10								10	100	12	5	7	
M5LV-256/74-12								12	83.3	15	6	8	
M5LV-256/104-5	144PQFP, 144TQFP	256 (10,000)	104	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/104-7								7.5	125	10	4	6	
M5(LV)-256/104-10								10	100	12	5	7	
M5(LV)-256/104-12								12	83.3	15	6	8	
M5-256/104-15								15	62.5	20	8	10	
M5LV-256/120-5	160PQFP	256 (10,000)	120	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/120-7								7.5	125	10	4	6	
M5(LV)-256/120-10								10	100	12	5	7	
M5(LV)-256/120-12								12	83.3	15	6	8	
M5-256/120-15								15	62.5	20	8	10	
M5LV-256/160-5	208PQFP	256 (10,000)	160	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5	55
M5(LV)-256/160-7								7.5	125	10	4	6	
M5(LV)-256/160-10								10	100	12	5	7	
M5(LV)-256/160-12								12	83.3	15	6	8	
M5-256/160-15								15	62.5	20	8	10	
M5(LV)-320/120-7	160PQFP	320 (12,500)	120	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/120-10								10	100	12	5	7	
M5(LV)-320/120-12								12	83.3	15	6	8	
M5(LV)-320/120-15								15	62.5	20	8	10	
M5(LV)-320/160-7	208PQFP	320 (12,500)	160	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/160-10								10	100	12	5	7	
M5(LV)-320/160-12								12	83.3	15	6	8	
M5(LV)-320/160-15								15	62.5	20	8	10	
M5(LV)-320/184-7	240PQFP	320 (12,500)	184	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/184-10								10	100	12	5	7	
M5(LV)-320/184-12								12	83.3	15	6	8	
M5(LV)-320/184-15								15	62.5	20	8	10	
M5(LV)-320/192-7	256BGA	320 (12,500)	192	4	40	Up to 32	Yes	7.5	125	10	4	6	70
M5(LV)-320/192-10								10	100	12	5	7	
M5(LV)-320/192-12								12	83.3	15	6	8	
M5(LV)-320/192-15								15	62.5	20	8	10	

Table 3. MACH 5 Devices (Continued)

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[1]			I_{CC} mA (Static)
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	
M5(LV)-384/120-7	160PQFP	384 (15,000)	120	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/120-10								10	100	12	5	7	
M5(LV)-384/120-12								12	83.3	15	6	8	
M5(LV)-384/120-15								15	62.5	20	8	10	
M5(LV)-384/160-7	208PQFP	384 (15,000)	160	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/160-10								10	100	12	5	7	
M5(LV)-384/160-12								12	83.3	15	6	8	
M5(LV)-384/160-15								15	62.5	20	8	10	
M5(LV)-384/184-7	240PQFP	384 (15,000)	184	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/184-10								10	100	12	5	7	
M5(LV)-384/184-12								12	83.3	15	6	8	
M5(LV)-384/184-15								15	62.5	20	8	10	
M5(LV)-384/192-7	256BGA	384 (15,000)	192	4	48	Up to 32	Yes	7.5	125	10	4	6	75
M5(LV)-384/192-10								10	100	12	5	7	
M5(LV)-384/192-12								12	83.3	15	6	8	
M5(LV)-384/192-15								15	62.5	20	8	10	
M5(LV)-512/120-7	160PQFP	512 (20,000)	120	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/120-10								10	100	12	5	7	
M5(LV)-512/120-12								12	83.3	15	6	8	
M5(LV)-512/120-15								15	62.5	20	8	10	
M5(LV)-512/160-7	208PQFP	512 (20,000)	160	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/160-10								10	100	12	5	7	
M5(LV)-512/160-12								12	83.3	15	6	8	
M5(LV)-512/160-15								15	62.5	20	8	10	
M5(LV)-512/184-7	240PQFP	512 (20,000)	184	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/184-10								10	100	12	5	7	
M5(LV)-512/184-12								12	83.3	15	6	8	
M5(LV)-512/184-15								15	62.5	20	8	10	
M5(LV)-512/192-7	256BGA	512 (20,000)	192	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/192-10								10	100	12	5	7	
M5(LV)-512/192-12								12	83.3	15	6	8	
M5(LV)-512/192-15								15	62.5	20	8	10	
M5(LV)-512/256-7	352BGA	512 (20,000)	256	4	64	Up to 32	Yes	7.5	125	10	4	6	100
M5(LV)-512/256-10								10	100	12	5	7	
M5(LV)-512/256-12								12	83.3	15	6	8	
M5(LV)-512/256-15								15	62.5	20	8	10	

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 4. MACH 5A Devices[1]

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A(3,5)-128/68-5	100PQFP	128	68	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/68-7								7.5	125	10	4	6
M5A(3,5)-128/68-10								10	100	12	5	7
M5A(3,5)-128/68-12								12	83.3	15	6	8
M5A(3,5)-128/74-5	100TQFP	128	74	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/74-7								7.5	125	10	4	6
M5A(3,5)-128/74-10								10	100	12	5	7
M5A(3,5)-128/74-12								12	83.3	15	6	8
M5A(3,5)-128/104-5	144TQFP	128	104	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/104-7								7.5	125	10	4	6
M5A(3,5)-128/104-10								10	100	12	5	7
M5A(3,5)-128/104-12								12	83.3	15	6	8
M5A(3,5)-128/120-5	160PQFP	128	120	4	16	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-128/120-7								7.5	125	10	4	6
M5A(3,5)-128/120-10								10	100	12	5	7
M5A(3,5)-128/120-12								12	83.3	15	6	8
M5A(3,5)-192/68-5	100PQFP	192	68	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/68-7								7.5	125	10	4	6
M5A(3,5)-192/68-10								10	100	12	5	7
M5A(3,5)-192/68-12								12	83.3	15	6	8
M5A(3,5)-192/74-5	100TQFP	192	74	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/74-7								7.5	125	10	4	6
M5A(3,5)-192/74-10								10	100	12	5	7
M5A(3,5)-192/74-12								12	83.3	15	6	8
M5A(3,5)-192/104-5	144TQFP	192	104	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/104-7								7.5	125	10	4	6
M5A(3,5)-192/104-10								10	100	12	5	7
M5A(3,5)-192/104-12								12	83.3	15	6	8
M5A(3,5)-192/120-5	160PQFP	192	120	4	24	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-192/120-7								7.5	125	10	4	6
M5A(3,5)-192/120-10								10	100	12	5	7
M5A(3,5)-192/120-12								12	83.3	15	6	8

Table 4. MACH 5A Devices[1] (Continued)

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A(3,5)-256/68-5	100PQFP	256	68	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/68-7								7.5	125	10	4	6
M5A(3,5)-256/68-10								10	100	12	5	7
M5A(3,5)-256/68-12								12	83.3	15	6	8
M5A(3,5)-256/74-5	100TQFP	256	74	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/74-7								7.5	125	10	4	6
M5A(3,5)-256/74-10								10	100	12	5	7
M5A(3,5)-256/74-12								12	83.3	15	6	8
M5A(3,5)-256/104-5	144TQFP	256	104	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/104-7								7.5	125	10	4	6
M5A(3,5)-256/104-10								10	100	12	5	7
M5A(3,5)-256/104-12								12	83.3	15	6	8
M5A(3,5)-256/120-5	160PQFP	256	120	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/120-7								7.5	125	10	4	6
M5A(3,5)-256/120-10								10	100	12	5	7
M5A(3,5)-256/120-12								12	83.3	15	6	8
M5A(3,5)-256/160-5	208PQFP	256	160	4	32	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A(3,5)-256/160-7								7.5	125	10	4	6
M5A(3,5)-256/160-10								10	100	12	5	7
M5A(3,5)-256/160-12								12	83.3	15	6	8
M5A3-320/120-5	160PQFP	320	120	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/120-6								6.5	166.7	10	3	5
M5A3-320/120-7								7.5	125	10	4	6
M5A3-320/120-10								10	100	12	5	7
M5A3-320/120-12								12	83.3	15	6	8
M5A3-320/160-5	208PQFP	320	160	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/160-6								6.5	166.7	10	3	5
M5A3-320/160-7								7.5	125	10	4	6
M5A3-320/160-10								10	100	12	5	7
M5A3-320/160-12								12	83.3	15	6	8
M5A3-320/192-5	256BGA	320	192	4	40	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-320/192-6								6.5	166.7	10	3	5
M5A3-320/192-7								7.5	125	10	4	6
M5A3-320/192-10								10	100	12	5	7
M5A3-320/192-12								12	83.3	15	6	8

Table 4. MACH 5A Devices[1] (Continued)

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	PT per Output	JTAG-ISP	Commercial		Ind'l[2]		
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[3] ns	t_{CO}[4] ns
M5A3-384/120-5	160PQFP	384	120	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/120-6								6.5	166.7	10	3	5
M5A3-384/120-7								7.5	125	10	4	6
M5A3-384/120-10								10	100	12	5	7
M5A3-384/120-12								12	83.3	15	6	8
M5A3-384/160-5	208PQFP	384	160	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/160-6								6.5	166.7	10	3	5
M5A3-384/160-7								7.5	125	10	4	6
M5A3-384/160-10								10	100	12	5	7
M5A3-384/160-12								12	83.3	15	6	8
M5A3-384/192-5	256BGA	384	192	4	48	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-384/192-6								6.5	166.7	10	3	5
M5A3-384/192-7								7.5	125	10	4	6
M5A3-384/192-10								10	100	12	5	7
M5A3-384/192-12								12	83.3	15	6	8
M5A3-512/120-5	160PQFP	512	120	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/120-6								6.5	166.7	10	3	5
M5A3-512/120-7								7.5	125	10	4	6
M5A3-512/120-10								10	100	12	5	7
M5A3-512/120-12								12	83.3	15	6	8
M5A3-512/160-5	208PQFP	512	160	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/160-6								6.5	166.7	10	3	5
M5A3-512/160-7								7.5	125	10	4	6
M5A3-512/160-10								10	100	12	5	7
M5A3-512/160-12								12	83.3	15	6	8
M5A3-512/192-5	256BGA	512	192	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/192-6								6.5	166.7	10	3	5
M5A3-512/192-7								7.5	125	10	4	6
M5A3-512/192-10								10	100	12	5	7
M5A3-512/192-12								12	83.3	15	6	8
M5A3-512/256-5	352BGA	512	256	4	64	Up to 32	Yes	5.5	181.8	7.5	3	4.5
M5A3-512/256-6								6.5	166.7	10	3	5
M5A3-512/256-7								7.5	125	10	4	6
M5A3-512/256-10								10	100	12	5	7
M5A3-512/256-12								12	83.3	15	6	8

Notes:

1. *Advance Information*
2. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
3. *Minimum setup time from input, I/O, or feedback to clock.*
4. *Maximum time from clock to output.*

MACH 1 & 2 FAMILIES

Table 5. MACH 1 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)	
MACH111-5	44PLCC, 44TQFP	32 (1250)	32	6	8	Up to 12	No	5	182	7.5	3.5	3.5	40	
MACH111-7								7.5	133	10	5.5	5		
MACH111-10								10	100	12	6.5	6		
MACH111-12								12	76.9	14	7	8		
MACH111-15								15	66.6	18	10	10		
MACH131-5	84PLCC	64 (2500)	64	6	16	Up to 12	No	5.5	182	7.5	3.0	4	75	
MACH131-7								7.5	133	10	5.5	5		
MACH131-10								10	100	12	6.5	6		
MACH131-12								12	76.9	14	7	8		
MACH131-15								15	66.6	18	10	10		

Table 6. MACH 2 Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)	
MACH211-7	44PLCC, 44TQFP	64 (2500)	32	6	8	Up to 16	No	7.5	133	10	5.5	4.5	40	
MACH211-10								10	100	12	6.5	6		
MACH211-12								12	83.3	14	7	8		
MACH211-15								15	66.6	18	10	10		
MACH221-7	68PLCC	96 (3750)	48	8	16	Up to 16	No	7.5	133	10	5.5	5	70	
MACH221-10								10	100	12	6.5	6		
MACH221-12								12	83.3	14	7	8		
MACH221-15								15	66.6	18	10	10		
MACH231-6	84PLCC	128 (5000)	64	6	16	Up to 16	No	6	166	-	5	4	135	
MACH231-7								7.5	133	-	5.5	5		
MACH231-10								10	100	12	6.5	6.5		
MACH231-12								12	83.3	14	7	8		
MACH231-15								15	66.6	18	10	10		

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 7. MACH 1SP Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)	
MACH111SP-5	44PLCC, 44TQFP	32 (1250)	32	2	8	Up to 12	Yes	5	182	7.5	3.5	3.5	40	
MACH111SP-7								7.5	133	10	5.5	5		
MACH111SP-10								10	100	12	6.5	6		
MACH111SP-12								12	76.9	14	7	8		
MACH111SP-15								15	66.6	18	10	10		
MACH131SP-5	100PQFP, 100TQFP	64 (2500)	64	6	16	Up to 12	Yes	5.5	182	7.5	3.0	4	75	
MACH131SP-7								7.5	133	10	5.5	5		
MACH131SP-10								10	100	12	6.5	6		
MACH131SP-12								12	76.9	14	7	8		
MACH131SP-15								15	66.6	18	10	10		

Table 8. MACH 2SP Devices

Device	Package	Macrocells (PLD Gates)	I/Os	Dedicated Inputs	Output Enables	PT per Output (w/ NO speed adder)	JTAG-ISP	Commercial		Ind'l[1]				
								t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)	
MACH211SP-6	44PLCC, 44TQFP	64 (2500)	32	2	8	Up to 16	Yes	6	166	-	5	4	40	
MACH211SP-7								7.5	133	10	5.5	4.5		
MACH211SP-10								10	100	12	6.5	6		
MACH211SP-12								12	83.3	14	7	8		
MACH211SP-15								15	66.6	18	10	10		
MACH221SP-7	100PQFP	96 (3750)	48	8	16	Up to 16	Yes	7.5	133	10	5.5	5	70	
MACH221SP-10								10	100	12	6.5	6		
MACH221SP-12								12	83.3	14	7	8		
MACH221SP-15								15	66.6	18	10	10		
MACH231SP-10	100PQFP, 100TQFP	128 (5000)	64	6	16	Up to 16	Yes	10	100	12	6.5	6.5	80	
MACH231SP-12								12	83.3	14	7	8		
MACH231SP-15								15	66.6	18	10	10		

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

The MACH110, MACH120, MACH130, MACH210, MACHLV210, MACH215, MACH220 and MACH230 devices are not listed above and are not recommended for new designs. However, they are still supported by Vantis. For technical or sales support, please call your local Vantis sales office or visit our Web site at www.vantis.com for more information.

VF1 FAMILY

Table 9. VF1 Devices

Device	Usable Gates	VGB Array Size	Package	I/Os	Global Clock Pins	RAM Bits	VGB FlipFlops	I/O Flip-Flops	JTAG	Commercial Speed Grades	Industrial Speed Grades
VF1012	12,000	14x14	144TQFP	108	4	3584	784	336	Yes	-1, -2	-1
			160PQFP	124	4	3584	784	336	Yes	-1, -2	-1
			208PQFP	164	4	3584	784	336	Yes	-1, -2	-1
			256BGA	168	4	3584	784	336	Yes	-1, -2	-1
VF1020	20,000	18x18	144TQFP	108	4	4608	1296	432	Yes	-1, -2	-1
			160PQFP	124	4	4608	1296	432	Yes	-1, -2	-1
			208PQFP	164	4	4608	1296	432	Yes	-1, -2	-1
			256BGA	204	4	4608	1296	432	Yes	-1, -2	-1
VF1025	25,000	20x20	208PQFP	164	4	5120	1600	480	Yes	-1, -2	-1
			256BGA	204	4	5120	1600	480	Yes	-1, -2	-1
			352BGA	240	4	5120	1600	480	Yes	-1, -2	-1
VF1036	36,000	24x24	208PQFP	164	4	6144	2304	576	Yes	-1, -2	-1
			256BGA	204	4	6144	2304	576	Yes	-1, -2	-1
			352BGA	288	4	6144	2304	576	Yes	-1, -2	-1

Table 10. Universal CMOS 16V8 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE16V8H-5	20J	8	10	8	Half Power CMOS PAL Device	5	166	–	3	4	125
PALCE16V8H-7	20P, S, J					7.5	125	–	5	5	115
PALCE16V8H-10						10	71.4	10	7.5	7.5	115
PALCE16V8H-15						15	50	15	12	10	90
PALCE16V8H-25						25	40	25	13	11	90
PALCE16V8Q-10	20P, J	8	10	8	Quarter Power CMOS PAL Device	10	71.4	–	7.5	7.5	55
PALCE16V8Q-15						15	50	15	12	10	55
PALCE16V8Q-20						–	–	20	13	11	65
PALCE16V8Q-25						25	40	25	15	12	55

Table 11. Universal CMOS 20V8 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE20V8H-5	28J	8	14	8	Half Power CMOS PAL Device	5	166	–	3	4	125
PALCE20V8H-7	24P, 28J					7.5	125	–	5	5	115
PALCE20V8H-10						10	71.4	–	7.5	7.5	115
PALCE20V8H-15						15	50	15	12	10	90
PALCE20V8H-25						25	40	25	15	12	90
PALCE20V8Q-10	24P, 28 J	8	14	8	Quarter Power CMOS PAL Device	10	71.4	–	7.5	7.5	55
PALCE20V8Q-15						15	50	–	12	10	55
PALCE20V8Q-20						–	–	20	13	11	65
PALCE20V8Q-25						25	40	25	15	12	55

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 12. Universal CMOS 22V10 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns			
PALCE22V10H-5	28J	10	12	8 to 16	Half Power Varied Prod Term Distribution Bus-Friendly ™	5	150	–	3	4	125
PALCE22V10H-7	24P, 28 J					7.5	133	–	4.5	4.5	115
PALCE22V10H-10	24P, S, 28J					10	110	10	6	6	120
PALCE22V10H-15	24P, S, 28J					15	58.8	15	10	10	90
PALCE22V10H-20	24P, 28J					–	–	20	12	12	100
PALCE22V10H-25	24P, S, 28J					25	35.7	25	15	15	90
PALCE22V10Q-10	24P, 28J	10	12	8 to 16	Quarter Power Bus-Friendly	10	110	–	6	6	55
PALCE22V10Q-15						15	58.8	–	10	10	55
PALCE22V10Q-25						25	35.7	–	15	15	55

Table 13. Universal CMOS 24V10 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns			
PALCE24V10H-15	28P, J	10	12	8 to 16	CMOS PAL Device	15	66	–	10	10	115
PALCE24V10H-25						25	50	–	12	12	115

Table 14. Universal CMOS 26V12 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns			
PALCE26V12H-7	28J	12	14	8 to 16	Adv. 22V10 M/C Bus-Friendly	7.5	125	–	3.5	6	115
PALCE26V12H-10	28P, J					10	105	10	5	9	115
PALCE26V12H-15						15	58.8	15	10	10	105
PALCE26V12H-20						20	43	20	13	12	105

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*

Table 15. Universal CMOS 29M16 PAL Devices

Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
						t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
PALCE29M16H-25	24P, 28J	16	5	8 to 16	Adv. Macrocell	25	33.3	–	15	15	100

Table 16. Zero Power CMOS PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
16V8	PALCE16V8Z-12	20P, J	8	10	8	Zero Power CMOS PAL Device	–	–	12	8	8	0.03
	PALCE16V8Z-15						–	–	15	10	10	0.015
	PALCE16V8Z-25	20P, S, J					25	50	25	20	10	0.015
22V10	PALCE22V10Z-15	24P, 28J	10	12	8 to 16	Zero Power	–	–	15	10	10	0.03
	PALCE22V10Z-25	24P, S, 28J					25	35.7	25	15	15	0.03

Table 17. 3.3-V Low Voltage CMOS PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
16V8	PALLV16V8-10	20P, S, J	8	10	8	3.3V	10	83.3	–	7	7	55
	PALLV16V8Z-20	20P, J				3.3V, Zero Power	–	–	20	15	10	0.03
22V10	PALLV22V10-7	28J	10	12	8 to 16	3.3V	7.5	133	–	4.5	5.5	75
	PALLV22V10-10	24P, 28J					10	110	–	5.5	6.5	60
	PALLV22V10-15						15	58.8	15	10	10	60
	PALLV22V10Z-25	24P, 28J				3.3V, Zero Power	–	–	25	15	15	0.03

Table 18. Asynchronous Universal PAL Devices

Family	Device	Package	I/Os	Dedicated Inputs	PT per Output	Feature	Commercial		Ind'l[1]			
							t_{PD} ns	f_{CNT} MHz	t_{PD} ns	t_{SS}[2] ns	t_{CO}[3] ns	I_{CC} mA (Static)
610	PALCE610H-15	24P, 28J	16	4	8	J-K F/F Programmable CLK	15	76.1	–	12	8	90
	PALCE610H-25						25	40	–	15	12	90
20RA10	PALCE20RA10H-7	28J 24P, 28J	10	10	4	Programmable CLK	7.5	100[4]	7.5	2.5	7.5	100
	PALCE20RA10H-10						10	76.9[4]	10	3	10	100
	PALCE20RA10H-15						15	52.6[4]	15	4	15	100
	PALCE20RA10H-20						20	37[4]	20	4	20	90
29MA16	PALCE29MA16H-25	24P, 28J	16	5	4 to 12	Prog. CLK, Adv M/C	25	33.3	–	15	15	100

Notes:

1. *MACH devices are dual-marked with both commercial and industrial speeds while CMOS PAL devices are marked separately.*
2. *Minimum setup time from input, I/O, or feedback to clock.*
3. *Maximum time from clock to output.*
4. *Specified as f_{MAX} (External Feedback)*

This databook contains the PAL device information for the PALCE16V8, PALLV16V8, PALCE20V8, PALCE22V10, and PALLV22V10. For information on other PAL devices, please refer to the datasheets on our Web site at www.vantis.com.

MACH Families

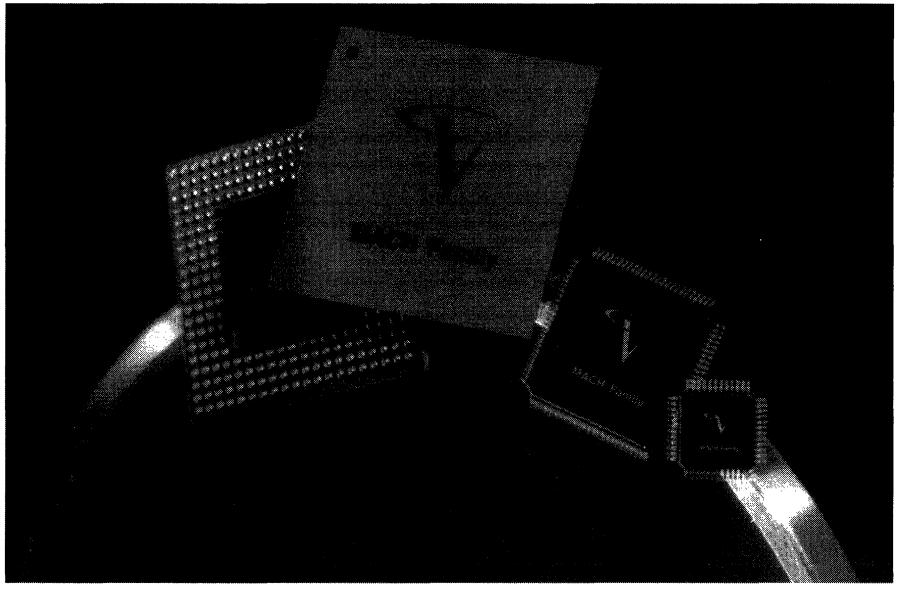

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Table 1. MACH 4 Device Features[1,2]

Feature	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4-256/128 M4LV-256/128
Macrocells	32	64	96	128	128	192	256
Maximum User I/O Pins	32	32	48	64	64	96	128
t_{PD} (ns)	7.5	7.5	7.5	7.5	7.5	7.5	7.5
f_{CNT} (MHz)	111	111	111	111	111	111	111
t_{COS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
t_{SS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Static Power (mA)	25	25	50	70	70	85	100
JTAG Compliant	Yes	Yes	Yes	Yes	No	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. *For information on the M4-96/96 device, please refer to the M4-96/96 datasheet at www.vantis.com.*
2. *"M4-xxx" is for 5-V devices. "M4LV-xxx" is for 3.3-V devices.*

Table 2. MACH 4A Device Features[1,2]

Feature	M4A3-32/32 M4A5-32/32	M4A3-64/32 M4A5-64/32	M4A3-96/48 M4A5-96/48	M4A3-128/64 M4A5-128/64	M4A3-192/96 M4A5-192/96	M4A3-256/128 M4A5-256/128
Macrocells	32	64	96	128	192	256
Maximum User I/O Pins	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.0	5.0	5.0	5.0	5.0
f_{CNT} (MHz)	182	182	182	182	182	182
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.0	4.0
t_{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0
Static Power (mA)	TBD	TBD	TBD	TBD	TBD	TBD
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. *All information on MACH 4A devices is Advance Information. Please contact a Vantis sales representative for details on availability.*
2. *"M4A5-xxx" is for 5-V devices. "M4A3-xxx" is for 3.3-V devices.*

GENERAL DESCRIPTION

The MACH® 4 family from Vantis offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. Both the MACH 4 and the MACH 4A families offer 5-V (M4-xxx and M4A5-xxx) and 3.3-V (M4LV-xxx and M4A3-xxx) operation.

All MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing capability also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time Fit and easy system integration with pin-out retention after any design change and refit. With multi-tiered central switch matrices, enhanced logic arrays, intelligent logic allocators with an XOR gate and multi-clocking, the MACH 4 family has D or T-type registers and latches as well as synchronous/asynchronous logic and flexible set/reset capabilities. For both 3.3-V and 5-V operations, MACH 4 products can deliver guaranteed fixed timing as fast as 5.0 ns t_{PD} and 182 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Tables 3 and 4).

Table 3. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-18
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	I
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	I
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	I
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	I
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	I
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	I
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	I

Note:

1. C = Commercial, I = Industrial

Table 4. MACH 4A Speed Grades

Device	Speed Grade[1, 2]							
	-50	-55	-60	-65	-7	-10	-12	-14
M4A3-32/32 M4A5-32/32	C	C	C	C	C, I	C, I	C, I	I
M4A3-64/32 M4A5-64/32	C	C	C	C	C, I	C, I	C, I	I
M4A3-96/48 M4A5-96/48	C	C	C	C	C, I	C, I	C, I	I
M4A3-128/64 M4A5-128/64	C	C	C	C	C, I	C, I	C, I	I
M4A3-192/96 M4A5-192/96	C	C	C	C	C, I	C, I	C, I	I
M4A3-256/128 M4A5-256/128	C	C	C	C	C, I	C, I	C, I	I

Notes:

1. *C = Commercial, I = Industrial*
2. *All information on MACH 4A devices is Advance Information. Please contact a Vantis sales representative for details on availability.*

The MACH 4 family offers 6 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Tables 5 and 6). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 5. MACH 4 Package and I/O Options (Number of I/Os in Table)

Package	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4-256/128 M4LV-256/128
44-pin PLCC	32	32					
44-pin TQFP	32	32					
48-pin TQFP	32	32					
84-pin PLCC					64		
100-pin TQFP			48	64			
100-pin PQFP				64			
144-pin TQFP						96	
208-pin PQFP							128
256-pin BGA							128

Table 6. MACH 4A Package and I/O Options[1] (Number of I/Os in Table)

Package	M4A3-32/32 M4A5-32/32	M4A3-64/32 M4A5-64/32	M4A3-96/48 M4A5-96/48	M4A3-128/64 M4A5-128/64	M4A3-192/96 M4A5-192/96	M4A3-256/128 M4A5-256/128
44-pin PLCC	32	32				
44-pin TQFP	32	32				
48-pin TQFP	32	32				
100-pin TQFP			48	64		
100-pin PQFP				64		
144-pin TQFP					96	
208-pin PQFP						128
256-pin BGA						128

Note:

1. All information on MACH 4A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

Vantis offers software design support for MACH devices in both the MACHXL® and DesignDirect development systems. The DesignDirect development system is the Vantis implementation software that includes support for all Vantis CPLD, FPGA and SPLD devices. This system is supported under Windows '95, '98 and NT as well as Sun Solaris and HPUX.

DesignDirect software is designed for use with design entry, simulaion and verification software from leading-edge tool vendors such as Cadence, Exemplar Logic, Mentor Graphics, Model Technology , Synopsys, Synplicity, Viewlogic and others. It accepts EDIF 2 0 0 input netlists, generates JEDEC files for Vantis PLDs and creates industry-standard EDIF, Verilog, VITAL-compliant VHDL and SDF simulation netlist for design verification.

DesignDirect software is also available in product configurations that include VHDL and Verilog synthesis from Exemplar Logic and VHDL, Verilog RTL and gate level timing simulation from Model Technology. Schematic capture and ABEL entry, as well as functional simulation, are also provided.

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4 architecture, the macrocells have been decoupled from the product terms through the logic allocator, and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

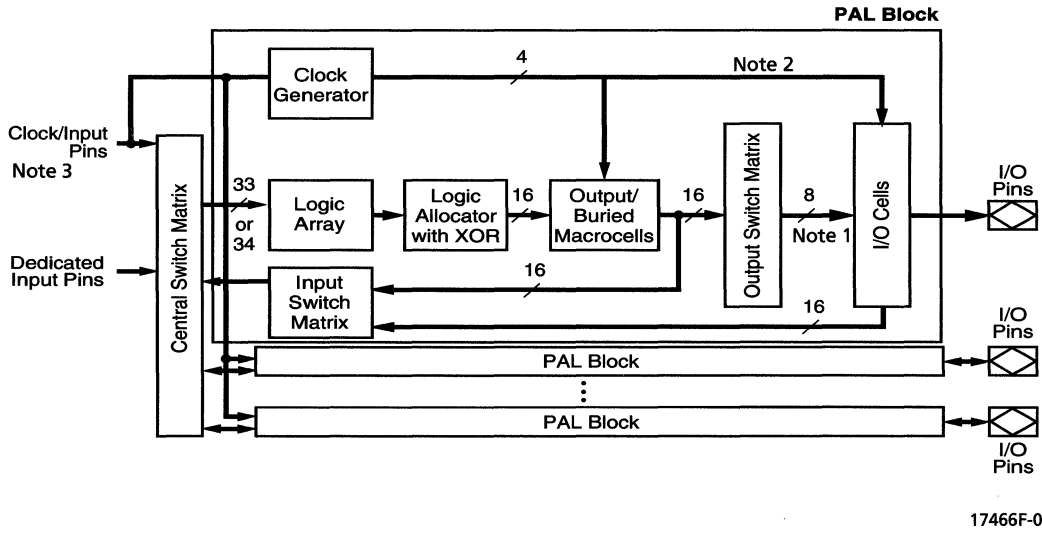


Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for M4(LV)-32/32 and M4A(3,5)-32/32 devices.*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32 or M4A(3,5)-32/32.*
3. *M4(LV)-192/96, M4(LV)-256/128, M4A(3,5)-192/96 and M4A(3,5)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 7), and are provided in both true and complement forms for efficient logic implementation.

Table 7. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4(LV)-32/32 and M4A(3,5)-32/32	33
M4(LV)-64/32 and M4A(3,5)-64/32	33
M4(LV)-96/48 and M4A(3,5)-96/48	33
M4(LV)-128/64 and M4A(3,5)-128/64	33
M4(LV)-128N/64	33
M4(LV)-192/96 and M4A(3,5)-192/96	34
M4(LV)-256/128 and M4A(3,5)-256/128	34

Because the number of product terms available for a given logic function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 8 and 9.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

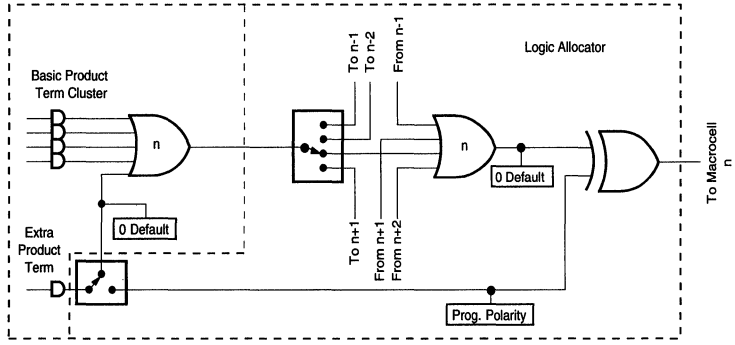
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

Table 8. Logic Allocator for MACH 4 Devices (except M4(LV)-32/32 and M4A(3,5)-32/32)

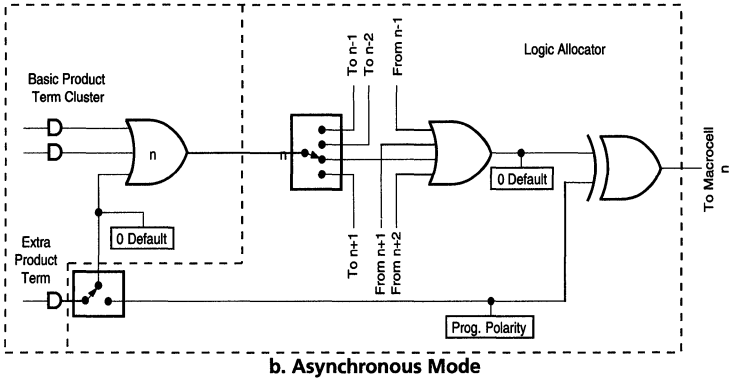
Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_7, C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7, C_8	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8, C_9	M_{15}	C_{14}, C_{15}

Table 9. Logic Allocator for M4(LV)-32/32 and M4A(3,5)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}



a. Synchronous Mode



b. Asynchronous Mode

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Figure 2. Logic Allocator: Configuration of Cluster "n" Set by Mode of Macrocell "n"

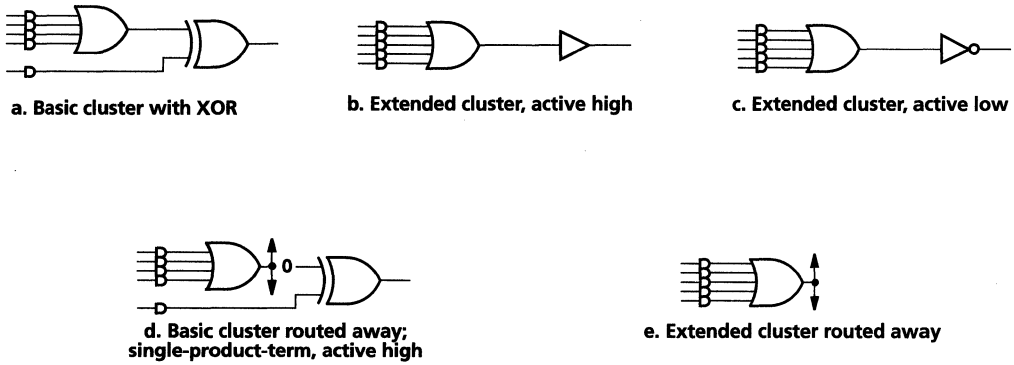


Figure 3. Logic Allocator Configurations: Synchronous Mode

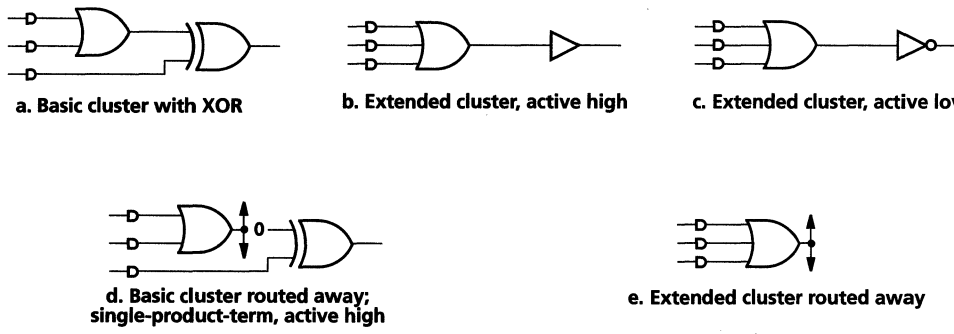


Figure 4. Logic Allocator Configurations: Asynchronous Mode

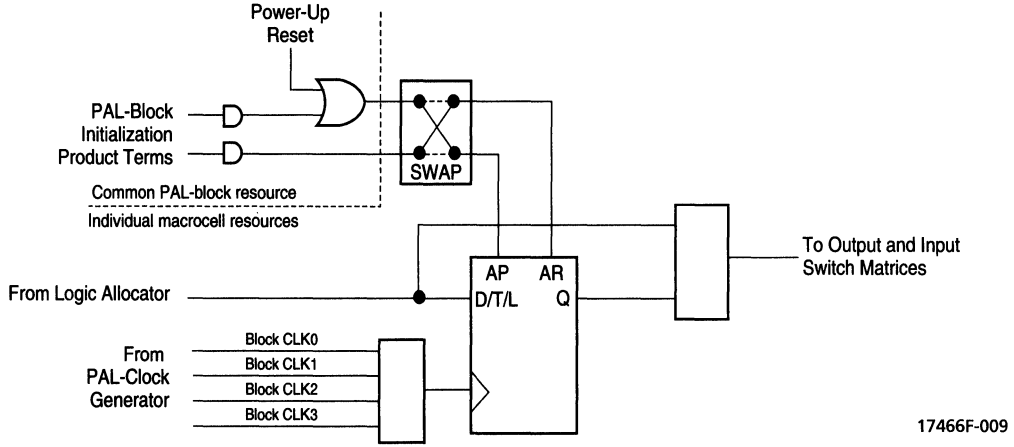
Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

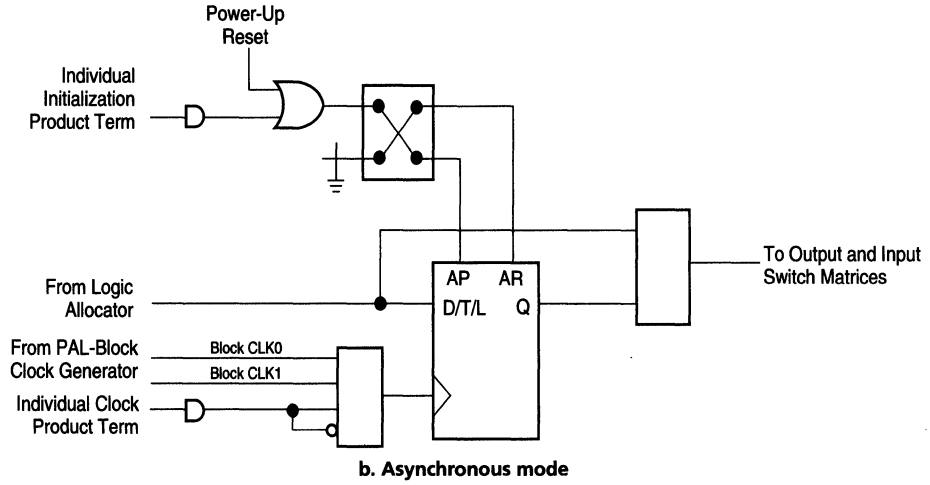
Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only effects clocking and initialization in the macrocell.



a. Synchronous mode

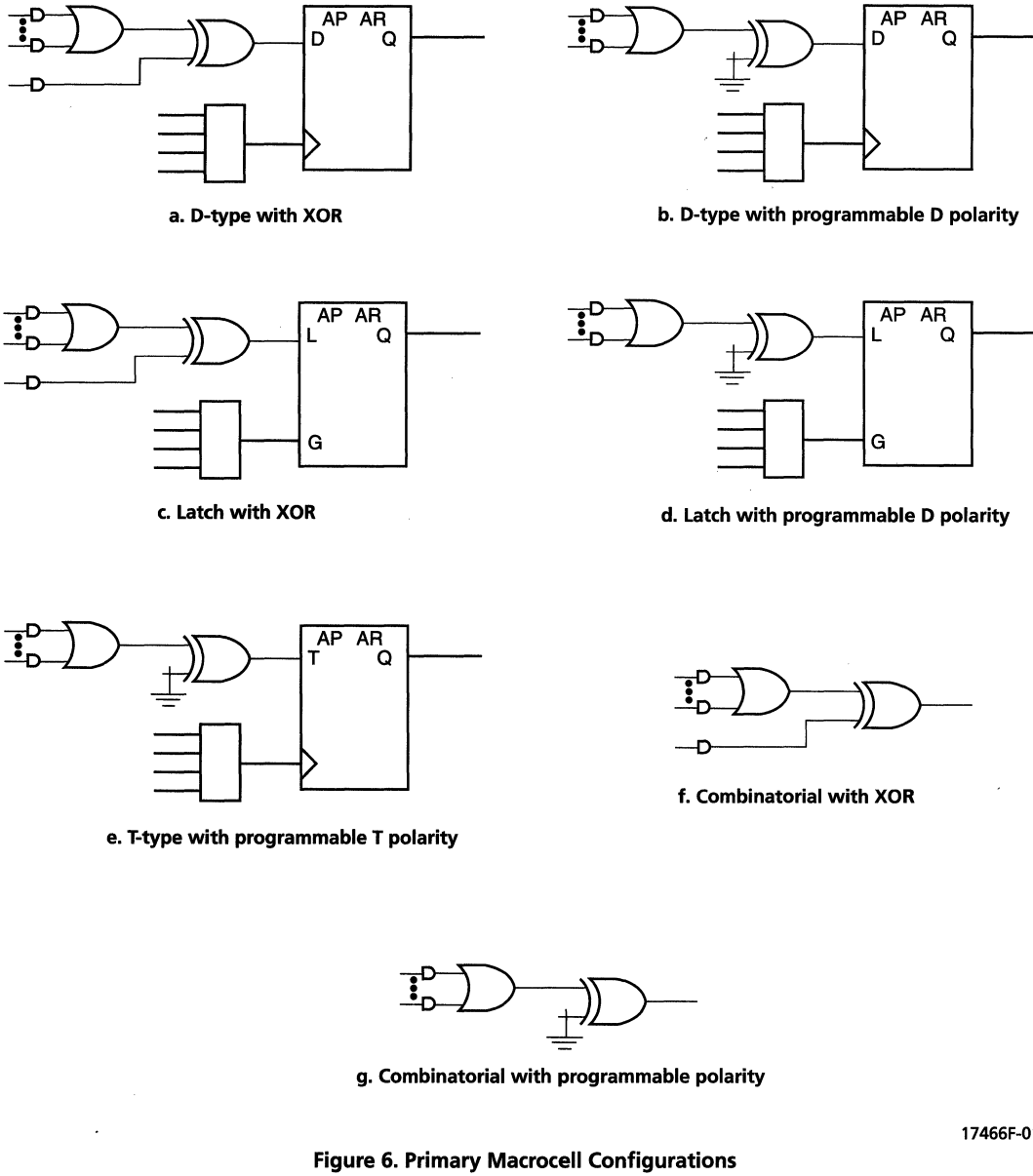


b. Asynchronous mode

Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 10. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



a. D-type with XOR

b. D-type with programmable D polarity

c. Latch with XOR

d. Latch with programmable D polarity

e. T-type with programmable T polarity

f. Combinatorial with XOR

g. Combinatorial with programmable polarity

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Figure 6. Primary Macrocell Configurations

Table 10. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

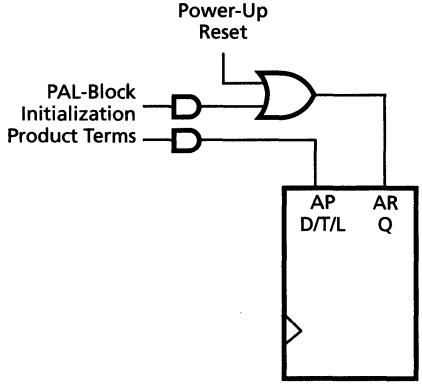
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

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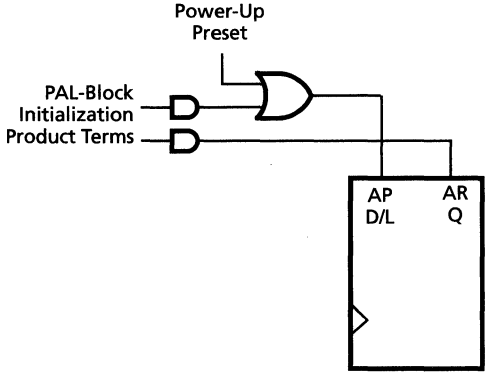

b. Power-up preset

17466F-013

Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.

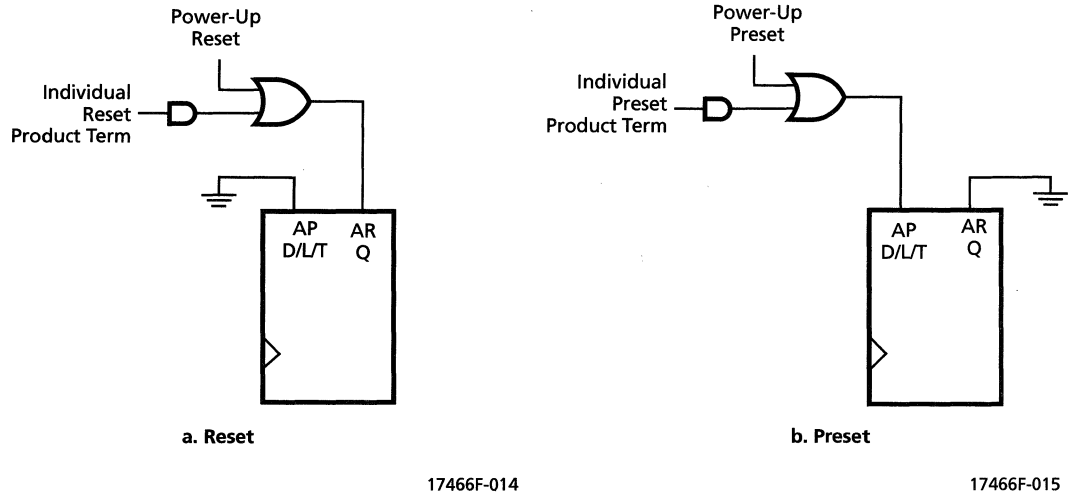

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Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 11. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 11. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 10
0	1	X	1
1	0	X	0
1	1	X	0

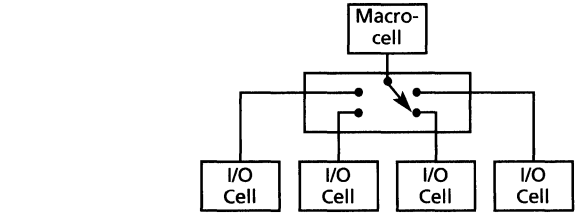
Note:

1. Transparent latch is unaffected by AR, AP

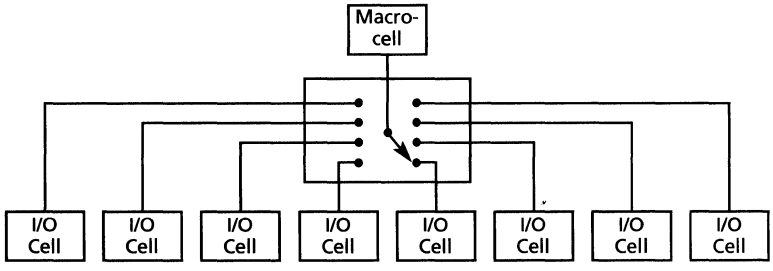
Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

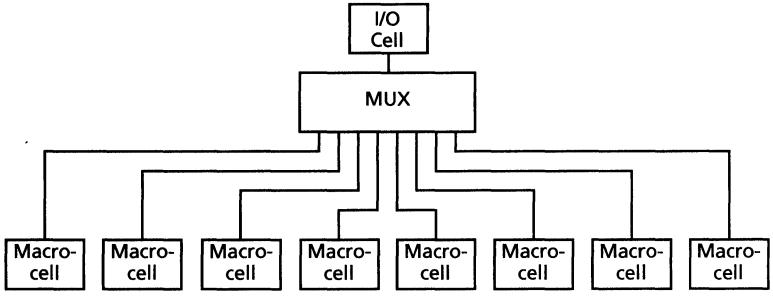
In MACH 4 devices (except M4(LV)-32/32 and M4A(3,5)-32/32), each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The M4(LV)-32/32 and M4A(3,5)-32/32 allow every macrocell to drive an I/O cell (Figures 12 and 13).



a. Macrocell drives one of 4 I/Os (except M4(LV)-32/32 and M4A(3,5)-32/32)



b. Macrocell drives one of 8 I/Os for M4(LV)-32/32 and M4A(3,5)-32/32



c. I/O can choose one of 8 macrocells

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Figure 9. MACH 4 Output Switch Matrix

Table 12. Output Switch Matrix Combinations for MACH 4 Devices (except M4(LV)-32/32 and M4A(3,5)-32/32)

Macrocell	Routable to I/O Pins
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 13. Output Switch Matrix Combinations for M4(LV)-32/32 and M4A(3,5)-32/32

Macrocell	Routable to I/O Pins
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
I/O Pin	**Available Macrocells**
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and in all but the M4(LV)-32/32 and the M4A(3,5)-32/32 devices, a flip-flop. An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

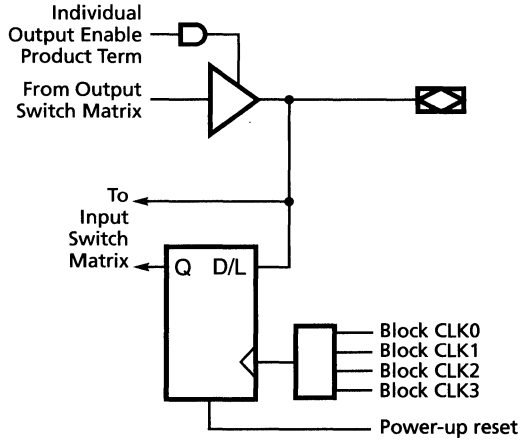


Figure 10. I/O Cell for MACH 4 Devices (except M4(LV)-32/32 and M4A(3,5)-32/32)

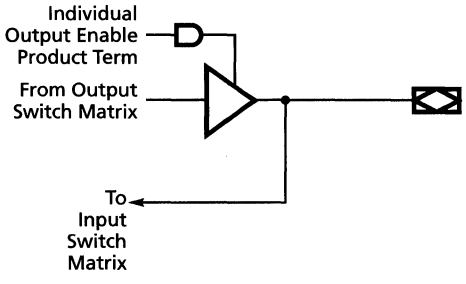


Figure 11. I/O Cell for M4(LV)-32/32 and M4A(3,5)-32/32

The MACH 4 I/O cell contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

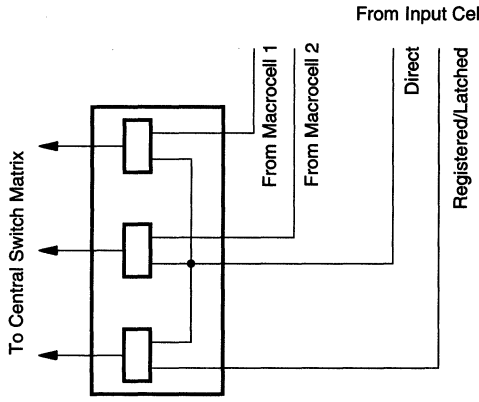
Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



Note: except M4(LV)-32/32 and M4A(3,5)-32/32

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Figure 12. MACH 4 Input Switch Matrix

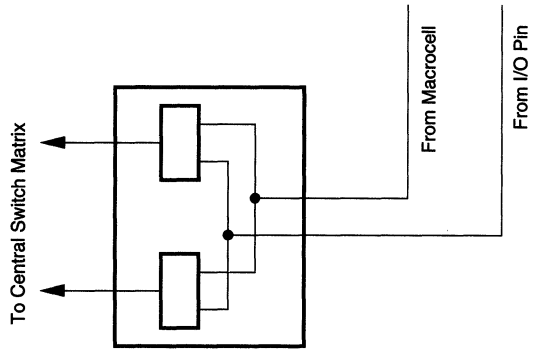

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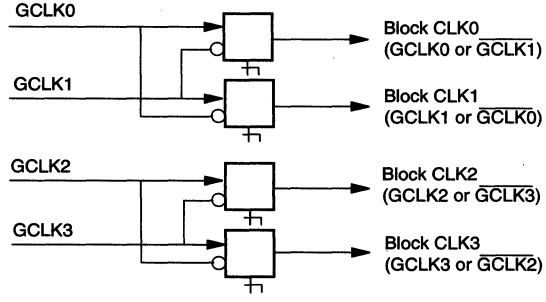
Figure 13. M4(LV)-32/32 and M4A(3,5)-32/32 Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466F-004

Figure 14. PAL Block Clock Generator [1]

Note:

1. *M4(LV)-32/32, M4A(3,5)-32/32, M4(LV)-64/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

Table 14. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4(LV)-32/32, M4A(3,5)-32/32, M4(LV)-64/32 and M4A(3,5)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 4 timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

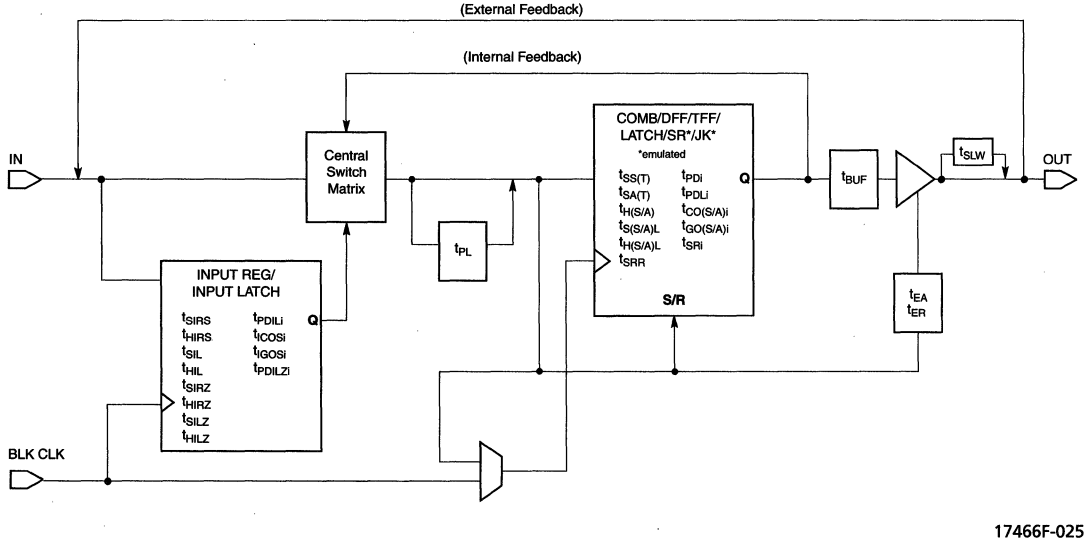


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Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other non-Vantis CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.

JTAG BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have JTAG boundary scan cells and are compliant to the JTAG standard, IEEE 1149.1. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

JTAG IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 4 devices provide In-System Programming (ISP) capability through their JTAG ports. This capability has been implemented in a manner that ensures that the JTAG port remains compliant to the IEEE 1149.1 standard. By using JTAG as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 4 devices can be programmed across the commercial temperature and voltage range. Vantis provides its free PC-based VantisPRO software to facilitate in-system programming. VantisPRO takes the JEDEC file output produced by Vantis' design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. VantisPRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, VantisPRO software can output files in formats understood by common automated test equipment. This equpment can then be used to program MACH 4 devices during the testing of a circuit board. For more information about in-system programming, refer to the separate document entitled *MACH ISP Manual.*

PCI COMPLIANT

MACH 4(A) devices in the -50/-55/-60/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

PULL UP OR BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level

"1." For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

All MACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are weakly pulled up. For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

POWER MANAGEMENT

Each individual PAL block in MACH 4 devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each MACH 4 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

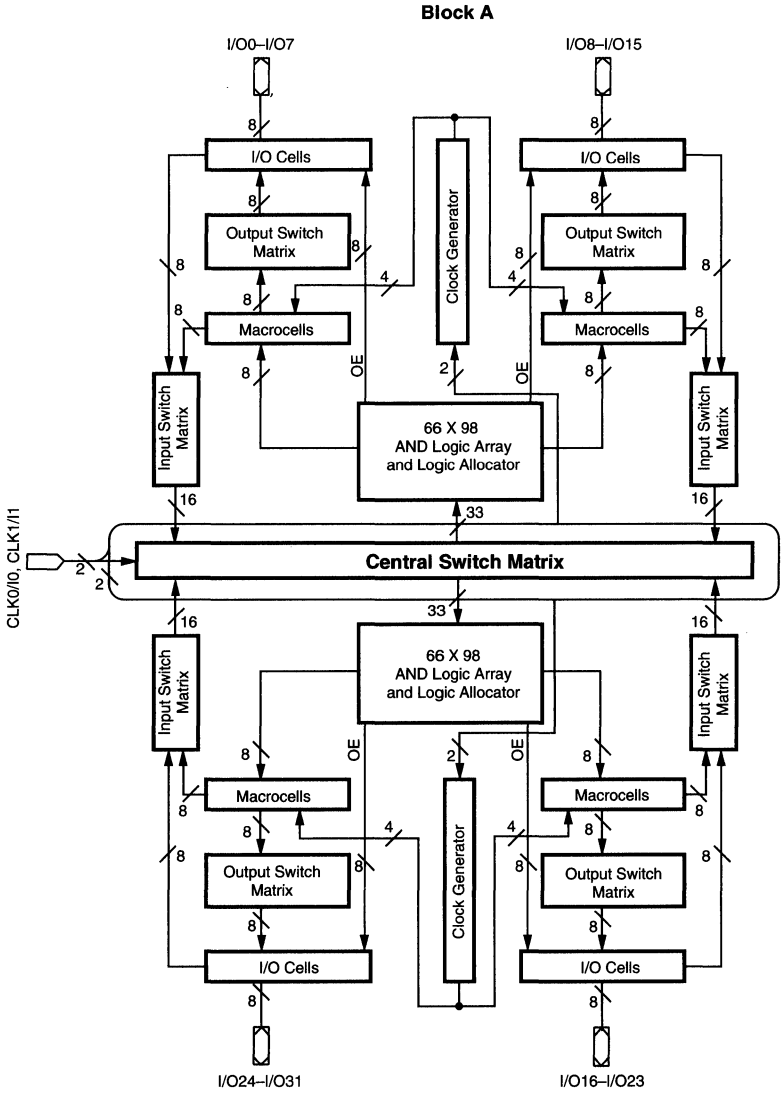
SECURITY BIT

A programmable security bit is provided on the MACH 4 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

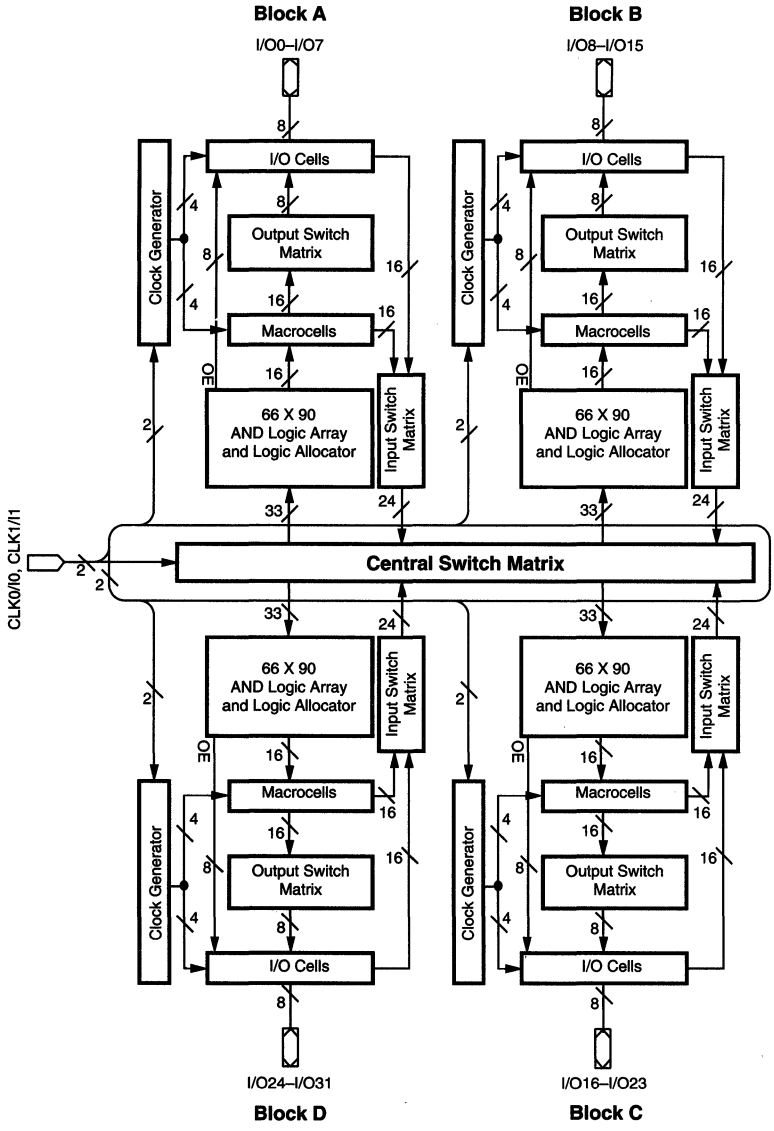
MACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.

BLOCK DIAGRAM – M4(LV)-32/32 AND M4A(3,5)-32/32



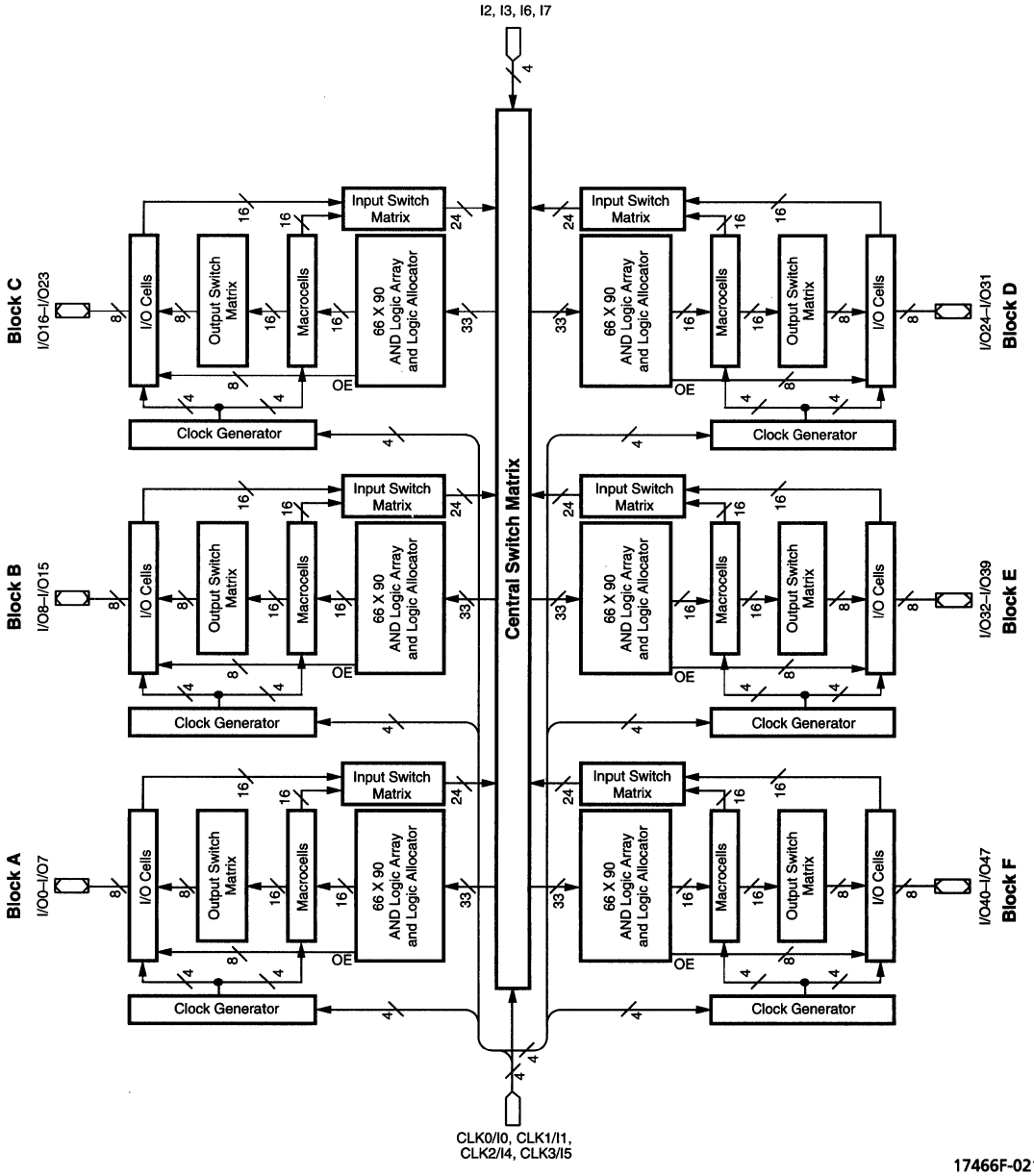
17466F-019

BLOCK DIAGRAM – M4(LV)-64/32 AND M4A(3,5)-64/32



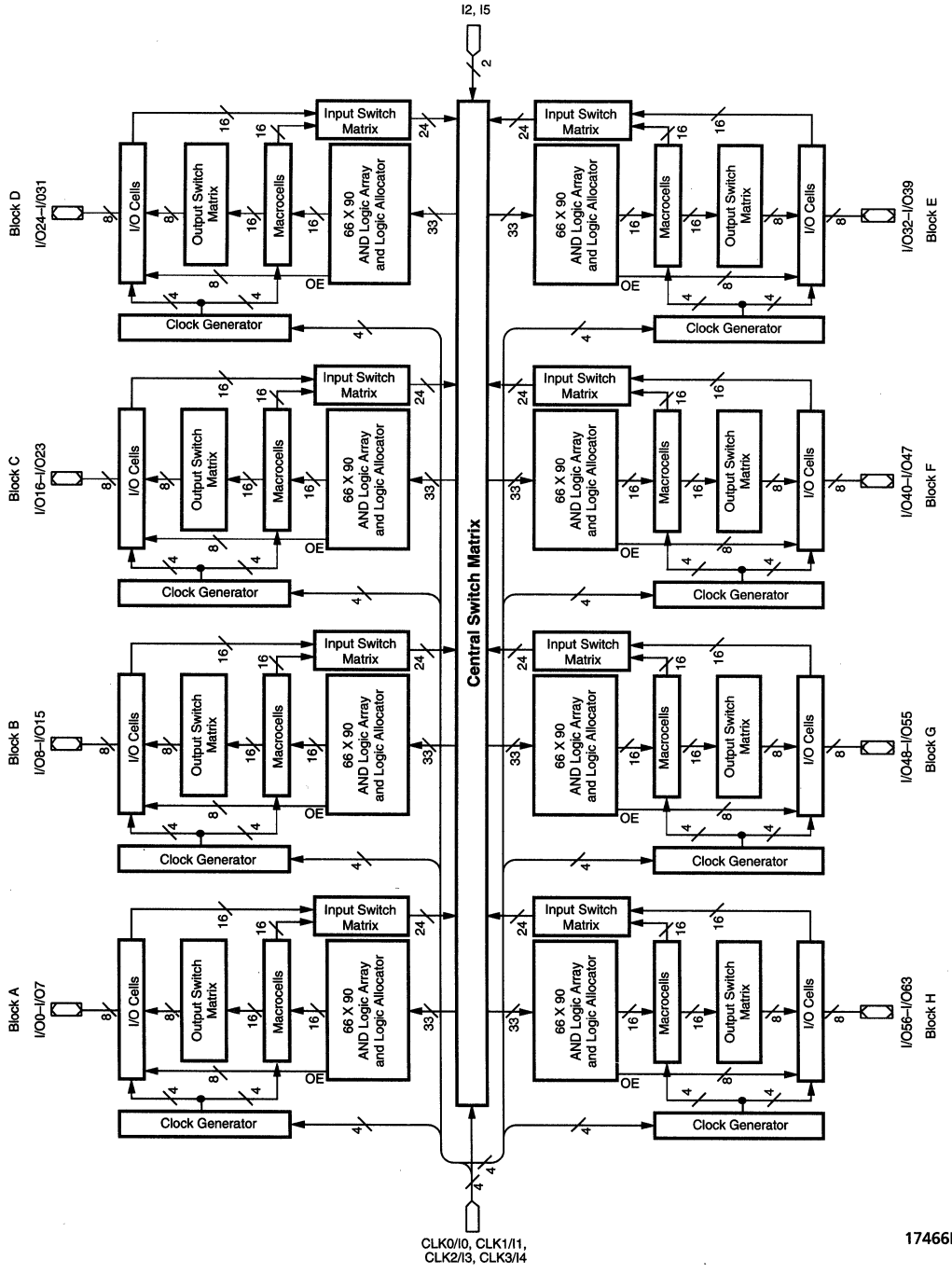
17466F-020

BLOCK DIAGRAM – M4(LV)-96/48 AND M4A(3,5)-96/48

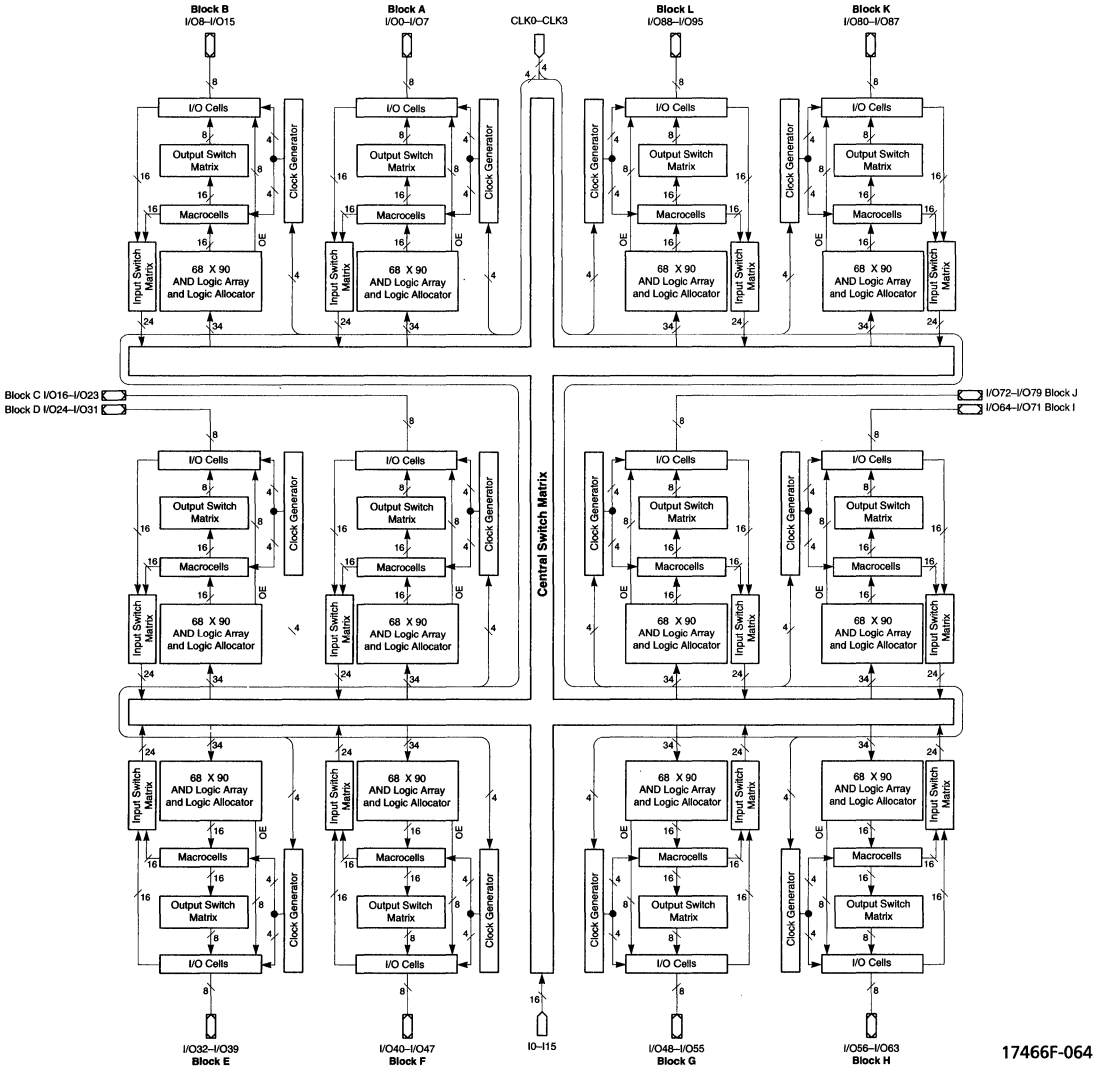


17466F-021

BLOCK DIAGRAM – M4(LV)-128N/64, M4(LV)-128/64 AND M4A(3,5)-128/64

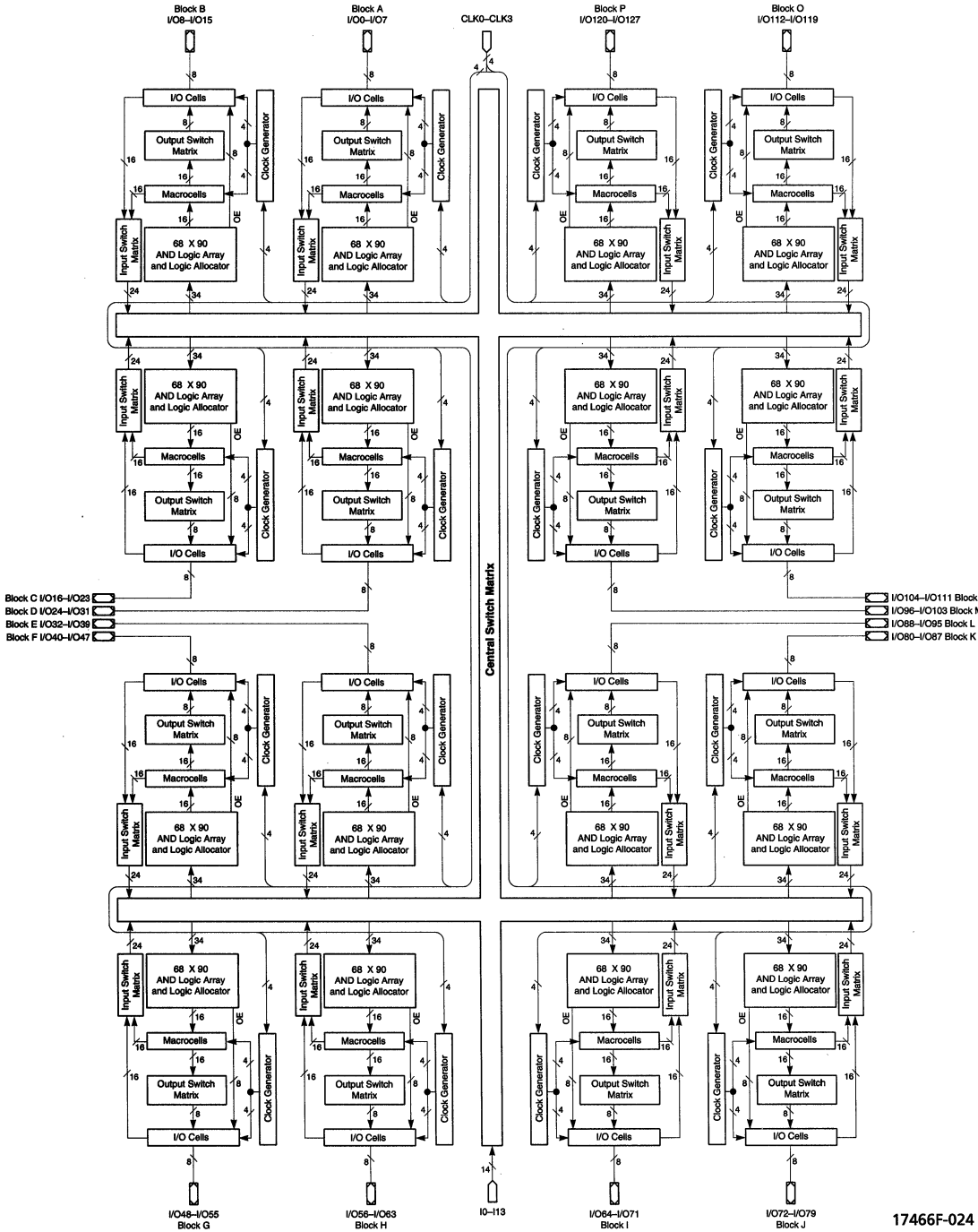


BLOCK DIAGRAM – M4(LV)-192/96 AND M4A(3,5)-192/96



17466F-064

BLOCK DIAGRAM – M4(LV)-256/128 AND M4A(3,5)-256/128



17466F-024

ABSOLUTE MAXIMUM RATINGS

M4 and M4A5

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -5°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

ABSOLUTE MAXIMUM RATINGS

M4LV and M4A3

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1]

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:														
t_{PDi}	Internal combinatorial propagation delay		5.5		8.0		10.0		12.0		13.0		16.0	ns
t_{PD}	Combinatorial propagation delay		7.5		10.0		12.0		14.0		15.0		18.0	ns
Registered Delays:														
t_{SS}	Synchronous clock setup time, D-type register	5.5		6.0		7.0		10.0		10.0		12.0		ns
t_{SST}	Synchronous clock setup time, T-type register	6.5		7.0		8.0		11.0		11.0		13.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	4.5		5.0		6.0		9.0		9.0		11.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{COSi}	Synchronous clock to internal output		3.5		4.5		6.0		8.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		5.5		6.5		8.0		10.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		7.5		10.0		12.0		16.0		16.0		18.0	ns
t_{COA}	Asynchronous clock to output		9.5		12.0		14.0		18.0		18.0		20.0	ns
Latched Delays:														
t_{SSL}	Synchronous Latch setup time	6.0		7.0		8.0		10.0		10.0		12.0		ns
t_{SAL}	Asynchronous Latch setup time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{HSL}	Synchronous Latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous Latch hold time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{PDLi}	Transparent latch to internal output		8.0		10.0		12.0		15.0		15.0		18.0	ns
t_{PDL}	Propagation delay through transparent latch to output		10.0		12.0		14.0		17.0		17.0		20.0	ns
t_{GOSi}	Synchronous Gate to internal output		4.0		5.5		8.0		9.0		9.0		10.0	ns
t_{GOS}	Synchronous Gate to output		6.0		7.5		10.0		11.0		11.0		12.0	ns
t_{GOAi}	Asynchronous Gate to internal output		9.0		11.0		14.0		17.0		17.0		20.0	ns
t_{GOA}	Asynchronous Gate to output		11.0		13.0		16.0		19.0		19.0		22.0	ns
Input Register Delays:														
t_{SIRS}	Input register setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.5		4.5		6.0		6.0		6.0		6.0	ns
Input Latch Delays:														
t_{SIL}	Input latch setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		4.0		4.0		4.0		5.0		5.0		6.0	ns
t_{PDILi}	Transparent input latch to internal feedback		2.0		2.0		2.0		2.0		2.0		2.0	ns
Input Register Delays with ZHT Option:														
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		ns

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input Latch Delays with ZHT Option:														
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:														
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		9.5		10.0		12.0		15.0		15.0		17.0	ns
t_{ER}	Output disable time		9.5		10.0		12.0		15.0		15.0		17.0	ns
Power Delay:														
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:														
t_{SRi}	Asynchronous reset or preset to internal register output		10.0		12.0		14.0		18.0		18.0		20.0	ns
t_{SR}	Asynchronous reset or preset to register output		12.0		14.0		16.0		20.0		20.0		22.0	ns
t_{SRR}	Asynchronous reset and preset register recovery time	8.0		8.0		10.0		15.0		15.0		17.0		ns
t_{SRW}	Asynchronous reset or preset width	10.0		10.0		12.0		15.0		15.0		17.0		ns
Clock/LE Width:														
t_{WLS}	Global clock width low	3.0		5.0		6.0		6.0		6.0		7.0		ns
t_{WHS}	Global clock width high	3.0		5.0		6.0		6.0		6.0		7.0		ns
t_{WLA}	Product term clock width low	4.0		5.0		8.0		9.0		9.0		10.0		ns
t_{WHA}	Product term clock width high	4.0		5.0		8.0		9.0		9.0		10.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	5.0		5.0		6.0		6.0		6.0		7.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		5.0		6.0		9.0		9.0		11.0		ns
t_{WIRL}	Input register clock width low	4.5		5.0		6.0		6.0		6.0		7.0		ns
t_{WIRH}	Input register clock width high	4.5		5.0		6.0		6.0		6.0		7.0		ns
t_{WIL}	Input latch gate width	5.0		5.0		6.0		6.0		6.0		7.0		ns

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:														
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	90.9		80.0		66.7		50.0		50.0		41.7		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	83.3		74.1		62.5		47.6		47.6		40.0		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	111.1		95.2		76.9		55.6		55.6		45.5		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	100.0		87.0		71.4		52.6		52.6		43.5		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	153.8		100.0		83.3		83.3		83.3		71.4		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	76.9		62.5		52.6		38.5		38.5		33.3		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	71.4		58.8		50.0		37.0		37.0		32.3		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	90.9		71.4		58.8		41.7		41.7		35.7		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	83.3		66.7		55.6		40.0		40.0		34.5		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	125.0		100.0		62.5		55.6		55.6		50.0		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	111.0		100.0		83.3		83.3		83.3		71.4		MHz

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

MACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:																		
t_{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.0		4.5		5.0		7.0		9.0		11.0	ns
t_{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t_{SS}	Synchronous clock setup time, D-type register	3.0		3.5		4.0		4.0		5.5		6.0		7.0		10.0		ns
t_{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.5		4.5		6.5		7.0		8.0		11.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		3.0		3.0		3.5		4.0		5.0		8.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.5		3.5		4.5		5.0		6.0		9.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	2.5		2.5		3.0		3.0		3.5		4.0		5.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		2.5		2.5		2.5		2.5		2.5		3.5		3.5	ns
t_{COS}	Synchronous clock to output		4.0		4.0		4.5		4.5		5.0		5.5		6.5		6.5	ns
t_{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t_{COA}	Asynchronous clock to output		6.5		6.5		7.0		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t_{SSL}	Synchronous latch setup time	4.0		4.0		4.5		4.5		6.0		7.0		8.0		10.0		ns
t_{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{PDLi}	Transparent latch to internal output		5.5		5.5		6.0		6.0		7.5		9.0		11.0		12.0	ns
t_{PDL}	Propagation delay through transparent latch to output		7.0		7.0		8.0		8.0		10.0		12.0		14.0		15.0	ns
t_{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t_{GOS}	Synchronous gate to output		4.5		4.5		5.0		5.0		6.0		7.5		10.0		11.0	ns
t_{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t_{GOA}	Asynchronous gate to output		7.5		7.5		8.0		8.0		11.0		13.0		16.0		18.0	ns

MACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input Register Delays:																		
t_{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t_{SIL}	Input latch setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		3.5		3.5		4.0		4.0		4.0		4.0		4.0		5.0	ns
t_{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
Input Register Delays with ZHT Option:																		
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t_{BUF}	Output buffer delay		1.5		1.5		2.0		2.0		2.5		3.0		3.0		3.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t_{SRi}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t_{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t_{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t_{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		5.0		6.0		6.0		ns

MACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		5.0		6.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t_{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

MACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:																		
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	143		133		118		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	125		125		111		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		154		154		125		118		95.2		74.1		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	154		161		143		143		111		105		87.0		69.0		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	250		250		200		200		154		125		100		83.3		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111		111		100		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	105		105		95.2		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	125		125		118		118		95.2		76.9		62.5		47.6		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	167		167		143		143		125		100		62.5		55.6		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

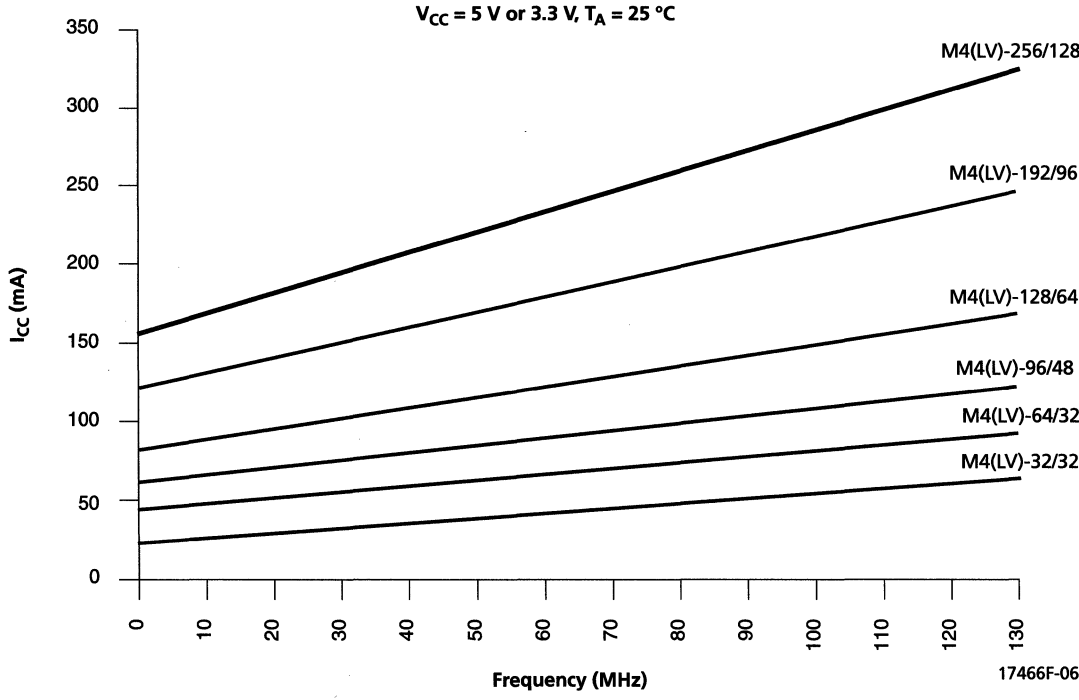


Figure 16. I_{CC} Curves at High Power Mode

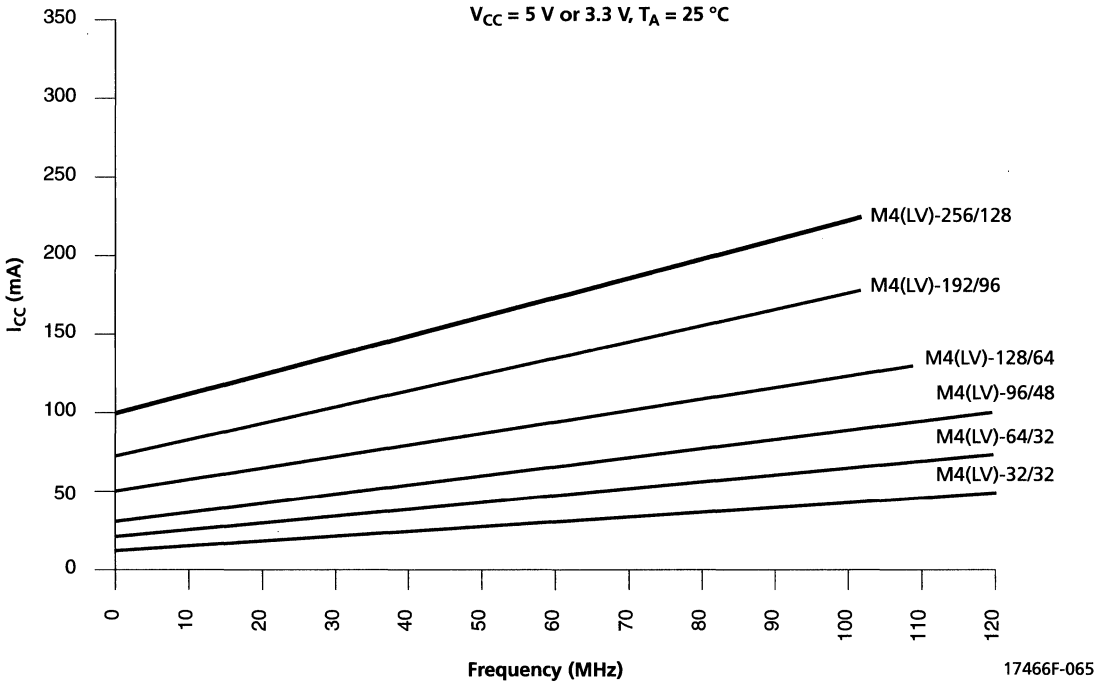
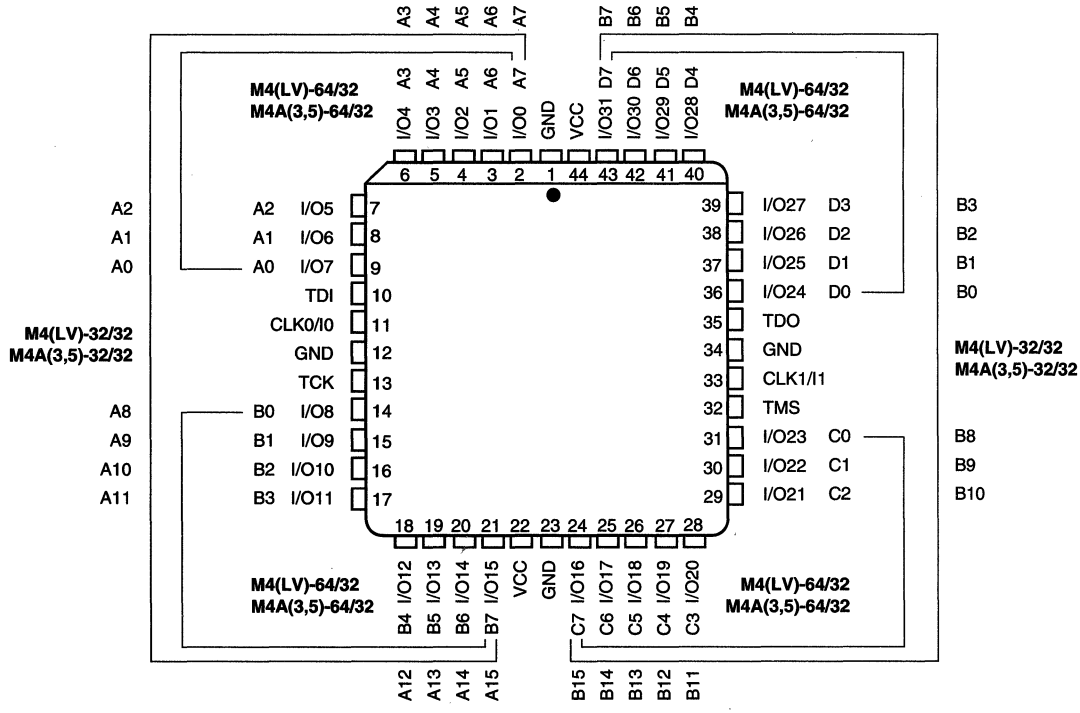


Figure 17. I_{CC} Curves at Low Power Mode

CONNECTION DIAGRAM (M4(LV)-32/32, M4A(3,5)-32/32, M4(LV)-64/32 AND M4A(3,5)-64/32)

Top View

44-Pin PLCC



17466F-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

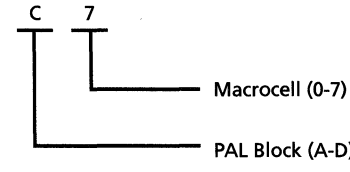
V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

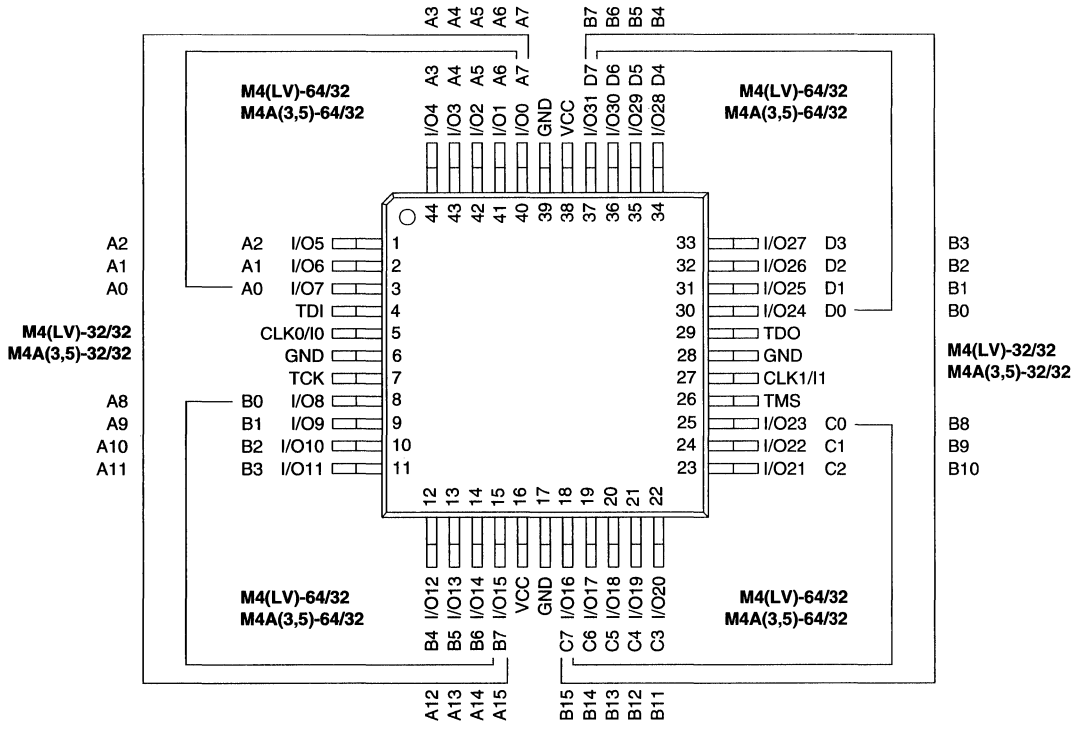
TDO = Test Data Out



CONNECTION DIAGRAM (M4(LV)-32/32, M4A(3,5)-32/32, M4(LV)-64/32 AND M4A(3,5)-64/32)

Top View

44-Pin TQFP



17466F-027

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

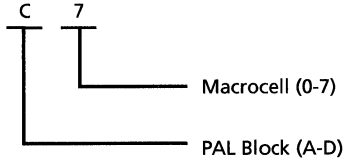
V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

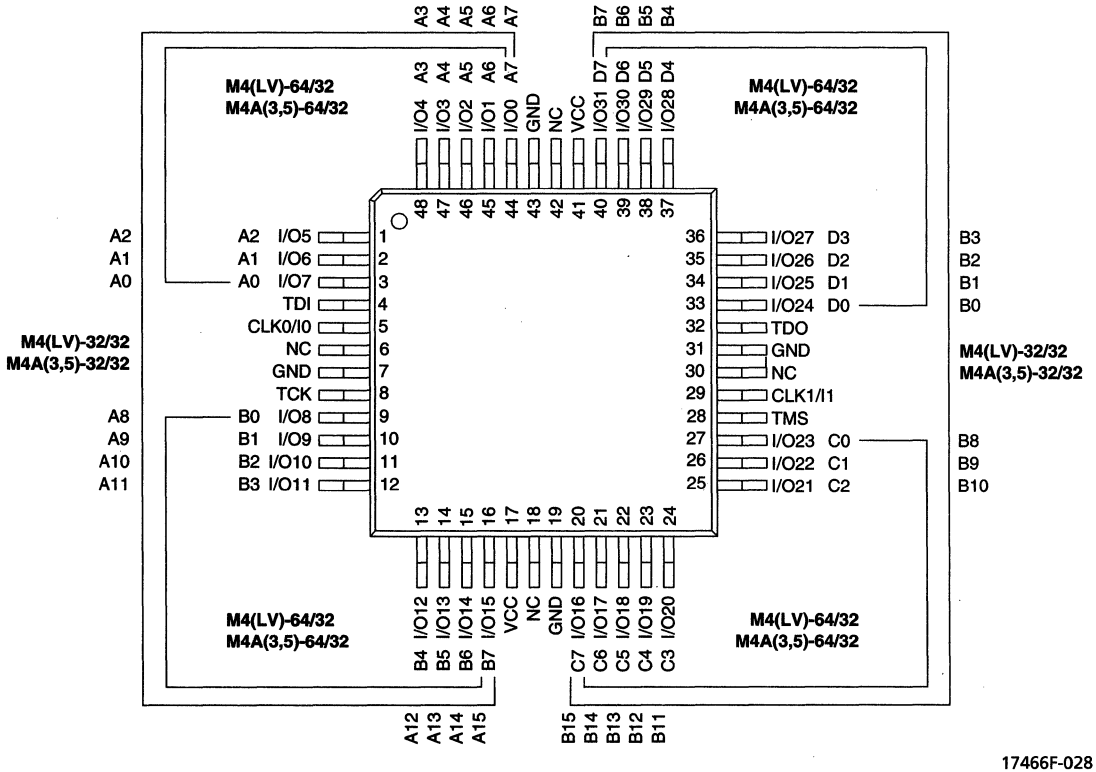
TDO = Test Data Out



CONNECTION DIAGRAM (M4(LV)-32/32, M4A(3,5)-32/32, M4(LV)-64/32 AND M4A(3,5)-64/32)

Top View

48-Pin TQFP



17466F-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

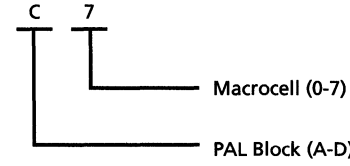
NC = No Connect

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

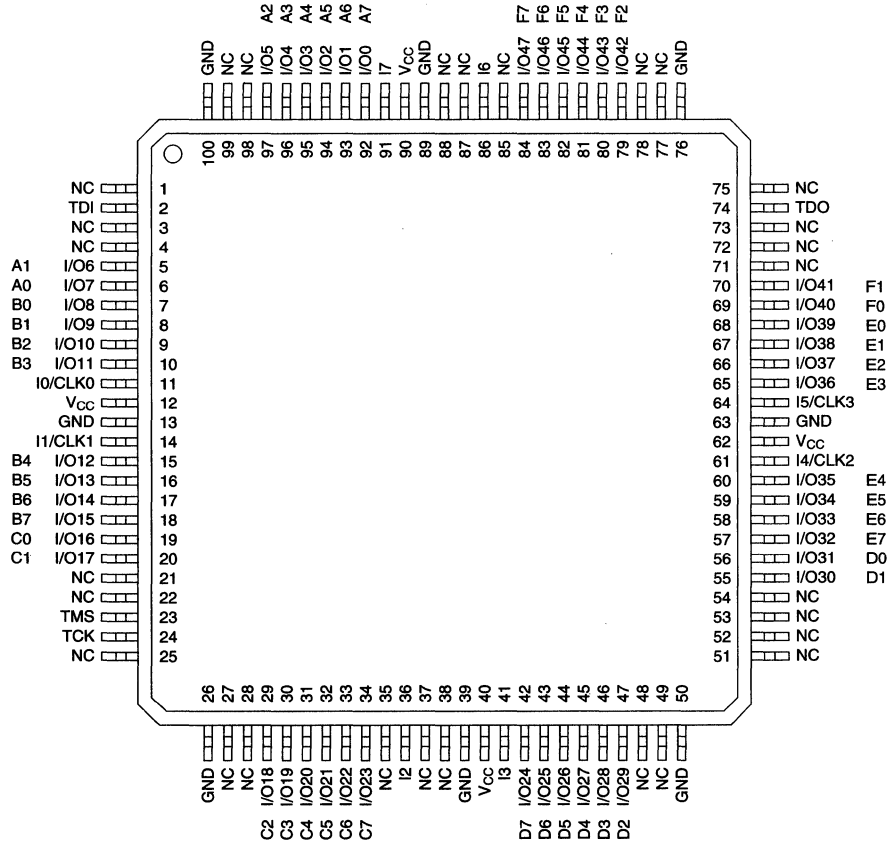
TDO = Test Data Out



CONNECTION DIAGRAM (M4(LV)-96/48 AND M4A(3,5)-96/48)

Top View

100-Pin TQFP



17466F-029

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

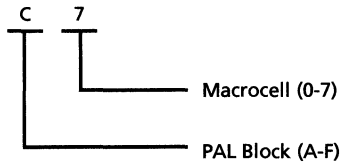
NC = No Connect

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

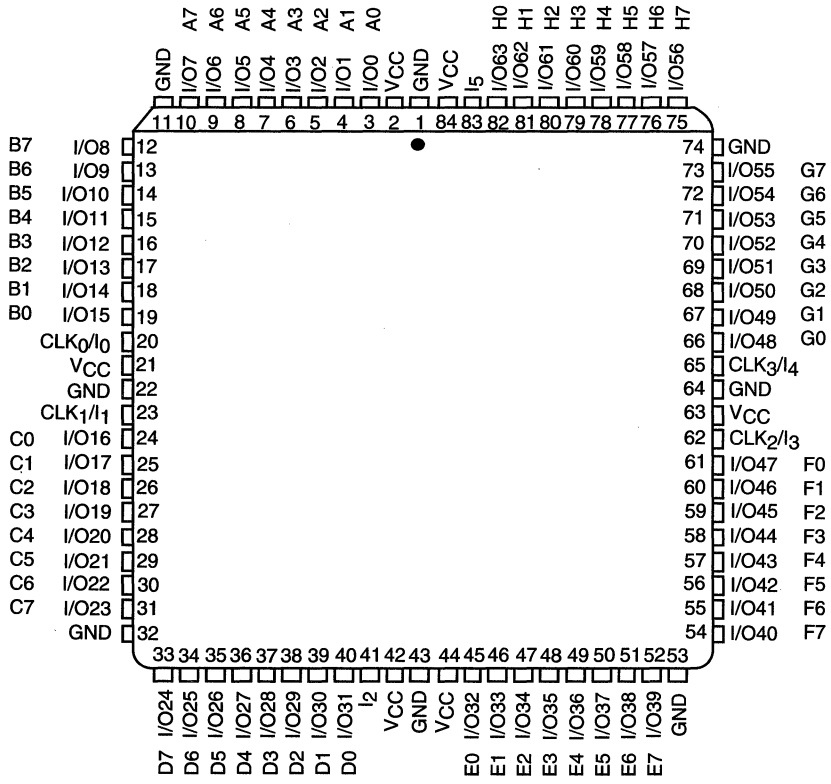
TDO = Test Data Out



CONNECTION DIAGRAM (M4(LV)-128N/64)

Top View

84-Pin PLCC



17466F-030

Note:
Pin-compatible with the MACH131, MACH231, MACH435.

PIN DESIGNATIONS

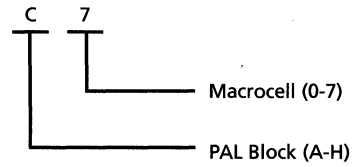
CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

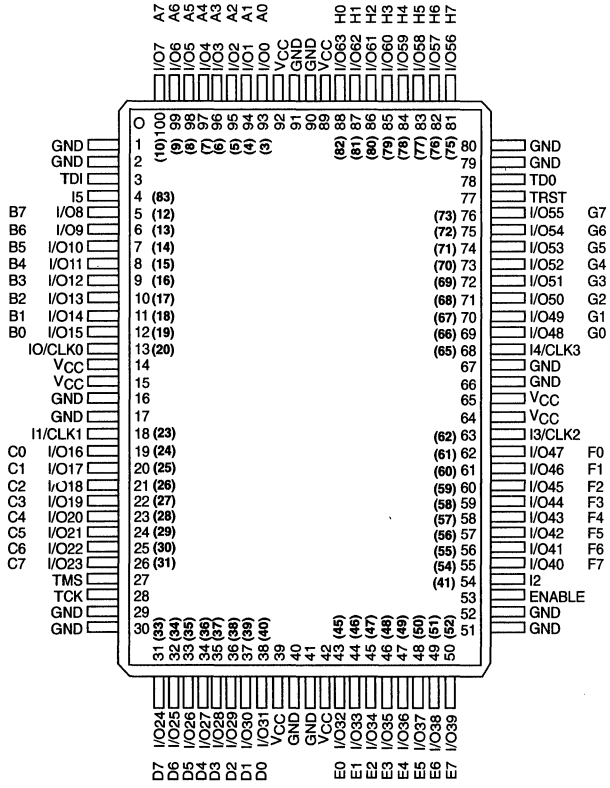
V_{CC} = Supply Voltage



CONNECTION DIAGRAM (M4(LV)-128/64 AND M4A(3,5)-128/64)

Top View

100-Pin PQFP

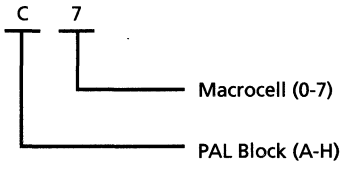


17466F-031

Note:
The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

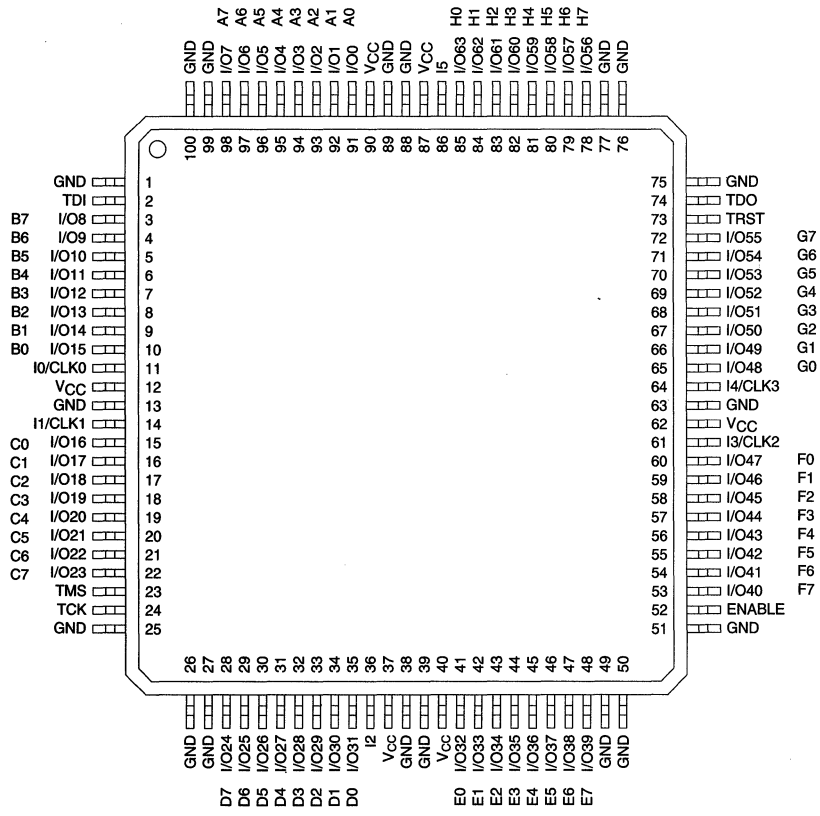
I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program



CONNECTION DIAGRAM (M4(LV)-128/64 AND M4A(3,5)-128/64)

Top View

100-Pin TQFP



17466F-032

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

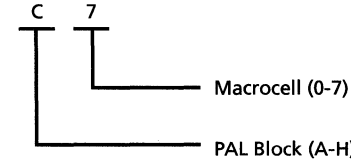
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

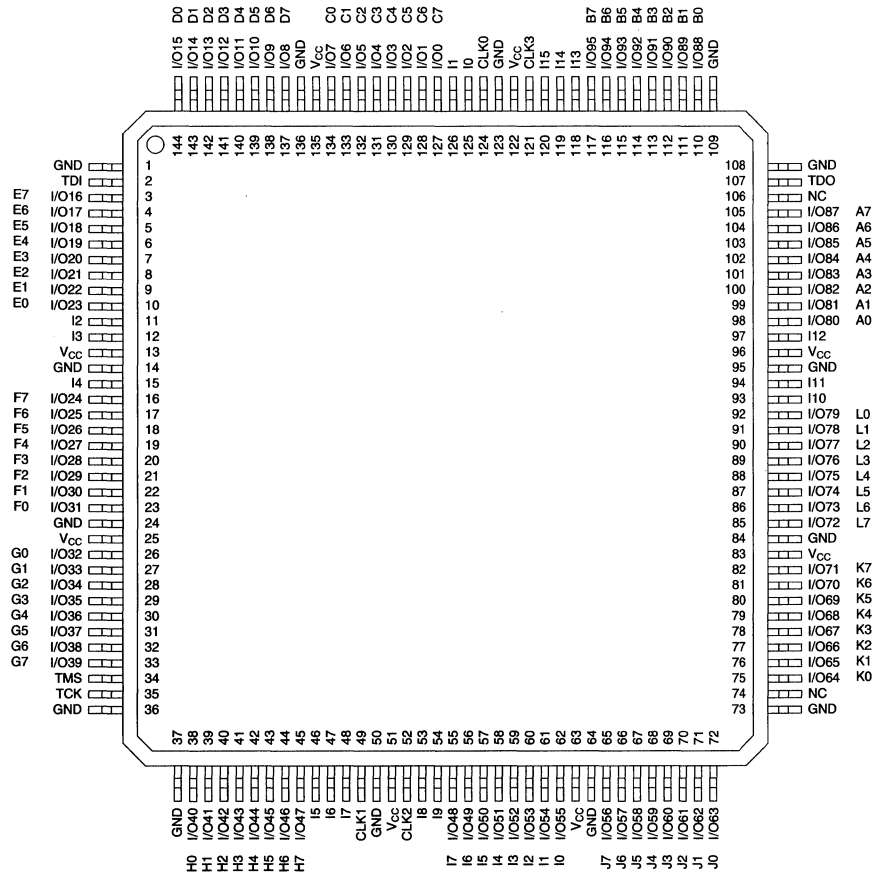
ENABLE = Program



CONNECTION DIAGRAM (M4(LV)-192/96 AND M4A(3,5)-192/96)

Top View

144-Pin TQFP



17466F-033

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

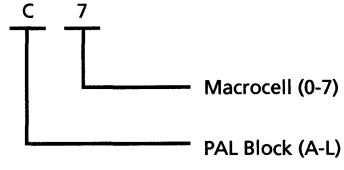
V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

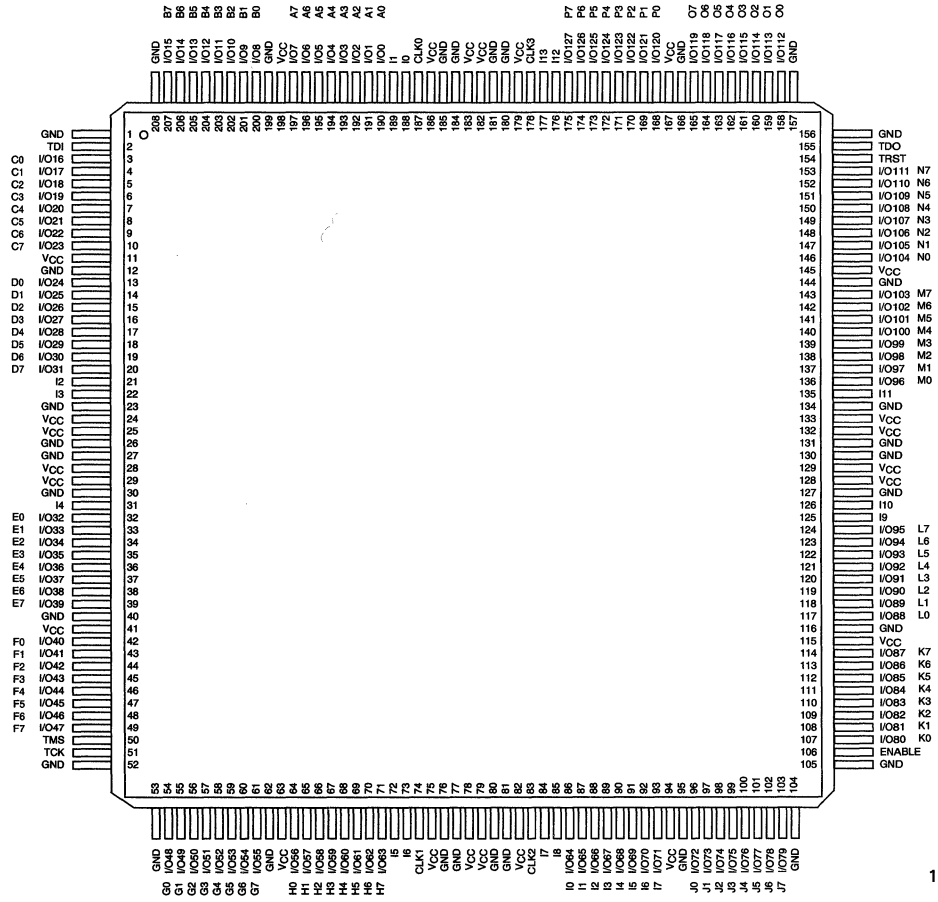
TDO = Test Data Out



CONNECTION DIAGRAM (M4(LV)-256/128 AND M4A(3,5)-256/128)

Top View

208-Pin PQFP



17466F-034

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

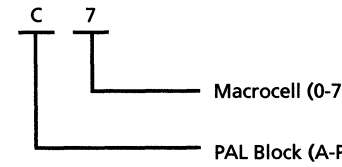
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

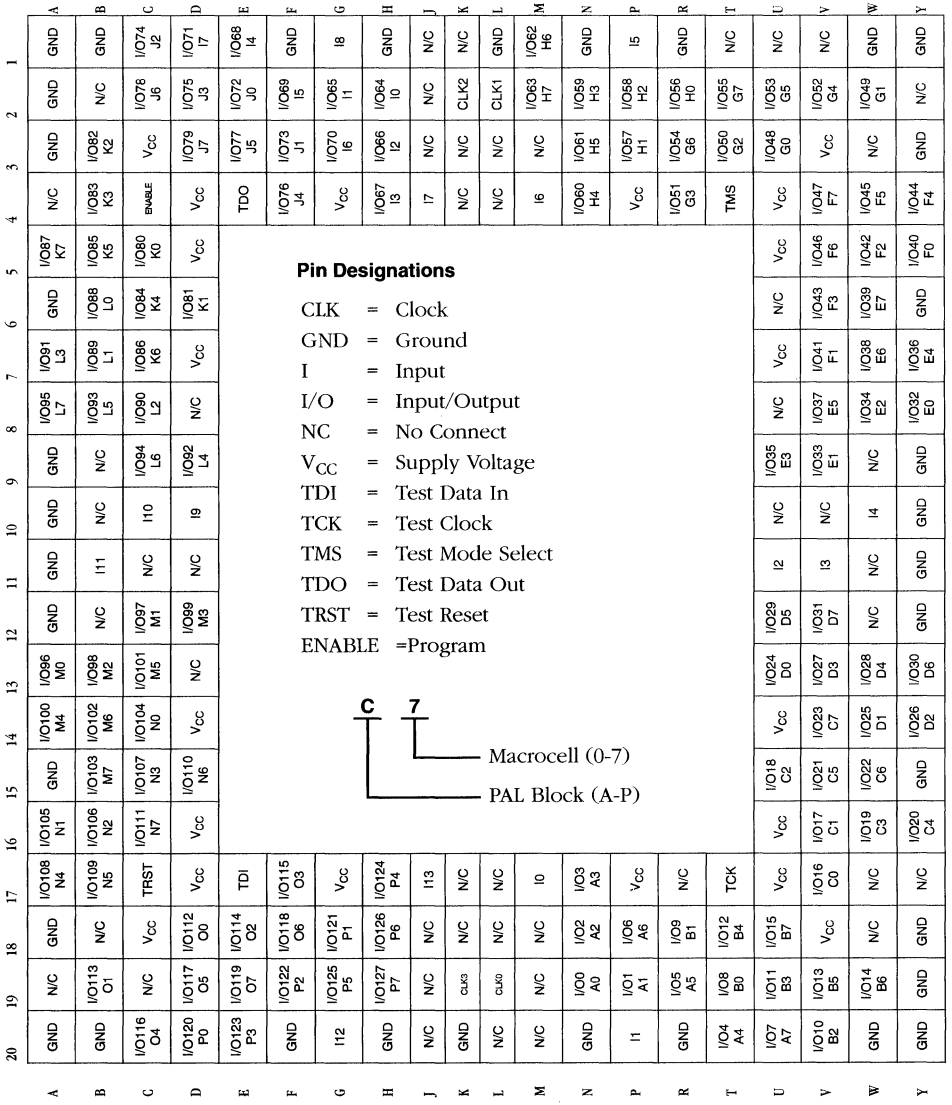
ENABLE= Program



CONNECTION DIAGRAM (M4(LV)-256/128 AND M4A(3,5)-256/128)

Bottom View

256-Pin BGA

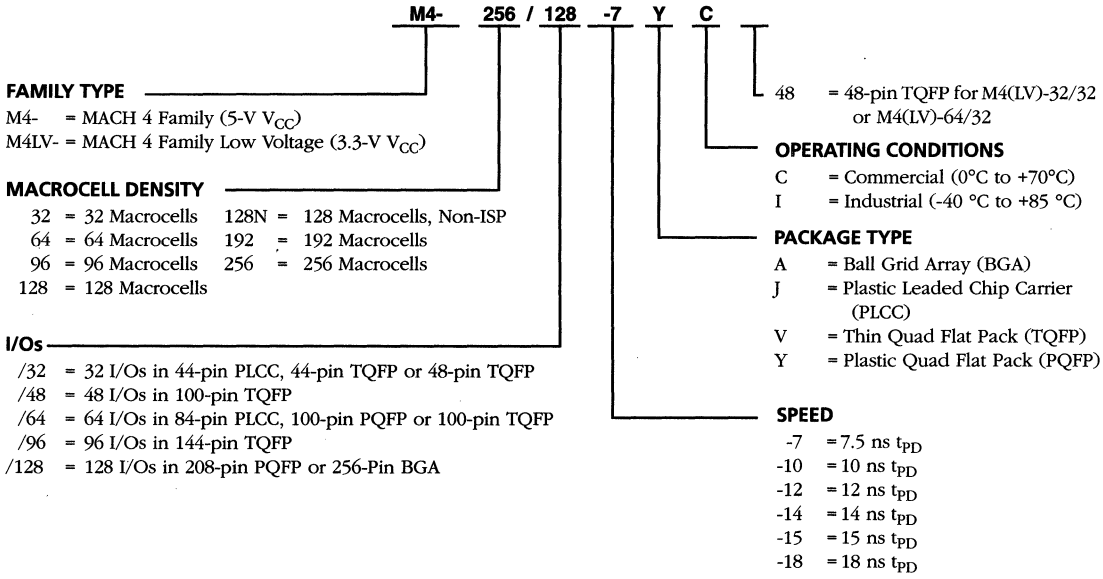


17466F-035

PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC, AC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JI, VI, VI48
M4LV-32/32		JI, VI, VI48
M4-64/32		JI, VI, VI48
M4LV-64/32		JI, VI, VI48
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JI
M4LV-128N/64		JI
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI, AI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT ORDERING INFORMATION

MACH 4A Devices Commercial and Industrial - 3.3V and 5V

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C

FAMILY TYPE

M4A3- = MACH 4 Family Low Voltage Advanced Feature (3.3-V V_{CC})
M4A5- = MACH 4 Family Advanced Feature (5-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 100-pin TQFP or 100-pin PQFP
/96 = 96 I/Os in 144-pin TQFP
/128 = 128 I/Os in 208-pin PQFP or 256-Pin BGA

SPEED

-50 = 5.0 ns t_{PD}
-55 = 5.5 ns t_{PD}
-60 = 6.0 ns t_{PD}
-65 = 6.5 ns t_{PD}
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}

PACKAGE TYPE

A = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40 °C to +85 °C)

48 = 48-pin TQFP for M4A3-32/32 or M4A3-64/32 M4A5-32/32 or M4A5-64/32

Valid Combinations		
M4A3-32/32	-50, -55, -60, -65, -7, -10, -12	JC, VC, VC48
M4A5-32/32		JC, VC, VC48
M4A3-64/32		JC, VC, VC48
M4A5-64/32		JC, VC, VC48
M4A3-96/48		VC
M4A5-96/48		VC
M4A3-128/64		YC, VC
M4A5-128/64		YC, VC
M4A3-192/96		VC
M4A5-192/96		VC
M4A3-256/128		YC, AC
M4A5-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

Valid Combinations		
M4A3-32/32	-7, -10, -12, -14	JI, VI, VI48
M4A5-32/32		JI, VI, VI48
M4A3-64/32		JI, VI, VI48
M4A5-64/32		JI, VI, VI48
M4A3-96/48		VI
M4A5-96/48		VI
M4A3-128/64		YI, VI
M4A5-128/64		YI, VI
M4A3-192/96		VI
M4A5-192/96		VI
M4A3-256/128		YI, AI
M4A5-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

VANTIS

BEYOND PERFORMANCE

MACH 5 CPLD Family

Fifth Generation MACH Architecture

Includes MACH 5A Family Advance Information

FEATURES

- **High logic densities and I/Os for increased logic integration**
  - 128 to 512 macrocell densities
  - 68 to 256 I/Os
- **Wide selection of density and I/O combinations to support most application needs**
  - 6 macrocell density options
  - 8 I/O options
  - Up to 5 I/O options per macrocell density
  - Up to 6 density & I/O options for each package
- **Performance features to fit system needs**
  - 5.5 ns t_{PD} Commercial, 7.5 ns t_{PD} Industrial
  - 182 MHz f_{CNT}
  - Four programmable power/speed settings per block
- **Flexible architecture facilitates logic design**
  - Multiple levels of switch matrices allow for performance-based routing
  - 100% routability and pin-out retention
  - Synchronous and asynchronous clocking, including dual-edge clocking
  - Asynchronous product- or sum-term set or reset
  - 16 to 64 output enables
  - Functions of up to 32 product terms
- **Advanced capabilities for easy system integration**
  - 3.3-V & 5-V JEDEC-compliant operations
  - JTAG (IEEE 1149.1) compliant for boundary scan testing
  - 3.3-V & 5-V JTAG in-system programming
  - PCI compliant (-5/-6/-7/-10/-12 speed grades)
  - Safe for mixed supply voltage system design
  - Programmable pull-up or Bus-Friendly™ Inputs & I/Os
  - Individual output slew rate control
  - Hot socketing
  - Programmable security bit
- **Advanced EE CMOS process provides high performance, cost effective solutions**
- **Supported by Vantis DesignDirect™ software for rapid logic development**
  - Supports HDL design methodologies with results optimized for Vantis
  - Flexibility to adapt to user requirements
  - Software partnerships that ensure customer success
- **Vantis and Third-party hardware programming support**
  - VantisPRO™ (formerly known as MACHPRO®) software for in-system programmability support on PCs and Automated Test Equipment
  - Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

Publication# **20446** Rev: **G**
Amendment/**0** Issue Date: **November 1998**

Table 1. MACH 5 Device Features [1]

Feature	M5-128 M5LV-128		M5-192	M5-256 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	160	160	160	192	192	192	192	256	256
t_{PD} (ns)	7.5	5.5	7.5	7.5	5.5	7.5	7.5	7.5	7.5	7.5	7.5
t_{SS} (ns)	4.0	3.0	4.0	4.0	3.0	4.0	4.0	4.0	4.0	4.0	4.0
t_{COS} (ns)	6.0	4.5	6.0	6.0	4.5	6.0	6.0	6.0	6.0	6.0	6.0
f_{CNT} (MHz)	125	182	125	125	182	125	125	125	125	125	125
Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
JTAG-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

Table 2. MACH 5A Device Features [1,2]

Feature	M5A3-128 M5A5-128		M5A3-192 M5A5-192		M5A3-256 M5A5-256		M5A3-320	M5A3-384	M5A3-512
Supply Voltage (V)	3.3	5	3.3	5	3.3	5	3.3	3.3	3.3
Macrocells	128	128	192	192	256	256	320	384	512
Maximum User I/O Pins	120	120	120	120	160	160	192	192	256
t_{PD} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
t_{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t_{COS} (ns)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
f_{CNT} (MHz)	182	182	182	182	182	182	182	182	182
Static Power (mA)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
JTAG-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

2. "M5A5-xxx" is for 5-V devices "M5A3-xxx" is for 3.3-V devices.

GENERAL DESCRIPTION

The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, JTAG testability, and advanced clocking options (Tables 1 and 2). Both the MACH 5 and the MACH 5A families offer 5-V (M5-xxx and M5A5-xxx) and 3.3-V (M5LV-xxx and M5A3-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on EECMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Tables 3 and 4). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification.*

Table 3. MACH 5 Speed Grades

Device	Speed Grade[1]					
	-5	-7	-10	-12	-15	-20
M5-128		C	C, I	C, I	C, I	I
M5LV-128	C	C,I	C, I	C, I	I	
M5-192		C	C, I	C, I	C, I	I
M5-256		C	C, I	C, I	C, I	I
M5LV-256	C	C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	I

Note:

1. C = Commercial grade, I = Industrial grade

Table 4. MACH 5A Speed Grades

Device	Speed Grade[1]					
	-5	-6	-7	-10	-12	-15
M5A3-128	C		C, I	C, I	C, I	I
M5A5-128	C		C, I	C, I	C, I	I
M5A3-192	C		C, I	C, I	C, I	I
M5A5-192	C		C, I	C, I	C, I	I
M5A3-256	C		C, I	C, I	C, I	I
M5A5-256	C		C, I	C, I	C, I	I
M5A3-320	C (Note 2)	C (Note 2)	C, I (Note 2)	C, I	C, I	I
M5A3-384	C (Note 2)	C (Note 2)	C, I (Note 2)	C, I	C, I	I
M5A3-512	C (Note 2)	C (Note 2)	C, I (Note 2)	C, I	C, I	I

Notes:

1. C = Commercial grade, I = Industrial grade. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

2. The –5 and –6 commercial and –7 industrial speed grades are under development for M5A3-320, M5A3-384, and M5A3-512. Please contact a Vantis sales representative for details on availability.

With Vantis' unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL® block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Vantis offers several I/O and package options to meet a wide range of design needs (Tables 5 and 6).

Table 5. MACH 5 Package and I/O Options [1]

Package	M5-128 M5LV-128	M5-192	M5-256 M5LV-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
100-pin TQFP	68, 74*	68	68, 74*			
100-pin PQFP	68	68	68			
144-pin TQFP	104*		104*			
144-pin PQFP	104	104	104			
160-pin PQFP	120	120	120	120	120	120
208-pin PQFP		160	160	160	160	160
240-pin PQFP				184	184	184
256-pin BGA				192	192	192
352-pin BGA						256

Note:

1. The I/O options indicated with a "" are only available for the "LV" devices.*

Table 6. MACH 5A Package and I/O Options[1]

Package	M5A3-128 M5A5-128	M5A3-192 M5A5-192	M5A3-256 M5A5-256	M5A3-320	M5A3-384	M5A3-512
100-pin PQFP	68	68	68			
100-pin TQFP	74	74	74			
144-pin TQFP	104	104	104			
160-pin PQFP	120	120	120	120	120	120
208-pin PQFP			160	160	160	160
256-pin BGA				192	192	192
352-pin BGA						256

Note:

1. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design, and both the 3.3-V and the 5-V device versions are in-system programmable through a JTAG-compliant interface.

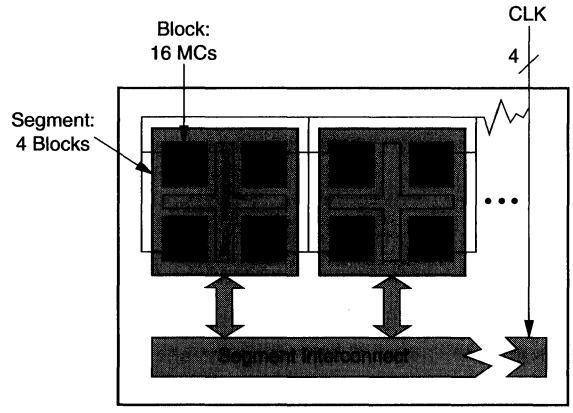
Vantis offers software design support for MACH devices in both the MACHXL® and DesignDirect development systems. The DesignDirect development system is the Vantis implementation software that includes support for all Vantis CPLD, FPGA and SPLD devices. This system is supported under Windows '95, '98 and NT as well as Sun Solaris and HPUX.

DesignDirect software is designed for use with design entry, simulation and verification software from leading-edge tool vendors such as Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys, Synplicity, Viewlogic and others. It accepts EDIF 2 0 0 input netlists, generates JEDEC files for Vantis PLDs and creates industry standard EDIF, Verilog, VITAL compliant VHDL and SDF simulation netlists for design verification.

DesignDirect software is also available in product configurations that include VHDL and Verilog synthesis from Exemplar Logic and VHDL, Verilog RTL and gate level timing simulation from Model Technology. Schematic capture and ABEL entry, as well as functional simulation, are also provided.

FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect (Figure 1). The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



20446G-001

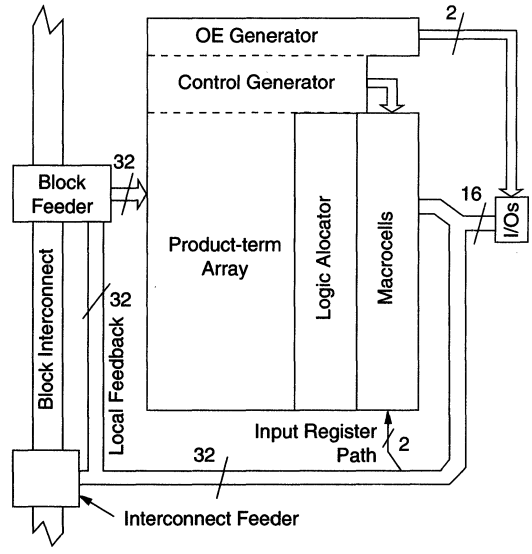
Figure 1. MACH 5 Block Diagram

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- I/O cells
- Product-term array and Logic Allocator
- Macrocells
- Register control generator
- Output enable generator

I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.



20446G-002

Figure 2. PAL Block Structure

PRODUCT-TERM ARRAY AND LOGIC ALLOCATOR

The product-term array uses the same sum-of-products architecture as Vantis' PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 of 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 7). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 7. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M_0	C_0, C_1, C_2, C_3, C_4	M_8	$C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}$
M_1	$C_0, C_1, C_2, C_3, C_4, C_5$	M_9	$C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}$
M_2	$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	M_{10}	$C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}$
M_3	$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	M_{11}	$C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_4	$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	M_{12}	$C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_5	$C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8$	M_{13}	$C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_6	$C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9$	M_{14}	$C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_7	$C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}$	M_{15}	$C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as "buried" macrocells to drive device logic via the matrix.

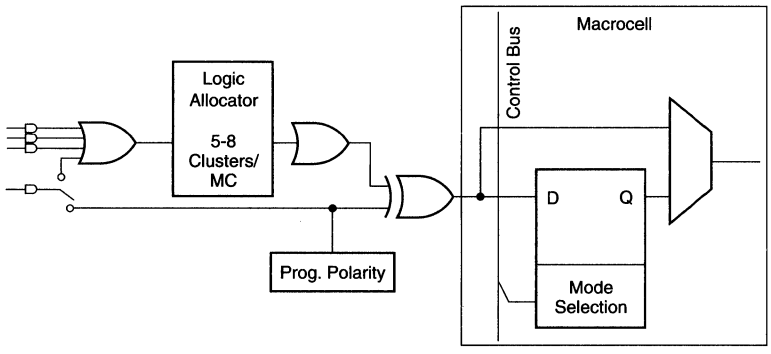


Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 1 Options

- Global clock (0, 1, 2, or 3) with positive edge clock enable

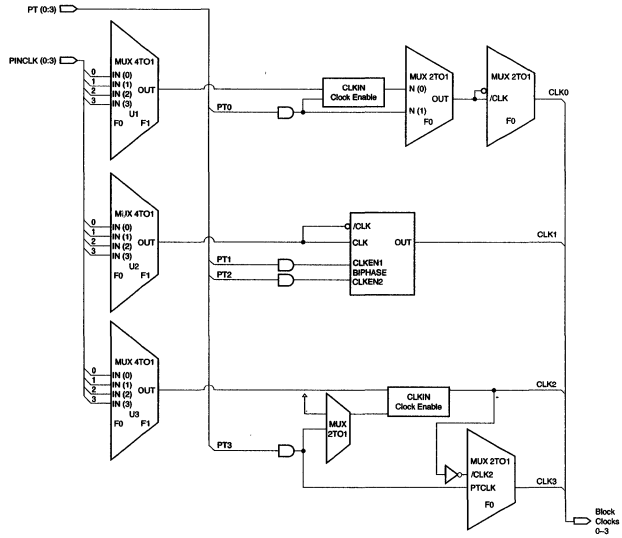
- Global clock (0, 1, 2, or 3) with negative edge clock enable
- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- Global clock (0, 1, 2, or 3) with clock enable

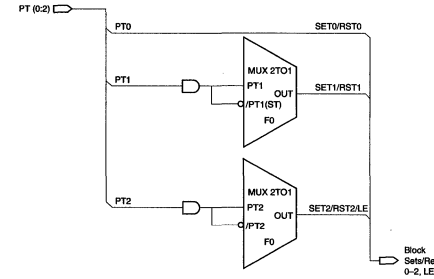
Clock Line 3 Options

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable



20446G-004

Figure 4. Clock Generator



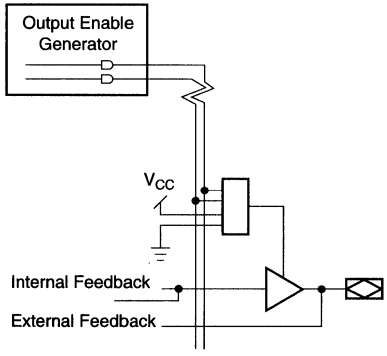
20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).



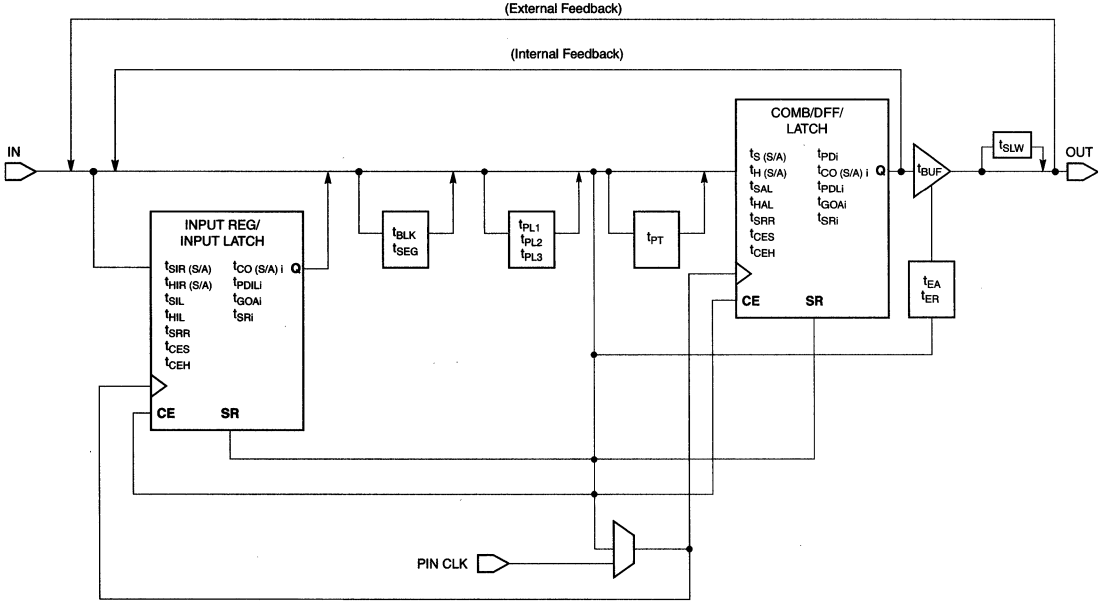
20446G-006

Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



20446G-014

Figure 7. MACH 5 Timing Model

MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

JTAG BOUNDARY SCAN TESTABILITY

All MACH 5 devices have JTAG boundary scan cells and are compliant to the JTAG standard, IEEE 1149.1. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

JTAG IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their JTAG ports. This capability has been implemented in a manner that insures that the JTAG port remains compliant to the IEEE 1149.1 standard. By using JTAG as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. Vantis provides its free PC-based VantisPRO software to facilitate in-system programming. VantisPRO software takes the JEDEC file output produced by Vantis' design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. VantisPRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, VantisPRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board. For more information about in-system programming, refer to the separate document entitled *MACH ISP Manual.*

PCI COMPLIANT

MACH 5(A) devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS [1]

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:
1. Except for M5-128, M5-192, and M5-256.

PULL-UP OR BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book. All MACH 5A devices have a programmable bit that configures all input and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/Os are weakly pulled up. For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 8). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 8. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

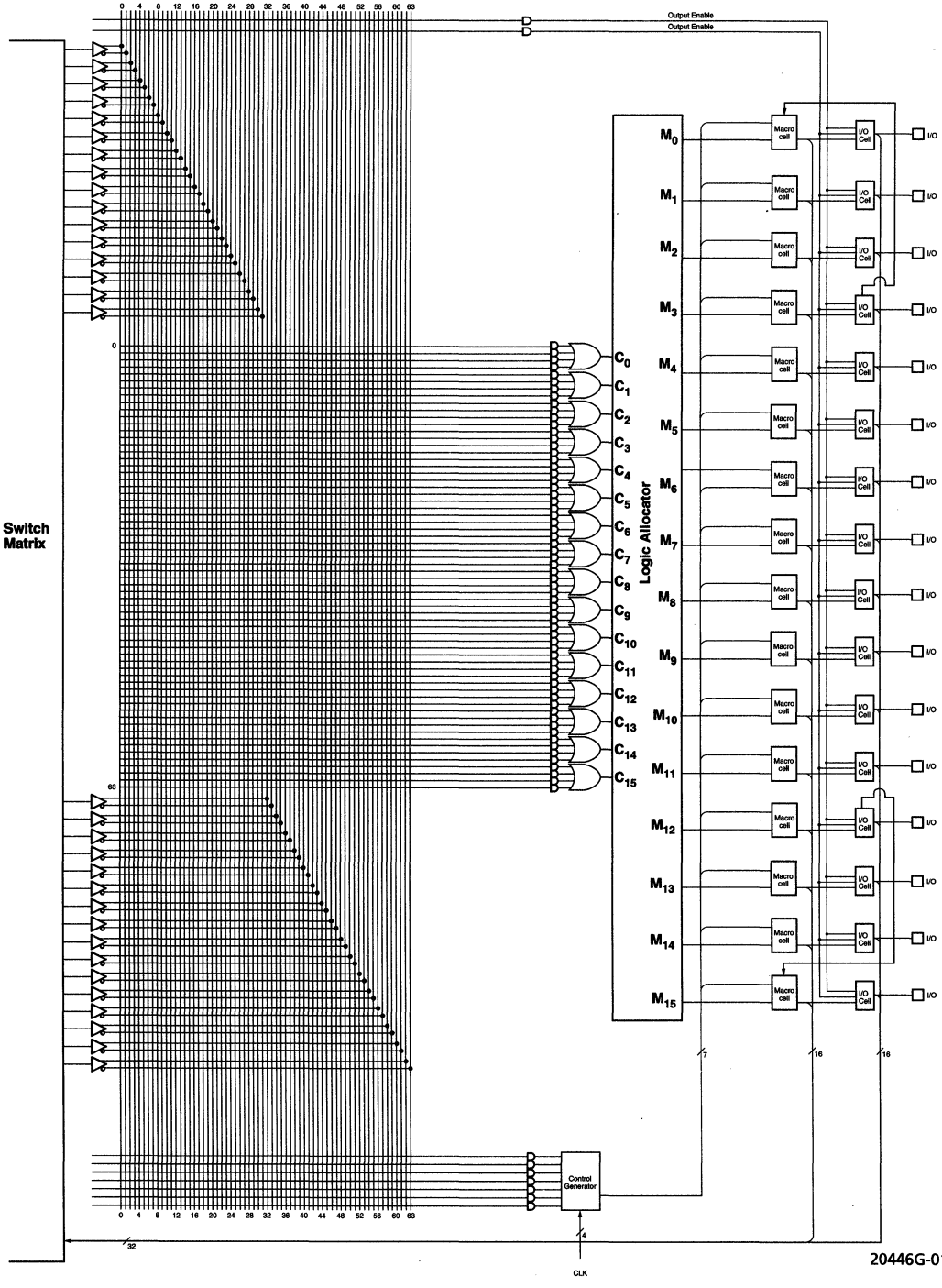
SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

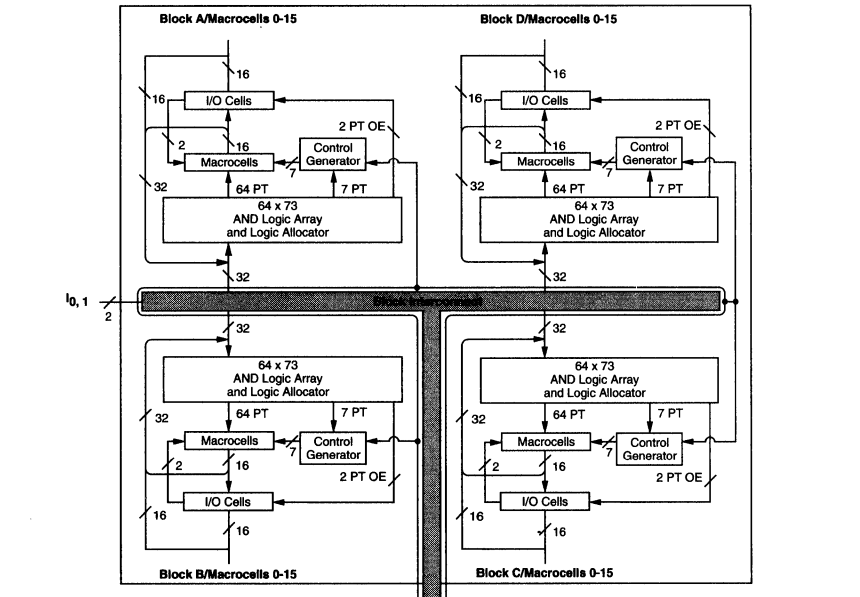
MACH 5A devices are well-suited for those applications that require hot socket capability. Hot socketing a device requires that the device, when powered-down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH device be minimal on active signals.

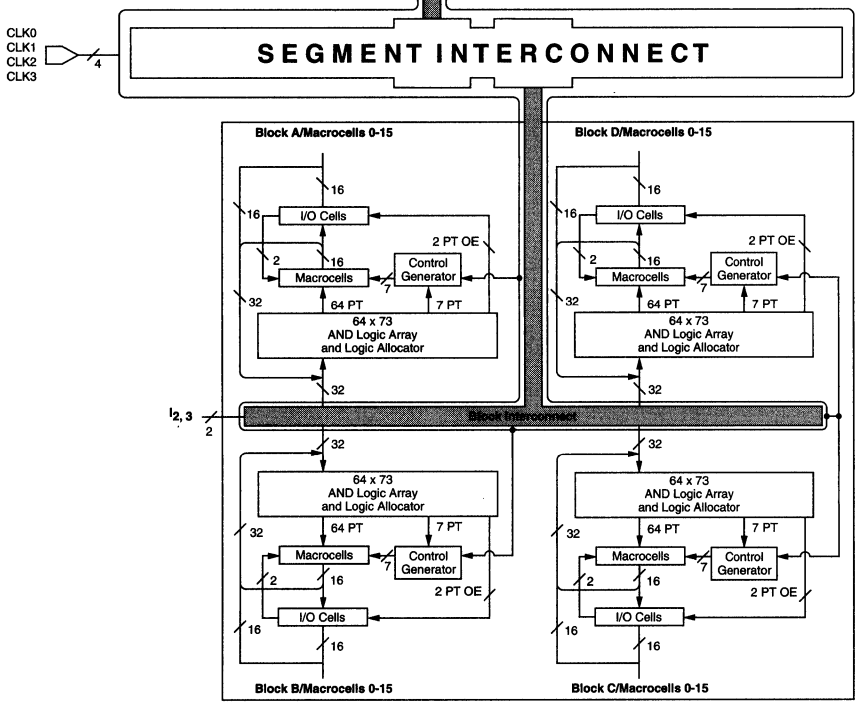
MACH 5 PAL BLOCK



BLOCK DIAGRAM — M5(LV)-128/XXX, M5A(3,5)-128/XXX

SEGMENT 0

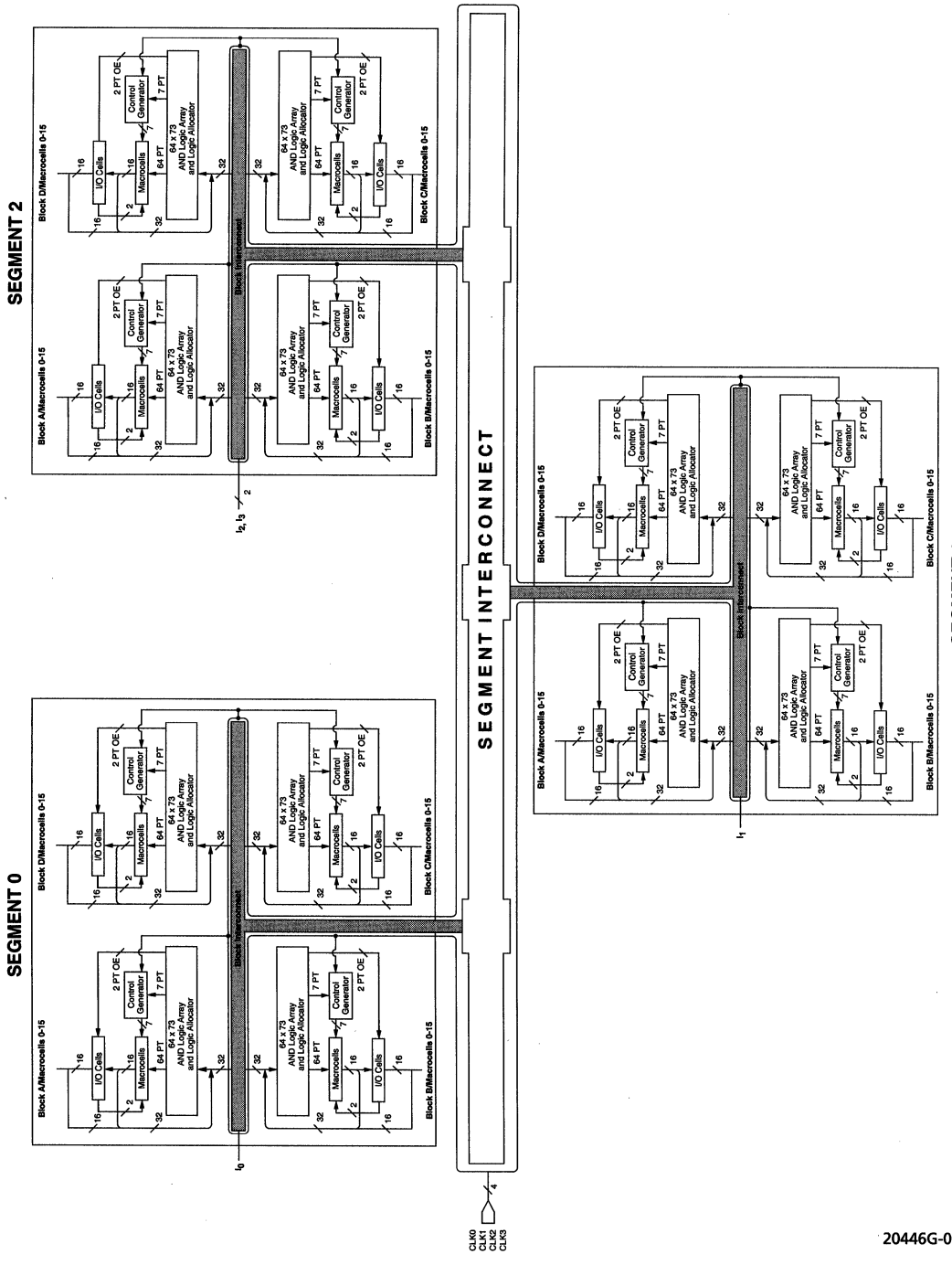




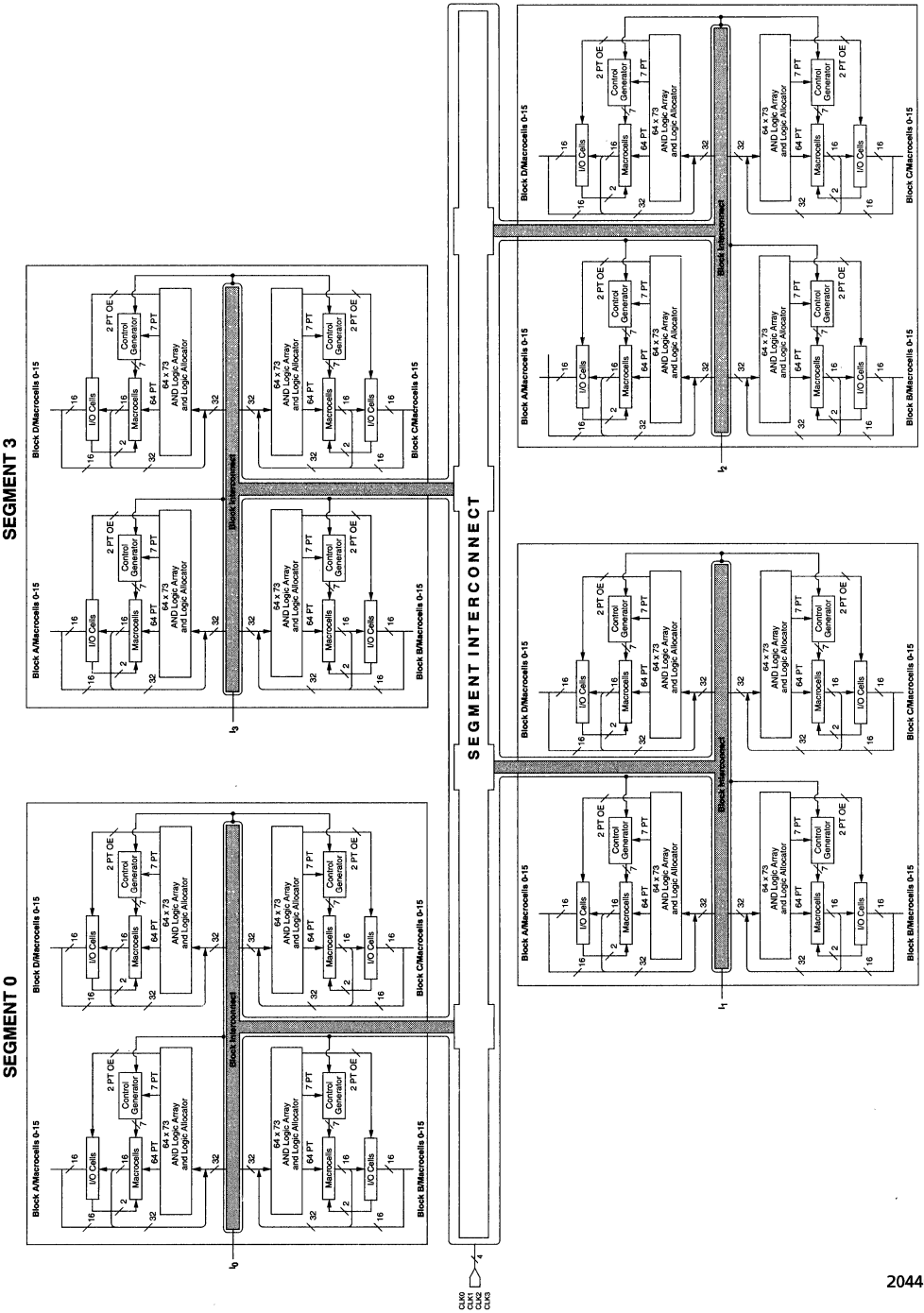
SEGMENT 1

20446G-007

BLOCK DIAGRAM — M5-192/XXX, M5A(3,5)-192/XXX

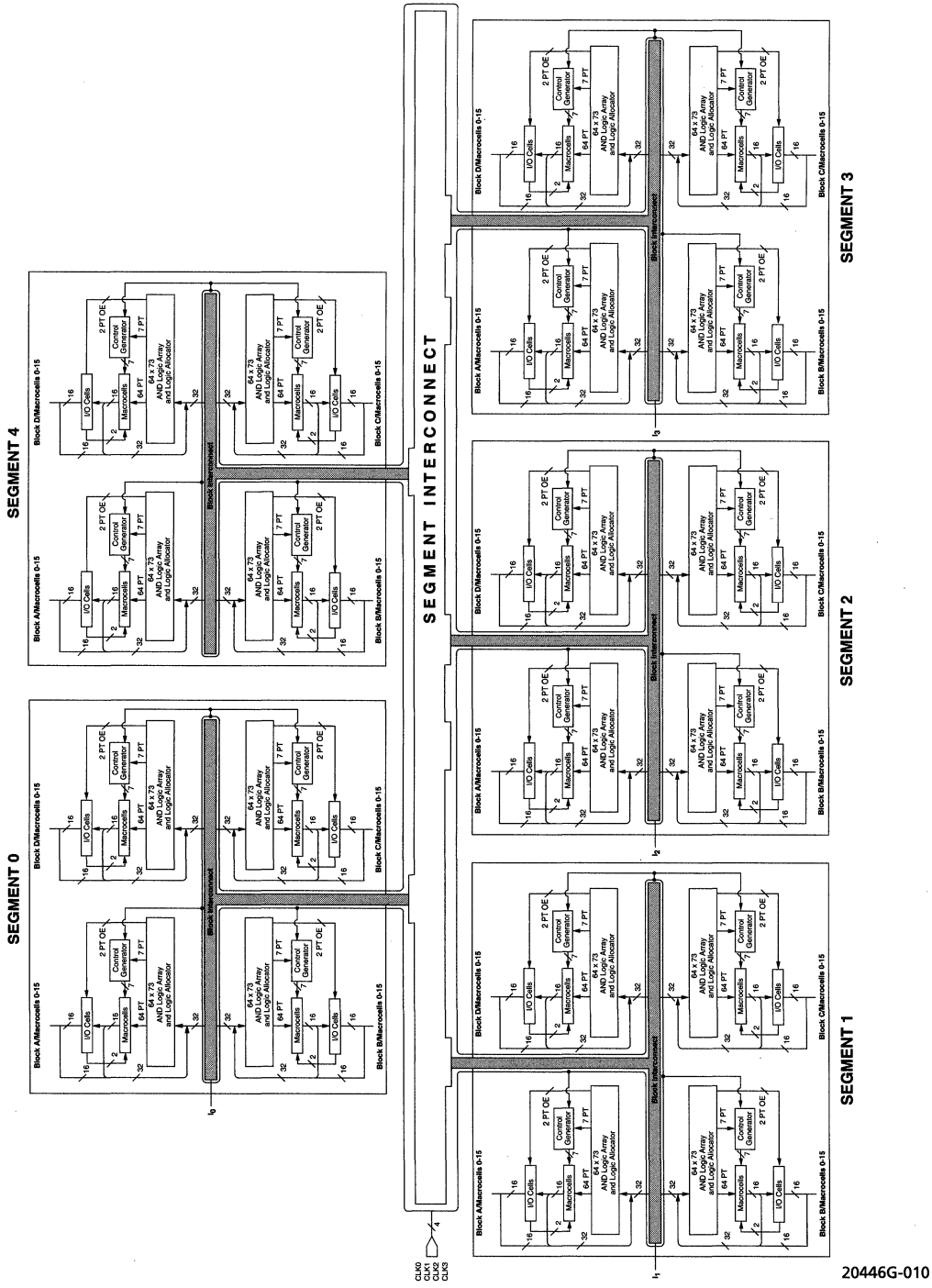


BLOCK DIAGRAM — M5(LV)-256/XXX, M5A(3,5)-256/XXX



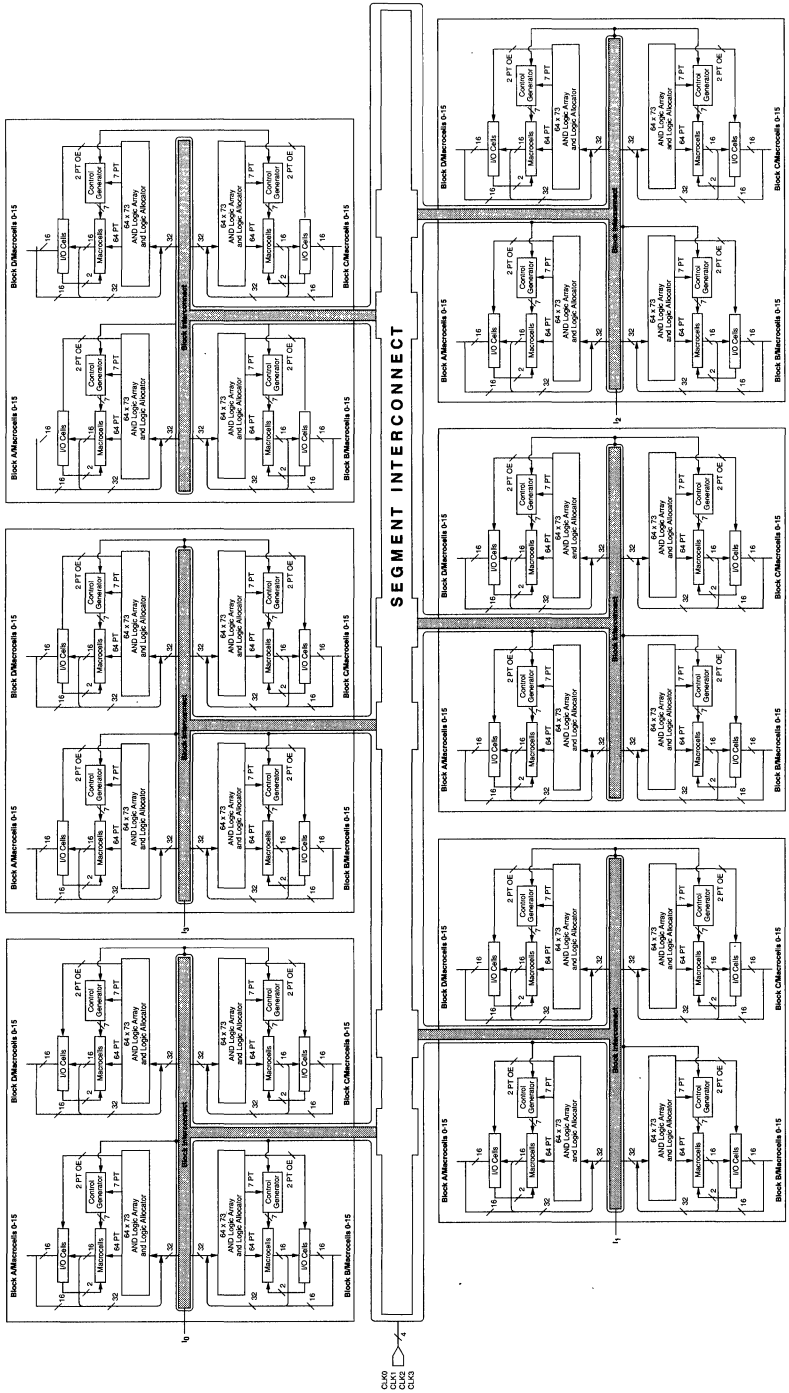
20446G-009

BLOCK DIAGRAM — M5(LV)-320/XXX, M5A3-320/XXX



20446G-010

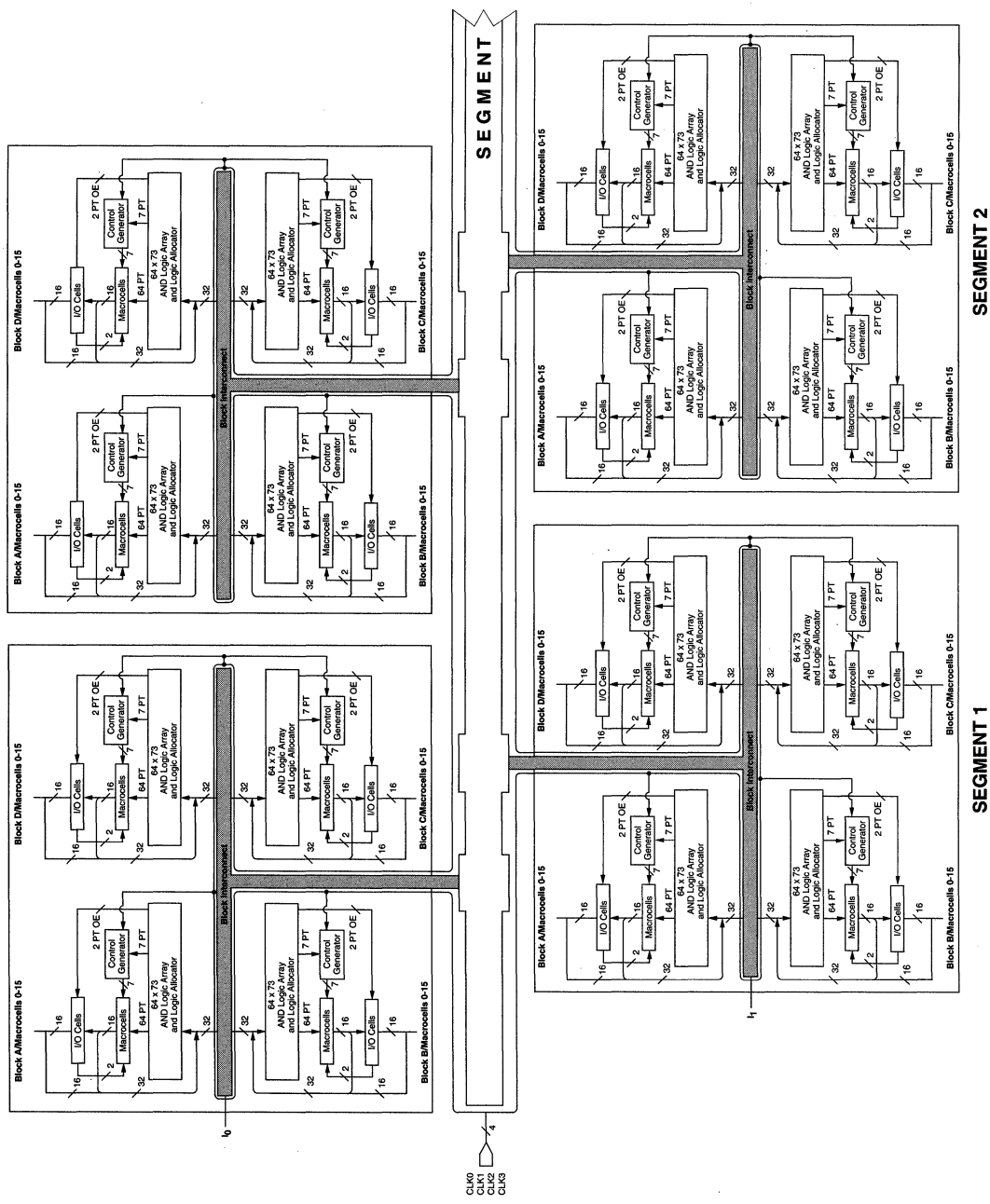
BLOCK DIAGRAM — M5(LV)-384/XXX, M5A3-384/XXX



20446G-011

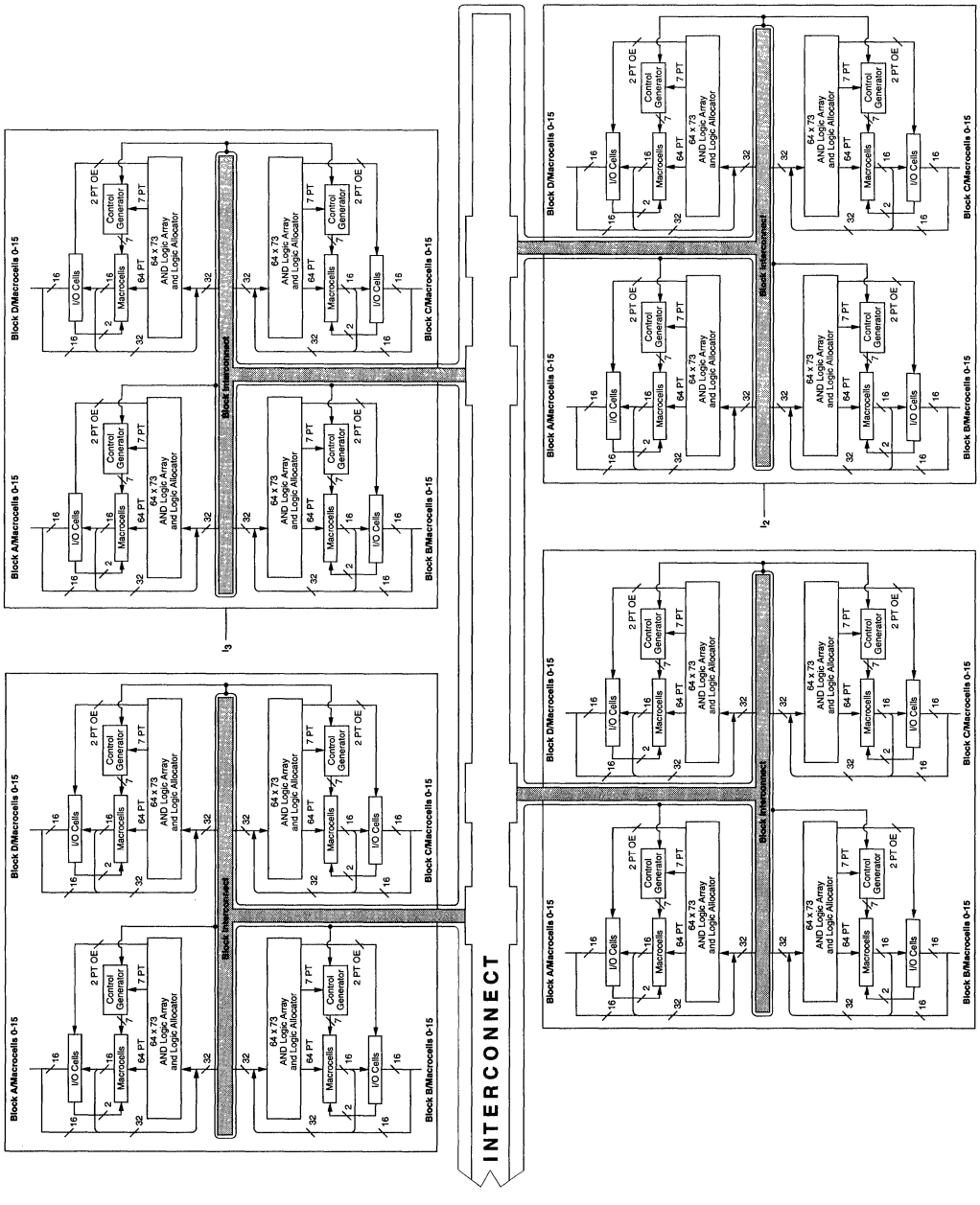
BLOCK DIAGRAM — M5(LV)-512/XXX, M5A3-512/XXX

Continued



20446G-012

BLOCK DIAGRAM — M5(LV)-512/XXX, M5A3-512/XXX



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20446G-013

ABSOLUTE MAXIMUM RATINGS

M5 and M5A5

Storage Temperature . . . . . -65°C to +150°C

Device Junction
Temperature (Note 1) . . . . . +130°C or +150°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-320, M5-384, M5-512, M5A5-128, M5A5-192, M5A5-256 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = -2.5 mA, V_{CC} = 5.25 V, V_{IN} = V_{IH} or V_{IL}			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 4)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 5)	-30		-180	mA

Note:

1. *150° for M5-128, M5-192 and M5-256 devices. 130° for M5-320, M5-384, M5-512 and all M5A5-xxx devices.*
2. *Total I_{OL} between ground pins should not exceed 64 mA.*
3. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
5. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*

ABSOLUTE MAXIMUM RATINGS

M5LV and M5A3

Storage Temperature . . . . . -65°C to +150°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4..5 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -100 µA	V_{CC} -0.2		V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = 3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 100 µA		0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = 16 mA (Note 1)		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		-15	-160	mA

Notes:

1. *Total I_{OL} between ground pins should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:														
t_{PDi}	Internal combinatorial propagation delay		3.5		5.5		8.0		10.0		13.0		18.0	ns
t_{PD}	Combinatorial propagation delay		5.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:														
t_{SS}	Synchronous clock setup time	3.0		4.0		5.0		6.0		8.0		10.0		ns
t_{SA}	Asynchronous clock setup time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		4.0		5.0		6.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		4.5		6.0		7.0		8.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		6.0		8.0		10.0		13.0		15.0		18.0	ns
t_{COA}	Asynchronous clock to output		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:														
t_{SAL}	Latch setup time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HAL}	Latch hold time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{PDLi}	Transparent latch internal		6.0		7.0		8.0		9.0		10.0		10.0	ns
t_{PDL}	Propagation delay through transparent latch		8.0		9.0		10.0		11.0		12.0		12.0	ns
t_{GOAi}	Gate to internal output		7.0		8.0		9.0		10.0		11.0		12.0	ns
t_{GOA}	Gate to output		9.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:														
t_{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		4.0		4.0		4.0		4.0		ns
t_{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:														
t_{SIL}	Input latch setup time	2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{HIL}	Input latch hold time	6.0		6.0		7.0		7.0		7.0		7.0		ns
t_{PDILi}	Transparent input latch		5.0		5.0		6.0		6.0		6.0		6.0	ns
Output Delays:														
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		9.5		10.0		12.0		15.0		20.0	ns
t_{ER}	Output disable time		7.5		9.5		10.0		12.0		15.0		20.0	ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Power Delays:														
t_{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t_{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t_{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:														
t_{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:														
t_{BLK}	Block interconnect delay		1.5		1.5		2.0		2.0		2.0		2.0	ns
t_{SEG}	Segment interconnect delay		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:														
t_{SRi}	Asynchronous reset or preset to internal register output		6.0		8.0		10.0		12.0		14.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		8.0		10.0		12.0		14.0		16.0		18.0	ns
t_{SRR}	Reset and set register recovery time	5.5		7.5		8.0		9.0		10.0		11.0		ns
t_{SRW}	Asynchronous reset or preset width	3.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:														
t_{CES}	Clock enable setup time	4.0		5.0		6.0		7.0		7.0		8.0		ns
t_{CEH}	Clock enable hold time	3.0		4.0		5.0		6.0		6.0		7.0		ns
Width:														
t_{WLS}	Global clock width low (Note 3)	2.5		3.0		4.0		5.0		6.0		6.0		ns
t_{WHS}	Global clock width high (Note 3)	2.5		3.0		4.0		5.0		6.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WHA}	Product term clock width high	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WIR}	Input register clock width low or high	3.0		4.0		5.0		6.0		7.0		8.0		ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:														
f_{MAX}	External feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{HS})$	200		167		125		100		83.3		83.3		MHz
f_{MAXA}	External feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{HA})$	167		125		100		83.3		71.4		62.5		MHz
f_{MAXI}	Maximum input register frequency $1/(t_{SIRS}+t_{HIRS})$ or $1/(2 \times t_{WICW})$	167		125		100		83.3		71.4		62.5		MHz

Notes:

1. *See "Switching Test Circuits" in the General Information Section of the Vantis 1999 Data Book.*
2. *Numbers in parentheses are for M5-128, M5-192, and M5-256.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).*

M5A(3,5) TIMING PARAMETERS OVER OPERATING RANGES [1]

		-5		-6		-7		-10		-12		-15		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:														
t_{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0	ns
t_{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0	ns
Registered Delays:														
t_{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		ns
t_{SA}	Asynchronous clock setup time	2.0		2.0		4.0		5.0		6.0		7.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	2.0		2.0		4.0		5.0		6.0		7.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0	ns
t_{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0	ns
t_{COAi}	Asynchronous clock to internal output		5.0		5.0		8.0		10.0		13.0		15.0	ns
t_{COA}	Asynchronous clock to output		7.0		7.0		10.0		12.0		15.0		17.0	ns
Latched Delays:														
t_{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		ns
t_{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		ns
t_{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0	ns
t_{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0	ns
t_{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0	ns
t_{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0	ns
Input Register Delays:														
t_{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		ns
t_{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		ns
Input Latch Delays:														
t_{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		ns
t_{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		ns
t_{PDILi}	Transparent input latch		5.0		5.0		5.0		6.0		6.0		6.0	ns
Output Delays:														
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		9.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		9.5		9.5		10.0		12.0		15.0	ns
Power Delays:														
t_{PL1}	Power level 1 delay		4.0		4.0		4.0		4.0		4.0		4.0	ns
t_{PL2}	Power level 2 delay		6.0		6.0		6.0		6.0		6.0		6.0	ns
t_{PL3}	Power level 3 delay		9.0		9.0		9.0		9.0		9.0		9.0	ns
Additional Cluster Delay:														
t_{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3	ns

M5A(3,5) TIMING PARAMETERS OVER OPERATING RANGES [1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Interconnect Delays:														
t_{BLK}	Block interconnect delay 320, 384 and 512 Macrocells		1.0		1.0		1.5		1.5		1.5		1.5	ns
t_{SEG}	Segment interconnect delay 320, 384, and 512 Macrocells		2.0		2.0		2.5		4.0		4.0		4.0	ns
t_{BLK}	Block interconnect delay 128, 192 and 256 Macrocells		1.5		1.5		1.5		1.5		1.5		1.5	ns
t_{SEG}	Segment interconnect delay 128, 192 and 256 Macrocells		2.5		2.5		2.5		4.0		4.0		4.0	ns
Reset and Preset Delays:														
t_{SRi}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0	ns
t_{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0	ns
t_{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		ns
t_{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		ns
Clock Enable Delays:														
t_{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		ns
t_{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		ns
Width:														
t_{WLS}	Global clock width low (Note 2)	2.5		3.0		3.0		4.0		5.0		6.0		ns
t_{WHS}	Global clock width high (Note 2)	2.5		3.0		3.0		4.0		5.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		ns
t_{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		ns
t_{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		ns
t_{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		ns
Frequency:														
f_{MAX}	External feedback, PAL block level Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133		125		100		83.3		71.4		55.6		MHz
	Internal feedback, PAL block level Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		125		100		83.3		62.5		MHz
	No feedback, PAL block level Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{HS})$	200		167		167		125		100		83.3		MHz
f_{MAXA}	External feedback, PAL block level Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111		111		71.4		58.8		47.6		41.7		MHz
	Internal feedback, PAL block level Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	143		125		83.3		66.6		52.6		45.5		MHz
	No feedback, PAL block level Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{HA})$	167		125		125		100		83.3		71.4		MHz
f_{MAXI}	Maximum input register frequency $1/(t_{SIRS}+t_{HIRS})$ or $1/(2 \times t_{WICW})$	167		125		125		100		83.3		71.4		MHz

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$)*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} =2.0 V	3.3 V or 5 V, 25 °C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} =2.0 V	3.3 V or 5 V, 25 °C, 1 MHz	10	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section of the Vantis 1999 Data Book.

I_{CC} CURVES AT HIGH /LOW POWER MODES

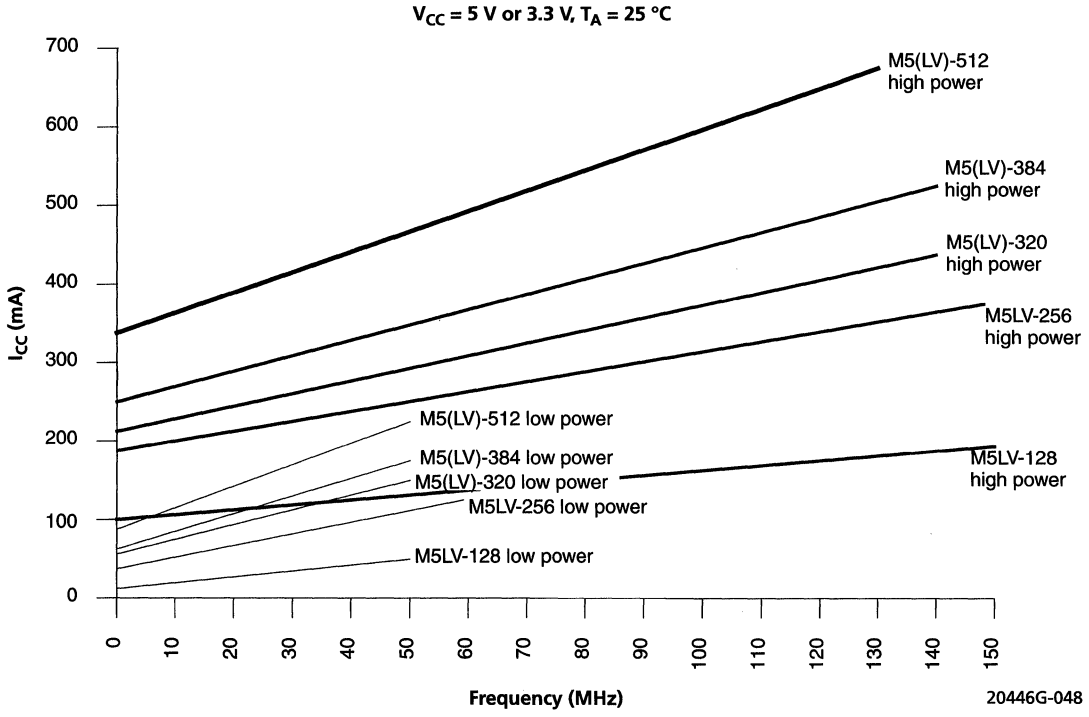


Figure 8. I_{CC} Curves at High/Low Power Modes

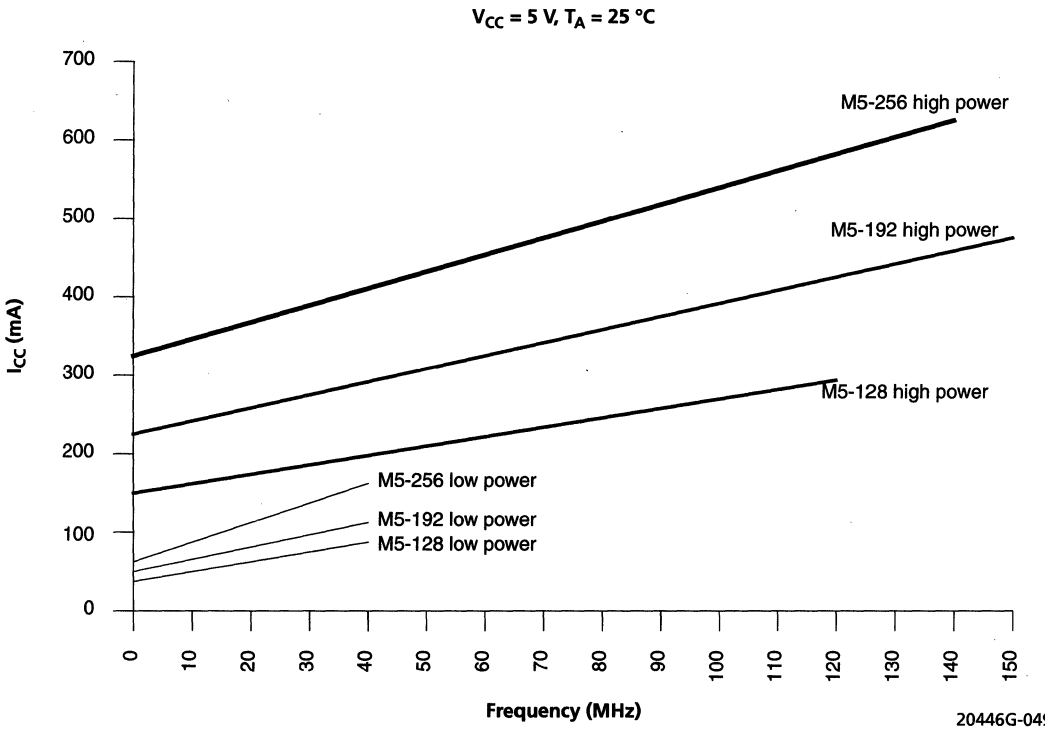
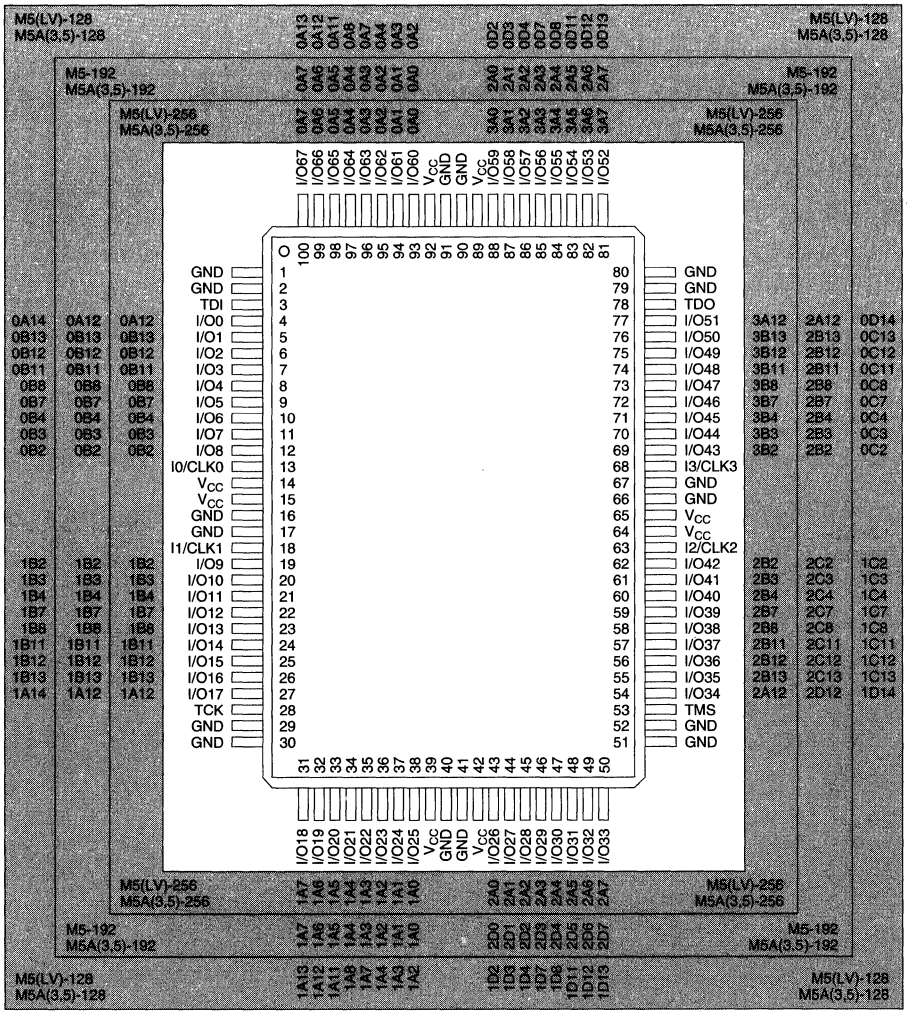


Figure 9. I_{CC} Curves at High/Low Power Modes

CONNECTION DIAGRAM

Top View

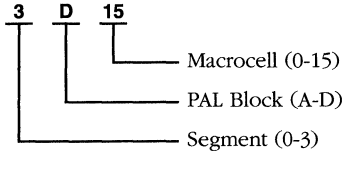
100-Pin PQFP (68 I/O)



20446G-016

Pin Designations

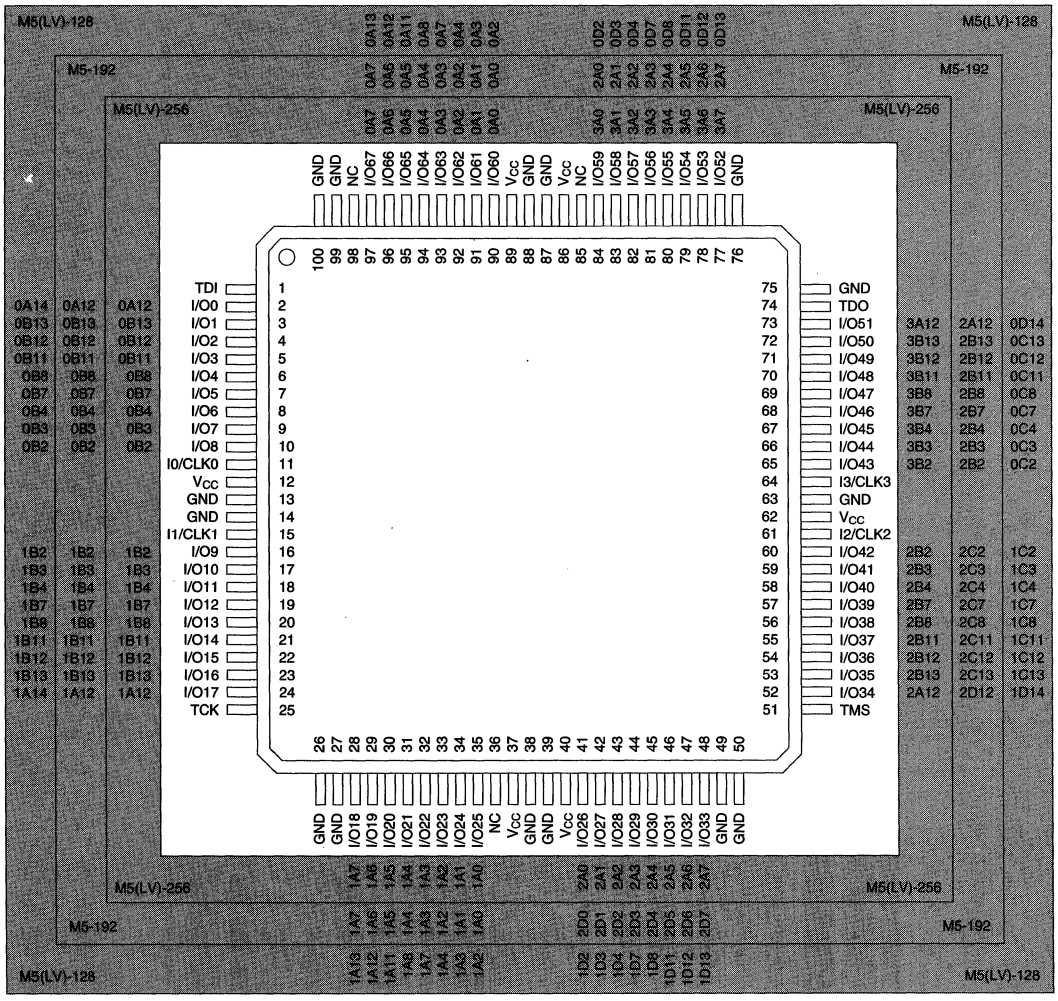
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

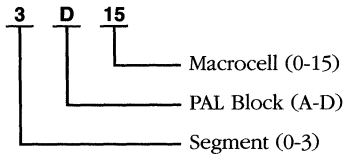
100-Pin TQFP (68 I/O)



20446G-017

Pin Designations

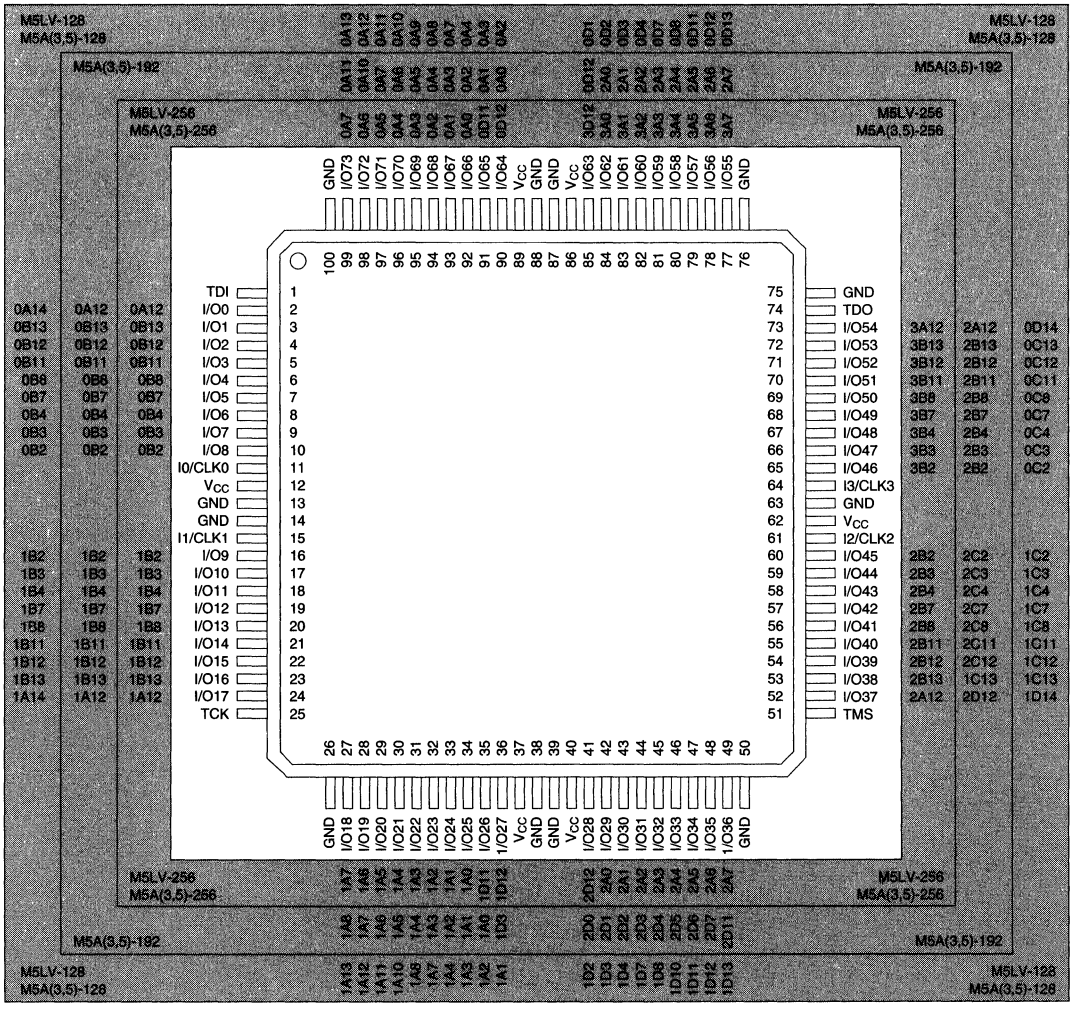
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

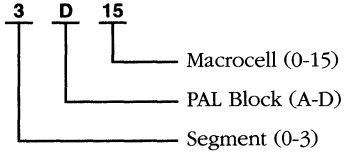
100-Pin TQFP (74 I/O)



20446G-018

Pin Designations

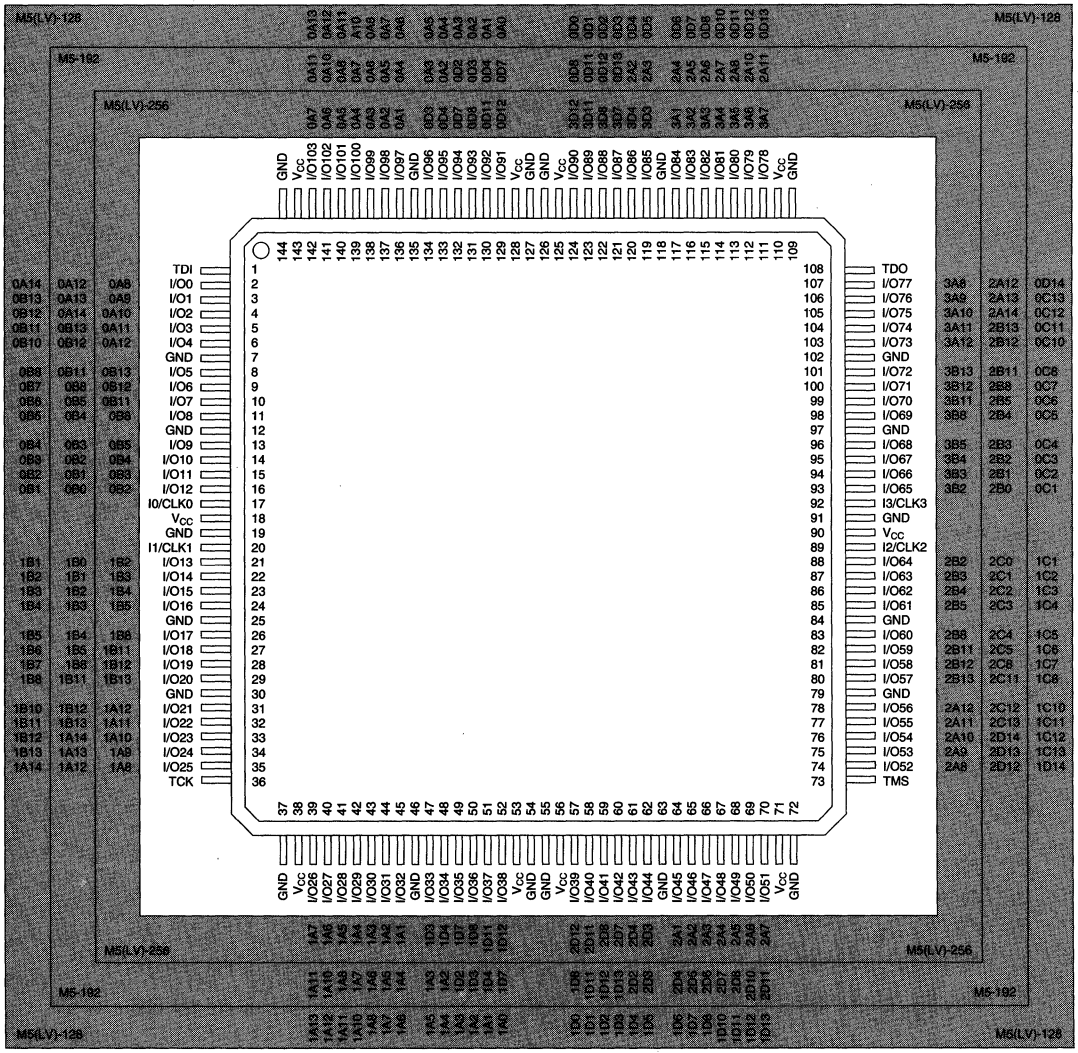
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

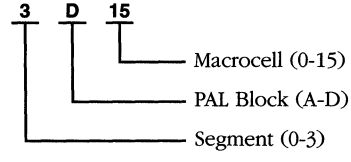
144-Pin PQFP



20446G-019

Pin Designations

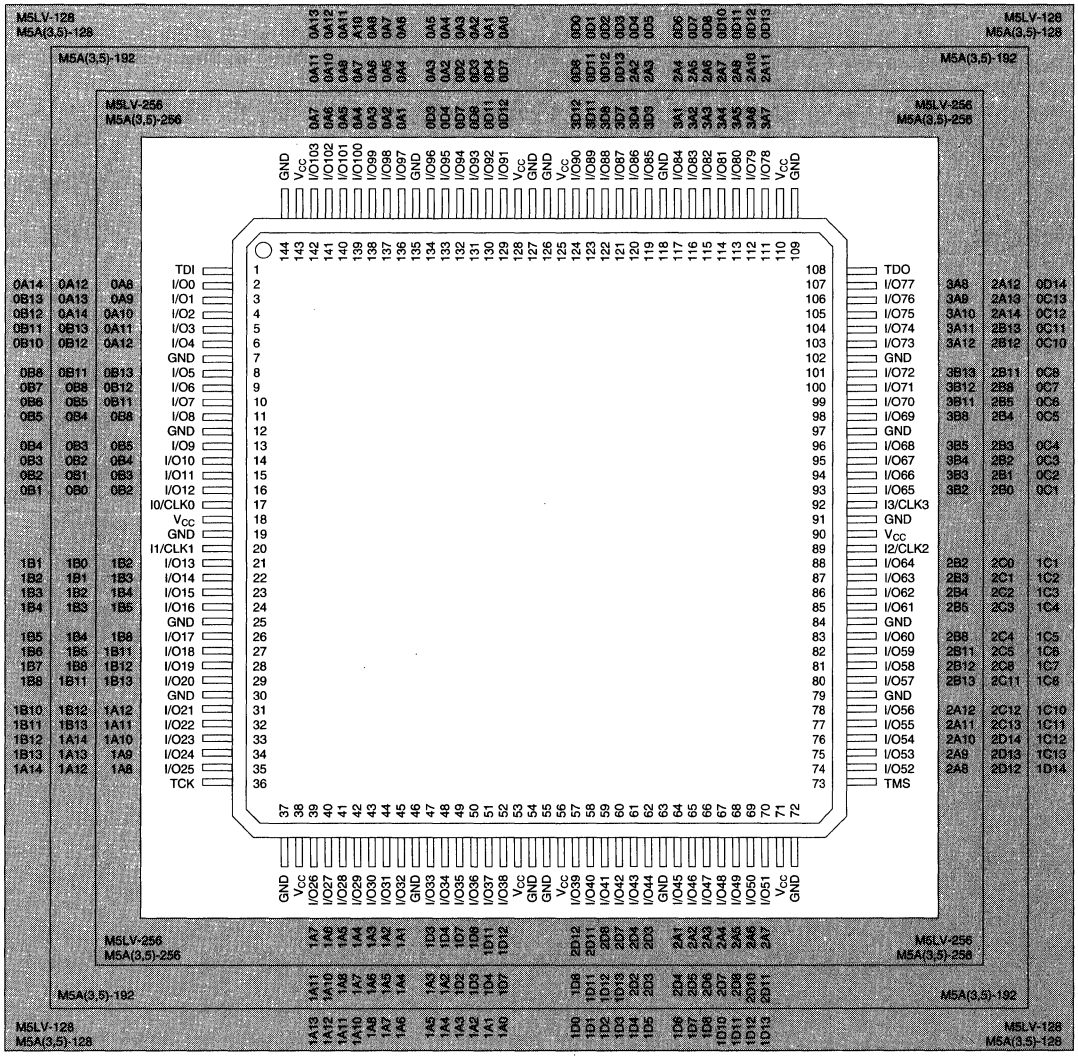
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

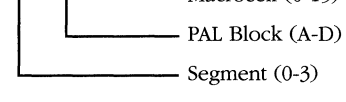
144-Pin TQFP



20446G-020

Pin Designations

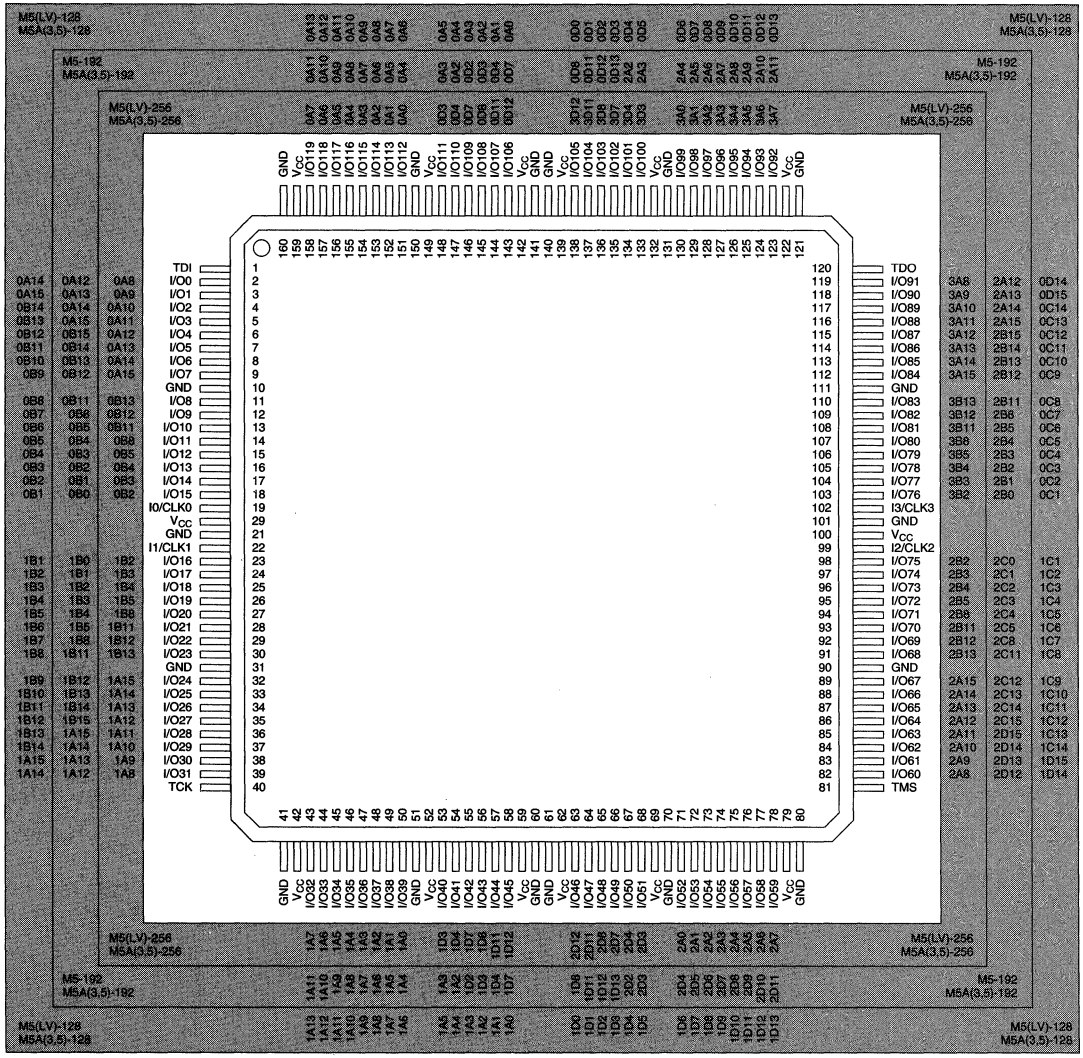
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

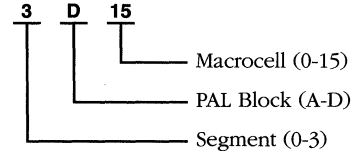
160-Pin PQFP (128, 192, 256 Macrocells)



20446G-021

Pin Designations

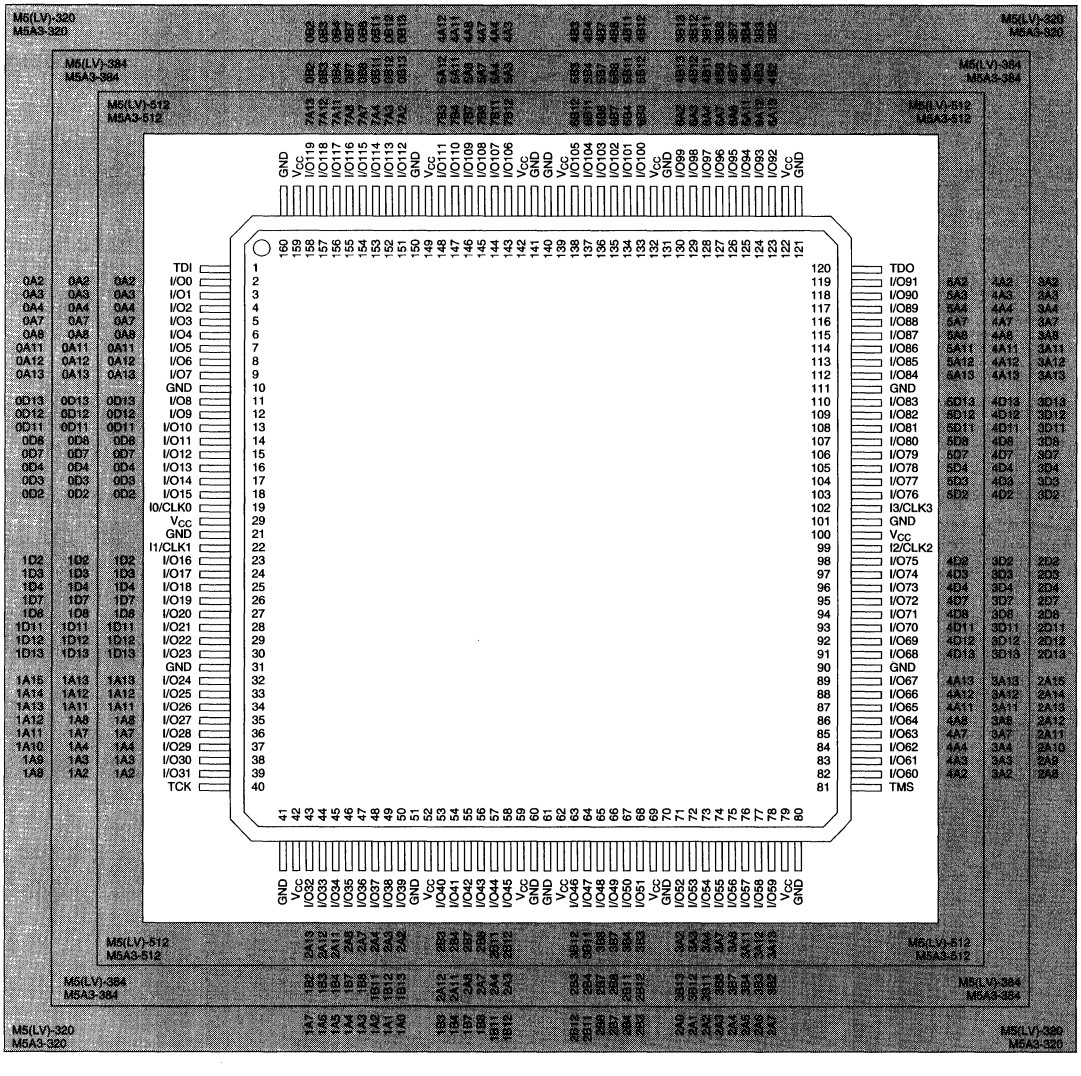
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

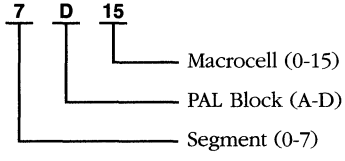
160-Pin PQFP (320, 384, 512 Macrocells)



20446G-022

Pin Designations

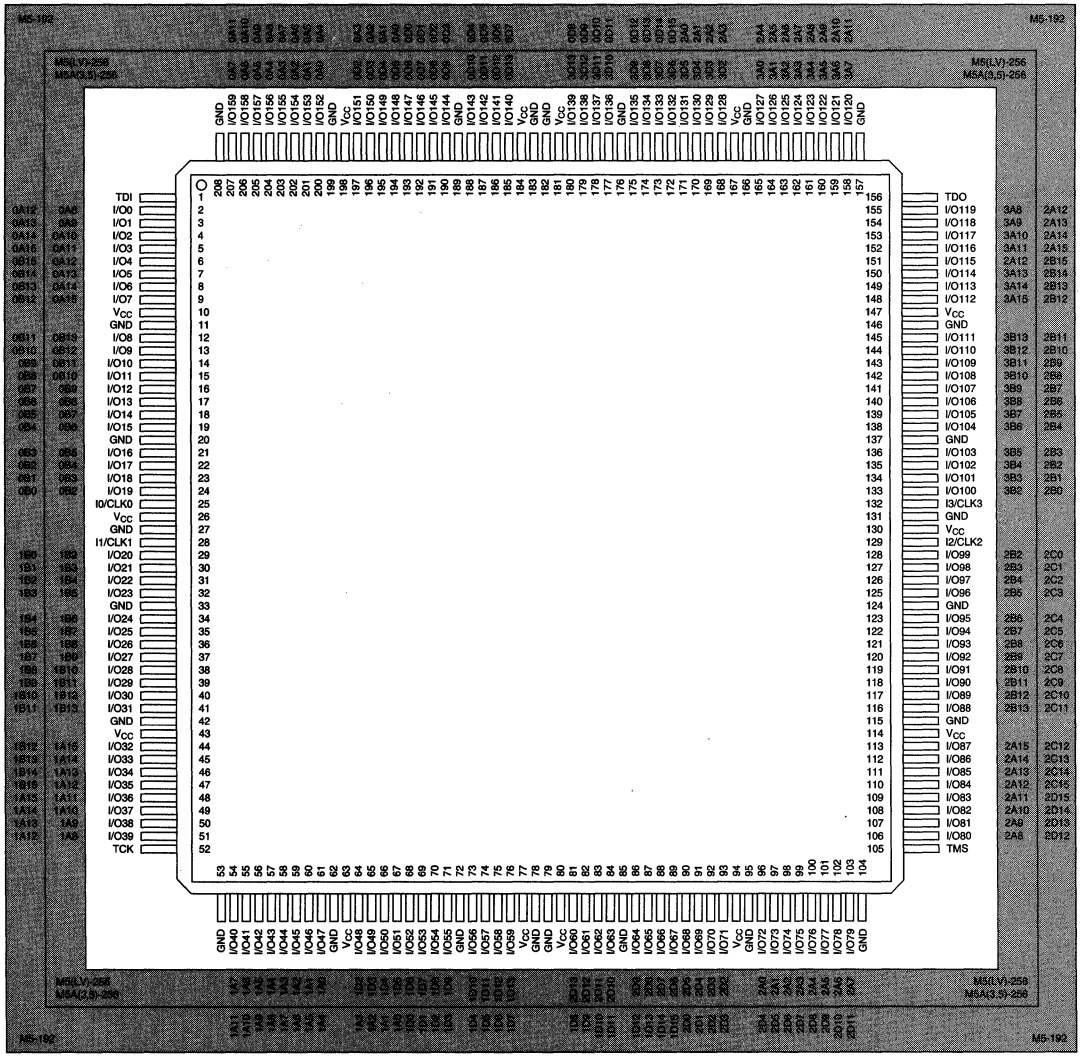
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

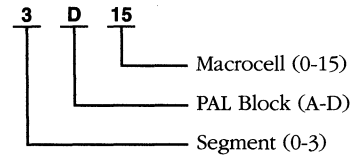
208-Pin PQFP (192, 256 Macrocells)



20446G-023

Pin Designations

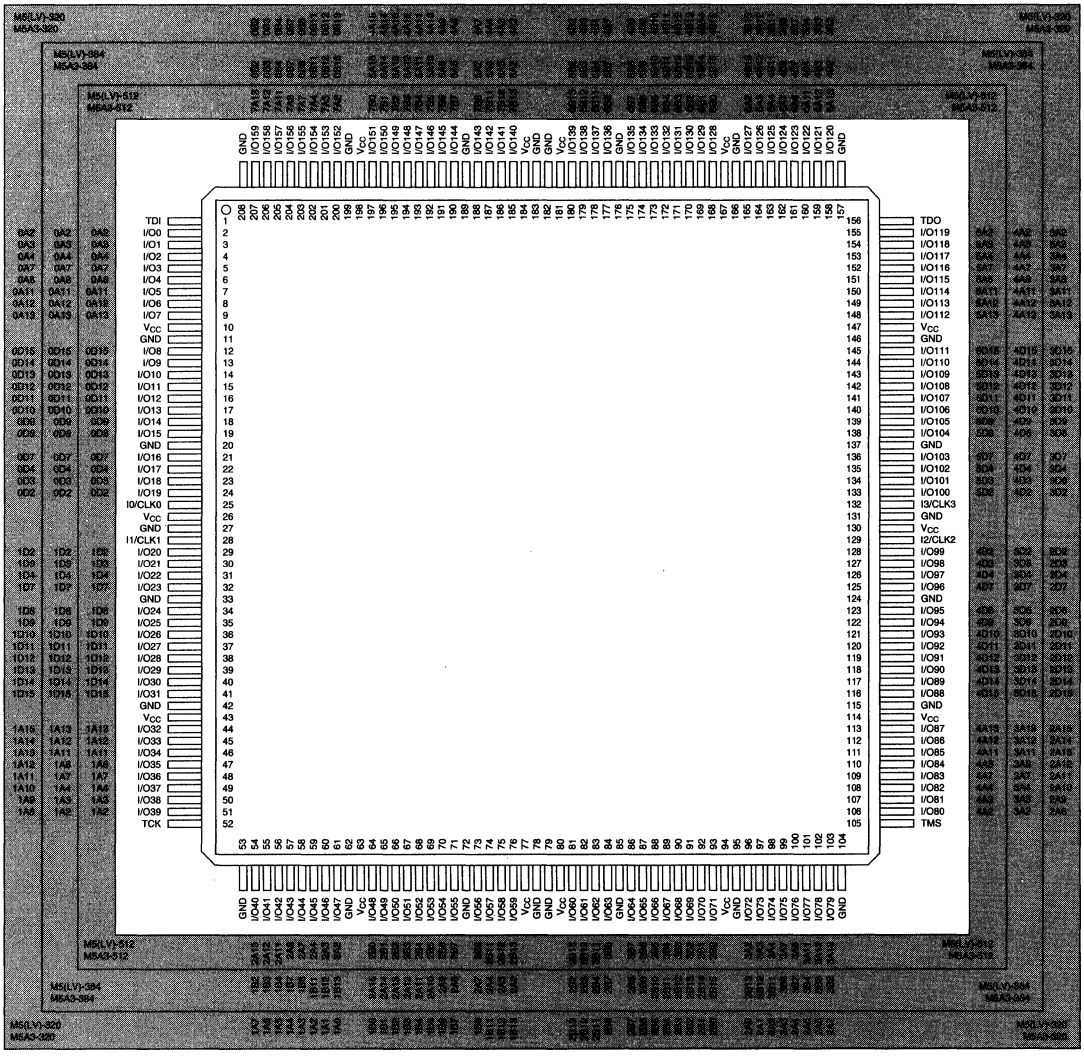
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

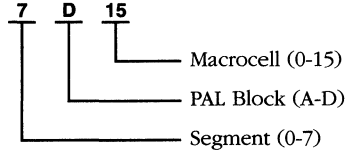
208-Pin PQFP (320, 384, 512 Macrocells)



20446G-024

Pin Designations

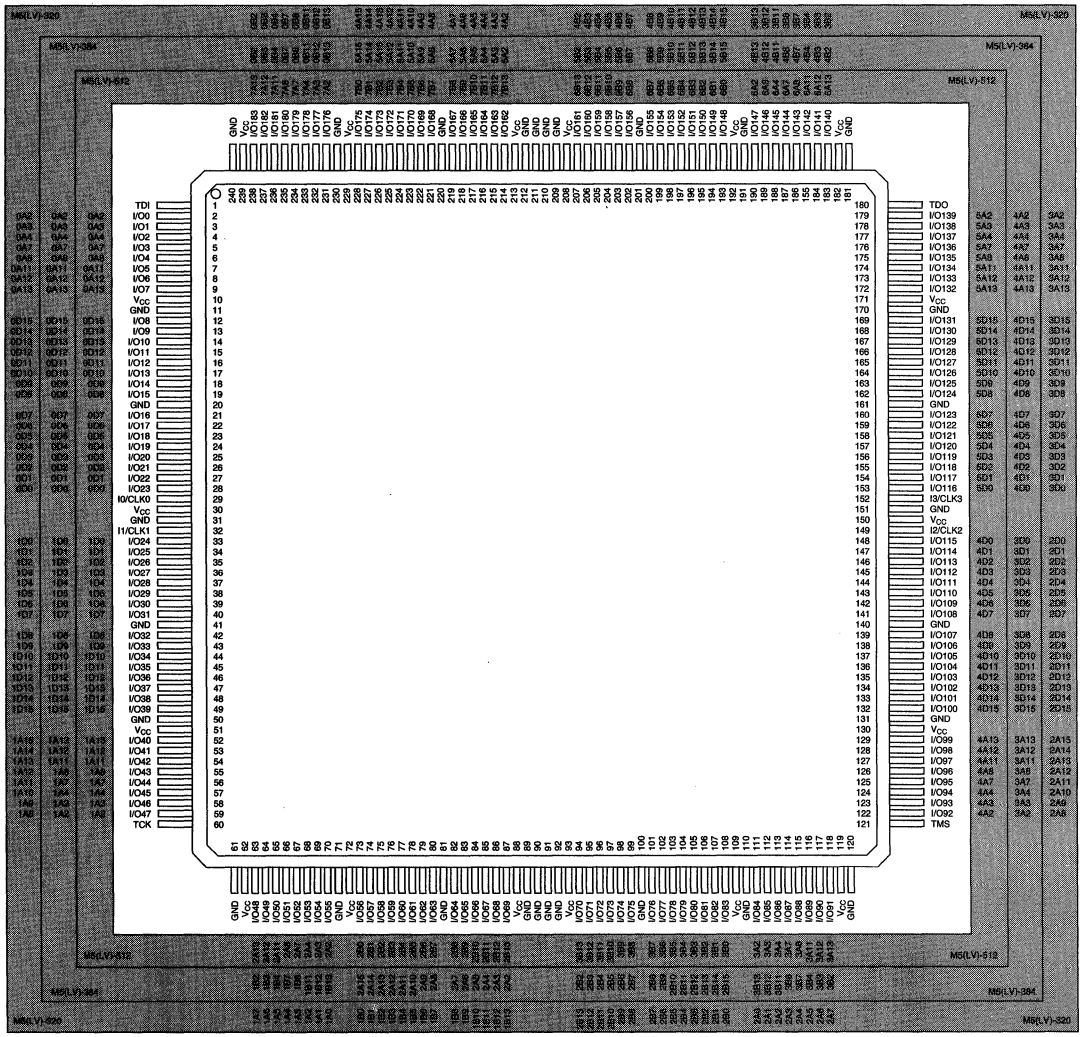
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM

Top View

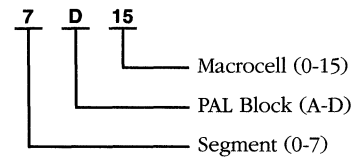
240-Pin PQFP



20446G-025

Pin Designations

CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



CONNECTION DIAGRAM — M5(LV)-320, M5(LV)-384, M5(LV)-512 M5A3-320, M5A3-384, M5A3-512

Bottom View (I/O Pin-outs)

256-Pin BGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND	I/O134	I/O128	GND	I/O116	I/O108	GND	GND	GND	GND	I/O76	I/O70	GND	I/O58	I/O44	GND	I/O11	GND
B	GND	I/O164	I/O148	I/O135	I/O129	I/O122	I/O117	I/O109	I/O102	I/O96	I/O90	I/O84	I/O77	I/O71	I/O64	I/O59	I/O45	I/O28	I/O12	GND
C	I/O181	I/O165	V_{CC}	I/O136	I/O130	I/O123	I/O118	I/O110	I/O103	I/O97	I/O91	I/O85	I/O78	I/O72	I/O65	I/O60	I/O46	V_{CC}	I/O13	I/O0
D	I/O182	I/O166	I/O149	V_{CC}	V_{CC}	I/O124	V_{CC}	I/O111	I/O104	I/O98	I/O92	I/O86	I/O79	V_{CC}	I/O66	V_{CC}	V_{CC}	I/O29	I/O14	I/O1
E	I/O183	I/O167	I/O150	TDO													TDI	I/O30	I/O15	I/O2
F	GND	I/O168	I/O151	I/O137													I/O47	I/O31	I/O16	GND
G	I/O184	I/O169	I/O152	V_{CC}													V_{CC}	I/O32	I/O17	I/O3
H	GND	I/O170	I/O153	I/O138													I/O48	I/O33	I/O18	GND
J	I/O185	I/O171	I/O154	I/O139													I/O49	I/O34	I/O19	I/O4
K	I/O186	I3/CLK3	I/O155	I/O140													I/O50	I/O35	IO/CLK0	GND
L	GND	I2/CLK2	I/O156	I/O141													I/O51	I/O36	I1/CLK1	I/O5
M	I/O187	I/O172	I/O157	I/O142													I/O52	I/O37	I/O20	I/O6
N	GND	I/O173	I/O158	I/O143													I/O53	I/O38	I/O21	GND
P	I/O188	I/O174	I/O159	V_{CC}													V_{CC}	I/O39	I/O22	I/O7
R	GND	I/O175	I/O160	I/O144													I/O54	I/O40	I/O23	GND
T	I/O189	I/O176	I/O161	TMS													TCK	I/O41	I/O24	I/O8
U	I/O190	I/O177	I/O162	V_{CC}	V_{CC}	I/O125	V_{CC}	I/O112	I/O105	I/O99	I/O93	I/O87	I/O80	V_{CC}	I/O67	V_{CC}	V_{CC}	I/O42	I/O25	I/O9
V	I/O191	I/O178	V_{CC}	I/O145	I/O131	I/O126	I/O119	I/O113	I/O106	I/O100	I/O94	I/O88	I/O81	I/O73	I/O68	I/O61	I/O55	V_{CC}	I/O26	I/O10
W	GND	I/O179	I/O163	I/O146	I/O132	I/O127	I/O120	I/O114	I/O107	I/O101	I/O95	I/O89	I/O82	I/O74	I/O69	I/O62	I/O56	I/O43	I/O27	GND
Y	GND	I/O180	GND	I/O147	I/O133	GND	I/O121	I/O115	GND	GND	GND	GND	I/O83	I/O75	GND	I/O63	I/O57	GND	GND	GND
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Pin Designations

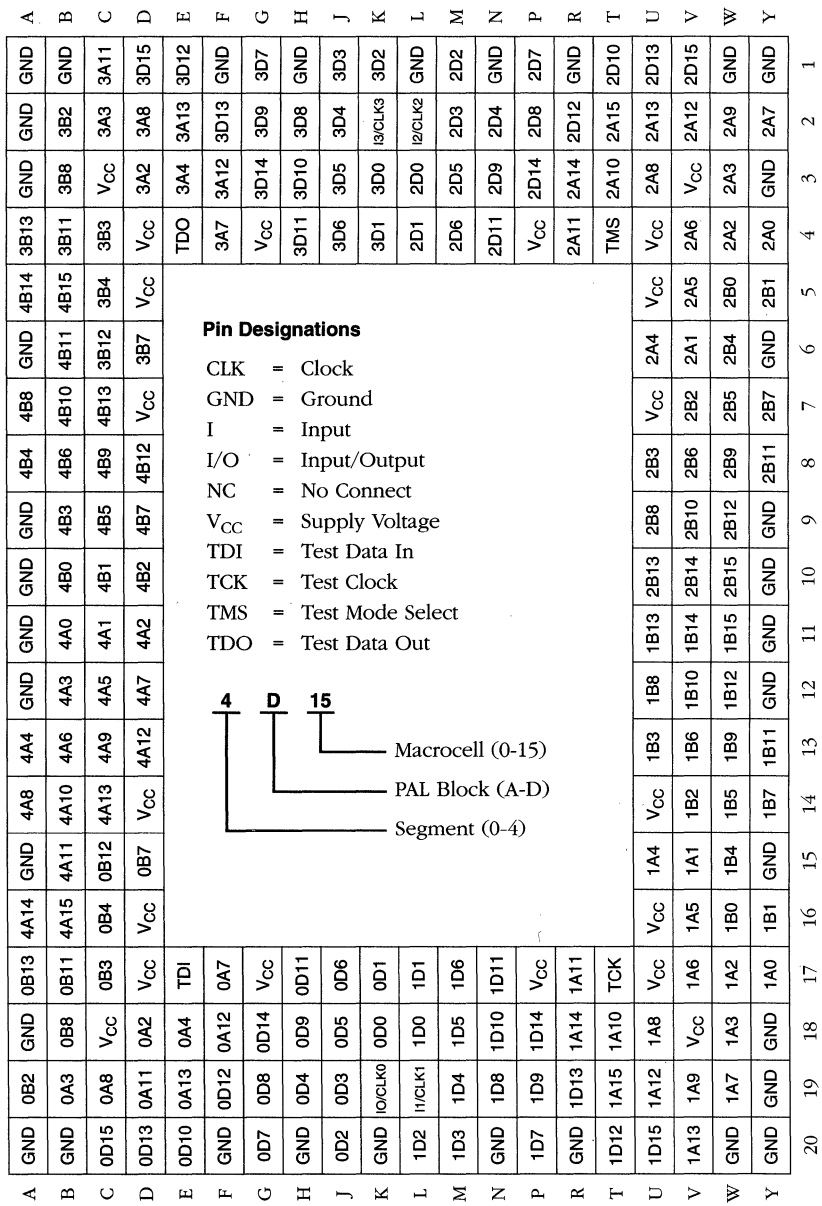
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

20446G-026

CONNECTION DIAGRAM — M5(LV)-320, M5A3-320

Bottom View (Macrocell Association)

256-Pin BGA

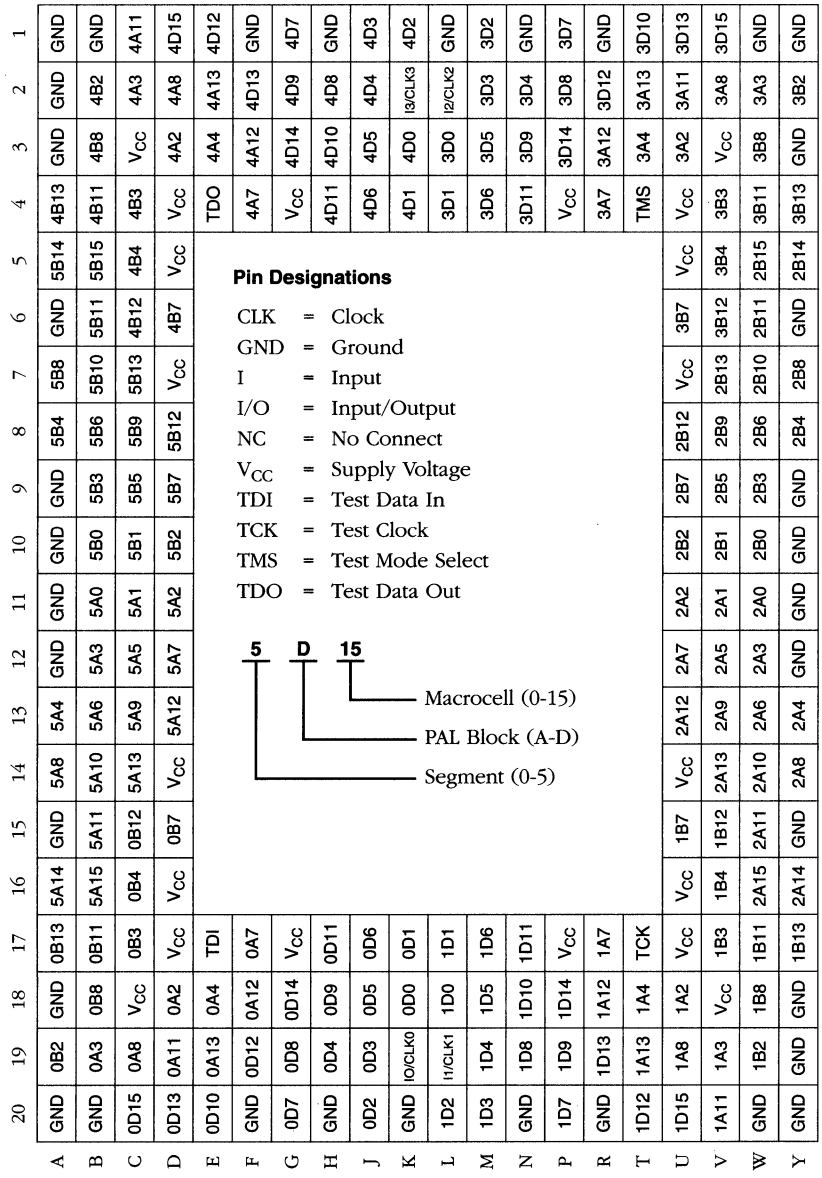


20446G-029

CONNECTION DIAGRAM — M5(LV)-384, M5A3-384

Bottom View (Macrocell Association)

256-Pin BGA

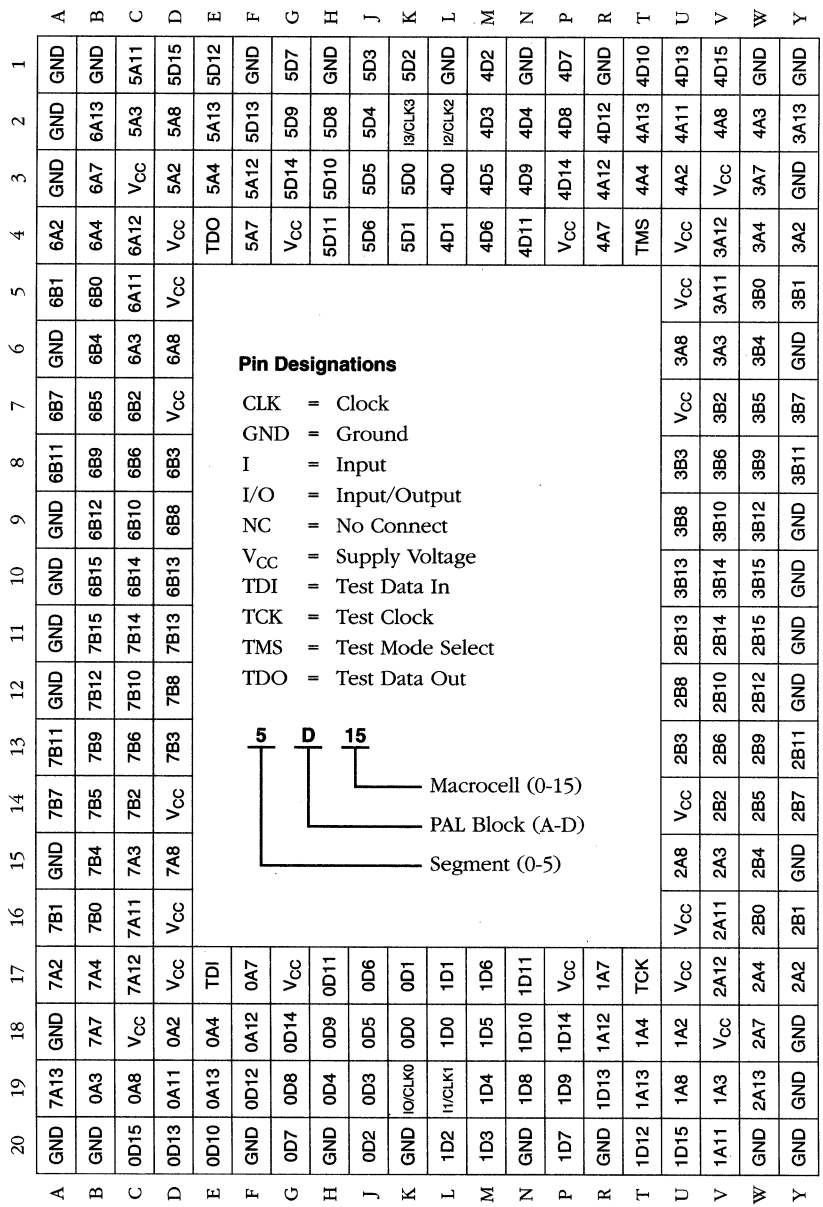


20446G-028

CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

Bottom View (Macrocell Association)

256-Pin BGA

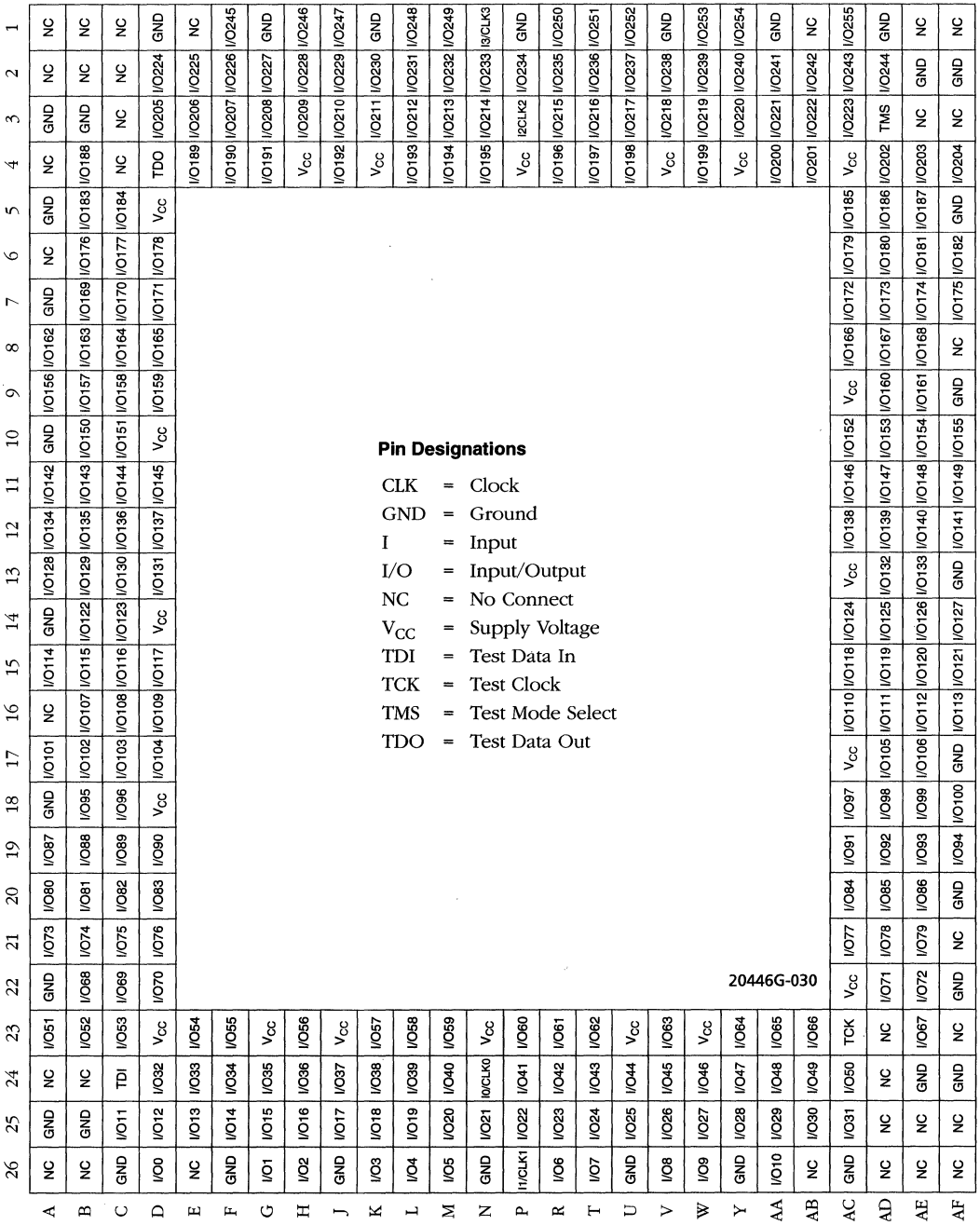


20446G-027

CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

Bottom View (I/O Pin-outs)

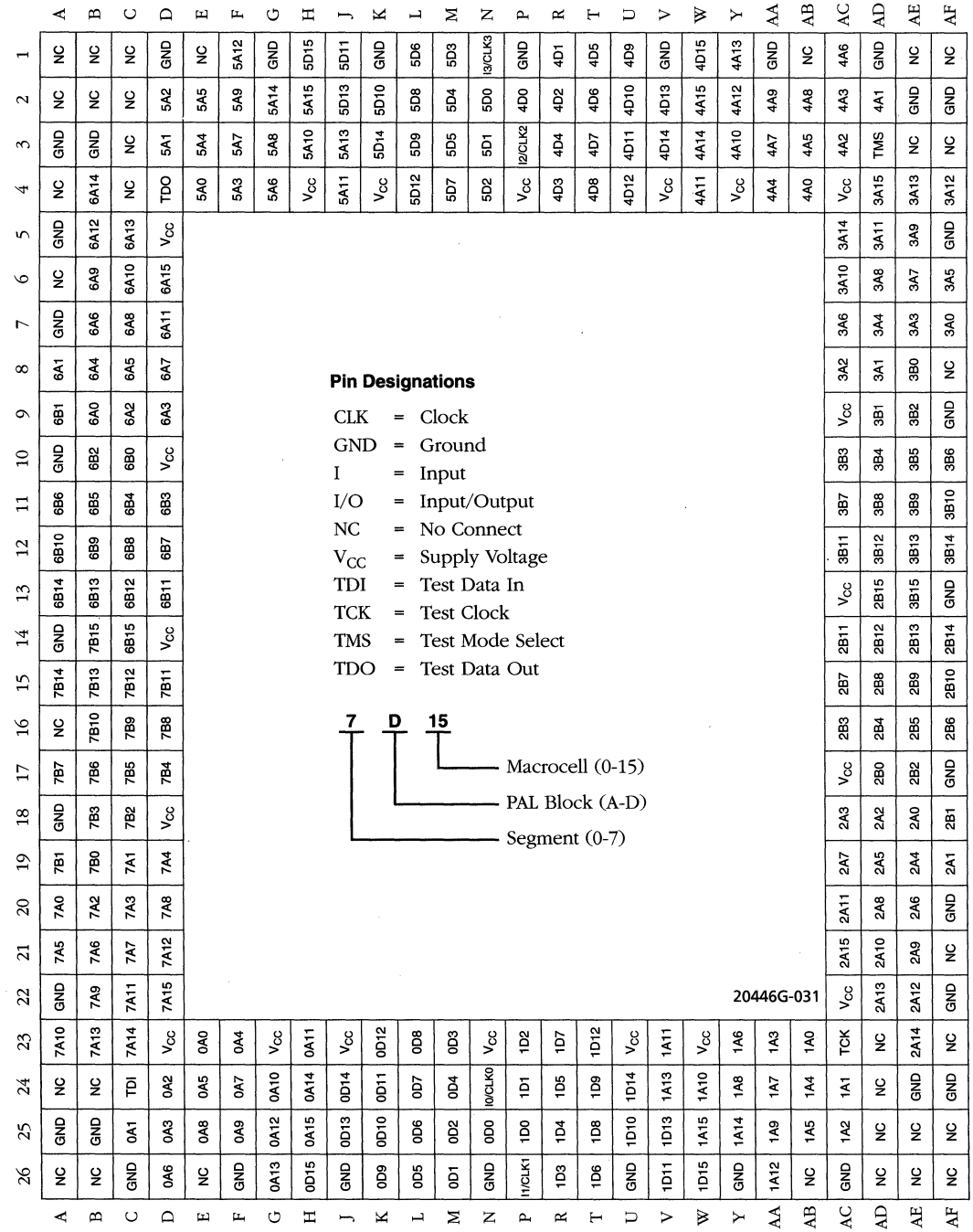
352-Pin BGA



CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

Bottom View (I/O Pin-outs)

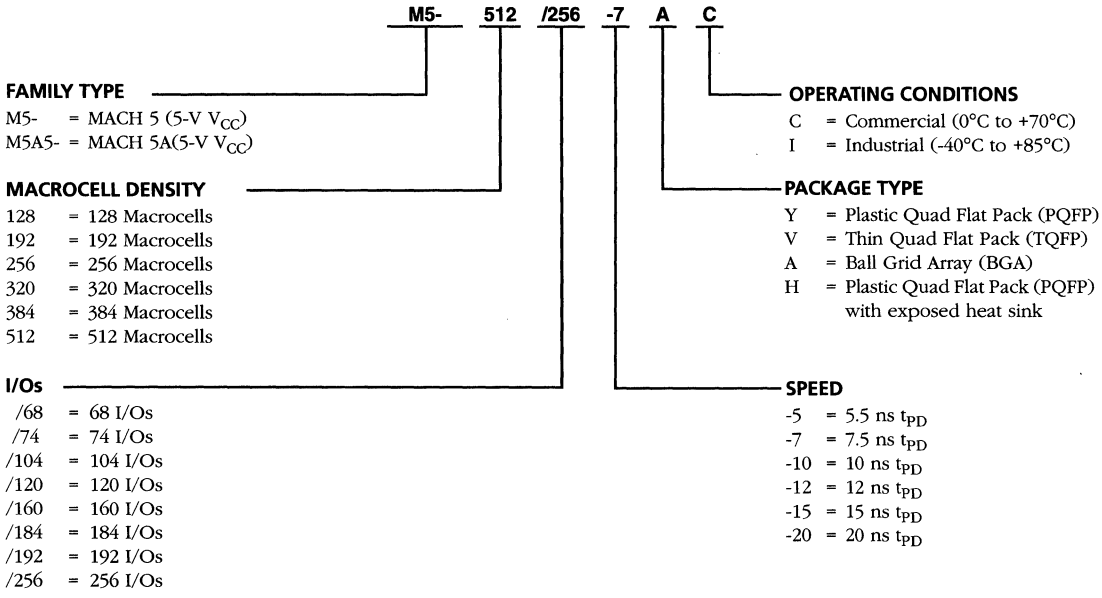
352-Pin BGA



ORDERING INFORMATION

5V M5 AND M5A5

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
M5-128/68	Commercial: M5: -7, -10, -12, -15 M5A5: -5, -7, -10, -12 Industrial: M5: -10, -12, -15, -20 M5A5: -7, -10, -12, -15	YC, VC, YI, VI
M5A5-128/68		YC, YI
M5A5-128/74		VC, VI
M5-128/104		YC, YI
M5A5-128/104		VC, VI
M5-128/120		YC, YI
M5A5-128/120		YC, YI
M5-192/68		YC, VC, YI, VI
M5A5-192/68		YC, YI
M5A5-192/74		VC, VI
M5-192/104		YC, YI
M5A5-192/104		VC, VI
M5-192/120		YC, YI
M5A5-192/120		YC, YI
M5-192/160		YC, YI
M5-256/68		YC, VC, YI, VI
M5A5-256/68		YC, YI
M5A5-256/74		VC, VI
M5-256/104		YC, YI
M5A5-256/104		VC, VI
M5-256/120		YC, YI
M5A5-256/120		YC, YI
M5-256/160		YC, YI
M5A5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN. All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., MACH5-512/256-7AC-10AI.

Valid Combinations		
M5-320/120	Commercial: -7, -10, -12, -15 Industrial: -10, -12, -15, -20	HC, HI
M5-320/160		HC, HI
M5-320/184		HC, HI
M5-320/192		AC, AI
M5-384/120		HC, HI
M5-384/160		HC, HI
M5-384/184		HC, HI
M5-384/192		AC, AI
M5-512/120		HC, HI
M5-512/160		HC, HI
M5-512/184		HC, HI
M5-512/192		AC, AI
M5-512/256		AC, AI

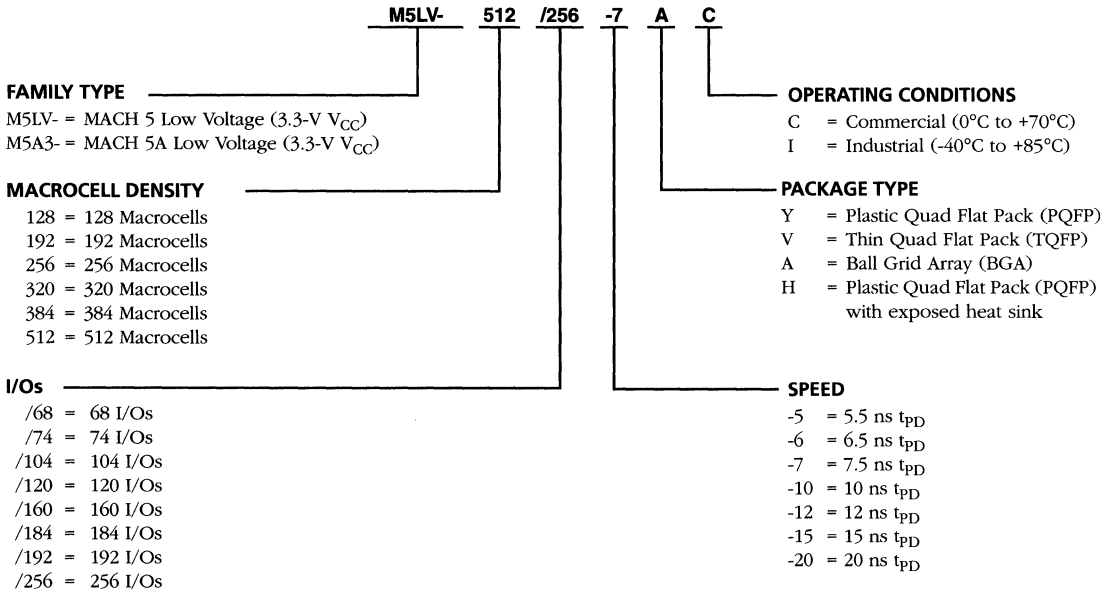
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

3.3V M5LV AND M5A3

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
M5LV-128/68	Commercial: M5LV: -5, -7, -10, -12 M5A3: -5, -7, -10, -12 Industrial: M5LV: -7, -10, -12, -15 M5A3: -7, -10, -12, -15	YC, VC, YI, VI
M5A3-128/68		YC, YI
M5LV-128/74		VC, VI
M5A3-128/74		VC, VI
M5LV-128/104		YC, VC, YI, VI
M5A3-128/104		VC,VI
M5LV-128/120		YC, YI
M5A3-128/120		YC, YI
M5A3-192/68		YC, YI
M5A3-192/74		VC, VI
M5A3-192/104		VC, VI
M5A3-192/120		YC, YI
M5LV-256/68		YC, VC, YI, VI
M5A3-256/68		YC, YI
M5LV-256/74		VC, VI
M5A3-256/74		VC, VI
M5LV-256/104		YC, VC, YI, VI
M5A3-256/104		VC, VI
M5LV-256/120		YC, YI
M5A3-256/120		YC, YI
M5LV-256/160		YC, YI
M5A3-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN. All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., MACH5 LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: M5LV: -7, -10, -12, -15 M5A3: -5, -6, -7, -10, -12 Industrial: M5LV: -10, -12, -15, -20 M5A3: -7, -10, -12, -15	HC, HI
M5A3-320/120		HC, HI
M5LV-320/160		HC, HI
M5A3-320/160		HC, HI
M5LV-320/184		HC, HI
M5LV-320/192		AC, AI
M5A3-320/192		AC, AI
M5LV-384/120		HC, HI
M5A3-384/120		HC, HI
M5LV-384/160		HC, HI
M5A3-384/160		HC, HI
M5LV-384/184		HC, HI
M5LV-384/192		AC, AI
M5A3-384/192		AC, AI
M5LV-512/120		HC, HI
M5A3-512/120		HC, HI
M5LV-512/160		HC, HI
M5A3-512/160		HC, HI
M5LV-512/184		HC, HI
M5LV-512/192		AC, AI
M5A3-512/192		AC, AI
M5LV-512/256		AC, AI
M5A3-512/256		AC, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

VANTIS

BEYOND PERFORMANCE

MACH 1 and 2 CPLD Families

High-Performance EE CMOS Programmable Logic

FEATURES

- **High-performance electrically-erasable CMOS PLD families**
- **32 to 128 macrocells**
- **44 to 100 pins in cost-effective PLCC, PQFP and TQFP packages**
- **SpeedLocking™ – guaranteed fixed timing up to 16 product terms**
- **Commercial 5/5.5/6/7.5/10/12/15-ns t_{PD} and Industrial 7.5/10/12/14/18-ns t_{PD}**
- **Configurable macrocells**
  - — Programmable polarity
  - — Registered or combinatorial outputs
  - — Internal and I/O feedback paths
  - — D-type or T-type flip-flops
  - — Output Enables
  - — Choice of clocks for each flip-flop
  - — Input registers for MACH 2 family
- **JTAG (IEEE 1149.1)-compatible, 5-V in-system programming available**
- **Peripheral component interconnect (PCI) compliant at 5/5.5/6/7.5/10/12 ns**
- **Safe for mixed supply voltage system designs**
- **Bus-Friendly™ inputs and I/Os reduce risk of unwanted oscillatory outputs**
- **Programmable power-down mode results in power savings of up to 75%**
- **Supported by Vantis DesignDirect™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for Vantis
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Vantis and third-party hardware programming support**
  - — VantisPRO™ (formerly known as MACHPRO®) software for in-system programmability support on PCs and Automated Test Equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

Publication# **14051** Rev: **K**
Amendment/**0** Issue Date: **November 1998**

Table 1. MACH 1 and 2 Family Device Features [1]

Feature	MACH111 (SP)	MACH131 (SP)	MACH211 (SP)	MACH221 (SP)	MACH231 (SP)
Macrocells	32	64	64	96	128
Maximum user I/O pins	32	64	32	48	64
t_{PD} (ns)	5.0	5.5	7.5 (6.0)	7.5	6.0 (10)
t_S (ns)	3.5	3.0	5.5 (5)	5.5	5 (6.5)
t_{CO} (ns)	3.5	4	4.5 (4)	5	4 (6.5)
f_{CNT} (MHz)	182	182	133 (166)	133	166 (100)

Note:

1. Values in parentheses ( ) are for the SP version.

GENERAL DESCRIPTION

The MACH® 1 & 2 families from Vantis offer high-performance, low cost Complex Programmable Logic Devices (CPLDs), addressing the growing need for speed in networking, telecommunications and computing. MACH 1 & 2 devices are available in speeds as fast as 5.0-ns t_{PD} and in densities ranging from 32 to 128 macrocells (Tables 1 and 2). The overall benefits for users include guaranteed high performance for entry-to-mid-level logic needs at a low cost.

Table 2. MACH 1 and 2 Family Speed Grades[1]

Device	-5	-6	-7	-10	-12	-14	-15	-18
MACH111	C (Note 2)		C, I	C, I	C, I	I	C	I
MACH111SP	C (Note 2)		C, I	C, I	C, I	I	C	I
MACH131	C (Note 3)		C, I	C, I	C, I	I	C	I
MACH131SP	C (Note 3)		C, I	C, I	C, I	I	C	I
MACH211			C	C, I	C, I	I	C	I
MACH211SP		C	C	C, I	C, I	I	C	I
MACH221			C	C, I	C, I	I	C	I
MACH221SP			C	C, I	C, I	I	C	I
MACH231		C	C	C	C, I	I	C	I
MACH231SP				C	C, I	I	C	I

Notes:

1. C = Commercial, I = Industrial

2. -5 speed grade for MACH111 (SP) = 5.0 ns t_{PD}

3. -5 speed grade for MACH131(SP) = 5.5 ns t_{PD}

The MACH 1 & 2 families consist of ten devices—five base options, each with a counterpart that includes JTAG-compatible in-system programming (ISP). These devices offer five different density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), and Plastic Leaded Chip Carrier (PLCC) packages from 44 to 100 pins (Table 3). Each MACH 1 & 2 device is PCI compliant and includes other features such as SpeedLocking architecture for guaranteed fixed timing, Bus-Friendly inputs and I/Os, and programmable power-down mode for extra power savings.

Table 3. MACH 1 and 2 Family Package and I/O Options

Device	44-pin PLCC	44-pin TQFP	68-pin PLCC	84-pin PLCC	100-pin TQFP	100-pin PQFP
MACH111	X	X				
MACH111SP	X	X				
MACH131				X		
MACH131SP					X	X
MACH211	X	X				
MACH211SP	X	X				
MACH221			X			
MACH221SP						X
MACH231				X		
MACH231SP					X	X

Note:

1. *The MACH110, MACH120, MACH130, MACH210, MACHLV210, MACH215, MACH220 and MACH230 are not listed above and not recommended for new designs. However, they are still supported by Vantis. For technical or sales support, please call your local Vantis sales office or visit our Web site at www.vantis.com for more information.*

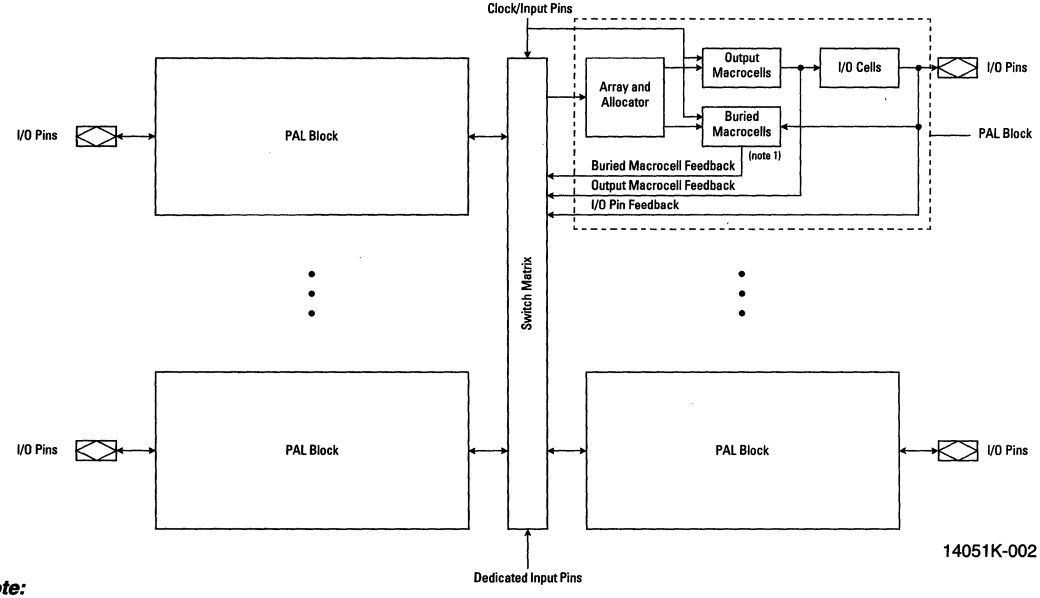
Vantis offers software design support for MACH devices in both the MACHXL® and DesignDirect development systems. The DesignDirect development system is the Vantis implementation software that includes support for all Vantis CPLD, FPGA, and SPLD devices. This system is supported under Windows '95, '98 and NT as well as Sun Solaris and HPUX.

DesignDirect software is designed for use with design entry, simulation and verification software from leading-edge tool vendors such as Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys, Synplicity, Viewlogic and others. It accepts EDIF 2 0 0 input netlists, generates JEDEC files for Vantis PLDs and creates industry-standard EDIF, Verilog, VITAL compliant VHDL and SDF simulation netlists for design verification.

DesignDirect software is also available in product configurations that include VHDL and Verilog synthesis from Exemplar Logic and VHDL, Verilog RTL and gate level timing simulation from Model Technology. Schematic capture and ABEL entry, as well as functional simulation, are also provided.

FUNCTIONAL DESCRIPTION

Each MACH 1 and 2 device consists of multiple, optimized PAL® blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of using multiple devices.



Note:

1. There are no buried macrocells in MACH 1 devices. All macrocells are output macrocells.

Device	PAL Blocks	Macrocells per Block	I/Os per Block	Product Terms per Block
MACH111(SP)	2	16	16	70
MACH131(SP)	4	16	16	70
MACH211(SP)	4	16	8	68
MACH221(SP)	8	12	6	52
MACH231(SP)	8	16	8	68

Figure 1. Overall Architecture of MACH 1 & 2 Devices

The switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with guaranteed fixed timing (SpeedLocking).

The switch matrix makes a MACH device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of the following elements:

- Product-term array
- Logic Allocator
- Macrocells
- I/O cells

Each PAL block additionally contains an asynchronous reset product term and an asynchronous preset product term. This allows the flip-flops within a single PAL block to be initialized as a bank. There are also output enable product terms that provide tri-state control for the I/O cells.

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix (Table 4), and are provided in both true and complement forms for efficient logic implementation.

Because the number of product terms available for a given function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

Table 4. PAL Block Inputs

Device	Number of Inputs to PAL Block	Device	Number of Inputs to PAL Block
MACH111	26	MACH211SP	26
MACH111SP	26	MACH221	26
MACH131	26	MACH221SP	26
MACH131SP	26	MACH231	32
MACH211	26	MACH231SP	32

Logic Allocator

The logic allocator (Figure 2) is a block within which different product terms are allocated to the appropriate macrocells in groups of four product terms called "product term clusters". The availability and distribution of product term clusters is automatically considered by the software as it fits functions within the PAL block. The size of the product term clusters has been designed to provide high utilization of product terms. Complex functions using many product terms are possible, and when few product terms are used, there will be a minimal number of unused, or wasted, product terms left over.

The product term clusters do not "wrap" around the logic block. This means that the macrocells at the ends of the block have fewer product terms available (Tables 5, 6, 7, 8).

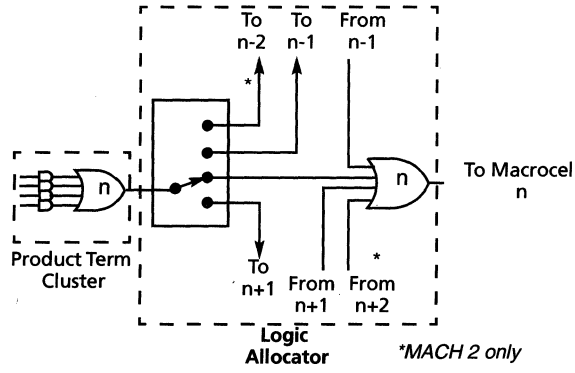


Figure 2. Product Term Clusters and the Logic Allocator

Table 5. Logic Allocation for MACH111(SP)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1	M_8	C_8, C_9
M_1	C_0, C_1, C_2	M_9	C_8, C_9, C_{10}
M_2	C_1, C_2, C_3	M_{10}	C_9, C_{10}, C_{11}
M_3	C_2, C_3, C_4	M_{11}	C_{10}, C_{11}, C_{12}
M_4	C_3, C_4, C_5	M_{12}	C_{11}, C_{12}, C_{13}
M_5	C_4, C_5, C_6	M_{13}	C_{12}, C_{13}, C_{14}
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}

Table 6. Logic Allocation for MACH131(SP)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1	M_8	C_7, C_8, C_9
M_1	C_0, C_1, C_2	M_9	C_8, C_9, C_{10}
M_2	C_1, C_2, C_3	M_{10}	C_9, C_{10}, C_{11}
M_3	C_2, C_3, C_4	M_{11}	C_{10}, C_{11}, C_{12}
M_4	C_3, C_4, C_5	M_{12}	C_{11}, C_{12}, C_{13}
M_5	C_4, C_5, C_6	M_{13}	C_{12}, C_{13}, C_{14}
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8	M_{15}	C_{14}, C_{15}

Table 7. Logic Allocation for MACH211(SP) and MACH231(SP)

Macrocell			Macrocell		
Output	Buried	Available Clusters	Output	Buried	Available Clusters
M_0		C_0, C_1, C_2	M_8		C_7, C_8, C_9, C_{10}
	M_1	C_0, C_1, C_2, C_3		M_9	C_8, C_9, C_{10}, C_{11}
M_2		C_1, C_2, C_3, C_4	M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_3	C_2, C_3, C_4, C_5		M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4		C_3, C_4, C_5, C_6	M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_5	C_4, C_5, C_6, C_7		M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6		C_5, C_6, C_7, C_8	M_{14}		C_{13}, C_{14}, C_{15}
	M_7	C_6, C_7, C_8, C_9		M_{15}	C_{14}, C_{15}

Table 8. Logic Allocation for MACH221(SP)

Macrocell			Macrocell		
Output	Buried	Available Clusters	Output	Buried	Available Clusters
M_0		C_0, C_1, C_2	M_6		C_5, C_6, C_7, C_8
	M_1	C_0, C_1, C_2, C_3		M_7	C_6, C_7, C_8, C_9
M_2		C_1, C_2, C_3, C_4	M_8		C_7, C_8, C_9, C_{10}
	M_3	C_2, C_3, C_4, C_5		M_9	C_8, C_9, C_{10}, C_{11}
M_4		C_3, C_4, C_5, C_6	M_{10}		C_9, C_{10}, C_{11}
	M_5	C_4, C_5, C_6, C_7		M_{11}	C_{10}, C_{11}

Macrocell

There are two fundamental types of macrocell: the output macrocell and the buried macrocell. The buried macrocell is only found in MACH 2 devices. The use of buried macrocells effectively doubles the number of macrocells available without increasing the pin count.

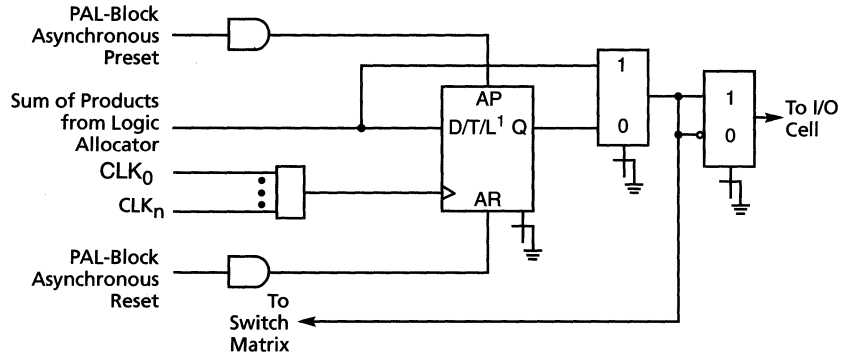
Both macrocell types can generate registered or combinatorial outputs. For the MACH 2 series, a transparent-low latch configuration is provided. If the register is used, it can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 9. Programmable polarity (for output macrocells) and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 9. Register/Latch Operation

Configuration	D/T	CLK/LE	Q+
D-Register	X	0,1,↓	Q
	0	↑	0
	1	↑	1
T-Register	X	0,1,↓	Q
	0	↑	Q
	1	↑	$\overline{Q}$
Latch	X	1	Q
	0	0	0
	1	0	1

The output macrocell (Figure 3) sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

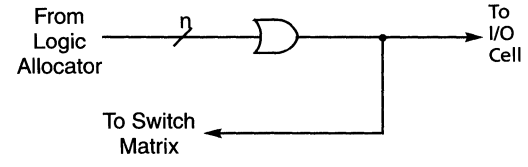
The buried macrocell (Figure 5) does not send its output to an I/O cell. The output of a buried macrocell is provided only as an internal feedback signal which feeds the switch matrix. This allows the designer to generate additional logic without requiring additional pins. The buried macrocell can also be used to register or latch inputs. The input register is a D-type flip-flop; the input latch is a transparent-low D-type latch. Once configured as a registered or latched input, the buried macrocell cannot generate logic from the product-term array. The basic buried macrocell configurations are shown in Figure 6.



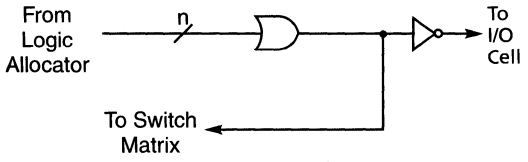
Note:

1. Latch option available on MACH 2 devices only.

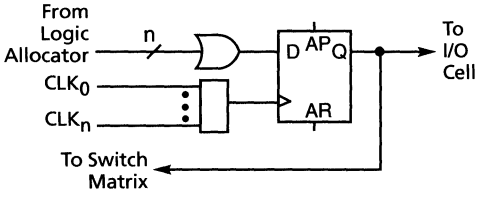
Figure 3. Output Macrocell



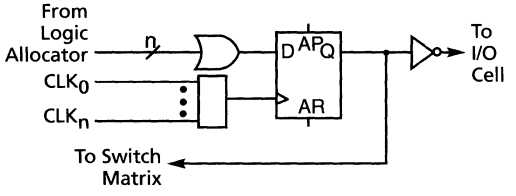
a. Combinatorial, active high



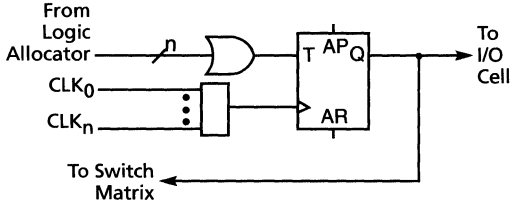
b. Combinatorial, active low



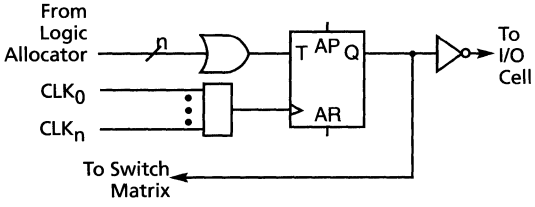
c. D-type register, active high



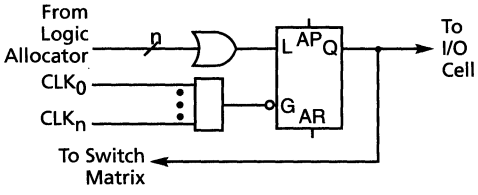
d. D-type register, active low



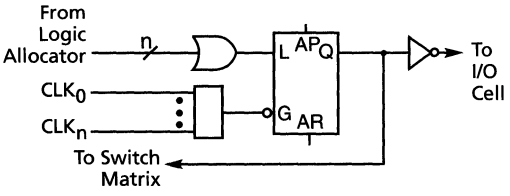
e. T-type register, active high



f. T-type register, active low



g. Latch, active high (MACH 2 only)



h. Latch, active low (MACH 2 only)

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Figure 4. Output Macrocell Configurations

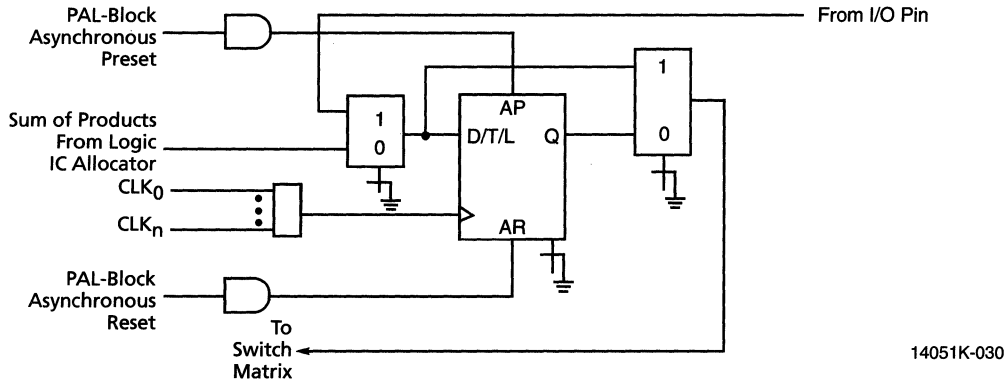


Figure 5. Buried Macrocell (MACH 2 only)

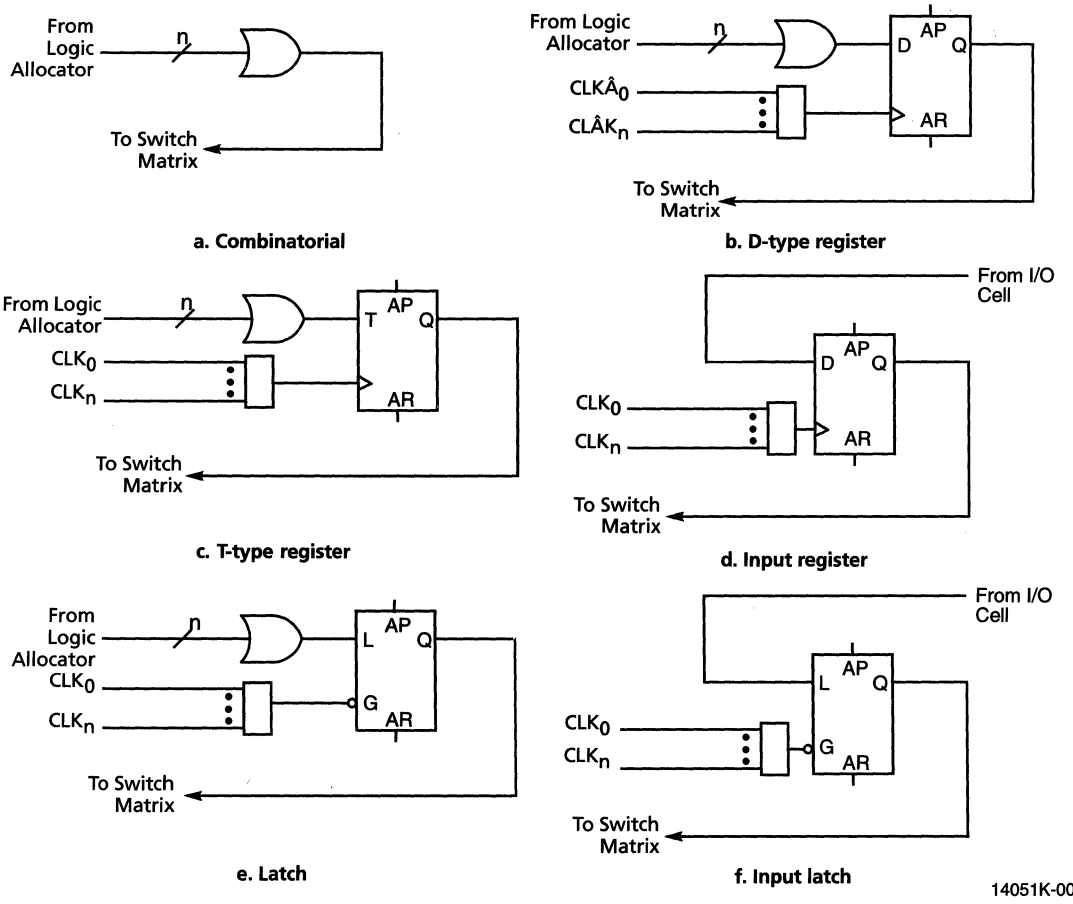


Figure 6. Buried Macrocell Configurations (MACH 2 only)

The flip-flops in either macrocell type can be clocked by one of several clock pins (Table 10). Registers are clocked on the rising edge of the clock input. Latches hold their data when the gate input is HIGH. Clock pins are also available as inputs, although care must be taken when a signal acts as both clock and input to the same device.

Table 10. Macrocell Clocks

Device	Number of Clocks Available	Device	Number of Clocks Available
MACH111	4	MACH211SP	2
MACH111SP	2	MACH221	4
MACH131	4	MACH221SP	4
MACH131SP	4	MACH231	4
MACH211	4	MACH231SP	4

All flip-flops have asynchronous reset and preset. This is controlled by the common product terms that control all flip-flops within a PAL block. For a single PAL block, all flip-flops, whether in an output or a buried macrocell, are initialized together. The initialization functionality of the flip-flops is illustrated in Table 11.

Table 11. Asynchronous Reset/Preset Operation

Configuration	AR	AP	CLK/LE	Q+
Register	0	0	X	See Table 9
	0	1	X	1
	1	0	X	0
	1	1	X	0
Latch	0	0	X	See Table 9
	0	1	0	Illegal
	0	1	1	1
	1	0	0	Illegal
	1	0	1	0
	1	1	0	Illegal
	1	1	1	0

I/O Cells

The I/O cells (Figure 7) provide a three-state output buffer. The three-state buffer can be left permanently enabled for use only as an output, permanently disabled for use as an input, or it can be controlled by one of two product terms for bi-directional signals and bus connections. The two product terms provided are common to a bank of I/O cells.

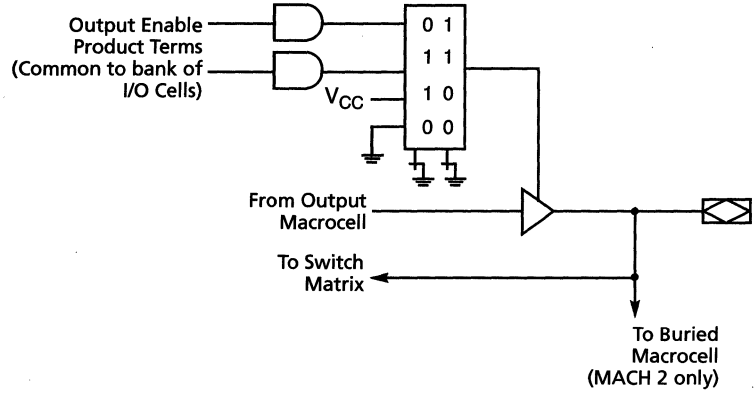


Figure 7. I/O Cell

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The unique MACH 1 & 2 architecture is designed for high performance—a metric that is met in both raw speed, and even more importantly, **guaranteed fixed speed**. The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other non-Vantis CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits (Figure 8). Speed *and* SpeedLocking combine to give designers easy access to the performance required in today's designs.

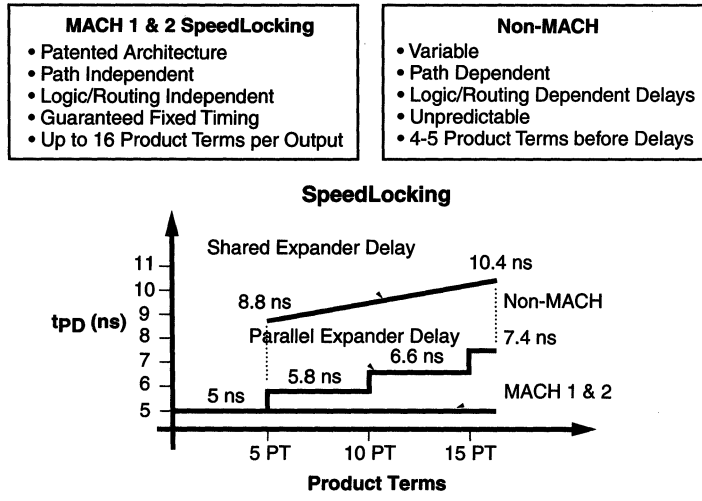


Figure 8. Timing in MACH 1 & 2 vs. Non-MACH Devices

JTAG IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACHxxxSP devices provide in-system programming (ISP) capability through their JTAG ports. This capability has been implemented in a manner that insures that the JTAG port remains compliant to the IEEE 1149.1 standard. By using JTAG as the communication interface through which ISP is achieved, customers benefit from a standard, well-defined interface.

MACHxxxSP devices can be programmed across the commercial temperature and voltage range. These devices tristate the outputs during programming. Vantis provides its free PC-based VantisPRO software to facilitate in-system programming. VantisPRO software takes the JEDEC file output produced by Vantis' design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. VantisPRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, VantisPRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACHxxxSP devices during the testing of a circuit board. For more information about in-system programming, refer to the separate document entitled *MACH ISP Manual.*

BUS-FRIENDLY INPUTS AND I/Os

The MACH 1 & 2 inputs and I/Os include two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

PCI COMPLIANT

The MACH 1 & 2 families in -5/-6/-7/-10/-12 speed grades are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH 1 & 2 families' predictable timing ensures compliance with the PCI AC specifications independent of the design.

POWER-DOWN MODE

The MACH 1 & 2 families feature a programmable low-power mode in which individual signal paths can be programmed for low power. These low-power speed paths will be slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 75%. If all of the signals in a PAL block are in low-power mode, then the total power is reduced even further.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

All MACHxxxSP and most of the MACH 1 & 2 devices are safe for mixed supply voltage system designs. These 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they can accept inputs from other 3.3-V devices. The MACH 1 & 2 families provide easy-to-use mixed-voltage design compatibility. For more information, refer to the Technical Note entitled *Mixed Supply Design with MACH 1 & 2 SP Devices.*

POWER-UP RESET

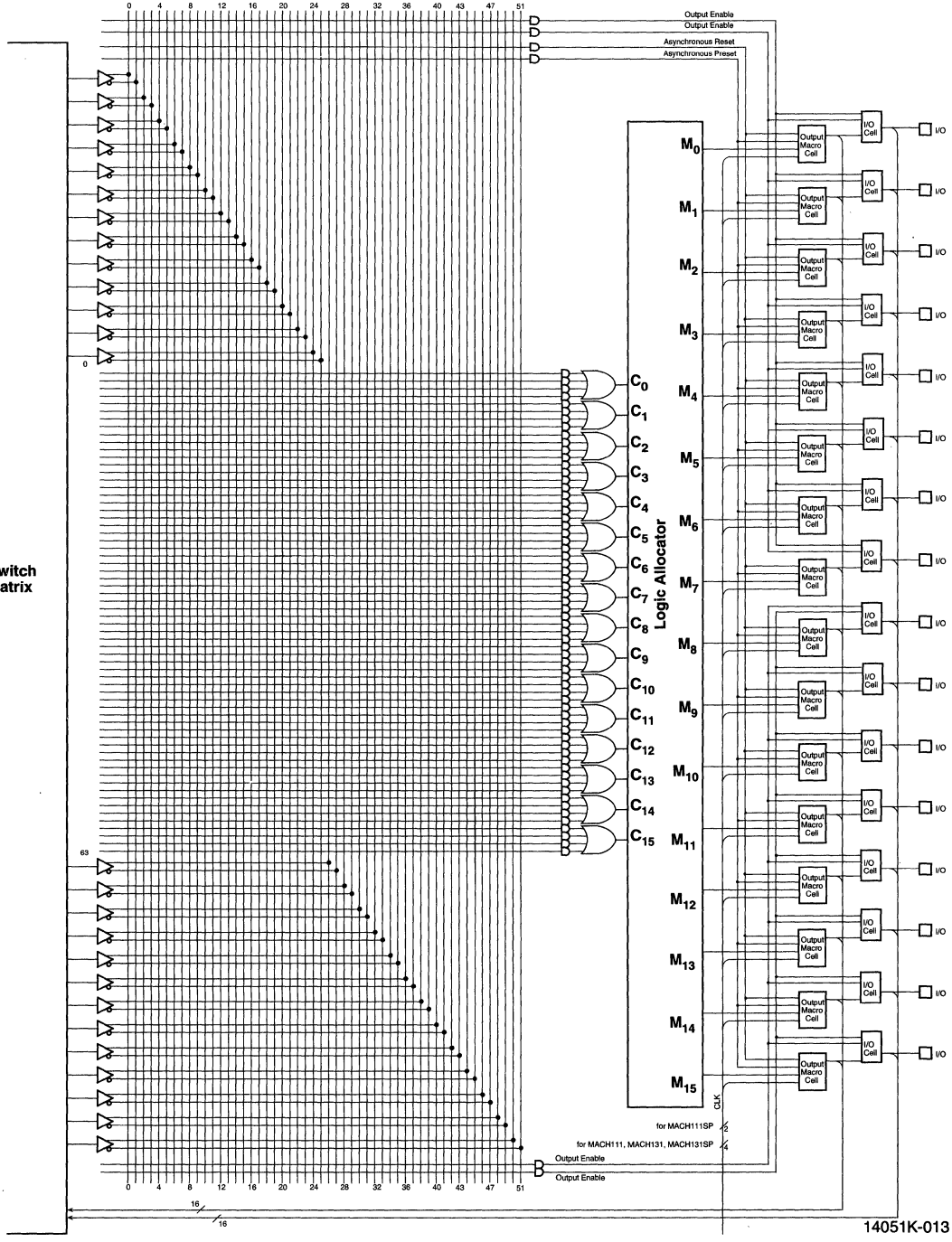
All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. To guarantee

initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

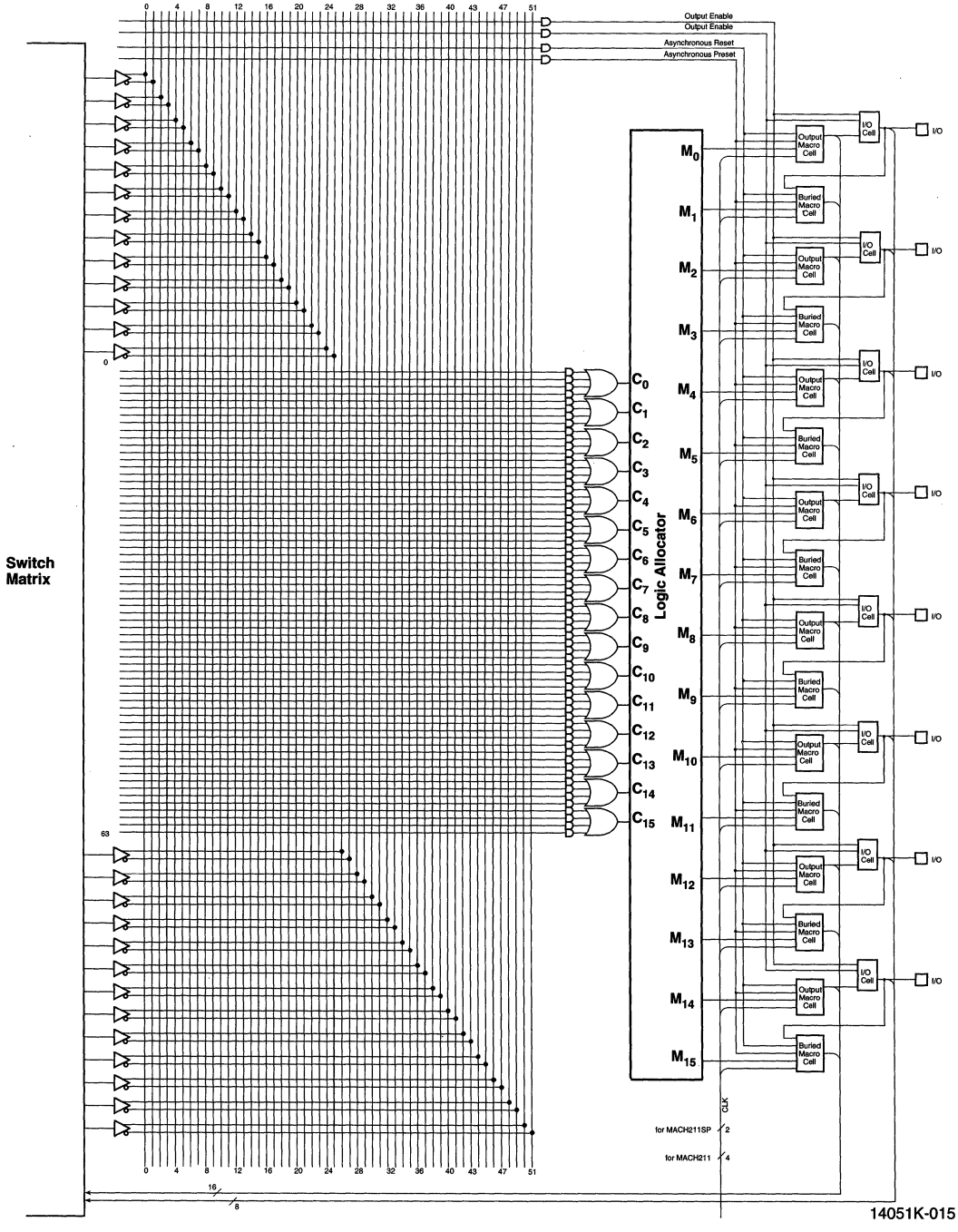
SECURITY BIT

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

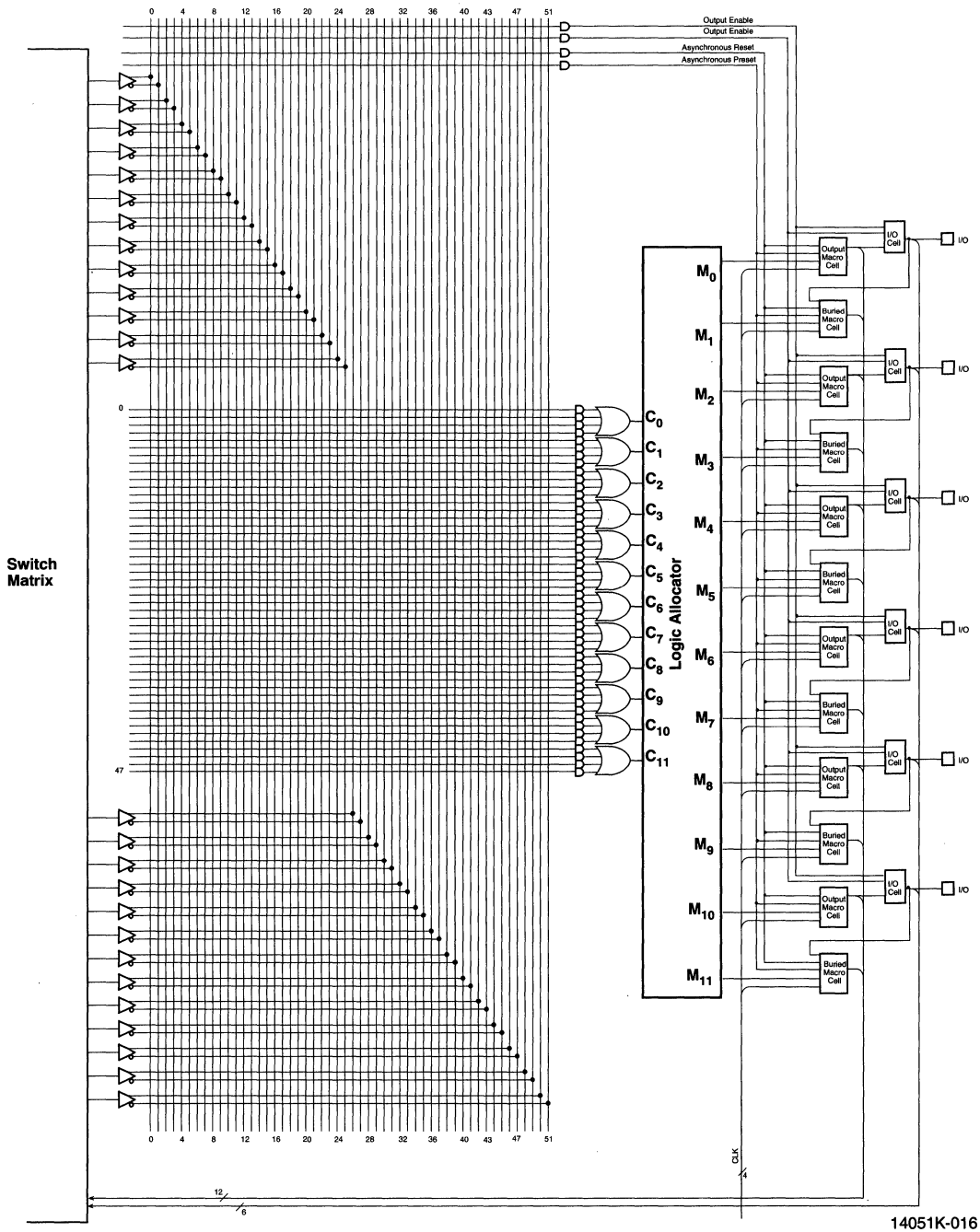
MACH111(SP) AND MACH131(SP) PAL BLOCK



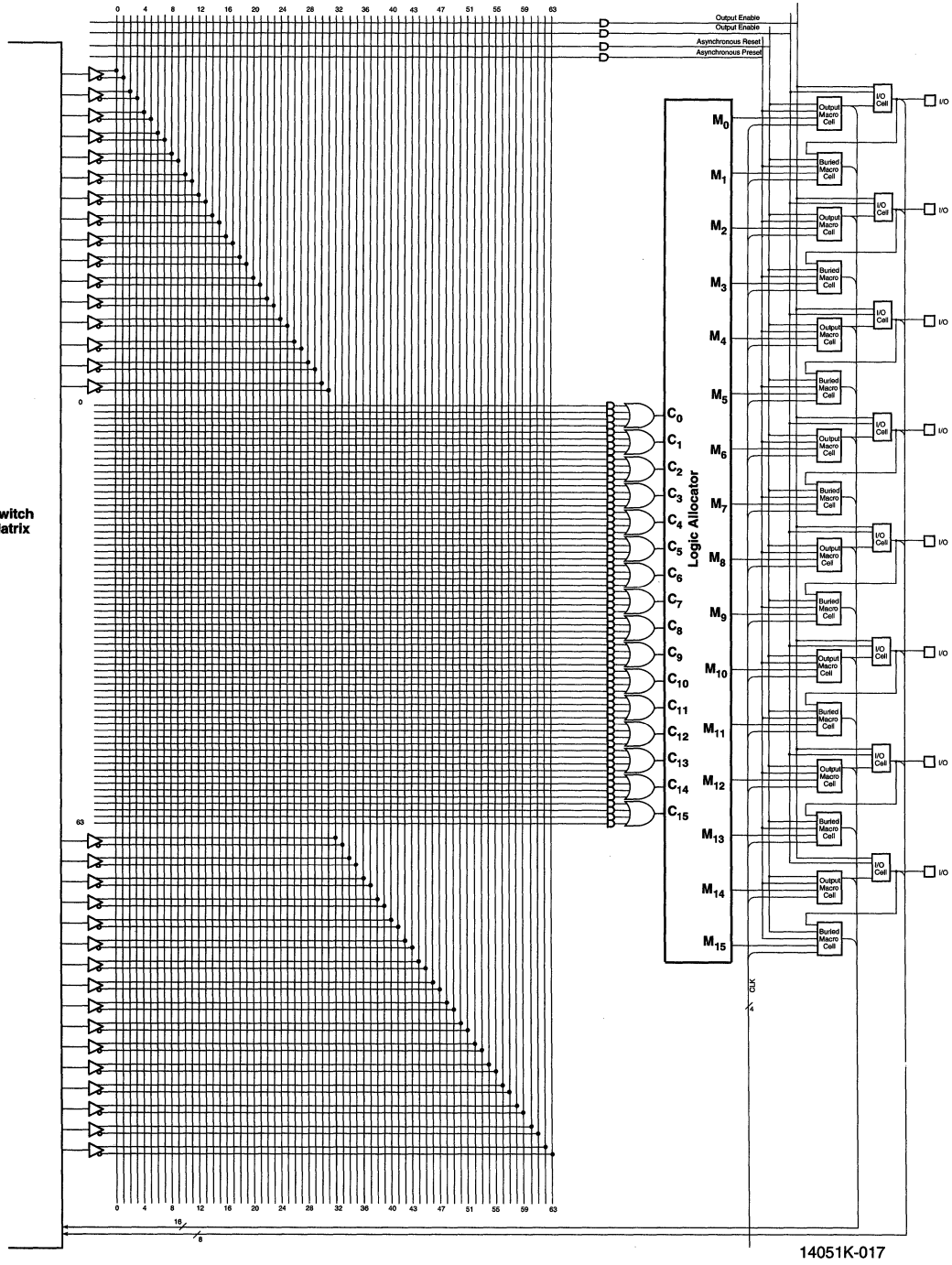
MACH211(SP) PAL BLOCK



MACH221(SP) PAL BLOCK



MACH231(SP) PAL BLOCK



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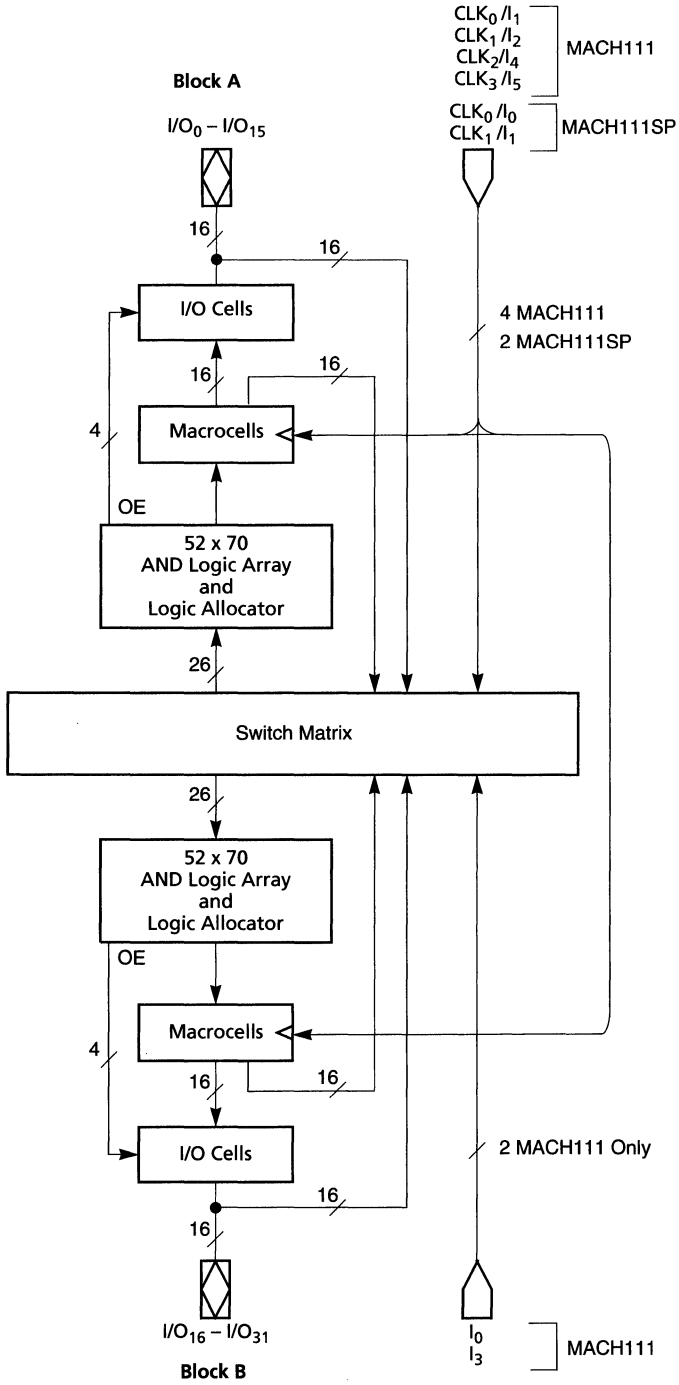
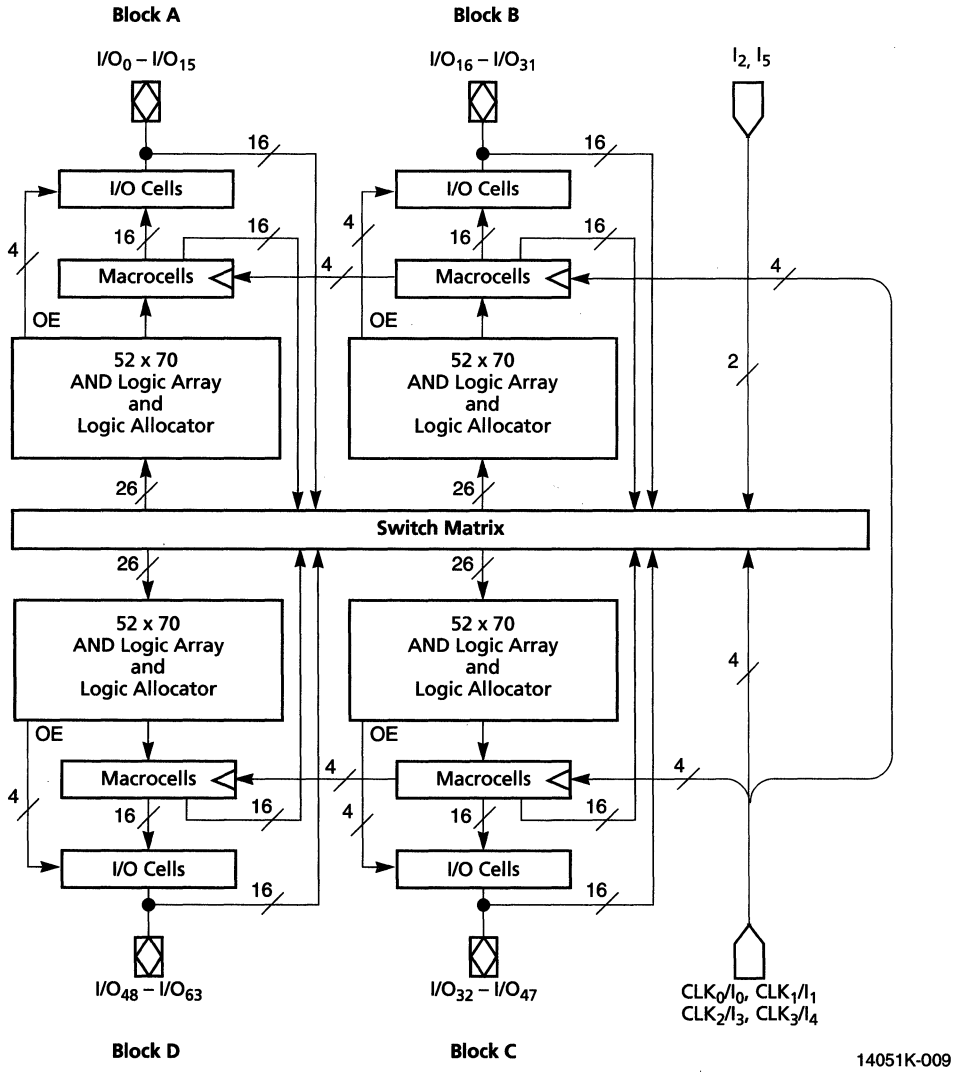
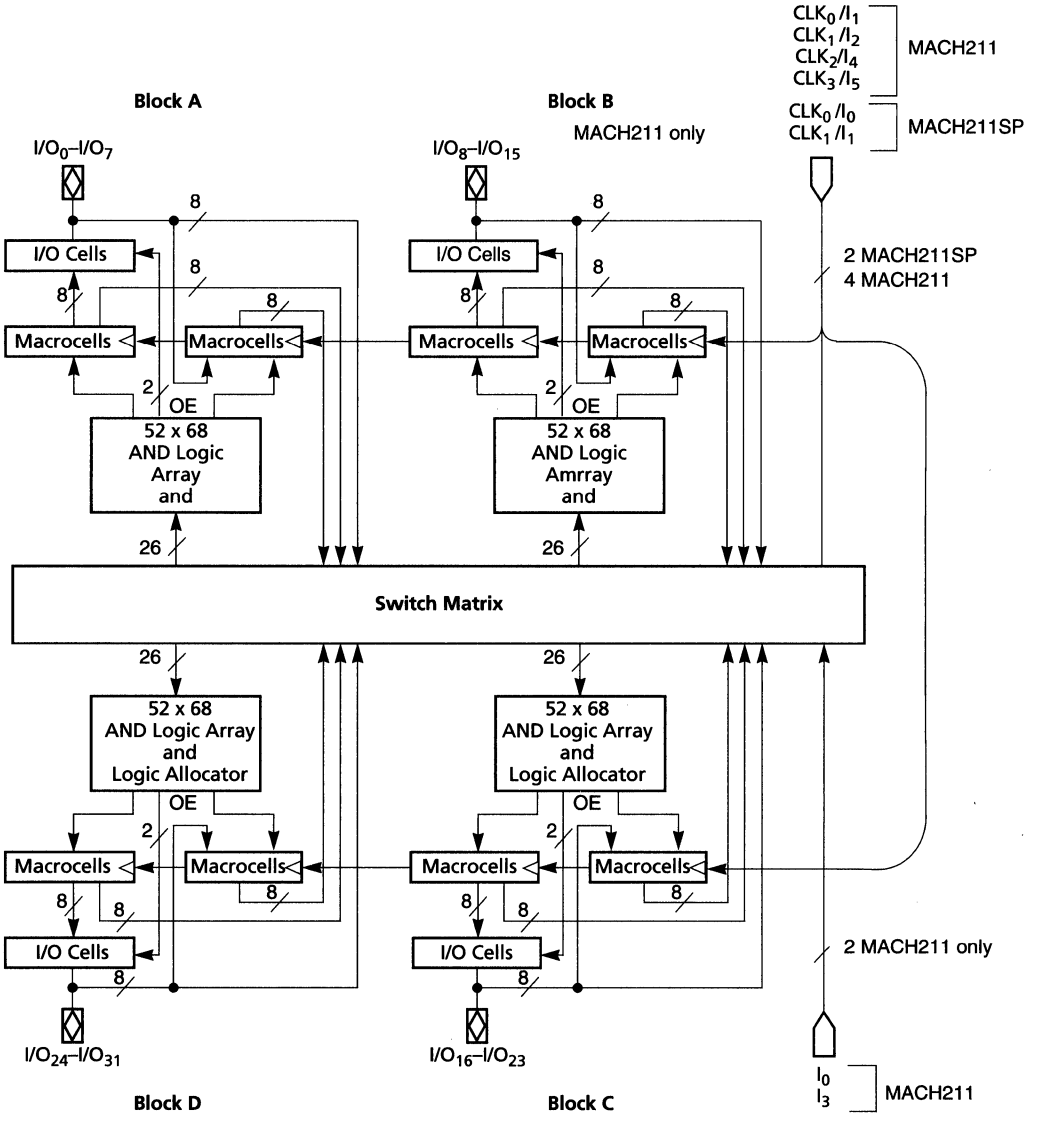
BLOCK DIAGRAM (MACH111, MACH111SP)



BLOCK DIAGRAM (MACH131, MACH131SP)

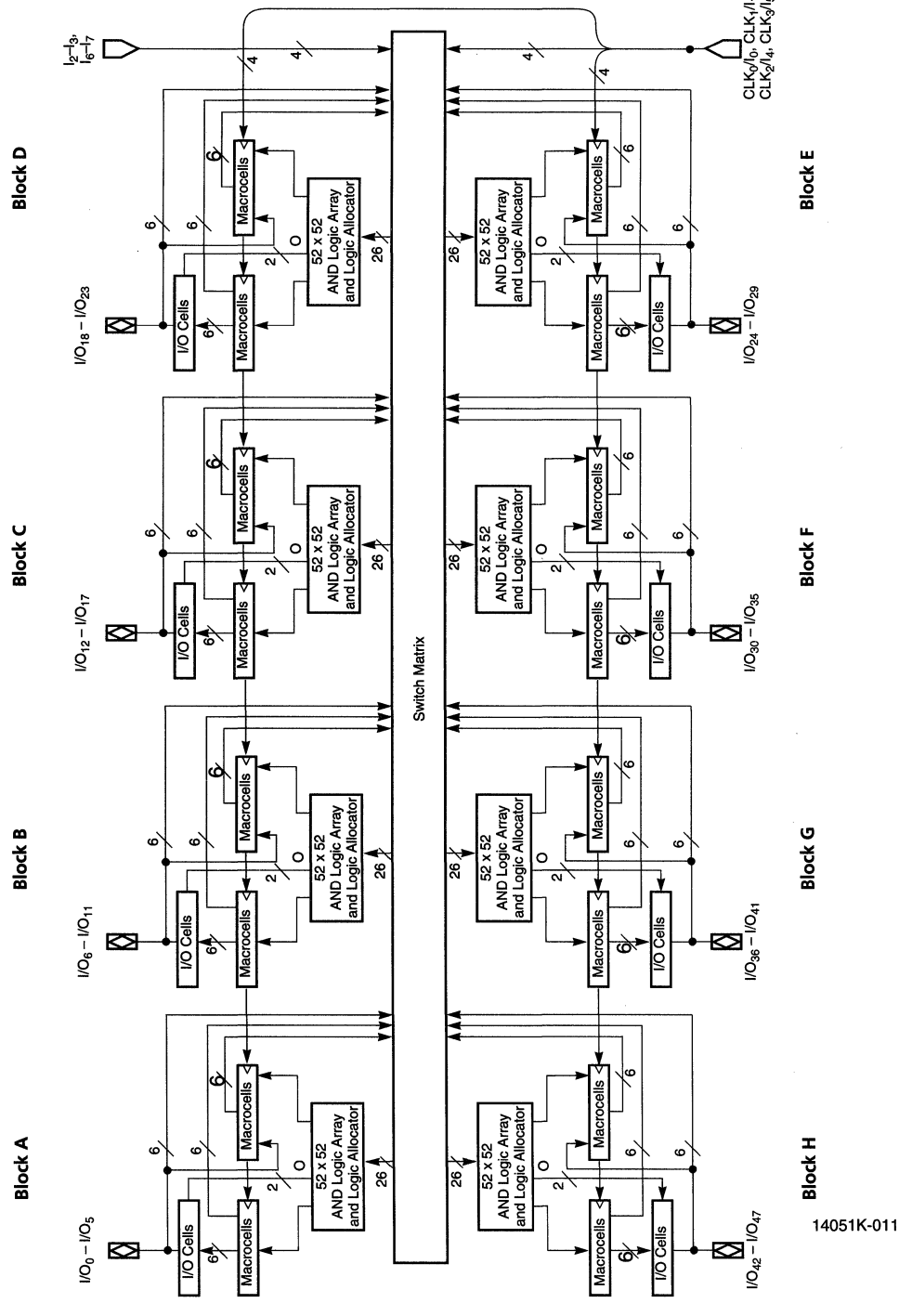


BLOCK DIAGRAM (MACH211, MACH211SP)

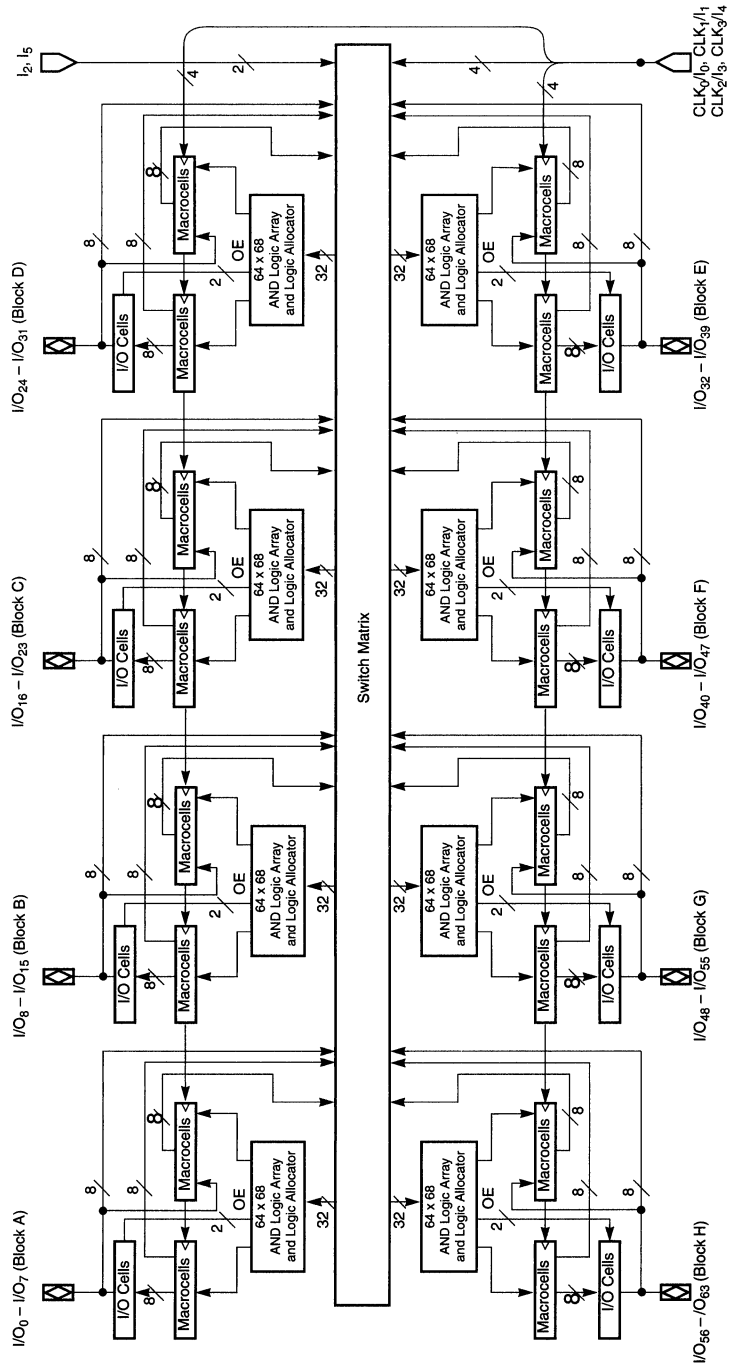


14051K-010

BLOCK DIAGRAM (MACH221, MACH221SP)



BLOCK DIAGRAM (MACH231, MACH231SP)



14051K-012

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
With Power Applied . . . . . -55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage . . -0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = –300 µA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 1)			3.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 2)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 5)	–30		–130 (Note 6), –160	mA

Notes:

1. *This applies to MACH111SP, MACH131SP, and die code "B" or later for MACH211(SP) and MACH231(SP). This does not apply to MACH111, MACH131, MACH221(SP), and die code "A" for MACH211(SP) and MACH231(SP).*
2. *Total I_{OL} for one PAL block should not exceed 64 mA.*
3. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
6. *For commercial temperature range only.*

MACH111 AND MACH111SP

SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-5		-7		-10		-12		-14		-15		-18		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				5		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	3.5		5.5		6.5		7		8.5		10		12		ns
			T-type	4		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time			0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output				3.5		5		6		8		10		10		12	ns
t_{WL}	Clock Width		LOW	2.5		3		5		6		6		6		7.5		ns
t_{WH}			HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback $1/(t_S + t_{CO})$	D-type	143		95		80		66.7		54		50		42		MHz
			T-type	133		87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})	D-type	182		133		100		76.9		69		66.6		53		MHz
			T-type	167		125		91		71.4		57		55.5		44		MHz
		No Feedback $1/(t_{WL} + t_{WH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{AR}	Asynchronous Reset to Registered Output				7.5		9.5		11		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)			4.5		5		7.5		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)			4.5		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered Output				7.5		9.5		11		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)			4.5		5		7.5		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)			4.5		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable				7.5		9.5		10		12		14.5		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable				7.5		9.5		10		12		14.5		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)				10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)				7		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)				3		3		3		3		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)				10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

MACH131 AND MACH131SP

SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description				-5		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					5.5		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback			D-type	3.0		5.5		6.5		7		8.5		10		12		ns
				T-type	3.5		6.5		7.5		8		10		11		13.5		ns
t_H	Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					4		5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	143		95		80		66.7		54		50		42		MHz
				T-type	133		87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	182		133		100		76.9		69		66.6		53		MHz
				T-type	167		125		91		71.4		57		55.5		44		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		125		83.3		83.3		83.3		66.7		MHz
t_{AR}	Asynchronous Reset to Registered Output					8.5		9.5		11		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered Output					8.5		9.5		11		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					7.5		9.5		10		12		14.5		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					7.5		9.5		10		12		14.5		15		18	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3		3		3		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book..*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

MACH211 AND MACH211SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-6		-7		-10		-12		-14		-15		-18		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				6		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	5		5.5		6.5		7		8.5		10		12		ns
			T-type	5.5		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time			0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output				4		4.5		6		8		10		10		12	ns
t_{WL}	Clock Width		LOW	2.5		3		5		6		6		6		7.5		ns
t_{WH}			HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback $1/(t_S + t_{CO})$	D-type	111		100		80		66.7		54		50		42		MHz
			T-type	105		91		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})	D-type	166		133		100		83.3		69		66.6		55.6		MHz
			T-type	150		125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback $1/(t_{WL} + t_{WH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			5		5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time			0		0		0		0		0		0		0		ns
t_{GO}	Gate to Output				7		7 7.5 (note 4)		7 8 (note 5)		10		11		11		13 (note 6) 13.5	ns
t_{GWL}	Gate Width LOW			2.5		3		5		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				9		9.5		12		14		17		17		20 (note 6) 20.5	ns
t_{SIR}	Input Register Setup Time			1.5		2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time			1.5		2		2		2		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				10		11		13		15		18		18		20 (note 6) 22	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	8		9		10		12		14.5		15		18		ns
			T-type	9		10		11		13		16		16		19.5		ns
t_{WICL}	Input Register Clock Width		LOW	2.5		3		5		6		6		6		7.5		ns
t_{WICH}			HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time			1.5		2		2		2		2		2		2.5		ns
t_{HIL}	Input Latch Hold Time			1.5		2		2		2		2.5		2.5		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				12		12		14		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				13		14		16		19		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			7		7.5		8.5		9		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			9		10		11		13		16		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW			2.5		3		5		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches				12		12.5		14		16		19		19		23	ns

MACH211 AND MACH211SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description	-6		-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		9		9.5		15		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)	4		5		10		10		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9		9.5		15		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)	4		5		10		10		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9		9.5		10		12		14		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9		9.5		10		12		14		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*
4. *MACH211 t_{GO} = 7 ns. MACH211SP t_{GO} = 7.5 ns.*
5. *MACH211, commercial t_{GO} = 7 ns.*
6. *The faster -18 t_{GO}, t_{PDL}, t_{ICO}, apply to MACH211 only, not MACH211SP.*

MACH221 and MACH221SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description				-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5.5		6.5		7		8.5		10		12		ns
				T-type	6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		ns
t_{CO}	Clock to Output					5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	3		5		6		6		6		7.5		ns
t_{WH}				HIGH	3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	95		80		66.7		54		50		42		MHz
				T-type	87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	133		100		83.3		69		66.6		55.6		MHz
				T-type	125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		167		100		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		0		ns
t_{GO}	Gate to Output					7		7 (note 2)		10		11		11		13.5	ns
t_{GWL}	Gate Width LOW				3		5		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9.5		12		14		17		17		20.5	ns
t_{SIR}	Input Register Setup Time				2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time				2		2		2		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					11		13		15		18		18		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	9		10		12		14.5		15		18		ns
				T-type	10		11		13		16		16		19.5		ns
t_{WICL}	Input Register			LOW	3		5		6		6		6		7.5		ns
t_{WICH}	Clock Width			HIGH	3		5		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		167		100		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		2		2		2.5		ns
t_{HIL}	Input Latch Hold Time				2		2		2		2.5		2.5		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					12		14		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					14		16		19		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				7.5		8.5		9		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				10		11		13		16		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW				3		5		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					11.5		14		16		19		19		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output					9.5		15		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 3)				5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				5		8		10		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output					9.5		15		16		19.5		20		24	ns

MACH221 and MACH221SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description	-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{APW}	Asynchronous Preset Width (Note 3)	5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	5		8		10		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9.5		12		12		14		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		12		12		14		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 4)		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuits" in the General Information section of the Vantis 1999 Data Book.*
2. *MACH221 t_{GO} = 7 ns. MACH221SP t_{GO} = 8 ns.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
4. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

MACH231 AND MACH231SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description				-6		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					6		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5		5.5		6.5		7		8.5		10		12		ns
				T-type	6		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					4		5		6.5		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	111		95		77		66.7		54		50		42		MHz
				T-type	100		87		72		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	166		133		100		83.3		69		66.6		55.6		MHz
				T-type	150		125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		125		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5		5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		0		0		ns
t_{GO}	Gate to Output					5		6		7.5		8.5		11		11		13.5	ns
t_{GWL}	Gate Width LOW				2		3		4		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9		9.5		14		14.5		17		17		20.5	ns
t_{SIR}	Input Register Setup Time				1.5		2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time				1.5		2		2.5		2.5		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					10		11		15.5		16		18		18		22	ns
t_{ICS}	Input Register Clock to output Register Setup			D-type	8		9		11		12		14.5		15		18		ns
				T-type	9		10		12		13		16		16		19.5		ns
t_{WICL}	Input Register Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WICH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency				200		167		125		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time				1.5		2		2		2.5		2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				1.5		2		2.5		3		3		3		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					11		12		17		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					13		14		18		19.5		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				7		7.5		10		10.5		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				9		10		11		13.5		16		16		19.5		ns

MACH231 AND MACH231SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description	-6		-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	2		3		4		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11		12.5		16		17		19		19		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9		9.5		13		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)	4		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9		9.5		13		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)	4		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9		9.5		10		12		15		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9		9.5		10		12		15		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		6		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V		8	pF

Note:

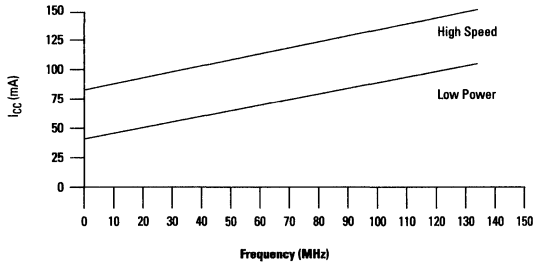
1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.*

I_{CC} vs. FREQUENCY

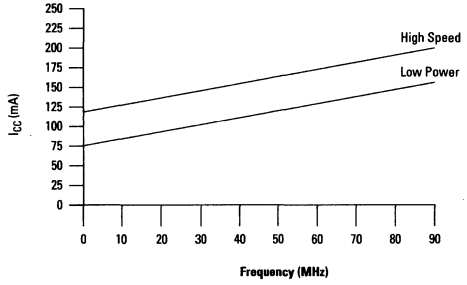
These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register.

T_A = 25°C, V_{CC} =5V

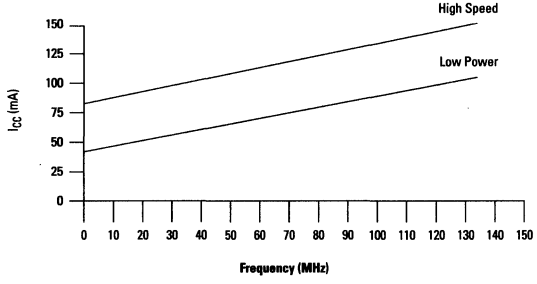
MACH111(SP)



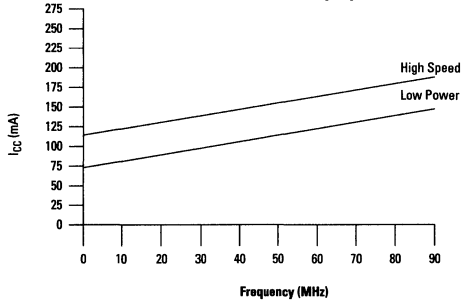
MACH131(SP)



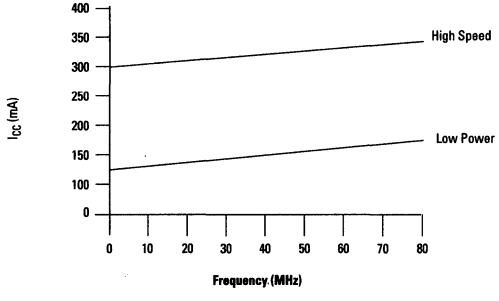
MACH211(SP)



MACH 221(SP)



MACH231



MACH231SP

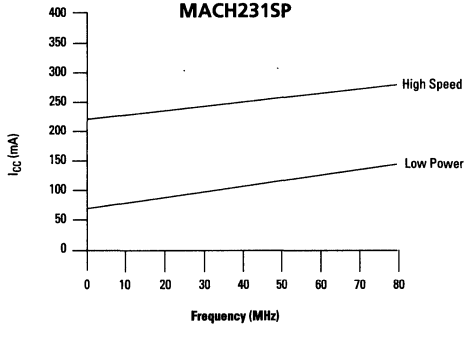


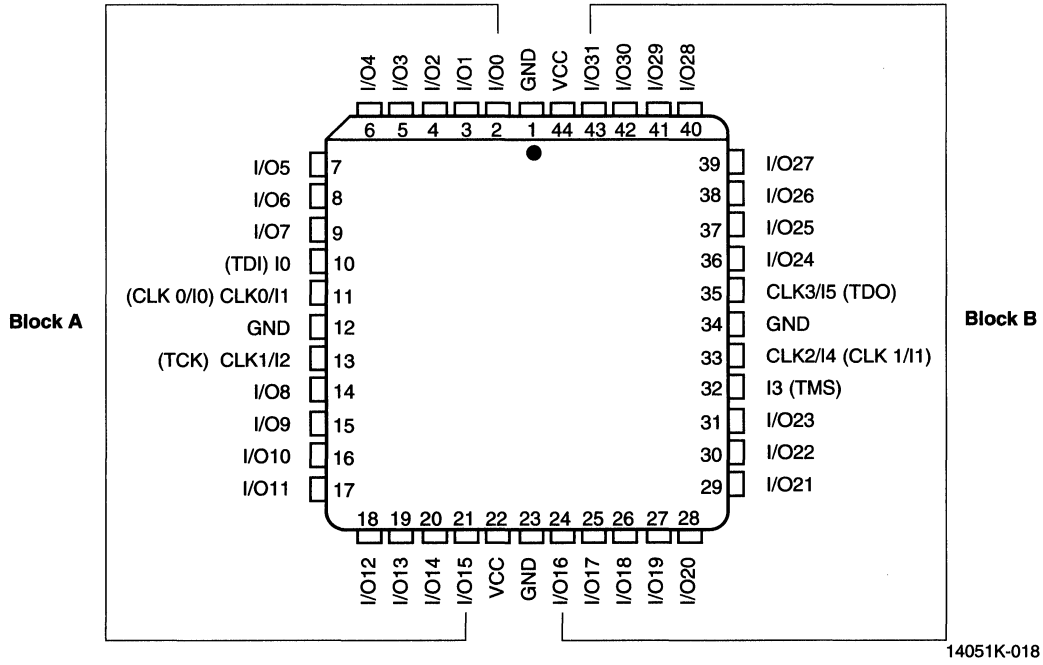
Table 12. I_{CC}

Device	Parameter Symbol	Parameter Description	Test Description	Typ	Unit
MACH111(SP) MACH211(SP)	I_{CC}	Supply Current (Static)	V_{CC} = 5V, T_A = 25°C, f = 0 MHz	40	mA
MACH221(SP)				70	
MACH131(SP)				75	
MACH231SP				80	
MACH231				135	
MACH111(SP) MACH211(SP)		Supply Current (Active)	V_{CC} = 5V, T_A = 25°C, f = 1 MHz	45	
MACH221(SP)				75	
MACH131(SP)				80	
MACH231SP				100	
MACH231				150	

CONNECTION DIAGRAM (MACH111-5/7/10/12/15 AND MACH111SP-5/7/10/12/15)

Top View

44-Pin PLCC



14051K-018

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

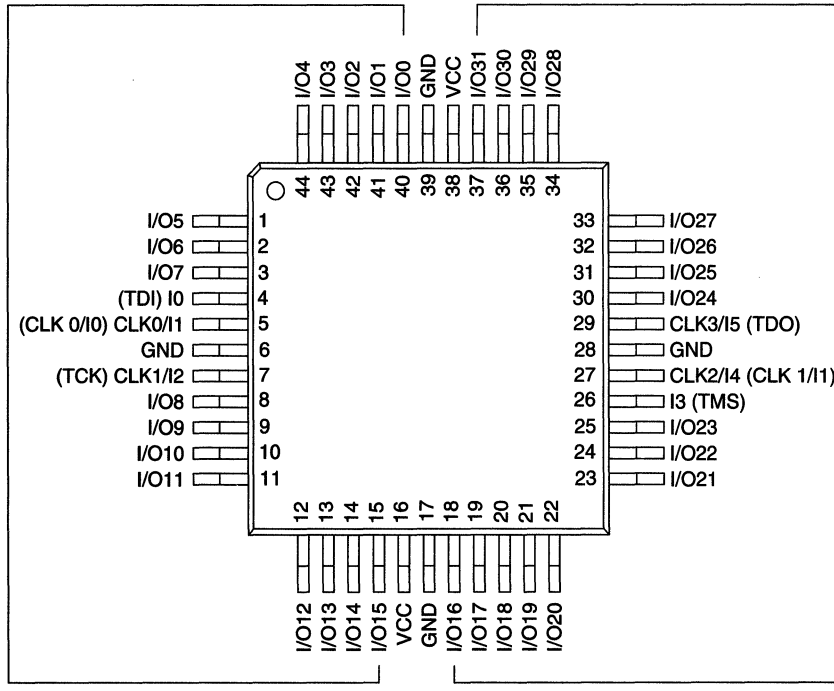
Note:

1. Pin designators in parentheses ( ) apply to the MACH111SP

CONNECTION DIAGRAM (MACH111-5/7/10/12/15 AND MACH111SP-5/7/10/12/15)

Top View

44-Pin TQFP



PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

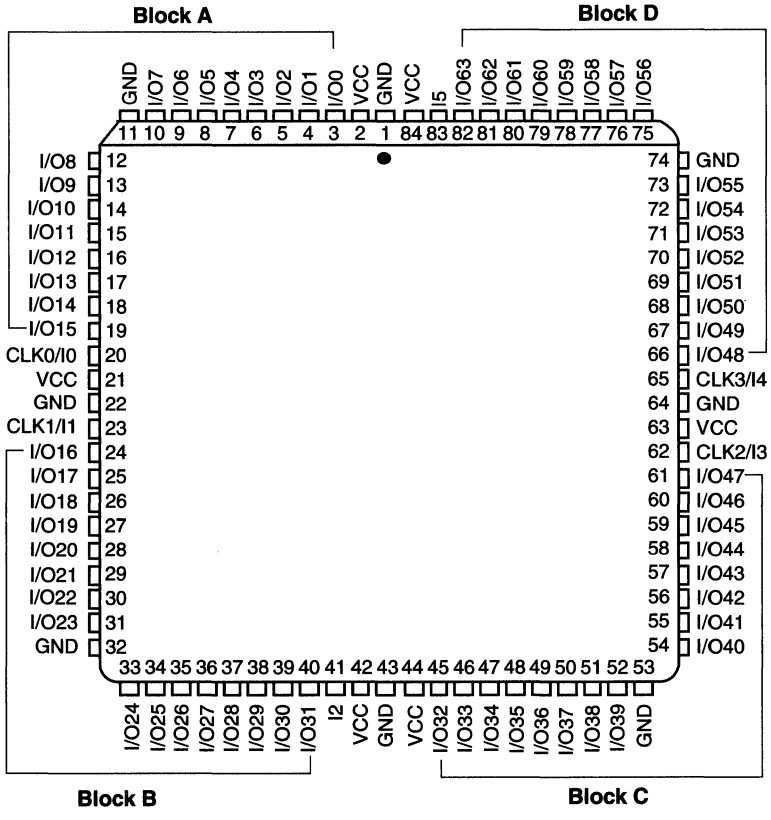
Note:

1. Pin designators in parentheses ( ) apply to the MACH111SP

CONNECTION DIAGRAM (MACH131-5/7/10/12/15)

Top View

84-Pin PLCC



14051K-020

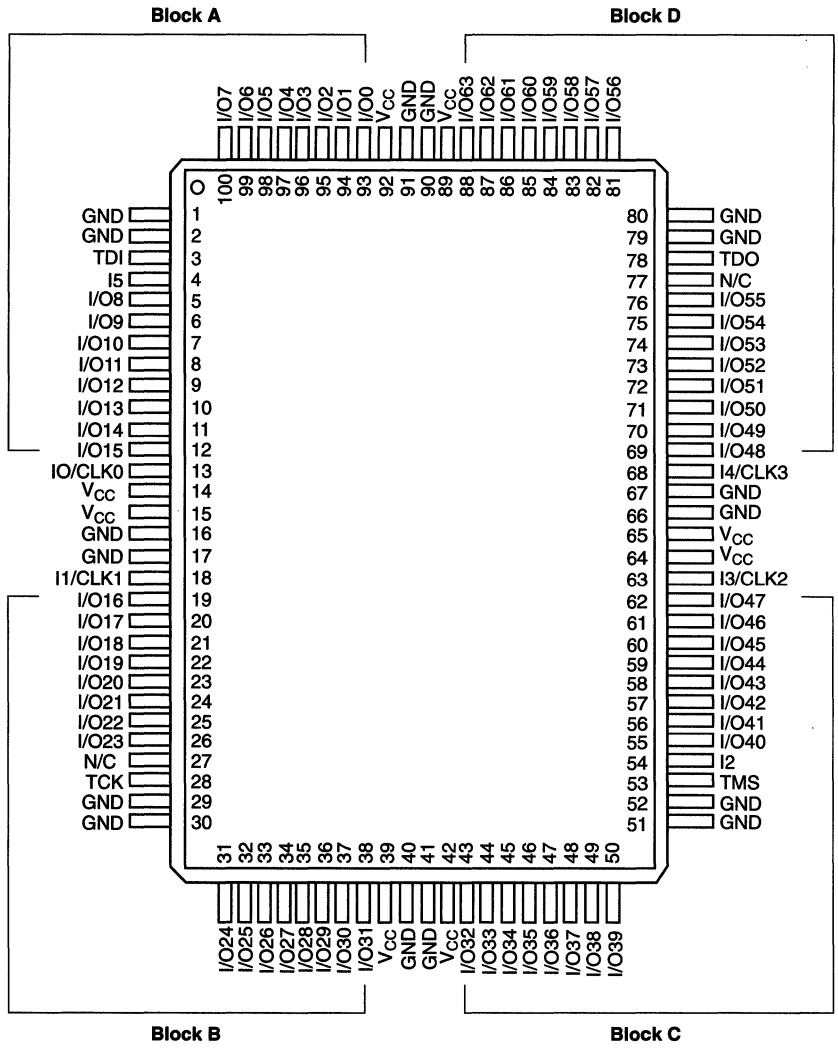
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

CONNECTION DIAGRAM (MACH131SP-5/7/10/12/15)

Top View

100-Pin PQFP



14051K-021

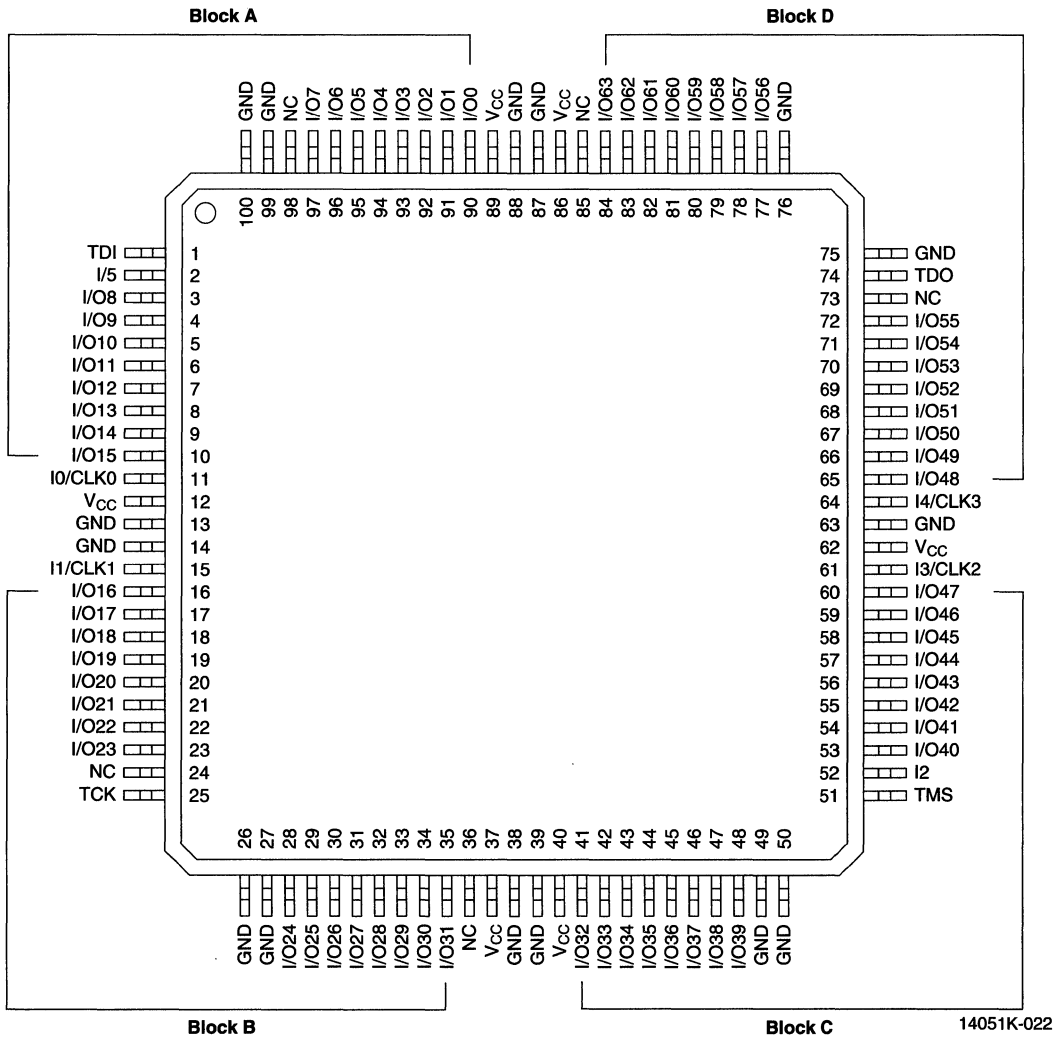
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (MACH131SP-5/7/10/12/15)

Top View

100-Pin TQFP



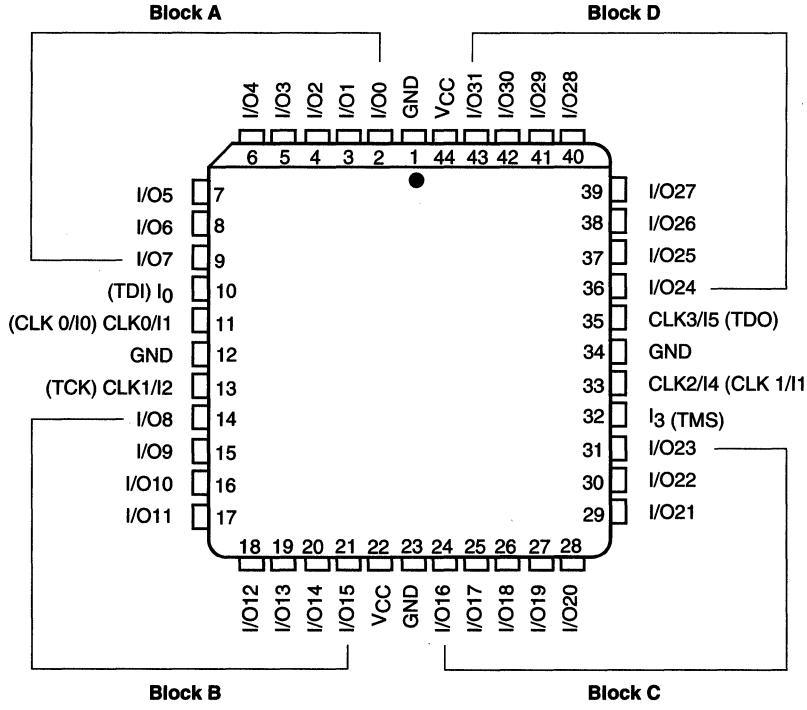
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (MACH211-7/10/12/15 AND MACH211SP-6/7/10/12/15)

Top View

44-Pin PLCC



14051K-023

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

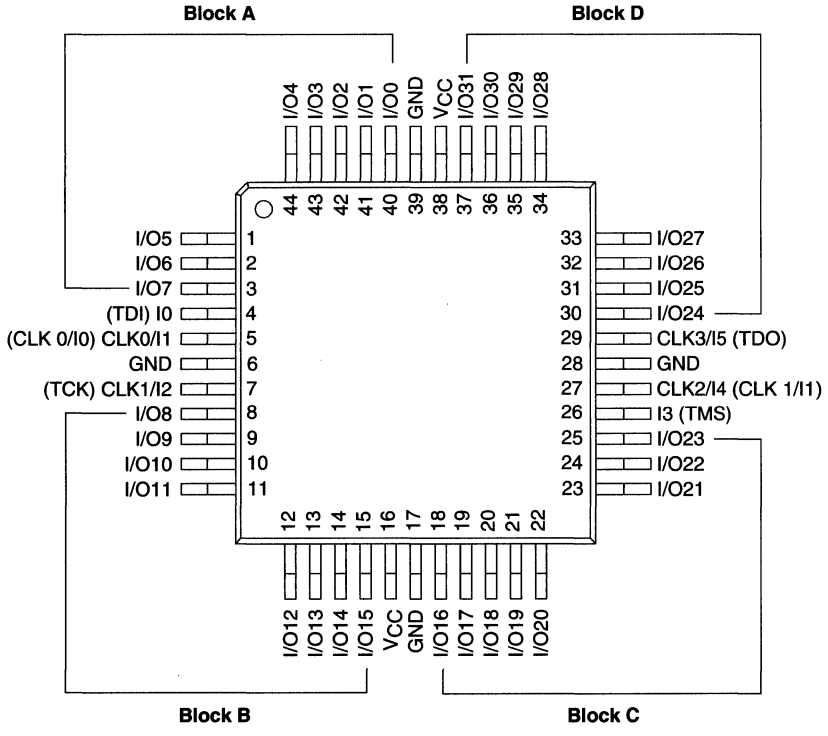
Note:

1. Pin designators in parentheses ( ) apply to the MACH211SP

CONNECTION DIAGRAM (MACH211-7/10/12/15 AND MACH211SP-6/7/10/12/15)

Top View

44-Pin TQFP



14051K-024

PIN DESIGNATIONS

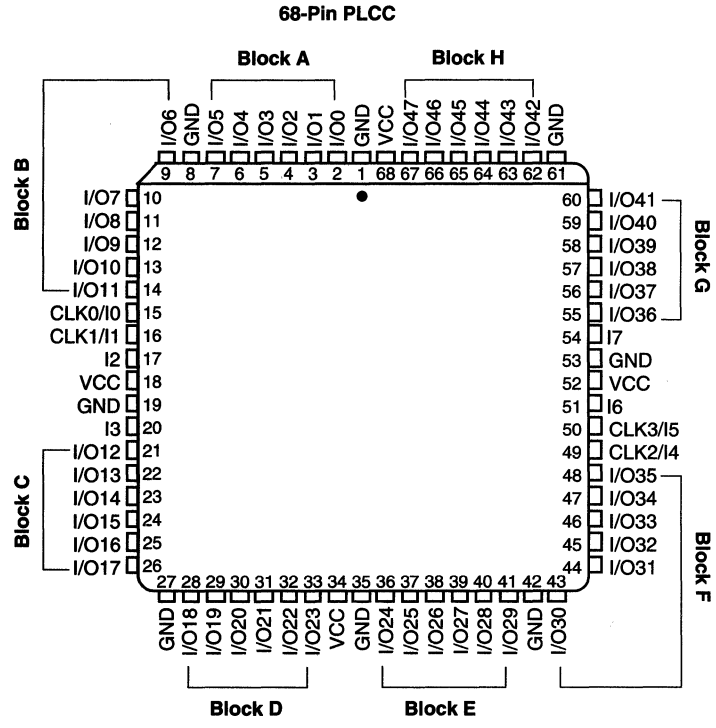
CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

Note:

1. Pin designators in parentheses ( ) apply to the MACH211SP

CONNECTION DIAGRAM (MACH221-7/10/12/15)

Top View



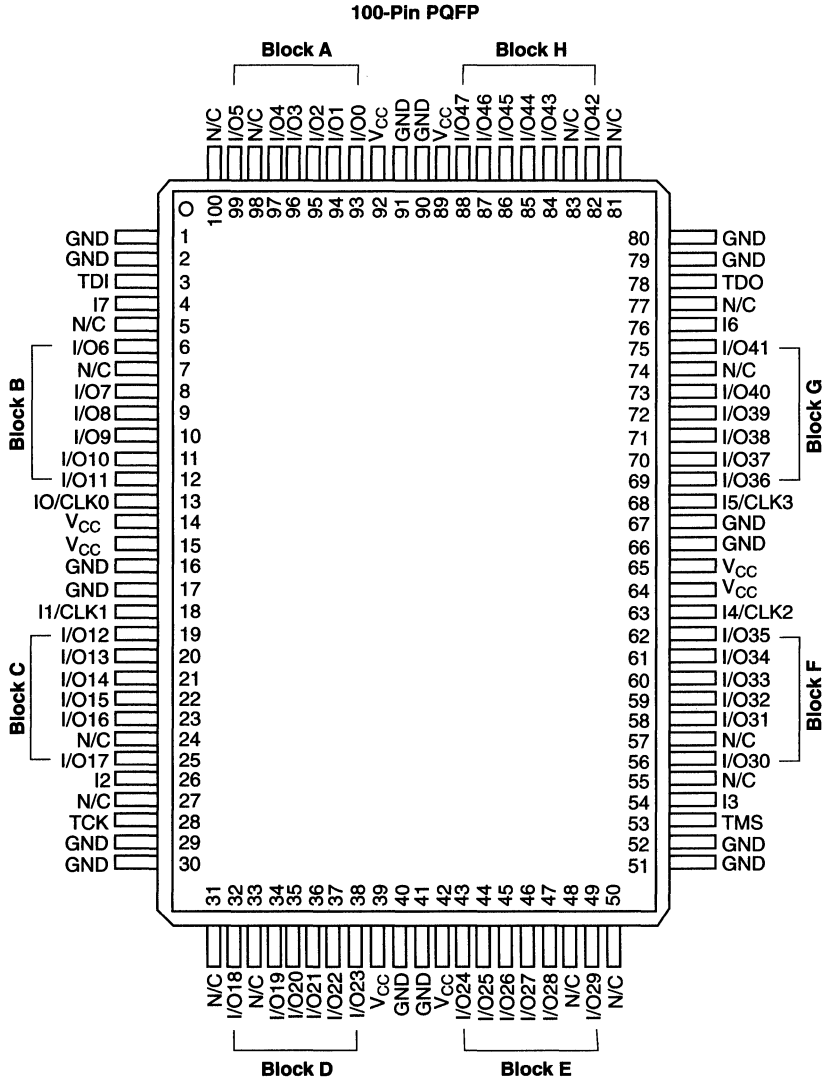
14051K-025

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

CONNECTION DIAGRAM (MACH221SP-7/10/12/15)

Top View



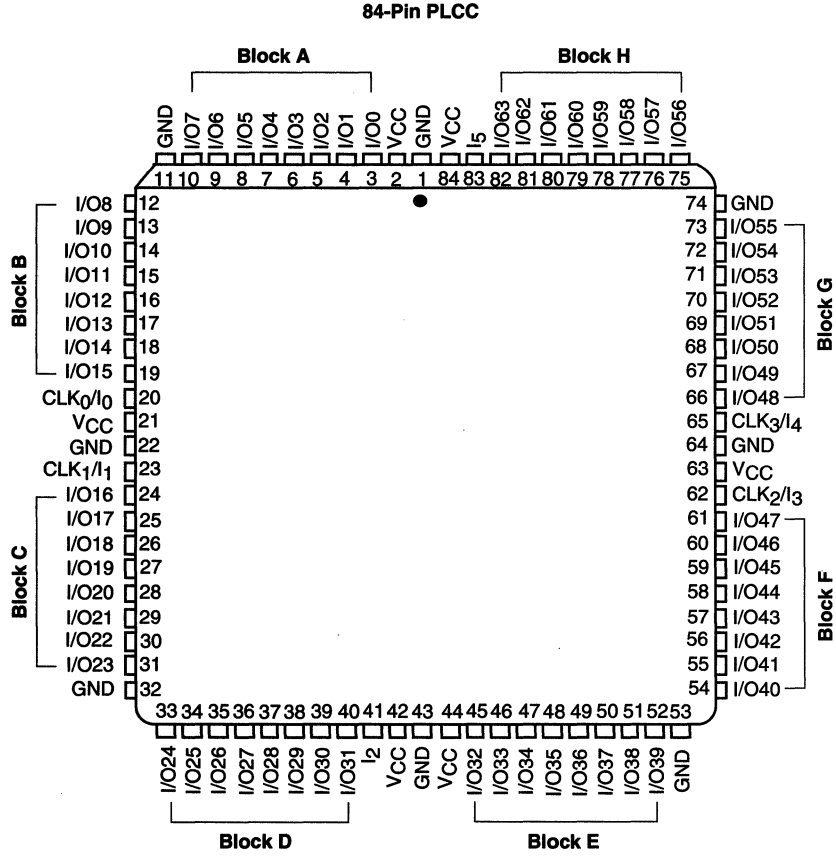
14051K-026

PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (MACH231-6/7/10/12/15)

Top View



14051K-027

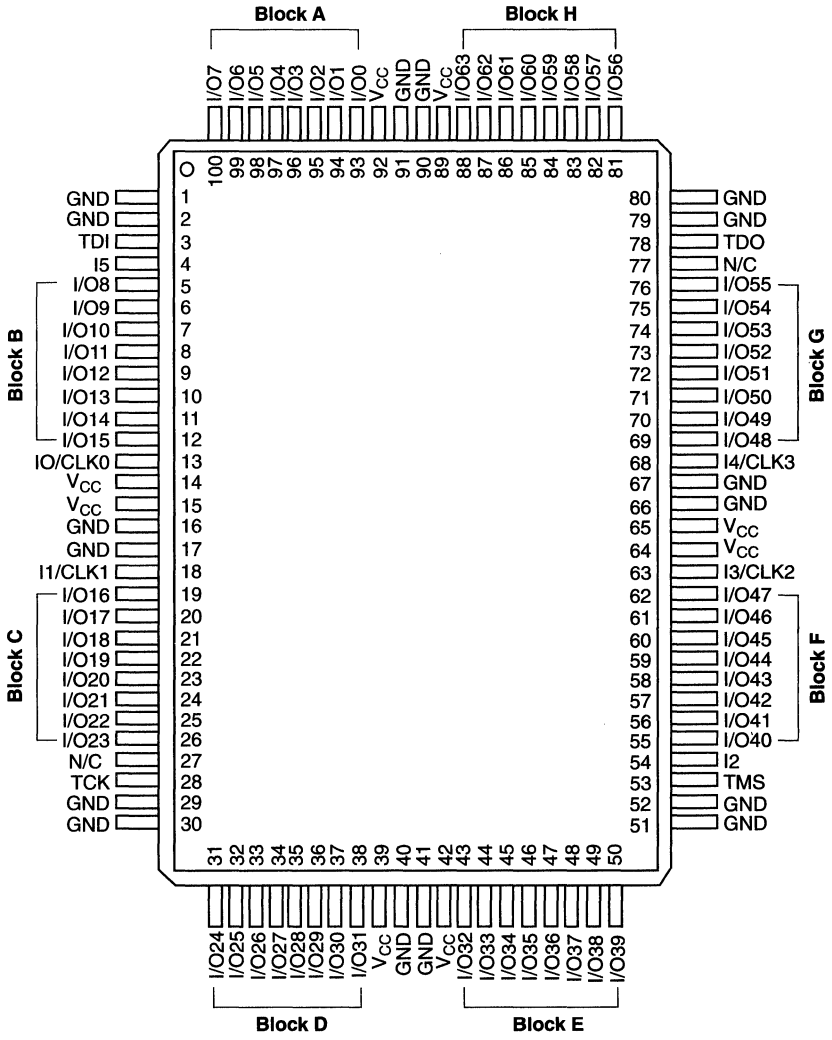
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

CONNECTION DIAGRAM (MACH231SP-10/12/15)

Top View

100-Pin PQFP



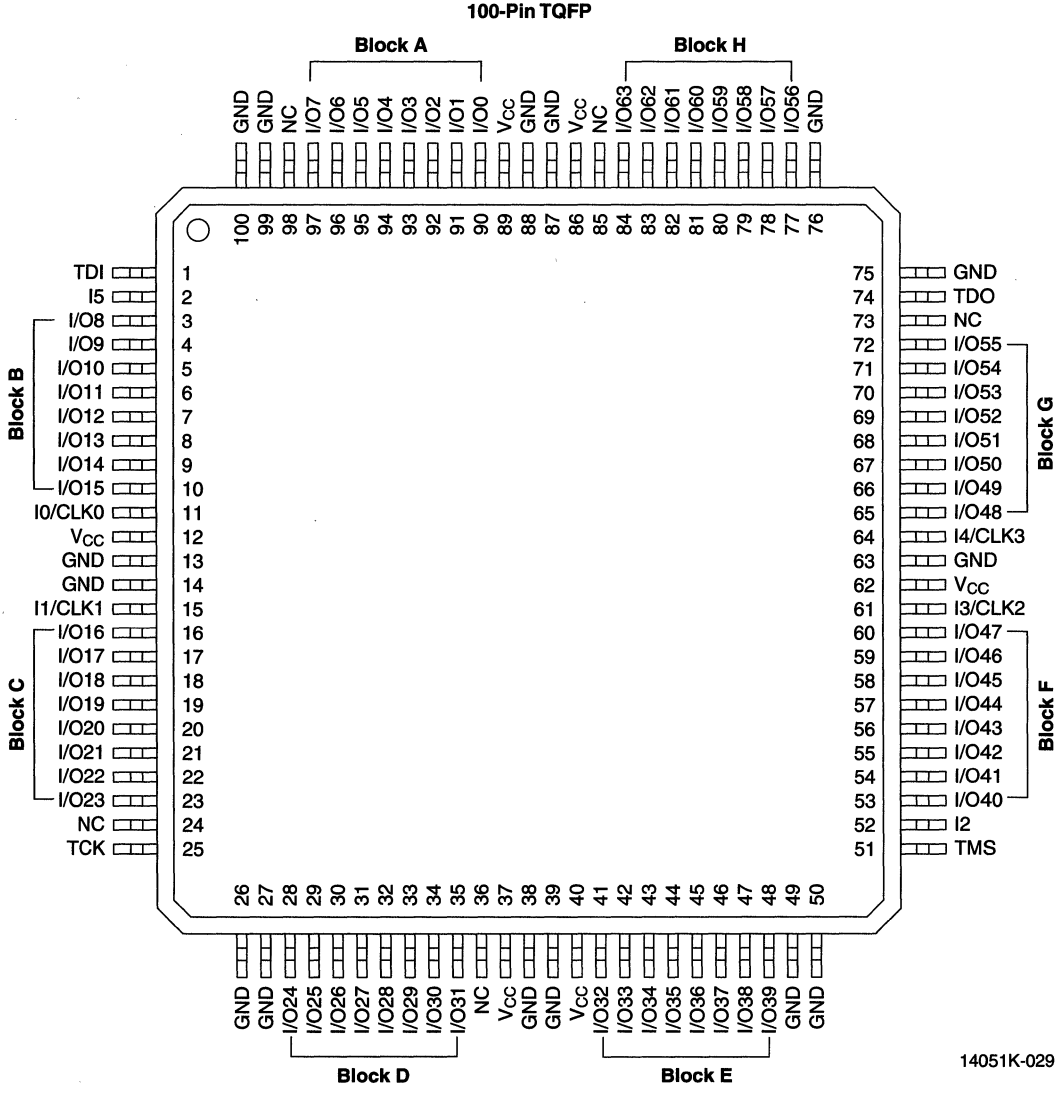
14051K-028

PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (MACH231SP-10/12/15)

Top View



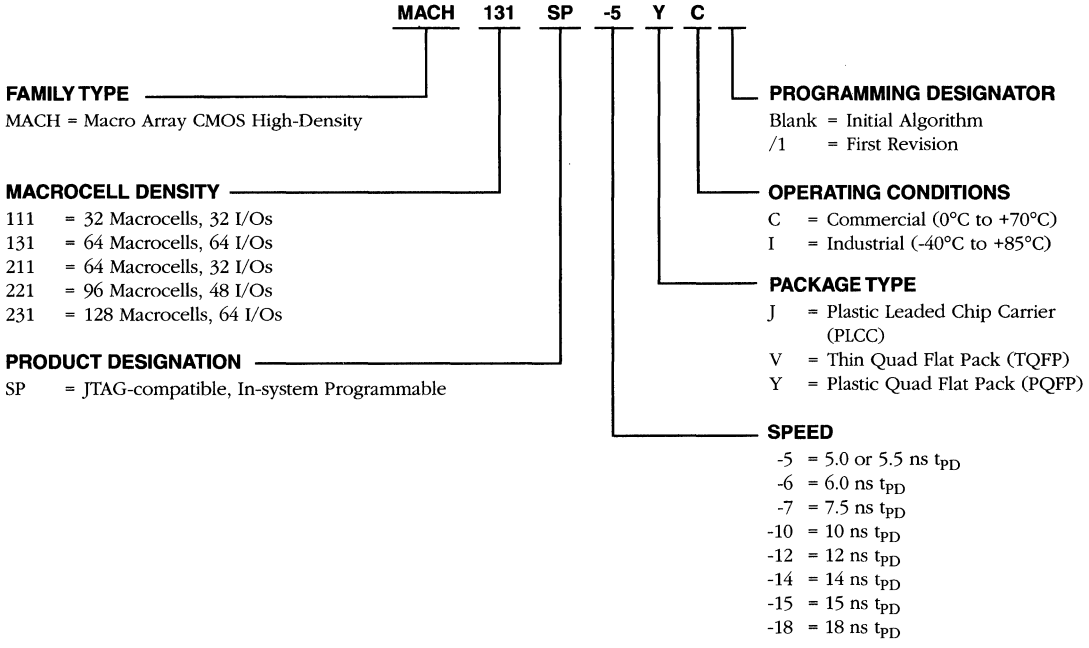
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

ORDERING INFORMATION

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations – Commercial		
MACH111	-5, -7, -10, -12, -15	JC, VC
MACH111SP	-5, -7, -10, -12, -15	JC, VC
MACH131	-5, -7, -10, -12, -15	JC/1
MACH131SP	-5, -7, -10, -12, -15	VC, YC
MACH211	-7, -10, -12, -15	JC, VC
MACH211SP	-6, -7, -10, -12, -15	JC, VC
MACH221	-7, -10, -12, -15	JC
MACH221SP	-7, -10, -12, -15	YC
MACH231	-6, -7	JC
	-10, -12, -15	JC/1
MACH231SP	-10, -12, -15	VC, YC

Valid Combinations – Industrial		
MACH111	-7, -10, -12, -14, -18	JI
MACH111SP	-7, -10, -12, -14, -18	JI
MACH131	-7, -10, -12, -14, -18	JI/1
MACH131SP	-7, -10, -12, -14, -18	YI
MACH211	-10, -12, -14, -18	JI
MACH211SP	-10, -12, -14, -18	JI
MACH221	-10, -12, -14, -18	JI
MACH221SP	-10, -12, -14, -18	YI
MACH231	-12, -14, -18	JI/1
MACH231SP	-12, -14, -18	YI

Valid Combinations

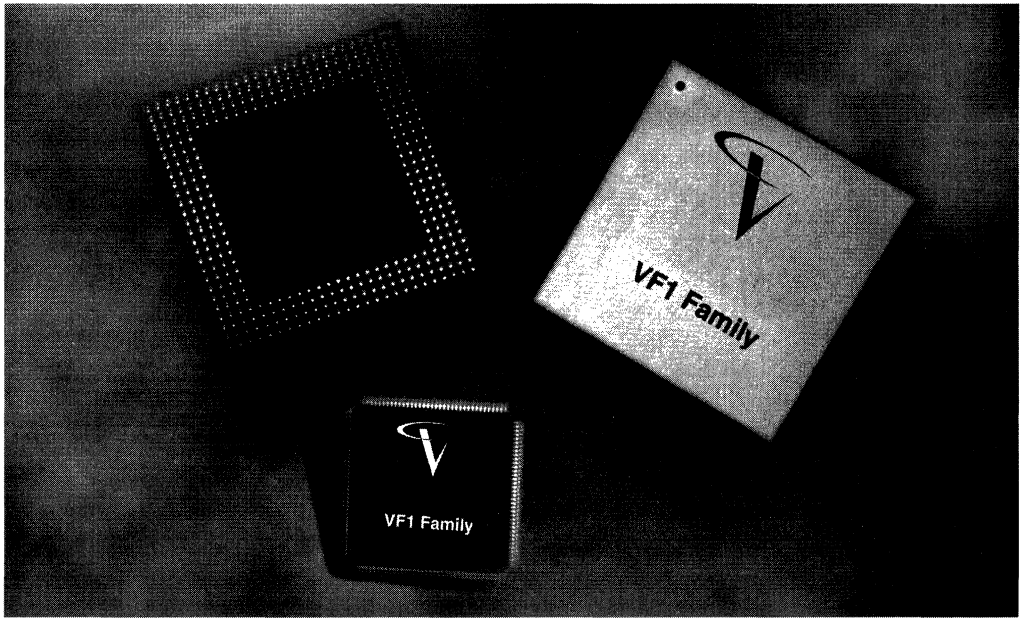
The Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note:

1. *All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e. MACH131SP-5YC-7YI*

VF1

VF1 FPGA Family



VANTIS

BEYOND PERFORMANCE

PRELIMINARY

VF1 FPGA Family

FEATURES AND BENEFITS

- **The industry's first Variable-Grain-Architecture™ enables high-density, high-performance designs for a wide range of applications**
  - — Architecture adapts to logic to enable synthesis-friendly, high-performance designs
  - — From three to six parallel inputs with all possible input combinations decoded in a single level of high-speed logic
  - — Up to 32 parallel input functions with a subset of input combinations decoded in only two logic levels
  - — Available in four sizes with 12K, 20K, 25K, and 36K gates
- **Variable-Length-Interconnect™ delivers predictable performance and First-Time-Fit™ layouts**
  - — High-speed direct connectivity minimizes connection lengths for maximum performance
  - — Variable-length connections span from two logic blocks to the entire chip, including I/Os
  - — Result is optimal length resource for every net
- **Flexible on-chip clocking options deliver up to 250MHz performance**
  - — Four low-skew global clocks minimize clock variations within the chip
  - — Two on-chip phase-locked loops (PLLS) synchronize on-chip clocks with the system clock
  - — PLLs provide 1x, 2x, and 3x frequency multiplication for on-chip clock synthesis
  - — Clocks generated on-chip may be used as global clocks
- **Vantis' hierarchical design methodology and DesignDirect™ software provide Ease-of-Success™ and First-Time-Fit**
  - — DesignDirect software supports Verilog and VHDL hardware description languages (HDLs) for design flexibility
  - — Integrates easily with a variety of third-party front-end design entry, simulation, and synthesis tools
  - — Easy-to-learn mapping and layout software coupled with fast run times and superior quality of results contribute to maximum productivity
  - — Vantis design software ensures First-Time-Fit results by examining a design prior to the place-and-route phase and determining whether or not it will fit into the chosen VF1™ FPGA
- **Pin-locking feature ensures that I/O pin assignments will not change when moving a design from one VF1 FPGA size to another or when making design changes**
  - — When making design changes or shifting density, special routing logic enables pin-locking with minimal performance degradation
  - — Allows shifting to higher or lower density FPGA without making changes to board layout
- **Zero-power Edge Connect lines allow easy implementation of NOR functions on input lines**
  - — Eight Edge Connect lines—two per side of the chip
  - — Input pins may be connected to these lines to implement NOR functions
  - — NOR functions consume zero power

Publication# **VF1003-DS-1**
Amendment/**0** Issue Date: **November 1998**

- **High-speed embedded dual-port memory simplifies the implementation of on-chip FIFOs and RAM**
  - — Needs fewer bits than single-port architectures to implement FIFOs and register stacks
  - — Minimizes access time for both read and write cycles
  - — Over 6K bits of embedded SRAM in the largest VF1 FPGA device in 32x4 configurable blocks
  - — Specific configurations may be defined by the user
- **Flexible I/O buffers allow interfacing to a wide variety of systems**
  - — I/O buffers are compatible with both 3.3V and 5V I/O levels
  - — Programmable slew rates reduce output signal over/under shoot
  - — Three-state control for I/O bus interconnections allow multiplexing on long interconnect lines
  - — PCI-compatible I/Os, coupled with optional 33MHz and 66MHz PCI buffers, allow easy interfacing to PCI buses
- **In-system programming via the built-in JTAG boundary scan port**
  - — Allows VF1 FPGAs to be programmed after mounting on a printed-circuit board
  - — Reduces the need for on-board SPROM
  - — When coupled with pin-locking, allows design changes to be made and loaded without removing the device from the board
- **Outperforms systems implemented with competitive reprogrammable FPGAs by 67% to 100%**
  - — High-performance registered I/O improves chip speed
  - — On-chip phase-locked loops with the ability to double or triple input clocks, up to 200 MHz, allows the Vantis FPGA to run up to three times faster than the system clock
  - — Embedded memory has 5ns read/write access time for fast loads and stores
  - — Pipelined logic capable of 250 MHz operation supports the development of high-performance systems

Table 1. Available Devices in the VF1 Family

Features	VF1012	VF1020	VF1025	VF1036
Typical gates	12,000	20,000	25,000	36,000
Array size (VGB)	14x14	18x18	20x20	24x24
Logic flip-flops	784	1296	1600	2304
DPSRAM blocks (32x4)	28	36	40	48
Total RAM bits	3584	4608	5120	6144
Clock pins	4	4	4	4
Maximum I/Os	168	216	240	288
Maximum I/O flip-flops	336	432	480	576

Table 2. Package Types and Total I/O Pins (including clock pins)

Packages	VF1012	VF1020	VF1025	VF1036
352 BGA			244	292
256 BGA	172	208	208	208
208 PQFP	168	168	168	168
160 PQFP	128	128		
144 TQFP	112			

OPERATIONAL DESCRIPTION

The Vantis VF1 FPGA family offers FPGA designers a level of performance that was once available only to ASIC gate array designers. The VF1's Variable-Grain-Architecture minimizes the logic and interconnect resources needed to implement high-performance, complex functions. It supports logic configurations with three to six logic inputs with all possible input combinations decoded in a single LUT (look-up table) level. It also supports configurations with up to thirty-two partially-decoded parallel inputs that use only two LUT levels.

Coupled with high-performance Variable-Length-Interconnect (VLI) and from 3.6K to 6.1K bits of embedded dual-port SRAM, the Variable-Grain-Architecture delivers the best performance in the FPGA industry in a cost-effective solution that virtually guarantees design success.

Superior performance coupled with densities from 12K to 36K logic gates makes the Vantis VF1 family the best choice for high-performance, complex FPGA-based designs. Designers who create high-performance, high-density designs typically employ a design methodology based on hardware description languages (HDLs) such as Verilog or VHDL to speed the design process and manage complexity. The Vantis design methodology employs third-party HDL design tools coupled with Vantis' physical mapping and layout software.

The VF1 overview that follows describes a new, sophisticated FPGA architecture that includes a rich set of building blocks and interconnect resources. The VF1 family is manufactured in a state-of-the-art deep-submicron 0.18-micron ($L_{effective}$) process technology for high performance and small die size. It uses four layers of metal interconnect to further enhance performance, reduce die size, and lower cost.

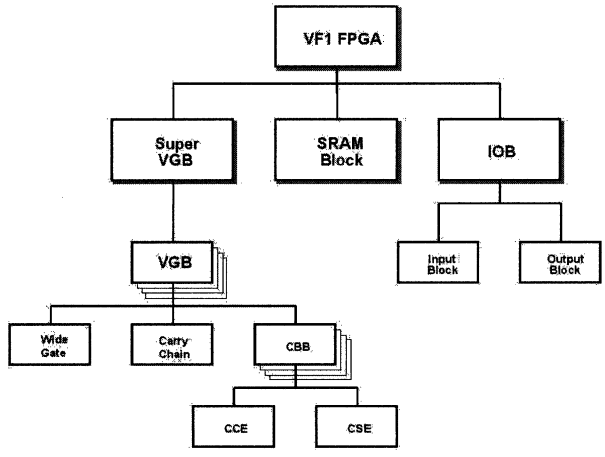
Variable-Grain-Architecture

The VF1 FPGA family employs a new variable-granularity architecture that allows virtually any level of logic complexity to be implemented using minimum chip resources. It comprises three levels of logic hierarchy (Figure 1):

Top Level: Super Variable-Grain-Block (Super VGB), SRAM, and I/O Block (IOB). The highest level building block in the VF1 architecture is the Super VGB. It is a symmetrical structure, made up of four VGBs, that can be combined to create complex, high-performance functions using local building blocks and local interconnect resources. Supporting Super VGBs at the top level are dual-port embedded SRAM and input/output blocks.

Second Level: Variable-Grain-Block (VGB). The next level, the VGB, includes four CBBs, logic to combine two or more CBBs to implement wide logic functions. Wide-gating logic supports complex functions with up to sixteen parallel inputs within a single VGB. The VGB also includes high-speed carry logic to build high-performance arithmetic functions and common control logic.

Configurable Building Blocks (CBB). The CBB is the lowest level building block. It includes six logic inputs, two 8-bit look-up tables (LUTs) to define logic functions, a flip-flop to save results, selectable outputs, and interconnections to other FPGA resources. A single CBB can implement two 3-input functions or one 4-input function using only the logic within the CBB.

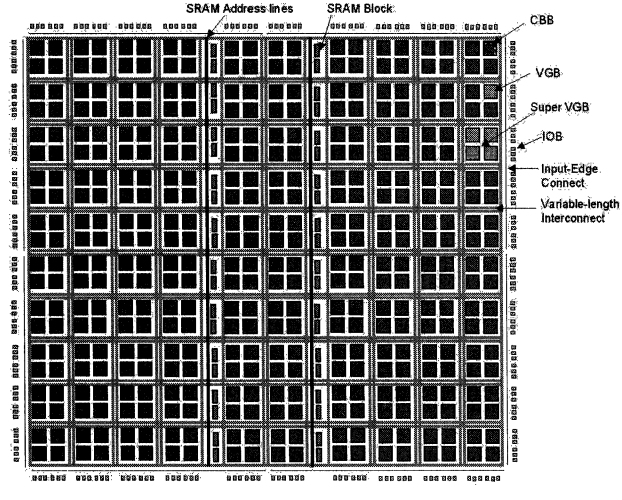


VF1ds-001

Figure 1. VF1 Family Architecture Hierarchy

A VF1 FPGA (Figure 1) is arranged in a matrix of Super VGBs, separated by routing channels made up of interconnect resources called Variable-Length-Interconnect. Figure 2 shows the architecture of the VF1025 FPGA. The VF1025 consists of a 20x20 matrix of VGBs with two columns of embedded SRAM running vertically near the center of the device. Each column of SRAM is supported by dedicated SRAM address lines.

There are three IOBs for each row and column of VGBs on each side of the chip. The VF1025, therefore, has 60 IOBs per side, giving a total of 240 IOBs for the device. Two input Edge Connect lines on each side of the device (eight lines total) may be connected to their adjacent IOBs to implement an input NOR function. The Edge Connect lines consume no power, even when implemented as a NOR function



VF1ds-002

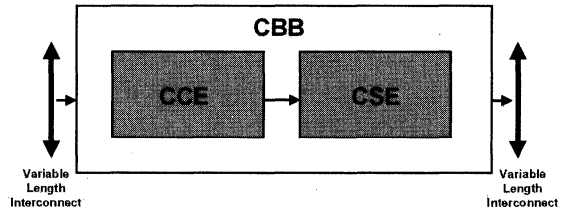
Figure 2. VF1 FPGA Architecture (VF1025 Shown)

A VGB in a VF1 FPGA corresponds roughly to one of the coarse-grained logic blocks found in competitive FPGA products—but a VGB is much more flexible. Its four CBBs can work independently as fine-grained elements to implement simple logic functions while using minimum resources, or they can be combined within the VGB and with other VGBs to handle very complex functions.

The following sections describe the VF1 architecture, starting at the CBB level and moving up the hierarchy.

CBB

A CBB consists of two parts: a configurable combinatorial element (CCE) and a configurable sequential element (CSE) (Figure 3). In general terms, the CCE receives logic inputs and generates outputs. The CSE stores and routes the outputs.

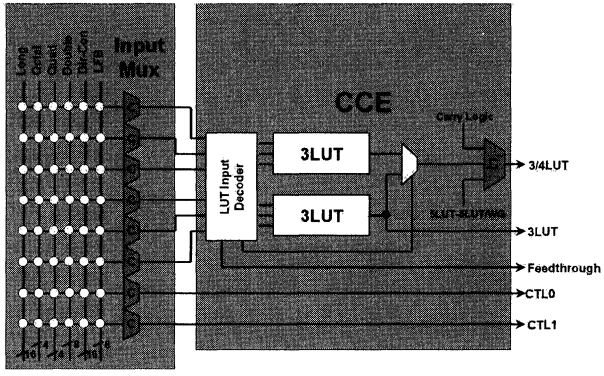


VF1ds-003

Figure 3. Configurable Building Block (CBB)

A CCE (Figure 4) contains two 8-bit, three-input look-up tables (3LUTs). The CCE receives inputs via VF1 Variable-Length-Interconnect routing resources, direct connections from adjacent VGBs, and local feedback within the VGB. (Inputs are covered in more detail later.) A LUT input decoder routes the inputs to the LUTs. The LUT input decoder spans all four CBBs in a VGB to enable the combining of CBBs to create five- and six-input functions. These wider functions are described later.

Bit patterns loaded into the LUTs define the output generated by each input combination.



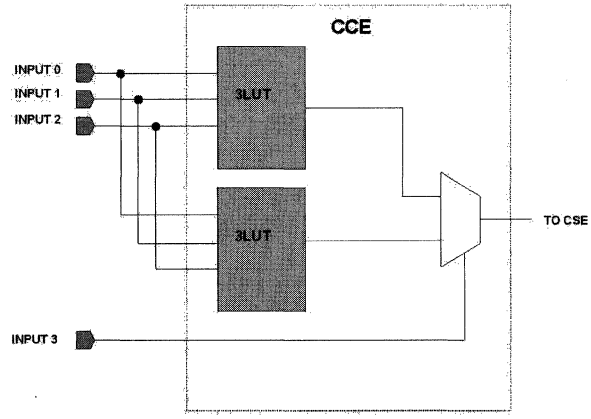
VF1ds-004

Figure 4. Configurable Combinatorial Element (CCE)

Note:
A C in a mux block indicates that the block's function is set by the VF1 configuration bitstream and is not a logical block that can be controlled dynamically

The two 3LUTs may generate individual outputs (Figure 4), or they may be combined into a 16-bit 4LUT that decodes four inputs (Figure 5). If the 3LUTs operate independently, one output follows the Feedthrough route to the CBB output while the other goes to the following CSE via the 3/4LUT path shown in Figure 4.

The Feedthrough line coming from the Input Switch is a special high-speed path that allows long-line routing resources to be routed from one line to another without going through a long-line switch matrix. The Feedthrough path provides better performance than the switch matrix path. This is covered in the *VGB Interconnect* section.



VF1ds-047

Figure 5. Four-Input CCE Configuration

The CSE (Figure 6) receives the outputs from the CCE via the top mux on the left (along with Carry Logic, CCE, and Wide Gating inputs) and the Feedthrough line on the bottom left. The top mux output may be stored in the CSE register or it may bypass the register and go directly to an output via a second mux. The output of the second mux goes to a direct connect line that connects to other VGBs and IOBs, and to a local feedback (LFB) line that connects to other CBBs within the same VGB.

The Feedthrough line from the lower 3LUT can be routed to VLI resources and to a second LFB line.

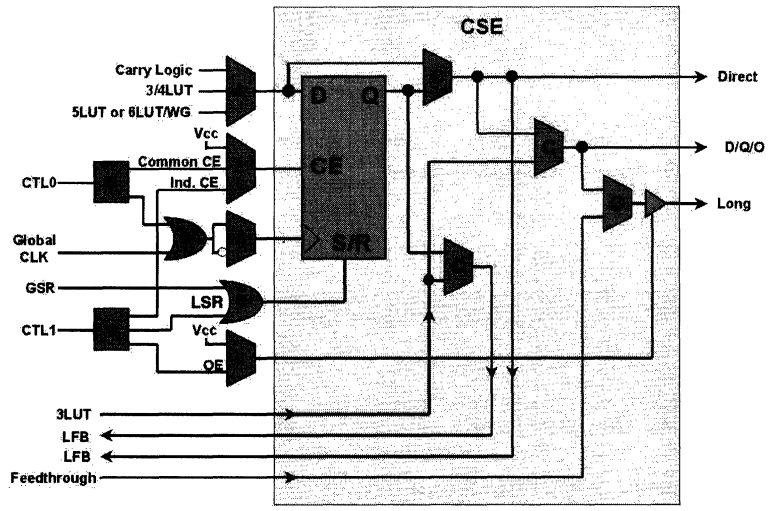


Figure 6. Configurable Sequential Element (CSE)

CSE register control signals consist of a clock enable (CE), a clock, and a direct set/reset. The register clock enable may be a common enable, a separately generated independent enable, or it may be tied to V_{cc}.

Both the register clock (CLK) and the set/reset signal (S/R) may be configured to meet specific design requirements. The polarity of the clock can be selected by configuring the mux that precedes the clock input to the register. The set/reset source may be configured as either local (LSR) or global (GSR). If a local set/reset is selected, it applies to all the registers in one VGB.

The Feedthrough line can be routed to a long interconnect line via a dedicated driver. The driver can be enabled by either being tied to V_{cc} or by a locally-generated output enable (OE). This function allows a signal from a long interconnect line to enter a Super VGB via a CBB input, bypass CBB logic, and connect directly to a shared Super VGB long-line driver. The long-line driver connects the signal to another long interconnect line. This is an alternative to using a switch at an intersection of long lines. It adds additional drive to the signal, allows the signal to be connected to lines that are parallel to the original line as well as perpendicular, and may have less delay than a switch at a line intersection.

VGB

The second level in the VF1 FPGA family hierarchy is the Variable-Grain-Block, or VGB (Figure 7). A VGB contains four CBBs plus common control functions, wide gating logic, and high-speed carry logic.

A VGB is a very flexible structure that can be combined in a variety of ways to create very simple or very complex logic structures. A VGB can be viewed as a fine-grained architecture when each CBB is used to implement a separate logic function. It becomes a coarse-grained architecture when the entire VGB is dedicated to a single function.

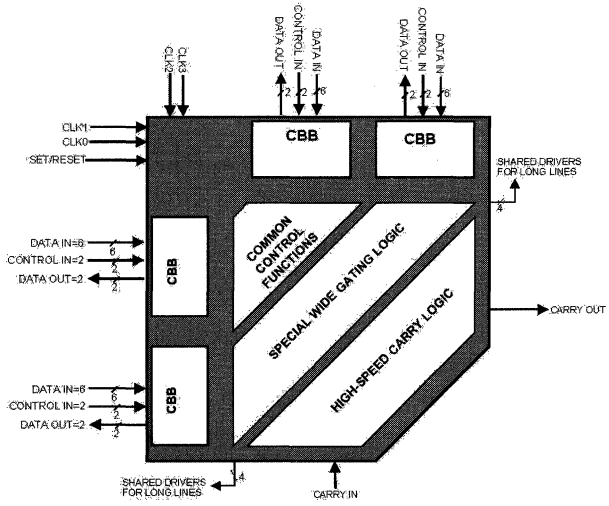
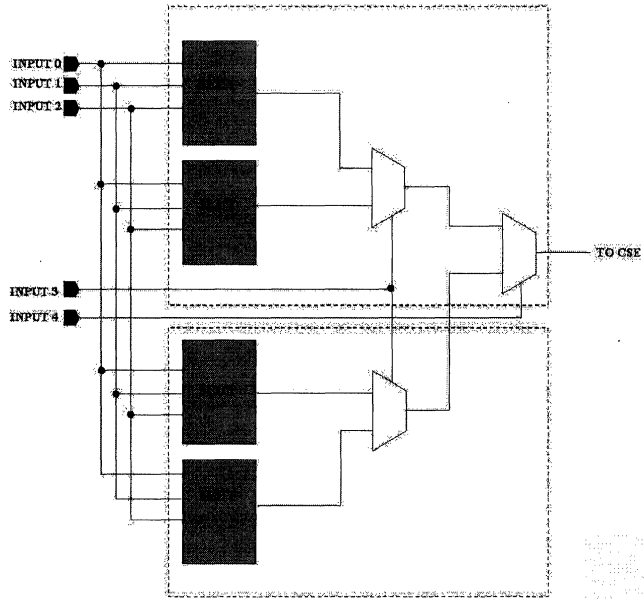


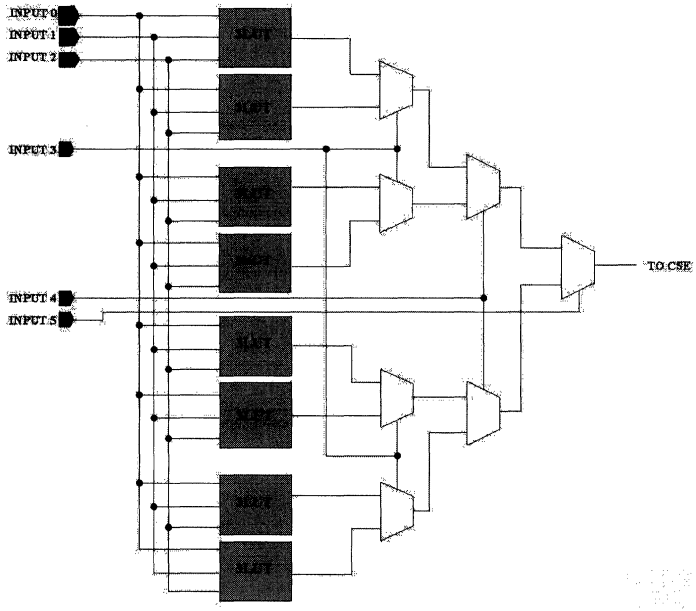
Figure 7. Variable-Grain-Block (VGB)

Just as the LUTs within a single CBB can be combined to create complex functions, the CBBs within a VGB can be combined. By combining the four 8-bit 3LUTs in two CBBs into a single 32-bit 5LUT, all possible combinations of five logic inputs can be decoded (Figure 8). By combining all four CBBs in a VGB into a single 64-bit 6LUT, all possible combinations of six inputs can be decoded (Figure 9). The combined output becomes an input to one of the CSEs (Figure 6, upper-left mux).



VF1ds-050

Figure 8. Five-Input Function Using Two CBBs



VF1ds-009

Figure 9. Six-Input Function Using Four CBBs in One VGB

Figure 10 shows some of the possible fully-decoded combinations that can be implemented in a single VGB. The left VGB in Figure 10 shows some combinations that are possible without combining CBBs. A single VGB can implement eight three-input functions, or four four-input functions, or four three-input functions plus two four-input functions. Other combinations are also possible.

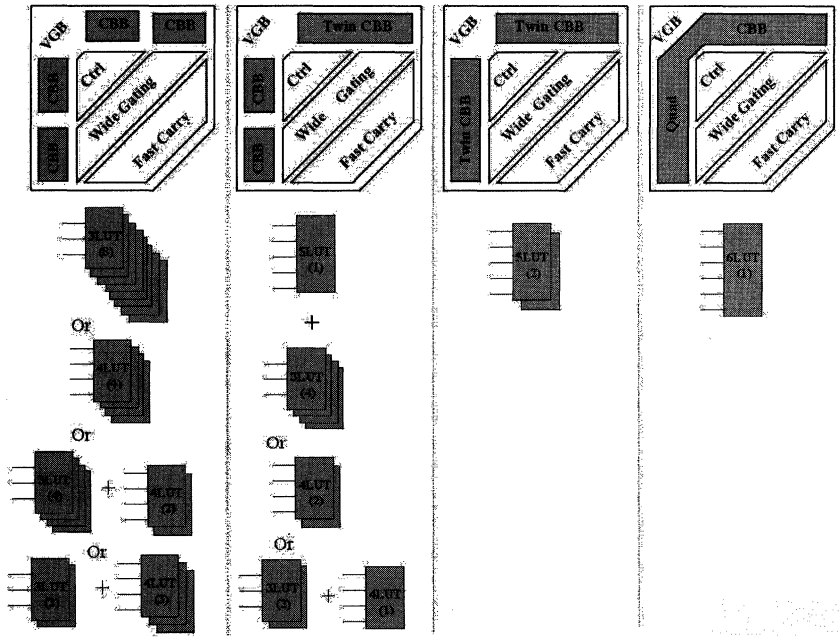


Figure 10. Examples of Logic Configurations in One VGB

The second VGB in Figure 10 shows some possible combinations when two CBBs are combined while two CBBs function independently. The combined CBBs form a 5LUT that implements a five-input function, while the independent CBBs implement various combinations of three- and four-input functions. The third VGB is configured for two five-input functions, and the fourth is configured for a single six-input function.

In many cases, however, an application does not require the decoding of every possible combination of a set of inputs. In these cases, configuring CBBs in combinations other than those described above can save device resources. For example, two CBBs may be configured as separate 4-input elements with their outputs multiplexed to decode an 8-input function using only two CBBs. Since each CBB decodes 16 combinations of four inputs, this configuration decodes 32 possible combinations of eight inputs.

Special wide-gating logic that is part of the VGB architecture is used to implement configurations up to 32 inputs in only two logic levels. The wide gating logic includes a dedicated 4LUT that is used to combine CBBs into functions with up to sixteen inputs using all four CBBs in one VGB (Figure 11). In this example, each CBB within a VGB is configured to fully decode four inputs.

Each of the four CBBs generates an output that becomes an input to the 4LUT in the wide gating logic. The 4LUT fully decodes the four inputs from the CBBs.

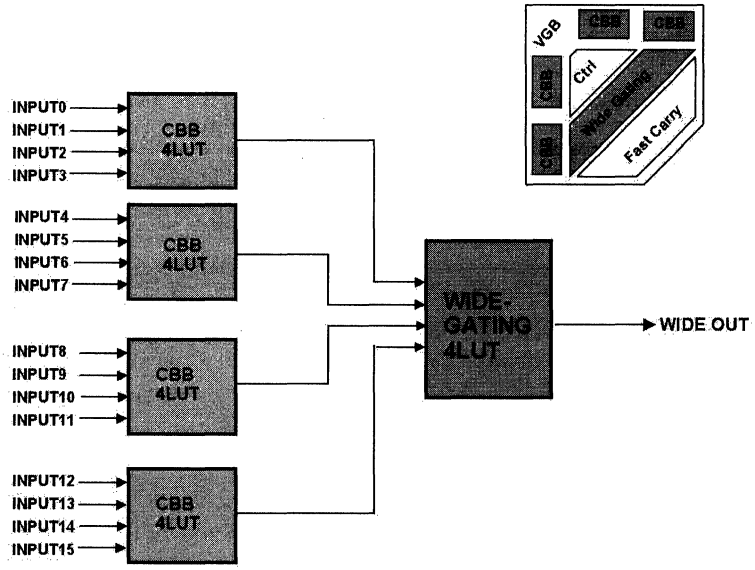
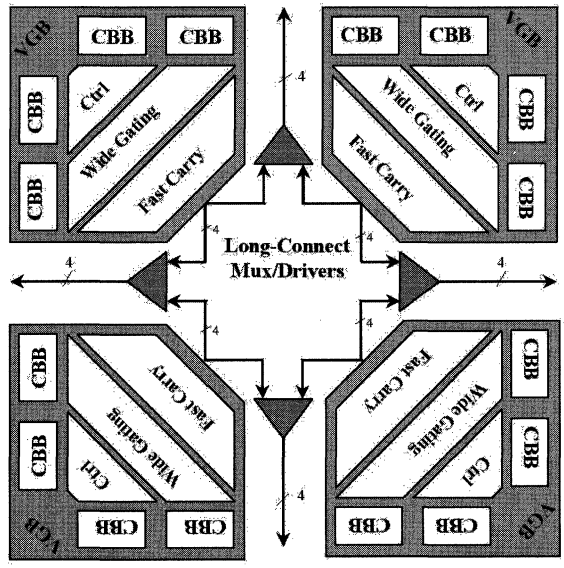


Figure 11. Decoding 16-Input Function Using Wide Gating Logic

The configuration in Figure 11 does not decode all 65,536 possible combinations of sixteen inputs. Instead, it decodes sixteen combinations of four inputs in each CBB for a total of 64 possible combinations. The wide-gating 16-bit LUT decodes sixteen possible combinations. The circuit, therefore, decodes 1024 combinations (16*64). For most logic functions this is quite adequate, and it is accomplished using only the high-speed, short-intraconnect logic contained in a single VGB.

Super VGB

The third hierarchical level is the Super VGB (Figure 12). It consists of four mirrored VGBs with four sets of shared long-connect multiplexers/drivers. The symmetrical arrangement of the Super VGB improves logic density and minimizes interconnect length for implementing complex functions. Inputs can come from any direction on the chip and outputs can go in any direction. Compared to architectures that force logic paths to flow in one general direction, this Super VGB symmetry shortens signal paths and thus improves both performance and density.



VF1ds-012

Figure 12. Super VGB Architecture

Each Super VGB has four sets of shared drivers, each set pointing in a different direction on the chip. These drivers allow a Super VGB to connect to the VLI lines (see *Interconnecting VGBs*) that provide general signal routing throughout the chip. Each set of shared drivers contains four individual drivers for a total of sixteen drivers in each Super VGB.

In addition to general interconnection of VGBs to long interconnect lines, the shared drivers are used to implement logic functions with up to 32 parallel inputs. Two 16-input functions (Figure 11) can be multiplexed using a shared driver, thus providing a 32-input function that decodes 2,048 possible conditions.

Interconnect Resources

In today's deep-submicron technologies, interconnect length often has a greater impact on device performance than gate or logic-block delays. The Vantis VF1 family minimizes most interconnect delays by providing multiple levels of interconnect resources that often allow complex functions to be implemented completely within a VGB or Super VGB. These complex functions, however, must be connected to other VGBs and to I/O blocks, therefore longer routing resources are needed.

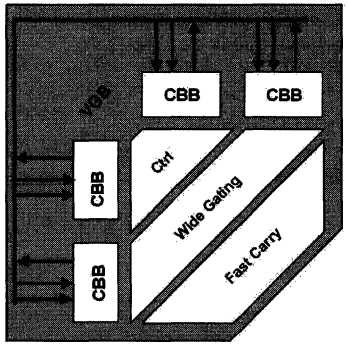
The VF1 architecture provides three levels of high-performance interconnect resources:

- **Local feedback** allows CBB outputs to feed back to the inputs of all CBBs within the same VGB.
- **Inter-VGB Direct connect** routes the outputs of every CBB in every VGB to the inputs of eight nearby VGBs and to IOBs.
- **Variable-Length-Interconnect** resources provide programmable interconnects that may span two VGBs, four VGBs, eight VGBs, and the entire FPGA.

These interconnect resources provide highly efficient routes for making component connections while maintaining maximum performance levels. In addition to maximizing performance, the VF1 family interconnect methodology allows Vantis' optimization, mapping, and place-and-route software tools to achieve First-Time-Fit results. It also simplifies pin locking and density shifting when moving from one VF1 FPGA to another within the same package type.

Local Feedback

The earlier description of CBBs shows how local feedback lines (LFBs) are routed back from the CBB outputs toward the CBB inputs. These LFBs are then routed to the inputs of every CBB in the same VGB (Figure 13). Local feedback provides a very powerful, high-performance routing resource that works entirely within the VGB and uses no general routing resources.

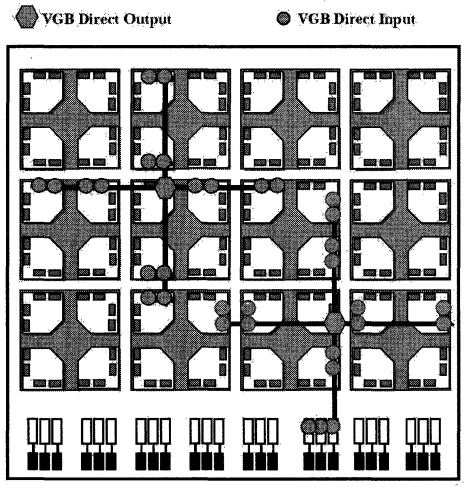


VF1ds-013

Figure 13. Local Feedback

Inter-VGB Direct Connect

Every CBB in every VGB has a direct-connect output that connects it to the inputs of two CBBs in eight other nearby VGBs (Figure 14). The direct connect routing shown in the upper left portion of Figure 14 shows how direct-connect lines are routed when the output CBB is not near the edge of the VF1 FPGA. The routing shown in the lower right shows how a direct-connect output connects to three IOBs when the output CBB is near the edge of the device.



VF1ds-014

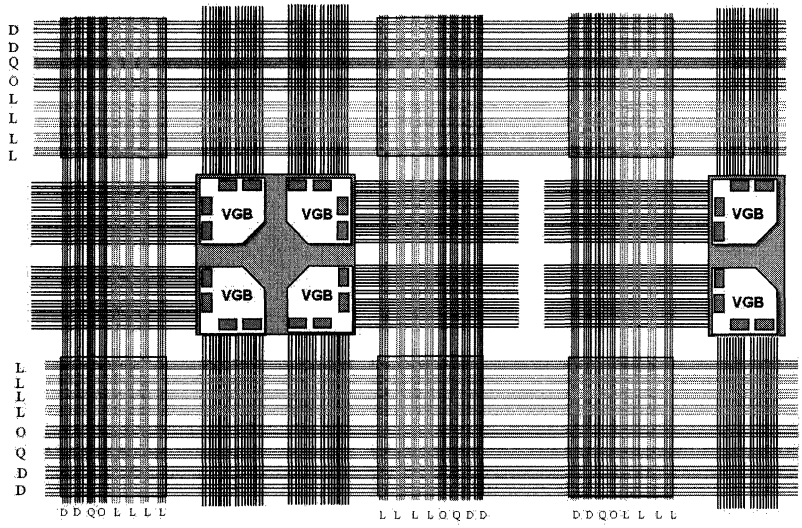
Figure 14. Inter-VGB Direct Connect

Only two direct-connect routes are shown in Figure 14, but every CBB in every VGB has the same direct-connect routing resources. The direct-connect capability allows VGBs that are adjacent to each other to be combined in very powerful logic structures without using slower general routing resources.

Variable-Length-Interconnect Resources

The VF1 family provides four types of Variable-Length-Interconnect resources that run in channels between Super VGBs, both horizontally and vertically (Figure 15). Two groups of interconnects run within each channel. Each group of interconnects includes the following:

- **Long Connect:** 16 lines run from edge to edge on the chip, both vertically and horizontally.
- **Octal Connect:** 4 lines span 8 VGBs both horizontally and vertically.
- **Quad Connect:** 4 lines span 4 VGBs (two Super VGBs) both horizontally and vertically.
- **Double (or Twin) Connect:** 8 lines span 2 VGBs both horizontally and vertically.



VF1ds-015

Figure 15. Variable-Length Interconnect Resources

The sixteen long-connect lines can be used to implement three-state buses, whereas octal, quad, and double connect lines cannot. CBBs can connect directly to octal, quad, and double connect lines, but cannot connect directly to long lines. A VGB output connects to a long line resource by using a shared long-line driver in a Super VGB.

VLI lines change direction by connecting with other VLI lines at switch matrixes located at the intersections of the horizontal and vertical groups of lines. Long lines, however, can bypass the switch matrix by using a CBB Feedthrough line, as described in the CBB section.

Interconnect Performance Considerations

Short connections deliver better performance than long connections. Interconnect resources, in order of performance, are:

- Local feedback within a single VGB
- Direct-connect lines between VGBs and from VGBs to IOBs
- Dual lines that span two VGBs
- Quad lines that span four VGBs
- Octal lines that span eight VGBs
- Long lines that span the entire VF1 FPGA

Vantis' DesignDirect software selects routing resources and calculates timing for both routing and logic delays. Designers can control routing indirectly by specifying timing constraints that must be met by the DesignDirect tools.

Carry Logic

Every VGB includes high-speed carry logic that facilitates the implementation of arithmetic circuits such as adders, subtracters, bit shifters, up/down counters, and comparators. To improve arithmetic speed, the carry chain within a VGB is placed between the CCEs and the CSEs within each CBB (Figure 16).

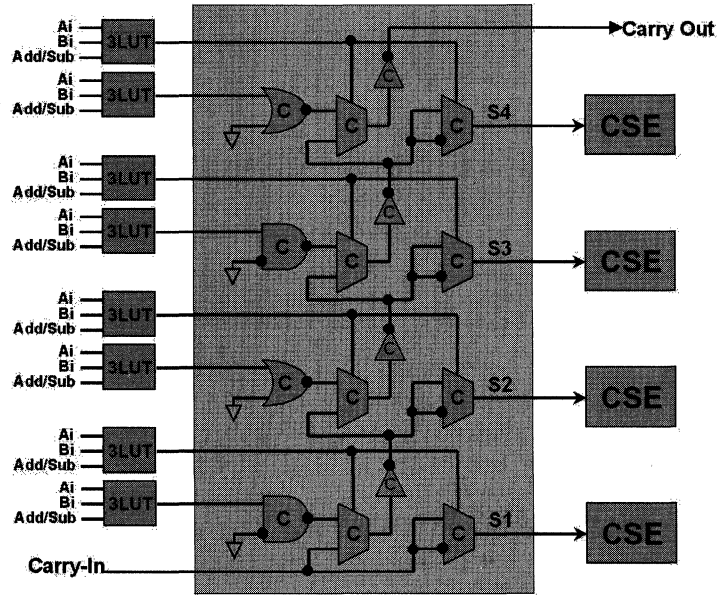
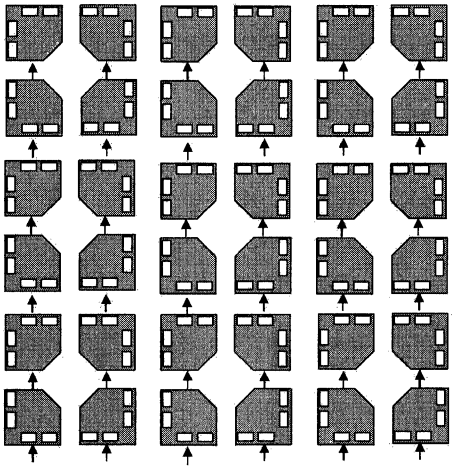


Figure 16. Carry Routing Within a VGB

A VGB receives a carry input from a preceding VGB in the arithmetic chain, and generates a carry for the following VGB (Figure 17). The carry chain between VGBs starts with the bottom VGB in a column and proceeds vertically through the column. Each column of VGBs has its own carry chain.



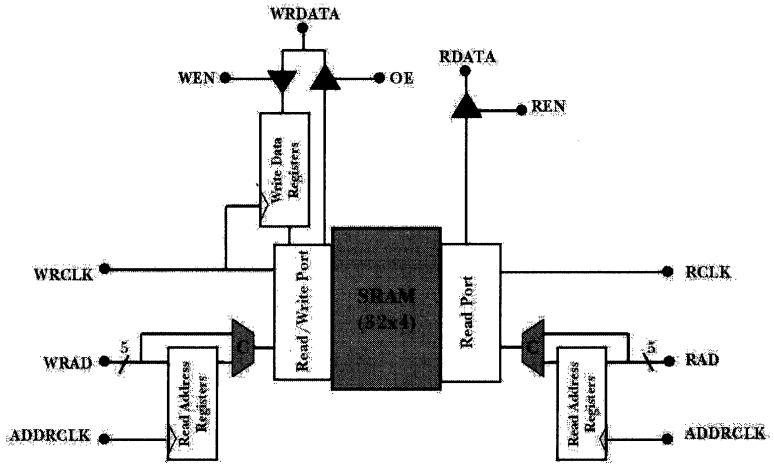
VF1ds-017

Figure 17. Carry Routing Between VGBs

Embedded Memory

Every VF1 FPGA family member includes embedded memory configured as 32x4 dual-port SRAM blocks (Figure 2). The dual-port configuration (one read/write port and one read port) allows an application to read from the read port while it is reading from or writing to the read/write port. This allows applications such as FIFOs and register stacks to run much faster, and requires only half as many memory bits to implement as a single-port RAM would require.

Specific memory structures are created by the Vantis DesignDirect software and are implemented by the configuration bitstream. In addition, initial memory contents can be loaded at configuration time.



VF1ds-018

Figure 18. VF1 Dual-Port SRAM

The embedded memory is implemented as two columns of memory blocks that run the full length of the FPGA device (Figure 2). Two columns of Super VGBs (four columns of VGBs) run between the memory columns, and additional columns of Super VGBs are outside the memory columns. This configuration minimizes the distance between Super VGBs and embedded memory, thus allowing shorter interconnects and faster memory access. It also simplifies density shifting and pin locking features. Table 3 lists the memory capacity of each VF1 FPGA family member.

Table 3. VF1 Embedded Memory Capacity

	VF1012	VF1020	VF1025	VF1036
VGB Array Size	14 x 14	18 x 18	20 x 20	24 x 24
Embedded Memory Blocks	28	36	40	48
Total Memory Bits	3584	4608	5120	6144

Note:
For a detailed description of memory access modes and timing, refer to the "VF1 Dual-Port SRAM Architecture and Timing" Technical Note.

One port of each SRAM block is a read/write port and the other is a read-only port (Figure 18). The read/write port on the left of Figure 18 consists of a write/read address input (WRAD) that may be stored in Read Address Registers, or may bypass the registers and go directly to the Read/Write Port. For write operations, the write address is stored in the Read/Write Port and write data is stored in the Write Data Registers.

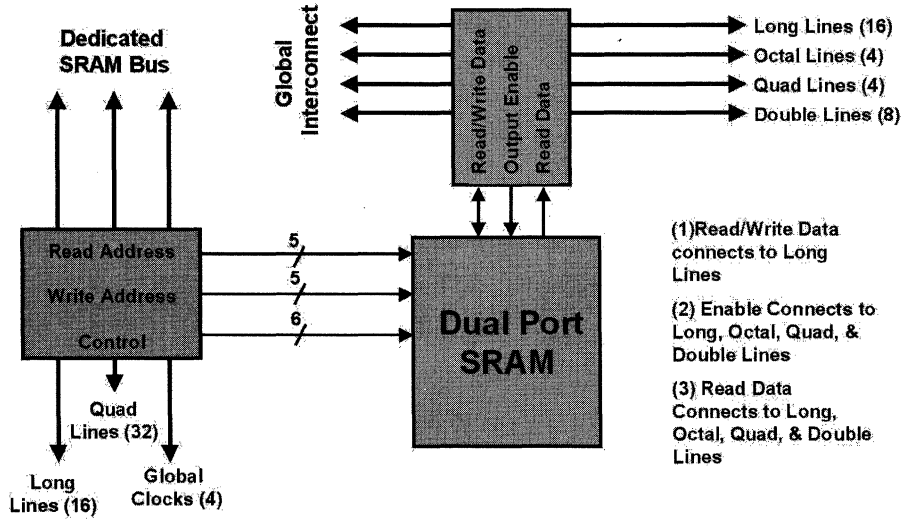


Figure 19. VF1 Dual-port SRAM Routing Resources

Memory read and write addresses come from dedicated SRAM address buses (Figure 19). There are five read address lines, five write address lines, and six control lines (including global clocks) connected to each 32x4 memory block. The SRAM address bus is driven by VLI quad and long lines. Read/write data for the read/write port connect to VLI long lines. Read data from the read port and output enable lines connect to any VLI resources.

Memory Modes

The VF1 embedded memory supports six single- and dual-port synchronous and asynchronous read and synchronous write operations. All single-port operations use the read/write port. The read-only port is used for dual-port operations. All write operations are synchronous. Read operations may be synchronous or asynchronous.

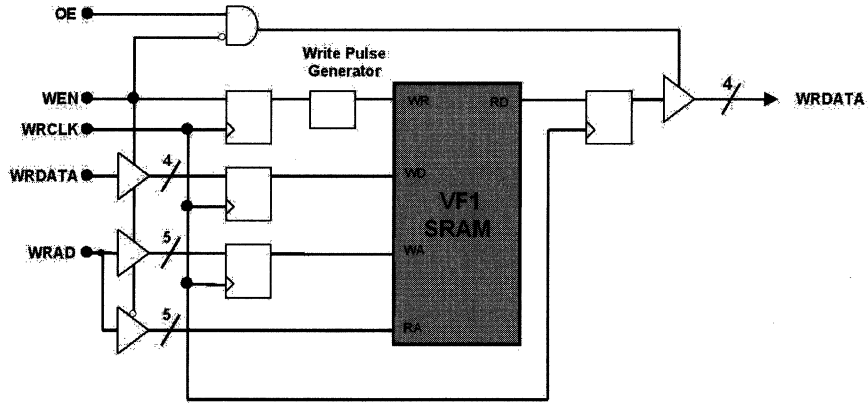
In dual-port operations, it is possible to read from the read port at the same time that the read/write port is performing a read or write. It is also possible to access the same address simultaneously. If the read/write port writes to an address at the same time that the read port reads the address, the read port will read the old contents of the address until the next clock cycle, at which time the contents of the address will change to the new data.

The mode diagrams that follow represent memory behavior and not physical memory implementation. The modes are:

- **Single-port synchronous read/write (Figure 20).** Both read and write operations are synchronized by WRCLK. Synchronous read operations register read data on the output.
- **Single-port synchronous write/asynchronous read (Figure 21).** This operation is identical to the synchronous read/write except that read data is not registered on the output.
- **Single-port synchronous write/asynchronous read, registered read address (Figure 22).** The read address is registered prior to the read/write port using a separate clock (ADDRCLK), rather than the WRCLK that is used for write and synchronous read operations.
- **Dual-port synchronous read/write (Figure 23).** This function adds a second read port to the single-port synchronous read/write operation. The read port functions identically to the read operations in the read/write port.
- **Dual-port synchronous write/asynchronous read (Figure 24).** In this mode the read port performs asynchronous reads while the read/write port performs synchronous writes or asynchronous reads.
- **Dual-port synchronous write/asynchronous read, registered read address (Figure 25).** The read port performs registered address read operations.

The timing diagrams in Figures 26-29 show the timing relationships for each mode. Write timing applies to the read/write port only, and read timing is identical for each port.

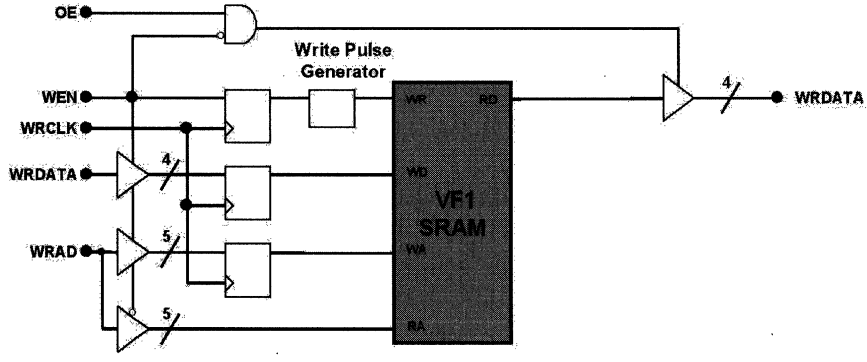
Note:
More detailed descriptions of these memory modes, plus detailed timing diagrams of each mode, are found in the "VF1 Dual-Port SRAM Architecture and Timing" Technical Note.



VF1ds-020

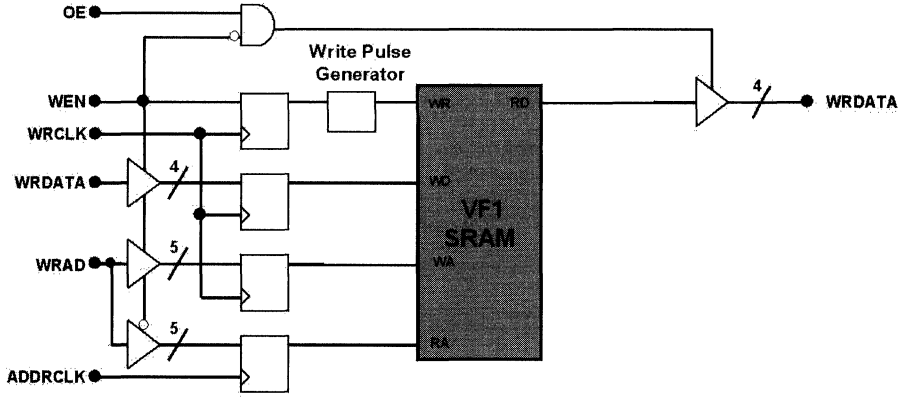
Figure 20. Single-Port Synchronous Read/Write

Note:
Diagram only represents behavior and not physical implementation



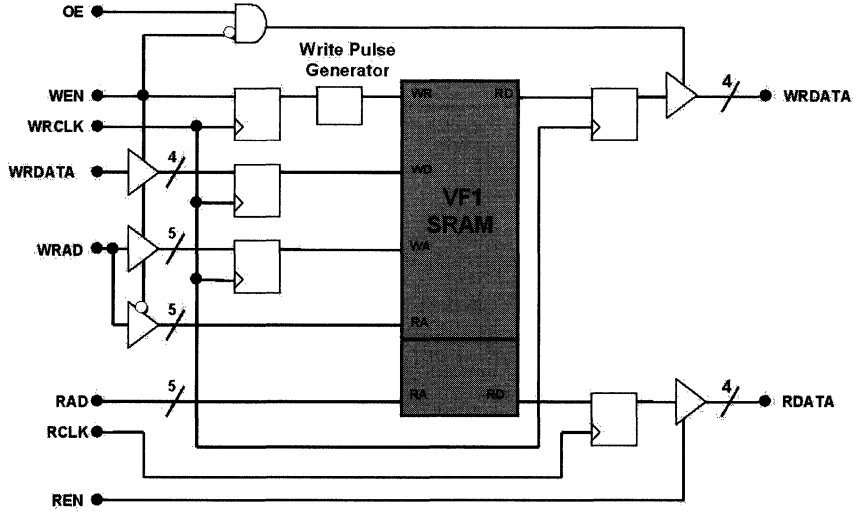
VF1ds-021

Figure 21. Single-Port Synchronous Write/Asynchronous Read



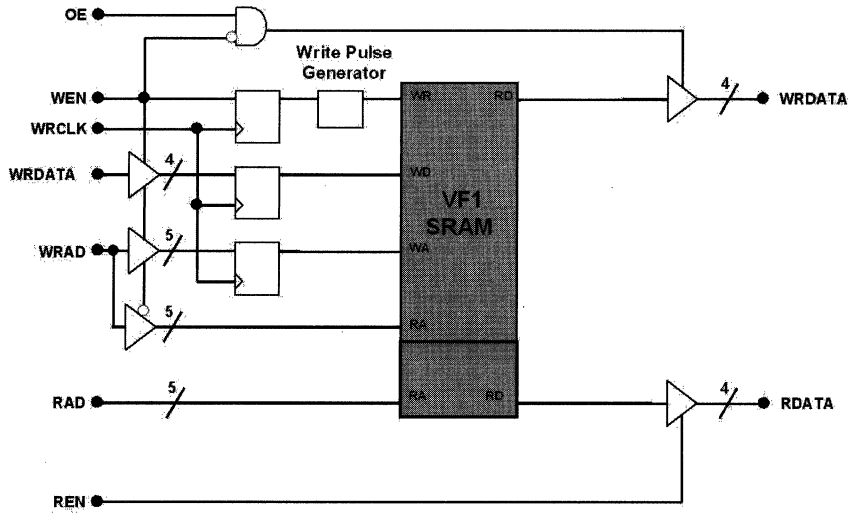
VF1ds-022

Figure 22. Single-Port Synchronous Write/Asynchronous Read, Registered Read Address



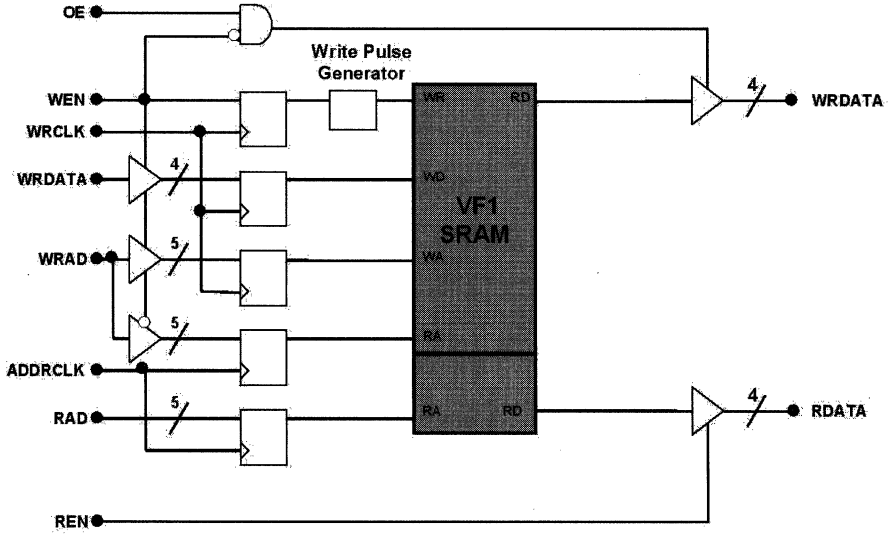
VF1ds-023

Figure 23. Dual-Port Synchronous Read/Write



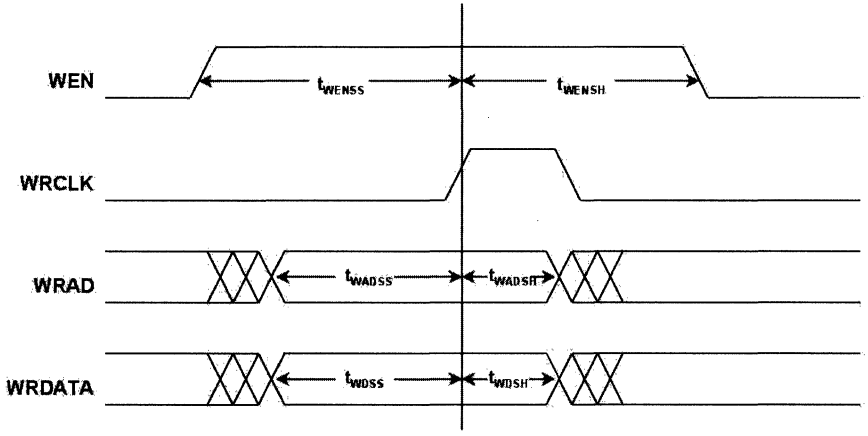
VF1ds-024

Figure 24. Dual-Port Synchronous Write/Asynchronous Read



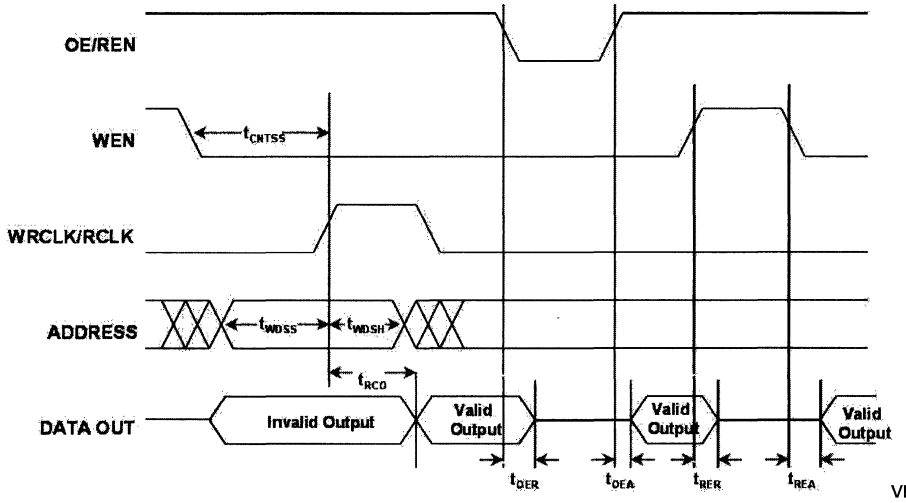
VF1ds-025

Figure 25. Dual-Port Synchronous Write/Asynchronous Read, Registered Read Address



VF1ds-026

Figure 26. Synchronous Write Timing



VF1ds-027

Figure 27. Synchronous Read Timing

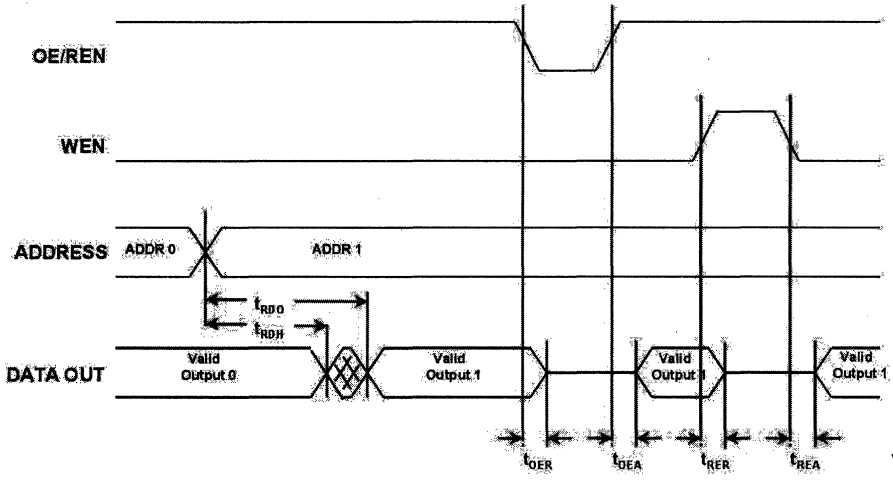


Figure 28. Asynchronous Read Timing

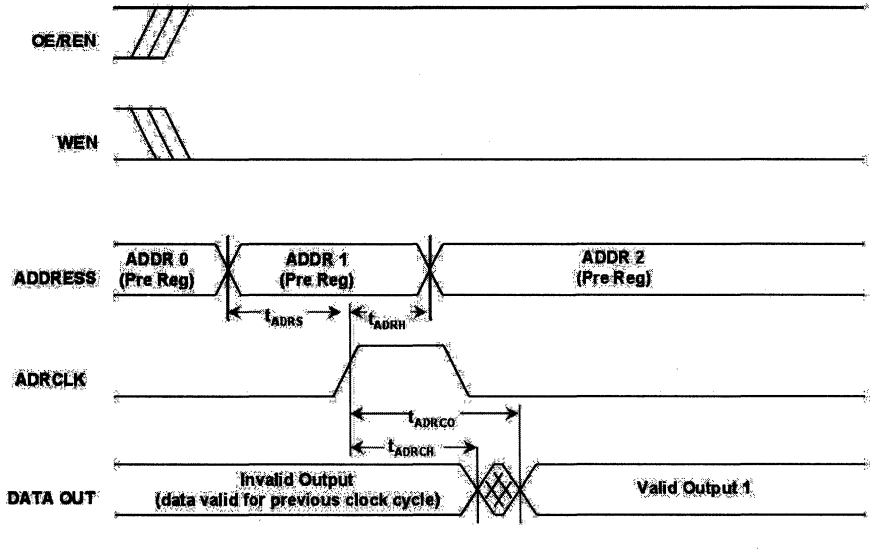


Figure 29. Asynchronous Read Timing with Registered Read Address

Input/Output Blocks

Input/output blocks (IOBs) provide an interface between the internal logic functions of the VF1 FPGA and the remainder of the system in which the device is installed. IOBs support input and output functions, and interface the VF1 FPGA to both 3.3V and 5V I/O levels.

IOB regions lie on all four sides of the FPGA (Figure 2). Each programmable IOB includes a pad, input logic, and output logic (Figure 30). The input and output sections function separately from each other, sharing only the I/O pad and common Set/Reset logic. The common Set/Reset signal is either the VF1 Global Set/Reset, or a local set/reset.

Separate input and output enable signals allow an IOB to function as both an input pin and an output pin in a design.

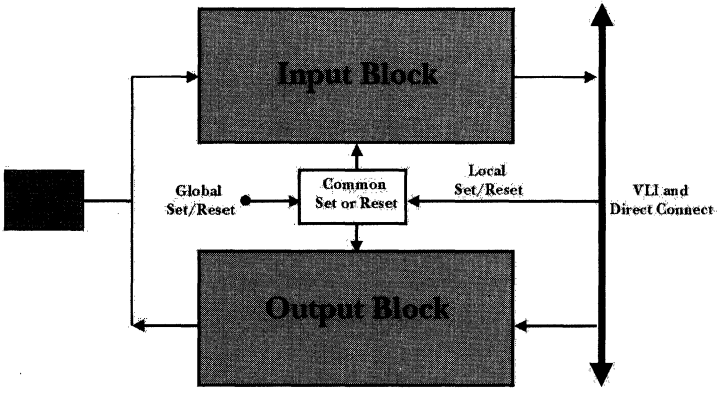


Figure 30. VF1 Input/Output Block (IOB)

Figure 31 gives a more detailed view of the programmable IOB. Both the input and output sections share a common set/reset signal. The set/reset may be locally-generated (LSR), or it may be the VF1 global signal (GSR). The input and output sections use separate clocks and separate clock enables.

The IOB input section includes an input buffer, input register/latch, and programmable logic to connect the input to appropriate interconnect lines. The input signal may either be registered or bypass the register. When the register is used, a delay may be inserted between the input pad and the register (Figure 32) to ensure zero hold time for the register when using an external clock. The delay is not used when an on-chip PLL generates the clock (refer to the PLL description later in this document).

Input signals may be routed to long lines, to shift-connect lines, to edge-connect lines, or directly to VGBs via direct connect lines. The long-line connections may be permanently enabled by tying to V_{cc}, disabled by tying to GND, or dynamically controlled via a locally-generated signal. Other connections are established when the VF1 FPGA is configured. Connections are described in more detail following the IOB output description.

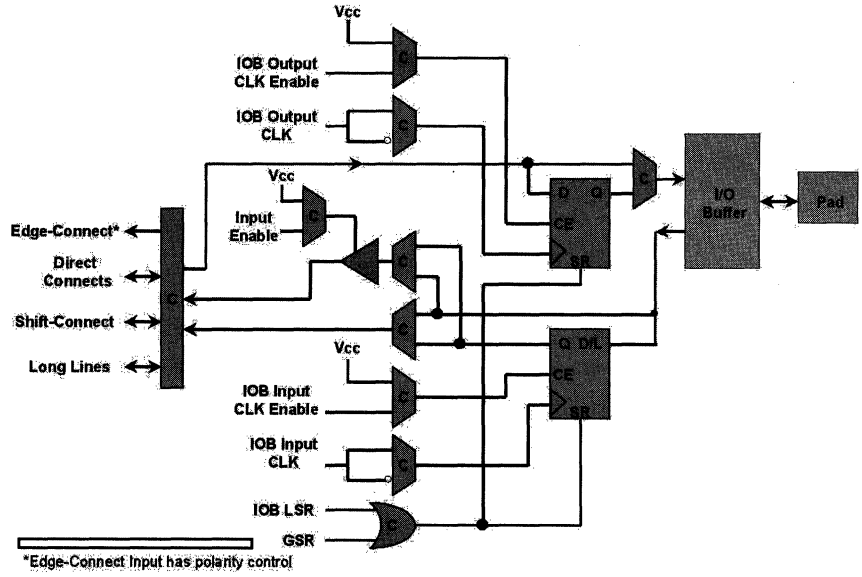
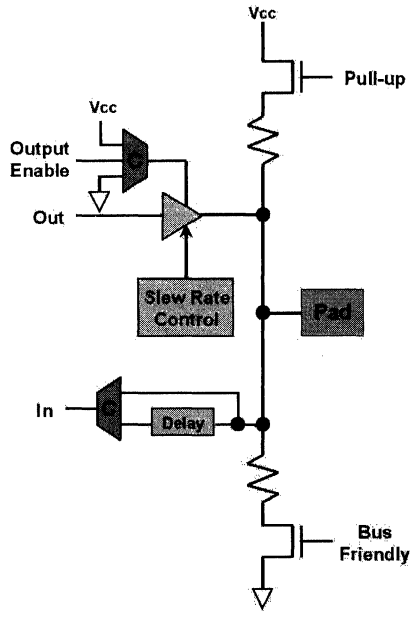


Figure 31. VF1 Input/Output Block

Note:
Edge-Connect input has polarity control

The IOB output section includes programmable interconnections from the VF1 logic, an output register, and an output buffer with programmable slew rate control (Figures 31 and 32). Output data may come from direct connect lines, long lines, or shift-connect lines. The output may be permanently enabled or disabled by tying to V_{cc} or GND, or controlled dynamically by a locally-generated enable signal.



VF1ds-032

Figure 32. VF1 I/O Buffer

The VF1 I/O buffer (Figure 32) offers designers a wide selection of programmable capabilities:

- **Three-state control capability** for interfacing to buses
- **Programmable pull-up resistor** for a weak high bias
- **Programmable Bus-Friendly™ architecture** to hold the last output value when the IOB goes into high-impedance mode
- **Output slew rate control** to reduce ringing
- **Programmable input delay** allows zero hold time from external clock
- **IEEE 1149.1 boundary scan** capability to simplify board testing

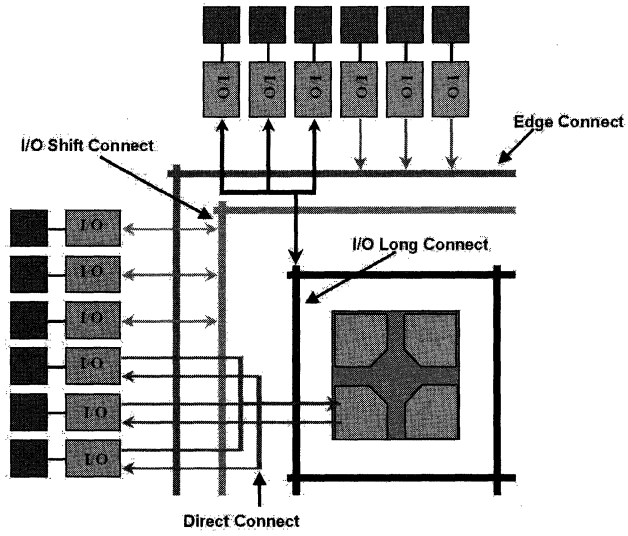


Figure 33. IOB Interconnect

IOBs may connect to long lines, shift-connect lines, direct-connect lines, and Edge Connect lines (Figure 33). Long-line connections allow any VGB anywhere in the VF1 FPGA to be connected to IOBs. Long-line connections are made to routing resources that are perpendicular to the edge of the device where the IOB is located. Each IOB may connect to two long-line channels.

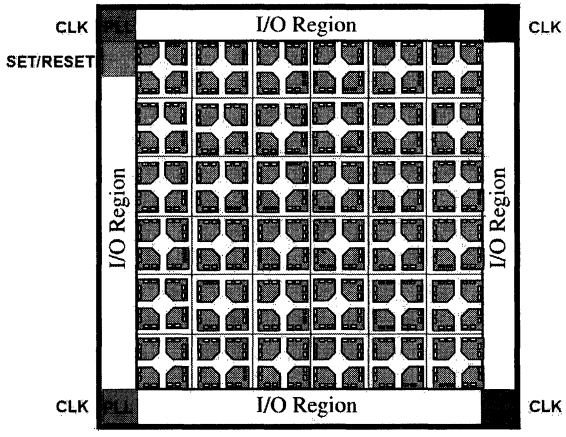
Shift-connect lines give the VF1 FPGA family a very powerful pin-locking capability when a design moves a design to either a higher or lower density VF1 FPGA. Shift-connect lines expand an IOBs long-line connection span from two channels to four, making it much more efficient to lock pin assignments when shifting from one device density to another.

Direct-connect lines connect IOBs directly with VGBs that are near the edge of the VF1 FPGA. These are the fastest connections between logic elements and I/O elements.

Edge Connect lines apply to inputs only. An IOB input section may be configured to connect to an Edge Connect line as well as another data line. The Edge Connect lines (two per side of the VF1 FPGA) are used to implement input NOR functions on IOB inputs.

Global Interconnect and PLL

Global signals in the VF1 family include four global clocks and a global set/reset function (Figure 34). The Set/Reset signal input is at one corner of the VF1 FPGA. The four global clock inputs are distributed with one CLK input at each corner. Two of the global clocks may be applied to embedded phase-locked loop (PLL) circuits for clock deskewing and frequency multiplication.

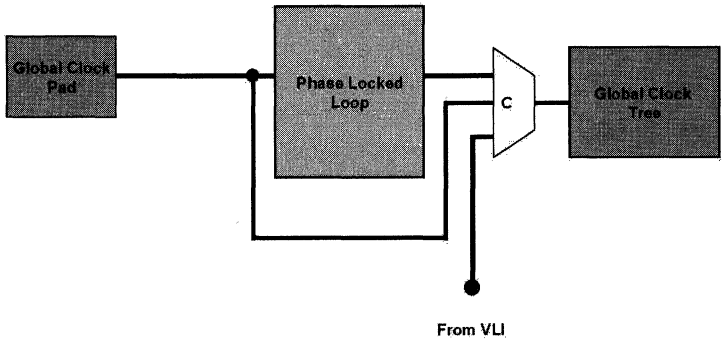


VF1ds-034

Figure 34. VF1 Global Interconnect

All four global clocks have individual clock trees that distribute them throughout the VF1 FPGA (Figure 35). These clock trees cannot be subdivided. Clocks associated with PLLs may either bypass the PLL circuit or may be applied to the PLL with the PLL output applied to the clock tree. In addition, clocks may be generated within the VF1 FPGA and distributed using the global clock tree (the VLI input in Figure 35).

Maximum input frequency on any clock pin is 250 MHz. Operation at the maximum frequency requires certain design considerations. Refer to Vantis applications notes for guidelines on high-frequency designs.



VF1ds-035

Figure 35. Global Clocks and PLL

PLL

The embedded analog PLL circuits can be used to deskew clocks from one chip to another and to synthesize on-chip clocks using an external reference frequency (usually an external clock input).

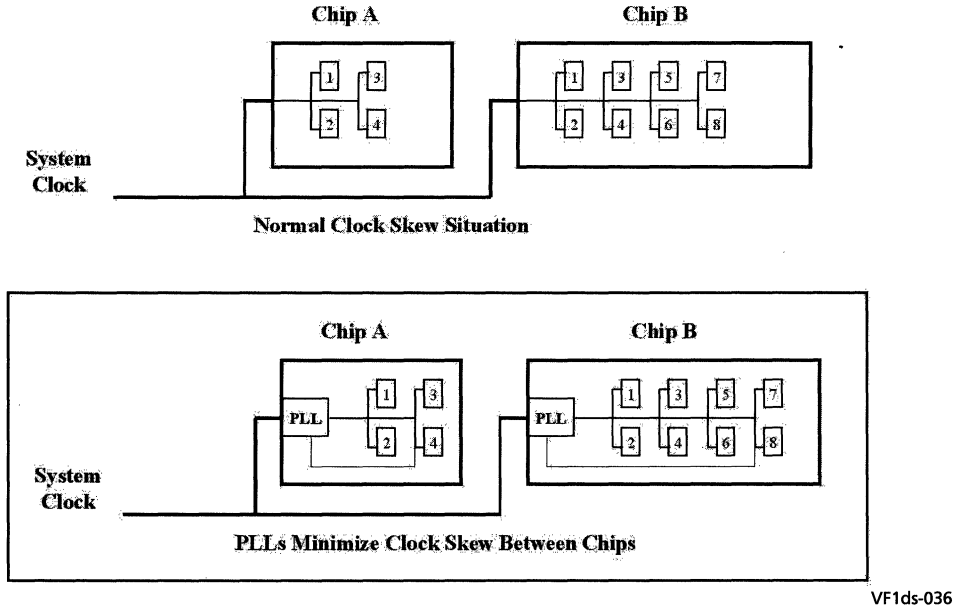
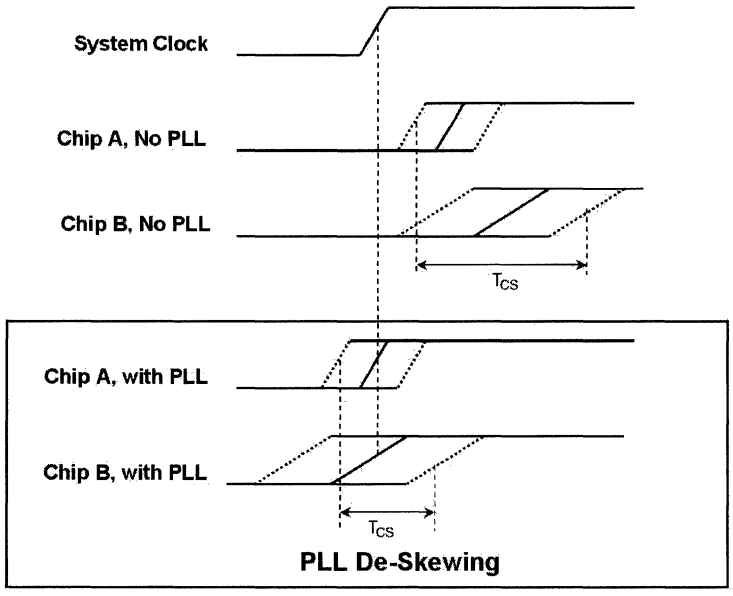


Figure 36. Deskewing Clocks with PLLs

Clock skew from one chip to another robs a system of much of its performance by delaying the generation of reliable outputs from larger chips. When a system clock is applied to two chips of different sizes (Figure 36), the clock will propagate through the chips at different rates. For example, the clock will reach flip-flop 4 in Chip A (Figure 36, upper diagrams) much sooner than it reaches flip-flop 8 in Chip B. Process and environmental variables also contribute to clock skew within a chip.

The waveforms (Figure 37, upper waveforms) show the results of skew in the two chips. The dotted lines in the chip waveforms show when the system clock reaches the first flip-flop in the chip and when it reaches the last. The solid line shows when the clock reaches the mid-point along each chip's clock trunk.

A PLL can "shift" the reference clock within a chip and reduce the time that it takes for the chip to generate its output. The PLL works by monitoring the reference clock and the clock signal at the end of the chip's clock trunk (Figure 36, lower diagrams). It then shifts the clock phase so that the shifted clock pulse reaches the end of each chip at the same time that the system clock reaches the chip input. The PLL effectively synthesizes a new clock at the same frequency as the system clock, but slightly shifted in phase (Figure 37, lower waveforms).



VF1ds-037

Figure 37. PLL Waveforms for Deskewing Clocks

Table 4. PLL operating conditions

Symbol	Parameter	Min	Max	Unit	Output Frequency
t_{RISE}	Input clock rise time		5	ns	
t_{FALL}	Input fall time		5	ns	
t_{INDUTY}		40	60	%	
F_{CLK1}	Input Clock Frequency with multiplication factor of 1	30	150	MHz	30 to 150 MHz
F_{CLK2}	Input Clock Frequency with multiplication factor of 2	16	100	MHz	32 to 200 MHz
F_{CLK3}	Input Clock Frequency with multiplication factor of 3	16	66	MHz	48 to 198 MHz
$t_{INCLKSTB}$	Input Clock Stability (between adjacent clocks)		100	ps	
t_{LOCK}	Time for PLL to acquire lock		30	µs	
$t_{TOTJITTER}$	Total jitter on PLL output (both accumulated and phase-to-phase measures as peak-to-peak)		500	ps	
$t_{OUTDUTY}$	Duty cycle for PLL output	40	60	%	

The PLL can also be used to synthesize on-chip clocks that are multiples of the system clock frequency, up to a maximum of 200MHz. For example, if the system clock operates at 66MHz, the on-chip PLL can double the clock to 132MHz or triple it to 198MHz. If the system clock runs at 100 MHz, the PLL can double it to 200 MHz for use within the VF1 FPGA.

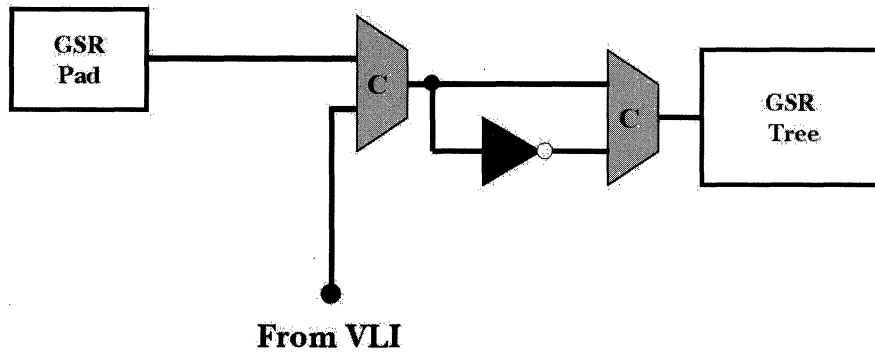
Table 4 lists the PLL operating conditions.

As shown in Table 4 (see t_{LOCK} signal), the PLL will acquire a lock on the reference clock within 30 µs, but it may acquire a lock much sooner. A LOCK status signal goes high when a lock is

acquired, so it is possible either to wait 30 µs or to test the LOCK signal to assure that the PLL has acquired a lock.

Global Set/Reset

The VF1 global set/reset signal (Figure 38) may be generated externally and applied to the VF1 FPGA via the Global Set/Reset input pin, or it may be generated within the VF1 FPGA. In addition, the polarity of the set/reset signal may be selected. Both of these conditions are determined at configuration time.



VF1ds-038

Figure 38. Global Set/Reset

Design Methodology

Complex systems with greater than 10K gates require a sophisticated software-based design methodology. While a schematic-based methodology may be adequate for smaller designs, and sometimes for portions of larger designs, a hardware-description language (HDL) is more appropriate for developing complex designs.

The Vantis design flow consists of two parts (Figure 39):

- **Design development** using third-party front-end development tools. These tools provide design entry, simulation, synthesis, and timing analysis. Designs are transferred from these tools to the Vantis tools in an EDIF file format. Some third-party tools can provide timing constraint files for use by the Vantis tools.
- **Design implementation** using Vantis physical design tools. These technology-specific tools provide optimization, mapping, timing calculation, and device programming. The output is a JEDEC bit-stream file for programming VF1 FPGAs via the JTAG port or the dedicated programming port.

The Vantis tools include a design manager, graphical user interface, and a logic editor and viewer. The logic editor and viewer enable viewing and moving logic elements down to the VGB level.

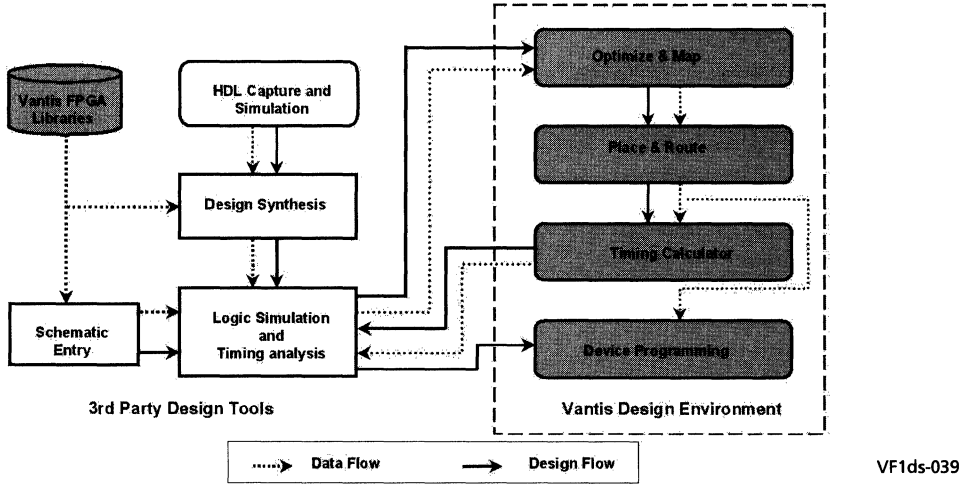
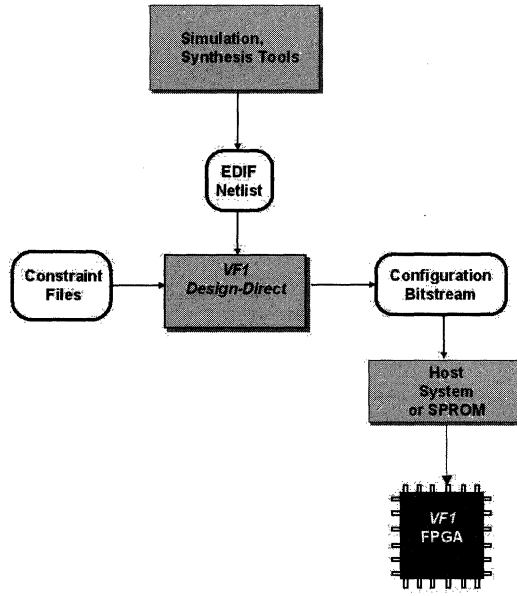


Figure 39. Vantis Design Methodology

Vantis design environment tools are timing driven, using timing constraint files that are provided by the third-party front-end tools (Figure 40). The Vantis tools generate timing files that can be fed back to the front-end tools for further simulation and timing analysis. The output of the design process is a configuration bitstream that is loaded a VF1 FPGA during configuration.



VF1ds-040

Figure 40. DesignDirect Inputs and Outputs

Detailed descriptions of the Vantis design methodology and tools are found in the *Design Methodology Users Manual* on the software CD-ROM.

JTAG Compatibility

VF1 family FPGA products are fully compliant with JTAG 1149.1. They implement the following standard JTAG instructions:

- BYPASS
- SAMPLE/PRELOAD
- EXTEST
- HIGHZ
- USERCODE
- IDCODE
- INTEST

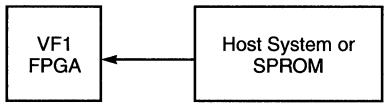
In addition, they implement three non-standard instructions that are used for configuring the VF1 FPGAs through the JTAG port. These instructions are described in the *Configuration modes* section that follows.

Configuration Modes

The VF1 family of devices consists of SRAM-based reprogrammable FPGAs that are configured, or programmed, every time they are powered up. Configuration is the process of loading configuration data into the device from either a companion SPROM or a host system (Figure 41).

The configuration data defines the device's functionality. In addition to power-up configuration, VF1 FPGAs can be reconfigured during operation (in-system programming) if the host system decides to change the device's functionality.

The following is a general description of each configuration mode. Detailed descriptions of all modes and timing are contained in the *VF1 Configuration Guide* Technical Note. The Vantis *VCM SPROM* data sheet describes the companion SPROM.



VF1ds-041

Figure 41. Configuring a VF1 FPGA

The VF1 FPGA family supports five configuration modes, two that use SPROMs and three that depend on a host processor. The modes are:

- **Master serial mode.** The VF1 automatically loads its configuration data from an external serial PROM.
- **Slave serial mode.** When two or more VF1 FPGAs in a system are loaded from the same PROM, the first device loaded is loaded in Master serial mode and subsequent devices are loaded in Slave serial mode. In this mode, the master device provides the CCLK signal to slave devices.
- **Asynchronous peripheral mode.** A host device provides configuration data a byte at a time in parallel to the VF1 FPGA. The VF1 FPGA serializes the data internally for loading.
- **Synchronous peripheral mode.** A host device provides the load clock to the VF1 FPGA and provides byte-wide configuration data on every eighth clock pulse.
- **JTAG mode.** The VF1 FPGA configuration data is loaded via the JTAG boundary scan circuitry. A host, such as a microprocessor, controls loading and provides configuration data.

Configuration modes are selected by the three mode pins, M0-M2, as shown in Table 5.

Table 5. Configuration Mode Selection Pins

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Synchronous Peripheral	0	1	1
Asynchronous Peripheral	1	0	1
JTAG	0	0	1

Modes are described briefly below. The Technical Note *VF1 Configuration Guide* provides comprehensive guidelines.

With the exception of the pins directly involved in configuration, all VF1 I/O pins are in three-state mode during configuration. Following configuration the state of the I/O pins is determined by the configuration pattern. Table 5 lists the pins that are used by the various configuration modes.

Table 6. Pins Used in Configuration Modes

Master Serial	Slave Serial	Synchronous Peripheral	Asynchronous Peripheral	JTAG	User Operation
M0 (I)	M0 (I)	M0 (I)	M0 (I)	M0 (I)	(I/O)/RTRIG
M1 (I)	M1 (I)	M1 (I)	M1 (I)	M1 (1)	(I/O)/RDO
M2 (I)	M2 (I)	M2 (I)	M2 (I)	M2 (I)	(I/O)
/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)	/PROGRAM (I)
/INIT (OD)	/INIT (OD)	/INIT (OD)	/INIT (OD)	/INIT (OD)	(I/O)
DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)
HDC (O)	HLC (O)	HLC (O)	HLC (O)		(I/O)
/LDC (O)	/LDC (O)	/LDC (O)	/LDC (O)		(I/O)
CCLK (O)	CCLK (I)	CCLK (I)	CCLK (O)		CCLK (I)
TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)
TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)
TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)
TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)
DOUT (O)	DOUT (O)	DOUT (O)	DOUT (O)		(I/O)
DIN0 (I)	DIN0 (I)	DIN0 (I)	DIN0 (I)		(I/O)
		DIN1 (I)	DIN1 (I)		(I/O)
		DIN2 (I)	DIN2 (I)		(I/O)
		DIN3 (I)	DIN3 (I)		(I/O)
		DIN4 (I)	DIN4 (I)		(I/O)
		DIN5 (I)	DIN5 (I)		(I/O)
		DIN6 (I)	DIN6 (I)		(I/O)
		DIN7 (I)	DIN7 (I)		(I/O)
		RDY/(/BUSY) (O)	RDY/(/BUSY) (O)		(I/O)
			/CS0 (I)		(I/O)
			CS1 (I)		(I/O)
			/WS (I)		(I/O)
			/RS (I)		(I/O)

Notes:
I = Input
O = Output
OD = Open Drain
I/O = Input/Output

Functions of the configuration mode signals are described below. Refer to the individual mode descriptions that follow for timing relationships of these signals.

M0/RTRIG **M1/RDO** **M2**	**Three multiplexed I/O pins that select the configuration mode.** During configuration, these pins are input pins and are sampled right after initialization to determine the configuration mode. In normal mode, M0 and M1 can be used as RTRIG and RDO for non-JTAG read-back.
/PROGRAM	**A dedicated input pin that initiates configuration.** A low level clears the configuration memory and puts the device into a WAIT state. The MODE pins are sampled. A low-to-high transition clears the configuration memory once more and starts the configuration process. If this pin is high during power up, the device will skip the WAIT state after clearing the configuration memory and will go directly into configuration mode.
/INIT	**A multiplexed I/O pin that indicates initialization status.** During device configuration /INIT is an open-drain status pin that can also be used to reset the serial EPROM for a Master device. A low /INIT when /PROGRAM is high indicates initialization is not complete and the device is not ready to receive data for configuration. Tying all the /INIT pins from different devices together ensures the Master device does not start configuration until all slave devices are initialized. For non-JTAG configuration modes, holding the /INIT pin low externally will delay configuration.
DONE	**A dedicated open drain pin that signals when configuration is done.** A low output indicates the device is in configuration. A high output indicates configuration is done and all the I/Os will be enabled. For non-JTAG configuration modes, enabling of all the I/Os in different devices can be synchronized by tying all the DONE pins together.
HDC	**A multiplexed I/O status pin that is Low During Configuration.**
/LDC	**A multiplexed I/O status pin that is Low During Configuration.**
CCLK	**A dedicated I/O pin for configuration clock input or output.** In the Master mode, this pin is the clock output from an internal oscillator that drives the serial EPROM and Slave VF1 FPGAs. In the Slave mode and Synchronous Peripheral mode, this pin receives a clock from the Master VF1 FPGA or from a host source.
TDI, TCLK, TMS, TDO	**TDI, TCLK, and TMS are dedicated input pins; TDO is a dedicated output pin.** These pins are used for JTAG boundary scan functions and for programming VF1 FPGAs in JTAG mode.
DOUT	**A multiplexed I/O pin to pass configuration data from the first VF1 FPGA in a chain to subsequent devices.** During configuration, this is an output pin for sending DIN data to daisy-chained devices.
DIN0-7	**Seven multiplexed I/O pins for byte-wide data input.** During Synchronous and Asynchronous Peripheral modes, these input pins receive parallel configuration data.
RDY/(/BUSY)	**A multiplexed I/O Ready or Busy status pin.** This pin indicates when it is appropriate to write another byte of data into the VF1 FPGA during Peripheral mode configuration. In Asynchronous peripheral mode, the pin is high (RDY) when the VF1 is ready to receive data, and it is low (/BUSY) when the VF1 is processing the last byte it received. In Synchronous peripheral mode, the signal is normally low and goes high for one CCLK period to acknowledge the receipt of a byte of configuration data.
/CS0, CS1, /WS, /RS	**Multiplexed I/O pins.** These four inputs are used in Asynchronous Peripheral mode. The chip is selected when /CS0 is low and CS1 is high. While the chip is selected, a low on /WS loads the data on DIN [0:7] into the internal data register. A low on /RS changes DIN7 into a status pin that outputs the same signal as the RDY/(/BUSY) pin.

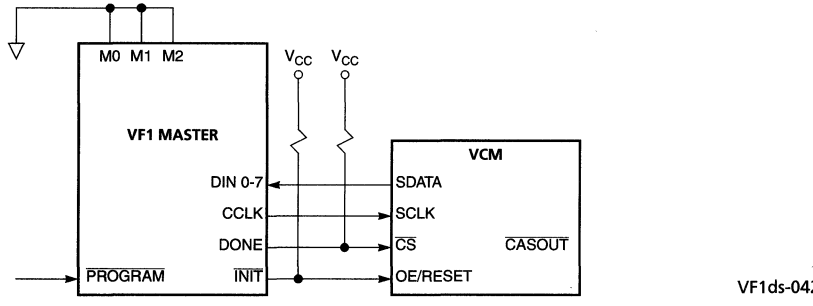


Figure 42. Master Serial Mode

Master Serial Mode

In Master serial mode, configuration data is loaded automatically from a serial PROM into the VF1 FPGA (Figure 42). On power-up, or when a PROGRAM command is received, both the /INIT signal and the DONE signal from the VF1 FPGA go low, generating /CE and /RESET signals to the serial EEPROM.

The /INIT signal goes high, enabling the output of the EEPROM. The VF1 FPGA generates the configuration clock, CCLK, and applies it to the EEPROM. CCLK clocks the configuration data out of the EEPROM and clocks it into the VF1 FPGA.

If two or more EEPROMs are required to hold the configuration data, the first EEPROM pulls its /CASOUT signal low when it has loaded its last data bit, enabling the second EEPROM to provide subsequent configuration data. The loading continues until the VF1 FPGA is fully configured at which time DONE goes high, halting the configuration process.

Configuration can also be initiated by the /PROGRAM command.

Both /INIT and DONE are open-collector drivers that require external pull-up resistors.

Slave Serial Mode

Slave serial mode is normally used when two or more VF1 FPGAs are configured in a daisy chain (Figure 43). In Figure 43 first VF1 FPGA in the chain is configured as a Master and all following devices are slaves. Two SPROMs are shown to illustrate how they may be cascaded to provide adequate storage for multiple configuration bitstreams. The Master VF1 FPGA generates the CCLK configuration clock for all devices in the chain as well as for the SPROMs.

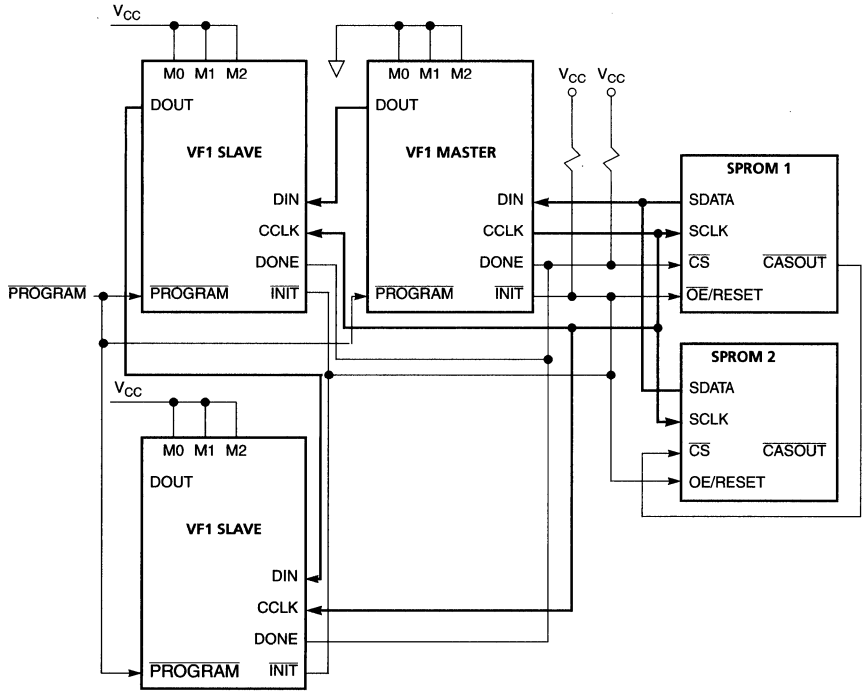


Figure 43. Slave Serial Mode

Configuration starts and proceeds the same as in Master serial mode until the Master device is loaded. At that point, the Master transmits subsequent configuration data out on its DOUT pin. That data goes to the DIN pin of the second device. When that device is loaded, it transmits subsequent data on its DOUT pin to the third device. This process continues until all VF1 FPGAs in the chain have been configured.

Figure 43 shows VF1 slave-mode devices following a master-mode device. This is not the only case in which slave-mode configuration is used. It may also be used following VF1 FPGAs configured in Synchronous or Asynchronous peripheral modes, or when a host system configures a VF1 FPGA directly in serial mode.

Asynchronous Peripheral Mode

Asynchronous Peripheral mode is used to load one or more VF1 FPGAs with byte-wide data from a microprocessor bus (Figure 44). The VF1 FPGA serializes each byte internally, so this mode offers no speed advantage over serial modes. Data transfer is made on the trailing edge of the logical AND of signals /WS and /CS0 being low and /RS and /CS1 being high. Chip select signals can be cycled or maintained at a static level during the configuration process. Each byte of data is written into the VF1 FPGA's DIN [7:0] input pins.

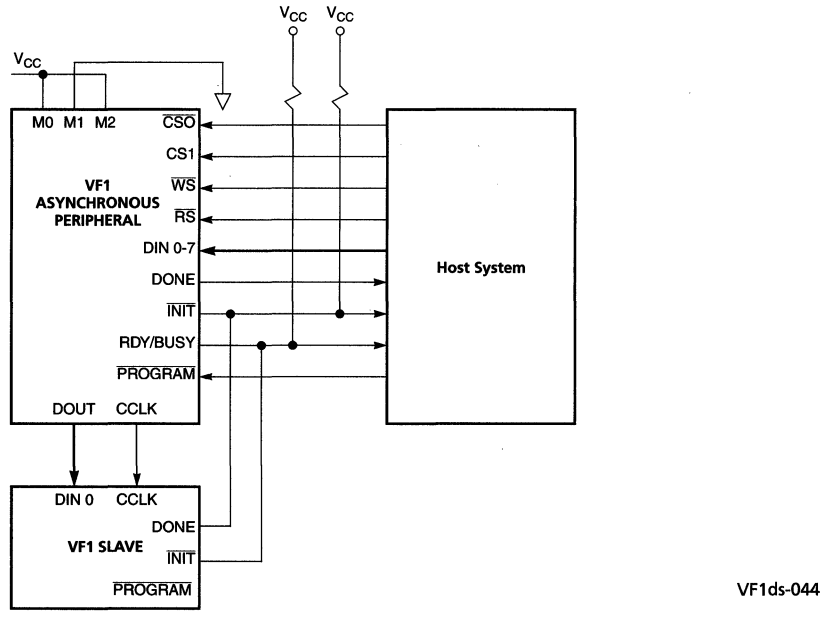


Figure 44. Asynchronous Peripheral Mode

When two or more VF1 FPGAs are daisy-chained for configuration, the lead device loads itself first and then it presents serial configuration data on its DOUT pin. It also generates the CCLK clock signal to control shifting of data into subsequent slave-mode devices in the daisy chain.

The RDY/(/BUSY) status output indicates when another byte can be loaded from the host system. A high indicates that the VF1 FPGA is ready to receive another byte, while a low indicates that it cannot accept a byte. The length of the low signal will vary depending on the shifting status of previously loaded bytes. In addition to appearing on its status pin, the RDY/(/BUSY) signal can be multiplexed on the DIN7 pin by setting chip select pin /WR high and setting pin /RD low.

Synchronous Peripheral Mode

In Synchronous Peripheral mode, a host system presents byte-wide data over a microprocessor bus and controls shifting of that data by inputting a clock signal to the VF1 FPGA's CCLK pin (Figure 45). The first data byte is clocked into the VF1 FPGA on the rising edge of the second CCLK pulse after /INIT goes high. Bytes are then clocked in on every eighth CCLK pulse. In this mode, the RDY/(/BUSY) signal acknowledges the loading of the byte by going high for one CCLK period on the same clock that loaded the byte. CCLK must remain active after the last byte is loaded to complete the shifting.

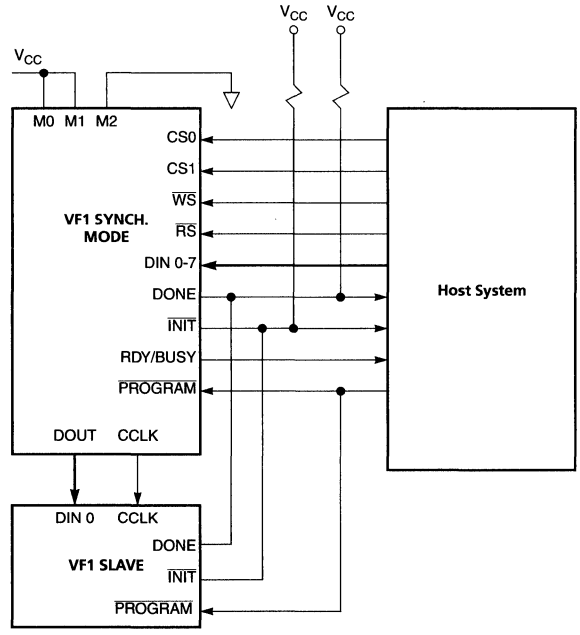


Figure 45. Synchronous Peripheral Mode

Synchronous Peripheral mode can be used in daisy-chain configurations. The first VF1 FPGA in the chain loads itself, and then presents serial data on its DOUT pin for loading into the following devices in the chain. CCLK is applied in parallel to all devices from the host system. The data appears on DOUT 1.5 cycles after it is loaded in parallel, which means that DOUT changes on a falling CCLK edge and the next VF1 FPGA loads data on the next rising edge.

JTAG Mode

In JTAG mode, VF1 FPGAs are configured using the JTAG pins TCLK, TMS TDI, and TDO. Three additional JTAG instructions support JTAG configuration mode:

- **PROG_MODE.** This instruction places the VF1 FPGA in programming mode.
- **PROGRAM.** Once the VF1 FPGA is in programming mode, this instruction shifts configuration data into the VF1 FPGA.
- **VERIFY.** After configuration this instruction is used to read back all configuration, VGB and I/O flip-flops, and embedded SRAM bits in the device.

A host system such as a microprocessor controls the configuration of the VF1 FPGA or devices and supplies configuration data. The host also provides the configuration clock.

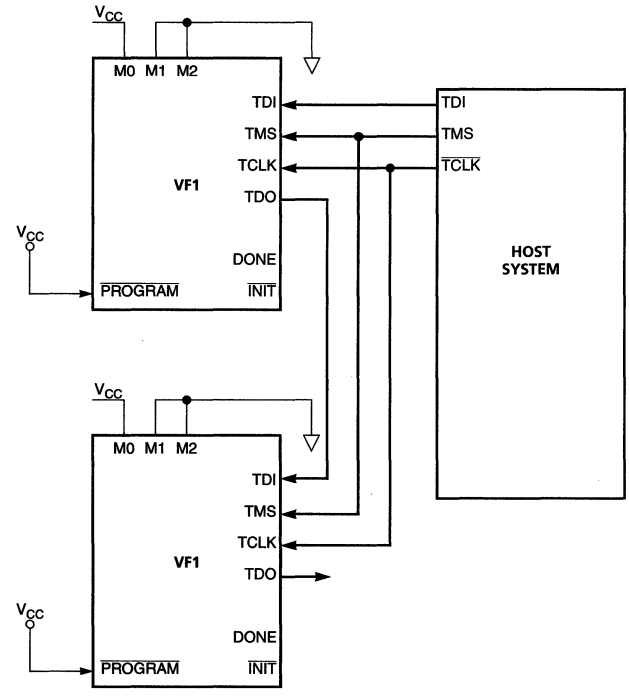


Figure 46. JTAG Mode

If two or more VF1 FPGAs are to be configured, they are arranged in a daisy chain with all devices selected for JTAG mode configuration (Figure 46). Data is applied to the TDI pin of the first device and the TDO pin of that device is connected to the TDI pin of the next device. The TMS and TCLK signals from the host are applied to all VF1 FPGAs in parallel.

In-System Programming

A VF1 FPGA is normally loaded with a configuration program when its host system is powered up. As described in the section above, this is often accomplished by loading the program from a separate SPROM. In the case of the Vantis VF1 family, the program may also be loaded through the JTAG port or the dedicated programming port.

The typical FPGA, however, is part of a larger system that includes a microprocessor. The system design can often be simplified by having the microprocessor, rather than a separate serial PROM, configure the VF1 FPGA. The microprocessor can configure the VF1 FPGA using host-driven Slave mode, Asynchronous Peripheral mode, Synchronous Peripheral mode, or JTAG mode. In most applications, JTAG mode will be used.

Using a host microprocessor to load the VF1 FPGA simplifies making design changes or installing ECOs after the device has been installed in a system. The new configuration program can simply be loaded into the microprocessor and then loaded into the VF1 FPGA, eliminating the need to swap PROMs or any other physical part of the system. It also allows dynamic changing of system

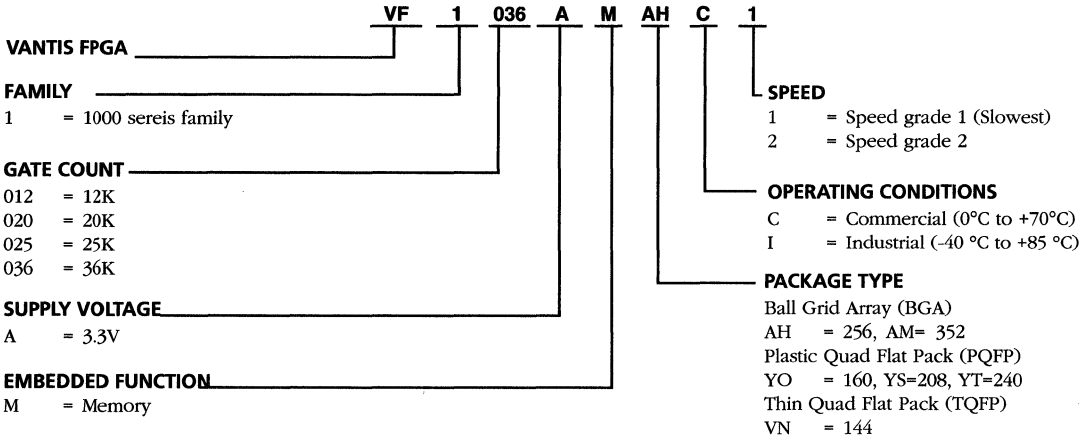
functionality by allowing multiple configuration programs to reside in the host system and be loaded into the VF1 FPGAs as needed.

Core Program

Vantis plans to offer high-value, reusable cores as part of its VF1 family. The first cores in this program are PCI cores that support both the 33MHz and 66MHz standards. Detailed information will be published later.

ORDERING INFORMATION

Vantis VF1 Series FPGAs



TECHNICAL SPECIFICATIONS

The following pages contain preliminary technical specifications for the VF1 family.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Device Junction Temperature . . . . . +120°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +4.0 V

DC Input Voltage . . . . . -0.5 to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C) . . . . . 200 mA

Note:

Stresses above those listed under Absolute Maximum Ratings may cause permantent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground. . . . . +3.0 V to +3.6 V

Note:

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Parameter	Parameter Description	Min	Max	Unit
V_{IH}	Input High Voltage	2.0		V
V_{IL}	Input Low Voltage		0.8	V
I_{IH1}	Input High Leakage Current (Vin = Max V_{CC} = 3.6V)		10.0	µA
I_{IL1}	Input Low Leakage Current (Vin = 0V)		-10.0	µA
I_{IH2}	Input High Leakage Current with Pull Up (Vin = Max V_{CC}=3.6V)		10.0	µA
I_{IL2}	Input Low Leakage Current with Pull Up (Vin = 0V)		-100.0	µA
I_{IH3}	Input High Leakage Current with Bus Friendly (Vin = Max V_{CC}=3.6V)		10.0	µA
I_{IL3}	Input Low Leakage Current with Bus Friendly (Vin = 0V)		-10.0	µA
V_{OH}	Output High Voltage @ I_{OH} = -4.0mA (LVTTL) (V_{CC} = 3.0V)	2.4		V
	Output High Voltage @ I_{OH} = -500uA (LVCMOS) (V_{CC} = 3.0V)	0.9V_{CC}		V
V_{OL}	Output Low Voltage @ I_{OL} = 12.0mA (LVTTL) (V_{CC} = 3.0V)		0.4	V
	Output Low Voltage @ I_{OL} = 1.5mA (LVCMOS) (V_{CC} = 3.0V)		0.1V_{CC}	V
I_{OZH1}	Off State Output Leakage with Bus High		10.0	µA
I_{OZL1}	Off State Output Leakage with Bus Low		-10.0	µA
I_{OZH2}	Off State Output Leakage with Bus High (Pull Up) (Note 1)		10.0	µA
I_{OZL2}	Off State Output Leakage with Bus Low (Pull Up) (Note 1)		-100.0	µA
I_{OZH3}	Off State Output Leakage with Bus High (Bus Friendly)		10.0	µA
I_{OZL3}	Off State Output Leakage with Bus Low (Bus Friendly)		-10.0	µA
I_{SC}	Output Short Circuit Current (Vout = 0.5V) (V_{CC} = Max V_{CC} = 3.6V)		300.0	mA
SI_{CC}	Standby Supply Current (Nominal V_{CC})		6.0	mA

Notes:

1. *JTAG and dedicated configuration pins have only Pull Up option.*
2. *Usage of PLL adds 20mA per PLL to the dynamic I_{CC}.*

AC CHARACTERISTICS

The following tables contain preliminary AC timing parameters for the VF1 FPGA family. It is recommended that the timing analysis tools in Vantis' DesignDirect software be used to calculate timing for a design. However, the following tables can be used to develop approximate delays for small circuits. Interconnect delays and interconnect driver delays are not included in these tables. Timing information will be updated as final characterization is done. The latest timing information is published on the Vantis Web site (www.vantis.com).

Input AC Parameters

IOB General Input Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{IN}	IOB Standard Input Delay	IOB to Direct Connect to CBB 4LUT	0.9	0.7	ns
t_{INXL}	IOB Transparent Input Latch Delay without Delay		1.5	1.2	ns
t_{INXLD}	IOB Transparent Input Latch Delay with Delay		6.4	5.3	ns
t_{ILLEA}	Input Long Line Enable Time		1.8	1.5	ns
t_{ILLER}	Input Long Line Disable Time		2.4	2.0	ns

IOB Input Set/Reset Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ISRGO}	IOB Input Register (Latch) Global Set/Reset → Interconnect Lines	1.5	1.2	ns
t_{ISRLO}	IOB Input Register (Latch) Local Set/Reset → Interconnect Lines	2.4	2.0	ns
$t_{ISRGREC}$	IOB Input Register (Latch) Global Set/Reset Recovery Time	0.5	0.4	ns
$t_{ISRLREC}$	IOB Input Register (Latch) Local Set/Reset Recovery Time	1.0	0.8	ns

IOB Input Register (Latch) Global Clock (Gate) Delays

Parameter	Parameter Description	-1	-2	Unit
t_{IRLGS}	IOB Input Register (Latch) Global Clock (Gate) Setup Time Without Delay	0.0	0.0	ns
t_{IRLGH}	IOB Input Register (Latch) Global Clock (Gate) Hold Time Without Delay	0.8	0.6	ns
t_{IRLGSD}	IOB Input Register (Latch) Global Clock (Gate) Setup Time With Delay	5.0	4.1	ns
t_{IRLGHD}	IOB Input Register (Latch) Global Clock (Gate) Hold Time With Delay	0.0	0.0	ns
t_{IRLGCO}	IOB Input Register (Latch) Global Clock (Gate) → Interconnect Lines	1.8	1.5	ns
$t_{IRLGCES}$	IOB Input Register (Latch) Global Clock Enable Setup Time	0.9	0.7	ns
$t_{IRLGCEH}$	IOB Input Register (Latch) Global Clock Enable Hold Time	0.0	0.0	ns

IOB Input Register (Latch) Local Clock (Gate) Delays

Parameter	Parameter Description	-1	-2	Unit
t_{IRLLS}	IOB Input Register (Latch) Local Clock (Gate) Setup Time Without Delay	0.0	0.0	ns
t_{IRLLH}	IOB Input Register (Latch) Local Clock (Gate) Hold Time Without Delay	1.8	1.5	ns
t_{IRLLSD}	IOB Input Register (Latch) Local Clock (Gate) Setup Time With Delay	4.0	3.3	ns
t_{IRLLHD}	IOB Input Register (Latch) Local Clock (Gate) Hold Time With Delay	0.0	0.0	ns
t_{IRLLCO}	IOB Input Register (Latch) Local Clock (Gate) → Interconnect Lines	2.8	2.3	ns

IOB Input Register (Latch) Local Clock (Gate) Delays (Continued)

Parameter	Parameter Description	-1	-2	Unit
$t_{IRLLCES}$	IOB Input Register (Latch) Local Clock Enable Setup Time	0.0	0.0	ns
$t_{IRLLCEH}$	IOB Input Register (Latch) Local Clock Enable Hold Time	0.8	0.6	ns

Output AC Parameters

IOB General Output Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{OUT}	IOB Standard Output Delay to Pad	CBB 4LUT Direct Connect to IOB	4.0	3.3	ns
t_{OEA}	Output Buffer Enable Time		4.5	3.7	ns
t_{OER}	Output Buffer Disable Time		6.2	5.1	ns
t_{SLW}	Output Buffer Slow Slew Rate Adder		1.8	1.5	ns

IOB Output Set/Reset Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORSRGO}	IOB Output Register Global Set/Reset → Pad	4.1	3.4	ns
t_{ORSRLO}	IOB Output Register Local Set/Reset → Pad	5.1	4.2	ns
t_{ORGREC}	IOB Output Register Global Set/Reset Recovery Time	0.5	0.4	ns
t_{ORLREC}	IOB Output Register Local Set/Reset Recovery Time	1.0	0.8	ns

IOB Output Register Global Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORGS}	IOB Output Register Global Clock Setup Time	0.4	0.3	ns
t_{ORGH}	IOB Output Register Global Clock Hold Time	0.4	0.3	ns
t_{ORGCO}	IOB Output Register Global Clock → Pad	4.5	3.7	ns
t_{ORGCES}	IOB Output Register Global Clock Enable Setup Time	1.0	0.8	ns
t_{ORGCEH}	IOB Output Register Global Clock Enable Hold Time	0.0	0.0	ns

IOB Output Register Local Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{ORLS}	IOB Output Register Local Clock Setup Time	0.0	0.0	ns
t_{ORLH}	IOB Output Register Local Clock Hold Time	1.4	1.1	ns
t_{ORLCO}	IOB Output Register Local Clock → Pad	5.4	4.5	ns
t_{ORLCES}	IOB Output Register Local Clock Enable Setup Time	0.0	0.0	ns
t_{ORLCEH}	IOB Output Register Local Clock Enable Hold Time	0.8	0.6	ns

CBB AC Parameters

Combinatorial Configurable Building Block (CBB) Delays

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{3LUT}	CBB Input → LUT → CBB Output (3-LUT)	IOB to Direct Connect to CBB to Direct Connect to IOB	2.2	1.8	ns
t_{4LUT}	CBB Input → LUT → CBB Output (4-LUT)		3.2	2.6	ns
t_{5LUT}	CBB Input → LUT → CBB Output (5-LUT)		3.6	3.0	ns
t_{6LUT}	CBB Input → LUT → CBB Output (6-LUT)		5.8	4.8	ns
t_{WG}	CBB Input → LUT → CBB Output (Wide Gate)		4.1	3.4	ns
t_{VFP}	CBB 3LUT Feedthrough		2.1	1.7	ns

Registered Configurable Building Block (CBB) VGB Global Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{3LUTGS}	CBB Input → VGB Global Clock Setup Time (3-LUT)	1.2	1.0	ns
t_{4LUTGS}	CBB Input → VGB Global Clock Setup Time (4-LUT)	2.2	1.8	ns
t_{5LUTGS}	CBB Input → VGB Global Clock Setup Time (5-LUT)	2.6	2.1	ns
t_{6LUTGS}	CBB Input → VGB Global Clock Setup Time (6-LUT)	4.7	3.9	ns
t_{WGGS}	CBB Input → VGB Global Clock Setup Time (Wide Gate)	3.0	2.5	ns
t_{3LUTGH}	CBB Input → VGB Global Clock Hold Time (3-LUT)	0.0	0.0	ns
t_{4LUTGH}	CBB Input → VGB Global Clock Hold Time (4-LUT)	0.0	0.0	ns
t_{5LUTGH}	CBB Input → VGB Global Clock Hold Time (5-LUT)	0.0	0.0	ns
t_{6LUTGH}	CBB Input → VGB Global Clock Hold Time (6-LUT)	0.0	0.0	ns
t_{WGGH}	CBB Input → VGB Global Clock Hold Time (Wide Gate)	0.0	0.0	ns
t_{VGCO}	VGB Global Clock → CBB Output	1.8	1.5	ns
t_{VGCES}	VGB Global Clock Enable Setup Time	0.5	0.4	ns
t_{VGCEH}	VGB Global Clock Enable Hold Time	0.4	0.3	ns
t_{VGSR}	VGB Global Set/Reset → CBB Output	1.4	1.1	ns
t_{VGREC}	VGB Global Set/Reset Recovery Time	0.3	0.2	ns

Super VGB Control Signals

Parameter	Parameter Description	-1	-2	Unit
t_{VFF}	VGB Feedthrough	1.1	0.9	ns
t_{SDEA}	Shared Driver Enable Time	2.4	2.0	ns
t_{SDER}	Shared Driver Disable Time	2.8	2.3	ns

Registered Configurable Building Block (CBB) VGB Local Clock Delays

Parameter	Parameter Description	-1	-2	Unit
t_{3LUTLS}	CBB Input → VGB Local Clock Setup Time (3-LUT)	0.5	0.4	ns
t_{4LUTLS}	CBB Input → VGB Local Clock Setup Time (4-LUT)	1.4	1.1	ns
t_{5LUTLS}	CBB Input → VGB Local Clock Setup Time (5-LUT)	1.8	1.5	ns
t_{6LUTLS}	CBB Input → VGB Local Clock Setup Time (6-LUT)	4.0	3.3	ns
t_{WGLS}	CBB Input → VGB Local Clock Setup Time (Wide Gate)	2.3	1.9	ns
t_{3LUTLH}	CBB Input → VGB Local Clock Hold Time (3-LUT)	0.0	0.0	ns
t_{4LUTLH}	CBB Input → VGB Local Clock Hold Time (4-LUT)	0.0	0.0	ns
t_{5LUTLH}	CBB Input → VGB Local Clock Hold Time (5-LUT)	0.0	0.0	ns
t_{6LUTLH}	CBB Input → VGB Local Clock Hold Time (6-LUT)	0.0	0.0	ns
t_{WGLH}	CBB Input → VGB Local Clock Hold Time (Wide Gate)	0.0	0.0	ns
t_{VLCO}	VGB Local Clock → CBB Output	2.4	2.0	ns
t_{VLCES}	VGB Local Clock Enable Setup Time	0.0	0.0	ns
t_{VLCEH}	VGB Local Clock Enable Hold Time	1.0	0.8	ns
t_{VLSR}	VGB Local Set/Reset → CBB Output	2.0	1.6	ns
t_{VLREC}	VGB Local Set/Reset Recovery Time	0.0	0.0	ns

VGB Carry Logic AC Parameters

VGB Combinatorial High Speed Carry Logic

Parameter	Parameter Description	Test Conditions	-1	-2	Unit
t_{OPSUM}	Operand/Control Input → Sum Logic Output → CBB Output	Direct Connect to CBB 3LUT Carry Logic	2.6	2.1	ns
$t_{OPCARRY}$	Operand/Control Input → Carry Logic Output		2.1	1.7	ns
t_{CSUM}	Carry Logic Input → Sum Logic Output → CBB Output		1.0	0.8	ns
t_{CCARRY}	Carry Logic Input → Carry Logic Output		0.4	0.3	ns

VGB Registered Global Clock High Speed Carry Logic

Parameter	Parameter Description	-1	-2	Unit
t_{OPGS}	Operand/Control Input → Sum Logic → VGB Global Clock Setup Time	1.6	1.3	ns
t_{OPGH}	Operand/Control Input → Sum Logic → VGB Global Clock Hold Time	0.0	0.0	ns
t_{CGS}	Carry Logic Input → Sum Logic → VGB Global Clock Setup Time	0.0	0.0	ns
t_{CGH}	Carry Logic Input → Sum Logic → VGB Global Clock Hold Time	0.6	0.5	ns

VGB Registered Local Clock High Speed Carry Logic

Parameter	Parameter Description	-1	-2	Unit
t_{OPLS}	Operand/Control Input → Sum Logic → VGB Local Clock Setup Time	0.9	0.7	ns
t_{OPLH}	Operand/Control Input → Sum Logic → VGB Local Clock Hold Time	0.0	0.0	ns
t_{CLS}	Carry Logic Input → Sum Logic → VGB Local Clock Setup Time	0.0	0.0	ns
t_{CLH}	Carry Logic Input → Sum Logic → VGB Local Clock Hold Time	1.2	1.0	ns

VF1 FAMILY PACKAGE PIN LISTS

VF1 family FPGA devices are available in five package types as listed in the table below. Pin lists for each package type and VF1 family device follow the table. The pin lists are arranged by package type and are sorted by signal type and name.

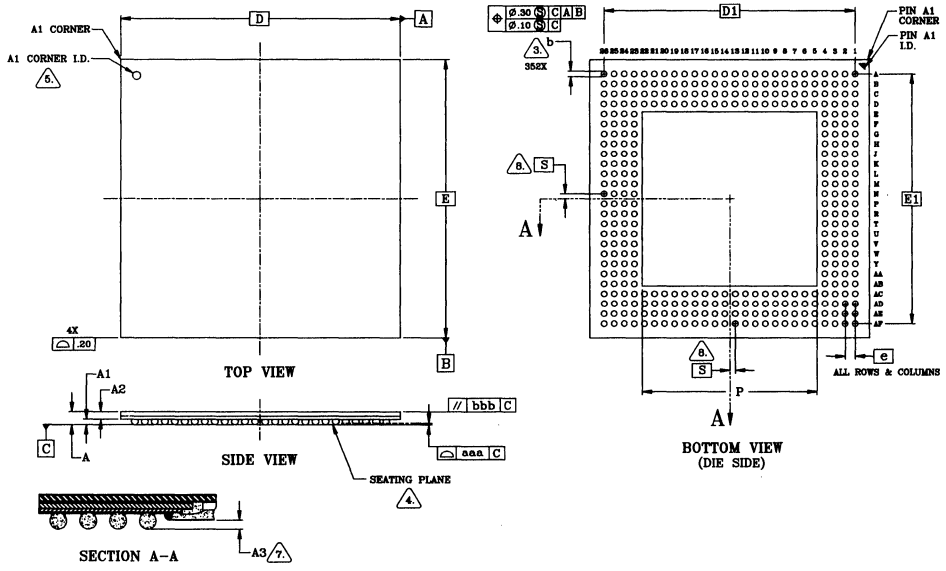
Within a given package, certain common signals appear on the same pins regardless of the VF1 FPGA in the package. For example, the VF1012, VF1020, VF1025, and VF1036 devices are available in the 256 BGA package. The SET/RESET signal, all CLKx inputs, JTAG interface signals, and all configuration signals appear on the same pins in the 256 BGA package for every member of the family. These common signals are listed at the beginning of each package type. These are followed by IOB (Input/Output Block) pin lists. IOB placement varies by family member within a single package type.

Each pin list includes a specification drawing of the package.

VF1 Family Package Options/Total Pins

Package	VF1012	VF1020	VF1025	VF1036
352 BGA			244	292
256 BGA	172	208	208	208
208 PQFP	168	168	168	168
160 PQFP	128	128		
144 TQFP	112			

352 BGA PACKAGE



Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD352 (MO-151(B)/BAR-2) Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3	0.15	0.45	seating plane clearance
D, E	35.00 BASIC		body size
D1, E1	31.75 BASIC		ball footprint
M	26 x 26		ball matrix size
N	352		total ball count
MR	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	20.4	21.2	encapsulation area
S	0.635 BASIC		solder ball placement

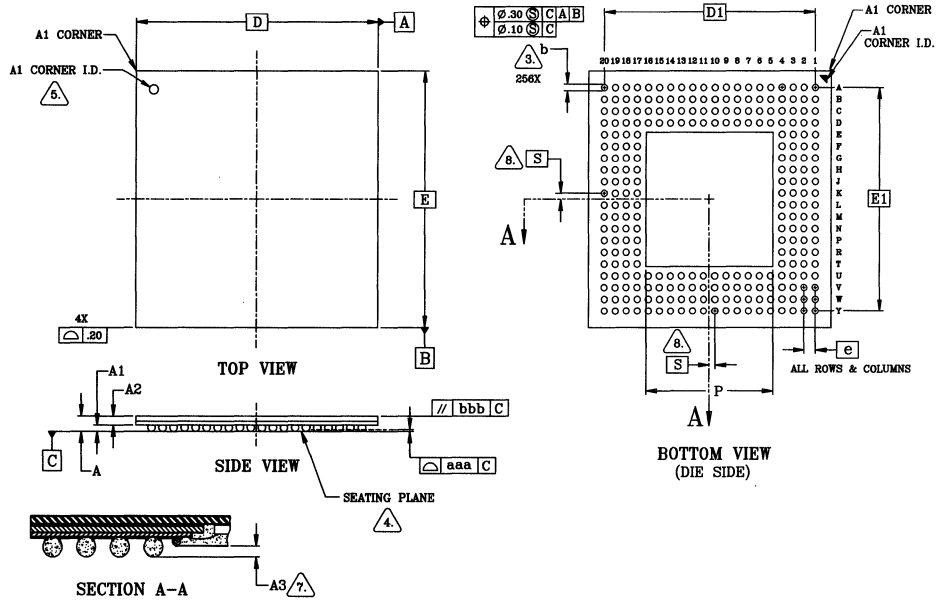
352 BGA Common Signals (VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	D1
	CLK0	B4
	CLK1	D25
	CLK2	AF23
	CLK3	AC1
JTAG Interface	TDI	D26
	TMS	D2
	TDO	AE4
	TCLK	A4
Configuration, Dedicated	PROGRAM	B23
	DONE	AC25
	CCLK	AF4
Configuration, Multiplexed	HDC	E26
	/LDC	E23
	/INIT	E24
	M0	E25
	M1	F26
	M2	AB26
	/CSO	AB25
	CS1	AB24
	/RS	AB23
	/WS	AC26
	RDY/(/BUSY)	AC2
	DOUT	AB1
	D7	AB4
	D6	AB3
	D5	AB2
	D4	F4
	D3	E1
	D2	E2
	D1	E3
	D0	E4
Power Pins	V_{CC} (17)	C3, AC3, C4, AC4, C23, AC23, C24, AC24, D3, AD3, D4, AD4, D13, AD23, D23, AD24, D24
	GND (35)	A1, B26, AE1, A2, C1, AE2, A3, C2, AE3, A24, C25, AE24, A25, C26, AE25, A26, N1, AE26, B1, P26, AF1, B2, AD1, AF2, B3, AD2, AF3, B24, AD25, AF13, B25, AD26, AF24, AF25, AF26

352 BGA INPUT/OUTPUT BLOCKS (VF1025, VF1036)

Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036	Signal	VF1025	VF1036
IOB1	A5	A5	IOB51	D20	D17	IOB101	V25	M26	IOB151	AE15	AE21	IOB201	V4	AF8	IOB251		P2
IOB2	D5	D5	IOB52	A21	A18	IOB102	V24	M25	IOB152	AD15	AC21	IOB202	U1	AE8	IOB252		P3
IOB3	C5	C5	IOB53	B21	B18	IOB103	V23	M24	IOB153	AC15	AD21	IOB203	U2	AD8	IOB253		P4
IOB4	B5	B5	IOB54	C21	C18	IOB104	W26	M23	IOB154	AF14	AF20	IOB204	U3	AC8	IOB254		N2
IOB5	A6	A6	IOB55	D21	D18	IOB105	W25	N26	IOB155	AE14	AE20	IOB205	U4	AF7	IOB255		N3
IOB6	B6	B6	IOB56	A22	A19	IOB106	W24	N25	IOB156	AD14	AD20	IOB206	T1	AE7	IOB256		N4
IOB7	D6	D6	IOB57	B22	B19	IOB107	W23	N24	IOB157	AC14	AC20	IOB207	T2	AD7	IOB257		M1
IOB8	C6	C6	IOB58	C22	C19	IOB108	Y26	N23	IOB158	AE13	AF19	IOB208	T3	AC7	IOB258		M2
IOB9	A7	A7	IOB59	D22	D19	IOB109	Y25	P25	IOB159	AD13	AE19	IOB209	T4	AF6	IOB259		M3
IOB10	B7	B7	IOB60	A23	A20	IOB110	Y24	P24	IOB160	AC13	AD19	IOB210	R1	AE6	IOB260		M4
IOB11	C7	C7	IOB61	E26	B20	IOB111	Y23	P23	IOB161	AF12	AC19	IOB211	R2	AD6	IOB261		L1
IOB12	D7	D7	IOB62	E23	C20	IOB112	AA26	R26	IOB162	AE12	AF18	IOB212	R3	AC6	IOB262		L2
IOB13	A8	A8	IOB63	E24	D20	IOB113	AA25	R25	IOB163	AD12	AE18	IOB213	R4	AF5	IOB263		L3
IOB14	B8	B8	IOB64	E25	A21	IOB114	AA24	R24	IOB164	AC12	AD18	IOB214	P1	AE5	IOB264		L4
IOB15	C8	C8	IOB65	F26	B21	IOB115	AA23	R23	IOB165	AF11	AC18	IOB215	P2	AD5	IOB265		K1
IOB16	D11	D8	IOB66	F25	C21	IOB116	AB26	T26	IOB166	AE8	AF17	IOB216	P3	AC5	IOB266		K2
IOB17	A12	A9	IOB67	F23	D21	IOB117	AB25	T25	IOB167	AD8	AE17	IOB217	P4	AC2	IOB267		K3
IOB18	B12	B9	IOB68	F24	A22	IOB118	AB24	T24	IOB168	AC8	AD17	IOB218	N2	AB1	IOB268		K4
IOB19	C12	C9	IOB69	G26	B22	IOB119	AB23	T23	IOB169	AF7	AC17	IOB219	N3	AB4	IOB269		J1
IOB20	D12	D9	IOB70	G25	C22	IOB120	AC26	U26	IOB170	AE7	AF16	IOB220	N4	AB3	IOB270		J2
IOB21	A13	A10	IOB71	G24	D22	IOB121	AE23	U25	IOB171	AD7	AE16	IOB221	M1	AB2	IOB271		J3
IOB22	B13	B10	IOB72	G23	A23	IOB122	AF22	U24	IOB172	AC7	AD16	IOB222	M2	AA1	IOB272		J4
IOB23	C13	C10	IOB73	H26	E26	IOB123	AC22	U23	IOB173	AF6	AC16	IOB223	M3	AA2	IOB273		H1
IOB24	A14	D10	IOB74	H25	E23	IOB124	AD22	V26	IOB174	AE6	AF15	IOB224	M4	AA4	IOB274		H2
IOB25	B14	A11	IOB75	H24	E24	IOB125	AE22	V25	IOB175	AD6	AE15	IOB225	L1	AA3	IOB275		H3
IOB26	C14	B11	IOB76	L23	E25	IOB126	AF21	V24	IOB176	AC6	AD15	IOB226	H2	Y1	IOB276		H4
IOB27	D14	C11	IOB77	M26	F26	IOB127	AE21	V23	IOB177	AF5	AC15	IOB227	H3	Y2	IOB277		G1
IOB28	A15	D11	IOB78	M25	F25	IOB128	AC21	W26	IOB178	AE5	AF14	IOB228	H4	Y3	IOB278		G2
IOB29	B15	A12	IOB79	M24	F23	IOB129	AD21	W25	IOB179	AD5	AE14	IOB229	G1	Y4	IOB279		G3
IOB30	C15	B12	IOB80	M23	F24	IOB130	AF20	W24	IOB180	AC5	AD14	IOB230	G2	W1	IOB280		G4
IOB31	D15	C12	IOB81	N26	G26	IOB131	AE20	W23	IOB181	AC2	AC14	IOB231	G3	W2	IOB281		F1
IOB32	A16	D12	IOB82	N25	G25	IOB132	AD20	Y26	IOB182	AB1	AE13	IOB232	G4	W3	IOB282		F2
IOB33	B16	A13	IOB83	N24	G24	IOB133	AC20	Y25	IOB183	AB4	AD13	IOB233	F1	W4	IOB283		F3
IOB34	C16	B13	IOB84	N23	G23	IOB134	AF19	Y24	IOB184	AB3	AC13	IOB234	F2	V1	IOB284		F4
IOB35	D16	C13	IOB85	P25	H26	IOB135	AE19	Y23	IOB185	AB2	AF12	IOB235	F3	V2	IOB285		E1
IOB36	A17	A14	IOB86	P24	H25	IOB136	AD19	AA26	IOB186	AA1	AE12	IOB236	F4	V3	IOB286		E2
IOB37	B17	B14	IOB87	P23	H24	IOB137	AC19	AA25	IOB187	AA2	AD12	IOB237	E1	V4	IOB287		E3
IOB38	C17	C14	IOB88	R26	H23	IOB138	AF18	AA24	IOB188	AA4	AC12	IOB238	E2	U1	IOB288		E4
IOB39	D17	D14	IOB89	R25	J26	IOB139	AE18	AA23	IOB189	AA3	AF11	IOB239	E3	U2			
IOB40	A18	A15	IOB90	R24	J25	IOB140	AD18	AB26	IOB190	Y1	AE11	IOB240	E4	U3			
IOB41	B18	B15	IOB91	R23	J24	IOB141	AC18	AB25	IOB191	Y2	AD11	IOB241		U4			
IOB42	C18	C15	IOB92	T26	J23	IOB142	AF17	AB24	IOB192	Y3	AC11	IOB242		T1			
IOB43	D18	D15	IOB93	T25	K26	IOB143	AE17	AB23	IOB193	Y4	AF10	IOB243		T2			
IOB44	A19	A16	IOB94	T24	K25	IOB144	AD17	AC26	IOB194	W1	AE10	IOB244		T3			
IOB45	B19	B16	IOB95	T23	K24	IOB145	AC17	AE23	IOB195	W2	AD10	IOB245		T4			
IOB46	C19	C16	IOB96	U26	K23	IOB146	AF16	AF22	IOB196	W3	AC10	IOB246		R1			
IOB47	D19	D16	IOB97	U25	L26	IOB147	AE16	AC22	IOB197	W4	AF9	IOB247		R2			
IOB48	A20	A17	IOB98	U24	L25	IOB148	AD16	AD22	IOB198	V1	AE9	IOB248		R3			
IOB49	B20	B17	IOB99	U23	L24	IOB149	AC16	AE22	IOB199	V2	AD9	IOB249		R4			
IOB50	C20	C17	IOB100	V26	L23	IOB150	AF15	AF21	IOB200	V3	AC9	IOB250		P1			

256 BGA PACKAGE



Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD256 (MO-151(B)/BAL-2)[1] Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3	0.15	0.45	seating plane clearance
D, E	27.00 BASIC		body size
D1, E1	24.13 BASIC		ball footprint
M	20 x 20		ball matrix size
N	256		total ball count
MR	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	14.8	15.2	encapsulation area
S	0.635 BASIC		solder ball placement

Note:

1. *BGD is Vantis' internal abbreviation for a wirebonded, plastic, cavity-down ball grid array that has been thermally enhanced with a heat sink.*

256 BGA COMMON SIGNALS (VF1012, VF1020, VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	D2
	CLK0	B4
	CLK1	D19
	CLK2	V17
	CLK3	U3
JTAG Interface	TDI	D18
	TMS	D3
	TDO	V4
	TCLK	C4
Configuration, Dedicated	/PROGRAM	C17
	DONE	U18
	CCLK	W4
Configuration, Multiplexed	HDC	D20
	/LDC	E17
	/INIT	E18
	M0	E19
	M1	E20
	M2	T19
	/CSO	T18
	CS1	T17
	/RS	U20
	/WS	U19
	RDY/(/BUSY)	U2
	DOUT	U1
	D7	T4
	D6	T3
	D5	T2
	D4	E1
	D3	E2
	D2	E3
	D1	E4
	D0	D1
Power Pins	VCC (20)	B2, B3, B18, B19, C2, C3, C18, C19,D4, D17, U4, U17, V2, V3, V18, V19, W2, W3, W18, W19.
	GND (20)	A1, A2, A3, A18, A19, A20, B1, B20, C1, C20, V1, V20, W1, W20, Y1, Y2, Y3, Y18, Y19, Y20.

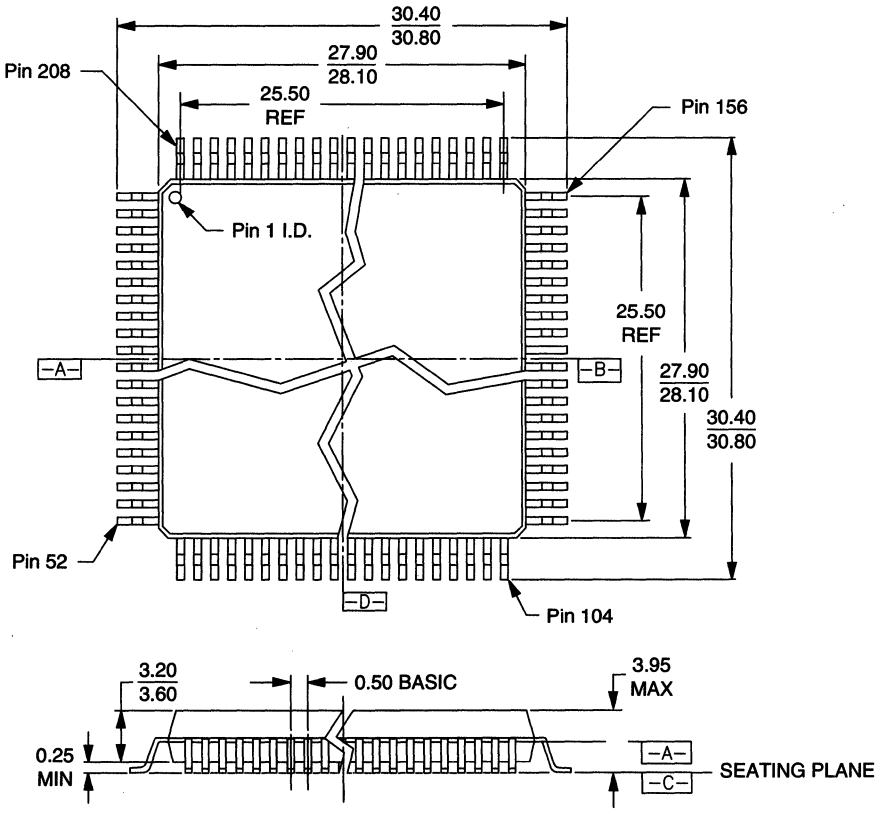
256 BGA INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB1	A4	A4	A4	A4	IOB51	G19	C16	A15	B14	IOB101	V12	R18		H20
IOB2	D5	D5	D5	D5	IOB52	G20	D16	B15		IOB102	W12	R17		J17
IOB3	C5	C5	C5	C5	IOB53	H17	A17	C15		IOB103	Y12	T20	N20	J18
IOB4	B5	B5	B5	B5	IOB54	H18	B17	D15		IOB104	V11	T19	N19	J19
IOB5	A5	A5	A5	A5	IOB55	H19	D20	A16	C14	IOB105	U11	T18	N18	J20
IOB6	D6	D6	D6	D6	IOB56	H20	E17	B16	D14	IOB106	W11	T17	N17	K20
IOB7	D7	C6	C6		IOB57	J17	E18	C16	A15	IOB107	Y11	U20	P20	K17
IOB8	C7	B6	B6		IOB58	K20	E19	D16		IOB108	W10	U19	P19	K18
IOB9	B7	A6	A6		IOB59	K17	E20	A17		IOB109	V10	W17	P18	K19
IOB10	A7	D7	D7	C6	IOB60	K18	F17	B17		IOB110	U10	Y17	P17	L20
IOB11	D8	C7	C7	B6	IOB61	K19	F18	D20	B15	IOB111	Y10	U16	R20	L19
IOB12	C8	B7	B7	A6	IOB62	L20	F19	E17	C15	IOB112	U9	V16	R19	L17
IOB13	B8	A7	A7		IOB63	L19	F20	E18	D15	IOB113	Y8	W16	R18	L18
IOB14	A8	D8	D8		IOB64	L17	G17	E19		IOB114	W8	Y16	R17	M20
IOB15	D9	C8	C8		IOB65	L18	G18	E20		IOB115	V8	U15	T20	M19
IOB16	A10	B8	B8	D7	IOB66	M20	G19	F17		IOB116	U8	V15	T19	M18
IOB17	D10	A8	A8	C7	IOB67	M19	G20	F18	A16	IOB117	Y7	W15	T18	M17
IOB18	C10	D9	D9	B7	IOB68	M18	H17	F19	B16	IOB118	W7	Y15	T17	N20
IOB19	B10	C9	C9		IOB69	M17	H18	F20	C16	IOB119	V7	U14	U20	N19
IOB20	A11	B9	B9		IOB70	N17	H19	G17	D16	IOB120	U7	V14	U19	N18
IOB21	B11	A9	A9		IOB71	P20	H20	G18	A17	IOB121	U6	W14	W17	N17
IOB22	D11	A10	A10	A7	IOB72	P19	J17	G19	B17	IOB122	Y5	Y14	Y17	P20
IOB23	C11	D10	D10	D8	IOB73	P18	J18	G20	D20	IOB123	W5	U13	U16	P19
IOB24	A12	C10	C10	C8	IOB74	P17	J19	H17	E17	IOB124	V5		V16	
IOB25	B12	B10	B10		IOB75	R20	J20	H18	E18	IOB125	U5		W16	
IOB26	C12	A11	A11		IOB76	R19	K20	H19	E19	IOB126	Y4		Y16	
IOB27	D12	B11	B11		IOB77	R18	K17	H20	E20	IOB127	U2	V13	U15	P18
IOB28	D13	D11		B8	IOB78	R17	K18	J17	F17	IOB128	U1	W13	V15	P17
IOB29	A14	C11		A8	IOB79	T20	K19	J18		IOB129	T4	Y13	W15	R20
IOB30	B14	A12		D9	IOB80	T19	L20	J19		IOB130	T3	U12	Y15	
IOB31	C14	B12	D11	C9	IOB81	T18	L19	J20		IOB131	T2	V12	U14	
IOB32	D14	C12	C11	B9	IOB82	T17	L17	K20	F18	IOB132	T1	W12	V14	
IOB33	A15	D12	A12	A9	IOB83	U20	L18	K17	F19	IOB133	R4	Y12	W14	R19
IOB34	B15	A13	B12	A10	IOB84	U19	M20	K18	F20	IOB134	R3	V11	Y14	R18
IOB35	C15	B13	C12	D10	IOB85	W17	M19	K19		IOB135	R2	U11	U13	R17
IOB36	D15	C13	D12	C10	IOB86	Y17	M18	L20		IOB136	R1	W11	V13	
IOB37	A16			B10	IOB87	U16	M17	L19		IOB137	P4	Y11	W13	
IOB38	B16			A11	IOB88	V16	N20		G17	IOB138	P3	W10	Y13	
IOB39	C16			B11	IOB89	W16	N19		G18	IOB139	P2	V10		T20
IOB40	D16	D13		D11	IOB90	Y16	N18		G19	IOB140	P1	U10		T19
IOB41	A17	A14		C11	IOB91	U15		L17		IOB141	N4	Y10		T18
IOB42	B17	B14		A12	IOB92	V15		L18		IOB142	M4	Y9		T17
IOB43	D20	C14	A13	B12	IOB93	W15		M20		IOB143	M3	W9		U20
IOB44	E17	D14	B13	C12	IOB94	Y15	N17	M19	G20	IOB144	M2	V9		U19
IOB45	E18	A15	C13	D12	IOB95	U14	P20	M18	H17	IOB145	M1	U9	U12	W17
IOB46	E19	B15	D13	A13	IOB96	V14	P19	M17	H18	IOB146	L3	Y8	V12	Y17
IOB47	E20	C15	A14	B13	IOB97	W14	P18			IOB147	L4	W8	W12	U16
IOB48	F17	D15	B14	C13	IOB98	Y14	P17			IOB148	L2	V8	Y12	V16
IOB49	G17	A16	C14	D13	IOB99	U13	R20			IOB149	L1	U8	V11	W16
IOB50	G18	B16	D14	A14	IOB100	U12	R19		H19	IOB150	K2	Y7	U11	Y16

256 BGA INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB151	K3	W7			IOB201		H2		U7	IOB251				L1
IOB152	K4	V7			IOB202		H3			IOB252				K2
IOB153	K1	U7			IOB203		H4			IOB253				K3
IOB154	J4	Y6	W11	U15	IOB204		G1			IOB254				K4
IOB155	H1	W6	Y11	V15	IOB205		G2	M4	Y6	IOB255				K1
IOB156	H2	V6	W10	W15	IOB206		G3	M3	W6	IOB256				J1
IOB157	H3	U6	V10		IOB207		G4	M2	V6	IOB257				J2
IOB158	H4	Y5	U10		IOB208		F1	M1		IOB258				J3
IOB159	G1	W5	Y10		IOB209		F2	L3		IOB259				J4
IOB160	G2	V5	Y9	Y15	IOB210		F3	L4		IOB260				H1
IOB161	G3	U5	W9	U14	IOB211		F4		U6	IOB261				H2
IOB162	G4	Y4	V9	V14	IOB212		E1		Y5	IOB262				
IOB163	F4	U2	U9		IOB213		E2		W5	IOB263				
IOB164	E1	U1	Y8		IOB214		E3	L2	V5	IOB264				
IOB165	E2	T4	W8		IOB215		E4	L1	U5	IOB265				H3
IOB166	E3	T3	V8	W14	IOB216		D1	K2	Y4	IOB266				H4
IOB167	E4	T2	U8	Y14	IOB217			K3	U2	IOB267				G1
IOB168	D1	T1	Y7	U13	IOB218			K4	U1	IOB268				
IOB169		R4	W7	V13	IOB219			K1	T4	IOB269				
IOB170		R3	V7	W13	IOB220			J1	T3	IOB270				
IOB171		R2	U7	Y13	IOB221			J2	T2	IOB271				G2
IOB172		R1	Y6	U12	IOB222			J3	T1	IOB272				G3
IOB173		P4	W6	V12	IOB223			J4		IOB273				G4
IOB174		P3	V6	W12	IOB224			H1		IOB274				
IOB175		P2	U6	Y12	IOB225			H2		IOB275				
IOB176		P1	Y5	V11	IOB226			H3	R4	IOB276				
IOB177		N4	W5	U11	IOB227			H4	R3	IOB277				F1
IOB178			V5	W11	IOB228			G1	R2	IOB278				F2
IOB179			U5	Y11	IOB229			G2		IOB279				F3
IOB180			Y4	W10	IOB230			G3		IOB280				
IOB181		N3	U2	V10	IOB231			G4		IOB281				
IOB182		N2	U1	U10	IOB232			F1	R1	IOB282				
IOB183		N1	T4	Y10	IOB233			F2	P4	IOB283				F4
IOB184		M4	T3	Y9	IOB234			F3	P3	IOB284				E1
IOB185		M3	T2	W9	IOB235			F4		IOB285				E2
IOB186		M2	T1	V9	IOB236			E1		IOB286				E3
IOB187		M1	R4	U9	IOB237			E2		IOB287				E4
IOB188		L3	R3	Y8	IOB238			E3	P2	IOB288				D1
IOB189		L4	R2	W8	IOB239			E4	P1					
IOB190		L2	R1		IOB240			D1	N4					
IOB191		L1	P4		IOB241				N3					
IOB192		K2	P3		IOB242				N2					
IOB193		K3	P2	V8	IOB243				N1					
IOB194		K4	P1	U8	IOB244				M4					
IOB195		K1	N4	Y7	IOB245				M3					
IOB196		J1	N3		IOB246				M2					
IOB197		J2	N2		IOB247				M1					
IOB198		J3	N1		IOB248				L3					
IOB199		J4		W7	IOB249				L4					
IOB200		H1		V7	IOB250				L2					

208 PQFP PACKAGE



16-038-PQR-1_AH
PRH208
EC95
8-13-97 lv

208 PQFP Common Signals (VF1012, VF1020, VF1025, VF1036)

Group	Signal	Pin
Clock Inputs	SET/RESET	207
	CLK0	2
	CLK1	54
	CLK2	105
	CLK3	157
JTAG Interface	TDI	53
	TMS	208
	TDO	156
	TCLK	1
Configuration, Dedicated	/PROGRAM	52
	DONE	104
	CCLK	155
Configuration, Multiplexed	HDC	55
	/LDC	56
	/INIT	57
	M0	58
	M1	59
	M2	99
	/CSO	100
	CS1	101
	/RS	102
	/WS	103
	RDY/(/BUSY)	158
	DOUT	159
	D7	160
	D6	161
	D5	162
	D4	202
	D3	203
	D2	204
	D1	205
	D0	206
Power Pins	VCC (16)	8, 112, 20, 125, 32, 137, 45, 149, 60, 164, 72, 177, 84, 189, 97, 201
	GND (16)	9, 21, 33, 46, 61, 73, 85, 98, 111, 124, 136, 148, 163, 176, 188, 200

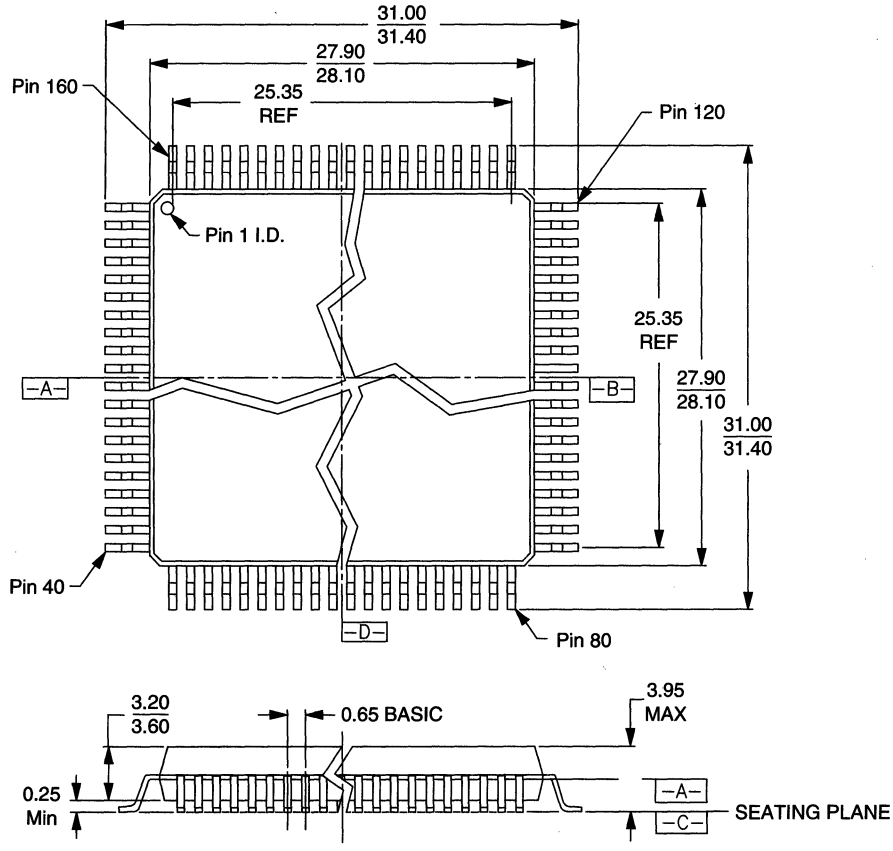
256 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB1	3	3	3	3	IOB51	65	48	40	37	IOB101	126	94		75
IOB2	4	4	4	4	IOB52	66	49	41		IOB102	127	95		76
IOB3	5	5	5	5	IOB53	67	50	42		IOB103	128	96	82	
IOB4	6	6	6	6	IOB54	68	51	43		IOB104	129	99	83	
IOB5	7	7	7	7	IOB55	69	55	44	38	IOB105	130	100	86	
IOB6	10	10	10	10	IOB56	70	56	47	39	IOB106	131	101	87	77
IOB7	11	11	11		IOB57	71	57	48	40	IOB107	132	102	88	78
IOB8	12	12	12		IOB58		58	49		IOB108	133	103	89	
IOB9	13	13	13		IOB59	74	59	50		IOB109	134	106	90	
IOB10	14	14	14	11	IOB60	75	62	51		IOB110	135	107	91	
IOB11	15	15	15	12	IOB61	76	63	55	41	IOB111		108	92	
IOB12	16	16	16	13	IOB62	77	64	56	42	IOB112	138	109	93	79
IOB13	17	17	17		IOB63	78	65	57	43	IOB113	139	110	94	80
IOB14	18	18	18		IOB64	79	66	58		IOB114	140	113	95	81
IOB15	19	19	19		IOB65	80	67	59		IOB115	141	114	96	
IOB16				14	IOB66	81	68	62		IOB116	142	115	99	
IOB17	22	22	22	15	IOB67	82	69	63	44	IOB117	143	116	100	
IOB18	23	23	23	16	IOB68	83	70	64	47	IOB118	144	117	101	82
IOB19	24				IOB69	86	71	65	48	IOB119	145	118	102	83
IOB20	25				IOB70	87		66	49	IOB120	146	119	103	86
IOB21	26				IOB71	88	74	67	50	IOB121	147	120	106	87
IOB22	27			17	IOB72	89	75	68	51	IOB122	150	121	107	88
IOB23	28			18	IOB73	90		69	55	IOB123	151	122	108	89
IOB24	29			19	IOB74	91		70	56	IOB124	152		109	
IOB25	30	24	24		IOB75	92		71	57	IOB125	153		110	
IOB26	31	25	25		IOB76	93			58	IOB126	154		113	
IOB27	34	26	26		IOB77	94		74	59	IOB127	158	123	114	90
IOB28	35	27		22	IOB78	95		75	62	IOB128	159	126	115	91
IOB29	36	28		23	IOB79	96	76			IOB129	160	127	116	92
IOB30	37	29		24	IOB80	99	77			IOB130	161		117	
IOB31	38				IOB81	100	78			IOB131	162		118	
IOB32	39				IOB82	101	79		63	IOB132	165		119	
IOB33	40				IOB83	102	80		64	IOB133	166	128	120	93
IOB34	41	30	27	25	IOB84	103	81		65	IOB134	167	129	121	94
IOB35	42	31	28	26	IOB85	106		76		IOB135	168	130	122	95
IOB36	43	34	29		IOB86	107		77		IOB136	169	131	123	
IOB37	44				IOB87	108		78		IOB137	170	132	126	
IOB38	47				IOB88	109	82		66	IOB138	171	133	127	
IOB39	48				IOB89	110	83		67	IOB139	172			96
IOB40	49	35		27	IOB90	113	86		68	IOB140	173			99
IOB41	50	36		28	IOB91	114				IOB141	174			100
IOB42	51	37		29	IOB92	115				IOB142	175			101
IOB43	55	38	30		IOB93	116				IOB143	178			102
IOB44	56	39	31		IOB94	117	87	79	69	IOB144	179			103
IOB45	57	40	34		IOB95	118	88	80	70	IOB145	180	134	128	106
IOB46	58	41	35	30	IOB96	119	89	81	71	IOB146	181	135	129	107
IOB47	59	42	36	31	IOB97	120	90			IOB147	182		130	108
IOB48	62	43	37	34	IOB98	121	91			IOB148	183	138		109
IOB49	63	44	38	35	IOB99	122	92			IOB149	184	139		110
IOB50	64	47	39	36	IOB100	123	93		74	IOB150	185	140		113

256 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020, VF1025, VF1036)

Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036	Signal	VF1012	VF1020	VF1025	VF1036
IOB151	186	141			IOB201				143	IOB251				
IOB152	187	142			IOB202		190			IOB252				
IOB153		143			IOB203		191			IOB253				
IOB154	190	144	131	114	IOB204		192			IOB254				183
IOB155	191	145	132	115	IOB205		193	180	144	IOB255				184
IOB156	192	146	133	116	IOB206		194	181	145	IOB256				
IOB157	193	147			IOB207		195	182	146	IOB257				
IOB158	194	150			IOB208		196			IOB258				
IOB159	195	151			IOB209		197			IOB259				185
IOB160	196	152		117	IOB210		198			IOB260				186
IOB161	197	153		118	IOB211		199		147	IOB261				187
IOB162	198	154		119	IOB212		202		150	IOB262				
IOB163	199	158	134		IOB213		203		151	IOB263				
IOB164	202	159	135		IOB214		204	183	152	IOB264				
IOB165	203	160			IOB215		205	184	153	IOB265				190
IOB166	204	161	138	120	IOB216		206	185	154	IOB266				191
IOB167	205	162	139	121	IOB217				158	IOB267				192
IOB168	206	165	140	122	IOB218				159	IOB268				
IOB169		166	141	123	IOB219				160	IOB269				
IOB170		167	142	126	IOB220				161	IOB270				
IOB171		168	143	127	IOB221				162	IOB271				193
IOB172		169	144		IOB222				165	IOB272				194
IOB173		170	145		IOB223			186		IOB273				195
IOB174		171	146		IOB224			187		IOB274				
IOB175		172	147	128	IOB225					IOB275				
IOB176		173	150	129	IOB226			190	166	IOB276				
IOB177		174	151	130	IOB227			191	167	IOB277				196
IOB178			152		IOB228			192	168	IOB278				197
IOB179			153		IOB229			193		IOB279				198
IOB180			154		IOB230			194		IOB280				
IOB181		175	158		IOB231			195		IOB281				
IOB182		178	159	131	IOB232			196	169	IOB282				
IOB183		179	160	132	IOB233			197	170	IOB283				199
IOB184			161		IOB234			198	171	IOB284				202
IOB185			162		IOB235			199		IOB285				203
IOB186			165		IOB236			202		IOB286				204
IOB187		180	166	133	IOB237			203		IOB287				205
IOB188		181	167	134	IOB238			204	172	IOB288				206
IOB189		182	168	135	IOB239			205	173					
IOB190		183	169		IOB240			206	174					
IOB191		184	170		IOB241				175					
IOB192		185	171		IOB242				178					
IOB193			172	138	IOB243				179					
IOB194			173	139	IOB244									
IOB195			174	140	IOB245									
IOB196			175		IOB246									
IOB197			178		IOB247				180					
IOB198			179		IOB248				181					
IOB199		186		141	IOB249				182					
IOB200		187		142	IOB250									

160 PQFP PACKAGE



16-038-PQR-1
PQR160
12-22-95 lv

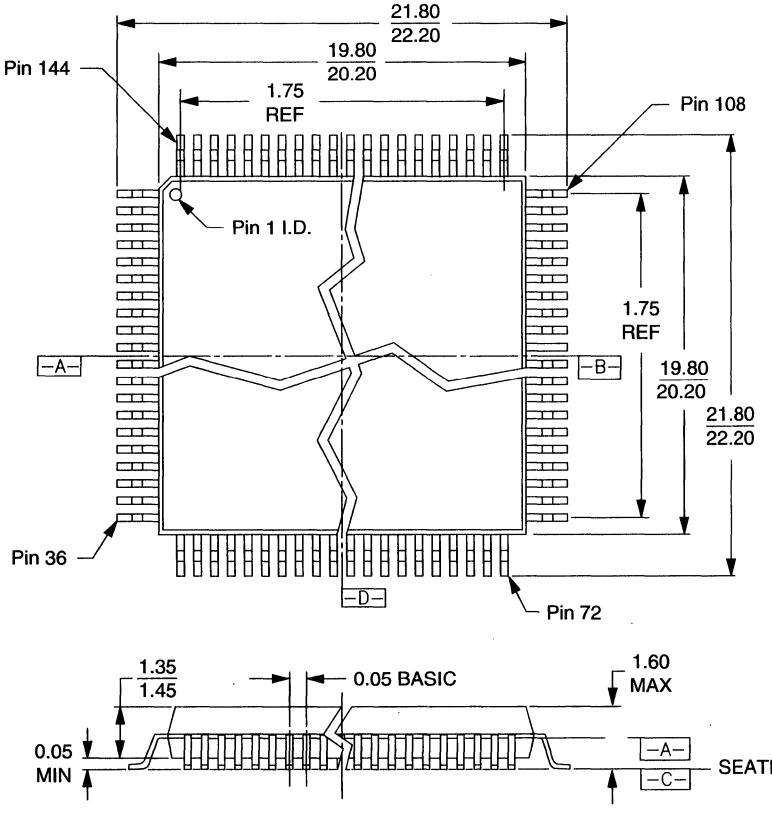
160 PQFP Common Signals (VF1012, VF1020)

Group	Signal	Pin
Clock Inputs	SET/RESET	159
	CLK0	2
	CLK1	42
	CLK2	81
	CLK3	121
JTAG Interface	TDI	41
	TMS	160
	TDO	120
	TCLK	1
Configuration, Dedicated	/PROGRAM	40
	DONE	80
	CCLK	119
Configuration, Multiplexed	HDC	43
	/LDC	44
	/INIT	45
	M0	46
	M1	47
	M2	75
	/CSO	76
	CS1	77
	/RS	78
	/WS	79
	RDY/(/BUSY)	122
	DOUT	123
	D7	124
	D6	125
	D5	126
	D4	154
	D3	155
	D2	156
	D1	157
	D0	158
Power Pins	VCC (12)	8, 20, 33, 48, 60, 73, 88, 101, 113, 128, 141, 153
	GND (12)	9, 21, 34, 49, 61, 74, 87, 100, 112, 127, 140, 152

160 PQFP INPUT/OUTPUT BLOCKS (VF1012, VF1020)

Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020	Signal	VF1012	VF1020
IOB1	3	3	IOB51	53	36	IOB101			IOB151	138	105	IOB201		
IOB2	4	4	IOB52	54	37	IOB102			IOB152	139	106	IOB202		142
IOB3	5	5	IOB53	55	38	IOB103	95	72	IOB153		107	IOB203		143
IOB4	6	6	IOB54	56	39	IOB104	96	75	IOB154	142	108	IOB204		144
IOB5	7	7	IOB55	57	43	IOB105	97	76	IOB155	143	109	IOB205		145
IOB6	10	10	IOB56	58	44	IOB106		77	IOB156	144	110	IOB206		146
IOB7	11	11	IOB57	59	45	IOB107		78	IOB157	145	111	IOB207		147
IOB8	12	12	IOB58		46	IOB108		79	IOB158	146	114	IOB208		148
IOB9	13	13	IOB59	62	47	IOB109	98	82	IOB159	147	115	IOB209		149
IOB10	14	14	IOB60	63	50	IOB110	99	83	IOB160	148	116	IOB210		150
IOB11	15	15	IOB61		51	IOB111		84	IOB161	149	117	IOB211		151
IOB12	16	16	IOB62		52	IOB112	102	85	IOB162	150	118	IOB212		154
IOB13	17	17	IOB63		53	IOB113	103	86	IOB163	151	122	IOB213		155
IOB14	18	18	IOB64	64	54	IOB114	104	89	IOB164	154	123	IOB214		156
IOB15	19	19	IOB65	65	55	IOB115	105		IOB165	155	124	IOB215		157
IOB16			IOB66	66	56	IOB116	106		IOB166	156	125	IOB216		158
IOB17	22	22	IOB67		57	IOB117	107		IOB167	157	126			
IOB18	23	23	IOB68		58	IOB118	108		IOB168	158	129			
IOB19			IOB69		59	IOB119	109	90	IOB169					
IOB20			IOB70	67		IOB120	110	91	IOB170					
IOB21			IOB71	68	62	IOB121	111		IOB171					
IOB22	24		IOB72	69	63	IOB122	114		IOB172					
IOB23	25		IOB73			IOB123	115		IOB173		130			
IOB24	26		IOB74			IOB124	116		IOB174		131			
IOB25		24	IOB75			IOB125	117		IOB175					
IOB26		25	IOB76	70		IOB126	118		IOB176					
IOB27		26	IOB77	71		IOB127	122	92	IOB177					
IOB28	27		IOB78			IOB128	123	93	IOB178					
IOB29	28		IOB79	72	64	IOB129	124	94	IOB179					
IOB30	29		IOB80	75	65	IOB130	125		IOB180					
IOB31			IOB81	76	66	IOB131	126		IOB181		132			
IOB32			IOB82	77		IOB132	129		IOB182		133			
IOB33			IOB83	78		IOB133			IOB183		134			
IOB34	30	27	IOB84	79		IOB134	130		IOB184					
IOB35	31	28	IOB85	82		IOB135	131		IOB185					
IOB36		29	IOB86	83		IOB136		95	IOB186					
IOB37	32		IOB87	84		IOB137		96	IOB187					
IOB38	35		IOB88	85	67	IOB138		97	IOB188					
IOB39	36		IOB89	86	68	IOB139	132		IOB189					
IOB40	37		IOB90	89	69	IOB140	133		IOB190		135			
IOB41	38		IOB91			IOB141	134		IOB191		136			
IOB42	39		IOB92	90		IOB142			IOB192		137			
IOB43	43	30	IOB93	91		IOB143			IOB193					
IOB44	44	31	IOB94			IOB144			IOB194					
IOB45	45		IOB95			IOB145	135	98	IOB195					
IOB46	46		IOB96			IOB146	136	99	IOB196					
IOB47	47		IOB97	92	70	IOB147	137		IOB197					
IOB48	50		IOB98	93	71	IOB148		102	IOB198					
IOB49	51	32	IOB99	94		IOB149		103	IOB199		138			
IOB50	52	35	IOB100			IOB150		104	IOB200		139			

144 TQFP PACKAGE



VF1ds-056

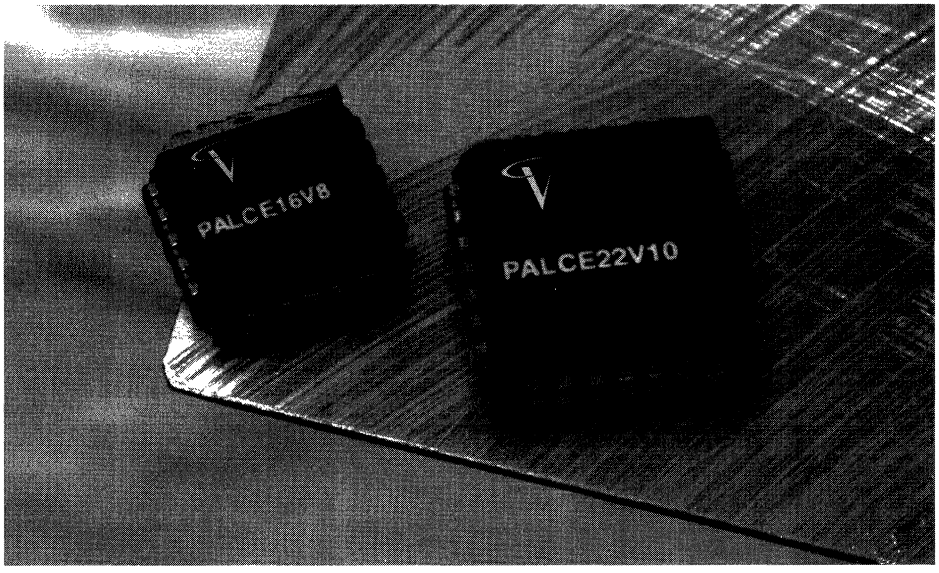
144 TQFP Signals (VF1012)

Group	Signal	Pin
Clock Inputs	SET/RESET	143
	CLK0	2
	CLK1	38
	CLK2	73
	CLK3	109
JTAG Interface	TDI	37
	TMS	144
	TDO	108
	TCLK	1
Configuration, Dedicated	PROGRAM	36
	DONE	72
	CCLK	107
Configuration, Multiplexed	HDC	39
	/LDC	40
	/INIT	41
	M0	42
	M1	43
	M2	67
	/CS0	68
	CS1	69
	/RS	70
	/WS	71
	RDY/(/BUSY)	110
	DOUT	111
	D7	112
	D6	113
	D5	114
	D4	138
	D3	139
	D2	140
	D1	141
	D0	142
Power Pins	VCC (12)	8, 17, 29, 44, 53, 65, 80, 92, 101, 116, 128, 137
	GND (12)	9, 18, 30, 45, 54, 66, 79, 91, 100, 115, 127, 136

144 TQFP INPUT/OUTPUT BLOCKS (VF1012)

Signal	VF1012	Signal	VF1012	Signal	VF1012	Signal	VF1012
IOB1	3	IOB43	39	IOB85	74	IOB127	110
IOB2	4	IOB44	40	IOB86	75	IOB128	111
IOB3	5	IOB45	41	IOB87	76	IOB129	112
IOB4	6	IOB46	42	IOB88	77	IOB130	113
IOB5	7	IOB47	43	IOB89	78	IOB131	114
IOB6	10	IOB48	46	IOB90	81	IOB132	117
IOB7		IOB49		IOB91		IOB133	
IOB8		IOB50		IOB92		IOB134	
IOB9		IOB51		IOB93	82	IOB135	118
IOB10	11	IOB52	47	IOB94		IOB136	
IOB11	12	IOB53	48	IOB95		IOB137	
IOB12	13	IOB54	49	IOB96		IOB138	
IOB13	14	IOB55	50	IOB97	83	IOB139	119
IOB14	15	IOB56	51	IOB98	84	IOB140	120
IOB15	16	IOB57	52	IOB99	85	IOB141	121
IOB16		IOB58		IOB100		IOB142	
IOB17	19	IOB59	55	IOB101		IOB143	
IOB18	20	IOB60	56	IOB102		IOB144	
IOB19		IOB61		IOB103	86	IOB145	122
IOB20		IOB62		IOB104	87	IOB146	123
IOB21		IOB63		IOB105	88	IOB147	124
IOB22	21	IOB64	57	IOB106		IOB148	
IOB23	22	IOB65	58	IOB107		IOB149	
IOB24	23	IOB66	59	IOB108		IOB150	
IOB25		IOB67		IOB109	89	IOB151	125
IOB26		IOB68		IOB110	90	IOB152	126
IOB27		IOB69		IOB111		IOB153	
IOB28	24	IOB70	60	IOB112	93	IOB154	129
IOB29	25	IOB71	61	IOB113	94	IOB155	130
IOB30	26	IOB72	62	IOB114	95	IOB156	131
IOB31		IOB73		IOB115	96	IOB157	132
IOB32		IOB74		IOB116	97	IOB158	133
IOB33		IOB75		IOB117	98	IOB159	134
IOB34	27	IOB76	63	IOB118		IOB160	
IOB35		IOB77		IOB119		IOB161	
IOB36		IOB78		IOB120		IOB162	
IOB37	28	IOB79	64	IOB121	99	IOB163	135
IOB38	31	IOB80	67	IOB122	102	IOB164	138
IOB39	32	IOB81	68	IOB123	103	IOB165	139
IOB40	33	IOB82	69	IOB124	104	IOB166	140
IOB41	34	IOB83	70	IOB125	105	IOB167	141
IOB42	35	IOB84	71	IOB126	106	IOB168	142

PAL Devices



VANTIS
BEYOND PERFORMANCE

PALCE16V8 and PALCE16V8Z Families

EE CMOS (Zero-Power) 20-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all 20-pin PAL® devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - 5-ns propagation delay for "-5" version
  - 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for the PAL16R8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Peripheral Component Interconnect (PCI) compliant**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support**
- **Fully tested for 100% programming and functional yields and high reliability**
- **5-ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 30-µA maximum standby current, the PALCE16V8Z allows battery-powered operation for an extended period.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

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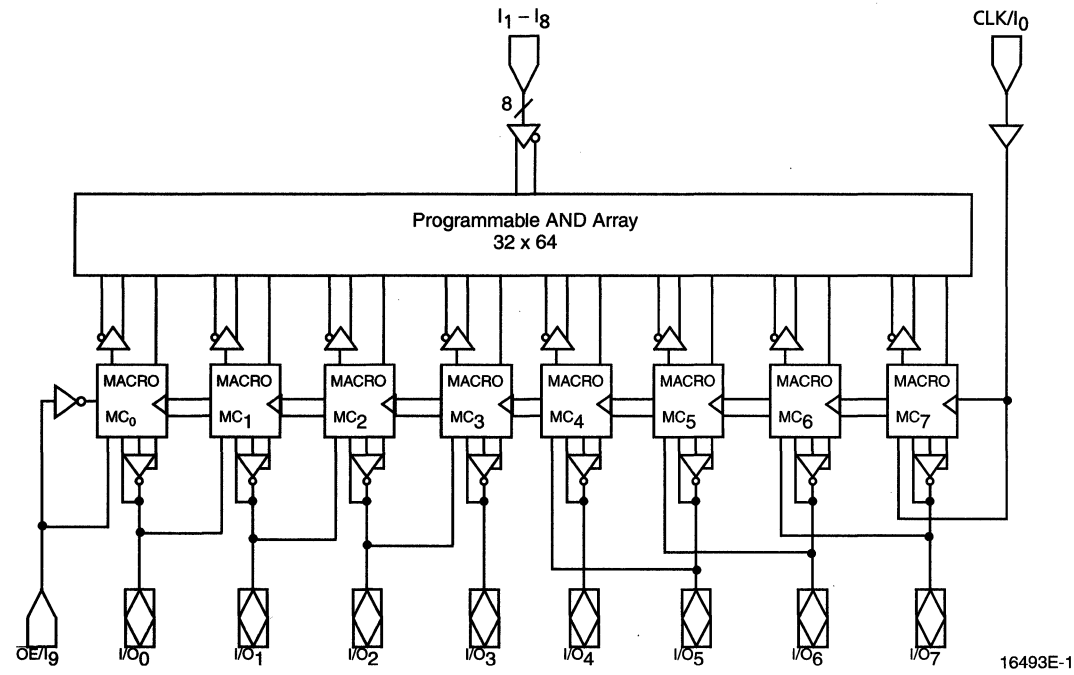
Amendment/**0** Issue Date: **November 1998**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

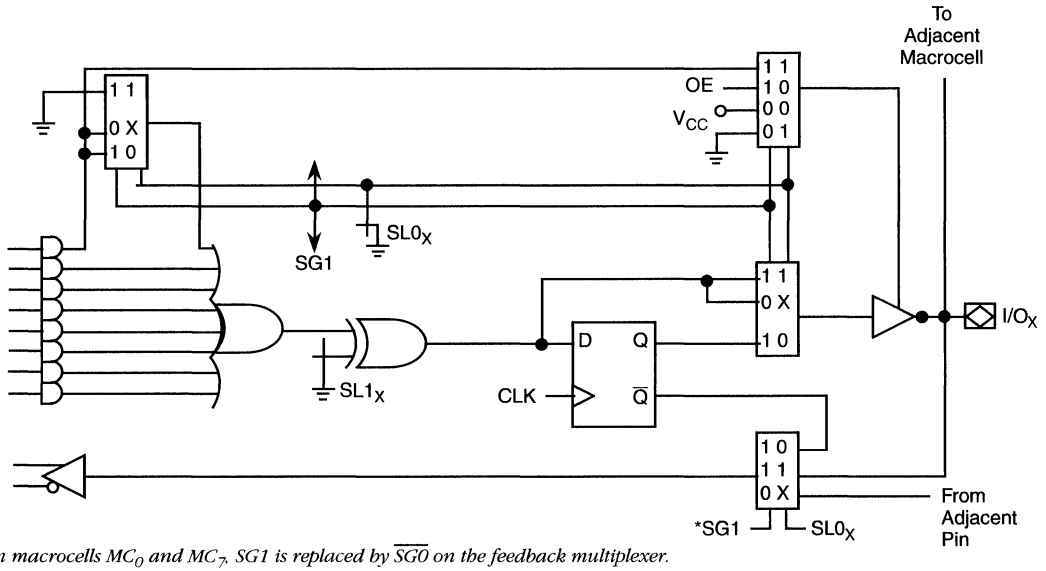
The PALCE16V8 is a universal PAL device. The PALCE16V8Z is the zero-power version of the PALCE16V8. It has all the architectural features of the PALCE16V8. In addition, the PALCE16V8Z has zero standby power and an unused product term disable feature for reduced power consumption. It has eight independently configurable macrocells (MC_0-MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state, and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file (JEDEC). This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them.

Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

16493E-2

Figure 1. PALCE16V8 Macrocell

CONFIGURATION OPTIONS

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces $\overline{SG1}$ on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_X$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_X$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_X$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 15 and 16. Pins 15 and 16 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_X$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_X$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_X$ = 1. The output buffer is disabled. Except for MC_0 and MC_7, the feedback signal is an adjacent I/O. For MC_0 and MC_7, the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

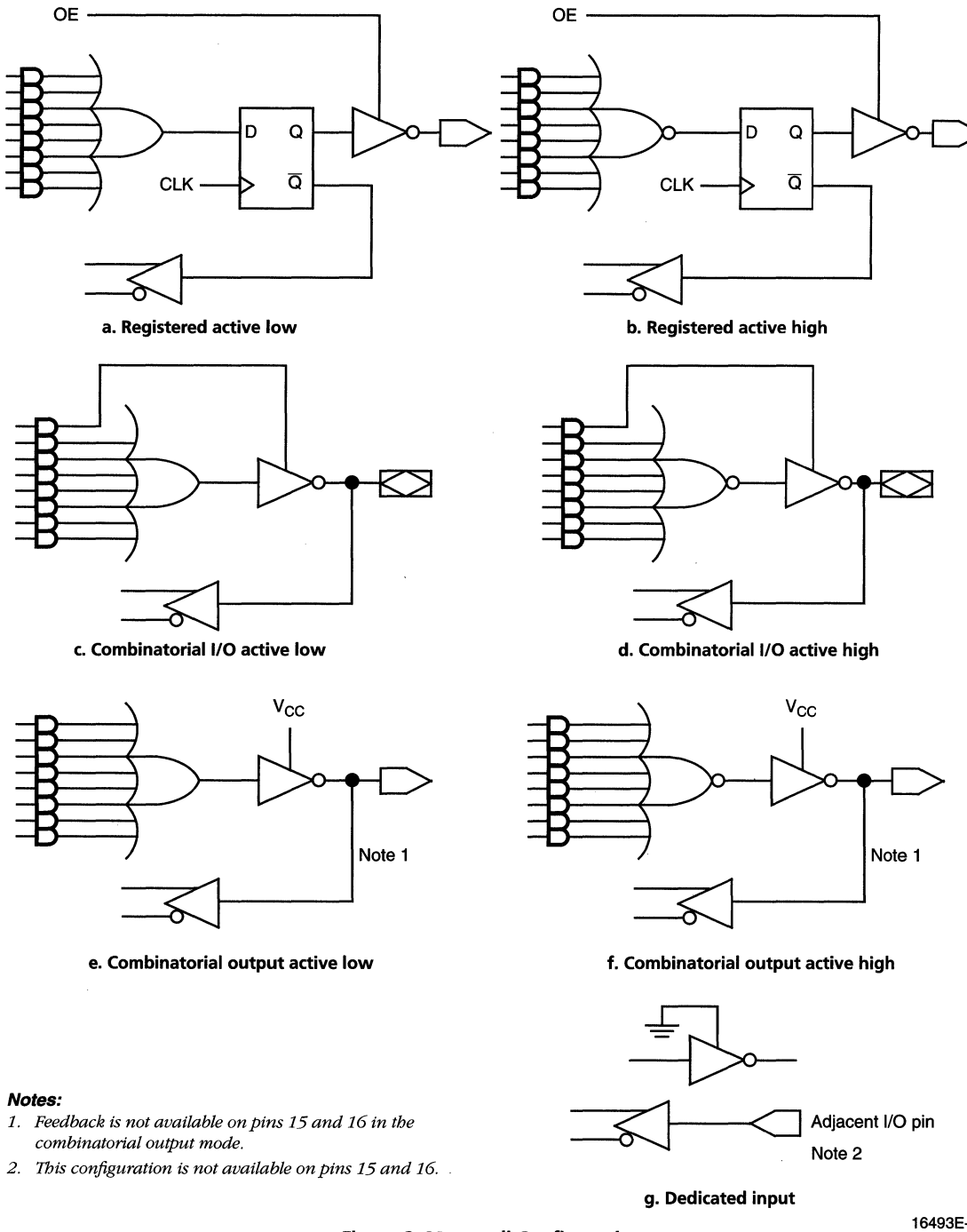
Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated	SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated
Device Uses Registers					Device Uses No Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4	1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
0	1	1	Combinatorial I/O	PAL16R6, 16R4	1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
					1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



16493E-2

Figure 2. Macrocell Configurations

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *This configuration is not available on pins 15 and 16.*

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE16V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE16V8 is fabricated with Vantis' advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

PCI Compliance

PALCE16V8 devices in the -5/-7/-10 speed grades are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE16V8's predictable timing ensures compliance with the PCI AC specifications independent of the design.

Zero-Standby Power Mode

The PALCE16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE16V8Z will go into standby mode, shutting down

most of its internal circuitry. The current will go to almost zero (I_{CC} < 15 µA). The outputs will maintain the states held before the device went into the standby mode. There is no speed penalty associated with coming out of standby mode.

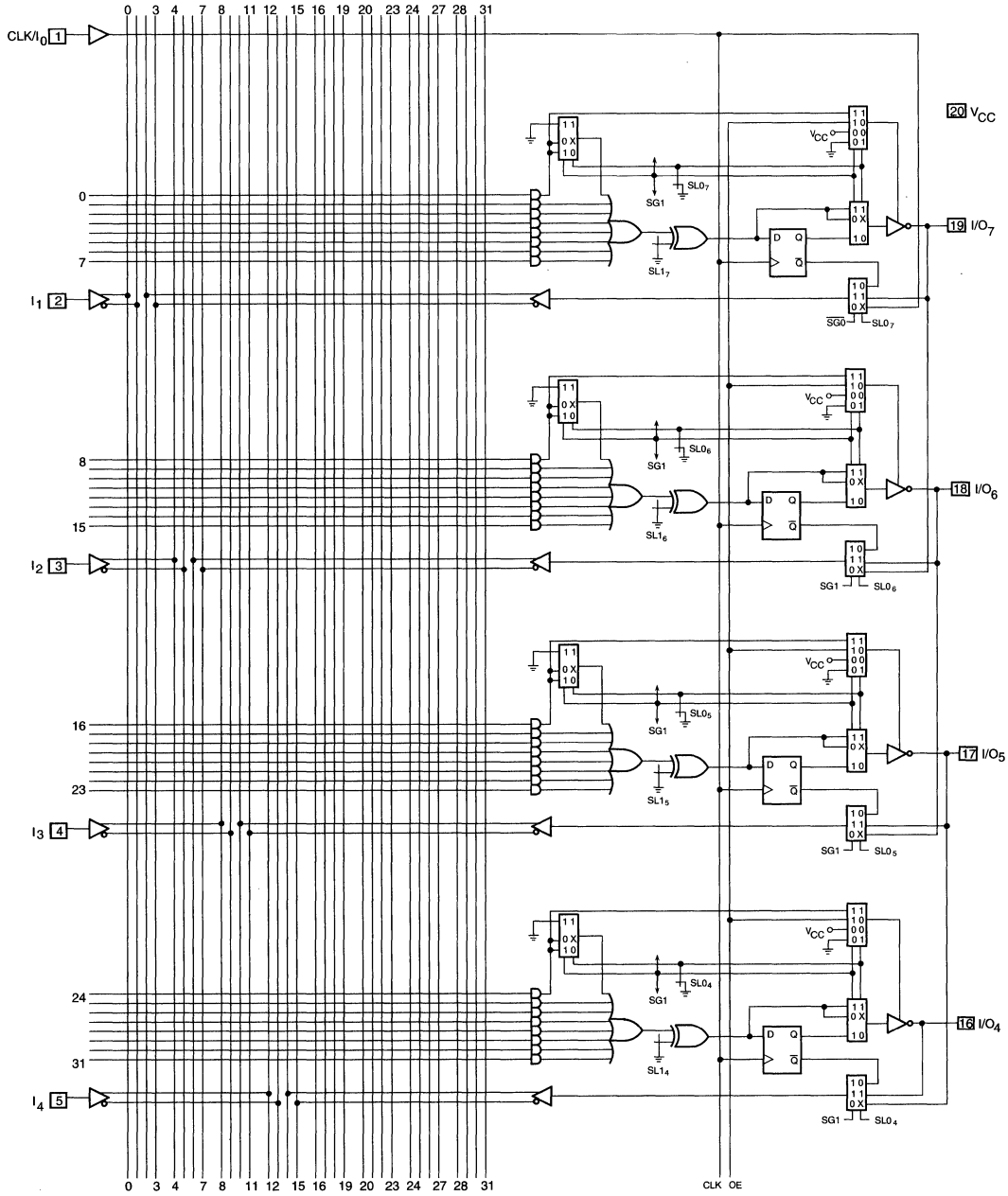
When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This saving is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE16V8Z, any product terms that are not used are disabled. Power is cut off from the product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graph, product-term disabling results in considerable power savings. This saving is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in a separate document entitled, *Minimizing Power Consumption with Zero-Power PLDs*.

LOGIC DIAGRAM



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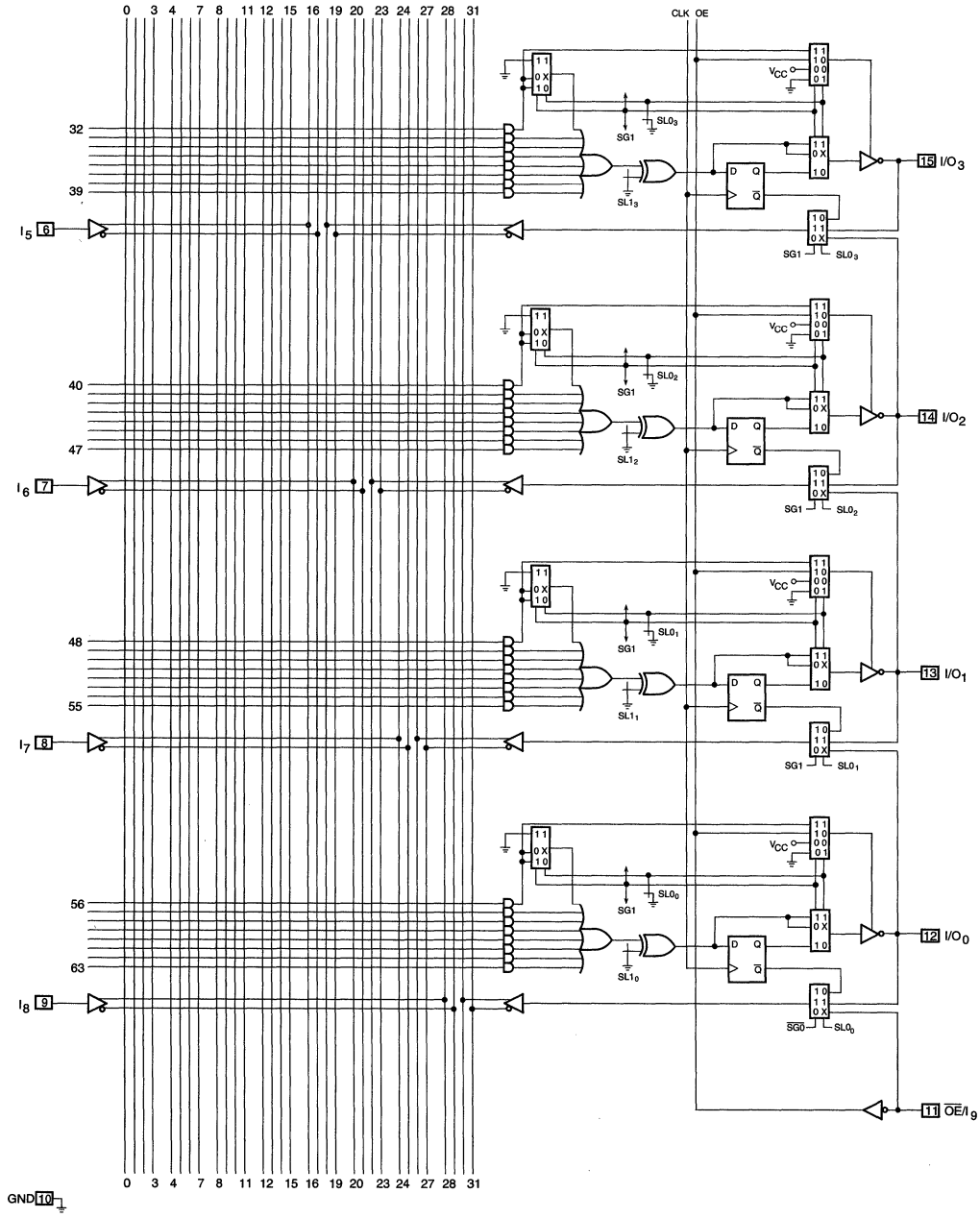
LOGIC DIAGRAM (CONTINUED)



16493E-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Static)	Supply Current for -5	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA
I_{CC} (Dynamic)	Supply Current for -7	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-5		-7		Unit
				Min [2]	Max	Min [2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output			1	5	3	7.5	ns
t_S	Setup Time from Input or Feedback to Clock			3		5		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			1	4	1	5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1		1	ns
t_{WL}	Clock Width	LOW		3		4		ns
t_{WH}		HIGH		3		4		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	142.8		100		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 5)	166		125		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	166		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	1	6	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	3	9	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	3	9	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
3. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to + 7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Temperature (T_A) Operating
in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Commercial Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		115	mA
	Industrial Supply Current			130	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-10		Unit
				Min [2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 4)	71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-10		Unit
				Min [2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 4)	71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to + 7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Temperature (T_A) Operating
in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC} (Dynamic)	Commercial Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	
	Industrial Supply Current		H		130	mA
			Q		65	

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		20		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		13		15		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				10		11		12	ns
t_{WL}	Clock Width	LOW		8		10		12		ns
t_{WH}		HIGH		8		10		12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S+t_{CO})$	45.5		41.6		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 3)	50		45.4		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		50.0		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		18		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		18		20	ns

Notes:

1. See "Switching Test Circuit" for test conditions.

2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

3. t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to + 7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		30	µA
	Supply Current (Dynamic)		f = 15 MHz		75	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-12		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				12	ns
t_S	Setup Time from Input or Feedback to Clock			8		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S+t_{CO})$	62.5		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$	77		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				8	ns
t_{EA}	Input to Output Enable Using Product Term Control				13	ns
t_{ER}	Input to Output Disable Using Product Term Control				13	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in standby mode.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to + 7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		15	µA
	Supply Current (Dynamic)		f = 25 MHz		75	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-15		Unit
				Min [2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S+t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$	58.8		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in standby mode.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to + 7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Temperature (T_A) Operating
in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		15	µA
	Supply Current (Dynamic)		f = 25 MHz		90	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25 °C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

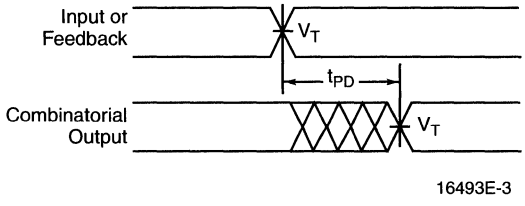
SWITCHING CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES[1]

Parameter Symbol	Parameter Description			-25		Unit
				Min [2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_S+t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$	50		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

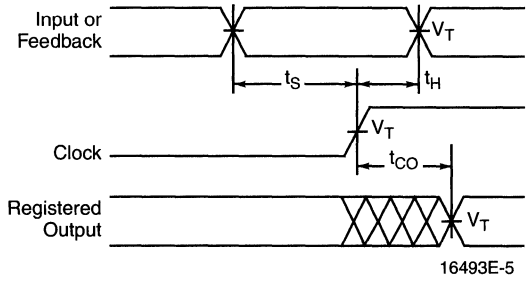
Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in standby mode.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 2 ns faster.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

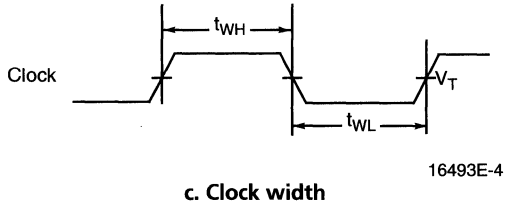
SWITCHING WAVEFORMS



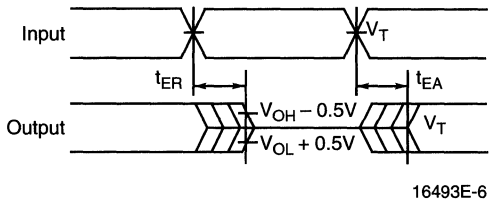
a. Combinatorial output



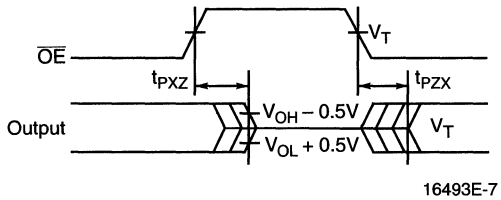
b. Registered output



c. Clock width



d. Input to output disable/enable

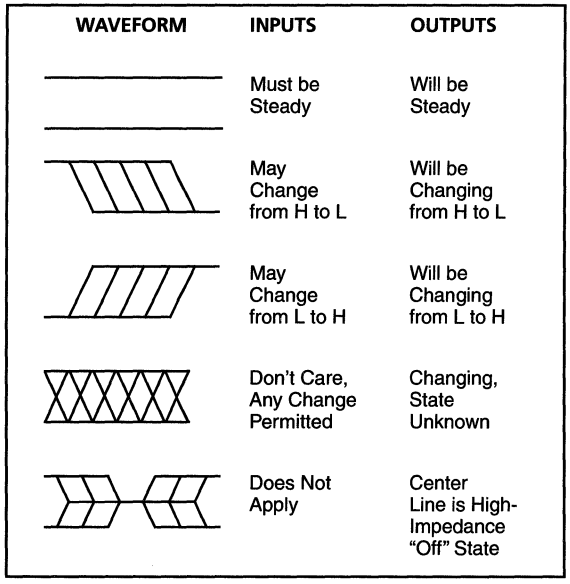


e. $\overline{OE}$ to output disable/enable

Notes:

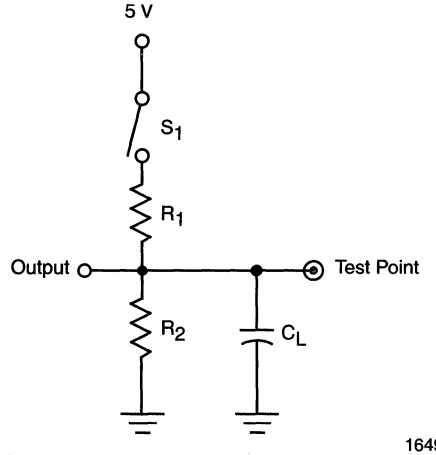
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT

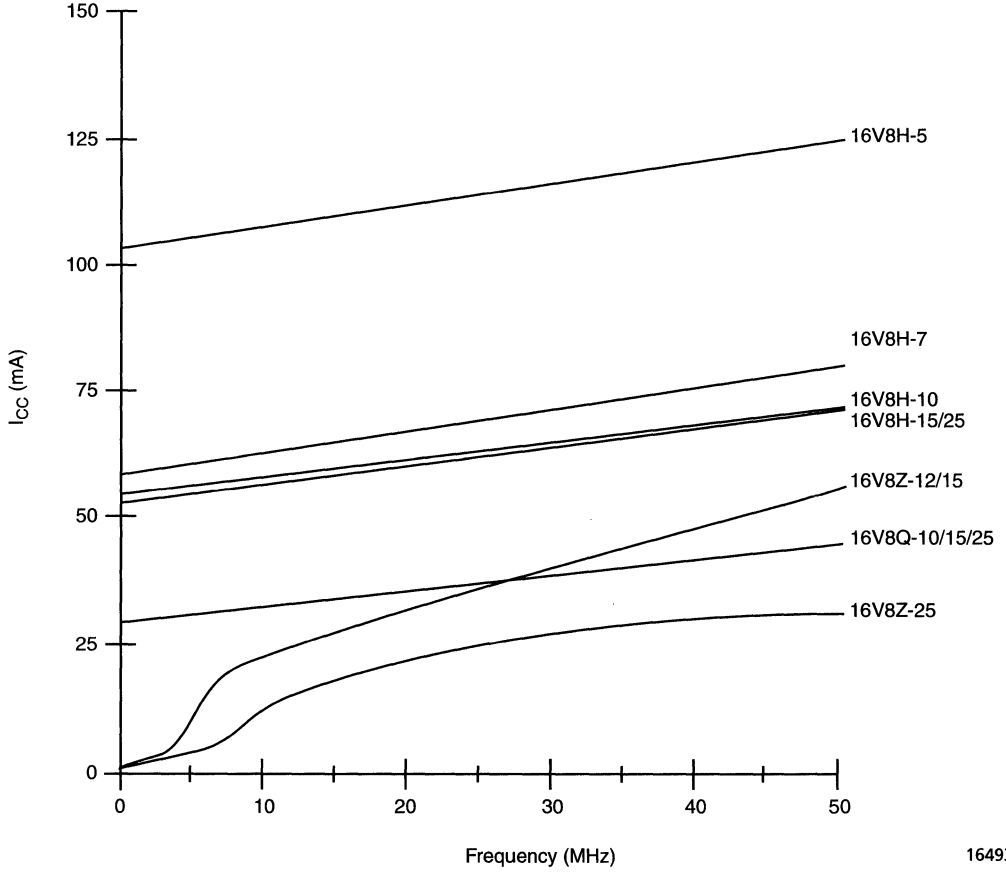


16493E-8

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open				1.5 V
	Z → L: Closed				
t_{ER}	H → Z: Open	5 pF		H-5: 200 Ω	H → Z: V_{OH} – 0.5 V
	L → Z: Closed				L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

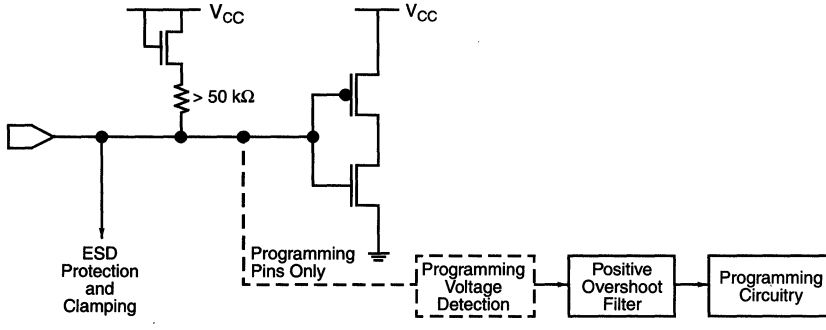
The PALCE16V8 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

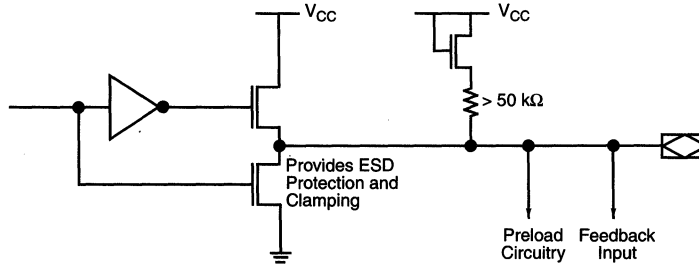
ROBUSTNESS FEATURES

PALCE16V8X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions. Selected /4 devices are also being retrofitted with these robustness features.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR PALCE16V8



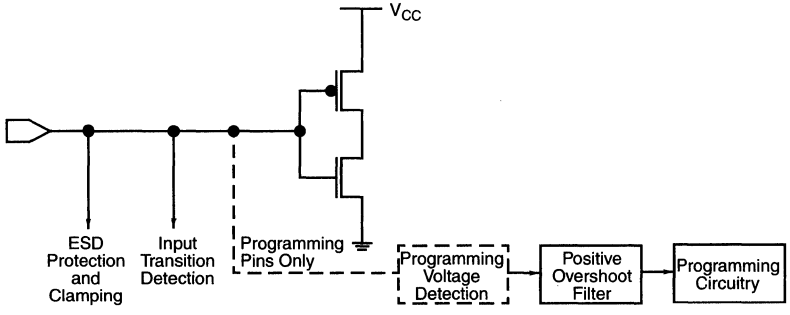
Typical Input



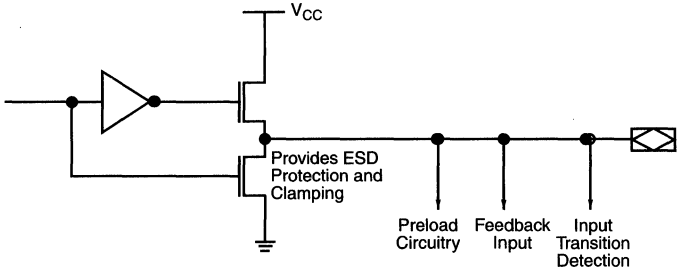
16493E-10

Typical Output

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR PALCE16V8Z



Typical Input



16493E-11

Typical Output

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			

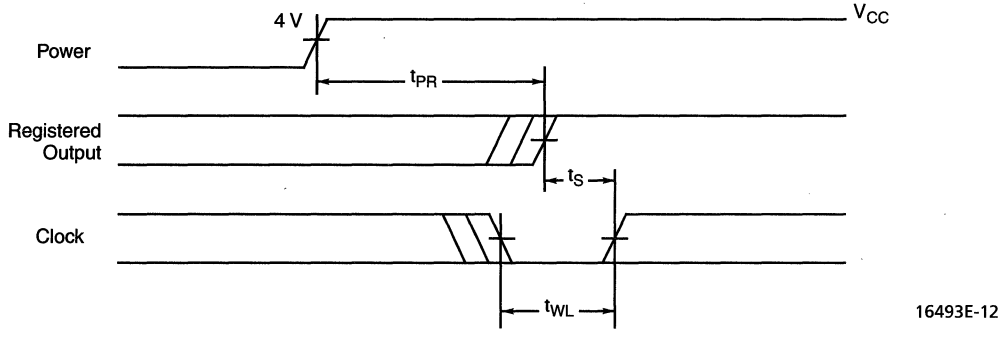


Figure 3. Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			PDID	PLCC	
θ_{jc}	Thermal impedance, junction to case		25	22	°C/W
θ_{ja}	Thermal impedance, junction to ambient		71	64	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	61	55	°C/W
		400 lfpm air	55	51	°C/W
		600 lfpm air	51	47	°C/W
		800 lfpm air	47	45	°C/W

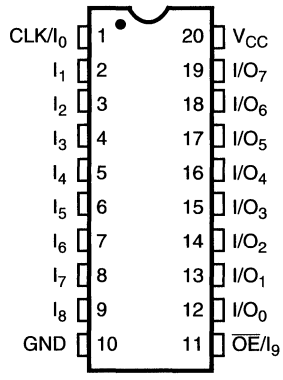
Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

CONNECTION DIAGRAMS

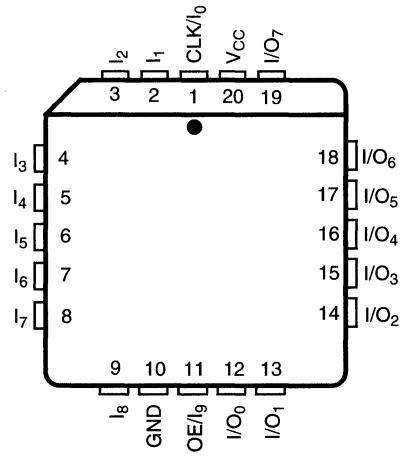
Top View

DIP/SOIC



16493E-9

PLCC



16493E-10

Note:
Pin 1 is marked for orientation.

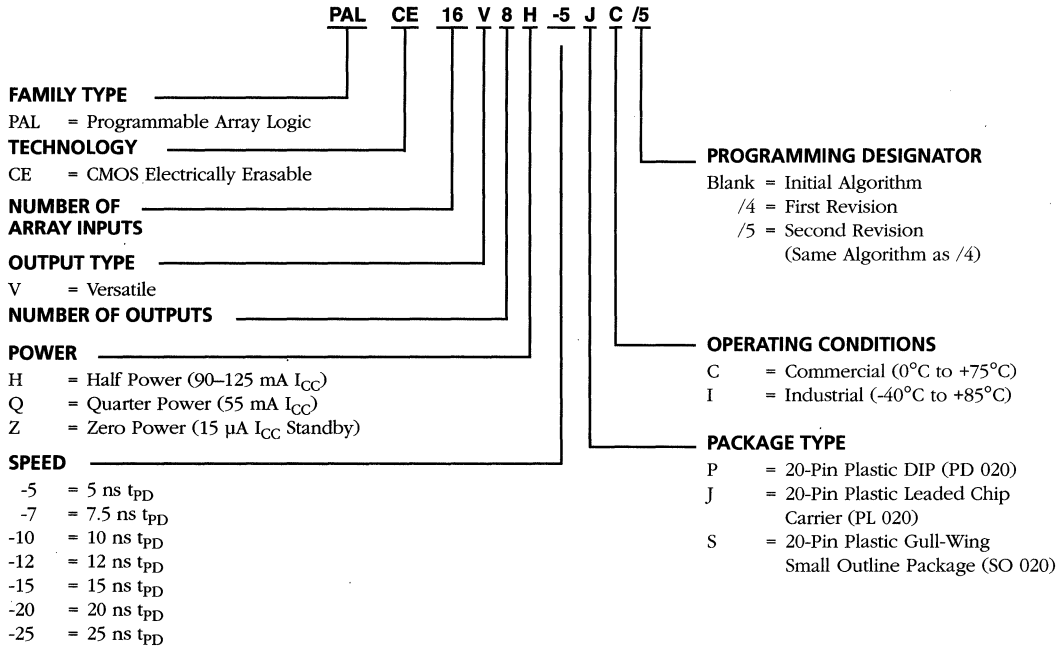
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-5	JC	/5
PALCE16V8H-7	PC, JC, SC	
PALCE16V8H-10	PC, JC, SC, PI, JI	/4
PALCE16V8Q-10	JC	/5
PALCE16V8H-15	PC, JC, SC	/4
PALCE16V8Q-15	PC, JC	
PALCE16V8Q-20	PI, JI	
PALCE16V8H-25	PC, JC, SC, PI, JI	
PALCE16V8Q-25	PC, JC, PI, JI	
PALCE16V8Z-12	PI, JI	
PALCE16V8Z-15		
PALCE16V8Z-25	PC, JC, SC, PI, JI, SI	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

VANTIS

BEYOND PERFORMANCE

FINAL COM'L:-10 IND:-20

PALLV16V8-10 & PALLV16V8Z-20

Low Voltage, Zero Power 20-Pin EE CMOS Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  — V_{CC} = +3.0 V to +3.6 V
- **Pin and function compatible with all 20-pin PAL® devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series**
- **Designed to interface with both 3.3-V and 5-V logic**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALLV16V8 is an advanced PAL device built with low-voltage, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALLV16V8 will directly replace the PAL16R8, with the exception of the PAL16C1.

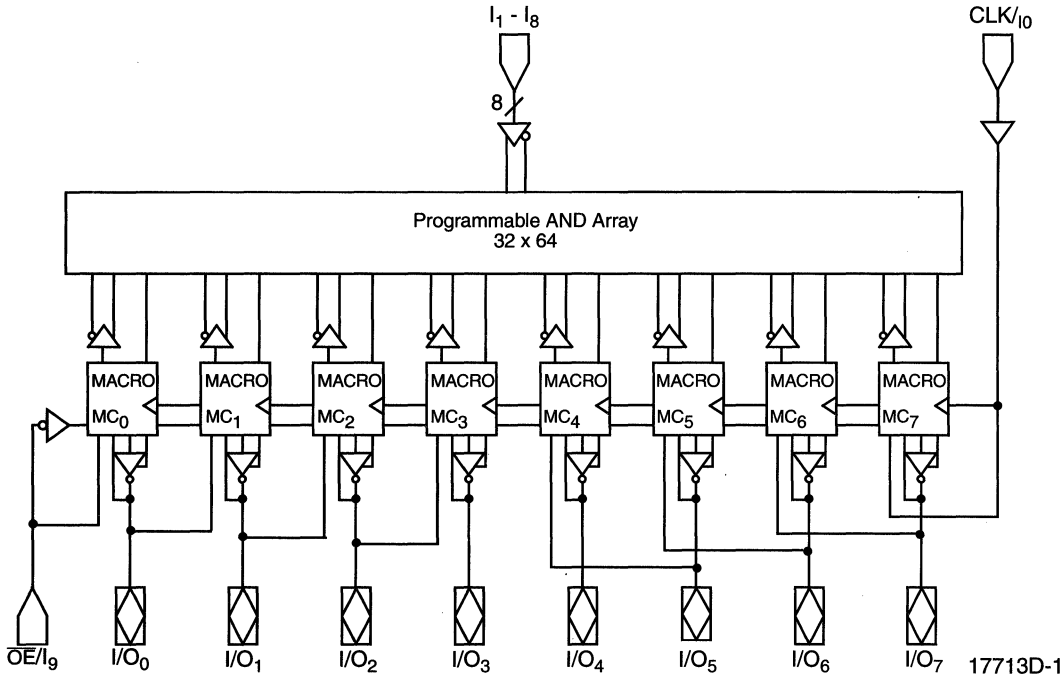
The PALLV16V8Z provides zero standby power and high speed. At 30-μA maximum standby current, the PALLV16V8Z allows battery powered operation for an extended period.

The PALLV16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

Publication# **17713** Rev: **E**
Amendment/**0** Issue Date: **November 1998**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The PALLV16V8 is a low-voltage, EE CMOS version of the PALCE16V8.

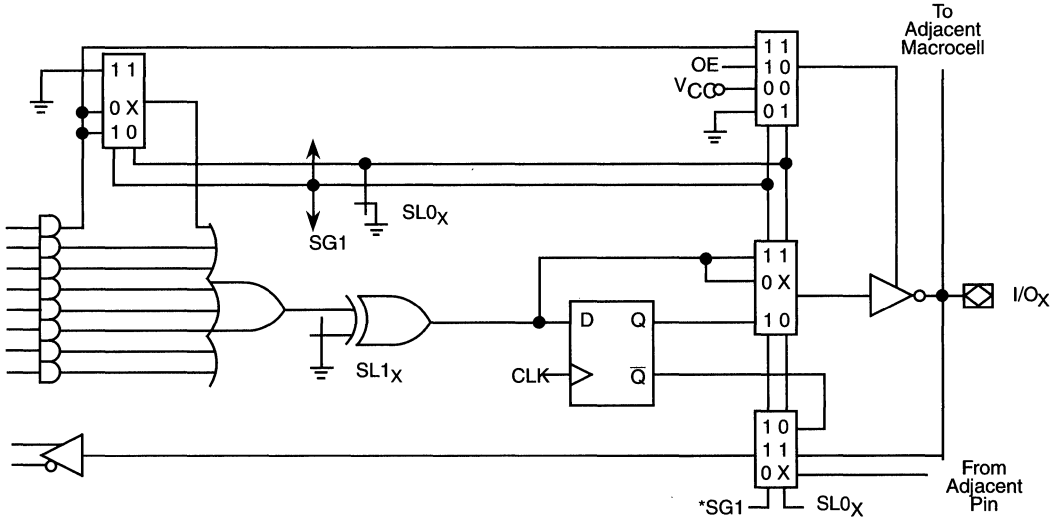
The PALLV16V8Z is a low-voltage, EE CMOS version of the PALCE16V8. In addition, the PALLV16V8Z has zero standby power and an unused product term disable feature for reduced power consumption.

The PALLV16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0-MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALLV16V8 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALLV16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALLV16V8. The programmer will program the PALLV16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALLV16V8. Here the user must use the PALLV16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.* 17713D-004

Figure 1. PALLV16V8 Macrocell

CONFIGURATION OPTIONS

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALLV16V8 will emulate a PAL16R8 family. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7,

$\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$=0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALLV16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$=0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$=1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and OE are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$=1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$=1. The output buffer is disabled. Except for MC_0 and MC_7, the feedback signal is an adjacent I/O. For MC_0 and MC_7, the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

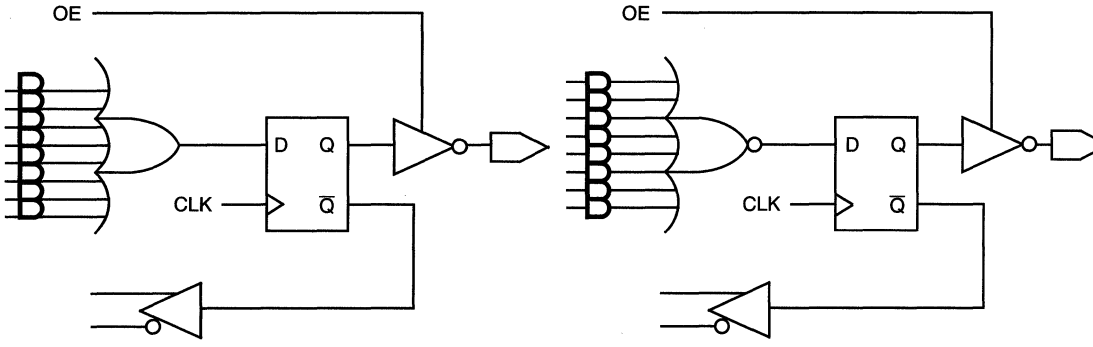
Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated	SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated
Device Uses Registers					Device Uses No Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4	1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
0	1	1	Combinatorial I/O	PAL16R6, 16R4	1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
					1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

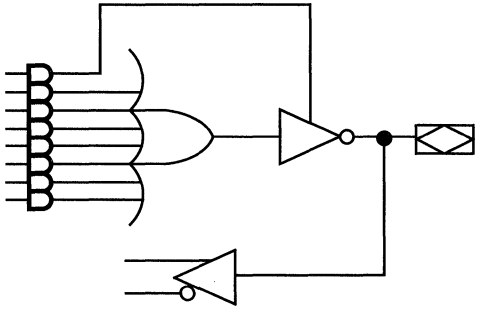
The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.

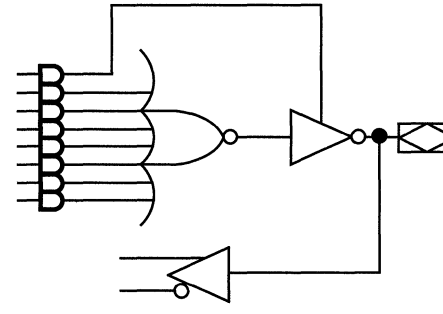


a. Registered active low

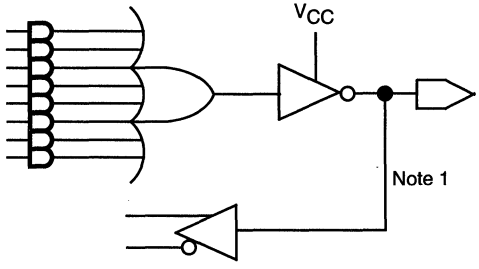
b. Registered active high



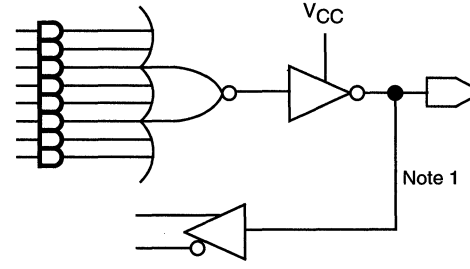
c. Combinatorial I/O active low



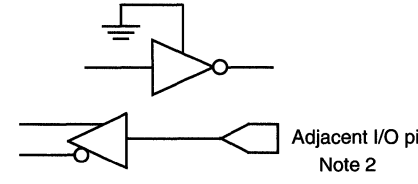
d. Combinatorial I/O active high



e. Combinatorial output active low



f. Combinatorial output active high



17713D-5

g. Dedicated input

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Benefits of Lower Operating Voltage

The PALLV16V8 has an operating voltage range of 3.0V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications. The PALLV16V8 inputs accept up to 5.5 V, so they are safe for mixed voltage design.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. A lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALLV16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALLV16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALLV16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALLV16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALLV16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALLV16V8 offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

Technology

The high-speed PALLV16V8Z is fabricated with Vantis' advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. This technology provides strong input-clamp diodes and a grounded substrate for clean switching.

Zero-Standby Power Mode

The PALLV16V8 features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALLV16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 30 µA). The outputs will maintain the states held before the device went into the standby mode. There is no speed penalty associated with coming out of standby mode.

When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This saving is illustrated in the I_{CC} vs. frequency graph.

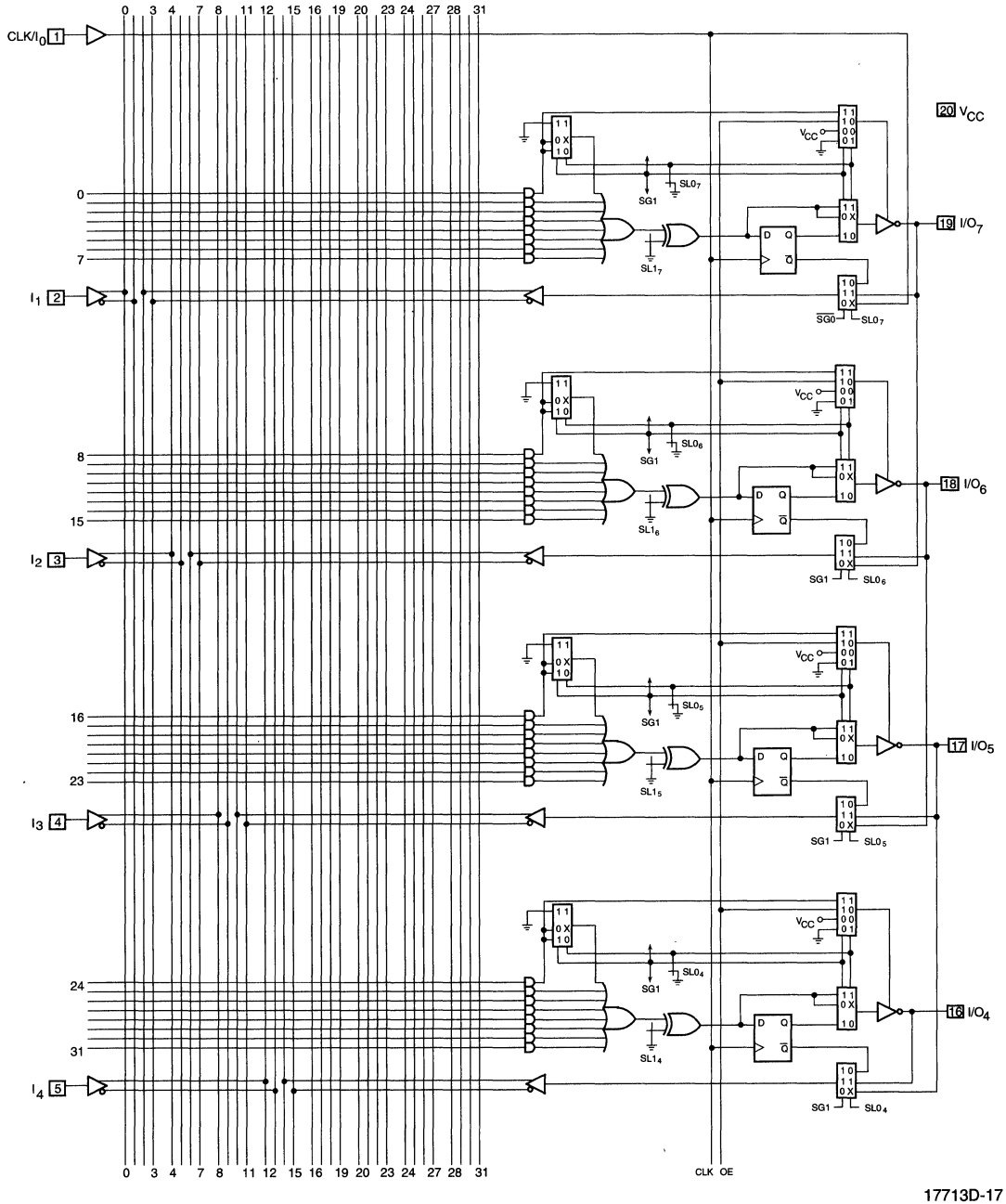
The PALLV16V8Z-20 has the free-running-clock feature. This means that if one or more registers are used, switching only the CLK will not wake up the logic array or any macrocell. The device will not be in standby mode because the CLK buffer will draw some current, but dynamic I_{CC} will typically be less than 2 mA.

Product-Term Disable

On a programmed PALLV16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graph, product-term disabling results in considerable power savings. This saving is greater at the higher frequencies.

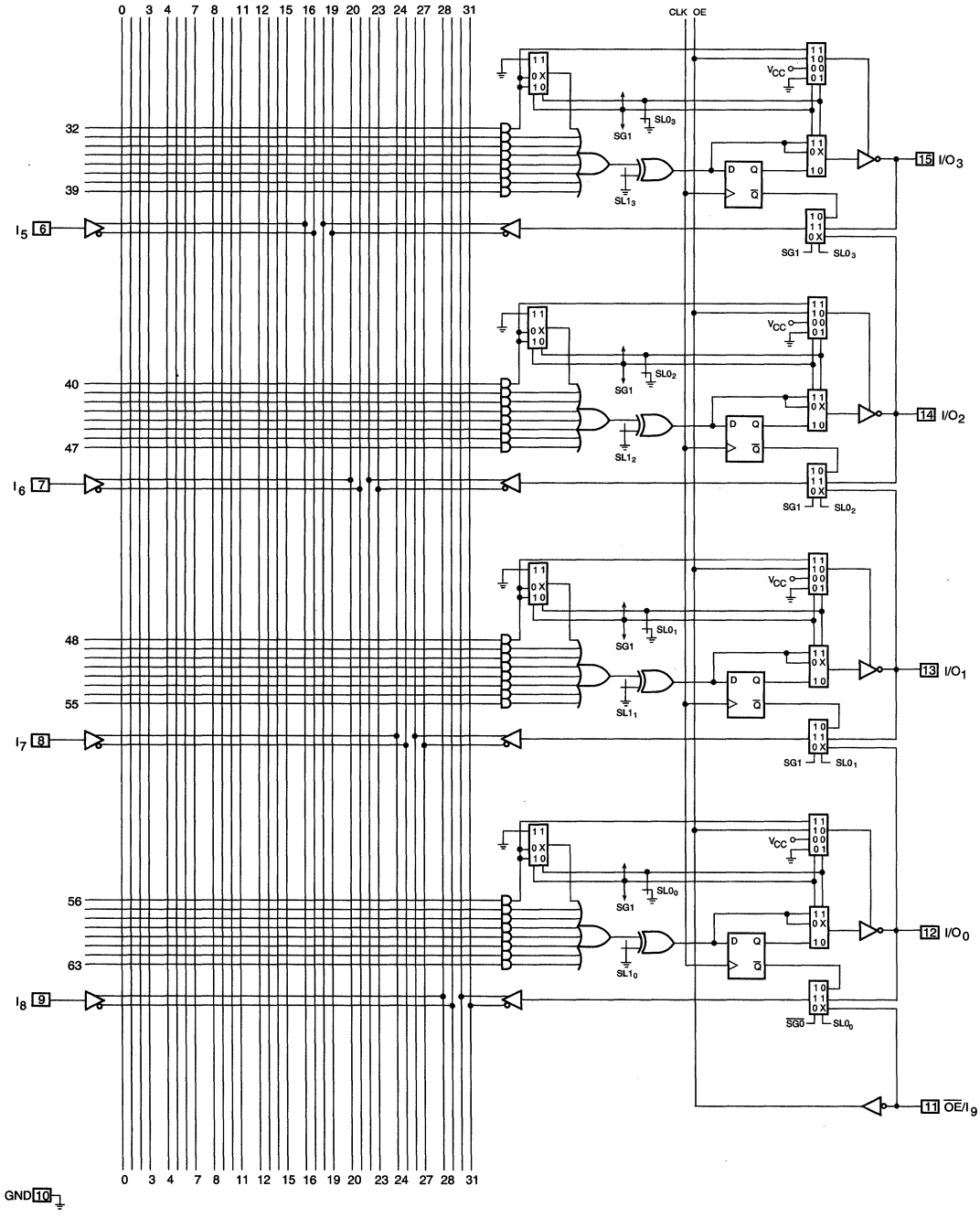
Further hints on minimizing power consumption can be found in a separate document entitled, *Minimizing Power Consumption with Zero-Power PLDs.*

LOGIC DIAGRAM



17713D-17

LOGIC DIAGRAM (CONTINUED)



17713D-18

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2001 V

Latch-up Current
(T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = –2 mA	2.4		V
			I_{OH} = –75 mA	V_{CC} - 0.2 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 mA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-50	-130	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz (Note 4)			55	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IL} and I_{OZL}).*
3. *Not more than one output should be shortened at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} - 3.3 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				10	ns
t_S	Setup Time from Input or Feedback to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Notes 2 and 3)	External Feedback	$1/(t_S + t_{CO})$	71.4		MHz
		Internal Feedback (fCNT	$1/(t_S + t_{CF})$	83.3		MHz
		No Feedback	$1/(t_S + t_H)$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				12	ns
t_{ER}	Input to Output Disable Using Product Term Control				12	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) - tS.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2001 V

Latch-up Current (T_A = -40°C to 85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = –2 mA	2.4		V
			I_{OH} = –75 µA	V_{CC} – 0.2 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-15	-75	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz (Note 4)	f = 0 MHz		30	µA
			f = 15 MHz		45	mA

Note:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

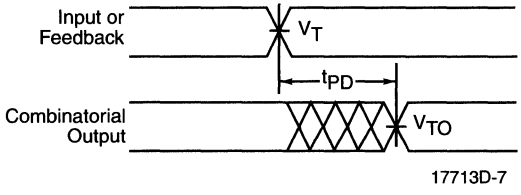
SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-20		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				20	ns
t_S	Setup Time from Input or Feedback to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback (fCNT)	$1/(t_S + t_{CF})$	50		MHz
		No Feedback	$1/(t_S + t_H)$	66.7		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				20	ns
t_{EA}	Input to Output Enable Using Product Term Control				20	ns
t_{ER}	Input to Output Disable Using Product Term Control				20	ns

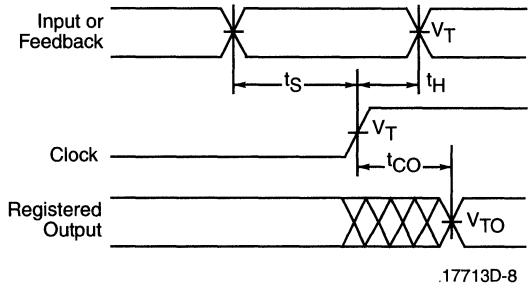
Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be about 2 ns faster.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

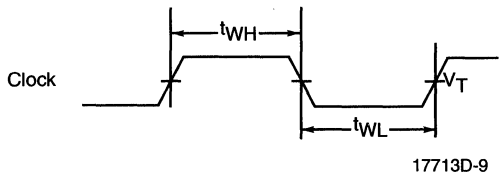
SWITCHING WAVEFORMS



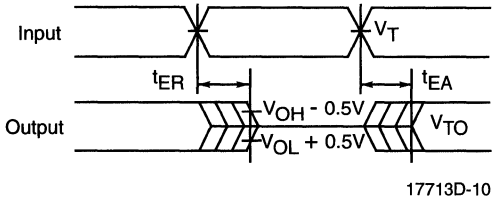
a. Combinatorial output



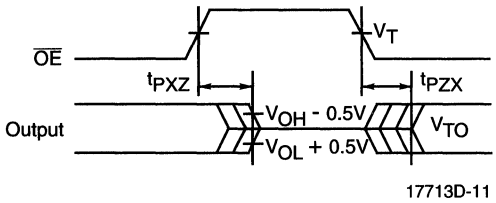
b. Registered output



c. Clock width



d. Input to output disable/enable



e. $\overline{OE}$ to output disable/enable

Notes:

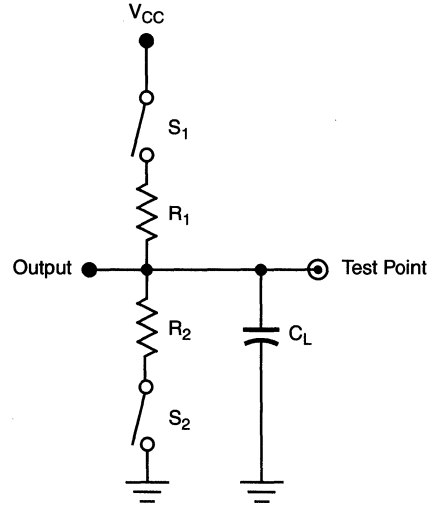
1. *V_T = 1.5 V for input signals and $V_{CC}/2$ for output signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

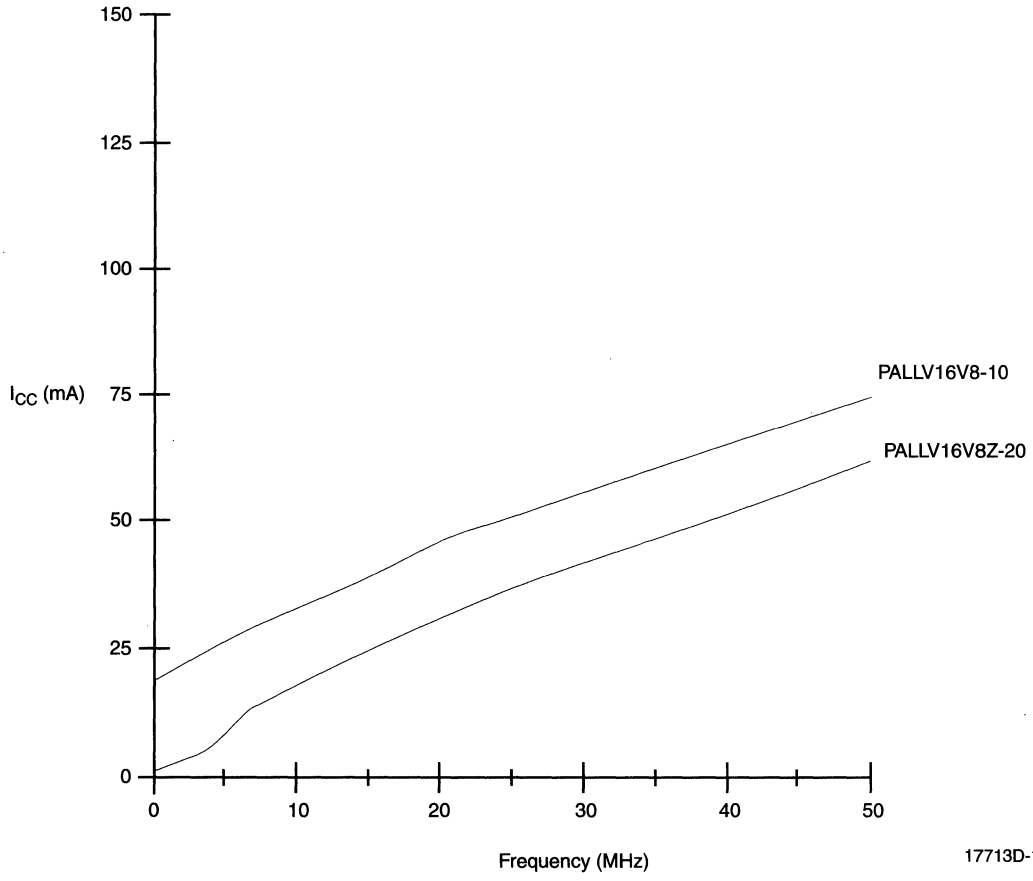
SWITCHING TEST CIRCUIT



17713D-12

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K	1.6K	$V_{CC}/2$
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				$V_{CC}/2$
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 3.3 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

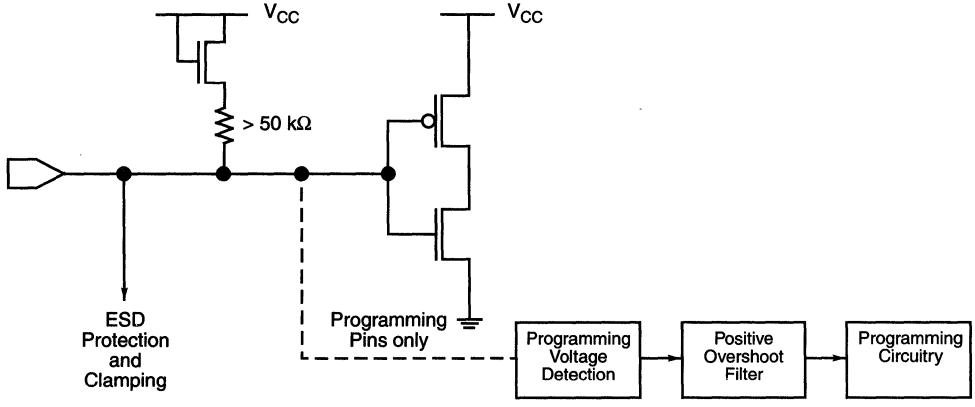
The PALLV16V8 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, devices can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

ROBUSTNESS FEATURES

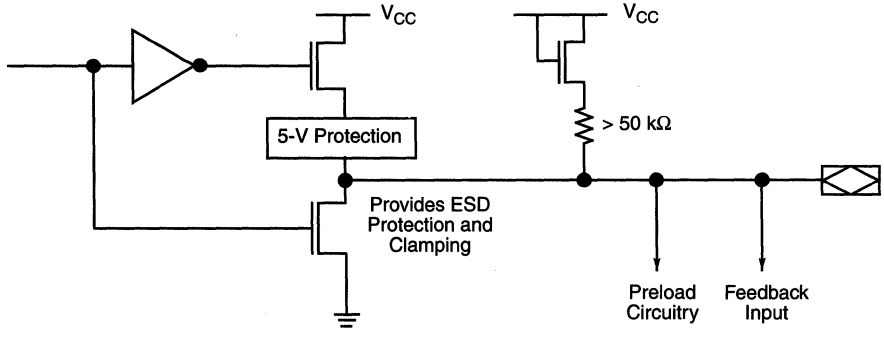
The PALLV16V8 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input

17713D-14



Typical Output

17713D-15

POWER-UP RESET

The PALLV16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			

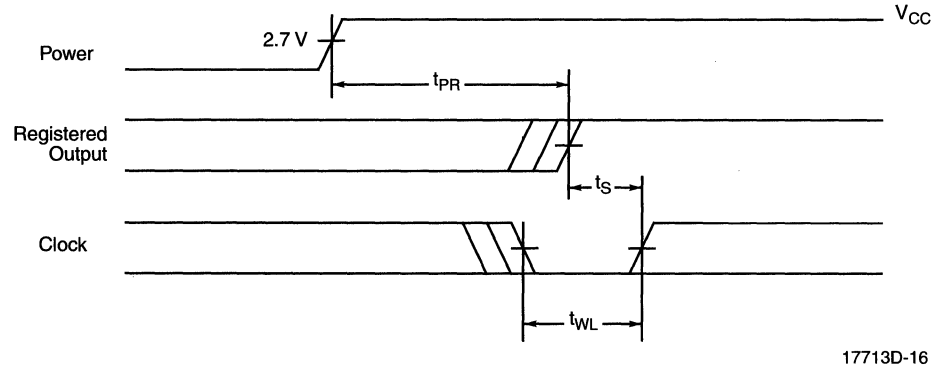


Figure 3. Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

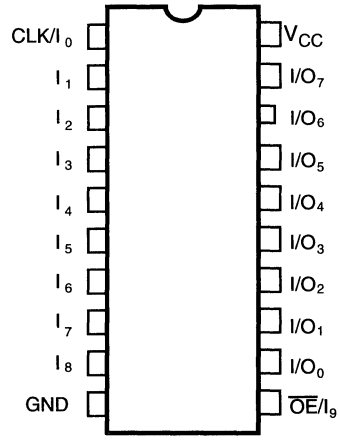
Parameter Symbol	Parameter Description		Typ		Unit
			PDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		20	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	57	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	58	41	°C/W
		400 lfpm air	51	37	°C/W
		600 lfpm air	47	35	°C/W
		800 lfpm air	44	33	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location ion the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant temperature. Therefore, the measurements can only be used in a similar environment.

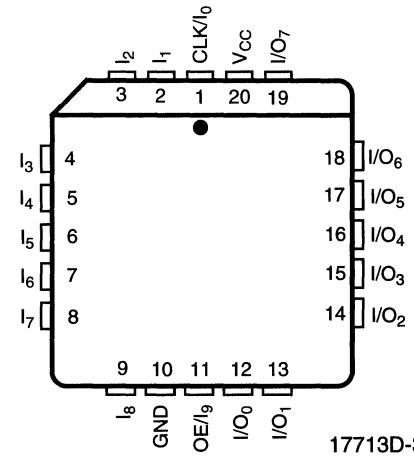
CONNECTION DIAGRAMS (TOP VIEW)

DIP/SOIC



17713D-2

PLCC



17713D-3

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

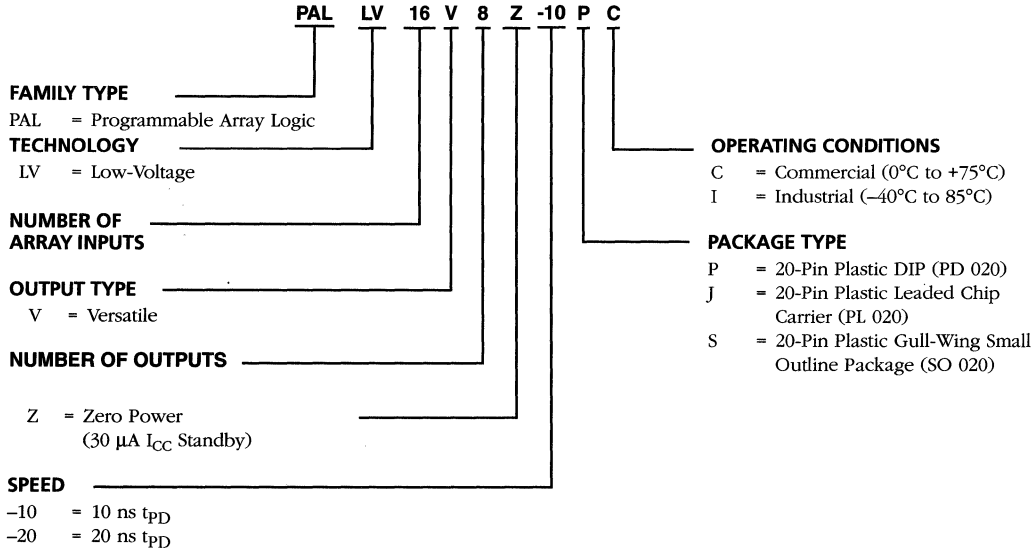
Note:
Pin 1 is marked for orientation.

PAL Devices

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALLV16V8-10	PC, JC, SC
PALLV16V8Z-20	PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released

VANTIS

BEYOND PERFORMANCE

COM'L: H-5/7/10/15/25, Q-10/15/25 IND: H-15/25, Q-20/25

PALCE20V8 Family

EE CMOS 24-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all PAL® 20V8 devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - 5-ns propagation delay for "-5" version
  - 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Programmable enable/disable control**
- **Outputs individually programmable as registered or combinatorial**
- **Peripheral Component Interconnect (PCI) compliant**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 24-pin plastic SKINNY DIP and 28-pin PLCC packages**
- **Extensive third-party software and programmer support**
- **Fully tested for 100% programming and functional yields and high reliability**
- **Programmable output polarity**
- **5-ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

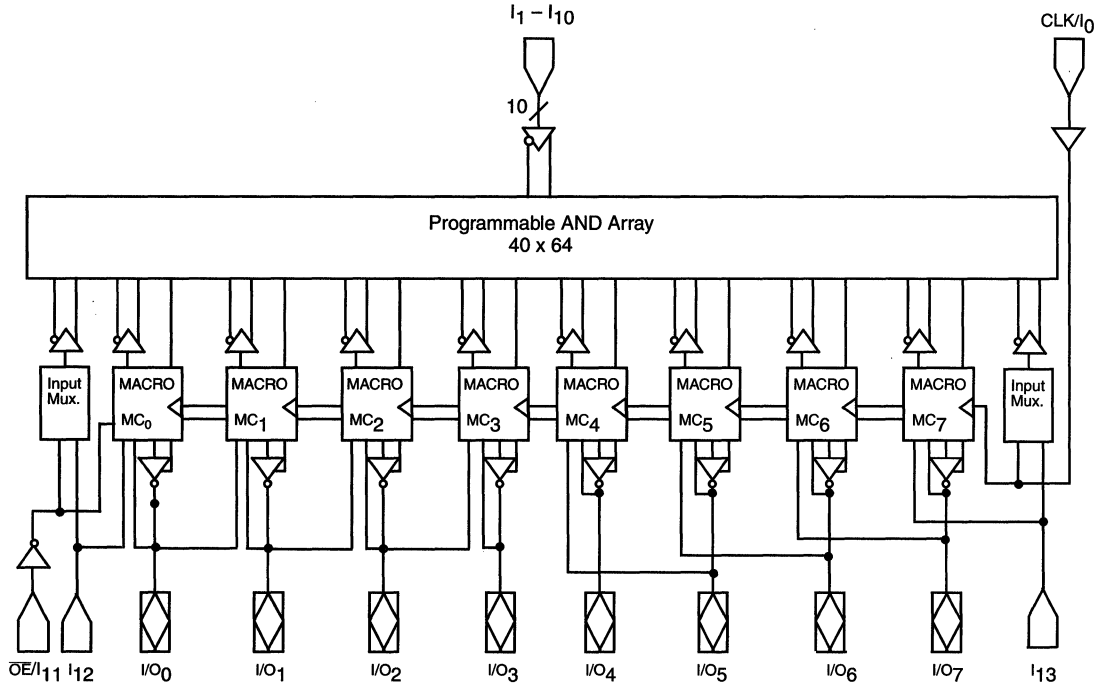
Device logic is automatically configured according to the user's design specification. A design is implemented using any of a number of popular design software packages, allowing automatic creation of a programming file based on Boolean or state equations. Design software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

Publication# **16491** Rev: **E**
Amendment/**0** Issue Date: **November 1998**

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM



16491E

FUNCTIONAL DESCRIPTION

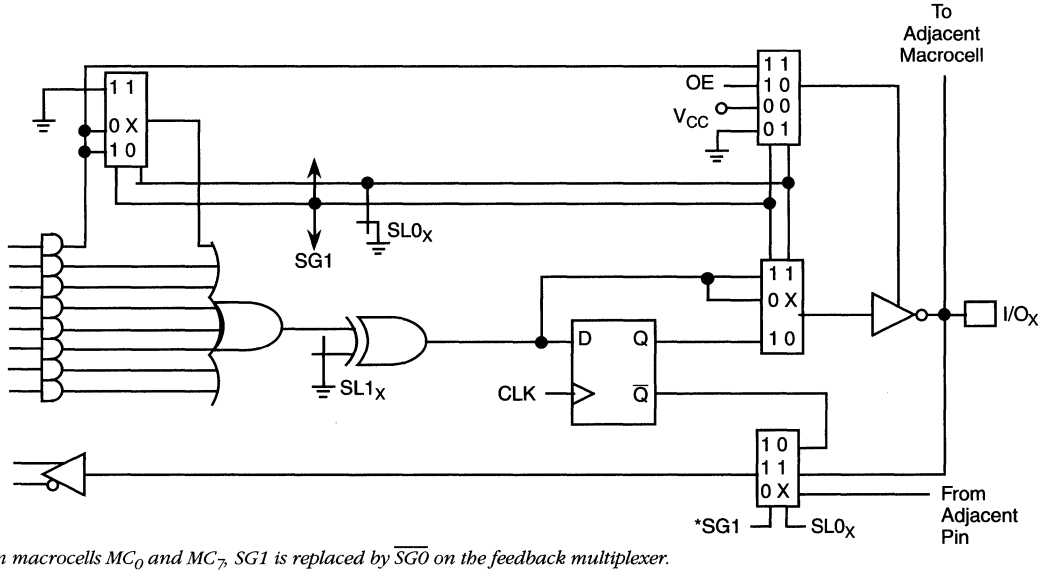
The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0-MC_7). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state, and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed

by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

16491E

Figure 1. PALCE20V8 Macrocell

CONFIGURATION OPTIONS

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer.

These configurations are summarized in Table 1 and illustrated in Figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins may be available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 18(21) and 19(23). Pins 18(21) and 19(23) do not use feedback in this mode.

Note:

1. *The pin number without parentheses refers to the SKINNY DIP package. The pin number in parentheses refers to the PLCC package.*

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

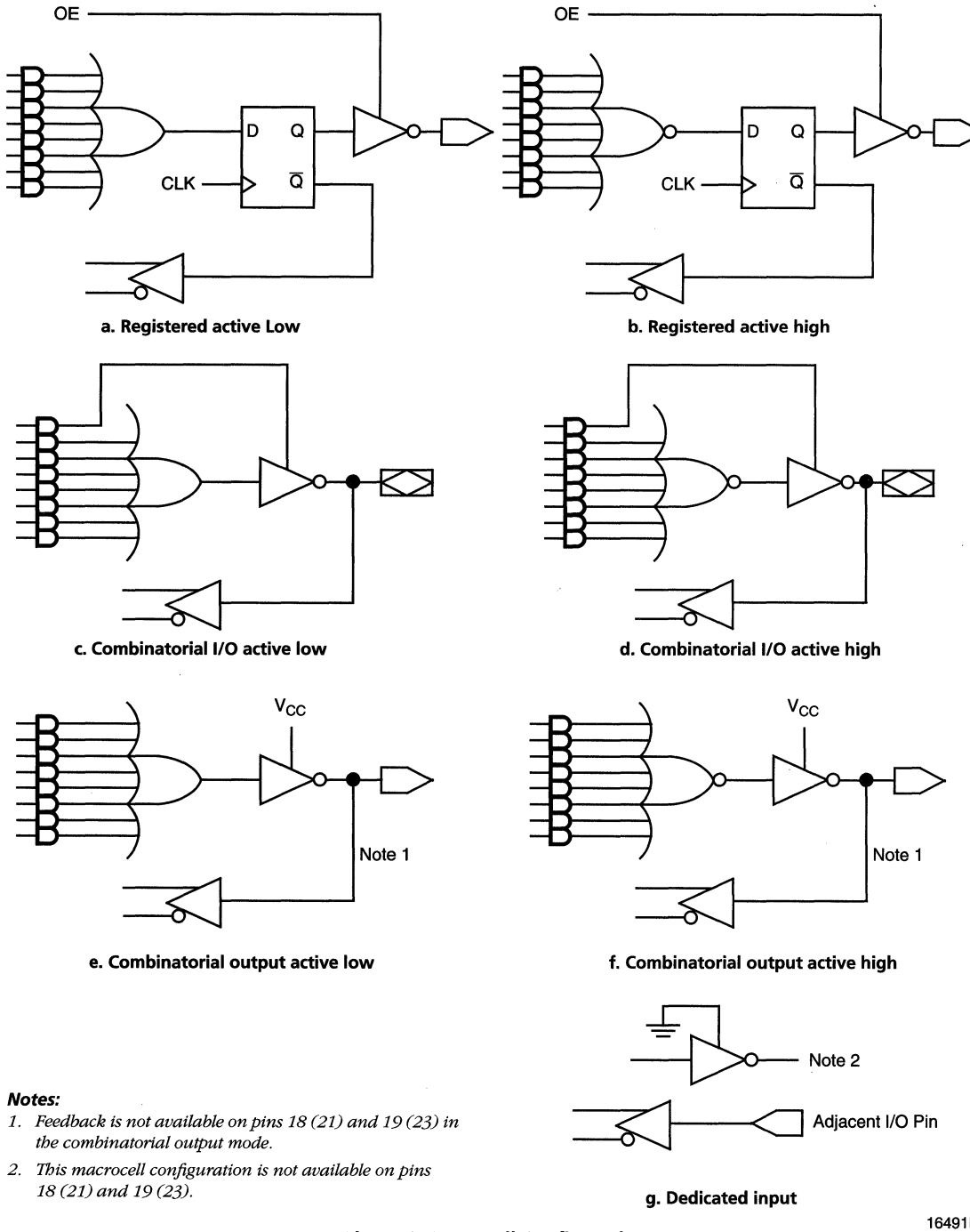
The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated	SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated
Device Uses Registers					Device Uses No Registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4	1	0	0	Combinatorial Output	PAL20L2, 18L4, 16L6, 14L8
0	1	1	Combinatorial I/O	PAL20R6, 20R4	1	0	1	Input	PAL20L2, 18L4, 16L6
					1	1	1	Combinatorial I/O	PAL20L8



Notes:

1. *Feedback is not available on pins 18 (21) and 19 (23) in the combinatorial output mode.*
2. *This macrocell configuration is not available on pins 18 (21) and 19 (23).*

16491E

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE20V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming and post-programming functional yields in the industry.

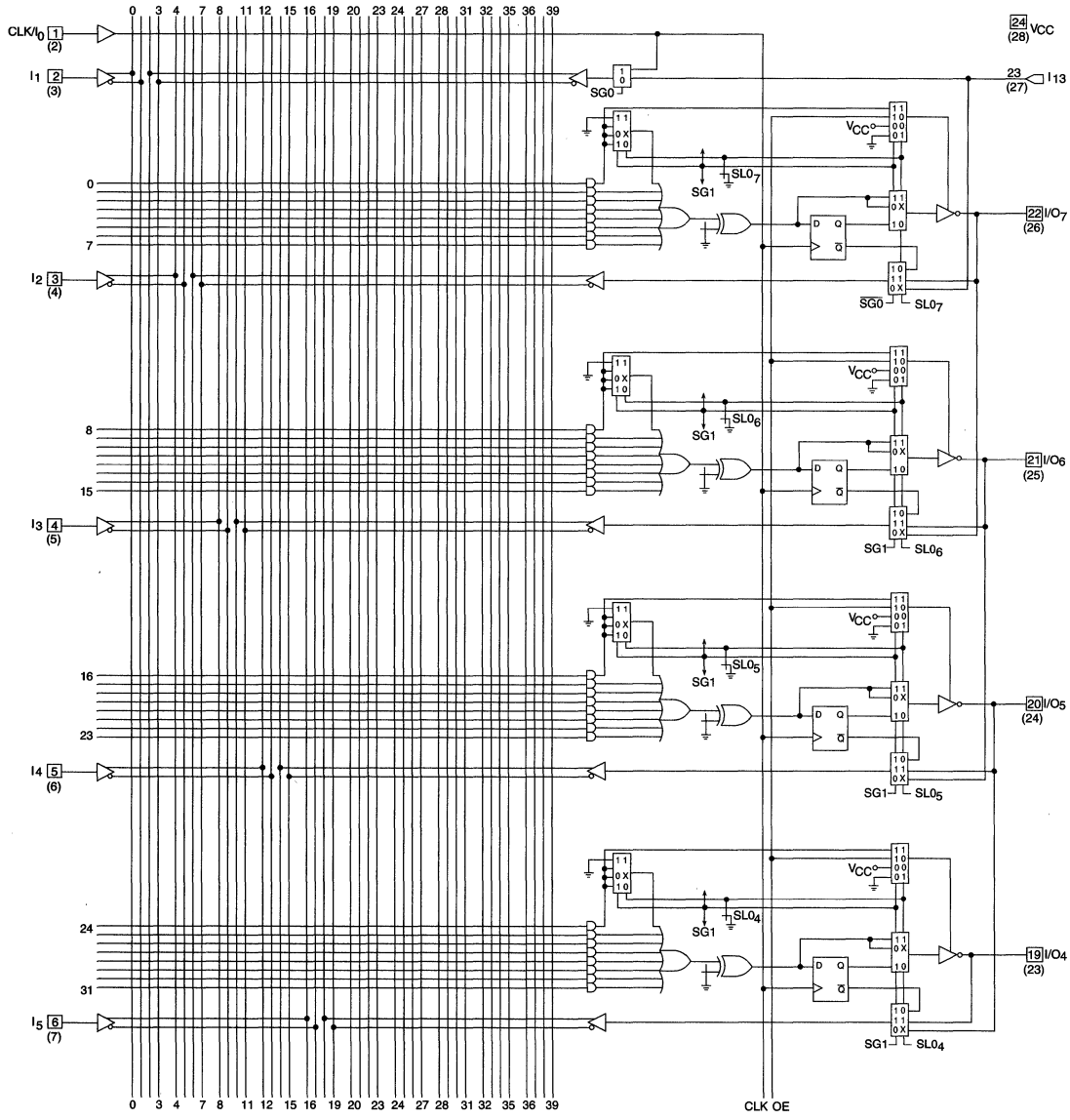
Technology

The high-speed PALCE20V8H is fabricated with Vantis' advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

PCI Compliance

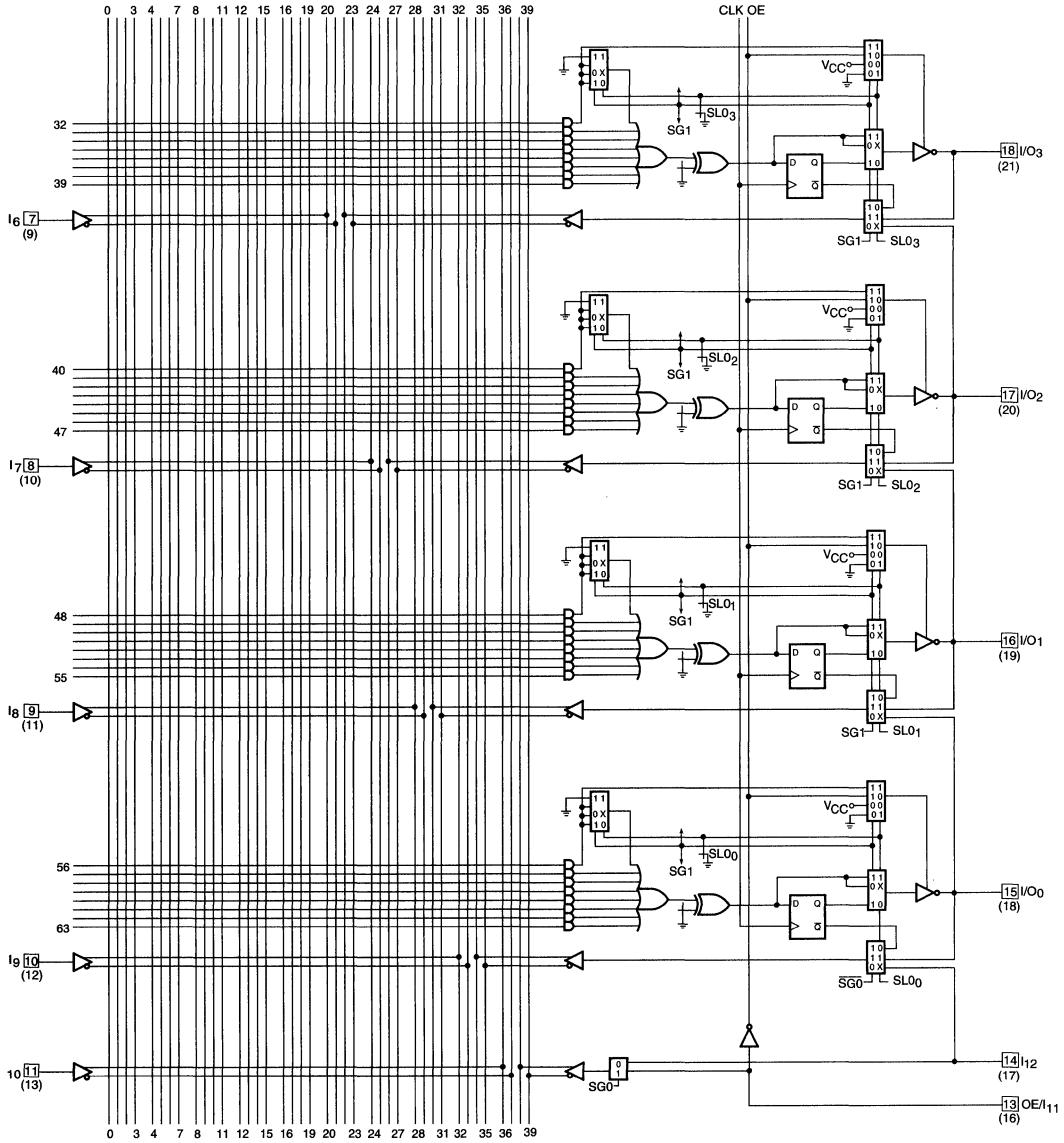
PALCE20V8H devices in the -5/-7/-10 speed grades are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE20V8H's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

LOGIC DIAGRAM



16491E

LOGIC DIAGRAM (CONTINUED)



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(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Static)	Supply Current for -5	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA
I_{CC} (Dynamic)	Supply Current for -7 and -10	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-5		-7		-10		Unit
				Min[2]	Max	Min[2]	Max	Min[2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output			1	5	3	7.5	3	10	ns
t_S	Setup Time from Input or Feedback to Clock			3		5		7.5		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output			1	4	1	5	3	7.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1		1		1	ns
t_{WL}	Clock Width	LOW		3		4		6		ns
t_{WH}		HIGH		3		4		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	142.8		100		66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 5)	166		125		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	166		125		83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	1	6	2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	1	6	2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	3	9	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	3	9	3	10	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
3. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Supply Current for -10	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz (Note 4)		55	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10		Unit
				Min[2]	Max	
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 4)	71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 3)	50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) Operating
in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H		130	mA
			Q		65	

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

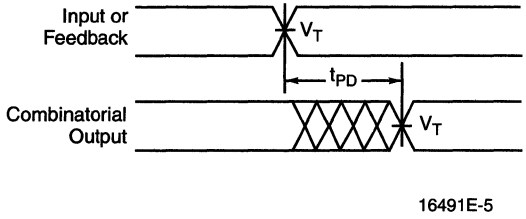
SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		20		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		13		15		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				10		11		12	ns
t_{WL}	Clock Width	LOW		8		10		12		ns
t_{WH}		HIGH		8		10		12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S+t_{CO})$	45.5		41.6		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S+t_{CF})$ (Note 3)	50		45.4		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		50.0		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		18		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		18		25	ns

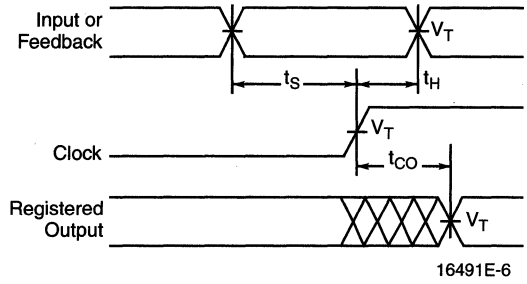
Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

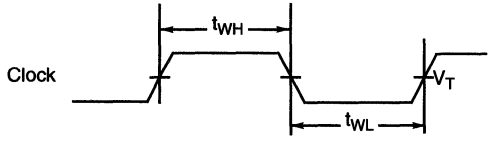
SWITCHING WAVEFORMS



a. Combinatorial output

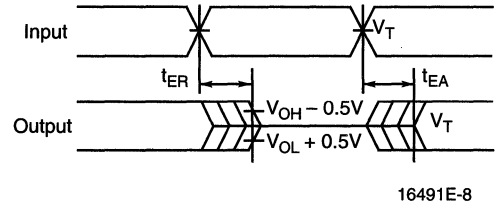


b. Registered output

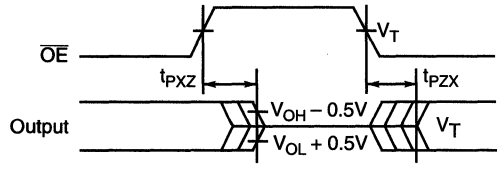


c. Clock width

16491E-7



d. Input to output disable/enable



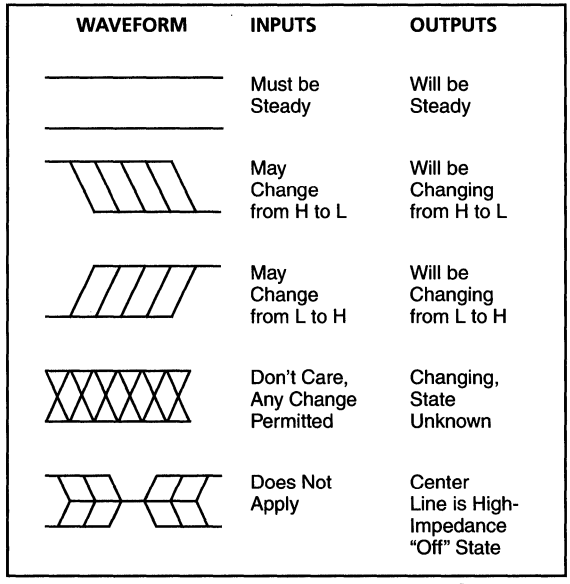
e. $\overline{OE}$ to output disable/enable

16491E-9

Notes:

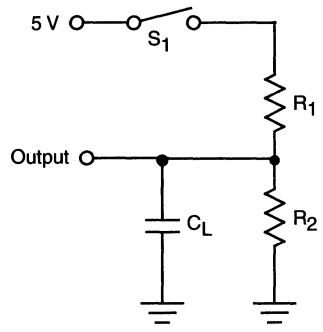
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT

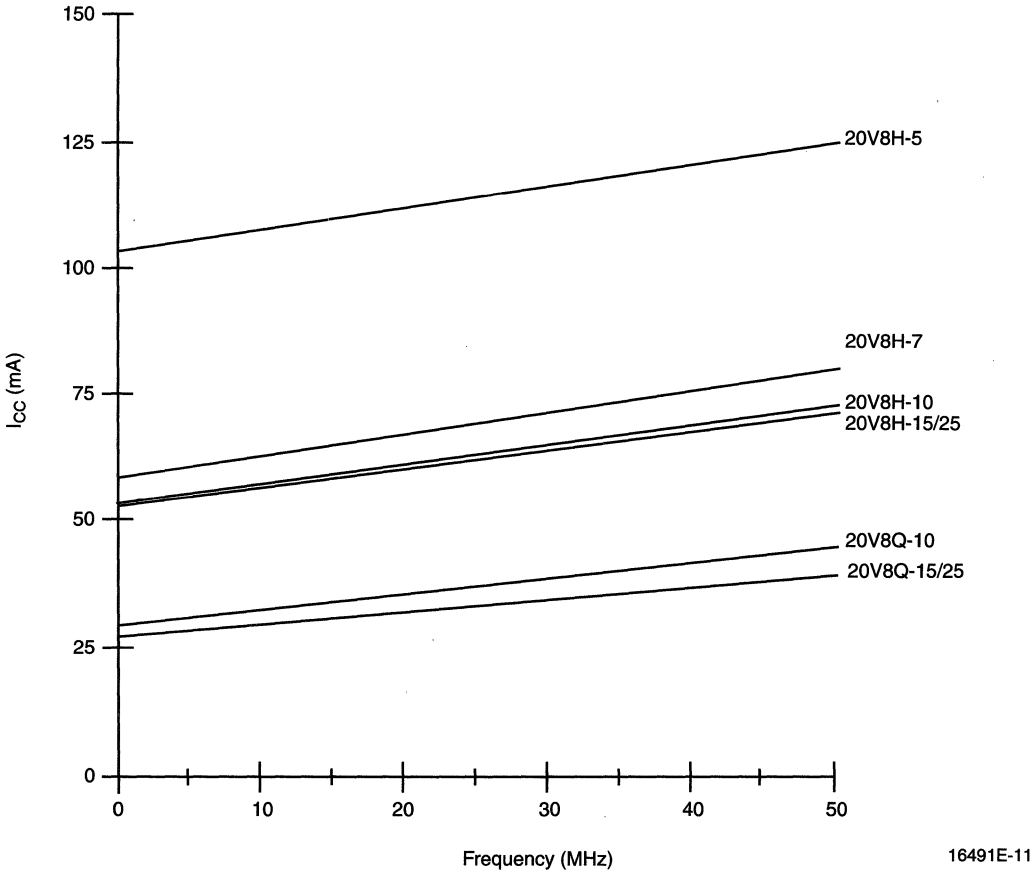


16491E-10

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open				1.5 V
	Z → L: Closed				
t_{PXZ}, t_{ER}	H → Z: Open	5 pF		H-5: 200 Ω	H → Z: V_{OH} – 0.5 V
	L → Z: Closed				L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

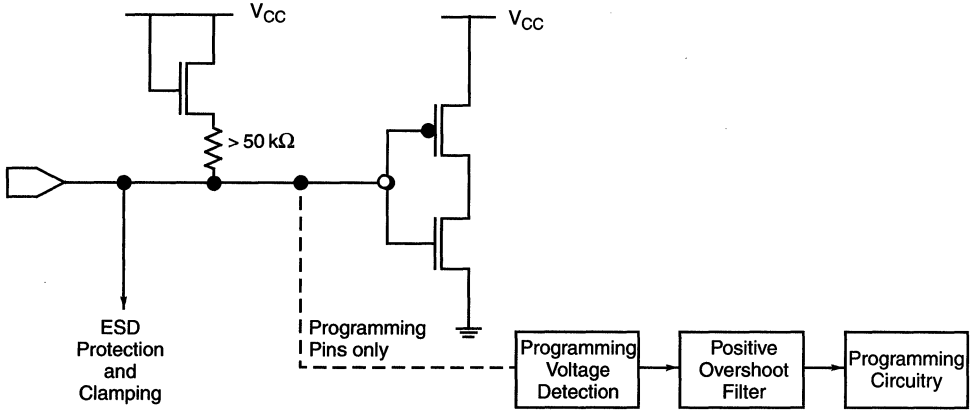
The PALCE20V8 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

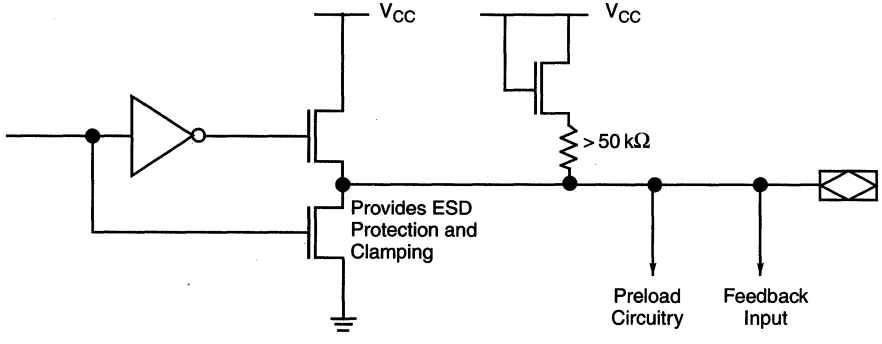
ROBUSTNESS FEATURES

The PALCE20V8X-X/5 have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR PALCE20V8H-7 AND PALCE20V8H-5



Typical Input

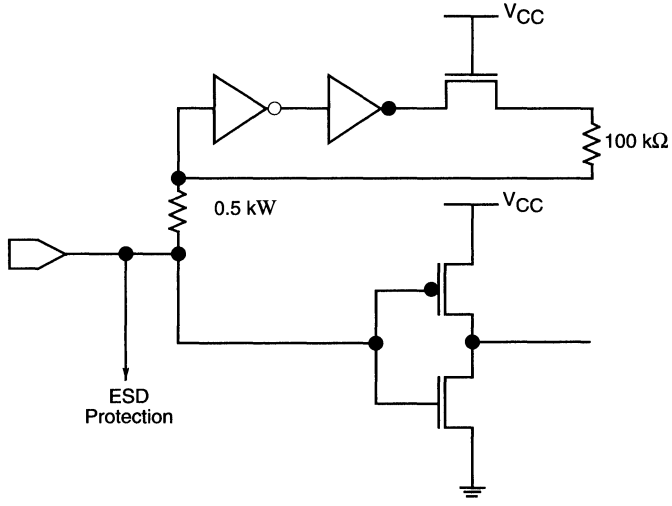


16491E-12

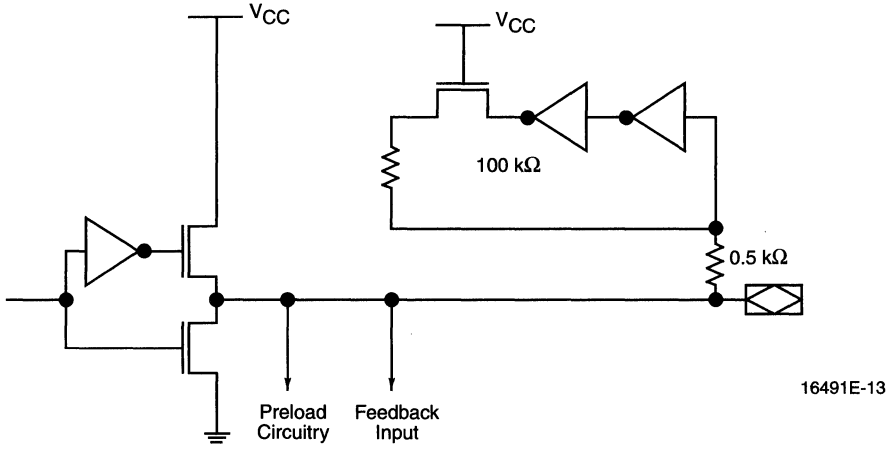
Typical Output

Device	Rev Letter
PALCE20V8H-7	A
PALCE20V8H-5	A

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /4 VERSIONS



Input



I/O

Device	Rev Letter
PALCE20V8H-10	M
PALCE20V8H-15	L, M
PALCE20V8H-15	M
PALCE20V8H--25	M
PALCE20V8H-25	M

Topside Marking:

Vantis CMOS PLDs are marked on top of the package in the following manner:

PALCEXXX

Datecode (3 numbers) Lot ID (4 characters)—(Rev Letter)

The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			

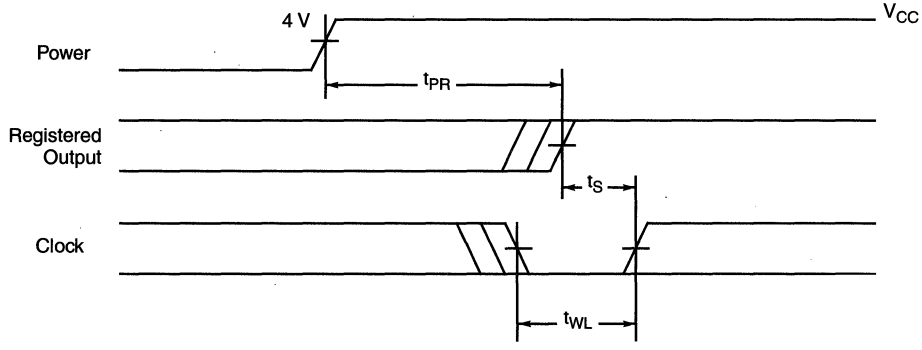


Figure 2. Power-Up Reset Waveform

16491E-15

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

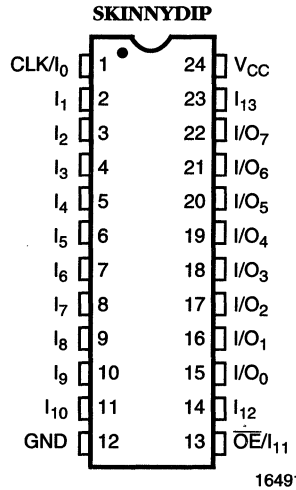
Parameter Symbol	Parameter Description		Typ		Unit
			PDID	PLCC	
θ_{jc}	Thermal impedance, junction to case		19	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	61	45	°C/W
		400 lfpm air	53	41	°C/W
		600 lfpm air	50	38	°C/W
		800 lfpm air	47	36	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

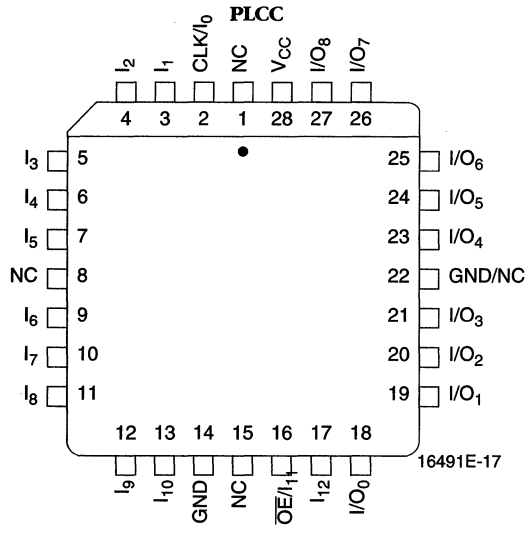
CONNECTION DIAGRAMS

Top View



16491E-16

Note:
Pin 1 is marked for orientation.



16491E-17

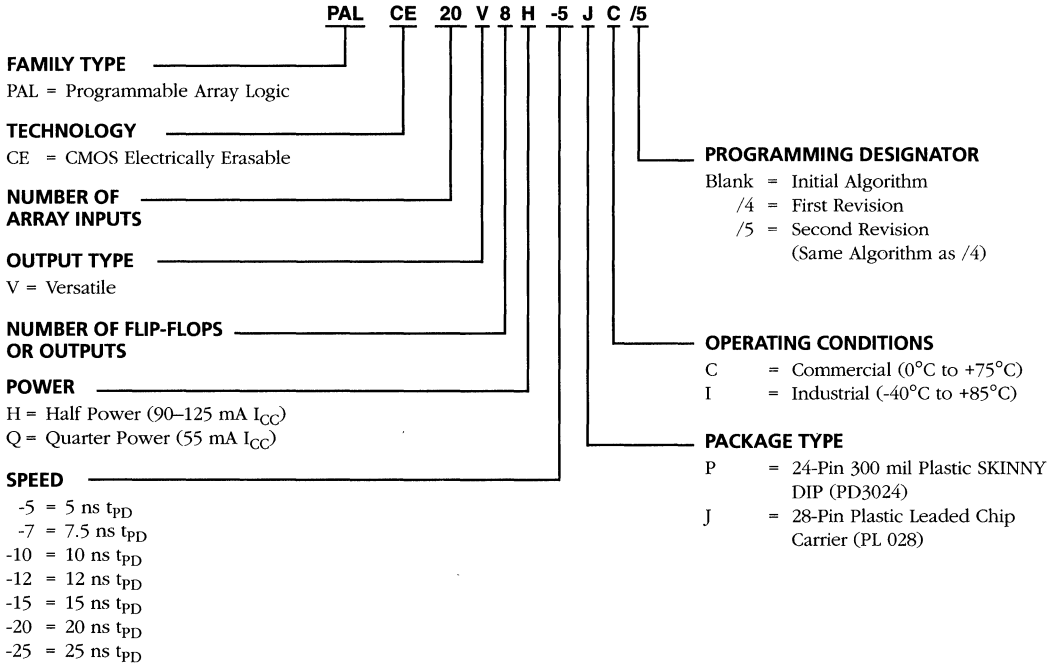
PIN DESIGNATIONS

CLK	=	Clock	NC	=	No Connect
GND	=	Ground	$\overline{OE}$	=	Output Enable
I	=	Input	V_{CC}	=	Supply Voltage
I/O	=	Input/Output			

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-5	JC	/5
PALCE20V8H-7	PC, JC	
PALCE20V8H-10		/4
PALCE20V8Q-10	PC	/5
PALCE20V8H-15	PC, JC, PI, JI	/4
PALCE20V8Q-15	PC, JC	
PALCE20V8Q-20	PI, JI	
PALCE20V8H-25	PC, JC, PI, JI	
PALCE20V8Q-25		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

VANTIS
BEYOND PERFORMANCE

PALCE22V10 and PALCE22V10Z Families

24-Pin EE CMOS (Zero Power) Versatile PAL Device

DISTINCTIVE CHARACTERISTICS

- **As fast as 5-ns propagation delay and 142.8 MHz f_{MAX} (external)**
- **Low-power EE CMOS**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Peripheral Component Interconnect (PCI) compliant (-5/-7/-10)**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support**
- **24-pin SKINNY DIP, 24-pin SOIC, and 28-pin PLCC**
- **5-ns and 7.5-ns versions utilize split leadframes for improved performance**

GENERAL DESCRIPTION

The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z is an advanced PAL® device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

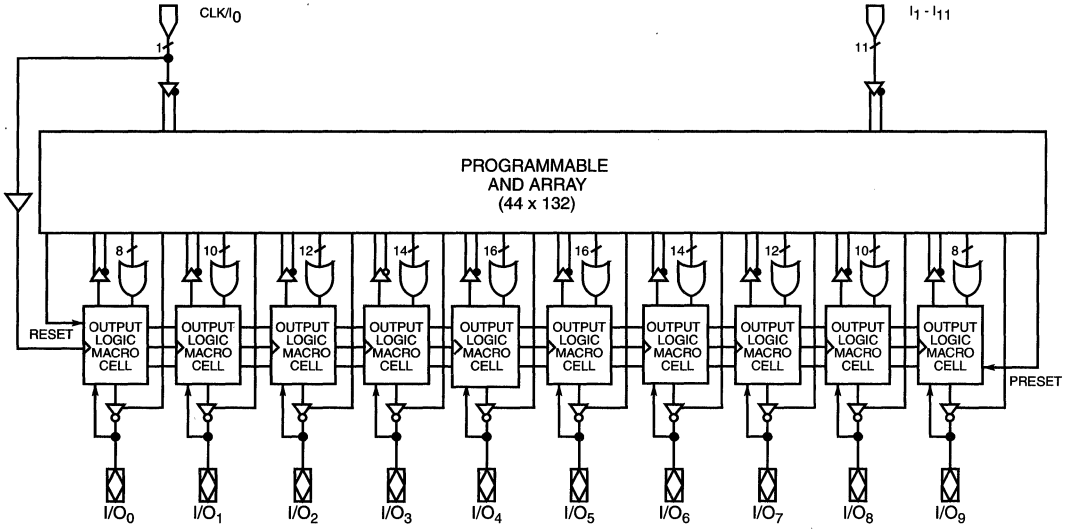
The PALCE22V10Z provides zero standby power and high speed. At 30 µA maximum standby current, the PALCE22V10Z allows battery-powered operation for an extended period.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active-high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

Publication# **16564** Rev: **E**
Amendment/**0** Issue Date: **November 1998**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

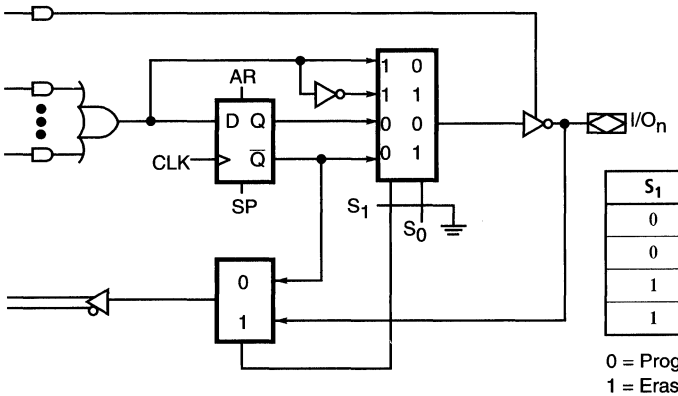
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with an EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

16564E-004

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

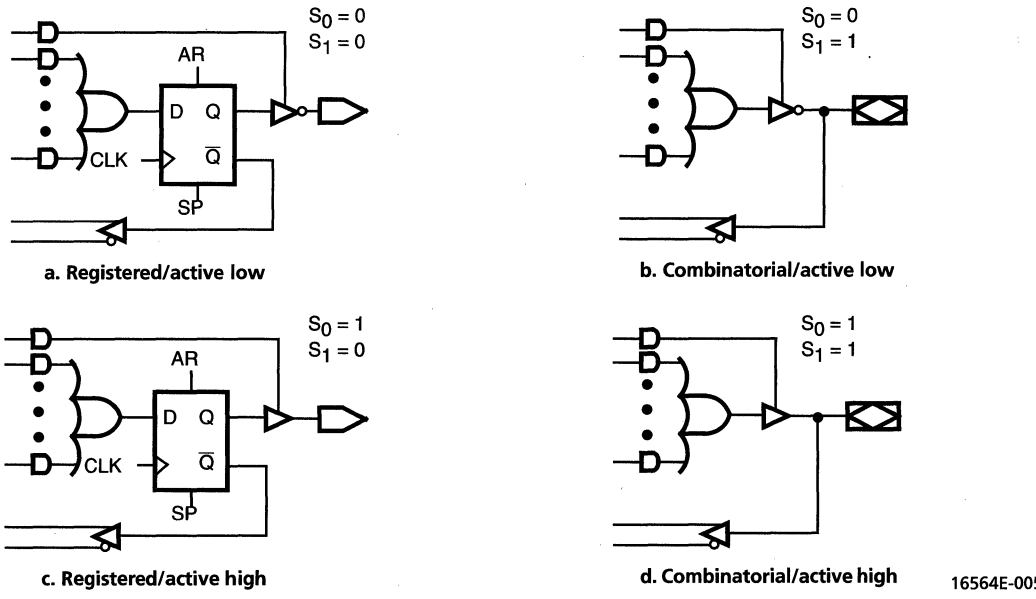


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bi-directional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has preset and reset product terms. These terms are connected to all registered outputs. When the synchronous preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic, and the reset delay time is 1000ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE22V10 is fabricated with Vantis' advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

PCI Compliance

The PALCE22V10H devices in the -5/-7/-10 speed grades are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE22V10H's predictable timing ensures compliance with the PCI AC specifications independent of the design.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down

most of its internal circuitry. The current will go to almost zero (I_{CC} < 30 µA). The outputs will maintain the states held before the device went into the standby mode.

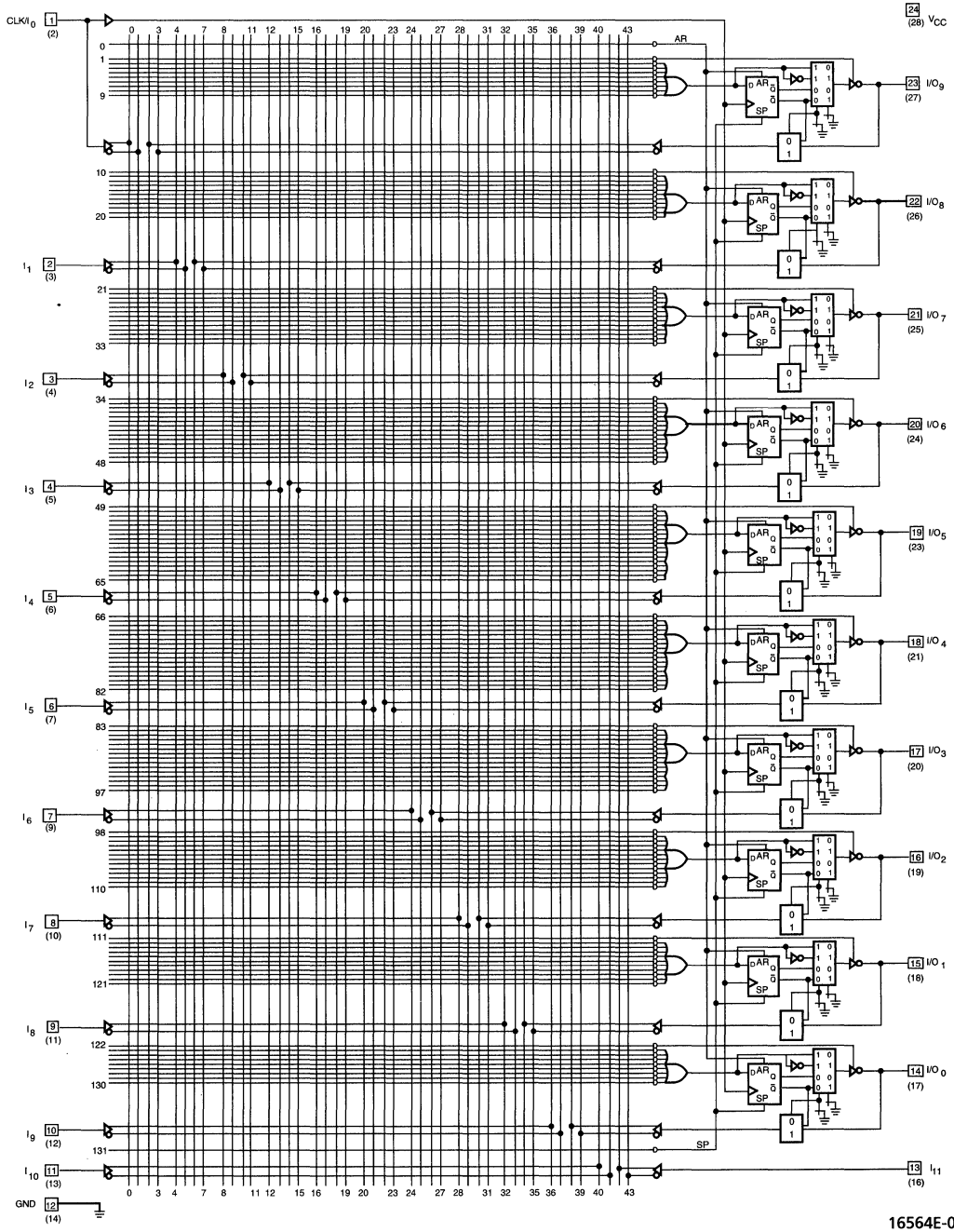
When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This saving is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graph, product-term disabling results in considerable power savings. This saving is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in a separate document entitled, *Minimizing Power Consumption with Zero-Power PLDs.*

LOGIC DIAGRAM



16564E-006

PAL Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with
Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	-30	-130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		125	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time, and the duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-5 Min	-5 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				5	ns
t_{S1}	Setup Time from Input or Feedback			3		ns
t_{S2}	Setup Time from SP to Clock			4		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 2)				0.5	ns
t_{AR}	Asynchronous Reset to Registered Output				7.5	ns
t_{ARW}	Asynchronous Reset Width			4.5		ns
t_{ARR}	Asynchronous Reset Recovery Time			4.5		ns
t_{SPR}	Synchronous Preset Recovery Time			4.5		ns
t_{WL}	Clock Width	LOW		2.5		ns
t_{WH}		HIGH		2.5		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	150		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	200		MHz
t_{EA}	Input to Output Enable Using Product Term Control				6	ns
t_{ER}	Input to Output Disable Using Product Term Control				5.5	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Skew is measured with all outputs switching in the same direction.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, VCC = Max T_A = 25°C (Note 3)	-30	-130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-7 PDIP Min	-7 PDIP Max	-7 PLCC Min	-7 PLCC Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	7.5	3	7.5	ns
t_{S1}	Setup Time from Input or Feedback			5		4.5		ns
t_{S2}	Setup Time from SP to Clock			6		6		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			2	5	2	4.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 2)				1		1	ns
t_{AR}	Asynchronous Reset to Registered Output				10		10	ns
t_{ARW}	Asynchronous Reset Width			7		7		ns
t_{ARR}	Asynchronous Reset Recovery Time			7		7		ns
t_{SPR}	Synchronous Preset Recovery Time			7		7		ns
t_{WL}	Clock Width	LOW		3.5		3.0		ns
t_{WH}		HIGH		3.5		3.0		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	100		111		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	125		133		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	142.8		166		MHz
t_{EA}	Input to Output Enable Using Product Term Control				7.5		7.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		7.5	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *Skew is measured with all outputs switching in the same direction.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with
Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect
to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . -0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, VCC = Max T_A = 25°C (Note 3)	-30	-130	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open , (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		120	mA

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S1}	Setup Time from Input or Feedback			6		ns
t_{S2}	Setup Time from SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	83.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 3)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:* $t_{CF} = 1/f_{MAX}$ *(internal feedback)* $- t_S$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	-30	-130	mA
I_{CC} (Static)	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0mA), V_{CC} = Max (Note 4)		55	mA

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time, and the duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test condition. Refer to the I_{CC} vs. frequency graph for typical I_{CC} characteristics.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			6		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	83		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CO})$ (Note 3)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-15) . . . . . +4.75 V to +5.25 V

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25) . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)		-30	-130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time, and the duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 3)	58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may vary.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = -3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current		V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current		V_{IN} = 0 V, V_{CC} = Max (Note 2)		-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		-100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	-30	-130	mA
I_{CC} (Static)	Supply Current	H-20/25	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		100	mA
		H-10/15			110	
I_{CC} (Dynamic)	Supply Current		V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz		130	mA

Notes:

1. *These are absolute values with respect to the device ground, and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time, and the duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10		-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				10		15		20		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		10		12		15		ns
t_H	Hold Time			0		0		0		0		ns
t_{CO}	Clock to Output				6		10		12		15	ns
t_{AR}	Asynchronous Reset to Registered Output				13		20		25		25	ns
t_{ARW}	Asynchronous Reset Width			8		15		20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		10		20		25		ns
t_{SPR}	Synchronous Preset Recovery Time			8			10		14	25		ns
t_{WL}	Clock Width	LOW		4		8		10		13		ns
t_{WH}		HIGH		4		8		10		13		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	83.3		50		41.6		33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 3)	110		58.8		45.4		35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		83.3		50		38.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10		15		20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				9		15		20		25	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OH} = -6 mA	3.84		V
			I_{OH} = -20 µA	V_{CC}-0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OL} = 16 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		-5	-150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		30	µA
			f = 15 MHz		100	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-15 Min	-15 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 3)	58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -6 mA	3.84		V
			I_{OH} = -20 µA	V_{CC}-0.1		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 16 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		-5	-150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	f = 0 MHz		30	mA
			f = 15 MHz		120	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

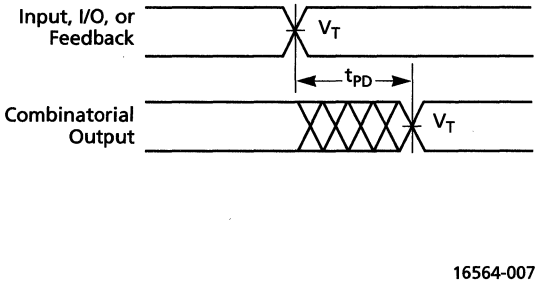
SWITCHING CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES [1]

Parameters Symbol	Parameter Description			-25		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Notes 3)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

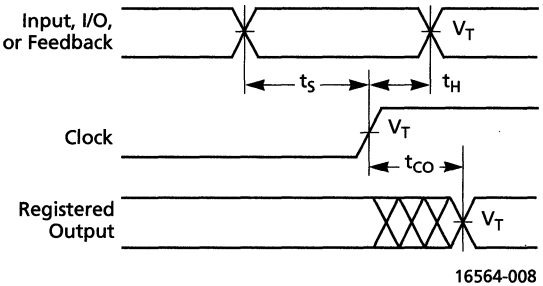
1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 5 ns faster.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

SWITCHING WAVEFORMS



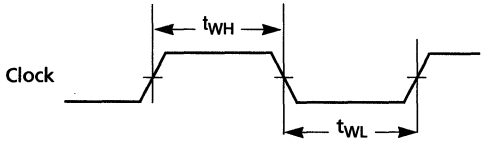
16564-007

a. Combinatorial output



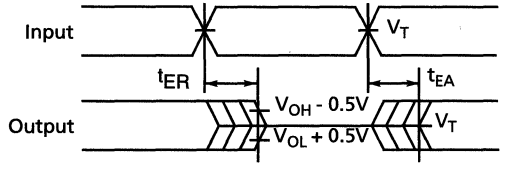
16564-008

b. Registered output



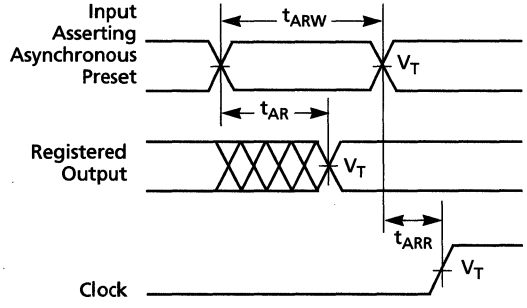
16564-009

c. Clock width



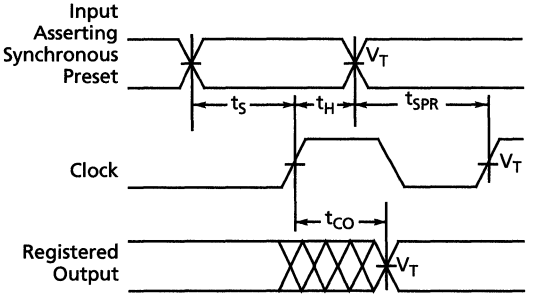
16564-010

d. Input to output disable/enable



16564-011

e. Asynchronous reset



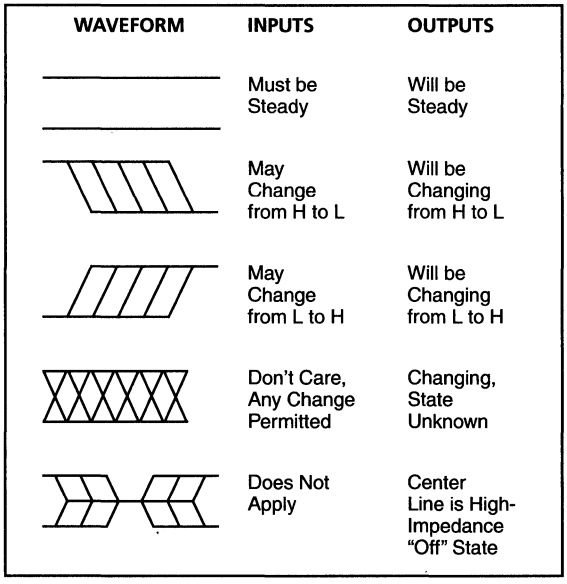
16564-012

f. Synchronous preset

Notes:

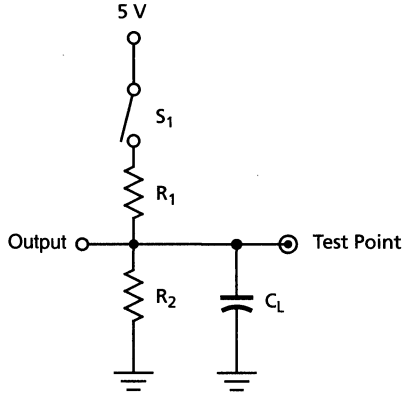
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



16564E-013

SWITCHING TEST CIRCUIT

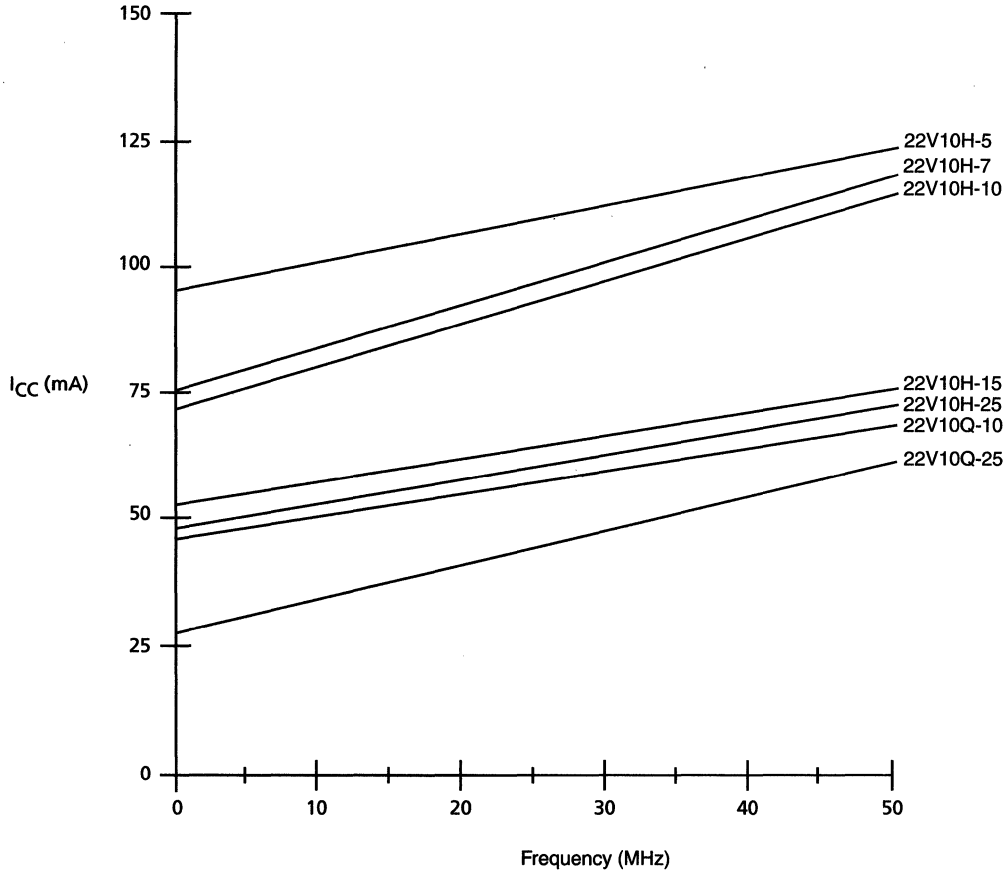


16564-014

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	All except H-5/7: 390 Ω	1.5 V
t_{EA}	Z → H: Open				1.5 V
	Z → L: Closed				
t_{ER}	H → Z: Open	5 pF		H-5/7: 300 Ω	H → Z: V_{OH} - 0.5 V
	L → Z: Closed				L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C

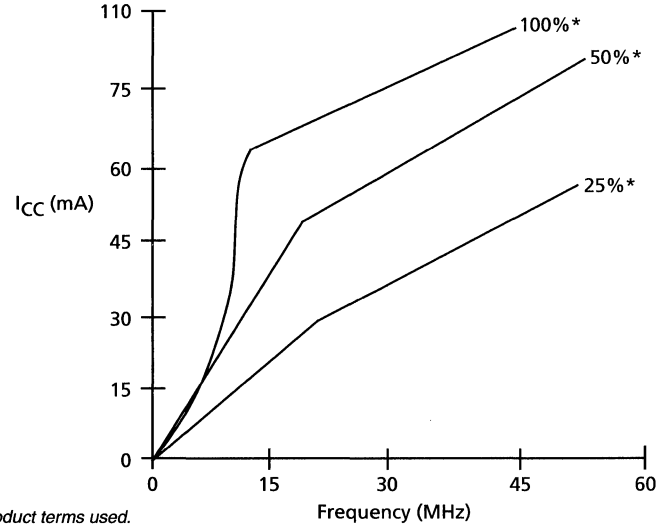


I_{CC} vs. Frequency 16564E-015

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE22V10Z-15
V_{CC} = 5.0 V, T_A = 25°C

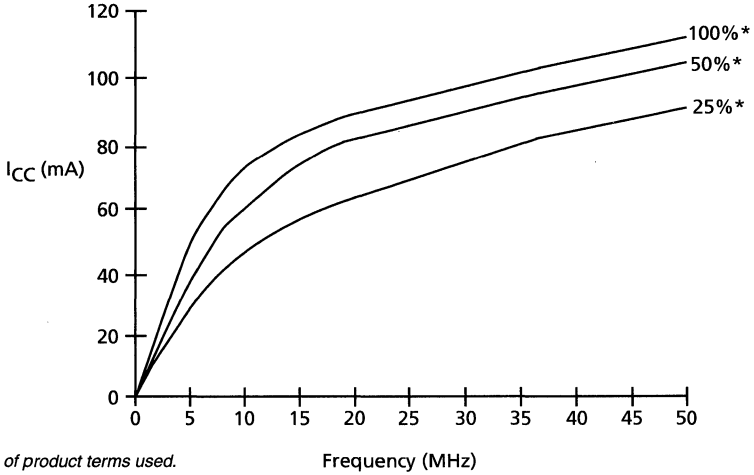


*Percent of product terms used.

16564E-016

I_{CC} vs. Frequency Graph for the PALCE22V10Z-15

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE22V10Z-25
V_{CC} = 5.0 V, T_A = 25°C



*Percent of product terms used.

16564E-017

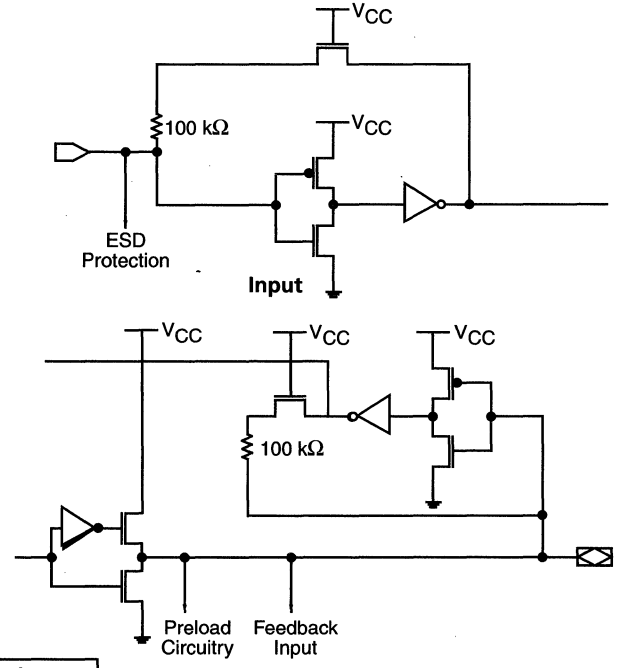
I_{CC} vs. Frequency Graph for the PALCE22V10Z-25

ENDURANCE CHARACTERISTICS

The PALCE22V10 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR SELECTED /4 DEVICES*



16564E-018

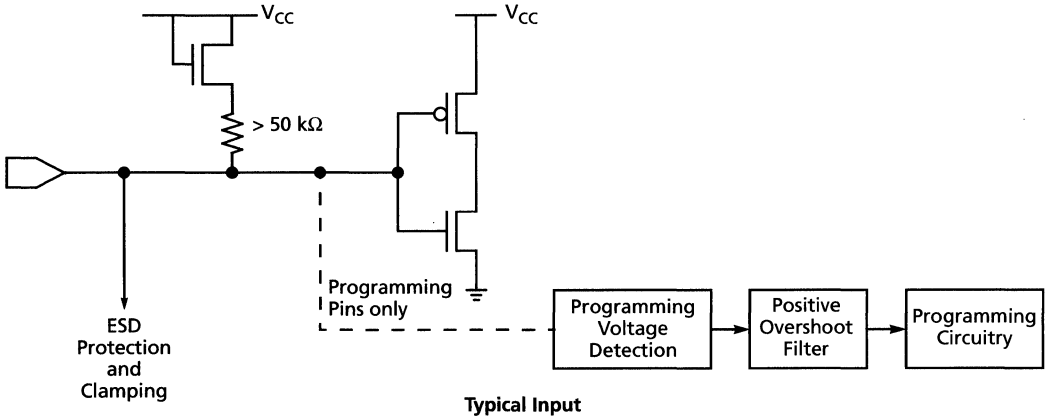
*

Device	Rev Letter
PALCE22V10H-15	H
PALCE22V10H-20H	
PALCE22V10H-25	
PALCE22V10Q-25I	I

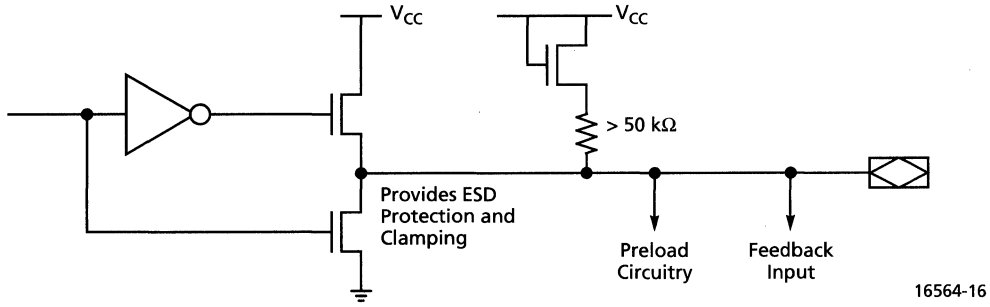
ROBUSTNESS FEATURES

The PALCE22V10X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 version.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION DEVICES

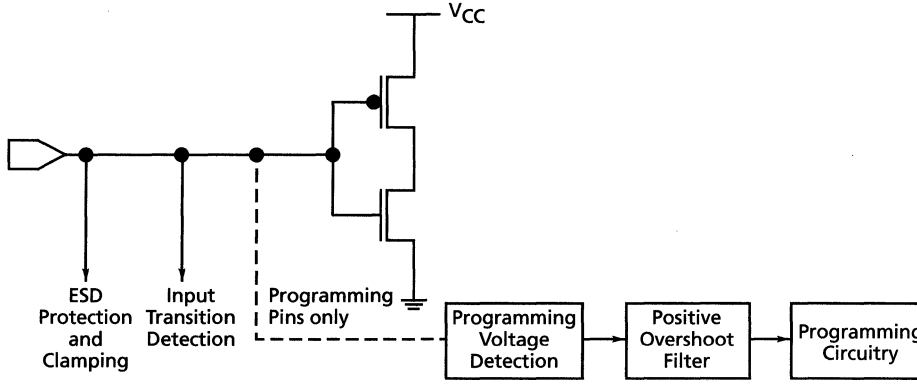


Typical Input

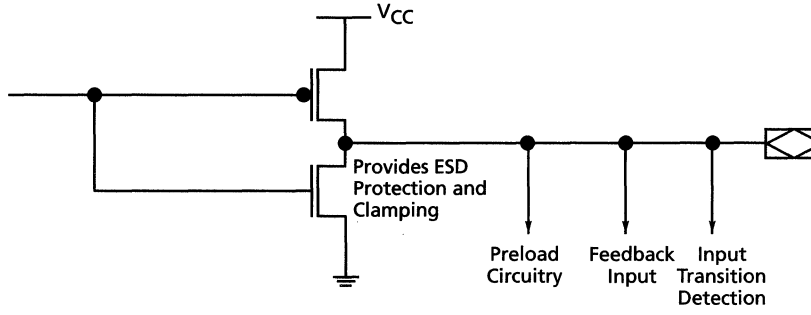


Typical Output

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR PALCE22V10Z



Typical Input



Typical Output

16564E-020

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

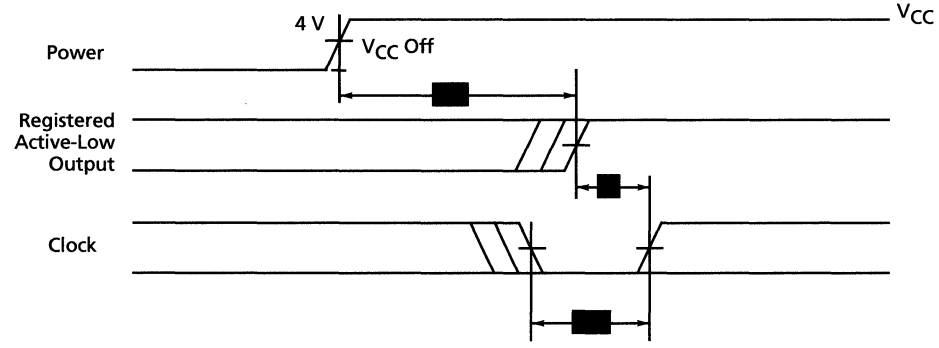


Figure 3. Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

PALCE22V10

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNY DIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		20	18	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	66	48	°C/W
		400 lfpm air	61	43	°C/W
		600 lfpm air	55	40	°C/W
		800 lfpm air	52	37	°C/W

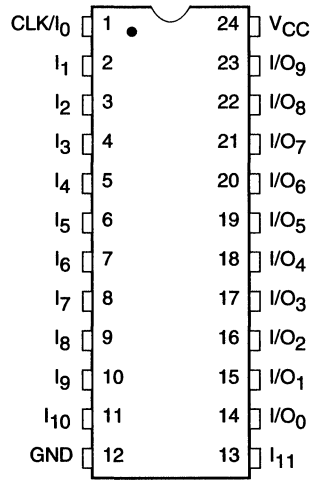
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

CONNECTION DIAGRAMS

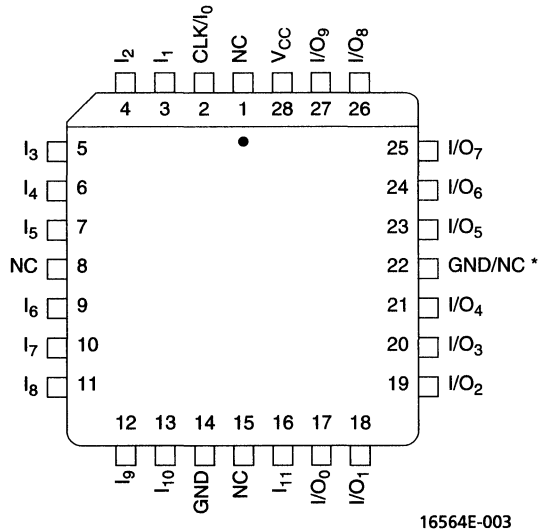
Top View

SKINNYDIP/SOIC



16564E-002

PLCC



16564E-003

**For -5, this pin must be grounded for guaranteed data sheet performance. If not grounded, AC timing may degrade by about 10%.*

Note:
Pin 1 is marked for orientation.

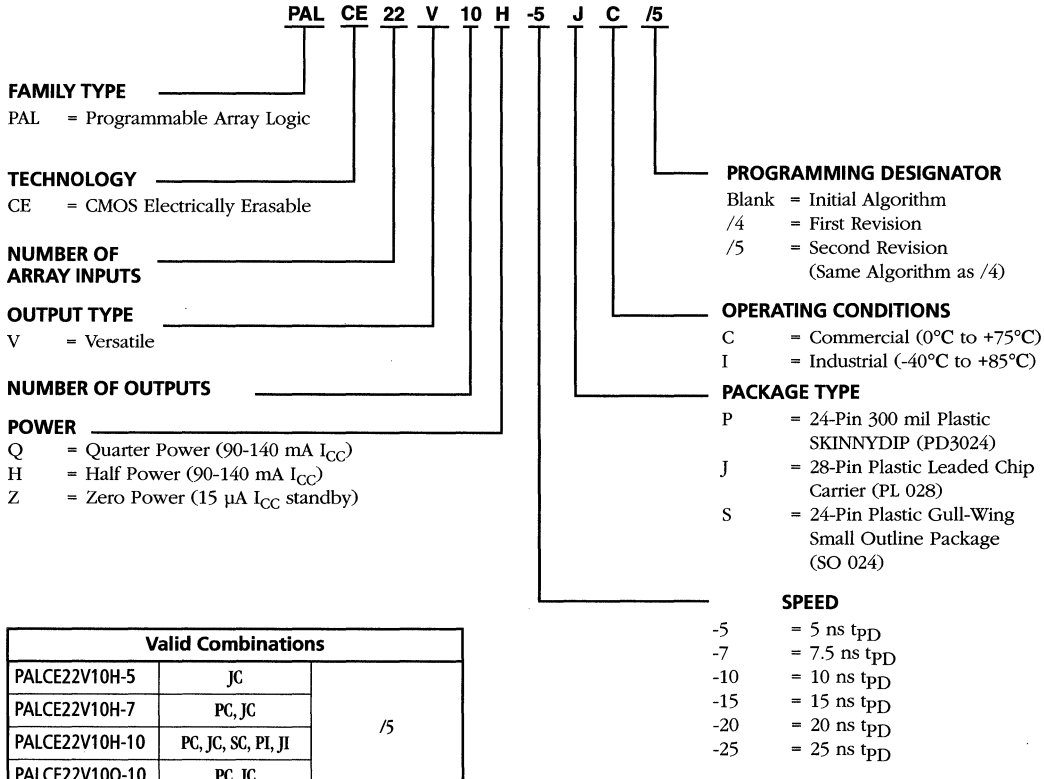
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10H-5	JC	/5
PALCE22V10H-7	PC, JC	
PALCE22V10H-10	PC, JC, SC, PI, JI	
PALCE22V10Q-10	PC, JC	
PALCE22V10H-15	PC, JC, PI, JI, SC	/4
PALCE22V10Q-15	PC, JC	/5
PALCE22V10H-20	PI, JI	/4
PALCE22V10H-25	PC, JC, SC, PI, JI	/4
PALCE22V10Q-25	PC, JC	
PALCE22V10Z-15	PI, JI	
PALCE22V10Z-25	PC, JC, SC, PI, JI, SI	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

VANTIS
BEYOND PERFORMANCE

PALLV22V10 and PALLV22V10Z Families

Low-Voltage (Zero Power) 24-Pin EE CMOS Versatile PAL Device

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  — V_{CC} = + 3.0 V to 3.6 V
- **Commercial and industrial operating temperature range**
- **7.5-ns t_{PD}**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support**
- **24-pin SKINNY DIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALLV22V10 is an advanced PAL® device built with low-voltage, high-speed, electrically-erasable CMOS technology.

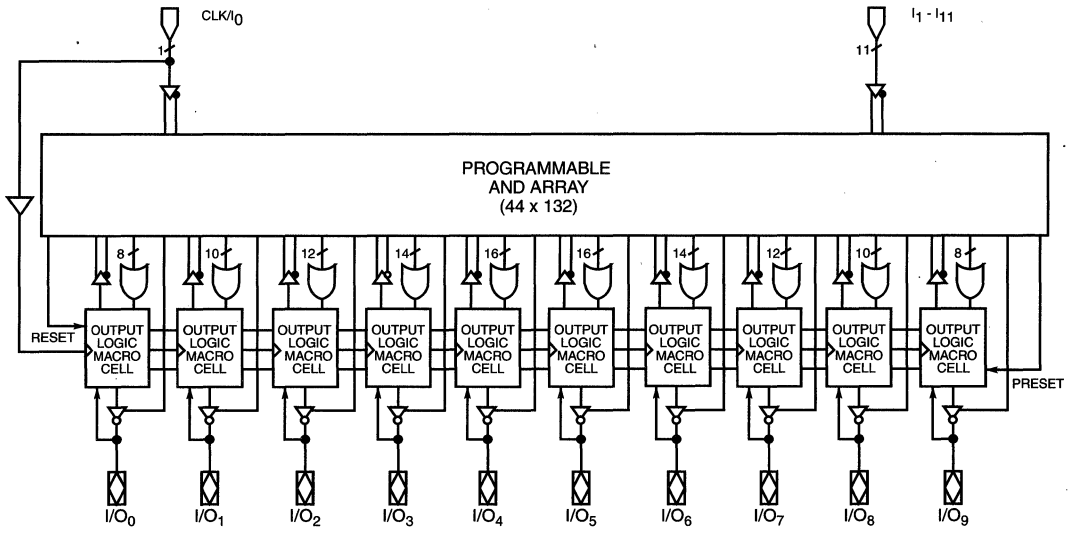
The PALLV22V10Z provides low voltage and zero standby power. At 30 µA maximum standby current, the PALLV22V10Z allows battery powered operation for an extended period.

The PALLV22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

Publication# **18956** Rev: **D**
Amendment/**0** Issue Date: **October 1998**

BLOCK DIAGRAM



18956D-001

FUNCTIONAL DESCRIPTION

The PALLV22V10 is the low-voltage version of the PALCE22V10. It has all the architectural features of the PALCE22V10.

The PALLV2210Z is the low-voltage, zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALLV22V10Z has zero standby power and an unused product term disable feature.

The PALLV22V10 allows the systems engineer to implement a design on-chip by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALLV22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

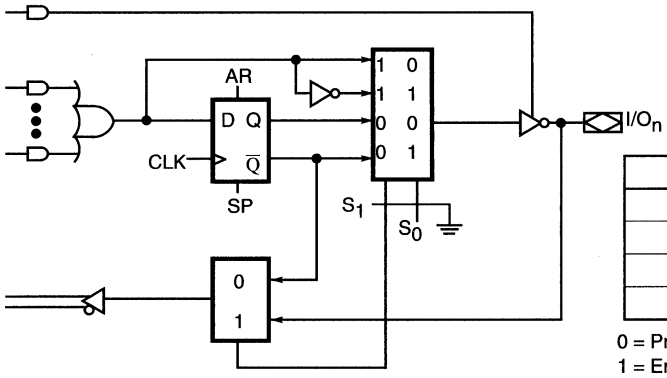
The PALLV22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALLV22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

18956C-004

Figure 1. Output Logic Macrocell Diagram

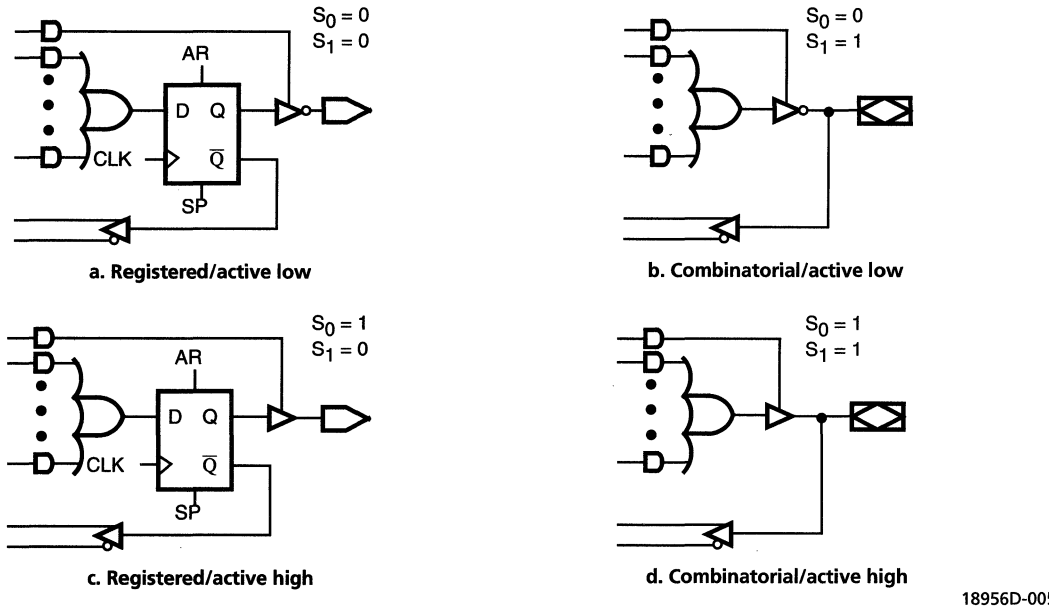


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bi-directional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high (S_0 = 1).

Preset/Reset

For initialization, the PALLV22V10 has additional preset and reset product terms. These terms are connected to all registered outputs. When the synchronous preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Benefits of Lower Operating Voltage

The PALLV22V10 has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3 V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. A lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

3.3-V (CMOS) and 5-V (CMOS and TTL) Compatible Inputs and I/O

Input voltages can be at TTL levels. Additionally, the PALLV22V10 can be driven with true 5-V CMOS levels due to special input and I/O buffer circuitry.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALLV22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic, and the reset delay time is 1000ns maximum.

Register Preload

The registers on the PALLV22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALLV22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALLV22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALLV22V10 offers a very high level of built-in quality. The erasability of the CMOS PALLV22V10 allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALLV22V10 is fabricated with Vantis' advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be 3.3-V and 5-V device compatible. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

Zero-Standby Power Mode

The PALLV22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 30 ns), the PALLV22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} <30 µA). The outputs will maintain the states held before the device went into the standby mode.

If a macrocell is used in registered mode, switching pin CLK/I_0 will not affect standby mode status for that macrocell. If a macrocell is used in combinatorial mode, switching pin CLK/I_0 will affect standby mode status for that macrocell.

This feature reduces dynamic I_{CC} proportionally to the number of registered macrocells used. If all macrocells are used as registers and only CLK/I_0 is switching, the device will not be in standby mode, but dynamic I_{CC} will typically be <2 mA. This is because only the CLK/I_0 buffer will draw current. The use of combinatorial macrocells will add on average 5 mA per macrocell (at 25 MHz) under these same conditions.

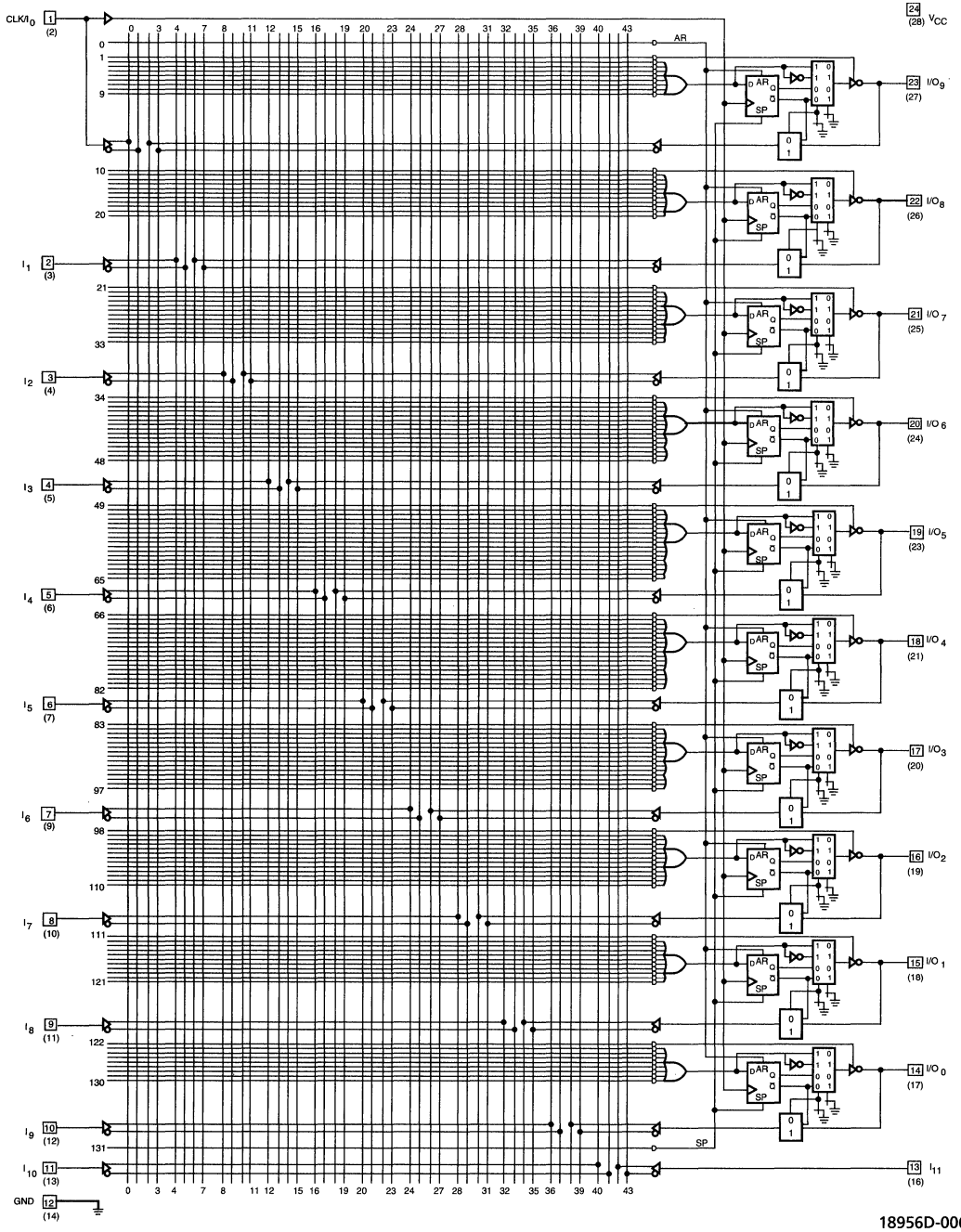
When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies.

Product-Term Disable

On a programmed PALLV22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. Product-term disabling results in considerable power savings. This saving is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in a separate document entitled, *Minimizing Power Consumption with Zero-Power PLDs.*

LOGIC DIAGRAM



18956D-006

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with
Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to +5.25 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to +5.25 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min	I_{OH} = -2 mA	2.4		V
			I_{OH} = -100 µA	V_{CC} -0.2		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA		0.5	V
			I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0	5.25	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			-100	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	mA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-100	mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-5	-75	mA
I_{CC} (Static)	Supply Current	Outputs f = 0 MHz, Open (I_{OUT} = 0 mA)	-10/15 Commercial		60	mA
			-7		75	mA
			-15 Industrial		75	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-7		-10		-15		Unit
				Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				7.5		10		15	ns
t_{S1}	Setup Time from Input, Feedback or SP to Clock			4.5		5.5		10		ns
t_{S2}	Setup Time from SP to Clock			5.5		7		10		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				5.5		6.5		10	ns
t_{AR}	Asynchronous Reset to Registered Output				11		13		20	ns
t_{ARW}	Asynchronous Reset Width			6		8		10		ns
t_{ARR}	Asynchronous Reset Recovery Time			6		8		10		ns
t_{SPR}	Synchronous Preset Recovery Time			6		8		10		ns
t_{WL}	Clock Width	LOW		3.5		4		6		ns
t_{WH}		HIGH		3.5		4		6		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	100		83.3		50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 3)	133		110		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	143		125		83.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control				9		11		15	ns
t_{ER}	Input to Output Disable Using Product Term Control				10		11		15	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with
Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to +5.5 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to +5.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to 85°C). . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground. . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min	I_{OH} = -2 mA	2.4		V
			I_{OH} = -100 µA	V_{CC} -0.3		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-5	-75	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max (Note 4)	f = 0 MHz		30	µA
			f = 15 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed under worst case test conditions. Refer to the I_{CC} vs. Frequency graph in this datasheet for typical I_{CC} characteristics.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

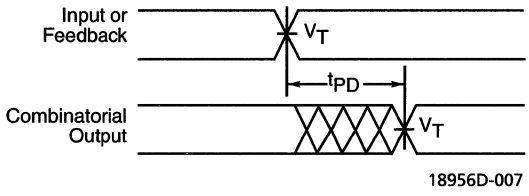
SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-25		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

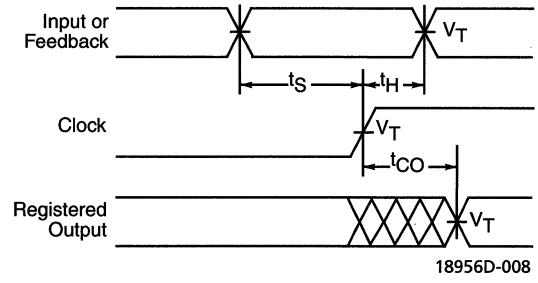
Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} may be slightly faster.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

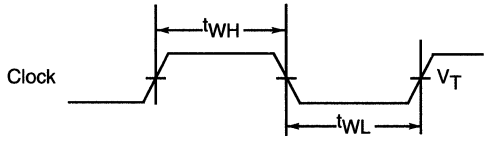
SWITCHING WAVEFORMS



a. Combinatorial output

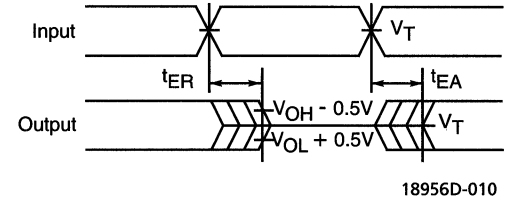


b. Registered output

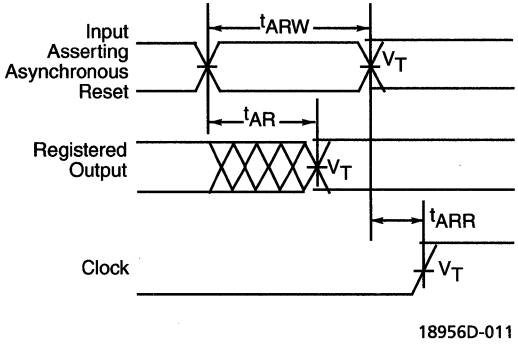


c. Clock width

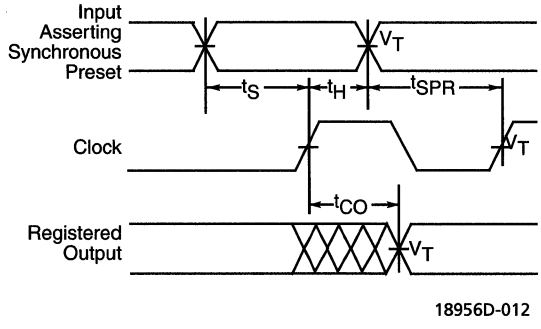
18956D-009



d. Input to output disable/enable



e. Asynchronous reset



f. Synchronous preset

Notes:

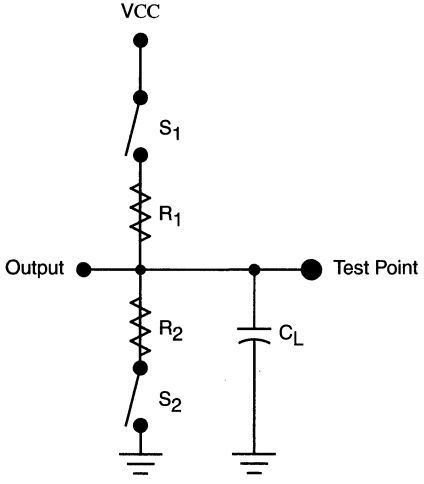
1. *V_T = 1.5 V for inputs signals and $V_{CC}/2$ for outputs signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

18956D-013

SWITCHING TEST CIRCUIT

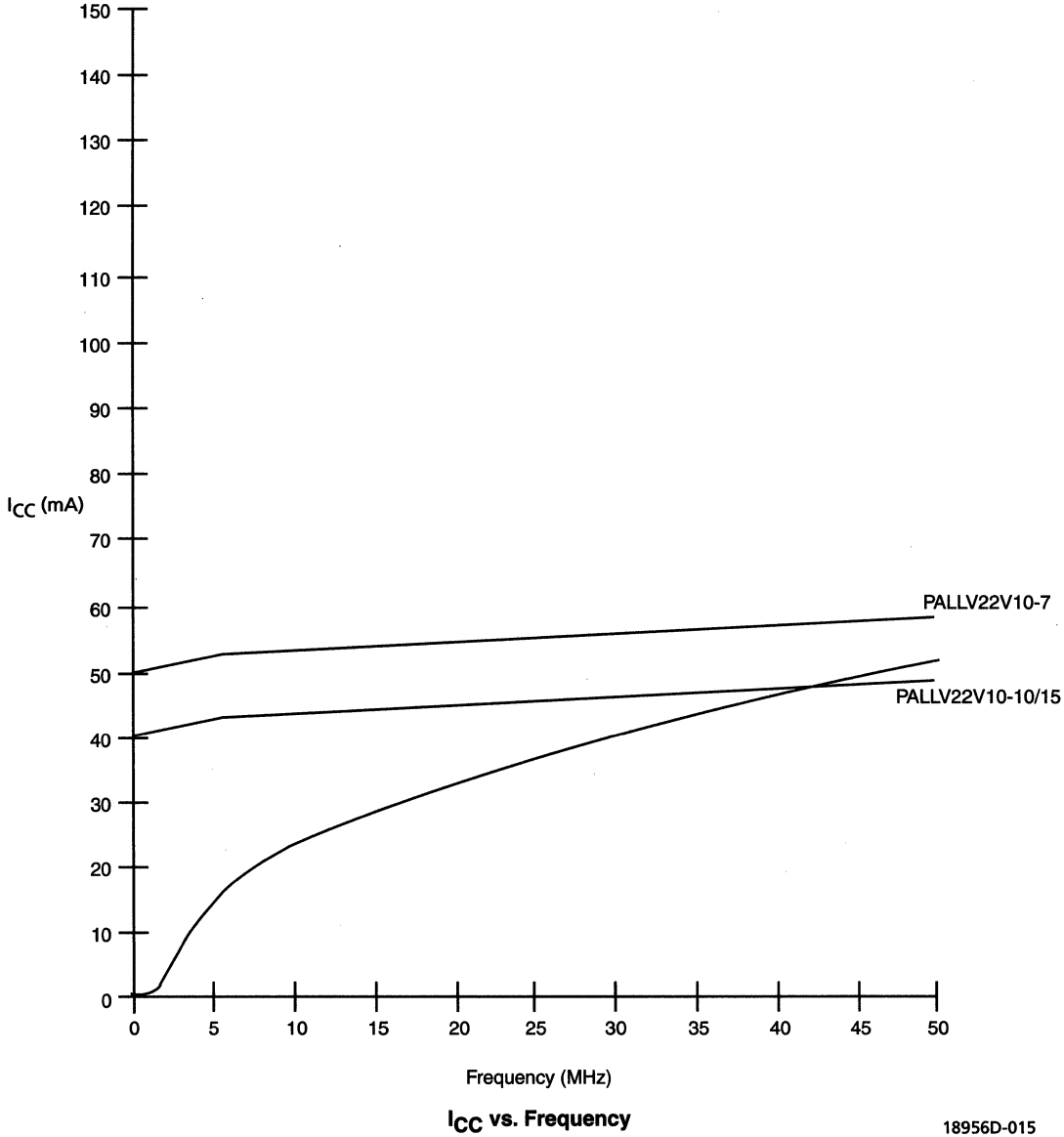


18956D-014

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K Ω	1.6K Ω	$V_{CC}/2$
t_{EA}	Z → H: Open Z →L: Closed	Z → H: Closed Z →L: Open				$V_{CC}/2$
t_{ER}	H →Z: Closed L →Z: Closed	H → Z: Closed L →Z: Open	5 pF			H → Z: V_{OH} - 0.5 V L →Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



I_{CC} vs. Frequency

18956D-015

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

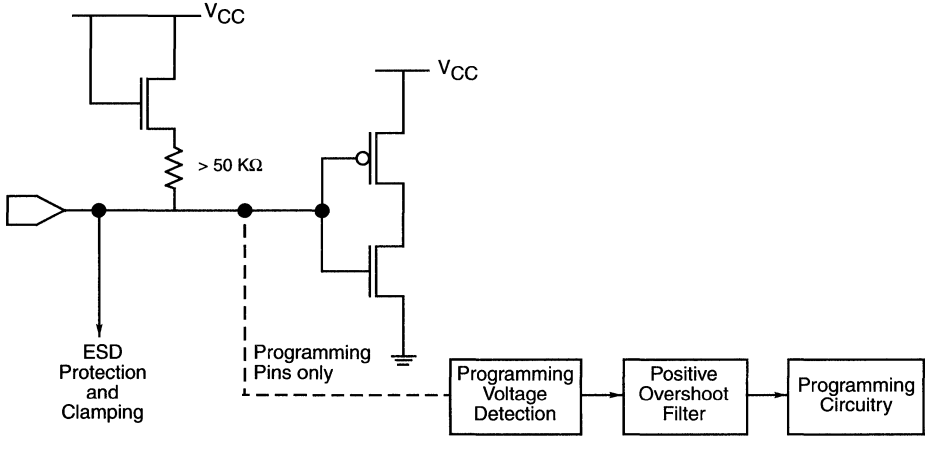
The PALLV22V10 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

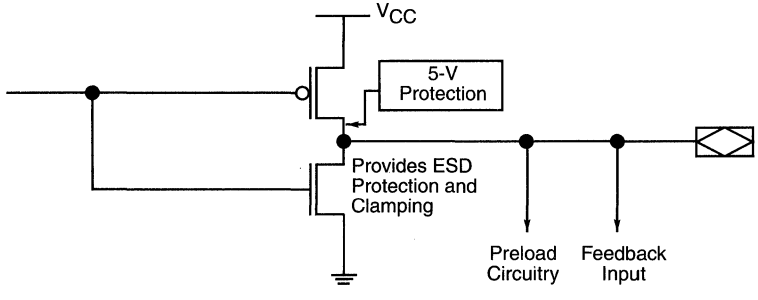
ROBUSTNESS FEATURES

The PALLV22V10 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

18956D-017

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

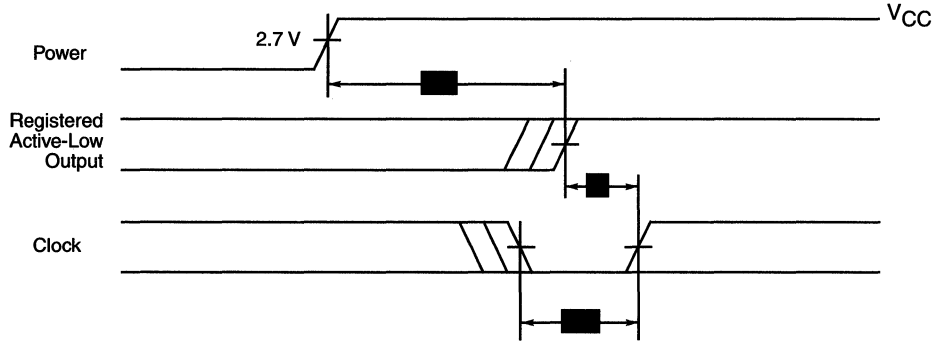


Figure 3. Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

PALLV22V10-10

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNY DIP	PLCC	
θjc	Thermal impedance, junction to case		26	20	°C/W
θja	Thermal impedance, junction to ambient		86	69	°C/W
θjma	Thermal impedance, junction to ambient with air flow	200 lfpm air	72	57	°C/W
		400 lfpm air	65	52	°C/W
		600 lfpm air	60	47	°C/W
		800 lfpm air	55	45	°C/W

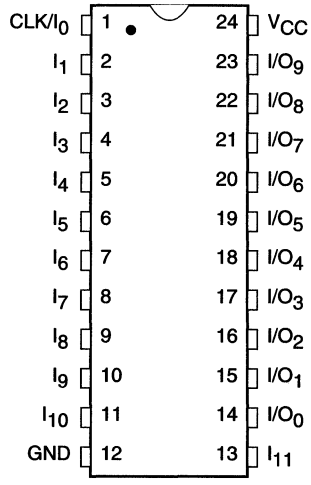
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

CONNECTION DIAGRAMS

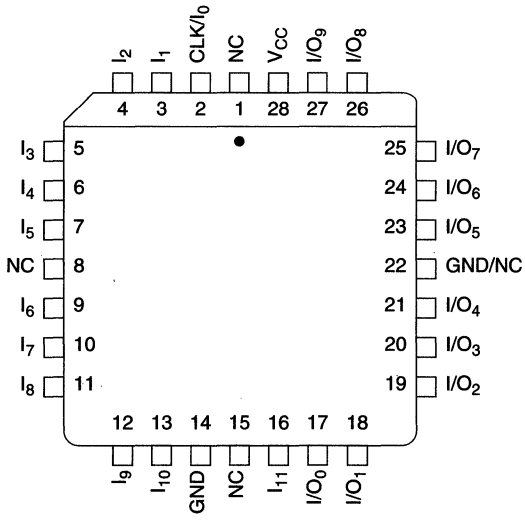
Top View

SKINNY DIP



18956D-002

PLCC



18956D-003

Note:
Pin 1 is marked for orientation.

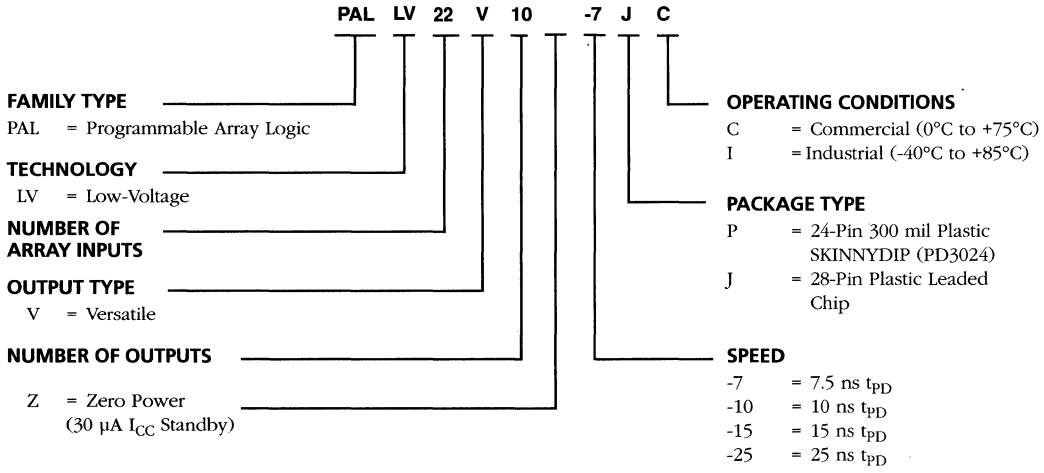
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALLV22V10-7	JC
PALLV22V10-10	PC, JC
PALLV22V10-15	PC, JC, JI
PALLV22V10Z-25	PI, JI

Valid Combinations

The Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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General Information

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f_{MAX} Theory and Calculations

INTRODUCTION

The f_{MAX} parameter is the maximum clock rate at which a device is guaranteed to operate. f_{MAX} is commonly referred to as the maximum operating frequency and can be thought of as the longest register-to-register time in a design. Due to the inherent flexibility of programmable logic devices, the maximum operating frequency calculation can vary. There are four different ways to calculate f_{MAX} in a design. In the discussion that follows, each one of the basic f_{MAX} calculations is examined, including a general description of the f_{MAX} design type and a detailed discussion of the f_{MAX} calculation.

F_{MAX} DESIGN TYPES

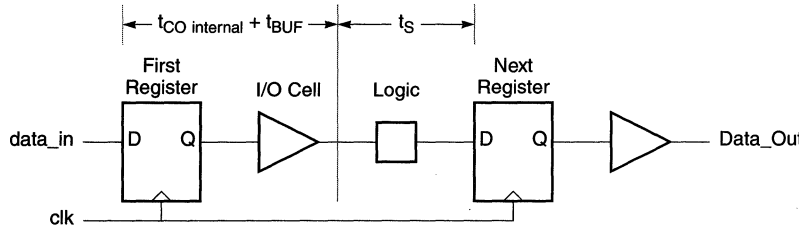
Type 1: External Feedback Timing Path

The first type of f_{MAX} design involves a signal path between two registers that is sent through the I/O cell and fed back into a register inside the part (or fed into a register on another chip). Figure 1a represents the MACH® device specification for f_{MAX} using an external data path. The period of the external feedback timing path is the sum of the setup time and the global clock to external output time. The reciprocal of this time is f_{MAX} and is calculated as:

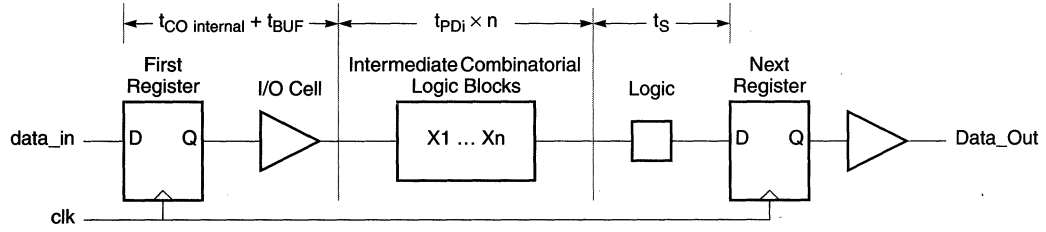
$$f_{MAX(External)} = \frac{1}{t_{COi} + t_{BUF} + t_S}$$

where t_S is the setup time, t_{COi} is the clock-to-feedback time for the flip flop, and t_{BUF} is the time from feedback through the I/O cell.

Publication# **AN004-1** Rev: **A**
Amendment/**0** Issue Date: **November 1998**



a. MACH Device f_{MAX} using an external feedback timing path AN004-001



b. f_{MAX} for a MACH design using an external feedback timing path and n number of intermediate combinatorial logic blocks AN004-002

Figure 1. External Feedback Timing Path

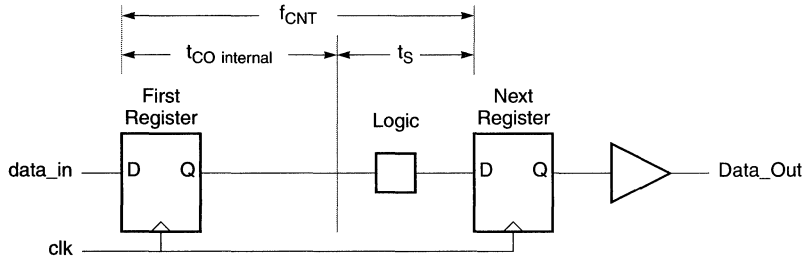
Figure 1b represents a typical design scenario involving an external feedback timing path and demonstrates how f_{MAX} is calculated in a design using intermediate combinatorial logic blocks. In Figure 1b, some intermediate combinatorial logic has been internally added between the registers. The addition of the intermediate logic causes the signal path to slow down by a factor of ($t_{PDi} \times n$), where n represents the number of combinatorial logic blocks between two registers. In this case, a combinatorial logic block is made up of all the product terms going through the logic array and macrocell only once. In the Figure 1b case, the longest timing path is the sum of the clock-to-output time of the register, delay through the I/O buffer, combinatorial propagation time, and the setup time. f_{MAX} is calculated by inverting the longest timing and becomes:

$$f_{MAX} = \frac{1}{t_{COi} + t_{BUF} + t_S + (t_{PDi} \times n)}$$

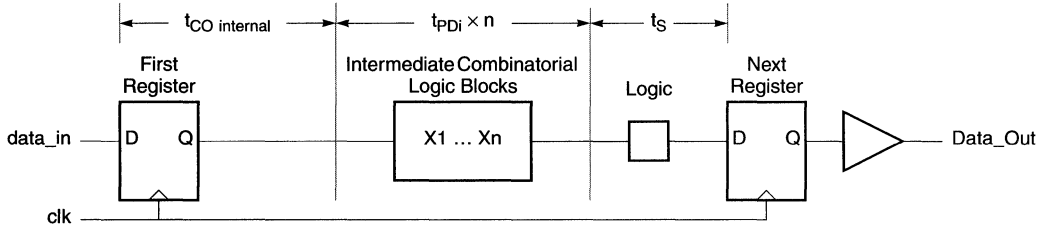
Type 2: Internal Feedback Path

In the second design, f_{MAX} is calculated for timing paths that use internal feedback. These paths do not go through the output buffer, but rather, they leave the macrocell and are sent back directly into the input or central switch matrix. In the case of internal feedback signals, f_{MAX} is calculated by using the t_{COi} timing parameter without t_{BUF}. In the circuit shown in Figure 2a, f_{MAX} is equal to f_{CNT}. The f_{CNT} parameter of Figure 2a is:

$$f_{MAX(Internal)} = \frac{1}{t_{COi} + t_S}$$



a. MACH device f_{MAX} using an internal feedback timing path AN004-003



b. f_{MAX} for a MACH design using an internal feedback timing path and n number of intermediate combinatorial logic blocks AN004-004

Figure 2. Internal Feedback Timing Path

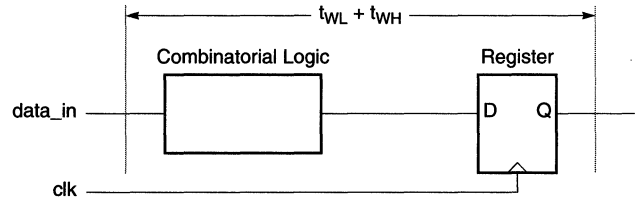
The design in Figure 2b is similar to Figure 1b in that intermediate, combinatorial logic blocks have been added between registers and consequently, f_{MAX} does not equal f_{CNT}. The difference is that the feedback for the timing path is internal and does not include t_{BUF}. In Figure 2b, f_{MAX} is calculated as:

$$f_{MAX} = \frac{1}{t_{COi} + t_S + (t_{PDi} \times n)}$$

Type 3: Registered Data Path with No Feedback

The third way f_{MAX} is calculated involves circuits using no feedback data paths. Figure 3 is an example of a design involving one register and no feedback data path. In this case, the input data is presented to the flip-flop and clocked through. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). This means that the clock period must be greater than or equal to the sum of the data setup and data hold times (clock period $\geq t_S + t_H$). In this instance, the maximum clock frequency, f_{MAX}, is determined by the duty cycle requirements for the clock (t_{WL} and t_{WH}). Therefore, the slowest time that the data path of Figure 3 can take is the clock period, and as a result, f_{MAX} is calculated as:

$$f_{MAX(No\ Feedback)} = \frac{1}{t_{WL} + t_{WH}}$$



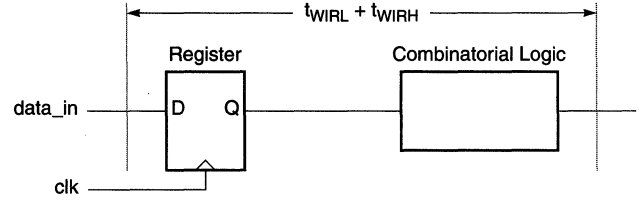
AN004-005

Figure 3. Registered Data Path with No Feedback

Type 4: Input Registered Data Path with No Feedback

The final f_{MAX} is calculated from a design using an input register. This is very similar to the previous type of f_{MAX} calculation. The minimum period will again be limited by the sum of the clock widths, which is $t_{WIRL} + t_{WIRH}$. In this situation, f_{MAX} is calculated as:

$$f_{MAX(IR)} = \frac{1}{t_{WIRL} + t_{WIRH}}$$

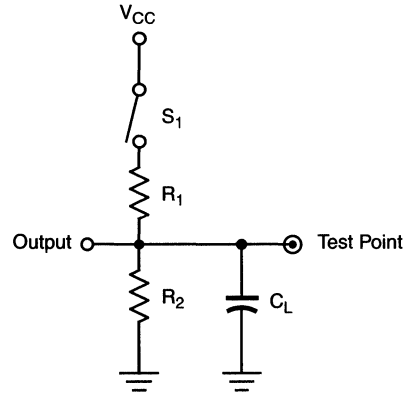


AN004-006

Figure 4. Input Registered Data Path with No Feedback

Switching Test Circuit

SWITCHING TEST CIRCUIT



Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF (30 pF)	300 Ω (1.6 KΩ)	390 Ω (1.6 KΩ)	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Notes:

1. *Values in parentheses are for 3.3-V devices.*
2. *Measurements are taken at minimum V_{CC} with no more than 4 blocks loading and no more than 4 I/Os switching with a maximum Commercial junction temperature of 100 °C, or Industrial junction temperature of 115 °C.*

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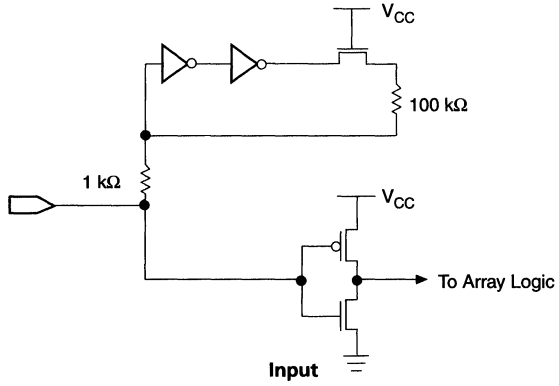
Endurance Characteristics

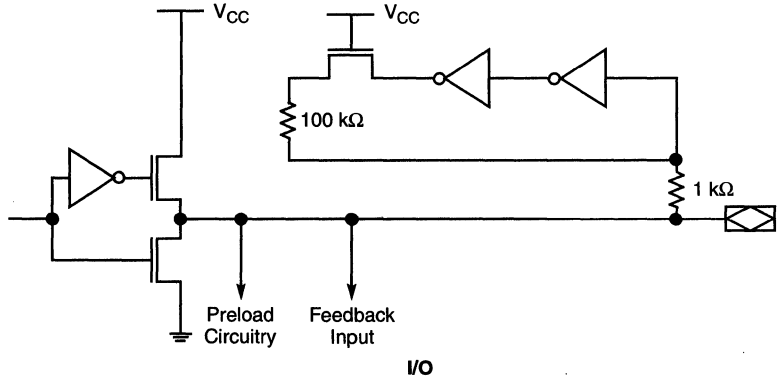
The MACH® families are manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Parameter Symbol	Parameter Description	Value	Unit	Test Conditions
t_{DR}	Min Pattern Data Retention Time	20	Years	Max Operating Temperature
		10	Years	Max Storage Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



19671B-001



19671B-002

Figure 1. Bus-Friendly™ Latch

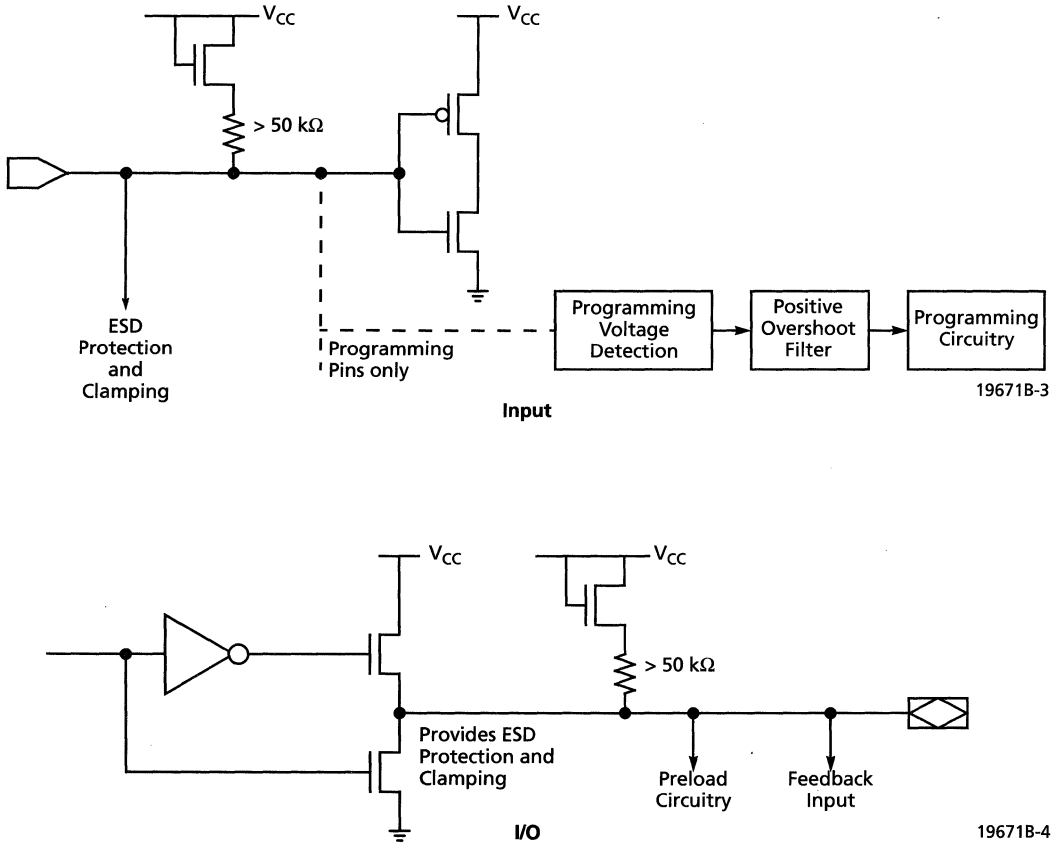


Figure 2. Pull-up Resistor

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Power-Up Reset

MACH® devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic from ground.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		
V_{PWR}	Power-up Voltage for 3.3V Devices	2.7	V
	Power-Up Voltage for 5V Devices	4	V

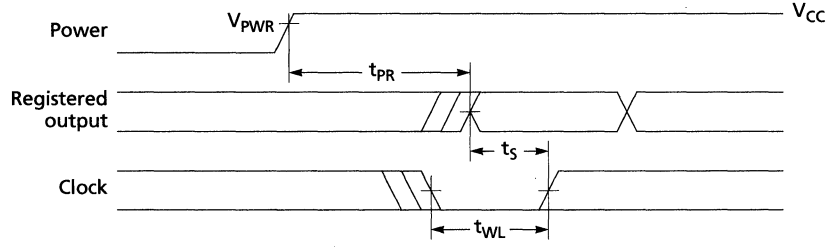


Figure 1. Power-Up Reset Waveform

LATCH-UP CIRCUIT

Latch-up is caused by an SCR (Silicon Controlled Rectifier) circuit. Fabrication of CMOS integrated circuits with bulk silicon processing creates a parasitic SCR structure. The behavior of this SCR is similar in principle to a true SCR. These structures result from the multiple diffusions needed for the formation of complementary MOS transistors in CMOS processing. The SCR structure consists of a four-layer device formed by diffused PNPN regions. These four layers create parasitic bipolar transistors illustrated in Figure 1.

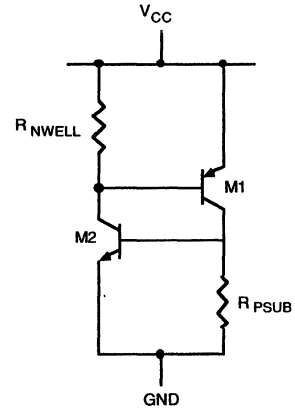
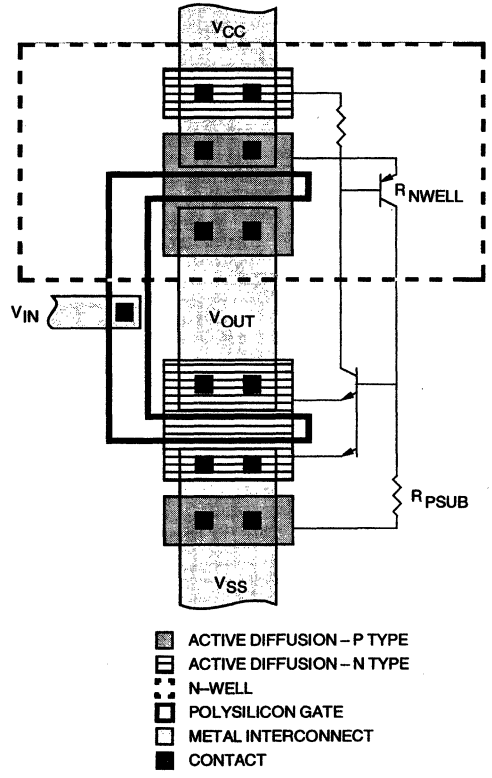


Figure 1. Parasitic Bipolar Transistors 14105C-001

Figure 2 shows a typical CMOS inverter layout with the schematic of the parasitic bipolar SCR structure. Figure 3 is a cross-sectional representation of the CMOS inverter, again with the schematic of the bipolar SCR structure.

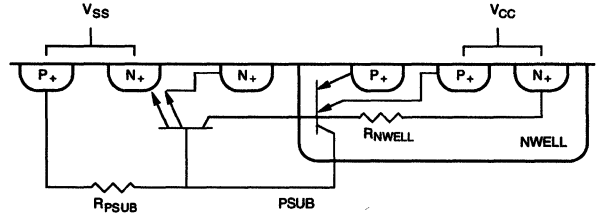
Any CMOS diffusion can become part of the parasitic SCR structure, since all of these parts are interconnected through the bulk silicon substrate resistance. Other parasitic resistors shown result from doped regions of the semiconductor. The magnitude to which the resistors resist current flow depends upon geometric size and doping level.

As illustrated in Figure 1, the complementary PNP and NPN transistors are cross-coupled, having common base-collector regions. The vertical PNP device, M1, has its base composed of the N-well diffusion, while the emitter and collector are formed from P-type source-drain and substrate regions, respectively. The lateral bipolar transistor, M2, base is the P substrate with emitter and collector junctions formed from N-type source-drain and N-well diffusions, respectively.



14105C-002

Figure 2. Typical CMOS Inverter Layout



14105C-003

Figure 3. Cross Section of CMOS Inverter

Latch-Up Conditions

Under normal bias conditions, the SCR conducts only leakage current, and the SCR structure is in the blocking state. However, as current flows across any of the parasitic resistors, a voltage drop is developed, turning on the parasitic bipolar base-emitter junction. The forward bias condition of this junction allows collector current to flow in the bipolar transistor. This collector current flows across the base-emitter resistor of the complementary bipolar transistor, creating a voltage sufficient to turn on the transistor.

A regenerative loop is now created between the complementary bipolar transistors such that current conduction becomes self-sustaining. Even after removal of the stimulus that triggered this action, the current conduction can continue. This region of operation is a high-current, low-resistance condition characteristic of a four-layer PNPN structure. This is referred to as latch-up. Once initiated, the excessive latch-up current can permanently damage an integrated circuit by fusing metal lines or destroying junctions.

CAUSES OF LATCH-UP

Latch-up may be initiated in numerous ways. Only the critical causes frequently encountered in a system environment will be discussed. These include power-up, supply overvoltage, and overshoot/undershoot at device pins.

Power-Up

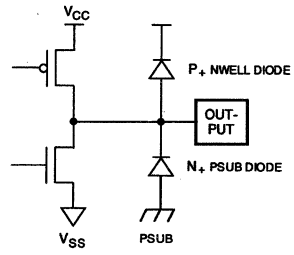
Caution must be exercised when powering up most CMOS ICs to avoid driving device pins before the supply voltage has been applied to the circuit. Placing a device or board in a "hot socket" will create this situation. When subjected to hot-socket insertion, voltage conditions at the device pins are uncertain such that the input diodes may be forward biased. Forward biasing the input diodes with a delayed or uncontrolled application of V_{CC} could cause the device to latch up. Some of Vantis' CMOS circuits have substantial immunity to hot socket power-up, but since this condition is uncertain and difficult to characterize, test, and guarantee, it should be avoided. Vantis' MACH®4 and MACH 5 devices have been designed to be hot socketable and will not latch up.

Supply Overvoltage

Supply levels exceeding the absolute maximum rating can cause a CMOS circuit to latch up. Elevated supply voltage may cause internal junctions to break down, producing substrate current capable of triggering latch-up. Latch-up is one of the reasons overvoltage should be avoided; other undesirable effects may result from this.

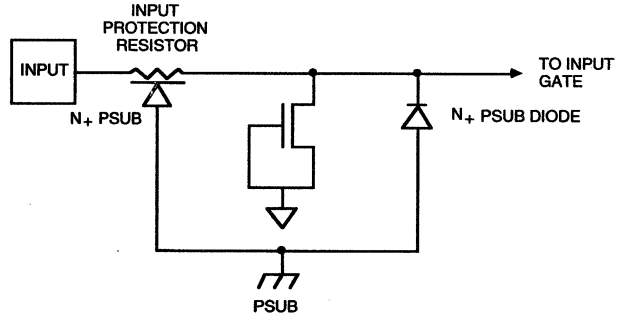
Overshoot/Undershoot

Generally, the I/O pins experience the noisiest electrical environment. Fast switching signals with a large capacitive load may overshoot, creating a transient forward bias condition at the I/O junction. These junction diodes are illustrated in Figures 4 and 5. Typically, this is where latch-up is most likely to be induced. Proper design of the input and output buffers is essential to minimize the risk of latch-up due to overshoot.



14105C-004

Figure 4. Junction Diode



14105C-005

Figure 5. Junction Diode

TESTING FOR LATCH-UP

Vantis characterizes the latch-up sensitivity of its devices before they are released to the market. Testing is done in such a way as to completely cover every possible latch-up condition, including V_{CC} overvoltage, pin overcurrent, and pin overvoltage.

V_{CC} Overvoltage Test

The V_{CC} overvoltage test is applied to all power (V_{CC}) pins. The test is performed at the highest guaranteed operating temperature of the device. All inputs and I/Os acting as inputs are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open).

V_{CC} max is applied to the V_{CC} pin. A positive high voltage pulse is then applied to the V_{CC} pin and returned to V_{CC} max. The occurrence of latch-up is detected if the voltage across the device is less than V_{CC} max, and the current through the device is greater than the normal DC operating current.

Pin Overcurrent Test

The pin overcurrent test is performed on every output, I/O pin, and non-current-limited input pin. Non-current-limited inputs are inputs which present a diode-like (or otherwise "infinite") current characteristic for input voltages in the range $(GND - V_{CC(TYP)}) < V_{IN} < (2 \times V_{CC(TYP)})$.

The pin overcurrent test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs should be floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. A three-state output under test should be disabled. A non-three-state output type under test should be a logic High when applying a positive current and a logic Low when applying a negative current. An I/O pin should be placed into the input mode.

A high current pulse is then applied to the pin under test. The magnitude of the pulse is stepped until latch-up is induced. Both positive and negative currents are tested. Latch-up is observed as described previously. The sensitivity of the device is the worst case sensitivity found on any pin of the device.

Pin Overvoltage Test

The pin overvoltage test is performed on current-limited inputs. Current-limited inputs are inputs which present a resistor-like (or otherwise "limited") current characteristic for input voltages in the range $(GND - V_{CC(TYP)}) < V_{IN} < (2 \times V_{CC(TYP)})$.

The pin overvoltage test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. Both positive and negative voltage pulses are applied to the pin under test. Latch-up is observed as described previously. The sensitivity of the device is the worst-case sensitivity found on any pin of the device.

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Ground Bounce

INTRODUCTION

The development of fast PLDs has increased the importance of analog considerations the digital designer has been able to overlook in the past. One of these is ground bounce. Ground bounce refers to the ringing on an output signal when one or more outputs on the same device are being switched from HIGH to LOW. This ringing can be in excess of 3 V. The system cannot consider the data valid until the ringing settles to below the V_{IL} of the receiving devices. The ringing in a fast device can last so long that a slower device with less ground bounce could actually be a faster solution.

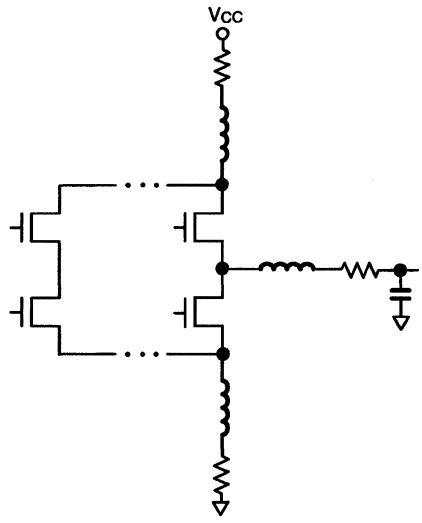
The phenomenon of ground bounce is associated with the inductance and resistance of the ground connection in the integrated circuit. As there is always some inductance and resistance, ground bounce cannot be totally eliminated; however, it can be reduced to a level tolerable to the system.

This article will discuss the mechanism of ground bounce in CMOS circuitry and the utilization of slew-rate control used by Vantis to minimize ground bounce to reasonable limits.

MECHANISM

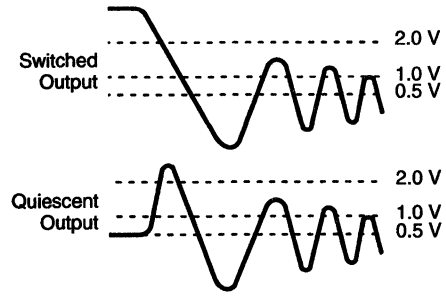
Figure 1 shows a schematic of an output driver and load including parasitic elements. The load capacitor is charged to the HIGH-level voltage. When the transistor turns on, the capacitor discharges into the transistor and lead impedance. The resultant RLC circuit will have a damped ringing (Figure 2). The peak amplitude depends on the edge rate of the switch and the RLC values, while the frequency of the ringing and the rate of decay depend only on the RLC values.

Publication# **13090** Rev: **C**
Amendment/**0** Issue Date: **November 1998**



13090C-001

Figure 1. Simplified Schematic of an Output Driver

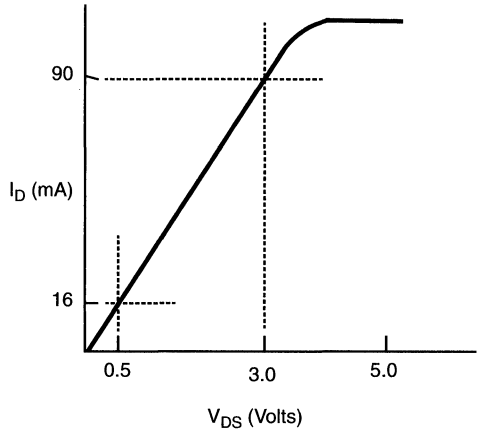


13090C-002

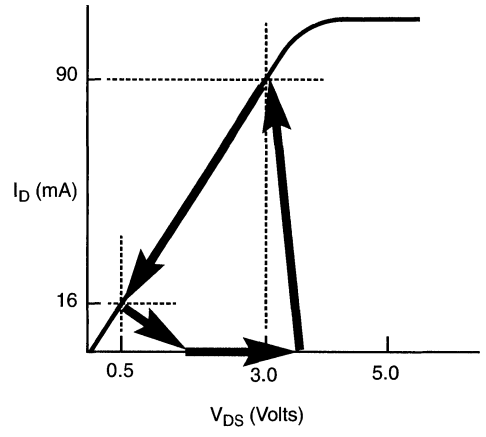
Figure 2. Ground Bounce

The ringing caused by a single output switching is normally below the LOW-threshold voltage. However, the voltage at the ground pad of the device is proportional to the number of outputs switching simultaneously. In addition, the voltage at the ground pad is coupled to any LOW output through its output transistor. Therefore, if enough outputs switch, ringing on the ground pad will be coupled to LOW outputs, causing the detection of false HIGHs.

Most PLDs used today have relatively low output drive current: 16 mA or 24 mA. It is tempting to think that the low current level will somehow limit the switching energy and therefore ground bounce. Actually, even a low-power transistor can pass a relatively large current. The transistor I-V curve in Figure 3a shows that a MOS transistor designed for 16 mA at 0.5 V will pass 90 mA at 3.0 V. Figure 3b shows the V/I path when the output transistor switches between HIGH and LOW. Notice that the transistor switches from 3.5 V at 0 mA to 3.0 V at 90 mA. If eight outputs were to switch simultaneously, 90 mA x 8, or 720 mA, would flow through the ground lead.



a. The DC curve of an output driver transistor



b. The path followed as the transistor switches between the HIGH and LOW levels

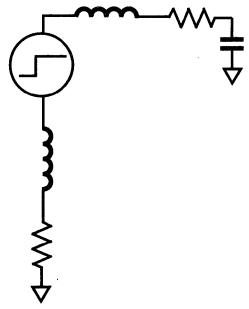
Figure 3. I-V Curves

This sudden current surge is actually self-limiting. As the ground-pad voltage rises due to the high current change, the internal V_{DS} and the available gate bias voltage are reduced, lowering the drive current. However, the ringing can still exceed 3 V.

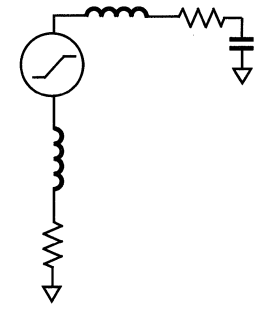
CONTROLLED EDGE RATE

The parameters that influence ground bounce are the inductances and resistances of the device, the capacitance of the load, and the edge rate. Of these, the only one that the chip manufacturer can directly control is the edge rate.

Turning on the output-driver transistor is equivalent to switching the charged load capacitor to ground. This can be represented by a step-voltage source in series with the capacitor (Figure 4a). Slowing down the rate that the output transistor can turn on changes the voltage source from a step to a ramp (Figure 4b). With a shallower slope, less energy is available for ringing, and the ground bounce amplitude is reduced.



a. Equivalent circuit of an output driver transistor with a capacitive load



b. Output driver circuit with slew-rate limiting

Figure 4. Schematic Circuitry

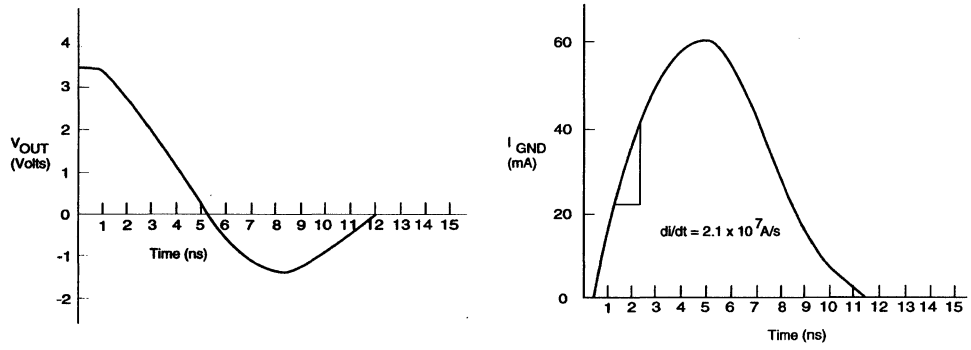
A SPICE simulation (Figure 5) illustrates the effect. The device without risetime control will have a very high charging current with a large di/dt: 2.1 x 10^7 A/s. Risetime control reduces the di/dt about 25%. This will result in a corresponding reduction in the voltage that can develop across the ground inductance.

Vantis has a proprietary technique that slows the edge rate of the output transistor, thereby reducing the amplitude of the ringing. Slowing down the fall time will add approximately one nanosecond to the output delay, but the system speed will still be greatly increased. On a high-capacitance load, a non-edge-rate-controlled device could ring for more than 25 ns. The additional delay required to allow for the ringing would be intolerable.

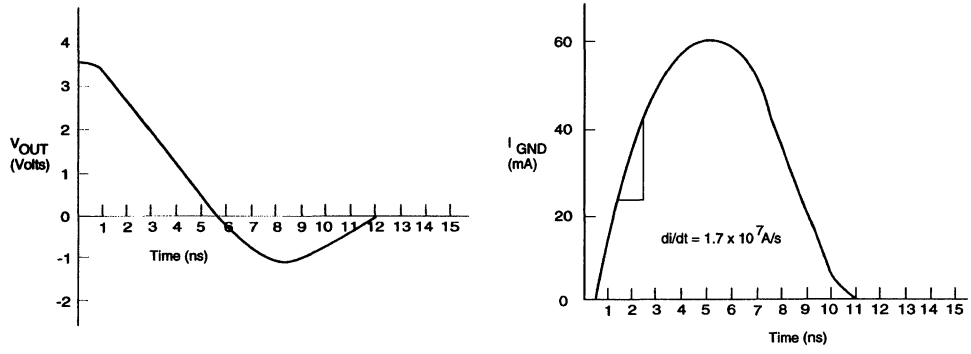
SYSTEM GROUND BOUNCE SOLUTIONS

There are some things that the system designer can do to reduce the ground bounce to a tolerable level.

1. Use Vantis MACH® devices that incorporate edge rate control. This is the first line of defense against ground bounce-related problems, and the most effective.
2. Use shorter lead packages. The bonding wires in a PLCC are 1/4 the length of the ground bonding wire in a DIP. The inductance is reduced proportionally. Any reduction in inductance will reduce the amplitude of the ringing.
3. Reduce capacitive loading. Capacitive loading in any system should be reduced as much as possible. This may involve consideration of the transmission line characteristics of the layout.
4. Limit the number of outputs switching simultaneously. If the load naturally has high-capacitance, such as a bus or memory board would, ground bounce can be reduced by limiting the number of outputs that can switch simultaneously in a single device. Many system designers consider 4 to be an acceptable upper limit.



a. Without risetime control



b. With risetime control

Figure 5. Effect of Risetime Control 13090C-007

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BEYOND PERFORMANCE

Metastability

INTRODUCTION

A significant number of digital systems must deal with inputs not synchronized to their own internal clocks. These asynchronous signals can arise from any of the various asynchronous protocols which are often used in bus designs; they can be the result of trying to share signals from systems with different clocks; or they may be the response of a system user, who is of course not synchronized with the system. The result can be metastability, a problem which can plague unwary designers. It is not a newly discovered phenomenon, but is normally dealt with somewhat qualitatively, and, unfortunately, is usually ignored as much as possible.

CAUSES OF METASTABILITY

The flip-flop setup time is the parameter that is most often at the root of metastability. The setup time is a requirement that data be made available at the input to the flip-flop before the clock signal arrives. The data must not only be there, but must also be stable.

In a PLD, the use of an array for the data adds to the setup time. The data passes through the array on its way to the flip-flop (Figure 1). The clock signal, on the other hand, goes directly from the clock pin to the flip-flop. Its path is much shorter than the data path. The setup time is a requirement that the data signal must be given more time to get to the flip-flop before the clock signal.

If the published setup time is satisfied, the data arrives at the flip-flop well before the clock, and the output to the flip-flop will change as desired (Figure 2). If the setup time is violated, then no guarantee can be made about what the output will do. The output could be normal, since the published setup time is a worst-case number. However, if the timing between the clock and data is just right, the output will be unstable for some time before it settles into some state. Neither the time the output remains unstable nor the final state is predictable (Figure 3). This condition is metastability.

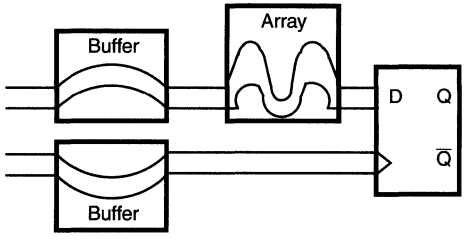

Figure 1. The Clock and Data Paths in a PLD

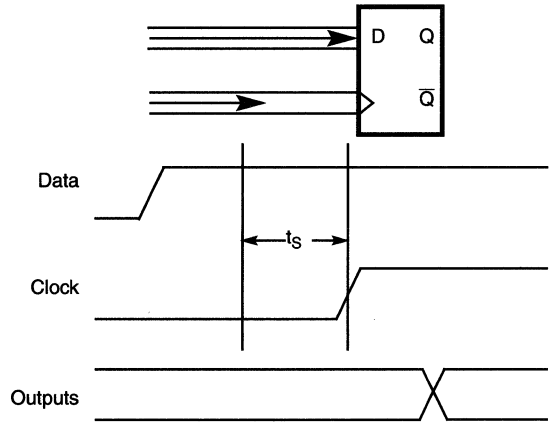

Figure 2. Output Response When the Setup Time Is Satisfied

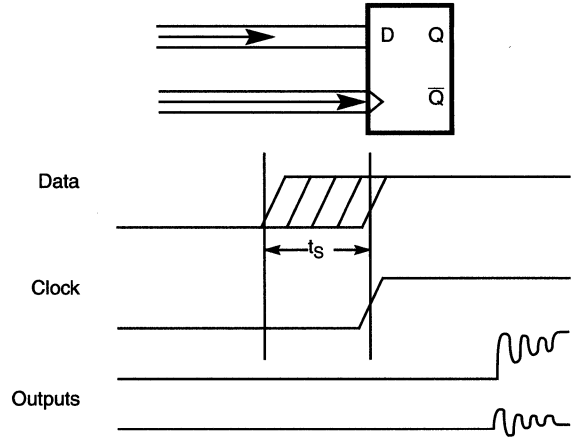

Figure 3. Possible Output Response When the Setup Time Is Violated

SOLUTIONS FOR METASTABILITY

The most common way of dealing with this problem is to synchronize the inputs with an extra flip-flop (Figure 4). If the first flip-flop goes metastable, hopefully the delay between clock pulses will allow the ringing to die down before clocking into the next flip-flop. This improves the chances of having good data in the second flip-flop.

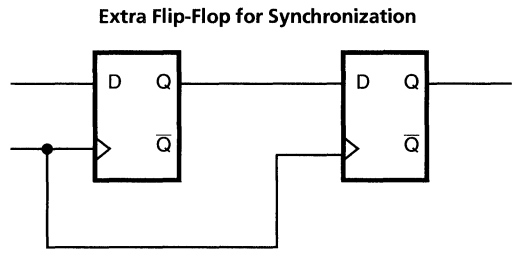

Figure 4. Dual Synchronizer

This method is not without its costs. Each extra stage of flip-flop means an extra clock delay of the data which must be absorbed by the system. Moreover, it is not foolproof. The possibility of metastability is reduced, but not eliminated. A flip-flop can go metastable if the preceding stage does not recover quickly enough.

The best way to avoid metastability is to avoid synchronization when possible. Many applications, such as bus arbitration schemes, use synchronization not because synchronization itself is necessary, but because it provides the only convenient way to store data. This unfortunately takes a system that is inherently asynchronous and adds some synchronizing elements in the middle.

SUMMARY

Metastability can occur in a number of different kinds of asynchronous systems, usually due to the inability to guarantee that the setup time of the flip-flops will be satisfied. In standard synchronous systems where the setup time (along with all other timing requirements) is specifically designed in, metastability will never be a problem.

In some situations, metastability is caused by the need to interface systems with different clocks. In this case, it will never be possible to completely eliminate the possibility of metastability. Instead, the designer must take steps to reduce the probability of a system failure due to metastability.

VANTIS

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Inside Vantis' EE CMOS PLD Technology

TECHNOLOGY DESCRIPTION

The EE CMOS technology used by Vantis in programmable logic is a single-poly, double- or triple-metal process. It has been optimized for high-speed programmable logic devices, which do not have the same density constraints of memory devices. The basic characteristics of the EE process are:

- CMOS
- Grounded substrate
- Single-poly, dual metal or single-poly, triple metal
- Five generations in production: EE4, EE5, EE6.5, EE7, EE8
- 1.3 µm, 0.9 µm, 0.7 µm, 0.45 µm, or 0.35 µm minimum feature
- 0.85 µm, 0.65 µm, 0.5 µm, 0.35 µm, or 0.25 µm gatelength (L_{eff})
- 150 Å or 80 Å gate oxide thickness
- 90 Å tunnel oxide thickness

CMOS PLDs use standard CMOS logic internally, with the addition of a programmable array. The output buffers of most devices are designed to be compatible with TTL circuits, and therefore have n-channel enhancement pull-up transistors.

Vantis' EE CMOS process for programmable logic is simplified by the absence of standard depletion-mode transistors in the more advanced processes. Depletion mode transistors are a vestige of NMOS design, and are not really needed. This results in the elimination of a mask and implant step, reducing the process cost and simplifying the structure.

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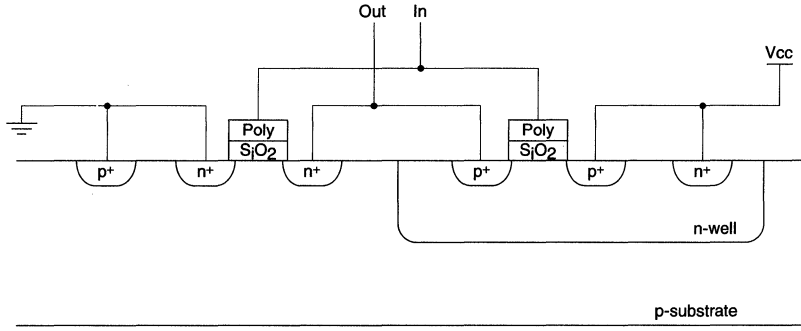
Transistor Cross-Section

Figure 1 shows a cross-section of a basic inverter. This is a very straightforward structure. The gates consist of poly-silicon; the other connections are made with metal.



16507C-001

Figure 1. CMOS Inverter Cross-Section

Erasable Technology

Any erasable CMOS technology is based upon the concept of stored charge. The charge is stored on a transistor with a **floating gate**—that is, a gate that has no connection. The transistor actually has two gates: one that floats, and one that acts as a control gate. The control gate is used to establish the field across the floating gate (see Figure 2).

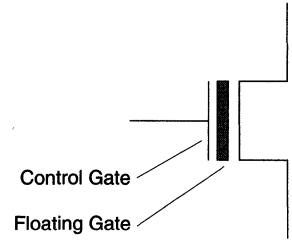


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Figure 2. Floating-Gate MOS Transistor

In the programmed state, there is a net deficit of electrons in the floating gate. The resulting positive charge turns the transistor ON. In the erased state, there are enough electrons on the control gate so that the negative charge turns the transistor OFF.

There are two basic ways of transferring the charge onto the floating gate: a) hot electron injection, and b) tunneling. Electrically erasable devices rely on tunneling.

Electrically-Erasable Technology

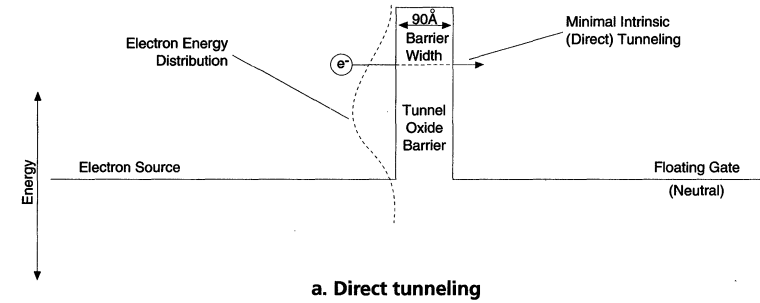
Electrically-erasable devices use **Fowler-Nordheim** tunneling as the mechanism for getting charge onto the floating gate. This is defined roughly as tunneling that occurs as a result of a field placed across the barrier that the electrons tunnel through.

Some amount of **direct** tunneling, or tunneling that occurs without an applied field, is always possible through any energy barrier. It may be extremely small or significant, depending on the width of the barrier. Since tunneling electrons are going through the barrier instead of over it, the height of the barrier does not affect the amount of tunneling.

For an electrically-erasable cell, the tunnel oxide is about one third the thickness of the oxide of a UV-erasable part; therefore, tunneling occurs at relatively low fields. Even so, the field used to cause tunneling is about five times the field used to cause hot-electron injection for UV parts. Note that tunneling is theoretically possible on a UV part using a very high field, and the normal electron injection would swamp out any tunneling that would occur.

Fowler-Nordheim tunneling involves placing a potential across the barrier which distorts the band diagram as shown in Figure 3. The "angle" caused by the applied potential effectively thins part of the already-thin barrier, making tunneling easier. It is this tunneling under bias that is used to program electrically-erasable devices. Note that by reversing the bias, the tunneling can occur just as well in the opposite direction. This is what makes electrical erasure possible.

Electrical erasure has advantages over UV erasure both in cost and quality. Because the erasure is electrical, no expensive window is required in the package. This makes erasability cost-effective even in high-volume production quantities. In addition, the fast erasure allows Vantis to reprogram the device many times, allowing many more paths to be tested than can be tested in a UV part. This provides much higher quality, especially in higher-density devices.



a. Direct tunneling

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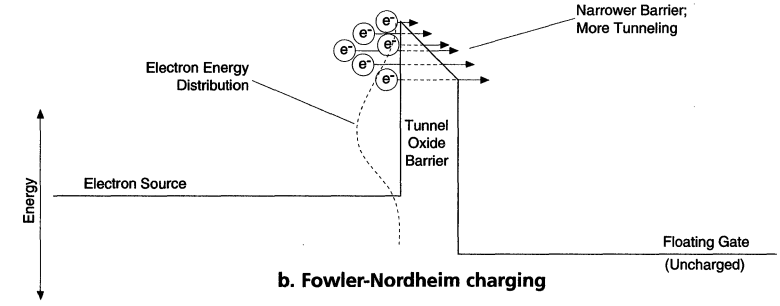

b. Fowler-Nordheim charging

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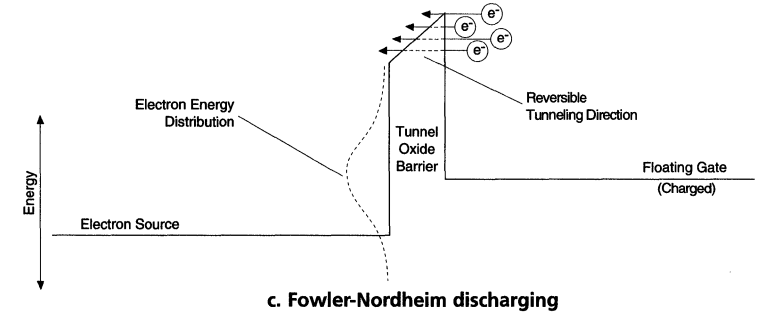


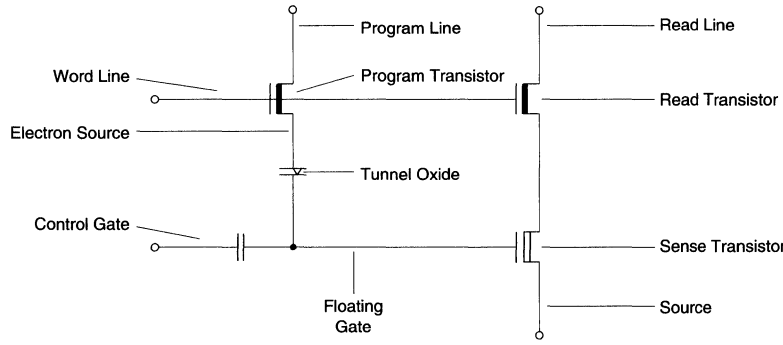
c. Fowler-Nordheim discharging

16507C-005

Figure 3. Energy Band Diagrams

Cell Configuration and Programming

The programming cell is shown in Figure 4. To improve device speed, the programming cell has been divided into the programming portion and the data path portion. In addition to speed, there are a number of other benefits to this approach. At the most basic level, this eliminates a poly-silicon layer, simplifying the process. This reduces costs and improves reliability



a. Circuit

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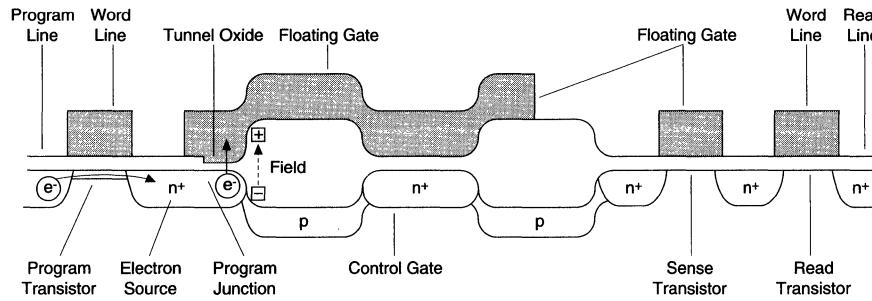


b. Cross-section

16507C-007

Figure 4. EE PLD Programming Cell

The programming half requires long-channel transistors capable of sustaining high electrical fields; the data path requires short-channel transistors that are fast. Note that this does take more space, but in PLDs, the size of the cell is not a limiting factor as it is in memories. In a PLD, the programming array can take up as little as 10% of the die area, while a memory typically uses more than 90% of the die area for the programming array.

Programming and erasure are complementary procedures in EE technology. However, the sense of programming and the sense of erasing are perhaps opposite to what one might assume. A cell is considered to be programmed if there is a charge deficit on the floating gate, providing a positive voltage; it is erased if there is excess charge on the floating gate, generating a negative voltage. This means that programming a device only requires turning ON those cells that are needed, rather than turning OFF all of the cells that are not needed.

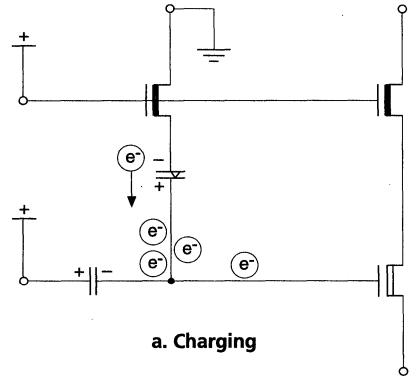
A cell fresh from wafer fabrication has no net positive or negative charge on the gate. To balance the threshold of the transistor for reliable turn-on and turn-off, a **cell implant** is used to center

the threshold voltage near 0 V. Programming and erasing involve either removing electrons from the conduction bands of the poly-silicon gate or adding excess electrons, providing a net charge that will move the gate voltage solidly to one side or the other of the threshold voltage.

When programming or erasing the device, a voltage is applied between the program and control gate nodes. The direction of the voltage determines whether the cell is erased or programmed.

When erasing, the control gate is given a positive voltage, and the program node is grounded. This attracts electrons from the program transistor across the tunnel oxide to the floating gate, turning the read transistor OFF (see Figure 5a).

When programming the cell, the program node voltage is elevated, and the control gate is grounded, reversing the electron flow, as indicated in Figure 5b. Enough electrons flow off the floating gate to leave a net positive charge; this turns the transistor ON.



a. Charging

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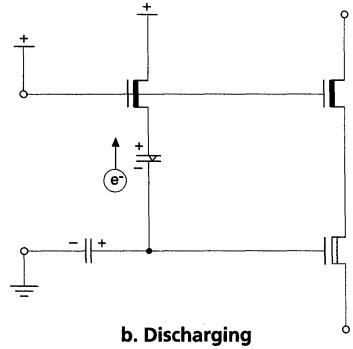

b. Discharging

16507C-009

Figure 5. Cell Biasing

Vantis has modified the programming cell to increase programming efficiency and has a number of patents on the resulting circuit. On traditional devices, the source node is grounded during programming. On Vantis' devices, the source node is raised to the same potential as the control gate, as shown in Figure 6. This increases the **coupling ratio** of the cell. The coupling ratio is the percentage of the applied field that appears across the tunnel oxide. When the source is grounded, the field across the tunnel oxide is reduced (since there is another capacitor in parallel with the tunnel oxide). By raising the source voltage, more of the field is available for programming. The coupling ratio can therefore be thought of as a measure of the programming efficiency; since the efficiency is higher, lower voltages are required for programming.

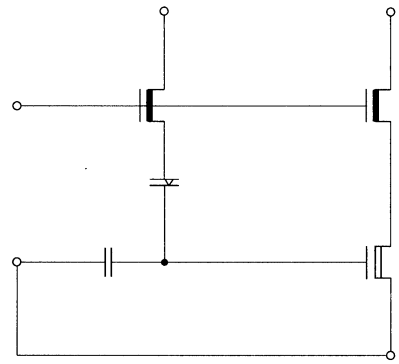

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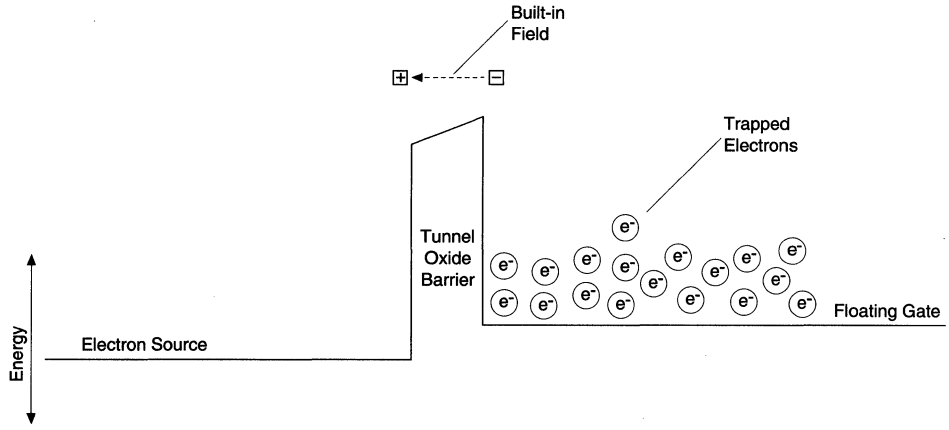
Figure 6. Source is at Same Potential as Control Gate to Improve Coupling Ratio

The split-cell configuration also allows a simpler programming algorithm, since the programmer can take advantage of the self-limiting nature of programming and erasure. The split cell places the read cell gate and the floating cell gate in "parallel" with each other. Therefore, the floating cell can be either completely charged (with a net excess of electrons) or completely discharged (with a net deficit of electrons, or an excess of holes), as shown in the energy diagrams in Figure 7. This is simple to do, since the electrons that have crossed the barrier set up a field that opposes further tunneling. As more electrons cross the barrier, the opposing field grows strong enough to block more electrons from tunneling (Figure 8). Regardless of the state of the floating cell, the select line will turn on or off the read transistor; the cell will only be read, however, if both the read transistor and the floating transistor are ON.



a. Charged (erased)

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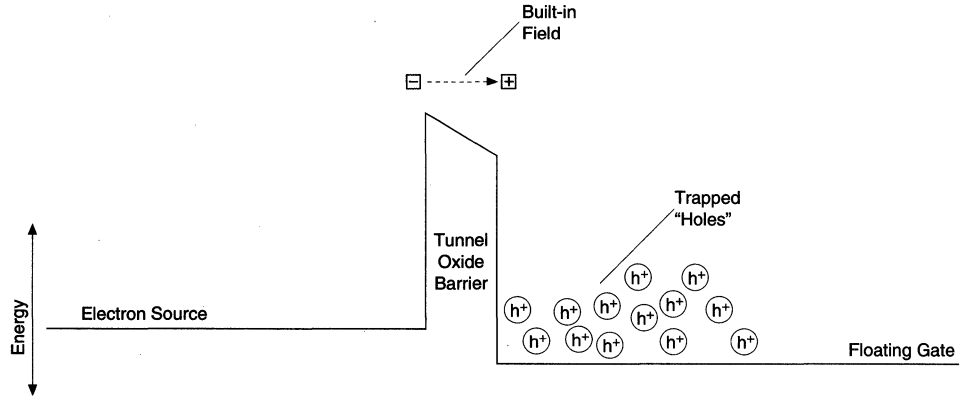

b. Discharged (programmed)

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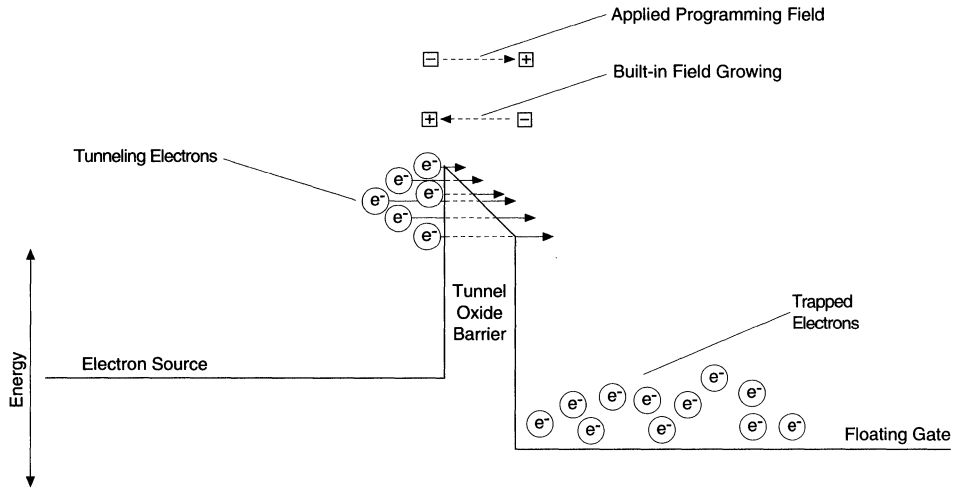
Figure 7. Stable EE Cell



a. Energy band diagram

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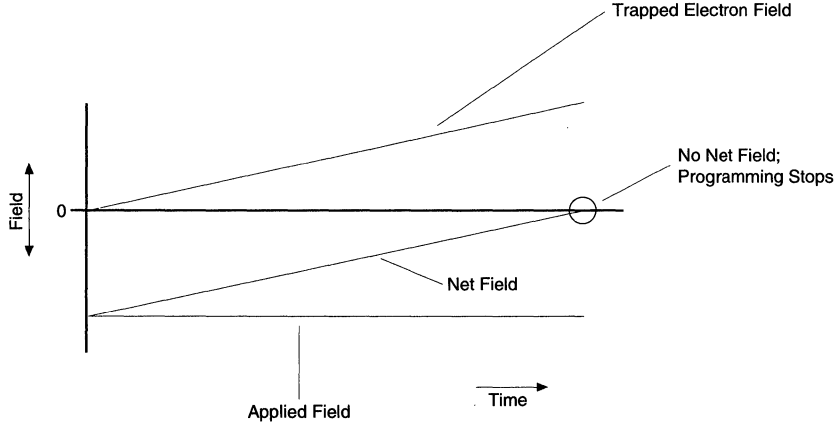
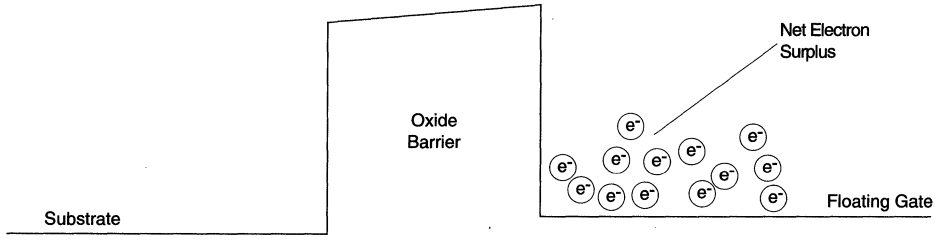


b. Fields vs time

16507C-014

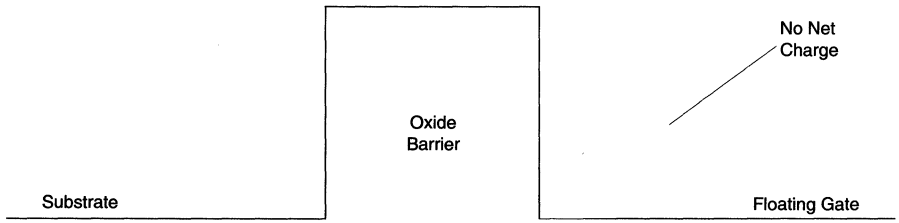
Figure 8. Self-Limiting Programming and Erasure

In standard one-transistor cells, the two gates are actually in "series". If the floating gate is charged, then the transistor is OFF, regardless of the state of the select line. In order to read the cell, the floating gate has to be neutralized so that the select line controls the transistor (Figure 9). If the floating gate were completely discharged, then the transistor would be ON regardless of the state of the select line. The programming algorithm is therefore more complicated, since the amount of charge removed must be monitored to ensure that just enough charge is removed to neutralize the floating gate.



a. Charged (programmed) state

16507C-015



b. Neutral (erased) state

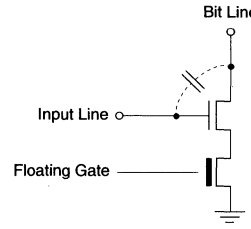
16507C-016

Figure 9. UV Cell

Array Configuration

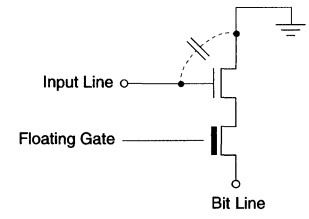
The discussion above focused on individual cells. These cells must be joined together to form a complete array that is driven by input lines and drives product terms.

There are two configurations used in Vantis' EE CMOS devices (see Figure 10). The configuration in Figure 10b provides some benefit to device speed because the parasitic capacitor does not couple the input line and the product term, but both approaches are actively used in designs.



a. Bit line at the drain

16507C-017



b. Bit line at the source

16507C-018

Figure 10. Two Array Configurations

PROGRAM INTEGRITY

Reliable programming of PLDs requires the use of well-calibrated, quality programming equipment. To ensure that the device is correctly programmed, the correct voltages and times must be applied.

As discussed above, it is impossible to over-charge or over-discharge the programming cell since the mechanism is self-limiting. This provides more leeway and makes the programming algorithms less sensitive to programmer variations. This ultimately provides higher, more consistent programming yields under real-life production programming conditions.

However, if the cell is under-programmed or under-erased, an insufficient amount of charge might transfer onto or off of the floating gate. When programming, this might not turn the read cell ON sufficiently, potentially slowing down the device. In the case of erasure, the read cell might be partially ON if it is not completely erased. This may cause "disconnected" inputs to appear partially connected. Thus, it is important to ensure that the programming pulsewidths are long enough to provide adequate programming.

If the programming voltages are slightly inaccurate, CMOS devices often can still be programmed correctly. However, excessive voltage might cause device damage if breakdown voltages are exceeded. Extremely low voltages might fail to engage the programming circuitry completely.

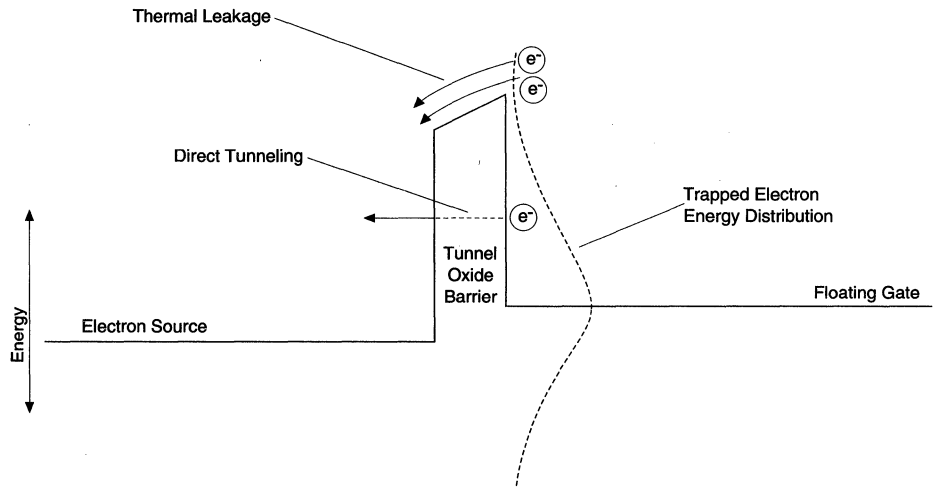
Because of the need for accurate programming, and for ensuring that the programming algorithms are up-to-date, we certify programmers that meet strict criteria for all products.

Data Retention

In an electrically-erasable device, the floating cell is programmed by forcing electrons to tunnel through the tunnel oxide into the floating gate. Ideally, these trapped electrons mean that the device remains programmed indefinitely. Actually, the charge cannot remain indefinitely, but its lifetime is normally extremely long. The stability of the program charge is called **data retention,** the ability of the device to retain its charge as programmed.

There are two basic leakage mechanisms: direct tunneling and thermal leakage. These mechanisms occur independent of whether the cell was programmed by electron injection or tunneling. The amount of direct tunneling is a function of the potential across the tunnel oxide, and is generally very low. Leakage is normally dominated by thermal charge decay.

On one side of the energy barrier, there are electrons with a distribution of energies (see Figure 11). Some have enough energy to escape over the top of the barrier. As the temperature is raised, more electrons achieve the energy required to overcome the barrier.



16507C-019

Figure 11. Data Loss Mechanisms

The tendency of the gate to leak can be modeled as an Arrhenius function, which means the formula for the programming "decay time" t_d has the form:

$$t_d = Ke^{E_a/kT}$$

where

E_a is the intrinsic **activation energy**
T is the temperature in Kelvin
k is Boltzmann's constant
K is a scaling constant.

If we can measure the rate at two known temperatures, then:

$$\frac{t_{d1}}{t_{d2}} = \frac{Ke^{E_a/kT_1}}{Ke^{E_a/kT_2}}$$

Note that the constant K drops out, so we need not be concerned with its specific value. From this we find that:

$$E_a = \frac{T_2 ln(t_{d1}) - T_2 ln(t_{d2})}{kT_1T_2}$$

This lets us measure E_a, which should be constant for a given process. The higher the value of E_a, the longer the decay time will be. This is because E_a roughly represents an energy "barrier" that must be overcome for an electron to leak away. The higher the barrier, the fewer electrons have the energy to overcome E_a.

Charge leakage can be aggravated by poor quality tunnel oxide. Defects in the oxide provide a lower energy path for discharging, effectively lowering E_a. Baking a device accelerates this leakage and identifies devices with weak oxide. Vantis uses a bake for all EE products to ensure that the production devices have a high E_a and therefore good data retention. The average E_a for all devices, including those with weak oxide, is about 0.8 eV. After eliminating the weak devices by a 250°C 24-hr bake, the average E_a is about 1.8 eV.

Data retention time depends on the temperature to which the devices are exposed. The higher the temperature, the shorter the decay time because the electrons have more energy, and more can leak off the gate.

There are two temperatures that may be of concern for different reasons: the maximum device storage temperature (150°C) and the maximum operating temperature (125°C for military). In the first case, the idea is to know that if a programmed part sits on a shelf for some period of time before being used, the program will remain intact for that time. The second case is intended to give an idea of how long a device will remain operational in-system.

Using the equation above to solve for the decay time at these temperatures, the result is several decades for the storage temperature, and even longer for the operating temperature. For room temperature, the exponential nature of the function makes the decay time increase to centuries.

Vantis specifies 10 years at the maximum storage temperature (an industry standard for EPROMs and EEPROMs), and 20 years in-system under worst-case military conditions. That the calculated numbers are so much higher builds confidence in the numbers specified. In general, the typical end-of-life failure mechanisms that affect all devices (and which are unrelated to the EE cells) will cause device wear-out before the program data is lost.

The integrity of the charge in the electrically-erasable cell also stands up to any electrical fields that exist in surrounding equipment. For charge to be transferred off of, or onto, the floating gate, a field must be placed across the oxide. Such a field cannot be generated outside the programming mode; an external field, no matter how strong, cannot set up the programming mode.

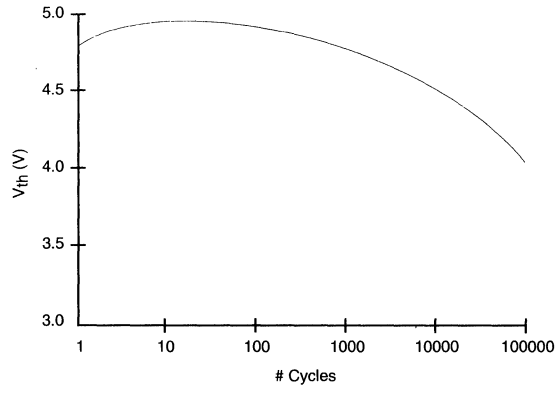
The charge might also be pulled through some other oxide if the field were large enough. However, to remove the charge through anything but the tunnel oxide requires an external field so high that the rest of the device would break down before any cell charge were ever lost. This would occur on any device, programmable or not. Therefore, any external field strong enough to remove charge from a floating cell will destroy the rest of the device first.

CELL ENDURANCE

Another factor that affects long-term data retention is the **cell endurance**. The endurance is the number of times the device can been erased and reprogrammed. Over time, the oxide can wear out, resulting in a gradual reduction in E_a. This occurs as defects are created in the oxide. These defects trap electrons, which then oppose the field that is required for programming. Given enough trapped charges, the established potentials will be insufficient for programming. This typically happens after hundreds of thousands of reprogramming cycles.

The ability to charge up a cell with good data retention can be measured by the *margin voltage*. This is the voltage that must be applied to the control gate to counteract the charge on the floating gate. If the gate is highly charged, a larger margin voltage is needed to overcome the charge. Thus, put simplistically, a higher margin voltage indicates better cell charging.

Figure 12 illustrates measurements of the margin voltage as the number of program/erase cycles is increased. By 100,000 cycles, the margin voltage still is greater than 4 V; for the cell to fail, the margin voltage must fall to below about 1 V.



16507C-020

Figure 12. Cell Endurance: Margin Voltage Solid After 100,000 Program/Erase Cycles

For EEPROMs, which often are reprogrammed in-system, it is important to know how many thousands of times the device can be reprogrammed. However, most EE PLDs are not intended to be programmed in-system, and probably are programmed very few times. Most production units are programmed only once by the user. Prototypes might be programmed tens of times at most. Therefore we specify a maximum number of 100 erase/reprogram cycles.

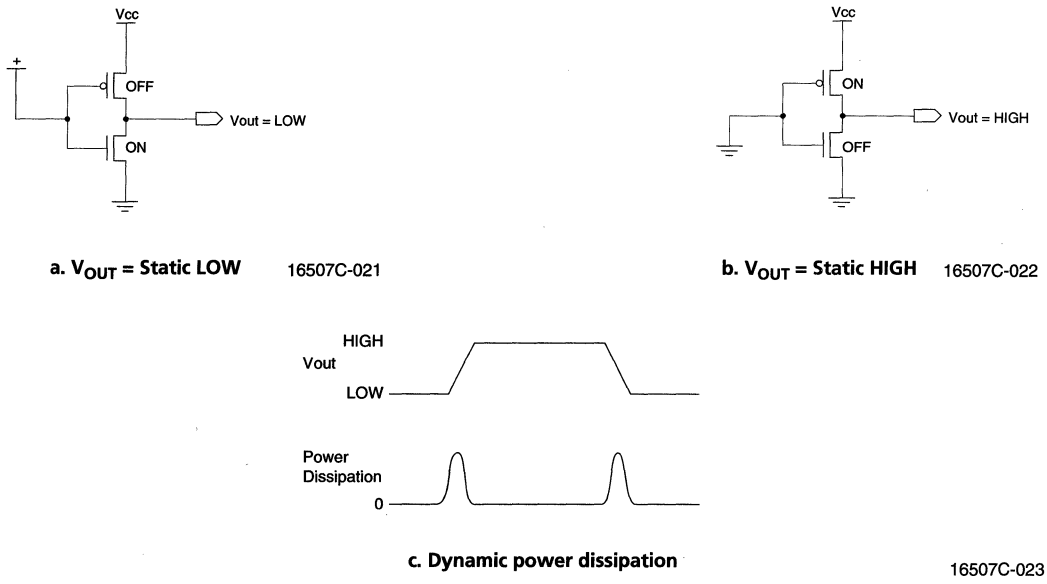
This does not imply that the devices are weaker than EEPROMs; it is just that more extensive testing would have to be done to justify specifying a larger number. Since this larger number is not needed, a cost savings is realized because of the test simplification. Note that the devices are actually programmed hundreds of times in testing before they are shipped out, giving outstanding programming and functional yields; however, the number of erase/reprogram cycles specified refers only to programming done by the user.

DEVICE CHARACTERISTICS

Power Dissipation

CMOS technology is associated with low power consumption, and indeed, all CMOS PLDs use lower power than their bipolar counterparts. However, most PLDs do not provide the zero-standby power that standard CMOS logic parts do.

The basic CMOS inverter lowers operating power because at any given time, only one of the two transistors can be fully ON. The other is OFF and blocks the flow of DC current. Thus, when the device is in a stable state, no current can flow. While the device is switching, both transistors are partially ON, allowing for a transient current spike. This means that power is consumed only when the device switches. Because a spike occurs for each transition, the average power consumption is affected by the frequency of operation (see Figure 13).



a. V_{OUT} = Static LOW 16507C-021

b. V_{OUT} = Static HIGH 16507C-022

c. Dynamic power dissipation 16507C-023

Figure 13. CMOS Inverter Power Dissipation

This type of circuitry is found throughout most of a PLD circuit. However, one portion of the PLD circuit does not use a standard CMOS inverter: the programmable array. One of the necessary elements of zero-power operation is that the output of the inverter have a voltage swing from ground to V_{CC}, so-called **rail-to-rail** operation. In the array, such a wide swing makes the propagation delays too long. To speed up the device, the sense amps that determine the state of a product term are designed to have a much more limited swing. This means the sense amps are constantly drawing power, even when not switching. These are the half- and quarter-power CMOS PLDs; their power consumption is still less than that of a bipolar PLD. Since most CMOS PLDs are used in TTL sockets, the CMOS PLDs work well.

I_{CC} vs V_L and Loading

The greatest external contributors to I_{CC} are the input HIGH level (V_{IH}) and the output load.

As the V_{IH} drops from its ideal level of V_{CC}, the inverter starts to draw current. The worst case scenario would be a V_{IH} at the minimum of 2.0 V, which could contribute some 5 mA per input buffer to the power consumption.

The output load can also have a dramatic effect on power dissipation, especially on devices that have many I/O pins. For an output driving a purely capacitive load, the power dissipation contributed by the load for one output is determined by the load capacitance, the frequency at which the output is switching, and the output voltage swing (V_S). The output stage will go through a process of repeatedly charging and discharging the capacitor. Although the direction of charge flow reverses itself every other transition, the relative voltage change does too, so that the power contribution is the same for a charge and a discharge.

If we consider the case of charging the capacitor, we will be placing a charge, Q_L, on the capacitor that is determined by:

$$Q_L = C_L V_O$$

where C_L is the load capacitance and V_O is the output voltage. The current contribution from this is:

$$i = \frac{d_{LQ}}{dt}$$
$$= \frac{C_L d_{V_o}}{dt}$$

In one half the output transition period t_P, the change in output voltage will be equal to the output swing Vs. This means that:

$$i = C_L \frac{V_S}{\frac{t_P}{2}}$$
$$= 2C_L \frac{V_S}{t_P}$$
$$= 2C_L V_S f_o$$

where f_O is the frequency at which the output is switching.

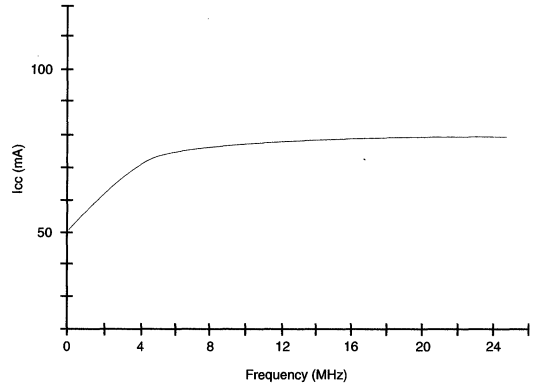
The power dissipation is the product of the current and the voltage. Since the voltage is changing during the time that the power is being dissipated, we can approximate by dividing the voltage swing by 2. This gives:

$$P = iv$$
$$= 2C_L V_S f_o \frac{V_S}{2}$$
$$= 2C_L V_S^2 f_o$$

This means that for a 100-output device (PLD or any other device) with each output driving 35 pF loads, where the output swing is 3 V and the output frequency is 50 MHz, the power dissipation contributed only by the load will be about 1.6 W regardless of the power dissipation of the chip itself.

I_{CC} vs Frequency

The operating current increases with frequency for standard CMOS devices. The difference is the current at low frequencies. A standard device typically can draw 35 mA at 0 MHz. Figure 14 shows a typical curve for standard devices.



16507C-024

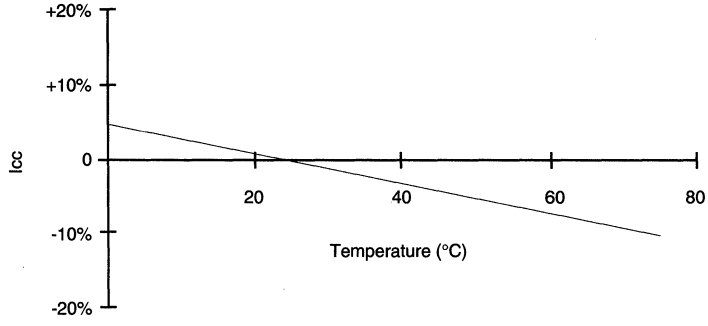
Figure 14. I_{CC} vs Frequency, Standard Device

I_{CC} vs Number of Product-Terms

The number of product terms switching can sometimes affect I_{CC}. On standard devices, however, the design of the particular sense amp determines whether the I_{CC} will increase or decrease with more product terms. Therefore, it cannot generally be predicted. From a practical standpoint, the change in I_{CC} due to different numbers of product terms is negligible.

I_{CC} vs Temperature

The amount of current drawn by a device depends on how much current can pass through the transistors. Simplistically speaking, the channel of a transistor can be modeled as a resistor. The resistance is affected by temperature since this affects the mobility of electrons. Electrons are less mobile in a hot device. The hotter the device, the more the molecules will vibrate and the harder it is for electrons to pass through without a collision with a molecule. This means that the resistance of the channel is higher, which in turn means that the device conducts less current. Therefore, I_{CC} is greatest when the device is cold, and is minimized when the device is hot. A typical curve is shown in Figure 15. This curve has been generalized by normalizing the current to the room temperature current.



16507C-025

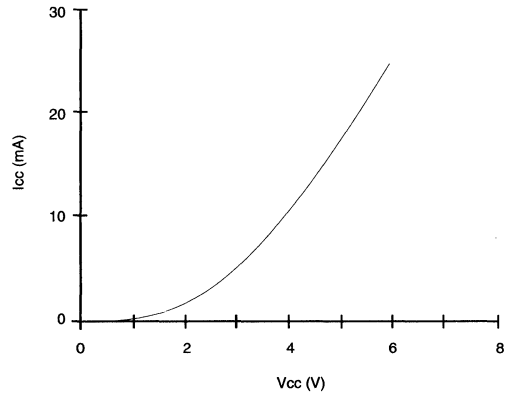
Figure 15. I_{CC} vs Temperature, Normalized to Room Temperature

I_{CC} vs V_{CC}

The variation of I_{CC} with changes in V_{CC} should come as no surprise; as V_{CC} increases, so does I_{CC}. This means that the power consumption actually increases roughly as the square of V_{CC}, since power consumption can be expressed as:

$$P = V_{CC} I_{CC} = \frac{V_{CC}^2}{R_{eff}}$$

where R_{eff} is defined as V_{CC}/I_{CC}. This is a simplification, of course, since R_{eff} is non-linear, and varies with V_{CC}. A typical I_{CC} vs V_{CC} curve is shown in Figure 16.



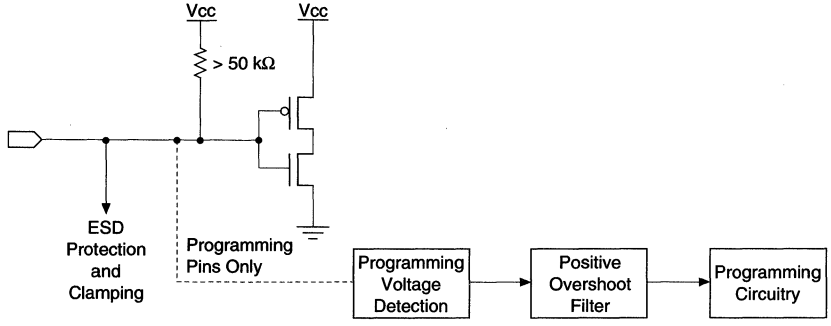
16507C-026

Figure 16. I_{CC} vs V_{CC}

Input/Output Structures

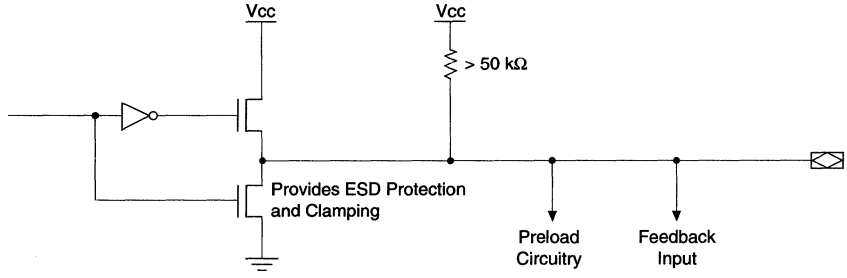
The basic input and input/output structures are shown in Figure 17. The ESD circuits and the programming voltage detection circuits will be discussed in more detail later.

Newer devices have pull-up resistors as shown below. In these devices, there is also a transistor in series with the resistor, which reduces die size and improves testability of the I/O circuit.



a. Input with pull-up resistor and overshoot filter

16507C-027



b. Output with pull-up resistor

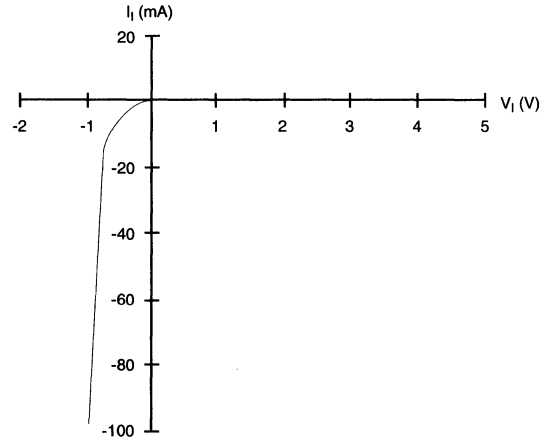
16507C-028

Figure 17. Equivalent Input/Output Schematics

I-V Curves

Figure 18 shows a typical I-V curve for an input buffer. Within the range of normal input signals, the input buffer has extremely high impedance, with diodes and MOS transistors that turn on when the input is below ground. On higher speed devices, this has the effect of a high-speed diode capable of clamping negative overshoot on noisy signals.

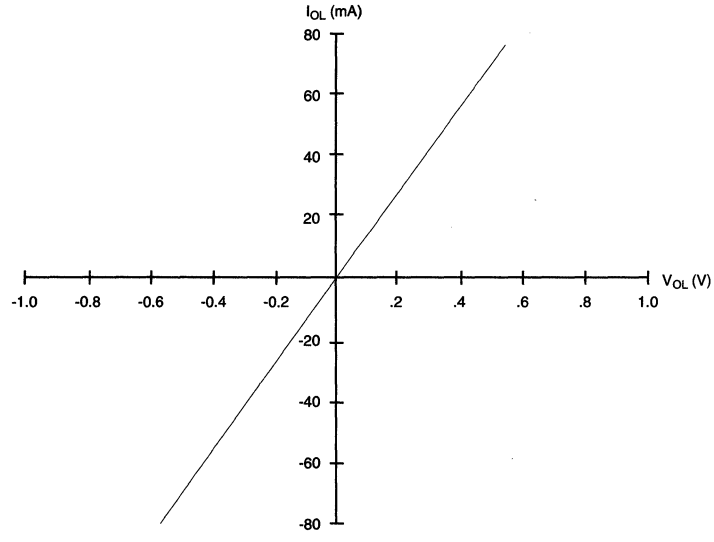
Since the input is effectively a capacitor, the impedance has no real component; the imaginary portion falls with increasing frequency. A typical device has an input capacitance of 8 pF at 1 MHz. Assuming a capacitance around 8 pF at higher frequencies, this yields a capacitive reactance of 2.5 KΩ at 50 MHz.



16507C-029

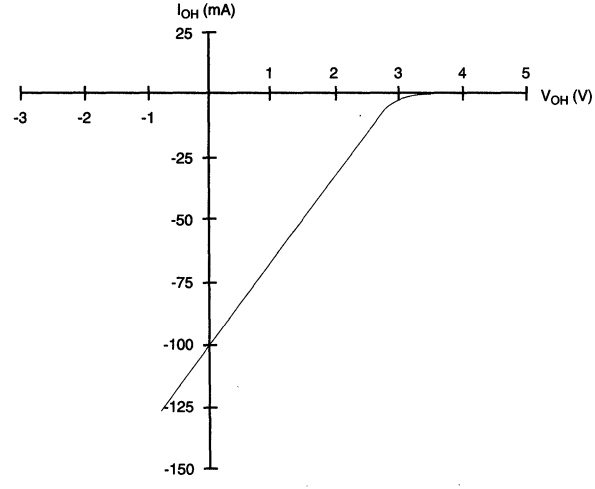
Figure 18. I-V Curve for an Input with No Pull-Up Resistor

Figure 19 shows typical I-V curves for high and low TTL-style outputs. The impedance of a low output is about 10 Ω; a high output has an impedance of about 30 Ω. The fact that the impedances are somewhat more symmetric than those found on a bipolar device makes it easier to terminate long traces accurately.



a. Output LOW

16507C-030

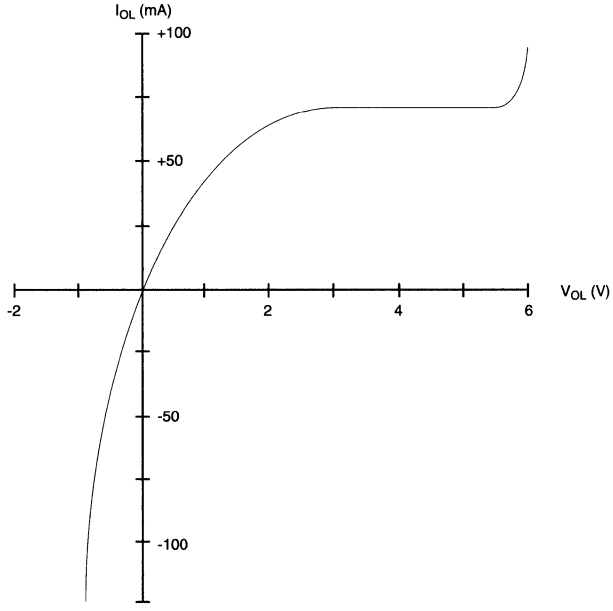


b. Output HIGH

16507C-031

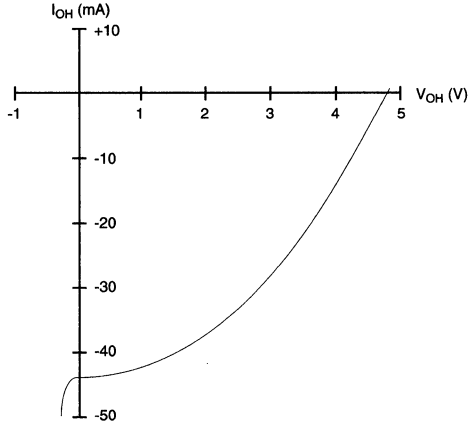
Figure 19. I-V Curves for a TTL-Style Output with No Pull-Up Resistor

Figure 20 shows the curves for rail-to-rail switching outputs. The p-channel impedance, when the output is HIGH, ranges from 200 Ω when extremely heavily loaded to about 50 Ω when lightly loaded. The n-channel impedance is lower, at about 10 Ω.



a. Output LOW

16507C-032



b. Output HIGH

16507C-033

Figure 20. Curves for a CMOS-Style Output

Output Drive vs Temperature and V_{CC}

The output drive varies with temperature just as I_{CC} does. As the temperature increases, electron mobility decreases, cutting the drive. Likewise, the drive increases as temperature decreases. For example, at 75° C, I_{OL} decreases by about 18% from its room temperature value; I_{OH} decreases by about 7%.

The drive also varies directly with V_{CC}, although the effect is most pronounced on I_{OH}; it increases by about 18% when taken from 5.0 V to 5.25 V. Because a low output transistor is already ON hard, the little extra bit of drive that its gate gets as V_{CC} goes to 5.25 V only increases I_{OL} by about 3%.

There is no explicit current-limiting resistor on the pull-up. The resistance of the pull-up channel limits the current. The fact that this resistance is smaller than what one might find in a bipolar device contributes to the more symmetric impedances, but also gives a higher short-circuit current ISC. The slew-rate-limiting circuit also limits the drive; slew-rate-limiting is discussed below.

AC Parameters

AC parameters vary with a number of conditions. The data sheet specifications designate one set of conditions that act as a benchmark for confirming the guaranteed performance, but as the application changes the conditions, the actual system performance may change.

t_{PD} vs Temperature

Propagation delays decrease (that is, they speed up) at colder temperatures for the same reasons that I_{CC} increases. In general, devices at 0°C operate about 15% faster than those at 75°C.

t_{PD} vs V_{CC}

As V_{CC} is increased, more power is available, and the device can operate faster. However, the effect is less pronounced than with temperature. A device operating with a 5.25 V supply runs about 4% faster than one running with a 4.75 V supply.

t_{PD} vs Loading

The t_{PD} increases as the device load increases, although much of this results from the increase in rise and fall times of the outputs. For every 50 pF change in load, roughly a 2- to 5-ns change in the rise and fall time can be expected. In addition, as the load increases, more transient current is switched, creating more internal noise. This can slow the speed path inside the chip.

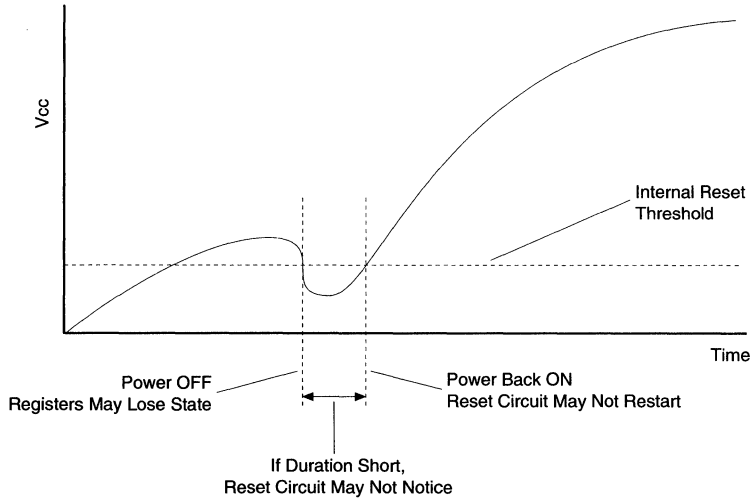
Power-Up Reset

Power-up reset is a feature that forces a device to power up into a known state. Without this feature, the power-up state is not known. Power-up reset helps make system initialization and testing simpler.

The ramp rate of V_{CC} is not critical to the power-up reset function. However, there are two other requirements: the supply ramp must be monotonic, and the clock must be suppressed until power-up is complete.

The monotonicity requirement basically says that there should be no low-going glitches in the power-up ramp (Figure 21). The danger in such glitches is that if the timing and voltage are just right, the registers themselves may think that the device powered down temporarily, causing them to lose their state. If the glitch is fast enough, however, the power-up reset circuit may not

notice the glitch and may think that everything is proceeding just fine. At the end, the registers may be in a random state. Even if the power glitches low enough for long enough time to shut down all circuits, the power-up timing must be restarted from the end of the glitch.

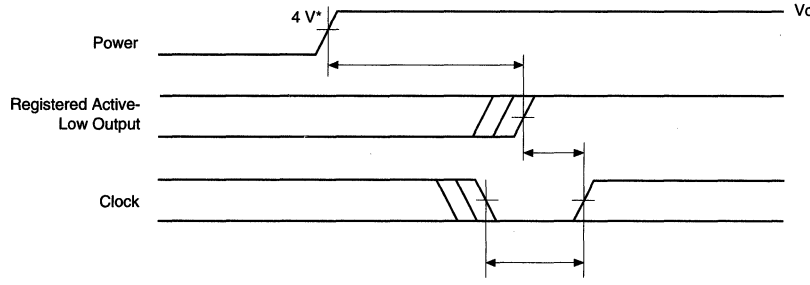


16507C-034

Figure 21. Non-Monotonic Power-Up Can Cause Power-Up Reset To Fail

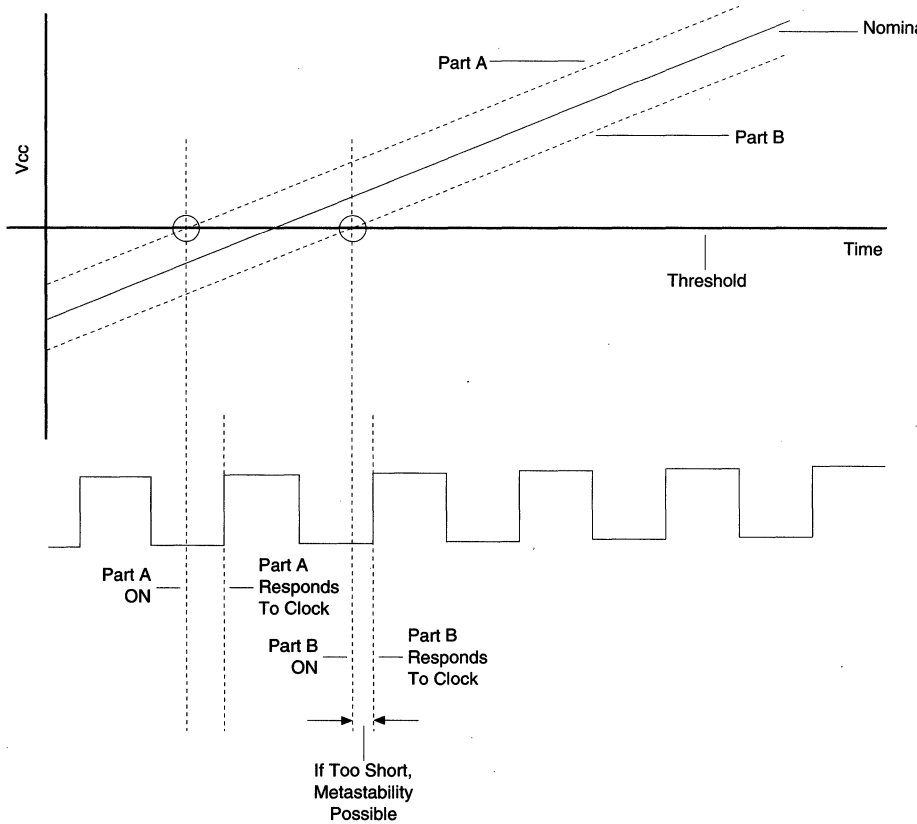
There is also a requirement that the clock not be running during power-up (Figure 22a). If the clock is running while the device is powered up, then as different parts of the device—and, indeed, the whole circuit board—turn on, parts of a single device, or different devices, may be out of synchronization with each other (Figure 22b). At some point, a part of a device will be ON enough to start recognizing the clock. It will then start to sequence as per the inputs it sees. If the inputs are not stable, the sequence may not be correct. In addition, if not all parts of the circuit or board recognize the clock at exactly the same time, some parts will start cycling before others, and the whole system will be out of synchronization.

The other potential (although remote) problem with clocking during power-up is metastability. If a register powers ON in time to see the clock edge, its setup time might have been violated, making the results at the output unpredictable.



a. Correct operation

16507C-035



b. Free-running clock places part B one clock cycle out of sync with part A

**2.7 V for Low-Voltage MACH*

16507C-036

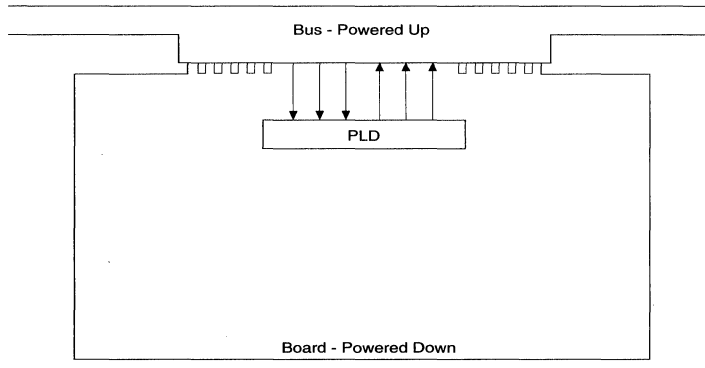
Figure 22. Clocking During Power-Up Reset

Powered-Down Characteristics

Some applications place the CMOS PLDs in a situation where it is itself powered down, but it is driving or is driven by other devices that are still powered up. This is especially typical of devices which talk directly to a bus (Figure 23).

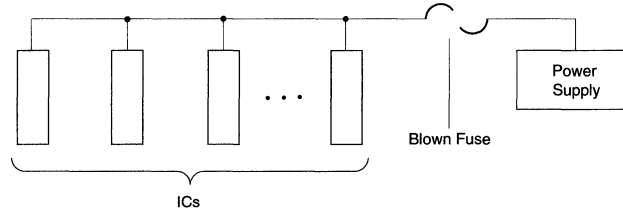
The characteristics of the device in such a condition depend on how the power was removed. There are two ways of removing power:

- Opening up the V_{CC} line (e.g., if V_{CC} is fused, and the fuse blows; Figure 24)
- Grounding V_{CC} (Figure 25)



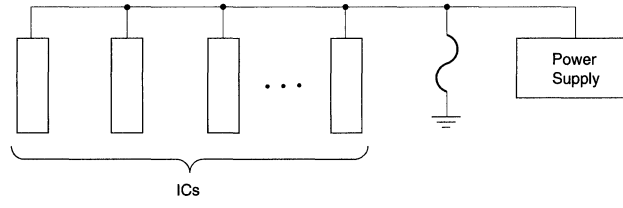
16507C-037

Figure 23. Powered-Down Device with Active Inputs and Outputs



16507C-038

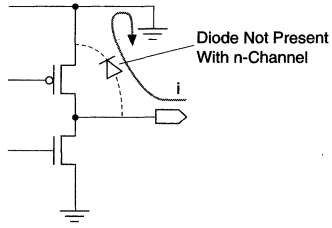
Figure 24. Power Down with V_{CC} Open



16507C-039

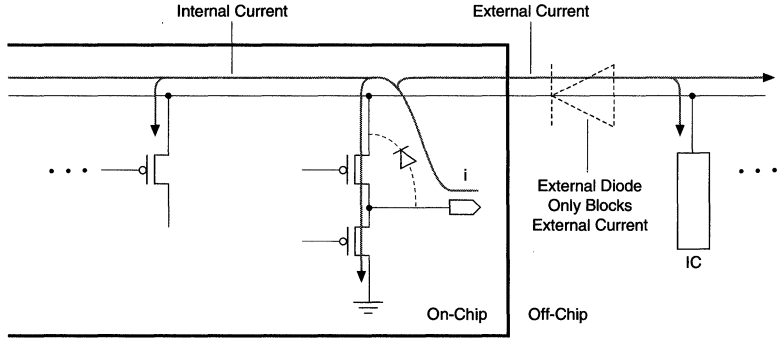
Figure 25. Power Down with V_{CC} Grounded

It is important to know whether, for a given device, there is some kind of path from the pin to V_{CC} when V_{CC} is lower than the pin voltage. If any current can flow, it is not necessarily catastrophic, but there can be some effect. If V_{CC} is grounded, then there is a direct path to ground for any current flowing from the pin to V_{CC} (Figure 26a). If V_{CC} is open, then the only path from V_{CC} to ground is through the device itself, and through the V_{CC} lines of any other devices on the same V_{CC} line (Figure 26b). In the latter case, the pin is essentially powering up the device(s) itself; realistically, it cannot provide enough power to drive the chip, and this could result in the pin being loaded down.



a. V_{CC} grounded

16507C-040



b. V_{CC} open

16507C-041

Figure 26. Powered-Down Current Paths with P-Channel Pull-Up

Most of Vantis' CMOS PLDs have no such path when powered down. Figures 27 and 28 show the I-V curves of inputs and I/O pins while V_{CC} is open and V_{CC} is grounded. Figure 27 is for TTL-compatible devices which have n-channel pull-ups on the outputs. Figure 28 is for the HC/HCT-compatible zero-power devices and others which have p-channel pull-ups.

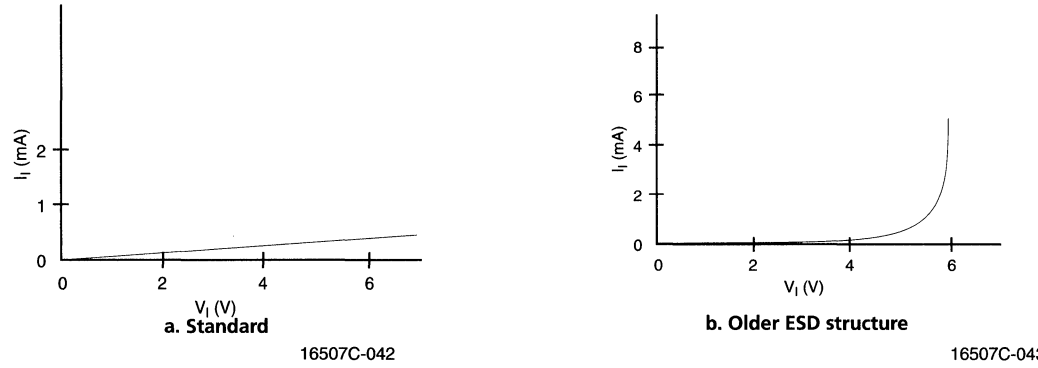


Figure 27. Power-Down Characteristics of TTL-style CMOS Inputs and Outputs

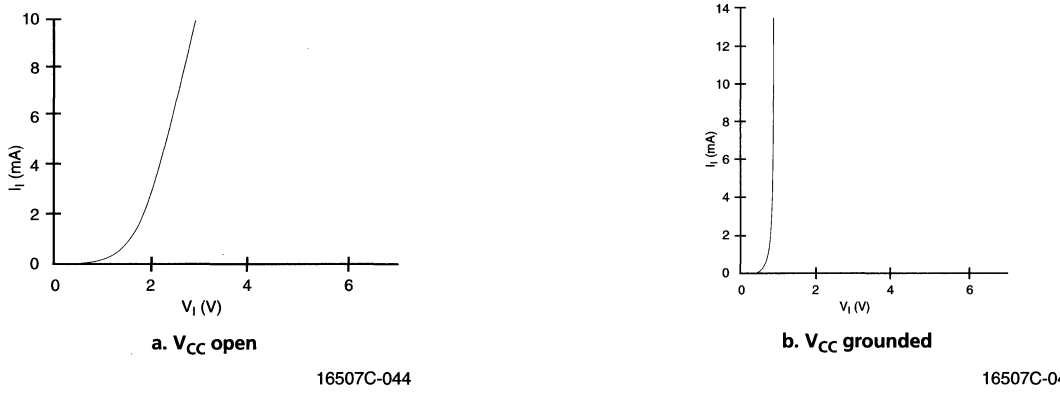
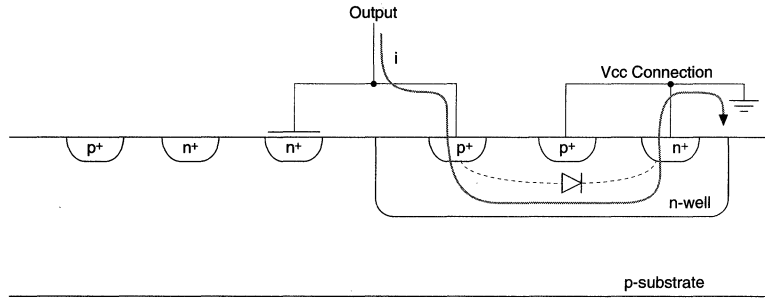


Figure 28. Power-Down Characteristics of CMOS-Style Output

Note that for most of the TTL-compatible devices, there is no leakage on the pins. This means that signals on a pin are not affected by the powered-down device. Therefore, it can be safely connected to an active bus. It also allows for safe **hot insertion or "hot socketing,"** where the device (or the board that contains the device) is plugged into a socket that has V_{CC} applied.

As a result of one of the ESD structures (which are discussed below), some devices do conduct some current when V_{CC} is powered down (Figure 28b). Newer devices do not have this characteristic. This is described in the following ESD section.

With the HC/HCT-compatible devices, the input structures are the same as for TTL devices, but the outputs conduct because of the p-channel pull-up. There is a parasitic diode between the output and V_{CC} (Figure 29). This can cause latch-up if the output voltage is higher than V_{CC}. Thus, it is not recommended that devices with p-channel outputs be directly connected to a bus if the device will be powered down while the bus is active. **Hot insertion** of these devices should also be avoided.



16507C-046

Figure 29. Parasitic Diode in CMOS-Style Outputs

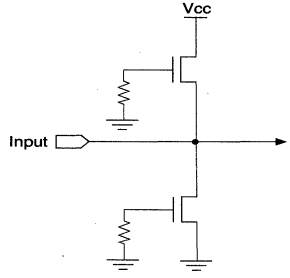
DEVICE INTEGRITY AND ROBUSTNESS

The reliability of Vantis' CMOS processes is documented in product and process qualifications. For EE process products, generally the extended life FIT rate is under 100. The rate for the devices with 2000 hours burn-in is around 30; similar devices with only 1000 hours burn-in have a FIT rate closer to 100. With more burn-in experience, the FIT rate will decline even further due to the statistics used to calculate FIT rates. The FIT rate calculation is such that with fewer burn-in hours, a lower confidence factor is applied, giving higher FIT rates on newer products even when there are no failures.

ESD

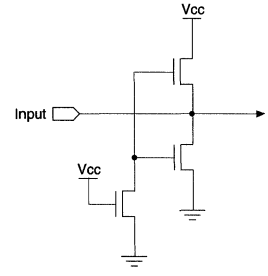
Every pin on the devices is protected against electro-static discharge (ESD), a formal name for static electricity shocks. Output pins rely on the large output drivers as protection. Inputs normally do not have large drivers, so a circuit must be added for input protection. These input protection circuits also provide clamping against negative overshoot.

All new devices make use of the structures in Figures 30a and 30c for ESD protection. Most input pins use the circuit in Figure 30a. On pins requiring high voltages, the circuit has been modified as shown in Figure 30c. Some older devices have the configuration shown in Figure 30b. Because the active pull-down transistor is not ON when V_{CC} is disconnected, it cannot necessarily hold off the ESD transistors; this causes the current seen in Figure 27b. This circuit is no longer being used in new devices.



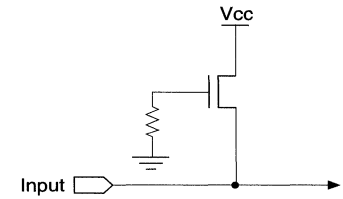
a. Standard

16507C-047



b. Older version

16507C-048



c. Supervoltage pins

16507C-049

Figure 30. ESD Protection

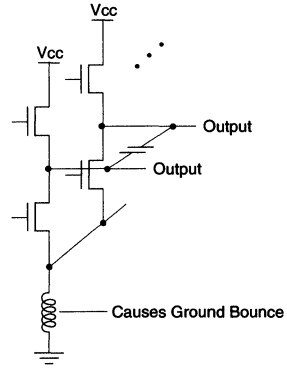
NOISE GENERATION AND SENSITIVITY

Vantis' CMOS PLDs are designed with noise concerns in mind. This affects both the amount of noise generated by the devices and the way in which the devices react to externally-generated noise. As more is understood about the nature of system-level noise, new design techniques are being used to make the devices quieter and more robust.

Ground Bounce

Ground bounce occurs when many outputs simultaneously switch from HIGH to LOW. This occurs because of the fact that CMOS devices generally have outputs that switch very quickly. If left uncontrolled, ground bounce can make a device with many outputs unusable.

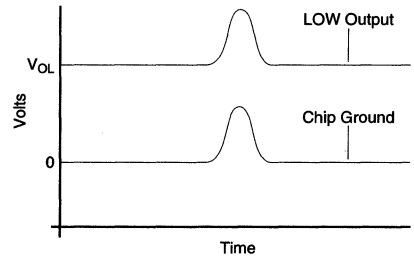
Ground bounce is generated by the natural parasitic inductance in the ground lead (see Figure 31). When a large current surge goes through the inductor, the high **di/dt** induces a voltage that puts the ground level on the chip at a higher voltage than the ground level seen on the board.



16507C-050

Figure 31. Origins of Ground Bounce

Any output that is at a static LOW level maintains a V_{OL} with respect to the chip ground. If the chip ground is bouncing with respect to the board ground, the LOW output will track the moving chip ground and will also appear to bounce (see Figure 32). This is sometimes seen as a glitch by the next device. Even if there is no output glitch, instances of high ground bounce can slow the performance of the internal circuits by temporarily starving them of power. In extreme cases, this can interrupt the internal circuits.

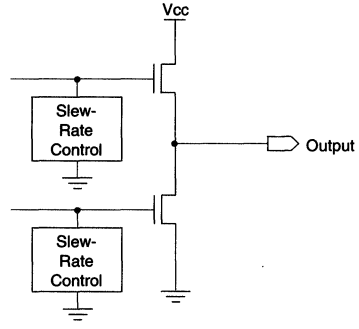


16507C-051

Figure 32. Symptoms of Ground Bounce

Excess ground bounce can be handled in two ways: by limiting the amount of ground inductance and by reducing the *di/dt*. Inductance can be reduced by improving the configuration of the ground pin.

Ground bounce is also controlled by limiting the slew rate of all the output drivers (see Figure 33). This slows down the fall time and reduces the rate of current change by as much as 25%.



16507C-052

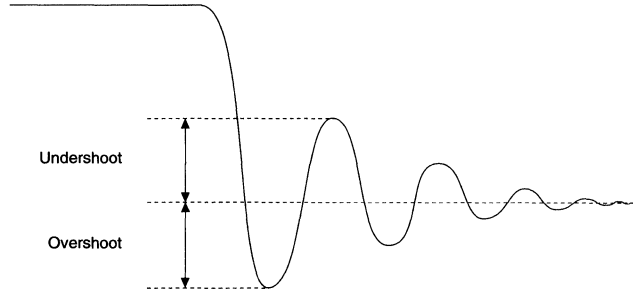
Figure 33. Output Drivers with Slew-Rate Control

Overshoot Sensitivity

Overshoot is a form of noise usually generated when signal traces act as transmission lines but have not been adequately terminated. The resulting reflections can cause significant overshoot, with as much as double the intended swing applied to the input in the negative or positive direction.

Negative Overshoot

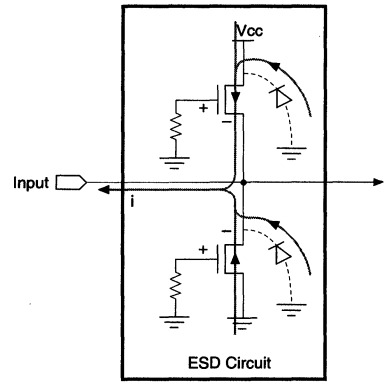
Negative overshoot (Figure 34) poses no problems for a device that has been carefully designed. There is no detrimental effect as long as no unexpected parasitic behavior occurs due to the fact that ground is no longer the most negative voltage. However, the ringing that usually follows overshoot can slow down system performance, since the system has to wait for the ringing to subside.



16507C-053

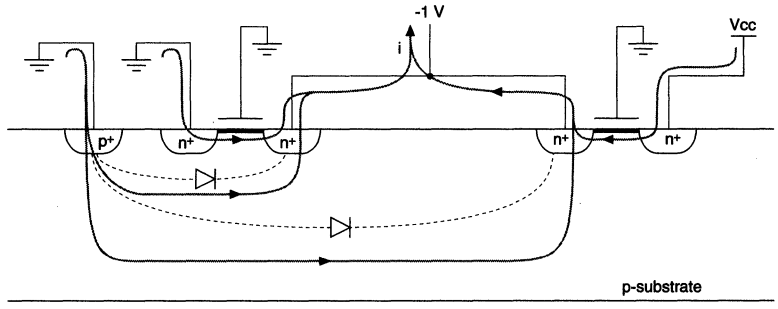
Figure 34. Definition of Negative Overshoot and Undershoot

Clamp diodes are useful for stealing the energy present in the ringing and cutting the ringing short. A fast clamp reacts to the overshoot as it occurs, cuts the amplitude of the overshoot, and reduces or eliminates ringing. Figure 35 shows the ESD protection circuit used on most input pins. Parasitic p-n junction diodes exist between the substrate and the n-type source and drain, although these diodes are relatively slow. Faster reaction is provided by the n-channel devices themselves. When the input is too negative, the gate-to-drain voltage is positive. If the drain is more negative than the threshold voltage, the transistors turn on in the reverse direction, with the drains acting as a sources. This happens very quickly and acts as a clamp. This will also happen on an I/O pin, with the low output driver acting as the clamp.



a. Circuit diagram

16507C-054

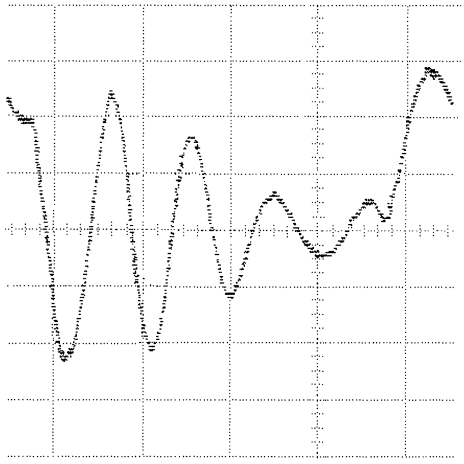


b. Cross-section

16507C-055

Figure 35. Negative Overshoot Clamping

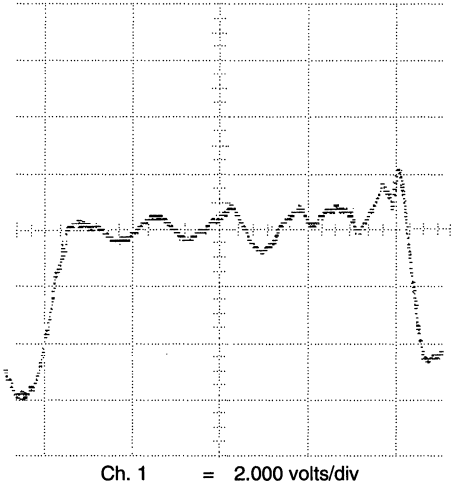
While it might appear that parts with negative substrate bias can "tolerate" more negative overshoot, it is really more accurate to say that these parts **allow** more negative overshoot, since there is no clamping. If there are effective input clamps, which are possible with a grounded substrate, then it will look like the part never gets as much negative overshoot. This does not mean it cannot handle the overshoot; it means that it is clamping the overshoot. If you take the part out of the socket, you will see that when unclamped, the overshoot will increase dramatically, as illustrated in Figure 36. Since Vantis' devices have a grounded substrate, they are inherently better equipped to handle negative overshoot.



Ch. 1 = 2.000 volts/div
Timebase = 50.0 ns/div

a. Signal driving empty socket

16507C-056



Ch. 1 = 2.000 volts/div
Timebase = 50.0 ns/div

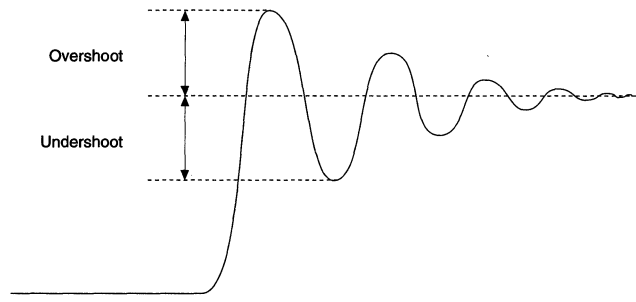
b. Signal driving same socket with CMOS PLDs in it

16507C-057

Figure 36. The Effect of Clamping

Positive Overshoot

Large amounts of positive overshoot (Figure 37) can be a problem on most PLDs, regardless of technology or vendor. This is because most PLDs are programmed using **supervoltages**, and the pins therefore have supervoltage detectors that turn on the programming or test circuits, and potentially disable parts of the normal operating circuitry.



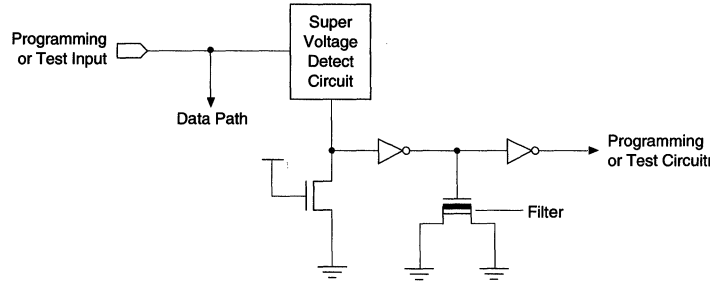
16507C-058

Figure 37. Definition of Positive Overshoot and Undershoot

If there is too much positive overshoot, the signal can travel into the programming voltage range, briefly activating the programming circuitry. This can result in functional interruptions, such as outputs momentarily starting to disable or going from HIGH to LOW.

For earlier devices, the problem can only be avoided by revising the design to reduce the overshoot. A particular design in a particular device may work, but this may be because that device has no supervoltage function on that particular pin. However, if an alternate source with different supervoltage pins is used, the design may not work.

New Vantis CMOS devices incorporate a filter, or delay circuit, that delays the reaction of the programming circuit for about 100 ns. This is enough to reject overshoot signals, which usually last for less than 30 ns. Positive overshoot will not cause any functional interruptions on devices with this protection (see Figure 38).



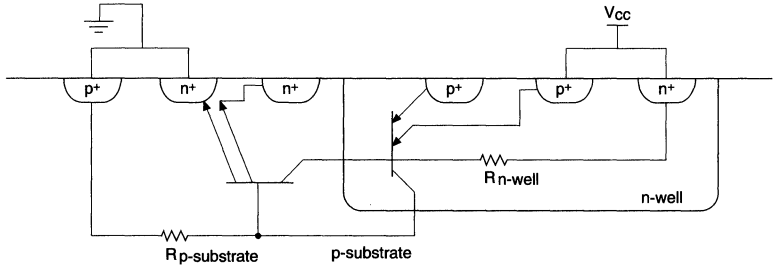
16507C-059

Figure 38. Positive Overshoot Filter

LATCH-UP

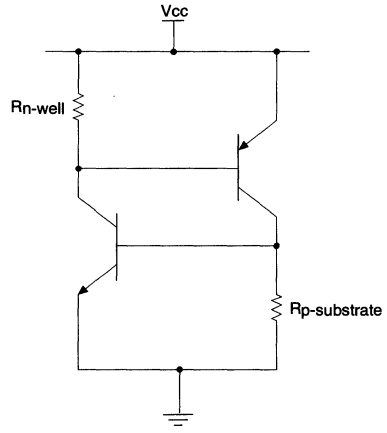
Latch-up occurs as a result of parasitic bipolar transistors between the n-channel and p-channel devices (see Figure 39a). These transistors form a parasitic SCR (see Figure 39b), which turns ON when triggered, conducting large amounts of current. It is usually impossible to shut OFF without removing all power from the device. The amount of current drawn is so high that it can either overload a power supply or, if the power supply can supply huge amounts of current, destroy the device.

Latch-up is normally triggered by an input or output at a voltage significantly above V_{CC} or below ground, with enough current drawn to cause the SCR to turn on. This condition usually occurs when hot socketing a vulnerable part; i.e., plugging a part into a powered-up board or inserting a board into a powered-up system. When this happens, the inputs and V_{CC} power up uncontrolled, and there is a risk of latch-up.



a. Cross-section

16507C-060



b. Equivalent schematic

16507C-061

Figure 39. Latch-up Mechanism

TTL-compatible outputs are intrinsically less susceptible to latch-up, since they have no p-channel pull-up. This accounts for nearly all of Vantis' CMOS PLDs; these devices can be used for hot-insertion.

For true CMOS outputs, the SCR is an intrinsic part of the CMOS structure and cannot be eliminated. The SCR must be made as difficult as possible to turn ON by using guard rings and very carefully laying out input and output circuits. All of Vantis' CMOS devices are guaranteed to endure a current pulse of 100 mA into or out of the pin without inducing latch-up; most devices can actually withstand over 500 mA.

GROUND BOUNCE

Because CMOS devices generally have higher output slew rates, designs having many outputs switching at the same time (particularly if the outputs are heavily loaded) can cause more ground bounce than that generated by a comparable TTL device. It is important to use devices with output slew rate control.

The slew-rate-limiting circuits help minimize the occurrence of conversion problems, but even when the output slew rate is limited, the signal still can switch more quickly than that from a TTL output. If a design cannot be modified to accommodate the faster edge rates, this ground bounce may make a conversion unfeasible. If design changes are possible, any of the following can be tried:

- Limit the number of outputs that can switch at once.
- Reduce the loading on the outputs.
- Go to a lower-lead-inductance package (like a PLCC).
- Ensure that the ground path on the circuit board has low inductance.

OVERSHOOT

The other possible problem when converting from bipolar to CMOS is reaction to signal overshoot in a noisy system. This is only an issue if the CMOS device has no overshoot protection. Overshoot sensitivity is not specifically related to CMOS, but results from programming algorithms being different between the technologies. This also can occur when changing between bipolar vendors, or when changing between CMOS vendors. If the noise on a signal can disturb supervoltage circuitry, this can be troublesome.

Different devices have different sensitivities; this accounts for some of the apparent incompatibility. However, the culprit usually is the fact that supervoltages appear on different pins for different devices, and the supervoltage functions vary. Thus, overshoot on one pin of a particular bipolar device might have had no effect. Once that device is changed (whether to CMOS or any other device that has no overshoot filter), the new device might react to the overshoot and cause problems.

The solution is to ensure that all signals are clean and have minimal overshoot, making them compatible with any device. Signal noise reduction can be accomplished most effectively by controlling the impedance of the signal traces and terminating correctly. As an alternative, if the driving device has extremely fast edge rates, it can be replaced with a device that has better controlled output slew rates.

SUMMARY

By concentrating on the needs of CMOS PLD users, Vantis has developed industry-leading CMOS technology that can provide cost-effective PLDs of unequalled quality, reliability, and performance. Vantis provides value through:

- State-of-the-art fabs, for better control of quality, reliability, volume, and costs
- Electrical erasure, for higher quality and lower cost
- The highest performance available
- Robust technology that is quiet and yet tolerant of noise
- An extremely broad offering of products; low and high density, low and zero power

This information has detailed many of the aspects of the technology that make it superior to any alternatives.

VANTIS

BEYOND PERFORMANCE

Product Reliability Monitoring Program

INTRODUCTION

Vantis is committed to providing products with unequaled product reliability. Throughout the life of our products, from technology development and product design to volume manufacturing, the reliability is constantly monitored to ensure our products meet exacting standards. The core of the production monitoring process is the Qualification Maintenance Program.

Vantis Qualification Maintenance Program (QMP)

Vantis' Qualification Maintenance Program is used to measure the reliability of all process technologies used on a regular basis. This program monitors the EEPROM wafer fabrication technologies used to manufacture Programmable Logic Devices. The program also provides extensive coverage of packaging technologies through environmental stress tests. Typically about 2500 devices per month are subjected to a battery of reliability stress tests with interval electrical testing.

The Qualification Maintenance Program has two purposes:

1. Improved Reliability Performance

Vantis maintains a Zero Tolerance mentality regarding defective units identified during reliability testing. Every reject is analyzed to determine the root cause of failure in order to drive continuous improvement through the implementation of corrective actions. Improvements in processing and device design are developed from the analysis of failed devices.

2. Generation of Reliability Data

QMP test results are used to assess the benefits of production burn-in, estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

Qualification maintenance testing is conducted on representative samples of devices from each wafer fabrication process technology. Samples are pulled from each process technology on a monthly basis. The sampling plan includes all technologies from all wafer foundry locations to ensure complete coverage. Devices are selected on the basis of complexity, production volume, and strategic importance. Process, package and product reliability qualification are used to determine device selection.

Devices that represent a design and technology family per EIA/JEDEC specifications are used on high volume technologies. This process and design grouping results in larger sample sizes so reliability assessment is statistically significant.

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QMP TESTS AND TEST CONDITIONS

A variety of stress testing is used to measure device reliability. The stress test employed and the test conditions used are shown in the table below.

Table 1. Reliability Monitor Stress Conditions

Stress	Readpoints	Sample Size (Typical)	Ambient Conditions	
			Hermetic	Plastic
Early Life	48,168 hours	600	150°C	150°C (Note 1), 125°C
HAST	96 hours	50	N/A	85% RH, 18 PSI, 130°C
Inherent Life	1000 hours	120	150°C	150°C (Note 1), 125°C
Temperature Cycle	100,1000 cycles	50	-65°C to 150°C	-65°C to 150°C, -40°C to 150°C (SMT)
Temperature Humidity Bias	1000 hours	50	N/A	85°C & 85% RH, 5V
Steam Pressure Pot	168 hours	50	N/A	121°C, 15 psig, no bias

Note:

1. Devices dissipating low power are life tested at 150°C

Plastic surface mount devices are pre-conditioned prior to undergoing temperature cycling and biased temperature and humidity stressing. Pre-conditioning is required in order to simulate the stresses that the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. A convection reflow profile and the pre-conditioning flow are shown below.

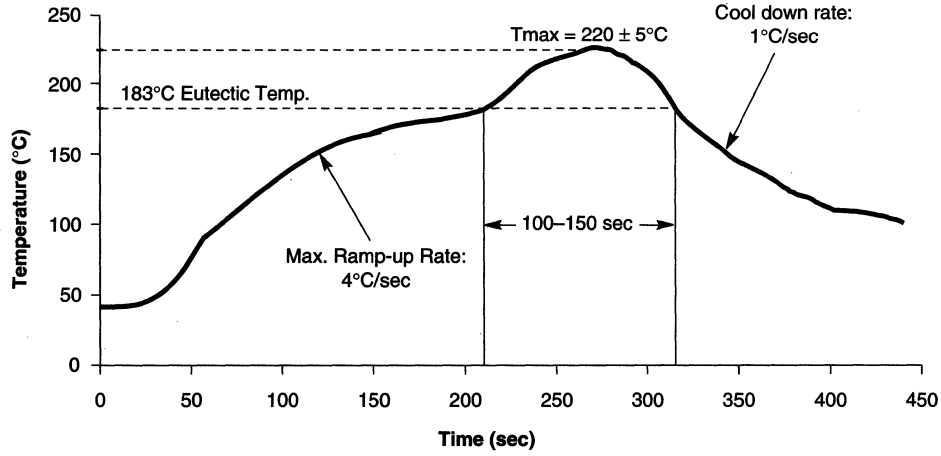

Figure 1. Reflow Soldering Profile for IR & Convection Oven

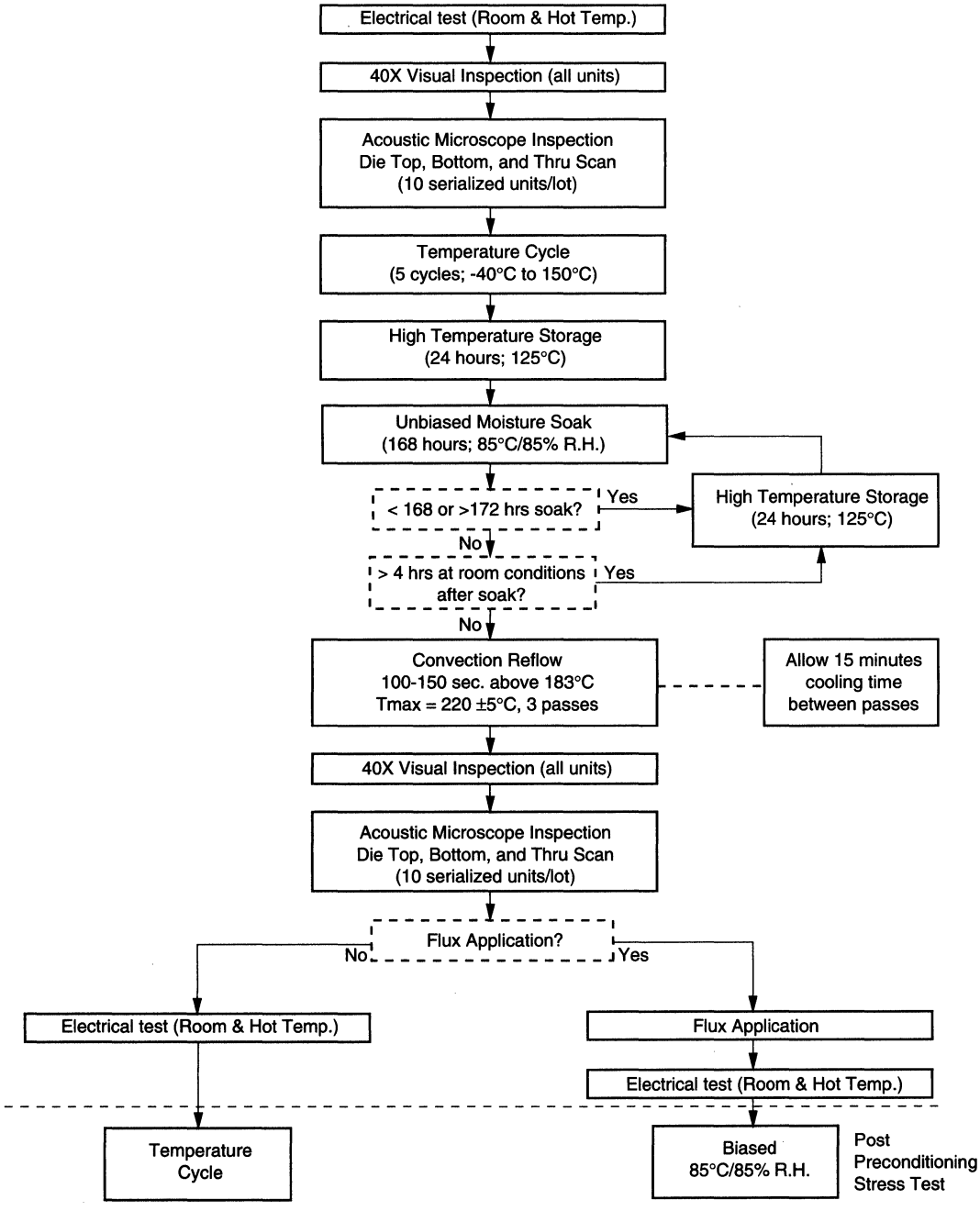

Figure 2. Standard Preconditioning Flow for Non-Dry-Packaged Packages

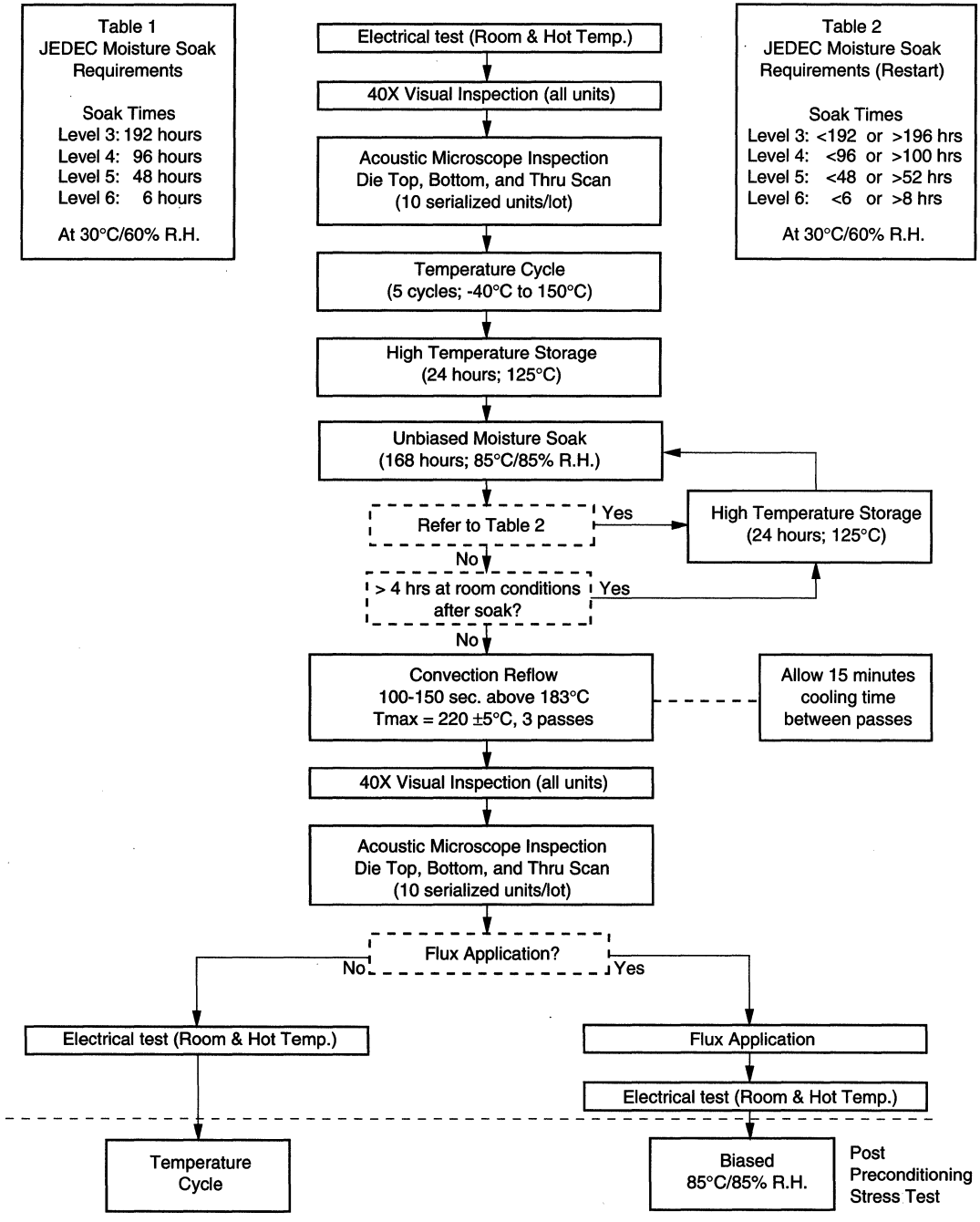

Figure 3. Standard Preconditioning Flow for Dry-Packaged Packages

FAILURE ANALYSIS

Every reject that is encountered during the course of QMP stress testing provides an opportunity for continuous improvement through identification and elimination of root cause. Additionally, there is a significant opportunity to understand the cause of variance in products, even while they meet specifications.

Failure analysis in the semiconductor industry has evolved towards a more thorough understanding of the device physics of the underlying process technologies. Different skills, knowledge and tools are also required to analyze defects that exhibit no morphology using conventional failure analysis techniques.

Electrical failure analysis of Vantis finished products is done by five Device Analysis Laboratories located around the world. A cooperative arrangement with suppliers of device analysis services allows Vantis to provide this capability world-wide. Two analysis sites are located in the United States: Austin and Sunnyvale; two are located in Asia Pacific: Penang, Malaysia and Bangkok, Thailand; and one in Frimley, England. These laboratories serve our local sites and customer base by providing analytical services on packaged devices. This includes analysis of our sub-micron products from qualification stresses, qualification monitor stresses, quality test failures, customer returns, and engineering evaluations.

All five of the laboratories have Scanning Electron Microscopes (SEMs) with X-ray analysis systems (EDX) attached. Sunnyvale and Austin have Field Emission SEMs with significantly enhanced resolution capability and windowless EDX detectors for extended analytical capability. Most sites have Scanning Acoustic Microscopes (SAMs) and X-ray capability for package evaluation. Austin, Sunnyvale, and Penang have e-beam microprober capability, which provides access to signals deep within a device. The same laboratories also have Focused Ion Beam (FIB) capability, which is used during new device debug (cutting and deposition of metal lines allowing for circuit modification) and for failure analysis where probe points can be created and where micro precision cuts aid in cross sectioning.

Other tools common to all labs include automatic decapsulation capability for plastic devices, both wet chemical and dry delayering (plasma and Reactive Ion Etch), optical microscopes with cameras, mechanical probe stations to electrically examine inside a device being evaluated, laser systems for circuit isolation, and polishing wheels for die and package cross sectioning. Each lab has a Layout Tool to provide engineers access to the physical layout drawings of the device that they are evaluating.

RELIABILITY DATA/ANALYSIS

The reliability data generated from the Qualification Maintenance Program (QMP) is used to predict field reliability. A detailed description of the modeling procedure used for estimating reliability under field conditions follows.

Average failure rates are calculated for time periods related to both early life and inherent life. The early life period corresponds to approximately the first 4,000 hours at field use conditions. The inherent life corresponds to the useful life beyond the first 4,000 hours of field operation. For these calculations, device operation temperature is assumed to be 55°C ambient. Voltage acceleration factors are used in the analysis wherever applicable.

The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated, and it is simply the reciprocal of the failure rate (λ). In addition, it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-piece sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

The conventional expression for the failure rate, λ, is:

$$\lambda = \frac{\chi^2(2n+2, 1-\alpha) \times 10^9}{2 \times ss \times t \times AF}$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2,1-\alpha)/2$ is the upper confidence value for "**n**" failures and upper confidence limit, α (expressed as a decimal value), **SS** is the sample size, **t** is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature

The χ^2 (chi square) value for 2n+2 degrees of freedom and the probability, 1-α, can be obtained from a table or calculated using Microsoft Excel chi squared inverse function [=CHIINV(1-α,2n+2)].

Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T50, the median time to failure, and sigma, the shape parameter. The Weibull distribution, which can be written in closed form as:

$$F(t) = 1-exp[-(t/c)^m],$$

is characterized by a characteristic life, c, and a shape parameter, m. The value of the shape parameter determines whether the failure rate is increasing (m>1), decreasing (m<1), or constant (m=1). The exponential distribution:

$$F(t) = 1-exp\ [-(t/c)],$$

is specified completely by the one parameter, c, called the mean time to failure (MTTF). Figures 4 and 5 show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

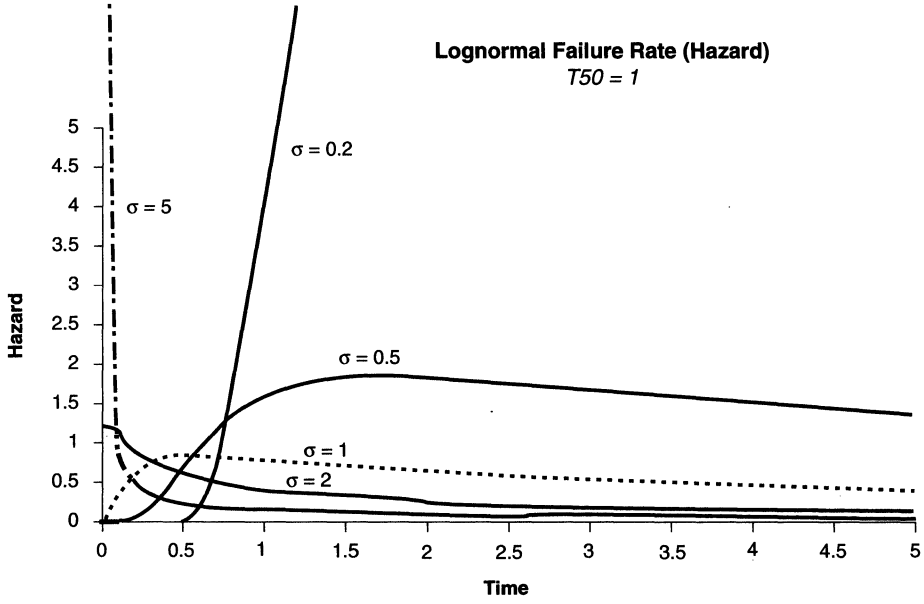

Figure 4. Lognormal Distribution

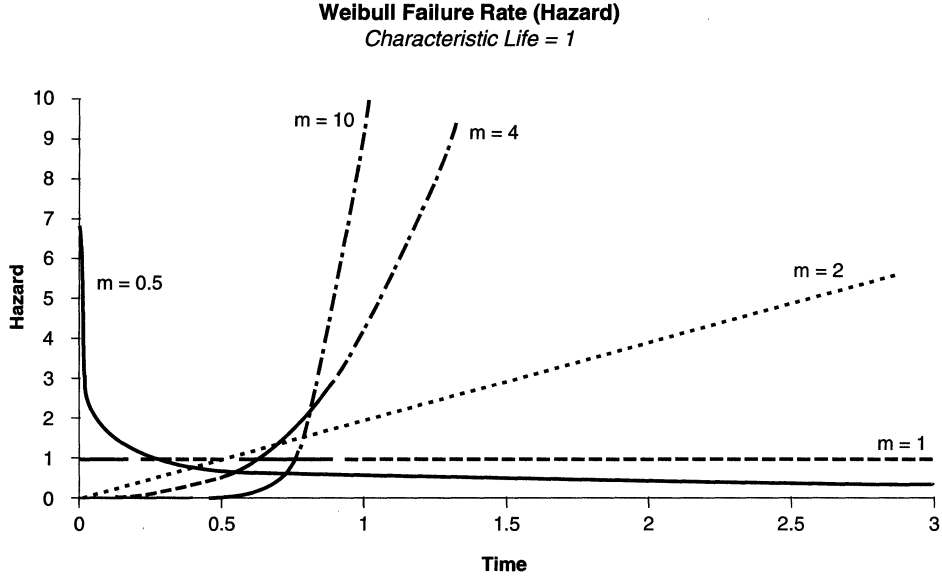

Figure 5. Weibull Distribution

Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Vantis reliability model.

Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

   In any production lot, a defective subpopulation may exist. These are devices that fail by a mechanism not common to the general population which is usually the result of some processing error or defect. These failures usually occur early and consequently are called Early Life failures. Early Life (EL) is defined as 4,000 field equivalent hours (FEH) -- actual life test hours multiplied by the acceleration factor for the mechanism.

   The early life failure rate will be reported in FITs (failures per billion unit-hours).

   Early Life failures will also be reported as DPM (defects per million) for 4,000 hours. The DPM value is obtained by multiplying the EL failure rate in FITS by 4,000 and dividing the result by 1,000 to obtain the EL failure rate as defects per million.

2. Inherent Life failures:

   Failures that occur in excess of 4,000 equivalent field hours are usually by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life (IL) failures. If the first read-time in a life test is equivalent to greater than 5,000 hours for a given mechanism, the data will be considered IL data, and unless there is no failure at this time,

it will be considered that no data exists for this mechanism for Early Life. If this first read-time has zero fails, Early Life will be calculated at 4,000 hours assuming no fails.

3. Estimation of thermal acceleration factors:

   The best known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration:

   Certain failure mechanisms are accelerated by voltage stresses above normal operating voltage. The formula for voltage acceleration is shown below:

$$VAF = exp[\{230\ \gamma\ (V_s - V_n)/T_{ox}\}]$$

   VAF is the voltage acceleration factor, $\mathbf{V_s}$ is the test voltage, $\mathbf{V_n}$ is the nominal operating voltage, $\mathbf{T_{ox}}$ is the oxide thickness in Å, and gamma (γ) is a constant of value "3" for oxide defect related mechanisms or "1" for intrinsic oxide related ones.

   For charge gain (floating gate devices), VAF varies just as the exponential of the voltage difference.

5. It is common in the reliability literature to see failure rates stated at a specified level of confidence:

   For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chance (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%.

VANTIS

BEYOND PERFORMANCE

Packages

INTRODUCTION

Vantis provides its programmable logic devices (PLDs) in a wide range of packages. These packages provide benefits such as high power dissipation capability, small footprint, and high I/O. This section provides details about the packages that Vantis supplies.

EXTERNAL LEAD DESIGNS

The shape of the leads on leaded surface-mount packages, which includes all but the BGA package, are formed in either a gull-wing or J-bend shape. Both lead shapes offer the advantage of being flexible, which allows them to absorb thermal expansion mismatches between the IC package and the board.

Plastic Package Design	Leadcounts	Lead Design/Direction
Leaded Chip Carrier (PLCC)	20—84 leads	J-Bend/4 sides
Quad Flat Pack (PQFP)	100—240 leads	Gull-wing/4 sides
Thin Quad Flat Pack(TQFP)	44—176 leads	Gull-wing/4 sides
Ball Grid Array (BGA)	256—352 balls	Solder Balls/Array
Plastic Dual-In-Line (PDIP)	20—28 leads	Through-hole
Small Outline Plastic (SOIC)	20—24 leads	Gull-wings/2 sides

- Gull-Wing Lead Design

  Gull-wing leads are similar to dual-in-line, through-hole leads except that the leads are bent at the tips to rest flat on the board surface. This provides a built-in standoff between the package and the board, enabling thorough board cleaning and easy-to-inspect solder joints.

- J-Bend Lead Design

  Like the gull-wing design, J-bend leaded packages can be mounted directly to the board, thus offering a built-in standoff and all the advantages inherent in this. A strong, inspectable bond is easily attainable provided the solder lands include extensions out from under the package. The J-bend design also allows easy socketing, which facilitates device testing and programming.

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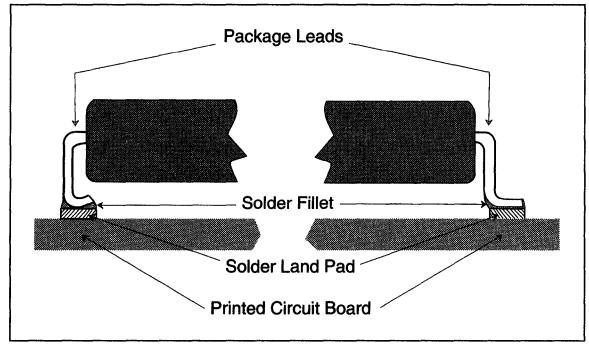

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Figure 1. J-Bend (On the Left) and Gull-Wing Lead Formations (On the Right) Allow Components to be Mounted onto the Surface of the Circuit Board

PACKAGE MATERIALS

The materials used in Vantis' plastic packages and flammability data are provided in this section.

Table 1. Flammability Ratings per Package Type and Size

Package	Leadcount	Ul Rating & Oxygen Index[1]	Resin Weight Per Unit (grams)	Compound Weight Per Unit (grams)
Plastic Leaded Chip Carriers (PL, PLH)	20 (PL)	94 V-0 & ≥28%	0.1	0.6
	28 (PL)		0.2	1.0
	44 (PL)		0.5	2.0
	68 (PL)		1.1	4.4
	84 (PL)		1.8	7.3
	84 (PLH)		1.4	5.8
Metric Plastic Quad Flat Pack (PQR)	100 (PQR)	94 V-0 & ≥28%	0.3	1.4
	144 (PQR)		1.2	4.8
	160 (PQR)		1.1	4.8
	208 (PQR)		1.2	4.8
Thermally Enhanced Metric Plastic Quad Flat Pack (heat spreader (PRH), heat sink (PQE))	160 (PQE)		0.9	3.8
	208 (PRH)		1.1	4.6
	208 (PQE)		0.9	3.8
	240 (PQE)		0.9	3.97
Thin Plastic Quad Flat Pack (1.0 mm thick (PQT); 1.4 mm thick (PQL) TQFP	44 (PQT)	94 V -0 & ≥ 28%	<0.1	0.1
	48 (PQL)		<0.1	0.1
	100 (PQL)		<0.1	0.3
	144 (PQL)		<0.1	0.7
	176 (PQL)		<0.1	0.7
Plastic Ball Grid Array	256 (BGD)	substrate: UL 94V-O glob top: UL 94HB	0.07 (Note 2)	0.26 (Note 3)
	352 (BGD)		0.12 (Note 2)	0.45 (Note 3)
Plastic Dual-In-Line	20	94 V -0 & ≥ 28%	0.3	1.2
	24 (PD3) (Note 3)		0.3	1.5
	28 (PD3) (Note 3)		0.4	1.6
Small Outline Plastic	20		<0.1	0.2
	24		<0.1	0.2

Notes:

1. *The mold compound is tested according to the ASTM Standard D2863-77,:Standard Method for Measuring Oxygen Concentration to Support Candlel-Like Combustion of Plastics (Oxygen Index)." The flammability rating is determined by the Underwriters Laboratories (UL) Standard 94, "Test for Flammability of Plastic Materials for Parts in Devices and Applications.*
2. *Refers to the weight of the glob-top encapsulation.*
3. *PD3 (300-mil) designates a PDIP design for which the package mil size is not what is standard for that lead count.*

Table 2. Package Materials [1]

Package Type & Leadcount	Package Part		Material	Percentage of Composition[2]
All Plastic Surface Mount Packages (excluding Ball Grid Array Packages)				
All Package Types and Lead Counts	Package body		epoxy novolac	13.0%—30.5%
			silica filler	69.5%—87.0%
			chlorine	7—80 ppm
			bromine	0.0%—0.9% weight
			antimony trioxide	0%—1.8%
			sodium	5—40 ppm
			potassium	0—10 ppm
	Die attach adhesive		epoxy	20%—30%
			silver filler	80%—70%
			sodium	5—50 ppm
			chlorine	5—50 ppm
			potassium	5—20 ppm
	Die-to-package interconnections	bond wire	gold	99.99%
	Leadframe	copper	copper	96.2%—99.9%
			nickel	3.0%
			iron	0.005%—2.35%
			silicon	0.65%
			magnesium	0.15%
			zinc	0.12%
			zirconium	0.0%—0.15%
			phosphorous, aluminum, manganese	traces, depending on the leadframe supplier
	Lead plating		tin/lead	85%, +5%, -0%/15%, -5%

Notes:

1. *Excluding the die*
2. *Ranges are provided in some cases, to cover the differences in materials per supplier. Contact your local Vantis sales representative for more product specific information.*

Table 3. Package Materials [1]

Package Type & Leadcount	Package Part		Material	Percentage of Composition [2]
Ball Grid Array Packages				
All Plastic Package Versions	Package body	substrate	organic resin	40%—60%
			glass fibers	40%—60%
		circuitry	copper (Note 3)	99%—100%
		solder mask	resin	40%—60%
			inorganic fillers	35%—55%
			additives	1%—10%
	Die attach adhesive		epoxy	20%—30%
			silver filler	70%—80%
	Die-to-package interconnections	bond wire	gold	99.99%
	Package-to-board outerconnections	solder balls	tin, lead	63%, 37% (eutectic)
	Glob top encapsulation		epoxy resin	20%—40%
			silica filler	60%—80%
	Heat spreader		copper	96%—99%
			iron	0%—2.4%

Notes:

1. *Excluding the die*
2. *Ranges are provided in some cases to cover the differences in materials per supplier. Contact your local Vantis sales representative for more product specific information.*
3. *The internal leads are electroplated with nickel, copper, and gold. These percentages vary depending on the specific package. Contact your local Vantis sales represenative should you need product specific information.*

Table 4. Materials Not Detectable in Vantis' Plastic Components

4-Aminodiphenyl and its salts	Hydrazine	Polyhalogenated Dibenzofurans/Dioxins
Ammonium Salts	2-Naphthylamine and its salts	Polychlorinated Naphthalenes
Arsenic	Nickel Tetracarbonyl	Polycyclic Compounds
Asbestos	N, N-Dimethylformamide	Selenium
Benzene	N, N-Dimethylacetamide	Tetrabromobenzylimidazole
Brominated Diphenyl Oxides	N-Nitrosoamines	Tetrabromobisphenol A
Cadmium and Cadmium Compounds	Mercury and Mercury Compounds	Tetrabromoethylene
Decabromodiphenyl Ether	Ozone Depleting Compounds	Toluene
4, 4-Diaminophenyl Methane	Octabromodiphenyl Ether	Triethylamine
Epichlorhydrine	Oils and Greases	Tris (2, 3-Dibromopropyl) Phosphate
Ethylene Glycol ethers	Palladium	Tris (aziridinyl) Phosphin Oxide
Fluorine	Phthalate	Vinyl Chloride Monomer
Formaldehyde	Halogenated Aliphatic Hydrocarbons	Xylene
Halogenated Aliphatic Hydrocarbons	Polyhalogenated Bi/Triphenyl Ethers	

Thermally Enhanced Plastic Package Designs

In addition to the standard package designs, Vantis' PLCC and PQFP package families include high-performance variations for devices having greater power and faster speed. We are also evaluating high-performance designs in our TQFP and BGA package families.

The high-performance package designs include two variations: one in which a heat spreader is embedded in the package, and the other entails assembling into the package a heat sink which is visible on the topside of the package.

Heat Spreader Design

This design includes a heat sink that is attached to a padless leadframe using a B-stage adhesive. The heat sink, referred to in this design as a heat spreader because it serves as the die attach pad, fills the narrow gap between where the die-attach pad would normally end and the leads begin. This provides a more efficient means of heat transferal since heat from the device no longer has to pass over a gap to escape to the leadframe. Also thermally advantageous, a thin strip of insulating tape in the B-stage epoxy allows the heat sink to be quite close to the leadframe without actually touching it (since to do so would cause an electrical short.

The heat sink also serves as a fixed potential plane in that its voltage level will not vary much from the voltage on the back of the die. Because the heat sink is underneath the die, separated from it by only the epoxy and the 0.003-inch thick insulating tape, it is closer to all the input/output, power, and ground leads than in a standard PLCC package (in which the closest ground is on the circuit board, ≈0.090 inch below the leads). This significantly lowers lead inductance which keeps the noise level down.

Comparative analysis of package performance using the same device in a standard versus a high-performance PLCC package have shown the latter to outperform the standard package in the areas of lead inductance, thermal impedance (θ_{ja}), speed, and yields.

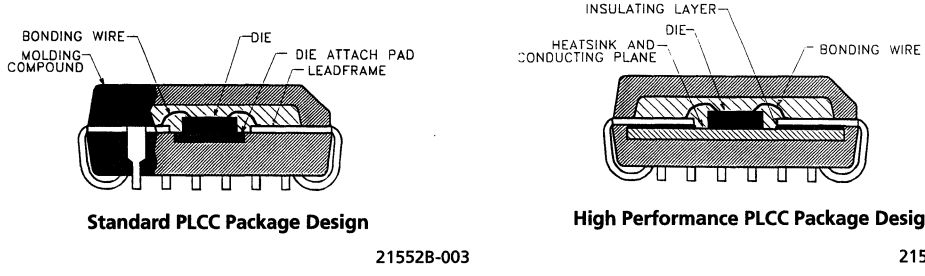

Figure 2. A High-Performance PLCC Package Includes a Heat Spreader Within the Package—a Feature not Present in a Standard PLCC Package Design

Exposed Heat Sink Design

For very high-power devices, it is necessary that the heat sink conduct the heat all the way to the surface of the IC package. For such devices, a much thicker heat sink is used to span the entire encapsulated portion of the leadframe. This design can be achieved in either a cavity-down version (see Figure 3), in which the heat sink is visible on the top of the package, or a cavity-up version,

in which the heat sink is exposed on the package bottom (Figure 3). This style of heat sink is sometimes referred to as a heat slug, since the metal comes in contact with the chip itself (as opposed to a heat sink that is attached to the exterior of the package body).

Thermal Performance Improvement

The improvement in thermal performance for, say, a 28-mm body PQFP, is approximately 30 percent for the heat spreader design and 60 percent for the exposed heat sink version.

Contact your Vantis sales representative should you need additional information about Vantis' high-performance plastic package designs.

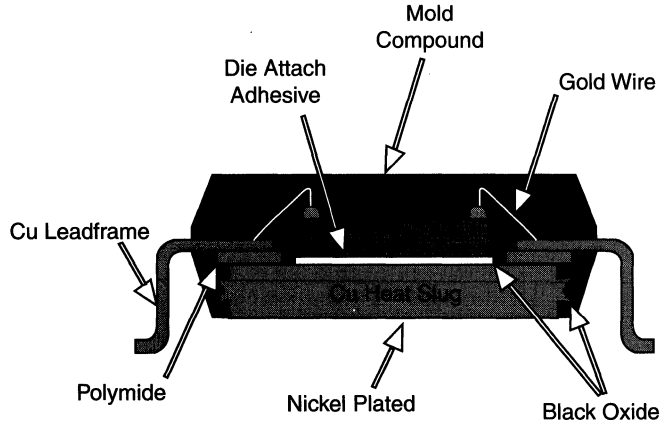

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Figure 3. A Heat Sink Assembled in a Thermally Enhanced PQFP (Known as PQE Package) is Visible on the Bottom Side of the Package

Plastic Leaded Chip Carrier (PLCC) Packages

The PLCC package design is an attractive alternative to higher leadcount plastic DIPs because it can accommodate larger die sizes and offer the advantages of SMT. Above 84 leads, the PLCC configuration and lead-pitch are impractical given the availability of lower profile, high leadcount packages, such as finer pitch PQFPs.

The PLCC package construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The quad-directional leads are trimmed and formed to a J-bend formation.

The 50-mil lead-pitch of a PLCC package is half the conventional lead spacing of a DIP. This, coupled with the PLCC leads being located on all four sides of the package, greatly reduce the footprint. A comparison of package dimensions is shown in Table 5.

Table 5. PLCC (PL) [1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches SQ.	Lead Pitch Inches	Package Weight (Grams)
20	0.125	0.05	0.65
28	0.205		1.07
44	0.426		2.22
68	0.908		4.62
84	1.33		7.45

Note:

1. PL is Vantis' internal abbreviation for a PLCC package.

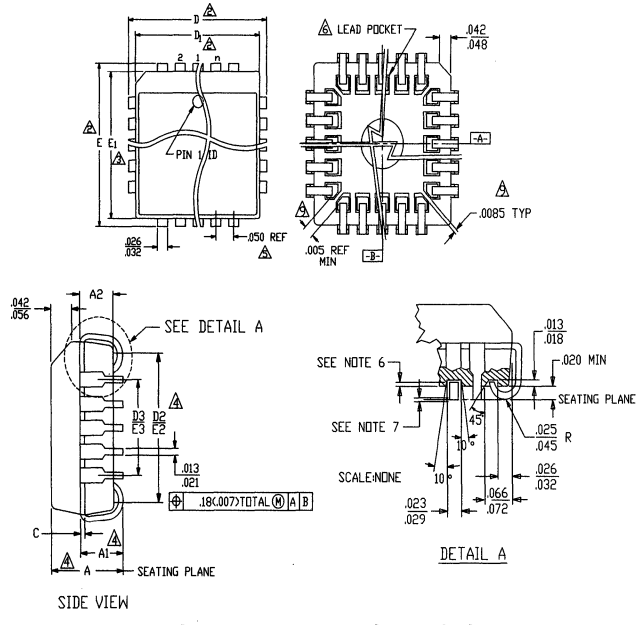

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Figure 4. Square Packages (PL)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)									
	PL 020		PL 028		PL 044		PL 068		PL 084, PLH084	
	(MS-018(A)AA)		(MS-018(A)AB)		(MS-018(A)AC)		(MO-047(B)AE)		(MO-047(B)AF)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180
A1	0.090	0.120	0.090	0.120	0.090	0.120	0.090	0.130	0.090	0.130
A2	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083
D, E	0.385	0.395	0.485	0.495	0.685	0.695	0.985	0.995	1.185	1.195
D1, E1	0.350	0.356	0.450	0.456	0.650	0.656	0.950	0.956	1.150	1.156
D2, E2	0.290	0.330	0.390	0.430	0.590	0.630	0.890	0.930	1.090	1.130
D3, E3	0.200 REF		0.300 REF		0.500 REF		0.800 REF		1.000 REF	
C	0.009	0.015	0.009	0.015	0.009	0.015	0.007	0.013	0.007	0.013

Notes:

1. *All dimensions are in inches.*
2. *Dimensions "D" and "E" are measured from the outermost point.*
3. *Dimensions "D1" and "E1" do not include corner mold flash. Allowable corner mold flash is 0.010 inch.*
4. *Dimensions "A, A1, D2, and E2" are measured from the points of contact to the base plane.*
5. *Lead spacing as measured from the center-line to the center-line shall be within ±0.005 inch.*
6. *J-bend lead tips should be located inside the "pockets."*
7. *Lead coplanarity shall be within 0.004 inch as measured from the seating plane.*
8. *Lead tweeze shall be within 0.0045 inch on each side as measured from a vertical flat plane.*
9. *The lead pocket may be rectangular (as shown) or oval. If the corner lead pockets are connected, then 0.005-inch minimum lead spacing is required.*
10. *PL is Vantis' internal abbreviation for a PLCC. PLH refers to one that has been thermally enhanced with an embedded heat spreader.*

Plastic Quad Flat Pack (PQFP) Packages

PQFP packages were developed primarily for high-leadcount applications. The finer lead-pitch of a PQFP enables this design to accommodate higher leadcount devices than desirable in PDIP, PLCC, and SOIC packages. As the benefits of the PQFP package configuration were realized within the industry, the design was extended to lower leadcounts.

The PQFP package construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The quad-directional leads are trimmed and formed to a gull-wing formation.

Vantis' PQFP package family includes a wide range of leadcount variations (from 100 to 240). For the most part, the package designs comply with JEDEC and/or EIAJ package versions. Some of the packages are thermally enhanced with either a heat spreader, embedded in the package body; or an exposed heat sink.

Table 6. PQFP (PQR)[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches SQ. (mm SQ.)	Lead Pitch Inches (mm)	Package Weight (Grams)
100 (PQR)	0.434 (280.0)	0.030 (0.80)	1.66
144 (PQR)	1.215 (784.0)	0.025 (0.65)	5.21, 5.34
160 (PQR)	1.215 (784.0)		5.30
160 (PQE)	1.215 (784.0)		5.37
208 (PQR, PRH)	1.215 (784.0)	0.020 (0.50)	9.53, 9.68
208 (PQE)			10.87
240 (PQE)	1.588 (1024.0)		15.07

Note:

1. *PQR (cavity up) is Vantis' internal abbreviations for metric PQFPs. Thermally ehanced versions are denoted as PRH (cavity up with heat spreaders) and PQE (cavity up with exposed heat sink).*

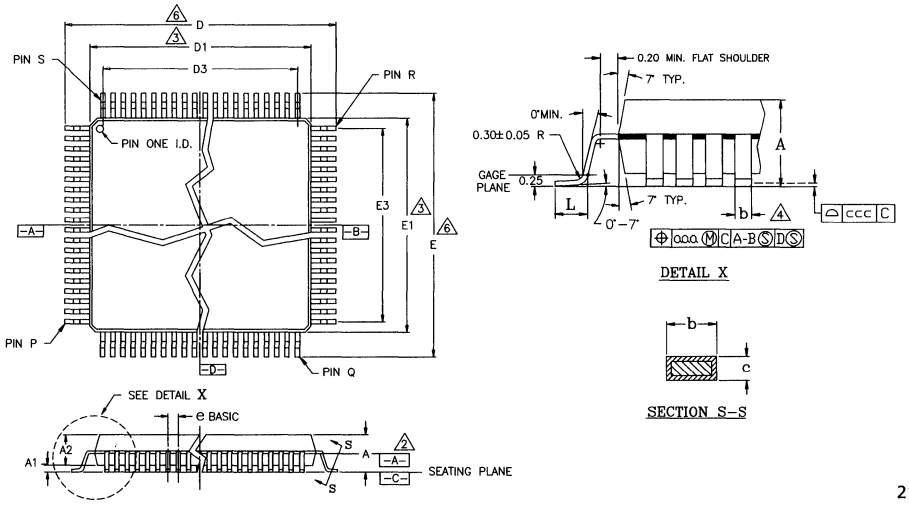


Figure 5. Rectangular Metric, Cavity-Up Packages (PQR)

Dimension Codes	Vantis Package Type & Leadcount PQR, PRH100 (MO-108(B)CC-1) Min	Max
A	—	3.35
A1	0.25	—
A2	2.70	2.90
b (Note 4)	0.22	0.38
c	0.15	0.23
D (Note 5)	17.00	17.40
D1 (Note 3)	13.90	14.10
D3	12.35 REF	
e (Note 7)	0.65 BASIC	
E (Note 5)	23.00	23.40
E1 (Note 3)	19.90	20.10
E3	18.85 REF	
aaa	0.13 NOM	
ccc	0.10 NOM	
L	0.73	1.03
Lead P	30	
Lead Q	50	
Lead R	80	
Lead S	100	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane —A— is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "D1 and E1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (Also see Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "D1 and E1" do include mold mismatch and are determined at datum plane —A—.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.076 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is ≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.076 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip) shall be within ±0.0085.*
10. *PQR is Vantis' internal abbreviation for a metric PQFP.*

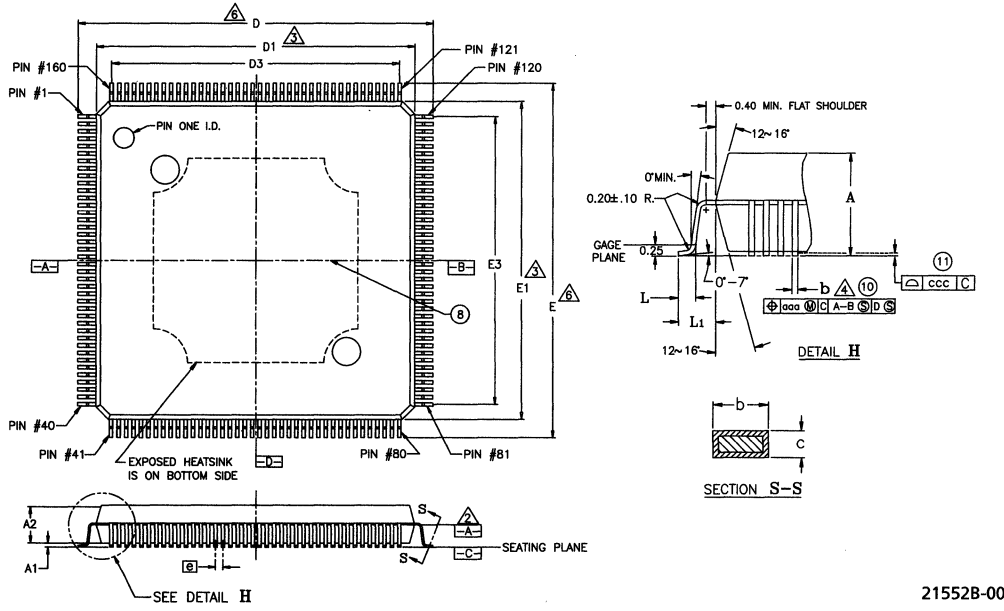
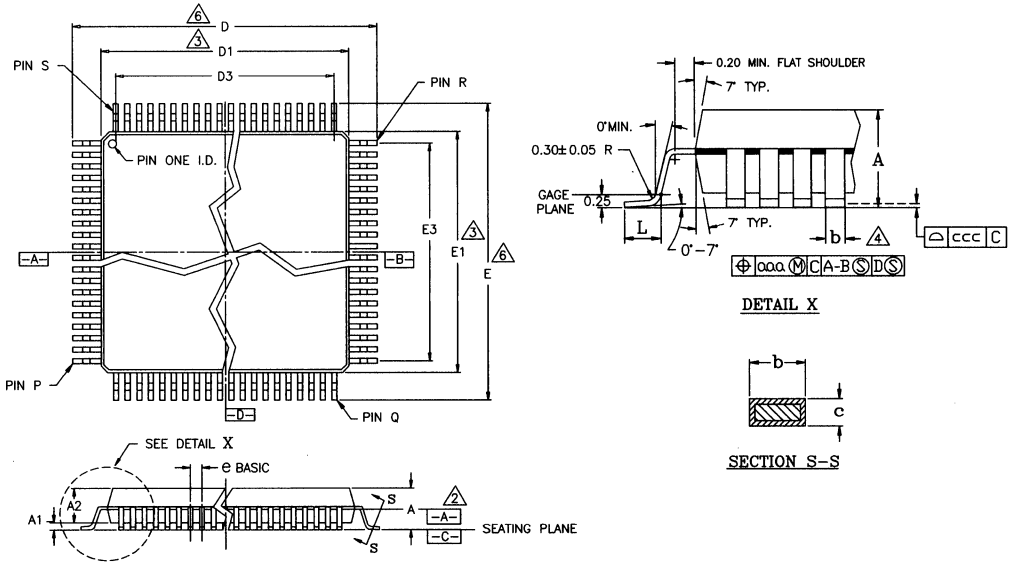


Figure 6. 160-Lead Square Metric, Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE160 (MS-022(A)/DD-2)	
	Min	Max
A	—	4.00
A1	0.25	0.45
A2	3.25	3.45
b	0.22	0.38
c	0.11	0.17
D, E	30.80	31.60
D1, E1	27.90	28.10
D3, E3	25.35 REF	
e	0.65 BASIC	
L	0.73	1.03
L1	1.60 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.10 mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP which has been thermally enhanced with an exposed heat sink.*



(see table of dimensions)

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Figure 7. Plastic Quad Flat Pack (PQFP) Packages

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)					
	PQR 144		PQR160		PQR, PRH 208	
	(MO-108(B)DC-1)		(MO-108(B)DD-1)		(MO-143(B)FA-1)	
	Min	Max	Min	Max	Min	Max
A	—	3.95	—	3.95	—	3.95
A1	0.25	—	0.25	—	0.25	—
A2	3.20	3.60	3.20	3.60	3.20	3.60
b (Note 4)	0.22	0.38	0.22	0.38	0.18	0.30
c	0.13	0.23	0.13	0.23	0.13	0.20
D, E (Note 5)	31.00	31.40	31.00	31.40	30.40	30.80
D1, E1 (Note 3)	27.90	28.10	27.90	28.10	27.90	28.10
D3, E3	22.75 REF		25.35 REF		25.50 REF	
e (Note 7)	0.65 BASIC		0.65 BASIC		0.50 BASIC	
aaa	0.13 NOM		0.13 NOM		0.08 NOM	
ccc	0.10		0.10		0.08	
L	0.73	1.03	0.73	1.03	0.50	0.75
Lead P	36		40		52	
Lead Q	72		80		104	
Lead R	108		120		156	
Lead S	144		160		208	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "D1 and E1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (Also see Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "D1 and E1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.08 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is ≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.08 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip shall be within ±0.0085.*
10. *PQR (cavity up) is Vantis' internal abbreviation for metric PQFPs. Thermally-enhanced PQFPs are denoted by those with heat spreaders embedded in them (PRH for cavity up).*

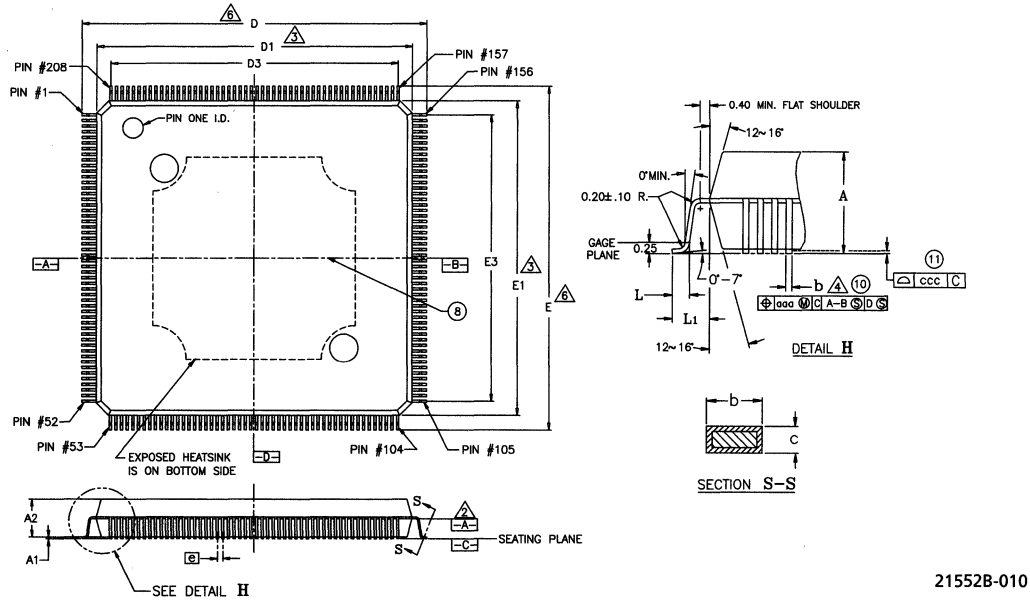

Figure 8. 208-Lead Metric Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE208 (MO-143(B)FA-1)	
	Min	Max
A	—	3.70
A1	0.25	0.42
A2	3.29	3.45
b	0.17	0.27
c	0.10	0.20
D, E	30.40	30.80
D1, E1	27.90	28.10
D3, E3	25.50 REF	
e	0.50 BASIC	
L	0.50	0.75
L1	1.30 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.08 mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP that has been thermally enhanced with an exposed heat sink.*

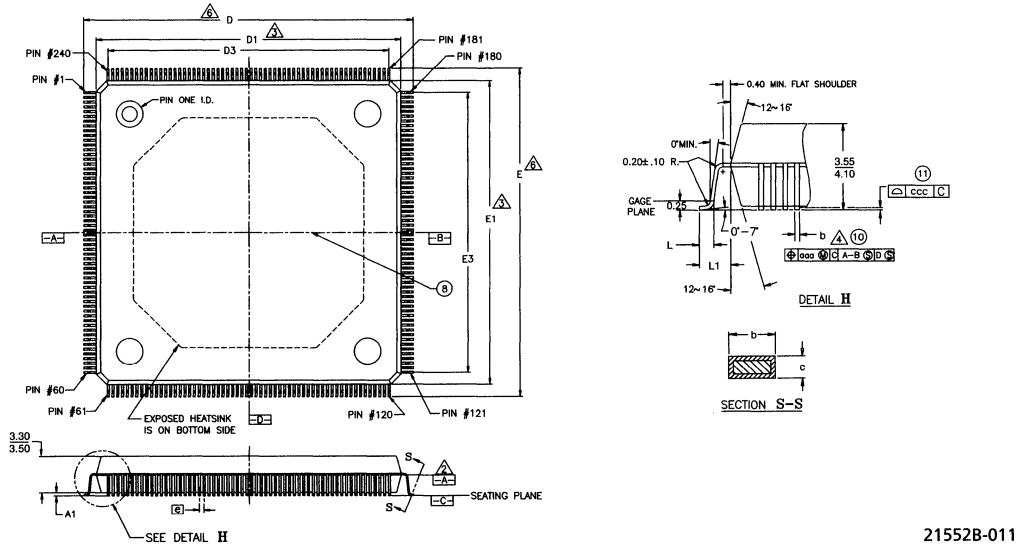

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Figure 9. 240-Lead Metric Cavity-Up Package with a Heat Sink (PQE)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)	
	PQE240 (MO-143(B)/GA)	
	Min	Max
A1	0.25	0.45
b	0.17	0.27
c	0.10	0.20
D, E	34.35	34.85
D1, E1	31.90	32.10
D3, E3	29.50 REF	
e	0.50 BASIC	
L	0.45	0.75
L1	1.30 NOM	
aaa	0.08 NOM	
ccc	0.08 NOM	

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -A- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.25 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -A-.*
6. *Dimensions "D and E" are measured from both the outermost points.*
7. *The pin-one ID may be inside the top ejector mark or separate.*
8. *The heatsink center line is aligned to the package body's center line at a tolerance of ±0.30 mm.*
9. *The half span (center of the package to the lead tip) shall be within 15.30 ± 0.165 mm.*
10. *No lead distortion (bent leads, etc.) shall cause deviation from the lead's true position by greater than ±0.04 mm at the maximum of the "b" dimension.*
11. *Lead coplanarity with respect to the seating plan shall not exceed 0.08mm.*
12. *PQE is Vantis' internal abbreviation for a cavity-up, metric PQFP that has been thermally enhanced with an exposed heat sink.*

Thin Quad Flat Pack (TQFP) Packages

The TQFP package is the same basic package design as a PQFP except the package is thinner, and the dimensions governing the solder land pattern are different. The thickness of the package body is 1.0 mm to 1.4 mm, versus the 3.5-mm thickness of a standard PQFP. This is possible because the die is back ground down to a 0.34-mm thickness.

The major applications for TQFP packages are in handheld products, small disk drives, double-sided boards, and PCMCIA cards.

Vantis' family of TQFP packages includes cavity-up versions (denoted internally as PQT and PQL) from 44 to 176 leads.

Table 7. TQFP[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches Sq. (mm sq.)	Lead Pitch Inches (mm)	Package Body Thickness Inches (mm)	Package Weight (Grams)
44 (PQT)	0.155 (100)	0.03 (0.80)	0.04 (1.00)	0.232
48 (PQL)	0.076 (49)	0.02 (0.5)	0.055 (1.4)	0.17
100 (PQL)	0.304 (196)	0.02 (0.50)	0.055 (1.40)	0.63
144 (PQL)	0.62 (400)	0.02 (0.50)	0.055 (1.40)	1.32
176 (PQL)	0.893 (576)	0.02 (0.50)	0.055 (1.40)	1.82

Note:

1. *PQT is Vantis' internal abbreviation for TQFPs having a package body thickness of 1.0 mm. PQL denotes TQFPs with package body thickness of 1.4 mm.*

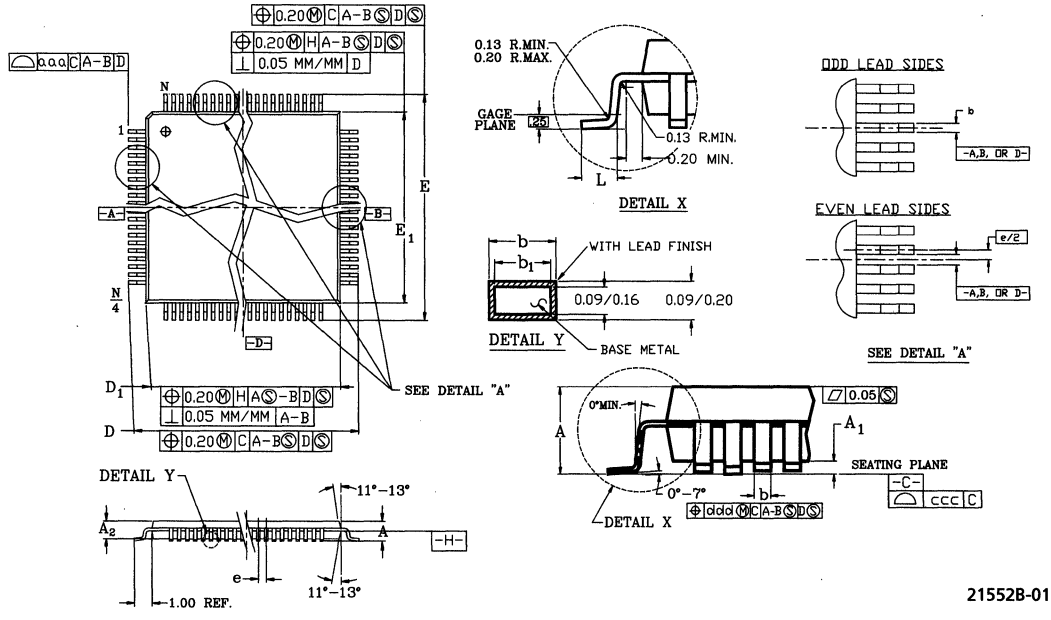

Figure 10. Thin Plastic Quad Flat Pack (TQFP) Packages

Vantis Package Type & Leadcount (JEDEC Drawing Number)										
Dimension Codes	PQT044 (MS-026(A)ACB)		PQL048 (MO-136(B)AE)		PQL100 (MS-026(A)BED)		PQL144 (MS-026(A)BFB)		PQL176 (note 12) (MS-026(A)BGA)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	—	1.20	—	1.60	—	1.60	—	1.60	—	1.60
A1	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.15
A2	0.95	1.05	1.35	1.45	1.35	1.45	1.35	1.45	1.35	1.45
D, E	11.80	12.20	9.00 BASIC		15.80	16.20	21.80	22.20	25.80	26.20
D1, E1	9.80	10.20	7.00 BASIC		13.80	14.20	19.80	20.20	23.80	24.20
L	0.45	0.75	0.45	0.75	0.45	0.75	0.45	0.75	0.45	0.75
N	44		48		100		144		176	
e	0.80 BASIC		0.50 BASIC		0.50 BASIC		0.50 BASIC		0.50 BASIC	
b	0.30	0.45	0.17	0.27	0.17	0.27	0.17	0.27	0.17	0.27
b1	0.30	0.40	0.17	0.23	0.16	0.23	0.17	0.23	0.17	0.23
ccc	—	0.10	—	0.08	—	0.08	—	0.08	—	0.08
ddd	—	0.20	—	0.08	—	0.08	—	0.08	—	0.08
aaa	—	0.20	—	0.20	—	0.20	—	0.20	—	0.20

Notes:

1. *All dimensions are in millimeters, and the dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.*
3. *Dimensions "E1 and D1" do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. (See also Note 5.)*
4. *Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius or the foot.*
5. *Dimensions "E1 and D1" do include mold mismatch and are determined at datum plane -H-.*
6. *Dimensions "D and E" are measured from both the innermost and outermost points.*
7. *Deviation from the lead-tip true position shall be within ±0.076 mm for packages having lead pitch >0.5 mm, and within ±0.04 mm when the pitch is ≤0.5 mm.*
8. *Lead coplanarity shall be within 0.10 mm for devices having lead pitch of 0.65—0.80 mm, and 0.08 mm when the lead pitch is 0.50 mm.*
9. *The half span (center of the package to the lead tip) shall be within ±0.16 mm.*
10. *"N" is the total number of terminals.*
11. *The top of the package is smaller than the bottom of the package by 0.15 mm.*
12. *PQT is Vantis' internal abbreviation for a 1.0-mm thick TQFP. PQL designates a 1.4-mm thick TQFP.*

Ball Grid Array (BGA) Packages

The BGA package is a relatively new package design which is gaining popularity as an attractive package solution for Programmable Logic and FPGA devices. It offers a high-density package with a smaller form/fit factor than a comparable leadcount quad flat pack package. More importantly, it is designed with solder balls instead of leads, which are more durable and loosely pitched than the fragile package leads of a comparable surface-mount component. This results in higher board yields.

Package Design

The package consists of a thin Printed Circuit Board (PCB) made of a BT epoxy laminate, double-sided, and overlaid with copper over which metallized wire bond pads and a die pad are fabricated. The wirebond pads extend outward to plated through-hole vias located around the board's periphery. These vias provide the electrical continuity from the top of the board to the other side where copper traces run from the holes to a matrix of solder bumps. The bumps are soldered onto a land pattern on a circuit board in the end-use application. A solder mask is photo defined on the backside of the package to contain the flow of solder during board assembly.

The die is attached to the die pad using a standard epoxy die attach method. Gold ball bonding is used to connect the die pads to the wire bond pads, and the die is encapsulated with epoxy encapsulation material to protect it.

Table 8. BGA Package Size Overview

Ball Count	Package Body Area (L X W) Inches Sq. (mm sq.)	Ball Pitch Inches (mm)	Package Weight (Grams)
256 (BGD) (Note 1)	1.13 (729.0)	0.05 (1.27)	4.23
352 (BGD) (Note 1)	1.90 (1225.0)		6.99

Note:

1. BGD is Vantis' internal abbreviation for a wirebonded, cavity-down, ball grid array, thermally enhanced with a heat slug

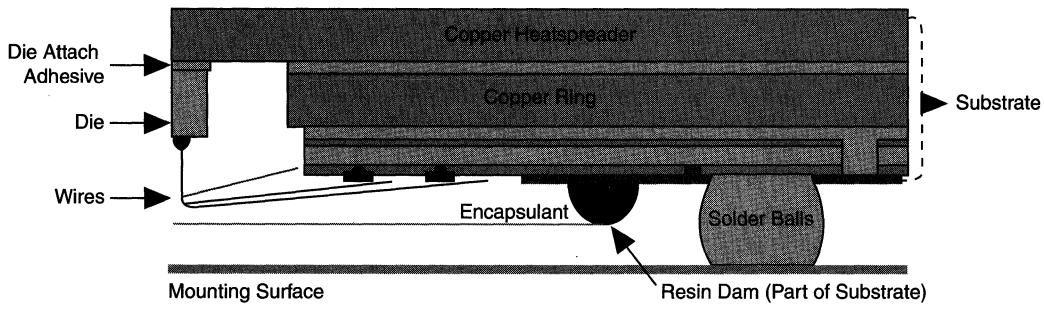

Figure 11. BGD Cross-section

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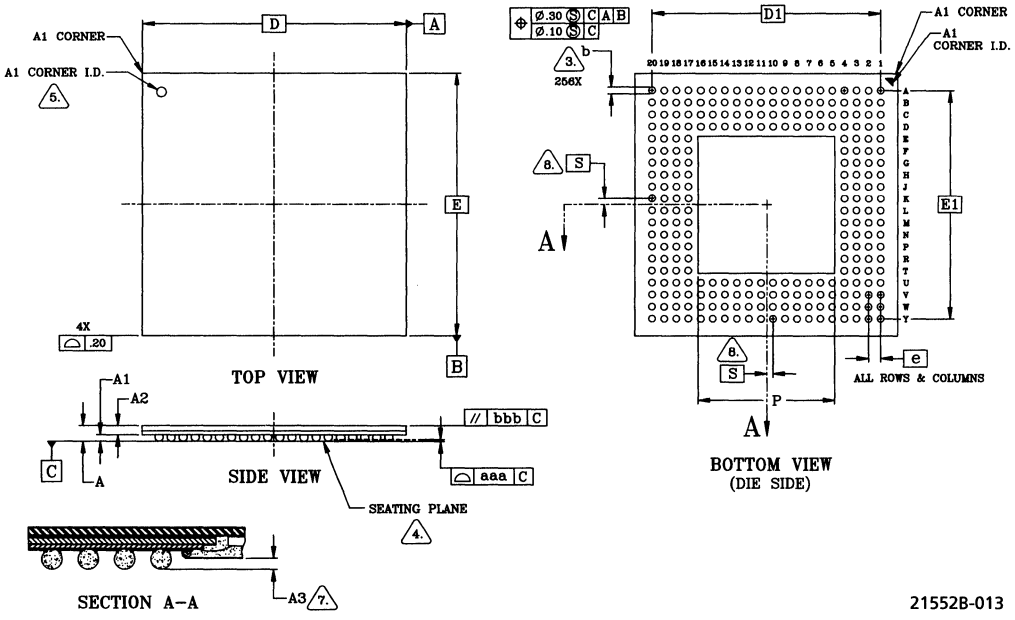


Figure 12. 256-Ball (27 x 27) Cavity-Down Package (BGD)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD256 (MO-151(B)/BAL-2)[1] Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3 (Note 7)	0.15	0.45	seating plane clearance
D, E	27.00 BASIC		body size
D1, E1	24.13 BASIC		ball footprint
M	20 x 20		ball matrix size
N	256		total ball count
MR (Note 6)	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	14.8	15.2	encapsulation area
S	0.635 BASIC		solder ball placement

Note:

1. *BGD is Vantis' internal abbreviation for a wirebonded, plastic, cavity-down ball grid array that has been thermally enhanced with a heat sink.*

Geometric Tolerances		
aaa	0.15	coplanarity
bbb	0.15	parallelism

Notes:

1. *All dimensions are in millimeters.*
2. *Dimensioning and tolerancing conform to ASME Y14.5M—1994.*
3. *Dimension "b" is measured at the maximum solder ball diameter on a plane parallel to datum C.*
4. *Datum C and the seating plane are defined by the spherical crowns of the solder balls.*
5. *A1 corner I.D. is marked with ink.*
6. *Refers to the number of peripheral rows or columns.*
7. *Refers to the height from the encapsulation to the seating plane.*
8. *"S" is measured with respect to datums A and B and defines the position of the solder balls nearest the package centerlines. When there is an odd number of solder balls in the outer row "S" = 0.000; when there is an even number of solder balls in the outer row the value "S" =e/2.*

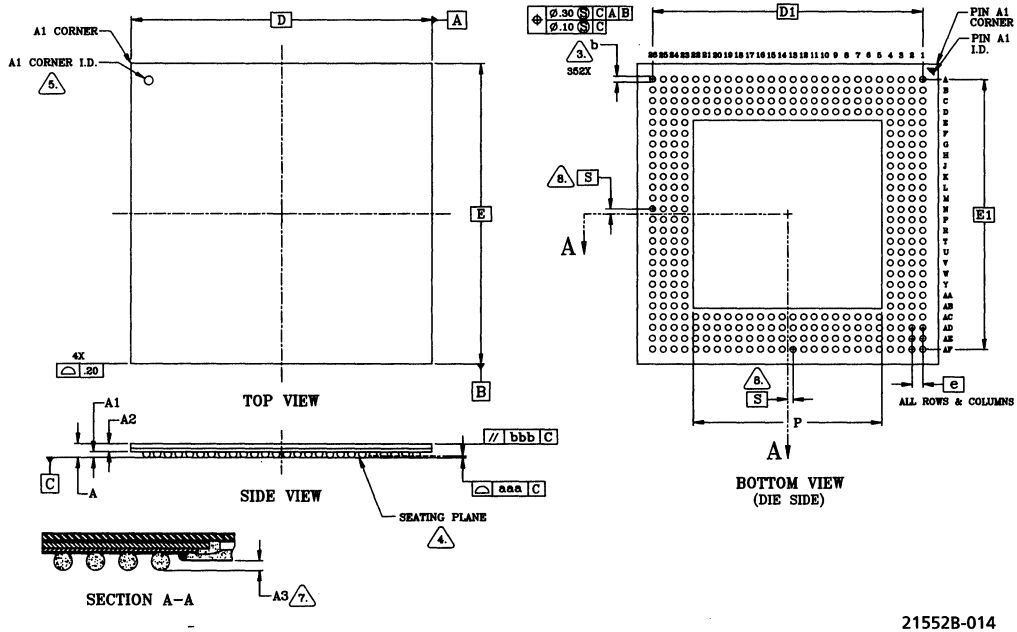


Figure 13. 352-Ball (35 x 35) Cavity-Down Package (BGD)

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number) BGD352 (MO-151(B)/BAR-2)		
	Min	Max	Note
A	1.10	1.65	overall thickness
A1	0.50	0.70	ball height
A2	0.60	0.95	body thickness
A3 (Note 7)	0.15	0.45	seating plane clearance
D, E	35.00 BASIC		body size
D1, E1	31.75 BASIC		ball footprint
M	26 x 26		ball matrix size
N	352		total ball count
MR (Note 6)	4		number of rows deep
e	1.27 BASIC		ball pitch
b	0.60	0.90	ball diameter
P	20.4	21.2	encapsulation area
S	0.635 BASIC		solder ball placement

Geometric Tolerances		
aaa	0.15	coplanarity
bbb	0.15	parallelism

Notes:

1. *All dimensions are in millimeters.*
2. *Dimensioning and tolerancing conform to ASME Y14.5M—1994.*
3. *Dimension "b" is measured at the maximum solder ball diameter on a plane parallel to datum C.*
4. *Datum C and the seating plane are defined by the spherical crowns of the solder balls.*
5. *A1 corner I.D. marked by ink.*
6. *Refers to the number of peripheral rows or columns.*
7. *Refers to the height from the encapsulation to the seating plane.*
8. *"S" is measured with respect to datums A and B and defines the position of the solder balls nearest the package centerlines. When there is an odd number of solder balls in the outer row "S" = 0.000; when there is an even number of solder balls in the outer row the value "S" =e/2.*
9. *BGD is Vantis' internal package abbreviation for a wirebonded, plastic, cavity-up package.*

Plastic Dual-In-Line Packages (PDIP)

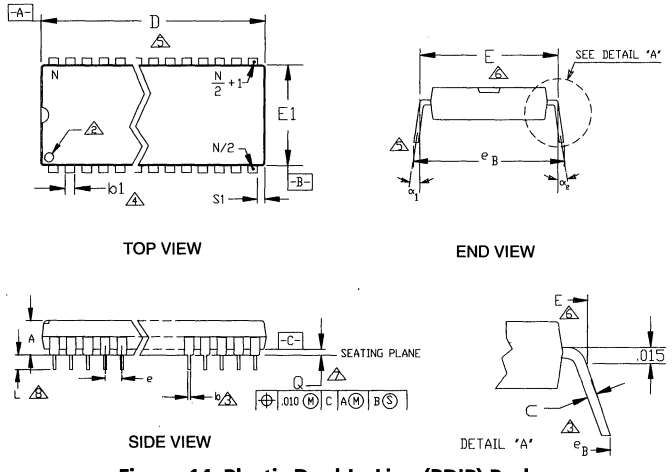
The Plastic Dual-In-Line package (PDIP) construction consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The leads are trimmed and formed to a through-hole lead design, with lead extensions along the two long ends of the rectangular package.

Table 9. PDIP (PD) Package Size Overview

Leadcount	Package Body Area (L X W) Inches	Lead Pitch Inches	Package Weight (Grams)
20	0.267	0.10	1.39
24	0.69		3.55
24 (PD3 (Note 1))	0.32		1.60
28	0.81		4.20

Note:

1. PD3 (300 mil) designate PDIP designs for which the package mil size is not what is standard for that lead count.



21552B-015

Figure 14. Plastic Dual-In-Line (PDIP) Packages

Dimension Codes	Vantis Package Type & Leadcount (JEDEC Drawing Number)									
	PD 020		PD 024		PD3024		PD 028		PD3028 (288 body)	
	(MS-001(D)AD)		(MS-011(B)AA)		(MS-011(B)AA)		(MS-011(B)AB)		(MO-095(A)AH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.200	0.140	0.225	0.140	0.200	0.140	0.225	0.140	0.180
b	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022
b1	0.045	0.065	0.045	0.065	0.045	0.065	0.45	0.65	0.45	0.60
C	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015
D	1.010	1.040	1.240	1.280	1.150	1.270	1.440	1.480	1.345	1.385
E1	0.240	0.280	0.520	0.580	0.240	0.280	0.530	0.580	0.275	0.295
E	0.300	0.325	0.600	0.625	0.300	0.325	0.600	0.625	0.300	0.325
e	0.090	0.110	0.120	0.160	0.120	0.160	0.090	0.110	0.090	0.110
L	0.120	0.160	0.090	0.110	0.090	0.110	0.120	0.160	0.120	0.150
Q	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060
S1	0.005	—	0.005	—	0.005	—	0.005	—	0.005	—
e_b	0.330	0.430	0.630	0.700	0.330	0.430	0.630	0.700	0.330	0.430
$(\alpha_1 - \alpha_2)$	0°	10°	0°	10°	0°	10°	0°	10°	0°	10°
(α_1, α_2)	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
N	20		24		24		28		28	

Notes:

1. *All dimensions are in inches.*
2. *A notch, tab, or pin one identification mark shall be located adjacent to the device pin one.*
3. *Lead thickness increases by a maximum of 0.003 inch when a the solder lead finish is applied.*
4. *These dimensions do not include mold flash or protrusion.*
5. *This dimension is measured from the outside of the leads and 0.015 inch below the plane of the package exit, as defined by the top of the lead.*
6. *This dimension is measured from the seating plane to the base plane.*
7. *This dimension is measured from the seating plane (or from the lowest point of the lead shoulder width that measures 0.040 inch) to the lead tip.*
8. *The difference between these two dimensions should not exceed 7°.*
9. *When standoff has radii, the seating plane location is defined where the lead width equals 0.040 inch.*
10. *PD is Vantis' internal designator for a plastic dual-in-line package.*

Small Outline (SOIC) Plastic Packages

The SOIC package is an surface-mount alternative for low leadcount devices. Its design is similar to the conventional Dual-In-Line (DIP) package—an attractive feature for circuit designers already familiar with DIPs and memory boards.

Like plastic DIPs, the SOIC package consists of a device attached to the die pad of a leadframe, the circuitry of which is wire bonded to the lead fingers. A plastic epoxy material is injection-molded to encapsulate the device/leadframe configuration. The leads extending from the two long sides of the rectangular package body are trimmed and formed to a gull-wing formation.

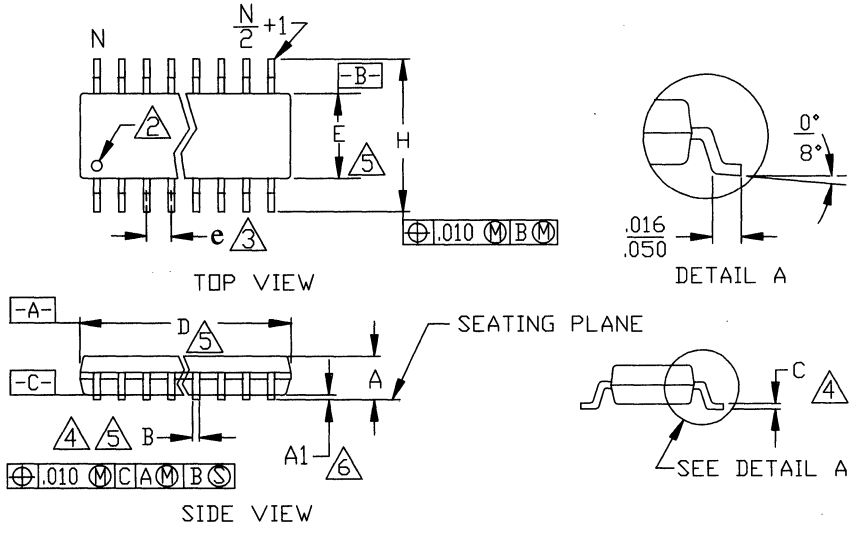
The 50-mil lead pitch of SOIC packages allows for considerable reduction in package size over comparable DIPs, as shown in the table to the right. Not only are SOIC packages smaller, they are lighter, too. This makes them ideal for foil/film mounting and virtually all automated board assembly operations.

Table 10. SOIC (SO)[1] Package Size Overview

Leadcount	Package Body Area (L X W) Inches Sq. (mm sq.)	Lead Pitch Inches (mm)	Package Weight (Grams)
20	0.149 (96.13)	0.05 (1.27)	0.51
24	0.180 (115.51)		0.62

Note:

1. SO is Vantis' internal abbreviation for an SOIC package.



21552B-017

Figure 15. JEDEC English Packages

Dimension Codes	Vantis Package Type & Leadcount			
	SO 20		SO 24	
	Min	Max	Min	Max
A	0.0926	0.1043	0.0926	0.1043
A1	0.0040	0.0118	0.0040	0.0118
B	0.0138	0.0192	0.0138	0.0192
C	0.0091	0.0125	0.0091	0.0125
D	0.4961	0.5118	0.5985	0.6141
e	0.050 BASIC		0.050 BASIC	
E	0.2914	0.2992	0.2914	0.2992
H	0.3940	0.4190	0.3940	0.4190
N	20		24	

Notes:

1. *All dimensions are in inches.*
2. *An identification mark shall be located adjacent to the device pin one.*
3. *Dimension "e" is measured at the center line of the leads.*
4. *Dimensions "B" and "C" increase by 0.003 inch maximum for all leads when solder dip lead finish is applied.*
5. *Dimension "B" does not include dambar protrusion. Allowable protrusion is 0.004 inch.*
6. *Dimensions "A1" is measured from the base plane of contact, which is made when the packaged is allowed to rest freely on a flat, horizontal surface.*
7. *Lead coplanarity shall be within 0.004 inch as measured from the seating plane.*
8. *SO is Vantis' internal abbreviation for an SOIC package.*

PACKAGE DESIGN ADVANTAGES

The BGA package design offers many advantages over other high leadcount packages.

Board Real Estate Savings

Because of the small package size, the BGA offers significant savings in board real estate, occupying about 51 percent of the space a comparable QFP requires. It has a lower profile, too, about one third as thick as a plastic quad flat pack (PQFP) package.

Electrical Performance

The BGA offers superior electrical performance because the shorter wirebond lengths in it help reduce inductance. Comparing a 169-ball BGA to a 160-Pin PQFP, the BGA shows a 31 percent reduction in signal capacitance and a 46 percent reduction in signal time delay.

Thermal Performance

Studies have been conducted that show that the BGA thermally outshines a comparable PQFP when it is fabricated with "thermal vias" (i.e., through-hole vias) underneath the die pad. These vias allow heat generated by the device to flow to the board, which would improve thermal performance provided the board has a conducting plane built into it. To more accurately ascertain the thermal performance of a BGA, the specific end-use application environment needs to be considered.

Board Assembly Advantages

The pitch of the solder balls on a BGA is far more manageable during board assembly, at 1.0 to 1.5 mm, than the typical 0.5-mm pitch of high leadcount Quad Flat Packs (QFPs).

BGAs can be handled with the same pick-and-place equipment that is used for conventional surface-mount devices, including solder reflow methods. During reflow assembly, the wetting action of the solder balls tends to pull them into alignment so that placement of the component on the solder land does not need to be nearly as precise as with a QFP. The alignment can be off by as much as 6 mils—more forgiving than the 3 mils (0.076 mm) required for fine lead-pitch QFPs.

Post Assembly Inspections

Once the BGA is mounted on the board, there is the challenge of how to inspect the ball joints. Thus far, x-ray techniques appear the most viable solution, although these systems can be quite expensive. Once the component is mounted, it can be removed and a new component remounted; however, there is currently no process for reworking the removed component for reuse.

Vantis' Development Plans

Vantis is currently shipping BGA packages with body sizes of 27 mm x 27 mm and 35 mm x 35 mm at 1.27 mm ball pitch. Vantis will continue to develop other enhanced BGA packages with smaller ball pitches, better thermal performance and higher ball counts with smaller body sizes for our future products.

THERMAL CHARACTERIZATION OF PACKAGES

With the increased density and complexity of CMOS VLSI semiconductor devices, the need to accurately evaluate the thermal properties of packaged Integrated Circuits (ICs) is fundamental to the understanding and prediction of device reliability and performance. Failure rates are inseparably tied to the operating temperature of the device, and they increase exponentially as the temperature of the device junction rises. Therefore, it is important that the junction temperature of every IC in the system be controlled to attain high reliability and a long operating life. Likewise, understanding the thermal properties of each component in the system is important for addressing overall thermal concerns at the system level given the end-use application environment.

Thermal performance data is usually measured in the form of thermal resistance or thermal impedance characteristics ($R\theta_{JA}$, θ_{JA}), and it is used to estimate the junction temperature of a device operating in a given environment. A certain amount of caution should be exercised, however, when using thermal data to design or evaluate systems because many factors influence the thermal performance of the chip-package combination. These factors include such phenomenon as the ambient temperature, the power dissipation of the chip, the thermal conductivity of the Printed Circuit Board (PCB), the proximity and power dissipation of neighboring devices, and the airflow through the system. Therefore, it is important to carefully evaluate and analyze the entire system and its environment before utilizing any standard thermal data. Vantis reports data using the JEDEC JESD51 specification format so that the end user can approximate the effect of the application environment.

The following sections detail the methodology and techniques used by Vantis to evaluate the thermal performance of our devices, with an emphasis on fundamental heat flow properties. Our methods comply with established standards, both government and commercial, and we meet or exceed all military specifications for testing and reporting data. Our thermal data is collected for still air, moving air, and isothermal case temperature, using measurement techniques that are in conformance with MIL-SPEC 883D, Method 1012.1 specifications. We also adhere to the recently published improved standards for the thermal test method, environmental considerations, and mounting surface specification. These were published by the Engineering Industries Association (EIA) and Joint Electronic Devices Engineering Council (JEDEC), and they are documented in the JESD51 series.

At Vantis, we are committed to providing current and relevant thermal information for every product we manufacture. In our state-of-the art thermal characterization facility, we can evaluate the thermal performance of any Vantis product. Customers interested in product-specific thermal data should contact a Vantis sales representative.

TERMINOLOGY

The most common terminology used in the industry for specifying thermal performance is the θ_{JA} term and related forms. These are used to describe the thermal characteristics of semiconductor devices in various environments such as natural or forced convection. They are also used when simulating an infinite heat sink as in junction-to-case measurements. In addition, a new term has been recently defined to meet the needs of end users of plastic surface-mount packages. Denoted as Ψ_{JT} this measurement will allow a case temperature measurement during thermal test, which can then relate the case temperature in a free convection boundary condition to the junction temperature. The Ψ_{JT} parameter also helps to validate junction temperature measurements and calculations during thermal characterization.

The terminology commonly used to specify thermal performance, and mathematical constructs for calculating thermal resistance parameters, are provided in the following pages.

MEASUREMENT METHODS

Vantis uses two primary test methods to evaluate the thermal resistance of packaged ICs: the live device method and the thermal test die method. In both methods, we utilize a heat source that is mounted within the package. For the live device method, it is a thermal test chip.

Thermal Resistance Terminology

θ_{JA}, $R\theta_{JA}$ = Thermal resistance from junction to ambient: resistance from the operating portion of a semiconductor device to a natural convection (still air) environment; °C/W.

θ_{JMA}, $R\theta_{JA}$ = Thermal resistance from junction to moving air: resistance from the operating portion of a semiconductor device to a forced convection (moving gas) environment surrounding the device; the gas is assumed to be air unless stated otherwise; °C/W.

θ_{JC}, $R\theta_{JC}$ = Thermal resistance from junction to case: resistance from the operating portion of a semiconductor device to the outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across the surface; °C/W.

θ_{JR}, $R\theta_{JR}$ = Thermal resistance from junction to reference point: resistance from the operating portion of a semiconductor device to a defined reference point within the specified environment surrounding the device; °C/W.

θ_{JX}, $R\theta_{JX}$ = Thermal resistance from junction to environment: resistance from the operating portion of a semiconductor device to a defined non-standard environment surrounding the device; °C/W.

θ_{JL}, $R\theta_{JL}$ = Thermal resistance from the operating portion of a semiconductor device to a liquid environment surrounding the device; °C/W.

θ_{CA}, $R\theta_{CA}$ = Thermal resistance from specified reference location on the case of a semiconductor device to an ambient environment surrounding the device; °C/W.

Ψ_{JT} = Thermal characterization parameter from device junction to the top center of the package surface; °C/W.

T_J = Junction temperature; °C.

T_A = Ambient temperature; °C.

T_C = Case temperature; °C.

T_R = Reference temperature; °C, to standard environment.

T_X = Reference temperature; °C, to non-standard environment.

P_H = Device power dissipation, steady state; Watts.

I_{CC} = Device current supply; Amperes.

V_{CC} = Device voltage supply; Volts.

P_D = Device power dissipation in watts ($V_{CC} \times I_{CC}$).

K_F = Kfactor; calibration constant for determining the $\Delta T/\Delta V$ relationship of the Thermally Sensitive Device (TSD); °C/mV.

TSD = Thermally sensitive device: usually a semiconductor junction which exhibits a linear relationship to temperature over a given temperature range with a constant current applied; °C/mV.

Note: θ_{JR} is an alternative symbol for $R\theta_{JR}$.

continued

Sample Calculations: Thermal Resistance

1) **For calibration of a Thermally Sensitive Device (TSD):**

$$K_F = \frac{T_{HI} - T_{LO}}{V_{LO} - V_{HI}} \quad (1)$$

where:

T_{HI} = High calibration temperature
T_{LO} = Low calibration temperature
V_{HI} = High TSD voltage
V_{LO} = Low TSD voltage

Note: This measurement is made at three or more temperatures to validate linearity of the TSD.

2) **For calculating thermal resistance:**

$$\theta_{JR} = \frac{T_J - T_R}{P_H} \quad (2)$$

where:

θ_{JR} is the thermal resistance from junction to some specified reference point for:

θ_{JA}: 2.54 mm below and 150 mm to the side of the device under test (see Figure 8.1)
θ_{JMA}: directly upstream from the device under test (see Figure 8.3).
θ_{JC}: side of the package directly adjacent to the backside of the die.

3) **For calculating the relationship between θ_{JA}, θ_{JC}, and θ_{CA}:**

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (3)$$

4) **For calculating junction temperature:**

$$T_J = T_R + (\theta_{JR} \times P_D) \quad (4)$$

where:

T_R is the temperature at some specified reference point.

θ_{JR} is the thermal resistance to some specified reference point, R, °C/W.

5) **Thermal characterization parameter, Ψ_{JT}, calculation:**

$$\Psi_{JT} = \frac{T_{JSS} - T_{TSS}}{P_H} \quad (5)$$

where:

Ψ_{JT} = Thermal characterization parameter from top surface of package to air.
T_{JSS} = Device junction temperature at steady-state power.
T_{TSS} = The package top surface, at steady-state power, measured by a thermocouple, infrared sensor, or fluoroptic sensor.

6) **Thermal characterization parameter, Ψ_{TA}, calculation:**

$$\Psi_{TA} = \frac{T_{TSS} - T_{ASS}}{P_H} \quad (6)$$

where:

Ψ_{TA} = Thermal characterization parameter from top surface of package to air.
T_{TSS} = Package (top surface) temperature at steady-state power.
T_{ASS} = The ambient temperature at steady-state power.

7) **For calculating the relationship between θ_{JA} and Ψ_{JT}:**

$$\theta_{JA} = \Psi_{JT} + \Psi_{TA} \quad (7)$$

Table 11. Typical Thermal Resistance Data (T_A=25°C. These Parameters are not Tested.)

Package Style	θ_{JC}[1] °C/W (Typ)	ψ_{JT}[2] °C/W (Typ)	θ_{Ja}[3] °C/W (Typ)	θ_{Jma} °C/W 200 lfpm (Typ)	θ_{Jma} °C/W 400 lfpm (Typ)	θ_{Jma} °C/W 600 lfpm (Typ)	θ_{Jma} °C/W 800 lfpm (Typ)
PL44		10.9	31.4	26.5	25	24.2	23.6
PL68		10	33	29.4	26.8	25.0	22.3
PL84		7.8	28.3	22.5	21.4	20.4	19.5
PLH84		3.2	15.9	13.2	11.5	9.7	8.8
PQE160	0.9	1.7	12.9	7.8	6.5	5.6	5
PQE208	0.9	1.9	11.6	6.4	5.2	4.6	4
PQE240	0.8	1.3	11.5	6.3	5.4	4.4	4.1
PQL48		4.7	32.5	26.4	24.8	22.8	21.8
PQL100		4.6	28.7	25.1	23.2	21.8	20.7
PQL144		6.4	29.5	26.1	24.9	23.3	22.2
PQR100		18.9	34.5	30.3	27.6	26	24.8
PQR144		13	32.1	22.1	18.5	18.2	17
PQR160		13.5	29.5	25.1	23.3	22	21.1
PQR208		17	51.4	46.6	44.4	42.8	41.7
PQT44		11.3	41	35	33.7	32.6	32
PRH144		5.1	19.5	16.4	14.1	12.5	11.7
PRH208		4.5	16.1	12.4	11.6	10.3	9.5
BGD256	1.2	2.9	14.5	11.7	10.7	9.8	9.1
BGD352	1	2.8	12.6	10.1	9.2	8.4	7.8

Notes:

1. *θ_{jc} is only valid for packages with direct thermal pathways to the surface of the package and should only be used to calculate junction temperature if a heat sink is applied.*
2. *ψ_{JT} is a thermal parameter allowing the calculation of junction temperature from a measured temperature at the top center of the package in natural convection. See JESD 51-2 for details (www.jedec.org/free standards)*
3. *All thermal data was generated according to EIA/JEDEC specifications JESD51 series. All measured packages were surface mounted on to 2S2P (2 signal, 2 internal Cu plane) boards.*

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

The live device method provides weighted average values for thermal resistance, and it can account for any hot spots or uneven temperature distributions on the die. The thermal test die method is preferred, however, because it enables the power dissipation and die size to be easily controlled. The following sections provide details on these two methods and the calibration process that is required.

CALIBRATION OF THE THERMALLY SENSITIVE DEVICE

When utilizing either the live device method or the thermal test die method, the Thermally Sensitive Device (TSD) must first be calibrated to determine the $\Delta T/\Delta V$ characteristics (i.e., the change in temperature over the change in voltage). (The TSD appropriate for each test method is defined in the sections that follow.)

The calibration factor (KF) for the TSD is used to relate the forward voltage of the TSD to a temperature, thereby allowing thermal resistance to be computed using the algorithm (1) provided under "Sample Calculations." The devices under test are calibrated over the temperature range of interest in either a convection type oven or a temperature controlled fluid bath.

Live Device Method

When measuring the thermal characteristics of a live semiconductor device, the device must first be biased to provide the typical power dissipation for that device type. Also, a TSD must be located on the die to enable the junction temperature to be measured and monitored. The most commonly used TSD is either the substrate isolation diodes or an ESD input protection diode. Substrate diodes are preferred because using an input diode for temperature sensing only gives the temperature information for a small region of the die. Substrate isolation diodes, on the other hand, provide an array of the intrinsic parasitic diodes inherent in many semiconductor processes.

To implement the electrical test method for a live device, the device must first be forward biased as it is in normal operation and allowed to dissipate power. Then it must be reverse biased and, at specified intervals (usually within 10 to 40 μs from the time power was removed), the TSD must be measured to determine the junction temperature. This is also referred to as the voltage-drop method or the pulse method. The parameter actually measured is the forward voltage drop of a semiconductor junction. The substrate isolation diodes are also electrically in parallel, so the junction temperature recorded is the weighted average of the hottest junction on the die, providing typical worst case values. Unfortunately, due to the increasing complexity of the silicon, the live device method is less popular and not widely used for high pin-count products. Biasing the die with the correct vectors and signals while switching from the forward- to reverse-bias modes is becoming more difficult, and in some cases impossible.

Thermal Test Die Method

When using the thermal test die method, a specially designed thermal test die is assembled into the IC package. This test die contains a resistive element for power dissipation. Semiconductor junctions (i.e., diodes) are used as TSD to enable the temperatures at various locations on the die to be measured. This method is used primarily to evaluate the thermal resistances of packages, generically, given the range of die sizes appropriate for the module size of the thermal test die (usually 75 to 100 mils^2). These modules can be arrayed to produce larger die sizes in increments of the unit module (i.e., 100 mils^2, 200 mils^2, etc.).

The thermal test die method is limited, however, in that it assumes evenly distributed power dissipation across the surface of the die. This typically produces a near-ideal heat source and lower thermal resistance results. Therefore, the die size and temperature distribution of the actual (production) device should be taken in to account when making these types of measurements. The temperature distribution of the production device can be determined by the use of non-contact thermometry methods such as liquid crystal thermography or infrared thermometry. The temperature distribution, assuming typical operating conditions, can then be computed based on

evidence of hot spots and the resulting temperature distribution across the die. Based on this analysis, the thermal properties of the production device can be correlated with those obtained with the thermal test die.

MEASUREMENT ENVIRONMENTS

When using thermal performance data for semiconductor devices, it is extremely important to consider the effects of the environment on the measured or modeled values. To simulate the environments devices will encounter in end-use applications, thermal measurements are taken in still and moving air environments and at the case (or package body) environment, as explained in the following sections.

Natural Convection (Still-Air) Environment

Natural convection measurements (θ_{JA}) are performed in a chamber which encloses one cubic-foot volume of still air. A diagram of a still-air chamber is shown in Figures 16 and 17. The test board near the device under test is mounted horizontally (or vertically, if requested) in the chamber, and the reference temperatures both inside and outside the chamber are monitored. The device is allowed to come to a steady state thermal condition both before and after heating power is applied.

Forced Convection (Moving-Air) Environment.

Forced convection (θ_{JMA})measurements are performed in a laboratory wind tunnel, a diagram of which is shown in Figure 18. The test boards can be mounted vertically or horizontally, depending on the requirement.

Air speeds of 100 to 1200 linear feet per minute (lfpm) are attainable in the tunnel. Air speed is monitored using a hot-wire anemometer, which is mounted on an XYZ stage near the device.

Case Environment

When taking case (θ_{JC}) measurements, a separate apparatus is required for hermetic versus plastic packages.

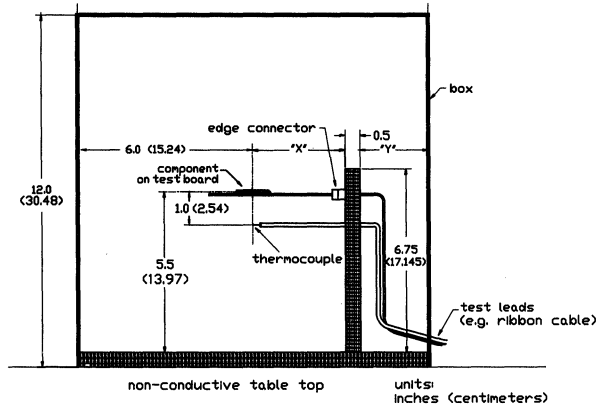


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Figure 16. Side View of the Natural Convection Fixture, Which is Used for Still-Air Tests

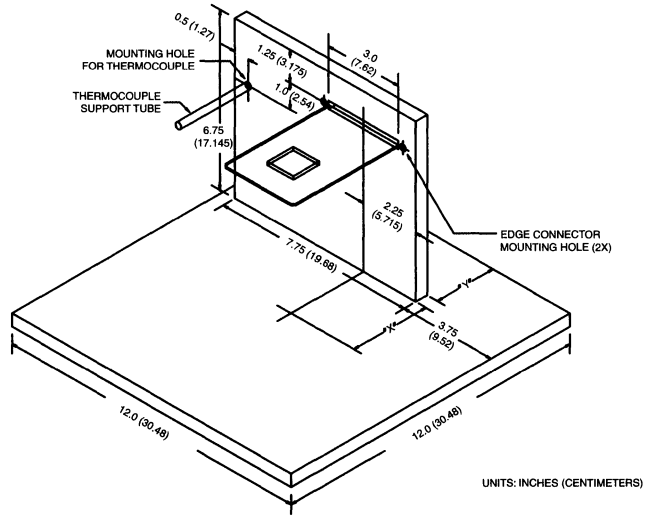

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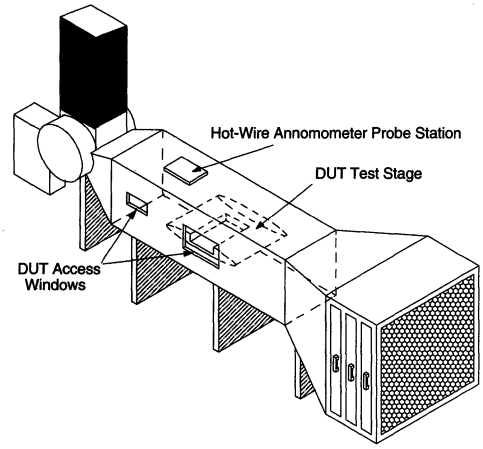
Figure 17. Isometric View of the Natural Convection Fixture

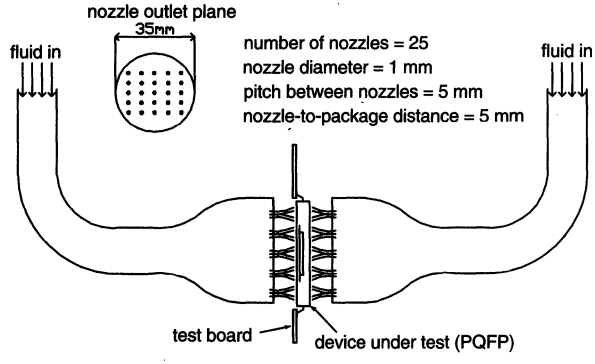
For hermetic packages, a thermoelectric device or cold plate is used to keep the case temperature constant during the measurement process. The package is placed against the cold plate and held in position with an adjustable clamp. A thin layer of thermal grease is used to thermally contact the package to the test fixture. A thermocouple is mounted into the test fixture that comes in contact with the package body to allow case temperature measurements. Fixtures for junction-to-case measurements are customized for each package style.

For plastic packages, a temperature-controlled fluid bath containing deionized water is used. Fluid is forced onto the package body from both sides from nozzles as shown in Figure 19. Due to the high heat transfer capabilities of this method, we assume the reference temperature is that of the liquid. This measurement is a relatively new technique that essentially provides the same boundary conditions as the cold plate method does for hermetic packages. But, caution should be used when attempting to calculate junction temperature from θ_{JC} values for plastic packages in end-use environments (see the following section on Ψ_{JT}).



21552B-021

Figure 18. Forced Convection Chamber, Which is Used To Conduct Moving-Air Tests



21552B-022

Figure 19. Jet Nozzle Impingement, Which is Used For Taking Case Measurements of a Plastic Package

THERMAL CHARACTERIZATION PARAMETER (Ψ_{JT})

A new parameter has gained popularity due to the misconceptions arising from using the value of θ_{JC} to calculate junction temperatures for plastic packaged devices in end-use environments. This parameter is proportional to the temperature difference between the top center of the package and the junction temperature, relative to the power dissipation. It is a useful parameter for verifying device temperatures in an end-use environment. The sample calculations on page 492 and 493 provide examples of calculations using this new parameter.

THERMAL TEST BOARDS

Before measuring the thermal characteristics of a semiconductor device, the component is assembled onto a test board using industry-standard techniques. The test boards Vantis uses for this are standardized to conform with the JEDEDC specification JESD51_3. Two types of test boards are commonly used: low-effective or high-effective thermal conductivity test boards.

Low-Effective Thermal Conductivity Test Boards

Low-effective thermal conductivity test boards are designed to simulate worst-case board mounting. These boards have no internal planes and minimum trace routing.

High-Effective Thermal Conductivity Test Boards

High-effective thermal conductivity test boards are fabricated to have two evenly spaced internal planes. These boards more closely reflect applications in which ground or power planes are used in the PCB.

For both board types, FR4 is used as the board material, and small gauge wire is used to connect the device to the test interface. The board dimensions are 76.2 mm wide by 114.3 mm long for packages having body sizes <28 mm. For package bodies ≥28 mm, the board size is 101.6 mm wide by 114.3 mm long.

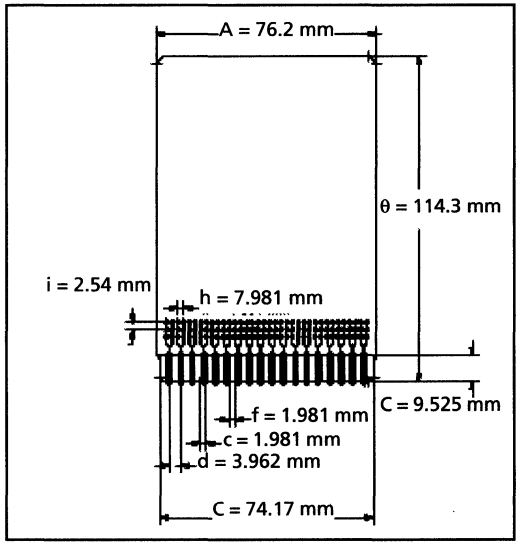


Figure 20. Thermal Test Board Design for IC Packages Having Body Sizes Less Than 28 mm

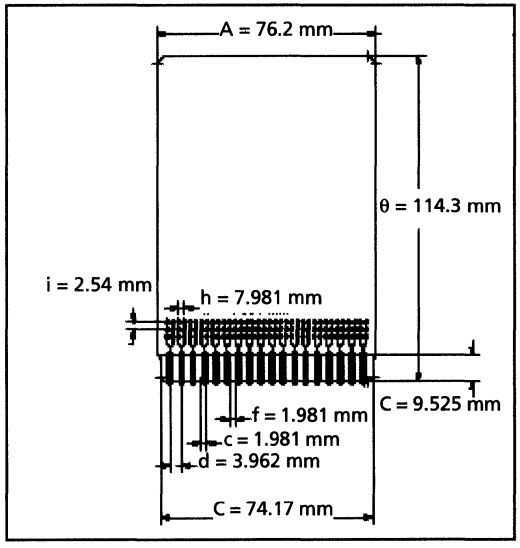


Figure 21. Thermal Test Board Design for IC Packages Having Body Sizes of 28 mm

(See Figures 20 and 21). By standardizing the board, the environment for testing is normalized to the board size, allowing comparisons between package families or package variations within a family. These PCB designs conform to JESD specifications.

PRODUCT CARRIERS PER PACKAGE TYPE

Packing methods for devices have become increasingly important to facilitate automated board assembly and optimize packing density. This goal, along with protecting product reliability, drives the design concepts behind some of the new packing systems.

Vantis offers several packing systems for its through-hole and surface-mount products. The table lists those systems that are used as a standard.

Vantis' packing system designs have kept pace with the sophistication of user needs and product sensitivity. This section provides in-depth descriptions of these designs.

Table 12. Product Carriers for IC Packages

Package Type	Leadcount	Device Carrier	Packing Container
Plastic Dual-In-Line	All leadcounts	Tube	Mini-Q or 1Q box
Plastic Leaded Chip Carrier	≥ 32 lead	Tube	Dry pack & 2k/4k box
		Tape & Reel (Note 1)	Dry pack & reel box
	All others	Tube	2k/4k box
		Tape & Ree (Note 1)	Reel box
Plastic Small Outline & Shrink Plastic Small Outlines	All leadcounts	Tube	Mini-Q or 1Q box
		Tape & Reel (Notes 1 & 2)	Reel box
Plastic Quad Flat Pack & Thin Plastic Quad Flat Pack	All leadcounts	Tray (Note 3)	Dry pack & tray box
Plastic Ball Grid Array	All configurations	Tray (Note 3)	Dry pack & tray box

Notes:

1. *Optional; upon request only*
2. *Except for the SO 028-lead package, which is not available in tape and reel.*
3. *These trays can withstand temperatures of -125 °C to 150 °C.*

Tubes

Tubes are used as unit carriers for most of our lower leadcount packages. The product carrier guide on the next page shows which package families are shipped in tubes as a standard.

All of our tubes are made of an antistatically coated PVC to protect product from electrical and mechanical damage. The tubes are designed to accommodate packages that are loaded with or without unit carriers depending on the package style. Tube sizes are standardized by package type to facilitate automated board assembly.

DEVICE LOADING

Devices are loaded into tubes, with each device pin one uniformly oriented (only one product date code per tube). A variety of end-plug designs, all of antistatic material, secure products in the tube and ensure that there is no excessive movement of product in the tube during shipping and handling. This protects the mechanical integrity of the package and leads; it also ensures an unimpaired dispensing of product for manufacturing operations.

When the end-plug design is a plastic stopper pin, all devices are loaded so pin one is oriented toward the green stopper pin to aid in manufacturing.

This section includes details about the quantity of devices per tube for each package style and leadcount. Vantis encourages but does not require ordering and shipping in full tube quantities. Following the quantity tables, dimension drawings for all of our tube sizes (by package type) are shown, along with the specific end-plug design used.

Consult your Vantis sales representative for additional information about our tubes.

Table 13. Q-Pack Tube and Box Quantity Information

Package		Leadcount	Devices Per Tube	Tubes Per Box	Devices Per Box
Plastic Leaded Chip Carriers	PL	20 lead, square	46	10	460
	PL, PLH	28 lead, square	37	15	555
	PL	44 lead, square	26	10 (note 1)	1040 (note 1)
	PL	68 lead, square	18	15 (note 2)	810 (note 2)
	PL, PLH	84 lead, square	15	16 (note 2)	720 (note 2)
Plastic Small Outline	SO	20 lead	38	15	570
	SO	24 lead	30	16	480

Notes:

1. *The tubes per box actually reflect the quantity of tubes in a dry pack bag, not the Q-Pack box. The device count per box, however, is accurate because four bags of parts are put in the box.*
2. *The tubes per box actually reflect the quantity of tubes in a dry pack bag, not the Q-Pack box. The device count per box, however, is accurate because three bags of parts are put in the box.*

Trays

Trays are used instead of tubes to protect higher leadcount packages from electrical and mechanical damage during handling and shipment. Trays are also suitable for product presentation to board assembly equipment.

All trays are uniformly sized, in compliance with standard JEDEC outlines. As much as possible, Vantis procures trays that are made of 25 percent recycled material. The PVC tray material is either carbon-filled or antistatically coated to provide ESD protection.

Trays for plastic packages can withstand continuous operation at temperatures up to 150°C.

Packages are placed in the trays so that the device pin one is oriented to the notched corner of the tray, enabling pick-and-place equipment setups to be compatible for all packages and leadcount.

For shipment, a stack of six trays are secured with straps; five containing parts and the sixth serving as a cover. The diagrams and tables that follow show tray dimensions per package and the quantities of parts per tray.

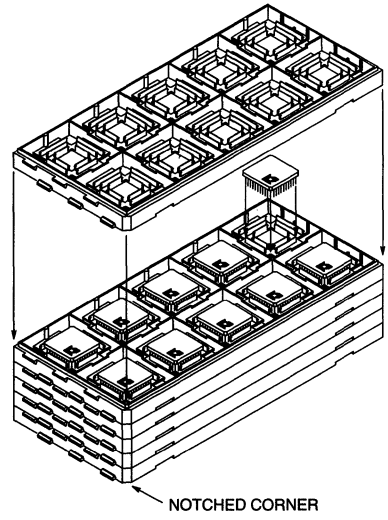


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Figure 22. Five Trays of Product are Stacked for Shipment, With a Sixth Tray Serving as a Cover, and All Devices are Uniformly Oriented so Pin One is Aligned With the Notched Corner of the Tray

Table 14. Tray Device Carriers: Full Tray Quantity Information All Applicable Packages – Tray and Box Quantities

Package		Leadcount	Device Per Tray	Trays Per Box [1]	Devices Per Box
Plastic Quad Flat Pack	PQR	100 lead	66	6 (Note 1)	330
	PQR, PRH, PQE	144 & 160 lead	24		120
	PQR, PRH, PQE	208 & 240 lead	24		120
Thin Plastic Quad Flat Pack	PQT	44 lead	160		800
	PQL	48 lead	250		1250
	PQL	100 lead	90		450
	PQL	144 lead	60		300
	PQL	176 lead	40		200
Plastic Ball Grid Array	BGD	256 ball	40		200
	BGD	352 ball	24		120

Note:

1. In all cases, the top tray is empty, serving as a cover.

Dry Pack Protection

Package cracking can occur when moisture-sensitive product is mounted directly onto a board, versus socket mounted, using a high temperature solder reflow process. As moisture in the encapsulation material heats and vaporizes, the pressure it creates can result in package cracking or delamination. Dry packing product keeps the moisture level in the encapsulation material below a critical level, providing you with "solder-safe" packages.

Product that is dry packed is first baked for 5 to 11 hours, depending on the product, at 125 °C and then sealed under a partial vacuum in a moisture barrier bag containing desiccant and a humidity indicator card. The bag interior is maintained at a safe relative humidity (RH) level of ≤20%. Once product is removed from the bag, or the bag seal is broken, the product should be board mounted within the recommended out-of-bag time (assuming the assumptions about the end-use factory environment are reasonably accurate). The out-of-bag time and the factory environment assumptions are listed on the dry pack caution label that is applied to the outside of every dry pack bag. If the out-of-bag time is exceeded, or the humidity indicator card upon opening the bag registers ≥30% RH, then product should be baked for 24 hours at 125 °C before board mounting. The tray in which Vantis ships product can withstand up to 150 °C; however, product in tubes or reels must be either put in metal tubes or baked for 192 hours at 40 °C at 5% RH.

Vantis determines the moisture sensitivity of our product by testing them per the JEDEC industry-standard A112-A/A113 process. Depending on the results, product classified under one of six sensitivity levels, with Level 1 being not moisture sensitive, The sensitivity rating for product is indicated on the dry pack caution label on the outside of every dry pack bag. The table lists the current sensitivity levels for all Vantis products that are dry packed.

Table 15. Vantis Moisture Sensitive Products

Package	Leadcount	JEDEC Level	Out-Of-Bag Time [1]
Plastic Leaded Chip Carriers (PLCCs)	≤ 28 Lead	2	1 year
	≥ 44 lead	3	168 hours
Metric (Note 2) Plastic Quad Flat Packs (PQFPs)	144 & 208 lead	3	168 hours
	All others	3	168 hours
Thin Plastic Quad Flat Packs (TQFPs)	All leadcounts	3	168 hours
Small Outline (SO)	≤ 24 lead	3	168 hours
Plastic Ball Grid Arrays (BGAs)	All ball counts	3	168 hours

Notes:

1. *Assumes an end-use factory environment of ≤30 °C and 60% RH.*
2. *Includes PQFP packages denoted internally by Vantis as PQR, PRH, and PQE.*

Tape & Reel: Full Reel Quantity Information

Tape-and reel device carriers are available for selected IC packages, as shown in the table below. This carrier is designed to protect product from mechanical and electrical damage, and it is suitable for device presentation to automatic pick-and-place equipment.

The tape-and-reel design consists of a pocketed carrier tape which is loaded with one device per pocket. Each device is oriented in the pocket so that its pin-one location complies with the Engineering Industries Association Standard 481. A protective cover tape is heated-sealed over the carrier tape to keep devices in the pockets. The carrier tape is made of conductive polystyrene, and the cover tape is antistatic polyester-both of which protect product from ESD damage.

Once loaded, the tape is wound onto an antistatic plastic reel for packing and shipment. Each reel is labeled with a standard inventory label identifying the contents. The number of device per full reel are provided in the table shown.

Package	Leadcount	Qty/Reel
Plastic Leaded Chip Carrier (PL, PLH)	20 lead	1000
	28 lead	750
	44 lead	500
	68 and 84 lead	250
Plastic Small Outline (SO)	20 and 24 lead	1000
Thin Plastic Quad Flat Pack (PQL, PQT)	44 lead (PQT)	1500
	48 lead (PQL)	2000
	100 lead (PQL)	1000
	144 lead (PQL)	500
Plastic Ball Grid Array (BGD)	256 ball count 352 ball count	TBD

Notes:

1. *300 mm of empty trailer pockets are provided at the beginning of the reel to facilitate feeding the tape into automatic board assembly equipment.*
2. *500 mm of empty leader pockets are provided at the end of the reel.*

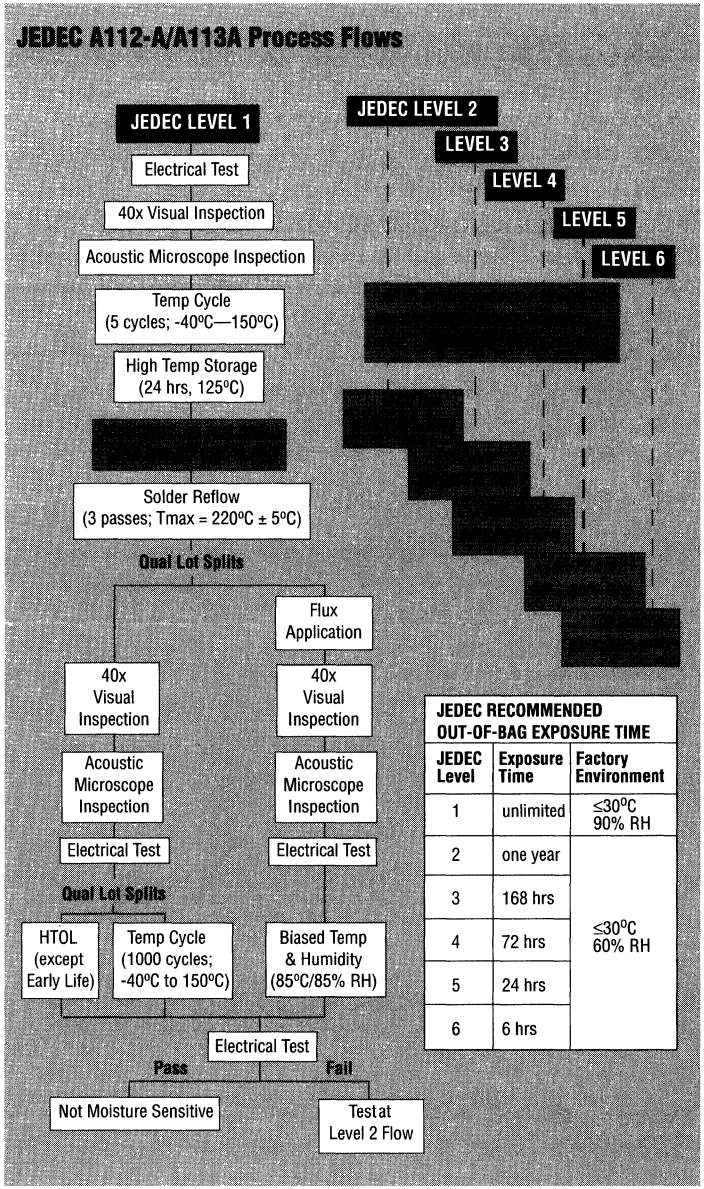
CONTROLLING MOISTURE

In designing packing materials and packing methods, Vantis is sensitive to the susceptibility of some IC packages to moisture-induced damage. The risk of this is highest when plastic encapsulation materials are used, as plastic is naturally permeable to moisture. The moisture in the package will increase or decrease to reach the Relative Humidity (RH) of the surrounding environment.

Therefore, controlling the moisture level in the package body is critical to reducing the risk of moisture-induced damage. Such damage may include delamination between the die and the plastic encapsulation material, which may result in open connections due to broken wirebonds. Package cracking may also occur when the components are exposed to the high temperatures and steep temperature gradients used in reflow board assembly techniques. Moisture in the package rapidly heats and vaporizes and, if there is sufficient steam due to the moisture in the package having reached a critical level, it will fracture the package to escape. This phenomenon is known as the "popcorn effect."

TESTING PRODUCTS FOR MOISTURE SENSITIVITY

To better understand and classify the moisture sensitivity of our products, Vantis has adopted the JEDEC test methods A112-A/A113A. These have been adopted by the industry as the standard process by which to determine the moisture sensitivity of IC components.



JEDEC RECOMMENDED OUT-OF-BAG EXPOSURE TIME

JEDEC Level	Exposure Time	Factory Environment
1	unlimited	≤30°C 90% RH
2	one year	≤30°C 60% RH
3	168 hrs	
4	72 hrs	
5	24 hrs	
6	6 hrs	

21552B-028

JEDEC Test Standard A112-A/A113A

This test standard (shown on page 507) defines six different moisture sensitivity levels, referred to as level 1, level 2, through to level 6. Each higher level denotes a higher level of sensitivity. Product that fails the level 1 flow is then tested at a higher level until it passes. Specific process steps in each flow subject the product to conditions designed to simulate the environment of an end-use application. Subsequent electrical testing and inspection steps determine if the device was damaged during the environmental stress steps.

The only difference between each A112-A/A113A flow is the parameters of the moisture soak step (also known as preconditioning). These parameters are designed to allow the component to absorb as much moisture as it can given its package size. The purpose of the testing is to determine the safe environmental conditions for product exposure.

Once it is determined that product is moisture sensitive (i.e., it fails the level 1 flow), Vantis dry packs the product for storage and shipment. This is done regardless of the type of product carrier used (e.g., tubes, trays, reels, etc.). Dry packing protects product from environmental moisture by maintaining the interior of the dry pack bag at ≤20 percent RH.

DRY PACKING PROCESS AND MATERIALS

The first step in the dry pack process is to remove any moisture buildup in the package by baking the finished product for 5 to 15.5 hours, depending on the package type, at 125 °C ± 5 °C. While baking, the product is contained in device trays (made of material that can withstand the high temperature) or aluminum trays or tubes. Within 50 hours after baking, the product is sealed in a dry pack bag under a partial vacuum. The bag is sealed using an impulse heat sealer at a seal time of 1.0 to 1.5 seconds; a seal pressure of 40 to 50 psi; and a temperature range of 191 °C to 232 °C.

Included in the dry pack bag are a prescribed number of humidity indicator cards and desiccant pouches, depending on the quantity of devices in the bag.

GENERAL REFERENCES

1. "Thermal Characteristics," Method 1012.1, MIL-STD-883C, Test Methods and Procedures for Microelectronics, Department of Defense, Washington, DC.
2. "Semiconductor Measurement Technology: Thermal Resistance Measurements," F.F. Oettinger and D.L. Blackburn, NIST Special Publication 400-86, Department of Commerce, Washington, DC.
3. Accepted Practices for Making Microelectronic Device Thermal Characteristics Tests - A User's Guide," JEDEC Engineering Bulletin No. 20, Electronic Industries Association, Washington, DC.
4. "Still-and Forced-Air Junction-To-Ambient Thermal Resistance Measurements of Integrated Circuit Packages," SEMI G38-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
5. "Junction-To-Case Thermal Resistance Measurements of Molded-Plastic Packages," SEMI G43-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
6. "Junction-to-Case Thermal Resistance Measurements of Ceramic Packages," SEMI G30-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
7. "Unencapsulated Thermal Test Chip," SEMI G32-86 Guideline, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
8. "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages," SEMI G42-88 Specification, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
9. "Thermal Transient Testing for Die Attachment Evaluation of Integrated Circuits," SEMI G46-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.
10. "Applying the Electrical Test Method To Thermal Characterization of MOS Integrated Circuits," B.S. Siegal, SAGE Enterprises, Mountain View, CA, 1985. (Semitherm 2 Conference Proceedings)
11. "An Electrical Technique for the Measurement of Integrated Circuit Thermal Resistance," TA7802, B. Siegal, SAGE Enterprises, Inc. Mountain View, CA.
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13. "How Fast Is It Blowing?: Design and Characterization of a Laboratory Wind Tunnel" Hayward, J.D., and Van Andel, R., Advanced Micro Devices, Sunnyvale, CA.
14. Microelectronics Packaging Handbook, Tummala, Rao R., Rymaszewski, Eugene J., 1989, Van Nostrand Reinhold
15. EIA/JEDEC JESD51, "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)," Electronic Industries Association, 1995
16. EIA JEDEC JESD 51_1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)," Electronic Industries Association, 1995

17.EIA JEDEC JESD 51_2, "Integrated Circuit Thermal Test Method - Environmental Conditions, Natural Convection (Still Air)," Electronic Industries Association, 1995

18.EIA/JEDEC JESD 51_3, "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," Electronic Industries Association, 1995

VANTIS APPROVED PROGRAMMERS[1]

For more information on the products listed below, please consult a local Vantis sales office.

Manufacturer	Model	Revision	Pin Count
Advin 1050-L E. Duane Ave. Sunnyvale, CA 94086 (408) 243-7000 www.advin.com	Pilot-U84 Pilot-U40 MVP	10.89 10.89 10.89	84 40 40
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 www.bpmicro.com	CP1128 BP1148 BP1200 BP1400 BP2100 BP2200	3.35 3.35 3.35 3.35 3.35 3.35	28 48 240 240 240 240
Data I/O 10525 Willows Road N.E. Redmond, WA 98073-9746 (800) 426-1045 www.data-io.com	UniSite M2900 M3900 AutoSite	5.8 5.8 5.8 5.8	84 40 84 84
HI-LO/Tribal Systems 44388 S. Grimmer Blvd. Fremont, CA 94538 (510) 623-8859 www.hilosystems.com.tw	ALL-07 FLEX-700	(Note 2) (Note 2)	68 68
SMS Im Grund 15 D-7988 Wangen, Germany 011-4975-2297280 www.sms-sprint.com	Sprint Expert Optima Gang Multisyte	A5/98 A5/98 A5/98	68 68 84
Stag Silver Court Watchmead Welwyn Garden City Herts AL7 1LT, UK 011-44-1-707-332148 www.stag.co.uk	Quasar Eclipse	10.89 7.11.97	84 84
System General 1603-A S. Main Street Milpitas, CA 95035 (408) 263-6667 www.sg.com.tw	Turpro-1/FX/TX	2.70x	40

Notes:

1. *Vantis does not support or accept rejects programmed on non-approved programmers.*
2. *Revision number is based on device type and module type.*

MACH DEVICE PROGRAMMING UPDATE

For the most up-to-date information, please visit our Web site www.vantis.com

Device	Data I/O Autosite	Data I/O Unisite	Data I/O 2900	Data I/O 3900	BP Micro 1128	BP Micro 1200/1400
MACH 110	1.5	3.3	1.4	1.3	1.86	2.05
MACH 111	2.6	4.7	3.6	2.6	3.062	3.042
MACH 111SP	5.6	5.6	5.6	5.6	NS	3.19
MACH 120	1.5	3.3	1.4	1.3	1.86	2.05
MACH 130	1.5	3.4	1.9	1.3	1.86	2.05
MACH 131	2.6	4.7	3.6	2.6	3.062	3.042
MACH 131/1	5.8	5.8	NA	5.8	NS	3.24
MACH 131SP	5.6	5.6	5.6	5.6	NS	3.24
MACH 210A/Q	1.5	3.3	1.4	1.3	1.86	2.05
MACHLV210	2.1	4.3	3.1	2.1	2.25C	2.25C
MACH 211	2.7	4.9	3.7	2.7	NA	3.075
MACH 211SP	2.9	5.2	4	3.1	NS	3.122
MACH 215	1.5	3.3	1.4	1.3	1.86	2.05
MACH 220	1.5	3.3	3.5	1.3	1.86	2.05
MACH 221	2.8	5.0	NS	2.8	3.122	3.122
MACH 221SP	5.6	5.6	5.6	5.6	NA	3.24
MACH 230	1.5	3.3	3.5	1.3	1.86	2.05
MACH 231	2.7	4.9	NS	2.7	NS	3.07
MACH 231/1	5.1	5.1	NA	5.1	NS	3.122
MACH 231SP	5.1	5.1	5.8	5.1	NS	3.122
MACH 355 or M4-96/96	2.6	4.8	3.7	2.6	NS	3.053
MACH 435	1.6	4.1	2.0	1.6	NS	2.21C
MACH 436 or M4-128N/64	5.5	5.5	NA	5.5	NS	3.26
MACH 445	2.6	4.8	3.7	2.6	NS	3.053
MACH 446 or M4-128/64	5.5	5.5	5.5	5.5	NS	3.26
MACH 466 or M4-256/128	5.5	5.5	5.5	5.5	NS	3.26
M4-32/32 44 pin PLCC	NA	5.7x	NA	5.7x	3.35	3.35
M4-32/32 44 pin PQFP	NA	5.7x	NA	5.7x	3.35	3.35
M4-32/32 48 pin TQFP	NA	5.7x	NA	5.7x	3.35	3.35
M4-64/32 44 pin PLCC	5.8	5.8	5.8	5.8	3.35	3.35
M4-64/32 44 pin PQFP	5.8	5.8	5.8	5.8	3.35	3.35
M4-64/32 48 pin TQFP	5.8	5.8	5.8	5.8	3.35	3.35
M4-96/48 100 pin TQFP	NA	5.7x	5.7x	5.7x	NA	3.35
M4-192/96 144 pin TQFP	NA	5.7x	5.7x	5.7x	NA	NA
M5LV-128/68 100 pin PQFP	NA	NA	NA	NA	NA	3.35
M5LV-128/68 100 pin TQFP	NA	NA	NA	NA	NA	3.35
M5LV-128/74 100 pin TQFP	NA	NA	NA	NA	NA	3.35
M5LV-128/104 144 pin PQFP	NA	NA	NA	NA	NA	3.35
M5LV-128/104 144 pin TQFP	NA	NA	NA	NA	NA	3.35

MACH DEVICE PROGRAMMING UPDATE (CONTINUED)

For the most up-to-date information, please visit our Web site www.vantis.com

Device	Data I/O Autosite	Data I/O Unisite	Data I/O 2900	Data I/O 3900	BP Micro 1128	BP Micro 1200/1400
M5LV-128/120 160 pin PQFP	NA	NA	NA	NA	NA	3.35
M5LV-256/68 100 pin PQFP	NA	5.6x	NA	NA	3.31	3.31
M5LV-256/68 100 pin TQFP	NA	5.6x	NA	NA	3.31	3.31
M5LV-256/74 100 pin TQFP	NA	NA	NA	NA	NA	3.36
M5LV-256/104 144 pin PQFP	NA	5.6x	NA	NA	NA	3.36
M5LV-256/104 144 pin TQFP	NA	NA	NA	NA	NA	3.36
M5LV-256/120 160 pin PQFP	NA	5.8	NA	NA	3.31	3.31
M5LV-256/160 208 pin PQFP	5.8	5.8	5.8	5.8	3.31	3.31
M5-128/68 100 pin PQ/TQ	5.6	5.6	5.6	5.6	NS	3.24
M5-128/104 144 pin PQFP	5.6	5.6	5.6	5.6	NS	3.23
M5-128/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.21
M5-192/68 100 pin PQ/TQ	5.6	5.6	5.6	5.6	NS	3.16
M5-192/104 144 pin PQFP	5.6	5.6	5.6	5.6	NS	3.23
M5-192/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.16
M5-192/160 208 pin PQFP	5.6	5.6	5.6	5.6	NS	3.16
M5-256/68 100 pin PQ/TQ	5.6	5.6	5.6	5.6	NS	3.17
M5-256/104 144 pin PQFP	5.6	5.6	5.6	5.6	NS	3.23
M5-256/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.17
M5-256/160 208 pin PQFP	5.6	5.6	5.6	5.6	NS	3.17
M5-320/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-320/160 208 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-320/184 240 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-320/192 256 ball BGA	5.6	5.6	5.6	5.6	NS	3.26
M5-384/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-384/160 208 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-384/184 240 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-384/192 256 ball BGA	5.6	5.6	5.6	5.6	NS	3.26
M5-512/120 160 pin PQFP	5.6	5.6	5.6	5.6	NS	3.24
M5-512/160 208 pin PQFP	5.6	5.6	5.6	5.6	NS	3.21
M5-512/184 240 pin PQFP	5.6	5.6	5.6	5.6	NS	3.26
M5-512/192 256 ball BGA	5.6	5.6	5.6	5.6	NS	3.26
M5-512/256 352 ball BGA	5.6	5.6	5.6	5.6	NS	3.26

Notes:

1. *Entries in this table are minimum required programming algorithm revisions. These revisions or current approved revisions are acceptable.*
2. *EV=Engineering version, under evaluation*
3. *NS=Not supported due to hardware limitations or marketing considerations; NA=contact Vantis or programmer vendors for support information.*
4. *x=Programming support on the programmer manufacturer's bulletin board is to be used with indicated revision*
5. *MACH is a registered trademark of Vantis Corp.*

MACH DEVICE PROGRAMMING UPDATE (CONTINUED)

Device	Stag Eclipse	HI-LO/Tribal ALL07/Flex700	ADVIN U40 / U84	SMS/Sprint Expert	Sys General Turpro-1/FX/TX
MACH 110	6.6.5	3.06	10.21	1/93	1.5
MACH 111	6.6.5	3.06	10.78C	A/95	2.21
MACH 111SP	7.1.30	3.33	10.85C	A7/97	2.32B
MACH 120	6.6.5	3.04	10.21	1/93	1.5
MACH 130	6.6.5	3.17	10.21	3/91	1.5cf
MACH 131	6.6.5	3.17	10.78C	A6/95	2.21
MACH 131/1	7.8.1	3.18D	10.85F2	B0/97	2.32B
MACH 131SP	7.6.13	3.18C	10.85F1	B0/97	2.32B
MACH 210A/Q	6.6.5	3.06	10.21	1/93	1.5
MACHLV210	6.6.5	3.06	10.75A	B5/96	2.12F
MACH 211	6.6.5	3.06	10.81	C/95	2.24A
MACH 211SP	7.1.30	3.32	10.83B	B5/96	2.25c
MACH 215	6.6.5	3.06	10.21	1/93	1.5
MACH 220	6.6.5	3.04	10.21	1/93	1.5
MACH 221	6.6.5	3.04	10.38B	VA/96	2.26
MACH 221SP	7.6.13	3.19B	10.86H	A0/97	2.32B
MACH 230	6.6.5	3.17	10.21	B/94	1.5cf
MACH 231	6.6.5	3.17	10.78C	A/95	2.21
MACH 231/1	6.6.5	3.17	10.83B	C0/96	2.25c
MACH 231SP	7.7.21	3.17	10.83B	B5/96	2.25c
MACH 355 or M4-96/96	7.8.1	3.17	10.80F	A6/95	2.21
MACH 435	6.6.5	3.17	10.65	1/93	1.68G
MACH 436 or M4-128N/64	7.9.4	3.19C	10.86J	B0/97	2.32D
MACH 445	7.1.30	3.17	10.80F	A6/95	2.21
MACH 446 or M4-128/64	7.9.4	3.19C	10.86J	A7/97	2.32B
MACH 466 or M4-256/128	7.9.4	3.19D	10.85E	A0/97	2.30K
M4-32/32 44 pin PLCC	NA	3.34D	NA	A5/98	NA
M4-32/32 44 pin PQFP	NA	3.34D	NA	A5/98	NA
M4-32/32 48 pin TQFP	NA	3.34D	NA	A5/98	NA
M4-64/32 44 pin PLCC	NA	3.34B	NA	A0/98	2.70E
M4-64/32 44 pin PQFP	NA	3.34B	NA	A0/98	NA
M4-64/32 48 pin TQFP	NA	3.34B	NA	A0/98	NA
M4-96/48 100 pin TQFP	NA	3.20J	NA	NA	NA
M4-192/96 144 pin TQFP	NA	3.20P	NA	NA	NA
M5LV-128/68 100 pin PQFP	8.10.16	3.03A	NA	B0/98	NA
M5LV-128/68 100 pin TQFP	8.10.16	3.03A	NA	B0/98	NA
M5LV-128/74 100 pin TQFP	NA	3.03C	NA	B0/98	NA
M5LV-128/104 144 pin PQFP	NA	3.03A	NA	B0/98	NA
M5LV-128/104 144 pin TQFP	NA	3.03A	NA	B0/98	NA
M5LV-128/120 160 pin PQFP	NA	3.03A	NA	B0/98	NA

MACH DEVICE PROGRAMMING UPDATE (CONTINUED)

Device	Stag Eclipse	HI-LO/Tribal ALL07/Flex700	ADVIN U40 / U84	SMS/Sprint Expert	Sys General Turpro-1/FX/TX
M5LV-256/68 100 pin PQFP	8.10.16	3.03A	NA	B0/98	NA
M5LV-256/68 100 pin TQFP	8.10.16	3.03A	NA	B0/98	NA
M5LV-256/74 100 pin TQFP	NA	3.03D	NA	B0/98	NA
M5LV-256/104 144 pin PQFP	8.10.16	3.03D	NA	B0/98	NA
M5LV-256/120 160 pin PQFP	NA	3.02C	NA	B0/98	NA
M5LV-256/160 208 pin PQFP	NA	3.02C	NA	B0/98	NA
M5-128/68 100 pin PQ/TQ	8.10.16	3.0C	10.85C	A0/97	2.32B
M5-128/104 144 pin PQFP	8.10.16	3.0C	10.85C	A0/97	2.32B
M5-128/120 160 pin PQFP	8.10.16	3.0B	10.85C	A0/97	2.32B
M5-192/68 100 pin PQ/TQ	8.10.16	3.0C	10.84B	A5/97	2.30K
M5-192/104 144 pin PQFP	8.10.16	3.0C	10.84B	A5/97	2.30K
M5-192/120 160 pin PQFP	8.10.16	3.0B	10.84B	C5/96	2.30K
M5-192/160 208 pin PQFP	8.10.16	3.0C	10.84B	C5/06	2.30K
M5-256/68 100 pin PQ/TQ	7.6.13	3.0C	10.84B	A0/97	2.30J
M5-256/104 144 pin PQFP	7.8.1	3.0C	10.84B	A5/97	2.30J
M5-256/120 160 pin PQFP	7.7.21	3.0B	10.84B	A5/97	2.30J
M5-256/160 208 pin PQFP	7.6.13	3	10.84B	C5/96	2.30J
M5-320/120 160 pin PQFP	7.8.1	3.02	10.86J	A5/97	2.35C
M5-320/160 208 pin PQFP	7.8.1	3.02	10.86H	A5/97	2.35C
M5-320/184 240 pin PQFP	7.8.1	3.02	10.87C	B0/97	2.35C
M5-320/192 256 ball BGA	7.8.1	3.02C	10.86H	B0/97	2.35C
M5-384/120 160 pin PQFP	7.8.1	3.02	10.86H	A5/97	2.35C
M5-384/160 208 pin PQFP	7.8.1	3.02	10.86H	A5/97	2.35C
M5-384/184 240 pin PQFP	7.8.1	3.02C	10.87C	B0/97	2.35C
M5-384/192 256 ball BGA	7.8.1	3.02C	10.86H	B0/97	2.35C
M5-512/120 160 pin PQFP	7.8.1	3.02	10.85E	A5/97	NA
M5-512/160 208 pin PQFP	7.8.1	3.02	10.85E	A0/97	NA
M5-512/184 240 pin PQFP	7.8.1	3.02	10.85E	B0/97	NA
M5-512/192 256 ball BGA	7.8.1	3.02C	10.86H	B0/97	NA
M5-512/256 352 ball BGA	7.8.1	3.02D	10.86H	B0/97	NA

Notes:

1. *Entries in this table are minimum required programming algorithm revisions. These revisions or current approved revisions are acceptable.*
2. *EV=Engineering version, under evaluation*
3. *NS=Not supported due to hardware limitations or marketing considerations; NA=Contact Vantis or programmer vendors for support information.*
4. *x=Programming support on the programmer manufacturer's bulletin board is to be used with indicated revision*
5. **=Require use of adapter*

MACH SOCKET ADAPTERS

The following sockets are available for adapting MACH products for programming through 28-pin DIP sockets on Approved Programmers.

Device	Package	California Integration Coordinators, Inc.	Emulation Technology, Inc.
MACH 110	44-pin PLCC		AS-44-28-01P-300-YAM
MACH 111	44-pin PLCC		AS-44-28-01P-300-YAM
	44-pin TQFP	CIC-44TQ-28D-B6-ENP	AS-44-28-01TQ-6ENP-SP
		CIC-44TQ-28D-A6-BNP	AS-44-28-01TQ-600-ENP
MACH 111SP	44-pin PLCC		AS-44-28-01P-300-YAM
	44-pin TQFP	CIC-44TQ-28D-B6-ENP	AS-44-28-01TQ-6ENP-SP
MACH 120	68-pin PLCC	CIC-68PL-28D-A6-YAM	AS-68-28-05P-300-YAM
MACH 130	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 131	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 131/1	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 131SP	100-pin PQFP	CIC-100QF-28D-A6-YAM	AS-100-28-03Q-600
	100-pin TQFP	CIC-100TQ-28D-B6-YAM	
MACH 210	44-pin PLCC		AS-44-28-01P-300-YAM
	44-pin TQFP	CIC-44TQ-28D-B6-ENP	AS-44-28-01TQ-6ENP-SP
		CIC-44TQ-28D-A6-BNP	AS-44-28-01TQ-600-ENP
MACH 211	44-pin PLCC		AS-44-28-01P-300-YAM
	44-pin TQFP	CIC-44TQ-28D-B6-ENP	AS-44-28-01TQ-6ENP-SP
		CIC-44TQ-28D-A6-BNP	AS-44-28-01TQ-600-ENP
MACH 211SP	44-pin PLCC		AS-44-28-01P-300-YAM
	44-pin TQFP	CIC-44TQ-28D-B6-ENP	AS-44-28-01TQ-6ENP-SP
MACH 215	44-pin PLCC		AS-44-28-01P-300-YAM
MACH 220	68-pin PLCC	CIC-68PL-28D-A6-YAM	AS-68-28-05P-300-YAM
MACH 221	68-pin PLCC	CIC-68PL-28D-A6-YAM	AS-68-28-05P-300-YAM
MACH 221SP	100-pin PQFP	CIC-100QF-28D-A6-YAM	AS-100-28-03Q-600
MACH 230	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 231	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 231/1	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 231SP	100-pin PQFP	CIC-100QF-28D-A6-YAM	AS-100-28-03Q-600
	100-pin TQFP	CIC-100TQ-28D-B6-YAM	
MACH 355 or M4-96/96	144-pin PQFP		AS-144-28-01Q-600
MACH 435	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 436 or M4-128N/64	84-pin PLCC	CIC-84PL-28D-A6-YAM	AS-84-28-04P-600-YAM
MACH 445	100-pin PQFP	CIC-100QF-28D-A6-YAM	AS-100-28-03Q-600
MACH 446 or M4-128/64	100-pin PQFP	CIC-100QF-28D-A6-YAM	AS-100-28-03Q-600
MACH 446 or M4-128/64	100-pin TQFP	CIC-100TQ-28D-E6-YAM	
MACH 466 or M4-256/128	208-pin PQFP	CIC-208PQ-28D-B6-YAM	AS-208-28-02Q-6
M4-256/128	256-ball BGA	CIC-256BGA-28D-B6-PLA	

Device	Package	California Integration Coordinators, Inc.	Emulation Technology, Inc.
M4-32/32 or M4-64/32	44-pin TQFP	CIC-44TQ-28D-C6-ENP	
	48-pin TQFP	CIC-48TQ-28D-A6-YAM	
	44-pin PLCC		AS-44-28-01P-3-YAM
M4-96/48	100-pin TQFP	CIC-100TQ-28D-E6-YAM	
M4-192/96	144-pin TQFP	CIC-144TQ-28D-B6-YAM	
MACH5-128	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	144-pin PQFP	CIC-144QF-28D-A6-YAM	
	100-pin PQFP	CIC-100QF-28D-C6-YAM	
	100-pin TQFP	CIC-100TQ-28D-D6-YAM Rev. 2	
MACH5-192	208-pin PQFP	CIC-208QF-28D-A6-YAM	AS-208-28-04Q-6YAM
	240-pin PQFP	CIC-240QF-28D-A6-YAM	
	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	144-pin PQFP	CIC-144QF-28D-A6-YAM	
	100-pin PQFP	CIC-100QF-28D-C6-YAM	
	100-pin TQFP	CIC-100TQ-28D-D6-YAM Rev. 2	
MACH5-256	208-pin PQFP	CIC-208QF-28D-A6-YAM	AS-208-28-04Q-6YAM
	240-pin PQFP	CIC-240QF-28D-A6-YAM	
	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	144-pin PQFP	CIC-144QF-28D-A6-YAM	
	100-pin PQFP	CIC-100QF-28D-C6-YAM	
	100-pin TQFP	CIC-100TQ-28D-D6-YAM Rev. 2	
MACH5-320	208-pin PQFP	CIC-208QF-28D-A6-YAM	AS-208-28-04Q-6YAM
	240-pin PQFP	CIC-240QF-28D-A6-YAM	
	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	256-pin BGA	CIC-256SBGA-28D-A6-PLA	
MACH5-384	208-pin PQFP	CIC-208QF-28D-A6-YAM	AS-208-28-04Q-6YAM
	240-pin PQFP	CIC-240QF-28D-A6-YAM	
	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	256-pin BGA	CIC-256SBGA-28D-A6-PLA	
MACH5-512	208-pin PQFP	CIC-208QF-28D-A6-YAM	AS-208-28-04Q-6YAM
	240-pin PQFP	CIC-240QF-28D-A6-YAM	
	160-pin PQFP	CIC-160QF-28D-A6-YAM	AS-160-28-02Q-600
	256-pin BGA	CIC-256SBGA-28D-A6-PLA	
	352-pin BGA	CIC-352SBGA-28D-A6-PLA	

Contacts:

California Integration Coordinators, Inc.
656 Main Street
Placerville, CA 95667
(916) 626-6168 Tel.
(916) 626-7740 Fax.

Emulation Technology, Inc.
World Headquarters
2344 Walsh Avenue, Building F
Santa Clara, CA 95051-1301 U.S.A.
(408) 982-0660 Tel.
(408) 982-0664 Fax

PAL DEVICE PROGRAMMING UPDATE

Device	Data I/O Autosite	Data I/O Unisite	Data I/O 2900	Data I/O 3900	BP Micro 1128	BP Micro 1200/1400
PALCE16V8Z-XX	1.5	3.6	1.9	1.3	1.86	2.05
PALCE16V8H/Q-XX/4/5	1.5	3.4	1.6	1.3	1.55	2.15
PALLV16V8-XX	2.1	4.4	3.2	2.2	2.25C	2.25C
PALLV16V8Z-XX	2.1	4.4	3.2	2.2	2.25C	2.25C
PALCE20V8H/Q-XX/4/5	2.5	4.7	3.5	2.5	2.19	2.05
PALCE22V10H/Q-XX/4/5	2.5	4.7	3.5	2.5	3.0	3.0
PALCE22V10Z	2.5	4.7	3.5	2.5	3.0	3.0
PALLV22V10Z-XX/5	2.5	4.7	3.5	2.5	2.25C	2.25C
PALLV22V10	2.5	4.7	3.5	2.5	2.33	2.33
PALCE20RA10H-XX	2.3	4.9	3.3	2.7	1.55	3.01
PALCE24V10	2.1	3.4	1.5	1.3	1.55	2.05
PALCE26V12-XX/4	2.7	4.9	1.9	2.7	1.79	1.68B
PALCE29M16/4	2.1	3.4	1.5	1.3	1.61	2.15
PALCE29MA16/4	2.1	3.4	1.5	1.3	1.61	2.15
PALCE610H-XX	2.3	4.5	3.3	2.3	2.19	2.21C

PAL DEVICE PROGRAMMING UPDATE (CONTINUED)

Device	Stag Quasar	Logical Devices AllPro 88	HI-LO / Tribal ALL07 / Flex700	ADVIN U40 / U84	SMS / Sprint Expert	Sys General Turpro-1 / FX / TX
PALCE16V8Z-XX	10.75A	2.2	3.54a	10.36	3/92	1.68B
PALCE16V8H/Q-XX/4/5	10.75A	2.1	3.54a	10.1	3.4	1.5
PALLV16V8-XX	10.75A	2.6	3.54a	10.75A	B/94	2.2
PALLV16V8Z-XX	10.75A	2.4	3.54a	10.75A	B/94	2.2
PALCE20V8H/Q-XX/4/5	10.75A	2.1	3.54a	10.1	1/93	1.5
PALCE22V10H/Q-XX/4/5	10.75A	2.2	3.54a	10.1	3/92	1.68B
PALCE22V10Z	10.75A	2.2	3.54a	10.1	3/92	1.5
PALLV22V10Z-XX/5	10.75A	2.4	3.54a	10.75A	B/92	2.2
PALLV22V10	10.77	2.4	3.54a	10.77	A/92	2.2
PALCE20RA10H-XX	10.75A	2.1	3.54a	10.21	3.5	1.5
PALCE24V10	10.75A	2.2	3.35	10.21	3.4	1.68B
PALCE26V12-XX/4	10.75A	2.2	3.35	10.39	3.5	1.68B
PALCE29M16/4	10.75A	2.2	3.54a	10.61	3.5	1.5
PALCE29MA16/4	10.75A	2.2	3.54a	10.61	A/95	1.5
PALCE610H-XX	10.75A	2.1	3.54a	10.75A	3.4	1.68G

Notes:

1. *Entries in this table are minimum required programming algorithm revisions. These revisions or current approved revisions are acceptable.*
2. *PAL is a registered trademark of Vantis Corp.*

SELF QUAL VENDORS

Advantech Equipment Corp. (Taiwan)	B & C Microsystems, Inc.	Elan Digital Systems, Ltd.
7FI, No 98, Ming Chuan Road Shin-Tien City, Taipei Taiwan Tel 011 886-2-2218-2325	846 Del Rey Avenue Sunnyvale, CA 94086 USA Tel (408) 730-5511	Elan House, Little Park Farm Road Sagensworth West, Farenham, Hants, PO15 5SJ UK
Electronic Engineering Tools	**ICE Technology Ltd.**	**Leap Electronic Co. Ltd.**
544 Weddell Drive, Suite 6 Sunnyvale, CA 94089 USA Tel (408) 734-8184	Unit 4, Penistone Court, Station Buildings Penistone, S.York S30 6HG UK Tel 011-44 (0) 1226-767404	6th Fl-4, No. 4, Lane 609 Chunghsin Road, Sec.5 Sangchung, Taipei Hsien Taiwan Tel 011 (886) 2-999-1860 x37
Logical Devices	**MICROPROSS**	**Minato Electronics, Inc. (USA)**
1221 South Clarkson Suite 200 Denver, CO 80202 USA Tel (303) 722-6868 x215	33, Rue Gantois 5900 Lille France Tel 33-03-20-74-6630	3628 Madison Ave., Suite 5 North Highlands, CA 95660 USA Tel (916) 348-6066
MQP Electronics Ltd.	**Owen Electronic Gmbh**	**Phyton, Inc.**
Unit 2 Park Road Centre Makmesbury, Wilts SN16 OBX UK Tel 011-0-1666-825-66	Fritz-Wunderlich-Strasse 51 Postfach 1104, D-6798 Kusel, Germany Tel 011-06381-4202-0	7206 Bay Parkway, 2nd Floor Brooklyn, NY 11204 USA Tel (718) 259-3191
Sunrise Electronics, Inc.	**Xeltek**	
675 Brea Canyon Road, Unit #6 Walnut, CA 91789 USA Tel (909) 595-7774	3444 De La Cruz Blvd. Santa Clara, CA 95054 USA Tel (408) 588-9942	

VANTIS

BEYOND PERFORMANCE

Technical Support

Vantis provides extensive technical support for its programmable logic devices and associated software and responds quickly to customers' technical questions via e-mail, fax or telephone. Vantis also provides a worldwide network of applications engineers to provide local support where required.

Vantis provides the following customer support services:

- Customer Design Support
- Technical Support Hotline
- Electronic Mail
- World Wide Web Site

CUSTOMER DESIGN SUPPORT

Vantis Field and Factory Applications Engineers (FAE) will assist customers with designs to find the best solution for customers' requirements. Please contact a local Vantis sales office for support. Vantis FAEs will then work with customers at their company site as needed to reach a satisfactory solution.

TECHNICAL SUPPORT HOTLINE

US & Canada	Phone:	(888) VANTIS-1 or (888) 826-8471
	Fax:	(408) 616-7894
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Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices

ABSTRACT

Vantis provides robust and feature-rich I/O structures on its MACH® 4 and MACH 5 families of devices. To take advantage of these features, it is helpful to understand the characteristics on both a family basis and a technology basis. This technical note will describe two Vantis I/O characteristics: hot socketing and mixed supply design as they pertain to the MACH 4 and MACH 5 families manufactured in Vantis' 0.50-µm (EE6.5) and 0.35-µm (EE7) process technologies.

BACKGROUND

The Vantis MACH 4 and MACH 5 CPLD families have superior routability, performance, and I/O characteristics that make them ideal for today's complex system designs. The routability features include multiple switch matrices, complex macrocell architectures, wide product-term allocators, and large numbers of inputs into the arrays. The performance features include fast, predictable speeds, power management capabilities, and slew rate control. Detailed information about MACH routability and performance can be obtained from the MACH data sheets.

The I/O characteristics are what really set the MACH 4 and MACH 5 devices apart from all other architectures. Some of the advanced features they offer to enhance a system design include Bus-Friendly™ latches, hot socketing, mixed supply capability, and PCI compliance. Due to their dependence on process technology, hot socketing and mixed supply design capability need additional description over that found in the data sheets.

Vantis has access to world class process technologies. The two process technologies used in the manufacture of the MACH 4 and MACH 5 devices are the 0.50-µm L_{eff} process and the 0.35-µm L_{eff} process. As device feature sizes are reduced, so must the voltage supply because of the internal electric fields that are generated across the gate oxides. The 0.50-µm process is a 5-volt technology, while the 0.35-µm process is a 3.3-volt technology. As a result, the designs used in the I/O and input buffers will be different and will have somewhat different characteristics. Table 1 shows which of these process technologies is used to manufacture the MACH 4 and MACH 5 devices, and what V_{CC} supplies each can be used with.

Table 1. Device Process and Supply Reference

V_{cc} Supply	0.50-µm	0.35-µm
3.3 Volts		All M4LV-M5LV
5 Volts	M5-128	All M4
	M5-192	M5-320,M5-384
	M5-256	M5-512

Application Notes

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HOT SOCKETING

Hot socketing is a feature that means different things to different designers. There are two common scenarios found in hot socketing environments. The first is when a board or device is plugged into a system that is already powered-up. The second is a board in a system where the board is powered-down while the system is still powered-up and active, and the powered-down board or devices continue to be connected to the active nets in the system. Due to design differences between the two manufacturing processes, various MACH devices will behave differently for each hot socketing scenario.

In the scenario where a device or board is plugged into an already powered-up system, the principal cause for concern is latch-up. When inserting a part or board, it can be several milliseconds before all of the required connections have been made, and there is no particular order in which those connections are made. As a result, signal pins can be connected and driven before either V_{CC} or ground, and this can lead to latch-up in CMOS devices if they are not designed to handle this condition. When a device latches-up, a low-impedance path to ground is formed within the device, and the device begins to sink large amounts of current. If the situation is not rectified quickly (i.e., by cycling the system power), the device could be thermally destroyed, necessitating its replacement.

In the scenario where a powered-down device is in a powered-up system, the possibility of signal disturbance can arise. Signal disturbance takes place when an inactive device affects the functionality of active signals. This can happen when the inactive device has a leakage path to either V_{CC} or ground, or when the device is driving the signal line during power-up or power-down. All MACH 4 and MACH 5 devices tri-state their I/Os during power-up and power-down, and as a result, this is not a concern for bus disturbance.

Hot Socketing Specification

The most dangerous of the two hot socketing scenarios takes place when a voltage is placed on an input, and the device goes into latch-up as a result. Most devices are designed to prevent latch-up from happening when V_{CC} is at a nominal level such as 5.0 volts or 3.3 volts. When V_{CC} is at 0.0 volts however, the situation is much different in that signals driven into inputs or I/Os could potentially force the device into latch-up. The hot socket latch-up current specification in Table 2 indicates the amount of latch-up current that MACH devices can tolerate without being damaged. This information also appears in the Absolute Maximum Ratings section of the device data sheets.

Table 2. I_{LUHS} Specification

Parameter Symbol	Parameter Description	Test Description	Max	Unit
I_{LUHS}	Hot Socket Latch-up Current	V_{CC} = 0.0 Volts, V_{IN} = 5.5 Volts	200	mA

The second of the two scenarios is much less dangerous from both the device standpoint and the system design standpoint. When a device no longer has power applied to it yet is still connected to active signals and busses, that device should have no effect on the active signals. If it does, precautions must be taken to ensure the system will not be adversely affected and can tolerate the strong leakage paths. If the system cannot tolerate the influence of the powered-down devices, there are design techniques that can be employed to work around the problems.

5-Volt, 0.50-µm I/O Buffer Hot Socketing Characteristics

The 5-volt, 0.50-µm MACH 5 devices are perhaps the most robust of the devices from the hot socketing standpoint. Not only do they meet the requirements for latch-up current, but they also have a minimal amount of leakage current when the devices have no power applied. During power-up, all of the MACH 4 and MACH 5 devices have their output drivers disabled such that the I/Os are in a high impedance state. Because of the design and the process, the 0.50-µm MACH 5 devices have a leakage current of less than 10 µA when V_{CC} = 0.0 volts and 0 V < V_{pin} < 5.5 V.

5-Volt, 0.35-µm I/O Buffer Hot Socketing Characteristics

As with the 5-volt, 0.50-µm devices, the 5-volt, 0.35-µm MACH 4 and MACH 5 devices also meet the requirements for latch-up. These devices are not as robust as the 0.50-µm devices when it comes to leakage current and source a significant amount of current that must be considered when using these devices in a hot socketing environment. During power-up and power-down, the output drivers are disabled. However, because of the nature of the 3.3-volt process and its design requirements, there is a parasitic diode that becomes forward biased and will source current when V_{CC} is less than 0.7 volts. The I-V curves in Figure 1 show the leakage current that can be expected on an input or I/O pin for a typical device when 0 V < V_{CC} < 0.6 V. Note that the differences in I_{LK} for 0.4 V < V_{CC} < 0.6 V are minimal and are represented in Figure 1 by V_{CC} = 0.6 volts.

The curves are shown with V_{PIN} at a maximum value of 3.0 volts. This was done because minimum V_{IH} levels for most devices are 2.0 volts or greater, and 3.0 volts will provide sufficient margin. When designing a system which could be affected by devices exhibiting leakage current when V_{CC} = 0 volts, the primary consideration that must be taken into account is the integrity of the signal levels and the ability to maintain minimum V_{IH} levels. Because the leakage currents are relatively small for this group of devices, the effects can be overcome with the use of pull-up resistors on the signals connected to the MACH device. To have the desired effect, the pull-up resistors must be placed at the system level that will remain powered-up rather than on the board where the MACH device is located that will be powered-down. The example below shows how to select the correct value for a pull-up resistor that will overcome the leakage current on a signal which needs to be held high during power-up:

Example: V_{CC} =5.0 volts, V_{IH} (min) = 2.0 volts

at V_{IH} (min) = 2.0 volts and a device V_{CC} of 0.0 volts (worst case), I_{LK} = 0.85 mA then RPU = (V_{CC} - V_{IH}) / I_{LK} = (5 V - 2 V) / 0.85mA = 3.53 KΩ

The pull-up resistor needed to maintain signal integrity would have a value of 3.3 KΩ.

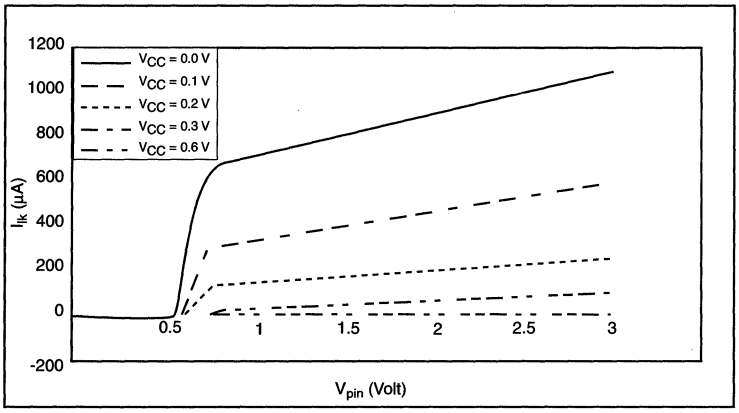

Figure 1. 5-Volt, 0.35-µm Typical Leakage Current Characteristics

3.3-Volt, 0.35-µm I/O Buffer Hot Socketing Characteristics

The 3.3-volt MACH 4 and MACH 5 devices meet the requirements for latch-up current but are significantly worse when it comes to leakage current as shown below in Figure 2. The maximum leakage current is nearly 9 mA when V_{CC} is 0 volts and V_{PIN} is 3.0 volts. Using the assumptions from the example above, the resistor value needed to maintain minimum V_{IH} levels is on the order of 462 Ω. This smaller resistor will have an adverse effect on both speed and power consumption and should be avoided. The reason for the increased leakage current is a result of the need for PMOS transistors in the design of the output buffers to pull the output up to the V_{CC} rail when the pin is driving high. The PMOS transistor creates a parasitic diode that is the source of the leakage when V_{CC} < 0.7 volts.

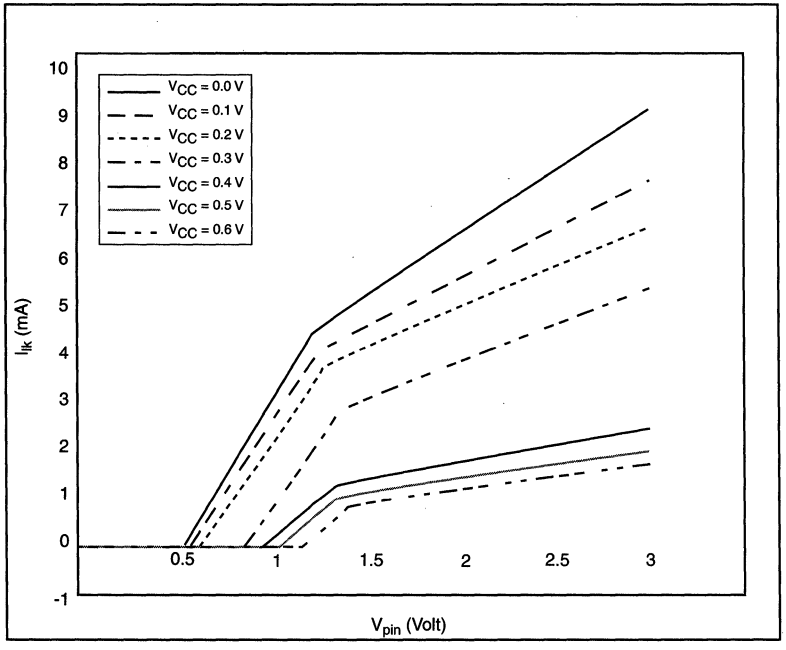

Figure 2. 3.3-Volt, 0.35-µm Typical Leakage Current Characteristics

As a result, the design techniques needed to use the 3.3-volt, 0.35-µm devices in a hot socketing environment are somewhat more difficult and costly to implement. One technique is to use buffers or FET equivalent switches on the signals connected between the MACH device and the system. The drawback to this approach is that additional board space is required and there is an additional delay in the speed paths. If board space is not at a premium and speed is not an issue, this may be an acceptable option. A second technique that can be implemented is the use of hot-socket connectors which keep power and ground supplied to the board until after the signal lines have been disconnected. They have longer power and ground pins that guarantee the I/Os are disconnected prior to (for hot removal) or connected after (for hot insertion) the supply connections. By doing so, there is no need to first power down a board before inserting or removing it from a system. When using this option, it is important for a designer to understand exactly how the system will respond in this situation. These techniques, while not optimal, will allow the use of these devices in a design requiring hot socketing capability.

MIXED SUPPLY DESIGN

As the semiconductor industry migrates from a 5-volt process technology to a 3.3-volt process technology, the need to be able to design in a mixed supply environment becomes increasingly important. There are four situations to be aware of when designing in such an environment to ensure the reliability of all devices. The first is when a 3.3-volt device drives the input of a 5-volt MACH device. The second is when a 5-volt MACH device drives the input of a 3.3-volt device. The third is when a 3.3-volt MACH device drives the input of a 5-volt device, and the final is when a 5-volt device drives the input of a 3.3-volt MACH device. All of the conditions are described by the minimum and maximum specifications for V_{OH} and V_{IH}.

5-Volt Tolerant and 3.3-Volt Safe Specifications

The specification for 5-volt tolerance deals with the device input levels while 3.3-volt safety deals with device output levels. For a 3.3-volt device to be 5-volt tolerant, it must be able to handle an input as great as V_{CC} (max) for the 5-volt device when V_{CC} of the 3-volt MACH device is at a minimum. For a 5-volt device to be 3.3-volt safe, its outputs must drive no higher than V_{IH} (max) of the 3.3-volt device when V_{CC} for the 3.3-volt device is at a minimum and V_{CC} for the 5-volt MACH device is at its maximum value. Furthermore, the source current of the pin being driven by the 5-volt MACH device should be 0 mA. Additionally, the same 5-volt MACH device must meet the minimum requirements needed to reliably interface with devices that conform to the TTL level specification. The TTL specification requires that the outputs drive no less than the V_{IH} (min) of the 5-volt TTL device when V_{CC} (5-volt TTL device) is at a minimum and with a load current of 3.2 mA. The ideal specifications are given in Table 3, and are derived from the requirements needed for both 5-volt TTL and 3.3-volt CMOS devices. The 3.3-volt CMOS requirements can be found in the JEDEC LVCMOS specification, JED-8A. The value for V_{OH} (max) is given for a 5-volt device driving into a 3.3-volt CMOS device that is operating at its minimum V_{CC} of 3.0 volts. In this condition, the determining factor is set by the CMOS device's V_{IH} (max) limit of V_{CC} + 0.3 when V_{CC} is at 3.0 volts and with no source current. If a nominal V_{CC} of 3.3 volts is assumed rather than the minimum V_{CC} of 3.0 volts, V_{OH} (max) will be 3.6 volts. The conditions necessary to meet the hot socketing requirements without going into latch-up also guarantee the V_{IH} specifications in Table 3. This includes all of the MACH 4 and MACH 5 devices. All of these MACH devices will also meet the minimum TTL specification for V_{OH} when V_{CC} = Min and I_{OH} = -3.2 mA. The following discussions will cover the V_{OH} maximum specification.

Table 3. 5-Volt Tolerant/3.3-Volt Safe Ideal Specifications

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4		V
V_{OH}	Output High Voltage	V_{CC} = Max, I_{OH} = 0 mA		3.3	V
V_{IH}	Input High Voltage	V_{CC} = Min		5.5	V

0.50-µm, 5-Volt Device Mixed Supply Design Characteristics

The 0.50-µm devices were not originally designed to meet the specifications given above, and as a result do not meet them. This does not, however, mean these devices cannot be used in a mixed supply environment. When V_{CC} is at 5.25 volts, an output will typically need to source less than 25 µA to provide an output voltage of 3.6 volts. Additionally, many systems will not be designed to operate at the maximum V_{CC} of 5.25 volts, but rather will operate at the more typical 5.0 volts. The design of the output buffer is such that when V_{CC} drops 0.1 volts, so does the output voltage. As a result, a more typical V_{OH} when V_{CC} is at 5.0 volts will be around 3.4 volts. This ensures that a 5-volt device can drive a 3.3-volt device running at 3.1 volts or greater.

The 0.50-µm devices were designed such that V_{OH} will be no greater than 3.3 volts with a source current of -3.2 mA when V_{CC} (min) = 4.75 volts. All of the 0.50-µm devices will meet this specification, but are not considered 3.3-volt safe since they do not meet an I_{OH} specification which is compatible with CMOS device inputs. These devices are tested to meet a specification of V_{OH} = 3.5 volts when V_{CC} = 5.25 volts and I_{OH} = -1.5mA.

An additional measure of safety can be added at the system level by using series current limiting resistors on those outputs that are required to be 3.3-volt safe. The series resistor should be no less than 150 Ω, which will limit the maximum amount of current driven into the 3.3-volt device's input. This also ensures that the current flow into the ESD structure on that input will be less than 10 mA, which is considered safe in terms of latch-up current (typically specified at 200 mA).

0.35-µm, 3.3-Volt and 5-Volt Device Mixed Supply Design Characteristics

The 0.35-µm, 3.3-volt devices will not have any difficulty meeting the V_{OH} (max) specifications because their output buffers can only drive up to the level of V_{CC}. As a result, for the 3.3-volt MACH 4 and MACH 5 devices, V_{OH} (max) = V_{CC}. The design of the 0.35-µm, 5-volt device output buffers limits the maximum output voltage to 3.3 volts when V_{CC} = Max and I_{OH} = 0 mA. All of the 0.35-µm MACH 4 and MACH 5 devices are safe for mixed supply design and can accept inputs from or drive outputs to any 3.3-volt or 5-volt device.

CONCLUSION

The MACH 4 and MACH 5 devices offer several advanced features that can be invaluable in a system design. To take full advantage of these features, the designer must be aware of the effects that each feature may have on the system. Because of process and design differences, not all of the devices will act in quite the same manner. The classifications for each of the devices are:

- 5-volt, 0.50-µm MACH 5 devices - M5-128, M5-192, and M5-256
- 5-volt, 0.35-µm MACH 4 and MACH 5 devices - All MACH 4 devices, M5-320, M5-384, and M5-512
- 3.3-volt, 0.35-µm MACH 4 and MACH 5 devices - All MACH 4LV and MACH 5LV devices

Where hot socketing is concerned, there are differences between all three of the categories that the designer needs to be aware of. With mixed supply design, the differences are found between the 0.50-µm devices and the 0.35-µm devices and are primarily concerned with V_{OH} levels. By knowing and understanding the differences between the devices, a designer will be able to best use the advanced features offered in each.

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MACH 4 Timing and High Speed Design

INTRODUCTION

When implementing a design into a MACH® 4 device, it is often critical to understand how the placement of the design will affect the timing. The MACH 4 device has numerous paths a signal can take, each of which affects the timing in one fashion or another. To more accurately describe the different paths, the MACH 4 timing model has been enhanced[1]. This application note explains the new MACH 4 timing model and high-speed design techniques utilizing this timing model.

MACH 4 ARCHITECTURE BASICS

The fundamental architecture of the MACH 4 device consists of multiple optimized PAL® blocks (PAL33/34V16) interconnected by a programmable central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with multiple paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins. This concept is illustrated in Figure 1. In a MACH 4 device, all signals incur the same delays, regardless of routing. Performance is design-independent and is guaranteed by Vantis' SpeedLocking™ feature.

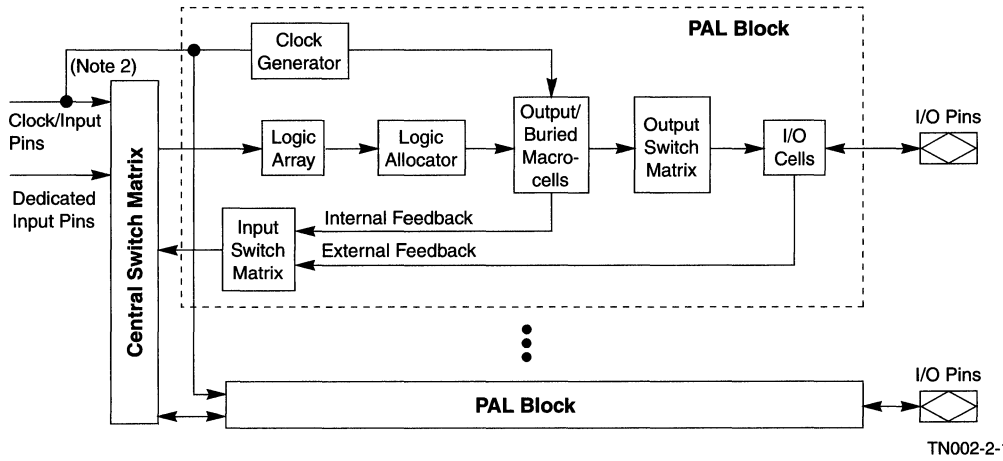

Figure 1. MACH 4 Block Diagram and PAL Block Structure

As indicated in Figure 1, any given macrocell output signal has two different feedback paths into the switch matrix. These two paths are referred to as **internal feedback** and **external feedback**.

1. The new timing model is implemented in MACHXL® software v.6.1 and later.
2. M4-192/96 and M4-256/128 do not have clock/input pins connected to central switch matrix.

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A signal uses internal feedback when it is fed back into the central switch matrix without going through the output switch matrix and the I/O cell. When a signal is fed back into the central switch matrix after having gone through the output switch matrix and the I/O cell, it is using external feedback. For simplicity, the output switch matrix and the I/O cell together are modeled as an output buffer. Both feedback types are shown below in Figure 2.

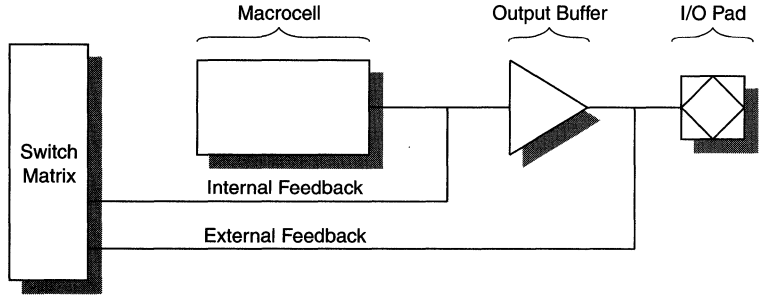

Figure 2. MACH 4 Signal Feedback Types

ENHANCED MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device while, at the same time, be easy to understand. To accomplish the accuracy, the distinction between internal and external feedback is made. To make the timing model easier to understand and use, the timing is modularized so that each logic element in the signal path will have its own parameters. In particular, the new parameters associated with the input register/latch are a result of this. A diagram representing the MACH 4 timing model is shown in Figure 3.

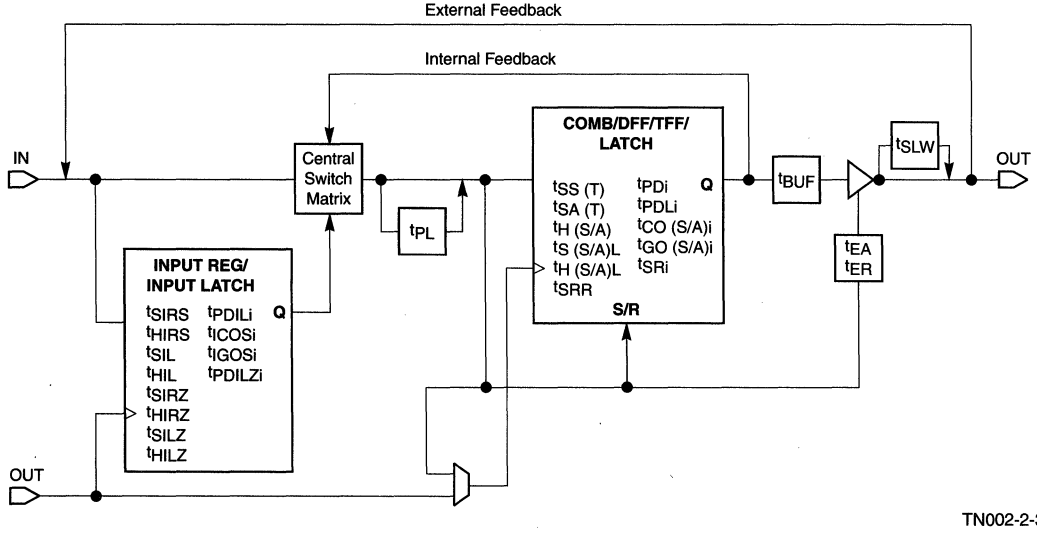

Figure 3. Enhanced MACH 4 Timing Model

Table 1 lists the MACH 4 timing parameters and their descriptions. To understand the new timing model and parameters, an understanding of the naming convention is necessary. An "i" has been added to all parameters that have delays that are "internal" to the device. Several parameters in both the macrocell register and the input register are affected by the change from external parameters to internal parameters. Delays for parameters that have an "i" appended to them are measured to an internal node rather than to an I/O. Table 2 describes the parameters using this convention.

Table 1. MACH 4 Family Timing Parameters

Combinatorial Delay:	t_{PDi}	Internal combinatorial propagation delay
Register Delays:	t_{SS}	Synchronous clock setup time, D-type register
	t_{SST}	Synchronous clock setup time, T-type register
	t_{SA}	Asynchronous clock setup time, D-type register
	t_{SAT}	Asynchronous clock setup time, T-type register
	t_{HS}	Synchronous clock hold time
	t_{HA}	Asynchronous clock hold time
	t_{COSi}	Synchronous clock to internal output
	t_{COAi}	Asynchronous clock to internal output
Latch Delays:	t_{SSL}	Synchronous Latch setup time
	t_{SAL}	Asynchronous Latch setup time
	t_{HSL}	Synchronous Latch hold time
	t_{HAL}	Asynchronous Latch hold time
	t_{PDLi}	Transparent latch to internal output
	t_{GOSi}	Synchronous Gate to internal output
	t_{GOAi}	Asynchronous Gate to internal output
Input Register Delays:	t_{SIRS}	Input register setup time
	t_{HIRS}	Input register hold time
	t_{ICOSi}	Input register clock to internal feedback
Input Latch Delays:	t_{SIL}	Input latch setup time
	t_{HIL}	Input latch hold time
	t_{IGOSi}	Input latch gate to internal feedback
	t_{PDILi}	Transparent input latch to internal feedback
Input Register Delays with ZHT Option:	t_{SIRZ}	Input register setup time - ZHT
	t_{HIRZ}	Input register hold time - ZHT
Input Latch Delays with ZHT Option:	t_{SILZ}	Input latch setup time - ZHT
	t_{HILZ}	Input latch hold time -ZHT
	t_{PDILZi}	Transparent input latch to internal feedback - ZHT

Table 1. MACH 4 Family Timing Parameters (Continued)

Output Delays:	t_{BUF}	Output buffer delay
	t_{SLW}	Slow slew rate delay adder
	t_{EA}	Output enable time
	t_{ER}	Output disable time
Power Delay:	t_{PL}	Power-down mode delay adder
Reset and Preset Delays:	t_{SRi}	Asynchronous reset or preset to internal register output
	t_{SRR}	Asynchronous reset and preset register recovery time

Table 2. MACH 4 Internal/External Parameters Description

External Parameter	Internal Parameter	Description
t_{PD}	t_{PDi}	Input, I/O, or feedback to feedback
t_{COS}	t_{COSi}	Global clock to feedback
t_{COA}	t_{COAi}	Product term clock to feedback
t_{SR}	t_{SRi}	Asynchronous Reset or Preset to registered or latched feedback
$t_{GO(S/A)}$	$t_{GO(S/A)i}$	Latch gate to feedback
t_{PDL}	t_{PDLi}	Input, I/O or feedback to feedback through transparent latch
	t_{BUF}	Feedback to Output

Many of the parameters from the original timing model can be derived from the new, modularized timing parameters. In the enhanced timing model, these original parameters have been eliminated. A list of the eliminated parameters and their derivations is shown in Table 3.

Table 3. Derivation of Eliminated Parameters

Eliminated Parameter and its Description		Derivation
t_{IGOL}	Input latch gate to output through transparent output latch	$t_{IGOSi} + t_{PDLi} + t_{BUF}$
t_{IGO}	Input latch gate to combinatorial output	$t_{IGOSi} + t_{PDi} + t_{BUF}$
t_{IGSA}	Input latch gate to output latch setup using PT output latch gate	$t_{IGOSi} + t_{SAL}$
t_{IGSS}	Input latch gate to output latch setup using global output latch gate	$t_{IGOSi} + t_{SSL}$
t_{ICO}	Input register clock to combinatorial output	$t_{ICOSi} + t_{PDi} + t_{BUF}$
t_{ICS}	Input register clock to output register setup, D-type	$t_{ICOSi} + t_{SS}$
t_{ICS}	Input register clock to output register setup, T-type	$t_{ICOSi} + t_{SST}$
t_{SLLA}	Setup time from input through transparent input latch to PT output gate	$t_{PDILi} + t_{SAL}$
t_{SLLS}	setup time from input through transparent input latch to output gate	$t_{PDILi} + t_{SSL}$
t_{PDLL}	Input to output through transparent input and output latches	$t_{PDILi} + t_{PDLi} + t_{BUF}$
t_{PDLI}	Input, I/O, or feedback to output through input register	$t_{PDILZi} + t_{PDi} + t_{BUF}$

Table 3. Derivation of Eliminated Parameters (Continued)

Eliminated Parameter and its Description		Derivation
t_{SLLAI}	Setup time from input through transparent input latch to PT output gate	$t_{PDILZi} + t_{SAL}$
t_{SLLSI}	Setup time from input through transparent input latch to output gate	$t_{PDILZi} + t_{SSL}$
t_{PDLLI}	Input to output through transparent input and output latches	$t_{PDILZi} + t_{PDLi} + t_{BUF}$

To maintain consistency with the timing models of other MACH families, some of the parameters have been renamed. In particular, the set/reset parameters, t_{RP}, t_{PRW}, and t_{PRR}, have been renamed to t_{SR}, t_{SRW}, and t_{SRR}. Information about all of the timing parameters can be found in the *MACH 4 (A) Family Data Sheet* and in Table 1.

Feedback Timing

In the original MACH 4 timing model, the only feedback path reported in a MACHXL timing report was the external feedback path. Signals using internal feedback were reported as if they had gone through the external feedback path. As a result, the reported delays for those signals would be greater than what would actually be seen in the real device. The new MACH 4 timing model now makes a distinction between those signals using internal feedback and those using external feedback.

To make the distinction between internal and external feedback, several timing parameters have been changed, and the parameter t_{BUF} has been introduced. All of the changed parameters deal with a signal going to the I/O pad. As an example, the parameter t_{PD} was originally defined as an input, I/O or feedback going to a combinatorial output. This parameter is now the sum of two parameters: t_{PDi} and t_{BUF}. The parameter t_{PDi} is defined as the time it takes an input, I/O or feedback to go through a combinatorial path to the internal feedback, while t_{BUF} is the time it takes to go from internal feedback through the output buffer and to the I/O pad.

Input Register/Latch Timing

Another area in which the MACH 4 timing model has been improved is in the reporting of input register/latch timing. Because there was no mechanism for reporting the internal timing of a MACH 4 device, the timing used for input registers/latches could become complicated. The specifications found in the original MACH 4 data sheets relied on timing that went through both an input register/latch and an output register/latch. As an example, the parameter t_{ICOA} represented the clock-to-output time for a signal to go through an input register to a combinatorial macrocell, plus the time it took to go through the combinatorial macrocell and to an I/O pad. This method of determining timing was very difficult for the software implementation of the timing model and for designers attempting to determine their timing requirements.

The MACH 4 timing model has greatly simplified the input register timing by reporting all parameters as internal feedback. The same parameter, t_{ICO}, will no longer exist but rather will be calculated as t_{ICOi}, the clock-to-internal feedback of the input register, plus a t_{PDi} and a t_{BUF}. Because of this modularized timing model, several of the original input register/latch specifications have been eliminated.

USING THE MACH 4 TIMING MODEL

The use of the MACH 4 timing model will be demonstrated using two examples. The first example is a combinatorial logic design and demonstrates the use of internal feedback. The second example is a synchronous sequential logic design and demonstrates how to calculate f_{MAX}.

Example 1

This combinatorial logic design is fit into an M4-64/32. A group of input signals are routed to Block A, which is in high power mode. Logic is generated in array "A" and allocated to macrocell A5, which is configured as a combinatorial path. This logic is sent to pad I/O6, which is configured to have a slow slew rate. The signal delay T1 of this path would be:

$$T1 = t_{PDi} + t_{BUF} + t_{SLW}$$

This logic is also fed back to the central switch matrix via the internal feedback path and then routed to Block D, which is in low power mode. A second logic is generated in array "D" using the first logic along with another group of input signals. This second logic is allocated to macrocell D8, which is configured as a combinatorial path. This second logic is sent to pad I/O31, which is in fast slew rate. The longest delay path of this design would be from Block A to I/O31 and the delay $T_{CRITICAL}$ is:

$$T_{CRITICAL} = t_{PDi} + t_{PL} + t_{PDi} + t_{BUF}$$

The original MACH 4 timing model required an additional t_{BUF} be added to the delay path because internal feedback was not defined.

Example 2

This synchronous sequential logic design has a 16-bit up-counter with load enable and reset. It is fit into an M4-96/48 using 16 macrocells configured with T-type registers. Register inputs are defined by the device inputs and flip-flop output, which is internally fed back to the switch matrix. Under these conditions, the period t_{CNT} is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs.

$$t_{CNT} = t_{COSi} + t_{SST}$$

The f_{MAX} is designated "f_{MAXINT}."

$$f_{MAXINT} = 1/t_{CNT}$$

Again, the original MACH 4 timing model required an additional t_{BUF} be added to the delay path when calculating t_{CNT} because internal feedback was not defined. Consequently, f_{MAX} was slower.

The modular approach to the MACH 4 timing model is straightforward, and its use merely requires the addition of internal parameters to arrive at the device timing.

HIGH SPEED DESIGN WITH MACH 4 DEVICES

While the possibility has always existed to control the implementation of high speed designs into a MACH 4 device, the reporting of the timing never made it easy because no distinction was made between internal and external feedback. The improved MACH 4 timing model makes that critical distinction, making it easier to understand how a design is fit into a device.

During the fitting process, the software may use external feedback on timing critical nodes where internal feedback may be required to meet a particular speed. It is also possible that the software feeds a signal into either the block or global switch matrices, which will affect timing. Constraints can be placed on a design to ensure that the critical paths are fit to meet timing. The more a design is constrained, the more difficult it becomes to fit the design. Some methods that can be used to constrain a design are briefly covered here and are more fully covered in the *MACHXL® User's Manual* and the Application Note entitled, *PI File Reference Guide*. MACHXL software uses the PI File to control the fitting process and constrain the design. It contains pinout and placement information along with directives that determine the fitting algorithms used.

Controlling Feedback

To control the signal feedback path, the PI File directives, FORCE_INTERNAL_FEEDBACK, can be utilized. This PI property forces a signal to use an internal feedback path rather than giving it a choice of using an external or internal feedback path. By forcing a signal to use internal feedback, the delay caused by the output buffer is saved.

CONCLUSION

The MACH 4 timing model provides for a more accurate, easier to understand timing calculation. It defines both internal and external feedback paths and simplifies the timing used for internal registers/latches. By using and understanding the timing model in the proper way, it becomes easier to control the critical path timing in a high speed design using the properties in the PI File.

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MACH 5 Timing and High Speed Design

INTRODUCTION

When implementing a design into a MACH® 5 device, it is often critical to understand how the placement of the design will affect the timing. The MACH 5 device has numerous paths a signal can take, each of which affects the timing in one fashion or another. To more accurately describe the different paths, the MACH 5 timing model has been changed. This technical note explains the new MACH 5 timing model.

MACH 5 ARCHITECTURE BASICS

The architecture used in the MACH 5 family of devices is the next step in the evolution of complex programmable logic devices (CPLDs). A CPLD can be viewed as a group of PLDs connected together by a programmable switch matrix. The MACH 5 devices take the concept of hierarchy one step further by connecting multiple CPLDs together with a programmable switch matrix. This concept is illustrated in Figure 1.

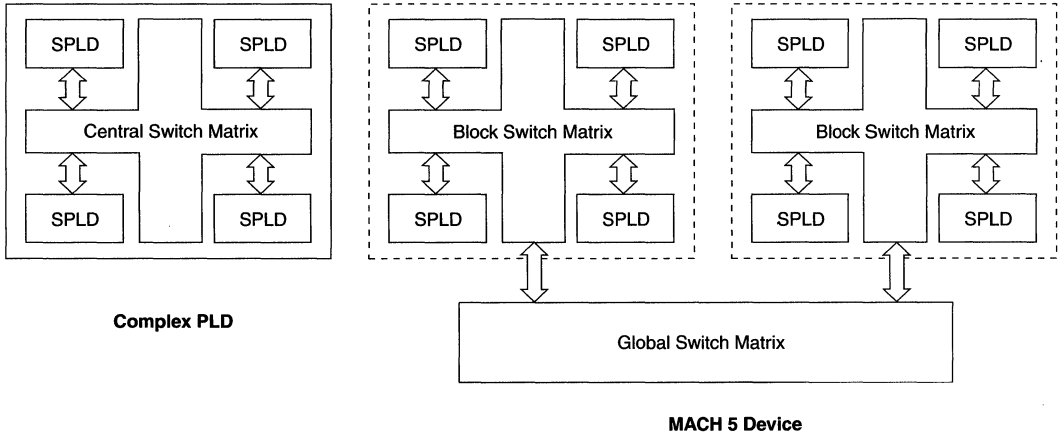

Figure 1. CPLD and MACH 5 Architecture Diagrams

There are several benefits inherent in the MACH 5 architecture including the ability to attain higher densities while maintaining fast speeds. These fast speeds, however, are only available on those paths that use local feedback from a block back into itself. If a signal has to go through a Block Switch Matrix or the Global Switch Matrix, there is an additional adder to speed. In the MACH 1, MACH 2, and MACH 4 devices, where all signals go through the Central Switch Matrix, there are no such adders, so the speed for any given path will be SpeedLocked™.

Application Notes

Feedback Types

Any given macrocell output signal will traditionally have two different feedback paths into the switch matrix. These two paths are referred to as **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback. Both feedback types are shown in Figure 2.

In the previous timing model used for the MACH 5 family of devices, the only feedback path reported in a timing report was the external feedback path. Signals using internal feedback were reported as if they had used an external feedback path. As a result, the reported delays for those signals would be greater than what would actually be seen in the real device. The MACH 5 timing model now makes a distinction between those signals using internal feedback and those using external feedback.

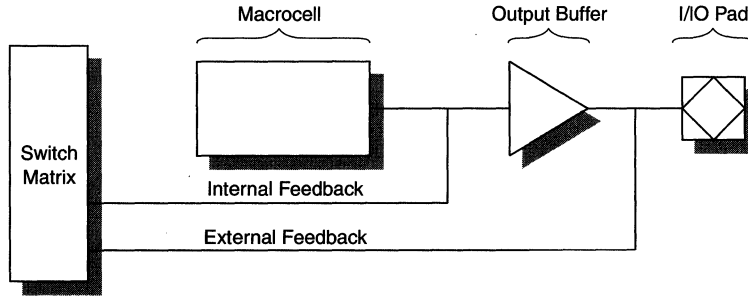

Figure 2. Feedback Types

Input Register Timing

Another area in which the MACH 5 timing model has been improved is in the reporting of input register timing. Because there was previously no mechanism for reporting the internal timing of a MACH 5 device, the timing used for input registers could become complicated. The specifications found in the original MACH 5 data sheets relied on timing that went through both an input register and an output register. As an example, the parameter t_{ICOA} represented the clock-to-output time for a signal to go through an input register to a combinatorial macrocell, plus the time it took to go through the combinatorial macrocell and to an I/O pad. This method of determining timing was very difficult for the software implementation of the timing model and for designers attempting to determine their timing requirements.

The MACH 5 timing model has greatly simplified the input register timing by reporting all as internal feedback. The same parameter, t_{ICOA}, will no longer exist but rather will be calculated as the clock-to-internal feedback of the input register plus a t_{PDi} and a t_{BUF}. The parameter t_{PDi} is the time it takes a signal to go through a combinatorial macrocell to internal feedback, and t_{BUF} is the time it takes a signal to go through the output buffer. Because of this timing methodology, several input register specifications have been removed from the MACH 5 data sheet.

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device while, at the same time, be easy to understand. To accomplish the accuracy, the distinction between internal and external feedback is made. To make the timing easier to understand, the input register specifications are simplified. A diagram representing the MACH 5 timing model is shown in Figure 3.

To make the distinction between internal and external feedback, several timing parameters have been changed, and the parameter t_{BUF} has been added. All of the changed parameters deal with a signal going to the I/O pad. As an example, the parameter t_{PD} was originally defined as an input, I/O or feedback going to a combinatorial output. This parameter is now the sum of two parameters: t_{PDi} and t_{BUF}. The parameter t_{PDi} is defined as the time it takes an input, I/O or feedback to go to a combinatorial feedback, while t_{BUF} is the time it takes to go from feedback, through the output buffer and to the I/O pad. The naming convention used for the changed parameters is to add an "i" after the original name if the signal is going to the internal feedback rather than to the I/O pad. A list of the changed parameters along with their definitions is given in Table 1.

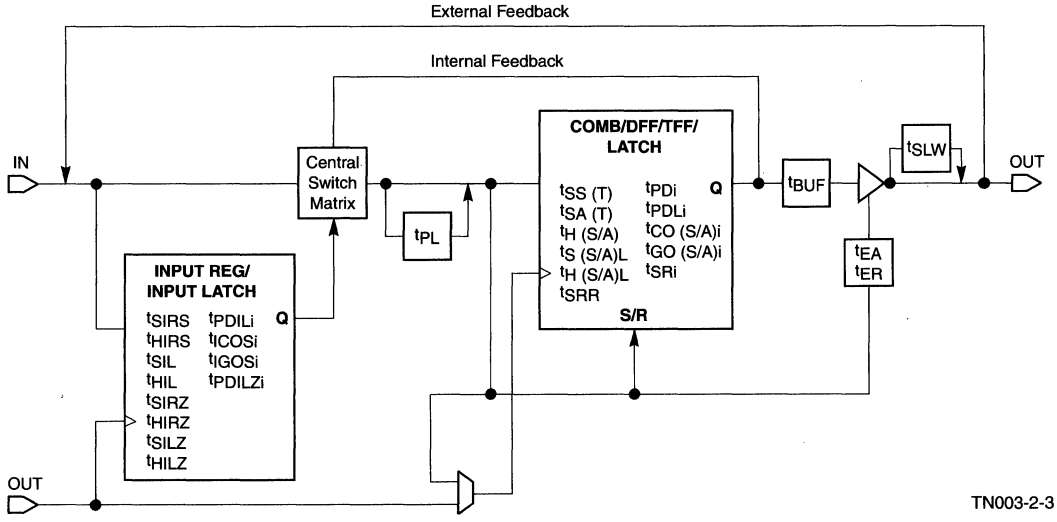

Figure 3. MACH 5 Timing Model

Table 1. MACH 5 Parameter Description

External Parameter	Internal Parameter	Description
t_{PD}	t_{PDi}	Input, I/O, or feedback to feedback
t_{COS}	t_{COSi}	Global clock to feedback
t_{COA}	t_{COAi}	Product term clock to feedback
t_{RP}	t_{SRi}	Asynchronous Reset or Preset to registered or latched feedback
t_{GO}	t_{GOAi}	Latch gate to feedback
t_{PDL}	t_{PDLi}	Input, I/O or feedback to feedback through transparent latch
	t_{BUF}	Feedback to Output

The input register in the MACH 5 device is a macrocell register that takes its input from an I/O pad rather than from the product term array. As a result, the output timing for an input register is the same as that for a macrocell register. Several input register parameters have been eliminated from the original MACH 5 timing model and data sheet because they can now be derived in the new timing model. Table 2 shows the derivations of the eliminated data specifications.

To maintain consistency with the timing models of other MACH families, some of the parameters have been renamed. In particular the set/reset parameters t_{RP}, t_{PRW}, and t_{PRR} have been renamed to t_{SR}, t_{SRW}, and t_{SRR}. Additionally, the latch parameters have been renamed to denote their asynchronous nature. The parameters t_{SL}, t_{HL}, and t_{GO} have been renamed to t_{SAL}, t_{HAL}, and t_{GOA}, respectively. Information about all of the timing parameters can be found in the *MACH 5(A) Family Data Sheet* and is shown below in Table 3.

Table 2. Derivations of Eliminated Parameters

Eliminated Parameter	Derivation
t_{PDIL}	$t_{PDILi} + t_{PDi} + t_{BUF}$
t_{ICOG}	$t_{COSi} + t_{PDi} + t_{BUF}$
t_{ICOA}	$t_{COAi} + t_{PDi} + t_{BUF}$
t_{PDLL}	$t_{PDILi} + t_{PDLi} + t_{BUF}$
t_{RCSS}	$t_{COSi} + t_{SS}$
t_{RCSA}	$t_{COSi} + t_{SA}$
t_{RCAS}	$t_{COAi} + t_{SS}$
t_{RCAA}	$t_{COAi} + t_{SA}$
t_{SLL}	$t_{PDLi} + t_{SL}$

Table 3. MACH 5 Internal Timing Parameter Definitions

Combinatorial Delay:	t_{PDi}	Input, I/O, or Feedback to Combinatorial Feedback
Register Delays:	t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock
	t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock
	t_{HS}	Register Data Hold Time Using a Global Clock
	t_{HA}	Register Data Hold Time Using a Product Term Clock
	t_{COSi}	Global Clock to Feedback
	t_{COAi}	Asynchronous Clock to Feedback
Latch Delays:	t_{SAL}	Setup Time from Input, I/O or Feedback to Product Term Gate
	t_{HAL}	Latch Data Hold Time
	t_{PDLi}	Input, I/O, or Feedback to Feedback through Transparent Latch
	t_{GOAi}	Latch Gate to Feedback
Input Register Delays:	t_{SIRS}	Input Register Setup Time Using a Global Clock
	t_{SIRA}	Input Register Setup Time Using a Product Term Clock
	t_{HIRS}	Input Register Hold Time Using a Global Clock
	t_{HIRA}	Input Register Hold Time Using a Product Term Clock
Input Latch Delays:	t_{SIL}	Input Latch Setup Time Using a Product Term Clock
	t_{HIL}	Input Latch Hold Time
	t_{PDILi}	I/O to Feedback Through Transparent Input Latch
Output Delays:	t_{BUF}	Feedback to I/O Through Output Buffer
	t_{SLW}	Slow Slew Rate Delay
	t_{EA}	Output Enable Time
	t_{ER}	Output Disable Time
Power Delays:	t_{PL1}	Power Level 1 Delay
	t_{PL2}	Power Level 2 Delay
	t_{PL3}	Power Level 3 Delay
Cluster Delay:	t_{PT}	Product Term Cluster Delay
Interconnect Delays:	t_{BLK}	Block Interconnect Delay
	t_{SEG}	Segment Interconnect Delay
Reset/Preset Delays:	t_{SRi}	Asynchronous Reset or Preset to Internal Register Output
	t_{SRR}	Reset and Set Register Recovery Time
Clock Enable Delays:	t_{CES}	Clock Enable Setup Time
	t_{CEH}	Clock Enable Hold Time

USING THE MACH 5 TIMING MODEL

The use of the MACH 5 timing model will be demonstrated with an example. The example includes multiple t_{PD} paths and demonstrates the use of internal feedback.

Example

Signal "A" enters the MACH 5-256 through Block A, Segment 0. It then goes to Node "B" in Block C, Segment 0 and to Output "C" in Block B, Segment 1. Node B is internally fed back to create Output "D" in Block A, Segment 2. Block B, Segment 1 is in high power and Block C, Segment 0 is in low power. All Outputs are configured to have a fast slew rate.

The timing from Signal "A" to Output "C" is given by:

$$t_{DELAY} = t_{PDi} + t_{SEG} + t_{BUF}$$

The t_{PDi} is the time it takes for the signal to go from the input in Block A, Segment 0 to feedback. Because the output is in a different segment, t_{SEG} is added. Finally, t_{BUF} is added as the time it takes to go from feedback to the output.

The timing from Signal "A" to Output "D" through Node "B" is given by:

$$t_{DELAY} = t_{DELAYAB} + t_{DELAYBD}$$

$$t_{DELAYAB} = t_{PDi} + t_{BLK} + t_{PL3}$$

$$t_{DELAYBD} = t_{PDi} + t_{SEG} + t_{BUF}$$

The delay path from Signal "A" to Output "D" is broken up into two elements. The delay from Signal "A" to Node "B", $t_{DELAYAB}$, includes t_{PDi} for the combinatorial delay to feedback, t_{BLK} because Signal "A" and Node "B" are in different blocks inside the same segment, and t_{PL3} because Block C, Segment 0 is in low power. The original MACH 5 timing model required an additional t_{BUF} be added to the delay path because internal feedback was not defined.

The delay path from Node "B" to Output "D", $t_{DELAYBD}$, includes t_{PDi} to account for the delay from feedback to output, t_{SEG} because Node "B" and Output "D" are in different segments, and t_{BUF} to account for the signal going to the output.

The use of the MACH 5 timing model is straightforward and merely requires the addition of internal parameters to arrive at the external parameters or device timing.

HIGH-SPEED DESIGN WITH MACH 5 DEVICES

While the possibility has always existed to control the implementation of high speed designs into a MACH 5 device, the reporting of the timing never made it easy because no distinction was made between internal and external feedback. The improved MACH 5 timing model makes that critical distinction, making it easier to understand how a design is fit into a device.

During the fitting process, the software may use external feedback on timing critical nodes where internal feedback may be required to meet a particular speed. It is also possible that the software feeds a signal into either the block or global switch matrices, which will affect timing. Constraints can be placed on a design to ensure that the critical paths are fit to meet timing. The more a design is constrained, the more difficult it becomes to fit the design. Some methods that can be used to constrain a design are briefly covered here and are more fully covered in the *MACHXL® User's Manual* and the Application Note entitled, *PI File Reference Guide*. MACHXL

software uses the PI File to control the fitting process and constrain the design. It contains pinout and placement information along with directives that determine the fitting algorithms used.

Controlling Feedback

Within the PI File, there are two directives available that provide for the control of signal feedback. The first of these directives, FORCE_INTERNAL_FEEDBACK, forces a signal to use an internal feedback path rather than giving it a choice of using an external or internal feedback path. By forcing a signal to use internal feedback, the delay caused by the output buffer is saved. The second directive, FORCE_LOCAL_FEEDBACK, forces signals to use a local feedback path back into the PAL® block rather than sending the signal into either the block or global level switch matrix. By doing this, the block or segment delay adders are saved.

Grouping Signals

In the PI file, MACHXL software provides for the grouping of signals into either the same block or the same segment. When signals are grouped into a single block, the chances that those signals will be fed back into that block using the local feedback paths increases significantly, thereby increasing the chances that the fastest timing possible is attained. Grouping signals does not guarantee, however, that local feedback will be used. The use of the FORCE_LOCAL_FEEDBACK directive along with grouping signals may be needed to get the required timing.

Pin and Node Locking

The third way to constrain a design is to force both pin locations and node locations. By doing so, the signals can be grouped within a block or segment, and it becomes easier to enforce local feedback on the critical path signals. Information on pin and node locking can be found in the *MACHXL User's Manual.*

CONCLUSION

The MACH 5 timing model provides for a more accurate, easier to understand timing calculation. It defines both internal and external feedback paths and simplifies the timing used for internal registers. By using and understanding the timing model in the proper way, it becomes easier to control the critical path timing in a high speed design using the properties in the PI file.

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MACH 5 Power

MACH® 5 devices are designed to optimize speed and power for high-performance, low-power designs. In a design file, signals are assigned one of the four power/speed levels. The default level is high-speed/high-power. The device can be powered down on a PAL® block by PAL block basis, and signals with the same speed/power setting are partitioned into PAL blocks set to that power level.

While most MACH 5 designs will safely operate within any available package, there are some designs and system conditions that may generate more heat than a package can reliably dissipate. The heat generated is a function of ambient temperature, device current, supply voltage, device loading, and output frequencies.

Power estimation should be done early in the design process. This can then be used to calculate heat generation and a package can be chosen accordingly. A design can also be modified to reduce power and thus reduce heat generation. There are also other ways to increase heat dissipation.

The formula below is for estimating MACH 5 current consumption:

$$I_{CC} = I_{CC}(\text{Device}) + I_{CC}(\text{DC LOAD}) + I_{CC}(\text{AC LOAD})$$

There are both internal and external (loading) current requirements.

DEVICE CURRENT COMPONENT

Device current in milliamps can be calculated with the following formula:

$$I_{CC}(\text{Device}) = (K0*BLK_{PL0}) + (K1*BLK_{PL1}) + (K2*BLK_{PL2}) + (K3*BLK_{PL3}) + (KAC*MC)*F_{AVE}$$

BLK_{PL0} = Number of PAL blocks in Power Level 0

BLK_{PL1} = Number of PAL blocks in Power Level 1

BLK_{PL2} = Number of PAL blocks in Power Level 2

BLK_{PL3} = Number of PAL blocks in Power Level 3

F_{AVE} = Average Output Frequency of Switching macrocells in MHz

MC = Total Macrocells used in the design

K0–K3 = Static Power Device Constants listed in Table 1

KAC = Dynamic Power Device Constant listed in Table 1

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Amendment/**0** Issue Date: **November 1998**

Table 1. Device Constants

Device	BLK_{TOT}	K0	K1	K2	K3	KAC	$T_{J\,(MAX)}$
M5-128	8	21.6	12.83	8.75	4.38	0.13	150 °C
M5LV-128	8	12.5	6.7	4.35	2.5	0.08	130 °C
M5-192	12	19.3	11.0	7.33	3.75	0.13	150 °C
M5-256	16	20.5	11.8	7.46	3.73	0.13	150 °C
M5LV-256	16	12.0	6.5	4.3	2.5	0.08	130 °C
M5-320 M5LV-320	20	10.5	6.75	4.35	2.85	0.08	130 °C
M5-384 M5LV-384	24	10.5	6.75	4.35	2.85	0.08	130 °C
M5-512 M5LV-512	32	10.5	6.47	4.35	2.56	0.08	130 °C

The BLK_{PL0}, BLK_{PL1}, BLK_{PL2}, BLK_{PL3}, and MC variables can be found in the report (.rpt) file. Below is an excerpt from a report file which shows these variables for a particular design. The average macrocell output frequency must be calculated by the designer.

```
POWER SUMMARY:
Number of blocks with power set to LOW is 0
Number of blocks with power set to MED_LOW is 0
Number of blocks with power set to MED_HIGH is 0
Number of blocks with power set to HIGH is 16

DEVICE RESOURCE UTILIZATION:
```

Resource	Available	Used	Remaining	%
Clock Pins:	4	0	4	0
I/O Pins:	160	160	0	100
Input Regs:	32	0	32	0
Macrocells:	**256**	**256**	**0**	**100**
Pterms	1168	1048	120	89
1-pt Clusters:	256	256	0	100
3-pt Clusters:	256	256	0	100
Feedbacks	512	216	296	42
Fanouts:	512	368	144	71
Intersegment Lines:	128	0	128	0

Device I_{CC} Is Affected by Temperature and Supply Voltage

I_{CC} is linearly affected by temperature. The given formula for typical conditions (16-bit counters in each PAL block, 25°C and 5-V V_{CC}). Temperature, V_{CC}, and the I_{CC} increase or decrease are shown in Tables 2 and 3. These values are characterized but not tested.

Table 2. Effect of Supply Voltage on I_{CC}

Supply Voltage (V)	M5-128	M5-192	M5-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
4.5 or 3.0 (LV)	–11%	–11%	–11%	–6%	–6%	–6%
4.75	–6%	–6%	–6%	–3%	–3%	–3%
5.25	+7%	+7%	+7%	+1%	+1%	+1%
5.5 or 3.6 (LV)	+13%	+13%	+13%	+3%	+3%	+3%

Table 3. Effect of Ambient Temperature on I_{CC}

Ambient Temperature	M5-128	M5-192	M5-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
T = –40°C	+14%	+14%	+14%	–4%	–4%	–4%
T = 0°C	+1%	+1%	+1%	–1%	–1%	–1%
T = 70°C	–1%	–1%	–1%	+2%	+2%	+2%
T = 85°C	–1%	–1%	–1%	+5%	+5%	+5%

LOAD COMPONENT

The AC load current required by capacitive loading is dependent on voltage, capacitance, and average output frequency.

AC Load Component

No. of I/Os used

$$I_{CC}\ (AC\ Load) = \sum_{n=1} F_n * C_n * (V_{OH} - V_{OL})$$

F_n = *Output frequency of output*

C_n = *Capacitive loading of output*

V_{OH} = *Output Voltage High of the output*

V_{OL} = *Output Voltage Low of the output*

DC Load Component

No. of I/Os used

$$I_{CC}\ (DC\ Load) = \sum_{n=1} V_{OUTn}/R_n$$

V_{OUTn} = *Output frequency of output*

R_n = *Resistive loading of output*

CALCULATING PACKAGE POWER REQUIREMENTS

A package must be able to dissipate enough power to keep the internal silicon junction temperature below the maximum allowable junction temperature ($T_{J(MAX)}$). The following formula is used to calculate the maximum power allowable for a particular package.

$$V_{CC} * I_{CC} \leq (T_{J(MAX)} - T_A)/\Theta_{JA}$$

V_{CC} = *Supply Voltage*

I_{CC} = *Calculated Current*

T_A = *Ambient Temperature*

Θ_{JA} = *Junction-Ambient Thermal Impedance*

The maximum allowable power for a package is dependent on the thermal resistance of that package. Packages with a low thermal resistance are able to dissipate more heat than packages with a high thermal resistances. Air flow can also reduce the thermal impedance. Θ_{JMA} is the junction to ambient thermal impedance with air flow.

THERMAL MANAGEMENT OPTIONS

If an application generates more heat than a package can dissipate, then steps can be taken to reduce heat generation such as:

1. **Power down additional PAL blocks**—Few designs require all signals to run at maximum frequencies. The four power/speed options per PAL block allow optimization for the lowest power at the highest speeds.
2. **Use an external heat sink**—The external heat sink will decrease the thermal impedance of a package and raise the maximum allowable temperature.
3. **Reduce the load on the outputs**—In many applications, heavily loaded outputs significantly increase power requirements. The Bus-Friendly™ inputs and I/Os do not require external resistive loading to float to a known state. Capacitive loading should also be monitored at high frequencies.
4. **Reduce device utilization**—Device current requirements depend on device utilization. Lowering utilization will lower the current required. Multi-device partition facilitates this process.
5. **Choose a package with lower thermal resistances**—Packages with a low thermal resistance are able to dissipate more heat than packages with a high thermal resistances.
6. **Reduce the average output frequency**—The average output frequency affects both the device and load components of power. Reducing the output frequency will reduce the required power.
7. **Reduce the number of outputs**—Reducing outputs reduces the load current required. Multi-device partitioning facilitates this process.
8. **Lower V_{CC}**—Use a 3.3-V device instead of a 5-V device. While I_{CC} is nearly identical, the lower V_{CC} results in lower power.

EXAMPLE POWER ESTIMATION

Counters

The average output frequency of a counter is one-eighth the output frequency of the least significant bit (LSB) of the counter. The most power efficient method for implementing several high speed counters would place the LSBs in a high speed PAL block and the most significant bits (MSBs) in a lower-power PAL block. If all PAL blocks are set to the same power level and the I_{CC} vs. frequency is measured, the following formula is used:

$$I_{CC}(\text{Device}) = BLK_{TOT}*K(x) + KAC*F_{AVE}*MC_{TOT}$$

An example of this is for the M5LV-256 device in high-power mode with a 16-bit counter pattern per PAL block at a clock frequency of 125 MHz. If positive or negative edge clocking is used, then the LSB, will switch at 62.5 MHz, and the average output frequency will be 8 MHz. The equation would be as follows:

$$I_{CC}(\text{Device}) = (16)*(12.0) + (0.08)*(8)*(256) = 356\ \text{mA}$$

If under the same conditions, biphase clocking is used, then a 125 MHz clock produces a 125 MHz LSB, and the average output frequency doubles to 16 MHz:

$$I_{CC}(\text{Device}) = (16)*(12.0) + (0.08)*(16)*(256) = 520\ \text{mA}$$

To determine if this design will run safely in the 208 PQFP package, the following calculation is done:

$$V_{CC}*I_{CC}*\Theta_{JA} + T_A \leq 130\,^{\circ}\text{C}$$

$$(3.3)(0.356)(33) + 70 = 108\,^{\circ}\text{C} \leq 130\,^{\circ}\text{C}$$

This design will safely operate in this package.

VANTIS

BEYOND PERFORMANCE

The Evolution of Bus-Friendly Inputs and I/Os

INTRODUCTION

Vantis' PLDs have evolved over time. Like Darwin's theory of evolution and adaptation, Vantis' PLDs have evolved and adapted to the dynamic world of digital logic. When Vantis' PLDs were first introduced to the market in the mid-1980s, they had different characteristics than the PLDs presently in existence. The older devices were larger in size, slower in speed, and hungrier for power than their contemporary counterparts. As the computer industry evolved to accommodate applications requiring faster, smaller, and lower power devices, PLDs were modified in order to accommodate these changes and stay competitive in the PLD market arena.

DEVICES WITH UNBIASED INPUTS AND I/O

Originally, Vantis introduced PLDs with unbiased inputs and I/Os which is basically a carry over of the bipolar configuration. The circuit configuration is shown in Figure 1 and consists of a buffer that is directly connected to the pin pad.

If the pin is left unconnected, this configuration is termed "floating" because an unused input pin is allowed to float to any state, since there is no circuitry that would bias the pin to a known state. The consequence in leaving the pin floating is that excessive noise or having a voltage near the threshold voltage of the PLD could influence the PLD to produce an unwanted oscillatory output that could disturb the system. In addition, the noise on V_{CC} will also increase due to this oscillation. Figure 2 shows the event of device oscillation due to a noisy input signal through an unused input pin.

Even though it is recommended to tie unused input pins to ground or V_{CC}, traces must be cut on a printed circuit board in order to free the tied pins when changes are made. Unfortunately, this poses an inconvenience to the customer. As a result, Vantis decided it was best to modify the input and I/O circuitry of all PLD devices.

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Amendment/**0** Issue Date: **November 1998**

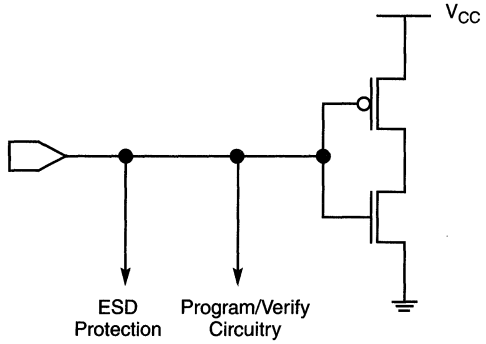


Figure 1. Equivalent Schematic of the Unbiased Input and I/O Scheme

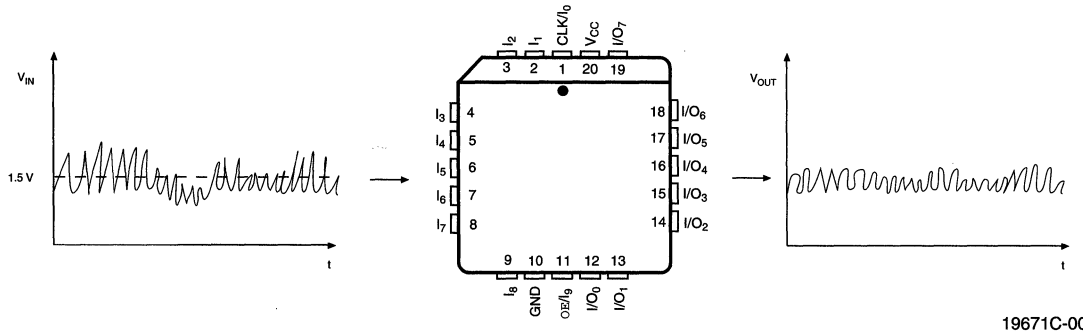


Figure 2. Output Oscillation Due to Noisy Input of an Unbiased "Floating" Input Pin

PULL-UP RESISTOR ENHANCEMENT

The improvement was to add a pull-up resistor to the input and I/Os so that if the pins were left floating, the device could pull its pin voltage to a known voltage state. Figure 3 shows the circuit configuration of the pull-up resistor scheme.

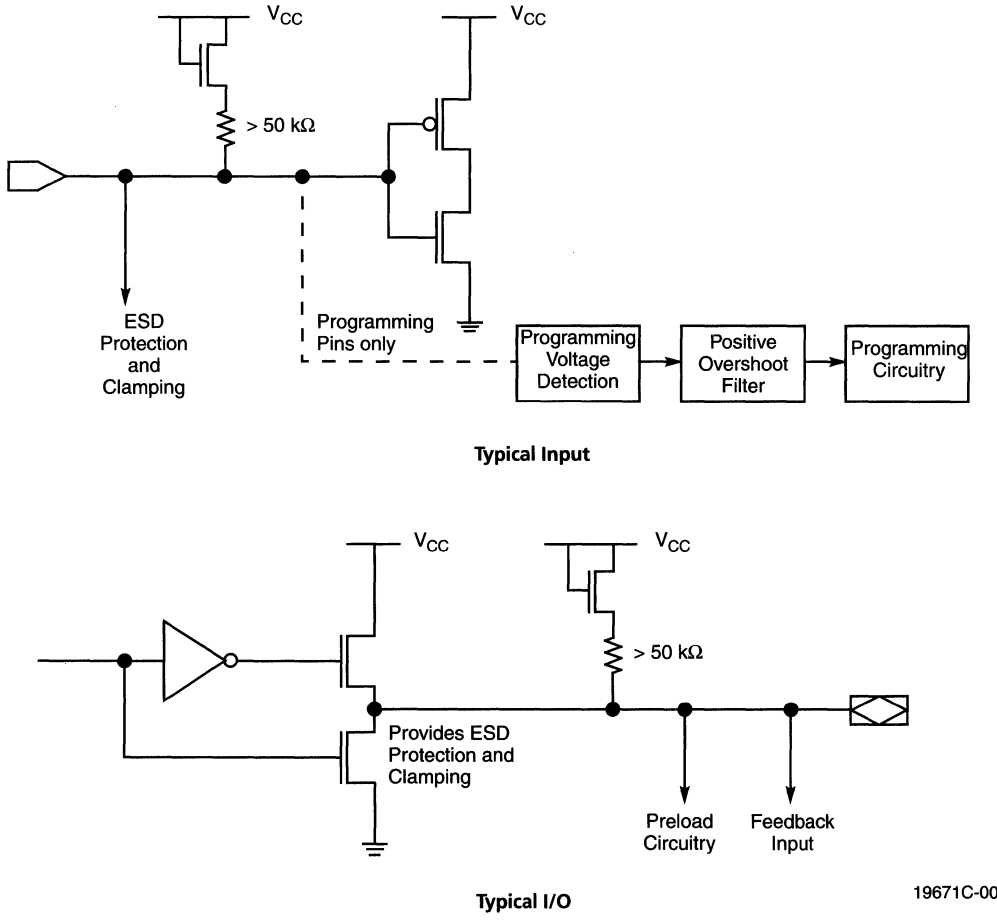
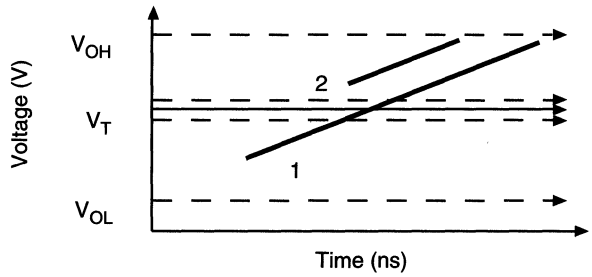


Figure 3. Equivalent Schematic of Pull-up Resistor Scheme

This scheme consists of a 50 kΩ resistor that is connected to a constant current source which is used to hold down any excessive current in the event that the 50 kΩ resistor is disabled. The pull-up resistor scheme pulls the voltage of the pin to about 3.5 V-4.0 V. The 50 kΩ resistor value is used because this value provides a voltage that is easy enough for another driver to overcome when necessary because of the current-limiting effect of the large resistance.

Even though the pin is pulled to a known state, the pull-up scheme can potentially introduce oscillation to a system if the voltage of a tri-state bus is left below the threshold voltage of the PLD. The reason for the potential problem is due to the nature of the pull-up resistor within the PLD. The internal pull-up resistor is only capable of pulling from a low to a high voltage state.

In addition, the slew rate is slow due to the 50 kΩ current-limiting resistor. Thus, when a pin voltage is left below the threshold voltage of the PLD, the pull-up resistor has no other choice but to pull the pin voltage slowly through the threshold voltage region of the PLD. On the contrary, if the voltage of the tri-state bus is at a voltage state higher than the threshold voltage of the PLD, then the PLD will not exhibit oscillation. Note that if some other device overpowers the weak pull-up resistor of the PLD causing the tri-state bus voltage to reside around the threshold voltage of the PLD, then device oscillation is also possible. Both the high and low tri-state bus scenarios are shown in slew rate curves in Figure 4.



Bus Scenario

1 = Tri-State Bus left low with Pull-up scheme
2 = Tri-State Bus left high with Pull-up scheme

19671C-004

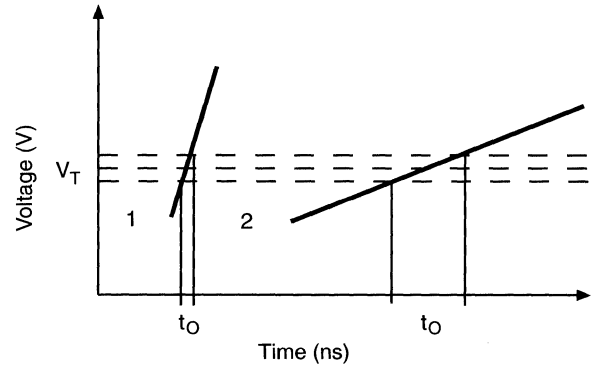
Figure 4. Slew Rate Comparison of Pull-up Scheme Showing Bus Scenarios

DEVICE OSCILLATION

The reason a device oscillates is because of the nature of the threshold voltage of the transistors within the input and I/O buffers of the PLD. Typically, the threshold voltage of an input buffer is 1.5 V. When a pin voltage is around the threshold voltage, the complementary transistor pair does not know whether to switch high or low, thus oscillation is possible at the output. Usually, this fickle nature lasts no more than a few nanoseconds; however, for faster systems this can be significant.

When a large pull-up resistor is used such as those used in the PLD industry, the slow slew rate allows the voltage to reside in the threshold region longer than if a smaller pull-up resistor is used. For comparison, Figure 5 shows the difference in the time of oscillation between a 50 kΩ resistor and a 1 kΩ resistor through slew rate curves.

Because the possibility of device oscillation could occur with the pull-up resistor scheme, another scheme had to be implemented.



1 = Slew rate of 1 kΩ pull-up resistor
2 = Slew rate of 50 kΩ pull-up resistor
t_O = Time of potential oscillation

19671C-005

Figure 5. Slew Rate Comparison Between a 1 kΩ and 50 kΩ Pull-up Resistor

BUS-FRIENDLY INPUT AND I/O

Bus-Friendly™ inputs and I/Os have the ability to hold the input buffer at either a high or a low depending on the last state of the pin connected to the bus. The scheme is termed "Bus-Friendly" because it allows the bus connected to the PLD to be left at any state (other than the 1.5 V threshold voltage of the input and I/O buffers). For PAL devices, the Bus-Friendly scheme is accomplished by reconfiguring already existing resources of the pull-up scheme as shown in Figure 6.

In MACH® devices, the scheme is configured slightly differently by having a separate circuit perform the "latch" characteristic as shown in Figure 7.

The Bus-Friendly circuitry pulls the voltage at the input buffer to a TTL voltage high or low. This input and I/O scheme is accomplished by a double inverter input buffer which loops back to the input of the PLD through a 100 kΩ resistor. This configuration acts as a "latch" because it holds the pin voltage of the PLD at either a TTL level high or low until the pin voltage of the PLD changes state. Bus-Friendly circuitry weakly holds the voltage so that another driver on the bus can overcome the voltage when necessary. Please note that the default state of the pin is no longer a voltage high but is rather dependent on the last driven state of the pin. Designers who need to have the pull-up feature will need to provide an external pull-up resistor rather than depend on the pull-up resistor of the PLD.

The Bus-Friendly scheme provides a solution to the instance where the pull-up scheme could potentially cause input buffer oscillation. As illustrated earlier in Figure 4, the pull-up scheme cannot resolve the case when the tri-state bus connected to the PLD is left at a voltage below the threshold voltage of the PLD. This type of bus scenario promotes undesirable device oscillation. The Bus-Friendly idea is an improvement over the pull-up resistor scheme because

the Bus-Friendly circuitry does not allow the voltage to cross the threshold region of the PLD, thus avoiding the possibility of device oscillation. Figure 8 shows how Bus-Friendly PLDs deal with the same bus scenarios that the pull-up resistor scheme did in Figure 4.

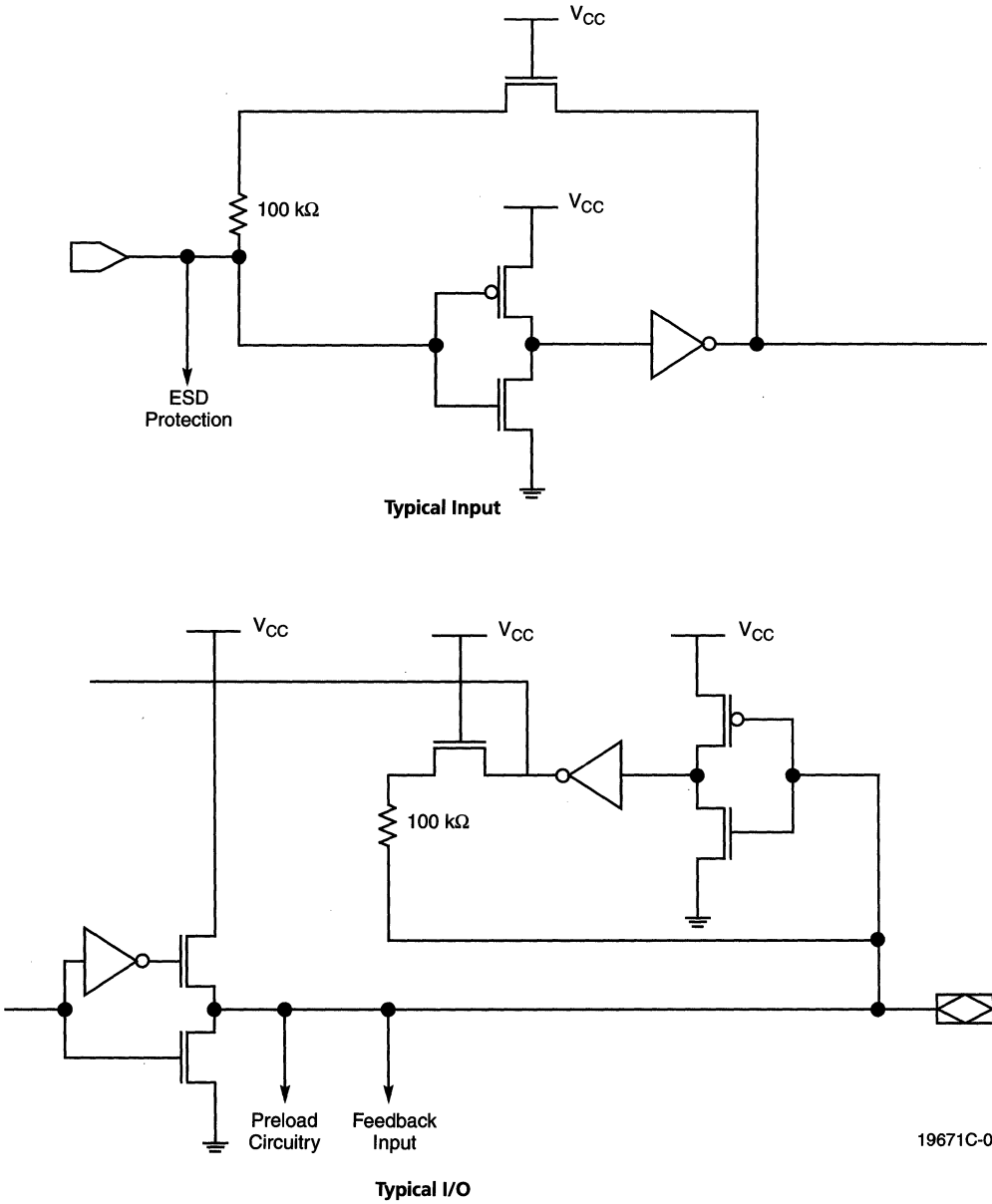


Figure 6. Equivalent Schematic of the Bus-Friendly Input and I/O for PAL Devices

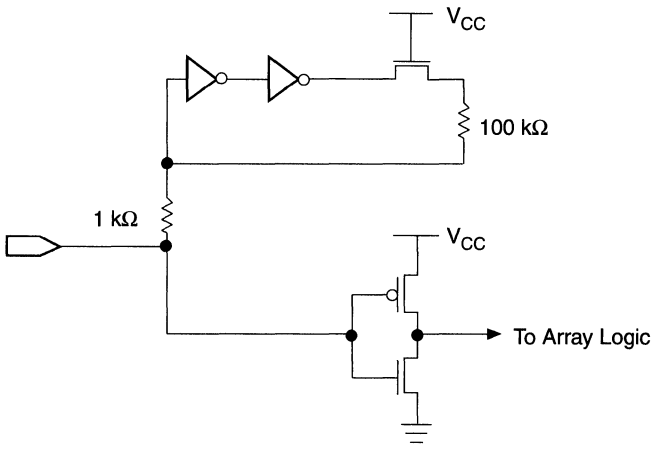


Figure 7. Equivalent Schematic of the Bus-Friendly Input and I/O for MACH CPLDs

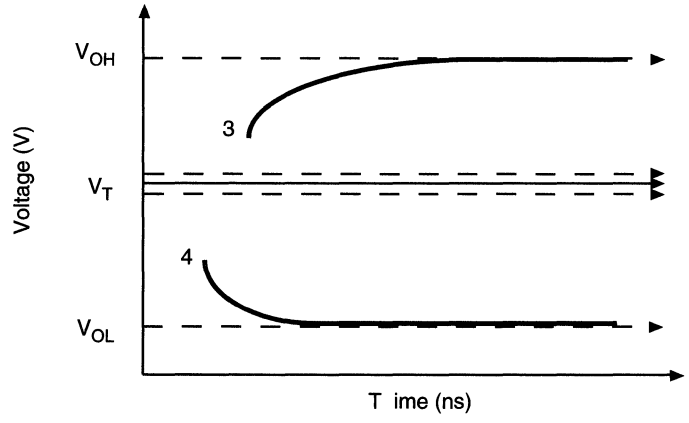


Figure 8. Slew Rate Comparison of Bus-Friendly Scheme Showing Bus Scenarios

Note that if another driver on the bus is forcing the tri-state bus to reside in the threshold voltage region of the PLD, then no matter what type of input and I/O scheme is used, the PLD can oscillate for a few nanoseconds.

The Bus-Friendly enhancement does not affect the existing DC and AC specifications for both the MACH and PAL products which previously had the pull-up resistor enhancement. Bus-Friendly was intended to remedy device oscillation without changing any of the device specifications.

SUMMARY

Just as the computer industry has evolved, so have Vantis' PLDs. The input and I/O circuitry of Vantis PLDs have changed to accommodate the different applications that have emerged due to the evolution of the computer industry. The circuitry has evolved from unbiased to pull-up to Bus-Friendly inputs and I/Os. The unbiased inputs and I/Os have disadvantages due to the nature of the floating input. When left unconnected, unbiased inputs and I/Os "float" and are susceptible to the influence of noise, which can cause the PLD to oscillate. Because of this oscillation, the pull-up resistor became the next link in the PLD input and I/O evolution chain.

The pull-up resistor can bias an unconnected pin to a high voltage state. However, the one-dimensional nature of the large pull-up resistor could not avoid device oscillation in particular situations. As board designs required the tri-state bus to be left low, the current-limiting, internal pull-up resistor would slowly pull the voltage of the pin through the threshold region of the PLD, thus causing device oscillation. Because this situation can potentially occur in different instances other than the low voltage, tri-state bus scenario, it was clear that a new pin bias scheme should be implemented.

Bus-Friendly inputs and I/Os have the ability to hold the last voltage state of the tri-state bus at a discrete TTL voltage level. The advantage of this scheme is that a tri-state bus can be at either a high or a low voltage state without having the PLD oscillate. It is because of this feature the name "Bus-Friendly" was used to describe this pin bias scheme.

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Mixed Supply Design with MACH 1 & 2 SP Devices

ABSTRACT

Vantis provides robust and feature-rich I/O structures on members of its MACH® 1 & 2 SP families. To make the most use of these features, it is helpful to understand their characteristics. This technical note will describe mixed supply design as it pertains to the MACH 1 & 2 SP[1] families.

MIXED SUPPLY DESIGN

As more and more devices move from a 5-volt to a 3.3-volt process technology, the need to be able to design in a mixed supply environment becomes increasingly important. Interfacing a 5-volt device with a 3.3-volt device requires special I/O buffer designs that prevent the 5-volt device from damaging the 3.3-volt device either by putting it into latch-up or by putting too high a voltage across the gate oxides. When a device latches-up, a low-impedance path to ground is formed within the device, and the device begins to sink large currents. If the situation is not rectified quickly (i.e., by cycling the system power), the device could be thermally destroyed, necessitating its replacement. When excessive voltages are driven across a gate oxide, long-term reliability problems could develop. There are two features semiconductor manufacturers provide to avoid the problems in interfacing 5-volt and 3.3-volt devices:

- *3.3-Volt Safety* — The maximum output voltage of a 5-volt device is limited to a level that is compatible with 3.3-volt devices.
- *5-Volt Tolerance* — The maximum allowable input voltage of a 3.3-volt device is such that it is compatible with the typical maximum output voltage of a 5-volt device.

This brief describes 3.3-volt safety in more detail and how the MACH 1 & 2 SP devices can be used in environments that require the use of a 3.3-volt safe device.

3.3-Volt Safe Specifications

For a 5-volt device to be safe for 3.3-volt devices, its outputs must drive no higher than the V_{IH} (max) of the 3.3-volt device when V_{CC} (3.3-volt device) is at a minimum, the V_{CC} (5-volt device) is at its maximum value and the source current of the pin being driven is 0 mA. Additionally, the same device must meet the minimum requirements needed to reliably interface with devices that conform to the TTL level specification. The TTL specification requires that the outputs drive no less than the V_{IH} (min) of the 5-volt TTL device when V_{CC} (5-volt TTL device) is at a minimum and with a load current of 3.2 mA. The ideal specifications are shown in Table 1, below. The specifications are derived from the requirements needed for both 5-volt TTL devices and 3.3-volt CMOS devices. The value for V_{OH} (max) is given for a 5-volt device driving into a 3.3-volt device operating at a minimum V_{CC} (3.0 volts for a 3.3-volt device). In this condition, the determining

1. The information contained in this technical note pertains to the revision B versions of the MACH211SP and MACH231SP. Revision A material for these devices has characteristics similar to those found in the 5-volt M5-128, M5-192, and M5-256 devices. Information about those devices is found in the technical note *Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices*. The revision information is found after the date code on the package (e.g., 9750 XXX **B**)

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Amendment/**0** Issue Date: **November 1998**

factor is set by the V_{IH} (max) requirements of V_{CC} + 0.3 with a V_{CC} of 3.0 volts. All of the devices will meet the specification, set by the need to be 5-volt TTL compatible, for V_{OH} (min) when V_{CC} = Min and I_{OH} = -3.2 mA.

Table 1. 5-Volt Tolerant/3.3-Volt Safe Ideal Specifications

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4		V
V_{OH}	Output High Voltage	V_{CC} = Max, I_{OH} = 0 mA		3.3	V

MACH 1 & 2 SP Mixed Supply Design Characteristics

These devices were not originally designed to meet the ideal specifications given above, and as a result do not meet them. This does not, however, mean these devices cannot be used in a mixed supply design environment because many designs are not designed to minimum and maximum specifications but rather to more typical specifications. When V_{CC} is at 5.25 volts, an output will typically need to source less than 25 µA to provide an output voltage of 3.6 volts. Additionally, many systems will not be designed to operate at both the maximum 5-volt V_{CC} of 5.25 volts and the minimum 3.3-volt V_{CC} of 3.0 volts, but rather will operate at the more typical 5.0 volts and 3.3 volts. The design of the output buffer is such that V_{OH} drops linearly with V_{CC} such that if V_{CC} drops 0.1 volts, so does V_{OH}. As a result, a more typical V_{OH}, when V_{CC} is at 5.0 volts, will be around 3.4 volts. Additionally, the V_{IH} of a device running at 3.3 volts is 3.6 volts, which further ensures that a 5-volt device can drive a 3.3-volt device without causing damage.

The specifications for MACH 1 & 2 SP devices stated that at V_{CC} (min) = 4.75 volts and with a source current of -3.2 mA, V_{OH} will be no greater than 3.3 volts. All of these devices will meet this specification, but this specification does not meet the requirements for being safe to drive a 3.3-volt device. To further ensure that these devices meet a specification which can be considered safe, they are tested to meet a V_{OH} of 3.5 volts when V_{CC} = 5.25 volts and I_{OH} = -300 µA. The MACH 1 & 2 SP test specifications are shown in Table 2.

Table 2. MACH 1 & 2 SP 3.3-Volt Safe V_{OH} Specifications

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4		V
V_{OH}	Output High Voltage	V_{CC} = 5.25 V, I_{OH} = -300 µA		3.5	V

Additional safety can be included as a part of a system design either by using series current limiting resistors or by using bleeder resistors to ground. The series resistor will be placed between the MACH device and the 3.3-volt device and should be no less than 150 Ω which will limit the maximum amount of current which could be driven into a pin and through the ESD structure to less than 10 mA. This current value is almost always considered safe in terms of latch-up specifications that are typically on the order of 200 mA into a pin. If a 12 KΩ resistor to ground is used, it will guarantee that V_{OH} does not go above 3.6 volts when V_{CC} of the MACH device is at 5.25 volts.

CONCLUSION

The MACH 1 & 2 SP devices offer several advanced features that can be invaluable in a system design. To take full advantage of these features, the designer must be fully aware of the characteristics of the features in each of the device types. The mixed supply design capability is a feature that allows for advanced system design using parts from different technologies but requires an understanding of the specifications needed for a 3.3-volt safe design in terms of V_{CC} and V_{OH} levels. In all situations, MACH 1 & 2 SP devices can be used in these designs given the proper design techniques and considerations.

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VF1 FPGA Power Estimation

INTRODUCTION

During the initial stage of system design, the power requirements for the system are considered. To estimate the system power, the power of each active subsystem must be calculated. When the subsystem is a printed circuit board, the power estimation for the subsystem is the sum of the power of each device. To facilitate the process of calculating power, all devices provide graphical or algebraic methods to estimate power. FPGAs are no exception, but they do provide special complexity. FPGAs can implement an indefinite amount of logic designs. Therefore, estimating the power of each design is as unique as the design. In this application brief, a method to estimate the VF1™ FPGA power is presented.

POWER DISSIPATION

The two components to power in semiconductor devices is static and dynamic power. Static power occurs during inactive device periods whereas dynamic power occurs during active device periods. Stated in equation form:

$$P_{TOTAL} = P_{STATIC} + P_{DYNAMIC}$$

Static power is a function of the static leakage current which a device dissipates. During an inactive period, a device connected to supply and ground has biased internal nodes. Parasitic junctions inherent to internal nodes become active during this period drawing leakage current. Hence, static power follows the equation:

$$P_{STATIC} = V_{CC}\, SI_{CC}$$

Conversely, dynamic power is not a function of leakage current; it is a function of dynamic internal and output switching. Dynamic internal and output switching both charge and discharge capacitive loads. Internal switching charges and discharges internal node capacitors whereas output switching charges and discharges external load capacitors. In either case, current is drawn and dissipated. In equation form:

$$P_{DYNAMIC} = P_{INT} + P_{OUT}$$

Note that output nodes can have internal pull-up resistors or latches to maintain known states during output tristate. The internal pull-ups or latches also contribute to the total power consumption and are included in output power. Moreover, the complexity of calculating PINT and POUT require separate sections for the calculation of each.

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INTERNAL POWER DISSIPATION (P_{INT})

The internal power dissipation of a device is a result of charging and discharging of internal nodes. However, the multiple designs which can be implemented into FPGAs have varying quantities of nodes. This variance provides a unique dilemma: how to produce an estimate for internal power? The method which the FPGA industry has adopted is to generate power data from FPGAs saturated with 16-bit counters. The data is used to determine the power factor K_{PWR} which is used in the following internal power equation:

$$P_{INT} = K_{PWR} V_{CC} F_{MAX} N_{CBB} T_{RATE}$$

Where: K_{PWR} = VF1 FPGA Power Constant (A/Hz)

V_{CC} = Supply Voltage (V)

F_{MAX} = Maximum Clock Frequency (Hz)

N_{CBB} = Total Number of VF1 FPGA Configurable Building Blocks Used

T_{RATE} = Average Number of Internal Nodes Toggling at a Given Clock (20% for most designs; 12.5% for 16-Bit Counters)

VF1 FPGA	K_{PWR} (A/Hz)
VF1012	TBD
VF1020	TBD
VF1025	7 E-12
VF1036	TBD

Output Power Dissipation (P_{OUT})

Output power dissipation is a function of capacitive load, supply voltage, output switching frequency, and the quantity of outputs switching at a given time. Stated mathematically:

$$P_{OUT} = \sum_{i=1}^{n} C_i V_i^2 F_i$$

Where: C_i = Output Capacitive Load (F)

V_i = Output Voltage Swing (V)

F_i = Output Switching Frequency (Hz)

n = Total Number of Outputs

The implication of the previous equation is that every output needs to be analyzed to calculate the output power. For a simpler estimation, the following simplifications can be made.

C_i	$\cong C_{avg}$	=	Average Output Load Capacitance (F)
V_i	$= V_o$	=	Output Voltage Swing (V)
F_i	$\cong 1/2\ F_{max}$	=	Average Output Switching Frequency (Hz)
n	$\cong N_{out} * T_{rate}$	=	(Total Number of Outputs) * (Percentage of Outputs Switching at a Given Time)

The simplifications result in the following equation:

$$P_{OUT} = 1/2\ C_{avg}\ V_o^2\ F_{max}\ N_{out}\ T_{rate}$$

EXAMPLE

For an example, consider a 32-bit counter running at 50 MHz and driving a 32-bit bus loaded with 30 pF. The target device is a VF1025. The capacity needed for this design is 32 CBBs and the toggle rate is 6.25%. Using this information, the internal and external power estimates are calculated below.

Internal Power:

$P_{INT} = K_{PWR}\ V_{CC}\ F_{MAX}\ N_{CBB}\ T_{RATE}$

$= (7E\text{-}12\ A/Hz)\ (3.3V)\ (5OE{+}6\ Hz)\ (32)\ (0.0625)$

$= 2.31\ mW$

Output Power:

$P_{OUT} = 1/2\ C_{avg}\ V_o^2\ F_{max}\ N_{out}\ T_{rate}$

$= 1/2\ (30E\text{-}12\ F)\ (3.3V)^2\ (5OE{+}6\ Hz)\ (32)\ (0.0625)$

$= 16.34\ mW$

Total Power:

$P_{TOT} = P_{STATIC} + P_{DYNAMIC}$

$= P_{STATIC} + P_{INT} + P_{OUT}$

$= 0{+}2.31\ mW + 16.34\ mW$

$= 18.65\ mW$

SUMMARY

Power estimation during the initial phase of system design must be calculated to determine whether system power constraints are satisfied. To calculate the system power, each individual device must provide a method to calculate power. For VF1 FPGAs, a method for calculating the total power dissipation has been provided. A designer should use this approach as an approximation. Actual power consumption will ultimately depend on the unique implementation of a design into a VF1 FPGA.

VANTIS

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VF1 FPGA Configuration Guide

INTRODUCTION

Configuration is the process of loading a VF1™ FPGA with a pattern that defines its applications identity. Because the VF1 family uses SRAM configuration memory, configuration must be performed every time the device is powered up. Configuration may also be done at any time that the system designer determines that configuration is needed.

The configuration program is a bitstream generated by Vantis DesignDirect™ place-and-route software. The bitstream is stored in either a host system or in a serial PROM (SPROM). It is downloaded from the host system or SPROM whenever the VF1 FPGA is powered up or whenever the host system initiates the configuration process.

Configuration Overview

Designers have a wide selection of configuration modes that may be used to configure a VF1 FPGA from either a host system or SPROM (Figure 1). If a VCM (Vantis Configuration Memory) SPROM is used, the VF1 FPGA will automatically read its configuration program from the SPROM whenever power is applied. A host system, on the other hand, configures the VF1 FPGA under the control of the host system, and may reconfigure the VF1 FPGA at any time.

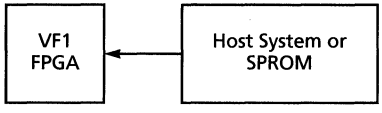

Figure 1. FV1 Device Configuration

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The Vantis VF1 FPGA family supports configuration via the JTAG boundary-scan port as well as via a dedicated configuration port using non-JTAG modes. In this discussion, the non-JTAG modes will be covered first, followed by the JTAG mode.

The basic configuration modes are listed below and are described in detail in a following section.

- **Master serial mode.** In this mode, the Master VF1 FPGA is loaded automatically from a companion SPROM whenever power is applied to the VF1 FPGA or when the PROGRAM pin is pulsed. The VF1 FPGA controls the entire configuration process. Multiple VF1 FPGAs may be configured in this mode with the first device configured as a Master, and subsequent devices configured as Slaves.
- **Slave serial mode.** With the exception of JTAG mode, which is described later, slave mode is used whenever a VF1 FPGA is not controlling the configuration process. Usually, slave-mode devices are the second and subsequent VF1 FPGAs when multiple devices are daisy-chained for

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21552B-0configuration. VF1 FPGAs may also be configured in Slave mode whenever a host system loads the devices serially and controls the configuration process.

- **Asynchronous peripheral mode.** This mode is used to transfer configuration data a byte at a time from a host system to a VF1 FPGA. The VF1 FPGA provides the configuration clock. The host system monitors a status line to determine when another byte of data can be transferred. The first device in a chain is configured in Asynchronous Peripheral mode and subsequent devices are configured in Slave serial mode.
- **Synchronous peripheral mode.** This mode is similar to asynchronous peripheral mode in that a host system transfers a byte of configuration data at a time, but the host system provides configuration clocks. The VF1 FPGA receives the byte of configuration data, serializes is, and stores it in configuration memory. The first device in a chain is configured in Synchronous Peripheral mode and subsequent devices are configured in Slave serial mode.
- **JTAG mode.** JTAG Mode allows a host system to configure VF1 FPGAs via the VF1 JTAG port. When this mode is used, all VF1 FPGAs in a chain are configured in JTAG mode.

Configuration Program

The configuration program is developed using Vantis' DesignDirect software (Figure 2). Designers select the configuration mode that will be used for their applications and the DesignDirect software generates a bitstream in the appropriate format for that specific mode.

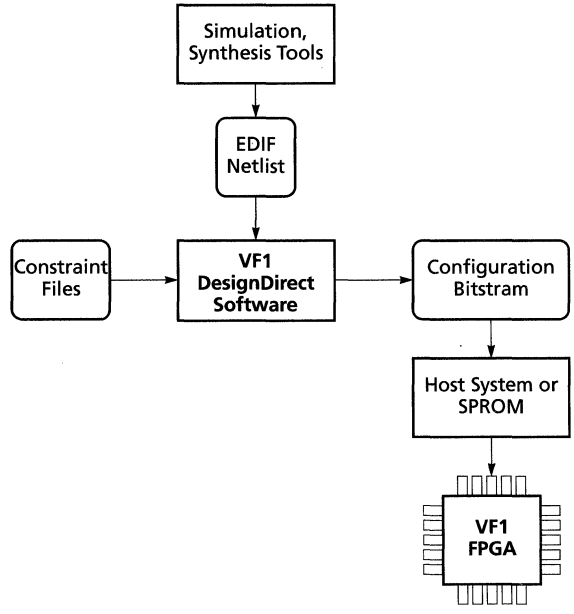

Figure 2. Configuration Program Development

21552B-002

With the exception of some header information, the configuration bitstream is the same regardless of the configuration mode used. The bitstream consists of a header; length count; multiple data frames, each with its own CRC for error detection; and a postamble (Table 1).

Table 1. Bitstream Format

Header	
-Fill bits	11111111
-Preamble	11110010
Length count	Count bits 23:0
Fill bits	11111111
Data frame(s)	Number of frames for each device type: VF1012=430 VF1020=546 VF1025=604 VF1036=720
-Start bit	0
-Data	Configuration data
-CRC bits	Error detection bits
-Stop bits	111
Postamble	11111111

Note:
The total number of bits required to configure a VF1 FPGA depends on the capacity of the device (Table 2).

Table 2. VF1 FPGA Configuration Bits

VF1 FPGA	Configuration Bits
VF1012	245,156
VF1020	385,476
VF1025	474,792
VF1036	669,656

Non-JTAG Overall Timing/Signal Functions

A relatively small number of signals perform the most important configuration functions in non-JTAG configuration modes. Figure 3 is a generic configuration diagram showing the key signals used to interface a VF1 FPGA to either a host system or an SPROM. Other signals take part in various modes (Appendix A, Tables A1 and A2), but the signals shown in Figure 3 and the general timing diagram in Figure 4 are common to all non-JTAG configuration modes:

1. **$\overline{\text{PROGRAM}}$**. A low-to-high transition on the $\overline{\text{PROGRAM}}$ pin starts the configuration sequence.
2. **M[2:0].** Three mode pins select the VF1 configuration mode.
3. **$\overline{\text{INIT}}$**. The $\overline{\text{INIT}}$ signal is pulled low during VF1 initialization prior to configuration, is released during configuration, and is pulled low if a bitstream error occurs during configuration. $\overline{\text{INIT}}$ is an open drain signal that requires a pull-up resistor tied to V_{CC}.
4. **DONE.** The DONE signal goes low during initialization and stays low until the VF1 FPGA is fully configured. DONE is an open drain signal that requires a pull-up resistor tied to V_{CC}.
5. **CCLK.** In Master mode and Asynchronous Peripheral mode, the VF1 FPGA generates its own configuration clock. In these modes, CCLK is an output. In Slave serial mode and Synchronous Peripheral mode, the CCLK configuration clock comes from some other source. In these cases, CCLK is an input.

6. **DIN[7:0].** Configuration data is received on the data in (DIN) pins. In serial configuration modes, all data is received on DIN 0, commonly referred to as DIN. In Synchronous and Asynchronous peripheral modes, data is received in bytes on DIN 0-7.
7. **DOUT.** VF1 FPGAs may be daisy chained for configuration, with all devices configured from a common source. In this case, the lead VF1 FPGA configures itself first and passes subsequent configuration data to the devices that follow via the DOUT pin. The DOUT pin is connected to the DIN pin of the following device.
8. **RDY/$\overline{\text{BUSY}}$.** When the VF1 FPGA is in one of the Peripheral modes, host systems monitor the RDY/$\overline{\text{BUSY}}$ signal to determine when the device is ready to receive another byte of configuration data.
9. **RDY/$\overline{\text{BUSY}}$ (DIN7).** Instead of monitoring the RDY/$\overline{\text{BUSY}}$ pin, a host system can read the RDY/$\overline{\text{BUSY}}$ status by monitoring the DIN7 pin.
10. **HDC, $\overline{\text{LDC}}$.** Two status signals, HDC (high during configuration) and $\overline{\text{LDC}}$ (low during configuration) may be monitored during the configuration process. Once configuration is completed, the status of these pins is defined by the configuration pattern and they become user I/O pins.

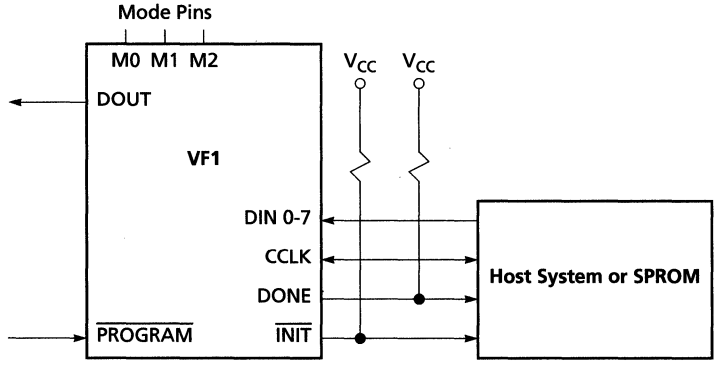

Figure 3. Common Non-JTAG Configuration Signals 21552B-003

Mode Selection

Three multiplexed mode-select pins, M[2:0], determine which mode will be used to configure a VF1 FPGA. Mode signals must be set up before power is applied to the chip and must remain constant until the VF1 FPGA completes the initialization process (while $\overline{\text{INIT}}$ is low). Mode signal setup is usually accomplished by tying the mode pins to the appropriate logic level via pull-up or pull-down resistors. Using resistors rather than tying the signals directly to VCC or GND frees the mode pins for use as I/O pins following the configuration process. Table 3 lists the pin assignments for each mode.

Table 3. Configuration Mode Selection Pins

	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Synchronous Peripheral	0	1	1
Asynchronous Peripheral	1	0	1
JTAG	0	0	1

Initialization

Figure 4 shows the timing relationships that exist between key signals during configuration of a VF1 FPGA, and Table 4 lists specific timing values for each VF1 family member. Initialization begins whenever there is a low-to-high transition on the PROGRAM pin, or when power is applied to the device. When PROGRAM goes low, the VF1 FPGA clears configuration memory and waits for PROGRAM to go high. When PROGRAM goes high, several events occur:

1. The VF1 configuration memory is reset again.
2. The VF1 INIT pin goes low while the device initializes itself for the configuration process.
3. The VF1 examines the mode pins M[2:0] to determine the configuration mode that will be used.
4. The DONE pin goes low, signaling that the VF1 FPGA must be configured. It stays low until the configuration process is completed.
5. The INIT pin goes high when initialization is complete and the VF1 FPGA is ready to receive configuration data.

When the VF1 FPGA is configured from a companion SPROM such as the Vantis Configuration Memory (VCM), the DONE and INIT signals control the operation of the SPROM, as explained in the Master serial mode description that follows. When a host system configures the VF1 FPGA, DONE and INIT provide status information for the host.

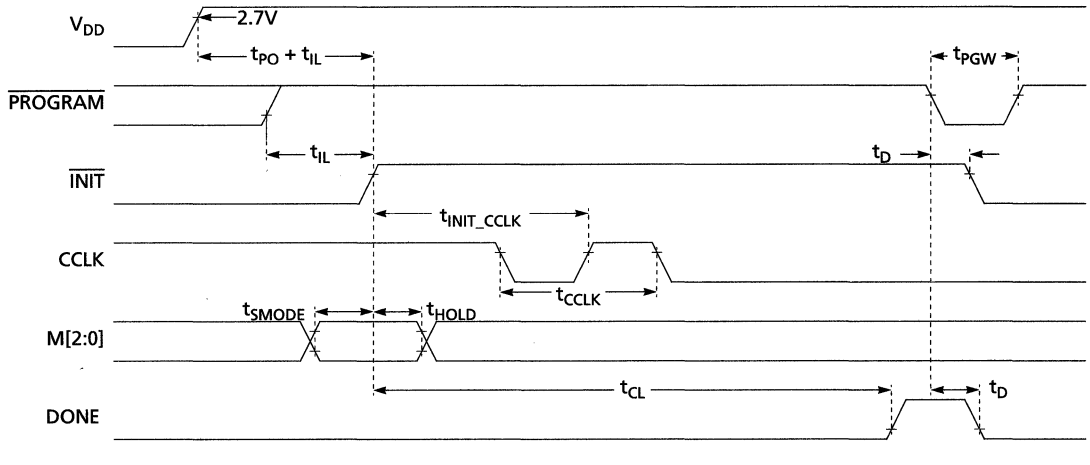

Figure 4. General Configuration Timing Characteristics

Table 4. General Timing Specifications

Parameter	Symbol	Min	Max	Unit
All Configuration Modes				
M[2:0] Setup Time to $\overline{\text{INIT}}$ High	t_{SMODE} (Note 2)	500		ns
M[2:0] Hold Time from $\overline{\text{INIT}}$ High	t_{HMODE}	500		ns
$\overline{\text{PROGRAM}}$ Pulse Width Low to Start Reconfiguration	t_{PGW}	1.5		µs
DONE or $\overline{\text{INIT}}$ Response Time to $\overline{\text{PROGRAM}}$ Pulse	t_D		1.0	µs
$\overline{\text{INIT}}$ Timing				
$\overline{\text{INIT}}$ High to CCLK Delay	t_{INIT_CCLK}			
Slave Serial		1.0		µs
Synchronous Peripheral		1.0		µs
Master Serial		200	900	ns
Initialization Latency	t_{IL}			
12K: Master Serial		165	620	µs
Other Modes		30	110	µs
20K: Master Serial		175	650	µs
Other Modes		35	140	µs
25K: Master Serial		180	665	µs
Other Modes		40	150	µs
36K: Master Serial		185	690	µs
Other Modes		50	180	µs
Power-On Reset Delay	t_{PO}			
Master Serial		35	130	ms
Other Modes		9	33	ms
Configuration Latency	t_{CL}			
12K: Master Serial		15	60	ms
Other Modes		25		ms
20K: Master Serial		25	100	ms
Other Modes		40		ms
25K: Master Serial		30	120	ms
Other Modes		45		ms
36K: Master Serial		45	165	ms
Other Modes		65		ms

Notes:

1. *All timing values are based on 1K pullup and 35 pF loading on open-drain outputs $\overline{\text{INIT}}$ and DONE.*
2. *In the case of Master mode, the minimum setup time is 500 ns to $\overline{\text{INIT}}$ High of Slave mode.*

Configuration Program Transfer

Once it is initialized, the VF1 FPGA reads configuration data from an SPROM or a host system. The following sections describe specific methods used to transfer data.

Table 1 describes the format of the configuration bitstream. A header is read first, followed by a bit count of the configuration program. If two or more VF1 FPGAs are configured in a daisy chain, the bit count includes the total of all configuration programs contained in the bitstream.

The bit count is loaded into a register in the VF1 FPGA. Even before the bit count is loaded, the VF1 FPGA begins counting every clock pulse on the CCLK pin. CCLK clocks may be generated internally in a VF1 FPGA (Master serial and Asynchronous peripheral modes) or may be received from some other source (Slave and Synchronous peripheral modes). Regardless of the source, every clock is counted and the count used to determine when configuration is complete. Since the VF1 FPGA reads one bit of data on each clock pulse, the clock pulse count corresponds to the number of data bits read by the device.

The VF1 FPGA loads configuration data a frame at a time. When the number of bits transferred matches the bit count that was read from the bitstream, the VF1 DONE signal goes high, signaling an end to the configuration process. In addition, either of the two status signals, HDC and $\overline{\text{LDC}}$, may be used to monitor the configuration process to determine when the VF1 FPGA is ready to process meaningful data.

Error Detection

During configuration, a VF1 FPGA checks CRC bits frame-by-frame to detect bitstream errors. If no errors occur, a high on the DONE pin signals the successful completion of the configuration process. If DONE is low, indicating that configuration did not complete successfully, the $\overline{\text{INIT}}$ signal may be sampled to help determine the reason. For example, a high $\overline{\text{INIT}}$ may indicate the VF1 FPGA was under-clocked, while a low $\overline{\text{INIT}}$ points to a bitstream error during configuration.

Configuration does not automatically begin again when an error occurs. The $\overline{\text{PROGRAM}}$ signal must be pulsed low to restart the configuration process.

JTAG Considerations in Non-JTAG Configuration Modes

Vantis VF1 FPGAs support JTAG boundary scan testing (IEEE STD 1149.1, IEEE standard test access port and boundary scan architecture). In addition to specifying industry-standard testing procedures, the IEEE specification gives manufacturers the ability to use JTAG ports for other purposes as well. VF1 FPGAs support both board level and device testing using JTAG, and provide a means for configuring VF1 FPGAs via the JTAG port. JTAG configuration is covered in a subsequent section of this document. This section discusses precautions that must be taken when using JTAG testing and non-JTAG configuration.

JTAG boundary scan instructions can control VF1 FPGA I/Os during JTAG testing. In normal mode (after completion of configuration), this does not create a problem because all JTAG instructions are supported. The problem may arise during non-JTAG mode configuration when DIN, DOUT, CCLK, $\overline{\text{INIT}}$, and DONE are sending out or receiving configuration handshaking signals.

The JTAG instructions INTEST, EXTEST or HI-Z, if executed during non-JTAG configuration, the outputs in the boundary scan register may corrupt the configuration process by overriding the configuration signal. Because of this probable conflict, the INTEST, EXTEST, and HI-Z instructions should not be used during non-JTAG mode configuration.

When the VF1 FPGA first powers up, its JTAG engine is initialized at TEST LOGIC RESET until V_{CC} reaches 2.7V and the VF1 internal power-up reset signal is released. This prevents the execution of any JTAG instructions. All the I/Os that are not used for configuration come up in 3-state mode with pull-ups. The boundary scan registers do not control the I/Os at this time.

After the power-up reset delay runs out, the VF1 begins its initialization in preparation for configuration. At this point, it is possible to start running BYPASS and instructions other than INTEST, EXTEST, and HI-Z.

When using non-JTAG configuration and JTAG boundary scan testing, you can handle potential conflicts in one of two ways:

1. Delay boundary scan testing until VF1 configuration is complete. The advantage of this approach is that all JTAG instructions for testing the VF1 FPGA are supported. The disadvantage is that the configuration process uses some board interconnections (those that interface the VF1 FPGA to its configuration source) before they are tested.
2. Use boundary scan to test board-level connections before configuring the VF1 FPGA, and use other JTAG tests following configuration. This approach allows board-level connections to be verified prior to configuration and chip functionality to be tested following configuration. However, it is a little more complex to implement than the first alternative.

Delay Boundary-Scan Testing

Delaying boundary-scan testing until VF1 configuration is complete is simple: monitor the VF1 DONE pin to ensure that configuration is complete before initiating any testing. The testing can begin as soon as the DONE pin goes high.

Be careful during boundary scan testing to ensure that testing does not re-trigger the configuration process. If the test process loads a "0" on the VF1 PROGRAM pin, a low-to-high transition will occur on the pin when testing is complete and the pin is allowed to go high again, thus initializing the VF1 and triggering a new configuration cycle. To avoid this problem, load a "1" on the PROGRAM pin to ensure that the signal remains high during boundary scan testing. Safe state information for the PROGRAM pin is included in the BSDL files for the VF1 FPGAs.

Boundary Scan Testing Before Configuration

Executing the JTAG boundary scan instructions prior to configuration allows board traces to be verified before they are used in the configuration process. To do boundary scan testing before configuration, follow these steps:

1. Hold the VF1 PROGRAM pin low after power-up, thereby holding the VF1 in the WAIT state and delaying initialization.
2. Perform boundary scan testing. After boundary scan testing is completed, set the JTAG engine to TEST LOGIC RESET. At this point, the boundary scan registers no longer control the I/Os. All the I/O's not used for configuration go into 3-state mode again, just as they were before the boundary scan test.
3. Toggle the PROGRAM pin to high to start initialization and configuration.
4. Once the VF1 FPGA is configured, additional JTAG tests may be conducted, provided care is taken to ensure that the PROGRAM pin is held high throughout the testing process.

Master Serial Mode

Master serial mode is most often used to configure VF1 FPGAs automatically on power up (Figure 5). Figure 6 and Table 5 show timing information. In this mode, the VF1 FPGA is connected to a VCM SPROM. On power up, or on command from a host system, the VF1 FPGA reads its configuration program from the VCM SPROM.

Note:

1. The VCM SPROM RESET polarity must be programmed for OE high and $\overline{\text{RESET}}$ low.

A simple four-wire interface connects the VF1 FPGA with the VCM SPROM:

- The VF1 DIN pin connects with the VCM SDATA (Serial data) pin.
- The VF1 CCLK pin connects with the VCM SCLK (Serial clock) pin.
- The VF1 DONE pin connects with the VCM $\overline{\text{CS}}$ (Chip select) pin.
- The VF1 $\overline{\text{INIT}}$ pin connects with the VCM OE (Output enable) $\overline{\text{RESET}}$ (Reset) pin.

If the $\overline{\text{PROGRAM}}$ pin is tied to V_{CC}, configuration starts automatically on power up. If $\overline{\text{PROGRAM}}$ is not tied to V_{CC}, the host system must cause a low-to-high transition on the $\overline{\text{PROGRAM}}$ pin to initiate the configuration process as described earlier.

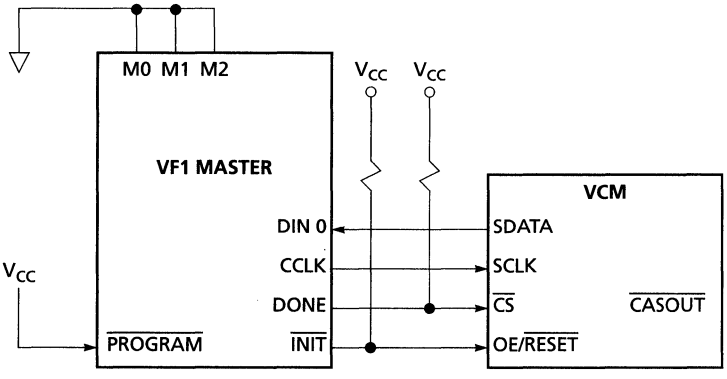

Figure 5. Master Serial Mode

21552B-005

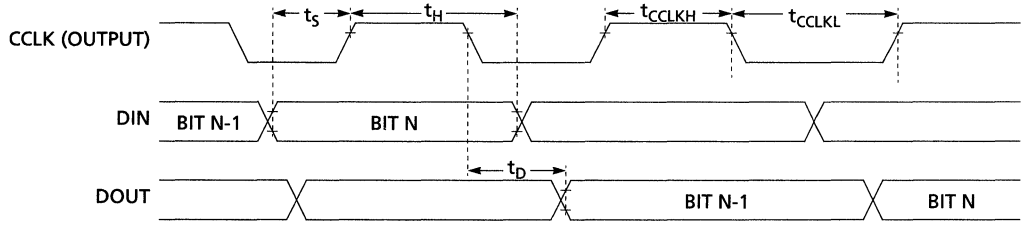

Figure 6. Master Serial Mode Timing Relationships

21552B-006

Table 5. Master Serial Mode Timing Values

Master Serial Mode	Symbol	Min	Max	Unit
DIN Setup Time	t_S	20		ns
DIN Hold Time	t_H	0		ns
CCLK High Time	t_{CCLKH}	33.5	100	ns
CCLK Low Time	t_{CCLKL}	33.5	100	ns
CCLK Period	t_{CCLK}	67	200	ns
CCLK Frequency	f_C	5	15	MHz
CCLK to DOUT	t_D		30	ns

When the $\overline{INIT}$ pin goes high, the transfer of the configuration bitstream from the VCM SPROM to the VF1 FPGA begins. A low on the VCM $\overline{CS}$ and a high on its OE/$\overline{RESET}$ pins cause the VCM to place the first bit of the configuration bitstream on its SDATA pin. The VF1 FPGA reads this bit on the rising edge of the first CCLK clock pulse. The same CCLK pulse signals the VCM to increment its internal address counter and place the second bit on the SDATA pin. This process continues until the configuration process is completed or is interrupted.

Slave Serial Mode

The primary difference between Master mode and Slave mode is the CCLK signal. CCLK is an input for VF1 FPGAs in Slave mode while it is an output in Master mode. Slave serial mode is used to configure VF1 FPGAs in daisy chains that are headed by Master devices (Figure 7), or when directly configured in serial mode by a host system (Figure 9). They may also follow Asynchronous Peripheral Mode devices (Figure 12) or Synchronous Peripheral Mode devices (Figure 10) in daisy chains. Figure 8 and Table 6 show Slave mode timing.

The Master-driven Slave serial mode is covered first, followed by Host-driven Slave serial mode. Other uses are covered in subsequent sections.

Master-Driven Slave Serial Mode

Figure 7 shows three VF1 FPGAs reading their configuration data from two SPROMs. The first VF1 FPGA in the chain is configured in Master mode while the second and third devices are configured in Slave mode.

The overall function of Master-driven slave serial mode is straightforward. The Master device reads the configuration bitstream from the SPROMs and configures itself. Once it is configured, it puts overflow configuration data on its DOUT pin where it is read by the first Slave VF1 FPGA. The first Slave device configures itself, and then puts overflow configuration data on its DOUT pin where it is read by the second Slave device. This process continues until the Master and all Slave devices in a chain have been configured. The following paragraphs describe the process in more detail.

Note:
Two SPROMs are shown in Figure 7. A single VCM (Vantis Configuration Memory) SPROM with a 1 Mbit memory capacity can hold the configuration programs for two VF1025 or VF1020 devices, four VF1012 devices, or one VF1036 device, as explained in the Vantis Configuration Memory data sheet. When the configuration program exceeds the capacity of one VCM SPROM, two or more may be cascaded to provide the necessary storage capacity. Refer to the Vantis Configuration Memory Data Sheet for details on how to cascade VCM SPROM devices.

The interface between the Master VF1 FPGA and the SPROMs is identical to that described in Master serial mode, above. The Master VF1 controls the configuration process by controlling the CCLK configuration clock

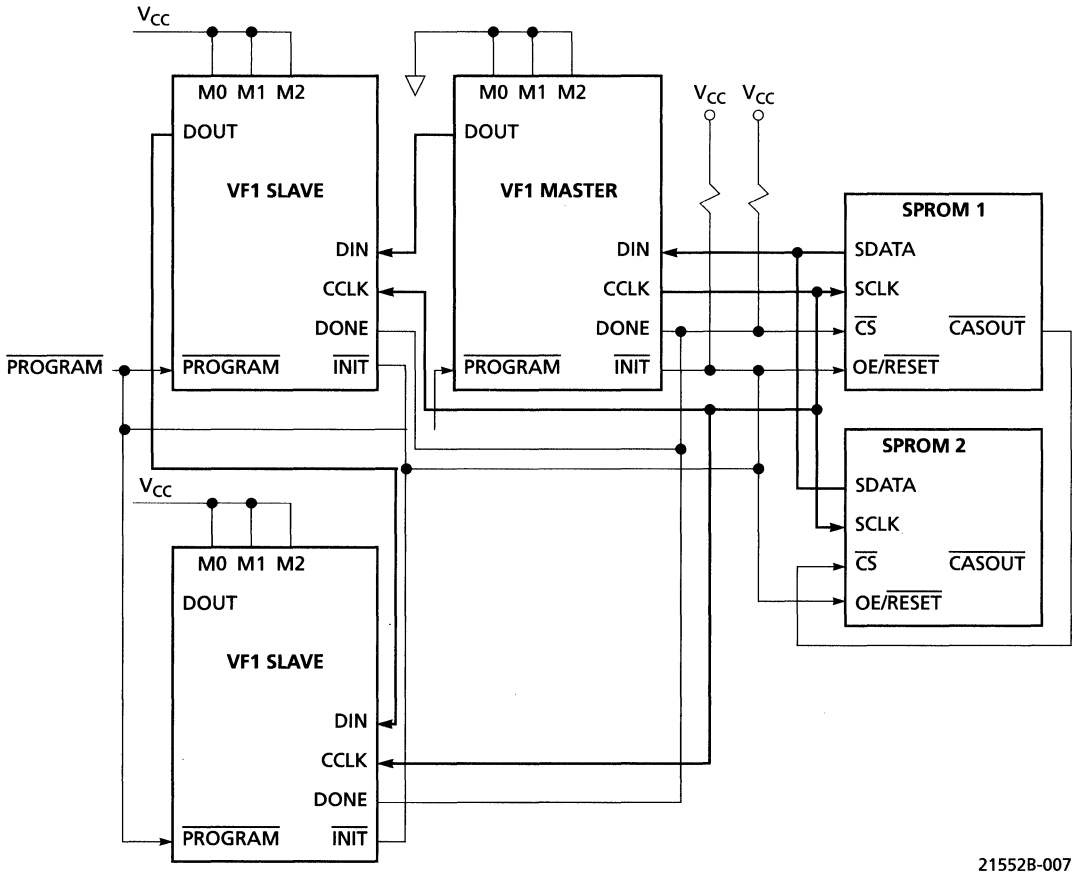

Figure 7. Slave Serial Mode, Master-Driven

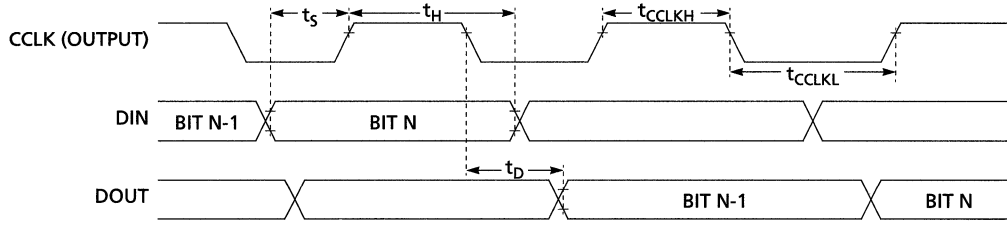

Figure 8. Slave Serial Mode Timing Relationships

21552B-008

Table 6. Slave Serial Mode Timing Values

Slave Serial Mode	Symbol	Min	Max	Unit
DIN Setup Time	t_S	20		ns
DIN Hold Time	t_H	0		ns
CCLK High Time	t_{CCLKH}	50		ns
CCLK Low Time	t_{CCLKL}	50		ns
CCLK Period	t_{CCLK}	100		ns
CCLK Frequency	f_C		10.0	MHz
CCLK to DOUT	t_D		30	ns

The DONE and $\overline{\text{INIT}}$ signals of all three devices are tied together to ensure that the configuration process does not begin until all VF1 FPGAs have completed the initialization process. The $\overline{\text{INIT}}$ signal is applied to the OE/$\overline{\text{RESET}}$ input of both SPROMs, while the DONE signal is applied to the $\overline{\text{CS}}$ input of the first SPROM only. The first SPROM's $\overline{\text{CASOUT}}$ (Cascade out) signal is applied to the $\overline{\text{CS}}$ input of the second SPROM.

The CCLK clock output from the Master VF1 is applied to the SCLK inputs of both SPROMs and to the CCLK pins of the Slave VF1 FPGAs.

The SDATA outputs of both SPROMs are tied together to provide a common DIN data input to the Master VF1 FPGA. The DOUT output pin of the Master device is applied to the DIN of the first Slave device, and the DOUT output of the first Slave is applied to the DIN input of the second Slave device. The same connections are used for any subsequent Slave devices in the chain.

When the $\overline{\text{INIT}}$ signal goes high, configuration proceeds as described in Master serial mode, with the following additions and exceptions:

1. The bit count that the Master device reads early in the configuration cycle is a count of the complete bitstream, including the configuration programs for all VF1 FPGAs in the chain.
2. All VF1 FPGAs receive every CCLK clock pulse and begin counting pulses with the first pulse received. The pulse count, therefore, will be the same in each VF1 FPGA throughout the configuration cycle.
3. The Master VF1 FPGA reads the header bytes and configuration bit count from the SPROMs, stores the bit count, and passes the information on to the first Slave VF1 FPGA via the Master's DOUT pin. The header and bit count are delayed by 1.5 clock cycles as they pass through the Master VF1 FPGA.
4. Once the header and bit count have been transmitted, the Master VF1's DOUT pin goes high and remains high until it is ready to transmit configuration data to the first Slave VF1 FPGA.
5. The first Slave VF1 FPGA reads the header bytes and bit count, stores the bit count in its internal counter, and passes the same header and bit count on to the next Slave VF1 FPGA. The Header and bit count are delayed by an additional 0.5 clock cycle as they pass through the first Slave VF1 FPGA. Once the header and bit count have been transmitted, the first Slave VF1's DOUT pin goes high and remains high until it is ready to transmit configuration data to the second Slave VF1 FPGA.
6. The second and subsequent Slave VF1 FPGAs read the header and bit count and store the bit count in their internal counters.
7. Following receipt of the header and bit count, the Master device receives configuration frames from the SPROM, performs a CRC check on each frame, and uses these frames to configure itself.
8. Once the Master VF1 is fully configured, it sends subsequent configuration frames to the first Slave device via the Master's DOUT pin. The start bit of the first configuration frame that the Slave device sees causes the Slave device to receive the frame, perform CRC checks, and use the frame data to configure itself. The Slave device continues to receive and store frames until it is fully configured.
9. When a Slave device is fully configured, it sends subsequent configuration data to down-stream Slave devices via its DOUT pin. This process continues until all Slave devices have been configured.

When the final Slave device is fully configured, the bit counter in each VF1 FPGA should match the bit count that was received from the SPROM early in the bitstream. When the counts match, all VF1 FPGAs will allow their DONE outputs to go high, thus signaling the end of the configuration process and removing the $\overline{\text{CS}}$ signal from the SPROMs. At the same time, the VF1 FPGA I/O pins are enabled and the FPGA begins to perform the functions that are defined by the configuration bitstream.

Error Detection

Each VF1 FPGA checks incoming configuration frames for errors as it receives them. If any VF1 FPGA detects a bitstream error, it pulls its $\overline{\text{INIT}}$ signal low, terminating the configuration process. Just as in Master serial mode, a pulse on the $\overline{\text{PROGRAM}}$ pins of all devices restarts the configuration process.

Host-Driven Slave Serial Mode

A system designer can eliminate configuration SPROMs from a system by loading VF1 FPGAs from a host system (Figure 9). Configuring VF1 FPGAs from a host system allows the host to precisely control the configuration process, and to reconfigure the VF1 FPGAs in the system at any time.

The configuration diagram shown in Figure 9 is similar to the Master-driven slave serial mode described above, with these differences:

1. The SPROMs are replaced by a host system.
2. All VF1 FPGAs are configured in Slave mode, with no Master mode device in the chain.
3. The host system provides the configuration clock for all VF1 FPGAs in the chain.
4. The host system controls the $\overline{\text{PROGRAM}}$ signal.

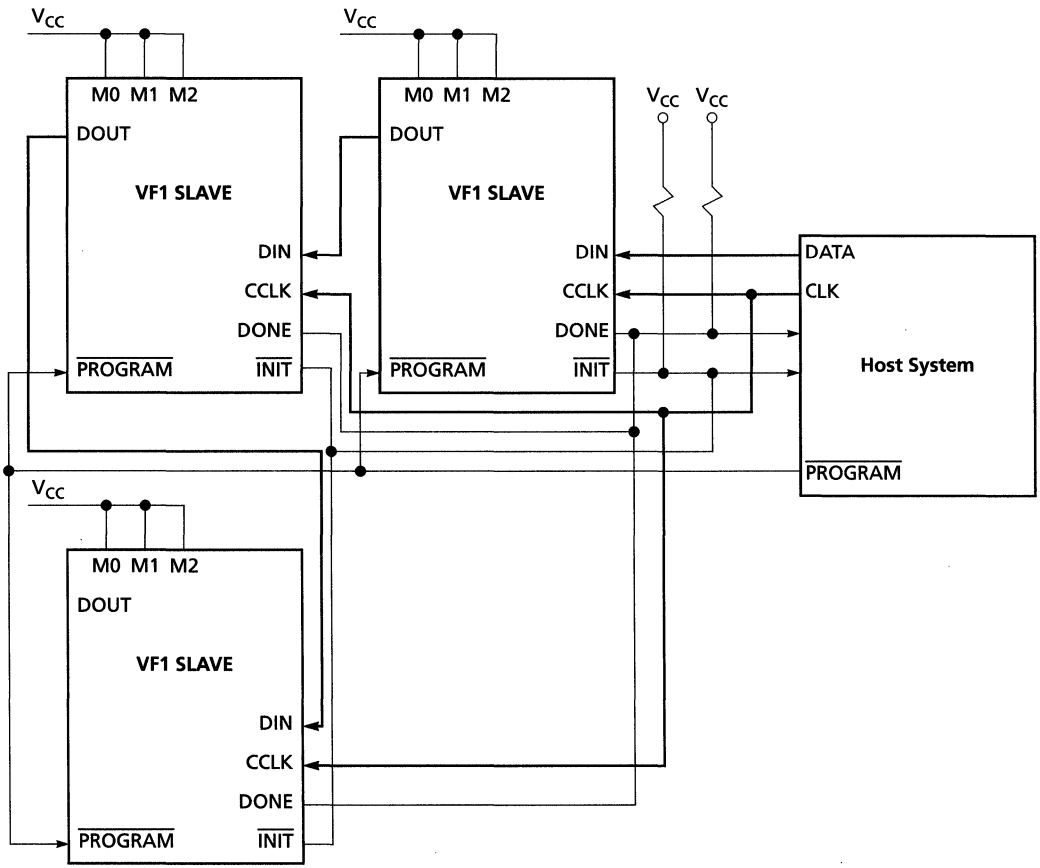

Figure 9. Slave Serial Mode, Host-Driven

21552B-009

The configuration process is similar to the Master-driven Slave serial mode with these exceptions:

1. The host system initiates configuration by the by pulsing the $\overline{\text{PROGRAM}}$ signal low. Even on power up, the VF1 FPGAs waits for the host system to initiate configuration.
2. The VF1 DONE and $\overline{\text{INIT}}$ signals provide status information to the host system. Host systems may also monitor the VF1 HDC (High during configuration) and $\overline{\text{LDC}}$ (Low during configuration) status signals during the configuration process, but the states of HDC and $\overline{\text{LDC}}$ are undefined following configuration.

Byte-Wide Data Transfers

Two configuration modes, Synchronous Peripheral mode and Asynchronous Peripheral mode, support byte-wide data transfers between a host system and VF1 FPGA.

When a VF1 FPGA receives a byte of configuration data, it serializes the byte and processes it as if it were received serially. Byte-wide transfers, therefore, offer another design alternative but not a means of speeding up the configuration process.

Synchronous Peripheral Mode

In Synchronous Peripheral mode, the host system sends byte-wide configuration data and the configuration clock (CCLK) to the VF1 FPGA. The VF1 FPGA receives the byte-wide data on its DIN 0-7 pins. If there are two or more VF1 FPGAs in a daisy chain, the first is configured in Synchronous Peripheral mode and all subsequent devices in Slave mode (Figure 10). Figure 11 and Table 7 show timing information.

Configuration proceeds as follows:

1. The host system initiates the configuration process by pulsing the VF1 $\overline{\text{PROGRAM}}$ pin low.
2. The first data byte is clocked into the VF1 FPGA on the rising edge of the second CCLK pulse after $\overline{\text{INIT}}$ goes high (Figure 11). Bytes are then clocked in on every eighth CCLK pulse.
3. The VF1 RDY/$\overline{\text{BUSY}}$ signal acknowledges the loading of the byte by going high for one CCLK period on the same clock that loaded the byte.
4. To complete the shifting of the last byte into configuration memory, the host system must continue providing CCLK pulses after the last byte is loaded. One way to do this is to continue providing CCLK pulses until the DONE pin goes high.
5. In daisy-chain configurations, the first VF1 FPGA in the chain loads itself and then presents serial data on its DOUT pin. The data appears on DOUT 1.5 CCLK cycles after it is loaded in parallel, which means that DOUT changes on a falling CCLK edge and the next VF1 FPGA loads data on the next rising edge.

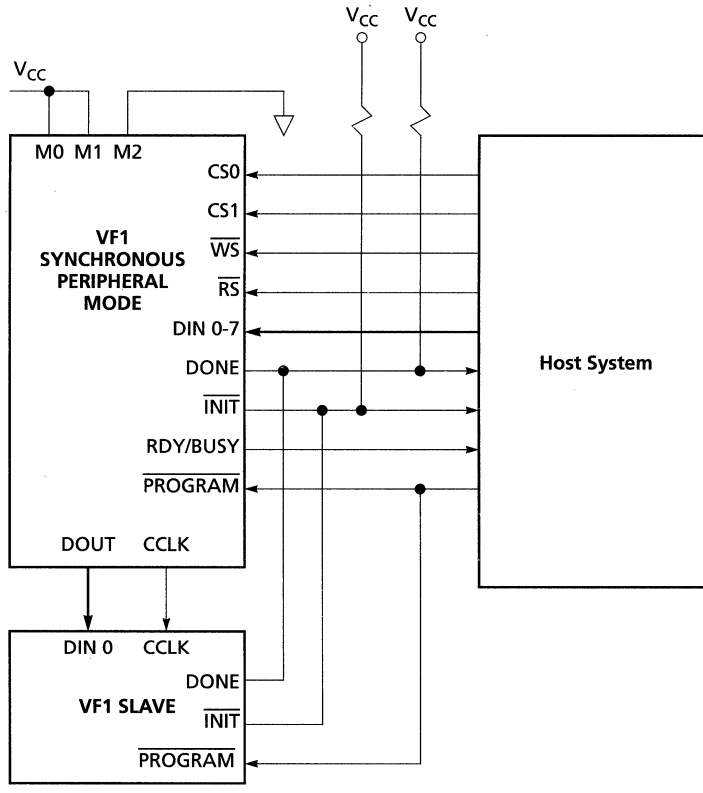

Figure 10. Synchronous Peripheral Mode

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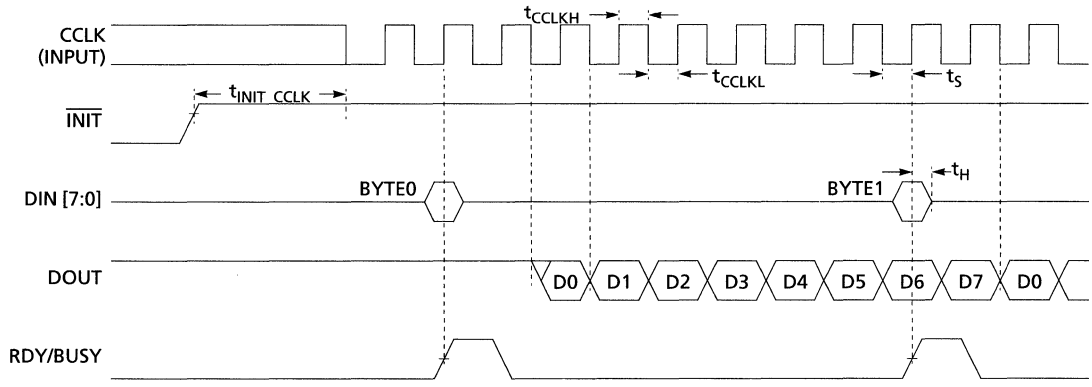

Figure 11. Synchronous Peripheral Mode Timing Relationships

21552B-011

Table 7. Synchronous Peripheral Mode Timing Values

Synchronous Peripheral Mode (Figure D)	Symbol	Min	Max	Unit
DIN Setup Time	t_S	20		ns
DIN Hold Time	t_H	0		ns
CCLK High Time	t_{CCLKH}	50		ns
CCLK Low Time	t_{CCLKL}	50		ns
CCLK Period	t_{CCLK}	100		ns
CCLK Frequency	f_C		10.0	MHz
CCLK to DOUT	t_D		30	ns

Asynchronous Peripheral Mode

In Asynchronous peripheral mode, a host system sends a byte of configuration data to a VF1 FPGA, or to the lead VF1 FPGA in a daisy chain (Figure 12). The VF1 FPGA receives the byte and generates its own clock to serialize the configuration data. The VF1 RDY/$\overline{\text{BUSY}}$ signal provides handshaking between the host system and the VF1 FPGA.

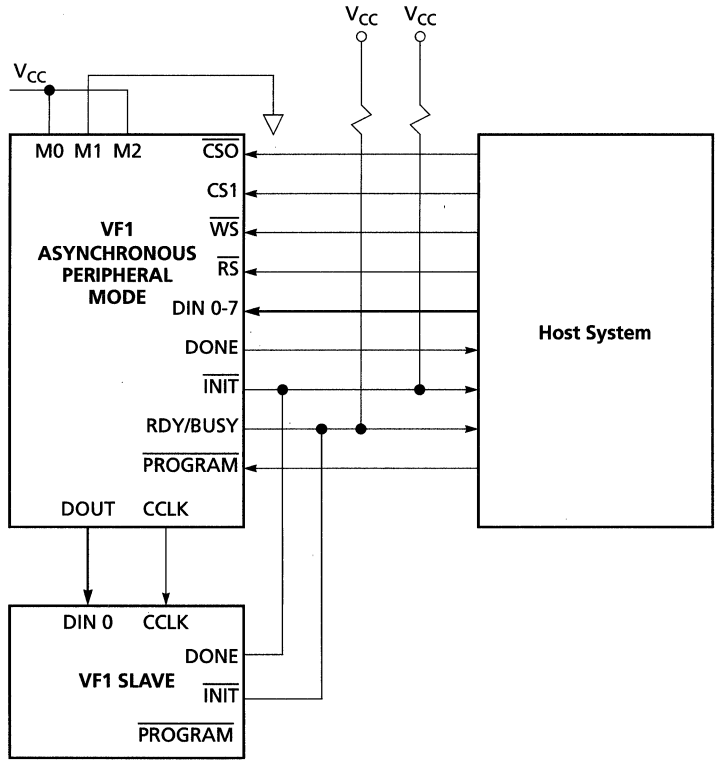

Figure 12. Asynchronous Peripheral Mode

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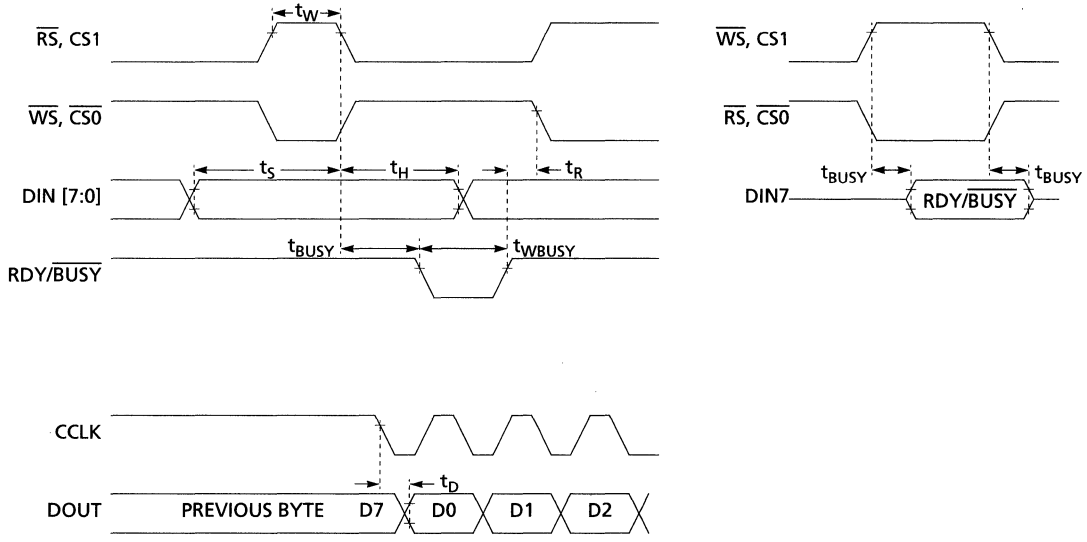

Figure 13. Asynchronous Peripheral Mode Timing Relationships

21552B-013

Table 8. Asynchronous Peripheral Mode Timing Values

Asynchronous Peripheral Mode	Symbol	Min	Max	Unit
RS WS CS0 CS1 Pulse Width	t_W	100		ns
DIN[7:0] Setup Time	t_S	20		ns
DIN[7:0] Hold Time	t_H	0		ns
RDY/BUSY Delay	t_{BUSY}		30	ns
RDY/BUSY Low	t_{WBUSY}	2	9	CCLK Periods
Earliest WR After End of Busy	t_R	0		ns
CCLK to DOUT	t_D		30	ns

Four signals control the writing of byte-wide data into the lead VF1 FPGA: WS (write select), CS0 (chip select 0), RS (read select), and CS1 (chip select 1). As stated earlier, RDY/BUSY provides handshaking. Figure 12 shows signal connections while Figure 13 and Table 8 show timing relationships:

1. As in all other non-JTAG modes, configuration is initiated by pulsing the VF1 FPGA(s) PROGRAM signal low. The VF1 DONE and INIT signals provide initialization and configuration status information to the host system.
2. When the VF1 FPGA is ready to receive a data byte, its RDY/BUSY signal goes high.
3. The host system places the data byte on the VF1 DIN 0-7 pins, usually via a microprocessor bus. The host selects the VF1 FPGA by setting CS0 low, CS1 high, and RS high. The host then pulses

$\overline{WS}$ low. The VF1 reads the data byte on the rising edge of the $\overline{WS}$ pulse. The VF1 uses both a holding register and a shift register for data bytes. A byte is received in the holding register and transferred to the shift register when the shift register is empty.

4. When the VF1 reads the byte, the RDY/$\overline{BUSY}$ signal goes low. The VF1 FPGA transfers the byte from the holding register where it was received into a shift register where the byte is serialized for VF1 configuration.
5. The RDY/$\overline{BUSY}$ signal goes high again when the VF1 is ready to receive another byte. If the shift register is empty when the holding register is loaded, the byte is transferred on the next clock and the RDY/$\overline{BUSY}$ signal goes high immediately. If the shift register is not empty, the RDY/$\overline{BUSY}$ signal stays low until the shift register is empty and the byte waiting in the holding register is transferred.

The designer can eliminate one status line by monitoring the RDY/$\overline{BUSY}$ signal on the microprocessor bus rather than at the RDY/$\overline{BUSY}$ output on the VF1 FPGA. Enabling the chip selects ($\overline{CS0}$ low and CS1 high), and selecting read mode ($\overline{WS}$ high and $\overline{RS}$ low) places the RDY/$\overline{BUSY}$ status on the VF1 DIN7 pin.

JTAG Mode

In JTAG mode, VF1 FPGAs are configured via the JTAG pins TCLK, TMS, TDI, and TDO (Figure 14). Figure 15 and Table 9 show timing information. Three instructions in addition to the standard JTAG instructions support JTAG the configuration mode:

- PROG_MODE. This instruction places the VF1 FPGA in programming mode. Scan cells control the VF1 I/Os during this instruction.
- PROGRAM. Once the VF1 FPGA is in programming mode, the PROGRAM instruction shifts configuration data into the VF1 FPGA. Scan cells control VF1 I/Os.
- VERIFY. After configuration this instruction is used to read back all configuration, VGB and I/O flip-flops, and embedded SRAM bits in the device.

A host system such as a microprocessor controls the configuration of the VF1 FPGA or devices and supplies configuration data. The host also provides the configuration clock TCLK.

If two or more VF1 FPGAs are to be configured, they are arranged in a daisy chain. Data is applied to the TDI pin of the first device and the TDO pin of that device is connected to the TDI pin of the next device. The TMS and TCLK signals from the host are applied to all VF1 FPGAs in parallel.

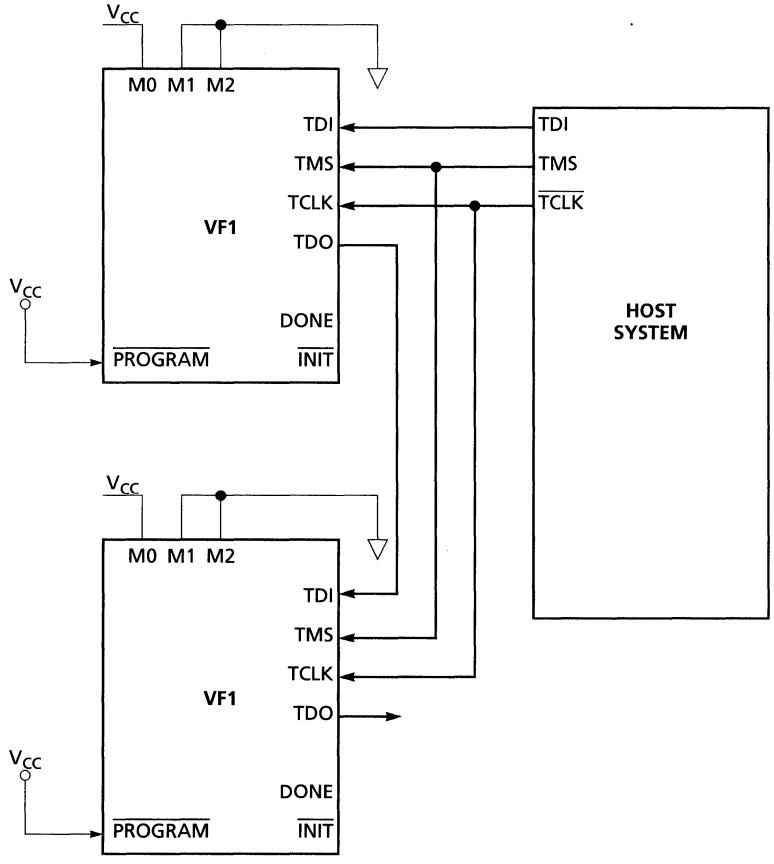

Figure 14. JTAG Mode

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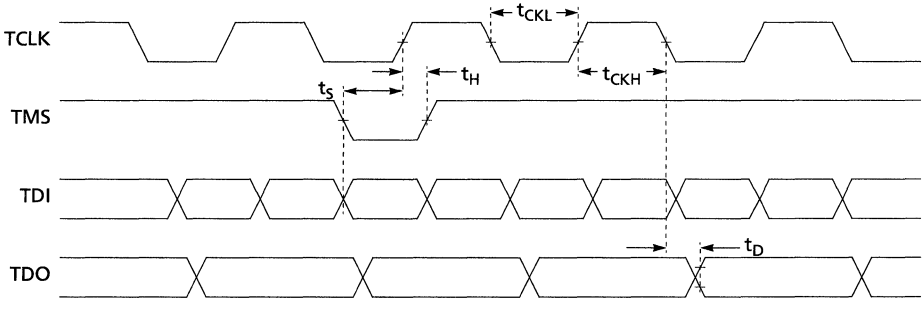

Figure 15. JTAG Mode Timing Relationships

21552B-015

Table 9. JTAG Mode Timing Values

JTAG Mode	Symbol	Min	Max	Unit
TDI/TMS to TCK Setup Time	t_S	40		ns
TDI/TMS Hold Time from TCK	t_H	40		ns
TCK Low Time	t_{CKL}	50		ns
TCK High Time	t_{CKH}	50		ns
TCK to TDO Delay	t_D		30	ns
TCK Frequency	t_{CKF}		10.0	MHz

DONE and $\overline{INIT}$

During non-JTAG configuration the $\overline{INIT}$ pin is an open-drain status pin that can be used to delay the start of configuration when it is driven low. In JTAG mode, however, this pin may be driven low or HIZ by the boundary scan register when executing PROG_MODE or PROGRAM instructions and override the non-JTAG functions of the pin.

To avoid having the boundary scan settings interfere with configuration, driving the $\overline{INIT}$ pin low in JTAG mode has no effect on holding off configuration. Therefore, the rules for using DONE and $\overline{INIT}$ when configuring two or more VF1 FPGAs are different in JTAG mode than in non-JTAG modes:

- Tying $\overline{INIT}$ pins together during JTAG configuration mode is not allowed.
- Tying DONE pins together in JTAG configuration mode is not allowed.

Configuration

The JTAG state machine automatically goes to TEST LOGIC RESET upon power up. Execution of JTAG configuration instructions can start after a time delay of $t_{PO}+t_{IL}$ (see Figure 4) when V_{CC} reaches 2.7 volts. This time delay period guarantees that the configuration memory is initialized. JTAG configuration uses the following instruction flow and pin settings:

1. Settings during power-on reset are $\overline{PROGRAM}$ = High. M0=1, M1=0, M2=0. VF1 I/O pins will come up in 3-state mode except $\overline{INIT}$ and DONE.
2. After V_{CC}=2.7 volts, wait until Tpo+Til time limit has passed.
3. Apply SAMPLE/PRELOAD instruction to load the UPDATE registers in the boundary scan cells.
4. Apply PROG_MODE instruction. At this point, VF1 I/O pins, including $\overline{INIT}$ and DONE, are controlled by boundary scan cells.
5. Apply PROGRAM instruction. At this point, VF1 I/O pins, including $\overline{INIT}$ and DONE, are controlled by boundary scan cells.
6. Go to RUN TEST IDLE. Wait 1 msec.
7. Shift in configuration data by applying TCLK clocks. The total number of t_{CLKs} = Total number of bits in the bitstream. Following the shifting in of all configuration data, VF1 cells will be in the modes defined by the configuration program.
8. Exit PROGRAM instruction and go to TEST LOGIC RESET.
9. When the first VF1 FPGA is configured, put it in BYPASS. If a second VF1 FPGA is to be configured, put any intermediate system devices in BYPASS and configure the second VF1 FPGA.

Put the second VF1 FPGA in BYPASS. Continue this process until all VF1 FPGAs have been configured.

10. The DONE pin may optionally be sampled to confirm successful configuration. If DONE is high, configuration was successful. If DONE is low, an error occurred or the device was not completely configured. Configuration must be repeated.

Vantis Programming Software

Vantis offers VantisPRO™ programming software that provides for the configuration, reconfiguration and readback of VF1 FPGAs using the JTAG mode. Given the configuration of the JTAG chain the VF1 FPGA is in, and the name of the bitstream file, the software can configure the VF1 FPGA through the parallel port on a personal computer. Additionally, the software can also be used to generate the files necessary to configure the VF1 FPGAs using automated test equipment such as full-scale board test systems or JTAG test equipment. VantisPro can generate configuration files for the HP3070, Teradyne test systems and Genrad test systems. Also, it generates the Serial Vector Format (SVF) files commonly used by JTAG test equipment software. The SVF files contain a simple instruction set that tells the hardware the state the JTAG state machine should be in and the data that should be shifted into or out of the part(s).

Vantis also offers a version of VantisPRO software that can be used by an embedded microprocessor to configure the devices in the JTAG mode. This software uses a compressed form of the SVF file generated by VantisPRO software to configure or readback a device. Information about VantisPRO software can be found in the separate document entitled, *MACH ISP Manual.*

Readback

The VF1 readback capability allows designers to read the configuration program back from the VF1 FPGA and compare it with the program that was written into the device. During configuration, a VF1 FPGA is set for one of three possible readback options:

- **Read Disable** (the default state). No readbacks are allowed.
- **Read Once.** One readback is allowed, then readbacks are disabled.
- **Read on Command**. Unlimited readbacks are allowed.

The readback selection is made when the DesignDirect software prepares the configuration pattern. During design development, the Read on Command option is normally used. In production systems, the Read Once option may be used if a host system will verify configuration, or the Read Disable option may be used if the VF1 configuration error detection logic is deemed adequate for reliable operation.

Readback Data

During readback, configuration data is read along with the data in the VF1 internal registers so that the Readback bitstream is not identical to the original bitstream in those particular locations reserved for the registers' internal nodes. In addition, the fill bits, preamble, length counter, and postamble are not read. DesignDirect software provides a mask that allows the readback data to be compared with the original bitstream, or to allow the content of internal registers to be separated from the configuration bitstream for analysis.

The VF1 family provides two readback methods:

- **JTAG readback.** Configuration data is read via the JTAG port using JTAG commands (Figure 14). This method is available following either JTAG or non-JTAG configuration. JTAG readback can be accomplished using the Vantis programming software described earlier.
- **Non-JTAG readback.** Configuration data is enabled with the RTRIG pin and read from the RDO pin (Figure 16. Figure 17 and Table 10 show readback timing information. This readback method is enabled only after non-JTAG configuration.

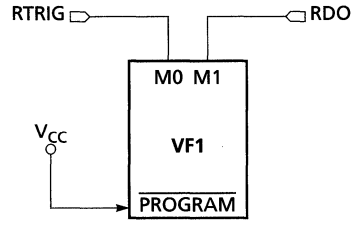

Figure 16. Non-JTAG

21552B-016

Non-JTAG Readback

Non-JTAG readback is enabled following any non-JTAG configuration modes (Master Serial, Slave Serial, Asynchronous Peripheral, and Synchronous Peripheral), provided one of a readback option was selected when the configuration bitstream was generated.

- Apply a low-to-high edge on RTRIG pin and hold RTRIG high.
- Apply four dummy clocks to the CCLK pin.
- Subsequent CCLKs clock out configuration data on RDO. The number of clocks required is: 4 dummy CCLKs + [1 CCLK + Total # of bits in a Frame + 3 CCLKs] times the number of Frames.
- Non-JTAG Readback can be halted by setting RTRIG pin low and after three positive CCLK edges.
- Start bits and stop bits are read as "Don't cares."

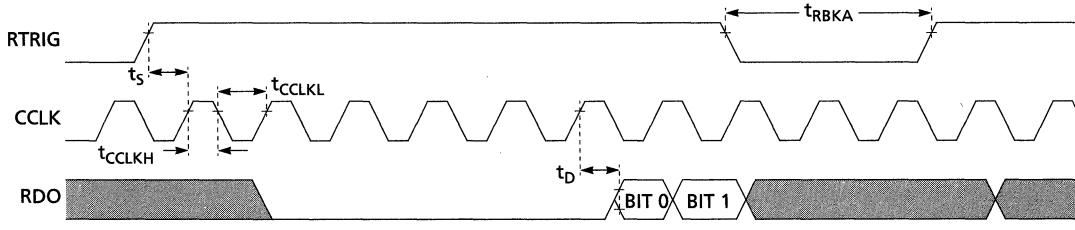

Figure 17. Non-JTAG Mode Readback Timing Values

21552B-017

Table 10. Non-JTAG Readback Timing Values

Readback	Symbol	Min	Max	Unit
RTRIG to CCLK Setup Time	t_S	40		ns
RTRIG Low Width to Abort Readback	t_{RBKA}	3		CCLK
CCLK Low Time	t_{CCLKL}	50		ns
CCLK High Time	t_{CCLKH}	50		ns
CCLK Frequency	f_C		10.0	MHz
CCLK to RDO Delay	t_D		30	ns

APPENDIX A

Configuration Signals

Table 11 describes the functions of all configuration signals. Table 12 summarizes the signals used in each configuration mode. The individual mode descriptions that follow describe how the signals are used in each mode.

Table 11. Configuration Signal Descriptions

M0/RTRIG **M1/RDO** **M2**	**Three multiplexed I/O pins that select the configuration mode.** During configuration, these pins are input pins and are sampled right after initialization to determine the configuration mode. Once configuration is complete, M0 and M1 can be used as RTRIG (Read trigger) and RDO (Read data out) for non-JTAG read-back.
$\overline{\text{PROGRAM}}$	**A dedicated input pin that initiates configuration.** A low level clears the configuration memory and puts the VF1 FPGA into a WAIT state. The MODE pins are sampled. A low-to-high transition clears the configuration memory once more and starts the configuration process. If this pin is high during power up, the device will skip the WAIT state after clearing the configuration memory and will go directly into configuration mode.
$\overline{\text{INIT}}$	**A multiplexed, open-drain I/O pin that indicates initialization status.** A low $\overline{\text{INIT}}$ when $\overline{\text{PROGRAM}}$ is high indicates initialization is not complete and the device is not ready to receive data for configuration. A high $\overline{\text{INIT}}$ (when DONE is low) indicates that initialization is complete and no configuration bitstream errors have occurred. For non-JTAG configuration modes, holding the $\overline{\text{INIT}}$ pin low externally will delay configuration.
DONE	**A dedicated open drain pin that signals when configuration is done.** A low output indicates the VF1 FPGA is in configuration mode. A high output indicates configuration is done and all the I/Os are enabled for normal operation. For non-JTAG configuration modes, enabling of all the I/Os in different devices can be synchronized by tying all the DONE pins together. Enabling the synchronization capability is the default condition, but can be disabled by the configuration bitstream.
CCLK	**A dedicated I/O pin for configuration clock input or output.** In the Master and Asynchronous peripheral modes, this pin is the clock output from an internal oscillator. In the Slave mode and Synchronous Peripheral mode, this pin receives a clock from the Master VF1 FPGA or from a host source. In Master serial mode, this signal clocks data from a companion SPROM such as a VCM SPROM.
DOUT	**A multiplexed I/O pin to pass configuration data from the first VF1 FPGA in a chain to subsequent devices.** During configuration, this is an output pin for sending overflow configuration data to daisy-chained devices.
DIN[7:0]	**Seven multiplexed I/O pins for byte-wide data input.** During Synchronous and Asynchronous Peripheral modes, these input pins receive parallel configuration data. During non-JTAG serial modes, DIN0 functions as the data in (DIN) pin.
RDY/$\overline{\text{BUSY}}$	**A multiplexed I/O Ready/$\overline{\text{Busy}}$ status pin.** This pin indicates when it is appropriate to write another byte of configuration data into the VF1 FPGA during Peripheral mode configuration.
TDI, TCLK, TMS, TDO	**TDI, TCLK, and TMS are dedicated input pins; TDO is a dedicated output pin.** These pins are used for JTAG boundary scan functions and for programming VH1 devices in JTAG mode.
$\overline{\text{CS0}}$, CS1, $\overline{\text{WS}}$, $\overline{\text{RS}}$	**Multiplexed I/O pins used in Asynchronous Peripheral mode.** These four pins are used for controlling configuration data entry in Asynchronous Peripheral mode. A write cycle is initiated by simultaneously asserting $\overline{\text{CS0}}$, CS1, and $\overline{\text{WS}}$, and deasserting $\overline{\text{RS}}$. A low to high transition on $\overline{\text{CS0}}$ or $\overline{\text{WS}}$ or a high to low transition on CS1 or $\overline{\text{RS}}$ loads the data on DIN[7:0] into the VF1. A low on $\overline{\text{RS}}$ and high on $\overline{\text{WS}}$ while $\overline{\text{CS0}}$ and CS1 are asserted changes DIN7 into a status pin that outputs the same signal as the RDY/BUSY pin.
HDC	**A multiplexed I/O status pin that is High During Configuration.**
$\overline{\text{LDC}}$	**A multiplexed I/O status pin that is Low During Configuration.**

Table 12. Signals Used in Each Configuration Mode

Master Serial	Slave Serial	Synchronous Peripheral	Asynchronous Peripheral	JTAG	User Operation
M0 (I)	M0 (I)	M0 (I)	M0 (I)	M0 (I)	(I/O)/RTRIG
M1 (I)	M1 (I)	M1 (I)	M1 (I)	M1 (1)	(I/O)/RDO
M2 (I)	M2 (I)	M2 (I)	M2 (I)	M2 (I)	(I/O)
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)
$\overline{\text{INIT}}$ (OD)	$\overline{\text{INIT}}$ (OD)	$\overline{\text{INIT}}$ (OD)	$\overline{\text{INIT}}$ (OD)	$\overline{\text{INIT}}$ (OD)	(I/O)
DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)	DONE (OD)
HDC (O)	HLC (O)	HLC (O)	HLC (O)		(I/O)
$\overline{\text{LDC}}$ (O)	$\overline{\text{LDC}}$ (O)	$\overline{\text{LDC}}$ (O)	$\overline{\text{LDC}}$ (O)		(I/O)
CCLK (O)	CCLK (I)	CCLK (I)	CCLK (O)		CCLK (I)
TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)	TDI (I)
TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)	TCLK (I)
TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)	TMS (I)
TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)	TDO (O)
DOUT (O)	DOUT (O)	DOUT (O)	DOUT (O)		(I/O)
DIN0 (I)	DIN0 (I)	DIN0 (I)	DIN0 (I)		(I/O)
		DIN1 (I)	DIN1 (I)		(I/O)
		DIN2 (I)	DIN2 (I)		(I/O)
		DIN3 (I)	DIN3 (I)		(I/O)
		DIN4 (I)	DIN4 (I)		(I/O)
		DIN5 (I)	DIN5 (I)		(I/O)
		DIN6 (I)	DIN6 (I)		(I/O)
		DIN7 (I)	DIN7 (I)		(I/O)
		RDY/BUSY(O)	RDY/BUSY(O)		(I/O)
			$\overline{\text{CS0}}$ (I)		(I/O)
			CS1 (I)		(I/O)
			$\overline{\text{WS}}$ (I)		(I/O)
			$\overline{\text{RS}}$ (I)		(I/O)

Note:

I = *Input*

O = *Output*

OD = *Open Drain*

I/O = *Input/Output*

BEYOND PERFORMANCE

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