COM'L: 25/33 MIL:-25

Am29CPL151H-25/33

CMOS 64-Word Field-Programmable Controller (FPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Implements complex state machines
- High-speed, low-power CMOS EPROM technology
- Functionally equivalent to the bipolar Am29PL141
- Seven conditional inputs (each can be registered as a programmable option), 16 outputs
- Up to 33-MHz maximum frequency
- 64-word by 32-bit CMOS EPROM
- Space-saving 28-pin OTP plastic SKINNYDIP® and PLCC packages and windowed ceramic SKINNYDIP package
- 29 instructions
  - Conditional branching, conditional looping, conditional subroutine call, multiway branch

GENERAL DESCRIPTION

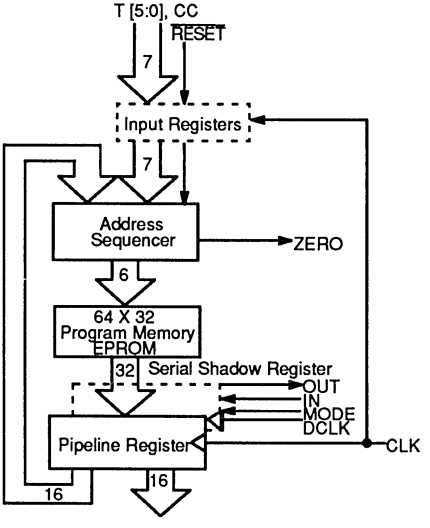
The Am29CPL151 is a CMOS, single-chip Field Programmable Controller (FPC). It allows implementation of complex state machines and controllers by programming the appropriate sequence of instructions. Jumps, loops, and subroutine calls, conditionally executed based on the test inputs, provide the designer with powerful control flow primitives.

Intelligent control may be distributed throughout the system by using FPCs to control various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units. An address sequencer, the heart of the FPC, provides the address to an internal 64-word by 32-bit EPROM.

The Am29CPL151 is functionally equivalent to the Am29PL141 but is manufactured in CMOS technology and offers a space-saving 300-mil SKINNYDIP package. A pin-compatible larger FPC is offered as the Am29CPL154 with a deeper 512 x 36 memory and added flexibility.

This UV-erasable and reprogrammable device utilizes proven floating-gate CMOS EPROM technology to ensure high reliability, easy programming, and better than 99.9% programming yields. The Am29CPL151 is offered in both windowed and One-Time Programmable (OTP) packages. OTP plastic SKINNYDIP and PLCC devices are ideal for volume production.

SIMPLIFIED BLOCK DIAGRAM



10135-001B

Publication# 10135 Rev. E Amendment/0
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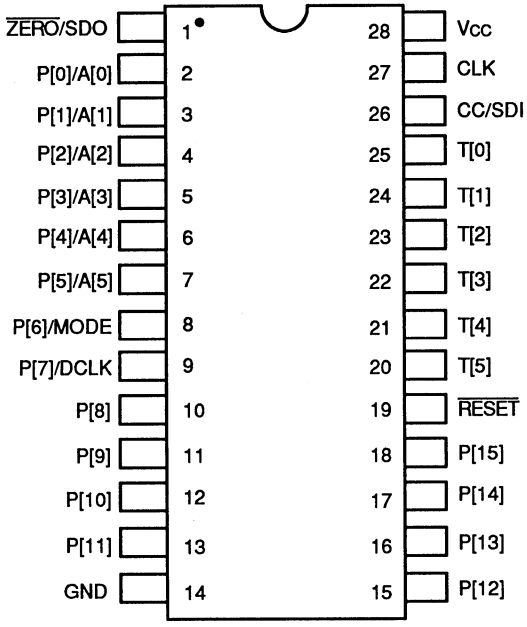
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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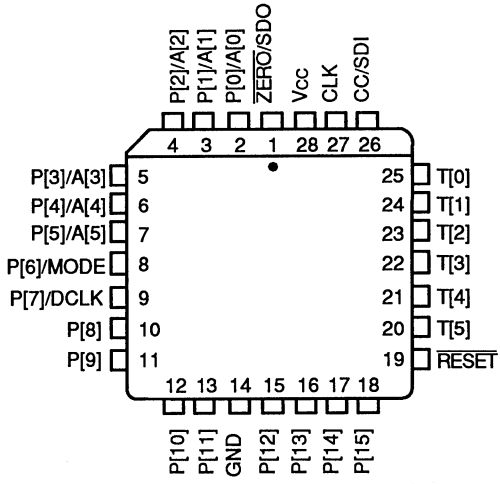
PLCC/LCC



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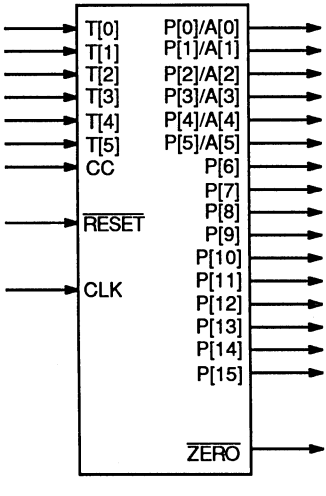
Note:
Pin 1 is marked for orientation.

LOGIC SYMBOLS

Normal Configuration



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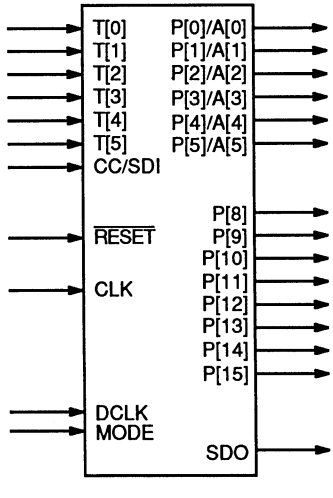
SSR® Diagnostics Configuration

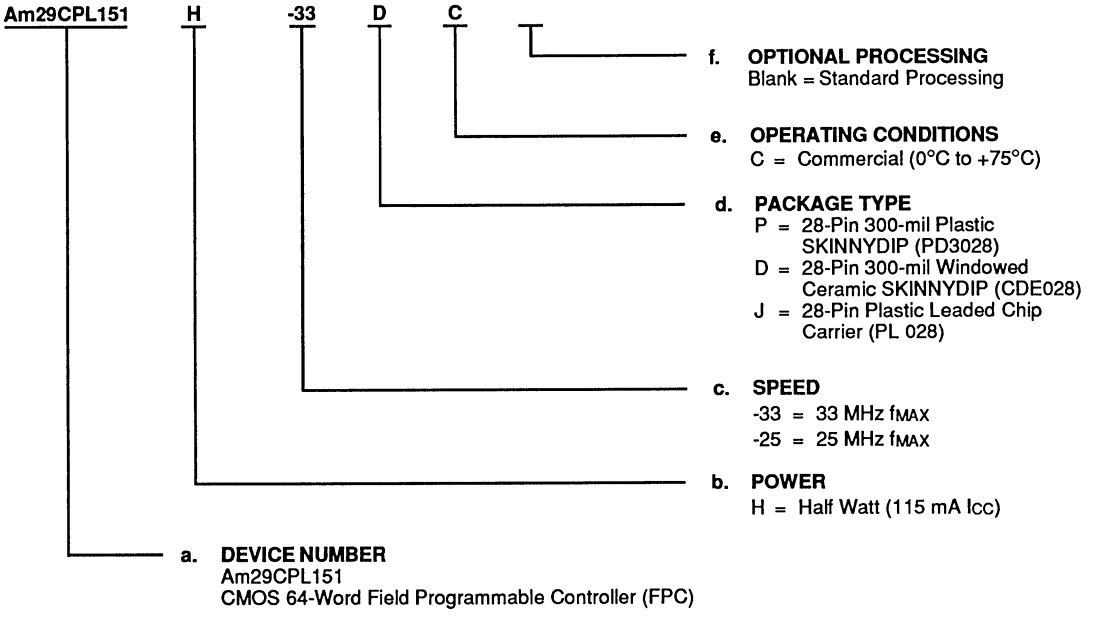


10135-005A

ORDERING INFORMATION
Commercial Products

AMD products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Package Type
e. Operating Conditions
f. Optional Processing



Valid Combinations	
Am29CPL151H-33	PC, DC, JC
Am29CPL151H-25	

Valid Combinations

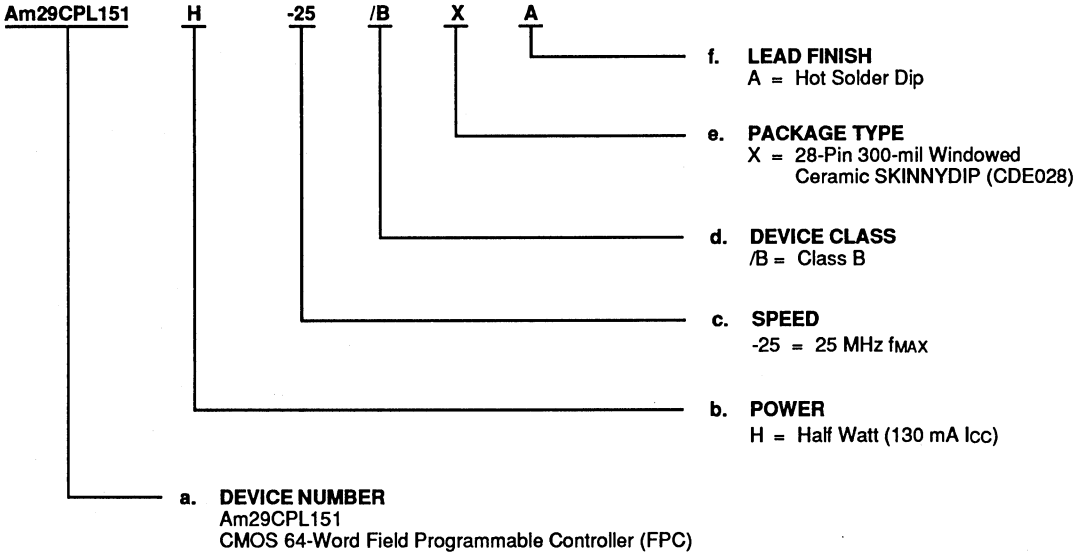
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
Am29CPL151H-25	/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

CC [SDI]
Optionally Registered Condition Code Test Input

When the TEST (P[24:22]) field of the executing instruction is set to 6 (binary 110), CC is selected to be the conditional input. In SSR diagnostic configuration, CC is also the Serial Data Input (SDI). An EPROM bit associated with this input may be programmed to make this input a registered input. The default state of this input is unregistered.

CLK
Clock Input

The rising edge of the clock latches the program counter, count register (CREG), subroutine register (SREG), pipeline register, and EQ flag. The rising edge of the clock also latches the test input registers, CC register, and the $\overline{\text{RESET}}$ register if their respective configuration bits are set to enable internal synchronizing registers.

P[15:8]
Outputs

The upper eight general-purpose control outputs are enabled by the OE signal from the pipeline register. When OE is HIGH, P[15:8] are enabled, and when LOW, P[15:8] are disabled.

P[7:6], P[5:0]/A[5:0] [DCLK, MODE]
Outputs

The lower eight general-purpose control outputs are permanently enabled. In the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK and P[6] becomes the diagnostic control input MODE. In expand mode (when the EXP bit is programmed) bits P[5:0] become the Program Memory address outputs A[5:0].

$\overline{\text{RESET}}$
Optionally Registered $\overline{\text{Reset}}$ Input; Active LOW

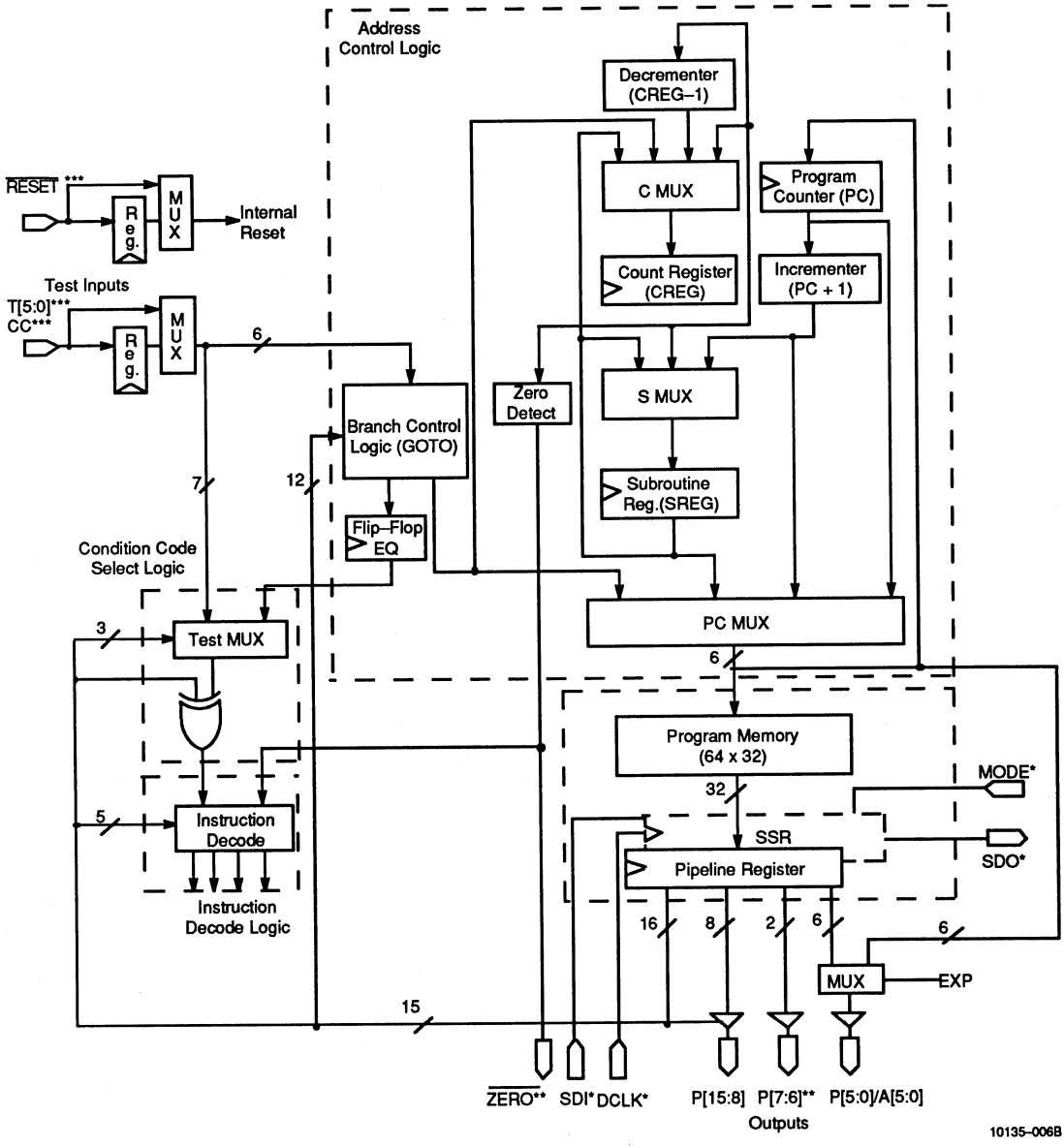
When the reset input is LOW, the output of the PC MUX is forced to the uppermost program address (63). On the next rising edge of the clock, this address (63) is loaded into the program counter; the instruction at location 63 is loaded into the pipeline register, and the EQ flag is cleared. A programmable configuration bit allows the option of making this a registered input. If $\overline{\text{RESET}}$ is internally registered, the first rising edge of the clock latches it. On the next rising edge of the clock, the EQ flip-flop is cleared and the contents of memory location 63 are loaded into the pipeline register. The default state of this input is unregistered.

T[5:0]
Optionally Registered Test Inputs

In conditional instructions, the TEST inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[5:0] inputs can also be used as a branch address when performing a program branch or as a count value to be loaded into the CREG. Each of these inputs has an EPROM bit associated with it. This bit may be programmed such that the corresponding input becomes a registered input. The default state of these inputs is unregistered.

$\overline{\text{ZERO}}$ [SDO]
Zero Output; Active LOW

A LOW state on the $\overline{\text{ZERO}}$ output indicates that the CREG value is zero. In the SSR diagnostic configuration, $\overline{\text{ZERO}}$ becomes the Serial Data Output (SDO). This change is only on the output pin; internally, the zero-detect function is unchanged.



* These pins available only in SSR mode.
** These pins available only in normal mode.
*** Each of the T[5:0], RESET, and CC inputs can be individually registered or left unregistered as a programmable option.

Figure 1. Am29CPL151 Detailed Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1, the detailed block diagram of the Am29CPL151, shows logic blocks and interconnecting buses that permit parallel performance of different operations in a single instruction. The FPC consists of four main logic blocks: the program memory, address control logic, condition code selection logic, and instruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The program memory contains the user-defined instruction flow and output sequence. The address control logic addresses the program memory. This control logic supports high-level instruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional instruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The instruction decode generates the control signals necessary to perform the instruction specified by the instruction part (P[31:16]) of the microword. The SSR enables in-system testing to isolate problems down to the IC level.

Program Memory

The FPC program memory is a 64-word by 32-bit EPROM with a 32-bit pipeline register at its output. The upper 16 bits (P[31:16]) of the pipeline register are internal to the FPC and form the instruction to control address sequencing. The format for instructions is: a one-bit synchronous Output Enable OE, a five-bit OPCODE, a one-bit test polarity select POL, a three-bit TEST condition select field, and a six-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

The lower 16 bits (P[15:0]) of the pipeline register are brought out as user-defined, general-purpose control outputs. The upper eight control outputs (P[15:8]) are disabled when OE is programmed as a LOW. The lower eight control bits (P[7:0]) are always enabled. Outputs P[5:0] will contain the next instruction address when the optional EXP EPROM cell is programmed.

Controlling External PROM

By programming the EXP bit, PC MUX is output over pins P[5:0]/A[5:0]. This feature can be used to extend the width of the output control word when external registered memories are used. In the diagram below, the Am29CPL151 controls external registered PROMs to provide an output control word (10 + N) bits wide (where N is the bit width of the PROMs).

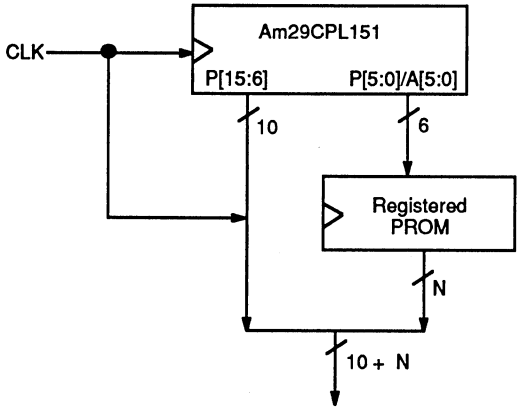


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Figure 2. Controlling External PROM

Address Control Logic

The address control logic consists of five smaller logic blocks. These are:

PC MUX –Program counter multiplexer

P CNTR –Program counter (PC) and incrementer (PC + 1)

SUBREG –Subroutine register (SREG) with subroutine mux (S MUX)

CNTR –Count register (CREG) with counter mux (C MUX), decrementer (CREG–1), and zero detect

GOTO –Specialized branch control logic

The PC MUX is a six-bit, four-to-one multiplexer. It selects either the PC, PC + 1, SREG, or GOTO output as the next microaddress input to the Program Memory and to the PC. The PC thus always contains the address of the instruction in the pipeline register. During a Reset, the PC MUX output is forced to all ones, selecting location 63 from Program Memory.

The P CNTR block consists of a six-bit register (PC) driving a six-bit combinatorial incrementer (PC + 1). Either the present or the incremented values of PC can address the Program Memory. The incremented value of PC can be saved as a subroutine return address. The present PC value can address the Program Memory when waiting for a condition to become valid. PC + 1 addresses the Program Memory for sequential program flow, for unconditional instructions, and as a default for conditional instructions.

The SUBREG block consists of a six-bit, three-to-one multiplexer (S MUX) driving a six-bit register (SREG). The three possible SREG inputs are PC + 1, CREG, and SREG. SREG normally operates as a one-deep stack to save subroutine return addresses. PC + 1 is the input source when performing subroutine calls, and PC MUX is the output destination when performing return from subroutine.

The CNTR block consists of a six-bit, four-to-one multiplexer (C MUX), driving a six-bit register (CREG); a six-bit combinatorial decrementer (CREG-1); and a zero-detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The SUBREG and CNTR can be considered as one logic block because of their unique interaction. Both have the other as an additional input source and output destination. The CREG can therefore be an additional stack location when not used for counting, and the SREG can be a nested-count location when not used as a stack location. Thus the SREG and CREG can operate in three different modes:

1. As a separate one-deep stack and counter
2. As a two-deep stack
3. As a two-deep nested counter

The GOTO logic block serves three functions:

1. It provides a six-bit count value from the DATA field in the pipeline register (P[21:16]) or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.
2. It provides a branch address from the DATA field in the pipeline register P[21:16] or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.
3. It compares T[5:0] masked by the MASK field P[21:16], called T*M, to the CONSTANT field from the pipeline register P[27:22]. If a match occurs, the EQ flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to masked test bits must be zero.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to sum-of-products can be performed since a no-match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

Note: A zero in the MASK field blocks the corresponding bit in the TEST field; a one activates the corresponding bit.

The constant field bits that correspond to masked test field bits must be zero. A zero is substituted for masked test field bits. The "POL" bit is a "don't care" when using test inputs to load registers.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Condition Code Selection Logic

The condition code selection logic consists of an eight-to-one multiplexer. The eight test condition inputs are the device inputs CC, T[5:0], and the EQ flag. The TEST field P[24:22] selects one of the eight conditions to test.

The polarity bit POL in the instruction allows the user to test for either a pass or fail condition. Refer to table1 for details.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

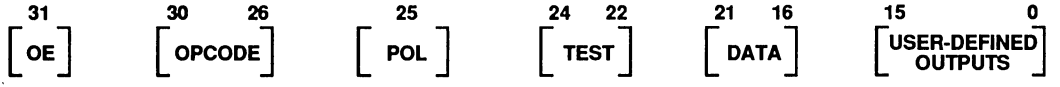
Instruction Decode

The instruction decoder is a PLA that generates the control for 29 different instructions. The decoder inputs include the OPCODE field P[30:26], the zero detection output from the CNTR, and the selected test condition code from the condition code selection logic.

Operational Modes

The Am29CPL151 operates as a six-bit microcontroller in normal mode, and there are several configuration bits that can be programmed to modify this normal operation. The EXP bit allows the six program address lines from the PC MUX to be output on the lower six bits of the output pins (P[5:0]) so that a user can expand the width of the control lines by using external registered memories. The SSR bit allows on-chip diagnostic capabilities for in-system testing. The remaining bits serve to individually select whether the input pins will be unsynchronized or not. The default setting of these bits (unprogrammed,1) will cause each pin to be unsynchronized, and so programming a given bit (to 0) will cause that corresponding input to become internally synchronized.

Am29CPL151 General Instruction Format



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WHERE:
OE = Synchronous Output Enable for P[15:8].
OPCODE = A five-bit opcode field for selecting one of the 28 single-data-field instructions.
POL = A one-bit test condition polarity select (refer to table 1).
TEST = A three-bit test condition select.

TEST[24:22]	UNDER TEST
000	T [0]
001	T [1]
010	T [2]
011	T [3]
100	T [4]
101	T [5]
110	CC
111	EQ

DATA = A six-bit conditional branch address, test input mask, or counter value field designated as PL in instruction mnemonics.

Table 1

Input Condition Being Tested	POL	Test Result
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

Am29CPL151 Comparison Instruction Format

10135-008B

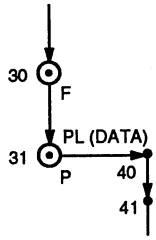
WHERE:
OE = Synchronous Output Enable for P[15:8].
OPCODE = Compare instruction (binary 100).
CONSTANT = A six-bit constant for equal-to comparison with T*M.
MASK = A six-bit mask field for masking the incoming T[5:0] inputs.

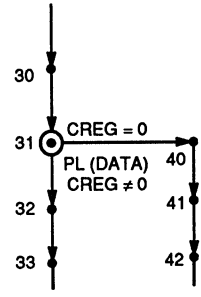
Am29CPL151 INSTRUCTION SET DEFINITION

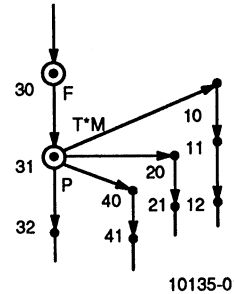
• = Other instruction
⊙ = Instruction being described
○ = Register in part

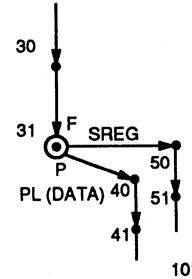
P = Test Pass
F = Test Fail
X,Y are arbitrary values in the CREG or SREG

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

19	GOTOPL	**IF (cond) THEN GOTO PL (data)**
		Conditional branch to the address in the PL (DATA field). The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-009A
				If (cond = true) Then
				PC = PL(data)
				Else
				PC = PC + 1

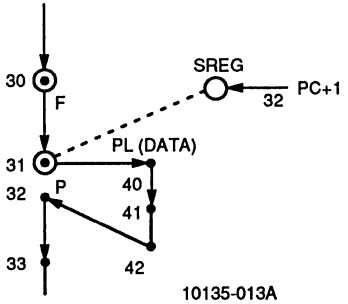
0B	GOTOPLZ	**IF (CREG = 0) THEN GOTO PL (data)**
		Conditional branch to the address in the PL (DATA field) when CREG is equal to zero. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and the CREG is equal to zero.
			
			10135-010A
				If (CREG = 0) Then
				PC = PL(data)
				Else
				PC = PC + 1

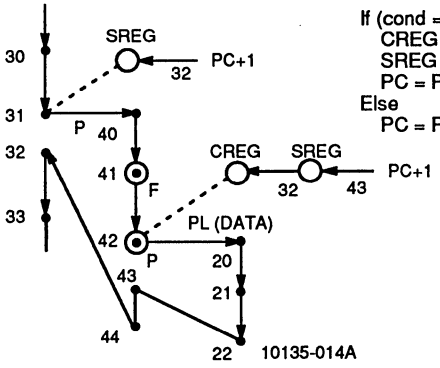
0F	GOTOTM	**IF (cond) THEN GOTO TM (data)**
		Conditional branch to the address defined by the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for multiway branches. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-011A
				If (cond = true) Then
				PC = T*M
				Else
				PC = PC + 1

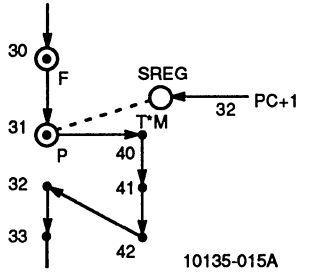
18	FORK	**IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)**
		Conditional branch to the address in the PL (DATA field) or the SREG. A branch to PL is taken if the condition is true and a branch to SREG if false. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-012A
				If (cond = true) Then
				PC = PL(data)
				Else
				PC = SREG

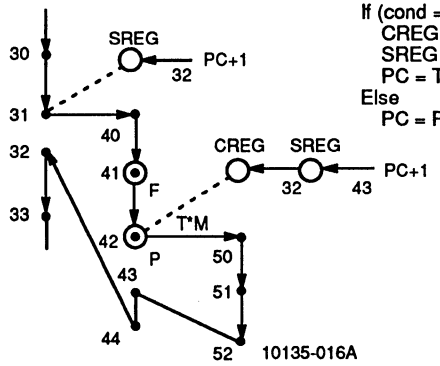
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

1C	CALPL	**IF (cond) THEN CALL PL (data)** Conditional jump to subroutine at the address in the PL (DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-013A	If (cond = true) Then
				SREG = PC + 1
				PC = PL(data)
				Else
				PC = PC + 1

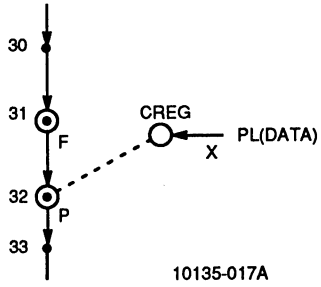
1D	CALPLN	**IF (cond) THEN CALL PL (data), NESTED** Conditional jump to subroutine at the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep stack, the PC + 1 is pushed into the SREG as the return address, and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset of the test field selects it and the condition passes.	 10135-014A	If (cond = true) Then
				CREG = SREG
				SREG = PC + 1
				PC = PL(data)
				Else
				PC = PC + 1

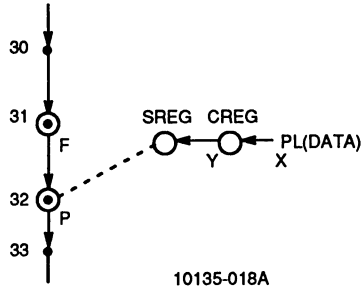
1E	CALTM	**IF (cond) THEN CALL TM (data)** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-015A	If (cond = true) Then
				SREG = PC + 1
				PC = T*M
				Else
				PC = PC + 1

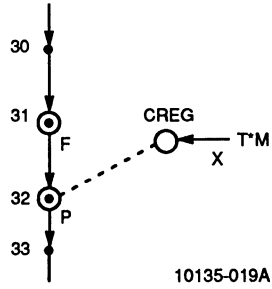
1F	CALTMN	**IF (cond) THEN CALL TM (data), NESTED** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field) nested. The PC + 1 is pushed into the SREG as the return address, and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset of the test field selects it and the condition passes.	 10135-016A	If (cond = true) Then
				CREG = SREG
				SREG = PC + 1
				PC = T*M
				Else
				PC = PC + 1

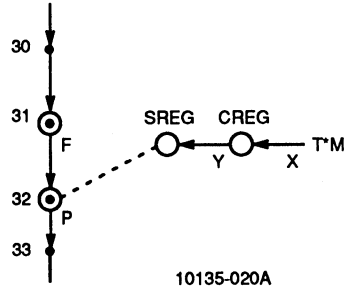
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

04	LDPL	**IF (cond) THEN LOAD PL (data)**
		Conditional load the CREG from the PL (DATA field).
			
			10135-017A
				If (cond = true) Then
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

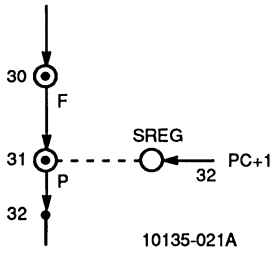
05	LDPLN	**IF (cond) THEN LOAD PL (data), NESTED**
		Conditional load the CREG from the PL (DATA field) nested. The CREG and SREG are treated as a two-deep nested count register, the previous CREG value is pushed into the SREG as a nested count, and the CREG is loaded from PL.
			
			10135-018A
				If (cond = true) Then
				SREG = CREG
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

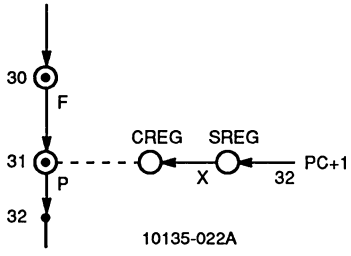
06	LDTM	**IF (cond) THEN LOAD TM (data)**
		Conditional load the CREG from the T*M (T[5:0] inputs under bit-wise mask from the DATA field).
			
			10135-019A
				If (cond = true) Then
				CREG = T*M
				PC = PC + 1
				Else
				PC = PC + 1

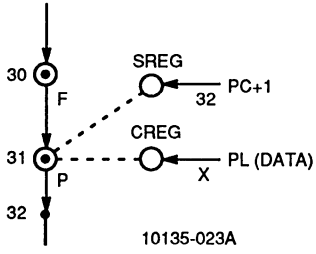
07	LDTMN	**IF (cond) THEN LOAD TM (data) NESTED** Conditional load the CREG from the T*M (T[5:0] inputs under bit-wise mask from the DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, the previous CREG value is transferred into the SREG, and the CREG is loaded from T*M.	 10135-020A	If (cond = true) Then SREG = CREG CREG = T*M PC = PC + 1

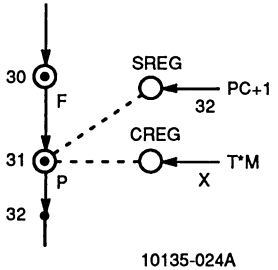
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

15	PSH	**IF (cond) THEN PUSH**
		Conditional push the PC + 1 into the SREG.
			
			10135-021A
				If (cond = true) Then
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

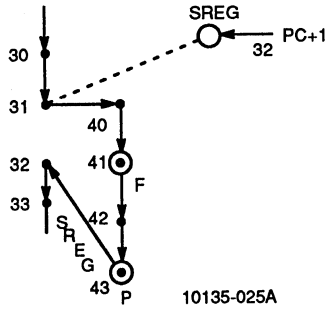
17	PSHN	**IF (cond) THEN PUSH, NESTED**
		Conditional push the PC + 1 into the SREG nested. This microinstruction treats the SREG and CREG as a two-deep stack, PC + 1 is pushed into SREG, and the previous value in SREG is transferred into the CREG.
			
			10135-022A
				If (cond = true) Then
				CREG = SREG
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

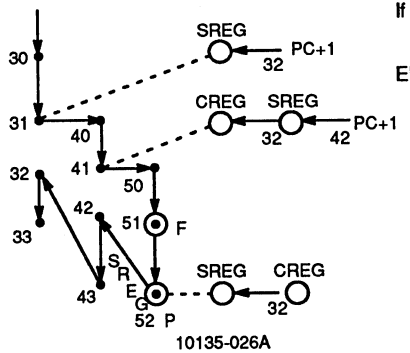
14	PSHPL	**IF (cond) THEN PUSH, LOAD PL (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the PL (DATA field).
			
			10135-023A
				If (cond = true) Then
				CREG = PL(data)
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

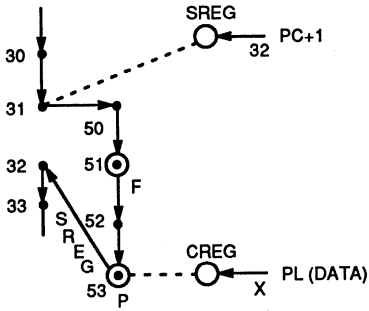
16	PSHTM	**IF (cond) THEN PUSH, LOAD TM (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the T*M (T[5:0] under bitwise mask from the DATA field).
			
			10135-024A
				If (cond = true) Then
				CREG = T*M
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

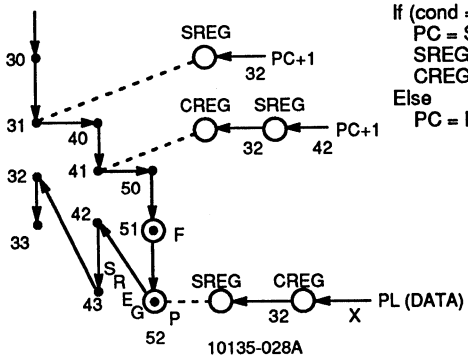
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

02	RET	**IF (cond) THEN RET**
		Conditional return from subroutine. The SREG provides the return from subroutine address.
			
			10135-025A
				If (cond = true) Then
				PC = SREG
				Else
				PC = PC + 1

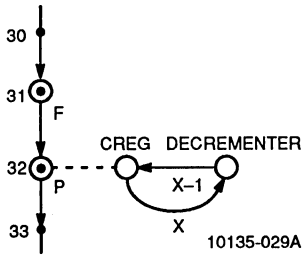
03	RETN	**IF (cond) THEN RET, NESTED**
		Conditional return from nested subroutine. This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-026A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				Else
				PC = PC + 1

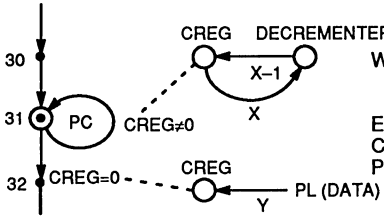
00	RETPL	**IF (cond) THEN RET, LOAD PL (data)**
		Conditional return from subroutine and load the CREG from the PL (DATA field). The SREG provides the return from subroutine address.
			
			10135-027A
				If (cond = true) Then
				CREG = PL(data)
				PC = SREG
				Else
				PC = PC + 1

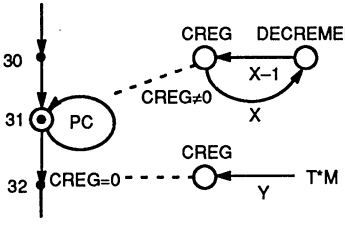
01	RETPLN	**IF (cond) THEN RET NESTED, LOAD PL (data)**
		Conditional return from nested subroutine and load the CREG from the PL (DATA field). This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-028A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				CREG = PL(data)
				Else
				PC = PC + 1

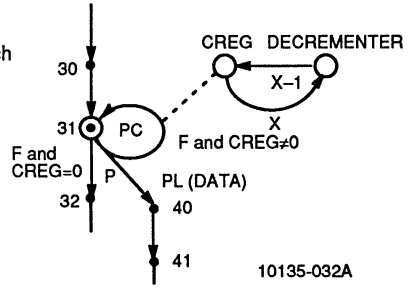
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

09	DEC	**IF (cond) THEN DEC**
		Conditional decrement of the CREG.
			
			10135-029A
				If (cond = true) Then
				CREG = CREG –1
				PC = PC + 1
				Else
				PC = PC + 1

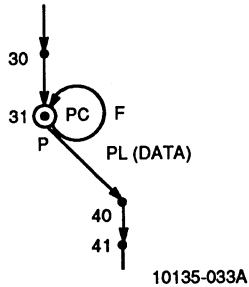
0C	DECPL	**WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the PL (DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be re-loaded from PL. This instruction does not depend on the pass/fail condition.
			
			10135-030A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = PL(data)
				PC = PC + 1

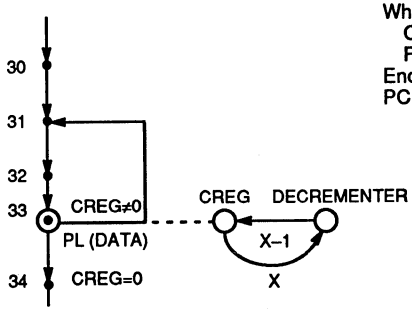
0E	DECTM	**WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while the CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from T*M. This instruction does not depend on the pass/fail condition.
			
			10135-031A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = T*M
				PC = PC + 1

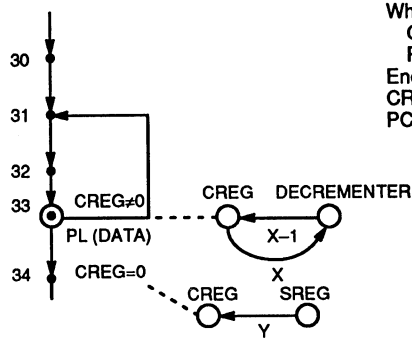
1B	DECGOPL	**If (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT**
		Conditional Hold/Count. The current instruction will be refetched and the CREG decremented until the condition under test becomes true or the counter is equal to zero. If the condition becomes true, a branch to the address in the PL (DATA field) is executed. If the counter becomes zero without the condition becoming true, a CONTINUE is executed. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-032A
				While (cond = false)
				If (CREG < > 0)
				CREG = CREG –1
				PC = PC
				Else
				PC = PC + 1
				End While
				PC = PL (data)

Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

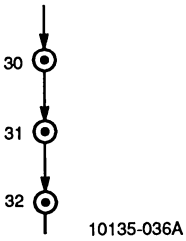
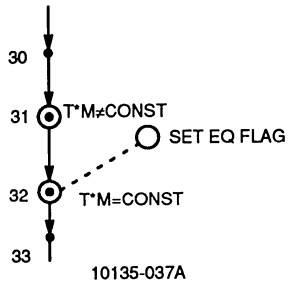
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

1A	WAIT	**IF (cond) THEN GOTO PL (data) ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When true, a branch to the address in the PL (DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-033A
				If (cond = true) Then
				PC = PL (data)
				Else
				PC = PC

08	LPPL	**WHILE (CREG < > 0) LOOP TO PL (data)**
		Conditional loop to the address in the PL (DATA field). This instruction is intended to be placed at the bottom of an iterative loop. If the CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the loop) is executed. If the CREG is equal to zero, looping is complete and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-034A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL (data)
				End While
				PC = PC + 1

0A	LPPLN	**WHILE (CREG < > 0) LOOP TO PL (data) ELSE NEST**
		Conditional loop to the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, and the instruction is intended to be placed at the bottom of an "inner-nested" iterative loop. If the CREG is not equal to zero, the CREG is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the inner loop) is executed. If the CREG is equal to zero, the inner loop is complete, and the count value for the outer loop is transferred from the SREG into the CREG. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-035A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL(data)
				End While
				CREG = SREG
				PC = PC + 1

Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
0D	CONT	**CONTINUE** The next sequential instruction is fetched unconditionally.	 10135-036A	PC = PC + 1
10–13 (100XX binary)	CMP	**CMP TM (mask) TO PL (constant)** This instruction performs bitwise Exclusive-OR of T*M (T[5:0] under bitwise mask from the MASK field) with CONSTANT (P[27:22]). If T*M equals CONSTANT, the EQ flag is set to one, which may be branched on in a following instruction. If not equal, the EQ flag is unaffected. This allows sequences of compares, in a manner analogous to sum-to-products, to be performed which can be followed by a single conditional branch if one or more of the comparisons are true. Note: The EQ flag is set to zero on reset or when EQ is selected as the test condition in a branch. Conditional returns on EQ leave the flag unchanged. Constant field bits that correspond to masked test field bits must be zero. This instruction does not depend on the pass/fail condition.	 10135-037A	Compare T*M and CONSTANT EQ = ((T [5:0] .AND. MASK) .XNOR. CONSTANT) .OR. EQ PC = PC + 1

INSTRUCTIONS BASED ON TEST CONDITIONS

Op-code	Mnemonic	Assembler Statement	Condition Pass				Condition Fail				
			PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	Notes
00	RETPL	IF (cond) THEN RET, LOAD PL (data)	SREG	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
01	RETPLN	IF (cond) THEN RET NESTED, LOAD PL (data)	SREG	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
02	RET	IF (cond) THEN RET	SREG	Hold	Hold	NC	PC + 1	Hold	Hold	NC	
03	RETN	IF (cond) THEN RET, NESTED	SREG	Load CREG	Hold	NC	PC + 1	Hold	Hold	NC	
04	LDPL	IF (cond) THEN LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
05	LDPLN	IF (cond) THEN LOAD PL (data), NESTED	PC + 1	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
06	LDTM	IF (cond) THEN LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC + 1	Hold	Hold	NC	
07	LDTMN	IF (cond) THEN LOAD TM (data), NESTED	PC + 1	Load CREG	Load TM	NC	PC + 1	Hold	Hold	NC	
09	DEC	IF (cond) THEN DEC	PC + 1	Hold	DEC	NC	PC + 1	Hold	Hold	NC	
0F	GOTOTM	IF (cond) THEN GOTO TM (data)	TM	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
14	PSHPL	IF (cond) THEN PUSH, LOAD PL (data)	PC + 1	PC + 1	Load PL	NC	PC + 1	Hold	Hold	NC	
15	PSH	IF (cond) THEN PUSH	PC + 1	PC + 1	Hold	NC	PC + 1	Hold	Hold	NC	
16	PSHTM	IF (cond) THEN PUSH, LOAD TM (data)	PC + 1	PC + 1	Load TM	NC	PC + 1	Hold	Hold	NC	
17	PSHN	IF (cond) THEN PUSH, NESTED	PC + 1	PC + 1	Load SREG	NC	PC + 1	Hold	Hold	NC	
18	FORK	IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)	PL	Hold	Hold	Reset	SREG	Hold	Hold	NC	1
19	GOTOPL	IF (cond) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
1A	WAIT	IF (cond) THEN GOTO PL (data) ELSE WAIT	PL	Hold	Hold	Reset	PC	Hold	Hold	NC	1
1C	CALPL	IF (cond) THEN CALL PL (data)	PL	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1D	CALPLN	IF (cond) THEN CALL PL (data), NESTED	PL	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1
1E	CALTM	IF (cond) THEN CALL TM (data)	TM	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1F	CALTMN	IF (cond) THEN CALL TM (data), NESTED	TM	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1

Key:
- PC = Program Counter
- SREG = Stack Register
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If COND = EQ and condition PASSES, reset EQ flag.
2. If COND = EQ and CREG ≠ 0, reset EQ flag.
3. If COND = EQ and CREG = 0, reset EQ flag.
4. Set EQ flag if CONST field = T*M.

INSTRUCTIONS DEPENDENT ON CREG

			CREG = 0				CREG ≠ 0				
Op-code	Mnemonic	Assembler Statement	PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	Notes
08	LPPL	WHILE (CREG < > 0) LOOP TO PL (data)	PC + 1	Hold	Hold	NC	PL	Hold	DEC	Reset	2
0A	LPPLN	WHILE (CREG < > 0) LOOP TO PL (data), ELSE NEST	PC + 1	Hold	Load SREG	NC	PL	Hold	DEC	Reset	2
0B	GOTOPLZ	IF (CREG = 0) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
0C	DECPL	WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC	Hold	DEC	NC	
0E	DECTM	WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC	Hold	DEC	NC	

INSTRUCTIONS DEPENDENT ON TEST CONDITION AND CREG VALUE

					Condition Pass			Condition Fail				
Op-code	Mnemonic	Assembler Statement	CREG Content	PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	Notes
1B	DECGOPL	IF (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT	≠ 0	PL	Hold	Hold	Reset	PC	Hold	DEC	NC	1
			= 0	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	

UNCONDITIONAL INSTRUCTIONS

Opcode	Mnemonic	Assembler Statement	PC MUX	SREG	CREG	EQ FLAG	Notes
0D	CONT	CONTINUE	PC + 1	Hold	Hold	NC	
10-13 (Binary 100XX)	CMP	CMP TM (mask) TO PL (constant)	PC + 1	Hold	Hold	Set	4

Key:
- PC = Program Counter
- SREG = Stack Register
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If COND = EQ and condition PASSES, reset EQ flag.
2. If COND = EQ and CREG ≠ 0, reset EQ flag.
3. If COND = EQ and CREG = 0, reset EQ flag.
4. Set EQ flag if CONST field = T*M.

Am29CPL151 SSR Diagnostics Option

As a programmable option, the Am29CPL151 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing to isolate problems down to the IC level.

The SSR diagnostics configuration activates a 32-bit-wide D-type register called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the Program Memory in normal mode or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. CC also functions as the Serial Data Input (SDI), $\overline{ZERO}$ becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in table 2.

Serially loading a test instruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test instruction. The test result can then be clocked into the pipeline register as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

Table 2

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
X	L	↑	H, L, ↓	S_0	$S_{i-1} \leftarrow S_i$ $S_{31} \leftarrow$ SDI	Hold	Serial Right-Shift Shadow Register
CC (Note 1)	L	H, L, ↓	↑	S_0	Hold	$P_i \leftarrow$ EPROM$_i$	Normal Operation; Load Pipeline Register from EPROM
L	H	↑	H, L, ↓	L	$S_i \leftarrow P_i$	Hold	Load Shadow Register from Pipeline Register (Note 2)
X	H	H, L, ↓	↑	SDI	Hold	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H, L, ↓	H	Hold	Hold	Hold Shadow Register

Notes:

1. During normal operation, this pin behaves as the CC input.
2. S7, S6 are undefined. S[15:8] load from the source driving pins P[15:8]. If P[31] in the microword is a ONE, S[15:8] are loaded from the pipeline register. If P[31] in the microword is a ZERO, S[15:8] are loaded from an external source.

Key:
H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
H, L, ↓ = Not a rising edge (steady state or falling edge)

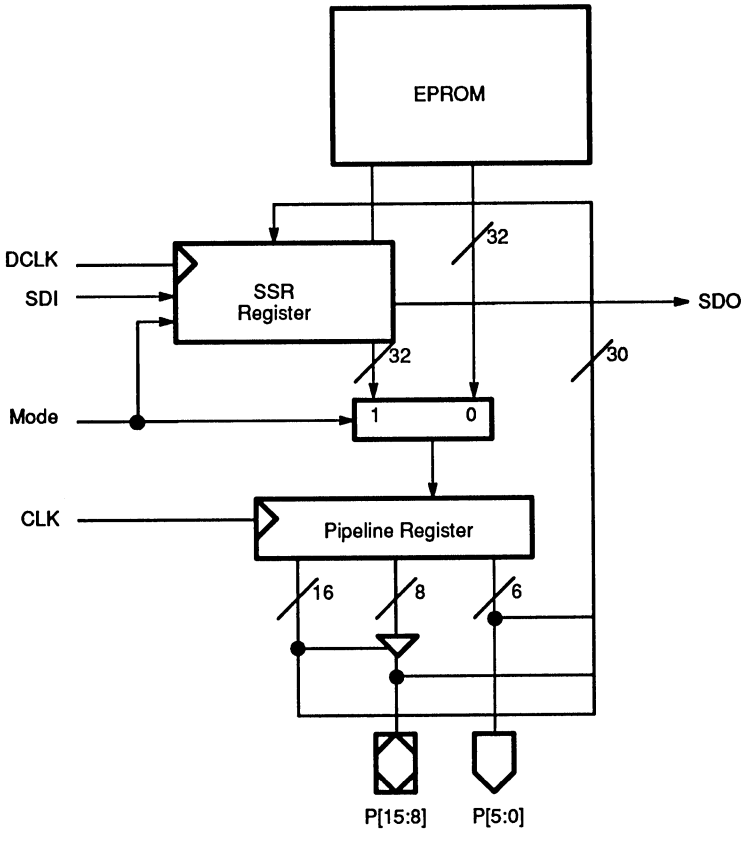


Figure 3. SSR Diagnostics Logic

Erasure

In order to fully erase all memory locations, it is necessary to expose the memory array to a standard ultraviolet light source having a wavelength of 2537 angstroms. The minimum recommended dose (UV intensity x exposure time) is 15 Wsec/cm^2. For a UV lamp with a 12 mW/cm^2 power rating, the exposure time would be about 30 minutes. The device should be located one inch from the source in a direct line.

It should be noted that erasure will begin with exposure to light having wavelengths less than 4000 angstroms. To prevent exposure to sunlight or fluorescent lighting, an opaque label should be affixed over the window after programming.

OTP (One-Time Programmable) Am29CPL151 devices are available in plastic and are ideal for volume production. They can be inventoried unprogrammed and used with current software revisions; there is no window to be covered to prevent light from changing data.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices

Ambient Temperature (T_A) Operating in Free Air	–0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		105	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		115	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V	25	pF
		Others		T_A = 25°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 2)

No.	Parameter Symbol	Parameter Description		H-33 Min.	H-33 Max.	H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			12		14	ns
2		CLK to A[5:0]			28		36	ns
3		CLK to $\overline{ZERO}$			21		29	ns
4	t_S	T[3:0] to CLK, Registered		8		8		ns
5		T[5:4] to CLK, Registered		10		10		ns
6		T[5:0] to CLK, Asynchronous (Note 3)		30		40		ns
7		CC to CLK, Registered		8		8		ns
8		CC to CLK, Asynchronous (Note 3)		30		40		ns
9		$\overline{RESET}$ to CLK, Registered		12		12		ns
10		RESET to CLK, Asynchronous (Note 3)		26		40		ns
11	t_H (Note 4)	CLK to T[5:0]		0		0		ns
12		CLK to CC		0		0		ns
13		CLK to $\overline{RESET}$		0		0		ns
14	t_{PZX}	CLK to P[15:8] Enable			30		40	ns
15	t_{PXZ}	CLK to P[15:8] Disable			30		40	ns
16	t_{WL}	CLK Width	LOW	12		16		ns
17	t_{WH}		HIGH	12		16		ns
18	t_P	CLK Period (Note 3)		30		40		ns
19	f_{MAX}	Maximum Frequency (1/tP)		33		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (CCT[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD

   CC to CLK setup time:
   CC (a) + (b) – (c) = CC to CLK setup time

   T[5:0] to CLK setup time:
   T[5:0] (a) + (b) – (c) = T[5:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-33 Min.	H-33 Max.	H-25 Min.	H-25 Max.	Unit
SSR Configuration								
20	t_{PD}	Mode to SDO			20		30	ns
21		SDI to SDO			20		30	ns
22	t_{CO}	DCLK to SDO			28		36	ns
23	t_S	Mode to CLK		11		15		ns
24		Mode to DCLK		11		15		ns
25		SDI to DCLK		11		15		ns
26		P[15:8] to DCLK		11		15		ns
27	t_H (Note 1)	CLK to Mode		6		6		ns
28		DCLK to Mode		0		0		ns
29		DCLK to SDI		0		0		ns
30		DCLK to P[15:8]		0		0		ns
31	t_{WL}	DCLK Width	LOW	15		20		ns
32	t_{WH}		HIGH	15		20		ns
33	t_P	DCLK Period		30		40		ns

Note:

1. These hold time parameters are tested on a sample basis.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = 25° C, 125° C, and –55° C.

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		120	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		130	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V	25	pF
		Others		T_A = 25°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

PRELIMINARY

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			20	ns
2		CLK to A[5:0]			40	ns
3		CLK to $\overline{ZERO}$			30	ns
4	t_S	T[3:0] to CLK, Registered		10		ns
5		T[5:4] to CLK, Registered		12		ns
6		T[5:0] to CLK, Asynchronous (Note 3)		40		ns
7		CC to CLK, Registered		10		ns
8		CC to CLK, Asynchronous (Note 3)		40		ns
9		$\overline{RESET}$ to CLK, Registered		16		ns
10		$\overline{RESET}$ to CLK, Asynchronous (Note 3)		40		ns
11	t_H (Note 4)	CLK to T[5:0]		0		ns
12		CLK to CC		0		ns
13		CLK to $\overline{RESET}$		0		ns
14	t_{PZX}	CLK to P[15:8] Enable			40	ns
15	t_{PXZ}	CLK to P[15:8] Disable			40	ns
16	t_{WL}	CLK Width	LOW	15		ns
17	t_{WH}		HIGH	15		ns
18	t_P	CLK Period (Note 3)		40		ns
19	f_{MAX}	Maximum Frequency (1/tP)		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (CC T[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD

   T[5:0] to CLK setup time:
   T[5:0] (a) + (b) – (c) = T[5:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time

   CC to CLK setup time:
   CC (a) + (b) – (c) = CC to CLK setup time
4. These hold time parameters are tested on a sample basis.

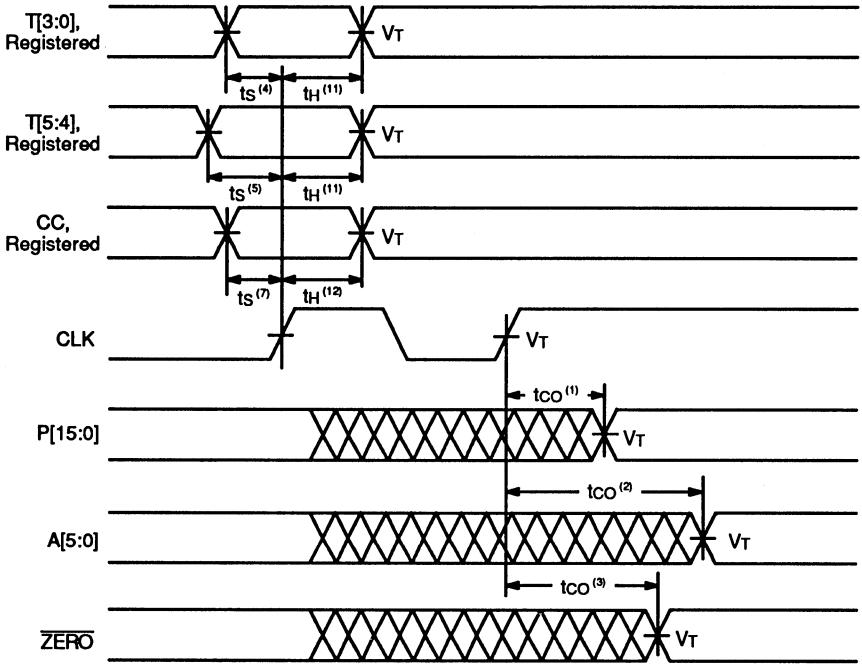
SWITCHING CHARACTERISTICS over MILITARY operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
SSR Configuration						
20	t_{PD}	Mode to SDO			30	ns
21		SDI to SDO			30	ns
22	t_{CO}	DCLK to SDO			36	ns
23	t_S	Mode to CLK		25		ns
24		Mode to DCLK		25		ns
25		SDI to DCLK		25		ns
26		P[15:8] to DCLK		25		ns
27	t_H (Note 1)	CLK to Mode		6		ns
28		DCLK to Mode		0		ns
29		DCLK to SDI		0		ns
30		DCLK to P[15:8]		0		ns
31	t_{WL}	DCLK Width	LOW	25		ns
32	t_{WH}		HIGH	25		ns
33	t_P	DCLK Period		60		ns

Note:

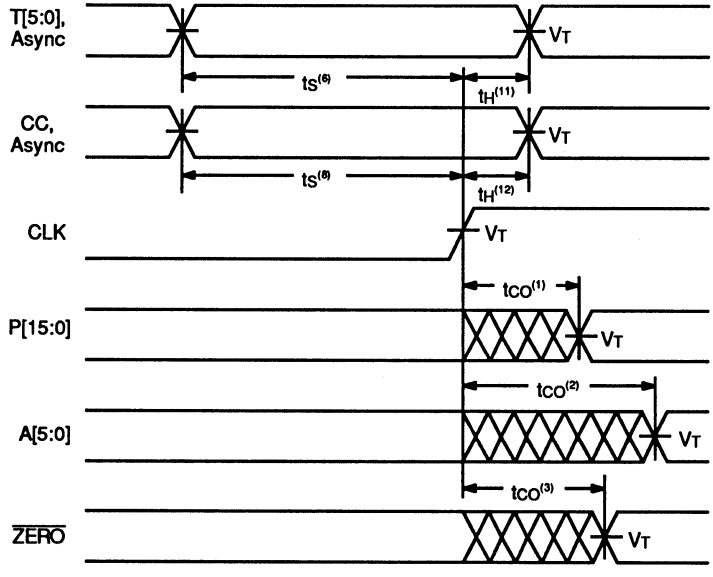
1. These hold time parameters are tested on a sample basis.

SWITCHING WAVEFORMS
Normal Configuration



10135-055A

Registered Test Inputs

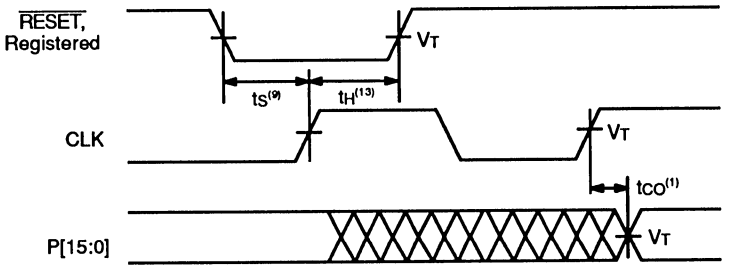


10135-056A

Asynchronous Test Inputs

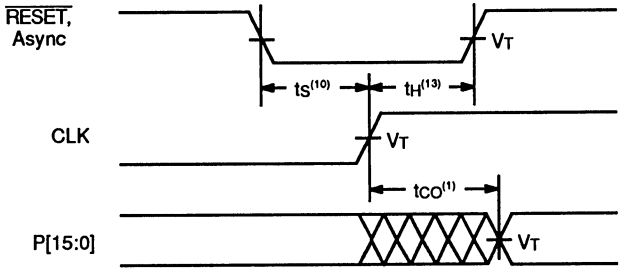
SWITCHING WAVEFORMS (Continued)

Normal Configuration



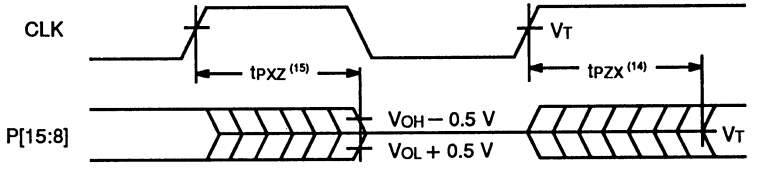
10135-057A

Registered $\overline{\text{RESET}}$



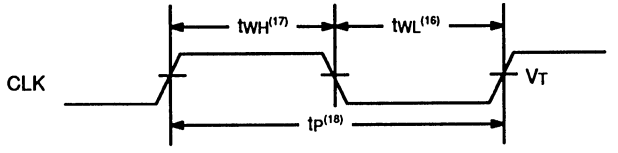
10135-058A

Asynchronous $\overline{\text{RESET}}$



10135-059A

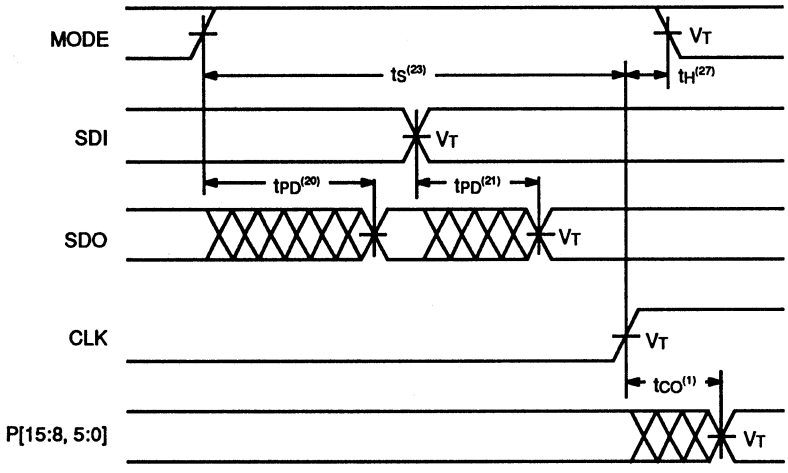
CLK to Output Disable/Enable



10135-060A

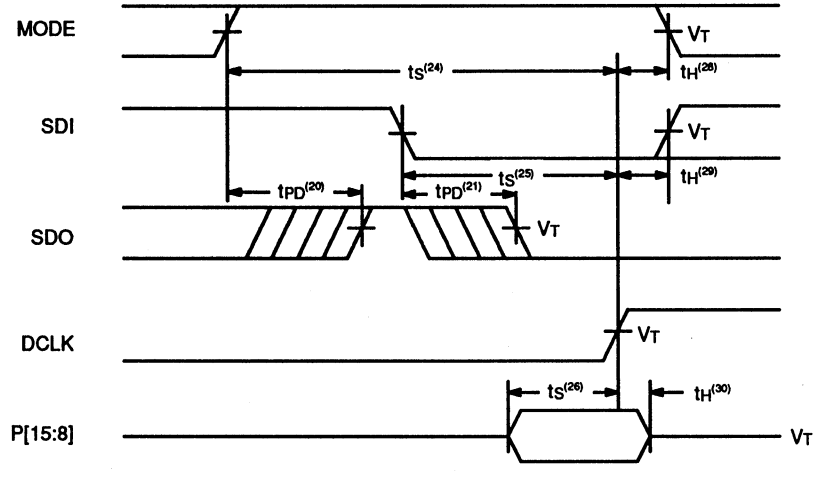
Clock Width/Period

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10135-061A

Load Pipeline Register from Shadow Register

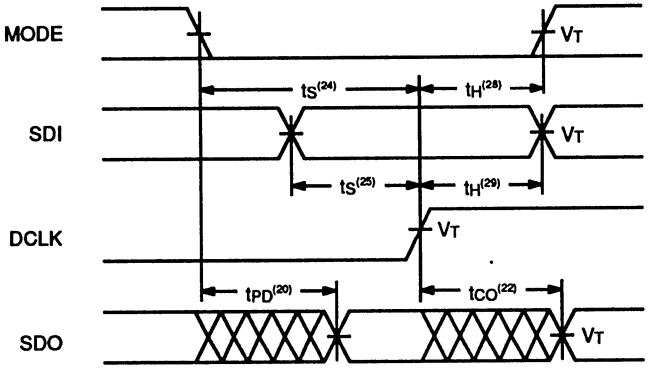


10135-062A

Load Shadow Register from Pipeline Register and/or Pins

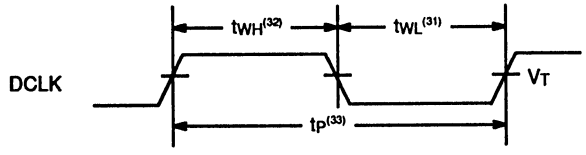
SWITCHING WAVEFORMS (Continued)

SSR Configuration



10135-063A

Shift Shadow Register



10135-064A

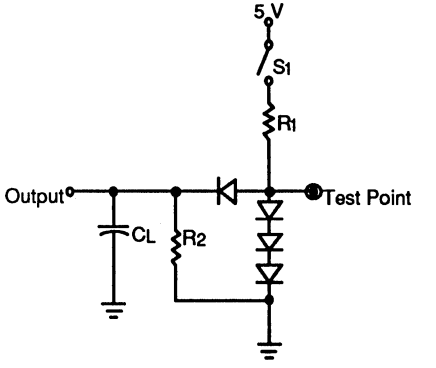
DCLK Width/Period

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

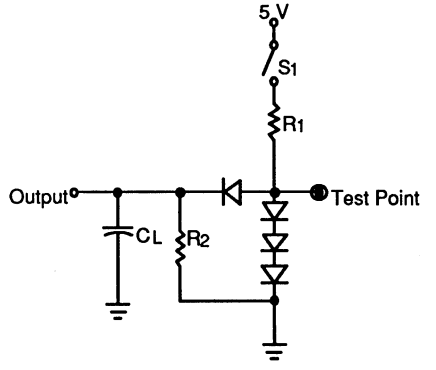
KS000010-PAL

SWITCHING TEST CIRCUIT



10135-053A

Three-State Outputs



10135-054A

Two-State Outputs

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	667 Ω	5 kΩ	667 Ω	5 kΩ	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Note:

Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω: t_r ≤ 2.5 ns.

TEST PHILOSOPHY AND METHODS

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in Vcc current as the device switches may cause erroneous function failures due to Vcc changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

7. Threshold Testing

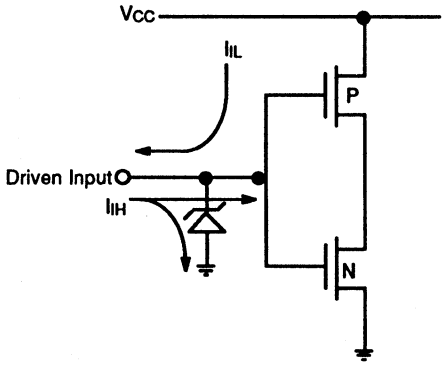
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

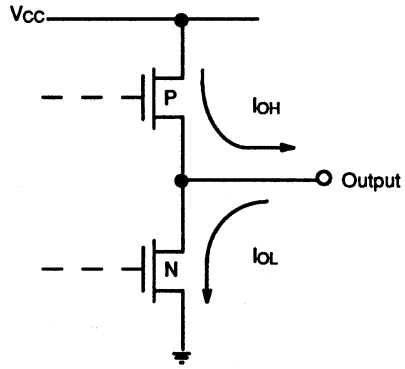
   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



10135-050A



10135-051A

Thermal Impedance Values (θ_{JA}), Typical	
28-Pin Plastic SKINNYDIP (PD3028)	50°C/W
28-Pin Windowed Ceramic SKINNYDIP (CDE028)	40°C/W
28-Pin Plastic Leaded Chip Carrier (PL 028)	55°C/W
28-Pin Windowed Ceramic Leadless Chip Carrier (CLV028)	55°C/W

APPROVED PROGRAMMERS (subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (713) 461-9430	Contact Manufacturer
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	System 29A, 29B LogicPak™ 303A-V04 Adapter 303A-011A-V08 Family/Pinout Codes: 94-7C UniSite™ rev. 2.4 (DIP) UniSite rev. 2.8 (PLCC)
Digelec Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Contact Manufacturer
JMC Hakusan High-Tech Park 807-1 Hakusan-Cho Midori-Ku Yokohama-City 226, Japan 045/939-6150	Contact Manufacturer
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020	ALLPRO™ rev. 1.49
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	Contact Manufacturer
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	
Sprint Expert International, Inc. 13720 Midway, Suite 105 Dallas, TX 75244 (214) 980-2896 or Vanderweydendreef 27 1900 Overijse, Belgium 2-687-4154	Contact Manufacturer
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire, United Kingdom AL7 1JT (707) 332148	System 3000 Rev. 7.0 Code: 94092
Systems General 244 S. Hillview Milpitas, CA 95035 (408) 263-6667 or 3F, No 6, Lane 4, Tun Hwa N. Rd. Taipei, Taiwan 2-721-2613	Contact Manufacturer

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DEVELOPMENT SYSTEMS (subject to change)

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Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	ABEL™ Software
ISDATA GmbH Haid-und-Neu-Str. 7 D-7500 Karlsruhe 1, West Germany 0721/69 30 92	LOG/iC™ Software
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	CUPL™ Software
Minc Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner™ Software
OrCAD Systems Corporation 1049 S.W. Baseline St., Suite 500 Hillsboro, OR 97123 (503) 640-9488	OrCAD/PLD™ Software
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	Acugen (Anvil) ATG™ Software
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLDtest Plus™ Software

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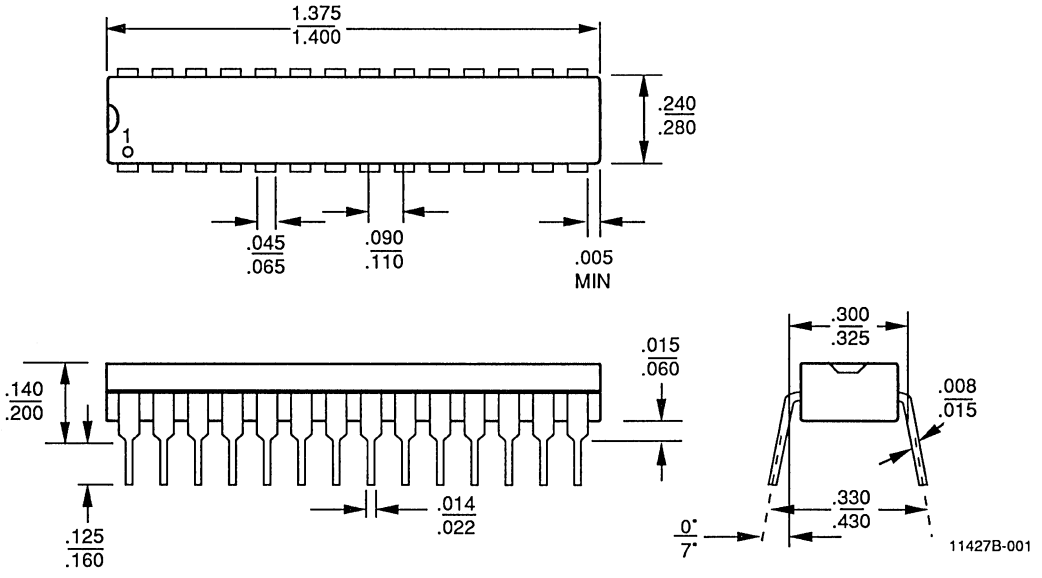
PHYSICAL DIMENSIONS

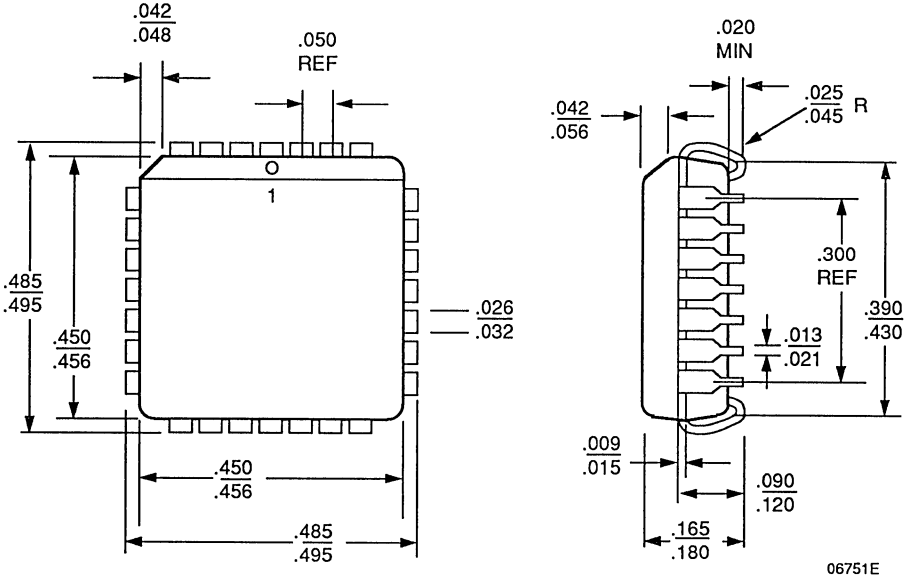
PD3028

28-Pin 300-mil PLASTIC SKINNYDIP



PL028

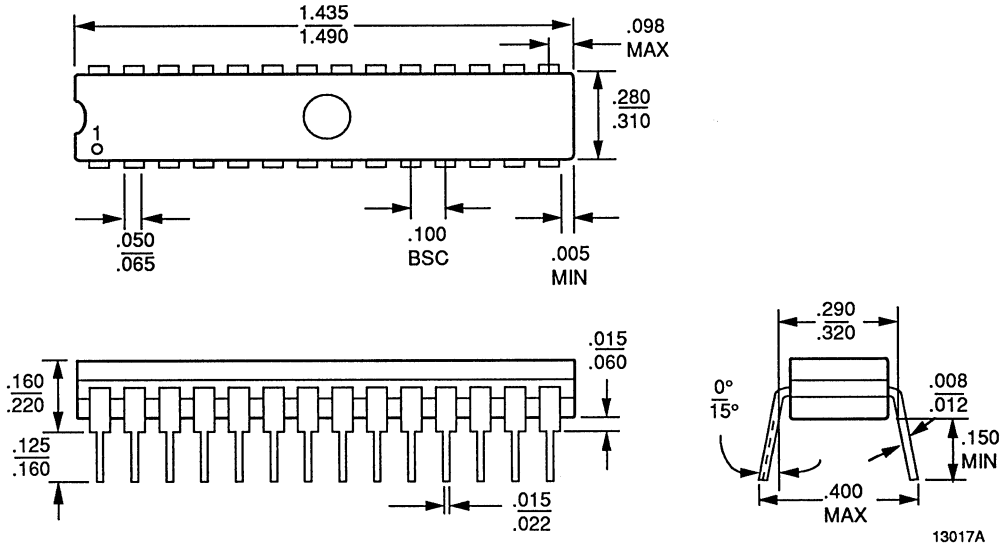
28-Pin Plastic Leaded Chip Carrier



PHYSICAL DIMENSIONS (Continued)

CDE028

28-Pin 300-mil Ceramic Windowed SKINNYDIP



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