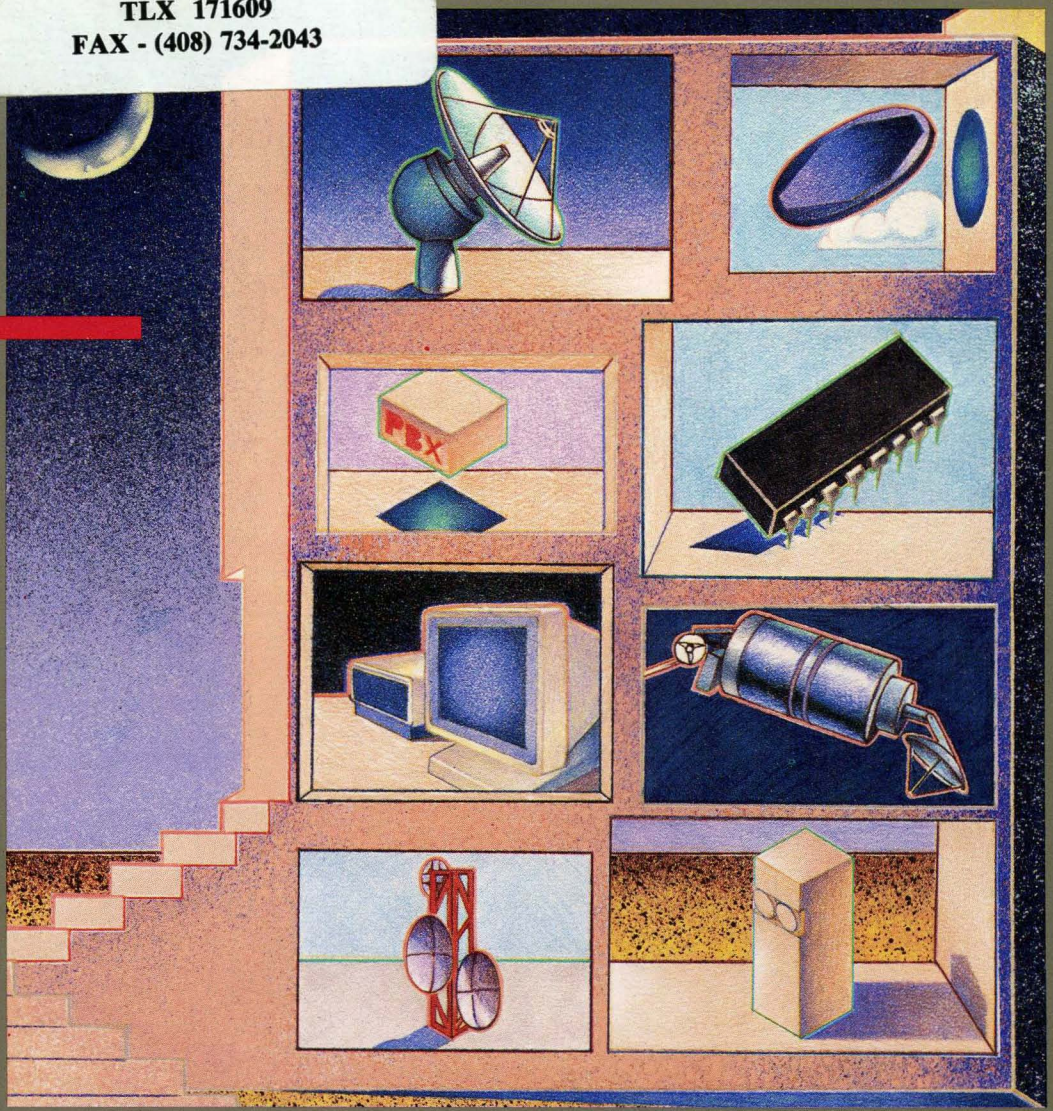
Data Book

AT&T

Communication Devices



AT&T

January 1987

1987

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The following AT&T trademarks are mentioned in this data book:

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Data sheets without a status marking are final and are issued when tool made samples are approved or when the product is delivered for usage, whichever occurs first. The other data sheet status markings used throughout this catalog are defined as:

ADVANCE – Issued at the exploratory stage of development when the principle characteristics are available. Some functional characteristics are subject to change.

PRELIMINARY – Issued after development for manufacture has been started. Some electrical and timing parameters are subject to change.

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1987 COMMUNICATION DEVICES DATA BOOK

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ALPHANUMERIC INDEX

INTRODUCTION

For more than a century, AT&T has set the standard for information exchange. AT&T innovation and excellence have created the most extensive, efficient, and reliable communications system in the world. This sophisticated voice and data communication system demands components of superior technology, quality, and reliability.

AT&T manufactures integrated circuits specifically designed to meet the needs of the communications market. The strong research and design capabilities of AT&T Bell Laboratories, combined with the high volume, high quality manufacturing capabilities of AT&T Technology Systems, allow us to maintain the leading edge in advanced technology devices.

In this new Information Age, the telephone and the computer are becoming one, and AT&T is building upon this merger with new products and services. New devices have been developed to interface these two complex fields into a highly flexible and reliable network. This catalog contains the technical information on devices used for switching, analog and digital transmission, data transmission and protocol control, integrated services digital network (ISDN) interfacing, and signal processing.

QUALITY AND RELIABILITY

AT&T standards and stringent processing controls, along with the design and construction techniques developed at AT&T Bell Laboratories, ensure the excellent quality and reliability of AT&T devices. Laboratory tests and field failure data confirm that high quality, reliable products are produced at the component, circuit pack/board, and system levels. Devices are tested by a comparison of the actual electrical, mechanical, or visual properties of the device against what is specified to the user or what is specified as a manufacturing requirement. Quality is determined at a single point in time; reliability is ascertained over a longer period of time.

The engineering quality control (QC) and final inspection (FI) organizations located at each integrated circuit (IC) manufacturing plant perform the actual inspection and testing of devices. After the products have been inspected, the resident quality assurance (QA) organizations audit the results of the tests to determine acceptability. Quality is usually stated in terms of the number of defects contained in an IC population.

Various mechanical tests are performed to ensure the integrity of internal lead bonds and the strength of exterior leads. Packages are visually inspected during assembly to check for defects such as poor alignment of bonds or damaged wires that could be a reliability risk. Assembly shop tests are then repeated by QA and FI on a sample of devices prior to shipment. Tests performed include worst-case conditions, speed, leakage, power supply current, etc. The tests are usually performed at room temperature and/or elevated temperature.

Operational life testing (OLT) is a method of testing for reliability using simulated worst-case field conditions. Mechanical and electrical stress conditions beyond normal specifications are applied to accelerate latent manufacturing defects. Effective screens for mechanical problems are thermal cycling and hot testing, since some mechanical defects are only minimally affected by accelerated stress conditions.

HANDLING AND MOUNTING

AT&T products have long life expectancy with a corresponding low failure rate when handling and operating specifications are followed by the user. Operating specifications include product mounting, use, operating limits, power requirements, environmental conditions, and other items specific to the product.

Device temperature specifications are usually given as T_A (temperature ambient).

Precaution against static discharge must always be observed since devices may be damaged or destroyed by electrostatic discharge. This includes grounding all personnel and equipment before contact with static-sensitive devices. Circuit packs/boards must be shipped in conductive plastic bags and stored in conductive plastic bags until used. Nonconductive plastic foam or boxes must never be used for device storage.

Integrated circuit devices may be inserted directly into printed circuit boards and mounted in any position. It is acceptable to bend the leads on the opposite side of the board to facilitate assembly. The devices may be soldered to printed circuit boards or inserted into sockets. The devices are not intended for spring-type socket insertion.

In assembly, the device solder bath (fountain) temperature should not exceed 300 °C for a maximum bath time limited to 10 seconds unless otherwise stated. For installation with a soldering iron, the iron temperature (tip) should not exceed 500 °C, and solder time per lead should be limited to 5 seconds unless otherwise stated.

Following completion of assembly and soldering operations, all printed wiring assemblies should be cleaned to remove fingerprints, dust, dirt, grease, excessive flux residue, and other foreign matter. A brush cleaning process using solvents is an acceptable cleaning method, provided only occasional isolated droplets of solvent come in contact with the devices and the component side of the board. The recommended solvents are chlorinated hydrocarbons such as trichloroethylene, 1,1,1-trichloroethane, and perchloroethylene.

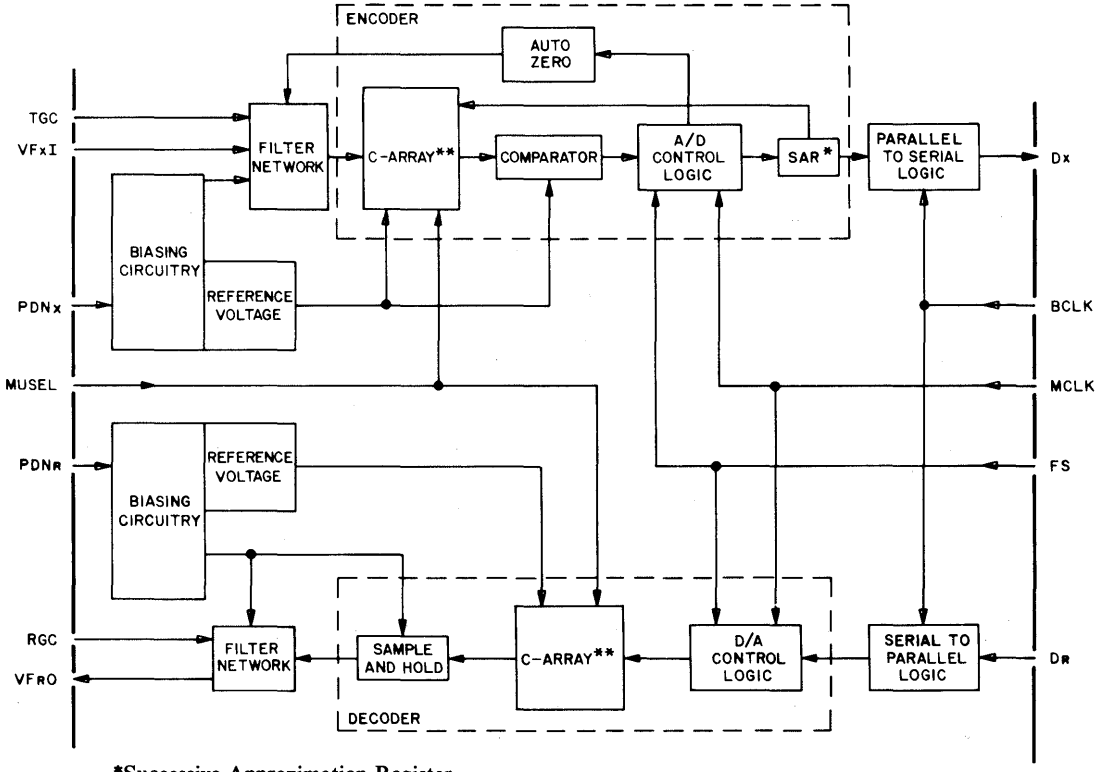
Where aggressive fluxes are employed in assembly of printed wiring, total immersion cleaning with high velocity spraying of aqueous solution or solvents such as fluorinated azeotrope is required. Stringent requirements must be placed on the cleanliness of the assemblies to assure removal of ionic residues.

FEATURES

- AT&T/CCITT compatible
- Pin-selectable μ-law or A-law operation
- Pin-selectable transmit and receive gain
- Variable data rate (128 kHz to 4.096 MHz)
- On-chip voltage reference
- TTL-compatible I/O
- No external components required
- ±5 V supply
- Latch-up free CMOS technology
- Low power dissipation
  - 20 mW typical power-down
  - 80 mW typical operation

DESCRIPTION

The T7500 PCM Codec With Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion, as well as the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed system. The T7500 device is available in an 18-pin plastic DIP or a 20-pin plastic small-outline J (SOJ) package for surface mounting.



*Successive Approximation Register
**Capacitor Array

Figure 1. T7500 PCM Codec With Filters Block Diagram

USER INFORMATION

Pin Descriptions

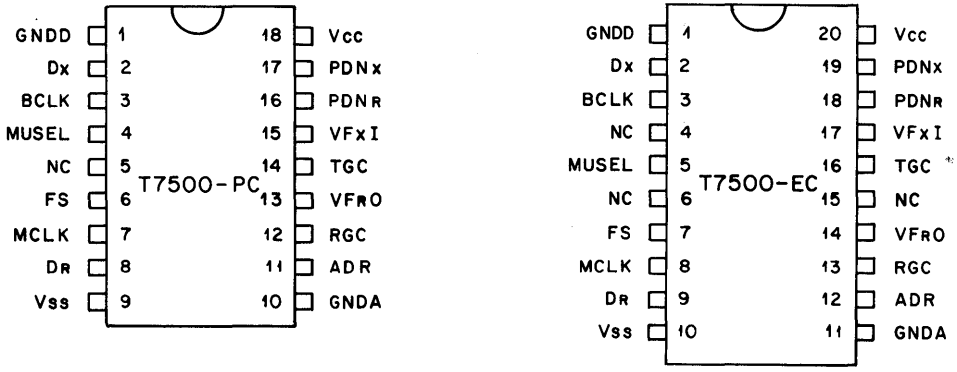


Figure 2. T7500 18-Pin Plastic DIP and 20-Pin Plastic SOJ Pin Function Diagrams

Table 1. T7500 Pin Descriptions

Symbol	Type	Name/Function
GNDD	–	**Ground (Digital).**
DX	O	**Data Transmit.** Eight-bit μ-law or A-law PCM inverted binary output.
BCLK	I	**Bit Clock.** PCM is transmitted and received at a rate defined by this input clock (128 kHz – 4.096 MHz).
MUSEL	I	**μ-law Select.** A high (1) or no connection on this pin results in μ-law conversion. Apply a low (0) to this pin for A-law encodings.
NC	–	**No Connection.**
FS	I	**Frame Synchronization.** An 8 kHz timing pulse is applied to this pin to initiate A/D and D/A conversion processes.
MCLK	I	**Master Clock.** 2.048 MHz
DR	I	**Data Receive.** This is the 8-bit μ-law or A-law PCM inverted binary input.
VSS	–	**–5 V Supply (±5%).**
GNDA	–	**Ground (Analog).**

Table 1. T7500 Pin Descriptions (Continued)		
Symbol	**Type**	**Name/Function**
ADR	I	**Address.** A low (0) or no connection on this pin enables the FS pulse. It is used for channel selection when more than one codec is used on a PCM bus.
RGC	I	**Receive Gain Control.** A low (0) or no connection on this pin sets the gain to 0 dB (0 output TLP); a high (1) on this pin sets the receive gain to +3 ±0.1 dB (+3 output TLP). When high, the gain is set with respect to the gain measured at 0 dB setting.
VFRO	O	**Voice Frequency Receive Output.** The maximum load permitted on this pin is 20 kΩ in parallel with 50 pF.
TGC	I	**Transmit Gain Control.** A high (1) or no connection on this pin sets the transmit gain to 0 dB (0 input TLP); a low (0) sets the transmit gain to −3 ±0.1 dB (+3 input TLP). When low, the gain is set with respect to the gain measured at 0 dB setting.
VFXI	I	**Voice Frequency Transmit Input.** Analog input to the transmit filters. The input impedance on this pin is greater than 400 kΩ.
PDNR	I	**Power-Down Receive.** A high (1) on this pin causes power-down of receive side. During receive-side power-down, VFRO is grounded through a low impedance and the receive-side analog circuitry is disabled. A low (0) or no connection allows normal receive-side operation.
PDNX	I	**Power-Down Transmit.** A high (1) on this pin causes power-down of transmit side. A transmit power-down causes the DX buffer to go into a high-impedance state and all encoder analog circuitry to be disabled. A low (0) or no connection allows normal transmit-side operation.
VCC	–	**5 V Supply (±5%).**

Overview

The T7500 PCM Codec is a synchronous device with a common master clock and synchronization input that drives both the transmit and receive sections. Device operation requires three logic inputs: MCLK, FS, and BCLK.

On power-up, the codec becomes active only after receiving a FS and ADR signal. The serial transfer of data to DR and from DX proceeds at a rate determined by BCLK (see Figure 4).

The digital output returns to a high-impedance state upon completion of this process and remains in this state until another set of synchronization and address signals is received. This allows the device to be used with a shared PCM bus (up to 64 channels at 4.096 MHz).

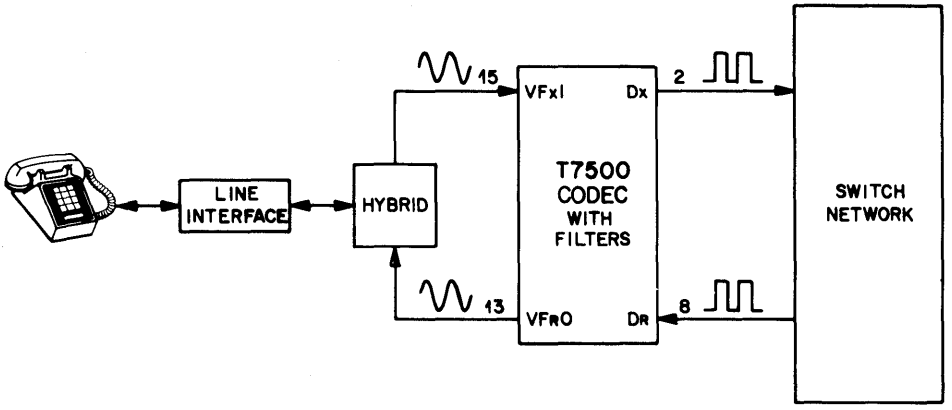


Figure 3. PCM System Block Diagram

The T7500 Codec has a power-down mode that reduces power consumption and heat dissipation when device operation is not required. Two pins are used for this power-down option. A high (1) applied to PDNR disables the receive side of the device; PDNX performs the same function on the transmit side of the device. Each side can be independently disabled. When the receive side is powered down, output VFRO is grounded through a low impedance and all receive-side analog circuitry is disabled. Transmit power-down results in output DX going into a high-impedance state and all transmit-side analog circuitry being disabled. The device is activated by applying a low (0) to both leads.

This device implements either μ-law or A-law PCM encoding. MUSEL is used to determine the type of encoding. Inverted binary format is used for μ-law encoding. Alternate digit inversion is used for A-law transmission.

Separate gain controls provide gain settings for the transmit and receive sections. Either 0 dB or −3 dB gain can be selected for the transmit side and either 0 dB or +3 dB for the receive side.

On-chip voltage referencing is provided, eliminating the need for external circuitry and gain trimming.

CHARACTERISTICS

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%; V_{SS} = −5 V ± 5%; GNDA = 0 V; GNDD = 0 V; OTLP, unless otherwise specified. Typical values are for T_A = 25 °C and nominal power supply values.

Digital Interface

Symbol	Parameter	Min	Max	Unit	Test Condition
I_{IL}	Low-Level Input Current	−20	–	μA	$GNDD \leq V_{IN} \leq V_{IL}$
I_{IH}	High-Level Input Current	–	20	μA	$V_{IH} \leq V_{IN} \leq V_{CC}$
V_{IL}	Input Low Voltage	–	0.8	V	–
V_{IH}	Input High Voltage	2.0	–	V	–
V_{OL}	Output Low Voltage	–	0.4	V	–
V_{OH}	Output High Voltage	2.4	–	V	–
C_I	Digital Input Capacitance	–	5	pF	–
I_L	Output Leakage Current	−50	50	μA	–

Power Dissipation

All measurements made at fBCLK = 2.048 MHz, outputs loaded.

Symbol	Parameter	Min	Typ	Max	Unit
I_{CC1}	V_{CC} Operating Current	–	8.5	15	mA
I_{SS1}	V_{SS} Operating Current	–	−7.5	−13	mA
I_{CC0}	V_{CC} Power-Down Current	–	2.0	7.0	mA
I_{SS0}	V_{SS} Power-Down Current	–	−2.0	−4.0	mA
V_{CC}	Positive Operating Voltage	4.75	5	5.25*	V
V_{SS}	Negative Operating Voltage	−4.75	−5	−5.25*	V
P_1	Operating Power Dissipation	–	80	147	mW
P_0	Power-Down Dissipation	–	20	55	mW

*Absolute maximum ratings are V_{CC} = 7.5 V, V_{SS} = −7.5 V. Exceeding these values may result in permanent internal damage.

Analog Interface – Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit
R_I	Input Resistance @ VFXI	0.4	1.1	–	MΩ
V_{OFF}	Input Offset Voltage @ VFXI	–	–	20	mV
C_L	Load Capacitance @ VFXI	–	20	40	pF

Analog Interface – Receive Filter Driver Amplifier Stage

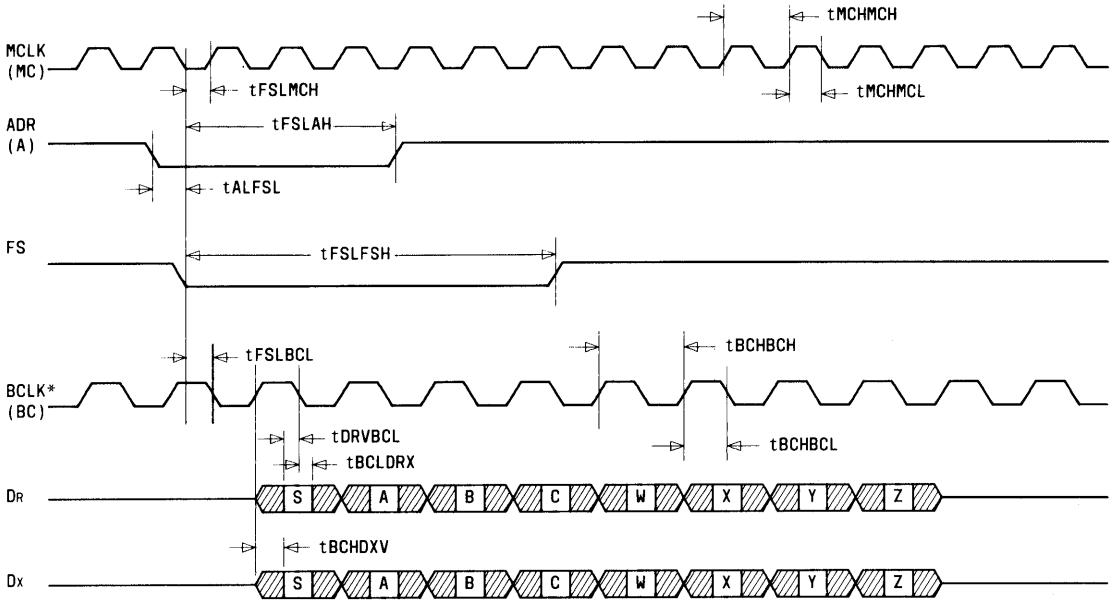
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
RO	Output Resistance @ VFRO for Voice Frequencies	–	50	–	Ω	–
VOFF	Output DC Offset @ VFRO	–	50	–	mV	Relative to GNDA
CL	Load Capacitance @ VFRO	–	–	50	pF	–
VO	Maximum Voltage Output Swing across RL, μ-law (A-law)	−2.229 (−2.229)	–	2.229 (2.229)	V	RGC = High (+3 TLP)
		−1.578 (−1.572)	–	1.578 (1.572)	V	RGC = Low (0 TLP)
RL	Load Resistance @ VFRO	20	–	–	kΩ	–

Timing Characteristics

Clock Section					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
tBCHBCH[1]	Bit Clock Period	.244	–	7.8	μs
tBCHBCL	Bit Clock Pulse Width	.4tBCHBCH	.5tBCHBCH	.6tBCHBCH	–
tMCHMCH[2]	Master Clock Period	–	488	–	ns
tMCHMCL	Master Clock Pulse Width	.4tMCHMCH	.5tMCHMCH	.6tMCHMCH	–
Data Section					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
tFSLMCH	Sync Set-Up Time Ref MC	90	.5tMCHMCH	tMCHMCH	ns
tFSLAH[3]	Address Hold Time	1.5tBCHBCH	3tBCHBCH	–	–
tALFSL	Address Set-Up Time	10	.5tBCHBCH	–	ns
tFSLFSH[4]	Sync Pulse Width	1.5tBCHBCH	2tBCHBCH	63	μs
tFSLBCL	Sync Set-Up Time	75	200	tBCHBCH−50	ns
tDRVBCL	DR Set-Up Time	50	200	–	ns
tBCLDRX	DR Hold Time	50	300	–	ns
tBCHDXV[5]	DX Delay Time	30	80	150	ns

[1]BCLK ranges from 128 kHz to 4.096 MHz.
[2]2.048 MHz.
[3]Max = constant low.
[4]Negative logic sense.
[5]DX max load ≤ 300 pF plus 1 medium-power TTL load.

Timing Diagram



* BCLK RANGES FROM 128 KHz TO 4.096 MHz, IT DETERMINES ADR, FS, DR, AND DX TIMING

Figure 4. I/O Timing

AC Characteristics – Transmission Parameters

Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
GE	Encoder Milliwatt Response (Transmit Gain Tolerance)					Signal input = .7746 Vrms
	μ-law	−0.15	± 0.08	0.15	dBm0	VCC and VSS are ± 5 %
	A-law	−0.18	±0.08	±0.18	dBm0	TA = 0 to 70 °C
GD	Digital Milliwatt Response (Receive Gain Tolerance)					
	μ-law	−0.15	±0.08	0.15	dBm0	VCC and VSS are ± 5 %
	A-law	−0.18	±0.08	0.18	dBm0	TA = 0 to 70 °C

Gain Tracking – Reference Level = 1.02 kHz, 0 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
GTX_{μ}	Transmit Gain Tracking Error: Sinusoidal Input, μ-law	−0.25 −0.50	0.25 0.50	dB dB	3 to −37 dBm0 −37 to −50 dBm0
GTXA	Transmit Gain Tracking Error: Sinusoidal Input, A-law	−0.25 −0.50	0.25 0.50	dB dB	3 to −37 dBm0 −37 to −50 dBm0
GTR_{μ}	Receive Gain Tracking Error: Sinusoidal Input, μ-law	−0.25 −0.50	0.25 0.50	dB dB	3 to −37 dBm0 −37 to −50 dBm0
GTRA	Receive Gain Tracking Error: Sinusoidal Input, A-law	−0.25 −0.50	0.25 0.50	dB dB	3 to −37 dBm0 −37 to −50 dBm0

Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
DXS	Transmit Signal to Distortion: Sinusoidal Input, μ-law (A-law)	36(35) 30(29) 25(25)	–	–	dB dB dB	$0 \leq$ VFXI ≤ -30 dBm0 −40 dBm0 −45 dBm0 (Input = 1.02 kHz)
DRS	Receive Signal to Distortion: Sinusoidal Input, μ-law (A-law)	36(35) 30(29) 25(25)	–	–	dB dB dB	$0 \leq$ DR ≤ -30 dBm0 −40 dBm0 −45 dBm0 (Input = 1.02 kHz)
DXSF	Transmit Single Frequency: Distortion Products	–	–	−28 −40	dBm0 dBm0	$0 \leq$ Input $\leq$ 2 MHz .2 $\leq$ Input $\leq$ 3.4 kHz
DRSF	Receive Single Frequency: Distortion Products	–	–	−28 −40	dBm0 dBm0	$0 \leq$ Input $\leq$ 2 MHz .2 $\leq$ Input $\leq$ 3.4 kHz
DXD	Transmit Absolute Delay	–	340	–	μs	–
DRD	Receive Absolute Delay	–	240	–	μs	–
DDAA	Delay Distortion: Analog-to-Analog	–	250 60 20 20 50 220	–	μs μs μs μs μs μs	f = 500 Hz f = 1 kHz f = 1.5 kHz f = 2 kHz f = 2.5 kHz f = 3 kHz

Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
FXC	Transmit Idle Channel Noise: C-Message Weighted	—	14	18 23	dBrnC0 dBrnC0	μ-law A-law
FRC	Receive Idle Channel Noise: C-Message Weighted	—	9	13 15	dBrnC0 dBrnC0	μ-law A-law
FXP	Transmit Idle Channel Noise: Phosphometric Weighted	—	−69	−67	dBm0p	—
FRP	Receive Idle Channel Noise: Phosphometric Weighted	—	−81	−75	dBm0p	—
PSRXCC	VCC Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at DX
PSRXSS	VSS Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at DX
PSRRCC	VCC Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz at VFRO
PSRRSS	VSS Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz at VFRO
FCXR	Crosstalk: Transmit to Receive, Single-Ended Outputs, μ-law (A-law)	—	—	−71 (−70)	dB	VFXI = 0 dBm0; 1.02 kHz signal measured at VFRO; DR = idle code
FCRX	Crosstalk: Receive to Transmit, Single-Ended Outputs, μ-law (A-law)	—	—	−71 (−70)	dB	DR = 0 dBm0; VFXI = GNDA; 1.02 kHz signal measured at DX

Transmit Filter Transfer Characteristics

Transmit Gain Relative to Gain at 1.02 kHz (GRX)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
16.67 Hz	–	−35	−30	dB
50 Hz	–	−33	−30	dB
60 Hz	–	−40	−30	dB
200 Hz	−1.8	−0.5	0	dB
300 to 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	0.01	0.125	dB
3380 Hz	−0.885	−0.7	0.015	dB
3980 Hz	–	−15.6	−13.3	dB
4600 Hz and above	–	–	−32	dB

*0 dBm0 signal input at VFXI.

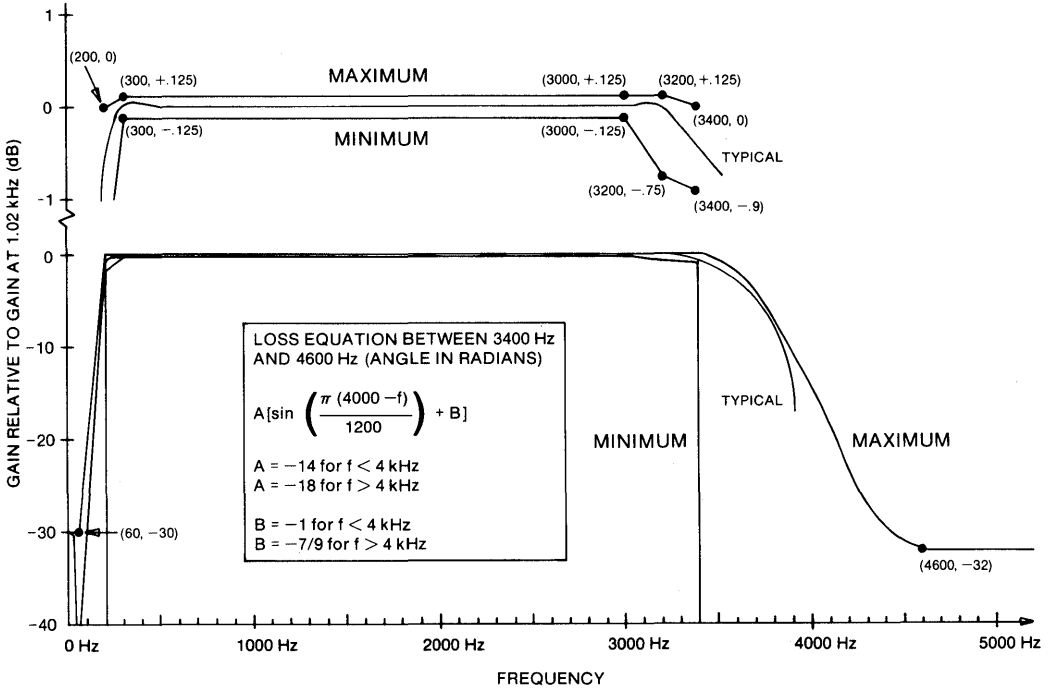


Figure 5. Transmit Filter Characteristics

Receive Filter Transfer Characteristics

Receive Gain Relative to Gain at 1.02 kHz (GRR)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
Below 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	±0.04	0.125	dB
3380 Hz	−0.885	−0.58	−0.015	dB
3980 Hz	–	−15.7	−13.3	dB
4600 Hz and above	–	–	−28	dB

*0 dBm0 signal input at DR.

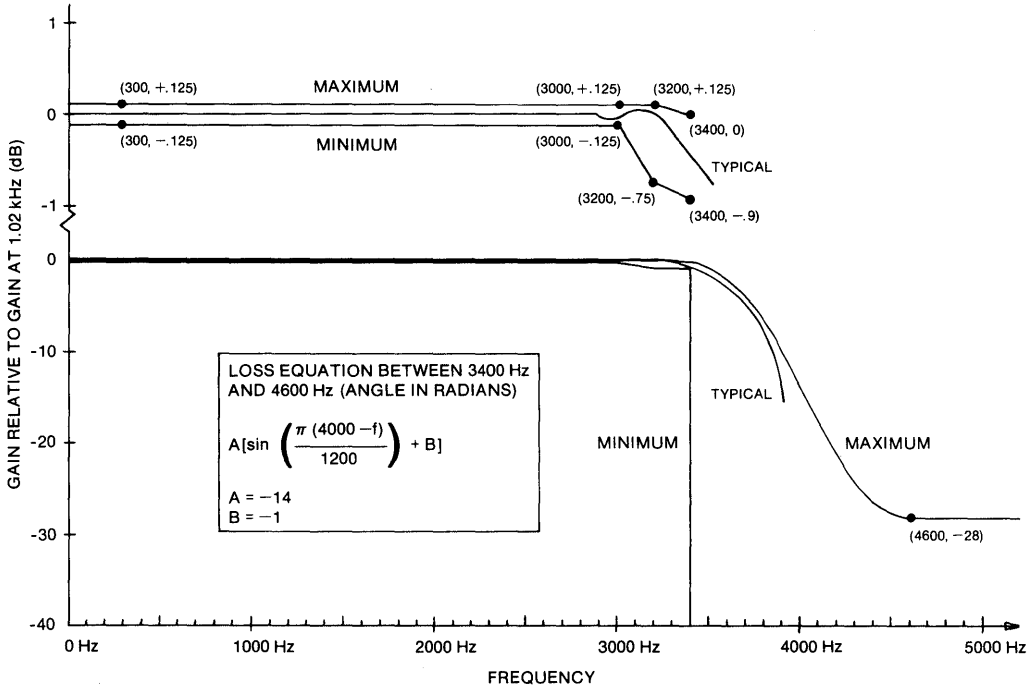


Figure 6. Receive Filter Characteristics

FEATURES

- AT&T/CCITT compatible
- Pin-selectable μ-law or A-law operation
- Pin-selectable transmit and receive gain
- Variable data rate (128 kHz to 4.096 MHz)
- On-chip voltage reference
- TTL-compatible I/O
- No external components required
- ± 5 V supply
- Latch-up free CMOS technology
- Low power dissipation
  - 20 mW typical power-down
  - 80 mW typical operation

DESCRIPTION

The T7501 PCM Codec With Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion, as well as the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed system. The T7501 device is available in an 18-pin plastic DIP or a 20-pin plastic small outline J (SOJ) package for surface mounting.

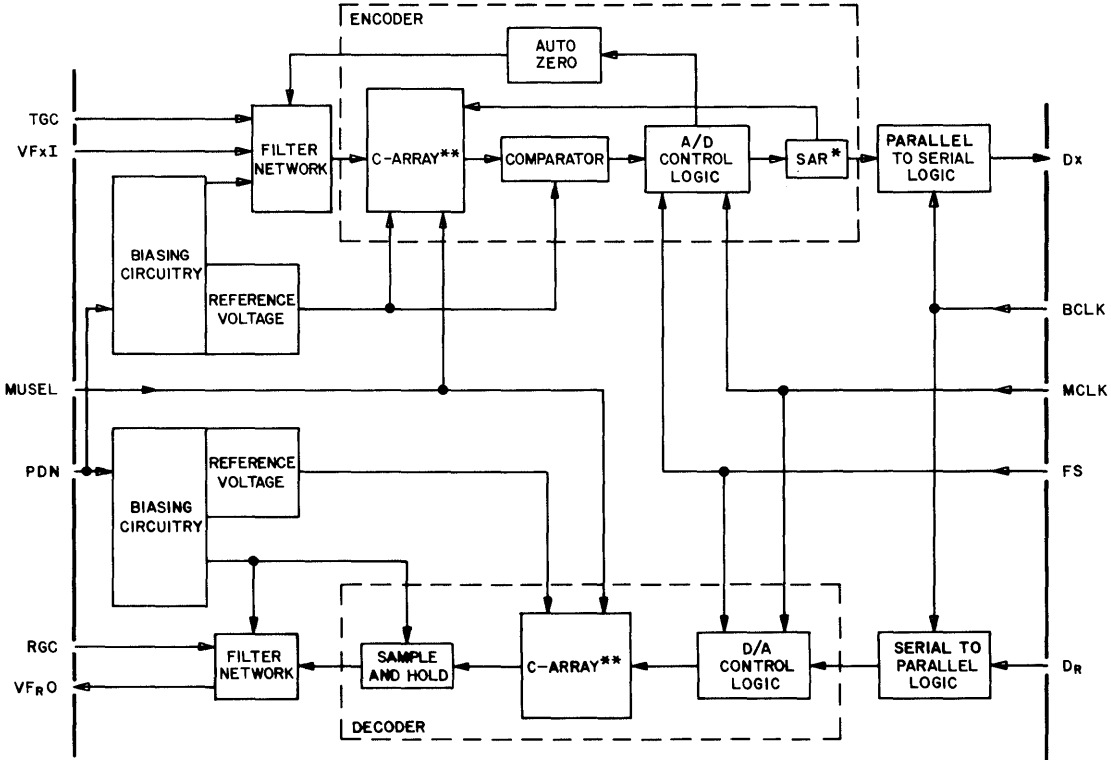


Figure 1. T7501 PCM Codec With Filters Block Diagram

USER INFORMATION

Pin Descriptions

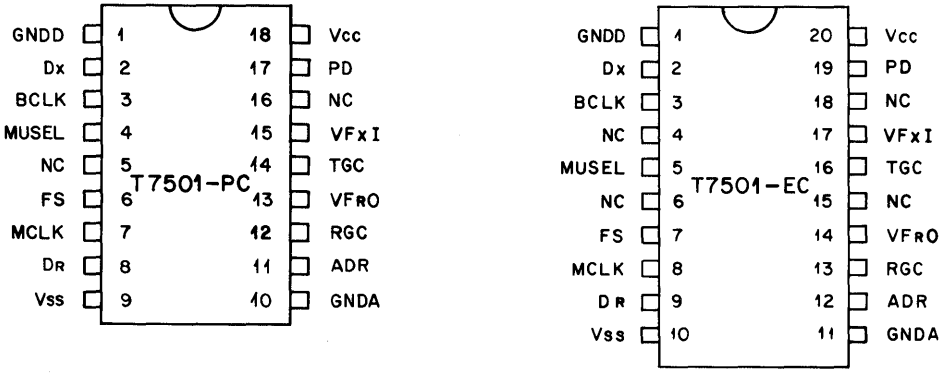


Figure 2. T7501 18-Pin Plastic DIP and 20-Pin Plastic SOJ Pin Function Diagrams

Table 1. T7501 Pin Descriptions

Symbol	Type	Name/Function
GNDD	—	**Ground (Digital).**
DX	O	**Data Transmit.** Eight-bit μ-law or A-law PCM inverted binary output.
BCLK	I	**Bit Clock.** PCM is transmitted and received at a rate defined by this input clock (128 kHz — 4.096 MHz).
MUSEL	I	**μ-Law Select.** A high (1) or no connection on this pin results in μ-law conversion. Apply a low (0) to this pin for A-law encodings.
NC	—	**No Connection.**
FS	I	**Frame Synchronization.** An 8 kHz timing pulse is applied to this pin to initiate A/D and D/A conversion processes.
MCLK	I	**Master Clock.** 2.048 MHz
DR	I	**Data Receive.** This is the 8-bit μ-law or A-law PCM inverted binary input.
VSS	—	**−5 V Supply (± 5%).**
GNDA	—	**Ground (Analog).**

Table 1. T7501 Pin Descriptions (Continued)		
Symbol	**Type**	**Name/Function**
ADR	I	**Address.** A low (0) on this pin enables the FS pulse. It is used for channel selection when more than one codec is used on a PCM bus. A high (1) or no connection on this pin disables FS.
RGC	I	**Receive Gain Control.** A low (0) on this pin sets the gain to 0 dB (0 output TLP); a high (1) or no connection on this pin sets the receive gain to +3 ±0.1 dB (+3 output TLP). When high, the gain is set with respect to the gain measured at 0 dB setting.
VFRO	O	**Voice Frequency Receive Output.** The maximum load permitted on this pin is 20 kΩ in parallel with 50 pF.
TGC	I	**Transmit Gain Control.** A high (1) or no connection on this pin sets the transmit gain to 0 dB (0 input TLP); a low (0) sets the transmit gain to −3 ±0.1 dB (+3 input TLP). When low, the gain is set with respect to the gain measured at the 0 dB setting.
VFXI	I	**Voice Frequency Transmit Input.** Analog input to the transmit filters. The input impedance on this pin is greater than 400 kΩ.
NC	—	**No Connection.**
PD	I	**Power-Down.** A high (1) or no connection on this pin causes power-down. The power-down causes the DX buffer to go into a high-impedance state and all encoder analog circuitry to be disabled, VFRO to be grounded through a low impedance, and the receive-side analog circuitry to be disabled. A low (0) allows normal transmit and receive operation.
VCC	—	**5 V Supply (±5%).**

Overview

The T7501 PCM Codec is a synchronous device with a common master clock and synchronization input that drives both the transmit and receive sections. Device operation requires three logic inputs: MCLK, FS, and BCLK.

On power-up, the codec becomes active only after receiving a FS and ADR signal. The serial transfer of data to DR and from DX proceeds at a rate determined by BCLK (see Figure 4).

The digital output returns to a high-impedance state upon completion of this process and remains in this state until another set of synchronization and address signals is received. This allows the device to be used with a shared PCM bus (up to 64 channels at 4.096 MHz).

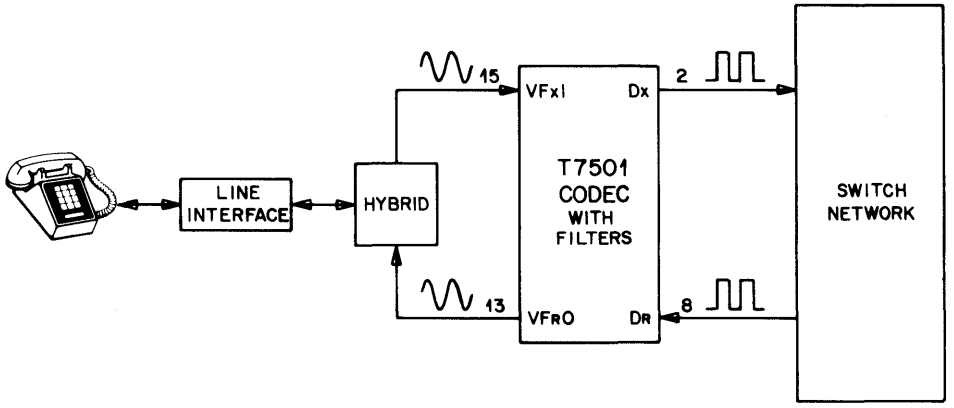


Figure 3. PCM System Block Diagram

The T7501 Codec has a power-down mode that reduces power consumption and heat dissipation when device operation is not required. A logic 1 applied to PD disables the receive and transmit functions of the device. When the device is powered down, output VFRO is grounded through a low impedance and all receive-side analog circuitry is disabled. Transmit power-down results in output DX going into a high-impedance state and all transmit-side analog circuitry being disabled.

A low (0) applied to PD activates the device. The analog transmit circuitry requires a setting time of 50 ms to guarantee that the DC offset will be less than 16 least significant bits. The 16 LSBs correspond to the first μ-law chord boundary.

This device implements either μ-law or A-law PCM encoding. MUSEL is used to determine the type of encoding. Inverted binary format is used for μ-law encoding. Alternate digit inversion is used for A-law transmission.

Separate gain controls provide gain settings for the transmit and receive sections. Either 0 dB or -3 dB gain can be selected for the transmit side and either 0 dB or +3 dB for the receive side.

On-chip voltage referencing is provided, eliminating the need for external circuitry and gain trimming.

CHARACTERISTICS

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 ± 5%; V_{SS} = -5 V ± 5%; GNDA = 0 V; GNDD = 0 V; OTLP, unless otherwise specified. Typical values are for T_A = 25 °C and nominal power supply values.

Digital Interface

Symbol	Parameter	Min	Max	Unit	Test Condition
I_{IL}	Low-Level Input Current	−20	—	μA	GNDD ≤ V_{IN} ≤ V_{IL}
I_{IH}	High-Level Input Current	—	20	μA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.0	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	—
V_{OH}	Output High Voltage	2.4	—	V	—
C_I	Digital Input Capacitance	—	5	pF	—
I_L	Output Leakage Current	−50	50	μA	—

Power Dissipation

All measurements made at fBCLK = 2.048 MHz, outputs loaded.

Symbol	Parameter	Min	Typ	Max	Unit
I_{CC1}	V_{CC} Operating Current	—	8.5	15	mA
I_{SS1}	V_{SS} Operating Current	—	−7.5	−13	mA
I_{CC0}	V_{CC} Power-Down Current	—	2.0	7.0	mA
I_{SS0}	V_{SS} Power-Down Current	—	−2.0	−4.0	mA
V_{CC}	Positive Operating Voltage	4.75	5	5.25*	V
V_{SS}	Negative Operating Voltage	−4.75	−5	−5.25*	V
P_1	Operating Power Dissipation	—	80	147	mW
P_0	Power-Down Dissipation	—	20	55	mW

*Absolute maximum ratings are V_{CC} = 7.5 V, V_{SS} = −7.5 V. Exceeding these values may result in permanent internal damage.

Analog Interface – Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit
R_I	Input Resistance @ VFxI	0.4	1.1	—	MΩ
V_{OFF}	Input Offset Voltage @ VFxI	—	—	20	mV
C_L	Load Capacitance @ VFxI	—	20	40	pF

Analog Interface – Receive Filter Driver Amplifier Stage

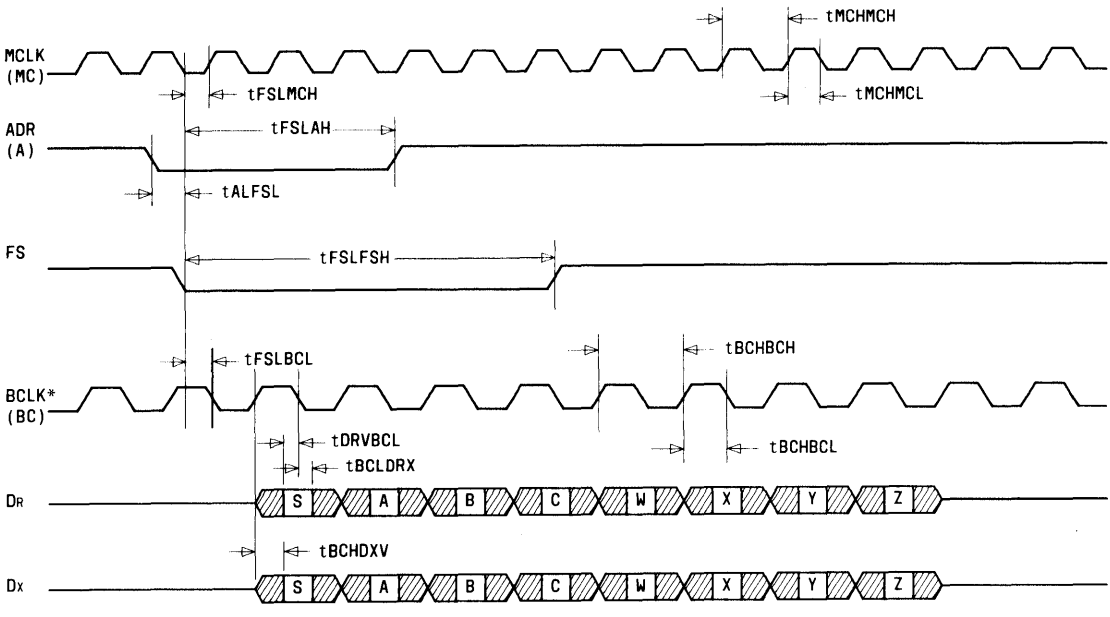
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
RO	Output Resistance @ VFRO for Voice Frequencies	–	50	–	Ω	–
VOFF	Output DC Offset @ VFRO	–	50	–	mV	Relative to GNDA
CL	Load Capacitance @ VFRO	–	–	50	pF	–
VO	Maximum Voltage Output Swing across RL, μ-law (A-law)	−2.229 (−2.229)	–	2.229 (2.229)	V	RGC = High (+3 TLP)
		−1.578 (−1.572)	– –	1.578 (1.572)	V	RGC = Low (0 TLP)
RL	Load Resistance @ VFRO	20	–	–	kΩ	–

Timing Characteristics

Clock Section					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
tBCHBCH[1]	Bit Clock Period	.244	–	7.8	μs
tBCHBCL	Bit Clock Pulse Width	.4tBCHBCH	.5tBCHBCH	.6tBCHBCH	–
tMCLMCL[2]	Master Clock Period	–	488	–	ns
tMCLMCH	Master Clock Pulse Width	.4tMCLMCL	.5tMCLMCL	.6tMCLMCL	–
Data Section					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
tFSLMCL	Sync Set-Up Time Ref MC	90	.5tMCLMCL	tMCLMCL	ns
tFSLAH[3]	Address Hold Time	1.5tBCHBCH	–	–	–
tALFSL	Address Set-Up Time	10	.5tBCHBCH	–	ns
tFSLFSH[4]	Sync Pulse Width	1.5tBCHBCH	2tBCHBCH	63	μs
tFSLBCL	Sync Set-Up Time	75	200	tBCHBCH−50	ns
tDRVBCL	DR Set-Up Time	50	200	–	ns
tBCLDRX	DR Hold Time	50	200	–	–
tBCHDXV[5]	DX Delay Time	30	80	150	ns

[1]BCLK ranges from 128 kHz to 4.096 MHz.
[2]2.048 MHz.
[3]Max = constant low.
[4]Negative logic sense.
[5]DX max load ≤ 50 pF plus 1 medium-power TTL load.

Timing Diagram



* BCLK RANGES FROM 128 KHz TO 4.096 MHz, IT DETERMINES ADR, FS, D_R, AND D_X TIMING

Figure 4. I/O Timing

AC Characteristics – Transmission Parameters

Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_E	Encoder Milliwatt Response (Transmit Gain Tolerance)					Signal input = .7746 Vrms
	μ-law	−0.15	±0.08	0.15	dBm0	V_{CC} and V_{SS} are ± 5 %
	A-law	−.18	±0.08	0.18	dBm0	T_A = 0 to 70 °C
G_D	Digital Milliwatt Response (Receive Gain Tolerance)					V_{CC} and V_{SS} are ± 5 % T_A = 0 to 70 °C
	μ-law	−0.15	±0.08	0.15	dBm0	V_{CC} and V_{SS} are ± 5 %
	A-law	−.18	±0.08	0.18	dBm0	T_A = 0 to 70 °C

Gain Tracking – Reference Level = 1.02 kHz, 0 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
$G_{TX\mu}$	Transmit Gain Tracking Error:	−0.25	0.25	dB	3 to −37 dBm0
	Sinusoidal Input, μ-law	−0.50	0.50	dB	−37 to −50 dBm0
G_{TXA}	Transmit Gain Tracking Error:	−0.25	0.25	dB	3 to −37 dBm0
	Sinusoidal Input, A-law	−0.50	0.50	dB	−37 to −50 dBm0
$G_{TR\mu}$	Receive Gain Tracking Error:	−0.25	0.25	dB	3 to −37 dBm0
	Sinusoidal Input, μ-law	−0.50	0.50	dB	−37 to −50 dBm0
G_{TRA}	Receive Gain Tracking Error:	−0.25	0.25	dB	3 to −37 dBm0
	Sinusoidal Input, A-law	−0.50	0.50	dB	−37 to −50 dBm0

Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
D_{XS}	Transmit Signal to Distortion:	36(35)	–	–	dB	$0 \leq VFxI \leq -30$ dBm0
	Sinusoidal Input, μ-law (A-law)	30(29)	–	–	dB	−40 dBm0
		25(25)	–	–	dB	−45 dBm0
						(Input = 1.02 kHz)
D_{RS}	Receive Signal to Distortion:	36(35)	–	–	dB	$0 \leq D_R \leq -30$ dBm0
	Sinusoidal Input, μ-law (A-law)	30(29)	–	–	dB	−40 dBm0
		25(25)	–	–	dB	−45 dBm0
						(Input = 1.02 kHz)
D_{XSF}	Transmit Single Frequency:	–	–	−28	dBm0	$0 \leq$ Input $\leq$ 2 MHz
	Distortion Products	–	–	−40	dBm0	.2 $\leq$ Input $\leq$ 3.4 kHz
D_{RSF}	Receive Single Frequency:	–	–	−28	dBm0	$0 \leq$ Input $\leq$ 2 MHz
	Distortion Products	–	–	−40	dBm0	.2 $\leq$ Input $\leq$ 3.4 kHz
D_{XD}	Transmit Absolute Delay	–	340	–	μs	–
D_{RD}	Receive Absolute Delay	–	240	–	μs	–
D_{DAA}	Delay Distortion:	–	250	–	μs	f = 500 Hz
	Analog-to-Analog	–	60	–	μs	f = 1 kHz
		–	20	–	μs	f = 1.5 kHz
		–	20	–	μs	f = 2 kHz
		–	50	–	μs	f = 2.5 kHz
		–	220	–	μs	f = 3 kHz

Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
FXC	Transmit Idle Channel Noise: C-Message Weighted	—	14	18 23	dBrnC0 dBrnC0	μ-law A-law
FRC	Receive Idle Channel Noise: C-Message Weighted	—	9	13 15	dBrnC0 dBrnC0	μ-law A-law
FXP	Transmit Idle Channel Noise: Psophometric Weighted	—	−69	−67	dBm0p	—
FRP	Receive Idle Channel Noise: Psophometric Weighted	—	−81	−75	dBm0p	—
PSRXCC	VCC Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at DX
PSRXSS	VSS Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at DX
PSRRCC	VCC Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz at VFRO
PSRRSS	VSS Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz at VFRO
FCXR	Crosstalk: Transmit to Receive, Single-Ended Outputs, μ-law (A-law)	—	—	−71 (−70)	dB	VFXI = 0 dBm0; 1.02 kHz signal measured at VFRO; DR = idle code
FCRX	Crosstalk: Receive to Transmit, Single-Ended Outputs, μ-law (A-law)	—	—	−71 (−70)	dB	DR = 0 dBm0; VFXI = GNDA; 1.02 kHz signal measured at DX

Transmit Filter Transfer Characteristics

Transmit Gain Relative to Gain at 1.02 kHz (GRX)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
16.67 Hz	–	−35	−30	dB
50 Hz	–	−33	−30	dB
60 Hz	–	−40	−30	dB
200 Hz	−1.8	−0.5	0	dB
300 to 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	0.01	0.125	dB
3380 Hz	−0.885	−0.7	0.015	dB
3980 Hz	–	−15.6	−13.3	dB
4600 Hz and above	–	–	−32	dB

*0 dBm0 signal input at VFXI.

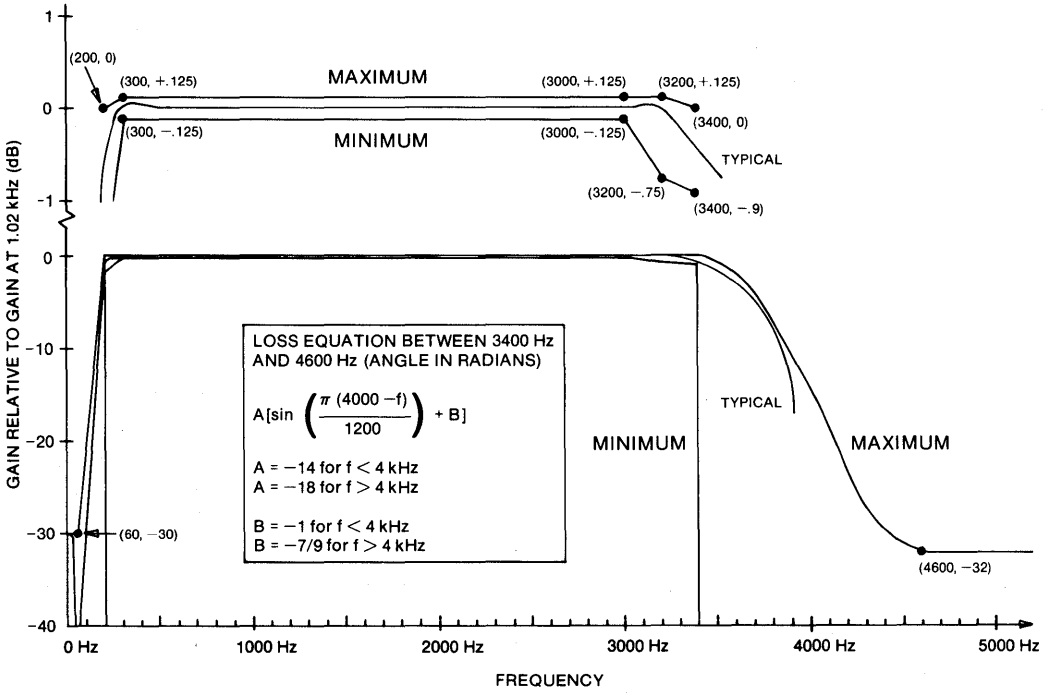


Figure 5. Transmit Filter Characteristics

Receive Filter Transfer Characteristics

Receive Gain Relative to Gain at 1.02 kHz (GRR)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
Below 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	±0.04	0.125	dB
3380 Hz	−0.885	−0.58	0.015	dB
3980 Hz	—	−15.7	−13.3	dB
4600 Hz and above	—	—	−28	dB

*0 dBm0 signal input at DR.

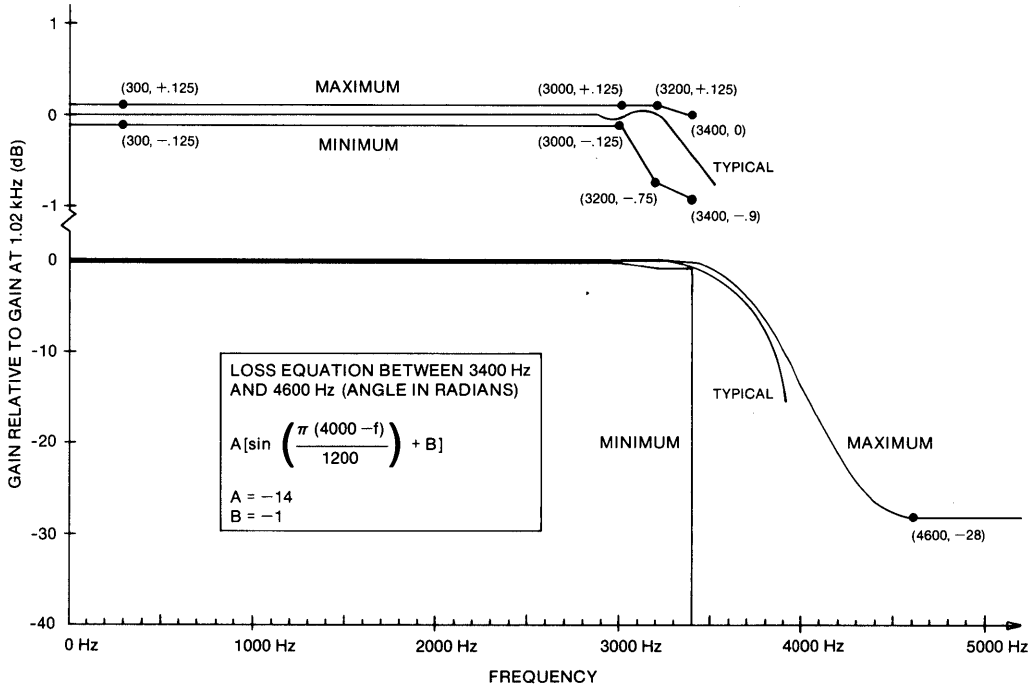


Figure 6. Receive Filter Characteristics

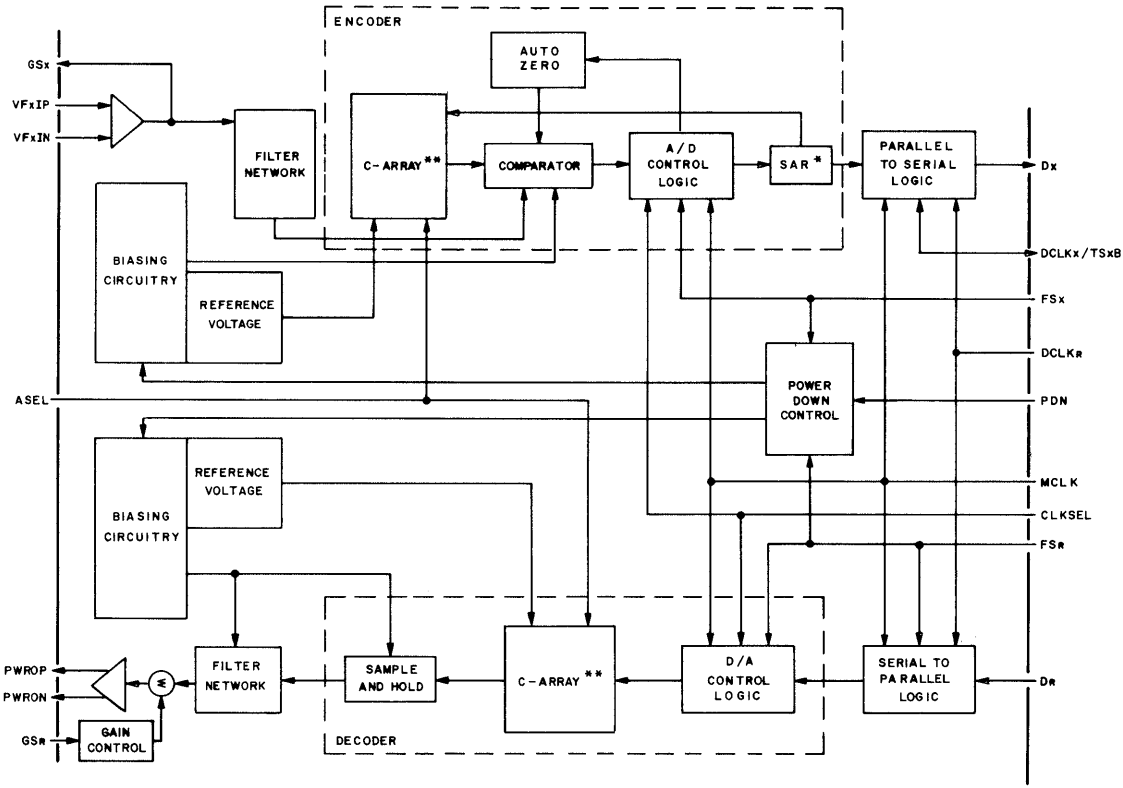
The information contained herein is preliminary and subject to change.

FEATURES

- AT&T/CCITT compatible
- Pin-selectable μ-law or A-law operation
- Differential or single-ended analog input and output, with gain setting
- Direct interface with transformer or electronic hybrids
- Variable data rate (64 kHz to 2.048 MHz)
- Pin-selectable master clock rate (1.536, 1.544, or 2.048 MHz)
- On-chip precision voltage references
- No external components required
- ±5 V operation
- CMOS technology for low power consumption
- Direct replacement for Intel 29C13

DESCRIPTION

The T7513 PCM Codec With Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion, as well as the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed system. The T7513 device is available in a 20-pin plastic DIP or in a 20-pin plastic small-outline J (SOJ) package for surface mounting.

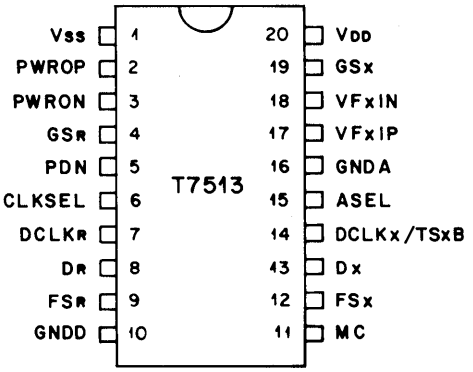


*Successive Approximation Register
**Capacitor Array

Figure 1. T7513 PCM Codec With Filters Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASEL	15	GSR	4
CLKSEL	6	GSX	19
DR	8	MC	11
DX	13	PDN	5
DCLKR	7	PWRON	3
DCLKX/TSXB	14	PWROP	2
FSR	9	VDD	20
FSX	12	VSS	1
GNDA	16	VFXIN	18
GNDD	10	VFXIP	17

Figure 2. T7513 20-Pin Plastic DIP or SOJ Package Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7513 Pin Descriptions

Pin	Symbol	Type	Name/Function
1	VSS	–	**−5 V Supply (±5%).**
2	PWROP	O	Noninverting output of receive power amplifiers. Can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
3	PWRON	O	Inverting output of power amplifiers. Functionally identical and complementary to PWROP.
4	GSR	I	**Receive Gain Setting Input.** Gain can be adjusted from 0 to −12 dB by using a resistive divider between PWROP and PWRON to vary the voltage at GSR.
5	PDN	I	**Power-Down Input.** A TTL-low on this pin places both the transmit and receive sections of the chip in power-down mode. When high or floating, the device functions normally.
6	CLKSEL	I	**Clock Select Input.** Must be tied to VSS (1.536 MHz), GNDD (1.544 MHz), or VDD (2.048 MHz) to reflect the frequency applied to the MC input.
7	DCLKR	I	**Receive Data Clock.** When tied to VSS, fixed data rate operation is selected. When not tied to VSS, DCLKR is the TTL-level receive data clock, which operates at data rates from 64 kHz to 2.048 MHz.
8	DR	I	**Receive PCM Input.** Data is clocked in on this input on the first eight consecutive negative transitions of DCLKR (variable rate mode) or MC (fixed rate mode) following the rising edge of FSR.

Table 1. T7513 Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
9	FSR	I	**8 kHz Receive Frame Synchronization Clock.** In fixed rate mode, FSR must be high for a minimum of one MC cycle. In variable rate mode, it must be held high for eight DCLKR cycles. The receive channel automatically enters the power-down mode whenever FSR is TTL-low for approximately 300 ms.
10	GNDD	–	**Digital Ground.** Internally separate from GNDA.
11	MC	I	**TTL-Level Master Clock Input.** MC frequency must be 2.048, 1.544, or 1.536 MHz, depending on the voltage at the CLKSEL input. In the fixed rate mode, this input also acts as the transmit and receive data clock.
12	FSx	I	**8 kHz Transmit Frame Synchronization Clock.** Operates independently of, but in a manner analogous to, FSR. The transmit channel automatically enters the power-down mode whenever FSx has been TTL-low for approximately 300 ms.
13	Dx	O	**Transmit PCM Output.** Data is clocked out on this lead on the first eight consecutive positive transitions of DCLKx (in variable rate mode) or MC (in fixed rate mode) following the rising edge of FSx. Dx remains in a high-impedance state unless the transmit time slot is activated by raising FSx.
14	DCLKx/TSxB	I/O	In variable rate mode, DCLKx is a TTL-level input, which operates between 64 kHz and 2.048 MHz as the transmit data clock. In fixed mode, this pin is an open-drain output providing a time slot enable strobe for use with an external 3-state buffer.
15	ASEL	I	**μ-law/A-law Select Input.** When tied to VSS, A-law operation is selected. When tied to VDD or GNDD, μ-law companding is selected.
16	GNDA	–	**Analog Ground.** Internally separate from GNDD.
17	VFxIP	I	Noninverting analog input to the uncommitted operational amplifier at the transmit filter input.
18	VFxIN	I	Inverting input to the uncommitted transmit operational amplifier.
19	GSx	O	Output of the transmit side uncommitted op amp. Internally, this node is the positive input to the transmit differential filters.
20	VDD	–	**5 V Supply (± 5%).**

Overview

The T7513 Codec is a synchronous device with a common master clock and independent synchronization and data timing signals for the transmit and receive channels. Permissible master clock frequencies are 2.048, 1.544, and 1.536 MHz. The chosen MC frequency must be reflected in the setting of the CLKSEL input. Data transfer on the Dx and DR lines is initiated by a rising edge on the associated FS input, with the data rate being determined by DCLK or by MC depending on the mode of operation selected.

The variable rate data mode is selected by connecting DCLKx and DCLKR to the transmit and receive data clocks, respectively. In this mode, DCLKx and DCLKR are independent, asynchronous clocks that may vary in frequency from 64 kHz to 2.048 MHz and that need to be synchronized to MC only at the beginning of each frame. Data transmission on the Dx lead is initiated on the rising edge of FSx, with bit timing being determined by DCLKx. FSx is required to be high for a minimum of eight DCLKx cycles in order that the full data word be transmitted. Receive data transfer on the DR input is controlled by FSR and DCLK in an analogous but independent manner.

The fixed data rate mode is selected by strapping DCLKR to VSS. In the fixed rate mode, data I/O is synchronized by the FSR and FSx inputs, but bit timing for both channels is determined by MC. The only available bit rates are 2.048, 1.544, or 1.536 MHz. FSR and FSx may operate independently and must be high for a minimum of one MC cycle. While in the fixed rate mode, the DCLKx pin becomes an open drain output which can be used to enable an external 3-state Dx buffer. (The internal Dx buffer continues to automatically enter a high-impedance mode whenever Dx is inactive.)

The T7513 Codec incorporates two power-down modes in order to reduce power consumption and heat dissipation when device operation is not required. The entire chip can be placed in power-down mode by placing a TTL low signal on the PDN input. Additionally, the transmit and receive sides of the device power down independently whenever the frame synchronization signal for that side has been low for approximately 300 ms.

The T7513 device implements either μ-law or A-law PCM encoding. A-law operation is selected by strapping the ASEL input to VSS. For μ-law operation, ASEL should be tied to either VDD or GNDD. Alternate digit inversion is used for A-law transmission.

Zero transmission level points in the table below are specified relative to the digital milliwatt sequence prescribed by CCITT recommendation G.711 with the codec configured for unity gain, single-ended input (GSx tied VFxIN, input at VFxIP) and maximum gain, single-ended output (GSR tied to PWRON and output measured between PWROP and GNDA). Under these conditions, an analog input of 1.064 Vrms

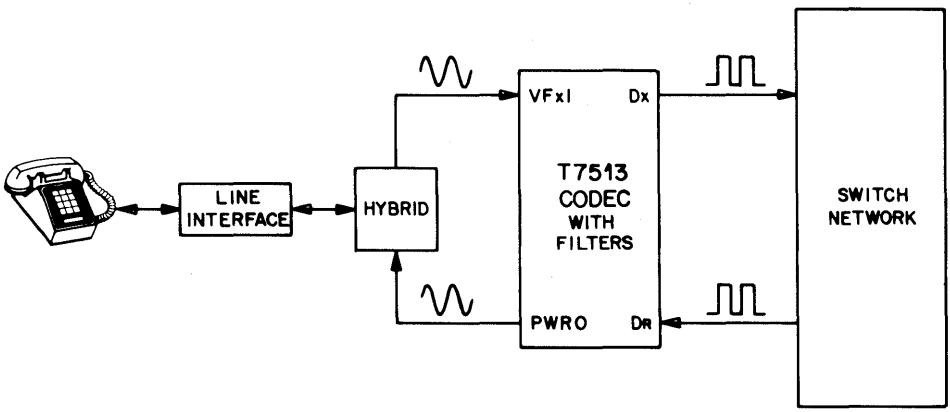


Figure 3. PCM System Block Diagram

applied to VFxIP will produce a 0 dBm digital code at Dx, while a 0 dBm code input at DR will produce an output of 1.503 Vrms at PWROP.

Table 2. Zero Transmission Level Points

Symbol	Parameter	Value	Unit	Test Conditions
OTLP1x	Zero Transmission Level Point: Transmit Channel (0 dBm0), μ-law	2.76 1.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP2x	Zero Transmission Level Point: Transmit Channel (0 dBm0), A-law	2.79 1.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP1R	Zero Transmission Level Point: Receive Channel (0 dBm0), μ-law	5.76 4.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP2R	Zero Transmission Level Point: Receive Channel (0 dBm0), A-law	5.79 4.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω

Analog Input

The analog input section of the T7513 Codec includes an uncommitted input amplifier to provide maximum flexibility in interfacing with transmission systems. Possible applications include 2-to-4-wire conversion and/or gain adjustment. A schematic of the input circuit is shown below. Note that a conventional single-ended unity gain configuration is achieved by simply connecting GSx to VFxIN and applying the analog between VFxIP and GNDA. The load impedance to ground at the GSx output should be greater than 10 kΩ in parallel with less than 50 pF.

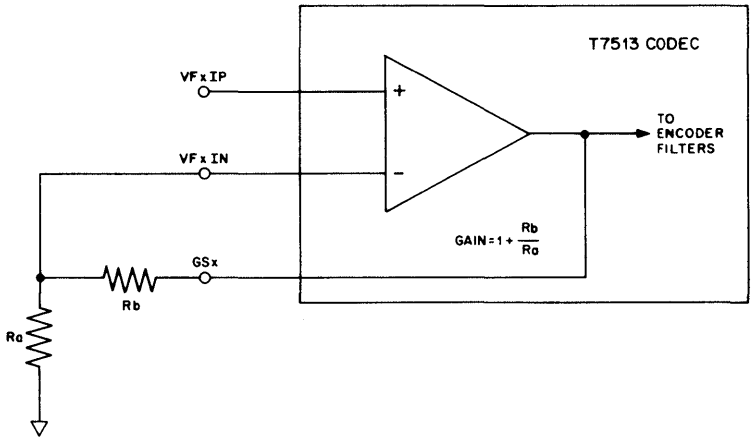


Figure 4. Analog Inputs

Analog Output

The analog output of the T7513 device is provided via a set of low-impedance complementary outputs, PWROP and PWRON. Either of the outputs can be used as a single-ended output to drive loads as low as 300 Ω or, alternatively, the outputs can be used together to provide a 600 Ω differential drive capability. Receive gain is set by interpolating the voltage at the buffered, high-impedance GSR input

between the voltages at the PWROP and PWRON nodes with a resistive divider network. Gain is variable from 0 to −12 dB, according to the relationship shown in the equation:

$$A = \left[\frac{1 + \left(\frac{R1}{R2}\right)}{4 + \left(\frac{R1}{R2}\right)} \right]$$

where R1 and R2 are connected as shown below and the output is taken single ended. Note that maximum gain (A=1) is achieved with GSR tied to PWRON (R1/R2 = ∞) and that minimum output (A=1/4) is achieved by connecting GSR to PWROP (R1/R2 = 0). For proper device operation, it is recommended that R1 and R2 be chosen such that R1 + R2 > 10 kΩ and that the parallel combination of R1 and R2 is less than 100 kΩ.

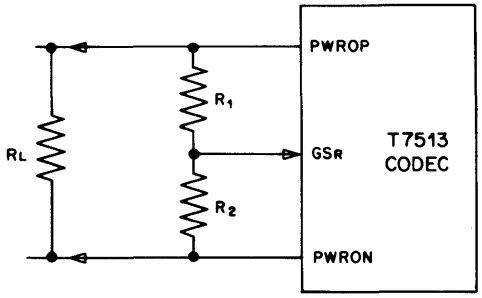


Figure 5. Analog Outputs

CHARACTERISTICS

DC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5% ; V_{SS} = −5V±5% ; GNDA = 0 V; GNDD = 0 V, unless otherwise specified. Typical values are for T_A = 25 °C and nominal power supply values.

Digital Interface

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low-Level Input Current	−20	—	—	μA	GNDD ≤ V_{IN} ≤ V_{IL}
I_{IH}	High-Level Input Current	—	—	20	μA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input Low Voltage	—	—	0.8	V	—
V_{IH}	Input High Voltage	2.0	—	—	V	—
V_{OL}	Output Low Voltage	—	—	0.4	V	—
V_{OH}	Output High Voltage	2.4	—	—	V	—
C_I	Digital Input Capacitance	—	—	5	pF	—
I_L	Output Leakage Current	−50	—	50	μA	—

Power Dissipation

All measurements made at fMC = fDCLK = 2.048 MHz, outputs unloaded

Symbol	Parameter	Min	Typ	Max	Unit
I_{DD1}	V_{DD} Operating Current	–	9.5	16	mA
I_{SS1}	V_{SS} Operating Current	–	−8.75	−15	mA
I_{DD0}	V_{DD} Power-Down Current	–	5.0	9	mA
I_{SS0}	V_{SS} Power-Down Current	–	−3.5	7	mA
V_{CC}	Positive Operating Voltage	4.75	5	5.25*	V
V_{SS}	Negative Operating Voltage	−4.75	−5	−5.25*	V
P_1	Operating Power Dissipation	–	90	150	mW
P_0	Power-Down Dissipation	–	45	80	mW

*Absolute maximum ratings are V_{DD} = 7.5 V, V_{SS} = −7.5 V. Exceeding these values may result in permanent internal damage.

Analog Interface — Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, VFxI+, VFxI−	–	–	100	nA	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
R_{IXI}	Input Resistance, VFxI+, VFxI−	10	–	–	MΩ	–
V_{OSXI}	Input Offset Voltage, VFxI+, VFxI−	–	–	25	mV	–
CMRR	Common Mode Rejection, VFxI+, VFxI−	55	–	–	dB	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
AVOL	DC Open Loop Voltage Gain, GSx	5000	–	–	–	–
fC	Open Loop Unity Gain Bandwidth, GSx	–	1	–	MHz	–
C_{LXI}	Load Capacitance, GSx	–	–	50	pF	–
R_{LXI}	Minimum Load Resistance, GSx	10	–	–	kΩ	–

Analog Interface — Receive Filter Driver Amplifier Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO−	–	1	–	Ω	–
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO−	–	75	±150	mV	Relative to GNDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−	–	–	100	pF	–

AC Characteristics – Transmission Parameters

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder.

The receive output is measured single ended, maximum gain configuration. All output levels are (sin x)/x corrected. Specifications are for synchronous operation.

Note 1: 0 dBm0 is defined as the zero reference point of the channel under test (OTLP). This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms for μ-law.

Note 2: Unity gain input amplifier: GSx is connected to VFx1−, signal input VFx1+; maximum gain output amplifier: GSR is connected to PWRO−, output to PWRO+.

Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
EmW	Encode Milliwatt Response (Transmit Gain Tolerance)	−0.18	±0.04	+0.18	dBm0	Signal input of 1.064 Vrms, μ-law; Signal input of 1.068 Vrms, A-law. T_A = 25 °C, V_{DD} = +5 V, V_{SS} = −5 V.
EmWTS	EmW Variation with Temperature and Supplies	−0.07	±0.02	+0.07	dB	±5% supplies, 0 to 70 °C. Relative to nominal conditions.
DmW	Digital Milliwatt Response (Receive Gain Tolerance)	−0.18	±0.04	+0.18	dBm0	Measure relative to $OTLP_R$ signal input per CCITT Recommendation G.711. Output signal of 1000 Hz, R_L = ∞ T_A = 25 °C; V_{SS} = −5 V, V_{DD} = 5 V.
DmWTS	DmW Variation with Temperature and Supplies	−0.07	±0.02	+0.07	dB	±5% supplies, 0 to 70 °C.

Gain Tracking – Reference Level = 1.02 kHz, 0 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
GT1x	Transmit Gain Tracking Error: Sinusoidal Input, μ-law	−0.25 −0.50	0.25 0.50	dB dB	+3 to −37 dBm0 −37 to −50 dBm0
GT2x	Transmit Gain Tracking Error: Sinusoidal Input, A-law	−0.25 −0.50	0.25 0.50	dB dB	+3 to −37 dBm0 −37 to −50 dBm0
GT1R	Receive Gain Tracking Error: Sinusoidal Input, μ-law	−0.25 −0.50	0.25 0.50	dB dB	+3 to −37 dBm0 −37 to −50 dBm0
GT2R	Receive Gain Tracking Error: Sinusoidal Input, A-law	−0.25 −0.50	0.25 0.50	dB dB	+3 to −37 dBm0 −37 to −50 dBm0

Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SDx	Transmit Signal to Distortion: Sinusoidal Input, μ-law (A-law)	36(35) 30(29) 25(25)	–	–	dB dB dB	0 ≤ VFx1 ≤ −30 dBm0 −40 dBm0 −45 dBm0 (Input = 1.02 kHz)
SDR	Receive Signal to Distortion: Sinusoidal Input, μ-law (A-law)	36(35) 30(29) 25(25)	–	–	dB dB dB	0 ≤ DR ≤ −30 dBm0 −40 dBm0 −45 dBm0 (Input = 1.02 kHz)
DPx	Transmit Single Frequency: Distortion Products	–	–	−28 −40	dBm0 dBm0	0 ≤ Input ≤ 2 MHz .2 ≤ Input ≤ 3.4 kHz
DPR	Receive Single Frequency: Distortion Products	–	–	−28 −40	dBm0 dBm0	0 ≤ Input ≤ 2 MHz .2 ≤ Input ≤ 3.4 kHz
DAX	Transmit Absolute Delay	–	340	–	μs	–
DAR	Receive Absolute Delay	–	240	–	μs	–
DDAA	Delay Distortion: Analog-to-Analog	–	250 60 20 20 50 220	–	μs μs μs μs μs μs	f = 500 Hz f = 1 kHz f = 1.5 kHz f = 2 kHz f = 2.5 kHz f = 3 kHz

Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
NXC	Transmit Idle Channel Noise: C-Message Weighted	—	14	18 23	dBrnC0 dBrnC0	μ-law A-law
NRC	Receive Idle Channel Noise: C-Message Weighted	—	9	13 15	dBrnC0 dBrnC0	μ-law A-law
NXP	Transmit Idle Channel Noise: Phosphometric Weighted	—	−69	−67	dBm0p	—
NXR	Receive Idle Channel Noise: Phosphometric Weighted	—	−81	−75	dBm0p	—
PSRR1	VDD Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at Dx
PSRR2	VSS Power Supply Rejection: Transmit Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at Dx
PSRR3	VDD Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at PWROP
PSRR4	VSS Power Supply Rejection: Receive Channel	−30	−35	—	dB	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at VFRO
CTXR	Crosstalk: Transmit to Receive, Single-Ended Outputs, μ-law (A-law)	—	—	−70	dB	VFxIP = 0 dBm0; 1.02 kHz signal measured at PWROP, DR = idle code
CTRX	Crosstalk: Receive to Transmit, Single-Ended Outputs, μ-law (A-law)	—	—	(−70)	dB	DR = 0 dBm0; VFxIP = GNDA; 1.02 kHz signal measured at Dx

Receive Filter Transfer Characteristics (Figure 6)

Receive Gain Relative to Gain at 1.02 kHz (GRR)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
Below 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	±0.04	0.125	dB
3380 Hz	−0.885	−0.58	−0.015	dB
3980 Hz	–	−15.7	−13.3	dB
4600 Hz and above	–	–	−28	dB

*0 dBm0 signal input at DR

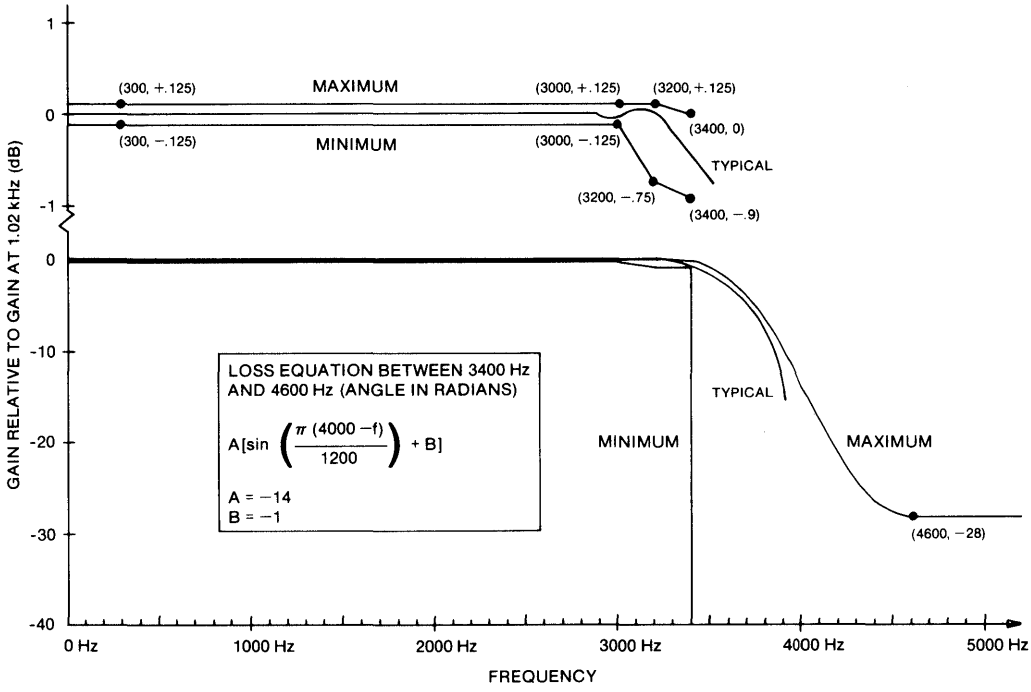


Figure 6. Receive Filter Characteristics

Transmit Filter Transfer Characteristics (Figure 7)

Transmit Gain Relative to Gain at 1.02 kHz (GRX)*				
Frequency	**Min**	**Typ**	**Max**	**Unit**
16.67 Hz	–	−35	−30	dB
50 Hz	–	−33	−30	dB
60 Hz	–	−40	−30	dB
200 Hz	−1.8	−0.5	0	dB
300 to 3000 Hz	−0.125	±0.04	0.125	dB
3140 Hz	−0.57	0.01	0.125	dB
3380 Hz	−0.885	−0.7	0.015	dB
3980 Hz	–	−15.6	−13.3	dB
4600 Hz and above	–	–	−32	dB

*0 dBm0 signal input at VFxIP

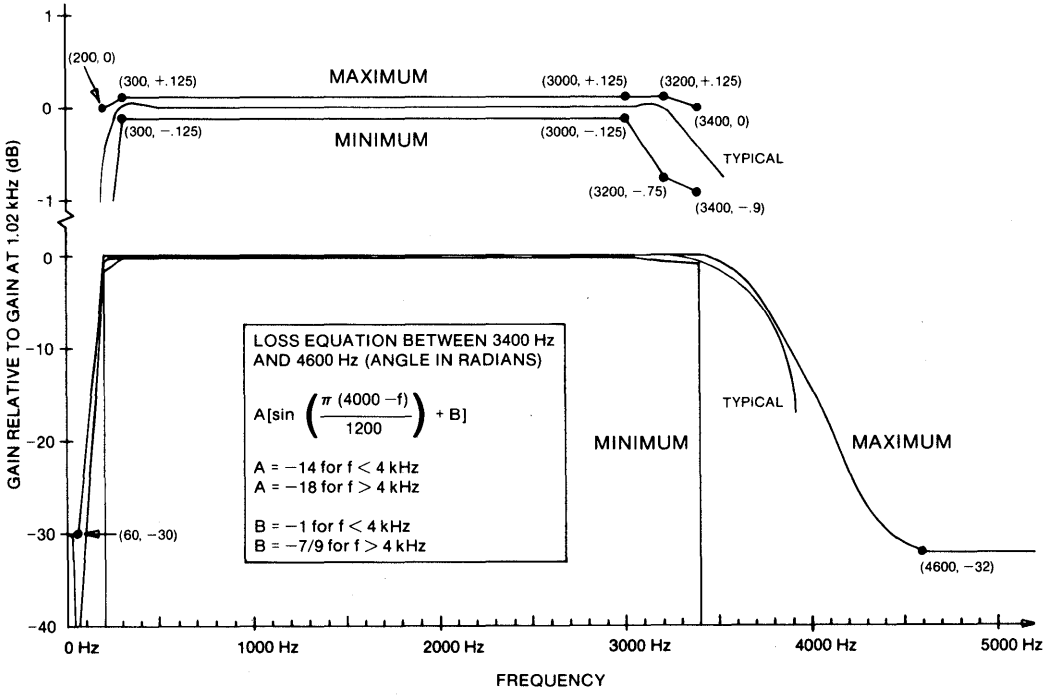


Figure 7. Transmit Filter Characteristics

Timing Characteristics

Clock Section (Figures 8, 9, 10, and 11)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHMCH	Clock Period, MC	488	–	–	ns	fMC = 2.048 MHz
tMCHMCL1	Clock Pulse Width, MC	220	–	–	ns	–
tDCLK	Data Clock Pulse Width	220	–	–	ns	64 kHz ≤ fDCLK ≤ 2.048 MHz
tCDC	Clock Duty Cycle, MC	45	50	55	%	–
tMCH1MCH2, tMCL2MCL1	Clock Rise and Fall Time	5	–	30	ns	–

Transmit Section, Fixed Data Rate Mode* (Figure 8)

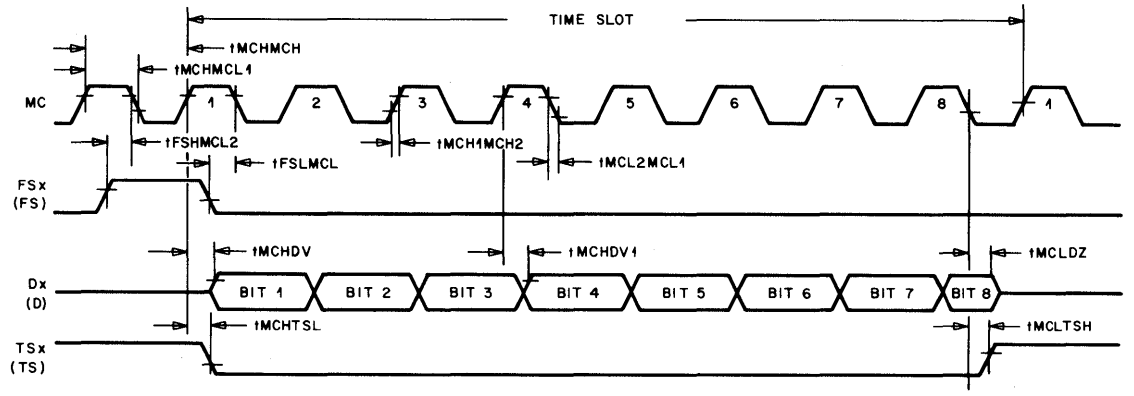
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHTDV	Data Enabled on TS Entry	0	–	145	ns	0 < CLOAD < 250 pF
tMCHDV1	Data Delay from MC	0	–	145	ns	0 < CLOAD < 250 pF
tMCLDZ	Data Float on TS Exit	60	–	215	ns	CLOAD = 0
tMCHTSL	Time-Slot X to Enable	0	–	145	ns	0 < CLOAD < 250 pF
tMCLTSH	Time-Slot X to Disable	60	–	215	ns	CLOAD = 0
tFSHMCL2	Frame Sync Delay	100	–	tMCHMCH−100	ns	–

*Timing parameters tMCHTDV, tMCLDZ, and tMCLTSH are referenced to a high-impedance state.

Receive Section, Fixed Data Rate Mode (Figure 9)

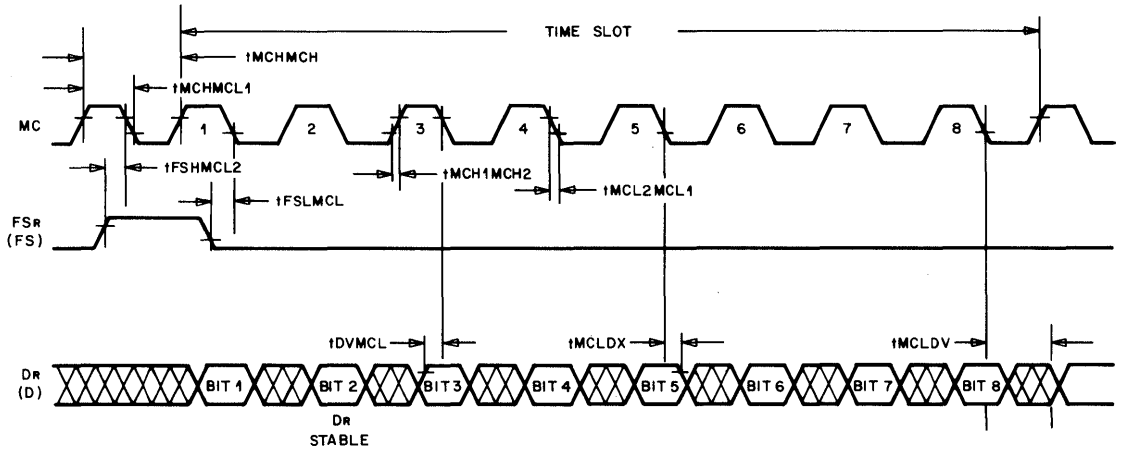
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tDVMCL	Receive Data Set-Up	10	–	–	ns	–
tMCLDV	Receive Data Hold	60	–	–	ns	–
tFSLMCL	Frame Sync Delay	100	–	tMCHMCH−100	ns	–
tSIGR	SIGR Update	0	–	2	μs	–

Timing Diagrams



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT tMCHTSV, tMCLTSH, tMCLDZ WHICH REFERENCE A HIGH IMPEDANCE STATE.

Figure 8. Fixed Data Rate Transmit Timing



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}

Figure 9. Fixed Data Rate Receive Timing

Transmit Section, Variable Data Rate Mode* (Figure 10)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-Slot Delay from DCLKx*	140	–	tDX–140	ns	–
tFSHMCL	Frame Sync Delay**	100	–	tMCHMCH–100	ns	–
tDCHDV	Data Delay from DCLKx	0	–	100	ns	0 < CLOAD < 250 pF
tFSHDV	Time-Slot to DX Active	0	–	50	ns	0 < CLOAD < 250 pF
tFSLDX	Time-Slot to DX Inactive*	0	–	80	ns	0 < CLOAD < 250 pF
tDX	Data Clock Period	488	–	15620	ns	64kHz < fDCLKx < 2.048 MHz
tFSHDV1	Data Delay from FSx	0	–	140	ns	–

*tFSLX minimum requirements override tFSHDCL maximum spec for 64 kHz operation.
**Timing parameters tFSHMCH and tFSLDX are referenced to a high impedance state.

Receive Section, Variable Data Rate Mode (Figure 11)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-Slot Delay from DCLKR*	140	–	tDR–140	ns	–
tFSHMCL	Frame Sync Delay	100	–	tMCHMCH–100	ns	–
tDVDCL	Data Set-Up Time	10	–	–	ns	–
tDCLDX	Data Hold Time	60	–	–	ns	–
tDR	Data Clock Period	488	–	15620	ns	64 kHz < fDCLKx < 2.048 MHz
tDCLFSL	Time-Slot End Receive Time	60	–	–	ns	–

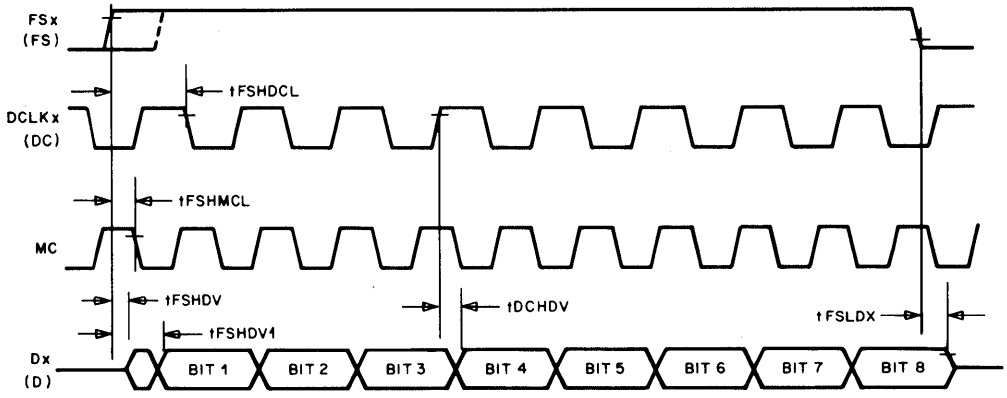
*tFSLR minimum requirements override tFSHDCL maximum spec for 64 kHz operation.

64 kB Operation, Variable Data Rate Mode

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSLX*	Transmit Frame Sync Minimum Downtime	488	–	–	ns	FSx is TTL high for remainder of frame
tFSLR**	Receive Frame Sync Minimum Downtime	1952	–	–	ns	FSR is TTL high for remainder of frame
tDCLK	Data Clock Pulse Width	–	–	10	μs	–

*tFSLX minimum requirements override tFSHDCL maximum spec for 64 kHz operation.
**tFSLR minimum requirements override tFSHDCL maximum spec for 64 kHz operation.

Variable Data Rate Timing



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT tFSHDA AND tFSLDX WHICH REFERENCE A HIGH IMPEDANCE STATE.

Figure 10. Variable Data Rate Transmit Timing

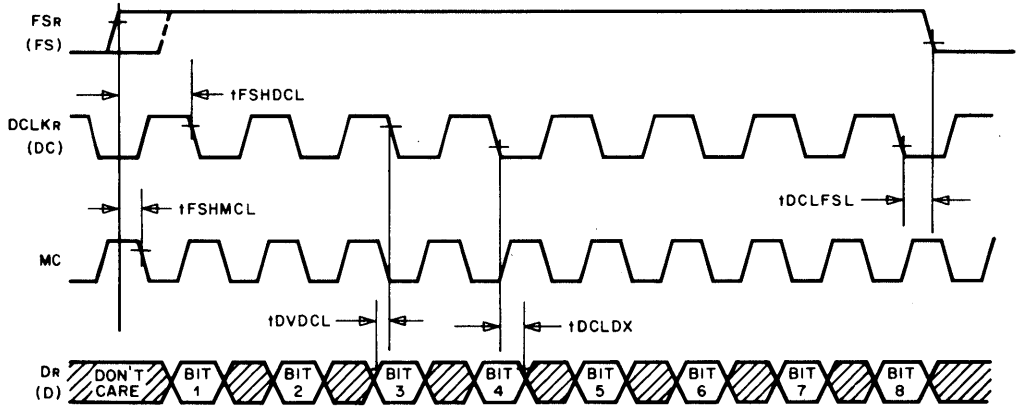


Figure 11. Variable Data Rate Receive Timing

A.C. TESTING: INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0"

Figure 12. AC Testing Input, Output Waveform

The information contained herein is preliminary and subject to change.

FEATURES

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120 mW nominal power
- Independent transmit and receive power-down
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format 16-bit PCM in 2s complement binary (LSB first)
- Gain selection – transmit: 0 or −3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR

DESCRIPTION

The T7520 High-Precision PCM Codec With Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. Anti-aliasing and reconstruction filters are provided on-chip, as well as precision voltage references. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM μ-law data. The T7520 Codec is a linear device with 16-bit PCM I/O data in 2s complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. The T7520 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

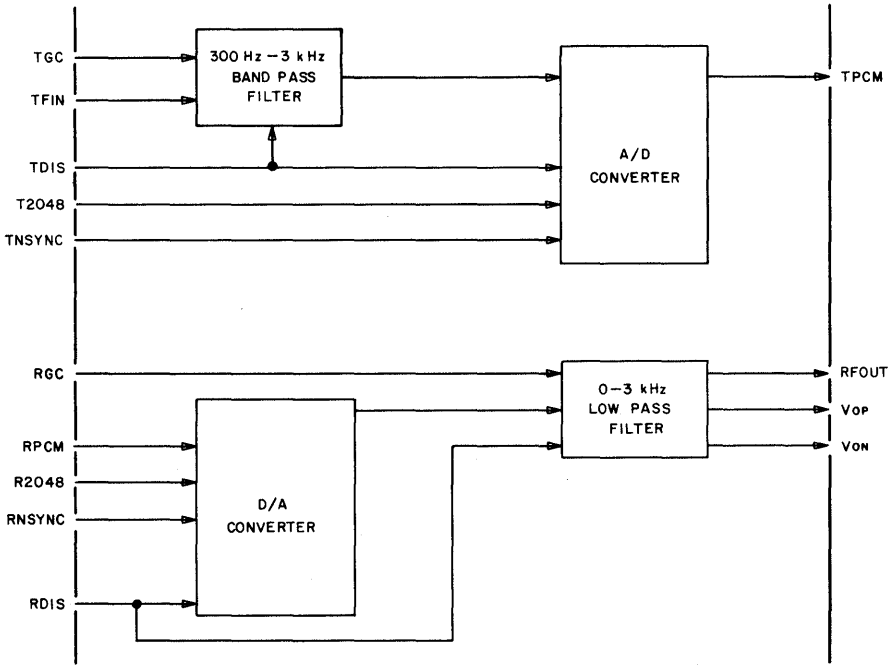
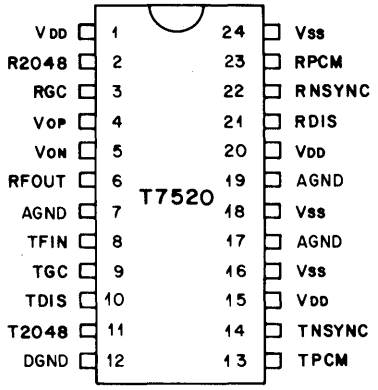


Figure 1. T7520 High-Precision PCM Codec With Filters Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin(s)
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
RDIS	21	TNSYNC	14
RFOUT	6	TPCM	13
RGC	3	T2048	11
RNSYNC	22	VDD	1, 15, 20
RPCM	23	VON	5
R2048	2	VOP	4
TDIS	10	VSS	16, 18, 24

Figure 2. T7520 Codec Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7520 Pin Descriptions

Symbol	Type	Name/Function
VDD	–	**5 V Supply (±5%).**
R2048	I	**Receive 2.048 MHz Clock.**
RGC	I	**Receive Gain Control.** A high on the pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT	O	**Receive Filter Output.** A 16-bit digital milliwatt reconstructed by the filter produces a 1.547 Vp signal (when RGC is high). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF capacitance.
AGND	–	**Ground (Analog).**
TFIN	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source.
TGC	I	**Transmit Gain Control.** A high on this pin sets the transmit gain to −3 dB; a low or no connection sets the gain to 0 dB.
TDIS	I	**Transmit Disable.** A high on this pin disables the transmit side; a low or no connection enables the transmit side.
T2048	I	**Transmit 2.048 MHz Clock.**
DGND	–	**Ground (Digital).**

CAUTION: Cavity cover is internally connected to AGND.

Table 1. T7520 Pin Descriptions (Continued)		
Symbol	**Type**	**Name/Function**
TPCM	O	**Transmit PCM.** This pin is used for the A/D 16-bit 2s complement binary PCM (LSB first) output. This pin will be 3-stated when inactive.
TNSYNC	I	**Transmit Synchronization.** An accurate timing pulse (negative going-edge trigger) used to start transmitting the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 14).
VSS	–	**−5 V Supply (±5%).**
RDIS	I	**Receive Disable.** A high on this pin disables the receive side; a low or no connection enables the receive side.
RNSYNC	I	**Receive Synchronization.** An accurate timing pulse (negative going-edge trigger) is used to start reading the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 14).
RPCM	I	**Receive PCM.** This pin is used for the D/A 16-bit PCM 2s complement binary (LSB first) input.
NC	–	**No Connection.**

Application Hints

The T7520 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the VDD pins must be tied together to avoid excessive substrate currents in the chip.

All the VSS pins must be tied together.

All the analog pins (AGND) must be tied together.

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8 kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed ground plane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown on Figure 3. The 3 to 5 Ω decoupling resistors in series with VDD and VSS with the 10 μF tantalum or low ESR aluminum capacitor form a low-pass filter (−3 dB frequency of about 5 kHz). The 0.2 μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated noise.

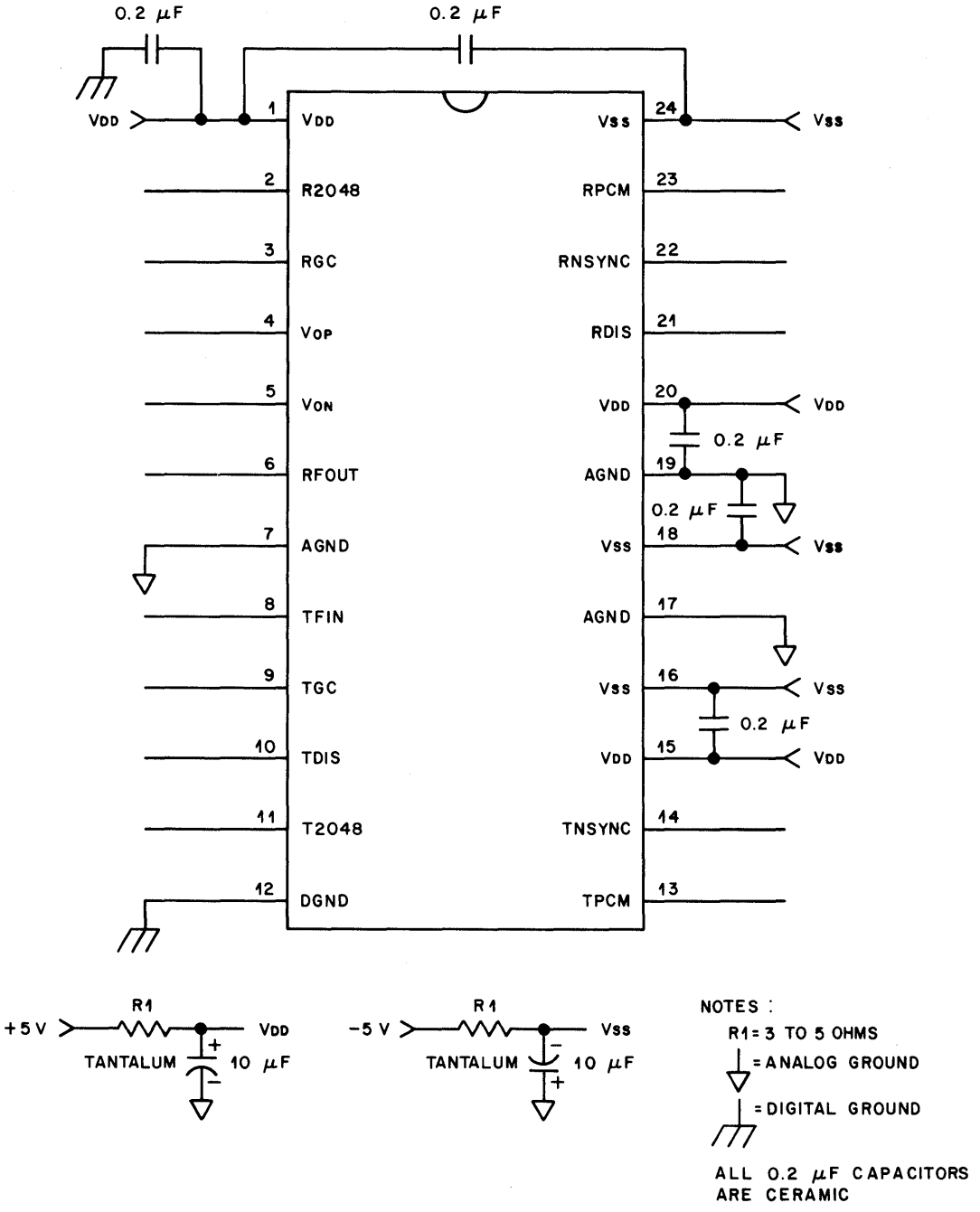


Figure 3. Codec Supply Decoupling

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a) but doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. In short, do not configure clocks in the manner shown on Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown on Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock. The sync clocks must also be locked in phase so that the TNSYNC and T2048 clock edges line up and the RNSYNC and R2048 clock edges line up. This relationship is shown on Figure 4b by the logic blocks run off the master clock, which is driving the codec sync inputs. The timing can be generated by software (in a DSP device, for example), but the sync timing must stay solid with respect to the master clock.

The best noise performance is achieved by using the fully synchronous timing of Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, VOP, and VON) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

CHARACTERISTICS

Electrical Specifications

Analog Interface

TFIN: Rin > 35 kΩ and Cin < 10 pF
RFOUT: ac impedance < 300 Ω, max current 150 μA
Any input can be between VSS and VDD without damaging the chip.

Digital Interface

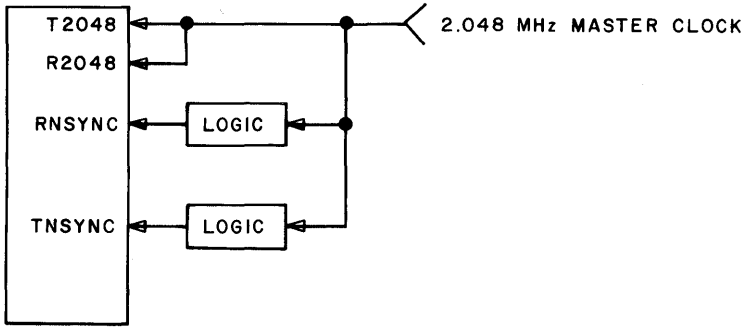
All inputs: TTL-compatible, Iin < 15 μA, < 5 pF loading
TPCM: Capable of driving a 50 pF capacitance to TTL voltage levels at 2.048 Mbits/s

Any input can be between VSS and VDD without damaging the chips.

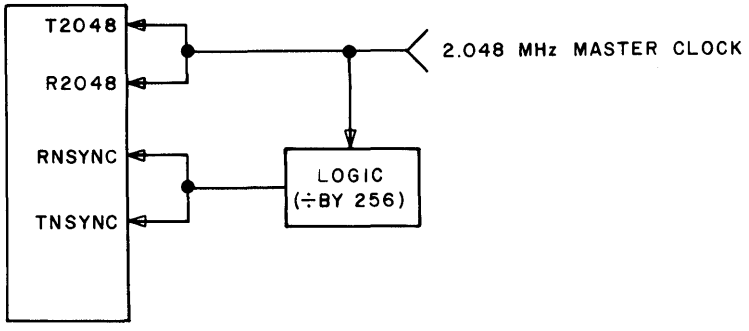
Temperature Range

0 to 70 °C: Meets specifications.

a. Not Recommended (Do Not Do This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Parameter		Limits			Unit
		Min	Typ	Max	
Operating Voltage		±4.75	±5	±5.25	V
Power Disspation					
Active, DIS=0		50	120	200	mW
Inactive, DIS=1		–	15	40	mW
Analog Overload at 1 kHz TGC=RGC=1	0 to 70 °C	±2.191	±2.229	±2.268	Vp
Absolute Gain (Gain Contrast) at 1.02 kHz, Full-Scale Input TGC=0, RCG=0	0 to 70 °C	−0.15	–	0.15	dB
Gain Tracking Transmit or Receive (1.02 kHz, 0 dB Full Scale Input, −3 dB Reference)					
0 dB to −40 dB		–	–	±0.2	dB
−40 dB to −53 dB		–	–	±0.4	dB
Signal-to-Distortion: Transmit or Receive (1.02 kHz) (0 dB = Full-Scale Input)					
0 dB to −25 dB		60	–	–	dB
−40 dB		45	–	–	dB
−45 dB		40	–	–	dB
Idle Channel Noise (Transmit)	TGC=1 or 0	–	9	13	dBC
Idle Channel Noise (Receive)	RGC=1	–	6	9	dBC
	RGC=0	–	3	6	dBC
Power Supply Rejection (End-to-End)					
1 kHz		35	–	–	dB
0—100 kHz White Noise		30	–	–	dBC
Absolute Delay (End-to-End), 1 kHz		–	–	575	μs

Note: 0 dBm = 90 dB = 0.775 Vrms (into 600 Ω)

Overload (1.00 kHz) Compression	
Input/Overload Level (dB)	**Max Increased Loss (dB) Relative to Overload −3 dB**
0	0.2
3	1.8
6	4.6

Note: The filter responses scale linearly with master clock.

In the following tables and associated figures, the ac characteristics assume the master clock (T2048, R2048) to be 2.048 MHz ± 100 ppm.

Frequency Response*		
Freq (Hz)	**Transmit Loss (dB)**	**Receive Loss (dB)**
50—60	≥20	±0.2
200	0.1 to 1.8	−0.05 to +0.2
300—3000	±0.125	±0.125
3200	−0.125 to +0.75	−0.125 to +0.75
3400	0.2 to 0.9	0.2 to 0.9
4000	>14	>14
≥4600	>32	>28
3400—4600	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$
4000—4600	$> 18 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - \frac{7}{9} \right]$	

*See Figures 5 through 9 for response curves.

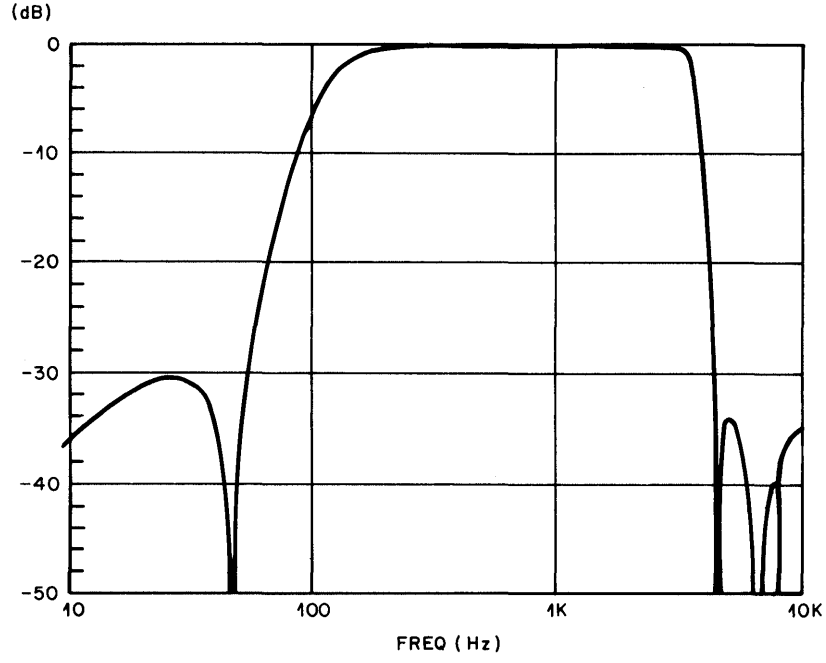


Figure 5. Transmit Path Frequency Response

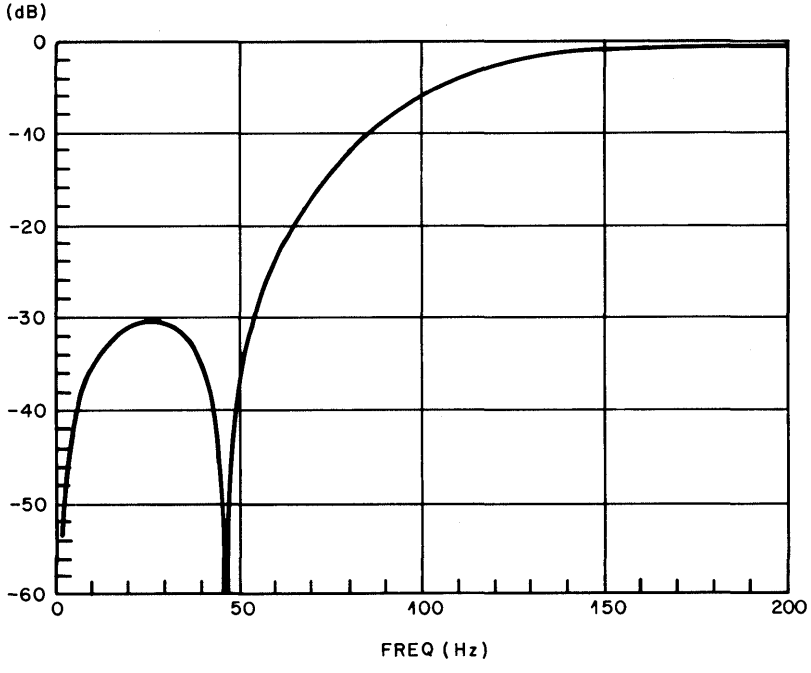


Figure 6. Transmit Path Low Frequency Response

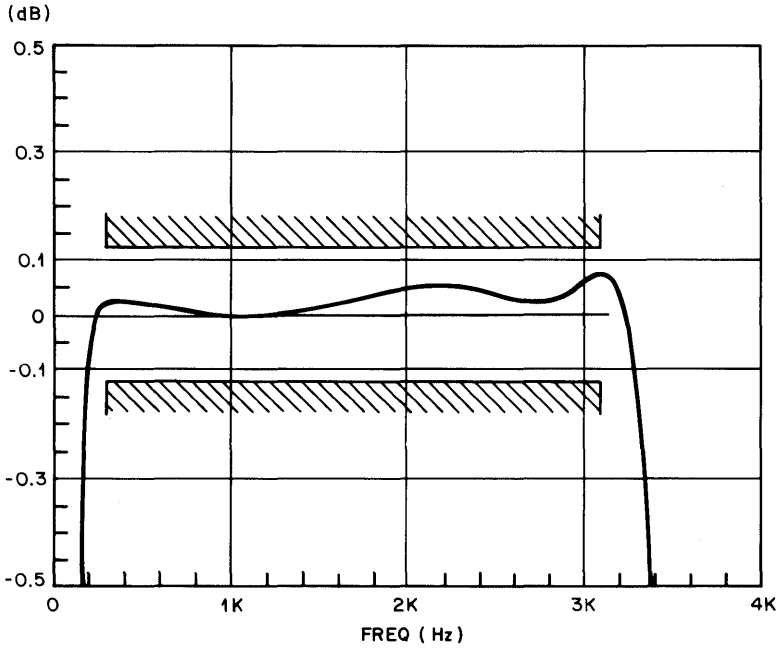


Figure 7. Transmit Path Voice Band Response

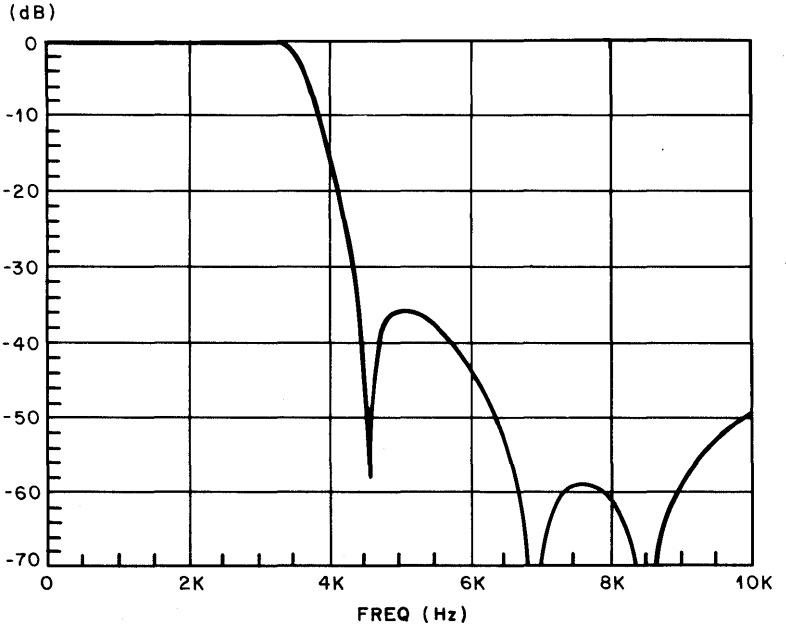


Figure 8. Receive Path Frequency Response

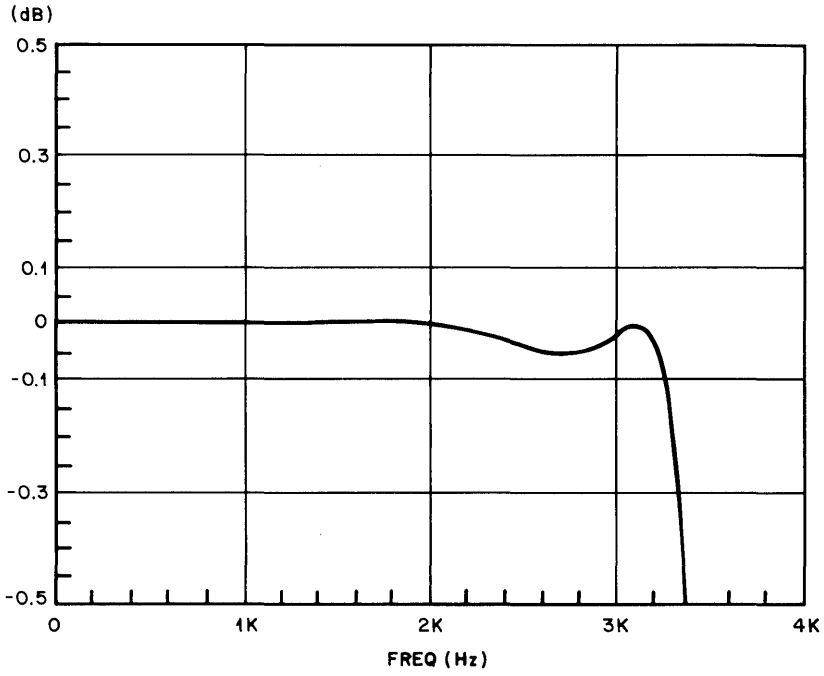


Figure 9. Receive Path Voice Band Response

Phase and Delay Distortion (End-to-End)*		
Freq (Hz)	**Phase Deviation from Linearity (Radians)**	**Delay Distortion (μs, max)**
<500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	–
500–700		300
700–2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at ±0.95 radians and 1850 Hz	75
2000–2500		150
2500–2700		200
2700–3000		375
>3000	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	–

*See Figures 10, 11, and 12 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) <−71 dB

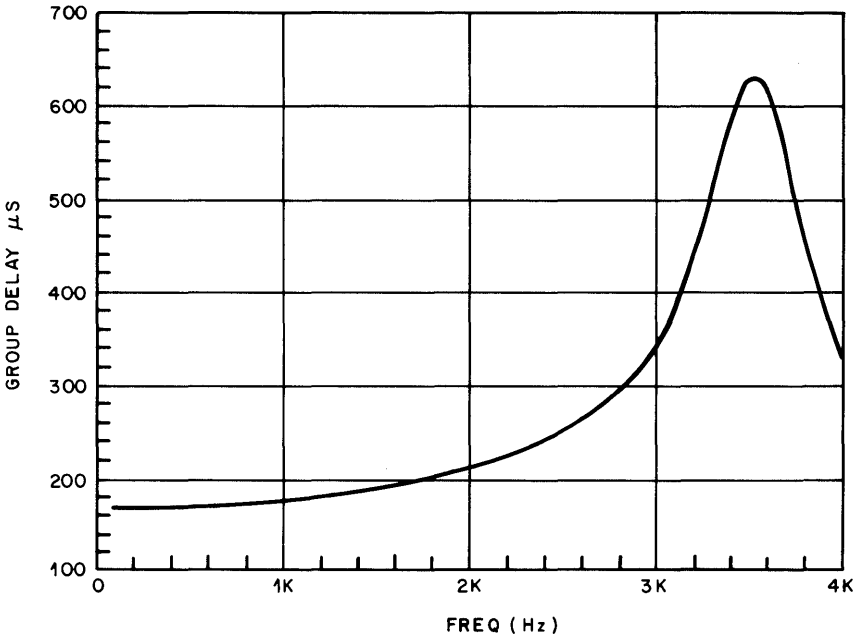


Figure 10. Receive Path Group Delay Response

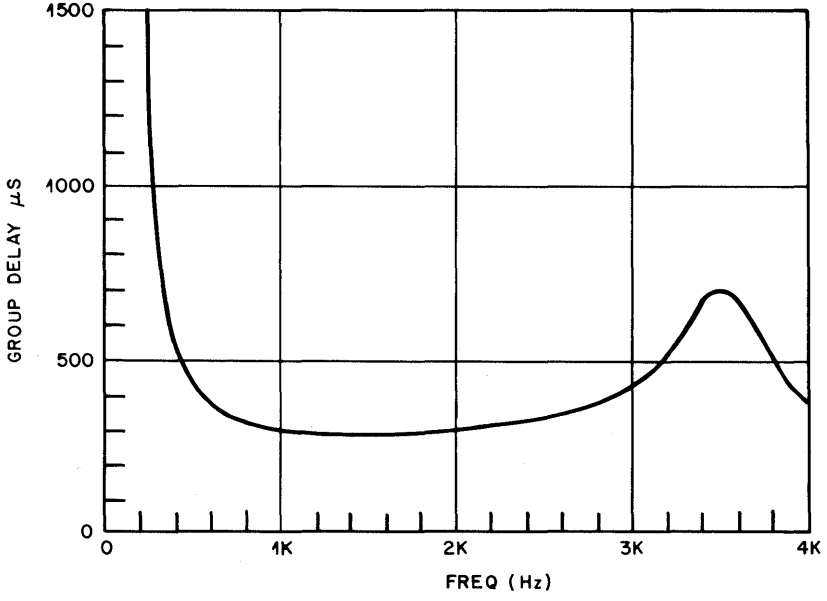


Figure 11. Transmit Path Group Delay Response

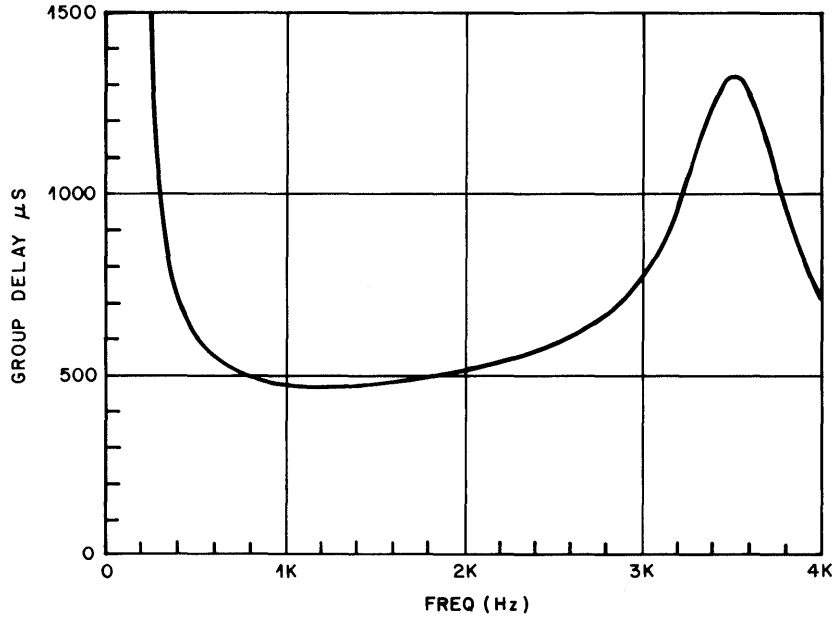


Figure 12. End-to-End Group Delay

Single Frequency Distortion*		
$\frac{\text{Input}}{\text{Max Input}}$ (dB)	Input Frequency (Hz)	$\frac{S}{N+D}$ (In the 0—4 kHz Band) (dB)
0	200 to 3400	60
−10		60
−20		60
−30		55
−40		45

*See Figure 13 for $\frac{S}{N+D}$ curve.

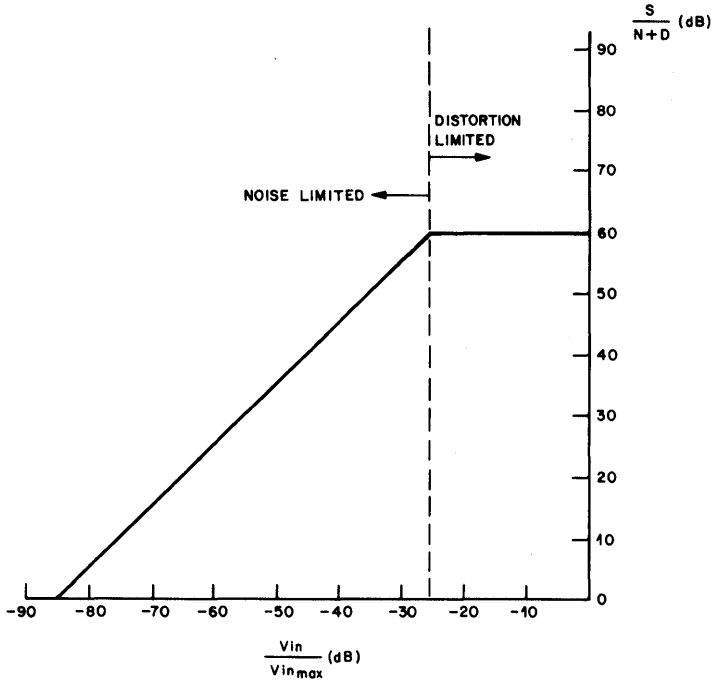


Figure 13. Signal to Impairment Characteristic of the Transmit and Receive Paths

Intermodulation Distortion (4-Tone Method; Input = −13 dBm0)
r2 < 60 dB below input r3 < 60 dB below input

Transmit (Encoder)	Gain	Input Voltage at 1 kHz Corresponding to:		
		Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
TGC = 0	0 dB	1.095	1.578	Vp
TGC = 1	−3.00 dB	1.547	2.229	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to:		
		Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	−3.00 dB	1.547	2.229	Vp
RGC = 0	0 dB	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown on Figure 14, with expanded details on Figure 15. The duty cycle of T2048 and R2048 must be between 45 and 55%. The encoder and decoder can operate back-to-back if RNSYNC=TNSYNC and R2048=T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization Delay	–	10	tCLK –75	ns
tCKLSYH	Synchronization Hold	–	0*	*	ns
tCKHTPV	Transmit Prop Delay	50pF	0	140	ns
tRSVCKL	Receive Set-Up Time	–	50	–	ns
tCKLRSX	Receive Hold Time	–	0	–	ns

*Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first negative going data clock edge (timing edge A on Figure 14) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

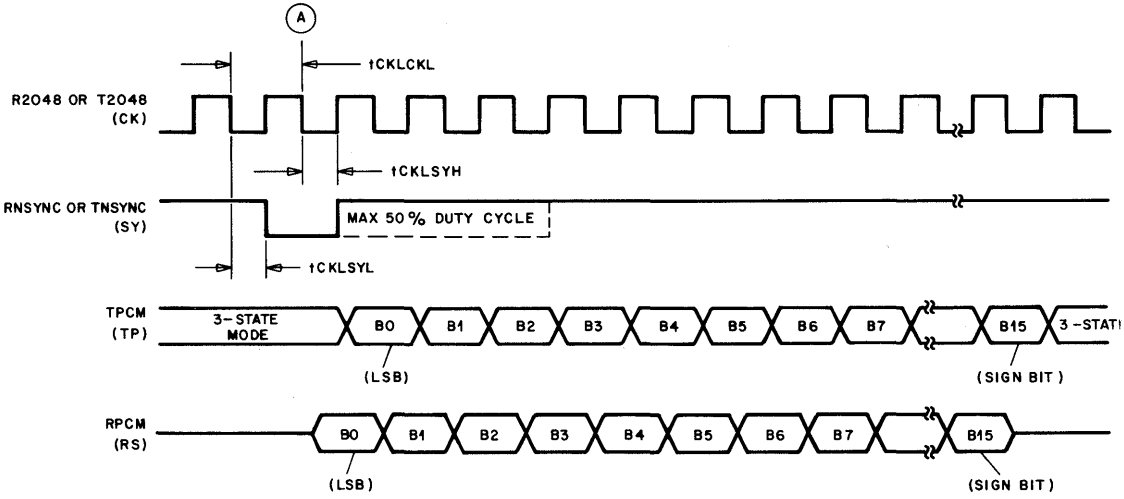


Figure 14. I/O Timing

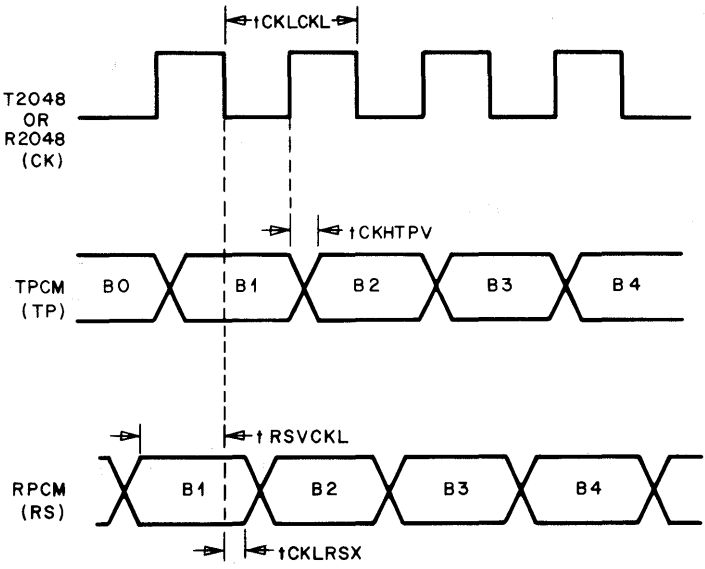


Figure 15. I/O Timing (Enlarged Section)

The information contained herein is preliminary and subject to change.

FEATURES

- A/D and D/A with on-chip D/A filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 100 mW nominal power
- Independent transmit and receive power-down
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format 16-bit PCM in 2s complement binary (LSB first)
- Gain selection – receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR

DESCRIPTION

The T7521 High-Precision PCM Codec Without Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device provides an on-chip reconstruction filter and a precision voltage reference. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM μ-law data. The T7521 Codec is a linear device with 16-bit PCM I/O data in 2s complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. An optional transmit filter may be supplied by the user for this device. The T7521 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

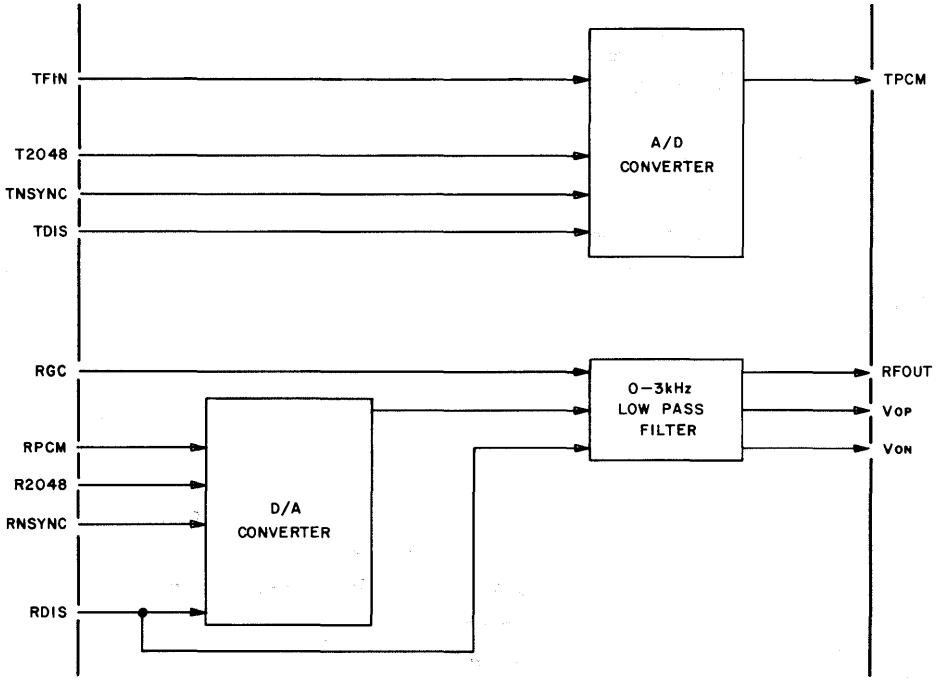
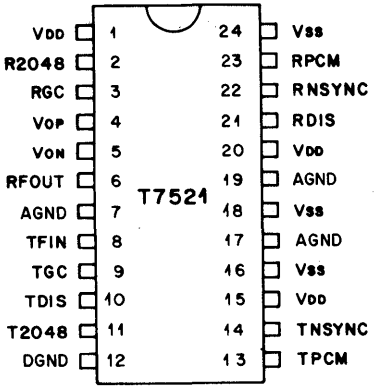


Figure 1. T7521 High-Precision PCM Codec Without Filters Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin(s)
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
RDIS	21	TNSYNC	14
RFOUT	6	TPCM	13
RGC	3	T2048	11
RNSYNC	22	VDD	1, 15, 20
RPCM	23	VON	5
R2048	2	VOP	4
TDIS	10	VSS	16, 18, 24

Figure 2. T7521 Codec Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7521 Pin Descriptions

Symbol	Type	Name/Function
VDD	–	**5 V Supply (±5%).**
R2048	I	**Receive 2.048 MHz Clock.**
RGC	I	**Receive Gain Control.** A high on the pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT	O	**Receive Filter Output.** A 16-bit digital milliwatt reconstructed by the filter produces a 1.547 Vp signal (when RGC is high). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF capacitance.
AGND	–	**Ground (Analog).**
TFIN	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source.
TGC	I	**Transmit Gain Control.** Option not used on this chip. Leave the TGC pin unconnected; do not use this pin as a signal tie point.
TDIS	I	**Transmit Disable.** A high on this pin disables the transmit side; a low or no connection enables the transmit side.
T2048	I	**Transmit 2.048 MHz Clock.**

CAUTION: Cavity cover is internally connected to AGND.

Table 1. T7521 Pin Descriptions (Continued)		
Symbol	**Type**	**Name/Function**
DGND	–	**Ground (Digital).**
TPCM	O	**Transmit PCM.** This pin is used for the 16-bit 2s complement binary PCM (LSB first) output. This pin will be 3-stated when inactive.
TNSYNC	I	**Transmit Synchronization.** An accurate timing pulse (negative going-edge trigger) used to start transmitting the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 9).
VSS	–	**−5 V Supply (±5%).**
RDIS	I	**Receive Disable.** A high on this pin disables the receive side; a low or no connection enables the receive side.
RNSYNC	I	**Receive Synchronization.** An accurate timing pulse (negative going-edge trigger) is used to start reading the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 9).
RPCM	I	**Receive PCM.** This pin is used for the 16-bit PCM 2s complement binary (LSB first) input.
NC	–	**No Connection.**

Application Hints

The T7521 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the VDD pins must be tied together to avoid excessive substrate currents in the chip.

All the VSS pins must be tied together.

All the analog ground pins (AGND) must be tied together.

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8 kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed ground plane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown on Figure 3. The 3 to 5 Ω decoupling resistors in series with VDD and VSS with the 10 μF tantalum or low ESR aluminum capacitor form a low-pass filter (−3 dB frequency of about 5 kHz). The 0.2 μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated noise.

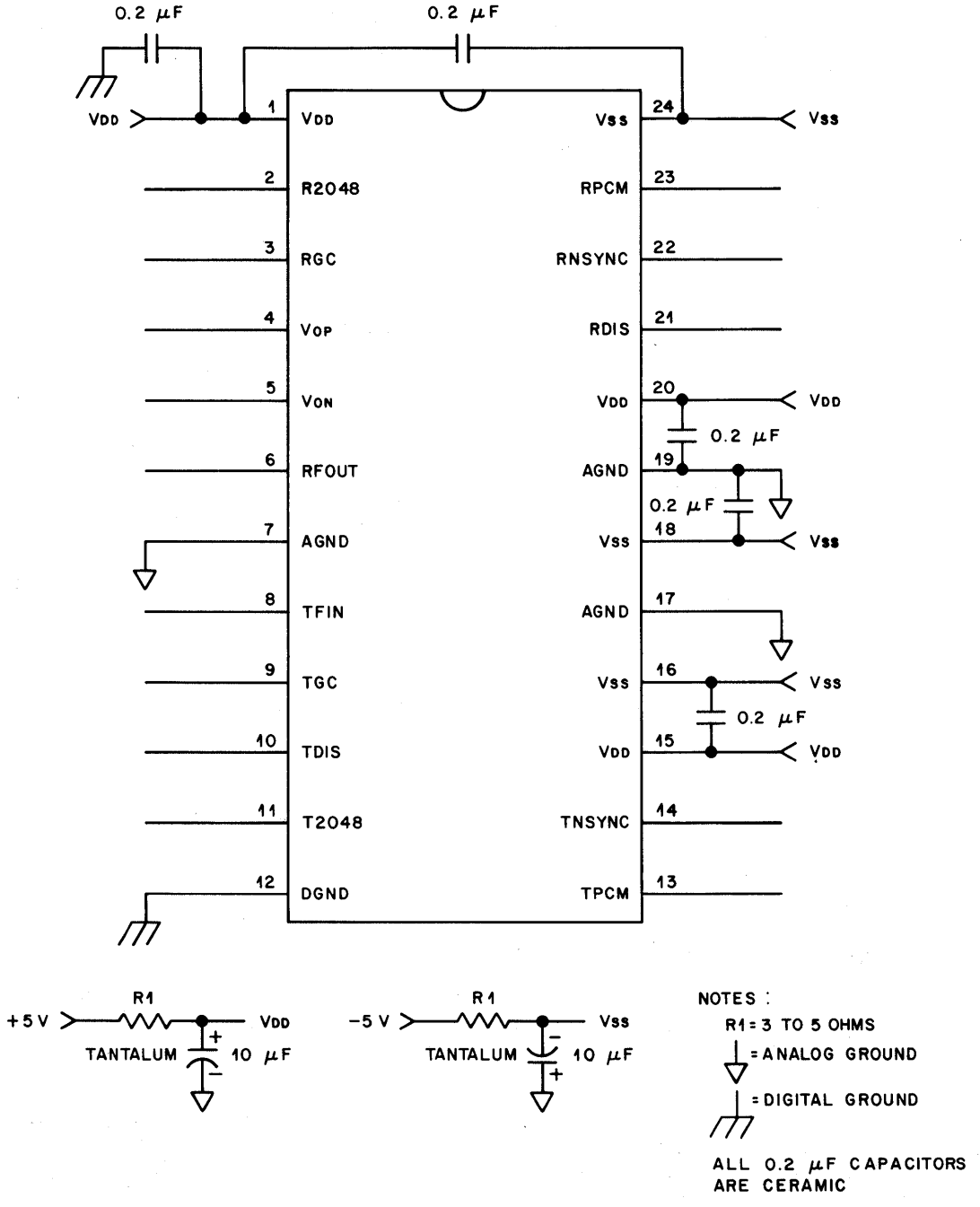


Figure 3. Codec Supply Decoupling

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a) but doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. In short, do not configure clocks in the manner shown on Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown on Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock. The sync clocks must also be locked in phase so that the TNSYNC and T2048 clock edges line up and the RNSYNC and R2048 clock edges line up. This relationship is shown on Figure 4b by the logic blocks run off the master clock, which is driving the codec sync inputs. The timing can be generated by software (in a DSP device, for example), but the sync timing must stay solid with respect to the master clock.

The best noise performance is achieved by using the fully synchronous timing of Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, VOP, and VON) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

Miscellaneous

The TFIN pin must have a dc path to ground. If the A/D signal source is ac coupled to the A/D, a resistor must be connected from TFIN to analog ground.

The A/D input must be driven from a fast settling source (0.1% in 6 μs). The input impedance is 100 k in parallel with 80 pF.

CHARACTERISTICS

Electrical Specifications

Analog Interface

TFIN: Rin > 100 kΩ, Cin < 100 pF
RFOUT: ac impedance < 300 Ω, max current 150 μA
Any input can be between VSS and VDD without damaging the chip.

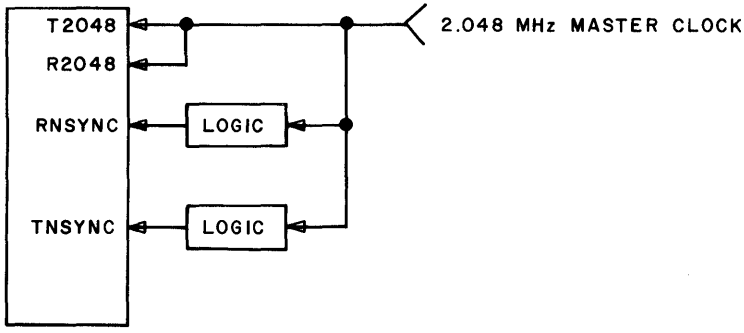
Digital Interface

All inputs: TTL-compatible, Iin < 15 μA, < 5 pF loading
TPCM: Capable of driving a 50 pF capacitance to TTL voltage levels at 2.048 Mbits/s
Any input can be between VSS and VDD without damaging the chip.

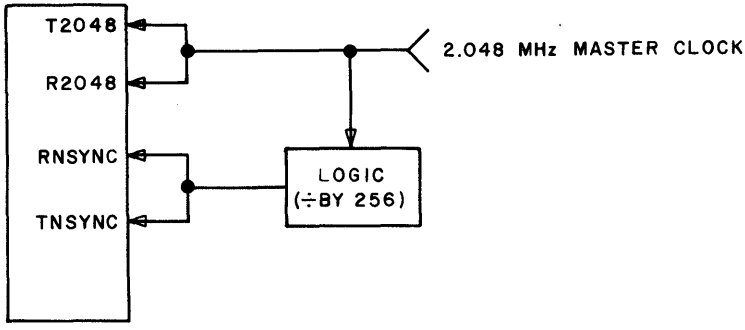
Temperature Range

0 to 70 °C: Meets specifications.

a. Not Recommended (Do Not Do This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Parameter		Limits			Unit
		Min	Typ	Max	
Operating Voltage		±4.75	±5	±5.25	V
Power Disspation					
Active, TDIS=RDIS=0		50	100	200	mW
Inactive, TDIS=RDIS=1		—	20	40	mW
Receive Analog Overload at 1 kHz RGC=1	0 to 70 °C	±2.191	±2.229	±2.268	Vp
Transmit (A/D) Overload at 1 kHz	0 to 70 °C	±2.70	±2.75	±2.80	Vp
Absolute Gain (Gain Contrast) at 1.02 kHz, Full-Scale −3 dB (RGC=0)	0 to 70 °C	−0.15	—	0.15	dB
Gain Tracking Transmit or Receive (1.02 kHz, Full-Scale = 0 dB, −3 dB Reference)					
0 dB to −40 dB		—	—	±0.2	dB
−40 dB to −53 dB		—	—	±0.4	dB
Signal-to-Distortion (1.02 kHz, Full-Scale = 0 dB)					
0 dB to −30 dB		60	—	—	dB
−40 dB		45	—	—	dB
−45 dB		40	—	—	dB
Idle Channel Noise (Transmit)		—	8	14	dBC
Idle Channel Noise (Receive)	RGC=1	—	6	9	dBC
	RGC=0	—	3	6	dBC
Power Supply Rejection (End-to-End)					
1 kHz		35	—	—	dB
0—100 kHz White Noise		30	—	—	dBC
Absolute Delay (End-to-End), 1 kHz		—	—	575	μs

Note: 0 dBm = 90 dB = 0.775 Vrms (into 600 Ω)

Overload (1.00 kHz) Compression (Receive, RGC = HIGH)	
Input/Overload Level (dB)	**Max Increased Loss (dB) Relative to Overload −3 dB**
0	0.2
3	1.8
6	4.6

Note: The filter responses scale linearly with the master clock.

In the following tables and associated figures, the ac characteristics assume the master clock (R2048) to be 2.048 MHz ± 100 ppm.

Frequency Response*	
Freq (Hz)	**Receive Loss (dB)**
200	−0.05 to +0.2
300—3000	±0.125
3200	−0.125 to +0.75
3400	0.2 to 0.9
4000	>14
≥4600	>28
3400—4600	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$

*See Figures 5 and 6 for receive response curves.

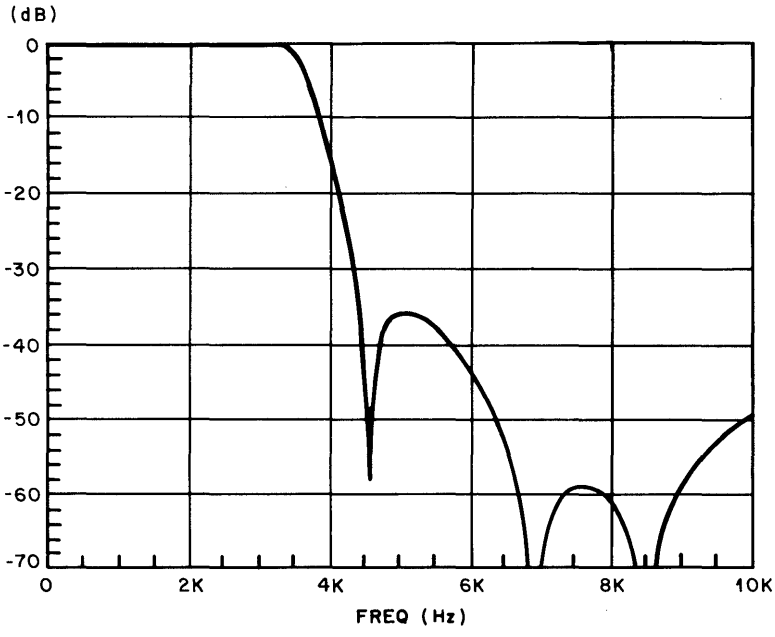


Figure 5. Receive Path Frequency Response

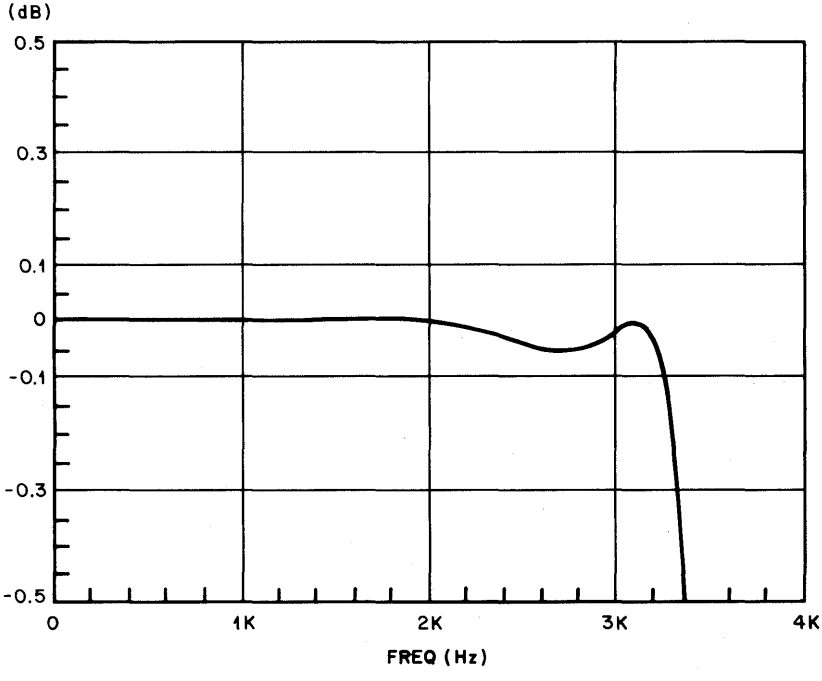


Figure 6. Receive Path Voice Band Response

Phase and Delay Distortion (End-to-End)*		
Freq (Hz)	**Phase Deviation from Linearity (Radians)**	**Delay Distortion (μs, max)**
<500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	–
500–700		300
700–2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at ±0.95 radians and 1850 Hz	75
2000–2500		150
2500–2700		200
2700–3000		375
>3000	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	–

*See Figures 6 and 7 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) <−71 dB

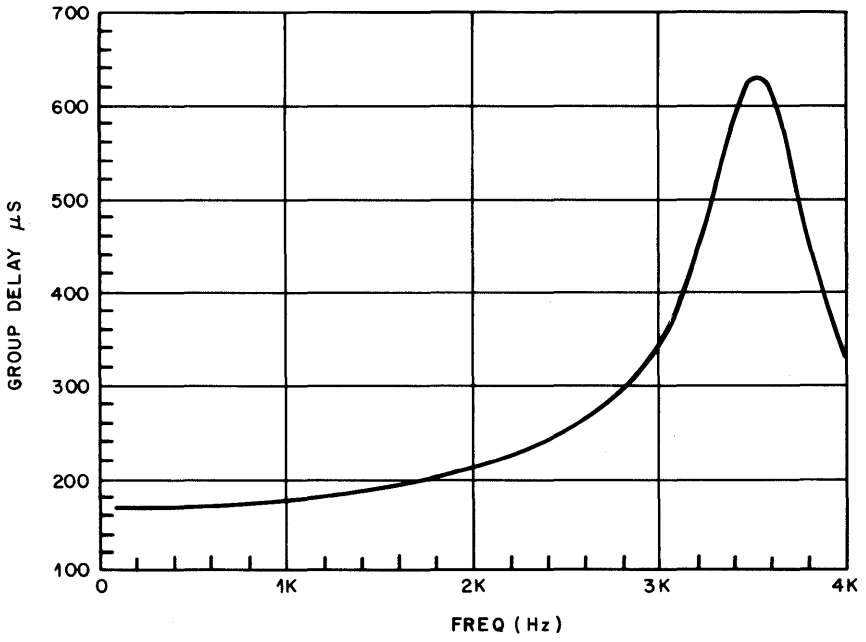


Figure 7. Receive Path Group Delay Response

Single Frequency Distortion*		
Input / Max Input (dB)	Input Frequency (Hz)	S/(N+D) (In the 0—4 kHz Band) (dB)
0	0 to 4000	−60
−10		−60
−20		−60
−30		−55
−40		−45

*See Figure 8 for S/(N + D) curve.

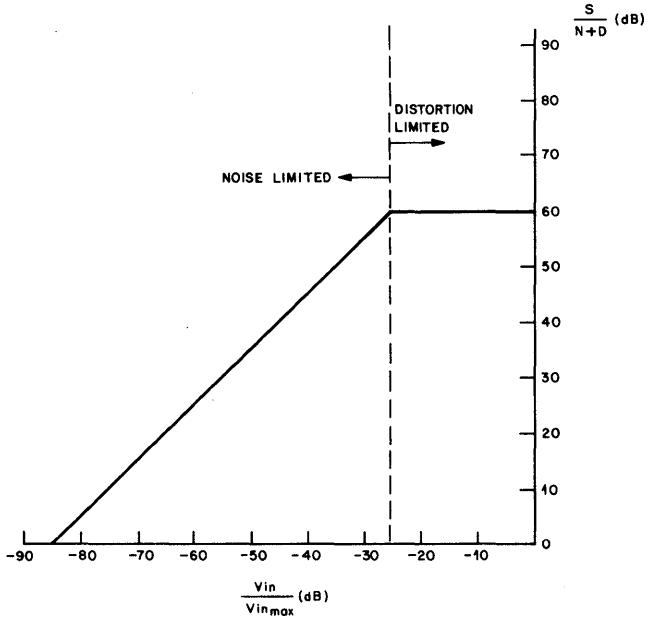


Figure 8. Signal to Impairment Characteristic of the Transmit and Receive Paths

Intermodulation Distortion (4-Tone Method; Input = − 13 dBm0)
r2 < 60 dB below input r3 < 60 dB below input

Transmit (A/D)	Gain	Input Voltage at 1 kHz Corresponding to: Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
—	0.0 dB	1.908	2.75	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to: Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	3.00 dB	1.547	2.229	Vp
RGC = 0	0 dB	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown on Figure 9, with expanded details on Figure 10. The duty cycle of T2048 and R2048 must be between 45 and 55%. The encoder and decoder can operate back-to-back if RNSYNC=TNSYNC and R2048=T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization Delay	—	10	tCLK −75	ns
tCKLSYH	Synchronization Hold	—	0*	*	ns
tCKHTPV	Transmit Prop Delay	50 pF	0	140	ns
tRSVCKL	Receive Set-Up Time	—	50	—	ns
tCKLRSX	Receive Hold Time	—	0	—	ns

*Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first negative going data clock edge (timing edge A on Figure 9) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

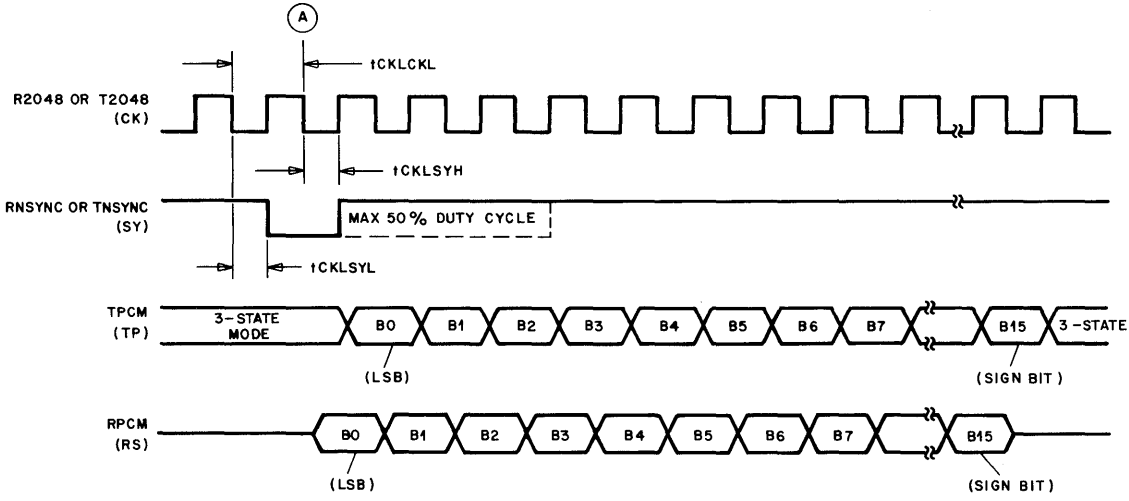


Figure 9. I/O Timing

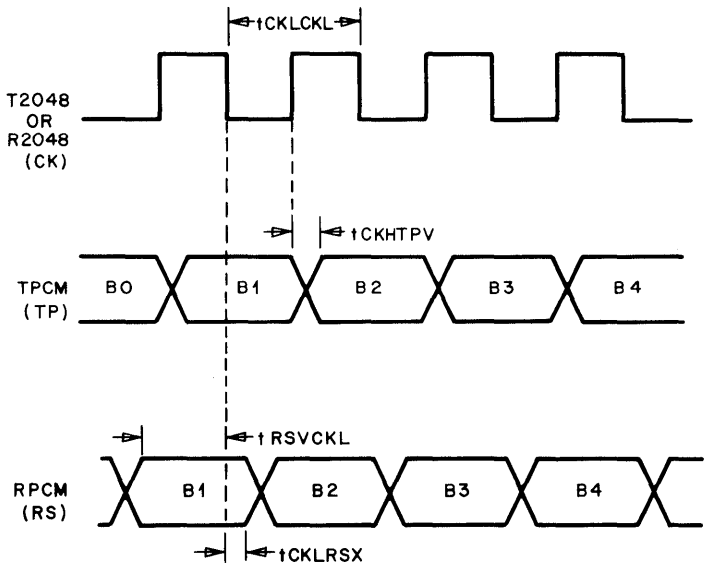


Figure 10. I/O Timing (Enlarged Section)

The information contained herein is preliminary and subject to change.

FEATURES

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120 mW nominal power
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format 16-bit PCM in 2s complement binary (LSB or MSB first)
- Gain selection – transmit: 0 or −3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR
- Filter/without filter selection

DESCRIPTION

The T7522 High-Precision PCM Codec with Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device provides anti-aliasing filters and a precision voltage reference. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM μ-law data. The T7522 Codec is a linear device with 16-bit PCM I/O data in 2s complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. This chip has programmable capabilities as LSB or MSB first I/O. The T7522 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

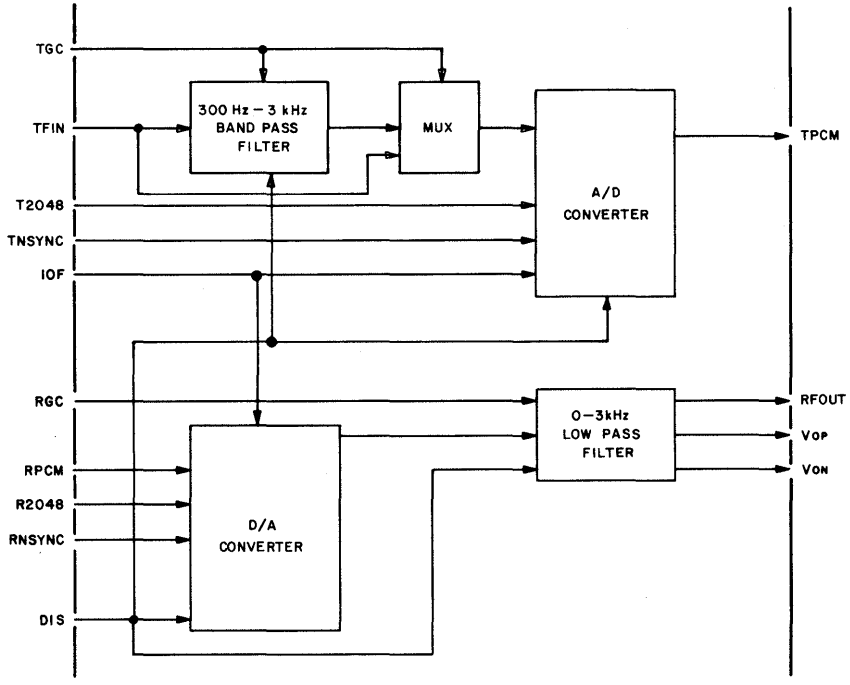
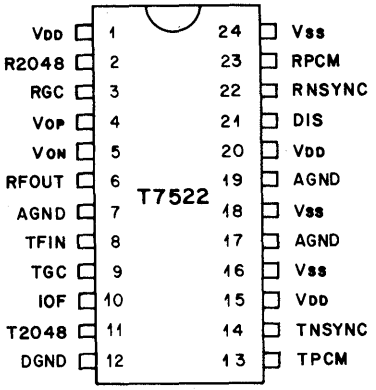


Figure 1. T7522 High-Precision PCM Codec With Filters Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin(s)
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
DIS	21	TNSYNC	14
IOF	10	TPCM	13
RFOUT	6	T2048	11
RGC	3	VDD	1, 15, 20
RNSYNC	22	VON	5
RPCM	23	VOP	4
R2048	2	VSS	16, 18, 24

Figure 2. T7522 Codec Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7522 Pin Descriptions

Symbol	Type	Name/Function
VDD	–	**5 V Supply (±5%).**
R2048	I	**Receive 2.048 MHz Clock.**
RGC	I	**Receive Gain Control.** A high on this pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT	O	**Receive Filter Output.** A 16-bit digital milliwatt reconstructed by the filter produces a 1.547 Vp signal (when RGC is high). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF capacitance.
AGND	–	**Ground (Analog).**
TFIN	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source.
TGC	I	**Transmit Gain Control.** A high on this pin sets the transmit gain to −3 dB; a low or open sets the gain to 0 dB. To bypass the bandpass filter, tie TGC to VSS.
IOF	I/O	**Input/Output Format.** A high sets I/O format to MSB first; a low or no connection sets the I/O format to LSB first.
T2048	I	**Transmit 2.048 MHz Clock.**
DGND	–	**Ground (Digital).**

CAUTION: Cavity cover is internally connected to AGND.

Table 1. T7522 Pin Descriptions (Continued)		
Symbol	**Type**	**Name/Function**
TPCM	O	**Transmit PCM.** This pin is used for the 16-bit 2s complement binary PCM (LSB or MSB first) output. (See IOF for PCM format.) This pin will be 3-stated when inactive.
TNSYNC	I	**Transmit Synchronization.** An accurate timing pulse (negative going edge trigger) used to start transmitting the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 14).
VSS	–	**−5 V Supply (±5%).**
DIS	I	**Chip Disable.** A high on this pin disables the chip (chip powered down); a low or no connection enables the chip.
RNSYNC	I	**Receive Synchronization.** An accurate timing pulse (negative going edge trigger) is used to start reading the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 14).
RPCM	I	**Receive PCM.** This pin is used for the 16-bit PCM 2s complement binary (LSB or MSB first) input. (See IOF for PCM format.)
NC	–	**No Connection.**

Application Hints

The T7522 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the VDD pins must be tied together to avoid excessive substrate currents in the chip.

All VSS pins must be tied together.

All the analog ground pins (AGND) must be tied together.

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8 kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed ground plane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown on Figure 3. The 3 to 5 Ω decoupling resistors in series with VDD and VSS with the 10 μF tantalum or low ESR aluminum capacitor form a low-pass filter (−3 dB frequency of about 5 kHz). The 0.2 μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated noise.

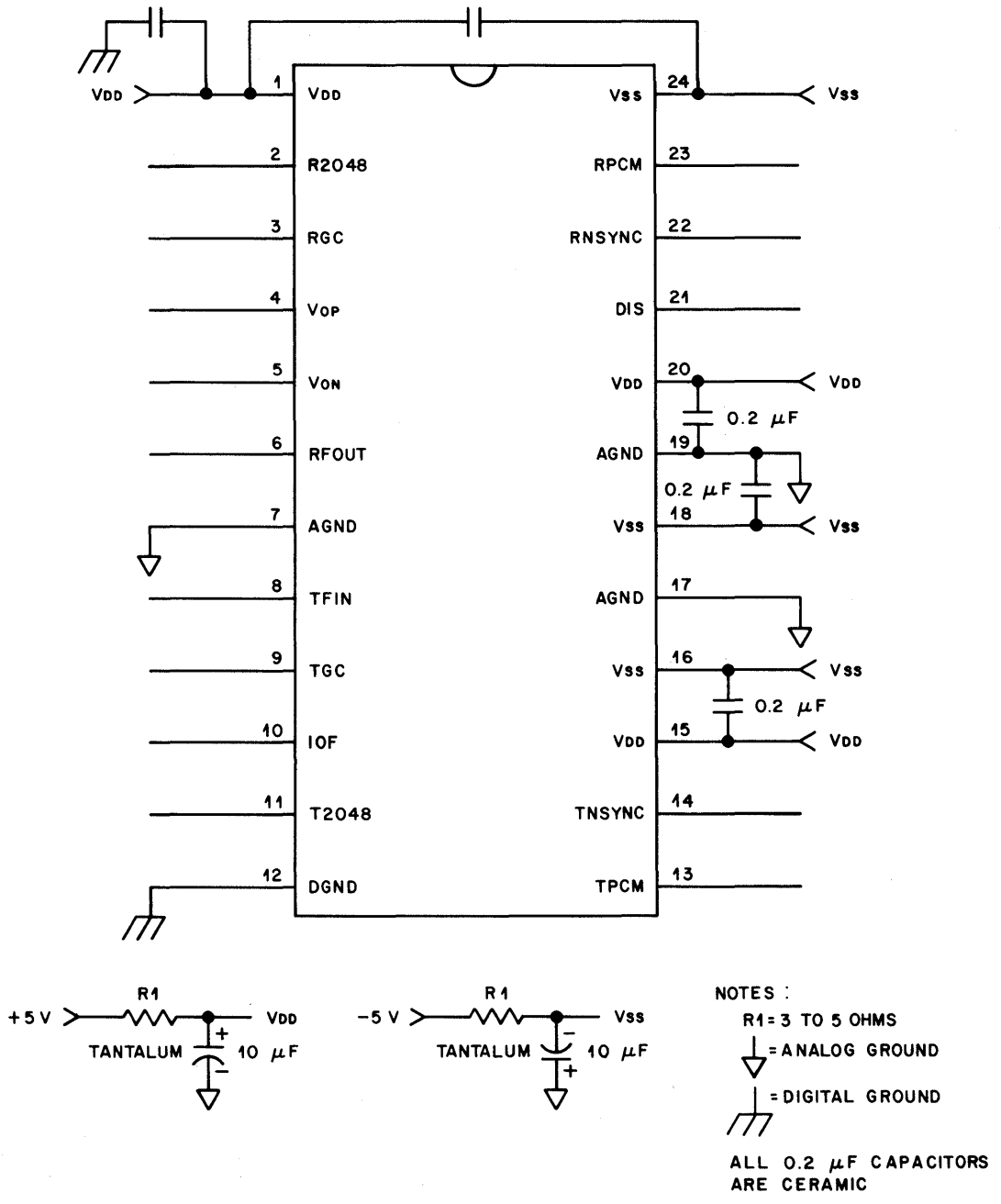


Figure 3. Codec Supply Decoupling

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a) but doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. In short, do not configure clocks in the manner shown on Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown on Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock. The sync clocks must also be locked in phase so that the TNSYNC and T2048 clock edges line up and the RNSYNC and R2048 clock edges line up. This relationship is shown on Figure 4b by the logic blocks run off the master clock, which is driving the codec sync inputs. The timing can be generated by software (in a DSP device, for example), but the sync timing must stay solid with respect to the master clock.

The best noise performance is achieved by using the fully synchronous timing of Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, VOP, and VON) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

CHARACTERISTICS

Electrical Specifications

Analog Interface

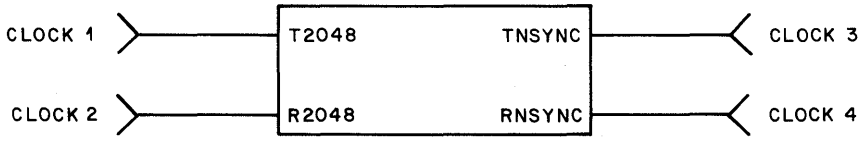
TFIN: Rin > 100 kΩ and Cin < 10 pF, when TGC = logic 1 or 0
Rin > 100 kΩ and Cin < 100 pF, when TGC = VSS
RFOUT: ac impedance < 300Ω, max current 150 μA
Any input can be between VSS and VDD without damaging the chip.

Digital Interface

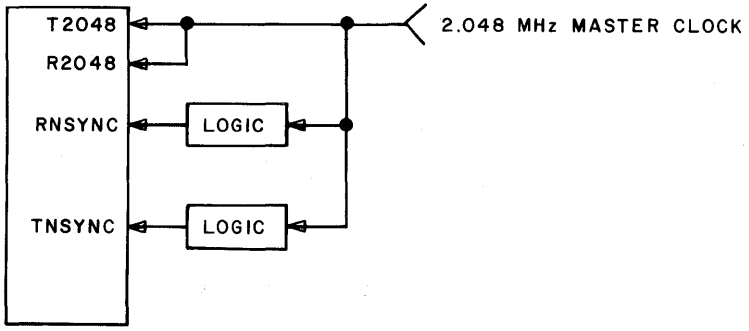
All inputs: TTL-compatible, Iin < 15 μA, < 5 pF loading
TPCM: Capable of driving a 50 pF capacitance to TTL voltage levels at 2.048 Mbits/s
Any input can be between VSS and VDD without damaging the chip.

Temperature Range

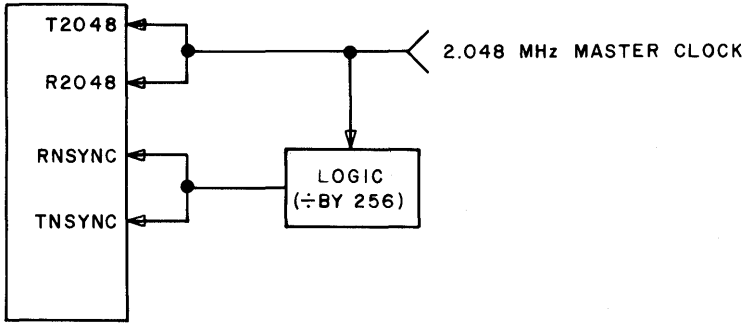
0 to 70 °C: Meets specifications.



a. Not Recommended (Do Do Not This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Parameter		Limits Min	Typ	Max	Unit
Operating Voltage		±4.75	±5	±5.25	V
Power Dissipation					
Active, DIS=0		50	120	200	mW
Inactive, DIS=1		–	15	40	mW
Analog Overload at 1 kHz TGC=RGC=1	0 to 70 °C	±2.191	±2.229	±2.268	Vp
Transmit (A/D) Overload at 1 k Hz TGC=VSS	0 to 70 °C	±2.70	±2.75	±2.80	Vp
Absolute Gain (Gain Contrast) at 1.02 kHz, Full-Scale −3 dB Input TGC=0, RGC=0	0 to 70 °C	−0.15	–	0.15	dB
Gain Tracking Transmit or Receive (1.02 kHz, 0 dB = Full-Scale Input, −3 dB Reference)					
0 dB to −40 dB		–	–	±0.2	dB
−40 dB to −53 dB		–	–	±0.4	dB
Signal-to-Distortion: Transmit or Receive (1.02 kHz) (0 dB = Full-Scale Input)					
0 dB to −25 dB		60	–	–	dB
−40 dB		45	–	–	dB
−45 dB		40	–	–	dB
Idle Channel Noise (Transmit)	TGC=1 or 0	–	9	13	dBC
	TGC=VSS	–	6	9	dBC
Idle Channel Noise (Receive)	RGC=1	–	6	9	dBC
	RGC=0	–	3	6	dBC
Power Supply Rejection (End-to-End)					
1 kHz		35	–	–	dB
0–100 kHz White Noise		30	–	–	dBC
Absolute Delay (End-to-End), 1 kHz		–	–	575	μs
DC Offset	Receive Path	–	8	140	mV
TGC=0,1	Transmit Path	–	35	235	LSB
TGC=VSS	Transmit Path	–	6	20	LSB

Note: 0 dBm = 90 dB = 0.775 Vrms (into 600 Ω)

Overload (1.00 kHz) Compression	
Input/Overload Level (dB)	**Max Increased Loss (dB) Relative to Overload −3 dB**
0	0.2
3	1.8
6	4.6

Note: The filter responses scale linearly with the master clock.

In the following tables and associated figures, the ac characteristics assume the master clock (T2048, R2048) to be 2.048 MHz ± 100 ppm.

Frequency Response*		
Freq (Hz)	**Transmit Loss (dB)**	**Receive Loss (dB)**
50—60	≥20	±0.2
200	0.1 to 1.8	−0.05 to +0.2
300—3000	±0.125	±0.125
3200	−0.125 to +0.75	−0.125 to +0.75
3400	0.2 to 0.9	0.2 to 0.9
4000	>14	>14
≥4600	>32	>28
3400—4000	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$
4000—4600	$> 18 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - \frac{7}{9} \right]$	

*See Figures 5 through 9 for response curves.

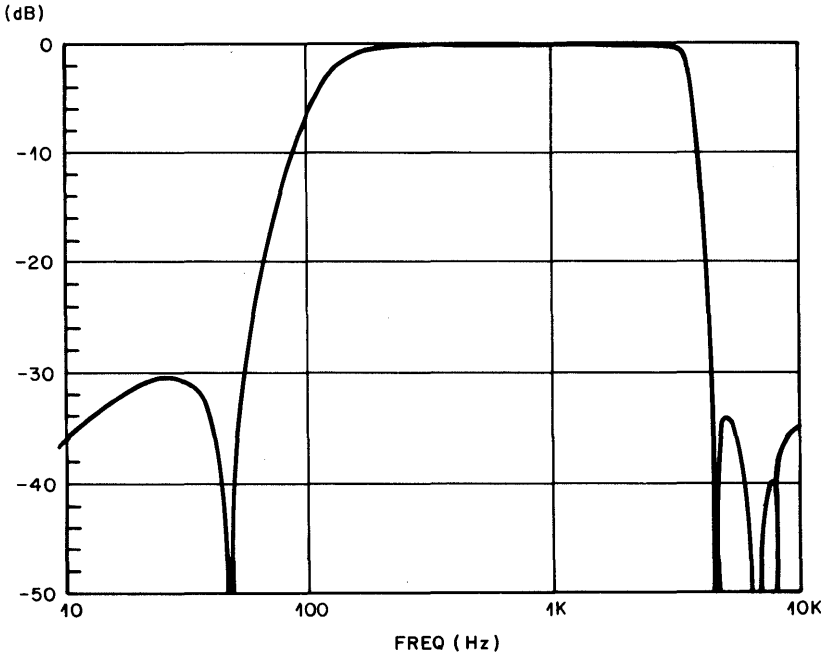


Figure 5. Transmit Path Frequency Response

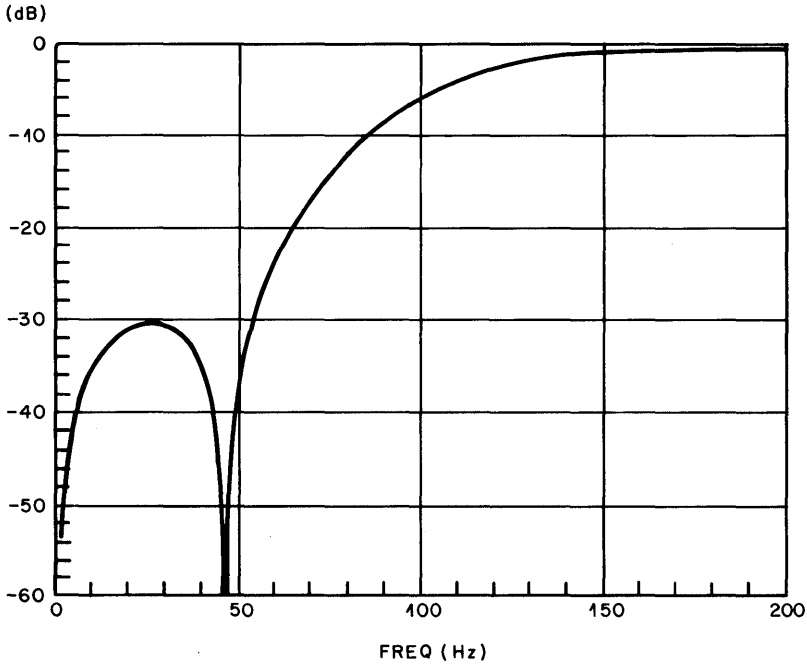


Figure 6. Transmit Path Low Frequency Response

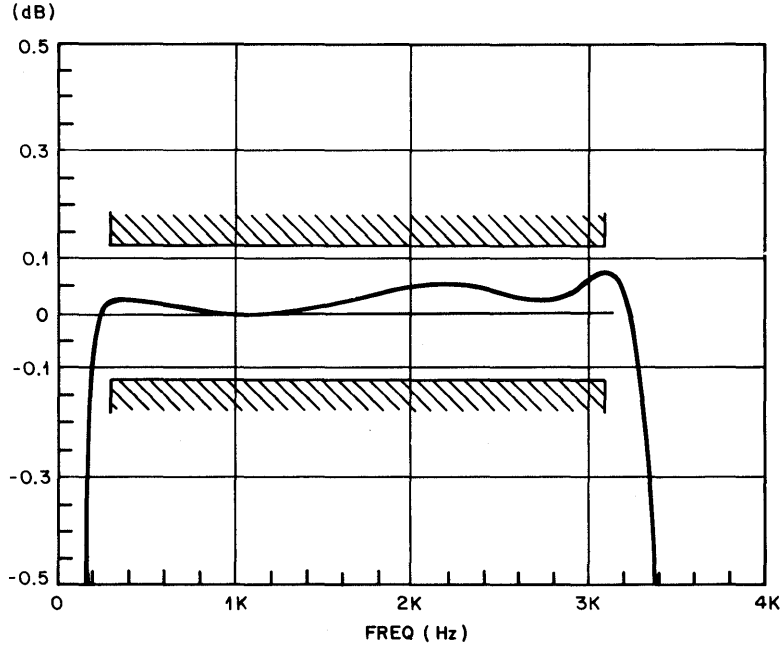


Figure 7. Transmit Path Voice Band Response

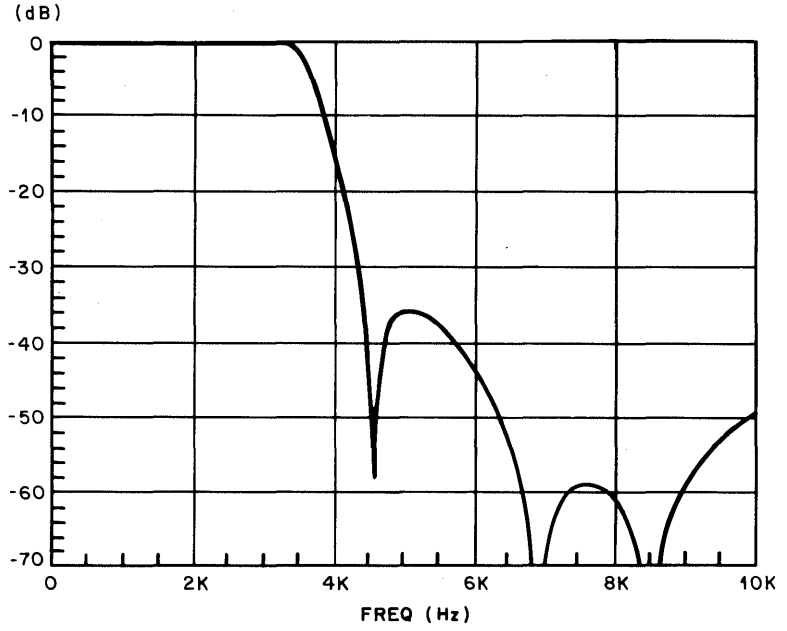


Figure 8. Receive Path Frequency Response

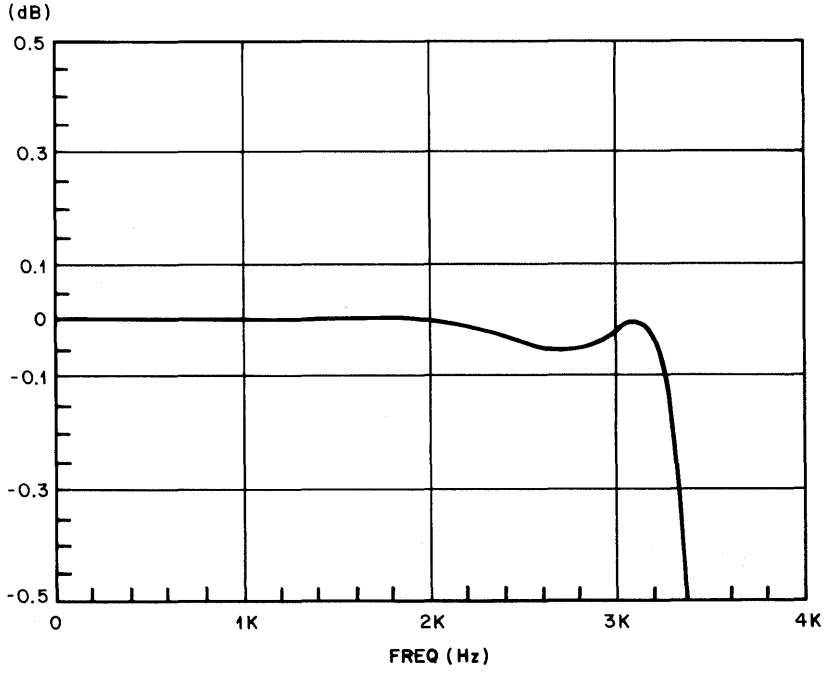


Figure 9. Receive Path Voice Band Response

Phase and Delay Distortion (End-to-End)*		
Freq (Hz)	**Phase Deviation from Linearity (Radians)**	**Delay Distortion (μs, max)**
<500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	–
500–700		300
700–2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at ±0.95 radians and 1850 Hz	75
2000–2500		150
2500–2700		200
2700–3000		375
>3000	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	–

*See Figures 10, 11, and 12 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) <−71 dB

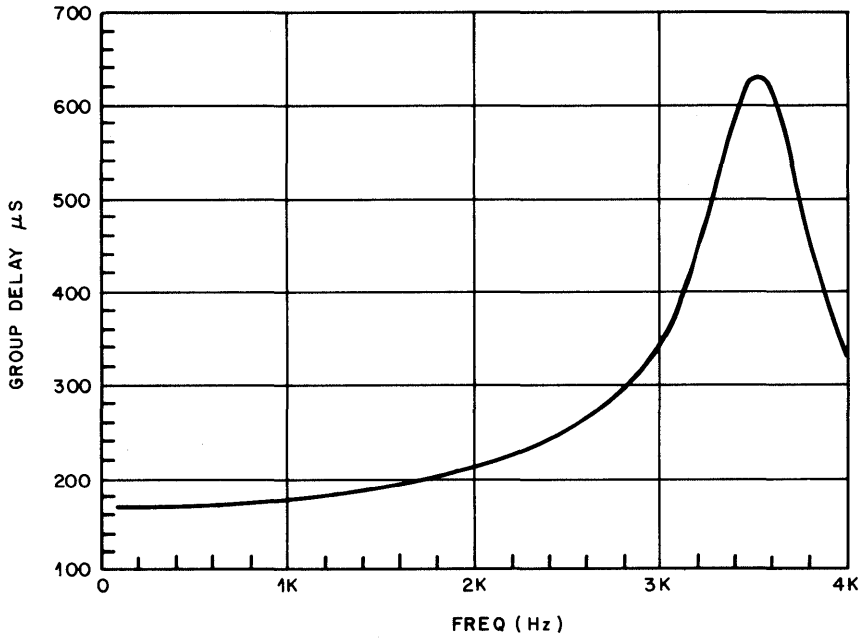


Figure 10. Receive Path Group Delay Response

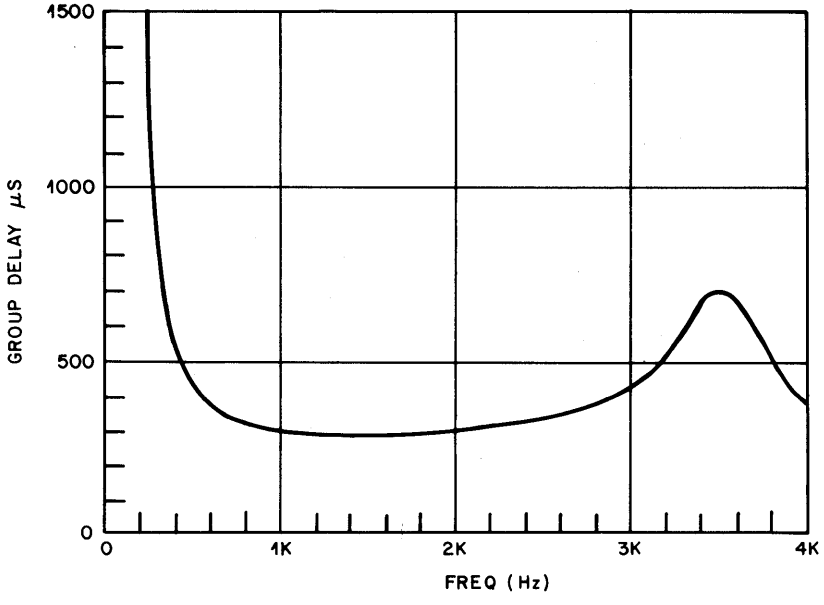


Figure 11. Transmit Path Group Delay Response

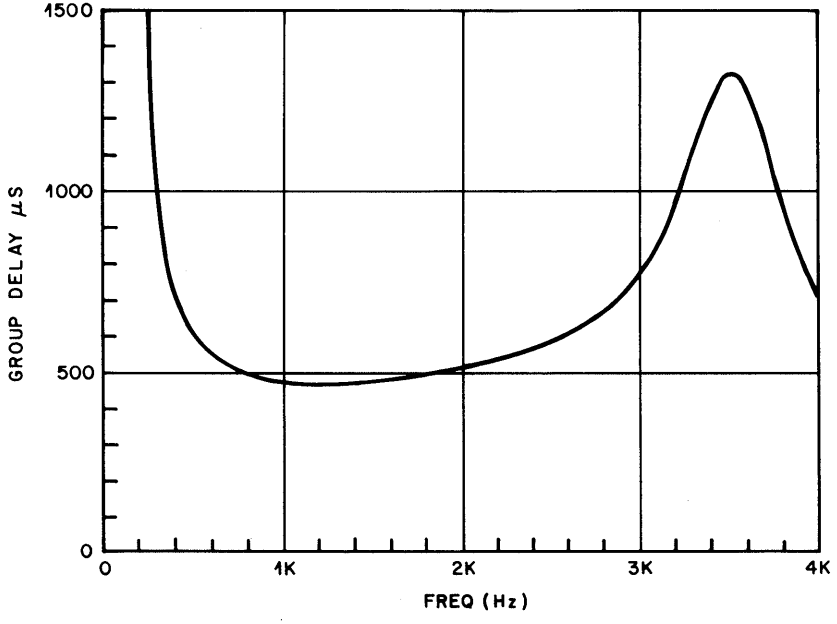


Figure 12. End-to-End Group Delay

Single Frequency Distortion*		
Input / Max Input (dB)	Input Frequency (Hz)	S / N + D (In the 0—4 kHz Band) (dB)
0	200 to 3400	60
−10		60
−20		60
−30		55
−40		45

*See Figure 13 for $\frac{S}{N+D}$ curve.

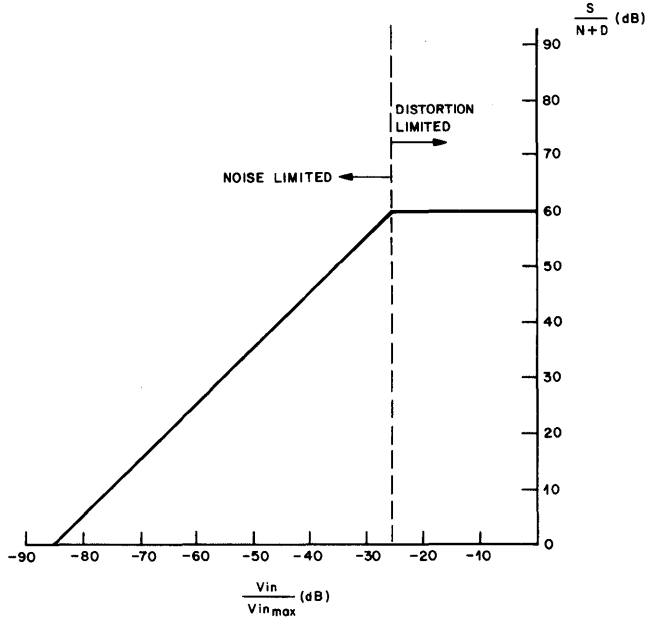


Figure 13. Signal to Impairment Characteristic of the Transmit and Receive Paths

Intermodulation Distortion (4 Tone Method; Input = −13 dBm0)
r2 < 60 dB below input r3 < 60 dB below input

Transmit (Encoder)	Gain	Input Voltage at 1 kHz Corresponding to:		
		Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
TGC = 0	0 dB	1.095	1.578	Vp
TGC = 1	−3.00 dB	1.547	2.229	Vp
TGC = VSS	—	1.908	2.750	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to:		
		Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	−3.00 dB	1.547	2.229	Vp
RGC = 0	0 dB	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown on Figure 14, with expanded details on Figure 15. The duty cycle of T2048 and R2048 must be between 45 and 55%. The encoder and decoder can operate back-to-back if RNSYNC=TNSYNC and R2048=T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization Delay	—	10	tCLK −75	ns
tCKLSYH	Synchronization Hold	—	0*	*	ns
tCKHTPV	Transmit Prop Delay	50 pF	0	140	ns
tRSVCKL	Receive Set-Up Time	—	50	—	ns
tCKLRSX	Receive Hold Time	—	0	—	ns

*Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first negative going data clock edge (timing edge A on Figure 14) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

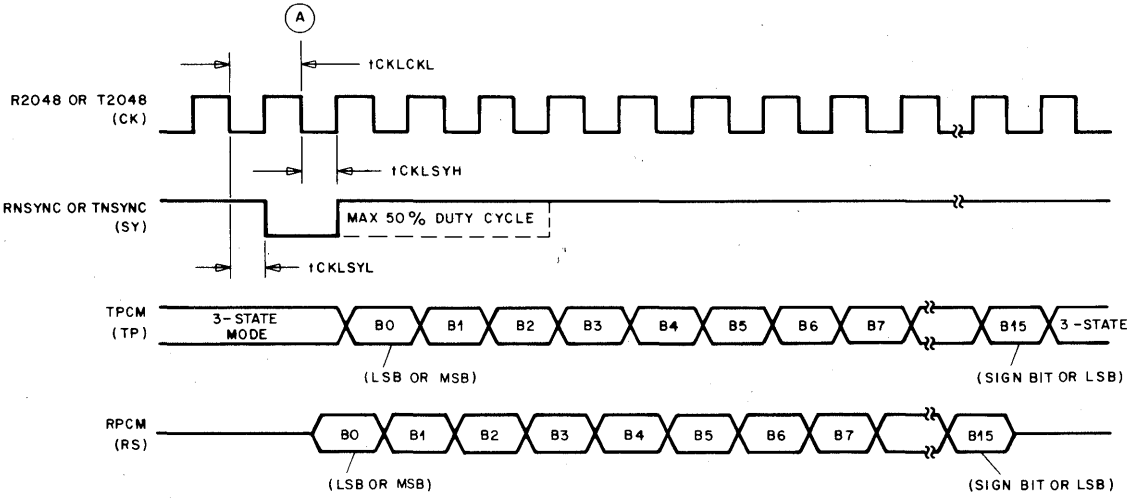


Figure 14. I/O Timing

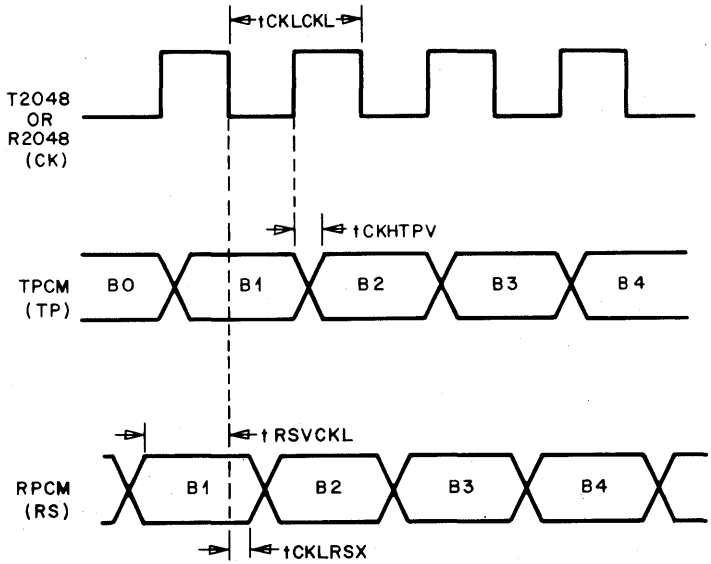


Figure 15. I/O Timing (Enlarged Section)

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FEATURES

The information contained herein is preliminary and subject to change.

- Programmable DES ciphering modes
  - Electronic codebook (ECB)
  - Cipher block chaining (CBC)
  - 1-, 8- or 64-bit cipher feedback (CFB)
  - Output feedback (OFB)
- Ciphering rates of 235,000 operations/second for any of the DES modes. Data throughput of 1.882 Mbytes/s using 64-bit DES output block
- On-chip RAM and ROM program memory
- Flags readable on the data bus or independent output pins
- Four sets of key and initial value registers
- Separate plain text and cipher text parallel (8-bit) ports
- Separate plain text and cipher text serial ports
- Separate serial key input port
- ECB program available in ROM

DESCRIPTION

The T7000A Digital Encryption Processor (DEP) is a programmable integrated circuit that provides a low-cost, high-security, cryptographic system for encrypting and decrypting digital signals. It is manufactured using CMOS technology, requires a single 5 V supply, and is supplied in a 40-pin plastic DIP. It implements four data encryption standard (DES) modes and is capable of performing multiple encryption operations or multiplexed key and initial value ciphering.

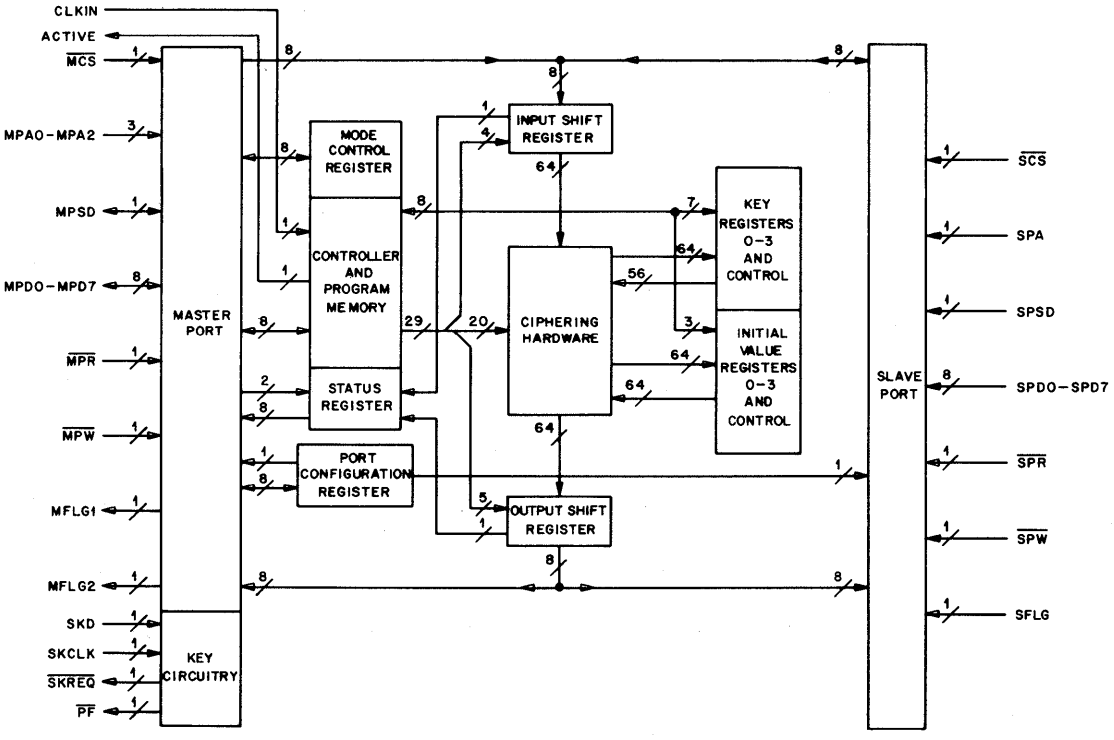
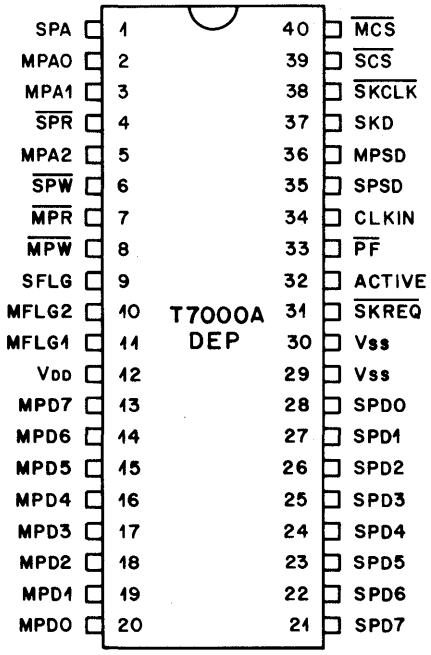


Figure 1. T7000A Digital Encryption Processor Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin
ACTIVE	32	SCS	39
CLKIN	34	SFLG	9
MCS	40	SKCLK	38
MFLG1	11	SKD	37
MFLG2	10	SKREQ	31
MPA0	2	SPA	1
MPA1	3	SPD0	28
MPA2	5	SPD1	27
MPD0	20	SPD2	26
MPD1	19	SPD3	25
MPD2	18	SPD4	24
MPD3	17	SPD5	23
MPD4	16	SPD6	22
MPD5	15	SPD7	21
MPD6	14	SPR	4
MPD7	13	SPSD	35
MPR	7	SPW	6
MPSD	36	VDD	12
MPW	8	VSS	29
PF	33	VSS	30

Figure 2. T7000A DEP Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7000A Pin Descriptions

Pin	Symbol	Type	Name/Function
1	SPA	I	**Slave Port Address.** When high (1), the contents of the status register can be read, but not written, to the slave port data bus. When low (0), either the input shift register (ISR) or output shift register (OSR) is accessed, depending on the port configuration programmed.
2 3	MPA0 MPA1	I I	**Master Port Address Bits 0 and 1.** Used with MPA2 (pin 5) for internal register selection.
4	SPR	I	**Slave Port Read.** Used with SPA (pin 1) to read from the output shift register (if the slave port is programmed as an output) or from the status register. Data is available on the slave port data bus following the falling edge of the pulse and remains on the bus as long as the SPR is low (0). SPW (pin 6) should be held high during a read pulse.
5	MPA2	I	**Master Port Address Bit 2.** Used with MPA0 and MPA1 (pins 2 and 3) for internal register selection.

Table 1. T7000A Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
6	$\overline{\text{SPW}}$	I	**Slave Port Write.** Used with SPA (pin 1) to write to the input shift register if the slave port has been programmed as an input. The data input is latched on the rising edge of the write pulse. $\overline{\text{SPR}}$ (pin 4) should be held high (1) during the write pulse.
7	$\overline{\text{MPR}}$	I	**Master Port Read.** Used with the master port address bus to read one of the internal registers. Data is available on the master port data bus following the falling edge of the pulse and remains on the bus as long as $\overline{\text{MPR}}$ is low (0). $\overline{\text{MPW}}$ (pin 8) should be held high (1) during the read pulse.
8	$\overline{\text{MPW}}$	I	**Master Port Write.** This lead is used with the master port address bus to write to one of the internal registers. The data input is latched into the addressed register on the rising edge of the write pulse. The $\overline{\text{MPR}}$ lead should be held high during the write pulse.
9	SFLG	O	**Slave Flag.** This active-high output indicates the status of either the input or output shift registers, depending on the port configuration programmed.* If the slave port is programmed as an input, the slave flag reflects the contents of the ISRFULL flag (status register – bit 4). If the slave port is programmed as an output, then the slave flag reflects the contents of the OSREMPTY flag (status register – bit 5). Both of these conditions can be read from the status register.
10	MFLG2	O	**Master Flag 2.** This active-high output indicates the status of the ISRFULL flag (status register – bit 4). This condition may also be read from the status register.*
11	MFLG1	O	**Master Flag 1.** This active-high output indicates the status of either the input or output shift register, depending on the port configuration programmed.* If the master port is programmed as an input, this lead reflects the contents of the ISRFULL flag (status register – bit 4). If the master port is programmed as an output, this pin indicates the contents of the OSREMPTY flag (status register – bit 5). If the master port is programmed as both input and output, this pin indicates the contents of the OSRFULL flag and MFLG2 (pin 10) indicates the contents of the ISRFULL flag. The status of the input and output shift register can also be read from the status register.
12	V_{DD}	–	**5 V Supply.**
13	MPD7	I/O	**Master Port Data Bit 7.**
14	MPD6	I/O	**Master Port Data Bit 6.**
15	MPD5	I/O	**Master Port Data Bit 5.** Bidirectional,
16	MPD4	I/O	**Master Port Data Bit 4.** 8-bit Master Port
17	MPD3	I/O	**Master Port Data Bit 3.** I/O bus.
18	MPD2	I/O	**Master Port Data Bit 2.**
19	MPD1	I/O	**Master Port Data Bit 1.**
20	MPD0	I/O	**Master Port Data Bit 0.**

*See Table 5

Table 1. T7000A Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
21	SPD7	I/O	**Slave Port Data Bit 7.**
22	SPD6	I/O	**Slave Port Data Bit 6.**
23	SPD5	I/O	**Slave Port Data Bit 5.** Bidirectional,
24	SPD4	I/O	**Slave Port Data Bit 4.** 8-bit Slave Port
25	SPD3	I/O	**Slave Port Data Bit 3.** I/O bus.
26	SPD2	I/O	**Slave Port Data Bit 2.**
27	SPD1	I/O	**Slave Port Data Bit 1.**
28	SPD0	I/O	**Slave Port Data Bit 0.**
29	VSS	—	**Ground.**
30	VSS	—	**Ground.**
31	$\overline{\text{SKREQ}}$	O	**Serial Key Request.** This active-low output indicates the DEP is expecting a key input. Active when IO Serial Act is programmed. The condition of this flag can be read from the status register.
32	ACTIVE	O	This active-high output flag is set by the microcode instruction IO ACT.
33	$\overline{\text{PF}}$	O	**Parity Fail.** When this output is low it indicates that one or more key input bytes had even parity. This flag is set on the 8th $\overline{\text{MPW}}$ pulse (pin 8) when the key is loaded through the parallel master port and on the 64th SKCLK pulse (pin 38) when the key is loaded serially. The status of this flag can be read from the status register.
34	CLKIN	I	**Clock Input.** The clock signal input at this lead determines all internal timing. A microcode instruction is executed every two clock cycles. The master and slave ports' read and write signals are not required to be synchronous with this clock signal. The frequency range of this clock is 10 kHz to 8 MHz.
35	SPSD	I/O	**Slave Port Serial Data.** Depending on the programmed port configuration, used to write data to the input shift register or read data from the output shift register. The first bit read or written is the most significant. When this port is selected by the port configuration register, the slave port signals $\overline{\text{SPW}}$, $\overline{\text{SPR}}$, and SFLG (pins 6, 4, and 9) are used for control. This port may not be used to read or write to any of the other six registers.
36	MPSD	I/O	**Master Port Serial Data.** Depending on the programmed port configuration, used to write data to the input shift register or read data from the output shift register. The first bit read or written is the most significant. When this port is selected by the port configuration register and master port address 0 is addressed, the master port signals $\overline{\text{MPW}}$, $\overline{\text{MPR}}$, MFLG1, and MFLG2 (pins 8, 7, 11, and 10) are used for control.
37	SKD	I	**Serial Key Data.** This input port is used to load key variables serially. The data on this pin is latched into key memory on the falling edge of the serial key clock during the execution of a serial load key program. The key is entered with the most significant bit first and every 8th bit is treated as an odd parity bit. A parity failure will not prevent the 56-bit key from being loaded.

Table 1. T7000A Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
38	SKCLK	I	**Serial Key Clock.** This clock is used to latch key data into key memory. Data is latched on the falling edge of the clock. The key input circuitry is inhibited after the 64th clock is received.
39	$\overline{SCS}$	I	**Slave Chip Select.** This active-low input enables the slave port inputs and outputs. When high, all slave port outputs are placed in a high-impedance state. The $\overline{SPW}$, $\overline{SPR}$, SPSD, and SPD0—SPD7 signals are affected.
40	$\overline{MCS}$	I	**Master Chip Select.** This active-low input enables the master port input and output leads. When high, all master port outputs are placed in a high-impedance state and all inputs are disabled. The $\overline{MPW}$, $\overline{MPR}$, MPSD, and MPD0—MPD7 signals are affected.

Overview

Figure 1 is a block diagram of the DEP device. There are three major sections: the ciphering hardware and peripheral circuitry, the controller and program memory, and the ports.

The **ciphering hardware** contains a high-speed hardware implementation of the National Bureau of Standards Data Encryption Algorithm (DEA) and the necessary hardware to configure the DES operating modes (see Figure 3). Both the key schedule and DES enciphering circuitry are part of the DEA algorithm. The remaining circuitry (seven multiplexers, an exclusive-OR gate, and a latch) is used for the DES operating modes. An input shift register (ISR), four key registers, four initial value registers, and an output shift register (OSR) support the ciphering hardware.

An **internal hardware controller** executes a 22-bit machine instruction every two clock cycles, thereby setting up the ciphering multiplexers and clocking the appropriate registers. Within the controller, a program counter is used to address the machine instruction stored in either RAM or ROM program memory. On-chip ROM (29 x 22 bits) contains a subroutine controlling the DES hardware, a load initial value program, a load key program, a serial load key program, and an ECB encrypt and decrypt program. These short programs are located at hexadecimal address 00 through 1c (see Figure 5). User accessible on-chip RAM (32 x 22 bits) allows the user to tailor the ciphering operation to meet system requirements and eliminate external hardware. These ciphering programs must start at hex address 20 and may not exceed hex address 3F.

Master and slave ports are provided so that the plain text and cipher text can be on separate buses. These ports have both serial and 8-bit parallel bidirectional data buses. When using the 8-bit parallel data bus, master or slave, the most significant data or key byte should be written/read first. In the serial mode, the most significant bit is written/read first.

Registers

Eight addressable, internal registers control device operation. Table 2 shows the register assignments for both the master and slave ports during either a read or write operation.

Both the **input and output shift registers** (master or slave port address 0) may be accessed from MPD, MPSD, SPD, or SPSD. The input shift register (ISR) is a 64-bit, write-only, shift register. The output shift register (OSR) is a 64-bit, read-only, shift register. The port configuration register controls which port, master or slave, is associated with the input or output shift register. These shift registers are used to input and output data and would not normally be accessed until the other registers are loaded.

Table 2. Register Assignments

Master Port (MP)		
MP Address	**Register**	**Size (Bytes)**
0 (Write)	Input Shift	8
0 (Read)	Output Shift	8
1	Status	1
2	Port Configuration	1
3	Mode Control	1
4	M1	1
5	M2	1
6	M3	1
Slave Port (SP)		
SP Address	**Register**	**Size (Bytes)**
0 (Write)	Input Shift	8
0 (Read)	Output Shift	8
1 (Read)	Status	1

If a parallel port is used, 8 bytes are read or written to empty or load these registers, except when the 1- or 8-bit cipher feedback (CFB) mode has been programmed. In these cases a single byte is expected. For 1-bit CFB, only the most significant bit of the byte is used.

If a serial port is used, 64 bits are read or written to empty or load these registers, except when the 1- or 8-bit CFB mode has been programmed. One bit is expected for 1-bit CFB and eight bits for 8-bit CFB.

The **status register** (master or slave port address 1) may be read or written from the master port data bus or read only from the slave port data bus (see Figure 4).

Bits 1 and 0 (QA1, QA0) are read/write address lines that are used to select key and initial value register pairs 0—3 when the microcode instruction bit INT is not set. Key and initial value registers are matched sets, i.e., 00 selects key register 0 and initial value register 0 (see Table 3). The values are loaded into these registers by executing the appropriate program in ROM.

Bit 2 of this register is not used.

Bit 3 is a read-only, active-high, serial key request (SKREQ) flag. The complement of this flag ($\overline{\text{SKREQ}}$) is available at output pin 31. SKREQ is microcode-controlled and goes active when the SERIAL and ACT instructions are executed simultaneously.

Bit 4 is a read-only, active-high, input shift register full (ISRFULL) flag. This flag appears on an output pin; the specific pin (MFLG1 , MFLG2 , or SFLG) is determined by the port configuration. An active signal indicates that the ISR is full and additional information written to that register is ignored. The ISRFULL flag is set automatically whenever the mode control register is written or after the microcode instruction SISRFOSRE is executed. It is cleared by microcode instruction CLISRF.

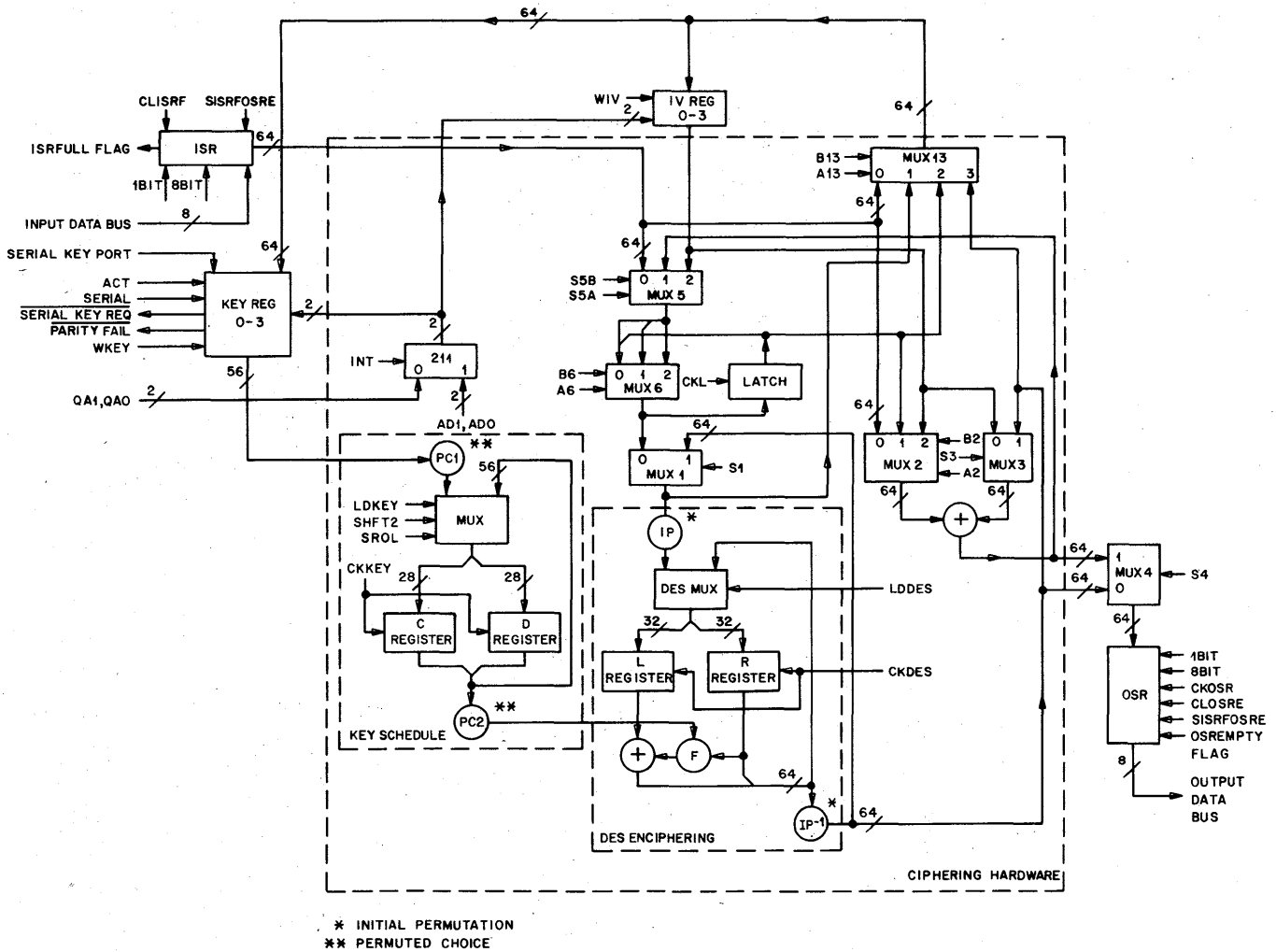


Figure 3. Ciphering Hardware Block Diagram

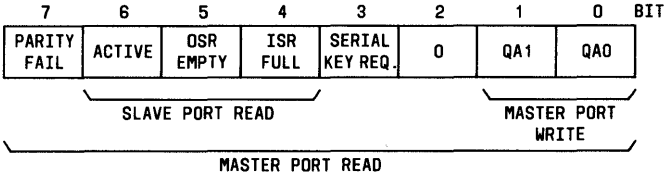


Figure 4. Status Register

Table 3. Key and Initial Value Register Addresses

Bits		Key and Initial Value Register Number
QA1	QA0	
0	0	0
0	1	1
1	0	2
1	1	3

Bit 5 is a read-only, active-high, output shift register empty (OSREMPTY) flag. This flag appears on an output pin; the specific pin (MFLG1 or SFLG) is determined by the port configuration. An active signal indicates that the OSR is empty and additional attempts to read that register are ignored. OSREMPTY is set automatically whenever the mode control register is written or after the microcode instruction SISRFOSRE is executed. It is cleared by the microcode instruction CLOSRE.

Bit 6 is a read-only, active-high, activity (ACTIVE) flag. This flag also appears on output pin 32 (ACTIVE). It is set by the microcode instruction IO ACT and indicates processor activity. The ACTIVE flag has no effect on device operation.

Bit 7 is a read-only, active-high, parity fail flag. The complement of this flag is available at output pin 33 ($\overline{PF}$). This flag is latched whenever the WKEY instruction is executed. An active condition indicates that one or more of the key bytes entered had even parity. Device operation is not inhibited by the parity fail flag.

The **port configuration register** (master port address 2) is a read/write register accessible only through the master port data bus. Table 4 defines the possible port configurations and associated hex code for data encryption and decryption.

The conditions indicated by the master and slave port flags are determined by the port configuration (see Table 5).

Bit 7 of the port configuration register is an input flag which is tested by microcode instruction LT?. This bit may be used to indicate the order in which the key schedule is used (encrypt or decrypt) or as a general-purpose conditional jump.

The **mode register** (master port address 3) is a read/write register accessible only through the master port data bus. This register is used to address on-chip memory for read/write operations and to begin program execution. Only the six least significant bits are used in this register.

Table 4. Port Configuration (MP Address = 2)				
Port Type	Input	Output	Hex Code*	
			Encrypt	Decrypt
Parallel	MPD	SPD	04	84
Parallel	SPD	MPD	11	91
Parallel	MPD	MPD	01	81
Serial	MPSD	SPSD	28	A8
Serial	SPSD	MPSD	62	E2
Parallel to serial	MPD	SPSD	08	88
Serial to parallel	SPSD	MPD	61	E1

* The most significant bit in the hex code for the port configuration is an input flag. It is tested by the microcode mnemonic LT?. In the microcode for the standard modes given in this document, this bit is tested to determine the order in which the DES key schedule should be used (encrypt or decrypt).

Table 5. Master and Slave Port Flag Conditions				
Port Configuration		Flag Condition		
Input	Output	$\overline{\text{MFLG1}}$	$\overline{\text{MFLG2}}$	$\overline{\text{SFLG}}$
MPD or MPSD	SPD or SPSD	ISRFULL	–	OSREMPTY
SPD or SPSD	MPD or MPSD	OSREMPTY	–	ISRFULL
MPD	MPD	OSREMPTY	ISRFULL	–

To run a microcode program, write the starting address for the set of instructions to be executed into the mode register. On the next instruction cycle, this address is loaded into a program counter and execution begins.

To read/write the program memory, the address of the instruction is loaded into the mode control register and one of the three hex bytes (M1, M2, or M3) which make up an instruction is read/written on a subsequent $\overline{\text{MPR}}/\overline{\text{MPW}}$ pulse. M1, M2, or M3 is selected using the master port address bus.

The M1, M2, and M3 registers (master port addresses 4—6, respectively) are accessible only through the master port data bus. These three bytes define a 22-bit microcode instruction stored in on-chip program memory. The two most significant bits of register M3 are not used.

Operation

It is important to use the following operating sequence with the DEP. Deviations from this sequence (e.g., loading the key before loading the ciphering program) may cause unpredictable results.

1. Load the ciphering program
2. Configure the ports
3. Load key and initial value register data
4. Execute the program

Load the Ciphering Program. The user may enter the microcode instructions for any of the DES mode programs (Figures 6—8), multiple programs, multiplexed programs, or his own unique cipher program. Thirty-two 22-bit instructions, starting at hex address 20, can be entered. Microcode instructions are loaded into RAM, a byte at a time, through the master port data bus to the address designated by the mode control register. The microcode address is first written to the mode control register (MP address 3), followed by the three hex bytes (M1, M2, and M3). These three bytes (MP addresses 4—6, respectively) constitute a 22-bit instruction.

Configure the Ports. Data flow, port selection, and the DES key schedule selection (encrypt and decrypt) are programmed by writing the appropriate hex code to the port configuration register (MP address 2). Table 4 shows the various port configuration options.

Load Key and Initial Value Register Data. There are four key and initial value registers that must be externally loaded. A key/initial value register address is written to the status register (see Tables 2 and 3 and Figure 4) and the load initial value program or one of the two load key programs is executed. The following is a description of the load key and initial value programs. The assembly language listings for these programs are shown on Figure 5.

After writing the starting address of the load initial value program (hex address 06) to the mode control register, the ISRFULL flag becomes inactive and the ACTIVE flag goes active. The eight initial value bytes may then be written to the input shift register through the master port data bus. After the eighth byte is written, the ISRFULL flag goes active and the content of the input shift register is copied to the addressed initial value register. The next internal machine instruction clears the ACTIVE flag.

After writing the starting address of the parallel load key program (hex address 0B) to the mode control register, the ISRFULL flag becomes inactive and the ACTIVE flag goes active. The eight key bytes may then be written to the input shift register through the master port data bus. After the eighth byte is written, the ISRFULL flag goes active and the content of the input shift register is copied to the addressed key register. Coincident with the program's WKEY instruction, the PARITY FAIL flag is set active high if any of the key bytes entered had even parity. The next internal machine instruction clears the ACTIVE flag.

After writing the starting address of the serial load key program (hex address 10) to the mode control register, the ACTIVE and serial key request (SKREQ) flags become active. The 64-bit key must then be clocked into the input shift register through the serial key port. After the last bit is entered, the content of the input shift register is copied into the addressed key register. One internal machine instruction cycle after the key is entered, the ACTIVE and SKREQ flags become inactive. Coincident with the program's WKEY instruction, the PARITY FAIL flag is set active high if any of the key bytes entered had even parity.

Execute the Program. After loading the microcode program, setting up the desired port configuration, and loading the key and initial value registers, the device is ready to begin a ciphering operation. The starting address of the microcode program is written to the mode control register. On the next internal machine cycle, this address is loaded into a program counter and execution begins. To execute the ECB mode, no microcode has to be loaded since it already exists in ROM. For this DES mode, step 1 should be omitted.

Input and output to the DEP device does not have to be synchronous with the input clock. The ISRFULL and OSREMPTY flags signal the host processor to write and read data. When these flags are inactive, data may be loaded into the input shift register and read from the output shift register by the port associated with these registers. These flags, tested in program memory by conditional machine instructions,

determine when to start or stop ciphering data. A typical ciphering program would contain the steps:

1. Multiplexer setup
2. Wait for input data
3. DES subroutine call
4. Wait until previous output data has been read
5. Latch output data and return to step 2

DES Mode Descriptions

The DEP is capable of performing all four DES operating modes: electronic codebook; cipher block chaining; 1-, 8- or 64-bit cipher feedback; and output feedback. Code for the ECB mode is stored in ROM beginning at location hexadecimal 12. The DEP may be programmed for the other modes via the RAM. Each mode can be used independently, combined with another mode, or used with multiple keys. For a detailed description of the DES modes refer to **Federal Information Processing Standards Publication 81**.

The **electronic codebook** (ECB) mode is primarily used to encrypt or decrypt keys or initial values through the use of a master key. It is a direct implementation of the DES algorithm. A 64-bit input data block results in a 64-bit output block. Consecutive data blocks are cryptographically independent. Figure 5 (Part 2 of 2) contains the assembly language listing for the ECB mode beginning at hexadecimal address 12.

The **cipher block chaining** (CBC) mode uses the DES algorithm in a 64-bit feedback mode resulting in consecutive output data blocks being cryptographically dependent. This dependence provides an error extension characteristic useful in protecting against an active system attack. Figure 6 contains the assembly language listing for the CBC mode.

The **cipher feedback** (CFB) mode is an additive stream cipher in which the DES algorithm is used to generate pseudo-random blocks. This mode provides cryptographic dependence of data blocks and error extension. It is not necessary that the input block be 64 bits. The input block may be 1, 8, or 64 bits. If the 1- or 8-bit mode is selected, a DES operation must be performed for every input bit or byte; consequently the data rate is reduced by a factor of 64 or 8, respectively. Figure 7 contains the assembly language listings for 1-, 8-, and 64-bit CFB modes.

The **output feedback** (OFB) mode uses the DES algorithm as a pseudo-random number generator. Encryption and decryption are identical operations and the security of the algorithm is dependent on the proper management of the initial value blocks. This mode has no error extension property; a 1-bit transmission error results in a 1-bit decryption error. This is an important property when transmitting over a noisy channel. Figure 8 contains the assembly language listing for the OFB mode.

These standard DES modes, after setup, may be executed in a minimum of seventeen instructions. With an 8 MHz input clock the instruction period is 250 nanoseconds, yielding a maximum of 235,000 ciphering operations per second. If the entire output block (all 64 bits) is used, the data throughput rate is 1.882 Mbytes/s.

Multiple encryption can be easily implemented with the DEP device. Using different keys, any of the previously mentioned DES modes can be cascaded to provide multiple encryption.

Figure 9 contains the assembly language listing for the ECB mode using 3 keys for encryption and decryption. Decryption is similar to encryption with the key schedules used in reverse order and the last key register used for encrypting used first for decrypting.

In addition to the four DES operating modes, multiple modes, and multiplexed modes, the user may choose to program a unique encryption method.

Figure 5 (Part 2 of 2) contains an assembly language listing (in ROM) for the ECB DES mode. Figures 6—9 contain assembly language listings for three DES modes and multiple key ECB. Each listing in Figures 6—9 begins at RAM hexadecimal address 20. When combining programs, program labels may have to be changed to prevent incorrect addressing. Also, duplicate code in some programs may be combined.

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
DES Subroutine				
0	c2	1f	0	:00 LDDES CKDES CKKEY
1	42	10	5	:01 CKDES CKKEY LLC 5
2	52	11	2	:02 CKDES SHFT2 CKKEY ILC 02
3	42	10	5	CKDES CKKEY LLC 5
4	52	11	4	:03 CKDES SHFT2 CKKEY ILC 03
5	42	13	0	CKDES CKKEY RET 0
Load Initial Value				
6	1	b	3	B6 IO LDMP ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
7	1	1a	0	CLISRF ADD
8	0	15	8	:10 ISRFT? 10
9	0	3c	0	WIV CLEAR
a	0	14	a	:20 GTO 20
Parallel Load Key				
b	1	b	3	B6 IO LDMP ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
c	1	1a	0	:25 CLISRF ADD
d	0	15	d	:30 ISRFT? 30
e	8	1c	0	WKEY CLEAR
f	0	14	f	:40 GTO 40
Serial Load Key				
10	1	b	7	B6 IO LDMP SERIAL ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
11	0	14	c	GTO 25

Figure 5. ROM Programs (Part 1 of 2)

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
ECB Encrypt or Decrypt				
12	1	c	0	B6 CLEAR DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
13	7	18	15	LDKEY CKKEY CLISRF LT? 100
14	2	19	1	CKKEY SROL SHFTR
15	0	15	15	:100 ISRFT? 100
16	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
17	0	17	1a	ISRFOSRET? 120
18	0	16	18	:110 OSRET? 110
19	0	d4	15	CLOSRE CKOSR GTO 100
1a	c3	d2	1	:120 CLISRF CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
1b	0	17	1a	:130 ISRFOSRET? 120
1c	0	14	18	GTO 110

Figure 5. ROM Programs (Part 2 of 2)

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
CBC Encrypt				
20	3	c	0	S5A B6 CLEAR DES INPUT = ISR^IV OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR^IV
21	7	18	23	LDKEY CKKEY CLISRF LT? 200
22	2	19	1	CKKEY SROL SHFTR
23	0	15	23	:200 ISRFT? 200
24	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
25	13	4	2c	:210 S3 S5A B6 GTO 130 DES INPUT = ISR^DESOUT OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR^DESOUT
26	0	15	26	:100 ISRFT? 100
27	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
28	0	17	2b	ISRFOSRET? 120
29	0	16	29	:110 OSRET? 110
2a	0	d4	26	CLOSRE CKOSR GTO 100
2b	c3	d2	1	:120 CLISRF CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
2c	0	17	2b	:130 ISRFOSRET? 120
2d	0	14	29	GTO 110
CBC Decrypt				
2e	7	1c	0	LDKEY CKKEY CLISRF CLEAR
2f	59	48	31	B2 S3 S4 B6 B13 LT? 250 DES INPUT = ISR OSR INPUT = IV^DESOUT IV INPUT = Qn LATCH INPUT = ISR
30	2	19	1	CKKEY SROL SHFTR
31	0	15	31	:250 ISRFT? 250
32	e3	12	1	CLISRF CKL LDDES CKDES CKKEY SUB 01
33	0	17	36	ISRFOSRET? 230
34	0	16	34	:220 OSRET? 220
35	0	f4	31	CLOSRE CKOSR WIV GTO 250
36	e3	f2	1	:230 CLISRF CKL WIV CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
37	0	17	36	ISRFOSRET? 230
38	0	14	34	GTO 220

Figure 6. Assembly Language Listing for CBC Mode

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
64-bit CFB Encrypt				
20	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
21	7	12	0	LDKEY CKKEY CLISRF SUB 00
22	1b	4	24	S3 S4 S5A B6 GTO 102 DES INPUT = ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = ISR^DESOUT
23	e3	d2	1	:101 LDDES CKDES CKL CKKEY CLISRF CLOSRE CKOSR SUB 01
24	0	17	23	:102 ISRFOSRET? 101
25	0	14	24	GTO 102
64-bit CFB Decrypt				
26	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
27	7	12	0	LDKEY CKKEY CLISRF SUB 00
28	19	4	24	S3 S4 B6 GTO 102 DES INPUT = ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = ISR
8-bit CFB Encrypt				
29	1d	b	10	S3 S4 S5B B6 IO 8BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
2a	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
2b	1a	84	24	S3 S4 S5A A6 GTO 102 DES INPUT = Qn<<8 || ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<8 || ISR^DESOUT

Figure 7. Assembly Language Listing for 1-, 8-, and 64-Bit CFB Modes (Part 1 of 2)

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
8-bit CFB Decrypt				
2c	1d	b	10	S3 S4 S5B B6 IO 8BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
2d	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
2e	18	84	24	S3 S4 A6 GTO 102 DES INPUT = Qn<<8 || ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<8 || ISR
1-bit CFB Encrypt				
2f	1d	b	8	S3 S4 S5B B6 IO 1BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
30	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
31	1a	4	24	S3 S4 S5A GTO 102 DES INPUT = Qn<<1 || ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 || ISR^DESOUT
1-bit CFB Decrypt				
32	1d	b	8	S3 S4 S5B B6 IO 1BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
33	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
34	18	4	24	S3 S4 GTO 102 DES INPUT = Qn<<1 || ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 || ISR

Figure 7. Assembly Language Listing for 1-, 8-, and 64-Bit CFB Modes (Part 2 of 2)

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
OFB Encrypt and Decrypt				
20	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
21	7	12	0	LDKEY CKKEY CLISRF SUB 00
22	98	4	24	S1 S3 S4 GTO 102 DES INPUT = DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 || ISR
23	e3	d2	1	:101 LDDES CKDES CKL CKKEY CLISRF CLOSRE CKOSR SUB 01
24	0	17	23	:102 ISRFOSRET? 101
25	0	14	24	GTO 102

Figure 8. Assembly Language Listing for OFB Mode

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
Subroutine for ECB with 3 Keys				
20	0	19	0	:20 SROL SHFTL
21	c6	18	24	LDDES CKDES LDKEY CKKEY LT? 25
22	2	1f	0	CKKEY
23	0	19	1	SROL SHFTR
24	2	14	1	:25 CKKEY GTO 01
3 Key ECB Encrypt				
/*				
25	1	1c	0	CLISRF CLEAR
26	1	a	1	:100 B6 ADD INT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
27	0	15	27	:110 ISRFT? 110
28	1	12	20	CLISRF SUB 20
29	81	a	3	B6 S1 ADD INT ADD0 DES INPUT = DESOUT OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
2a	0	12	20	SUB 20
2b	0	1a	5	ADD INT ADD1
2c	0	12	20	SUB 20
2d	0	16	2d	:140 OSRET? 140
2e	0	d4	26	CLOSRE CKOSR GTO 100
3 Key ECB Decrypt				
2f	1	1c	0	CLISRF CLEAR
30	1	a	5	:200 B6 ADD INT ADD1 DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
31	0	15	31	:210 ISRFT? 210
32	1	12	20	CLISRF SUB 20
33	81	a	3	B6 S1 ADD INT ADD0 DES INPUT = DESOUT OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
34	0	12	20	SUB 20
35	0	1a	1	ADD INT
36	0	12	20	SUB 20
37	0	16	37	:240 OSRET? 240
38	0	d4	30	CLOSRE CKOSR GTO 200

Figure 9. Assembly Language Listing for the ECB Mode Using 3 Keys

Instruction Set

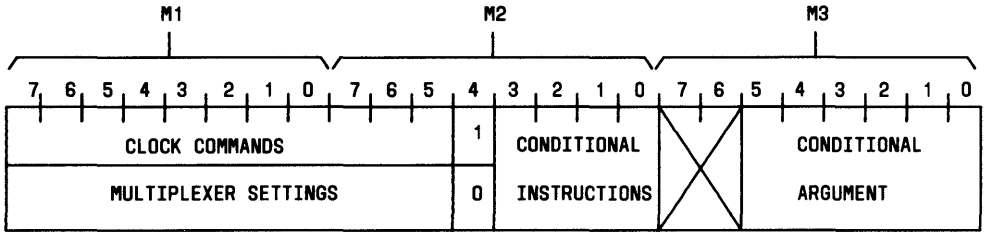


Figure 10. 22-Bit Instruction Diagram

Bytes M1, M2, and M3 constitute a 22-bit instruction. Bit 4 of byte M2 determines which set of instructions will be used in bits 0—7 of byte M1 and bits 5—7 of byte M2. If bit 4 of byte M2 is high (1), the clock command instructions are used. If this bit is low (0), the multiplexer setting instructions are used.

Bits 0—3 of byte M2 are decoded to one of thirteen conditional instructions. With the exception of RET and CLEAR, these instructions use the third byte, M3, as an argument. A description of each instruction is given in Table 6.

The timing diagram for the instruction set is shown on Figure 14. An instruction is executed every two clock cycles. The ciphering rate may be computed by multiplying the number of instructions in the ciphering operation by twice the CLKIN period.

Table 6. Instruction Set (Part 1 of 3)

Clock Commands (M2, Bit 4 = 1)

Byte	Bit	Mnemonic	Instruction
M1	7	LDDES	Enables the DES multiplexer to receive the output from MUX 1 when high or from the DES itself when low.
M1	6	CKDES	Clocks the DES L and R registers.
M1	5	CKL	Clocks the latch register.
M1	4	SHFT2	Enables the key circuitry to rotate 2 positions when high and 1 position when low.
M1	3	WKEY	Latches the key register currently addressed.
M1	2	LDKEY	Enables the key schedule C and D registers to be loaded from the addressed key register when high. When low, the contents of the C and D registers may be rotated 1 or 2 positions, left or right, depending on the state of the instructions SHFT2, SROL, and CKKEY. These two registers are used in the key schedule generation for the DES algorithm.
M1	1	CKKEY	Clocks the key schedule C and D registers.
M1	0	CLISRF	Clears the ISRFULL flag and allows data to be written into the ISR.
M2	7	CLOSRE	Clears the OSREMPTY flag and allows data to be read from the OSR.
M2	6	CKOSR	Clocks the output from MUX 4 into the OSR.
M2	5	WIV	Writes the output of MUX 13 into the initial value memory.

Table 6. Instruction Set (Part 2 of 3)

Multiplexer Settings (M2, Bit 4 = 0)

Byte	Bit	Mnemonic	Instruction
M1	7	S1	Selects the input line for MUX 1. A low selects input line 0; a high selects input line 1.
M1 M1	6 5	B2 A2	Select the input line for MUX 2. **B2 A2 Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both B2 and A2 are high (1).
M1	4	S3	Selects the input line for MUX 3. A low selects input line 0; a high selects input line 1.
M1	3	S4	Selects the input line for MUX 4. A low selects input line 0; a high selects input line 1.

Table 6. Instruction Set (Part 2 of 3 — Continued)

Multiplexer Settings (M2, Bit 4 = 0)

Byte	Bit	Mnemonic	Instruction
M1 M1	2 1	S5B S5A	Select the input line for MUX 5. **S5B S5A Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both S5B and S5A are high (1).
M1 M2	0 7	B6 A6	Select the input line for MUX 6. **B6 A6 Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both B6 and A6 are high (1).
M2 M2	6 5	B13 A13	Select the input line for MUX13. **B13 A13 Input Line** 0 0 0 0 1 1 1 0 2 1 1 3

Table 6. Instruction Set (Part 3 of 3)

Conditional Instructions

M2, Bits				Mnemonic	Instruction
3	2	1	0		
0	0	0	0	LLC	Loads the loop counter with the least significant nibble in M3. There is only one loop counter.
0	0	0	1	ILC	Decrements the loop counter and jumps to the address in M3 if the loop counter is not zero.
0	0	1	0	SUB	The current program counter instruction address is incremented and latched before the program jumps to the address specified by M3. Only one level of subroutine call is allowed.
0	0	1	1	RET	Return from subroutine. The program jumps to the address latched when the preceding SUB command was executed.
0	1	0	0	GTO	The program jumps to the address in M3.
0	1	0	1	ISRFT?	If the ISR is not full, the program jumps to the address specified by M3.
0	1	1	0	OSRET?	If the OSR is not empty, the program jumps to the address specified by M3.
0	1	1	1	ISRFOSRET?	If the ISR is full and the OSR is empty, the program jumps to the address specified by M3.
1	0	0	0	LT?	If bit 7 of the port configuration register is low, the program jumps to the instruction address in M3. This bit may be used to select the order in which the key schedule is used (encrypt or decrypt).

Table 6. Instruction Set (Part 3 of 3 — Continued)

Conditional Instructions (Continued)

M2, Bits				Mnemonic	M3, Bit	Mnemonic	Instruction
3	2	1	0				
1	1	1	1	UI	—	—	Unconditional increment to next instruction.
1	1	0	1	—	—	—	Not used.
1	1	1	0	—	—	—	Not used.
1	0	0	1	SROL	0 = 1	SHFTR	Latches a right key schedule rotation.
					0 = 0	SHFTL	Latches a left key schedule rotation.
1	0	1	0	ADD	2 1	ADD1 ADD0	Latches the key/initial value register address. **ADD1 ADD0 Reg Pair** 0 0 0 0 1 1 1 0 2 1 1 3
					0	INT	A high specifies the internal key/initial value address bus; a low specifies the key/initial value address specified by bits 0 and 1 of the status register.
1	0	1	1	IO	5	SISRFOSRE	A high sets both the ISRFULL flag and the OSREMPTY flag active.
					4 3	8BIT 1BIT	Selects 1-, 8-, or 64-bit CFB mode. **1-Bit 8-Bit CFB Mode** 0 0 64-Bit 0 1 8-Bit 1 0 1-Bit 1 1 Illegal
					2	SERIAL	Sets the key circuitry for a serial key input when high, and parallel key input when low.
					1	LDMP	A high sets the input circuitry to receive data from the master port regardless of the conditions programmed in the port configuration register.
					0	ACT	A high sets the ACTIVE flag in the status register and output pin 32 goes high.
1	1	0	0	CLEAR	NA	NA	Initializes control logic in the DEP. Specifically, this instruction sets the following bits low: ACT, LDMP, SERIAL, 1BIT, 8BIT, INT, ADD0, ADD1, SHFTL, SHFTR. This instruction is typically used in the first line of a program.

NA — Not applicable.

CHARACTERISTICS

Clocks

CLKIN: 10 kHz to 8 MHz
SKCLK: 10 kHz to 1.6 MHz

On-Chip Memory

ROM: 29 x 22 bits (hex address 00—1C)
RAM: 32 x 22 bits (hex address 20—3F)

ROM Address Map	
Address	**Program**
00	DES hardware subroutine
06	Load initial value
0B	Parallel load key
10	Serial load key
12	ECB Encrypt or Decrypt

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Current		I_{DD}	—	—	90	mA	0 °C, V_{DD} = 5.5 V
Input Voltage	Low	V_{IL}	—	—	0.8	V	
	High	V_{IH}	2.0	—	—	V	
Output Voltage	Low	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	High	V_{OH}	2.4	—	—	V	I_{OH} = 400 μA
Power Dissipation		PD	—	0.3	0.5	W	0 °C, V_{DD} = 5.5 V
			—	—	0.4	W	70 °C, V_{DD} = 5.5 V

Maximum Ratings

Voltage range on any pin with respect to ground (V_{SS}) ..... −0.5 to V_{DD} + 0.5 V
Storage Temperature Range (Tstg) ..... −65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Units
tAVRL	Address Set-Up Time (Read)	70	–	ns
tAVWL	Address Set-Up Time (Write)	70	–	ns
tCLKINHCLKINH	CLKIN Period	0.125	100	μs
tDVWH	Data Valid to Write Pulse Rising Edge	80	–	ns
tPCHPCH	Instruction Period	2tCLKINHCLKINH	–	ns
tRHDX	Read Pulse to Data Bus Float	–	80	ns
tRHFLGH	Last Read Pulse to Rising $\overline{\text{MFLG}}$ or $\overline{\text{SFLG}}$	–	80	ns
tRHRH	$\overline{\text{MPR}}$ or $\overline{\text{SPR}}$ Period	2tCLKINHCLKINH	–	ns
tRLDV	Read Pulse to Data Valid	–	70	ns
tSKCLKHSKCLKH	SKCLK Period	0.625	–	μs
tSKCLKLSKDX	Serial Key Data Hold Time	70	–	ns
tSKCLKLSKREQH	Last Falling Serial Key Clock to Rising Serial Key Request	–	4tCLKINHCLKINH + tWHFLGH	ns
tSKDVSKCLKL	Serial Key Data Set-up Time	70	–	ns
tSKREQLSKCLKL	Serial Key Request to First Falling Serial Key Clock	4tCLKINHCLKINH	–	ns
tWHDX	Write Pulse Data Hold	15	–	ns
tWHFLGH	Last Write Pulse to Rising $\overline{\text{MFLG}}$ or $\overline{\text{SFLG}}$	–	60	ns
tWHWH	$\overline{\text{MPW}}$ or $\overline{\text{SPW}}$ Period	2tCLKINHCLKINH	–	ns

Timing Diagram Nomenclature

Term	Definition	Term	Definition	Term	Definition
ADR	Address	M1D	M1 Data	PD	Port Data
CD	Cipher Data	M2D	M2 Data	SD	Status Data
MD	Mode Data	M3D	M3 Data	UD	Unciphered Data (Plain Text)

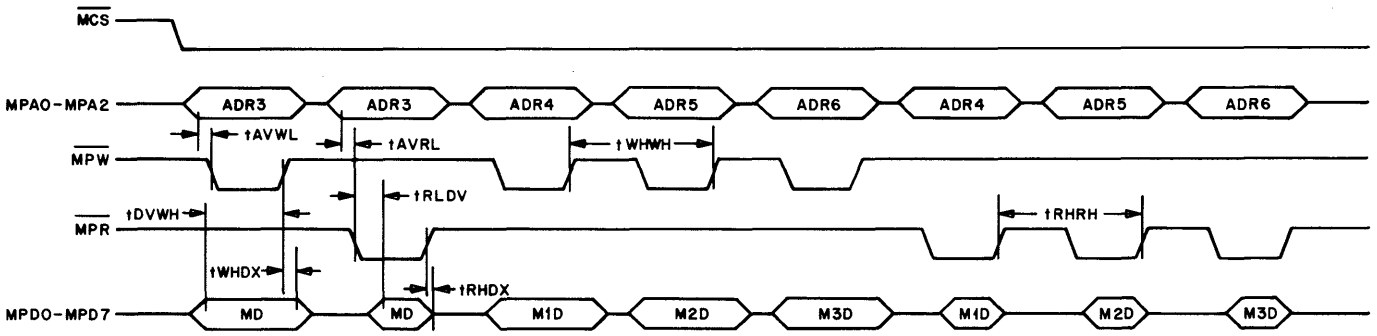


Figure 11. Memory Load Timing

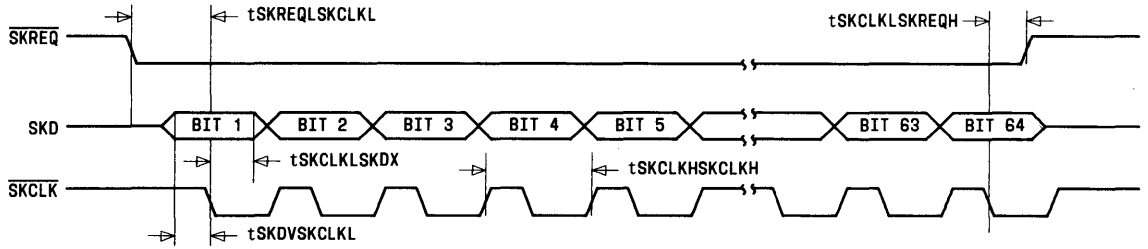
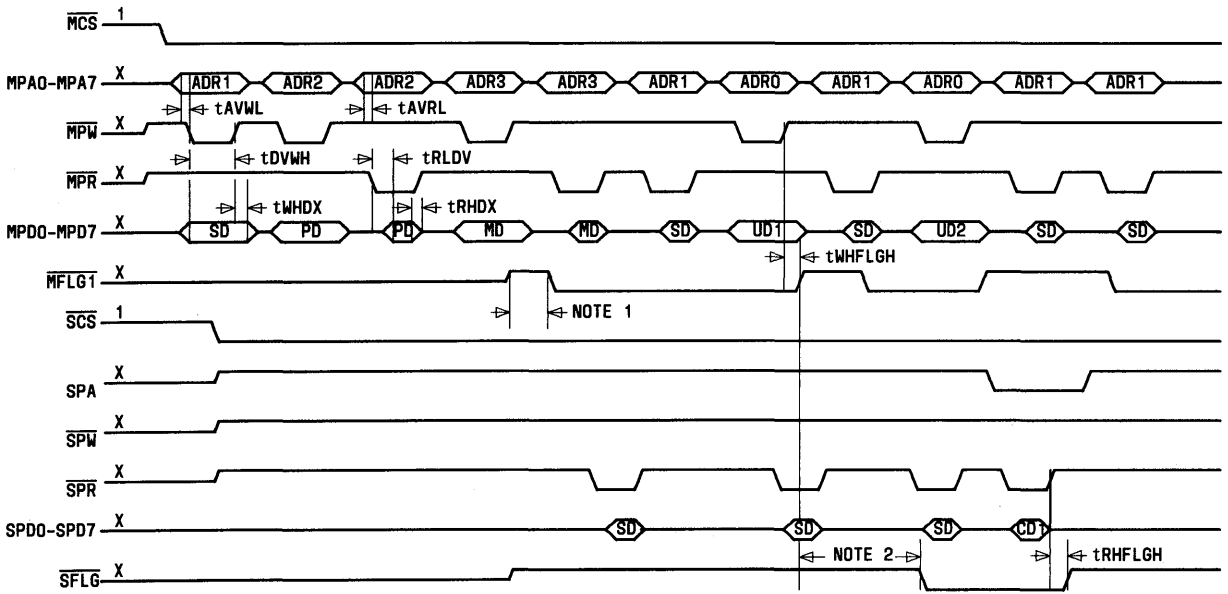
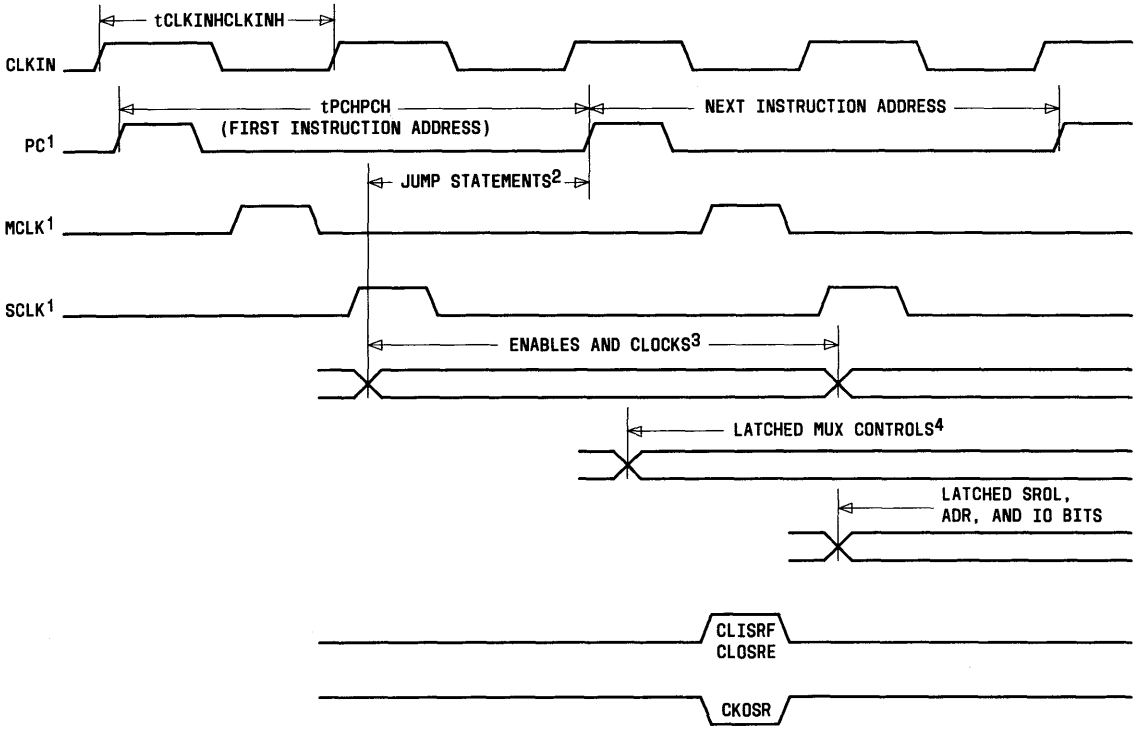


Figure 12. Serial Key Timing



Notes:
1. This time is determined by the number of program instructions before instruction CLISRF.
2. This time determined by the number of program instructions between the time MFLG1 GOES high and instruction CLOSRE. (Ciphering algorithm time).

Figure 13. 8-bit CFB Mode Timing with the Master Port Configured for Input and the Slave Port as an Output



Notes:
1. PC (Program Counter), MCLK, and SCLK are internal nonoverlapping clocks generated from CLKIN.
2. LLC, ILC, SUB, RET, GTO, ISRFT?, OSRET?, ISRFOSRET?, LT?
3. LDDES, CKDES, CKL, SHFT2, WKEY, LDKEY, CKKEY, WIV.
4. S1, A2, B2, S3, S4, S5A, S5B, A6, B6, A13, B13.

Figure 14. Internal Machine Instruction Timing

FEATURES

- On-chip or external high frequency oscillator source option
- On-chip or external jitter oscillator source option
- Generation of a 536-bit random number available in 8-bit bytes
- Internal verification of RNG output on the data bus
- Data ready and alarm output flags readable from the data bus or independent output pins allowing either processor interrupt or processor polled configuration
- Internal 4-bit statistical "run-up" test with programmable limits (elementary randomness check)
- External access to generated statistics

DESCRIPTION

The T7001 Random Number Generator (RNG) integrated circuit produces random bits based on the phase jitter of a free-running oscillator. The output data stream is truly random, not pseudo-random. The T7001 RNG is processed in CMOS technology, requires a single 5 V supply, and is supplied in a 32-pin plastic DIP.

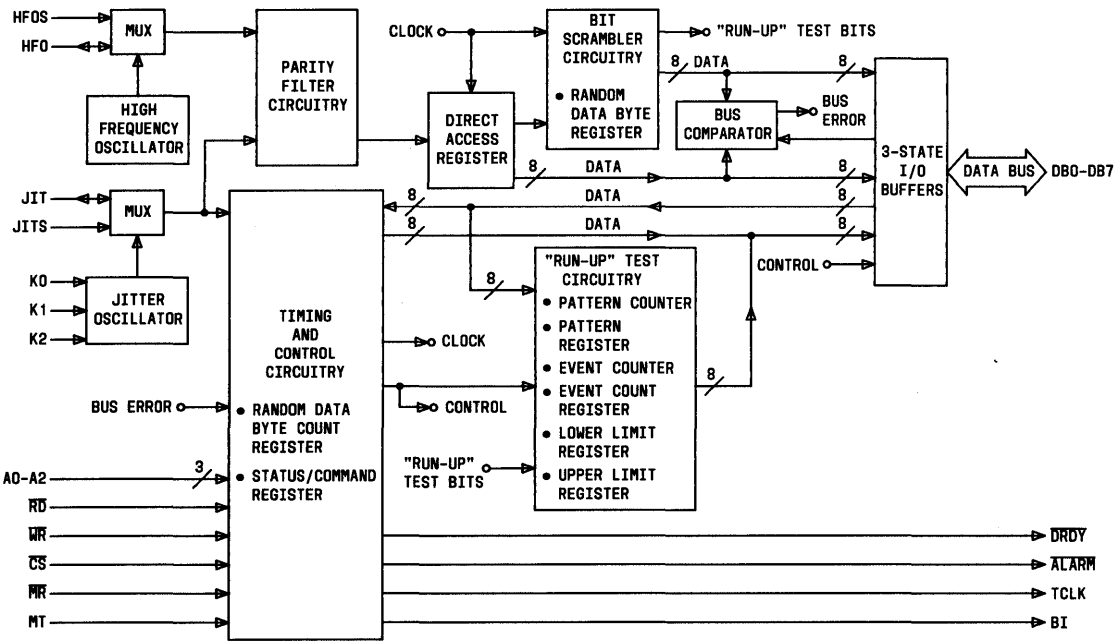
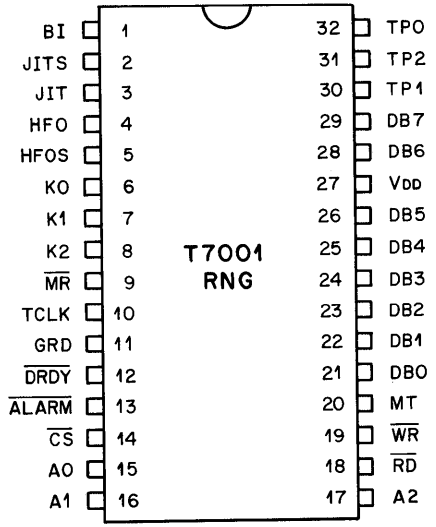


Figure 1. T7001 Random Number Generator Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin
A0	15	HFO	4
A1	16	HFOS	5
A2	17	JIT	3
ALARM	13	JITS	2
BI	1	K0	6
CS	14	K1	7
DB0	21	K2	8
DB1	22	MR	9
DB2	23	MT	20
DB3	24	RD	18
DB4	25	TCLK	10
DB5	26	TP0	30
DB6	28	TP1	31
DB7	29	TP2	32
DRDY	12	VDD	27
GRD	11	WR	19

Figure 2. T7001 Pin Function Diagram and Alphabetical List of Symbols

Table 1. T7001 Pin Descriptions

Pin	Symbol	Type	Name/Function
1	BI	O	**Test Pin.** Output of the positive-edge-triggered sampling D flip-flop which has the high-frequency oscillator (HFO) as its data input and the jitter oscillator (JIT) as its clock. It may be used to verify that both HFO and JIT are working properly.
2	JITS	I	**Jitter Select.** Determines the jitter signal source for the device. When low (0), the internal jitter oscillator is used. When high (1), an external jitter oscillator signal is expected at JIT (pin 3).
3	JIT	I/O	**Jitter.** Output of the internal jitter oscillator when JITS (pin 2) is low (0). When JITS is high (1), this pin is an input for an external jitter oscillator.
4	HFO	I/O	**High-Frequency Oscillator.** Output of the internal high-frequency oscillator when HFOS (pin 5) is low (0). This pin is the input for an external high-frequency oscillator signal when HFOS is high (1).
5	HFOS	I	**High-Frequency Oscillator Select.** Determines the high-frequency signal source for the device. When low (0), the internal high-frequency oscillator (8 MHz) is selected. When high (1), an external oscillator signal is expected at HFO (pin 4).
6 7 8	K0 K1 K2	I	A resistor (R) is connected between K0 and K1, and a capacitor (C) is connected between K0 and K2 to control the frequency of the on-chip jitter oscillator. The approximate frequency is determined by the equation: $f = \frac{1}{2.2\ RC}$

Table 1. T7001 Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
9	$\overline{MR}$	I	**Master Reset.** This active-low input resets the device when $\overline{CS}$ (pin 14) is active. A master reset puts the command bits in the status/command register to the inactive state and clears the random data-byte, event count, and random data-byte count registers. The pattern lower-limit, and upper-limit registers are unaffected by a master reset.
10	TCLK	O	**Test Clock.** This output is used with the direct access register to monitor the random data byte at the input to the 536-bit shift register. Random data is latched into the register on the rising edge of TCLK (pin 10) and can be read after this edge. Using the internal random-bit generator (with jitter osc. set to 1 kHz) the TCLK period is approximately 32 ms. Using a different oscillator frequency or an external random-bit generator, the TCLK period is computed by multiplying the JIT input (pin 2) period by 32.
11	GRD	–	**Ground.**
12	$\overline{DRDY}$	O	**Data Ready.** This active-low flag indicates that the "run-up" test was passed and that a 67-byte random number is stored in the random data-byte register. This flag may also be read from the status/command register. The $\overline{DRDY}$ flag goes inactive following the 67th $\overline{RD}$ pulse (pin 18), when the random data-byte register (address 0) is addressed.
13	$\overline{ALARM}$	O	**Alarm.** This active-low flag indicates either a "run-up" test failure or a bus error. Both of these conditions may be read from the status/command register. This flag can only be cleared by a master reset.
14	$\overline{CS}$	I	**Chip Select.** This active-low input enables $\overline{RD}$ (pin 18), $\overline{WR}$ (pin 19), $\overline{MR}$ (pin 9), and the address bits (pins 15, 16, and 17). When inactive the data bus output buffers are held in a high-impedance state regardless of the state of any other input.
15 16 17	A0 A1 A2	I	**Address Bus Bit 0.** **Address Bus Bit 1.** **Address Bus Bit 2.**
18	$\overline{RD}$	I	**Read.** This active-low input is used to read one of the eight internal registers. Data appears on the data bus following the falling edge of this signal and remains on the bus as long as $\overline{RD}$ is low. $\overline{WR}$ (pin 19) should be held high (inactive) during a read operation.
19	$\overline{WR}$	I	**Write.** This active-low input is used to write to one of three internal registers. The data is latched into the addressed register on the rising edge of the write pulse. $\overline{RD}$ (pin 18) should be held high (inactive) during a write operation.

Table 1. T7001 Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
20	MT	I	**Manufacture Test.** This pin must be grounded for device operation.
21	DB0	I/O	**Data Bus Bit 0.** Bidirectional 3-state I/O leads.
22	DB1		**Data Bus Bit 1.**
23	DB2		**Data Bus Bit 2.**
24	DB3		**Data Bus Bit 3.**
25	DB4		**Data Bus Bit 4.**
26	DB5		**Data Bus Bit 5.**
27	VDD	–	**5 V Supply.**
28	DB6	I/O	**Data Bus Bit 6.** Bidirectional 3-state I/O leads.
29	DB7		**Data Bus Bit 7.**
30	TP0	–	**Manufacture Test Point.**
31	TP1	–	**Manufacture Test Point.** No connect.
32	TP2	–	**Manufacture Test Point.**

Overview

Random bits are generated in a positive edge-triggered D-type flip-flop via the sampling of a high-frequency square wave by a pulse stream with a relatively high, randomly varying period (low, randomly varying frequency). This flip-flop is part of the parity filter circuitry shown on Figure 1. Groups of samples from the D flip-flop are fed through a parity filter. The output from this filter is fed into a bit scrambler. The bit scrambler receives these bits, performs exclusive-OR operations with previous bits, and sends the results to the random data-byte register.

The sources of both the high-frequency and the jitter (low frequency) signals are user selectable. HFOS (pin 5) determines the high frequency signal source. A low (0) on this pin selects the internal 8 MHz oscillator and configures HFO (pin 4) as an output for monitoring the signal. A high (1) on HFOS configures HFO as an input pin for an externally generated high-frequency signal. In critical applications it is recommended that an externally generated high frequency signal be used. Weak coupling or interaction between the low frequency clock signal and the internal 8 MHz oscillator has been observed and this may affect the randomness of the number produced. The use of an external high frequency square wave oscillator, preferably crystal controlled, substantially reduces any possibility of coupling.

JITS (pin 2) determines the source of the jitter oscillator signal. A low (0) on this pin selects the internal jitter oscillator and configures JIT as an output for monitoring the signal. The frequency of this oscillator is determined by an RC network at K0, K1, and K2. The equation for calculating the approximate frequency is $f = \frac{1}{2.2\ RC}$ (R must be $\geq$ 2 kΩ). Figure 3 shows the RC network connections. A high (1) on this pin configures JITS as an input for an externally generated signal.

A "run-up" test compares (1000 times) the last four bits in the random data byte register with a 4-bit pattern. If the number of times these two patterns match is outside the upper and lower limits programmed by the user during device initialization, the test fails and an alarm condition results. The result of this test (the number of times the patterns matched) can be read from the event counter register.

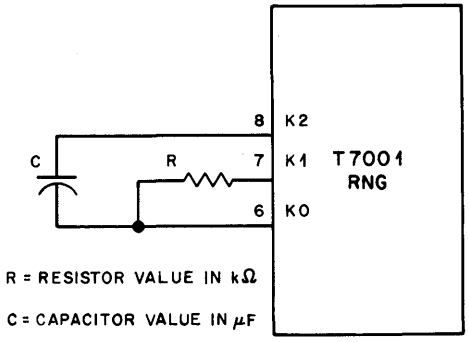


Figure 3. RC Network

The random data-byte register is a 536-bit (67 byte) shift register. After the random number is generated, the register is read a byte at a time using one read pulse per byte (67 read pulses).

During a read of the random data-byte register, the external bus data is compared with the register data. If there is any discrepancy, a bus error results and device operation is halted. The bus error flag state may be read from the status/command register or on the output $\overline{\text{ALARM}}$ pin. This error indicates a hardware failure, improper device operation, or a bus contention problem.

Data ready ($\overline{\text{DRDY}}$) and alarm output flags are readable from either the data bus or independent output pins. This feature allows configuration of either processor interrupt or processor polled systems.

Registers

There are eight addressable registers. Five are read-only registers and three are read/write registers. Table 2 contains the register assignments for the RNG.

The **random data-byte register** (address 0) is a read-only shift register that stores the random number. Sixty-seven $\overline{\text{RD}}$ pulses are used to read the random number. The device remains inactive until all 67 bytes are read or until a master reset is issued.

The **status/command register** (address 1) is a read/write register (see Figure 4). It must be written before certain device operations can begin.

Bit 0 is a read-only, active-low data ready flag used to indicate that a "run-up" test has passed and a 67-byte random number is stored in the random data-byte register. This flag remains active until all 67 random data bytes have been read, a bus error is detected, or a master reset is issued. This information is also available on output $\overline{\text{DRDY}}$.

Bit 1 is a read/write, active-high, master-reset command. When active, a master reset condition exists until this bit is cleared by a low pulse on external $\overline{\text{MR}}$ or by writing a zero to this bit.

Bit 2 is a read/write, active-high, free-run command. In the inactive state, the device executes a single "run-up" test and halts operation. If the test passes, the $\overline{\text{DRDY}}$ flag goes active and all 67 random data bytes must be read (or a master reset issued) before a second "run-up" test is begun.

If bit 2 is active (set), the device continually executes "run-up" tests. The $\overline{\text{DRDY}}$ flag goes active after the first "run-up" test passes and remains active until a failure occurs. Data can be read from the random data-byte register continuously during "run-up" tests, but this is a bad practice. To maximize randomness, data should be read only when the $\overline{\text{DRDY}}$ flag is active. When the first $\overline{\text{RD}}$ pulse accesses the random

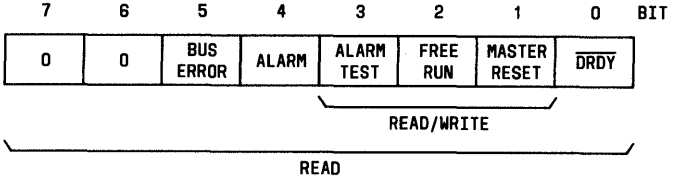


Figure 4. Status/Command Register

Table 2. Register Assignments

Address		Register	Size (Bits)
0	(Read)	Random data byte	536
1	(Read/Write)	Status/command	8
2	(Read)	Event count	8
3	(Read)	Pattern	4
4	(Read/Write)	Lower limit	8
5	(Read/Write)	Upper limit	8
6	(Read)	Random data-byte counter	8
7	(Read)	Direct access	8

byte register, the current "run-up" test halts. After the sixty-seventh $\overline{RD}$ pulse, the "run-up" tests start anew. Bit 2 can be set at any time during device operation. An external master reset ($\overline{MR}$) pulse clears bit 2, but an internal master reset (bit 1) has no affect.

Bit 3 is a read/write, active-high, alarm-test command (ALRMT). If active, a known sequence of zeros and ones is automatically loaded into the random data-byte register producing known event counts for the "run-up" test. The generated counts are given in Table 3. This test is used to check the "run-up" and alarm circuitry. It can also be used to produce a known pattern in the random data-byte register that can be read if desired. These "run-up" test counts and random data byte patterns (see Table 3) are not user selectable.

In order for this test to operate correctly, the device must first be cleared using the internal master reset command (set bit 1). Then, on a subsequent write cycle, the internal master reset command bit must be cleared simultaneously with the setting of the alarm test bit, i.e., writing the hexadecimal sequence 0A, 08 to the status/command register. Bit 3 is cleared with an external master reset. Internal master reset has no effect.

Bit 4 is a read-only, active-high, alarm flag. The complement of this flag is available at $\overline{ALARM}$ (pin 13). An active alarm flag indicates that either a "run-up" test has failed or a bus error has been detected. This flag can only be cleared by a master reset.

Bit 5 is a read-only, active-high, bus error flag. It becomes active if there is a discrepancy between the data in the random data byte register and the data appearing externally on the eight-bit bidirectional data bus during a random data byte read operation. An active bus error flag causes $\overline{ALARM}$ to go low and bit 4 of the command/status register to go high. This condition can only be cleared by a master reset.

Table 3. Alarm Test Register Data

Pattern (Hex)	Event Count (Hex)	Random Data Byte Register					
		Byte Number	Byte (Hex)	Byte Number	Byte (Hex)	Byte Number	Byte (Hex)
		1	71	23	E8	45	C9
0	A0	2	F0	24	A1	46	61
1	21	3	EC	25	C8	47	B0
2	4E	4	A1	26	73	48	E0
3	25	5	58	27	B0	49	A1
4	55	6	73	28	E8	50	C9
5	3B	7	F0	29	A1	51	61
6	15	8	EC	30	C8	52	B0
7	4E	9	A1	31	73	53	A2
8	28	10	58	32	B0	54	A1
9	52	11	73	33	E0	55	C9
A	42	12	F0	34	A1	56	61
B	38	13	E8	35	C8	57	B0
C	1D	14	A1	36	73	58	A2
D	3F	15	58	37	B0	59	A1
E	47	16	73	38	E0	60	C9
F	2A	17	B0	39	A1	61	41
		18	E8	40	C8	62	B0
		19	A1	41	61	63	A2
		20	58	42	B0	64	A9
		21	73	43	E0	65	C9
		22	B0	44	A1	66	41
						67	B0

Bits 6 and 7 are always low (0) and are unused.

The **event count register** (address 2) is a read-only register. This register stores the hex event count from the most recently completed "run-up" test. It is an 8-bit register with a maximum displayable count of 255 (hex FF). A reading of less than 255 indicates the actual event count obtained during the last "run-up" test; a reading of 255 indicates an event count of 255 or more. This register is cleared with a master reset.

The **pattern register** (address 3) is a read-only register that stores the 4-bit hex pattern associated with the most recently completed "run-up" test. A pattern counter is incremented at the completion of every successful "run-up" test. If the "run-up" test fails, the pattern counter is not changed and the test is repeated following a master reset. A master reset does not affect this counter or the pattern register (address 3). The counter assumes an arbitrary state during power-up and increments from there.

The **lower-limit register** (address 4) is a read/write register. It stores the hex lower limit associated with the "run-up" test and must be written before proper operation of the device can begin.

The **upper-limit register** (address 5) is a read/write register. This register stores the hex upper limit associated with the "run-up" test and must be written before proper operation of the device can begin.

The **random data-byte counter register** (address 6) is a read-only register. This down counter register keeps track of the number of random bytes left in the random data-byte register. Following an active data ready signal, this register is preset to hex 43 (decimal 67). After the 67 random data bytes have been read, this register is at hex 0 and remains there until the next active data ready signal.

The **direct access register** (address 7) is a read-only register. Along with TCLK, it allows the user to continually monitor the random data byte at the input to the 536-bit shift register. The random data is latched into this register on the rising edge of the TCLK signal and can be read after this edge.

Data read from this register has not been subjected to the bit scrambler and may have high bit-to-bit correlation. Thus, this data should not be used in place of data obtained from the random data-byte register, but should only be used for device monitoring and/or testing.

Operation

The upper- and lower-limit registers and the status/command register, which control device operation, must be written by the host processor before proper operation begins. Figure 6 shows the timing of a basic write cycle.

After the controlling processor has initialized the T7001 device, random number generation is initiated with an external $\overline{MR}$ pulse. Random bits are then generated and fill the 536-bit (67 byte) random data-byte register. Following the initial fill, a "run-up" test is executed.

During a "run-up" test, the last four bits in the random data-byte register are compared to the contents of a 4-bit pattern counter. If both bit patterns match, the event count register is incremented. At the end of one thousand non-overlapping, four-bit tests on a fixed pattern, the result accumulated in the event counter is compared to the contents of the upper- and lower-limit registers. If the event count is outside the stored limits, the test fails. It takes approximately 18 seconds to execute a "run-up" test with the low-frequency jitter oscillator set to 1 kHz. If a different frequency is used, the testing time may be computed by multiplying the jitter oscillator period by 18160.

If the random bits are independent, with $P(1) = P(0) = 0.5$, the probability of any 4-bit pattern is 0.0625 and the expected event count for 1000 samples is 62.5. The event count has a binomial distribution with a standard deviation of 7.65. Using the normal approximation to the binomial distribution, the probability of a test failing can readily be computed. For example, if the limits are set at plus or minus twice the standard deviation, then the probability of the test failing is 0.0456 (taken from the table of values for the Standard Normal Distribution Function). At plus or minus three times the standard deviation, the probability of the test failing is 0.0026. The upper and lower limits are stored as binary numbers in the upper- and lower-limit registers. Since the upper- and lower-limit registers are eight bits in length, the largest value that can be stored in the upper-limit register is hexadecimal FF while the smallest number which can be stored in the lower-limit register is hexadecimal 00. If these maximum and minimum values are used for the upper and lower limits of the "run-up" test respectively, the test is inoperative, i.e., the test never fails.

If the "run-up" test is inoperative, there is no automatic warning or check of device malfunction such as high frequency oscillator failure. Low frequency oscillator failure is detected by cessation of device operation since that oscillator is used to clock the entire device. Detection of high frequency oscillator failure occurs only when the "run-up" test is operative. If a "run-up" test is initiated with a master reset and the high frequency oscillator is stuck either high or low, the event count register will contain either hexadecimal FF or 00 at the end of the test. Thus, if the upper- and lower-limit registers were set to hexadecimal FE and 01 respectively, the "run-up" test would fail. The chance of a fully operational device failing under these conditions is $1 - 6.22 \times 10^{-16}$. Thus, in order to be warned of device malfunction, the "run-up" test should always be kept operative. If, for some reason, the user wants to make the test inoperative, it may be best to set the "run-up" test upper and lower limits to FE and 01, respectively. These limits will effectively remove the "run-up" test but maintain the warning of gross malfunction, i.e., high-frequency oscillator failure.

If the "run-up" test passes, the $\overline{\text{DRDY}}$ flag goes active and the host processor can address the random data-byte register to read the 67 bytes. Figure 8 shows the timing required for successive random data byte read cycles to completely empty the random data-byte register. At the end of the sixty-seventh read pulse, the device begins generating the next 67 byte random number. If the "run-up" test fails, the $\overline{\text{DRDY}}$ flag remains inactive, the alarm flag goes active, and repeated attempts to read the random data yield the same byte. The alarm condition can only be cleared by a master reset. The random data-byte register can be accessed during a "run-up" test, but this is not a good practice. During the "run-up" test, bits are scrambled in a way which removes bit-to-bit correlation between successively generated samples at the front-end D-type flip-flop. The scrambling process is not complete until the "run-up" test has finished.

CHARACTERISTICS

Clocks

HFO (internal): 8 MHz

HFO (external): 12 MHz max

Jitter (internal): Determined by RC (see Figure 5); R should be greater than 2 kΩ; frequency, f_{JIT}, should be much lower than the frequency of HFO, f_{HFO}; i.e., $4000\ f_{JIT} < f_{HFO}$

Jitter (external): Frequency, f_{JIT}, should be much lower than the frequency of HFO, f_{HFO}; i.e., $4000\ f_{JIT} < f_{HFO}$

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 10%, GRD = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Current		I_{DD}	—	5.5	14	mA	T=20 °C, V_{DD}=5.5V, Voltage on inputs and I/O pins = V_{DD}
			—	20	50	mA	T=20 °C, V_{DD}=5.5V, Voltage on inputs and I/O pins = 2.0 V
Input Leakage		I_L	—	—	±10	μA	V_{IN}=V_{DD} to 0.0 V
Input Voltage	Low	V_{IL}	0	—	0.6	V	
	High	V_{IH}	2.2	—	V_{DD}	V	
Output Voltage	Low	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 μA
	High	V_{OH}	2.4	—	—	V	I_{OH} =−40 μA
Power Dissipation		PD	—	30.25	77	mW	T=20 °C, V_{DD}=5.5 V, Voltage on inputs and I/O pins = 2.0 V
			—	110	275	mW	T=20 °C, V_{DD}=5.5 V, Voltage on inputs and I/O pins = 2.0 V

Maximum Ratings

DC Supply Voltage Range (V_{DD}) ..... 5 ± 10%
Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... −65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

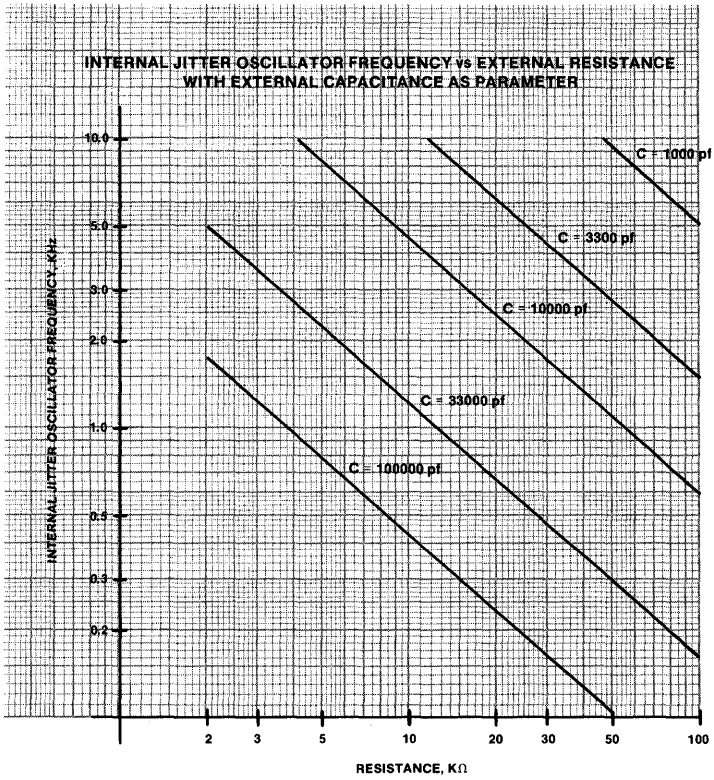


Figure 5. RC Network Selection Diagram

Timing Characteristics

Symbol	Description	Min	Max	Unit	Test Conditions
tAVRDL	Address to $\overline{RD}$ set-up time	50	—	ns	—
tAVWRL	Address to $\overline{WR}$ set-up time	50	—	ns	—
tCSLRDL	$\overline{CS}$ to $\overline{RD}$ set-up time	50	—	ns	—
tCSLWRL	$\overline{CS}$ to $\overline{WR}$ set-up time	50	—	ns	—
tDBVWRH	$\overline{WR}$ edge to data bus set-up time	400	—	ns	—
tMRLMRH	$\overline{MR}$ pulse width time	1.0	—	μs	—
tRDHAX	$\overline{RD}$ to address hold time	50	—	ns	—
tRDHCSH	$\overline{RD}$ to $\overline{CS}$ hold time	70	—	ns	—
tRDHDBZ	$\overline{RD}$ to data bus 3-state time	10	100	ns	—
tRDLDBV	$\overline{RD}$ to data delay time		260	ns	CL = 100 pF
tRDLRDH	$\overline{RD}$ pulse width time	400	—	ns	—
tWRHAX	$\overline{WR}$ to address hold time	50	—	ns	—
tWRHCSH	$\overline{WR}$ to $\overline{CS}$ hold time	70	—	ns	—
tWRHDBX	Data hold time for $\overline{WR}$	35	—	ns	—
tWRLWRH	$\overline{WR}$ pulse width time	400	—	ns	—

Timing Diagrams

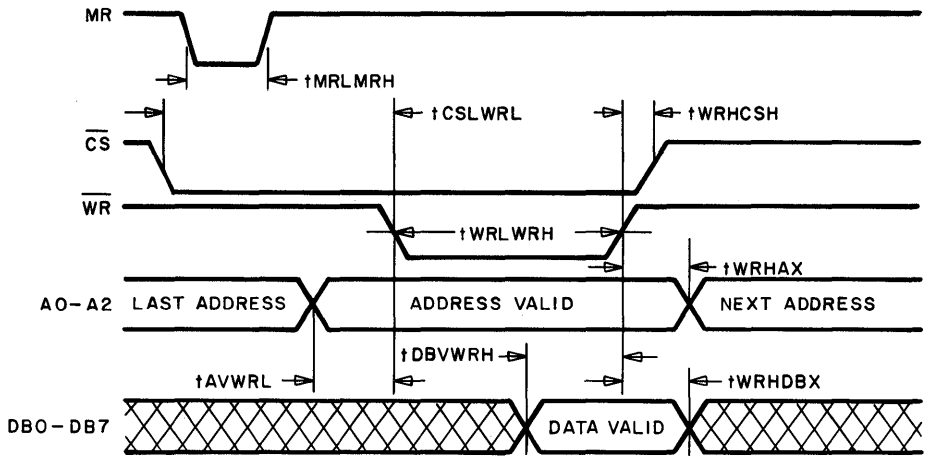


Figure 6. Write Cycle Timing

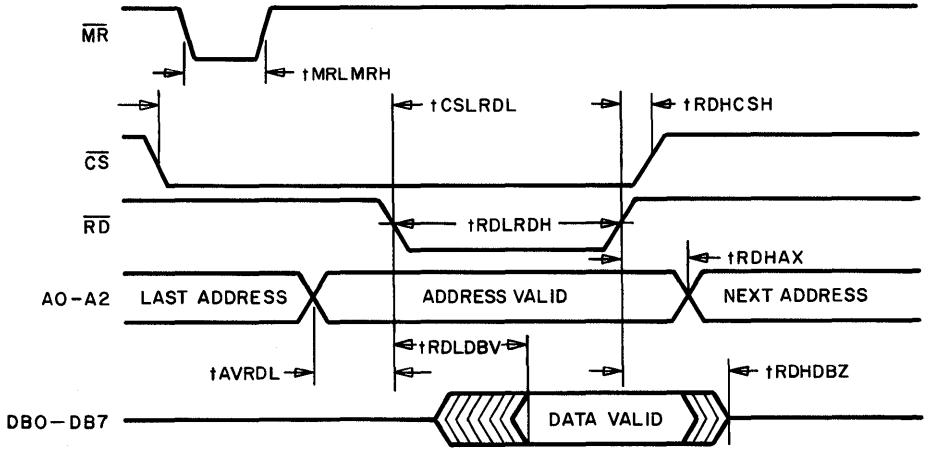


Figure 7. Read Cycle Timing

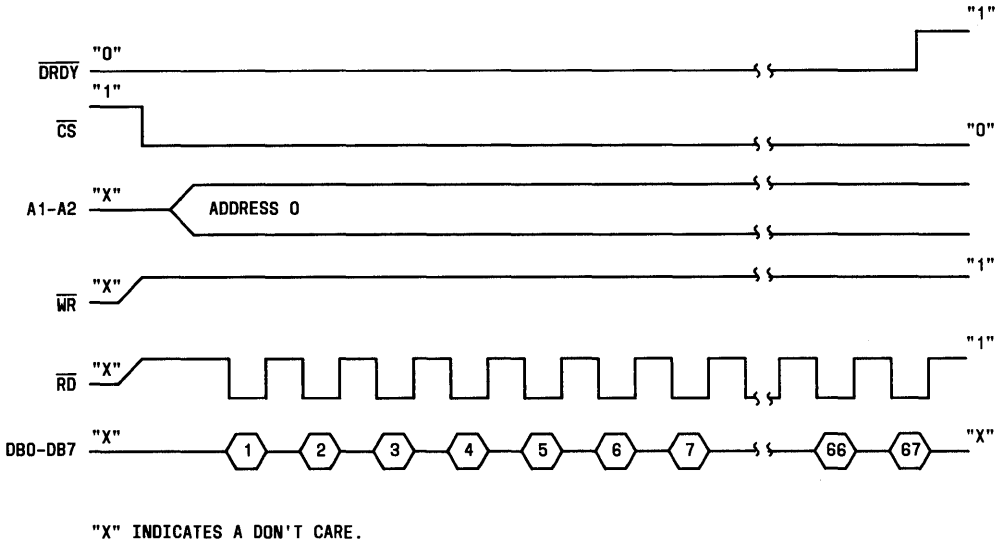


Figure 8. Random Data Byte Register Read Operation Timing

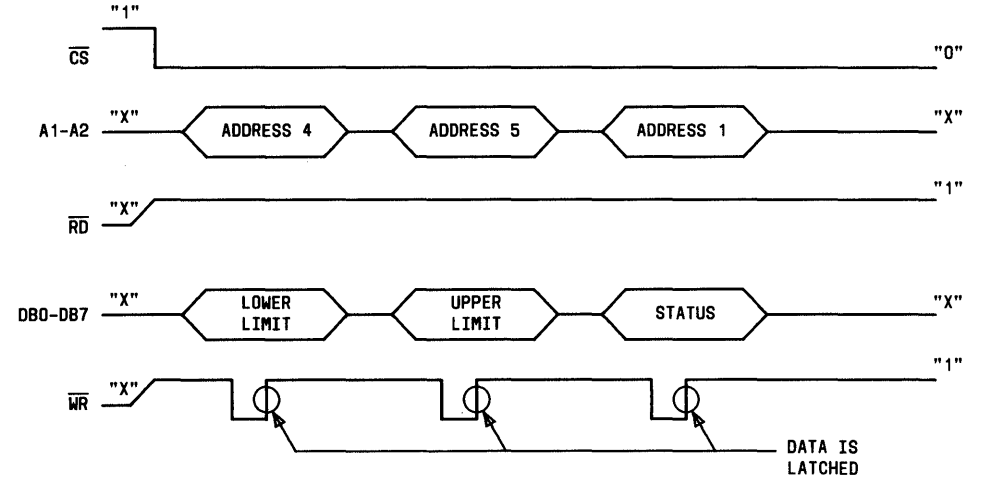


Figure 9. Lower- and Upper-Limit Registers and Status/Command Register Write Operation Timing

The information contained herein is preliminary and subject to change.

FEATURES

- Full-duplex operation using frequency division multiplexing (FDM)
- Complete analog and digital signal processing functions and handshake protocol for 0—300 and 1200 b/s modem
- Microprocessor programmable with either multiplexed or separate data and addressing
- Scrambler and descrambler capabilities
- 2100 Hz, 2225 Hz, or unscrambled mark answer tones at answering set
- 8- through 11-bit character modes
- Synchronous or asynchronous operation
- Factory-set carrier detect and transmit levels
- Self-test using analog and digital loopback techniques
- 1800 Hz tone with high-band signal (CCITT V.22)
- Compromise equalizer
- Overspeed capability to 2.3% (CCITT V.22)
- Transmit signal levels programmable for either voice or data jack
- All digital outputs are TTL compatible
- Low-power consumption
- Full digital and analog testing of all functions and parameters on assembled modem
- Factory burn-in

DESCRIPTION

The T7010 Switched Capacitor Modem (SCM) integrated circuit is a full-duplex data modem consisting of two chips fabricated using CMOS technology. The two chips, one mostly analog and one all-digital, are packaged in a dual-cavity 40-pin ceramic DIP. The mostly analog chip provides analog functions using 10 V switched capacitor technology. The all-digital chip provides TTL-output compatible, digital functions using 5 V logic. The SCM is a general-purpose modem for use in stand-alone data sets or for use in data and graphics terminals that interface directly with telephone networks. This microprocessor peripheral can be used to transmit full-duplex data on 2-wire switched voice telephone networks and on point-to-point circuits. The SCM supports a variety of transmission standards which include 0—300 b/s frequency shift keying (FSK) for AT&T Standard 103 and 1200 b/s differential phase shift keying (DPSK) for AT&T Standard 212L1A and CCITT V.22. Transmit and filtering functions compatible with 2400 b/s CCITT V.22 bis transmission, using quadrature amplitude modulation (QAM), are included.

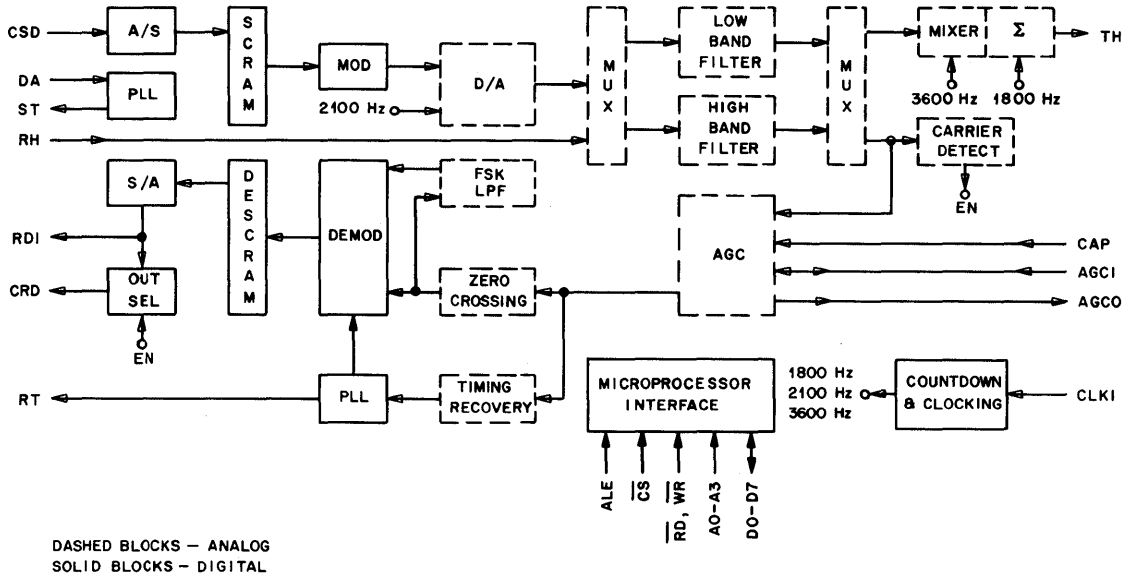
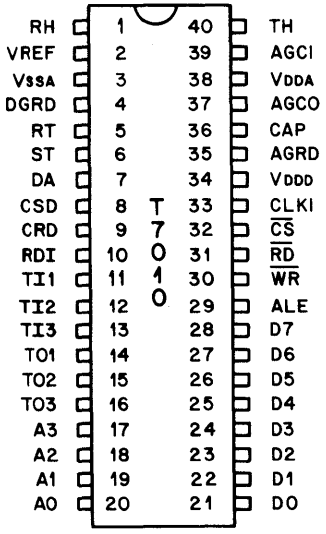


Figure 1. T7010 Switched Capacitor Modem Functional Sections

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin(s)
A0	20	$\overline{DGRD}$	4
A1	19	$\overline{RD}$	31
A2	18	RDI	10
A3	17	RH	1
AGCI	39	RT	5
AGCO	37	ST	6
AGRD	35	TH	40
ALE	29	TI1–TI3	11–13
CAP	36	TO1–TO3	14–16
CLKI	33	VDDA	38
CRD	9	VDDD	34
$\overline{CS}$	32	VREF	2
CSD	8	VSSA	3
D0–D7	21–28	$\overline{WR}$	30
DA	7		

Figure 2. T7010 Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7010 Pin Descriptions

Pin	Symbol	Type	Name/Function
1	RH	I	**Receive From Hybrid.** Input for incoming modulated voice-data from the hybrid.
2	VREF	O	**Voltage Reference.** Connect a 5 μF capacitor between this pin and VSSA (pin 3).
3	VSSA	—	**−5 V (Analog) Supply.** Connect a 5 μF capacitor between this pin and VDDA (pin 38).
4	DGRD	—	**Digital Ground.**
5	RT	O	***Receive Timing.** Provides received bit clock.
6	ST	O	***Send Timing.** Provides transmit bit clock.
7	DA	I	****Transmit Signal Timing.** External transmit bit clock input.
8	CSD	I	**Customer Send Data.** Receives data in binary form from user interface.
9	CRD	O	**Customer Receive Data.** Output for received data in binary form to the user interface after clamping by carrier detect.
10	RDI	O	***Received Data Internal.** Output for received data in binary form prior to clamping.
11	TI1	I	****Test Input 1.** Receives the data rate from an external demodulator. Also used for test during manufacture.
12	TI2	I	****Test Input 2.** Binary data input to the on-chip descrambler from an external demodulator. Also used for test during manufacture.
13	TI3	I	****Test Input 3.** Receives synchronizing signal for data frame. Also used for test during manufacture.
14	TO1	O	***Test Output 1.** Provides the received signal baud rate (600 Hz). Also used for test during manufacture.
15	TO2	O	***Test Output 2.** Provides a 9600 Hz clock obtained from the received signal timing recovery circuit. Also used for test during manufacture.
16	TO3	O	***Test Output 3.** Provides the sign of the last update to receiver timing recovery phase lock loop. Also used for test during manufacture.
17—20	A3—A0	I	**Address Bus.** Address leads associated with the selection of 8 bits of data for data bus. For a microprocessor with separate address and data leads, while ALE (pin 29) is high, A3—A0 must be valid at $\overline{CS}$ time, and remain valid during $\overline{CS}$. For a microprocessor with multiplexed address/data leads, A3—A0 must be valid at high-to-low ALE transition, and A0—A3 are strapped to D0—D3, respectively.

*Leave disconnected if not required.
**Should be connected to DGRD if not required.

Table 1. T7010 Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
21—28	D0—D7	I/O	**Multiplexed Data/Address Bus.** D0—D7 form an 8-bit, bidirectional, 3-state data bus. The data bus direction is controlled by the logic states of $\overline{WR}$, $\overline{RD}$, and $\overline{CS}$ (pin 30—32). Outputs are normally high impedance (third-state). If register addresses are multiplexed on the data bus, A0—A3 must be strapped to D0—D3, respectively.
29	ALE	I	**Address Latch Enable.** Internally latches the A0—A3 address when this pin makes a high-to-low transition. The internal address follows A0—A3 when ALE is high, and holds last A0—A3 input when ALE is low.
30	$\overline{WR}$	I	**Write Enable (Active Low).** Enables writing of data bus into digital logic circuits. Data is latched internally on the low-to-high transition of the $\overline{WR}$ pulse.
31	$\overline{RD}$	I	**Read Enable (Active Low).** A logic low at $\overline{RD}$ enables the contents of a selected internal register to be placed on the data bus.
32	$\overline{CS}$	I	**Chip Select (Active Low).** Enables read and write of the databus. Does not affect operation of ALE.
33	CLKI	I	**Clock Input.** This pin must be connected to a 4.9152 MHz ±100 ppm square wave with a 50 ±10% duty cycle.
34	V_{DDD}	—	**5 V (Digital) Supply.**
35	AGRD	—	**Analog Ground.** Provides ground reference for RH, TH, and AGCO signals. Connects to power supply common terminal.
36	CAP	—	**Automatic Gain Control Capacitor.** Connect a 1 μF capacitor between this pin and AGRD (pin 35). Also connect to AGCO (pin 37) through a 100 kΩ resistor.
37	AGCO	O	**Automatic Gain Control Output.** Provides a filtered and amplified received signal. Signal is approximately 2 Vp-p, and will not drive an impedance less than 50 kΩ. Pin must be connected to CAP via a 100 kΩ resistor.
38	V_{DDA}	—	**5 V (Analog) Supply.** Analog circuits power input for the device. A 5 μF smoothing capacitor should be connected between this pin and V_{SSA} (pin 3), and a 1 μF smoothing capacitor should be connected between this pin and AGRD (pin 35).
39	AGCI	I/O	***AGC Input.** Test purposes only.
40	TH	O	**Transmit to Hybrid.** Provides the modulated voice data output. Will not drive an impedance less than 50 kΩ.

*Leave disconnected if not required.

Architecture

The T7010 SCM is AT&T 212A compatible and uses the frequency division multiplexing technique to achieve full duplex operation on a 2-wire circuit. It has data transmission rates of 0 to 300 b/s using FSK modulation and 1200 b/s using DPSK modulation. Figure 1 is a diagram of the functional sections of the SCM. The solid blocks indicate all-digital functions and the dashed blocks indicate analog functions.

The SCM functions as a microprocessor peripheral that modulates and demodulates digital data. A basic voice/data modem interface application is shown on Figure 3. On the receive side, the SCM operates directly from the line hybrid with hybrid attenuation of 8.0 dB. On the transmit side, a 600-ohm line drive buffer is required and the total SCM-to-line attenuation must be adjusted to 7.0 dB.

Data is entered on the CSD input. For 1200 b/s transmission, the data may be either asynchronous ASCII character format or a synchronous bit stream. In the asynchronous mode, the asynchronous/synchronous (A/S) circuit locks to the character start bit and converts the data to a synchronous stream for transmission. In the synchronous mode, the A/S circuit is bypassed and the data must be locked to the ST output or a bit clock must be supplied on the DA input and the SCM will lock to this external clock. The data is then scrambled and translated to phase changes of a carrier in the modulator circuit. For 300 b/s transmission, the A/S and scrambler circuits are bypassed and there is no synchronization of the data to the SCM via external clocks. The modulator circuit translates the data into discrete frequencies. The data is then converted from digital to analog and band limited by the transmission filter. The data for transmission on the analog facilities appears on the transmit to TH. The transmit power may be set to either voice or data jack (V/D) levels (see **Analog Characteristics**).

The analog receive data enters the RH input and is band limited in the receive filter. The carrier detect circuit turns on for energy above the threshold level. An automatic gain control (AGC) circuit amplifies the signal. The AGC output goes to: a timing recovery circuit which extracts the symbol clock and phase locks the receiver timing to it; a limiter which converts the signal to TTL levels for the demodulator; and output AGCO for input to an external demodulator, if desired. For 1200 b/s synchronously received data, the demodulator extracts the phase changes off the carrier. The data is then descrambled and converted to asynchronous ASCII character format in the synchronous to asynchronous (S/A) circuit. The customer received data appears on CRD. If synchronous data is sent, the S/A circuit is bypassed and a RT is provided. For 300 b/s received data, the received frequencies are translated to digital data in the demodulator, and the descrambler and S/A circuits are bypassed.

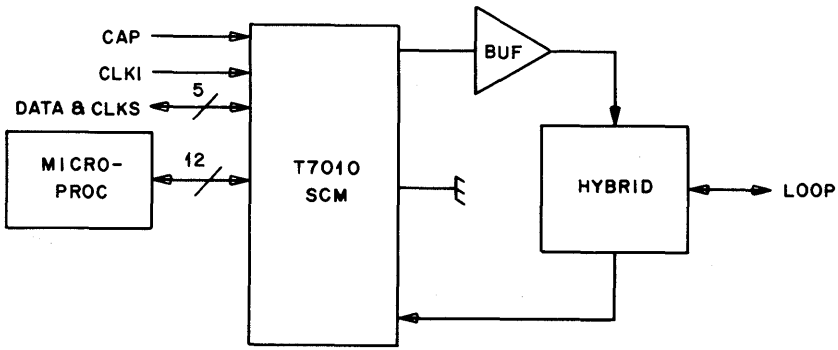


Figure 3. SCM Application

Digital Description

The digital circuitry consists of a microprocessor interface, A/S and S/A character buffers, a scrambler and descrambler, a modulator and a demodulator, a transmit PLL and timing recovery PLL, and an output select circuit.

The SCM can be programmed to provide complete startup handshaking or startup control, or handshake timing may be completely controlled by a microprocessor. A microprocessor interface permits control and monitoring of the SCM by a processor. This interface can be configured to be compatible with microprocessors having multiplexed or separate data and address buses. All control and status information transfer is via the bus. This information consists of data mode, test modes, options, terminal interface, and line interface. The send and receive data and bit clocks and the hybrid interface are separate device inputs and outputs.

Asynchronous to Synchronous and Synchronous to Asynchronous Character Buffers. The A/S and S/A character buffers convert ASCII character format (start bit, data bits, and stop bit) to a synchronous bit stream. In the asynchronous mode there are no bit clocks between the data source and SCM. The buffer synchronizes to a start bit transition, then samples the data bits until a stop bit is detected, at which time it is conditioned to synchronize to the next start bit. The buffer can be set for character lengths of 8, 9, 10, or 11 bits, including start and stop bits. The transmitter and receiver must be set for the same character length. Since the data source is not locked to the SCM, the data may be faster or slower than the transmission rate. The buffer compensates for this by dropping or adding stop bits in the transmitter and reinserting or deleting them in the receiver. The SCM transmitter can accept data at a 2.5% underspeed and can be set to accept data at a 1% (AT&T 212A) or 2.3% (CCITT V.22) overspeed. The SCM receiver can be set to shorten all bits by the overspeed selected or only shorten stop bits by a maximum of 25%.

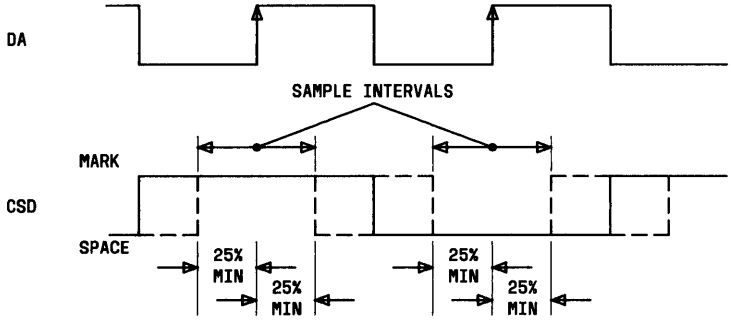
Transmitter Phase Lock Loop. The transmitter timing may be set to free run from the oscillator and provide a bit clock to the data source on ST, phase lock to a bit clock on DA from the data source, or phase lock to the recovered receiver timing. If the DA input is used, the clock supplied must be 1200 Hz ±0.01%. The phase lock loop has a bandwidth of 1200 ± 2.4 Hz and will phase lock in 213 ms.

Scrambler/Descrambler. The scrambler/descrambler is a 17-tap self-synchronizing circuit with taps on bits 14 and 17. The scrambler and descrambler include a protection circuit (to prevent activation of remote digital loop) which inverts the next bit after 64 consecutive 1s at the scrambler output. This protection circuit may be set active or inactive to be either CCITT V.22 or AT&T 212 compatible. The scrambler or descrambler is not used for 300 b/s data.

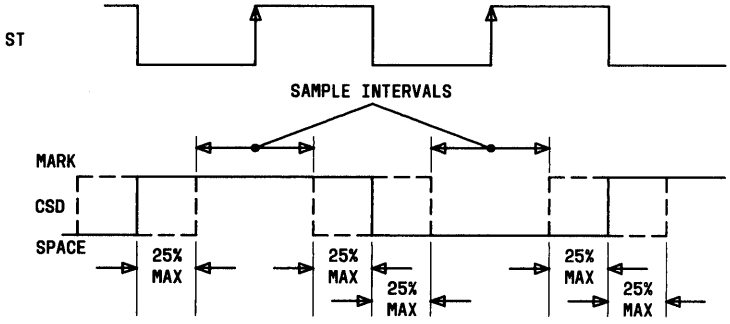
Modulator. The 0 to 300 b/s modulator is frequency shift keyed (FSK). Discrete frequencies are transmitted relative to the send data. The low-band space and mark frequencies are 1070 Hz and 1270 Hz, respectively, and the high-band frequencies are 2025 Hz and 2225 Hz.

The 1200 b/s modulator is differential phase shift keyed (DPSK). The data is grouped into 2-bits and then gray coded into one of four phase changes of a carrier signal every 1.667 ms (1/600 Hz). The phase changes are multiples of 90°. The carrier is 1200 Hz for the low band and 2400 Hz for the high band.

The modulator can also be used for 2400 b/s data transmission by means of a quadrature amplitude modulation (QAM) scheme. This scheme groups four bits into a change in the carrier. The symbol rate (600 Hz) and carrier frequencies are the same as the 1200 b/s modulator.



A. External Timing



B. Internal Timing

Figure 4. Synchronous Transmission Timing

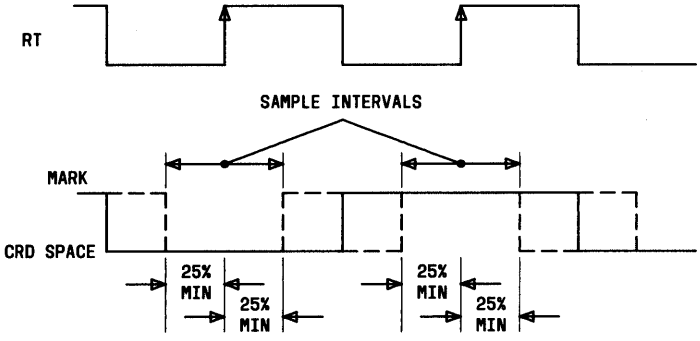


Figure 5. Synchronous Reception Timing

Timing Recovery. The timing recovery phase lock loop tracks a 600 Hz signal which is filtered out of the data signal by the analog circuit. This phase lock loop provides the clocking for the receiver circuits and RT. The phase lock loop has a fast acquire mode during startup of the call which automatically switches to a slow tracking mode when the data mode is entered. The bandwidth is 600 ± 9.3 Hz in the fast mode and 600 ± 0.290 Hz in the slow mode. It will phase lock in 53 ms in the fast mode and 1700 ms in the slow mode. When there is no received signal and the phase lock loop cannot lock, the RT output is 1200 ± 38.7 Hz in the fast mode and 1200 ± 2.4 Hz in the slow mode.

Demodulator. The 0 to 300 b/s demodulator translates the received frequency back to digital data. The 1200 b/s demodulator uses a coherent scheme. The phase changes of the received line signal are determined by comparing the received signal to a fixed reference at the same carrier frequency. These phase changes are then translated back to digital data.

Data Output. This circuit allows the RDI output to be enabled by the carrier detect circuitry giving output on CRD.

Analog Description

Figure 6 is a block diagram of the analog section of the SCM device. RH is conditioned by preamplification and an anti-aliasing filter (receiver filter) before sampling by the band-splitting filters. A multiplex switch selects a high- or low-band filter, depending upon whether the modem is in the originate or answer mode, respectively. A pretrimmed carrier detect circuit determines the received signal level. A linear automatic gain control circuit (AGC) adapts to varying signal levels and provides fixed amplitude signal output. The AGC output is passed to a zero-crossing comparator and to a squarer, 600 Hz filter, and timing recovery comparator. For FSK signal detection, the output of the zero-crossing comparator is passed to a clocked shift register and filter.

In the transmit path from CSD, the signal waveforms are generated digitally and converted to analog by the transmit digital-to-analog converter (Transmit DAC). The relative amplitudes are controlled by precision capacitor matching. The absolute amplitude is factory adjusted. The resulting waveforms are multiplexed through either a high- or low-band filter. When transmitting in high band, an additional 1807 Hz signal may be added to meet European requirements. A 3600 Hz mixer allows analog loop feedback during self test. An anti-alias smoothing filter generates a continuous signal at the output.

Transmitted Voice/Data Signal Levels. The twisted-pair loop port which connects to the modem may be either a data jack or a voice jack. The modem has a switched transmit level that is selectable by the microprocessor. A data jack allows a maximum average line transmit level of −4 dBm and a voice jack that allows a maximum line signal of −9 dBm. The SCM is designed to operate with a hybrid having an attenuation of 8.0 dB from line to SCM (RH) and 7.5 dB from SCM (TH) to line, and a worst case return loss (echo) of 10 dB. All the tones at the different frequencies and amplitudes specified in Table 14 under **Analog Characteristics** are generated on chip. The FSK tones and PSK carrier are output at TH with a voltage equivalent to a 600 Ω power level of 3.0 dBm in data jack mode.

The basic QAM tones are generated at low-band voltage levels equivalent to −2.4 dBm, 4.5 dBm, and 7.1 dBm on a data jack. All transmitted levels are reduced by 5.5 dB when the voice jack option is selected.

As an option when transmitting in the high band only, a 1800 Hz guard tone can be added to the signal at a level of −6 ± 1 dB relative to the normal level of the signal power in the high band. All transmitted levels in the high band are reduced by approximately 1 dB when the 1800 Hz tone is used.

The in-band noise power at the SCM TH output is approximately 1 mVrms. The out-of-band signal power specifications when transmitting data at the output of the SCM device are shown in Table 15.

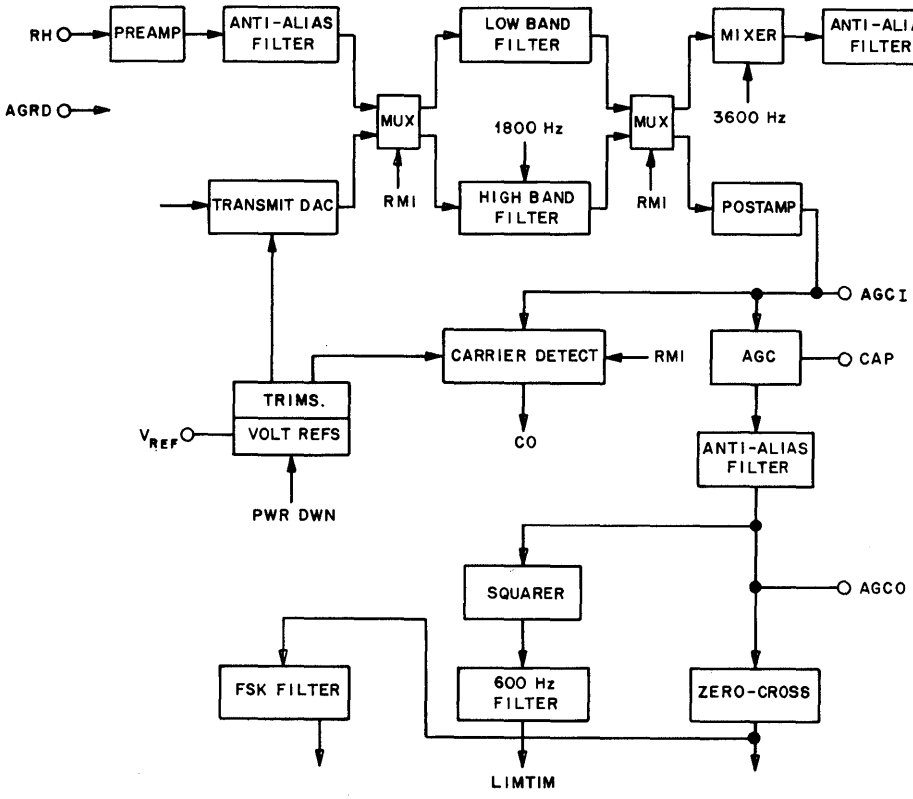


Figure 6. SCM Analog Block Diagram

Analog Signal Processing. The internal high-band/low-band filter absolute gain (0 dB relative gain point) is designed to be 22 dB from RH to AGCI.

The relative filter frequency responses have a passband ripple specification of ±0.7 dB. The high-band filter has a 2 dB slope in the passband. Fixed compromise equalization is included in the modem filters. This equalization is shared equally between transmitter and receiver. The group delay of the transmitter output is designed to be within ±100 μs over the frequency range 800—1600 Hz (low band) and 2000—2800 Hz (high band).

The equivalent noise of the preamplifier and filter referred back to RH is approximately −75 dBm equivalent (135 μVrms).

Automatic Gain Control Circuit. The chip includes an automatic gain control circuit with an adaptive attenuation range of 39 dB. Following power-up, offset levels are acquired in 2 seconds. During handshake, gain acquisition to 1 dB of fully acquired data signal peaks occurs in less than 30 ms. The AGC peak-to-peak output signal is 2 ±1 V. The AGC acquisition and release is inhibited following call setup unless the signal level changes by more than approximately 2 dB for more than approximately 100 ms. The output of the AGC is a continuous analog signal. The noise level measured at AGCO with the filter connected and with zero applied signal at RECH is approximately 65 dBrnC.

Carrier Detect Circuit. The carrier detection function is provided on chip and conforms to V.22 and V.22 bis standards. Carrier detect is indicated before the signal exceeds −51 dBm applied at input RH. It is released for a signal 2 to 3 dB lower than its detect point, but not less than −56 dBm. The acquisition time is 40−205 ms for all coding schemes. Release time for a nonvalid carrier is 17 ±7 ms with FSK and PSK input and 40−65 ms for 2400 b/s QAM.

Registers

The SCM contains ten 8-bit registers, seven of which are write-only and three of which are read-only, which are addressable through the microprocessor bus interface. The write-only registers are used to control and configure the SCM. The read-only registers are used to monitor SCM status. Four address bits define the register addresses. When the most significant address bit (A3) is zero, the remaining bits define registers used in the modem mode where complete AT&T 212 and CCITT V.22 startup and handshaking functions are done within the SCM. When A3 is one, the registers addressed allow the SCM to be used as a transceiver with control and timing of startup done by a microprocessor.

The following register descriptions assume that the user is familiar with AT&T 212-type data set operation, options, and standards. In the register assignment tables, the notation Ribj defines bit j of register i. Set is defined as logic 1 and clear is defined as logic 0. The register addresses are coded in hexadecimal and there is no register 7. Table 2 summarizes the functions of the ten registers and gives the abbreviated name or function of each bit in a register. Tables 3 through 12 describe the function of each register bit.

Table 2. SCM Register Assignments

Register		Address		Register Bits							
Name	No.	A3−A0	R/W	7	6	5	4	3	2	1	0
Line Control	0	0000	W	RNG	TD	H	D1	ASYNC OPTION	DTR	PWR DWN	PWR RST
Customer Control	1	0001	W	TRANSMIT TIMING		VOICE/ DATA	ORIG. SPEED	RDL	AL	DL	ST
Modem Status	2	0010	R	ERR	TM	RM	DSR	SPEED INDICATION		RLS	CTS
Relay & Lamp Drivers	3	0011	R	DLI	STI	SD	RD	CO	ARD	LCRD	RRD
Options A/S & Handshake	4	0100	W	A/S	OVER SPEED	CHARACTER LENGTH		T & R BAND ASSIGNMENTS		PL	ANS TONE
Options CCITT & Disconnect	5	0101	W	DSR AFT TONE	2100 ANS	1800 TONE	AUTO ANS	SSD	RSD	LCD	RRDL
RD, SD Control & Chip Test	6	0110	W	SD CLMP	ST CLMP	RD CLMP	RT CLMP	TEST			TEST RESET
Transceiver Control 1	8	1000	W	BYPASS SCRAM	BYPASS DESC*	BYPASS PROT**	I/E REC	ORIG. SPEED	μP MARK	μP 2100 EN	μP 1800EN
Transceiver Control 2	9	1001	W	μPCON	μPLID	μPHST	μPLST	μPCF	μPCS	SDSEL	SD1100
Transceiver Status	A	1010	R	SSD-TRAN	RDL-CLMP	LID	MID	RDFSK	RDUM	RDSM	RD1100

*DESC is DESCRAM
**PROT is PROTECT

Table 3. Register 0 Modem Line Control & Telephone Interfaces (Write Only)

Bit	7	6	5	4	3	2	1	0
Field	RNG	TD	H	D1	ASYNC OPTION	DTR	PWRDWN	PWRRST

Bit	Name	Description
		Telephone Interface
7	RNG	**Ringing.** Set (1) indicates ringing to the SCM, which in turn sets the transmit and receive bandpass filters in the answer mode and enters the data mode in the answer state. This bit should follow the ringing voltage on the telephone line.
6	TD	**Talk/Data.** Set (1) indicates talk mode. Clear (0) indicates data mode if H (R0b5) is set, or on-hook if H is clear.
5	H	**Loop Current.** Set (1) indicates loop current to SCM (off-hook mode). This bit is only used if TD is used to enter the data mode.
4	D1	**Originate.** Set (1) this bit and then clear (0) to enter the data mode in the originate state. Do not leave in set state.
3	ASYNC OPTION	**Asynchronous Option.** Options the received character timing when in the asynchronous mode (R4b7 = 0). Clear (0) selects the data bits to be at the bit rate and the stop bit to be shortened by up to 25%. Set (1) selects the data and stop bits to all be shortened by up to 2.3%.
2	DTR	**Data Terminal Ready.** Set (1) indicates data terminal ready to the SCM. This bit typically follows the data terminal ready (CD) output of a terminal and indicates to the modem that a terminal is connected.
1	PWRDWN	**Power-Down.** When set (1), the SCM goes into power-down or low-power mode that inhibits clocks and turn off amplifiers. Clear (0) is normal operating mode.
0	PWRRST	**Power Reset.** Set (1) and then clear (0) to perform power-up reset. This initializes the chip after power-up, which must be done to ensure proper operation, and resets all write registers to the clear state, which is the standard 212 default configuration. This bit must be cleared before writing to any other bits. Power reset takes 8 seconds to completely reset the SCM after power-up. PWRRST must not be used between calls to drop the call. This would result in the improper setting of the timers (see R2b4, DSR, Table 5). Clear (0) is normal operating mode.

Table 4. Register 1 Customer Control (Write Only)

Bit	7 6	5	4	3	2	1	0
Field	TRANSMIT TIMING	VOICE/ DATA	ORIG. SPEED	RDL	AL	DL	ST

Bit	Name	Description
7, 6	TRANSMIT TIMING	Synchronous mode options: 00 Internally generated clock used as the transmitter timing reference. This value should be used when in the asynchronous mode. 01 External transmitter timing is phase locked to the DA input. 10 Slave transmitter timing to the local received timing signal. 11 Unused.
5	VOICE/DATA	Transmitter output signal level options: Clear (0) selects data jack mode which gives −4 dBm transmit signal. Set (1) selects voice jack mode which gives −9 dBm transmit signal.
4	ORIG. SPEED	Selects 300 b/s or 1200 b/s data rate for originating modem. R8b3 defines 2400 b/s rate.

R8b3	R1b4	Data Rate	R8b3	R1b4	Data Rate
0	0	300 b/s	1	0	Unused
0	1	1200 b/s	1	1	2400 b/s

		Modem Test Modes
3	RDL	**Remote Digital Loop.** Set (1) requests a remote digital loopback test which places the remote set into a digital loopback mode.
2	AL	**Analog Loop.** Set (1) requests an analog loopback test. This test loops the transmit signal to the receive signal through the hybrid and allows testing of the local data set.
1	DL	**Digital Loop.** Set (1) requests a digital loopback test. This test loops received data to send data at the terminal interface. Thus, data sent from a remote data set can be looped back, testing both data sets and the transmission facility. **Note:** AL and DL must be mutually exclusive.
0	ST	**Self-Test.** Set (1) requests a self-test. In this mode a dotting pattern (alternating ones and zeros) is applied to data sent and then compared to received data. Errors in received data cause ERR (R2b7) to be set. The self-test feature may be used in the data mode or for AL or RDL testing.

Table 5. Register 2 Modem Status to Terminal Interface (Read Only)

Bit	7	6	5	4	3 2	1	0
Field	ERR	TM	RM	DSR	SPEED INDICATION	RLS	CTS

Bit	Name	Description
7	ERR	**Error.** Set (1) indicates a self-test error condition. This bit is reset after a read to this register. It must be reset, by reading register 2 and ignoring data in bit 7, following the initiation of a self-test.
6	TM	**Test Mode.** Set (1) indicates when the modem has entered a test mode by either local or remote activation. This bit is not set until the modem has finished the necessary test startups and has successfully entered the test mode requested.
5	RM	**Ring Memory.** Set (1) indicates that ringing has been detected and the modem has entered the data mode as an answer set. Bit remains set until the end of the call.
4	DSR	**Data Set Ready.** Set (1) indicates that modem has entered data mode and begun handshaking. This bit corresponds to EIA signal CC. It also indicates that a call has completed disconnect (DSR=0) and is ready to begin a new call.
3, 2	SPEED INDICATION	Indicates data rate at which SCM is operating when in data mode. **b3 b2 Data Rate** **b3 b2 Data Rate** 0 0 300 b/s 1 0 Unused 0 1 1200 b/s 1 1 2400 b/s
1	RLS	**Received Line Signal.** Set (1) when handshaking is complete and the received data is valid. This bit corresponds to EIA signal CF.
0	CTS	**Clear to Send.** Set (1) when handshaking is complete, the transmitter is on, and the send data input has been unclamped. This bit corresponds to EIA signal CB.

Table 6. Register 3 Modem Status to Lamps and Relays (Read Only)

Bit	7	6	5	4	3	2	1	0
Field	DLI	STI	SD	RD	CO	ARD	LCRD	RRD

Bit	Name	Description
		Test Mode Indications
7	DLI	**Digital Loop Active.** Set (1) indicates SCM device is in digital loop mode, either locally or remotely activated.
6	STI	**Self-Test Active.** Set (1) indicates SCM device is in self-test mode.
		Customer Data
5	SD	**Send Data.** State of send data at input to modulator.
4	RD	**Received Data.** State of received data at output of demodulator.
3	CO	**Energy Detected.** Set (1) indicates energy is detected on the line.
		Control For Line Interface Relays
2	ARD	**A Relay Driver.** Set indicates line is in use (modem is active).
1	LCRD	**Line Control Relay Driver.** Set (1) indicates to disconnect the telephone from line and connect the modem.
0	RRD	**Ring Relay Driver.** Set (1) indicates to ring the telephone. This bit is a function of R0b7, RNG (Table 3), and some internal conditions of the SCM.

Table 7. Register 4 Options-Asynchronous/Synchronous Converter and Handshaking (Write Only)

Bit	7	6	5 4	3 2	1	0
Field	A/S	OVER SPEED	CHARACTER LENGTH	T & R BAND ASSIGNMENTS	PL	ANSTONE

Bit	Name	Description
7	A/S	**Asynchronous/Synchronous.** This option applies to 1200 b/s and 2400 b/s data rates and is a don't care for 300 b/s data rates. Set (1) selects synchronous data mode; customer uses ST and RT clock outputs to synchronize modem and terminal. Clear (0) selects asynchronous data mode (ASCII character format). Clocks are not used in this mode.
6	OVERSPEED	**Overspeed.** This option only applies in the asynchronous mode. Set (1) for character overspeed of 2.3% over nominal bit rate (CCITT V.22). Clear (0) for 1% overspeed (AT&T 212A).
5, 4	CHARACTER LENGTH	**Character Length.** Character length including start and stop bits (only applies in asynchronous mode). **b5 b4 Length** — **b5 b4 Length** 0 0 10-bit character — 1 0 8-bit character 0 1 9-bit character — 1 1 11-bit character

Table 7. Register 4 Options-Asynchronous/Synchronous (Continued)

Bit	Name	Description
3, 2	T & R BAND ASSIGNMENTS	**Transmit and Receive Band Assignments.** **b3 b2 Band Assignment** 0 0 Normal (originate modem transmits in low band and receives in high band; answer modem transmits in high band and receives in low band). 0 1 Reverse normal band assignment. 1 0 Originate only (force modem to transmit in low band). 1 1 Answer only (force modem to transmit in high band).
1	PL	**Private Line.** Set (1) selects a private line handshaking sequence. This mode eliminates the silent interval before the answer tone is sent in the answer modem (V.22 without V.25 auto-answer). Care must be taken not to select the 1800 Hz option (R5b5) if the low-band is transmitting. Clear (0) selects the normal mode for DDD lines.
0	ANSTONE	**Answer Tone.** Set (1) selects answer tone to be PSK unscrambled mark at 1200 b/s (CCITT compatible). Clear (0) selects answer tone to be a 2225 Hz FSK tone (AT&T 212 compatible). This mode should be selected if 300 b/s operation is to be used.

Table 8. Register 5 Options—CCITT & Disconnect (Write Only)

Bit	7	6	5	4	3	2	1	0
Field	DSR AFT TONE	2100 ANS	1800 Hz	AUTOANS	SSD	RSD	LCD	RRDL

Bit	Name	Description
		CCITT Options
7	DSR AFT TONE	**DSR After Tone.** Set (1) selects DSR (R2b4) of the answer mode modem to turn on after the silent interval following the 2100 Hz tone (CCITT compatible). Clear (0) selects DSR of the answer mode modem to turn on when the modem is connected to the line (212 compatible).
6	2100 ANS	Set (1) selects the 2100 Hz European answer tone to precede the handshaking sequence of the answer mode modem (CCITT compatible). Clear (0) selects a 212 compatible handshaking sequence (no 2100 Hz tone).
5	1800 Hz	Set (1) selects an 1800 Hz guard tone to be transmitted by the answer mode modem during data transmission. Clear (0) disables the 1800 Hz guard tone (212 compatible).
4	AUTOANS	**Automatic Answer.** Set (1) selects the modem to detect ringing and puts the modem in the answer mode, then selects the modem to wait for a manual indication to enter the data mode. Clear (0) selects the modem to detect ringing and puts the modem in the answer mode, and then to automatically enter the data mode if data terminal ready (R0b2) is set.

Table 8. Register 5 Options—CCITT & Disconnect (Write Only) (Continued)		
Bit	**Name**	**Description**
		Modem Disconnect Options
3	SSD	**Send Space Disconnect.** Clear (0) selects the modem to send steady spaces for approximately 4 seconds before disconnecting in response to loss of carrier (line energy) or DTR (R0b2) going low. Set (1) selects disconnecting without sending spaces.
2	RSD	**Receive Space Disconnect.** Clear (0) selects the modem to disconnect in response to steady spaces being received for approximately 1.6 seconds. Set (1) selects the modem to ignore steady spaces being received.
1	LCD	**Loss of Carrier Disconnect.** Clear (0) selects the modem to disconnect if carrier (line energy) is lost for more than 350 ms. Set (1) selects the modem to ignore loss of carrier.
0	RRDL	**Respond to Remote Digital Loop.** Clear (0) selects the modem to respond to a remote digital loop handshaking sequence and enter the digital loop test mode. Set (1) selects the modem to ignore a remote digital loop handshaking sequence.

Table 9. Register 6 Data & Timing Output Clamps and Chip Test (Write Only)

Bit	7	6	5	4	3—1	0
Field	SDCLMP	STCLMP	RDCLMP	RTCLMP	TEST	TEST RESET

Bit	Name	Description
		Customer Data and Timing Output Clamps
7	SDCLMP	**Send Data Clamp.** Set (1) clamps send data input to mark. If the SCM is in data mode it will send scrambled marks. Clear (0) is the normal mode.
6	STCLMP	**Send Timing Clamp.** Set (1) clamps send timing output to mark. Clear (0) is normal mode for synchronous operation.
5	RDCLMP	**Received Data Clamp.** Set (1) clamps received data output to mark. Clear (0) is the normal mode.
4	RTCLMP	**Received Timing Clamp.** Set (1) clamps received timing output to mark. Clear (0) is normal mode for synchronous operation.
		Chip Test
3—1	TEST	Bits 3—1 are 000 for normal operating mode.
0	TEST RESET	Set (1) for manufacture test reset. Clear (0) for normal operation.

Table 10. Register 8 Transceiver Control 1 (Write Only)

Bit	7	6	5	4	3	2	1	0
	BYPASS				ORIG.			
Field	SCRAM	DESCRAM	PROTECT	I/E REC	SPEED	μPMARK	μP2100EN	μP1800EN

Bit	Name	Description
		Scrambler/Descrambler Bypass Control
7	SCRAM	**Scrambler.** Set (1) selects bypassing the scrambler in the transmitter data path. Clear (0) selects the scrambler (normal operation).
6	DESCRAM	**Descrambler.** Set (1) selects bypassing the descrambler in the receiver data path. Clear (0) selects the descrambler (normal operation).
5	PROTECT	Set (1) selects overriding the scrambler/descrambler RDL lockup protection circuit (212 compatible). Clear (0) selects the scrambler/descrambler protection circuit (CCITT V.22 compatible).
4	I/E REC	**Internal/External Receiver.** Clear (0) selects the SCM 1200 b/s coherent demodulator. Set (1) bypasses the SCM demodulator and allows an external demodulator to be connected between the AGCO and the TI and the TO pins.
3	ORIG. SPEED	Clear (0) selects the speed of modem as 300 b/s or 1200 b/s (see R1b4). Set (1) selects the speed of modem as 2400 b/s if R1b4 is also set.
		Transmit Signal Control
2	μPMARK	Set (1) forces transmission of unscrambled marks. This overrides all other send data controls. Clear (0) is normal mode.
1	μP2100EN	Set (1) forces 2100 Hz to be transmitted in the answer mode modem if the low-speed transmitter is enabled. Clear (0) is the normal mode and allows the SCM to time the 2100 Hz tone (if selected by R5b6).
0	μP1800EN	Set (1) forces the 1800 Hz tone to be transmitted in the answer mode modem. This bit can only be set if the data set is transmitting in the high band, that is RM (R2b5) is set. Clear (0) is the normal mode and allows the SCM to time the 1800 Hz tone (if selected by R5b5).

Table 11. Register 9 Transceiver Control 2 (Write Only)

Bit	7	6	5	4	3	2	1	0
Field	μPCON	μPLID	μPHST	μPLST	μPCF	μPCS	SDSEL	SD1100

Bit	Name	Description
Control of Transceiver by Overriding Internal Handshake Timing of SCM		
7	μPCON	Clear (0) is the normal mode for the SCM to operate as a 212 modem with complete handshake and startup timing done within the SCM. Set (1) overrides the handshake timing in the SCM and gives the microprocessor control through R9b6—R9b2. This allows the SCM to be used as a transceiver instead of a complete modem.
6	μPLID	Control of AGC acquire time constant and timing recovery phase lock loop tracking time constant when R9b7=1. Set (1) is slow gear used during data mode. Clear (0) is fast gear used for startup.
5	μPHST	Control of high-speed PSK transmitter (1200 and 2400 b/s) when R9b7=1. Set (1) turns transmitter on. Clear (0) turns transmitter off.
4	μPLST	Control of low-speed FSK transmitter (300 b/s) when R9b7=1. Set (1) turns transmitter on. Clear (0) turns transmitter off.
3	μPCF	Control of carrier detect time interval when R9b7=1. Clear (0) indicates to the SCM transceiver that the RLS time interval has not expired. Set (1) indicates that the RLS time interval has expired.
2	μPCS	Control of the clear to send time interval when R9b7=1. Clear (0) indicates to the SCM transceiver that the CTS time interval has not expired. Set (1) indicates that the CTS time interval has expired.
Control of Send Data To Transmitter (Note: Bits 1, 0 and R6b7 are mutually exclusive.)		
1	SDSEL	Clear (0) is the normal mode for customer send data input. Set (1) overrides clamping of send data due to CTS and some of the test modes and allows direct input to the transmitter.
0	SD1100	Clear (0) is the normal mode. Set (1) forces transmission of scrambled double dotting (alternating 1100 pattern) in 1200 b/s mode. The A/S circuit must be disabled (R4b7=1). Alternating 11110000 will be transmitted if the modem is in 2400 b/s mode.

Table 12. Register A Transceiver Status (Read Only)

Bit	7	6	5	4	3	2	1	0
Field	SSDTRAN	RDLCLMP	LID	MID	RDFSK	RDUM	RDSM	RD1110

Bit	Name	Description
		SCM Handshake Indicators
7	SSDTRAN	Set (1) when the transmitter is sending steady spaces during a send space disconnect. Clear (0) during other modes.
6	RDLCLMP	Set (1) during remote digital loopback handshaking in requesting modem. Clear (0) during the remote digital loopback test and other modes.
5	LID	Clear (0) during idle mode. Set (1) after 232 to 310 ms of PSK scrambled mark has been received and remains set for the remainder of the data mode.
4	MID	Clear (0) during idle mode. Set (1) after 135 to 155 ms of answer tone (2225 Hz or unscrambled FSK mark determined by R4b0) has been received and remains set for the remainder of the data mode.
		Received Data Indicators
3	RDFSK	Set (1) indicates that the receiver has received FSK mark (1270 or 2225 Hz) for at least 135 to 155 ms and is still detecting FSK mark. Clear (0) indicates FSK mark is not being received.
2	RDUM	Set (1) indicates that the receiver has received PSK unscrambled mark for at least 135 to 155 ms and is still detecting PSK unscrambled mark. Clear (0) indicates PSK unscrambled mark is not being received.
1	RDSM	Set (1) indicates that the receiver has received PSK scrambled mark for at least 19 to 38 ms and is still detecting PSK scrambled mark. Clear (0) indicates PSK scrambled mark is not being received.
0	RD1100	Set (1) indicates that the receiver has received unscrambled double dotting in the 1200 b/s mode or quad dotting in the 2400 b/s mode for at least 12 to 18 ms and is still detecting double or quad dotting. Clear (0) indicates double or quad dotting is not being received.

External Demodulator Interface

An external demodulator (I/E REC) operating at 1200 b/s or 2400 b/s can be used instead of the SCM 300 b/s and 1200 b/s receivers. In this case, the SCM still performs the receive band pass filtering, the timing recovery, the automatic gain control, descrambling, and S/A receiver functions. AGCO provides the received signal and the TO pins provide recovered timing clocks to the external demodulator. The TI pins provide data and clocks from the external demodulator to the SCM descrambler circuit. The TI and TO pins also provide access to internal nodes of the SCM for manufacturer testing; they are multiplexed to various nodes via the microprocessor interface.

Operating Modes

Data Mode (Telephone and Terminal Interface)

Data mode entry is determined by the indications provided to the SCM telephone and terminal interface control bits. An originate and answer modem must be defined for full duplex operation to determine which frequency band the SCM device uses for transmitting and receiving. This is accomplished by use of the ringing signal which defines the answer modem and transmission in the high frequency band. The ring memory (RM) indicator is on for the answering SCM device.

The SCM goes into the answer mode when ringing indication (RNG) is provided and data terminal ready (DTR) is on (see Figure 7). The SCM may answer automatically or manually. In the auto answer mode, RNG indication causes the SCM to enter the data mode, i.e., bring up data set ready (DSR) and set the line control relay driver (LCRD) indication. In the manual answer mode, the RNG indication is remembered for 7.25 seconds after a ring. If the originate mode is requested in that interval, then the answer mode is entered. The data mode can then be entered manually by talk/data (TD) going from talk to data while loop current (H) is present or by writing D1 on and off again.

The SCM goes into the originate mode if RNG was not provided and DTR is on. The data mode may only be entered manually as described above.

Modem Mode

In the modem mode, complete AT&T 212 and CCITT V.22 startup and handshaking are done in the SCM device. Once the SCM device enters the data mode (i.e., DSR is brought up), modem handshaking

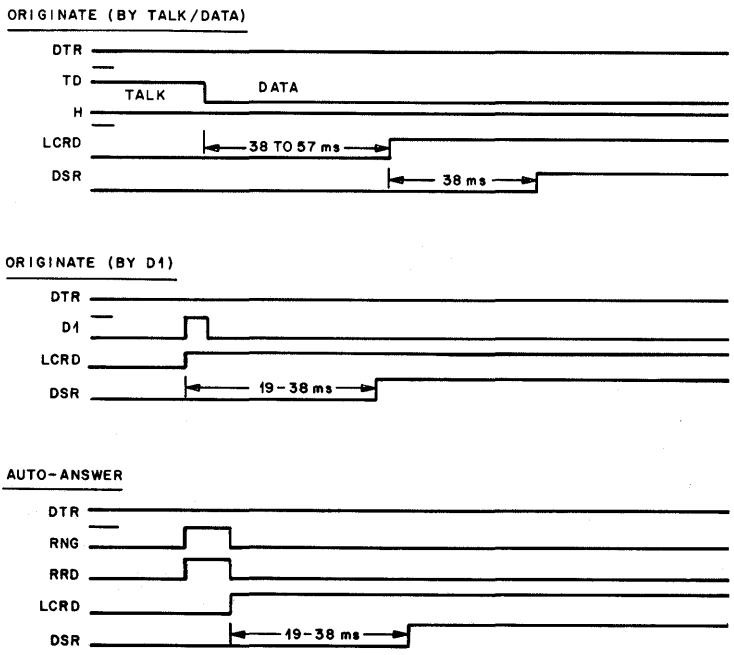


Figure 7. Data Mode Entry

begins. The answering SCM device has a two-second silent interval followed by an optional 2100 Hz tone and a short silent interval. Then the answer ton (optionally unscrambled DPSK mark or 2225 Hz) is sent. A private line option bypasses the two-second silent interval and sends answer tone as soon as DSR is brought up. The answering SCM device then waits for a response from the originating SCM device. If FSK mark is received (300 b/s requested by the originating SCM device), the SCM device interacts at 300 b/s. Then CRD is unclamped and the clear-to-send (CTS) and received line signal (RLS) indications are brought up. If DPSK scrambled mark is received (1200 b/s requested by the originating SCM device), the SCM device interacts at 1200 b/s. The answering SCM responds by transmitting a DPSK scrambled mark in the high band, unclamps CRD, and brings up the CTS and RLS indications. An 1800 Hz tone may be optionally transmitted along with data in the answering SCM.

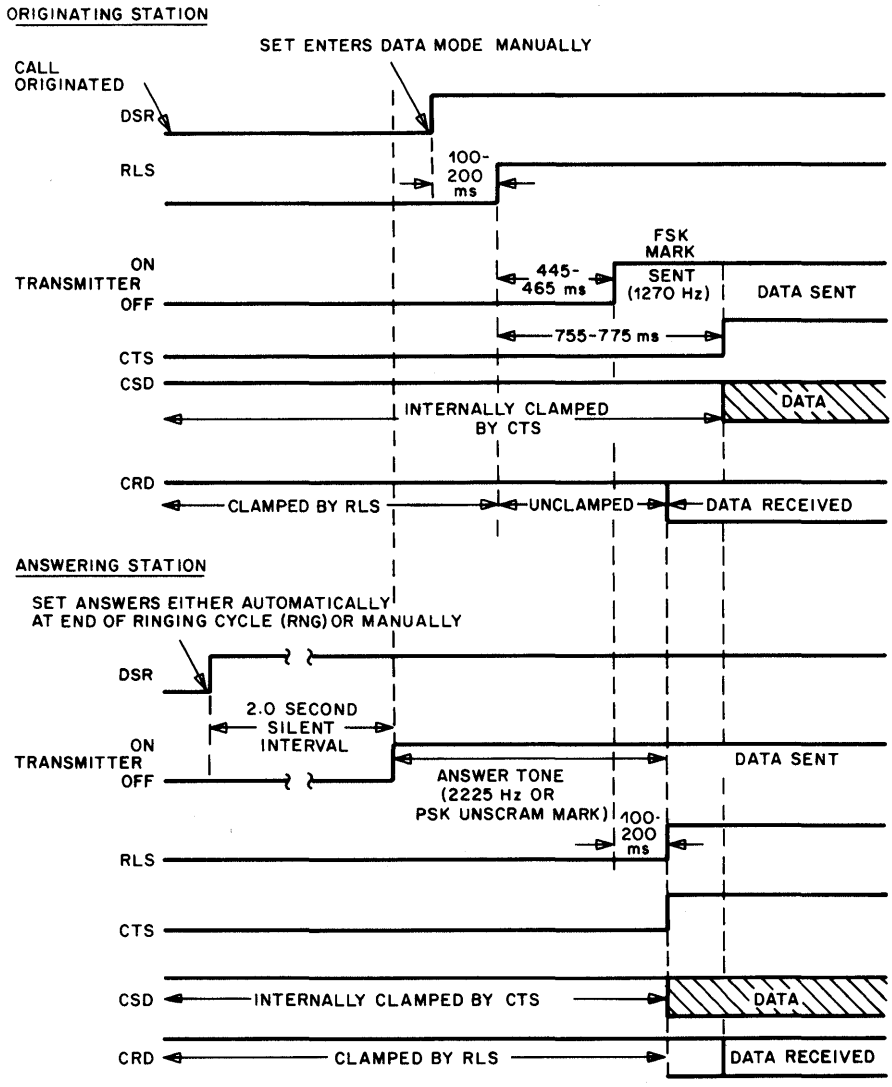
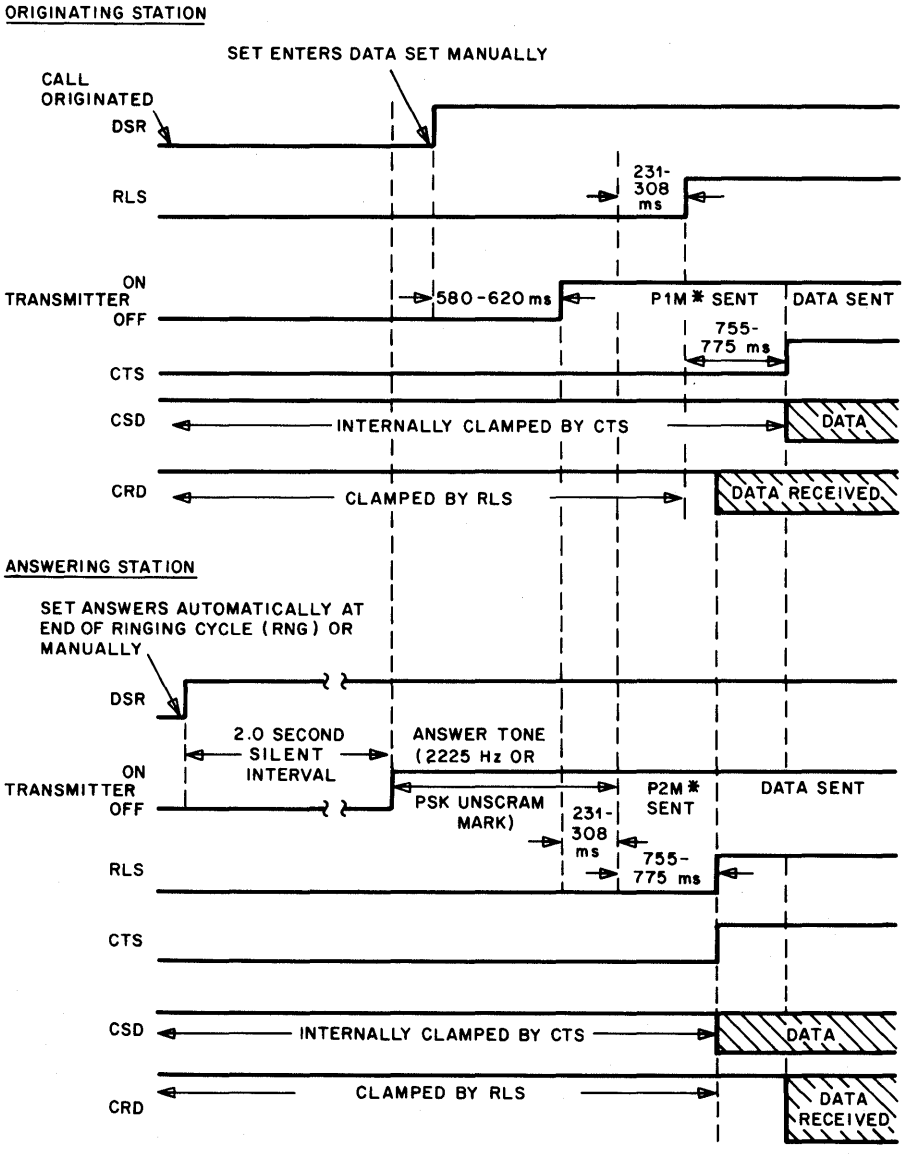


Figure 8. Low-Speed Connect Sequence (DTR On; Automatic or Manual Operation)

Once DSR has been brought up, the originating SCM device will detect the answer tone. If 300 b/s operation is selected (by the ORIG SPEED control) the CTS and RLS indicators will be brought up, the FSK mark is transmitted in the low-band, and CRD clamping is removed. If 1200 b/s operation is selected, a DPSK scrambled mark is transmitted and the originating SCM device waits for a response of a DPSK scrambled mark from the answering SCM device; the CRD clamping is removed and the CTS and RLS indicators are brought up.



*P1M IS THE LOW BAND PHASE SHIFT KEYED SIGNAL REPRESENTING A MARKING DATA SEQUENCE. P2M IS THE SIMILAR SIGNAL IN THE HIGH BAND.

Figure 9. High-Speed Connect Sequence (DTR On; Automatic or Manual Operation)

Transceiver Mode

In the transceiver or the microprocessor control (μPCON) mode, the handshaking timers in the SCM device are disabled and control of startup is through the microprocessor interface. The FSK transmitter (μPLST), the DPSK transmitter (μPHST), the AGC and timing recovery gearshifting (μPLID), the clear-to-send timer signal timer (μPCS), and the received line signal timer (μPCF) are controllable. The SCM device has internal pattern generators that can be selected for transmission. They are unscrambled mark (μPMARK), 1200 b/s double dotting (SD1100), a 2100 Hz tone (μP2100EN), and a 1800 Hz tone (μP1800EN). The SCM device has internal pattern detectors that monitor received data and give an indication of data patterns being received. Two of the indicators, answer tone (MID) and DPSK scrambled mark (LID) time a pattern for a specified time interval and then latch. The remaining indicators time a pattern for a specified time and set a bit; when the pattern goes away the bit clears. These indicators are FSK mark (RDFSK), DPSK unscrambled mark (RDUM), DPSK scrambled mark (RDSM), and 1200 b/s double dotting (RD1100). The scrambler and descrambler circuits may be bypassed (Bypass Scram or Descram).

Disconnect Modes

In the data mode, the SCM device disconnects several ways from either the modem or transceiver modes. It always disconnects if the talk mode is entered or DTR is turned off for more than 50 ms. It may optionally disconnect for loss of a line signal (LCD) for more than 307 ms or spaces being received (RSD) for more than 1.74 seconds. Another option enables the transmission of 4 seconds of space (SSD) before disconnecting due to loss of the line signal or DTR being turned off. Figures 10—14 illustrate the high- or low-speed disconnect sequences.

Test Modes

Standard 212 loopback tests and handshaking control to initiate a remote digital loopback (RDL) are provided. An analog loopback test (AL) connects the transmit signal to the receive signal through the hybrid, permitting the testing of the local SCM device. A digital loopback test (DL) effectively connects CSD to CRD and slaves the transmitter timing to the recovered receiver timing. This permits testing from a remote SCM device.

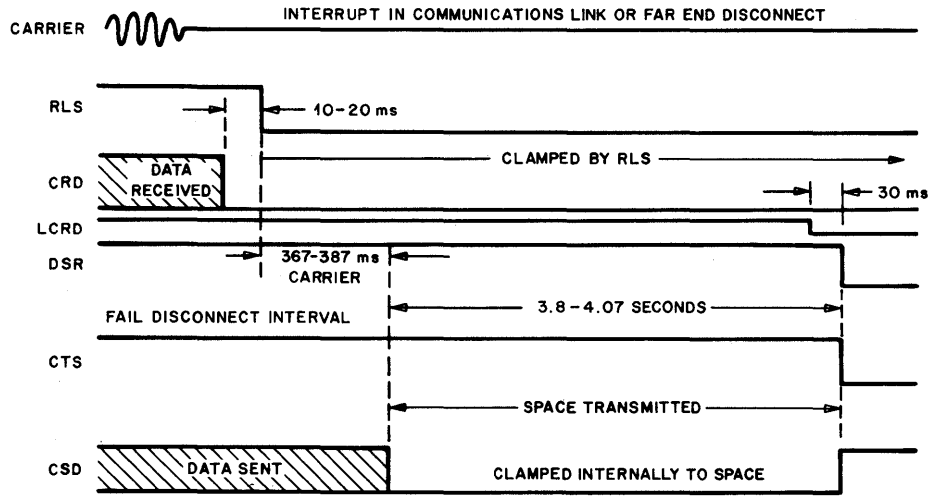


Figure 10. Long Space Transmit by Carrier Fail Disconnect

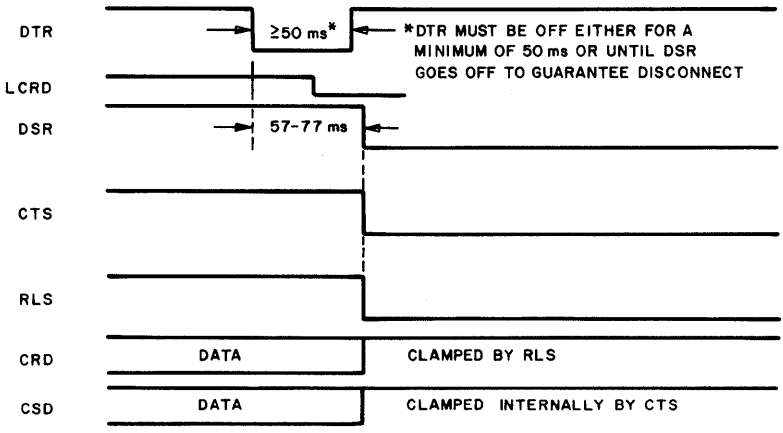


Figure 11. DTR Disconnect

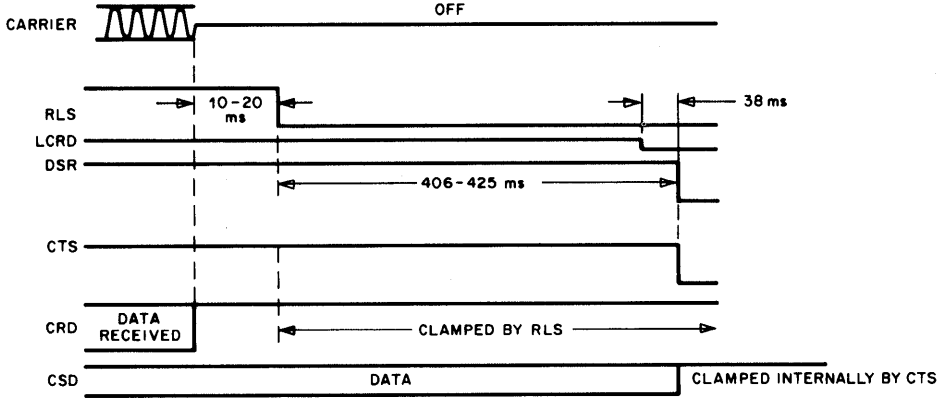


Figure 12. Carrier Fail Disconnect

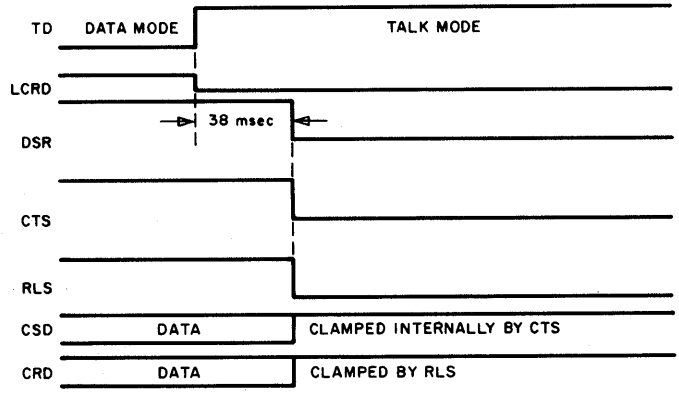


Figure 13. Data-to-Talk Transfer

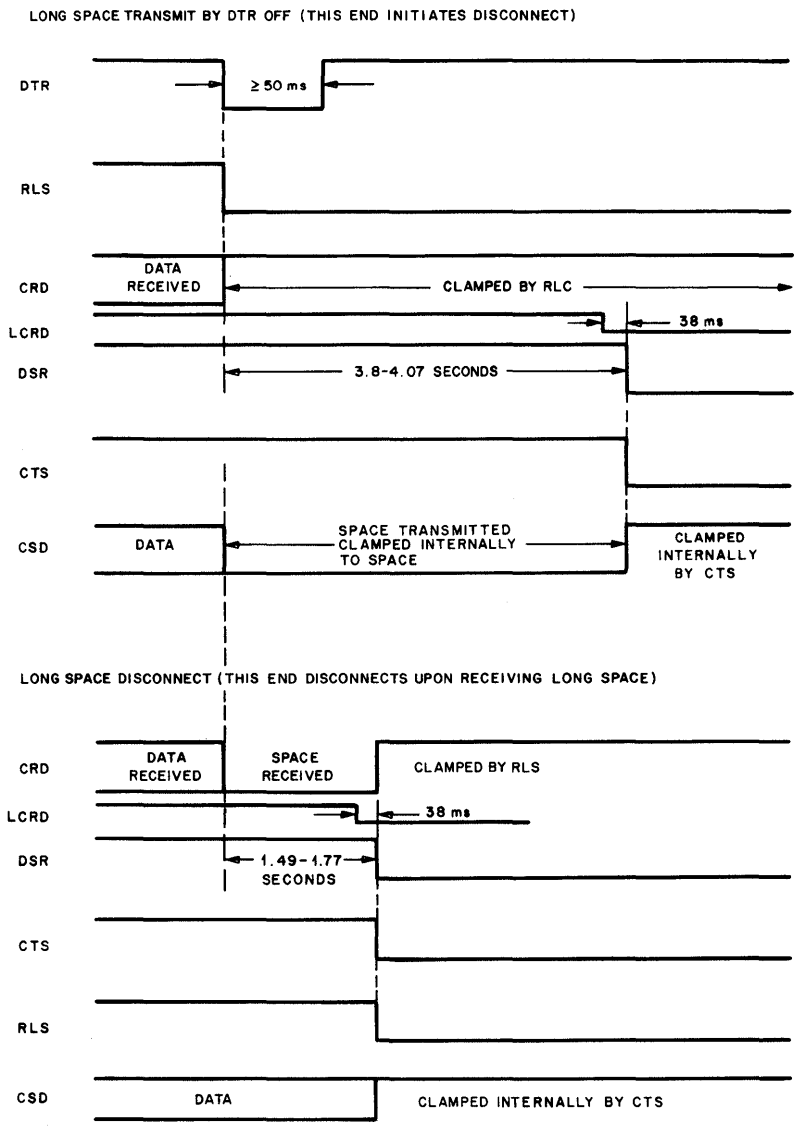


Figure 14. Long Space Transmit and Disconnect

The DL test disables received space disconnect for the remainder of the test and disables loss of carrier disconnect for the remainder of the call. A remote digital loopback test (RDL) initiates a DL from a remote SCM. AL and DL tests can be run at 300 b/s and 1200 b/s data rates; RDL tests can only be initiated at 1200 b/s data rates. A response to RDL (RRDL) option permits disabling of a remotely activated DL.

A self-test generator and error comparator included in the SCM device may be used in the data mode, AL test mode, or RDL test mode. The self-test (ST) generator transmits a dotting pattern which is monitored for errors (ERR) in the receiver. When the SCM device is in a test mode, the test mode (TM) indication is on.

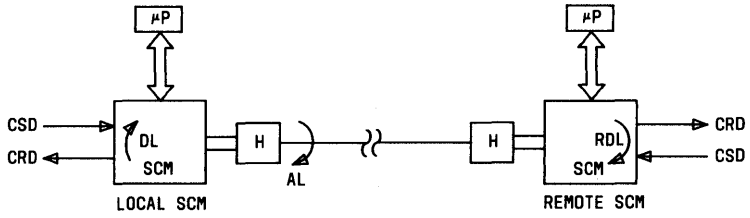


Figure 15. Loopback Tests

212A Compatibility Requirements

Several 212A-compatible options and functions were not included in the SCM device. However, these options and functions can be performed in software by the microcomputer that controls the SCM device. The following list of options and functions provides complete 212A compatibility if performed by the SCM-controlling microcomputer.

- The SCM device will not clamp the CTS, RLS, SPEED INDICATION, or DSR bits (R2b0—R2b4) during the digital loop or self-test mode. The corresponding signals to the customer through the EIA interface (CB, CF, CI, or CC) are clamped by the microcomputer to be 212 compatible.
- The line control bits D1, H, TD, RNG (R0b4—R0b7) are typically inputs from relays or switch contacts in the telephone set. If this is the case, the microcomputer debounces these inputs for approximately 6.5 to 13 ms before passing along an input change to the SCM device.
- The microprocessor keeps the digital loop (DL) and analog loop (AL) (R1b1—R1b2) test request mutually exclusive.
- During an analog loop (AL) test the telephone line is made busy in the 212. The make busy function is part of the telephone line interface circuitry and thus is not in the SCM device. Therefore, when an AL test is requested, the make busy function is also activated.
- When the SCM device is operating in 300 b/s or 1200 b/s asynchronous mode, the send timing (EIA/ST) and received timing (EIA/RT) outputs are not meaningful. These can be clamped (off) under microcomputer control by the STCLMP and RTCLMP bits (R6b4 and R6b6).
- EIA lead CE (ring indicator) can be set in the 212 to turn on only during ringing and then turn off, or to turn on during ringing and remain on for the remainder of the call. The SCM bit RRD (R3b0) indicates when ringing is present and bit RM (R2b5) indicates the modem is in the answer mode until the call is dropped. To accomplish the CE option, the microcomputer can output either (RRD) or (RRD + RM).
- 212 option permits the CB (clear-to-send) and CF (received line signal) EIA signals from the modem to be separate or common. The corresponding SCM bits CTS and RLS (R2b0 and R2b1) operate in the separate mode. To provide the common mode, the microcomputer must turn off CB whenever CF turns off.
- 212 option permits data to cross the EIA interface only in the high speed mode (1200 b/s). The SCM device allows data to cross the interface in 300 b/s or 1200 b/s mode. For this option, the microcomputer must clamp the CB, CF, CI, CC, and BB signals at the EIA interface when the SCM is in the low-speed mode (R2b2 and R2b3 equal 00).
- The 212 has an option to turn on EIA signal CC (data set ready) during analog loop test. The SCM device does not turn on the corresponding DSR bit (R2b4) during analog loop test. For this option, the microcomputer must turn on EIA signal CC in response to bit TM (R2b6) after it requests the SCM device to do an analog loop test (R1b2).

CHARACTERISTICS

Electrical Characteristics

T_A = 0 to 70 °C; V_{DDD} = V_{DDA} = 5 ± 0.25 V; DGRD = AGRD = 0 V; V_{SSA} = −5 ± 0.25 V

Parameter	Symbol	Min	Max	Unit
Input Logic Voltage				
Low	V_{IL}	–	0.8	V
High	V_{IH}	2.0	–	V
Output Logic Voltage				
Low, I_{OL} = 2.0 mA	V_{OL}	–	0.4	V
High, I_{OH} = −80 μA	V_{OH}	2.4	–	V
Output Leakage Current (3-state output high Z)				
High, V_{OH} = 4.5 V	–	–	10	μA
Low, V_{OL} = 0.0 V	–	–	−10	μA
Input Leakage Current (Logic pins)				
High, V_{IH} = 5.0 V	–	–	7.5	μA
Low, V_{IL} = 0.0 V	–	–	−7.5	μA
Input Leakage Current (RH, CAP)	I_{RH}	–	±7	μA
V_{IN} = 0 V	I_{CAP}	–	±1	μA

Operating Conditions

T_C = 0 to 70 °C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{DDD}	4.75	5.0	5.25	V	
	DGRD	0	0	0	V	
	V_{DDA}	4.75	5.0	5.25	V	
	V_{SSA}	−4.75	−5.0	−5.25	V	
	AGRD	0	0	0	V	
Power Supply Noise Ripple Voltage		–	–	≤1	mVp–p	0–3 kHz and multiples of (153 kHz ± 3 kHz)
Power Supply Current	I_{DD}	9.1	11.5	14.6	mA	
	I_{SSA}	−7.5	−10.0	−13.0	mA	

Maximum Ratings

Continuous Output Current (From Any Output) ..... 10 mA
Voltage range of any digital lead relative to DGRD ..... −0.5 to +5.5 V
Ambient Operating Temperature Range (TA) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... −40 to +95 °C
Continuous voltage range of any analog lead relative to AGRD ..... (−5 ± 0.25) V to (5 ± 0.25) V

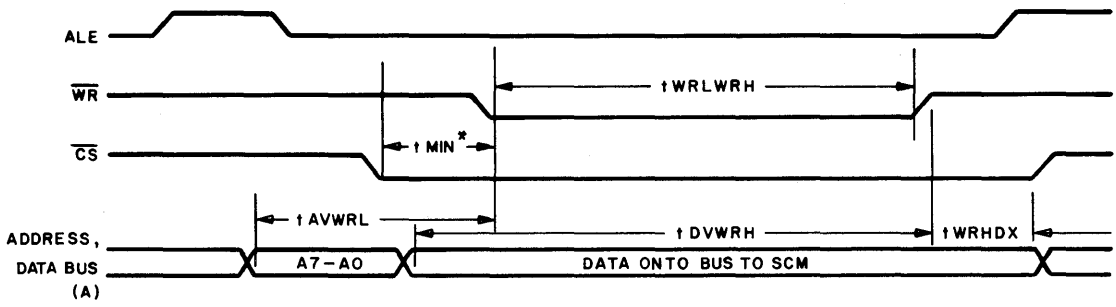
Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

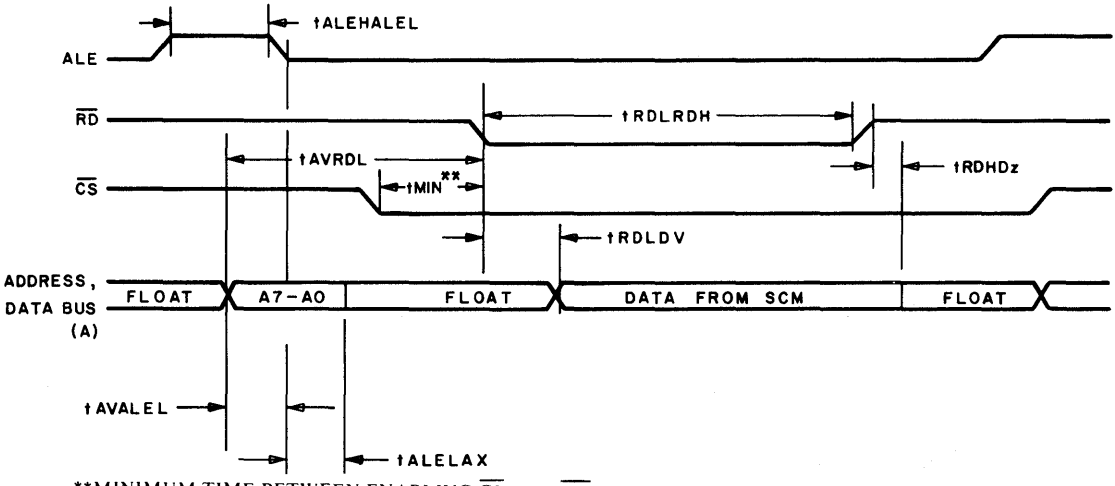
$V_{DDD} = V_{DDA} = 5 \pm 0.25$ V, $C_C = 100$ pF

Symbols	Description	Min	Max	Unit
tALEHALEL	ALE Pulse Width	70	—	ns
tALELAX	Address Hold After ALE	40	—	ns
tAVALEL	Address Set-Up to ALE	40	—	ns
tAVRDL	Address to $\overline{RD}$	110	—	ns
tAVWRL	Address to $\overline{WR}$	110	—	ns
tDVWRH	Data Set-Up Before $\overline{WR}$	220	—	ns
tRDHDZ	Data Float After $\overline{RD}$	—	75	ns
tRDLDV	$\overline{RD}$ to Valid Data Out	—	200	ns
tRDLRDH	$\overline{RD}$ Pulse Width	300	1 ms	ns
tWRHDX	Data Held After $\overline{WR}$	70	—	ns
tWRLWRH	$\overline{WR}$ Pulse Width	200	—	ns



* MINIMUM TIME BETWEEN ENABLING $\overline{CS}$ AND $\overline{WR}$ (0 sec)

A. Register Being Written



**MINIMUM TIME BETWEEN ENABLING $\overline{CS}$ AND $\overline{RD}$ (0 sec)

B. Register Being Read

Figure 16. Timing Diagrams

Analog Characteristics

Table 13. Input Voice/Data Signal Levels

Parameter	Data Jack	Voice Jack
Max. transmitted signal on line	−4.0 dBm average	−9 dBm worst case
Max. echo at the SCM (RH)	−6.0 dBm (1.10 Vp-p)*	−11 dBm (0.617 Vp-p)*
Max. received signal at SCM (RH)	−20 dBm (0.217 Vp-p)*	−17 dBm (0.306 Vp-p)*

* For FSK the peak-to-peak voltages shown are correct. For 1200 b/s PSK and 2400 b/s QAM, the peak-to-peak voltages are increased by 1.4 and by 1.9, respectively.

Table 14. Typical Output Signal Levels (TH) for 212L1A and V.22
(T_A = 0 to 70 °C, V_{DDD} = V_{DDA} = 5 ± 0.25 V, V_{SSA} = −5 ± 0.25 V)

	FSK				PSK		Guard	Answer	Unit
	1070	1270	2025	2225	1200	2400	1800	2225, 2100	Hz
Data Jack									
Without 1800 Hz Tone	3.0	3.0	2.5	2.5	3.0	3.0	—	2.5	dBm
With 1800 Hz Tone	—	—	—	—	—	2.0	−2.5	—	dBm
Voice Jack									
Without 1800 Hz Tone	−2.5	−2.5	−3.0	−3.0	−2.5	−2.5	—	−3.0	dBm
With 1800 Hz Tone	—	—	—	—	—	−3.5	−8.0	—	dBm

Table 15. Transmitter Out-Of-Band Power Limits at Specific Frequencies

Frequency (F)	Line	SCM Output (TH)	
3995−4005 Hz	<−22 dBm	<−13.5 dBm	<164 mVrms
4−12 kHz	<−18 dBm	<−9.5 dBm	<335 mVrms
12−90 kHz	<(23−40 log F) dBV*	<(31.5−40 log F) dBV*	<10 mVrms
90 kHz−1 MHz	<−55 dBV	<−46.5 dBV	<4.7 mVrms

*Where F is a number in the range of 12−90 and represents kHz.

FEATURES

- Signal separation for two-to-four wire operation
- DTMF generation for dialing
- Detection of call progress tones/status
- Low-power standby mode
- Asynchronous access to registers
- AGC audio output for customer monitoring
- Facilitates lower modem system cost

DESCRIPTION

The T7011 Modem Interface Chip (MIC) integrated circuit operates as a standard microprocessor peripheral providing the interconnection required between a modem and a telephone network. Previous modem subsystems required several ICs and discrete devices to implement the functions available on a single T7011 MIC. The T7011 MIC is fabricated using VLSI CMOS technology, requires 5 and −5 V supplies, and is available in a 24-pin plastic DIP.

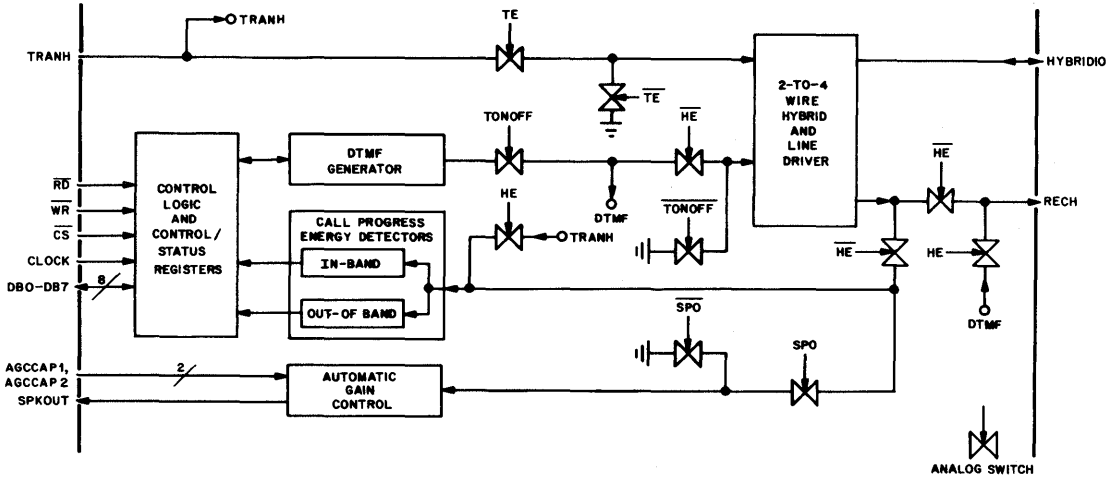
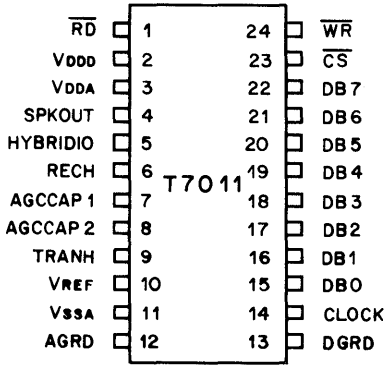


Figure 1. T7011 Modem Interface Chip Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin
AGCCAP1	7	RECH	6
AGCCAP2	8	SPKOUT	4
AGRD	12	TRANH	9
CLOCK	14	VDDA	3
$\overline{CS}$	23	VDDD	2
DB0–DB7	15–22	VREF	10
DGRD	13	VSSA	11
HYBRIDIO	5	$\overline{WR}$	24
$\overline{RD}$	1		

Figure 2. T7011 Pin Diagram and Alphabetical Listing of Symbols

Table 1. T7011 Pin Descriptions

Pin	Symbol	Type	Name/Function
1	$\overline{RD}$	I	**Read.** Used with $\overline{CS}$ (pin 23) to read the internal status register via the data bus.
2	VDDD	–	**5 V (Digital) Supply.** Connect a 5.0 μF electrolytic and 0.1 μF ceramic capacitor between this pin and DGRD (pin 13). Tie directly to VDDA (pin 3).
3	VDDA	–	**5 V (Analog) Supply.** Tie directly to VDDD (pin 2).
4	SPKOUT	O	**Speaker Out.** Automatic gain controlled analog output for monitoring call progress. This output is maintained at 1.5 V peak for an input between −40 and −16 dBm and has an impedance of 2 kΩ.
5	HYBRIDIO	I/O	**Hybrid I/O.** Analog I/O pin for connection to the primary side of the coupling transformer. See **Two-to-Four Wire Hybrid** under **Functional Description.**
6	RECH	O	**Receive from Hybrid.** Analog output with an impedance of 2 kΩ for connection to modem receive. When combined with the T7010 Switched Capacitor Modem (SCM), this pin is connected to pin 1 (RH) on the T7010 SCM.
7	AGCCAP1	–	**AGC Time Constant Adjustment Pin 1.** Connect a 1.0 μF electrolytic capacitor between this pin (+ terminal to AGCCAP1) and AGRD (pin 12).
8	AGCCAP2	–	**AGC Time Constant Adjustment Pin 2.** Connect a 1.0 μF ceramic nonelectrolytic capacitor between this pin and AGRD (pin 12).

Table 1. T7011 Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
9	TRANH	I	**Transmit to Hybrid.** High impedance analog input (50 kΩ) for connection to modem transmit. When combined with the T7010 Switched Capacitor Modem (SCM), this pin is connected to pin 40 (TH) on the T7010 SCM.
10	VREF	—	**Voltage Reference.** Connect a 5.0 μF electrolytic capacitor between this pin (+ terminal to VREF) and VSSA (pin 11).
11	VSSA	—	**−5 V (Analog) Supply.** Connect a 5.0 μF electrolytic and 0.1 μF ceramic capacitor between this pin and AGRD (pin 12).
12	AGRD	—	**Analog Ground.** Tie to DGRD (pin 13).
13	DGRD	—	**Digital Ground.** Tie to AGRD (pin 12).
14	CLOCK	I	**Clock Input.** Used for internal timing: frequency = 4.9152 MHz ± 100 PPM, with a duty cycle of 50% ± 10%.
15–22	DB0–DB7	I/O	**Data Bits 0–7.** Bidirectional data bus used to write to control register and read the status register.
23	$\overline{CS}$	I	**Chip Select.** Used when writing to or reading the registers.
24	$\overline{WR}$	I	**Write.** Used with $\overline{CS}$ to write a control byte to the control register via the data bus.

System Application

The use of the T7011 MIC with a 1200 b/s modem and a microprocessor is shown on Figure 3. Since the operation of the T7011 device is independent of the modem, the T7011 MIC is suitable for use with low- and high-speed modem systems.

Note: The T7010 is configurable for 300, 1200, or 2400 b/s.

Functional Description

Control/Status Registers. The functions of the T7011 MIC are controlled by writing to its control register and monitored by reading its status register. The control register is an 8-bit latch and the status register

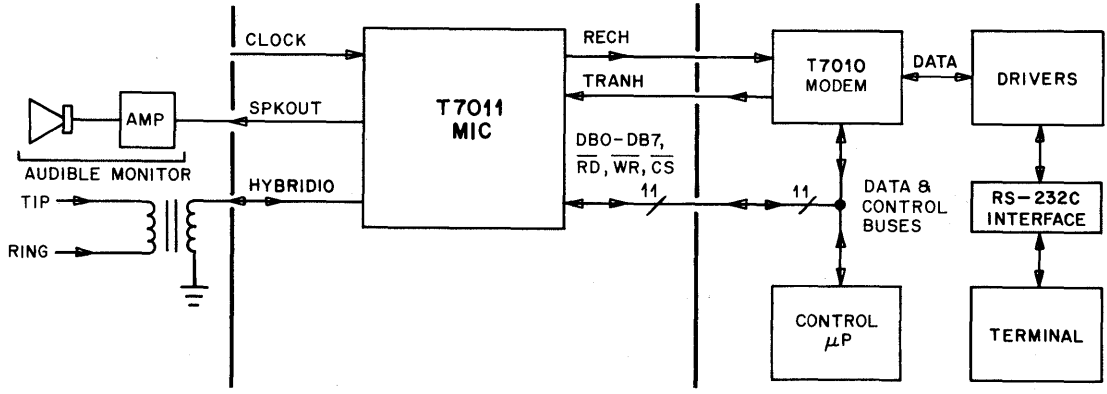


Figure 3. Typical System Application

uses the 7 most significant bits. Both can be accessed asynchronously through a microprocessor-compatible I/O bus (see Tables 2 and 3).

Two-to-Four Wire Hybrid. Conversion of receive and transmit signals between a four-wire modem and a two-wire telephone loop is achieved through an electronic hybrid (differential amplifier) and a 600 Ω line driver. The operation of the hybrid is directed by control register bit 6 (HE).

When the hybrid is enabled (HE = 0), operation is in the two-wire mode. The signals received at HYBRIDIO are routed through the hybrid to RECH, SPKOUT, and the detectors (IBE, OBE). Any generated dual-tone multifrequencies (DTMFs) go through the hybrid to HYBRIDIO. The signals received at TRANH may be routed through the hybrid, depending on the status of the control register bit 5 (TE), to HYBRIDIO.

When the hybrid is disabled (HE = 1), operation is in the four-wire mode. The signals received at TRANH are routed only to SPKOUT and the detectors (IBE, OBE). Also, any generated DTMFs go to RECH.

Note: The IC hybrid resistors were chosen to match the AT&T 2624P, 2624H or 2713D Transformers. The matching provides maximum sidetone rejection for a 600 Ω line termination.

Standby Mode. In the low-power standby mode, only the digital portion of the chip is active. The control/status registers and control logic are always operational. This power saving feature is especially attractive for application in portable communication instruments. The T7011 MIC goes into low-power standby mode by writing 07H to the control register and returns to normal operation by subsequently writing any other code to the control register. The status of the power standby mode can be determined by reading STDBYN (bit 1 of the status register).

DTMF Generation. Dual-tone multifrequencies (DTMFs) are generated for dialing. Single tones may be generated for testing. Tone generation is controlled by a 5-bit combination. Any one of the 16 DTMFs or 8 single tones can be generated by writing the specific bit pattern to the control register (see Table 4). The state of tone generation can be determined by reading TONOFF (bit 2 of the status register).

Call Progress Tone Detectors. Energy detectors are used to indicate the presence of a dial tone, busy signal, or ring signal. For example, a busy signal after dialing can be indicated by monitoring the cadence of the in-band-energy (IBE) detector. The out-of-band-energy (OBE) detector is used to disqualify a signal as being supervisory. This automatic call progress detection feature can be especially useful for customers who cannot audibly monitor the call. The status of IBE and OBE is accessed by reading the status register bits 3 and 4, respectively.

Audio Output. The audio output (SPKOUT) provides audible monitoring of a call in progress. This function is enabled by writing a "1" to bit 7 (SPO) of the control register. Likewise, the status of this function may be observed by reading bit 7 of the status register. When enabled, the SPKOUT output is established at a constant level of 1.5 V peak by an automatic gain control (AGC) circuit for call progress input signals over the normal range of −40 dBm to −16 dBm. When disabled, the SPKOUT output voltage is limited to less than 2 mV RMS.

Power Supplies. There are two power supply connections for 5 V: V_{DDA} and V_{DDD}. The analog portion of the chip is supplied by V_{DDA}. The digital portion is supplied by V_{DDD}. However, the substrate of the integrated circuit is connected to both V_{DDA} and V_{DDD}. If separate positive power supplies are used, the potential for signal noise is increased as the disparity between the amplitudes of the positive supplies increases. For this reason, V_{DDA} and V_{DDD} should be tracking supplies. A better solution is to connect V_{DDD} and V_{DDA} (pins 2 and 3) together at the T7011 MIC terminals and use a single source of 5 V power.

Table 2. Control Register Format – Write Option

Bit	7	6	5	4	3	2	1	0
Field	SPO	HE	TE	B4	B3	B2	B1	B0

Bit	Symbol	Name/Description
7	SPO	**Speaker Output.** When set (1), SPKOUT (pin 4) is enabled. When cleared (0), SPKOUT is disabled.
6	HE	**Hybrid Enable.** When HE is cleared (0), the hybrid is enabled and operates in the two-wire mode. When HE is set (1), the hybrid is disabled and operates in the four-wire mode.
5	TE	**Transmit Enable.** If HE is clear (0), the TE bit can enable or disable the TRANH signal from passing through the hybrid to HYBRIDIO. When TE is set (1), the TRANH signal is enabled. When TE is cleared (0), TRANH is disabled and provides low noise output at HYBRIDIO (pin 5).
4–0	B4–B0	**Tone Control Bits and Standby.** See Table 4.

Table 3. Status Register Format – Read Option

Bit	7	6	5	4	3	2	1	0
Field	SPO	HE	TE	OBE	IBE	TONOFF	STDBYN	–

Bit	Symbol	Name/Description
7	SPO	**Speaker Output Status.** Set (1) indicates enabled; clear (0) indicates disabled.
6	HE	**Hybrid Enable Status.** Clear (0) indicates enabled; set (1) indicates disabled.
5	TE	**Transmit Enable Status.** Set (1) indicates enabled; clear (0) indicates disabled.
4	OBE	**Out-of-Band Energy Status.** Set (1) indicates energy present; clear (0) indicates energy absent.
3	IBE	**In-Band Energy Status.** Set (1) indicates energy present; clear (0) indicates energy absent.
2	TONOFF	**Tone On/Off Status.** Set (1) indicates tone on; clear (0) indicates tone off.
1	STDBYN	**Standby/Normal Status.** Set (1) indicates normal power operation; clear (0) indicates low-power operation.
0	–	Not used.

Table 4. Tone Control Bit Patterns

Control Register					Function		
B4	B3	B2	B1	B0			
0	0	0	0	0	Terminate single tone, DTMF, or low-power operation.		
0	0	0	0	1	Reserved, do not use.		
0	0	0	1	0			
0	0	0	1	1			
0	0	1	0	0			
0	0	1	0	1			
0	0	1	1	0			
0	0	1	1	1	Operate in low-power standby mode until normal power operation returns by subsequent write of any other code.		
					Frequency (Hz)	**Telephone Digit**	**Action**
0	1	0	0	0	697	–	Single Tone
0	1	0	0	1	770	–	Single Tone
0	1	0	1	0	852	–	Single Tone
0	1	0	1	1	941	–	Single Tone
0	1	1	0	0	1209	–	Single Tone
0	1	1	0	1	1336	–	Single Tone
0	1	1	1	0	1477	–	Single Tone
0	1	1	1	1	1633	–	Single Tone
1	0	0	0	0	941 + 1336	0	DTMF
1	0	0	0	1	697 + 1209	1	DTMF
1	0	0	1	0	697 + 1336	2	DTMF
1	0	0	1	1	697 + 1477	3	DTMF
1	0	1	0	0	770 + 1209	4	DTMF
1	0	1	0	1	770 + 1336	5	DTMF
1	0	1	1	0	770 + 1477	6	DTMF
1	0	1	1	1	852 + 1209	7	DTMF
1	1	0	0	0	852 + 1336	8	DTMF
1	1	0	0	1	852 + 1477	9	DTMF
1	1	0	1	0	941 + 1209	*	DTMF
1	1	0	1	1	941 + 1477	#	DTMF
1	1	1	0	0	697 + 1633	–	DTMF
1	1	1	0	1	770 + 1633	–	DTMF
1	1	1	1	0	852 + 1633	–	DTMF
1	1	1	1	1	941 + 1633	–	DTMF

CHARACTERISTICS

Electrical Characteristics

T_A = 0 to 70 °C, V_{DDD} = V_{DDA} = 5 V ± 5%, DGRD = AGRD = 0 V, V_{SSA} = −5.0 ± 0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
Input Logic Voltage					
(Low)	V_{IL}	–	–	0.8	V
(High)	V_{IH}	2.0	–	–	V
Output Logic Voltage					
(Low, I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	V
(High, I_{OH} = −80 μA)	V_{OH}	2.4	–	–	V
Output Leakage Current (3-state output high-Z)					
(High, V_{OH} = 4.5 V)	–	–	–	10	μA
(Low, V_{OL} = 0.0 V)	–	–	–	−10	μA
Input Leakage Current (Logic pins)					
(High, V_{IH} = 5.0 V)	–	–	–	7.5	μA
(Low, V_{IL} = 0.0 V)	–	–	–	−7.5	μA
External Load Resistance (Applied)	R_L @ RECH	50	–	–	kΩ
	R_L @ SPKOUT	50	–	–	kΩ
Input Resistance	R_I @ TRANH	–	50	–	kΩ
Output Resistance	R_O @ HYBRIDIO	–	487	–	Ω
	R_O @ SPKOUT	–	2000	–	Ω

Maximum Ratings

Continuous Output Current (from any output) ..... 10 mA
Voltage range of any digital lead relative to DGRD ..... −0.5 to +7.0 V
Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... −40 to +95 °C
Continuous voltage range of any analog lead relative to AGRD (not to exceed power supply voltages) ..... ±5.0 V ± 5%

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Operating Conditions

T_A = 0 to 70 °C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{DDD}	4.5	5.0	5.5	V	
	DGRD	0	0	0	V	
	V_{DDA}	4.5	5.0	5.5	V	–
	V_{SSA}	−4.5	−5.0	−5.5	V	
	AGRD	0	0	0	V	
Power Supply Noise Ripple Rejection	PSRR	−55	−65	–	dB	1 kHz
		−35	−45	–	dB	3 kHz
Power Supply Current (Normal)	IDD	8.5	10.0	15.0	mA	–
	ISSA	−7.5	−10.0	−14.0	mA	–
Power Supply Current (Standby)	IDD	–	1.5	3.0	mA	V_{IL} = 0.8 V, max
	ISSA	–	0.2	1.0	mA	V_{IH} = 3.5 V, min

DTMF Signal Characteristics

Description	Min	Typ	Max	Unit
Frequency variation per frequency component	−1.0	–	1.0	%
Time from −55 dBm to 90% of steady state per frequency component	–	–	5	ms
Voltage amplitude per frequency component, low group	−4.7	−3.2	−2.1	dBm
Voltage amplitude per frequency component, high group	−2.2	−0.7	1.2	dBm
Voltage amplitude per frequency pair	−0.2	1.2	3.0	dBm
Voltage amplitude per frequency pair, difference	–	–	4.0	dB
Extraneous signals 500—3000 Hz, dB below DTMF	30	–	–	dB

Note: The DTMF signals should meet these output levels when using the following test standards:

1. The HYBRIDIO pin is terminated with a resistive load of 935 Ω. This is the reflected impedance as measured on the primary of the AT&T 2624P Transformer at 1800 Hz (mid-frequency) when the secondary is connected to a 600 Ω telephone line.
2. When measuring dBm, a high-impedance instrument calibrated for 600 Ω termination is used.

Hybrid Characteristics

Description*	Min	Typ	Max	Unit
Gain from TRANH to HYBRIDIO	−1	—	1	dB
Gain from HYBRIDIO to RECH	−1	—	1	dB
Gain from TRANH to RECH	—	−23	−19	dB
HYBRIDIO (THD)**	−55	−63	—	dB

*The hybrid is tested with a 935 Ω resistive load at HYBRIDIO.
**Total Harmonic Distortion (THD)

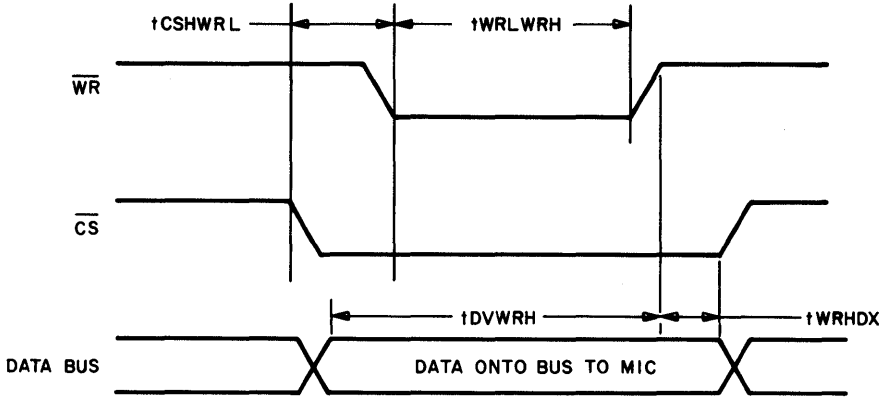
Call Progress Tone Detector Characteristics

Symbols	Description	Typical	Unit
IBE	Frequency Range	300 to 650	Hz
	Sensitivity	−16 to −40	dBm
	On Time Response	20 to 40	ms
	Off Time Response	10 to 35	ms
OBE	Frequency Range	825 to 3000	Hz
	Sensitivity	−16 to −40	dBm
	On Time Response	20 to 40	ms
	Off Time Response	10 to 35	ms

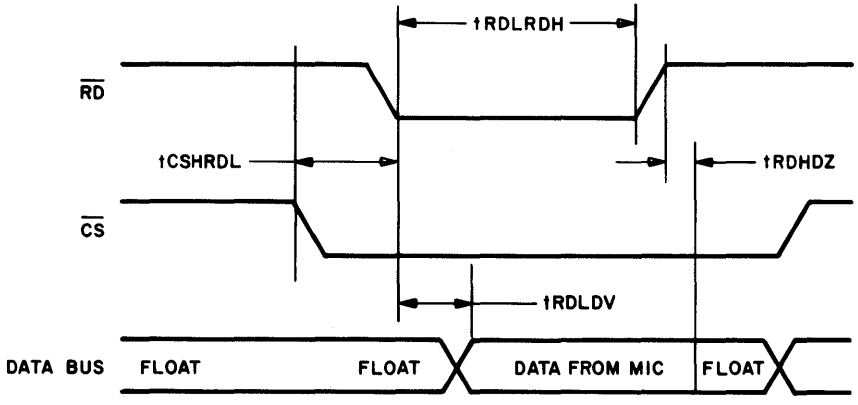
Timing Characteristics

$V_{DDD} = V_{DDA} = 5.0 \pm 0.5$ V, $C_C = 100$ pF, $T_A = 0$ to 70 °C

Symbols	Description	Min	Max	Unit
tCSHRDL	$\overline{CS}$ Hold Before $\overline{RD}$	110	—	ns
tCSHWRL	$\overline{CS}$ Hold Before $\overline{WR}$	110	—	ns
tDVWRH	Data Set-Up Before $\overline{WR}$	220	—	ns
tRDHDZ	Data Float After $\overline{RD}$	—	75	ns
tRDLDV	$\overline{RD}$ to Valid Data Out	—	200	ns
tRDLRDH	$\overline{RD}$ Pulse Width	300	—	ns
tWRHDX	Data Held After $\overline{WR}$	70	—	ns
tWRLWRH	$\overline{WR}$ Pulse Width	200	—	ns



A. Registers Being Written



B. Registers Being Read

Figure 4. Timing Diagram

The information contained herein is advance and subject to change.

FEATURES

- 2400 b/s compatible with V.22 bis
- 1200 b/s compatible with 212A or CCITT V.22
- 300 b/s compatible with AT&T 103
- Supports AT&T command set
- 1800 Hz guard tone compatibility
- Asynchronous or synchronous operation for 1200 and 2400 b/s
- Programmable AGC audio output for call progress signal monitoring
- Call progress signal detection
- DTMF tone generation
- Adaptive equalization for 1200 and 2400 b/s
- True self-test using analog loopback
- Digital loopback and remote digital loopback capability
- Pretrimmed carrier detect on-chip
- Transmit level selectable for voice data jack applications
- On-chip differential electronic hybrid with selectable 2- or 4-wire operation.
- On-chip 600 Ω differential line driver

DESCRIPTION

The T7019 Modem Analog Companion Processor performs analog processing functions required for modem applications. It is controlled through a serial interface by the T7018 device, an 8397 16-bit microcontroller. The T7019 device is used as a companion device to the T7018 16-bit microcontroller to form a 300/1200/2400 bps intelligent modem subsystem that meets a variety of different standards. These standards include CCITT V.22 bis, CCITT V.22, AT&T 212A, and AT&T 103. The T7019 chip is manufactured in CMOS technology and is packaged in a 28-pin plastic DIP or 28-pin SOJ small outline package. The T7018 chip is packaged in a 68-pin pin grid array (PGA) or a 68-pin plastic leaded chip carrier (PLCC). Both use a single 5 V supply.

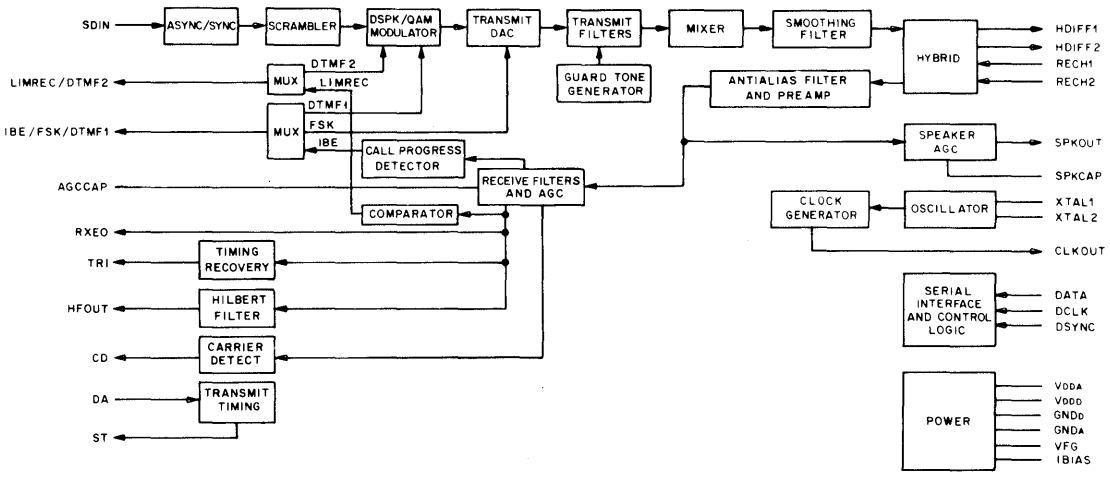


Figure 1. T7018 Modem Companion Processor Block Diagram

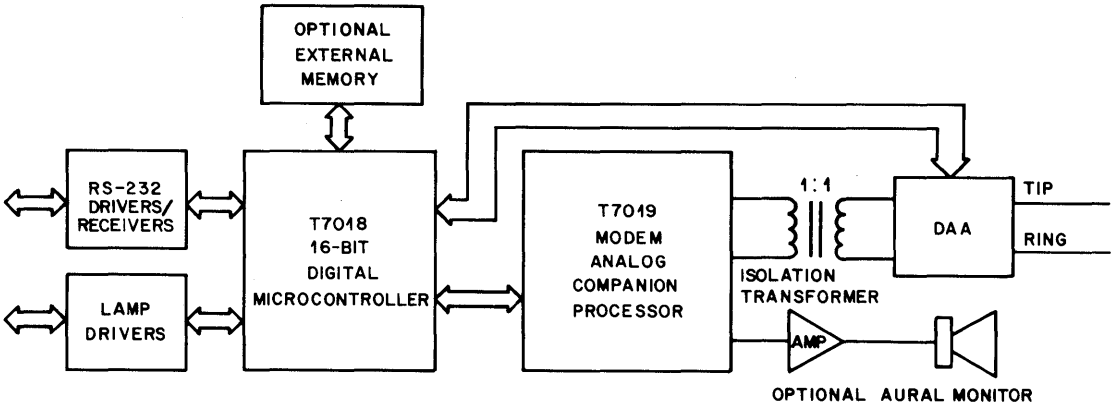


Figure 2. Application Diagram of T7018/T7019 Chip Set for 300/1200/2400 bps Modem

FEATURES

- 5 MHz clock (max)
- 250 kb/s serial data rate (max)
- 8-bit data bus
- 16-bit address bus
- 6 bidirectional address leads for accessing internal registers
- Link initialization and supervision
- Error detection and automatic recovery via packet retransmission
- Automatic appending and testing of 16-bit frame check sequence (FCS) field
- Zero-bit insertion and deletion (for data transparency)
- Programmable address field
- Modulo-8 frame sequence numbering
- 3-bit programmable window size (k)
- Four independently programmable timers (T1—T4)
- Wait-state generator (on DMA side) for slow memory
- Triple-channel DMA with standard interface
- Programmable retransmission counter (N2)
- Password exchange mechanism for dial-up operation
- Daisy-chain DMA structure for easy expansion to multiple XPC-8 applications
- Transmit and receive data buffers accessed indirectly through a look-up table
- Memory error service via external parity checking circuitry
- Programmable bus interface to enable the XPC-8 to be configured for a Motorola or Intel bus
- Two independent test configurations (far-end loopback and near-end loopback) to verify XPC-8 operation and physical level services
- 3-state output buffers to assist system diagnostics
- Programmable flag-fill option that specifies the minimum number of flags between frames

DESCRIPTION

The T7100A X.25 Protocol Controller integrated circuit is a level 2 controller with an 8-bit data bus (XPC-8). It is a single-chip VLSI device fabricated using NMOS silicon gate technology, requires a single 5 V supply, and is available in a 48-pin ceramic DIP. The XPC-8 implements the data link control functions defined in the X.25 packet switching communication standard. It satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. The XPC-8 also is in compliance with CCITT X.25 1980 and ISO 7776 (which is at the draft international standard (DIS) level). The protocol controller is byte-oriented, with a maximum transmit and receive data rate of 250 kb/s. All inputs and outputs are TTL-compatible.

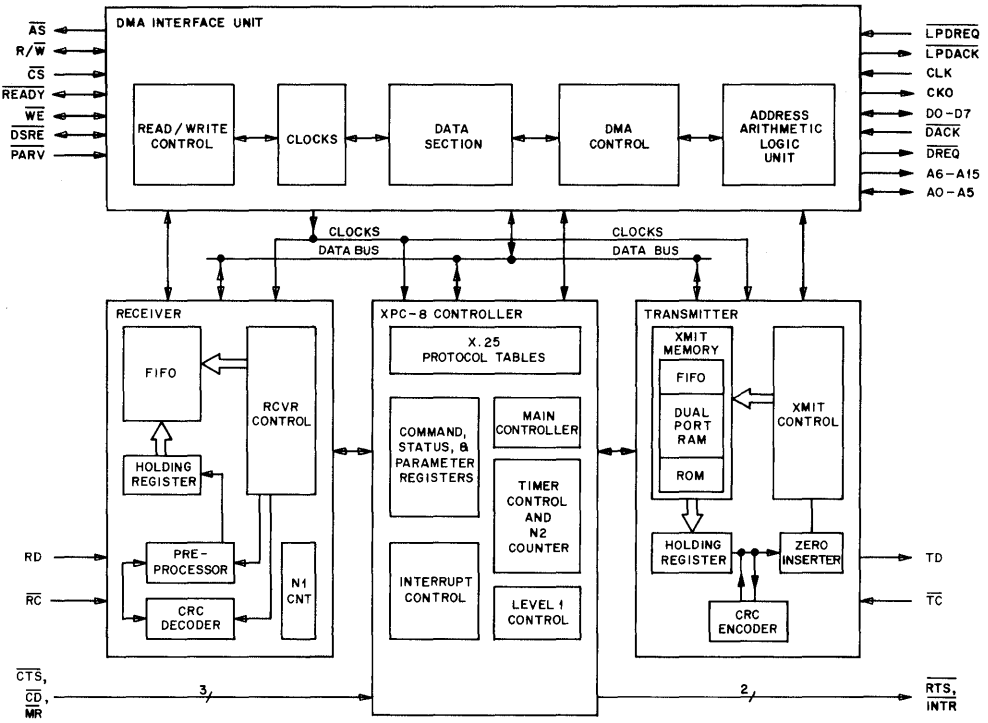
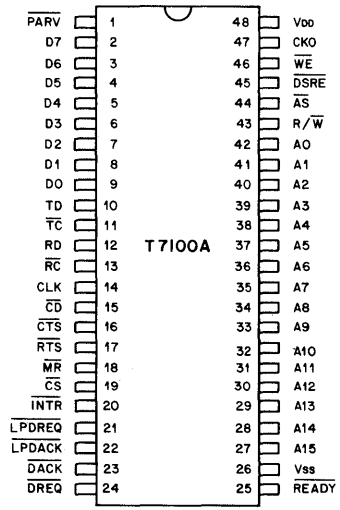


Figure 1. T7100A X.25 Protocol Controller (XPC-8) Block Diagram

USER INFORMATION

Pin Descriptions



Sym	Pin	Sym	Pin	Sym	Pin
A0	42	$\overline{AS}$	44	$\overline{DSRE}$	45
A1	41	$\overline{CD}$	15	$\overline{INTR}$	20
A2	40	CKO	47	$\overline{LPDACK}$	22
A3	39	CLK	14	$\overline{LPDREQ}$	21
A9	38	$\overline{CS}$	19	$\overline{MR}$	18
A5	37	$\overline{CTS}$	16	$\overline{PARV}$	1
A6	36	D0	9	$\overline{RC}$	13
A7	35	D1	8	RD	12
A8	34	D2	7	$\overline{READY}$	25
A9	33	D3	6	$\overline{RTS}$	17
A10	32	D4	5	R/$\overline{W}$	43
A11	31	D5	4	$\overline{TC}$	11
A12	30	D6	3	TD	10
A13	29	D7	2	VDD	48
A14	28	$\overline{DACK}$	23	VSS	26
A15	27	$\overline{DREQ}$	24	$\overline{WE}$	46

Figure 2. T7100A Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7100A X.25 Protocol Controller Pin Descriptions

Pin(s)	Symbol	Type	Name/Function
1	$\overline{\text{PARV}}$	I	**Parity Valid.** Notifies the XPC-8 that external parity checking circuitry has detected an error on an attempted DMA read or write operation. If this occurs on two consecutive attempts at running a bus cycle, then a hard parity error (HPE) interrupt will be generated (see Tables 7 and 8).
2—9	D7—D0	I/O*	**8-Bit Data Bus.** Used by the host CPU to access XPC-8 on-chip registers. Used by the XPC-8 during DMA operations to access system memory.
10	TD	O	**Transmit Data.** XPC-8 serial data output line.
11	$\overline{\text{TC}}$	I	**Transmit Clock.** 1x clock input needed to operate the transmitter.
12	RD	I	**Receive Data.** XPC-8 serial data input lead.
13	$\overline{\text{RC}}$	I	**Receive Clock.** 1x clock input controlling receiver operations.
14	CLK	I	**Master Clock Input.** Controls internal chip sequencing. The clock input must have a minimum frequency of 250 kHz ($f_{CLK} \geq 17\ f_{RC}$ and $f_{CLK} \geq 17\ f_{TC}$) and a maximum frequency of 5 MHz.
15	$\overline{\text{CD}}$	I	**Carrier Detect.** Indicates that the level 1 interface (e.g., a modem) is receiving and modulating a usable signal. Transitions on this signal cause interrupts (see Table 8). The state of the $\overline{\text{CD}}$ lead does not otherwise affect XPC-8 operation.
16	$\overline{\text{CTS}}$	I	**Clear-To-Send.** Indicates to the XPC-8 that the level 1 interface is ready. The data link will not come up until $\overline{\text{CTS}}$ is asserted (low). $\overline{\text{CTS}}$ must remain low while the link is up, or else an interrupt occurs (see Table 8) and the XPC-8 enters an inactive state until $\overline{\text{CTS}}$ is re-asserted (low).
17	$\overline{\text{RTS}}$	O	**Request-To-Send.** Indicates that the XPC-8 is requesting the physical link. $\overline{\text{RTS}}$ remains low while the link is up.
18	$\overline{\text{MR}}$	I	**Master Reset.** Resets the XPC-8 and selects between Motorola and Intel bus configurations. When low, all XPC-8 outputs are in the 3-state condition.
19	$\overline{\text{CS}}$	I	**Chip Select.** Must be asserted (low) to allow access to internal XPC-8 registers. When asserted, R/$\overline{\text{W}}$, $\overline{\text{WE}}$, $\overline{\text{DSRE}}$, and A0—A5 become inputs; $\overline{\text{READY}}$ becomes an output.
20	$\overline{\text{INTR}}$	O	**Interrupt Request.** Indicates that the XPC-8 is requesting interrupt service. This lead goes high when the CPU reads the interrupt register.
21	$\overline{\text{LPDREQ}}$	I	**Low Priority DMA Request.** Used to daisy-chain DMA requests in systems that use more than one XPC-8 without a bus arbiter. If daisy-chain DMA is not being used, $\overline{\text{LPDREQ}}$ must be tied high (5 V).
22	$\overline{\text{LPDACK}}$	O	**Low Priority DMA Acknowledge.** Used to daisy-chain acknowledgments in systems using more than one XPC-8 without a bus arbiter.

* Indicates 3-state output capability during normal operations.

Table 1. T7100A X.25 Protocol Controller Pin Descriptions (Continued)			
Pin(s)	**Symbol**	**Type**	**Name/Function**
23	$\overline{\text{DACK}}$	I	**DMA Acknowledge.** When the host CPU drives this pin low, the XPC-8 has been granted use of the system bus. $\overline{\text{AS}}$, $\overline{\text{DSRE}}$, R/$\overline{\text{W}}$, $\overline{\text{WE}}$, and the address pins become outputs.
24	$\overline{\text{DREQ}}$	O	**DMA Request.** When low, the XPC-8 is requesting use of the system bus.
25	$\overline{\text{READY}}$	I/O*	**Ready.** This pin is pulled low by the XPC-8 when a CPU read or write to an on-chip register is completed. During DMA cycles, the XPC-8 executes wait states until this lead is pulled low to indicate that the current read or write access has been completed.
26	VSS	—	**Ground.**
27—36	A15—A6	O*	**16-Bit Address Bus.** When $\overline{\text{CS}}$ is asserted (low), A0—A5 are used in the input mode to address the internal registers of the XPC-8. All sixteen address lines are used to access system memory during DMA cycles.
37—42	A5—A0	I/O*	
43	R/$\overline{\text{W}}$	I/O*	**Read or Write.** Indicates whether the next data transfer performed is a read (high state) or a write (low state). This signal may be used to control the direction of external bidirectional buffers placed on the data leads.
44	$\overline{\text{AS}}$	O*	**Address Strobe.** This signal is used for both Motorola and Intel read and write operations. When low, it signifies that a valid memory address is currently on the address leads.
45	$\overline{\text{DSRE}}$	I/O*	**Data Strobe or Read Enable.** The mode of this signal is determined during master reset. In a Motorola bus configuration, $\overline{\text{DSRE}}$ becomes a data strobe. In an Intel bus configuration, $\overline{\text{DSRE}}$ becomes a read enable.
46	$\overline{\text{WE}}$	I/O*	**Write Enable.** This signal goes low when the XPC-8 performs a DMA write operation in either Intel or Motorola bus modes. For Intel bus mode, $\overline{\text{WE}}$ is used as an input when the CPU accesses the internal XPC-8 registers ($\overline{\text{CS}} = 0$). For Motorola bus mode, $\overline{\text{WE}}$ should be connected to VDD through an external resistor (10 kΩ typical value). It should not be connected directly to VDD, as damage may occur when $\overline{\text{WE}}$ switches to an output during DMA operations.
47	CKO	O	**Clock Output.** Buffered internal clock, runs at half the frequency of the input clock.
48	VDD	—	**5 V Supply.**

* Indicates 3-state output capability during normal operation.

Overview

The XPC-8 performs complete link-level control according to the X.25 data communications protocol. It generates supervisory and unnumbered frames automatically without intervention by the host CPU. The host CPU must initialize the XPC-8 and supply buffers for the data fields of received and transmitted information frames. The CPU is notified of important events via interrupts. The XPC-8 contains a transmitter, a receiver, an XPC-8 controller, and an interface unit (see Figure 1).

Architecture

Transmitter

The transmitter constructs frames on command from the XPC-8 controller. It handles the transmission of continuous flags, aborts, and idle-channel indications automatically. It contains a transmitter controller, 4-byte first-in-first-out (FIFO) buffer, RAM, ROM, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. The FIFO is used for temporary storage of data delivered from host memory to the transmitter by the interface unit via Direct Memory Access (DMA). The transmitter memory (RAM/ROM) is used to store the various bytes needed to construct a frame. Frames are formed by sequentially loading the holding register with bytes read from the transmitter memory and FIFO, serially shifting these bytes through the zero inserter and, finally, sending the bit stream out on the transmit data (TD) lead. Data is shifted on the falling edge of the transmit clock ($\overline{TC}$). The CRC encoder calculates the frame check sequence (FCS) and appends it following the control field or following the data field for frames with data. The zero inserter performs bit stuffing to ensure data transparency.

Receiver

The receiver processes incoming data and notifies the XPC-8 controller of received frames and other link conditions. It contains a preprocessor, receiver controller, 6-byte FIFO, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link and removes the zeros inserted for data transparency. Frames are identified and checked for proper format by the receiver controller. Data received as part of the information field of a frame is loaded into the FIFO. The interface unit, informed of the presence of received data, is responsible for reading data out of the FIFO and writing it to system memory.

Frames are checked for errors by means of the FCS in the CRC decoder. The XPC-8 acts only on frames that are received error-free. Frames received with errors are discarded. Frames with addresses other than the programmed command or response address are also discarded.

Interface Unit

The interface unit provides the interface between the host CPU and the XPC-8 transmitter and receiver via triple-channel DMA (Direct Memory Access). It consists of four sections: an address arithmetic logic unit (AALU), a data section, a read/write controller, and a DMA controller.

The AALU contains four registers (not user-accessible) that are used to calculate and store the buffer pointers and byte counters for the transmit and receive channels. A fifth register is used to implement a third DMA channel for the processing of received acknowledgments. The additional channel enables the host to use its memory more efficiently by freeing the transmit data buffers as acknowledgments are received for them. Data throughput is also increased as a result of the enhanced memory management capabilities, as compared to implementation in software.

The read/write controller generates the control signals to access data from the host memory, while the data section routes the data from the host memory to various XPC-8 internal locations. The DMA controller coordinates the actions of the other three sections and connects them to the XPC-8 controller.

Under command of the XPC-8 controller, the DMA controller is instructed to open data buffers for the transmitter and receiver in system memory. The locations of these data buffers are specified by the TLOOK and RLOOK table elements that the host CPU supplies.

When data is available for the transmitter, the read-write machine fetches bytes of data from system memory and routes them through the data section to the transmitter FIFO. The DMA continues to

load bytes of data into the transmitter FIFO until the FIFO is full. The transmitter signals the interface unit for more data when two bytes or less remain in the FIFO. The loading process ends when the number of bytes specified in the TLOOK element has been loaded into the transmitter FIFO. The TLOOK element corresponding to the frame being sent is then placed in the unacknowledged state.

The reverse process is used for the receiver. The DMA controller instructs the read-write controller to write bytes of received data out to system memory via the data section when the receiver FIFO contains two or more bytes of data. The interface unit continues to write out data until it is notified by the receiver of an error-free end-of-frame condition. At this time, it finishes writing out the remaining bytes of data, updates the RLOOK element with the number of bytes received, and places the element into the frame complete state. If the receiver reports an error condition at the end of the frame, the RLOOK element is untouched and remains in the ready state.

XPC-8 Controller

The XPC-8 controller handles the interface between the transmitter, the receiver, and the interface unit, and contains all the logic needed to implement the X.25 protocol. Some specific tasks of the XPC-8 controller include configuring the link as specified by the parameter and command registers, maintaining the status registers, directing the interface unit to acquire receive or transmit data buffers, directing the transmitter to send specific frames, managing timing functions, and notifying the host CPU of certain data link conditions through a set of interrupts.

Principles of Operation

CPU Interface

The CPU has access to 27 internal XPC-8 registers. These registers are used to configure and monitor the XPC-8. The CPU configures the XPC-8 by writing the command and parameter registers. Status information can be accessed by reading one of the eight status registers and is used to monitor XPC-8 operations. The CPU is notified of special events with an interrupt. Special events are encoded in the interrupt register, which can then be accessed by the CPU.

Each register is assigned a unique address and can be accessed by providing the proper Motorola or Intel read/write cycle while the XPC-8 is selected ($\overline{CS}$ is low). Table 2 lists the XPC-8 register addresses.

Table 2. XPC-8 Register Addresses

Register Name	Symbol	Address (Hex)
Command Register	CR	00
Status Register 0	SR0	01
Status Register 1	SR1	02
Status Register 2	SR2	03
Status Register 3	SR3	04
Status Register 4	SR4	05
Status Register 5	SR5	06
Status Register 6	SR6	07
Status Register 7	SR7	08

Table 2. XPC-8 Register Addresses (Continued)		
Register Name	**Symbol**	**Address (Hex)**
Interrupt Register	IR	09
Parameter Register 0	PR0	0A
Parameter Register 1	PR1	0B
Parameter Register 2	PR2	0C
Parameter Register 3	PR3	0D
Parameter Register 4	PR4	0E
Parameter Register 5	PR5	0F
Parameter Register 6	PR6	10
Parameter Register 7	PR7	11
Parameter Register 8	PR8	12
Parameter Register 9	PR9	13
Parameter Register 10	PR10	14
Parameter Register 11	PR11	15
Parameter Register 12	PR12	16
Parameter Register 13	PR13	17
Parameter Register 14	PR14	18
Parameter Register 15	PR15	19
Parameter Register 16	PR16	1A

XPC-8 Registers

The XPC-8 registers are divided into four classes: command, status, interrupt, and parameter.

- **Command Register** (read/write) – controls seven XPC-8 functions: send permission, receive permission, mandatory disconnect, active/passive link initialization, password exchange mode, password verification, and link disconnect mode (see Table 3).
- **Status Registers** (read only) – these eight registers contain information regarding the present status of the XPC-8. The status registers provide such information as the present state of the XPC-8, V(S), V(R), NA, and LNA (see Figure 3 and Tables 4, 5, and 6).
- **Interrupt Register** (read only) – contains a 5-bit interrupt code and a lost interrupt (LSTIN) bit. This register is backed by a 4-byte FIFO buffer whose output is automatically loaded into the interrupt register as soon as the contents of the register have been read by the CPU. If the 4-byte buffer overflows, the LSTIN bit of this register is set. The LSTIN bit is cleared as soon as the interrupt register is read. A zero interrupt code indicates that all of the outstanding interrupts have been read by the host (see Tables 7 and 8).
- **Parameter Registers** (write only) – these seventeen registers specify system constants and modes of operation. Examples include timer values, window size, TLOOK starting address, command and response address, test modes, etc. Parameter Registers 1–16 can only be written when the logical link is disconnected and MDISC = 1 (see Figure 4 and Table 9).

Table 3. Command Register Definitions

Bit	7	6	5	4	3	2	1	0
Field	DISCMOD	PWOK2	PWOK1	PWXCH	ACT/PAS	RECR	MDISC	SEND

Bit	Symbol	Name/Description
0	SEND	**Send.** Controls the transmission of packets. If 0, it inhibits the XPC-8 from sending new packets. If 1, it enables the XPC-8 to send new packets. Retransmissions occur automatically, regardless of the SEND bit state. SEND is cleared during a valid reset or if a hard parity error occurs during a transmit channel DMA operation (see Table 8).
1	MDISC	**Mandatory Disconnect.** If 0, logical link establishment is permitted. If 1, the logical link goes to a logically disconnected state, and the XPC-8 responds to all inquiries with a disconnected mode (DM) frame and idles (transmit all 1s) between frames. MDISC is set during a valid reset.
2	RECR	**Receiver Ready.** Indicates to the XPC-8 the availability of receive data buffers in system memory. If 0, no receive data buffers are available. If 1, receive data buffers have been allocated and are available. RECR is cleared during a valid reset, if a hard parity error (see Table 8) occurs during a receive channel DMA operation, or if a receiver overrun occurs.
3	ACT/PAS	**Active/Passive.** Specifies the XPC-8 action during link set-up. If 0, the XPC-8 passively awaits link set-up. If 1, the XPC-8 actively pursues link set-up. ACT/PAS is cleared during a valid reset.
4	PWXCH	**Password Exchange.** Specifies whether the XPC-8 should actively pursue a password exchange (PWXCH = 1) or passively await the initiation of a password exchange by a remote DTE (PWXCH = 0). PWXCH is cleared during a valid reset.
5	PWOK1	**Password Verified.** These bits are used by the host CPU to notify the XPC-8 of the results of its received password examination. These bits are cleared during a valid reset and are interpreted with PWXCH (bit 4) as: **Code** (b6 b5 b4) — **Condition** 0 1 0 — Valid password command received 0 1 1 — Valid password response received 1 0 0 — Valid password command was not received 1 0 1 — Valid password response was not received
6	PWOK2	
7	DISCMOD	**Disconnect Mode.** Specifies which of two states the XPC-8 assumes when logically disconnected. If 0, the XPC-8 responds to all inquiries (command frames with their poll bits set) with a DM frame while logically disconnected. This implies that link set-up can be successfully pursued only from the local side of the link. If 1, the XPC-8 responds to all inquiries as specified by the X.25 protocol. In this case, link set-up can be successfully pursued from either side of the link. DISCMOD is set during a valid reset.

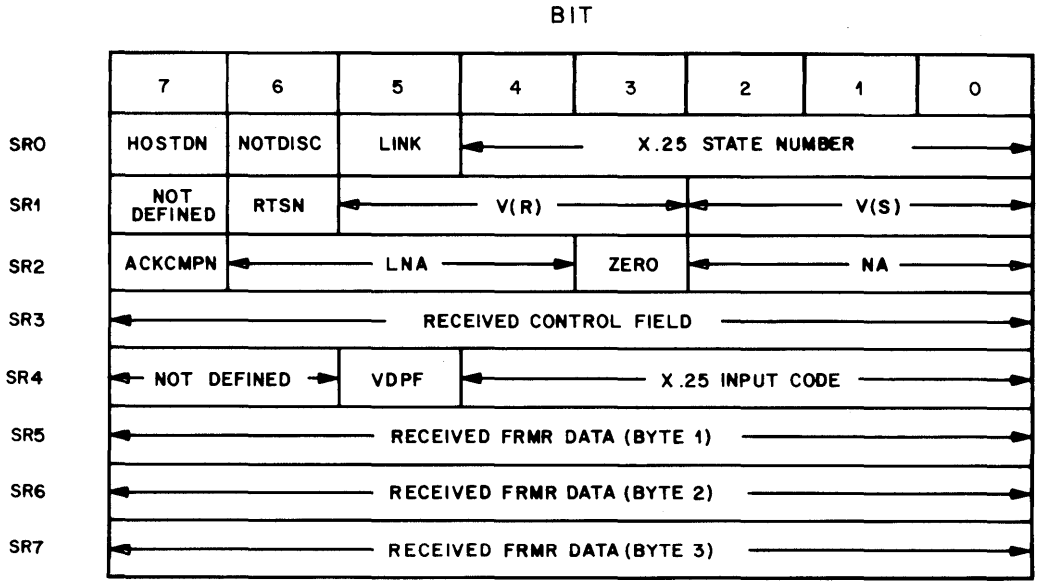


Figure 3. Status Registers

Table 4. Status Registers

Reg(s)	Bit(s)	Symbol	Name/Description
0	0—4	XST	**X.25 State Number.** Specifies the present state of the X.25 protocol (see Table 5).
0	5	LINK	**Link Status.** Indicates whether the XPC-8 has entered the information transfer phase. If 0, the XPC-8 has not entered this phase and information transfer is not permitted. If 1, the XPC-8 is in the information transfer phase (X.25 State ≥ S6).
0	6	NOTDISC	**Not Disconnected.** Indicates whether a logical link exists between two level 2 entities. If 0, the logical link is disconnected. If 1, the logical link is connected and the level 2 entities are communicating (X.25 State ≥ S4).
0	7	HOSTDN	**Host Done (Active Low).** Indicates whether the host CPU has reassigned transmit and receive data buffers in preparation for link reinitialization. If 0, the host has completed all transmit data buffer reassignments. If 1, the host must reassign transmit and receive data buffers before link reinitialization is permitted. This bit is cleared when the CPU writes to status register 0. Bits 0—6 of status register 0 cannot be written, and HOSTDN can only be cleared. It is the act of writing to this register that clears HOSTDN.

Table 4. Status Registers (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
1	0–2	V(S)	**Send State Variable.** Denotes the sequence number of the next in-sequence I frame to be transmitted. V(S) is used to index into the TLOOK table to indicate the TLOOK element that describes the next packet to be transmitted.
1	3–5	V(R)	**Receive State Variable.** Denotes the sequence number of the next in-sequence I frame to be received. V(R) is used to index into the RLOOK table to indicate the RLOOK element that describes the receive data buffer for the next received packet.
1	6	RSTN	**Request to Send (Active Low).** If 0, the XPC-8 is requesting to use the physical link.
1	7	–	**Reserved.** This bit is used for test purposes.
2	0–2	NA	**Next Acknowledge Expected.** Contains the sequence number of the earliest unacknowledged packet. If there are no outstanding packets, NA = V(S).
2	3	–	**Zero.** This bit is not used and is tied low.
2	4–6	LNA	**Last Next Acknowledge Expected.** When NA is updated, the old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC-8.
2	7	ACKCMPN	**Acknowledgments Complete (Active Low).** To prepare for logical link reinitialization, the CPU must reallocate transmit buffers. Before reallocation begins, the CPU should check ACKCMPN to be sure that the interface unit has finished processing all received acknowledgments. If 0, the interface unit has processed all the acknowledgments received from the remote DXE and the CPU can begin transmit buffer reallocation. If 1, received acknowledgments are still being processed.
3	0–7	RECEIVED CONTROL FIELD	**Received Control Field.** Holds the control field of the most recently received error-free frame.
4	0–4	XCT	**X.25 Input Code.** Contains an encoding of what the X.25 protocol considers its most recent input stimulus (see Table 6).
4	5	VDPF	**Valid Poll/Final.** Indicates whether the poll/final bit of the last received error-free frame was a 1 or a 0.
4	6–7	–	**Reserved.** These bits are used for test purposes.
5–7	0–7	FRMR DATA FIELD	**Received FRMR Data Field.** Registers 5, 6, and 7 hold the first, second, and third bytes, respectively, of the data field contained in the received FRMR frame.

Table 5. Status Register 0, Bits 0—4 (XST)						
State Number b4	b3	b2	b1	b0	State	Name
0	0	0	0	0	S0	Super logical disconnect
0	0	0	0	1	S1	Logical disconnect
0	0	0	1	0	S2a	Awaiting XID command
0	0	0	1	1	S2b	Awaiting XID response
0	0	1	0	0	S3	Link set-up
0	0	1	1	1	S4	Frame rejected
0	0	1	0	1	S5	Disconnect request
0	0	1	1	0	S6	Information transfer
0	1	0	0	0	S7	REJ frame sent
0	1	0	0	1	S8	Waiting for acknowledgment
1	0	0	0	1	S9	Station busy
0	1	0	1	0	S10	Remote station busy
0	1	1	1	1	S11	States 9 and 10
1	0	0	0	0	S12	States 8 and 9
0	1	0	1	1	S13	States 8 and 10
1	1	0	1	0	S14	States 8, 9, and 10
1	1	0	1	1	S15	States 7 and 9
0	1	1	0	0	S16	States 7 and 10
0	1	1	0	1	S17	States 7, 9, and 10

Table 6. Status Register 4, Bits 0—4 (XCT)			
Input Code	Description	Input Code	Description
0	Local stop	15	I frame received
1	Local start	16	UA received
2	T1 expired	17	FRMR received
3	T4 expired	18	DM received
4	Unrecognized frame	19	SABM received
5	Valid XID command received	20	Invalid N(R)
6	Station busy	21	Valid XID response
7	I frame available (code seen after reset)	22	T2 expired
8	Busy condition clears	24	Idle link detected for T3
9	Invalid N(S)	25	N2 exceeded
10	Initiate password exchange	26	DISC received
11	Wait for password exchange	28	REJ response received
12	REJ command frame received	29	RR response received
13	RR command frame received	30	RNR response received
14	RNR command frame received		

Table 7. Interrupt Register

Bit	7	6	5	4 0
Field	LSTIN	ZERO	ZERO	INTERRUPT REGISTER

Bit(s)	Name/Description
0—4	**Interrupt Code.** This 5-bit number may take on a value from 0 to 27. Each value indicates a different interrupt condition, as described in Table 8.
5—6	**Zero.** These bits are not used and are tied low.
7	**LSTIN.** A one (1) in this bit position indicates the loss of one or more interrupt codes due to the overflow of the interrupt FIFO. This bit is cleared upon reading the interrupt register.

Table 8. Interrupt Register Codes

Code	Interrupt	Name/Description
0	NULL	Indicates no outstanding interrupt conditions.
1	SABM	An SABM (set asynchronous balanced mode) command frame was received while the XPC-8 was in the information transfer phase.
2	UA	An unnumbered acknowledgement (UA) frame was received while the XPC-8 was in the information transfer phase.
3	DM	**Disconnect Modes.** A disconnected mode (DM) frame was received.
4	FRMRR	**Frame Reject Received.** A frame reject (FRMR) frame was received. The data field of the FRMR is stored in status registers 5—7.
5	DISC	**Disconnect.** A disconnect (DISC) frame was received while the XPC-8 was in the information transfer phase.
6	IDLNK	**Idle Link.** An idle link condition has prevailed for a period in excess of T3.
7	N2EXC	**N2/C2 Counter Exceeded.** If this interrupt occurs during a password exchange, it should be interpreted as a C2 counter exceeded condition. Otherwise, it should be interpreted as an N2 exceeded condition.
8	RF1P	A response frame with its final bit set was received without having transmitted a command frame with its poll bit set.
9	LK01	The XPC-8 has entered the information transfer phase (the logical link has come up).
10	LK10	The XPC-8 has left the information transfer phase (the logical link has gone down).

Table 8. Interrupt Register Codes (Continued)		
Code	**Interrupt**	**Name/Description**
11	XIDR	**XID Received.** An XID frame was received and its data field placed in system memory.
12	NOXIDR	**No XID Received.** An XID command frame was transmitted and an XID response frame was not received for a period of T4.
13	FRMRXW	**Frame Reject Transmitted** (W = 1). A frame reject was transmitted because a frame was received with an invalid control field.
14	FRMRXX	**Frame Reject Transmitted** (X = 1, W = 1). A frame reject was transmitted because a frame was received whose control field is considered invalid because the frame contains an information field that is not permitted, or because the frame is a supervisory or unnumbered frame of incorrect length.
15	FRMRXY	**Frame Reject Transmitted** (Y = 1). A frame reject was transmitted because the information field received exceeded the maximum established capacity set by parameter N1.
16	FRMRXZ	**Frame Reject Transmitted** (Z = 1). A frame reject was transmitted because the control field received contained an invalid N(R).
17	PKR	**Packet Received.** The XPC-8 has received an I frame and stored its information field in system memory.
18	XBA	**Transmitted Block Acknowledged.** The XPC-8 has received and processed acknowledgments for one or more previously transmitted I frames.
19	RCVOVR	**Receiver Overrun.** The receiver FIFO data buffer has overflowed because information field data bytes were being received faster than the interface unit could store them in system memory. The receiver FIFO is six bytes deep.
20	XUNDR	**Transmitter Underrun.** The transmitter FIFO data buffer has underflowed because information field data bytes were being transmitted faster than the interface unit could replenish the FIFO with data read from system memory. If the transmitter FIFO is empty when more data is needed for transmission, the transmitter aborts the frame and generates this interrupt. The XPC-8 attempts to retransmit the information frame if the SEND bit remains set. The host CPU may discontinue retransmission attempts by clearing the SEND bit. The transmitter FIFO is four bytes deep.
21	RLKNRDY	**RLOOK Not Ready.** The XPC-8 has read the RLOOK table element referenced by V(R) and it was not ready (i.e., RECRDY = 0). The XPC-8 goes to a station busy state.
22	CTSLST	**Clear-to-Send Lost.** The clear-to-send ($\overline{\text{CTS}}$) input has gone high while the XPC-8 was in the information transfer phase.

Table 8. Interrupt Register Codes (Continued)		
Code	**Interrupt**	**Name/Description**
23	CARFND	**Carrier Found.** Indicates that the carrier detect ($\overline{CD}$) signal from the physical link has been established (went low).
24	CARLST	**Carrier Lost.** Indicates that the carrier detect ($\overline{CD}$) signal from the physical link has been lost (went high).
25	NOAD	**No Address.** The TLOOK starting address is zero. This is not a valid starting address.
26	HPE	**Hard Parity Error.** The XPC-8 was notified of a parity error on each of two attempts to complete a DMA read or write cycle. The XPC-8 is notified of parity errors through the $\overline{PARV}$ pin. If the error occurred during a transmit channel DMA operation, the SEND bit of the command register is cleared. If the error occurred during a receive channel DMA operation, the RECR bit of the command register is cleared.
27	NULIF	**Null I Frame Received.** An I frame without an information field was received. The XPC-8 treats null I frames as any other I frame except that it generates this interrupt.

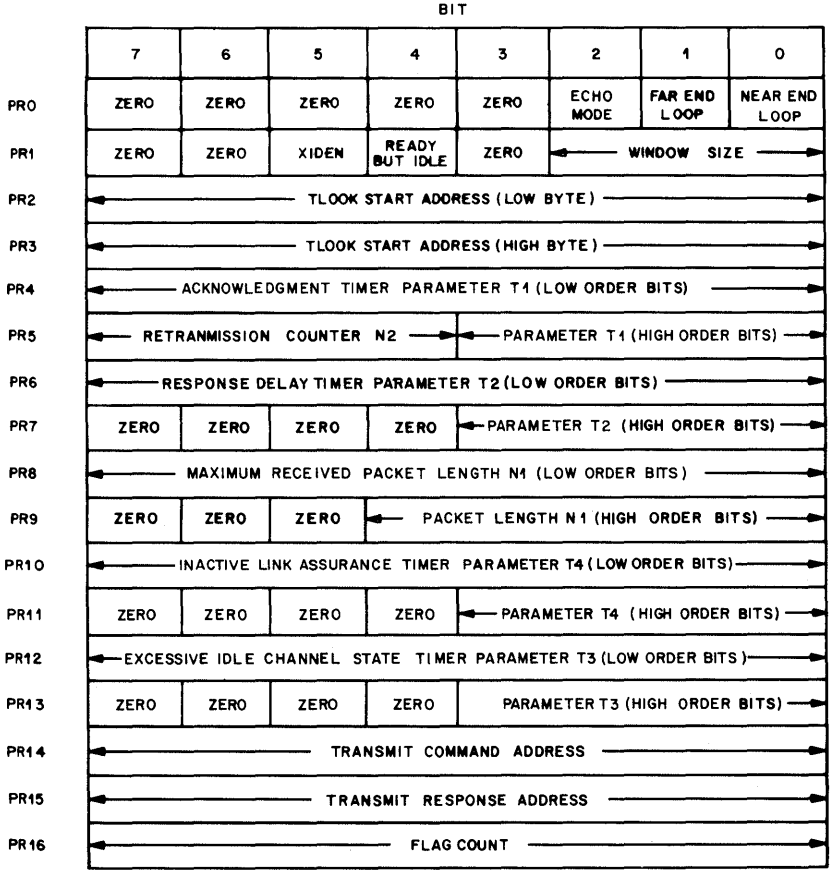


Figure 4. Parameter Registers

Table 9. Parameter Register Definitions

Reg(s)	Bit(s)	Symbol	Name/Description
0	0	NELT	**Near-End Loop Test.** Setting (1) this bit causes the XPC-8 to enter the near-end loopback test mode.
0	1	FELT	**Far-End Loop Test.** Setting (1) this bit causes the XPC-8 to enter the far-end loopback test mode.
0	2	ECHO	**Echo Mode.** Setting (1) this bit causes the XPC-8 to transmit what it receives unaltered (i.e., the RD and TD pins are internally connected).
0	3–7	–	**Reserved.** These bits must be cleared (0).
1	0–2	k	**Window Size.** Maximum allowable number of outstanding I frames. An outstanding I frame should be considered to be any frame which has not been acknowledged by the remote DXE (either DTE or DCE). The window size must not equal zero.
1	3	–	**Reserved.** This bit must be cleared (0).
1	4	RDYIDL	**Ready But Idle.** The bit has meaning only when the logical link is disconnected and MDISC = 0. If RDYIDL is 0, the XPC-8 sends flags between frames. If 1, the XPC-8 idles between frames.
1	5	XIDEN	**XID Enable.** Setting (1) this bit enables the password exchange mechanism.
1	6–7	–	**Reserved.** These bits must be cleared (0).
2–3	0–7	TLOOK START ADDRESS	**TLOOK Table Starting Address.** Indicates the starting address in system memory of the first element in the transmitter look-up TLOOK table. The address must not equal zero.
4	0–7	T1 (Low Byte)	**Acknowledgment Timer Parameter.** T1 is the maximum time that the XPC-8 waits for an acknowledgement. The period of the T1 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T1} = 32{,}768 \times \frac{\text{T1 parameter}}{f_{CKO}}$.
5	0–3	T1 (High Bits)	
5	4–7	N2	**Transmission and Retransmission Counter.** The maximum allowable number of transmissions and retransmissions of a frame without receiving an acceptable response.
6	0–7	T2 (Low Byte)	**Response Timer Parameter.** T2 is the maximum time that the XPC-8 waits before responding to an inquiry from the remote DXE. The period of the T2 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T2} = 32{,}768 \times \frac{\text{T2 parameter}}{f_{CKO}}$.
7	0–3	T2 (High Bits)	

Table 9. Parameter Register Definitions (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
7	4—7	—	**Reserved.** These bits must be cleared (0).
8	0—7	N1 (Low Byte)	**Maximum Received Packet Length.** The maximum number of bytes that the receiver accepts in the information field of a frame before rejecting the received frame. Note that the XPC-8 parameter N1 specifies **bytes**, not bits.
9	0—4	N1 (High Bits)	
9	5—7	—	**Reserved.** These bits must be cleared (0).
10	0—7	T4 (Low Byte)	**Inactive Link Assurance Timer Parameter.** During intervals when the T1 timing function is not performed (i.e., there are no outstanding unacknowledged I-frames or P-bit frames), an appropriate S-format command frame with the P-bit set is transmitted every T4 time units to verify the status of the remote DXE. The period of the T4 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T4} = 32{,}768 \times \frac{\text{T4 parameter}}{\text{fCKO}}$.
11	0—3	T4 (High Bits)	
11	4—7	—	**Reserved.** These bits should be cleared to zero.
12	0—7	T3 (Low Byte)	**Excessive Idle Channel State Timer Parameter.** T3 specifies the amount of time that the XPC-8 accepts the reception of an idle condition before taking alternate actions. The period of the T3 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T3} = 32{,}768 \times \frac{\text{T3 parameter}}{\text{fCKO}}$.
13	0—3	T3 (High Bits)	
13	4—7	—	**Reserved.** These bits must be cleared (0).
14	0—7	TCA	**Transmit Command Address.** Address field of the command frames transmitted by the XPC-8 (the station address of far end of link).
15	0—7	TRA	**Transmit Response Address.** Address field of the response frames transmitted by the XPC-8 (the station address of this station).
16	0—7	FLGCNT	**Flag Count.** Specifies the minimum number of extra flags between frames. The value of flag count is cleared (0) on reset. A value of zero causes the minimum number of flags between frames to default to one. FLGCNT is a special feature of the XPC-8 and is not part of the X.25 protocol.

Bus and I/O Logic

Bits A0—A5 of the address bus are bidirectional and are used to access the 27 internal registers. When the chip is selected, R/$\overline{W}$, $\overline{WE}$, $\overline{DSRE}$, and address lines A0—A5 become inputs. $\overline{READY}$ becomes an output.

DMA operations are controlled by the interface unit. The XPC-8 uses DMA to access system memory to read and write TLOOK table elements, RLOOK table elements, and data fields of information frames. A daisy-chain DMA priority scheme may be implemented for multiple XPC-8 applications.

The data bus can be configured to be either Motorola or Intel compatible. Bus mode selection is handled by providing one of two reset sequences.

XPC-8 Master Reset

When the master reset ($\overline{MR}$) is asserted (low), all outputs are put into the high-impedance state and the parameter registers are cleared (0) except for the TLOOK starting address – parameter registers 2 and 3. The command register is set to 82H (DISCMOD = 1, MDISC = 1, all other bits are cleared (0)).

In addition, the master reset is used to choose between the Intel and Motorola bus modes. A reset pulse must be held low for at least six cycles of CKO to be considered a valid reset request. Glitch protection circuitry guarantees that glitches of less than one CLK period are ignored. If a single valid reset request is provided, the XPC-8 bus will be configured for the Motorola bus standard. If a second valid reset request is provided within thirty cycles of CKO, the XPC-8 switches to the Intel bus standard. $\overline{MR}$ must be held high for at least six cycles of CKO after a reset pulse before the XPC-8 can recognize a second reset pulse. Any reset pulses occurring after the thirty cycles of CKO are interpreted as a new reset sequence (see Figure 11).

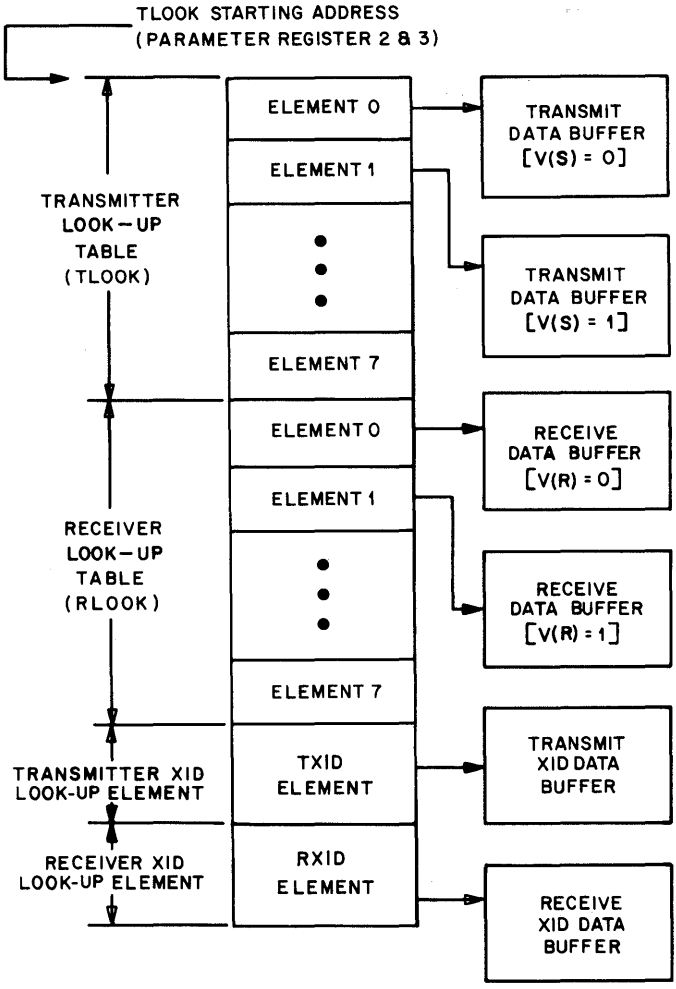
Transmitter and Receiver Look-Up Tables

System memory contains data buffers that store transmit and receive data. The pointers used to access these buffers are also stored in system memory. The location of data to be transmitted is described by pointers in the transmitter look-up table (TLOOK) elements and the location of data to be received is described by pointers in the receiver look-up table (RLOOK) elements. Figure 5 is a diagram of the system memory interface.

The TLOOK table is a block of eight 8-byte elements in system memory starting at the TLOOK STARTING ADDRESS (parameter registers 2 and 3). Each element in the TLOOK table describes a buffer corresponding to one packet of data to be transmitted by the XPC-8. The TLOOK list of elements is used as a modulo-8 circular queue. Figure 6 and Table 10 present the bit assignments and descriptions for the TLOOK elements.

The RLOOK table is a block of eight 8-byte elements in system memory immediately following the TLOOK table. Each element in the RLOOK table describes a buffer corresponding to one packet to be received by the XPC-8. The RLOOK list of elements is also used as a circular queue. Figure 7 and Table 11 present the bit assignments and descriptions for the RLOOK elements.

In addition to the two look-up tables described above, there are two single-element look-up tables (TXID and RXID) that are used only during password exchange. They are located in system memory immediately following the RLOOK elements. The TXID and RXID look-up tables are used to describe the transmit password and receive password data buffers, respectively. Their format is identical to that of the TLOOK and RLOOK elements.



Note: Each element has 8 bytes of data.

Figure 5. XPC-8/CPU System Memory Interface

Table 10. TLOOK Element Definitions

Reg(s)	Bit(s)	Symbol	Name/Description
1	0	BRDY	**Buffer Ready.** Setting (1) this bit indicates to the XPC-8 that data associated with this element is ready to be transmitted. BRDY should be the last bit of the TLOOK element to be set by the CPU after preparing a buffer. The SEND bit of the command register should then be set (1) to command the XPC-8 to begin transmitting packets. The XPC-8 clears BRDY and sets NACK after all of the data associated with this element has been accessed by DMA and loaded into the transmitter FIFO.
1	1–5	—	**Reserved.** These bits should be cleared (0).

Table 10. TLOOK Element Definitions (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
1	6	NACK	**Not Acknowledged.** The XPC-8 sets NACK and clears BRDY after all the data associated with this look-up element has been accessed and loaded into the transmitter FIFO. The XPC-8 clears this bit when the frame associated with this element has been acknowledged.
1	7	ACK	**Acknowledged.** The XPC-8 sets ACK and clears NACK when an acknowledgment is received for the packet associated with this look-up element. An XBA interrupt is generated to notify the CPU of one or more acknowledgments.
2	0–7	TCNT (Low Byte)	**Transmit Count.** The number of bytes in a transmit data packet is specified by this 16-bit number. The X.25 Protocol Standard limits the number of bytes in an information field to 4K + 4 (including the packet header) and, therefore, bits 6 and 7 of byte 3 should always be cleared (0).
3	0–7	TCNT (High Byte)	
4	0–7	TSA (Low Byte)	**Transmit Start Address.** This 16-bit number is the location in system memory of the first byte of transmit data associated with this TLOOK element.
5	0–7	TSA (High Byte)	
6–8	0–7	–	**Spare.** Not used.

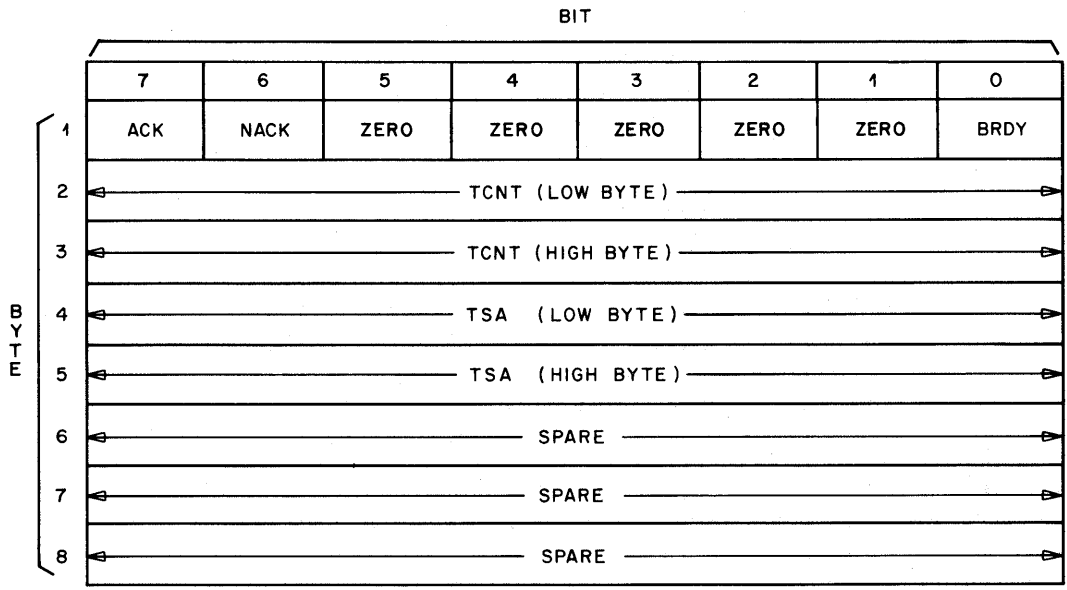


Figure 6. TLOOK Element

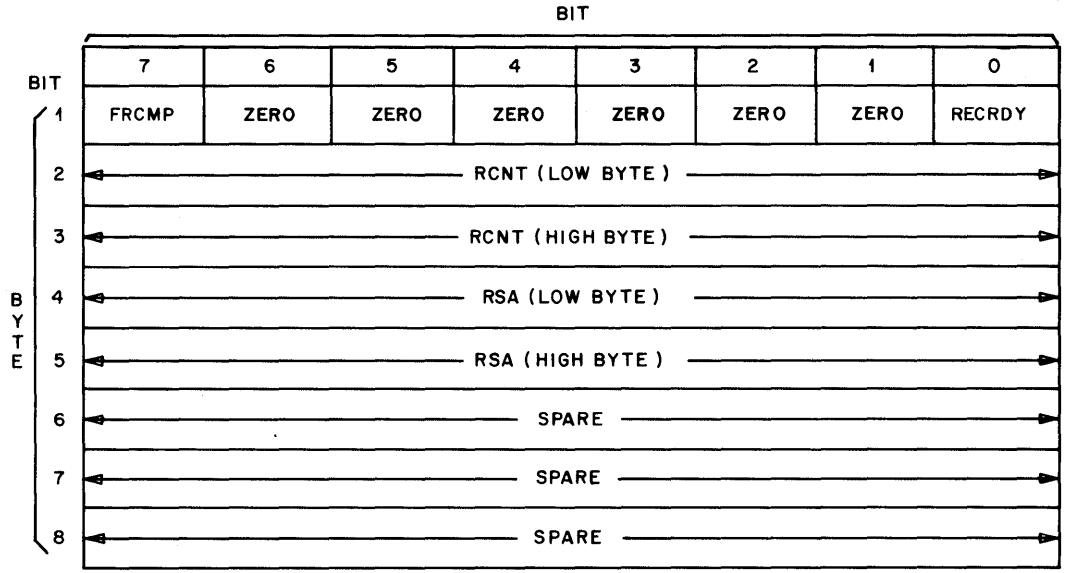


Figure 7. RLOOK Element

Table 11. RLOOK Element Definitions

Reg(s)	Bit(s)	Symbol	Name/Description
1	0	RECRDY	**Receiver Ready.** Setting (1) this bit indicates to the XPC-8 that the data buffer associated with this element is ready to receive data. The receive start address field of the RLOOK element should be specified before the CPU sets the RECRDY bit. After the XPC-8 receives a valid packet and stores the information field in the buffer associated with the look-up element, it clears RECRDY and sets FRCMP.
1	1–6	–	**Reserved.** These bits should be cleared (0).
1	7	FRCMP	**Frame Complete.** When a valid packet is received, the XPC-8 writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is used to notify the CPU of the received packet.
2	0–7	RCNT (Low Byte)	**Receiver Count.** This 16-bit number specifies how many bytes of system memory have been filled by the received packet. The XPC-8 writes this location after a valid information frame has been received and written to system memory without error.
3	0–7	RCNT (High Byte)	
4	0–7	RSA (Low Byte)	**Receive Start Address.** This 16-bit number specifies the address in system memory of the first byte of received data in the packet. This address is written only by the CPU.
5	0–7	RSA (High Byte)	
6–8	0–7	–	**Spare.** Not used.

DMA Operation

Direct memory access (DMA) on the XPC-8 is used to read and write data fields of I frames, data fields of XID frames, and the TLOOK and RLOOK tables in system memory. To initiate a DMA cycle, the XPC-8 requests the use of the data bus by forcing $\overline{\text{DREQ}}$ low. The host CPU signifies that the bus is available for use by the XPC-8 by forcing $\overline{\text{DACK}}$ low. This allows $\overline{\text{DSRE}}$, $\overline{\text{WE}}$, R/$\overline{\text{W}}$, $\overline{\text{AS}}$, and A0—A15 to become outputs.

Once the XPC-8 has control of the system bus, it expects to have use of the bus until it finishes its DMA operations. The XPC-8 holds the system bus for a maximum of 5 read or write cycles.

Slow memory handshaking is provided through the $\overline{\text{READY}}$ input. A read or a write continues until $\overline{\text{READY}}$ goes low. A DMA write cycle must not extend more than 100 μs.

Parity checks are not performed on-chip. The results of any off-chip parity checking schemes should be supplied through $\overline{\text{PARV}}$. $\overline{\text{PARV}}$ is sampled on the falling edge of the CKO cycle following the detection of valid $\overline{\text{READY}}$. If $\overline{\text{PARV}}$ is sampled low, parity is assumed to be valid. If $\overline{\text{PARV}}$ is high, the XPC-8 makes a second attempt to complete the read or write operation. If the second attempt also fails, a hard parity error interrupt is generated and DMA operations halts. $\overline{\text{PARV}}$ should be tied low if parity is not being checked.

A priority DMA scheme may be implemented in a daisy-chain fashion for multiple XPC-8 applications with no additional hardware. The $\overline{\text{DREQ}}$ pin of the lowest priority XPC-8 is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC-8. The $\overline{\text{DREQ}}$ pin for the highest priority XPC-8 is tied to the $\overline{\text{BUSREQUEST}}$ input of the CPU. The $\overline{\text{BUSGRANT}}$ output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC-8. The $\overline{\text{LPDACK}}$ of the highest priority XPC-8 is tied to $\overline{\text{DACK}}$ of the next highest priority XPC-8 and this continues until the lowest priority XPC-8 is reached. The $\overline{\text{LPDREQ}}$ of the lowest priority XPC-8 must be tied high (see Figure 8).

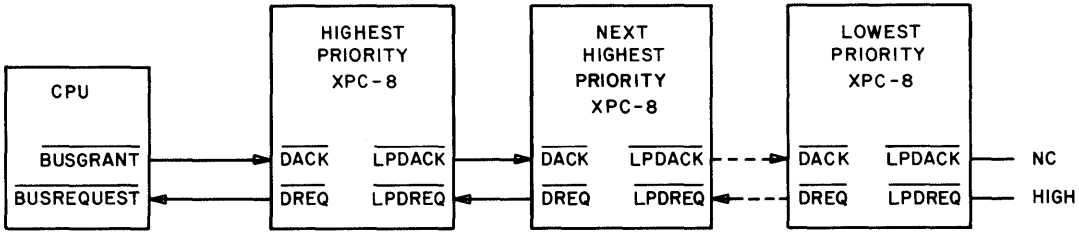


Figure 8. DMA Priority Scheme Interconnection

Test Modes

The XPC-8 has four test modes: near-end loopback, far-end loopback, echo, and output 3-state.

The near-end loopback test permits the XPC-8 to talk to itself. The transmitter output and receiver input are internally connected while in this mode of operation. The receiver automatically interchanges the command and response addresses to allow the protocol to function properly.

The far-end loopback test is used to check the near-end XPC-8 and the data link. The local XPC-8 is placed in far-end loopback test mode, while the remote XPC-8 is placed in echo mode. The receiver in the local XPC-8 interchanges the command and response addresses. Data arriving at the remote XPC-8, which is in the echo mode, is internally routed without CPU or XPC-8 intervention to the transmitter data output.

Output buffers are 3-stated whenever $\overline{MR}$ is forced low. This feature should be used during board test/debug.

CHARACTERISTICS

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter		Symbol	Min	Max	Unit	Test Conditions
Input Voltage	Low	V_{IL}	–	0.8	V	–
	High	V_{IH}	2.2*	–	V	–
Output Voltage	Low	V_{OL}	–	0.4	V	I_{OL} = 2.2 mA
	High	V_{OH}	2.4	–	V	I_{OH} = −400 μA
Power Supply Current		I_{DD}	–	460	mA	–
Output Off Current	Low	I_{OZL}	–	−10	μA	V_{OL} = 200 mV
	High	I_{OZH}	–	10	μA	V_{OH} = 5.25 V
Power Dissipation		PD	–	2.2	W	V_{DD} = 5.0 V

*MOS input level

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... 0 to 85 °C
Power Dissipation (PD) ..... 2.5 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Table 12. DMA Timing

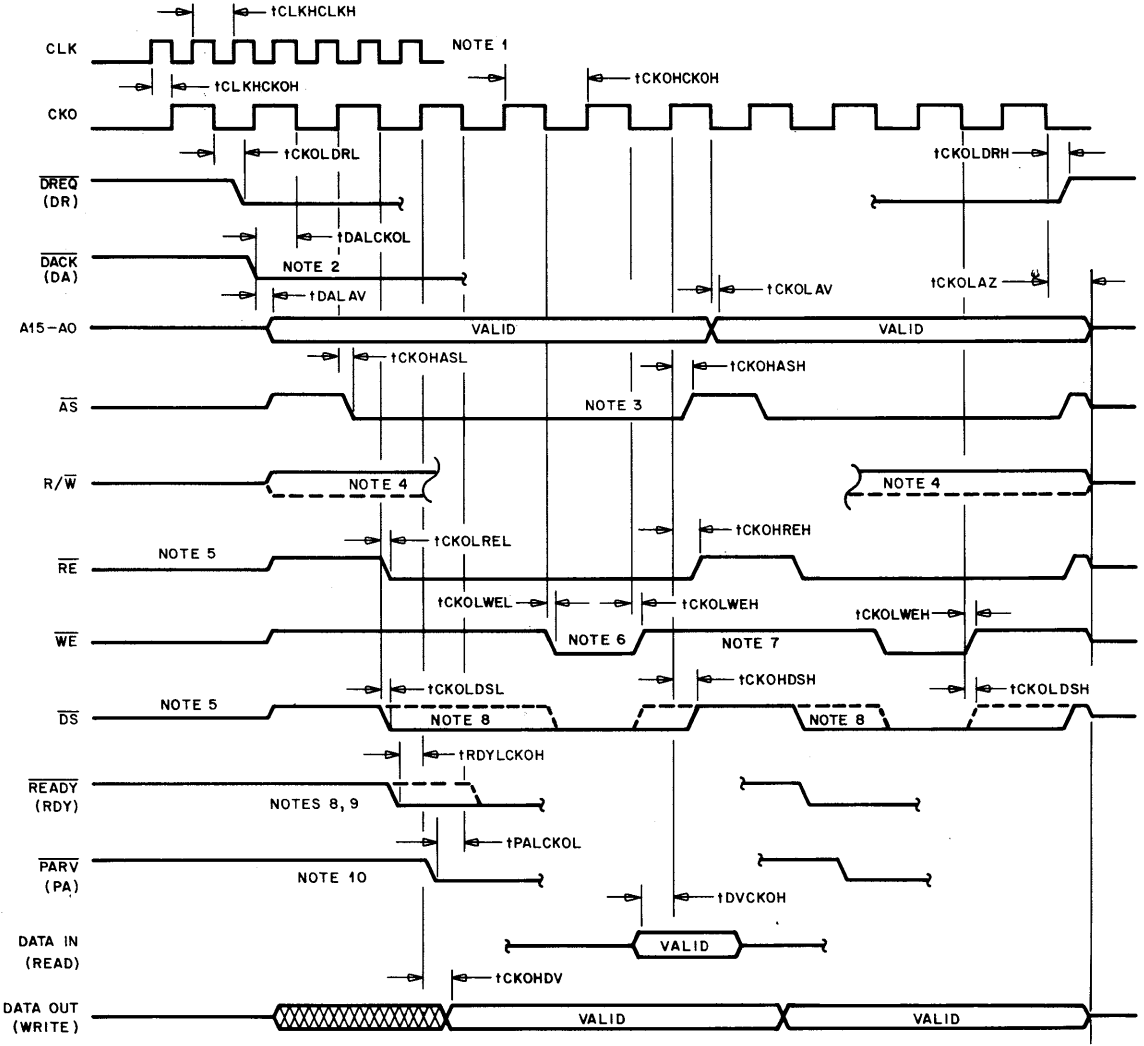
Symbol	Description	Min	Max	Unit
tCKOHASH	$\overline{AS}$ Release Offset	–	125	ns
tCKOHASL	$\overline{AS}$ Offset	–	102	ns
tCKOLAV	Address Settle Time	–	92	ns
tCKOLAZ	Address Disable Offset	–	160	ns
tCKOHCKOH	CKO Period	400	8000	ns
tCKOLDRH	$\overline{DREQ}$ Release Offset	–	95	ns
tCKOLDRL	$\overline{DREQ}$ Offset	–	140	ns
tCKOHDV	Data Valid Offset	–	200	ns
tCKOHREH	$\overline{RE}$ Release Offset	–	160	ns
tCKOLDSH	$\overline{DS}$ Release Offset (Write)	–	100	ns
tCKOHDSH	$\overline{DS}$ Release Offset (Read)	–	160	ns
tCKOLDSL	$\overline{DS}$ Low Offset (Motorola, Read)	–	44	ns
tCKOLDSL	$\overline{DS}$ Low Offset (Motorola, Write)	–	44	ns
tCKOLREL	$\overline{RE}$ Low Offset (Intel, Read)	–	44	ns
tCKOLWEH	$\overline{WE}$ Release Offset	–	70	ns
tCKOLWEL	$\overline{WE}$ Low Offset (Intel, Write)	–	34	ns
tCLKHCKOH	Clock Offset	–	130	ns
tCLKHCLKH	CLK Period	200	4000	ns
tDALAV	Address Enable Offset	–	135	ns
tDALCKOL	$\overline{DACK}$ Set-Up Time	230	–	ns
tDVCKOH	Data Set-Up Time	170	–	ns
tPALCKOL	$\overline{PARV}$ Set-Up Time	180	–	ns
tRDYLCKOH	$\overline{READY}$ Set-Up Time	145	–	ns

Table 13. CPU Read and Write Timing

Symbol	Description	Min	Max	Unit
tAVCSL	Address Valid Before $\overline{CS}$ Low (Address Set-Up)	0	–	ns
tDSLDV	$\overline{DS}$ Low to Data Valid (Access Time)	–	150	ns
tRELDV	$\overline{RE}$ Low to Data Valid (Access Time)	–	150	ns
tDSHDZ	$\overline{DS}$ High to Data 3-State	–	190	ns
tREHDZ	$\overline{RE}$ High to Data 3-State	–	190	ns
tCKOHRDYH	Ready Release Offset (Read)	–	250	ns
tCKOHRDYH	Ready Release Offset (Write)	–	345	ns
tCKOHRDYL	Ready Active Offset (Read)	–	160	ns
tCKOHRDYL	Ready Active Offset (Write)	–	160	ns
tCSLCKOL	$\overline{CS}$ Set-Up Time	390	–	ns
tDSHRWV	$\overline{DS}$ Release to R/$\overline{W}$ Change	50	–	ns
tRWVDSL	R/$\overline{W}$ Release to $\overline{DS}$ Change	90	–	ns
tDSHCKOL	$\overline{DS}$ Release Set-Up Time	390	–	ns
tDSLCKOL	$\overline{DS}$ Set-Up Time	212	–	ns
tDSHAX	$\overline{DS}$ High to Address Change	0	–	ns
tAVDSL	Address Valid Before $\overline{DS}$ Low (Address Set-Up)	0	–	ns
tDVCKOH	Data Set-Up Time	0	–	ns
tDXCKOH	Data Hold Time	155	–	ns
tREHCKOL	$\overline{RE}$ Release Set-Up Time	390	–	ns
tRELCKOL	$\overline{RE}$ Set-Up Time	212	–	ns
tREHAX	$\overline{RE}$ High to Address Change	0	–	ns
tAVREL	Address Valid Before $\overline{RE}$ Low (Address Set-Up)	0	–	ns
tWEHCKOL	$\overline{WE}$ Release Set-Up Time	280	–	ns
tWELCKOL	$\overline{WE}$ Set-Up Time	250	–	ns
tWEHAX	$\overline{WE}$ High to Address Change	0	–	ns
tAVWEL	Address Valid Before $\overline{WE}$ Low (Address Set-Up)	0	–	ns

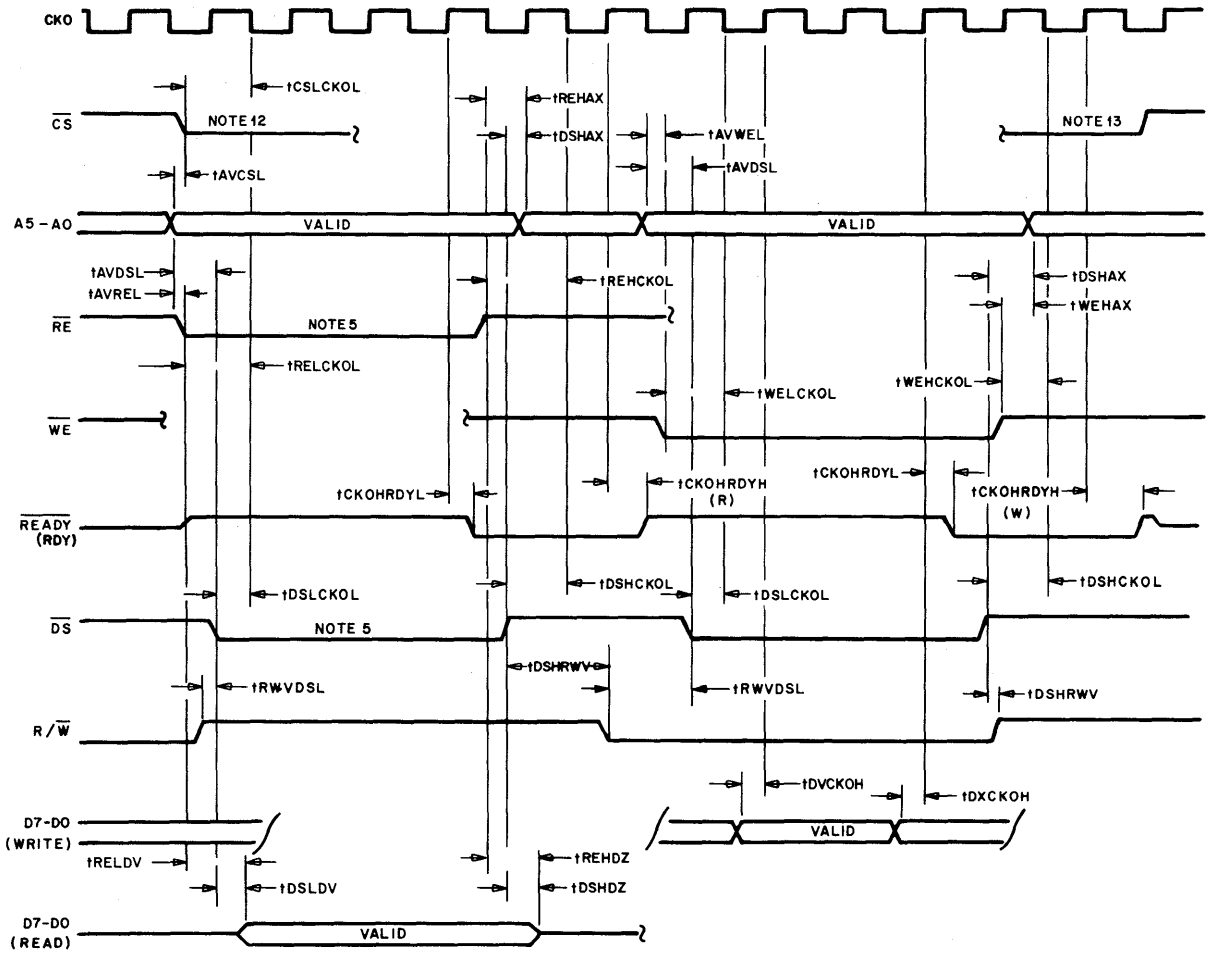
Table 14. Reset Timing

Symbol	Description	Min	Max	Unit
tMRHMRH	Time Allowed for Switching to Intel Bus Mode (Intel)	–	30tCKOHCKOH	–
tMRHMRL	Time Between Reset Pulses (Intel)	6tCKOHCKOH	–	–
tMRLMRH	Valid Reset Time (Motorola and Intel)	6tCKOHCKOH	–	–
tPU	Power-Up Delay Time (Motorola and Intel)	40tCKOHCKOH	–	–



Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 9. DMA Timing Diagram

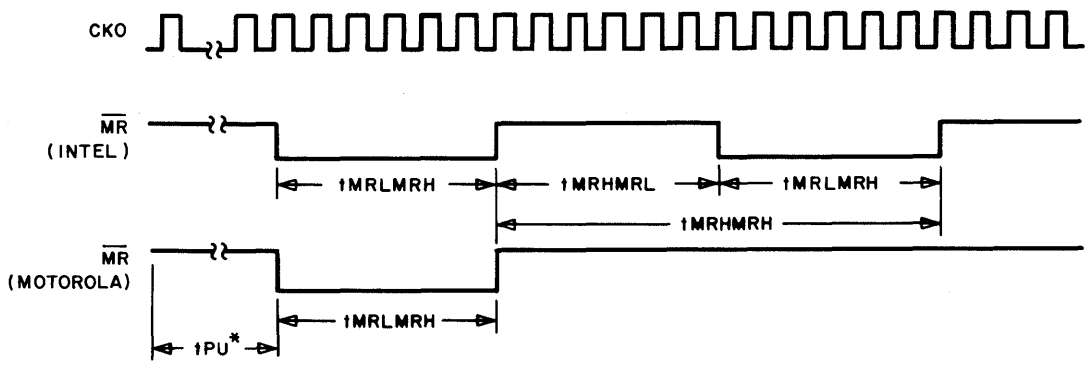


Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 10. CPU Read and Write Cycles

Timing Diagram Notes for Figures 9 and 10

1. CLK must have a duty cycle between 45% and 55%.
2. $\overline{\text{DACK}}$ is sampled on every falling edge of CKO until it tests low.
3. Read or write cycles may extend for one extra CKO cycle to allow for internal synchronization.
4. R/$\overline{\text{W}}$ is valid by the first falling edge of $\overline{\text{AS}}$. Dotted line is for write cycle only. Entire DMA cycle is for either a read or a write.
5. $\overline{\text{DS}}$ and $\overline{\text{RE}}$ are multiplexed on the same pin. $\overline{\text{RE}}$ is selected for the Intel bus configuration. $\overline{\text{DS}}$ is selected for the Motorola bus configuration.
6. The write cycle must not be extended (using $\overline{\text{READY}}$) for more than 100 μs.
7. If a $\overline{\text{PARV}}$ error occurs, the trailing edge of $\overline{\text{WE}}$ is concurrent with the trailing edge of $\overline{\text{AS}}$.
8. Dotted line is for write only.
9. $\overline{\text{READY}}$ is sampled on every rising edge of CKO until it tests low.
10. $\overline{\text{PARV}}$ is sampled on the falling edge of CKO following the detection of a valid $\overline{\text{READY}}$.
11. During TLOOK and RLOOK element reads, the read cycles are extended an additional two CKO cycles.
12. Due to internal synchronization, there may be an extra CKO cycle inserted before the falling edge of $\overline{\text{READY}}$.
13. Forcing $\overline{\text{CS}}$ high while executing a read or write cycle ends that cycle.



*Time required from power-up to the first reset

Figure 11. Motorola and Intel Reset Sequences

The information contained herein is preliminary and subject to change.

FEATURES

- 24-bit address bus to address a 16 Mbyte address space
- Dual-channel DMA with standard interface including DMA request, DMA acknowledge, DMA read, and DMA write
- Independently programmable T1 and T4 timers
- Programmable retransmission counter
- Transmit and receive buffers accessed indirectly through a lookup table
- Programmable modulo 8 or 128 frame sequence numbering
- Programmable window size (transmit and receive)
- Selectable 16-bit (CRC-CCITT) or 32-bit polynomial for frame checking sequence (FCS)
- Wait-state generator (on DMA side) for slow memory
- Programmable interframe flag fill
- Error detection and automatic recovery via packet retransmission
- Link initialization and supervision
- Independently programmable transmit and receive window size
- Password exchange mechanism for dial-up operation
- Programmable retransmission counter
- Programmable X.25 or X.75 operation
- Supports 8- or 16-bit data buses
- Intel, Motorola, or *WE* 32100 Microprocessor DMA interface (data bus)
- Sixteen programmable event counters with optional interrupt capability
- Daisy-chain DMA structure for priority-controlled CPU interfaces
- Two independent test modes (far-end loopback and near-end loopback) to verify the XPC and its link
- Optional parity generation and checking across data bus interface on all DMA operations
- Six bidirectional address leads for accessing 51 internal XPC registers
- 2 MHz clock
- Single 5 V supply

DESCRIPTION

The T7102 X.25/X.75 Protocol Controller (XPC) integrated circuit is an X.25/X.75 level 2 protocol controller. It is a single-chip LSI device available in a 70-pin pin grid array package and is fabricated using N-channel silicon gate MOS technology. The T7102 XPC implements an augmented X.25 level 2 data communications standard for packet switching. It satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. This device also implements X.75 level 2 protocol, used in internetwork applications. The protocol controller is bit-oriented with a maximum transmit and receive speed of 333 kb/s. A set of programmable registers controls and records vital events during data transmission.

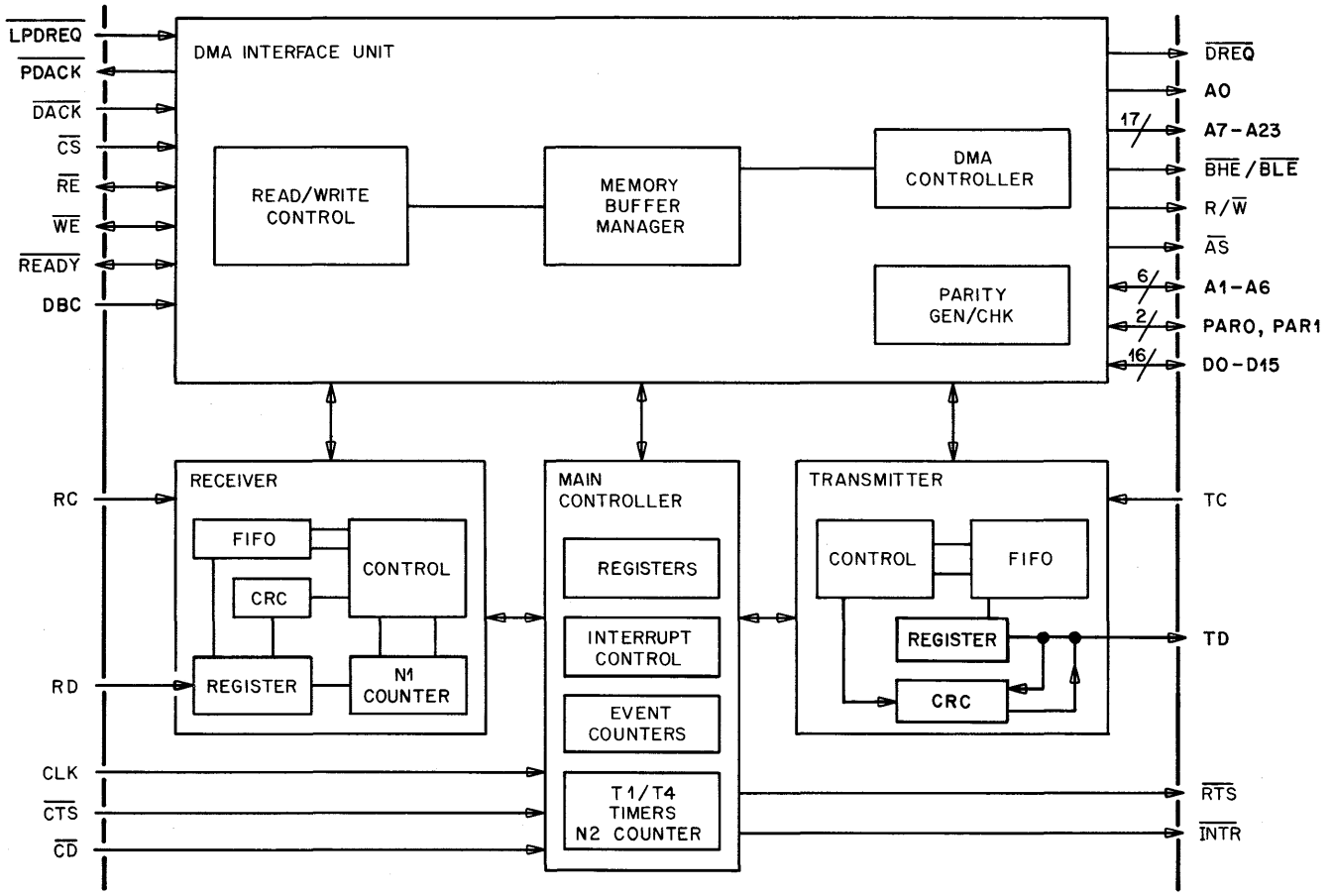
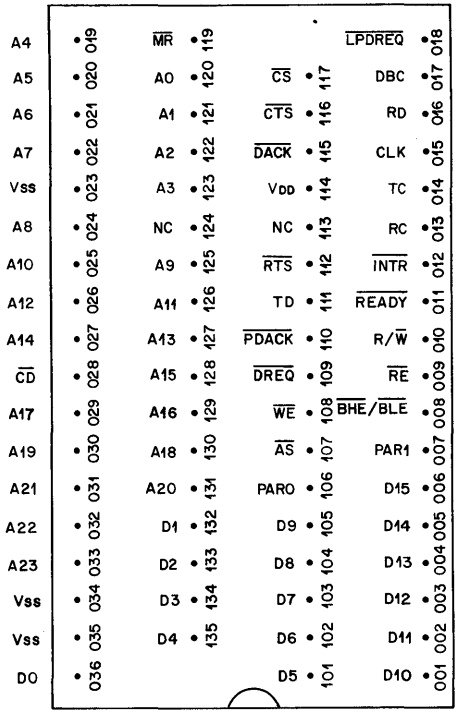


Figure 1. T7102 X.25/X.75 Protocol Controller (XPC) Block Diagram

USER INFORMATION

Pin Descriptions



Sym	Pin	Sym	Pin	Sym	Pin
A0	120	A23	33	D15	6
A1	121	$\overline{AS}$	107	$\overline{DACK}$	115
A2	122	$\overline{BHE}$/	8	DBC	17
A3	123	$\overline{BLE}$		$\overline{DREQ}$	109
A4	19	$\overline{CD}$	28	$\overline{INTR}$	12
A5	20	CLK	15	$\overline{LPDREQ}$	18
A6	21	$\overline{CTS}$	116	$\overline{MR}$	119
A7	22	$\overline{CS}$	117	PAR0	106
A8	24	D0	36	PAR1	7
A9	125	D1	132	$\overline{PDACK}$	110
A10	25	D2	133	RC	13
A11	126	D3	134	RD	16
A12	26	D4	135	$\overline{RE}$	9
A13	127	D5	101	$\overline{READY}$	11
A14	27	D6	102	$\overline{RTS}$	112
A15	128	D7	103	R/$\overline{W}$	10
A16	129	D8	104	TC	14
A17	29	D9	105	TD	111
A18	130	D10	1	VDD	114
A19	30	D11	2	VSS	23,34,
A20	131	D12	3		35
A21	31	D13	4	$\overline{WE}$	108
A22	32	D14	5		

Figure 2. T7102 Pin Grid Array (PGA) Package Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7102 PGA Package Pin Descriptions

Pin	Symbol	Type	Name/Function
1	D10	I/O*	**Data Bus Bit 10.** Part of 16-bit data bus. If DBC (pin 17) is high, full 16-bit bus is used for operation. If DBC is low, lower 8 bits (pins 36, 132—135, and 101—103) are used for all operations.
2	D11		**Data Bus Bit 11.**
3	D12		**Data Bus Bit 12.**
4	D13		**Data Bus Bit 13.**
5	D14		**Data Bus Bit 14.**
6	D15		**Data Bus Bit 15.**
7	PAR1	I/O*	**Parity on High Data Byte.** Parity generation and checking of high byte of data bus. Valid only during DMA operations.

*Indicates 3-State condition.

Table 1. T7102 PGA Package Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
8	$\overline{BHE}/\overline{BLE}$	O*	**Byte High Enable (Active Low).** The XPC uses this line to control access to the high data byte when it has a 16-bit data bus. Access is to low byte in Motorola configuration (see Table 18).
9	$\overline{RE}$	I/O*	**Read Enable (Active Low).** Input during CPU access of XPC registers. Output during DMA read cycles.
10	R/$\overline{W}$	O*	**Read or Write (Active Low).** If 0, XPC wants to write to main memory. If 1, XPC wants to read from main memory. Not used during internal XPC register read/write operations.
11	$\overline{READY}$	I/O*	**Ready (Active Low).** This signal is used as an input during DMA read and write cycles to allow slow memory to be accessed. During DMA operations, $\overline{RE}$ and $\overline{WE}$ (pins 9 and 108) remain active low as long as $\overline{READY}$ is held high. During CPU read/write operations of internal XPC registers, $\overline{READY}$ line is an output. It goes low to signal the CPU that operation is complete.
12	$\overline{INTR}$	O	**Interrupt Request (Active Low).** This indicates that the XPC is requesting service. This returns high when CPU reads the interrupt register.
13	RC	I	**Receive Clock.** 1x clock input.
14	TC	I	**Transmit Clock.** 1x clock input.
15	CLK	I	**Clock.** This controls internal sequencing of the chip. The clock must be a square wave with a minimum frequency of 250 kHz and a maximum frequency of 2 MHz. ($f_{CLK} \geq 6f_{RC}$ and $f_{CLK} \geq 6f_{TC}$).
16	RD	I	**Receive Data.** Serial data input line.
17	DBC	I	**Data Bus Configuration.** This pin must be wired to either V_{SS} or V_{DD} to configure the XPC data bus for either 8-bit or 16-bit operation. (V_{SS} = 8 bit; V_{DD} = 16 bit).
18	$\overline{LPDREQ}$	I	**Low-Priority DMA Request (Active Low).** This pin is used to daisy-chain DMA requests in systems without a bus arbiter that uses more than one XPC. Tie high on lowest priority XPC in the daisy chain.
19	A4	I/O*	**Address Bus Bit 4.** Part of 24-bit address bus. When $\overline{CS}$ (pin 117)
20	A5	I/O*	**Address Bus Bit 5.** is asserted, A1—A6 (pins 121—123 and 19—21)
21	A6	I/O*	**Address Bus Bit 6.** are used in input mode to address XPC
22	A7	O*	**Address Bus Bit 7.** internal registers. Otherwise entire bus is used to address system memory.
23	V_{SS}	O	**Ground.**
24	A8		**Address Bus Bit 8.**
25	A10	O*	**Address Bus Bit 10.** Part of 24-bit address bus.
26	A12		**Address Bus Bit 12.** (See description of pins 19—22).
27	A14		**Address Bus Bit 14.**
28	$\overline{CD}$	I	**Carrier Detect (Active Low).** $\overline{CD}$ generates two interrupts to notify the host of level 1 activity. No further processing is done by the XPC.

*Indicates 3-state condition

Table 1. T7102 PGA Package Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
29	A17		**Address Bus Bit 17.**
30	A19	O*	**Address Bus Bit 19.** Part of 24-bit address bus.
31	A21		**Address Bus Bit 21.** (See description of pins 19—22).
32	A22		**Address Bus Bit 22.**
33	A23		**Address Bus Bit 23.**
34	VSS	—	**Ground.**
35	VSS	—	**Ground.**
36	D0		**Data Bus Bit 0.**
101	D5		**Data Bus Bit 5.**
102	D6	I/O*	**Data Bus Bit 6.** Part of 16-bit data bus.
103	D7		**Data Bus Bit 7.** (See description of pins 1—6).
104	D8		**Data Bus Bit 8.**
105	D9		**Data Bus Bit 9.**
106	PAR0	I/O*	**Parity on Low Data Byte.** Parity generation and checking of low byte of data bus. Valid only during DMA operations.
107	$\overline{AS}$	O*	**Address Strobe (Active Low).** The XPC uses this signal during DMA operations to indicate that it has placed a valid address on address bus.
108	$\overline{WE}$	I/O*	**Write Enable (Active Low).** Input during CPU access of XPC registers. Output during DMA write cycles.
109	$\overline{DREQ}$	O	**DMA Request (Active Low).** The XPC uses this line to tell CPU it needs address and data bus for DMA cycles.
110	$\overline{PDACK}$	O	**Propagated DMA Acknowledge (Active Low).** This pin is used to daisy-chain acknowledgements in systems using more than one XPC. $\overline{PDACK}$ output of one XPC connects to $\overline{DACK}$ input of the next lower priority XPC.
111	TD	O	**Transmit Data.** XPC serial data output line.
112	$\overline{RTS}$	O	**Request to Send (Active Low).** When asserted this signal indicates to level 1 that the XPC is ready to transmit either data or flags over link. $\overline{RTS}$ remains low while link is up.
113	NC	—	**No Connection.**
114	VDD	—	**5 V Supply.**
115	$\overline{DACK}$	I	**DMA Acknowledge (Active Low).** When this signal is low, CPU indicates that the XPC has been granted system buses and all floating outputs of the XPC become TTL drivers. $\overline{DACK}$ must remain low until $\overline{DREQ}$ (pin 19) is removed.
116	$\overline{CTS}$	I	**Clear to Send (Active Low).** Level 1 interface notifies the XPC that the data set is ready to send by setting this line active low. Link cannot come up until $\overline{CTS}$ is asserted. $\overline{CTS}$ must remain asserted when link is up.
117	$\overline{CS}$	I	**Chip Select (Active Low).** Must be asserted to allow access to internal registers of the XPC. When asserted, $\overline{RE}$, $\overline{WE}$, and six bidirectional address leads become inputs, and $\overline{READY}$ becomes an output.

*Indicates 3-state condition.

Table 1. T7102 PGA Package Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
119	$\overline{MR}$	I	**Master Reset (Active Low).** When this line is asserted, all command, status, and parameter registers are cleared (0) except for the mandatory disconnect (MDISC) and the DISCMODE bits in command register 0 which are set (1). $\overline{MR}$ must be high for at least two CLK periods after power-on. Minimum low time for reset is 1.5 CLK periods. All outputs are 3-stated when $\overline{MR}$ is asserted and $\overline{CS}$ is low.
120	A0	O*	**Address Bus Bit 0.**
121	A1	I/O*	**Address Bus Bit 1.** Part of 24-bit address bus
122	A2	I/O*	**Address Bus Bit 2.** (See description of pins 19—22).
123	A3	I/O*	**Address Bus Bit 3.**
124	NC	—	**No Connection.**
125	A9		**Address Bus Bit 9.**
126	A11		**Address Bus Bit 11.**
127	A13		**Address Bus Bit 13.** Part of 24-bit address bus.
128	A15	O*	**Address Bus Bit 15.** (See description of pins 19—22).
129	A16		**Address Bus Bit 16.**
130	A18		**Address Bus Bit 18.**
131	A20		**Address Bus Bit 20.**
132	D1		**Data Bus Bit 1.**
133	D2	I/O*	**Data Bus Bit 2.** Part of 16-bit data bus.
134	D3		**Data Bus Bit 3.** (See description of pins 1—6).
135	D4		**Data Bus Bit 4.**

*Indicates 3-state condition.

Overview

The T7102 XPC performs complete link-level control according to X.25 and X.75 data communications protocols. The device generates supervisory and unnumbered frames automatically without intervention by the host CPU. The host must supply buffers for the data fields of received and transmitted information frames. The CPU is notified of important events via interrupts. The XPC contains a transmitter, a receiver, a controller, and an interface unit, as shown on Figure 1.

Architecture

Transmitter. The transmitter constructs frames on command from the main controller. It contains a transmitter controller, 4-byte FIFO (first in, first out) buffer, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. It handles the transmission of continuous flags, aborts, or idle-channel indications automatically. Bit stuffing is implemented to ensure data transparency.

The transmitter FIFO and the transmitter holding register control the flow of information from main memory to the data link. The transmitter FIFO is used as temporary storage for data delivered from memory to the transmitter by the DMA controller. The DMA controller can read two bytes of data at a time from main memory and place them into the transmitter FIFO. The transmitter holding register is loaded in parallel fashion from the transmitter FIFO. The various bytes needed to construct a frame are also loaded into the holding register. When the data is ready to be transmitted, it is shifted out serially through the transmit data (TD) lead on the negative edge of the transmit clock (TC).

The CRC encoder calculates the frame check sequence (FCS) and appends it following the data field or after the control field for frames without data. The FCS is calculated over the address, control, and data fields. The zero inserter performs bit stuffing to ensure data transparency.

Receiver. The receiver processes incoming data and notifies the controller of received frames and other link conditions. The receiver contains a preprocessor, receiver controller, 4-byte FIFO, receiver register, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link, and deletes the zeros that were added for data transparency. Received data (RD) is latched on the positive edge of the receive clock (RC). Frames are identified and checked for proper format by the receiver controller.

The information field of a frame is loaded into the FIFO and is DMAed to memory by the interface unit.

The frame is checked for transmission errors by means of the CRC. The XPC acts on frames that are received error-free. Frames received with errors are discarded. The XPC maintains the number of link errors in the counter registers.

Controller. The controller interprets results from the receiver, transmitter, and internal registers, and implements the actions of the protocol. The X.25/X.75 protocol block contains the logic used to implement the entire X.25/X.75 level 2 protocol. Some specific tasks of the main controller involve configuring the link as specified by the parameter and command registers, maintaining the status registers, analyzing received frames and taking appropriate action, logging certain events in the bank of 16 event counters, directing the transmitter to send specific commands or responses, directing the interface unit to acquire receive and transmit data buffers, managing timing directions, and notifying the host of data link conditions through a set of interrupts.

DMA Interface Unit. The interface unit provides the interface between main memory and the transmitter and receiver via 2-channel DMA. It consists of a data bus selector, parity generator and checker, address controller, read/write machine, data section, and DMA controller.

The data bus selector controls the width of the external data bus and data byte ordering. The data bus can be set at either 8 or 16 bits wide by strapping the data bus selector pin to either V_{SS} or V_{DD}, respectively. The internal data bus is 8 bits wide. Data byte ordering is accomplished via a parameter register.

Parity is generated and checked over each byte of the data bus during DMA operations if parity is enabled. Parity is not checked or generated when the host accesses the XPC registers.

The address controller calculates and stores the addresses for the elements and buffer pointers for the transmit and receive channels.

The read/write machine generates the control signals to access data from memory, while the data section routes the data from memory to the transmit FIFO and from the receive FIFO to memory.

The DMA controller, on request from the controller, opens data buffers for the transmitter and receiver and controls the sequencing of the other sections.

A DMA priority scheme may be implemented in a daisy-chain fashion for multiple XPC applications with no additional hardware.

Loopback Test Control. The loopback test control connects the RD and TD pins as required by the near-end loopback test, far-end loopback test, or echo mode.

Table 2. XPC Register Addresses

Address				Address			
Hex	Dec	Status*	Name	Hex	Dec	Status*	Name
00	0	R/W	Command Register	32	50	R/W	Parameter Register 9
02	2	RO	Status Register 0	34	52	R/W	Parameter Register 10
04	4	RO	Status Register 1	36	54	R/W	Parameter Register 11
06	6	RO	Status Register 2	38	56	R/W	Parameter Register 12
08	8	RO	Status Register 3	3A	58	R/W	Parameter Register 13
0A	10	RO	Status Register 4	3C	60	R/W	Parameter Register 14
0C	12	RO	Status Register 5	3E	62	R/W	Parameter Register 15
0E	14	RO	Status Register 6	40	64	R/W	Counter Register 0
10	16	RO	Status Register 7	42	66	R/W	Counter Register 1
12	18	RO	Status Register 8	44	68	R/W	Counter Register 2
14	20	RO	Status Register 9	46	70	R/W	Counter Register 3
16	22	RO	Status Register 10	48	72	R/W	Counter Register 4
18	24	RO	Status Register 11	4A	74	R/W	Counter Register 5
1A	26	RO	Status Register 12	4C	76	R/W	Counter Register 6
1C	28	RO	Status Register 13	4E	78	R/W	Counter Register 7
1E	30	RO	Interrupt Register	50	80	R/W	Counter Register 8
20	32	R/W**	Parameter Register 0	52	82	R/W	Counter Register 9
22	34	R/W	Parameter Register 1	54	84	R/W	Counter Register 10
24	36	R/W	Parameter Register 2	56	86	R/W	Counter Register 11
26	38	R/W	Parameter Register 3	58	88	R/W	Counter Register 12
28	40	R/W	Parameter Register 4	5A	90	R/W	Counter Register 13
2A	42	R/W	Parameter Register 5	5C	92	R/W	Counter Register 14
2C	44	R/W	Parameter Register 6	5E	94	R/W	Counter Register 15
2E	46	R/W	Parameter Register 7	60	96	R/W	Counter Register 16
30	48	R/W	Parameter Register 8	62	98	R/W	Counter Register 17
				64	100	R/W	Parameter Register 16

*Read/write (R/W) or read only (RO) status.
**Parameter registers can be written to only when MDISC is set high.

Principles of Operation

CPU Interface

The CPU interface is used to specify commands to the XPC and receive status information from the XPC. The XPC is a peripheral device that accepts commands and provides interrupts and results back to the CPU when necessary. Through the CPU interface the CPU loads the command, parameter, and counter registers with the characteristics of the serial interface. The XPC provides status information and interrupts via the status and interrupt registers. The CPU accesses these registers via bits A1—A6 of the address bus. When $\overline{CS}$ is asserted, $\overline{RE}$, $\overline{WE}$, and the six address leads become inputs, and the $\overline{READY}$ lead becomes an output. Only the low order byte of the data bus is used for register read/write operations. The XPC ignores the upper byte during write operations a forces a 3-state condition on the upper data byte during read operations. The registers always appear on D0—D7 regardless of the byte ordering that is selected. Table 2 lists the register addresses for the XPC.

Master Reset

When the master reset ($\overline{MR}$) is asserted, the parameter registers are set to zero, the command register is set to 82H (DISCMODE=1, MDISC=1), and the interrupt register is set to zero. Status registers 9—13 and the counter registers are not initialized.

$\overline{MR}$ must be high for at least 2 CLKs after power-on. Minimum low time for reset is 1.5 CLK periods.

When the XPC detects a reset, it performs an internal reset sequence which requires 8 CLK periods. After the reset sequence, the XPC enters a set-up state in which the CPU can configure the parameter and counter registers. While in the set-up state, the XPC will transmit 1's and ignore any frames that are received. The XPC exits the set-up state and enters the operational state when the CPU clears MDISC in the command register.

Parameter register values can be changed by first placing the XPC in the set-up state with a reset, or by setting MDISC while the XPC is in the operational state. An exception to this is parameter register 0, which can be configured only in the set-up state.

$\overline{MR}$ is also used with $\overline{CS}$ to provide board isolation capabilities. If $\overline{CS}$ is low when $\overline{MR}$ is asserted, $\overline{INTR}$, $\overline{RTS}$, TD, $\overline{DREQ}$, and $\overline{DACK}$ will be placed in the high impedance state. If $\overline{CS}$ is high when $\overline{MR}$ is asserted, these pins will remain high or low. All other outputs will be placed in the high impedance state when $\overline{MR}$ is asserted regardless of the state of $\overline{CS}$.

Registers

The XPC contains 51 addressable registers for controlling and observing its operational mode. The registers are divided into five classes: command, status, interrupt, parameter, and counter.

Command Register — controls seven XPC functions: send, receive, mandatory disconnect, active or passive link initialization, password exchange, password verification, and disconnect mode. The command register can be written to at any time.

Status Registers — these fourteen registers report the state of the XPC, input conditions, and other vital information regarding the XPC to the CPU, e.g., the values of the state variables V(s) and V(r).

Interrupt Register — the register's lower six bits present an encoded reason for a particular interrupt issued to the CPU. Some reasons for the interrupts are packet received, parity error, idle link detected, and frame reject. This register is backed up by a four-word FIFO, enabling several interrupts to occur before the CPU can service the XPC. Bit 7 contains a lost interrupt bit. This bit is independent of the LSTIN bit in status register 0 and is implicitly cleared after a read of the interrupt register. If no interrupts are pending, the interrupt register will contain 00H.

Parameter Registers — these seventeen registers determine system constants and the mode of operation; for example, the period of the T1 and T4 timers and the address of the TLOOK table. The XPC can also be put into a test mode to test either itself or itself and the link. These registers can be written to only when MDISC is set high. An exception to this is parameter register 0, which can be configured only in the set-up state.

Counter Registers — these eighteen registers monitor the occurrence of 16 different events on the data link. These down counters monitor such events as the number of rejected frames received, the number of times timer T1 expired, and the number of parity errors. The counter registers can be written to at any time.

Table 3. Command Register Definitions

Bit	7	6	5	4	3	2	1	0
Field	DISCMODE	PWOK2	PWOK1	PWXCH	ACT/PAS	RECR	MDISC	SEND

Bit(s)	Symbol	Name/Description
0	SEND	**Send.** Controls transmission of packets. If 0, inhibits XPC from sending new packets. If 1, enables XPC to send new packets. The XPC will clear this bit if the link goes down or if the next transmit element is not ready. Retransmissions occur automatically, regardless of the send bit state.
1	MDISC	**Mandatory Disconnect.** Selects whether XPC may bring the link up or remain disconnected. If 0, XPC may bring the link up. If 1, XPC transmits all ones during fill times and remains disconnected. If the XPC is in the information transfer phase when MDISC is set, it will transmit a DISC frame and exit the information transfer phase. MDISC is set high (1) during a master reset (see Table 4).
2	RECR	**Receiver Ready.** Indicates availability of receiver buffers. If 0, no receiver buffers available. If 1, receiver buffers are allocated and available. The XPC will clear this bit if the receiver overruns, if the buffer chain segment is not ready, or if the receive element referenced by V(r) is not ready. If cleared while the XPC is in the information transfer phase, the XPC will enter the station busy state and ignore all incoming I-frames.
3	ACT/PAS	**Active/Passive.** Specifies XPC action in the disconnected phase. If 0, XPC passively awaits link setup. If 1, XPC actively initiates link setup (see Table 4).
4	PWXCH	**Password Exchange.** Determines which end of the link initiates password exchange. If 0, other end of link initiates password exchange. If 1, XPC initiates password exchange.
5, 6	PWOK1, PWOK2	**Password Verified.** Enables host to notify the XPC about correct action to take in response to a received password. Bits 4, 5, and 6 are interpreted as: **Code** **b6 b5 b4** **Condition** 0 1 0 Valid password command received 0 1 1 Valid password response received 1 0 0 Valid password command was not received 1 0 1 Valid password response was not received
7	DISCMODE	**Disconnect Mode.** Specifies disconnected state. DISCMODE is set (1) during master reset. DISCMODE must be set (1) for passive operation, and must be cleared (0) for XID operation. See Table 4.

Table 4. Disconnected Phase Operation

Protocol State	XIDEN	DISCMODE	ACT/PAS[1]	MDISC	Description
S0	0	x	x	1[2]	Does not respond to received frames until MDISC is cleared.[3]
					Responds to P-Bit Frame with DM final.[4]
S0	0	0	0	0	Respond to P-Bit Frame with DM final[5].
S1	0	1	0	0	Link can be initialized by remote DXE.
X	0	x	1	0	Initiate link set-up.
S0	1	0	0	0	Wait for XID transfer.
S0	1	0	1	0	Initiate XID transfer.
S0	1	0	x	1	Does not respond to received frames until MDISC is cleared.
S0	1	1	x	x	Do not use.

[1]Use PWXCH instead of ACT/PAS if XIDEN is 1.
[2]Interframe fill is idle (all 1s).
[3]MDISC not cleared yet after reset.
[4]MDISC previously cleared after reset.
[5]Interframe fill is flags.

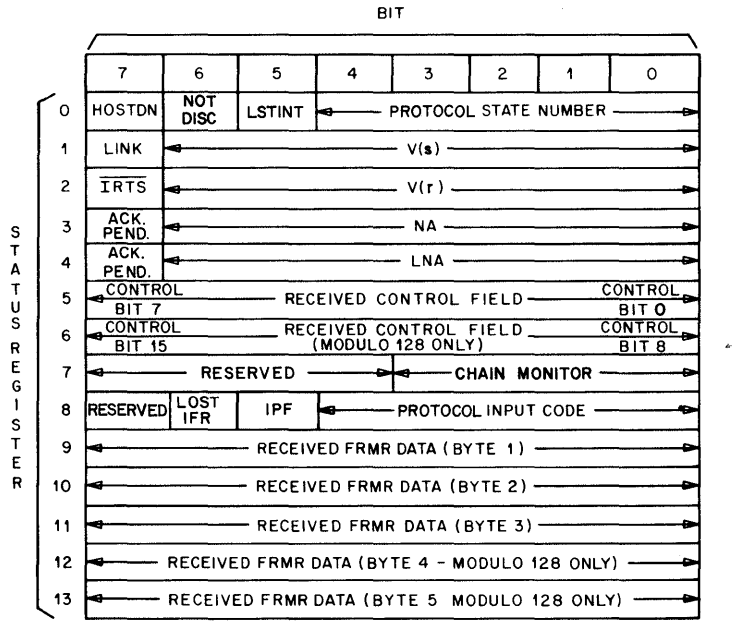


Figure 3. Status Registers

Table 5. Status Registers			
Reg(s)	**Bit(s)**	**Symbol**	**Name/Description**
0	0–4	–	**Protocol State Number**. Encoding of protocol state (see Table 6).
0	5	LSTINT	**Lost Interrupt**. Indicates if interrupts were lost. If 0, no interrupts were lost. If 1, interrupt register FIFO overflowed and interrupts were lost. This bit is implicitly cleared after a read of status register 0.
0	6	NOTDISC	**Not Disconnected.** This bit is cleared (0) if the XPC is disconnected or in XID phase. It is set (1) when the device is in link setup or information transfer phase (protocol state ≥ S3).
0	7	HOSTDN	**Host Done (Active Low).** Allows monitoring of internal host done bit in the event that the interrupt informing the host of link-down condition was lost. If 1, the host must reassign transmit and receive buffers before link reintialization is permitted. The XPC sets this bit when an SABM frame is received while it is in information transfer phase (LINK=1) or when the XPC exits the information transfer phase (LINK=0). This bit is cleared by writing to status register 0 or parameter register 1.
1	0–6	V(s)	**Send State Variable**. The sequence number, N(s), of next I frame to be transmitted and an index into TLOOK table to access buffer containing data for that frame.
1	7	LINK	**Link**. Indicates status of transmission link. If 0, information transfer is not possible. If 1, the XPC is in the information transfer phase (protocol state ≥ S6).
2	0–6	V(r)	**Receive State Variable**. Expected value of sequence number, N(s), of next I frame to be received and an index into RLOOK table for receiver buffer associated with that packet.
2	7	$\overline{\text{IRTS}}$	**Internal Request to Send**. Indicates that the XPC wants to acquire link. If 0, XPC wants link. If 1, XPC does not want link.
3	0–6	NA	**Next Acknowledgement Expected**. Number of earliest unacknowledged packet. If no outstanding packets, NA = V(s).
3	7	ACKPEND	**Acknowledgements Pending**. This bit goes high when the DMA has received acknowledgement processing to do. When all appropriate TLOOK elements have been updated this bit goes low. Before the host clears HOSTDN or reallocates transmit buffers, it must check that this bit is low.
4	0–6	LNA	**Last Next Acknowledgment Expected**. Whenever NA is updated, old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC.
4	7	ACKPEND	**Acknowledgements Pending**. See ACKPEND description above.
5	0–7	RECEIVED CONTROL FIELD	Holds control field of most recently received error free frame.

Table 5. Status Registers (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
6	0–7	RECEIVED CONTROL FIELD	Holds second byte of control field in modulo 128 mode only.
7	0–3	CHAIN MONITOR	Indicates which chain segment of receiver buffer is currently being used.
7	4–7	–	These bits are for internal use and should be masked when reading status register 7.
8	0–4	PROTOCOL INPUT CODE	Contains an encoding of what the protocol considers to be its most recent input stimulus (see Table 7).
8	5	IPF	Last poll/final bit upon which the XPC has acted. This bit is used in conjunction with the protocol input code.
8	6	LOST IFR	Cleared (0) for normal operation. Set (1) if I-frame was received but no receive buffers were available or if receiver overrun occurs. This bit is cleared (0) when the XPC exits the station busy condition.
8	7	–	This bit is for internal use and should be masked when reading status register 8.
9–11	0–7	RECEIVED FRMR FIELD	Holds first, second, and third bytes of data field contained in a received FRMR frame.
12, 13	0–7	RECEIVED FRMR DATA FIELD	Holds fourth and fifth byte of data field in FRMR frame (modulo 128 only).

Table 6. Status Register 0 – Protocol State Number Encoding

State Number					State	Name
b4	b3	b2	b1	b0		
0	0	0	0	0	S0	Logically disconnected
0	0	0	0	1	S1	Logically disconnected
0	0	0	1	0	S2a	Awaiting XID command
0	0	0	1	1	S2b	Awaiting XID response
0	0	1	0	0	S3	Link setup initiated
0	0	1	1	1	S4	Frame rejected
0	0	1	0	1	S5	Disconnect request
0	0	1	1	0	S6	Information transfer
0	1	0	0	0	S7	REJ frame sent
0	1	0	0	1	S8	Waiting acknowledgment
1	0	0	0	1	S9	Station busy
0	1	0	1	0	S10	Remote station busy

Table 6. Status Register 0 — Protocol State Number Encoding (Continued)						
State Number						
b4	b3	b2	b1	b0	State	Name
0	1	1	1	1	S11	S9 and S10
1	0	0	0	0	S12	S8 and S9
0	1	0	1	1	S13	S8 and S10
1	1	0	1	0	S14	S8, S9, and S10
1	1	0	1	1	S15	S7 and S9
0	1	1	0	0	S16	S7 and S10
0	1	1	0	1	S17	S7, S9, and S10

Table 7. Status Register 8 — Input Code	
Input Code*	Description
0	Local stop — disconnect link
1	Local start — initiate link setup
2	Busy condition clears
3	Valid XID command received
4	T1 expired
5	T3/T4 expired
6	Station has become busy
7	I-frame available (Reset condition also)
8	Invalid N(s) in last received I-frame
9	Unrecognized frame received
10	I-frame received
11	RNR command received
12	REJ command received
13	RR command received
14	SABM received
15	DISC received
16	UA received
17	FRMR received
18	DM received
19	Valid XID response received
20	Idle link detected for T3
21	Wrong N(s) in last received I-frame
23	N2 exceeded
24	Invalid N(r)in last received I-frame
26	Initiate password exchange
27	RNR response received
28	REJ response received
29	RR response received
30	Wait for password exchange

*This code is represented as a binary number in the 5-bit protocol input code field in the status register.

Table 8. Interrupt Vector Register

Bit	7	6	5	4	3	2	1	0
Field	LOST INTERRUPT	NOT DEFINED	INT5	INT4	INT3	INT2	INT1	INT0

Code*	Interrupt	Name/Description
1	SABM	**Link Reset Received.** An SABM or SABME command frame was received while the XPC was in the information transfer phase. Link is reinitialized when HOSTDN is cleared.
2	UA	**UA Received While Link Is Up.** The XPC initializes link because an unnumbered response frame was received acknowledging an unnumbered command never sent. Link is reinitialized when HOSTDN has been cleared. If in X.75 mode, a FRMR frame is sent.
3	DM	**DM Received.** The XPC will attempt to initialize link if it is in active mode because it received an unsolicited unnumbered response frame indicating that far end of link is in disconnected state. If in X.75 mode, a FRMR frame is sent.
4	FRMRR	**Frame Reject (FRMR) Received.** The interrupt is issued after data is stored in status registers 9—13.
5	DISC	**Received DISC While Link is Up.** This interrupt occurs when a disconnect command is received while the XPC is in the information transfer phase, causing link to go down.
6	IDLINK	**Idle Link Detected.** If the XPC detects 15 or more contiguous 1s, it starts timer T3 if T1 is not running. If a flag is not detected before timer T3 expires, an idle link is reported and this interrupt is issued. If timer T1 is running, the XPC waits for T1 to finish before starting T3.
7	N2EXC	**N2/C2 Counter was Exceeded.** XPC attempts to initialize link if in active mode because maximum number of retransmissions (N2) was exceeded. If in password exchange, this counter is interpreted as a C2 counter.
8	RF1P	**F = 1 Received Without Sending P = 1.** This interrupt occurs when a response frame with final bit set to 1 was received but XPC did not send a command frame with poll bit set to 1. In X.25 mode, the frame is discarded. In X.75 mode, the XPC will send a FRMR frame to begin link reset procedures.
9	LK01	**Link is Up.** The XPC goes from one of the disconnected or link setup states to the information transfer phase (the logical link has come up).
10	XIDRCVD	**XID Frame Received.** An XID frame was received and its data field placed in main memory.

* This code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit. This bit is implicitly cleared after the interrupt register is read.

Table 8. Interrupt Vector Register (Continued)		
Code*	**Interrupt**	**Name/Description**
11	NOXIDR	**No XID Response.** An XID command was transmitted and no response was received in time T4.
12	FRMRX-W	**Frame Reject Transmitted — W = 1.**** Receipt of command or response that is invalid or not implemented and cannot be corrected by retransmission.
13	FRMRX-X	**Frame Reject Transmitted — X = 1.**** Receipt of S- or U-frame with an information field which is not permitted.
14	FRMRX-Y	**Frame Reject Transmitted — Y = 1.**** Receipt of an I frame with an information field which exceeds the maximum established length N1.
15	FRMRX-Z	**Frame Reject Transmitted — Z = 1.**** Receipt of an invalid N(r).
16	PKR	**Packet Received.** This interrupt is issued after the XPC has received an I-frame and stored its data field in main memory. V(r) points to the next element in the RLOOK table when this interrupt is issued.
17	XBA	**Transmitted Block Acknowledged.** Issued when the XPC receives acknowledgment for one or more previously transmitted I-frames.
18	RCVOVR	**Receiver Overrun.** Receiver FIFO overflowed because new characters are being brought in faster than DMA can save them in main memory. The receiver FIFO is four bytes deep. The XPC clears the RECR bit in the command register when issuing this interrupt.
19	XUNDR	**Transmitter Underrun.** The transmitter FIFO buffer became empty during transmission and frame was aborted. If the send bit is set, the XPC will attempt to retransmit the I-frame. The transmit FIFO is four bytes deep.
20	PPROB	**Parity Error.** If the DMA reads a main memory location and an error is detected, it reads it again. This interrupt is issued if the error is repeated. If an I-frame is in transmission, it will be aborted.
21	RLKNRDY	**Receiver Look-Up (RLOOK) Table Not Ready.** XPC read RLOOK element referenced by V(r), and found that RECRDY bit is zero. It clears RECR bit in the command register when issuing this interrupt.
22	LDCHM	**Going to Next Chain Segment.** The DMA has filled a buffer segment, and automatically transfers (chains) to next segment.
23	BFOVF	**Buffer Overflow (Next Chain Segment Not Ready).** The DMA read the transfer address before transferring to next buffer and it was zero. This interrupt occurs only for the receive buffers. XPC clears the RECR bit in the command register when issuing this interrupt.
24	BADIFLD	**Received I-Field is Not an Integral Number of Bytes.** The length of data field of a received I frame is not an integral number of bytes and the XPC is in byte mode. Bit 5 of byte 0 of the RLOOK element will be set.

* This code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit. This bit is implicitly cleared after the interrupt register is read.

** W, X, Y, and Z are bits in the information field of a frame reject response that indicates the reason that a frame is being frame rejected. The XPC automatically generates this response.

Table 8. Interrupt Vector Register (Continued)		
Code*	**Interrupt**	**Name/Description**
25	CTSLST	**Clear to Send Lost.** Clear-to-send $\overline{CTS}$ input on the XPC went high. The XPC will go into inactive state until $\overline{CTS}$ goes low.
26	ODAD	**Odd Address.** TLOOK starting address is odd and data bus set for 16-bit operation. The XPC will set MDISC and go into the setup state.
27	NOAD	**No Address.** TLOOK starting address is zero. The XPC will set MDISC and go into the setup state.
28	RCOVF	**Receiver Counter Overflowed.** Data field longer than the maximum 4096 bytes permitted by DMA was received.
29	LK10	**Link is Down.** XPC goes to a link setup or disconnect state. HOSTDN must be cleared to resume normal operation.
30	CTSACQ	**Clear to Send Acquired.** $\overline{CTS}$ input went low.
31	RCLST	**Receive Carrier Lost.** $\overline{CD}$ input went high. The XPC takes no further action.
32	CO†	**Countout in Counters 0, 1.** Register Addresses 64, 66.
33	CO	**Countout in Counter 17.** Register Address 98.
34	CO	**Countout in Counters 2, 3.** Register Addresses 68, 70.
35	CO	**Countout in Counter 16.** Register Address 96.
36	CO	**Countout in Counter 4.** Register Address 72.
37	CO	**Countout in Counter 5.** Register Address 74.
38	CO	**Countout in Counter 6.** Register Address 76.
39	CO	**Countout in Counter 7.** Register Address 78.
40	CO	**Countout in Counter 8.** Register Address 80.
41	CO	**Countout in Counter 9.** Register Address 82.
42	CO	**Countout in Counter 10.** Register Address 84.
43	CO	**Countout in Counter 11.** Register Address 86.
44	CO	**Countout in Counter 12.** Register Address 88.
45	CO	**Countout in Counter 13.** Register Address 90.
46	CO	**Countout in Counter 14.** Register Address 92.
47	CO	**Countout in Counter 15.** Register Address 94.
48	RCACQ	**Receive Carrier Acquired.** $\overline{CD}$ input went low. The XPC takes no further action.

* This code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit. This bit is implicitly cleared after the interrupt register is read.

† Interrupt on countout bit in parameter register 1 must be set for the CO interrupts to occur.

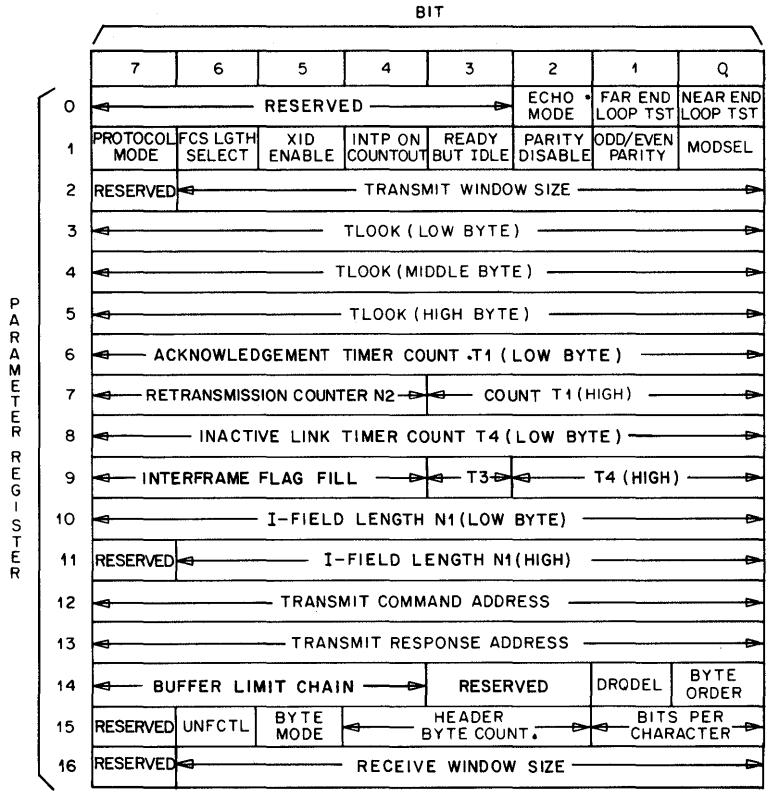


Figure 4. Parameter Registers

Table 9. Parameter Registers

Reg(s)	Bit(s)	Symbol	Name/Description
0	0	NEAR-END* LOOP TEST	Setting this bit high causes the XPC to enter the near-end loopback test mode. TD and RD are internally tied together; the XPC transmits 1s on TD. Both RC and TC must be applied and must be synchronized with each other. $\overline{CTS}$ must be active low.
0	1	FAR-END* LOOP TEST	Setting this bit high causes the XPC to enter, in conjunction with link controller at far-end of loop, the far-end loopback test. The remote station must be in echo mode. Both RC and TC must be applied. $\overline{CTS}$ must be active low.
0	2	ECHO MODE*	Setting this bit high causes data coming into receiver data (RD) input to appear at transmitter data (TD) output. The XPC takes no action on received frames. Neither RC nor TC need be applied.

*These bits cause the specified action only if set after a chip reset and before MDISC is cleared.

Table 9. Parameter Registers (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
0	3–7	–	These bits are for internal use and are not writable.
1	0	MODSEL	**Modulus Select.** If 0, selects modulo 8, normal sequence numbering. If 1, selects modulo 128, extended sequence numbering.
1	1	ODD/EVEN PARITY	**Status of XPC Parity.** If 0, even parity. If 1, odd parity.
1	2	PARITY DISABLE	Setting this bit high disables the parity generation and checking capability. The parity pins should not be connected if parity is disabled.
1	3	READY BUT IDLE	If 0, XPC transmits continuous stream of flags when logically disconnected and not sending frames. If 1, XPC transmits continuous stream of ones as interframe fill when logically disconnected.
1	4	INTERRUPT ON COUNTOUT	If this bit is set high, the XPC issues an interrupt if any of the counter registers are decremented to zero.
1	5	PASSWORD ENABLE	Setting this bit high causes the XPC to require a password exchange with far end of link before the link set-up is allowed.
1	6	FCS LENGTH SELECT	If 0, XPC uses standard 16-bit CRC generator polynomial. If 1, XPC uses 32-bit CRC generator polynomial.
1	7	PROTOCOL MODE	If this bit is set (1), the XPC is in X.75 mode. If this bit is cleared (0), the device is in X.25 mode.
2	0–6	TRANSMIT WINDOW SIZE	Maximum allowable number of outstanding I-frames (must not equal zero). An outstanding I-frame is considered to be any I-frame which has not been acknowledged by the remote DXE. Valid values are 1–7 for modulo 8, and 1–127 for modulo 128.
2	7	–	This bit is for internal use and is not writable.
3–5	0–7	TLOOK	**Transmitter Look-Up Table Pointer.** Starting address in main memory of first element of transmitter lookup table.
6	0–7	T1 (Low Byte)	This number is proportional to period of the T1 timer. It is the maximum time the XPC will wait for an acknowledgment. $T1\ COUNT_{DECIMAL} = \frac{fCLK}{16384} \times T1\ PERIOD_{SEC}$.
7	0–3	T1 (High Bits)	
7	4–7	N2	X.25 retransmission counter. Valid values are 1–15 which determine the maximum number of transmissions and retransmissions of a frame without receiving an acceptable response.

Table 9. Parameter Registers (Continued)

Reg(s)	Bit(s)	Symbol	Name/Description
8 9	0–7 0–2	T4 (Low Byte) T4 (High Bits)	A number proportional to period of the T4 timer. Maximum time a station will allow without frames being exchanged on data link. This parameter is also used as part of the pseudo T3 timer. $T4\ COUNT_{DECIMAL} = \frac{fCLK}{16384} \times T4\ PERIOD_{SEC.}$
9	3	T3	Maximum time a station will receive an idle condition before resetting the link. If T3=0, the period of T3 = the period of T4. If T3=1, the period of T3 = T4 period + $\frac{2^{25}}{fCLK}$.
9	4–7	INTERFRAME FLAG FILL	A weighted code specifying the minimum number of flags to be inserted between frames (see Table 10).
10 11	0–7 0–6	N1 (Low Byte) N1 (High Bits)	**Maximum I-Field Length.** The XPC will frame reject (FRMR) any I-frame whose IFIELD length exceeds N1 bits.
11	7	–	This bit is for internal use and is not writable.
12	0–7	TRANSMIT COMMAND ADDRESS	Address field of command frames transmitted by the XPC. Station address of far-end link.
13	0–7	TRANSMIT RESPONSE ADDRESS	Address field of response frames transmitted by the XPC. Station address of this station.
14	0	BYTE ORDER	Clear (0) Intel data bus convention used by DMA. D7–D0 is even byte; D15–D8 is odd byte. Set (1) Motorola data bus convention used by DMA. D7–D0 is odd byte. D15–D8 is even byte. $\overline{BHE}$ becomes $\overline{BLE}$ when this bit is set (see Figure 9 and Table 18).
14	1	DMA REQUEST DELAY	If this bit is set, the DMA logic will wait for $\overline{DACK}$ to go high (1) before reasserting $\overline{DREQ}$. If this bit is clear (0), the DMA logic will not wait for $\overline{DACK}$ to be set (1) before reasserting $\overline{DREQ}$.
14	4–7	LIMIT	Size of buffer segments for both receiver and transmitter. Buffer segments must be sized in 64-byte multiples. Limit = $\frac{\text{BUFFER SEGMENT}}{64} - 1$. Maximum buffer segment = 64(1+15) = 1024 bytes.
15	0,1	BITS PER CHARACTER	Characters are 5, 6, 7, and 8 bits in length and are right-justified with zeros in most significant bits (see Table 11).
15	2–4	HEADER BYTE COUNT	Data field of an I frame might consist of a number of characters proceeded by some 8-bit header bytes. This field specifies number of 8-bit bytes in header (see Table 12).
15	5	BYTE MODE	If 0, a received fractional byte length data field is permitted. If 1, received I-frames must be an integral number of 8-bit bytes.
15	6	UNFCTL	Used in modulo 128 operation only. If 0, unnumbered control field is two bytes. If 1, unnumbered control field is one byte.

Table 9. Parameter Registers (Continued)			
Reg(s)	**Bit(s)**	**Symbol**	**Name/Description**
15	7	—	This bit is for internal use and is not writable.
16	0—6	RECEIVE WINDOW SIZE	Used in X.75 mode only. The maximum allowable number of packets that can be received before an acknowledgement must be sent. Valid values are 1—7 for modulo 8, and 1—127 for modulo 128.
16	7	—	This bit is for internal use and is not writable.

Main Memory

Main memory contains data buffers which store transmit and receive data. The pointers used to access these buffers are also stored in main memory. These pointers are located in the lookup tables. The location of data to be transmitted is represented by pointers in the transmitter lookup table (TLOOK) elements and the location of data to be received is represented by pointers in the receiver lookup table (RLOOK) elements.

Table 10. Interframe Flag Fill	
Flag Fill Parameter	**Minimum Number of Flags**
0	1
1	2
2	4
3	6
4	16
5	18
6	20
7	22
8	64
9	66
10	68
11	70
12	80
13	82
14	84
15	86

Table 11. Bits Per Character Encoding		
Parameter Register 15		**Number of Bits per Character**
b1	**b0**	
0	0	8
0	1	7
1	0	6
1	1	5

Table 12. Header Byte Count			
Parameter Register 15			**Number of Header Bytes**
b4	**b3**	**b2**	
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 13. Counter Registers

Counter	Register Number	Description of Event Counted
0	64	Sup. and unnumbered frames received (low byte)
1	66	Sup. and unnumbered frames received (high byte)
2	68	Sup. and unnumbered frames sent (low byte)
3	70	Sup. and unnumbered frames sent (high byte)
4	72	REJ frames received
5	74	REJ frames sent
6	76	RNR frames received
7	78	RNR frames sent
8	80	I-frames retransmitted
9	82	Number of times T1 expired
10	84	Null packets received
11	86	Short frames received
12	88	I-fields greater than N1 received
13	90	Bad frame check sequences received
14	92	Invalid addresses received
15	94	Invalid control fields received
16	96	Number of aborts received
17	98	Number of parity errors

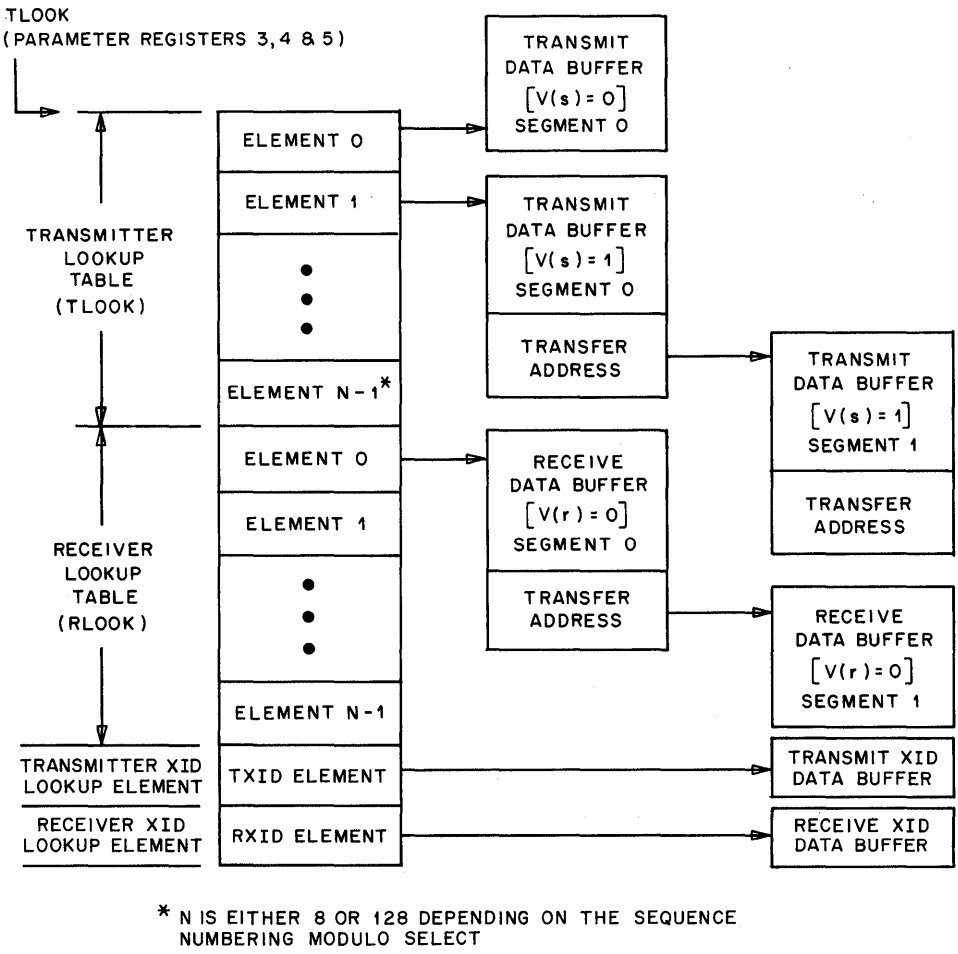
Note: Sup. stands for supervisory.

The TLOOK table is a list of N 8-byte elements in main memory starting at address TLOOK (stored in parameter registers 3, 4, and 5). N is either 8 or 128 and is determined by the modulus select bit in parameter register 1. Each element in the TLOOK table describes the buffers corresponding to one packet of data to be transmitted by the XPC. The TLOOK list of elements is actually used like a circular queue with element number V(s) at the head.

The RLOOK table is a list of N 8-byte elements in main memory immediately following the TLOOK table. Each element in the RLOOK table describes the buffers corresponding to one packet of data to be received by the XPC. The RLOOK list of elements is maintained as a circular queue also. The head of the queue has element V(r) in it.

The XID table is a list of two 8-byte elements in main memory immediately following the RLOOK table. Element 0 is the transmit element and element 1 is the receive element. The TXID and RXID elements are identical to the TLOOK and RLOOK elements, respectively.

When buffer chaining is used, if a transfer address of 0 is encountered the buffer will be considered to have ended. Transfer addresses immediately follow the buffers in main memory and are three bytes long (low, middle, and high bytes). Buffer segments must be sized in multiples of 64 bytes. The maximum buffer segment can be 1024 bytes. The XPC determines the size of the buffer segment from the limit field in parameter register 14.



Note: Each element consists of 8 bytes. Each transfer address consists of 3 bytes.

Figure 5. Main Memory Configuration

DMA Operation

The XPC uses a dual-channel DMA to read and write the data fields of I frames and XID frames, and the TLOOK and RLOOK tables. The full 16-bit data bus is used for this operation when the DBC pin is connected to V_{DD}. An 8-bit data bus (lower byte of data bus) is used when DBC is connected to V_{SS}.

When the XPC is configured with an 8-bit data bus, DMA may begin on even or odd byte boundaries for the RLOOK and TLOOK tables and buffers. With an 8-bit data bus, the XPC reads and writes one byte at a time. The upper data byte (D15—D8) is not used.

When the XPC is configured with a 16-bit data bus, DMA must begin on even word address boundaries for the RLOOK and TLOOK tables and buffers. $\overline{BHE}/\overline{BLE}$ from the DMA controller is used to access the odd byte of a 16-bit word. $\overline{BHE}/\overline{BLE}$ allows individual selection of even bytes (A0 = 0, $\overline{BHE}/\overline{BLE}$ = 1) or both odd and even bytes as words (A0 =0, $\overline{BHE}/\overline{BLE}$ = 0).

When BYTORD is high, the data bus is configured in Motorola mode. $\overline{BHE}$ is then considered $\overline{BLE}$. The odd byte will appear on D7—D0 (see Figure 9 and Table 18).

To initiate a DMA bus cycle, the XPC requests the use of the bus by forcing $\overline{DREQ}$ low. The host CPU indicates that the bus is available by forcing $\overline{DACK}$ low. This allows $\overline{RE}$, $\overline{WE}$, R/$\overline{W}$, $\overline{BHE}/\overline{BLE}$, A0—A23, and $\overline{AS}$ to become outputs and $\overline{READY}$ to become an input. Once the DMA has control of the bus, it expects to have use of the bus until it has finished its DMA operation. For some operations, the DMA can request the use of the bus within 2 CLK periods after it has relinquished bus control. For those applications where $\overline{DACK}$ is quick enough to respond within 2 CLK periods, DRQDEL in parameter register 14 can be set to zero. If $\overline{DACK}$ is slow to respond, DRQDEL must be set high.

Slow memory handshaking is provided through the $\overline{READY}$ input. The DMA will hold a read or write until it samples $\overline{READY}$ low.

When instructed to open a transmit element, the DMA will calculate the address of the particular TLOOK element from the TLOOK base address and the value of V(s), and will proceed to read the bytes of the element. If the BRDY bit in the first byte is zero, the DMA will abort the TLOOK read. The XPC will clear the SEND bit in the command register and information transmission is suspended. If BRDY is high, the DMA will continue to read the TLOOK element, placing the transmit count in a byte counter and the transmit buffer pointer in an address counter register. The DMA then fetches the data to be transmitted from memory and routes it to the transmitter FIFO. The transmitter will signal the DMA for more data when the transmit FIFO contains two bytes or less. The loading process ends when the number of bytes specified by the transmit count has been loaded into the transmit FIFO. The DMA then places this TLOOK element in the not acknowledged state by setting the NACK bit and clearing the BRDY bit in the element. The TLOOK element is available for retransmission when in this configuration.

When an acknowledgement is received, the DMA will clear the NACK bit and set the ACK bit of all the TLOOK elements whose information buffers have been acknowledged. The DMA will then issue an XBA interrupt indicating that the data associated with one or more TLOOK elements has been acknowledged. The host can then reallocate the TLOOK elements to send more information frames.

When instructed to open a receive element, the DMA will calculate the address of the particular RLOOK element from the TLOOK base address and the value of V(r) and will proceed to read the bytes of the element. If the RECRDY bit in the first byte is zero, the DMA will abort the RLOOK read. The XPC will clear the RECR bit in the command register and any information frames that are received will be discarded. If RECRDY is high, the DMA will continue to read the RLOOK element, placing the receive

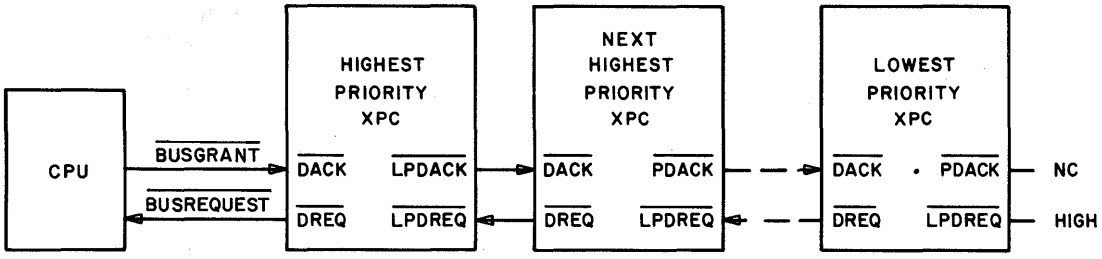


Figure 6. DMA Priority Scheme Interconnection

buffer pointer in an address counter register. When the receive FIFO contains two or more bytes of data, the DMA will route the data from the FIFO and write it out to memory. The DMA continues to write data to memory until it is notified by the receiver of an end-of-frame condition. At this time the DMA flushes out the receive FIFO and updates the RLOOK element with the number of bytes received and places the element in the frame complete state. The DMA then issues a PKR interrupt, notifying the host that an information frame was received and the data was placed in memory. The host can then reallocate the RLOOK element in anticipation of receiving more information frames.

The DMA accesses the transmit and receive buffers two bytes at a time when configured for 8-bit data buses and one word at a time when configured for 16-bit data buses. If the number of bytes in the buffer is odd, the last access will be a single byte access.

A priority DMA bus arbitration scheme may be implemented using a daisy chain for multiple XPC applications with no additional hardware. The $\overline{\text{DREQ}}$ pin of the lowest priority XPC is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC. $\overline{\text{DREQ}}$ for the highest priority XPC is tied to the HOLD input of the CPU. The hold acknowledge output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC. The $\overline{\text{PDACK}}$ of the highest priority XPC is tied to $\overline{\text{DACK}}$ of the next highest priority XPC and this continues until the lowest priority XPC is reached. The $\overline{\text{LPDREQ}}$ input of the lowest priority XPC must be tied high.

Caution: When resetting an XPC in a chain, $\overline{\text{CS}}$ must be held high for that XPC. If $\overline{\text{CS}}$ is low when the XPC is reset, the outputs will go to a 3-state condition and the propagated request and acknowledge signals will be disrupted.

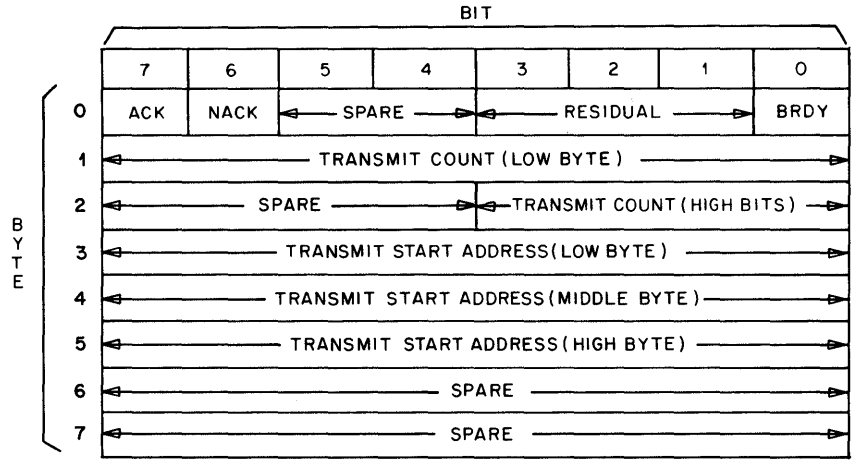


Figure 7. TLOOK Element Layout

Table 14. TLOOK Elements

Byte(s)	Bit(s)	Symbol	Name/Description
0	0	BRDY	**Buffer Ready**. Setting this bit tells the XPC that data associated with this element is ready to be transmitted. BRDY is the last bit to be set by CPU. After all the data of a frame has been accessed, the XPC clears the BRDY bit and sets the NACK bit of the associated element. If the NACK bit is set, it also indicates that the buffer is available to the XPC for retransmission.
0	1–3	RESIDUAL	**Residual**. The XPC allows the CPU to select the number of bits that should be transmitted from the last byte of data. (See Table 17). When in byte mode there should be no residual bits.
0	4, 5	SPARE	**Spare**. Not used.
0	6	NACK	**Not Acknowledged**. The XPC sets this bit after all the data has been accessed. The XPC clears this bit when the packet associated with this element becomes acknowledged.
0	7	ACK	**Acknowledged**. The XPC sets this bit when a packet associated with this element becomes acknowledged and generates an XBA interrupt to the CPU. Only then may the CPU reuse this buffer.
1 2	0–7 0–3	TRANSMIT COUNT	**Transmit Count**. The number of bytes in a data packet is specified by this 12-bit number. Byte 1 is the low order byte and byte 2 is the high order nibble.
2	4–7	SPARE	**Spare**. Not used.
3–5	0–7	TRANSMIT START ADDRESS	**Transmit Start Address**. This 24-bit number is the location in main memory of the first byte of data in the packet associated with this element.
6, 7	0–7	SPARE	**Spare**. Not used.

Table 15. TLOOK Residual Field

TLOOK Element Byte 0			Bits Transmitted From Last Memory Byte
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

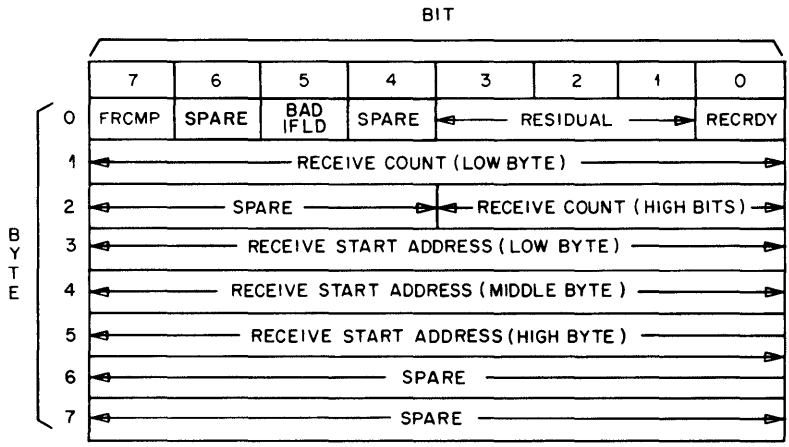


Figure 8. RLOOK Element Layout

Table 16. RLOOK Elements

Byte(s)	Bit(s)	Symbol	Name/Description
0	0	RECRDY	**Receiver Ready**. Setting this bit tells the XPC that the data buffer associated with this element is ready to receive data. All fields of the RLOOK element should be initialized before the CPU sets the RECRDY bit. After the XPC receives a valid packet and stores it in memory, it clears the RECRDY bit of the associated element.
0	1—3	RESIDUAL	**Residual Bits**. After the XPC receives a frame, it writes the number of bits stored in the last byte into the residual bits field (see Table 19).
0	4	SPARE	**Spare**. Not used.
0	5	BADIFLD	A fractional byte length frame was received and stored in the buffer pointed to by this element. The XPC will also generate a BADIFLD interrupt. This bit will be set only if the XPC is in byte-mode.
0	6	SPARE	**Spare**. Not used.
0	7	FRCMP	**Frame Complete**. When a valid I-frame is received completely, the XPC writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is generated to notify the CPU of the received packet.
1 2	0—7 0—3	RECEIVER COUNT	**Receiver Count**. This 12-bit number specifies how many bytes of memory have been filled by the packet. The XPC writes this after the I-frame has been received.
2	4—7	SPARE	**Spare**. Not used.
3—5	0—7	RECEIVE START ADDRESS	**Receive Start Address**. This 24-bit address is the location in main memory of the first byte of received data for the packet.
6, 7	0—7	SPARE	**Spare**. Not used.

Table 17. RLOOK Residual Field

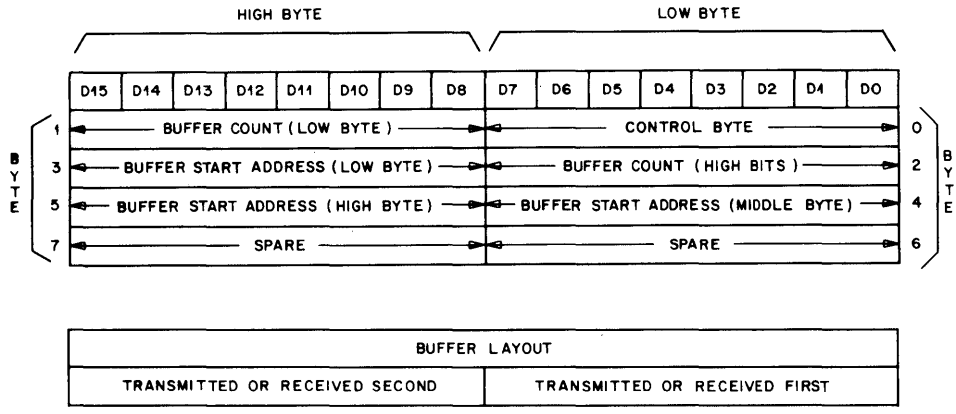
RLOOK Byte 0			Received Bits in Last Memory Character Bits per Character=*			
b3	b2	b1	8	7	6	5
0	0	0	8	7	6	5
0	0	1	1	1	1	1
0	1	0	2	2	2	2
0	1	1	3	3	3	3
1	0	0	4	4	4	4
1	0	1	5	5	5	x
1	1	0	6	6	x	x
1	1	1	7	x	x	x

*x denotes don't care condition.

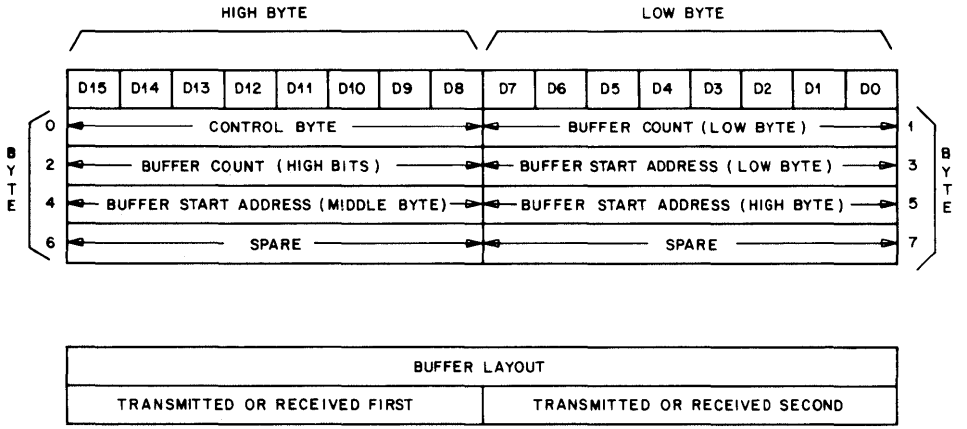
Table 18. Intel and Motorola Modes*

BYTORD	$\overline{BHE}/\overline{BLE}$	Mode	Read		Write	
			D15–D8	D7–D0	D15–D8	D7–D0
0	0	Intel	Input	Input	Output	Output
0	1	Intel	3-state	Input	3-state	Output
1	0	Motorola	Input	Input	Output	Output
1	1	Motorola	Input	3-state	Output	3-state

*DBC =1, A0 = 0



Receive or Transmit Element in Intel Mode (BYTORD=0)



Receive or Transmit Element in Motorola Mode (BYTORD=1)

Note: The above figures explain how the elements are laid out in memory for each value of BYTORD in 16-bit mode (DBC=1).

Figure 9. Receive or Transmit Element Layout

CHARACTERISTICS

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 ± 0.25 V, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Voltage					
Low	V_{IL}	−0.5	0.8	V	–
High	V_{IH}	2.0	V_{DD}	V	–
Output Voltage					
Low	V_{OL}	–	0.45	V	I_{OL} = 1.7 mA
High	V_{OH}	2.4	–	V	I_{OH} = −400 μA
Power Supply Current	I_{DD}	–	400	mA	–
Input Current					
High	I_{IH}	–	10	μA	V_{IH} = 5.25 V
Output Float Current					
Low	I_{OZL}	–	−10	μA	V_{OL} = 0.4 V
High	I_{OZH}	–	10	μA	V_{OH} = 5.25 V
Power Dissipation	PD	–	2.0	W	V_{DD} = 5.0

Maximum Ratings

Ambient Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... −65 to +125 °C
Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Power Dissipation (PD) ..... 2.8 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Unit
Clock Timing (Figure 10)				
tCKHCKL	Clock High Time	240	3760	ns
tCKLCKH	Clock Low Time	240	3760	ns
tCKHCKH	CLK Period (Sum of tCKHCKL and tCKLCKH)	500	4000	ns
Receive Clock Timing (Figure 11)				
tRCHRCL	RC High Time	3tCKHCKH	–	–
tRCLRCH	RC Low Time	3tCKHCKH	–	–
tRCHRDX	RD Hold Time	1.5CKHCKH	–	–
tRDVRCH	RD Set-Up Time	1.5CKHCKH	–	–
Transmit Clock Timing (Figure 12)				
tTCHTCL	TC High Time	3tCKHCKH	–	–
tTCLTCH	TC Low Time	3tCKHCKH	–	–
tTCLTDX	TD Transition Delay	tCKHCKH	2.5 tCKHCKH	–
Reading XPC Registers (Figure 13)				
tAVREL	Address Set-Up Time	0	–	ns
tREHAX	Address Hold Time	0	–	ns
tCSLREL	$\overline{CS}$ Set-Up Time	0	–	ns
tREHCSX	$\overline{CS}$ Hold Time	0	–	ns
tCKHRYL	Ready Wait Propagation Time	tCKHCKLMIN+ tCKLRYL+10 ns	13.5tCKHCKH+ tCKLRYL	–
tCKLRYL	$\overline{READY}$ Transition Delay	0	265	ns
tREHRYH	$\overline{READY}$ Hold Time After $\overline{RE}$ Goes High	210	–	ns
tREHREL	Interoperation Delay Time	tCKHCKH	–	–
tRELCKH	$\overline{RE}$ Set-Up Time for Ready Wait Propagation	120	–	ns
tDVCKL	Data Valid Set-Up Time for Event Counter Registers	25	–	ns
tCSLDV	Time to Data Valid for Nonevent Counter Registers	50	250	ns
tCSHDZ	Data Hold Time	0	–	ns
tAVDX	Data Hold Time	0	–	ns
tCSHRYX	$\overline{READY}$ Hold Time After $\overline{CS}$ Goes High	0	50	ns

Symbol	Description	Min	Max	Unit
	Writing XPC Registers (Figure 14)			
tAVWEL	Address Set-Up Time	0	–	ns
tRYLAX	Address Hold Time	0	–	ns
tCSLWEL	$\overline{CS}$ Set-Up Time	0	–	ns
tRYLCSX	$\overline{CS}$ Hold Time	0	–	ns
tWELDV	Data Set-Up Time	–	tCKHCKLMIN	–
tRYLDX	Data Hold Time	0	–	ns
tWELCKH	$\overline{WE}$ Set-Up Time for Ready Wait Propagation	140	–	ns
tRYLWEH	$\overline{WE}$ Hold Time	0	–	ns
tCKHRYL	Ready Wait Propagation Time	3tCKHCKH+ tCKLRYL	13.5tCKHCKH tCKLRYL	–
tCKLRYL	$\overline{READY}$ Transition Delay	0	265	ns
tWEHRYH	$\overline{READY}$ Hold Time After $\overline{WE}$ Goes High	245	–	ns
tWEHWEL	Interoperation Delay Time	tCKHCKH	–	–
tCSHRYX	$\overline{READY}$ Hold Time After $\overline{CS}$ Goes High	0	50	ns
	DMA Read Cycle (Figure 15)			
tCKLDRL	$\overline{DREQ}$ Transition Delay	–	265	ns
tCKHDRH	$\overline{DREQ}$ Transition Delay	–	175	ns
tDALCKL	$\overline{DACK}$ Set-Up Time	160	–	ns
tDRHDAH	$\overline{DACK}$ Response Time to Removal of $\overline{DREQ}$ DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH –	 – ns
tDALRWV	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ Delay Time from $\overline{DACK}$ Low	–	200	ns
tCKLAV	Address Valid Delay Time from CLK Low	–	325	ns
tCKHASL	$\overline{AS}$ Transition Delay	–	160	ns
tCKHASH	$\overline{AS}$ Transition Delay	–	185	ns
tCKLREL	$\overline{RE}$ Transition Delay	–	125	ns
tCKHREH	$\overline{RE}$ Transition Delay	–	190	ns
tRYLCKH	$\overline{READY}$ Set-Up Time	70	–	ns
tWELDV	Data Set-Up Time	–	tCKHCKLMIN	–

Symbol	Description	Min	Max	Unit
	DMA Read Cycle (Figure 15)			
tRYLDX	Data Hold Time	0	–	ns
tWELCKH	$\overline{WE}$ Set-Up Time for Ready Wait Propagation	140	–	ns
tRYLWEH	$\overline{WE}$ Hold Time	0	–	ns
tCKHRYL	Ready Wait Propagation Time	3tCKHCKH+ tCKLRYL	13.5tCKHCKH tCKLRYL	–
tCKLRYL	$\overline{READY}$ Transition Delay	0	265	ns
tWEHRYH	$\overline{READY}$ Hold Time After $\overline{WE}$ Goes High	245	–	ns
tWEHWEL	Interoperation Delay Time	tCKHCKH	–	–
tCSHRYX	$\overline{READY}$ Hold Time After $\overline{CS}$ Goes High	0	50	ns
tCKLDRL	$\overline{DREQ}$ Transition Delay	–	265	ns
tCKHDRH	$\overline{DREQ}$ Transition Delay	–	175	ns
tDALCKL	$\overline{DACK}$ Set-Up Time	160	–	ns
tDRHDAH	$\overline{DACK}$ Response Time to Removal of $\overline{DREQ}$ DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH –	 – ns
tDALRWV	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ Delay Time from $\overline{DACK}$ Low	–	200	ns
tCKLAV	Address Valid Delay Time from CLK Low	–	325	ns
tCKHASL	$\overline{AS}$ Transition Delay	–	160	ns
tCKHASH	$\overline{AS}$ Transition Delay	–	185	ns
tCKLREL	$\overline{RE}$ Transition Delay	–	125	ns
tCKHREH	$\overline{RE}$ Transition Delay	–	190	ns
tCKLRYH	$\overline{READY}$ Hold Time	50	–	ns
tDVCKL	Data Set-Up Time Without Parity With Parity	 50 120	 – –	 ns ns
tCKHDX	Data Hold Time	130	–	ns
tRELREH	Minimum Read Strobe	1.5tCKHCKH	–	–
tCKHRWZ	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ Hold Time	0	220	ns
tCKHAZ	Address Hold Time	0	290	ns
tCKHASZ	$\overline{AS}$ Hold Time	0	220	ns

Symbol	Description	Min	Max	Unit	
DMA Read Cycle (Figure 15)					
tCKHREZ	$\overline{RE}$ Hold Time	0	220	ns	
DMA Multiple Byte Read Operation (Figure 16)					
tASHASL	Address Transition and Set-Up Time	–	tCKHCKH	–	–
tREHREL	Delay Time Between Read Operations	–	1.5tCKHCKH	–	–
tCKLDRH*	DMA Bus Access Time DBC = 0 DBC = 1	 4.5tCKHCKH** 4.5tCKHCKH**	 – –	 19.5tCKHCKH† 10.5tCKHCKH††	 – –

*No parity errors and no wait states generated
**1-byte or word read
†6-byte read
††3-word read

Symbol	Description	Min	Max	Unit
DMA Write Cycle (Figure 17)				
tCKLDRL	$\overline{DREQ}$ Transition Delay	–	265	ns
tCKHDRH	$\overline{DREQ}$ Transition Delay	–	175	ns
tDALCKL	$\overline{DACK}$ Set-Up Time	140	–	ns
tDRHDAH	$\overline{DACK}$ Response Time to Removal of $\overline{DREQ}$ DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH –	 – ns
tDALRWV	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ Delay Time from $\overline{DACK}$ Low	–	200	ns
tCKLAV	Address Valid Delay Time from CLK Low	–	325	ns
tCKASL	$\overline{AS}$ Transition Delay	–	160	ns
tCKHASH	$\overline{AS}$ Transition Delay	–	185	ns
tCKLWEL	$\overline{WE}$ Transition Delay	–	135	ns
tCKLWEH	$\overline{WE}$ Transition Delay	–	180	ns
tRYLCKL	$\overline{READY}$ Set-Up Time	35	–	ns
tCKLRYH	$\overline{READY}$ Hold Time	60	–	ns
tCKLDV	Data Valid Delay Time	–	260	ns
tCKLDX	Data Hold Time	tCKHCKH	–	–
tWELWEH	Minimum Write Strobe	tCKHCKH	–	–
tCKHRWZ	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ Hold Time	0	220	ns
tCKHAZ	Address Hold Time	0	290	ns
tCKHASZ	$\overline{AS}$ Hold Time	0	220	ns

Symbol	Description	Min	Max	Unit
	DMA Write Cycle (Figure 17)			
tCKHWEZ	$\overline{WE}$ Hold Time	0	220	ns
tCKHDZ	Data Time to 3-State	–	0	ns
	DMA Multiple Write Operation (Figure 18)			
tCKLBEH	$\overline{BHE}/\overline{BLE}$ Transition Delay	–	210	ns
tASHASL	Address Transition and Set-Up Time	tCKHCKH	2tCKHCKH	–
tWEHWEL	Delay Time Between Write Operations	2tCKHCKH	3tCKHCKH	–
tCKLDRH*	DMA Bus Access Time			
	DBC = 0	4.5tCKHCKH**	11.5tCKHCKH†	–
	DBC = 1	4.5tCKHCKH**	8.5tCKHCKH††	–

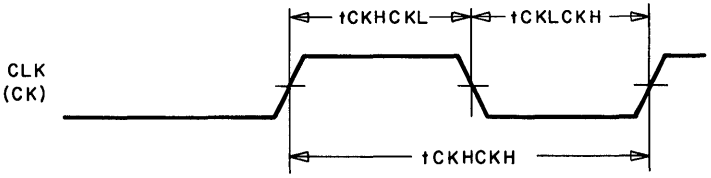
*No parity errors and no wait states generated
**1-byte or word write
†3-byte write
††2-word write

Symbol	Description	Min	Typ	Max	Unit
	Transmit Element Acknowledgement (Figure 19)				
tCKLDRH	DMA Bus Access Time*	–	8.5tCKHCKH	–	–
tCKLRWL	R/$\overline{W}$ Transition Delay	0	–	160	ns
tASHASL	Address Transition and Set-Up Time	–	3tCKHCKH	–	–
tREHWEL	Interoperation Delay Time	–	3.5tCKHCKH	–	–

*No parity errors and no wait states generated

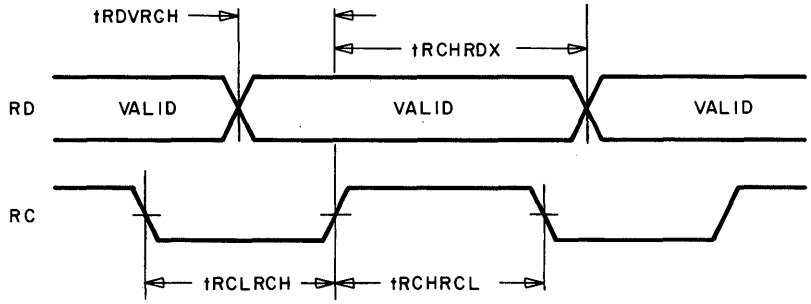
Symbol	Description	Min	Max	Unit
	DMA Daisy Chain Timing (Figure 20)			
tLDLCKL	$\overline{\text{LPDREQ}}$ Set-Up Time to be Sampled Low	70	—	ns
tCKLDRL	$\overline{\text{DREQ}}$ Transition Delay After $\overline{\text{LPDREQ}}$ is Sampled Low	—	265	ns
tDALPDL	$\overline{\text{PDACK}}$ Transition Delay After $\overline{\text{DACK}}$ Goes Low	—	170	ns
tLDHDRH	$\overline{\text{DREQ}}$ Transition Delay After $\overline{\text{LPDREQ}}$ Goes High	—	140	ns
DRQDEL=0 tLDHCKL	$\overline{\text{LPDREQ}}$ Set-Up Time to be Sampled High	75	—	ns
tCKLDRL	$\overline{\text{DREQ}}$ Transition Delay After $\overline{\text{LPDREQ}}$ is Sampled High and XPC is Requesting Bus Time	tCKHCKH	—	—
tCKLPDH	$\overline{\text{PDACK}}$ Transition Delay After $\overline{\text{LPDREQ}}$ is Sampled High	—	160	ns
tCKLDRL	Delay Time Between XPC Relinquishing Bus and Requesting Bus Due to Lower Priority XPC	tCKHCKH	—	—
tDRHDAH	$\overline{\text{DACK}}$ Response Time to Removal of $\overline{\text{DREQ}}$	0	tCKHCKH	—
DRQDEL=1 tLDHPDH	$\overline{\text{PDACK}}$ Transition Delay After $\overline{\text{LPDREQ}}$ Goes High	—	410	ns
tDAHCKL	$\overline{\text{DACK}}$ Set-Up Time to be Sampled High	20	—	ns
tCKLDRL	$\overline{\text{DREQ}}$ Transition Delay After $\overline{\text{DACK}}$ is Sampled High	—	220	ns
	Interrupt Timing (Figure 21)			
tCKLINTL	Interrupt Transition Delay	0	140	ns
tREHINTH	Interrupt Transition Delay	0	150	ns
tINTHINTL	Time Before Next Interrupt	1.5tCKHCKH	—	—
	Reset Timing (Figure 22)			
tCKLMRL	Time Before Asserting $\overline{\text{MR}}$ after Power-On	2tCKHCKH	—	—
tMRLMRH	Reset Pulse Width	1.5tCKHCKH	—	—

Timing Diagrams



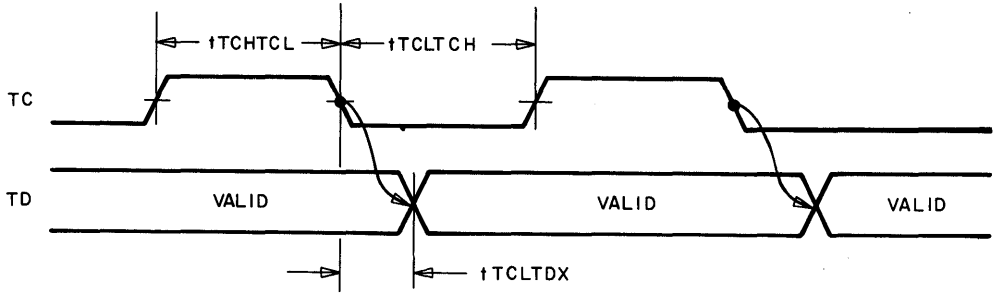
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 10. Clock Timing



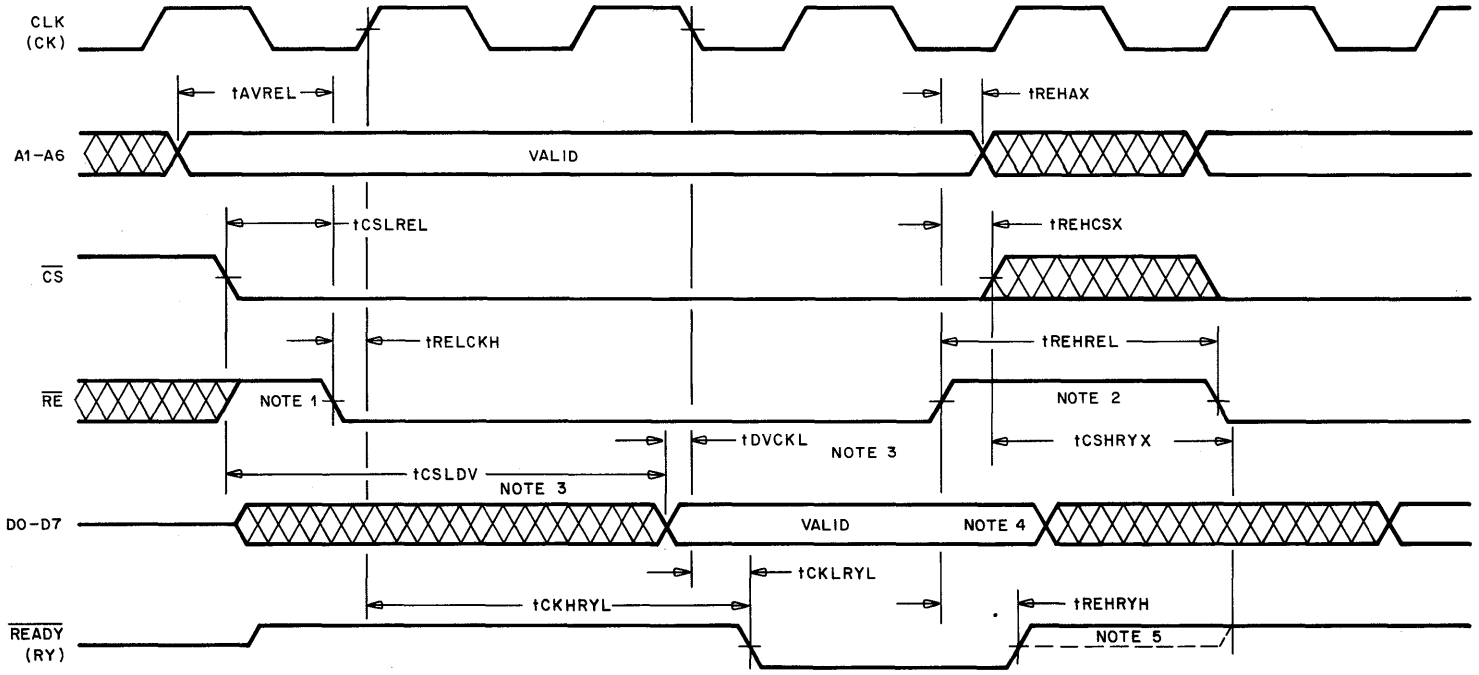
Notes: When in loopback modes and TC is tied to RC, the maximum delay on TD (tTCLTDX) meets the minimum RD set-up time (tRDVRCH) up to the maximum fTC = 6fCLK and fRC = 6fCLK.
Refer to page following Figure 22 for timing diagram notes.

Figure 11. Receive Clock Timing



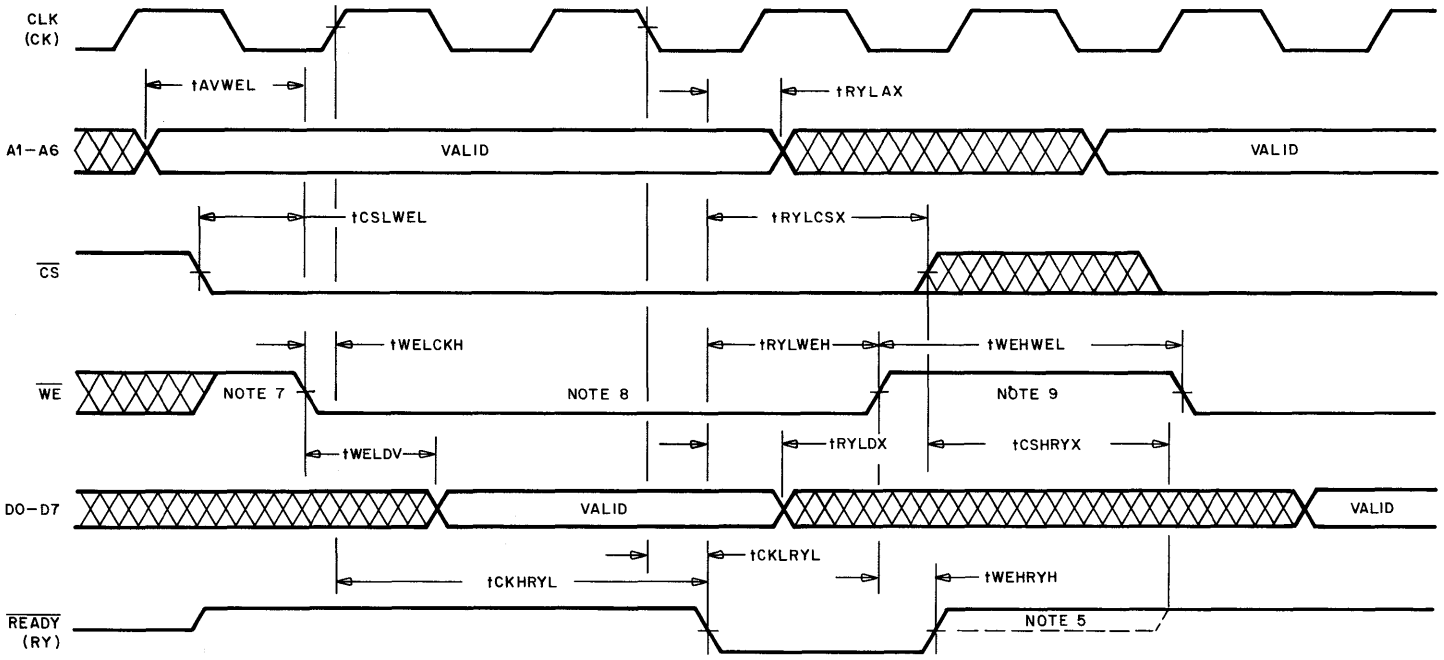
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 12. Transmit Clock Timing



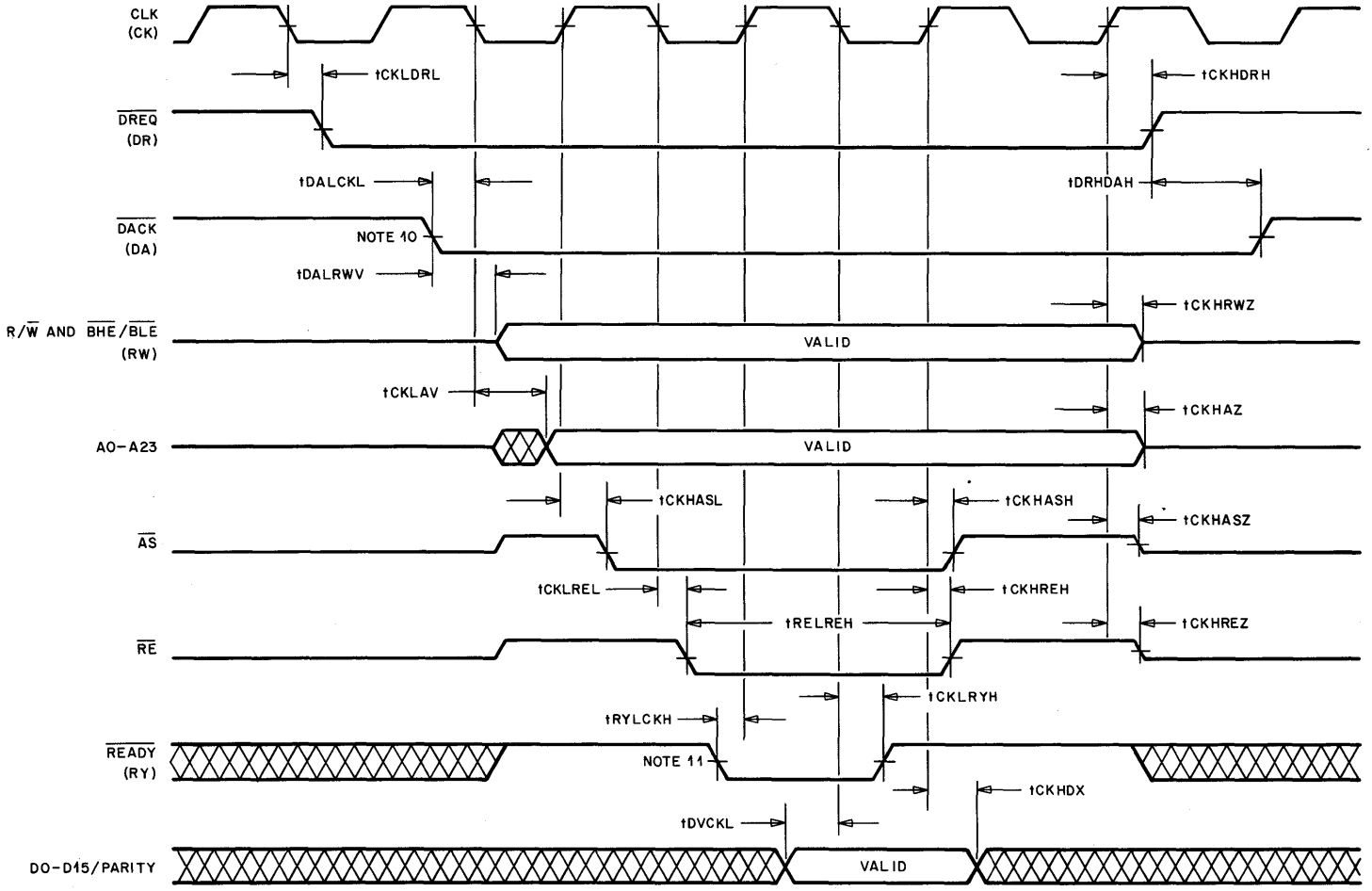
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 13. Reading XPC Registers



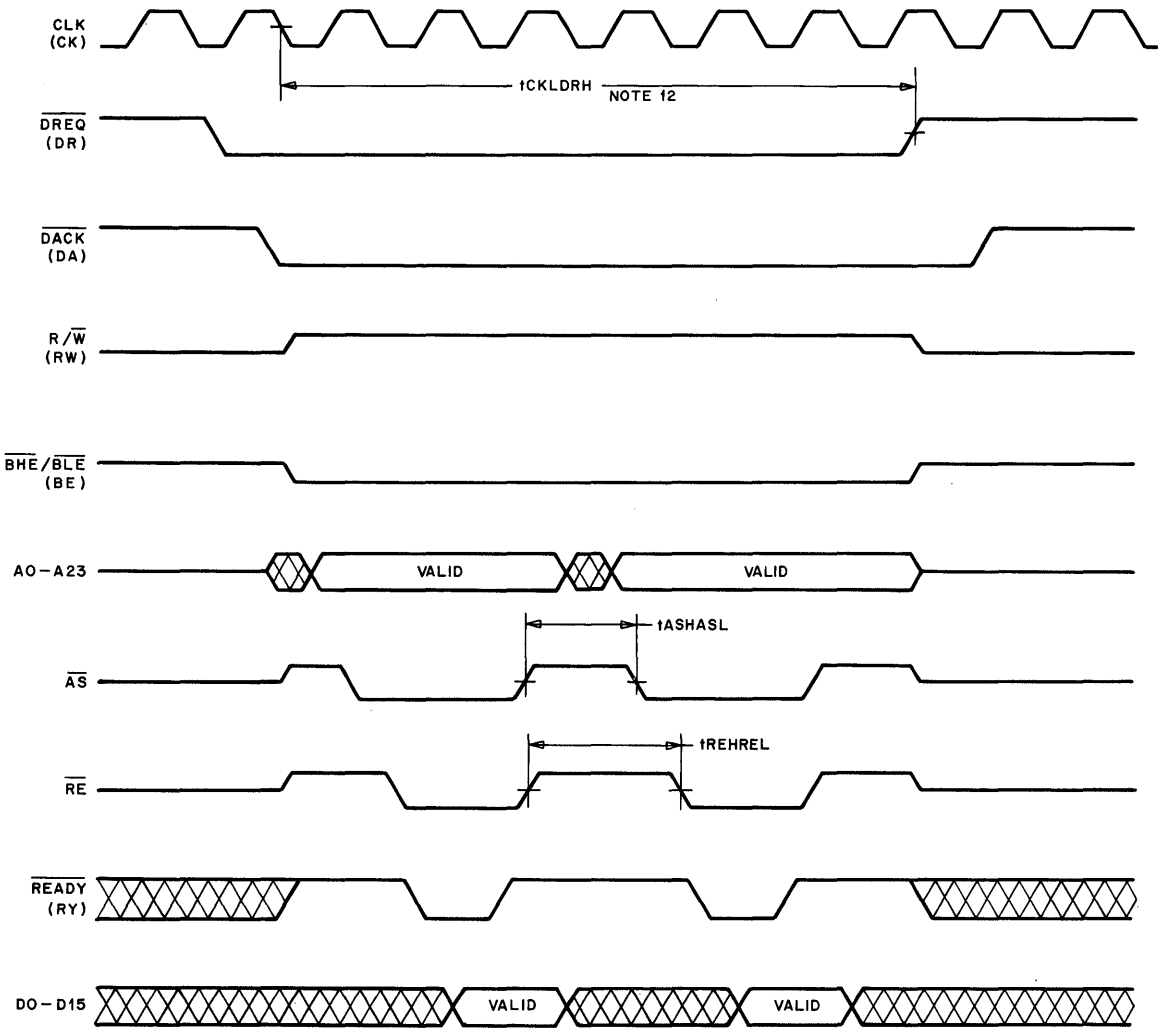
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 14. Writing XPC Registers



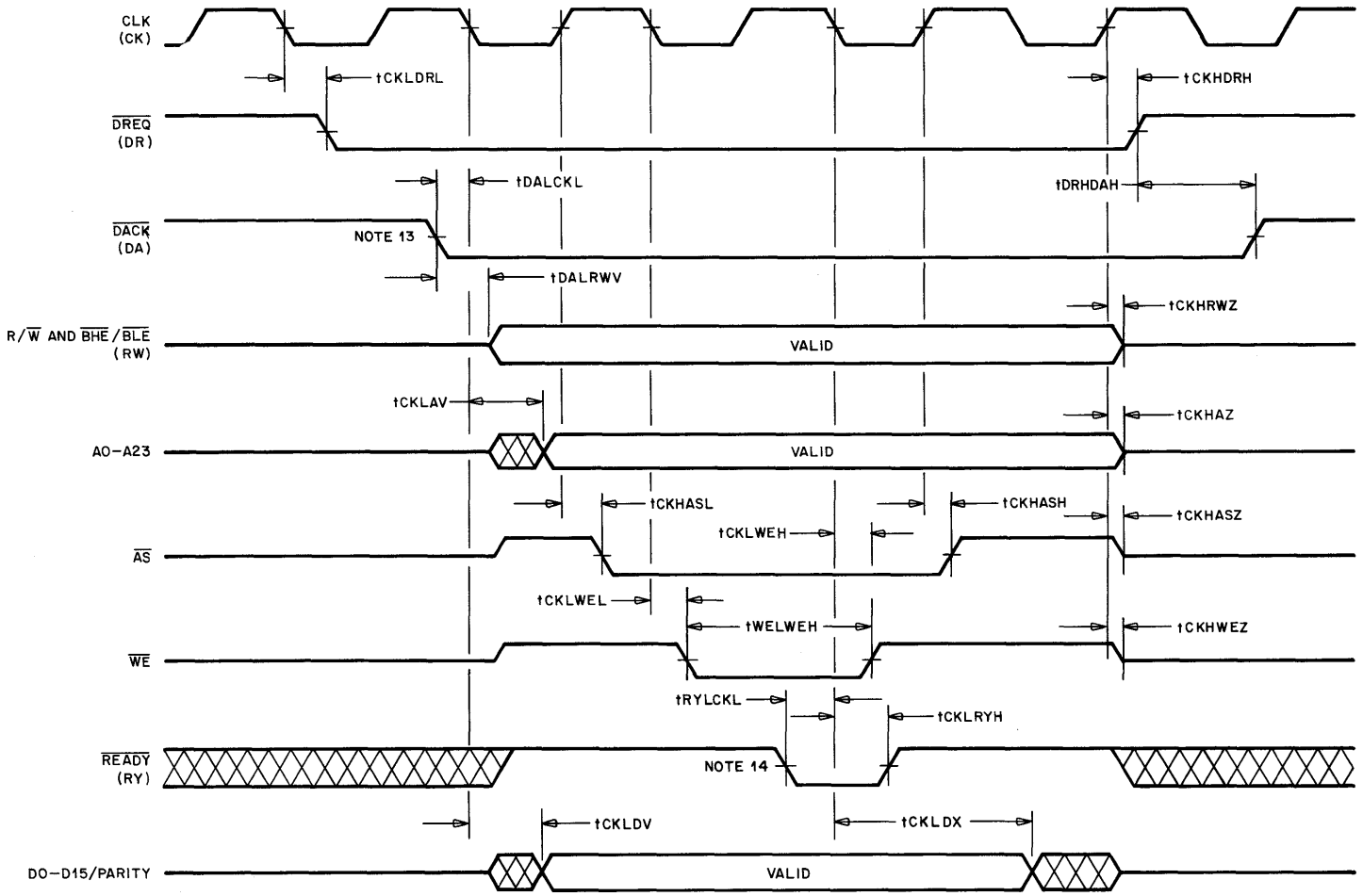
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 15. DMA Read Cycle



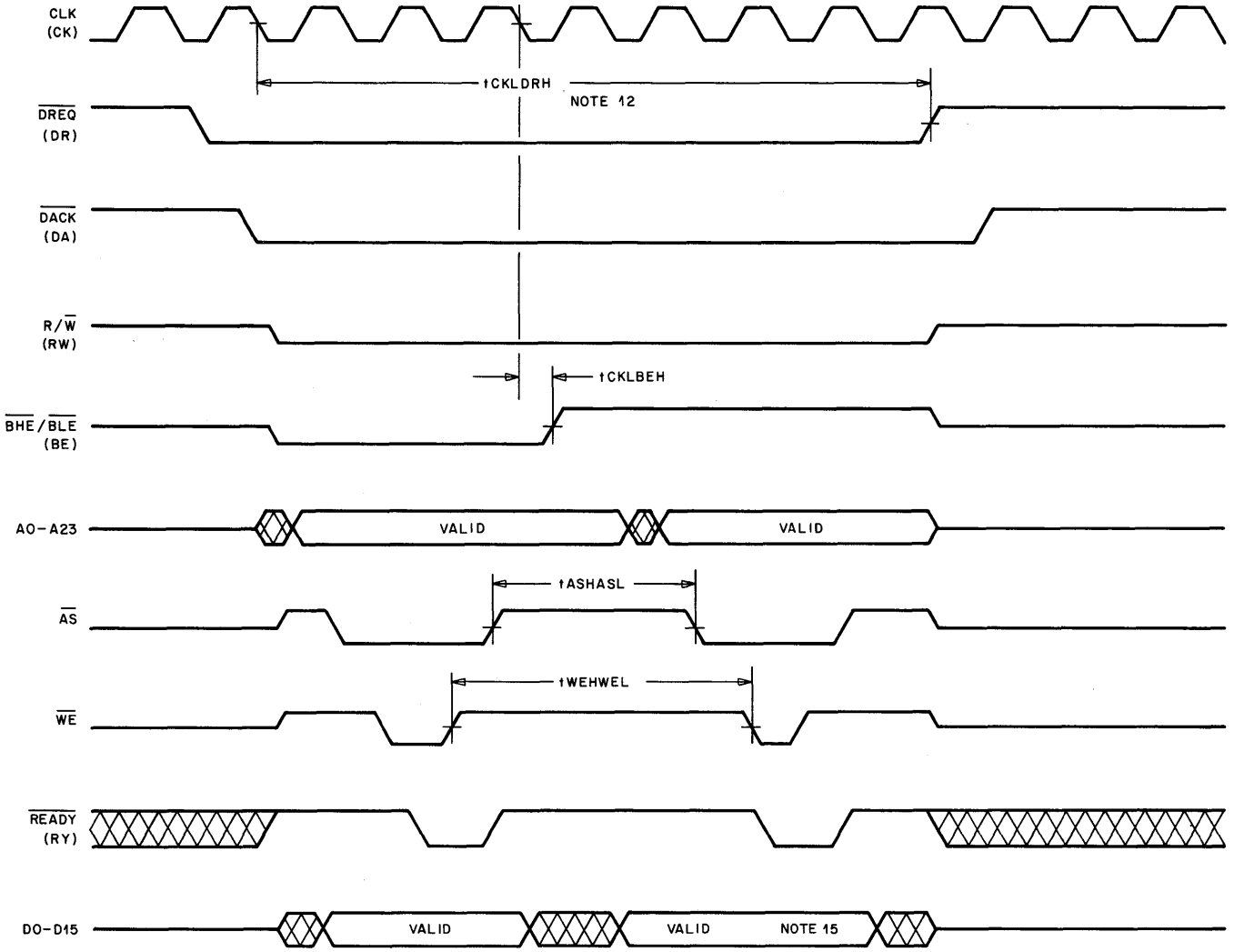
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 16. DMA Multiple Byte Read Operation



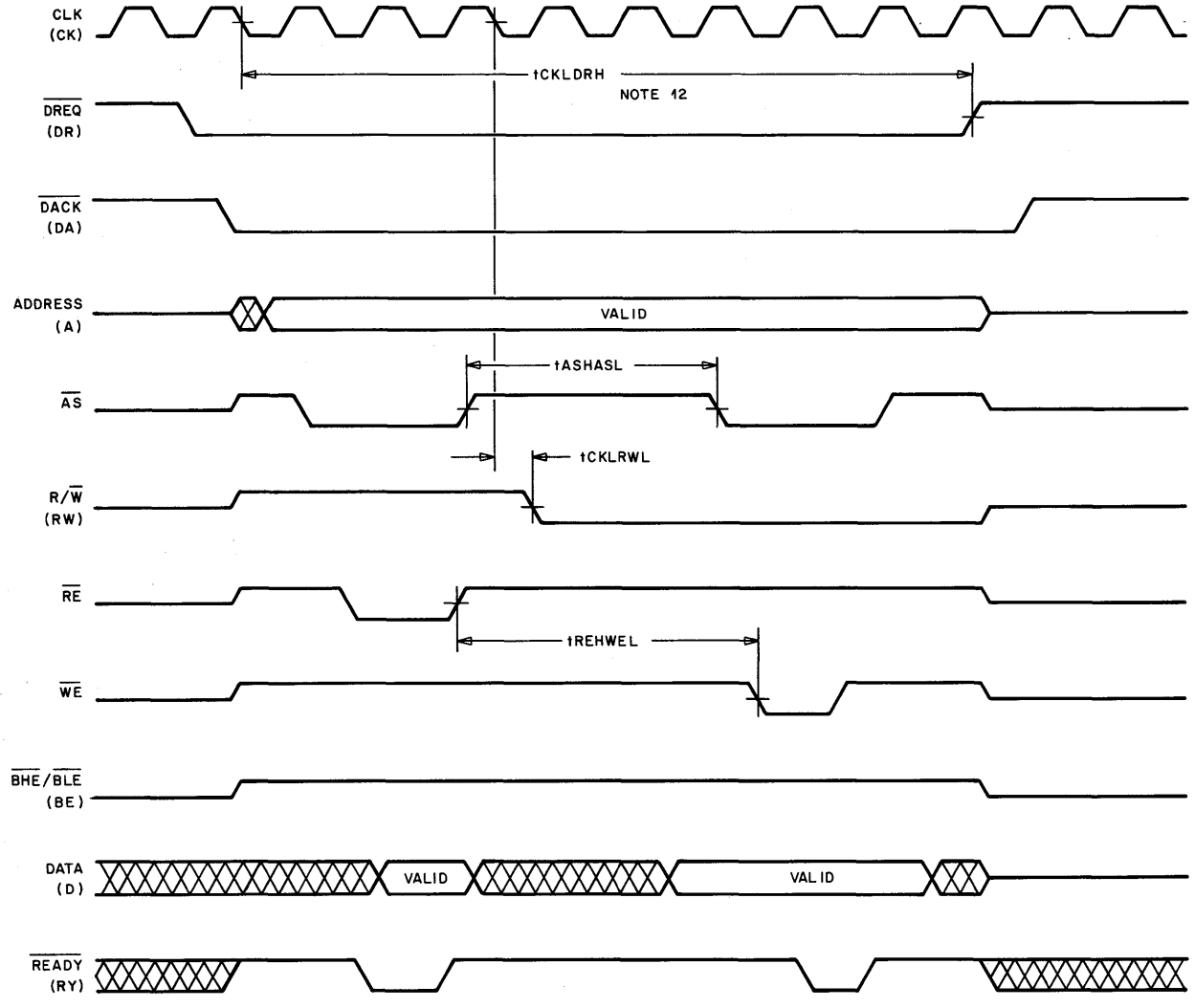
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 17. DMA Write Cycle



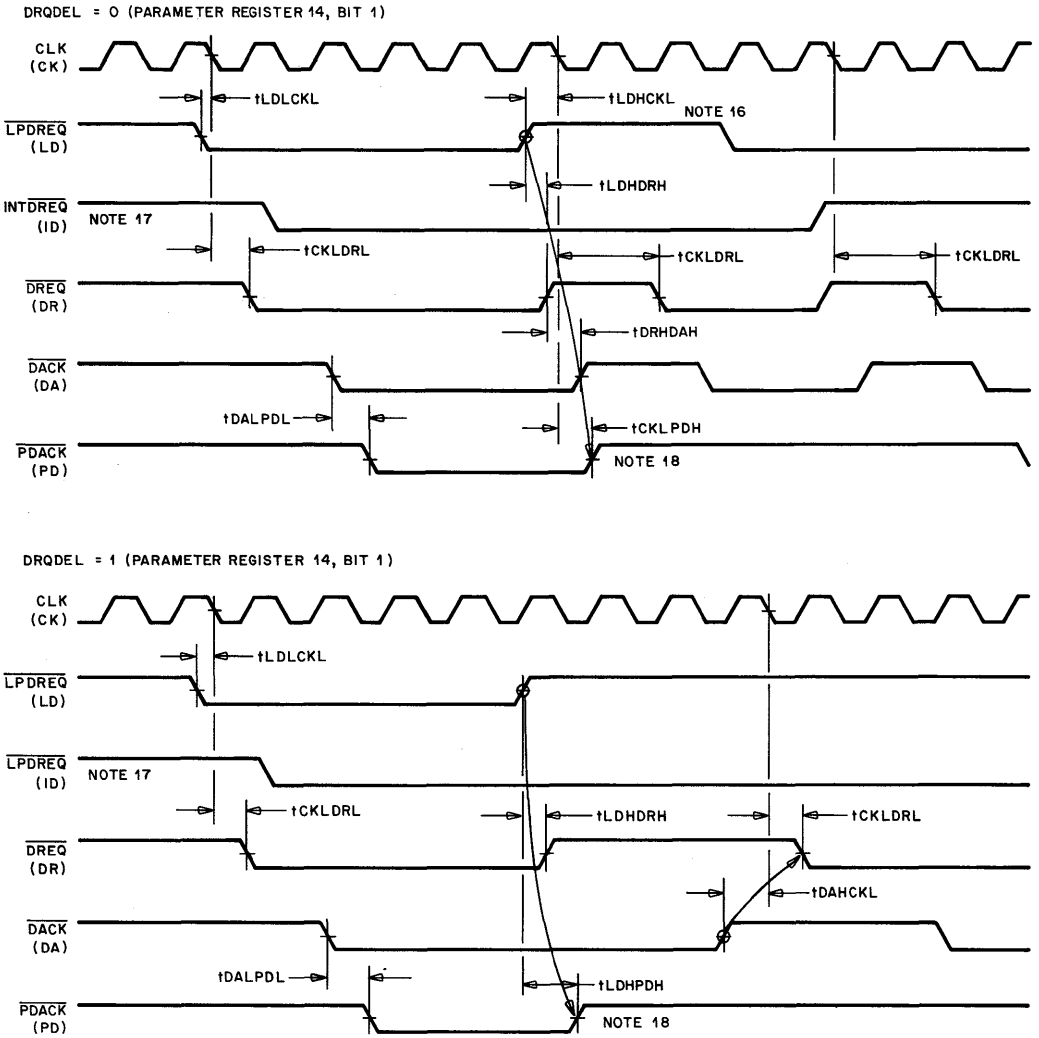
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 18. DMA Multiple Byte Write Operation



Note: Refer to page following Figure 22 for timing diagram notes.

Figure 19. Transmit Element Acknowledgement (Read-Modify-Write)



Note: Refer to page following Figure 22 for timing diagram notes.

Figure 20. DMA Daisy Chain Timing Between Any 2 XPC Devices

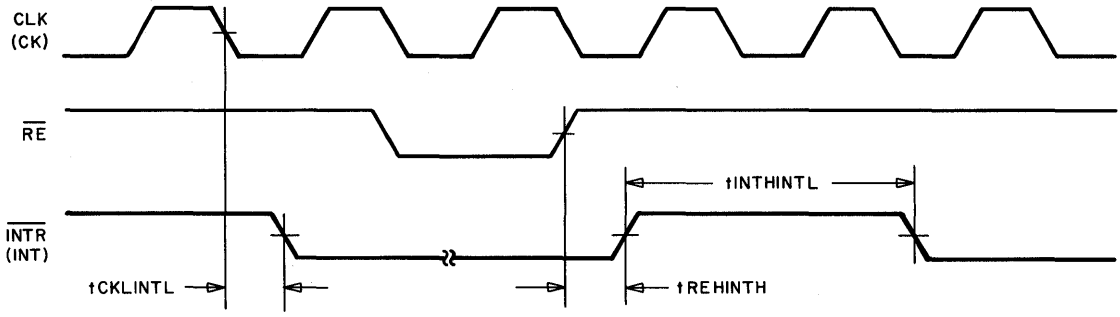


Figure 21. Interrupt Timing

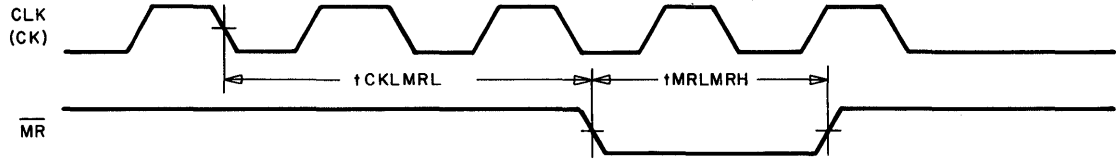


Figure 22. Reset Timing

Notes:

1. $\overline{RE}$ is sampled on the rising edge of CLK. Ready wait propagation does not begin unti $\overline{RE}$ is sampled low.
2. tREHREL is also the minimum time before a write can occur.
3. When reading nonevent counter registers, tCSLDV should be used. tDVCKL is the time before the clock edge on which $\overline{READY}$ goes low that the event counter data is valid. tDVCKL should be used only when reading event counter registers.
4. Data remains on the data bus until $\overline{RE}$ goes high or the address changes. Data can change while $\overline{READY}$ is low and should be latched externally with the $\overline{READY}$ signal.
5. If $\overline{CS}$ is high, the XPC does not drive the $\overline{READY}$ pin.
6. $\overline{CS}$ can go high or remain low during an interoperation period.
7. $\overline{WE}$ is sampled on the rising edge of CLK. Ready wait propagation does not being until $\overline{WE}$ is sampled low.
8. Register is written some time within $\overline{WE}$ low window.
9. tWEHWEL is also the minimum time before a read can occur.
10. $\overline{DACK}$ is sampled on the falling edge of CLK. The read cycle will not begin until $\overline{DACK}$ is sampled low.
11. $\overline{READY}$ is sampled on the rising edge of CLK. The DMA will enter a wait state until $\overline{READY}$ is sampled low.
12. tCKLDRH begins on the first falling edge of CLK after $\overline{DACK}$ is sampled low.
13. $\overline{DACK}$ is sampled on the falling edge of CLK. The write cycle will not begin until $\overline{DACK}$ is sampled low.
14. $\overline{READY}$ is sampled on the falling edge of CLK. The DMA will enter a wait state until $\overline{READY}$ is sampled low.
15. D8—D15 (Intel Mode — BYTORD = 0) or D0—D7 (Motorola Mode — BYTORD = 1) is not valid if $\overline{BHE}/\overline{BLE}$ is high.
16. $\overline{LPDREQ}$ is sampled on the falling edge of CLK. tCKLDRL is measured from the edge that $\overline{LPDREQ}$ is sampled high.
17. $\overline{INTDREQ}$ is the XPC internal DMA request. It is shown to illustrate the timing between 2 XPC devices.
18. Removal of $\overline{PDACK}$ is a function of $\overline{LPDREQ}$. $\overline{DACK}$ does not propagate from the CPU to remove $\overline{PDACK}$.

The information contained herein is preliminary and subject to change.

FEATURES

Host Interface Features

- Compatible with iAPX86, MC68000, or *WE* 32100 Microprocessor systems
- On-chip 16 channel DMA memory address generator with buffer manager and interrupt controller with a 4 Mbyte/s maximum data transfer rate
- Wait-state generator
- 16-bit data and 20-bit address buses
- Bus error handling
- Transmit and receive buffers accessible through memory-mapped look-up elements
- Parallel interrupts with full handshaking

Serial Interface Features

- 8-channel multiplexed serial input/output
- Automatic flag transmission and detection
- Zero bit insertion and deletion
- CRC generation and detection using CCITT-16 polynomial
- Abort/idle detection and transmission
- Detection of transmitter underrun and receiver overrun
- 2 Mb/s continuous serial data rate; 4.096 Mb/s maximum instantaneous data rate
- Up to 8 Kbytes per frame
- Programmable data inversion
- Near-end loop test and echo modes

DESCRIPTION

The T7110 Synchronous Protocol Data Formatter With Serial Interface (SPYDER-S) integrated circuit is a synchronous packet data communications controller device. It is used to interface data link level lines using bit-synchronous (HDLC/SDLC) protocols to 16-bit or 32-bit microprocessor systems. All inputs and outputs of the T7110 SPYDER-S are TTL-compatible. It is fabricated using CMOS technology, requires a single 5 V supply, and is available in a 68-pin chip carrier.

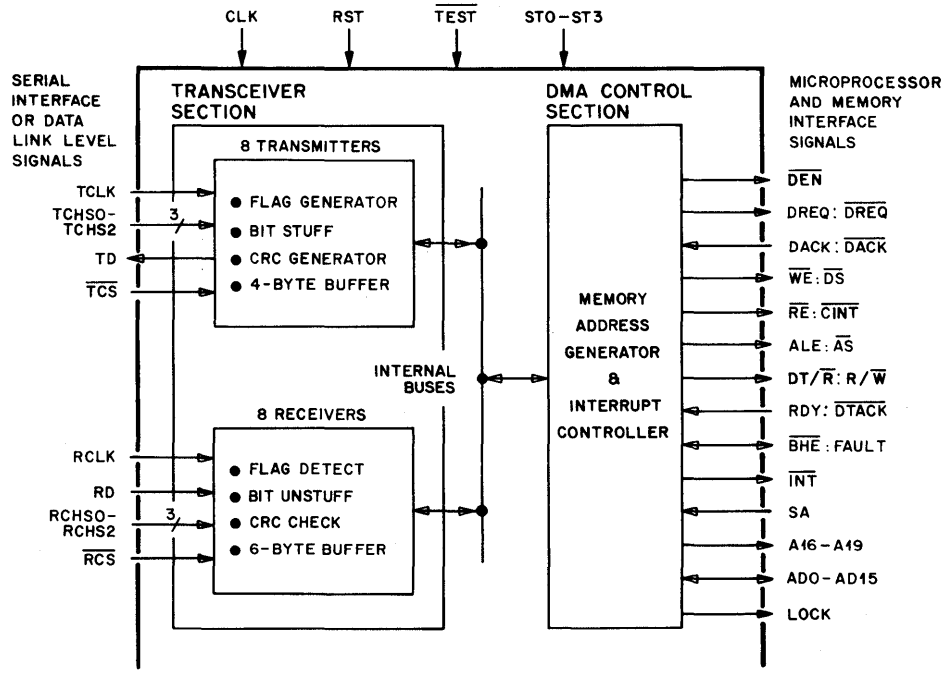


Figure 1. T7110 SPYDER-S Simplified Block Diagram

USER INFORMATION

Pin Descriptions

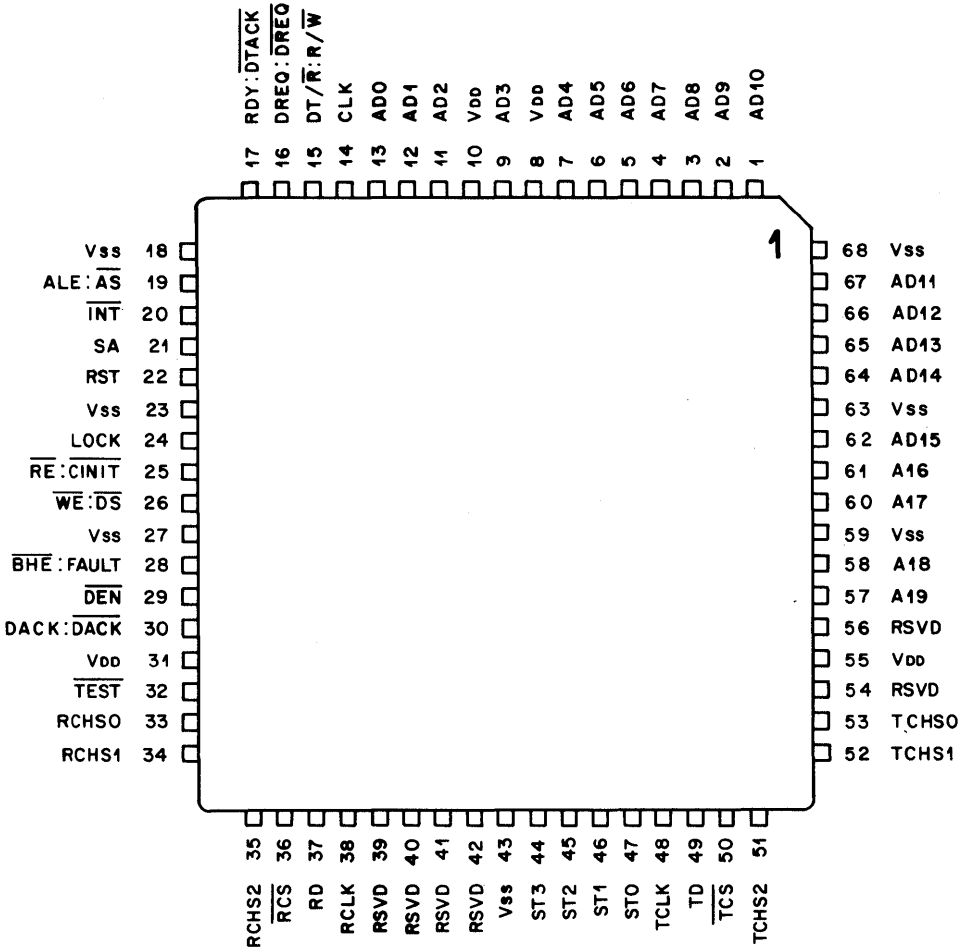


Figure 2. T7110 SPYDER-S Pin Function Diagram and Alphabetical Listing of Symbols (Part 1 of 2)

Symbol*	Pin(s)	Symbol*	Pin(s)
A16, A17	61, 60	RDY: $\overline{\text{DTACK}}$	17
A18, A19	58, 57	$\overline{\text{RE}}$: $\overline{\text{CINIT}}$	25
AD0–AD2	13–11	RST	22
AD3	9	RSVD	39–42, 54, 56
AD4–AD10	7–1	SA	21
AD11–AD14	67–64	ST0–ST3	47–44
AD15	62	TCH0–TCH2	53–51
ALE: $\overline{\text{AS}}$	19	TCLK	48
$\overline{\text{BHE}}$: FAULT	28	$\overline{\text{TCS}}$	50
CLK	14	TD	49
DACK: $\overline{\text{DACK}}$	30	$\overline{\text{TEST}}$	32
$\overline{\text{DEN}}$	29	VDD	8, 10, 31, 55
DREQ: $\overline{\text{DREQ}}$	16	VSS	18, 23, 27, 43
DT/$\overline{\text{R}}$: R/$\overline{\text{W}}$	15		59, 63, 68
$\overline{\text{INT}}$	20	$\overline{\text{WE}}$: $\overline{\text{DS}}$	26
LOCK	24		
RCHS0–RCHS2	33–35		
RCLK	38		
$\overline{\text{RCS}}$	36		
RD	37		

*A colon separates two symbol names which are defines per the microprocessor interface (modes M2, M3:M4 or iAPX86:MC68000/ *WE* 32100 CPU).

Figure 2. T7110 SPYDER-S Pin Function Diagram and Alphabetical Listing of Symbols (Part 2 of 2)

Table 1. T7110 Pin Descriptions

Pin	Symbol*	Type	Name/Function
1	AD10	I/O	**Address/Data Bus Bit 10.**
2	AD9		**Address/Data Bus Bit 9.**
3	AD8		**Address/Data Bus Bit 8.**
4	AD7		**Address/Data Bus Bit 7.**
5	AD6		**Address/Data Bus Bit 6.**
6	AD5		**Address/Data Bus Bit 5.**
7	AD4		**Address/Data Bus Bit 4.**
8	VDD	–	**5 V Supply.**
9	AD3	I/O	**Address/Data Bus Bit 3.**
10	VDD	–	**5 V Supply.**
11	AD2	I/O	**Address/Data Bus Bit 2.**
12	AD1		**Address/Data Bus Bit 1.**
13	AD0		**Address/Data Bus Bit 0.**
14	CLK	I	**Clock.** 8 MHz (max) input clock.

* A colon separates two symbol names which are defined per the microprocessor interface (modes M2, M3:M4 or APX86:MC68000/ *WE* 32100 CPU).

Table 1. T7110 Pin Descriptions (Continued)

Pin	Symbol*	Type	Name/Function
15	DT/$\overline{R}$:R/$\overline{W}$	O	**Data Transmit/Received: Read/Write.** In the M4 mode, this signal indicates whether a read or write operation is to occur. In modes M2 and M3, this signal is used to control the direction of data flow through data bus transceivers (e.g., the 8286 and 8287 transceivers). DT/$\overline{R}$ = VOH during a write. DT/$\overline{R}$ = VOL during a read.
16	DREQ:$\overline{DREQ}$	O	**DMA Request.** Indicates that the SPYDER-S requires the system bus for data transfer.**
17	RDY:$\overline{DTACK}$	I	**Ready:Data Acknowledge.** Indicates when data is valid. Double latched in modes M3 and M4; assumed synchronous in mode M2.
18	VSS	—	**Ground.**
19	ALE:$\overline{AS}$	O	**Address Latch Enable:Address Strobe.** In all modes, this signal indicates that a valid address is on the address/data bus.
20	$\overline{INT}$	O	**Interrupt Request.** Informs the host that an interrupt is pending.**
21	SA	I	**SPYDER Attention.** Informs the SPYDER-S that a host command is pending. SA should be at least two clock cycles wide.
22	RST	I	**Reset.** A positive pulse is used to reset the SPYDER-S. This pulse should be at least four clock cycles wide.
23	VSS	—	**Ground.**
24	LOCK	O	**Lock.** Indicates to the host not to access the bus; it will be asserted after the host has granted SPYDER-S the bus and is only used when accessing data buffer descriptors in the shared (SHR=1) mode.
25	$\overline{RE}$:$\overline{CINIT}$	O	**Read Enable:Cycle Initiate.** In modes M2 and M3, this signal indicates that data is to be read. In the M4 mode, this signal indicates that a data cycle is to begin.†
26	$\overline{WE}$:$\overline{DS}$	O	**Write Enable:Data Strobe.** In modes M2 and M3, this signal indicates that data is to be written. In mode M4, this signal indicates that data is valid on the data pins.†
27	VSS	—	**Ground.**
28	$\overline{BHE}$: FAULT	O: I	**Byte High Enable:Bus Fault.** In modes M2 and M3, this signal determines if data is to be enabled onto AD8—AD15. In mode M4, this signal indicates a bus fault.
29	$\overline{DEN}$	O	**Data Enable.** Provided as an output enable for bus transceivers (e.g., the 8286 and 8287 transceivers). It is asserted when there is valid data on the address/data bus.

* A colon separates two symbol names which are defined per the microprocessor interface (modes M2, M3:M4 or iAPX86:MC68000/*WE* 32100 CPU).

** This pin is in the High-Z state when $\overline{TEST}$ is asserted. It is driven high or low at all other times.

† This pin is in the High-Z state when $\overline{TEST}$ is asserted or when the SPYDER-S does not have the bus (DACK: $\overline{DACK}$ is negated). It is driven high or low at all other times.

Table 1. T7110 Pin Descriptions (Continued)

Pin	Symbol*	Type	Name/Function
30	DACK: $\overline{\text{DACK}}$	I	**DMA Acknowledge.** Indicates that the SPYDER-S has been granted the system bus.
31	V_{DD}	—	**5 V Supply.**
32	$\overline{\text{TEST}}$	I	All pins 3-state when this pin is active low.
35—33	RCHS2—RCHS0	I	**Receive Channel Selects 0—2.** RCHS2 RCHS1 RCHS0 Channel 0 0 0 0 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7
36	$\overline{\text{RCS}}$	I	**Receive Chip Select.** Indicates RCHS0—RCHS2 are valid.
37	RD	I	**Received Data.**
38	RCLK	I	**Receive Clock.**
39—42	—	Tie low	**Reserved.**
43	V_{SS}	—	**Ground.**
44—47	ST3—ST0	I	**Strap 3—0.** Strap options. ST3 ST2 Mode Description 0 0 Normal user mode 0 1 Reserved for 1 0 internal bus 1 1 monitoring mode ST1 ST0 Mode Microprocessor Interface 0 0 M1 Reserved 0 1 M2 iAPX86 Maxmode (synchronous) 1 0 M3 iAPX86 Minmode (asynchronous) 1 1 M4 MC68000/*WE* 32100 Microprocessor
48	TCLK	I	**Transmit Clock.**
49	TD	O	**Transmit Data.**
50	$\overline{\text{TCS}}$	I	**Transmit Chip Select.** Indicates TCHS0—TCHS2 are valid.

*A colon separates two symbol names which are defined per the microprocessor interface (modes M2, M3:M4 or iAPX86:MC68000/*WE* 32100 CPU).

Table 1. T7110 Pin Descriptions (Continued)

Pin	Symbol*	Type	Name/Function
51–53	TCHS2–TCHS0	–	**Transmit Channel Selects 0–2.** TCHS2 TCHS1 TCHS0 Channel 0 0 0 0 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7
54	–	Tie low	**Reserved.**
55	VDD	–	**5 V Supply.**
56	–	Tie low	**Reserved.**
57	A19	O	**Address Bus Bit 19.**
58	A18	O	**Address Bus Bit 18.**
59	VSS	–	**Ground.**
60	A17	O	**Address Bus Bit 17.**
61	A16	O	**Address Bus Bit 16.**
62	AD15	I/O	**Address/Data Bus Bit 15.**
63	VSS	–	**Ground.**
64	AD14	I/O	**Address/Data Bus Bit 14.**
65	AD13	I/O	**Address/Data Bus Bit 13.**
66	AD12	I/O	**Address/Data Bus Bit 12.**
67	AD11	I/O	**Address/Data Bus Bit 11.**
68	VSS	–	**Ground.**

* A colon separates two symbol names which are defined per the microprocessor interface (modes M2, M3:M4 or iAPX86:MC68000/*WE* 32100 CPU).

Overview

The SPYDER-S device acts as a coprocessor, handling the low-level formatting functions required for most bit synchronous (HDLC/SDLC type) protocols. A physical level line interface (such as the AT&T DS-1 chip set) is required to derive the SPYDER-S device data link level information from the physical layer (cables, etc.,) signals. It detects and inserts packet delimiters (flags), checks and generates error detection codes (CRC), and detects and transmits abort/idle sequences ensuring data transparency. Protocol specific tasks, such as flow control, are accomplished by a host processor. The SPYDER-S device and host processor exchange all commands and messages through shared areas in memory.

An on-chip 16-channel DMA memory address generator and buffer manager maintains linked lists of free and full buffers allowing data transfer without real-time host intervention.

The serial interface (data link side) can transmit or receive data at a rate equal to one-fourth the clock frequency. With a CLK of 8 MHz, the link side can be clocked at 2 MHz on the transmit as well as on the receive lines. A maximum instantaneous (burst) rate of up to 4.096 Mb/s can be sustained for 8 bits.

The host memory interface can accommodate a maximum data transfer rate of 4 Mbytes/s. This is possible if the CLK frequency is 8 MHz, no wait-states occur, and DACK and RDY are always asserted allowing each memory read or write of a word (2 bytes) to occur every bus cycle (equal to 4 clock cycles or 500 ns). Different interrupt conditions on each one of the eight bidirectional channels can be reported and acknowledged in parallel. All these features are coupled with the ability to interface with the iAPX86, MC68000, or *WE* 32100 Microprocessor series.

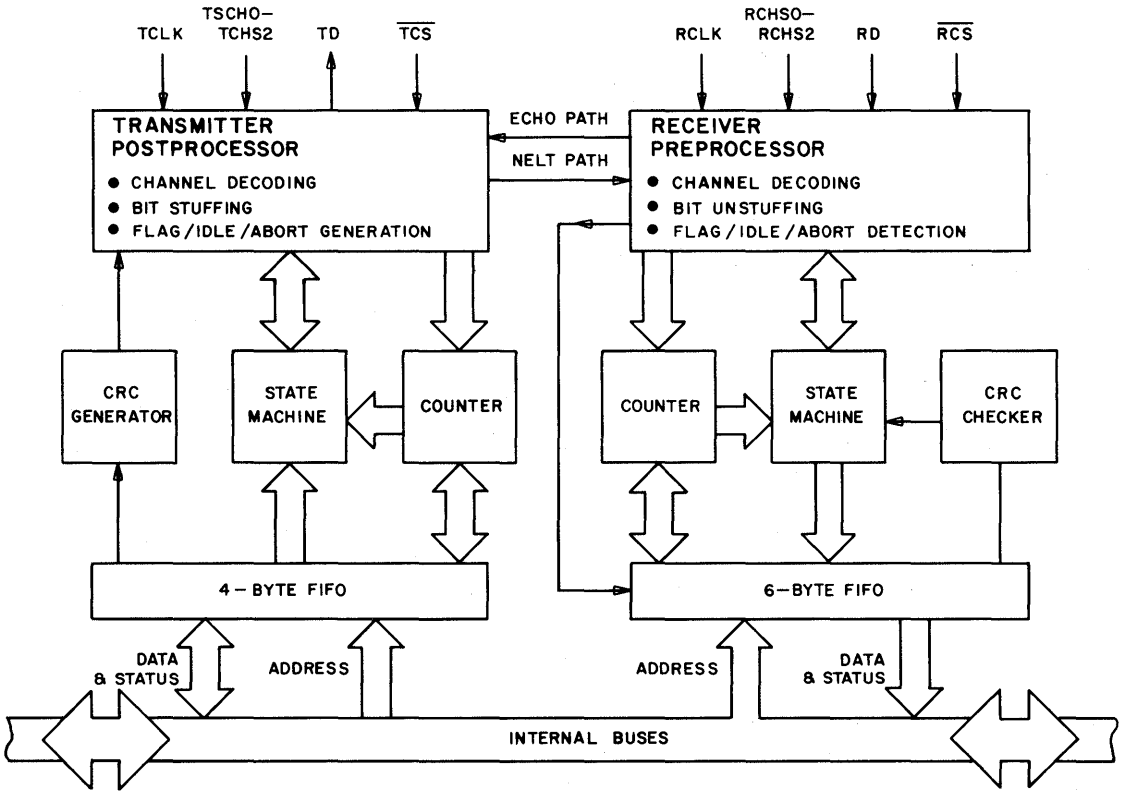


Figure 3. SPYDER-S Transceiver

The Serial Interface and the HDLC Transceivers

The SPYDER-S device has 8 transceivers (transmitters/receivers). The receivers receive time division multiplexed serial data, clocked in by RCLK, on the RD line. Using the receiver channel selects (RCHS2—0) and $\overline{RCS}$, the data is passed to the appropriate receiver. Similarly, one of the 8 transmitters is activated by providing a channel address (TCHS2—0) and asserting $\overline{TCS}$, thus clocking data onto TD at the TCLK rate.

The transceivers transmit/receive frames using the HDLC/SDLC format:

12345678*	12345678*	12345678*		16 ..... 1*	12345678*
Opening Flag	**Address**	**Control**	**Information**	**FCS**	**Closing Flag**
F**	A†	C†	I	CRC	F
01111110	8 bits	8 bits	≥ 0 bits	16 bits	01111110

*Order of bit transmission/reception
**1st byte transmitted/received
†In HDLC the A field can be extended to multiple bytes.
In HDLC the C field can be extended to 2 bytes.
In SDLC the A & C fields are always 1 byte.

As far as the SPYDER-S device is concerned, it can only recognize flags, idles, and aborts. The 16 bits preceding the closing flag are the CRC and the rest are data bits (the A, C, and I fields) which are either fetched from the host memory (for transmission) or stored in the host memory (when received) without further processing by the SPYDER-S device.

Zero Bit Insertion/Deletion (Bit Stuffing/Unstuffing) and Data Transparency

Bit stuffing is performed only on the A, C, I (collectively referred to as the data field), and CRC fields of the frame. Whenever five 1s occur between flags, a zero bit is automatically inserted after the fifth one, regardless of the next bit. On the receive side, if five successive 1s are detected followed by a zero, the zero is assumed to have been inserted and will be deleted (bit unstuffing). Note that a transmitted data field never contains any characters which are defined to assist the transmission protocol such as flags (01111110), aborts (01111111), or idles (11111111), all of which contain a pattern consisting of five 1s followed by at least another one. This allows the data to pass through transparently (with bit unstuffing) and only the flags, aborts, and idles are screened by the receiver. This property is referred to as data transparency (or code transparency) and is made possible by zero bit insertion/ deletion.

Flags

All flags have the binary configurations 01111110 (0x7E) and are used for frame synchronization. They can also be used as time fill characters between frames. It is possible to have the closing flag of one frame be the opening flag of the next frame (flag sharing).

The receiver recognizes the 01111110 pattern as a flag. Two successive flags may or may not share the intermediate zero bit and are identified as two flags (i.e., both 011111101111110 and 01111110011111110 are acceptable). The received data bytes are stored in the 6 byte receiver FIFO. When another flag is identified, it is treated as the closing flag. The last 2 bytes are cleared from the FIFO since they are assumed to be the CRC. Recall that a 01111110 sequence in the A, C, I, or FCS fields is prevented by zero bit insertion and deletion.

When data is fetched from the host memory for transmission, the transmitter in the SPYDER-S device automatically generates an opening flag before the first bit is transmitted. Similarly, when the last data byte is acquired from the last buffer for a frame, a closing flag will be appended to the frame after the CRC. A number of flags equal to FCNT will then be transmitted. Whenever n flags occur, 8n bits will be sent. The flags will not share the intermediate 0 bits even though the SPYDER-S device receivers are capable of recognizing such a stream of consecutive flags.

Aborts

The binary configuration of the abort character is 01111111 (0x7F). If a HALT channel command is issued, the transmitter will finish shifting out the current data byte and then transmit the abort sequence with no CRC being sent.

The action taken by the transmitter after the abort depends on whether the other bits are set or cleared in the channel command word. The SPYDER-S device sets the ABT status bit in the transmit frame descriptor (TFD) of the aborted frame.

The receiver recognizes the abort sequence whenever it receives seven consecutive 1s. It will result in the abort bit being set in the status byte of the receive frame descriptor (RFD). The receiver FIFO and the CRC generator will also be cleared. However, if an ABT is received with less than three complete bytes in the FIFO, the ABT bit will not be set and the current frame is ignored since none of the data bytes were ever written into a data buffer. If three or more bytes are in the receiver FIFO, as well as data from the previous frame, when an ABORT is received, then only the second frame is lost and the LLI is issued (if not masked).

Idles

The idle character has the binary configuration 11111111 (0xFF) and is an alternative time fill character to the flag. Note that even if idles are being sent between frames, there will still be an opening and closing flag to delimit the frame.

A channel's TFD can be set up so that it transmits idles between frames or can command a channel to idle whenever a frame is not being sent.

If the receiver begins to receive idles instead of flags, then the status change (STC) interrupt as well as the IDLE status bit are both set in the first word of the CCB of that particular channel. If the SPYDER-S device begins receiving flags instead of idles then the STC interrupt bit will be set and the IDL bit will be cleared in the appropriate channel control block. Note that an idle condition is reported when fifteen or more consecutive 1s have been detected.

ECHO and NELT Modes

In the echo mode, all received bits are retransmitted and the channel does not perform any processing on the data, nor does it report data to the host.

In the near-end loop test (NELT) mode, whatever is transmitted onto the TD line is also looped back internally to the receiver. This can be used, for example, to verify the CRC generator/checker.

Transmitter Underrun

An underrun occurs when the transmitter has transmitted all the bytes that were in its 4 byte FIFO, but the frame is not yet complete. Thus, at the conclusion of the last valid byte that was transmitted for this channel, an abort sequence (01111111) will be transmitted, followed by flags or idles (based on the IDL bit in the TFD). A UNR interrupt will also be issued if not masked and the UNR status bit is set in the TFD.

Receiver Overrun

This occurs if the 6 byte limit of the receiver FIFO is exceeded, i.e., data has been received faster than it has been read out of the receiver and written to the host memory. If the SPYDER-S device has not internally read the overrun status from a receiver before a new frame is completed, then the SPYDER-S device will report an LLI interrupt to the host.

Memory Interface

The SPYDER-S/host memory interface has a format compatible with general-trade Local Area Network (LAN) controllers. Table 2 provides a summary of the memory descriptors. The overall scheme of descriptors and buffers is illustrated on Figure 4. For all descriptors, the descriptor address must lie on a power-of-two (word) boundary. For example, eight byte descriptors occur every four locations (8 bytes or four words) and have 0s for the lower three bits of their address.

The **SPYDER Configuration Pointer** (SCP), address 0xFFFFC, points to the intermediate SPYDER control block, which provides initialization information for the entire SPYDER-S device. Table 3 shows the bit assignments of the SCP.

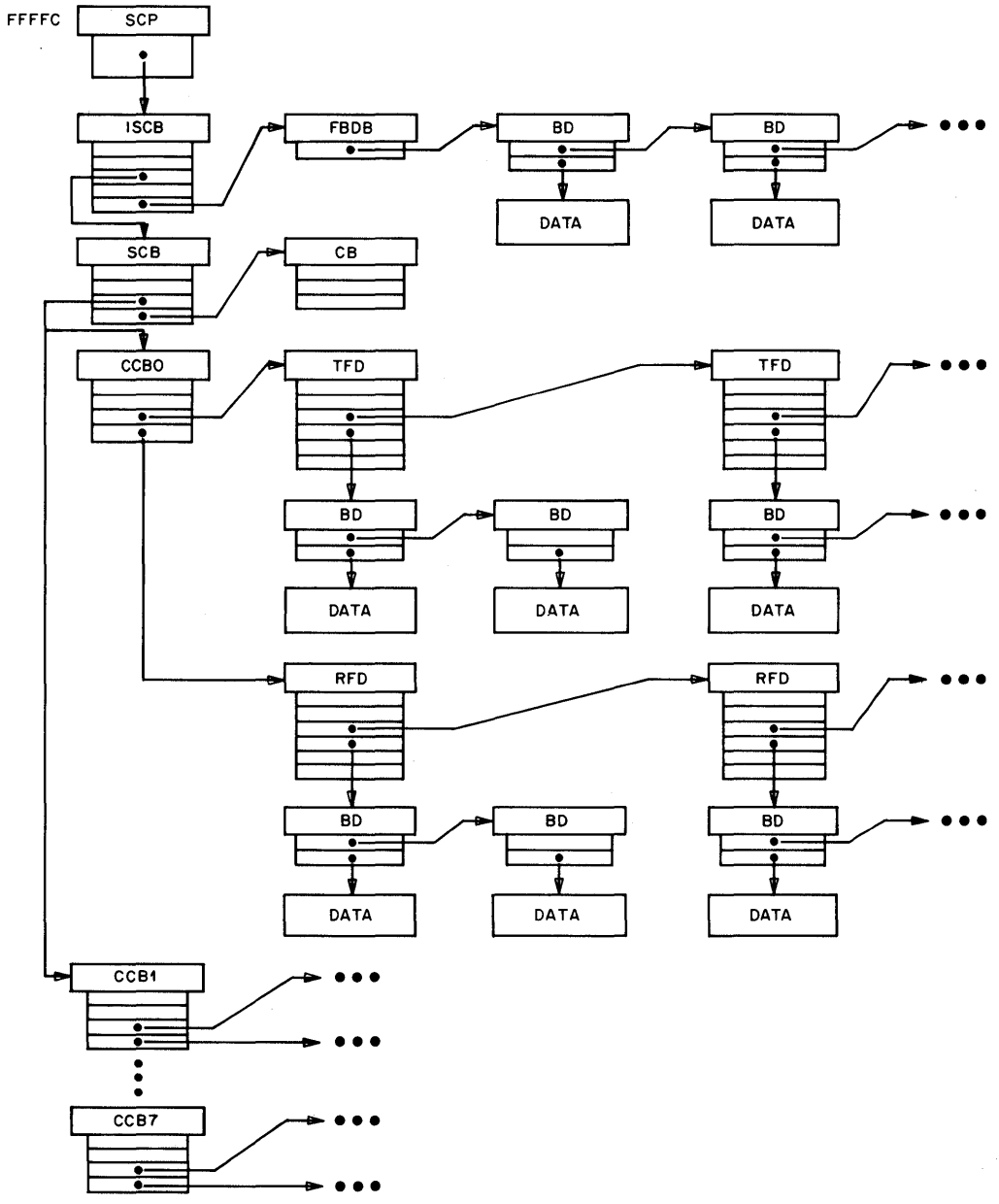
The **Intermediate SPYDER Control Block** (ISCB) must lie on 16-byte boundaries (ISCB address bits A3—A0 are 0s). Table 4 shows the ISCB bit assignments. BUSY indicates to the host that the SPYDER-S device is being initialized. This bit is set by the host and reset by the SPYDER-S device when it has read the SPYDER control block (SCB) base and offset addresses. The configuration is not completed at the point when SPYDER-S device clears BUSY; this merely indicates that SPYDER-S device has finished accessing the SCP and ISCB descriptor, which may be common to several SPYDER-S device devices in a system. The SPYDER-S device never reads BUSY and is provided as a maintenance feature to the host. The SCB offset address is the offset portion of the SCB address, which must lie on an 8-byte boundary (A0—A2 are 0s). The third word of ISCB must be zero. The **Free Buffer Descriptor Block** (FBDB) offset address specifies the free buffer descriptor block address offset. The FBDB specifies the next free buffer descriptor (NFBD) offset address (see Table 5). If the buffer contains 0xFFFF, there are no free buffers on the buffer list.

Table 2. Summary of SPYDER-S Memory Descriptors

Number per SPYDER-S	Number of Locations (16-Bit Words)	Name/Function
1	2	**SPYDER Configuration Pointer (SCP).** SCP is located at address location 0xFFFFC. This 20-bit address points to the start of the intermediate SPYDER control block.
1	5	**Intermediate SPYDER Control Block (ISCB).** This descriptor provides addresses to the SPYDER control block, free buffer descriptor block, and the four most significant bits of the base address of all descriptors. Only one ISCB needs to be present in a system of SPYDER-S devices, although one ISCB can be assigned per SPYDER-S.

Table 2. Summary of SPYDER-S Memory Descriptors (Continued)		
Number per SPYDER-S	Number of Locations (16-Bit Words)	Name/Function
1	1	**Free Buffer Descriptor Block (FBDB).*** This is the address of the next free buffer descriptor on the free buffer list. The last buffer descriptor on the list points to 0xFFFF as the next buffer descriptor and may not be used.
1	4	**SPYDER Control Block (SCB).*** This provides interrupt/acknowledge pointers to all channels, a global command, and a pointer to the configuration and channel control blocks.
1	3	**Configuration Block (CB).*** CB provides both global and channel set-up parameters.
8	4	**Channel Control Block (CCB).*** CCB provides channel interrupt/acknowledge information, channel commands, and transmit/receive frame descriptor queue pointers.
8+	6	**Transmit Frame Descriptor (TFD).*** This descriptor gives the address of the first data buffer descriptor and the next TFD, while providing transmit buffer allocation control. The number of TFDs in a system depends on the size of the user's queue for each channel. Initial frame bytes (such as address and control words) may be written to this descriptor to save data buffer accesses on supervisory frames. In this case, the host would specify whether the current frame is supervisory and how many bytes are in the TFD, up to a maximum of 4 bytes.
8+	6	**Receive Frame Descriptor (RFD).*** This descriptor gives the address of the first data buffer descriptor and the next RFD, while providing buffer allocation control. Initial frame bytes may be read by the host and written by the SPYDER-S in the RFD. In this case, the SPYDER-S would specify whether the current frame is supervisory and how many bytes have been written in the RFD, up to a maximum of 4 bytes.
8+	4	**Transmit Buffer Descriptor (TBD).*** TBD provides the 20-bit address of the data buffer, buffer control, chaining, and a count of the number of bytes to be transmitted from this buffer.
8+	4	**Receive Buffer Descriptor (RBD).*** RBD provides the 20-bit starting address of the data buffer, buffer control, chaining, and a count of the number of bytes in the buffer. The SPYDER-S may then write up to this number of bytes from the received frame before fetching a new RBD.

*The most significant 4 bits of the 20-bit address of the location where this block/descriptor resides are specified in the fourth word of the ISCB. This is the same as the high 4 bits of the SCB address; all descriptors for a SPYDER-S lie on this 64 kbyte page of memory.



SCP – SPYDER Configuration Pointer
ISCB – Intermediate SPYDER Control Block
FBDB – Free Buffer Descriptor Block
SCB – SPYDER Control Block
CCB – Channel Control Block
CB – Configuration Buffer
TFD – Transmit Frame Descriptor
RFD – Receive Frame Descriptor
BD – Buffer Descriptor

Figure 4. SPYDER-S Memory-Mapped Buffers and Descriptors Scheme

Table 3. SPYDER Configuration Pointer (SCP)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISCB Address (Low 16 bits)															
Reserved												(High 4 bits)			

Table 4. Intermediate SPYDER Control Block (ISCB)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Busy
SCB Address (Low 16 Bits)															
Reserved – Must Be Zero															
Reserved												SCB Address (High 4 bits)			
FBDB Offset Address															

Table 5. Free Buffer Descriptor Block (FBDB)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Next Free Buffer Descriptor (NFBD)															

The **SPYDER Control Block** must lie on 8-byte boundaries (SCB address bits A0—A2 are 0s). Table 6 contains the bit assignments for the SCB. The eight channel interrupt bits are allocated such that setting bit (i+8) indicates the presence of one or more interrupts on channel i. These bits are set and cleared by the SPYDER-S device.

The fault bit (FLT) is set if a bus fault occurs when the SPYDER-S device is interacting with memory. The SPYDER-S device sets this bit and interrupts the host. After generating an interrupt, the SPYDER-S device stops all processing and waits for a SPYDER attention (SA) from the host. On receiving SA, the SPYDER-S reads the BOOT bit which, if set, causes a software reset of the SPYDER-S device. SPYDER-S reconfiguration occurs after a subsequent SA. Only a BOOT instruction allows the SPYDER-S device to recover. Bus faults are only reported when the host configures the SPYDER-S device for a processor interface that provides a FAULT input signal. The TFC interrupt is nonmaskable during configuration. Whether it is asserted or not is based entirely on the INT bit in the TFD.

Eight bits are allocated for channel attention. Setting bit i+8 indicates that interrupts have been acknowledged by the host on channel i. These bits are updated by the host. The channel attention bits are used during configuration to specify the interrupt mask. For example, if the host sets bit 15, then the interrupt occurring at bit 15 of the interrupt code byte in each channel control block (CCB) is masked out. If the host allows all interrupt conditions to cause an interrupt, the channel attention bits are all cleared during configuration. Conversely, if all channel attention bits are set during configuration, the SPYDER-S device will only issue an interrupt in the case of a bus fault. Interrupts are not maskable on a per-channel basis, except the TFC, which is maskable per frame.

When the SPYDER-S device has been configured and is in operation, channel attention bits indicate to the SPYDER-S device which channels have interrupt acknowledgements and/or commands from the host. The host sets these acknowledge and command bits in the CCBs (see Table 8), then sets up the channel attention byte in the SCB, finally giving the SPYDER-S device an SA so that the SPYDER-S device reads and processes these commands and acknowledgements. For a more detailed description, see

Operational Description. Note that after the SPYDER-S device processes and/or acknowledges the channel commands, the channel attention bits are cleared.

The BOOT bit is set by the host when a software reset is required. The SPYDER-S device checks this bit and the channel attention byte whenever the host asserts SA. The reboot procedure completely reconfigures the chip, starting with the SPYDER-S device accessing a new ISCB address from the hard-wired SCP address. When the SPYDER-S device detects that the BOOT bit is set after the host sends an SA, all chip processes are halted and the transmitters begin idling immediately. When the host detects this condition, which is indicated when the SERV bit is cleared, it sends a second SA which starts the reboot procedure. The SPYDER-S device remains halted until the second SA is given, thereafter it reconfigures; this allows the host to set up a new set of descriptors without bus competition from the SPYDER-S device.

The channel control block (CCB) provides the offset address pointer to the channel control blocks. The CCBs are consecutively configured in memory; the CCB offset thus specifies the offset of the CCB for channel 0; the CCB for channel 1 is at offset (CCB + 8), and so on. The memory mapping does not depend on whether channels are turned on or off. The CCB address lies on 64-byte boundaries. The configuration block (CB) specifies the address offset of the configuration block, which specifies initialization parameters for the SPYDER-S device.

The **Configuration Block** provides all set-up parameters prior to the start of SPYDER-S device operations. It must lie on 8-byte boundaries (address bits A0—A2 are 0s). One CB exists for each SPYDER-S device in the system. Table 7 contains the bit assignments for the CB.

The channel switch allows the user to specify whether each channel is on or off. For example, if C7 is set, channel 7 is on.

If three or more channels are switched on, any of the 8 available channels may be selected. Note that channel selection is read by SPYDER-S device during configuration only. In order to change the list of channels switched on, the host processor must reboot the SPYDER-S device.

The next location contains various user-defined global configuration options of the SPYDER-S device. These options apply to all channels on a given SPYDER-S device.

If the read header (RHDR) bit is set, the SPYDER-S device reads the initial frame bytes (1 to 4 bytes, as required) from the TFD.

If the write header (WHDR) bit is set, the SPYDER-S device writes the initial frame bytes (1 to 4 bytes, as required) into the received frame descriptor (RFD). This reduces bus occupancy when, for example, HDLC supervisory frames having 1 or 2 byte address and control words are received.

To provide the most memory-efficient allocation of data buffers for receive frames, each SPYDER-S device channel can be configured to share a receive data buffer free list with other channels on this SPYDER-S device or with all channels in all SPYDER-S devices in a system. This is achieved by setting the share buffer free list (SHR) bit in the configuration block.

In various configurations, the user may require that the upper and lower bytes of a 16-bit word of data transferred between the SPYDER-S device and memory be swapped. This capability is accomplished by setting swap bytes (SWB). If SWB is cleared, the byte ordering is for modes M2 and M3 with the lower byte at even addresses. For mode M4, SWB should be set. For a definition of each mode of operation, see the strap options in Table 1.

If an echo bit (EC0—EC7) is set, it indicates that channel is in the echo mode, i.e., if EC0 is set, then channel 0 is in the echo mode. When in echo mode, received data is retransmitted without any processing.

The N1 count applies to the maximum permitted length of an incoming HDLC frame, including level 2 and level 3 header information and may be up to 8191 bytes.

The **Channel Control Blocks**, address CCB + 8i (for channel i), are on 8-byte boundaries (address bits A0—A2 are 0s). There are eight CCBs per SPYDER-S device. See Table 8 for the CCB bit assignments. These blocks are configured sequentially, starting with channel 0, whose address is read from the SPYDER-S control block.

The 7-bit interrupt code allows each bit to represent a distinct interrupt condition, permitting several different interrupts to occur on one channel without loss. Table 9 contains the interrupt code bit assignments. Only bit 7 of the 9-bit status field is used. If this bit is set, the channel is in an idle condition. Therefore, if the SPYDER-S device sets STC and the host reads the idle bit as a 1, this channel has entered the idle state. When the SPYDER-S device sets STC and the host reads a 0 for the idle bit, the idling condition has cleared on this channel.

The seven interrupt acknowledge bits allocate a bit to each potential interrupt, which the host sets when it has acknowledged that interrupt. The SPYDER-S device clears each bit when it detects the acknowledgement. See **Operational Description** for the interrupt/acknowledge procedure.

The nine channel command bits allow the host to define up to nine different commands that the SPYDER-S device is required to execute for this channel. These commands are given in Table 10.

Table 6. SPYDER Control Block (SCB)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Interrupt								Reserved						FLT	SERV
Channel Attention								Reserved							BOOT
Channel Control Block (CCB) Offset Address (for channel 0)															
Configuration Block (CB) Offset Address															

Table 7. Configuration Block (CB)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Switch								Reserved							
C7	C6	C5	C4	C3	C2	C1	C0								
Reserved			RHDR	WHDR	SHR	SWB	Reserved	Echo Switch							
								EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
Reserved			N1 Count (applies to all channels)												

Table 8. Channel Control Block (CCB)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Code							Status								
Interrupt Acknowledge							Channel Command								
Transmit Frame Descriptor Queue															
Receive Frame Descriptor Queue															

Table 9. Interrupt Code Bit Assignments

Bit	Name	Description
15	LLI	**Lost Local Interrupt.** Indicates that more than one interrupt of a given type occurred on this channel without being serviced by the host.
14	NRB	**No Free Receive Buffer Descriptors.** Indicates that the host has failed to point the SPYDER-S to a valid receive buffer descriptor, RBD. (The offset pointed to by the next RBD was 0xFFFF).
13	NRF	**No Free Receive Frame Descriptors.** Indicates that SPYDER-S has already accessed the receive frame descriptor (RFD) with the end-of-list (EOL) bit set, and is now receiving a new frame but has not received an assigned RFD to use.
12	TFC	**Transmit Frame Complete.** SPYDER-S sets this bit when a transmitted frame is complete, if the transmit frame descriptor (TFD) for this frame has the interrupt (INT) bit set. Frame status is given in TFD.
11	UNR	**Underrun.** The transmitter has underrun.
10	FRM	**Frame Received.** This interrupt occurs when a frame is received. The status of the received frame is given in the RFD of that frame.
9	STC	**Status Change.** This interrupt indicates that the channel has started or stopped idling depending on the setting of the IDL bit in status bit 7.

Table 10. Channel Command Descriptions

Bit	8	7	6	5	4	3	2	1	0
Field	INV	NELT	ECHO	IDLE	HALT	RQE	RQD	TQE	TQD

Command Name	Command Description
NULL	When commands bits are set, 0xXF, there are no new channel commands.*
HALT=1	**Halt.** The transmitter aborts the current frame and then sends flags. No new transmit frame descriptor (TFD) is accessed and no new frames are sent.
TQD=1	**TQ Define.** The transmitter reads a new TFD address from the CCB for this channel and then accesses the TFD at the read address. It then begins transmitting the specified frame. This allows the host to alter which TFD is accessed next, thereby redefining the sequence of transmitted frames. The host may use this command to implement a retransmission after a HALT is issued. Its structure is useful since there is no requirement for the host to know which frame was last sent. The host must ensure that the new TFD address is defined in the CCB before issuing this command and interrupting the SPYDER-S by asserting SA. Note that this command enables the transmitter.

*x = don't care.

Table 10. Channel Command Descriptions (Continued)	
Command Name	**Command Description**
TQE=1	**TQ Extend.** The transmitter reads the TFD address from the last TFD in the queue, where the EOL bit was previously set by the host, and then accesses the TFD at the read address. It then begins transmitting the specified frame. This allows the host to extend the queue of TFDs, allowing more frames to be sent. The host must ensure that the new TFD address is defined in the last TFD of the queue before issuing this command and interrupting the SPYDER-S by asserting SA. This command also enables the transmitter. If the transmitter has not read the TFD with EOL set, then no special action is taken by the SPYDER and it continues to access TFDs according to the newly defined queue.
RQD=1	**RQ Define.** The receiver reads a new receive frame descriptor (RFD) address from this channel's CCB and then accesses the RFD at the read address. The next received frame utilizes this RFD, allowing the host to redefine the next RFD accessed. This is useful if an error on the receiver requires the frame descriptor queue to be redefined. The host must ensure that the new RFD address is defined in the CCB before issuing this command and interrupting the SPYDER-S by asserting SA. Note that this command also enables the receiver to handle incoming data.
RQE=1	**RQ Extend.** The receiver reads the RFD address from the last RFD in the queue, where the host had previously set the EOL bit, and then accesses the RFD at the read address. This allows the host to extend the RFD queue periodically. This command is useful in the case of a circular RFD queue, since the host could set the EOL bit in one of the RFDs and periodically redefine the end of the list as the received frames are processed. The host must ensure that the new RFD address is redefined in the last accessed RFD before issuing this command and interrupting the SPYDER-S by asserting SA. Note that this command enables the receiver to handle incoming data. The host may execute the command at any time without risk of a malfunction of the SPYDER-S.
HALT=1, TQD=1	**Retransmit.** The transmitter aborts the current frame and begins to send flags or idles. It also reads the address of the next TFD from this channel's CCB and begins to transmit the frame specified. This command is useful when the host performs frame retransmission, since there is no requirement to know which TFD was last accessed. The host must ensure that the new TFD address is specified in the CCB prior to issuing this command and interrupting the SPYDER-S by asserting SA.
ECHO	**Echo.** If set, this command causes the channel to enter the echo mode, where it provides dumb retransmission of all received data. This is used when the other end of the link is in far-end loopback test mode. If the host stops echoing on a channel by making this bit a 0, it may simultaneously set TQD and RQD so that the initial frame descriptors will be set up by the SPYDER-S. This is necessary only when the host stops echoing without resetting and reconfiguring the chip.
IDLE=1	**Idle.** The transmitter idles after the closing flag of the current frame. If no frames are currently being transmitted, the SPYDER-S begins idling as soon as it services this command. After accessing a new TFD, it follows that frame's transmission with flags if the TFD IDL bit is cleared, or it idles after the frame if the TFD IDL bit is set. This command is used when the host wants a transmitter to idle without waiting for the transmitter to access a TFD with the IDL bit set. At start-up, the transmitter idles until its TFD is set up, after which it sends flags.
INV=1	All data is inverted just prior to transmission and immediately after reception in the transceiver.

Table 10. Channel Command Descriptions (Continued)	
Command Name	**Command Description**
IDLE=0	**Idle Off.** The transmitter sends flags after the end of the current frame. If no frames are currently being transmitted, it begins sending flags as soon as the SPYDER-S services this command. After accessing a new TFD, it begins sending flags immediately if no frames are transmitted. After accessing a new TFD, it follows that frame's transmission with flags if the TFD IDL bit is cleared, or idles after the frame if the TFD IDL bit is set. This command is used when the host wants a transmitter to send flags without waiting for the transmitter to access a TFD with IDL bit clear. At start-up, the transmitter idles until its TFD is set up, after which it send flags.
NELT=1	**Near-End Loop Test.** This command places the channel into the near-end loopback test mode. Note that this command may be executed in parallel with other channel commands, thus allowing their execution in the near-end loopback mode.

Note: If the host has no commands to write to a channel but has interrupts to acknowledge, the channel command byte must be 0xFF. When the SPYDER-S device has serviced all commands and acknowledgements on a channel, the acknowledge/command word is cleared to 0x0F. The null value is not 0x00, since this is a valid command. If the channel command is set with TQD and TQE both 1s, or with RQD and RQE both 1s, this is an invalid command and will be ignored by the SPYDER-S device.

The first **Transmit Frame Descriptor** (TFD) address is provided in the associated channel's CCB. Each TFD points to subsequent TFDs, with free buffers maintained separately for each channel. Table 11 contains the bit assignment for TFD.

If the user selects RHDR=1 (reading initial frame bytes from the TFDs), then each TFD must lie on 16-byte boundaries (a3—a0 are 0). If RHDR=0, TFDs may lie on 8-byte boundaries.

The frame complete (FC) bit indicates frame transmission is complete and the TFD has been processed by the SPYDER-S device.

The host sets the buffer ready (BRDY) bit if the current TFD is set up. When SPYDER-S device first accesses the TFD, it clears FC and BRDY before sending the frame. After the frame has been sent, FC and BRDY are both set. The SPYDER-S device never reads either BRDY or FC; these bits are provided as a maintenance feature for the user.

The SPYDER-S device sets bit 7 of the STATUS bits if the transmitter underruns. Bit 6 is set if this frame was aborted as the result of a HALT command. The other STATUS bits are currently undefined.

The host uses the end-of-list (EOL) bit to indicate that this is the last TFD in the list for this channel.

If STOP is set at configuration for the first TFD of any channel, the frame associated with this TFD will not be sent. Otherwise, if STOP=0, the first frame on that channel will be sent immediately after configuration by the SPYDER-S device. If DCRC is set, a CRC is neither calculated nor appended to this frame.

The host sets the idle (IDL) bit if it wants the SPYDER-S device to idle after transmitting this frame. However, if the DCRC option is selected in the TFD, then the IDL option may not be selected.

If the interrupt (INT) bit is set, the host requests an interrupt from the SPYDER-S device when this frame is sent. If the INT bit is not set, then the TFC will not be issued. TFC interrupts are maskable per frame and therefore cannot be masked during configuration.

When RHDR=0, then all the data to be sent is located in data buffers. These are pointed to by the TBDs which are attached to a TFD. Also note that SUP and HDR(1—0) are ignored by the SPYDER-S device while SSUP and SHDR(1—0) are ignored by the host in this case.

When RHDR=1, then the host will set up each TFD containing initial bytes from this frame. Up to 4 bytes may be written in the TFD. If all bytes of a frame are contained in the TFD, the host sets up the TFD with SUP=1 and the byte count in bits HDR(1—0). If the frame is linger than 4 bytes, the host sets up HDR(1—0) with the byte count contained in the TFD and clears SUP to 0. This causes the SPYDER-S device to send bytes in the TFD and then to look-up the data buffer and send further bytes from there.

In all cases where RHDR=1, the SPYDER-S device writes SHDR(1—0) bits to indicate how many bytes were sent from the TFD as a maintenance feature to the host. Table 12 contains the HDR(1—0) bit settings.

The host may write any header or other bytes in this descriptor to save having to set up a data buffer for short frames such as supervisory frames.

(FCNT + 1) is the minimum number of flags that are transmitted between the FCS of the first frame and the address field of the second frame. If FCNT is zero then the closing flag of the first frame also serves as the opening flag of the second frame (flag sharing). If IDL is set in the TFD, then at least FCNT octets of 1s are sent between the closing flag of the current frame and the opening flag of the next frame. If FCNT is zero (even if IDL is set), then flag sharing occurs. After a RESET of the SPYDER-S device, only one flag is sent before the address field is transmitted, regardless of FCNT. In other words, FCNT becomes effective only after the closing flag of the first frame, following a reset.

The host maintains a queue of receive frame descriptors (RFD) for each channel and each RFD points to the next RFD. RFDs lie on 16-byte boundaries (the four least significant RFD queue address bits are always 0) if the host selects WHDR=1 (write initial frame bytes into the RFDs). If WHDR =0, the RFD is 8 bytes long and the least significant RFD queue address bits are 0. Table 13 contains the bit assignments for RFD.

The received frame complete bit, FC, is set by the SPYDER-S device and indicates that the host may process the buffer.

Table 11. Transmit Frame Descriptor (TFD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC	BRDY	Reserved			SSUP	SHDR1	SHDR0	STATUS							
EOL	STOP	DCRC	IDL	INT	SUP	HDR1	HDR0	FCNT							
Next Transmit Frame Descriptor															
First Transmit Buffer Descriptor															
Level 2 Header — First 2 Bytes															
Level 2 Header — Second 2 Bytes															

Table 12.
HDR1 and HDR0 Bit Settings

Bits	Meaning
01	1 Byte Header
10	2 Byte Header
11	3 Byte Header
00	4 Byte Header

Table 13. Receive Frame Descriptor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC	BRDY	Reserved			SSUP	SHDR1	SHDR0	STATUS							
EOL	Reserved					HDR1	HDR0	Reserved							
Next Receive Frame Descriptor Address															
First Receive Buffer Descriptor Address															
Level 2 Header — First 2 Bytes															
Level 2 Header — Second 2 Bytes															

Table 14. Receiver STATUS Information

Bit	Name	Description
7	GRF	**Good Received Frame.** CRC is correct.
6	BRF	**Bad Received Frame.** CRC is bad.
5	BBC	**Bad Byte Count.** Indicates partial byte received.
4	OVR	**Receiver Overrun**
3	ABT	**Abort.** Frame was aborted.
2	LFR	**Long Frame Received.** Exceeds N1 bytes.
1	—	Reserved.
0	—	Reserved.

Table 15. Buffer Descriptor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOF	BRDY	NACK	CNT												
Next Buffer Descriptor															
Current Buffer Address (Low 16 bits)*															
Reserved*													(High 4 bits)		

*Buffer descriptors must lie on 8-byte boundaries (such that a2—a0 are zero).

The host sets the BRDY bit if the RFD and associated buffers are set up. The SPYDER-S device sets and clears FC and BRDY as for TFDs. Note that SPYDER-S device never reads FC or BRDY, which are provided as host maintenance bits.

When the received frame is complete, the SPYDER-S device writes the STATUS bits. The descriptions of these bits are given in Table 14.

EOL is set by the host, if this is the last RFD ready at this time. If the host changes the EOL bit after configuration, it is recommended that the processor check the BRDY bit in the RFD in which EOL was changed in order to ensure that SPYDER-S device has not read the previous value of the EOL.

When WHDR=0, all data received is put into buffers by the SPYDER-S device. Each frame is allocated an RFD which points to one or more RBDs, each of which points to a data buffer. Also note that the SPYDER-S device ignores HDR(1—0) and the host ignores both SSUP and SHDR(1—0) in this case.

When WHDR=1, then up to 4 bytes of the received frame may be written into its RFD. The host specifies the maximum number of bytes it wishes to write into the RFD using HDR(1—0). If the received frame is small enough to fit into the host allocated space in the RFD, the SPYDER-S device will signify this by setting SSUP=1. This means that there are SHDR(1—0) bytes in the received frame and that there are no data buffers attached to the RFD.

By resetting SSUP=0, the SPYDER-S device indicates to the host that the received frame is larger than the space allocated in the RFD and that the SPYDER-S has written the received data into one or more data buffers.

The buffer descriptor applies to both transmit and receive data buffers and occurs on 8-byte boundaries. Transmit buffer descriptors are attached to a TFD when that frame is set up to be sent over a channel by the host, since the host already knows the composition of the frame. On the receive side, the host may allocate a dedicated queue of buffer descriptors to each RFD, or may alternatively take buffers from a free list, which will share buffers across one or more SPYDER-S devices in a system. Table 15 contains the bit assignments for the buffer descriptor.

The EOF bit indicates the last buffer descriptor of a frame and is set by the host before the beginning of a frame for TBDs. It is set by the SPYDER-S device for the last buffer of a received frame. BRDY is set if the buffer is ready and is cleared by the SPYDER-S device when it accesses this BD.

The host sets up the buffer descriptor with BRDY being 1 and NACK a 0. When the SPYDER-S device accesses this BD, BRDY is cleared and NACK is set to 1. When the SPYDER-S device releases the descriptor, BRDY remains a 0 and NACK is cleared. The SPYDER-S device never reads these bits; they are provided for system maintenance. If the next buffer descriptor field is 0xFFFF then there is no next buffer descriptor.

The number of bytes in the buffer is written in count (CNT). For transmit frames, the CNT value indicates the number of bytes to be sent; CNT remains after the SPYDER-S device releases the buffer descriptor. For received frames, CNT indicates space allocated in this buffer. When the SPYDER-S device releases this buffer descriptor, it writes the byte count received into CNT. The user must allocate at least two bytes in each receiver data buffer.

The data buffer address must begin on an even byte boundary (a0 is zero), but may be an even or odd number of bytes long. For mode 4 strapping option the order of the data buffer address words is reversed from that shown above to allow a direct 32-bit read operation to be executed.

Operational Description

All host/SPYDER-S communication is performed by accessing memory-mapped data structures. The following describes the operation of the SPYDER-S device using these structures.

Initialization Procedure

The host must give an RST pulse lasting at least four clock (CLK) periods. The SPYDER-S device internally resets 16 CLK periods after the falling edge of RST. Following a hardware or software reset, the host sets up the SPYDER configuration pointer (SCP), intermediate SPYDER control block (ISCB), free buffer descriptor block (FBDB), and SPYDER control block (SCB) (including the channel control block (CCB) and configuration block (CB) addresses). The host also configures addresses for the CCBs, including receive frame descriptor (RFD) and transmit frame descriptor (TFD), for all active channels. Following a hardware reset, it is not necessary for the host to set the BOOT bit in the SCB; this is merely used as a software reset allowing a reconfiguration of the SPYDER-S device to occur at any

time the host chooses after the SPYDER-S device has concluded initial configuration. The SPYDER-S device begins the initialization procedure after receiving the first SPYDER attention (SA) following a reset. Note that all SA pulses must be at least two clock cycles wide. It then fetches the ISCB address from location 0xFFFFC, and reads the SCB and FBDB addresses from the ISCB. The SPYDER-S device then reads the CB address from the SCB and the configuration parameters contained in the CB. For all active channels, not echoing, it then reads the TFD and RFD addresses from the appropriate CCB. Finally, the SPYDER-S device clears the busy bit in the ISCB, interrupts the host without setting any channel interrupt bits, and waits for an SA. After an SA is received, the SPYDER-S device begins transmitting frames and processing received frames.

Host/SPYDER-S Command Handshake

The SPYDER-S device recognizes two classes of commands: the BOOT command and channel commands. The BOOT command is bit 0 of the second word in the SCB. When set by the host and read by the SPYDER-S device, the device performs a software reset (or reboot) beginning at the SCP. To make the device perform this function, the host sets this bit in the SCB and asserts SA. The SPYDER-S device then checks the second word of the SCB for the BOOT bit and channel attention bits. The BOOT bit takes precedence; if set, the SPYDER-S device returns to reset; after another SA the device performs reconfiguration.

Channel commands apply to a particular channel allowing the host to manipulate a particular transmitter or receiver. The host executes a channel command on channel i by writing the channel command byte of the CCBi, setting bit i of the channel attention byte of the SCB, and issuing an SA. The SPYDER-S device reads the channel attention byte of the SCB, and, recognizing bit i as set, reads the interrupt ack/channel command word of CCBi. The SPYDER-S device services any interrupt acknowledgements that the host has performed and executes the specified channel command, clearing the channel attention byte, and setting the second CCB word to 0x000F. Note that if other interrupts occur and the host does not acknowledge all interrupts on this channel, then the interrupt line is asserted, but the channel command byte is still cleared. An explanation of channel commands is given in Table 10. The SPYDER-S device may be told to service any or all of the eight channels with a single SA; additionally, each channel may give several commands and/or acknowledges for each SA. This parallelism also exists in the way that SPYDER-S device may report several interrupting channels, each with several interrupts, when giving a single $\overline{\text{INT}}$ to the host.

After issuing an SA, the host should not alter the contents of the interrupt ack/channel command word or the channel attention byte until the SPYDER-S device has serviced them. The host knows that the SPYDER-S device has serviced all channels when the device clears the channel attention byte.

Host/SPYDER-S Interrupt Handshake

$\overline{\text{INT}}$ is asserted when the channel interrupt bits are written in the SCB. The signal remains asserted until the host gives the SA pulse. Upon receiving this, $\overline{\text{INT}}$ is immediately negated. Upon processing the channel commands and acknowledgements, $\overline{\text{INT}}$ will be reasserted if there are still unacknowledged interrupts on any channel.

Interrupts are issued and acknowledged as follows.

SPYDER-S:

1. Sets an interrupt code in CCBi (i indicates any one of 8 channels).
2. Then sets interrupt bit i in the SPYDER control block (SCB) channel interrupt byte.
3. Drives the interrupt line active low (not a pulse). While waiting for SA from the host, the SPYDER-S device may write additional interrupt codes and channel interrupts.

The Host:

4. Reads the channel interrupt byte and appropriate interrupt code.
5. Then executes an interrupt service routine.
6. Sets interrupt acknowledge bit(s) in CCB(s), while also writing channel commands if desired.
7. Sets channel attention bit(s) in the SCB.
8. SA is driven active by a positive pulse with a width of two clock cycles. This pulse must last for at least two CLK periods and must come at this point in the interrupt/acknowledge cycle and occur only once. In host software the SA pulse should occur as the instruction adjacent to the host CPU instruction to return from servicing the interrupt routine. If the host asserts multiple SA pulses, there is a possibility that the SPYDER-S device will reassert the interrupt line while the host is still in the interrupt service routine, creating a potential software malfunction.
9. The interrupt pin becomes inactive.
10. Reads the channel attention byte.
11. Then reads the interrupt acknowledge bits in CCBi, for all i where channel attention bit i is set. The channel command byte is also read.
12. Clears interrupt code bits that have been acknowledged and services the channel command specified, clearing this byte when serviced.
13. Clears the channel interrupt bits for those channels whose interrupts have all been acknowledged.
14. If there are any interrupts that have not been serviced, $\overline{\text{INT}}$ is driven active.

Free Buffer Maintenance

The SPYDER-S device may allocate memory for received data by fetching buffers from a free list. The user has the choice of maintaining one free list for each SPYDER-S device in a system or having all devices share a common free list. Alternatively, separate buffer queues may be maintained per frame.

A local free list is maintained by clearing the share free list (SHR) bit in the CB to 0. When the host elects to share the receiver data buffers, SHR is set (1) at configuration and the SPYDER-S device reads the address offset of the first data buffer descriptor from the FBDB location. The SPYDER-S device accesses this data buffer descriptor, reads the next buffer descriptor address from it, and writes this offset to the FBDB. In this way, the next receiver requiring a data buffer will use the descriptor just written to the FBDB. The SPYDER-S device will not relinquish the bus while performing this read-modify-write sequence, using the LOCK pin to indicate that it wishes to retain bus ownership temporarily.

If the host does not require a shared free list and clears SHR to 0, the SPYDER-S device accesses the first receiver data buffer for a frame from the RFD. Subsequent buffer descriptor addresses are acquired from the current data buffer descriptor. If the buffer free list is exhausted, the SPYDER-S device informs the host with a no free receive buffer descriptor (NRB) interrupt. The host marks the end of the buffer descriptor queue by writing the next buffer descriptor address as 0xFFFF. The current frame will also be abandoned. The SPYDER-S device attempts to process frames as long as there are RFDs available. When the SPYDER-S device runs out of RFDs, a no free receive frame descriptor (NRF) interrupt is issued and the device waits for the host to reconfigure the RFD queue.

The host enables a shared received data buffer free list by setting SHR to 1. If the host wishes to share a free list across all SPYDER-S devices in a system, then the location of the FBDB is the same for all devices. Lists may be shared within each SPYDER-S device by setting up one distinct FBDB address per SPYDER-S in the system. Note that the device checks whether the next buffer descriptor after the one it is about to use is at 0xFFFF. When this happens, the NRB interrupt will occur on this channel. Hence, FBDB itself is never set to 0xFFFF.

Interfacing Requirements

Typical high-end and low-end configurations using the SPYDER-S device are presented on Figures 5 and 6.

Bus Arbitration

The SPYDER-S device uses a DMA request (DREQ) and DMA acknowledge (DACK) to gain access to the system bus. DREQ is asserted when the SPYDER-S wants to access the bus. The host grants it by asserting DACK. Since the device often performs several memory transactions in a burst, it attempts to do this unless the host negates DACK (in which case the SPYDER-S device completes the current memory transaction and negates DREQ for 1 clock cycle before reasserting it, waiting for DACK).

If, during the operation, RDY is inactive, then wait-states are inserted until RDY is asserted by the host. If the host is always RDY, then consecutive bus operations will require four clock cycles each.

The LOCK signal is asserted by the SPYDER-S device when sharing data buffers with other devices (i.e., when SHR is set in the configuration block). Once the host has granted the bus to the SPYDER-S device (DACK=active), then DACK should not be negated as long as LOCK is asserted. DREQ will not be withdrawn during a LOCK sequence. Consequently, it will be a violation of the specifications to negate DACK while LOCK is asserted.

Bus arbitration among multiple SPYDER-S devices must be accomplished through external arbitration circuitry. Its simple but exact implementation depends on user preference.

$\overline{WE}$:$\overline{DS}$, $\overline{RE}$:$\overline{CINIT}$, DT/$\overline{R}$,:R/$\overline{W}$, and ALE:$\overline{AS}$ are outputs that 3-state when the SPYDER-S device does not have the system bus. This allows more than one SPYDER-S device to be connected in the system. If there are extended periods during which neither the SPYDER-S device nor the host will drive the bus, then pull-up resistors are recommended. ALE:$\overline{AS}$ will need a pull-down (modes M2 and M3) or a pull-up (mode M4) under similar conditions.

Interface Configuration

The SPYDER-S device can be configured to interface with general-trade 16-bit processors or the AT&T 32-bit microprocessor family. Mode selection determines which bus interface is used. The modes are selected using the ST0 and ST1 strap option pins. The straps are sampled into transparent latches while RESET is active.

Modes M2 and M3

The iAPX86 bus interface can be configured to operate either synchronously (max mode – M2) or asynchronously (min mode – M3). Both the synchronous and asynchronous bus control interfaces are accomplished using $\overline{RE}$, $\overline{WE}$, and an asynchronous RDY line. In M3, $\overline{RE}$ and $\overline{WE}$ remain asserted with wait-states, extending them until RDY is activated by the host. In M2, $\overline{RE}$ and $\overline{WE}$ are not extended with wait-states while waiting for the RDY to be asserted.

The assertion and negation of these signals is dependent on the following CLK edges (see timing diagram).

$\overline{RE}/\overline{WE}$	Assertion	Negation
M2 (Synch.)	↑ CLK-T2	↓ CLK-T4
M3 (Asynch.)	↓ CLK-T3	↓ CLK-T5

↑ CLK-T2 is read, "Rising CLK edge that begins bus cycle -T2."
↓ CLK-T4 is read, "Falling CLK edge during bus cycle -T4."

Mode M4

Mode M4 is distinguished from modes M2/M3 by the provision of $\overline{DS}$ and R/$\overline{W}$ as opposed to $\overline{RE}$, $\overline{WE}$, and $\overline{BHE}$. Consequently, byte operations are not possible in M4. When the SPYDER is granted the system bus via the $\overline{DREQ}/\overline{DACK}$ handshaking (see **Bus Arbitration**), $\overline{AS}$, $\overline{DS}$, and $\overline{CINIT}$ are pulled from their High-Z state to their inactive state on the next rising CLK edge (start of T2). The address is put on the address/data bus. Additionally, the R/$\overline{W}$ line goes to the appropriate level, depending on whether a read or write is to be performed. On the next rising CLK edge, $\overline{AS}$ is asserted (beginning of T3). If a memory write is to occur, the address/data bus is enabled. $\overline{DS}$ is asserted and negated as follows:

	Assertion	Negation
$\overline{DS}$ (Read, i.e., R/$\overline{W}$ = V_{OH})	↓ CLK-T3	↓ CLK-T5
$\overline{DS}$ (Write, i.e., R/$\overline{W}$ = V_{OL})	↑ CLK-T4	↓ CLK-T5

$\overline{DTACK}$ is sampled in T4 and wait states are asserted with the $\overline{DS}$ being extended until the host asserts $\overline{DTACK}$.

Link Side (Serial Interface) Timing

If a continuous data rate is to be maintained, it is recommended that the TCLK period and RCLK period be equal to four times the CLK period. However, a burst serial data rate of 4.096 Mb/s can be sustained for 8 bit times. This implies that minimum TCLK and RCLK periods equal to 1.953 times the CLK period are acceptable (see Figure 8).

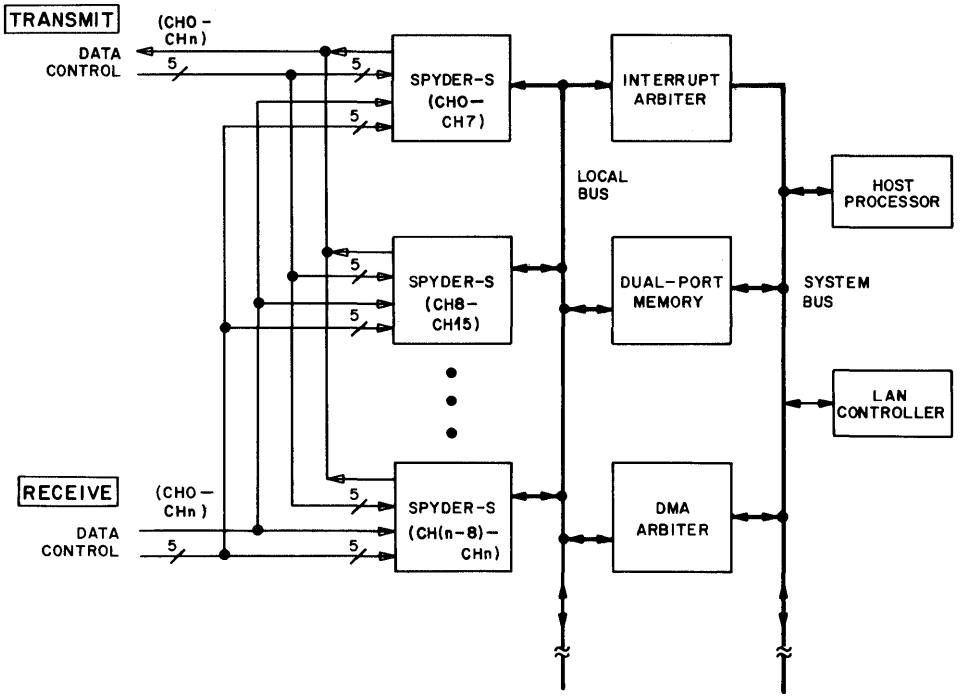


Figure 5. High-End Synchronous SPYDER-S Configuration

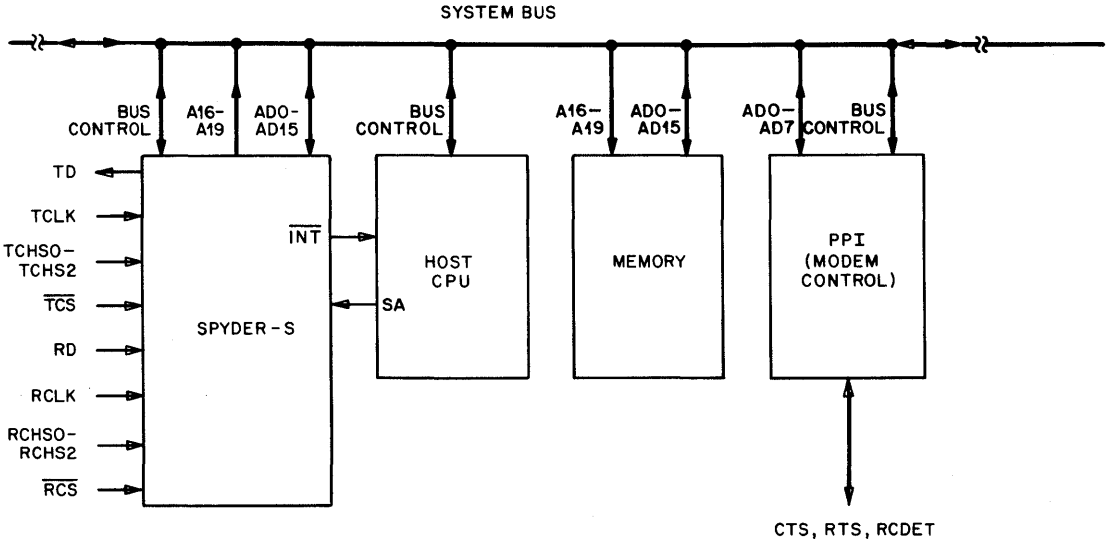


Figure 6. Low-End SPYDER-S System Configuration

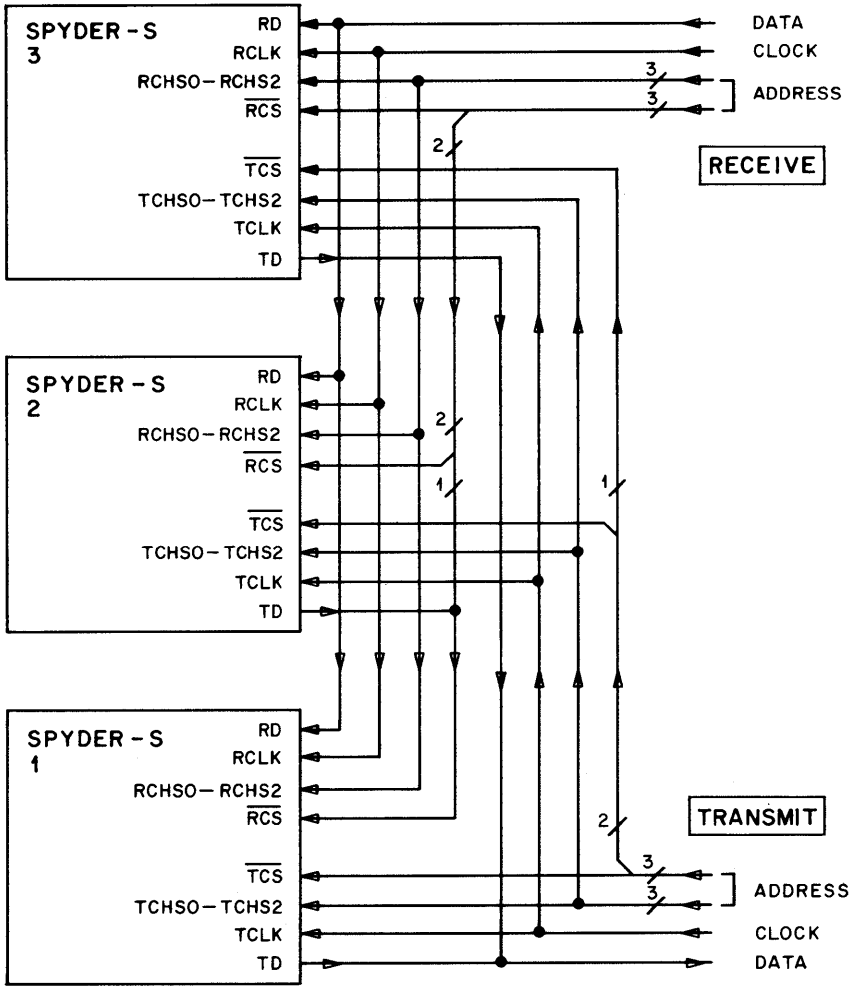
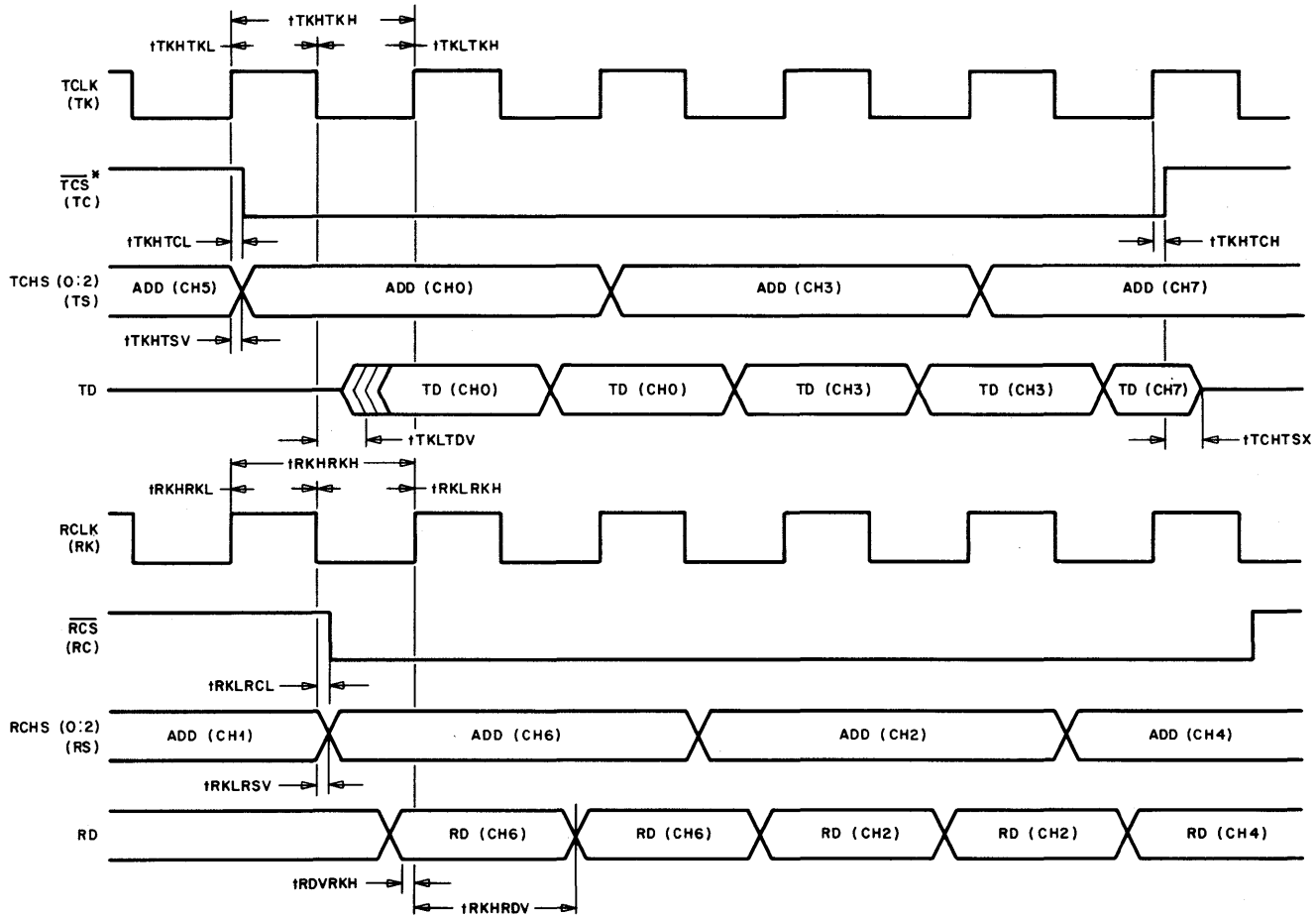


Figure 7. Line Interface Connections for a 24-Channel Data Link



* NOTE: AN ACTIVE LOW $\overline{TCS}$ DOES NOT CAUSE THE TD LINE TO BE DRIVEN UNTIL AFTER THE NEGATIVE EDGE OF TCLK.

Figure 8. Serial Data Link Side Timing

CHARACTERISTICS

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V

Parameter		Symbol	Min	Max	Unit
Input Voltage	Low	V_{IL}	–	0.8	V
	High	V_{IH}	2.0	V_{DD} + 0.5	V
Output Voltage	Low	V_{OL}	–	0.4	V
	High	V_{OH}	2.8	–	V

Maximum Ratings

Voltage range on any pin with respect to ground (V_{SS}) ..... −0.5 V to +7 V
Ambient Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... 0 to 85 °C
Power Dissipation (PD) ..... <1W
Source and sink current from input and/or output pin ..... 2.4 mA

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurance of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Serial Data Link Side Timing				
Symbol	**Description***	**Min**	**Max**	**Unit**
tTKHTKH	TCLK Period	1.953 CLK	–	–
tTKHTKL	TCLK High	50	–	ns
tTKLTKH	TCLK Low	50	–	ns
tTKLTDV	TCLK Low to Valid Data	–	64	ns
tTKHTCL	TCLK High to $\overline{TCS}$ Low[1]	0	tTKHTKL−40	ns
tTKHTCH	TCLK High to $\overline{TCS}$ High[1]	0	tTKHTKL−40	ns
tTKHTSV	TCLK High to TCHS Valid[1]	0	tTKHTKL−40	ns
tTCHTSX	$\overline{TCS}$ high to TD 3-State	–	25	ns
tRKHRKH	RCLK Period	1.953 CLK	–	–
tRKHRKL	RCLK High	50	–	ns
tRKLRKH	RCLK Low	50	–	ns
tRDVRKH	RD Valid to RCLK	15	–	ns
tRKHRDV	RD Hold Time	15	–	ns
tRKLRCL	RCLK Low to $\overline{RCS}$[2]	0	tRKLRKH−40	–
tRKLRSV	RCLK Low to RCHS Valid[2,3]	0	tRKLRKH−40	–

* All notes appear at the end of the table.

All Modes				
Symbol	**Description***	**Min**	**Max**	**Unit**
tCKHCKH	Input Clock Period	125	2000	ns
tCKLCKH	Clock Low Time	58	1000	ns
tCKHCKL	Clock High Time	58	1000	ns
tT	Transition Time[4]	–	5	ns
tCKHCV	Control Line Valid Delay from Clock High[5]	0	50	ns
tCKHLKH	LOCK Active Delay[6]	0	50	ns
tCKHLKL	LOCK Inactive Delay	0	50	ns
tCKLAV	Address (A) Valid Delay	0	50	ns
tCKLAZ	Address (A) Float Delay	0	50	ns
tCKLAWV	Data Output (AD) Valid Delay	0	50	ns
tARVCKL	Data Input (AD) Set-Up Time	50	–	ns
tCKLARZ	Data Input Hold Time	50	–	ns
tCKHAWZ	AD Float Delay	0	40	ns
Modes M2 and M3				
tCKHDRH	DREQ Active Delay	0	50	ns
tCKHDRL	DREQ Inactive Delay	0	50	ns
tDRHDRL	DREQ Active Width[7]	6tCKHCKH−50	–	ns
tDRLDRH	DREQ Inactive Width	tCKHCKH−30	–	ns
tCKLDRH	DREQ Reassertion Delay[11]	tCKHCKH+ tCKLCKH	tCKHCKH+ tCKLCKH+30	ns
tDAHCKL	DACK Active Input Set-Up Time	25	–	ns
tDAHDAL	DACK Active Time	tCKHCKH+25	–	ns
tDALCKL	DACK Inactive Input Set-Up Time	50	–	ns
tCKLDAH	DACK Input Hold Time	50	–	ns
tCKLDNL	$\overline{\text{DEN}}$ Active Delay	0	50	ns
tCKLDNH	$\overline{\text{DEN}}$ Inactive Delay	0	50	ns
tCKHAEH	ALE Active Delay	0	50	ns
tAEHAEL	ALE Active Width	tCKHCKH−25	tCKHCKH+25	ns
tCKHAEL	ALE Inactive Delay	0	50	ns
tCKHTS	Control Line 3-State Delay	0	50	ns
tCKLBEL	$\overline{\text{BHE}}$ Active Delay	0	50	ns
tCKLREL	Read Enable Active Delay	0	50	ns
tCKLWEL	Write Enable Active Delay	0	50	ns
tCKLBEH	$\overline{\text{BHE}}$ Inactive Delay	0	50	ns
tCKLREH	Read Enable Inactive Delay (M2)	0	50	ns
tCKHREH	Read Enable Inactive Delay (M3)	tCKHCKL	tCKHCKL+50	ns
tCKLWEH	Write Enable Inactive Delay (M2)	0	50	ns
tCKHWEH	Write Enable Inactive (M3)	tCKHCKL	tCKHCKL+50	ns
tAZREL	$\overline{\text{RE}}$ Delay After Address 3-State	0	–	ns
tBELBEH	$\overline{\text{BHE}}$ Active Width[8]	tCKHCKH−40	tCKHCKH+40	ns
tRYHCKH	RDY Input Set-Up Time (M2)	20	–	ns

* All notes appear at the end of the table.

Modes M2 and M3 (Continued)				
Symbol	**Description***	**Min**	**Max**	**Unit**
tCKHRYL	RDY Input Hold Time (M2)[9]	20	–	ns
tRYHRYL	RDY Pulse Width (M2)[10]	40	–	ns
tRYHCKL	$\overline{\text{RDY}}$ Input Set-Up Time (M3)	20	–	ns
tCKLRYL	RDY Input Hold Time (M3)	20	–	ns
tRYHRYL	RDY Pulse Width (M3)[10]	tCKHCKH+20	–	ns
Mode M4				
tCKHDRL	DREQ Active Delay	0	50	ns
tCKHDRH	DREQ Inactive Delay	0	50	ns
tDRLDRH	DREQ Active Width	6tCKHCKH–50	–	ns
tDRHDRL	DREQ Inactive Width	tCKHCKH–30	–	ns
tDAHCKL	DACK Input Set-Up Time	50	–	ns
tCKLDAL	DACK Input Hold Time	50	–	ns
tCKLDRL	DREQ Reassertion Delay[11]	tCKHCKH+ tCKLCKH	tCKHCKH+ tCKLCKH+30	ns
tDALCKL	DACK Input Set-Up Time	25	–	ns
tDALDAH	DACK Active Time	tCKHCKH+25	–	ns
tCKLDNL	$\overline{\text{DEN}}$ Active Delay	0	50	ns
tCKLDNH	$\overline{\text{DEN}}$ Inactive Delay	0	50	ns
tCKHASH	$\overline{\text{AS}}$ Active Delay	0	35	ns
tASHASL	$\overline{\text{AS}}$ Active Width	tCKHCKH–25	tCKHCKH+25	ns
tCKHASL	$\overline{\text{AS}}$ Inactive Delay	0	35	ns
tCKHTS	Control Line Float Delay	0	50	ns
tCKLCIL	$\overline{\text{CINIT}}$ Active Delay	0	50	ns
tCKHDSL	Data Strobe Inactive Delay	0	50	ns
tCKLCIH	$\overline{\text{CINIT}}$ Inactive Delay	0	50	ns
tCKLDSH	Data Strobe Active Delay	0	50	ns
tCKLRWL	Control Line Inactive Delay (for a Write)	0	50	ns
tAZDSL	$\overline{\text{DS}}$ Delay After Address Output Float	0	–	ns
tDTLCKL	$\overline{\text{DTACK}}$ Input Set-Up Time	20	–	ns
tCKLDTH	$\overline{\text{DTACK}}$ Input Hold Time[9]	20	–	ns
tDTLDTH	$\overline{\text{DTACK}}$ Active Pulse Width[10]	tCKHCKH+20	–	ns

[1] For proper operation, transmitter chip select and channel select should change state following the rising edge of TCLK.

[2] For proper operation, receive chip select and channel select should change state following the falling edge of RCLK.

[3] If TCLK and RCLK are connected together, TD can feed RD directly, but $\overline{\text{RCS}}$ and RCHS2–0 should be delayed by 1/2 clock cycle from $\overline{\text{TCS}}$ and TCHS2–0. Note that a load of 50 pF on TD is assumed. An additional delay of 3.8 ns per 50 pF of additional load must be added.

[4] tT = 5 ns to rise from 0.4 V to 2.4 V of fall from 2.4 V to 0.4 V.

[5] Control line (C) represents the following control signals: ALE:$\overline{\text{AS}}$, DT/$\overline{\text{R}}$: R/$\overline{\text{W}}$, $\overline{\text{BHE}}$, RE:$\overline{\text{CINIT}}$, WE:$\overline{\text{DS}}$, and $\overline{\text{DEN}}$.

[6] LOCK is asserted if the SPYDER-S wants to hold the bus until it finishes its bus operation. Once the host has granted the bus to the SPYDER-S, no other device should access the bus if asserted, i.e., DACK should not be removed. DREQ will not be removed during a LOCK sequence.

[7] The SPYDER-S releases the bus after the bus is granted only if:
a. The SPYDER-S finishes bus operation(s) while DACK is active.
b. The SPYDER-S finishes the current bus cycle when DACK is inactive (see Note 6 also).
c. The SPYDER-S aborts the current cycle when FAULT (Mode M4) is active.

[8] In all 3 modes (M2, M3, M4) only word transfers are performed. However in M2 and M3, $\overline{BHE}$ is asserted to indicate word transfers and is negated during byte operations. $\overline{BHE}$ is multiplexed with FAULT in M4.

[9] RDY:$\overline{DTACK}$ is latched on the falling edge of T4 in modes M3 and M4 and is sampled on the rising edge beginning T5 in mode M2.

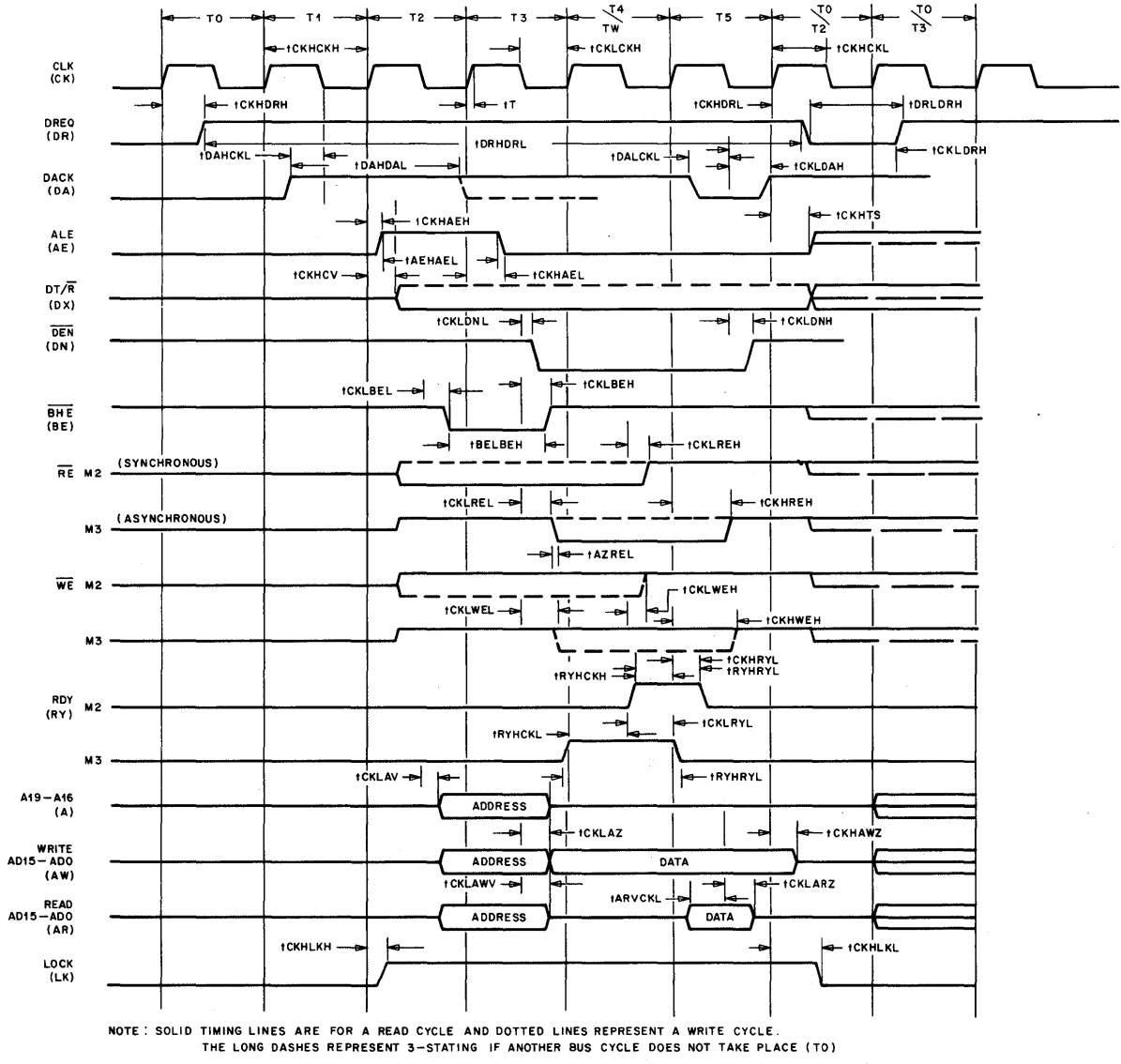
[10] In modes M3 and M4, if the minimum active pulse width is satisfied, then the setup and hold times can be ignored. If RDY:$\overline{DTACK}$ is not detected to be active when required, as shown in the timing diagram, then a WAIT (tW) state will be inserted.

In M2, DT/$\overline{R}$ and $\overline{DEN}$ are stretched by wait-states.
In M3, $\overline{RE}$, $\overline{WE}$, $\overline{DEN}$, and DT/$\overline{R}$ are stretched by wait-states.
In M4, R/$\overline{W}$, $\overline{DS}$ and $\overline{DEN}$ are stretched by wait-states.

[11] If DACK is sampled to be inactive on the falling CLK edge in T5 while DREQ was asserted, then DREQ will negate itself about one-half clock cycle later and reassert itself approximately one clock cycle after that (applies to all 3 modes).

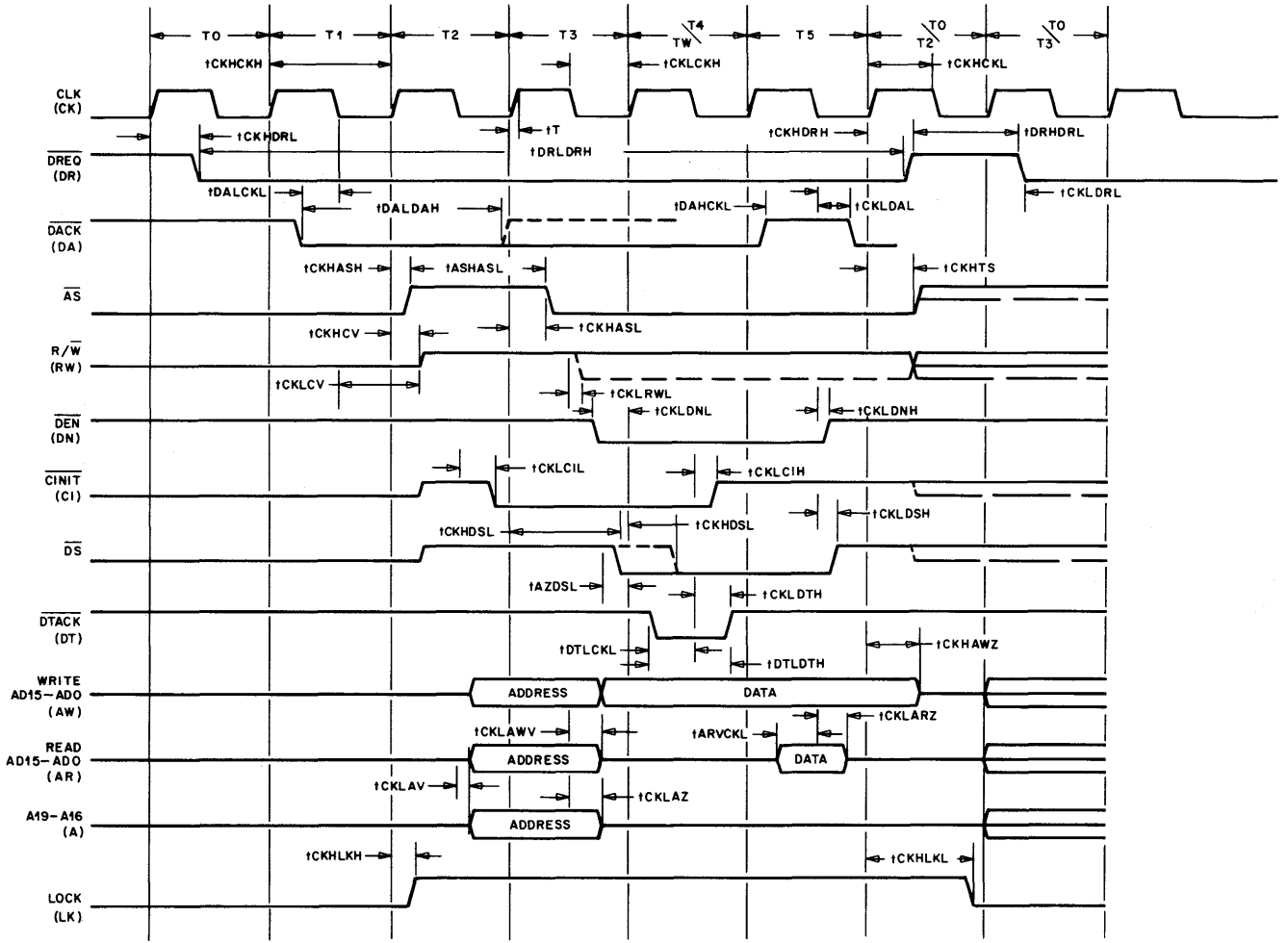
Timing Diagrams

Note: Solid timing lines are for a read cycle and dotted lines represent a write cycle.



NOTE: SOLID TIMING LINES ARE FOR A READ CYCLE AND DOTTED LINES REPRESENT A WRITE CYCLE.
THE LONG DASHES REPRESENT 3-STATING IF ANOTHER BUS CYCLE DOES NOT TAKE PLACE (TO)

Figure 9. Timing for Modes M2 and M3



NOTE: SOLID LINES REPRESENT A READ, DOTTED LINES A WRITE. THE LONG DASHED REPRESENT 3-STATING IF ANOTHER BUS CYCLE DOES NOT OCCUR.

Figure 10. Timing for Mode M4

The information contained herein is preliminary and subject to change.

FEATURES

Host Interface

- Compatible with 8088 and 80188 microprocessor-based systems and 8051 microcontroller
- Compatible with 8237 and 8257 DMA controllers in extended write mode
- Simple register control interface
- Wait-state initiator (8088 and 80188)
- Receiver end-of-frame interrupt
- Programmable receive and transmit queue interrupts with variable fill levels
- Programmable receive and transmit DMA requests with variable fill levels

Serial Link Interface

- Full-duplex serial receive and transmit data lines
- Separate receive and transmit clocks
- 4 Mb/s maximum data rate
- Six-byte receive queue
- Four-byte transmit queue
- Programmable request-to-send/clear-to-send handshaking
- Near- and far-end loop test modes
- Automatic flag transmission and detection
- Data metering via programmable interframe spacing
- Zero-bit insertion and deletion for data transparency
- CRC-CCITT 16-bit polynomial generation and check with inhibit option
- Abort/idle detection and transmission
- Detection of transmitter underrun and receiver overrun
- Optional inversion of serial bit streams

DESCRIPTION

The T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines using HDLC bit-synchronous protocol to 8-bit microprocessor or microcontroller systems. All inputs and outputs of the T7111 ANT are TTL-compatible. It is implemented using CMOS technology and requires a single 5 V supply. The device is available in a 28-pin plastic DIP for standard through-hole mounting or in a 28-pin plastic DIP small-outline J-lead (SOJ) for surface mounting.

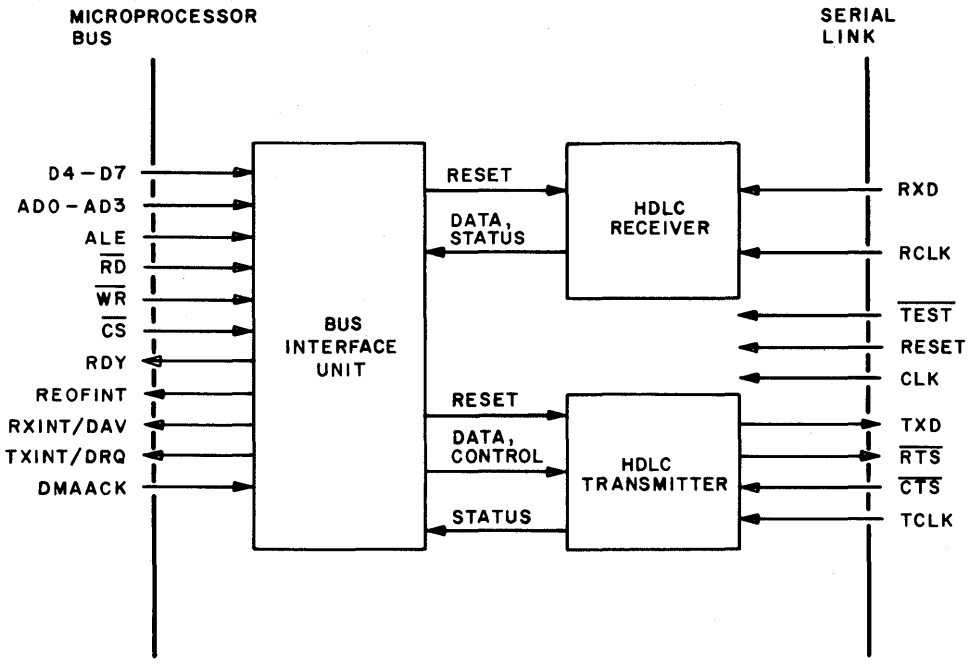
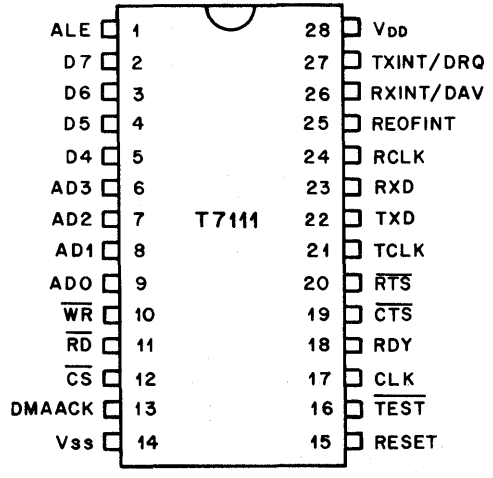


Figure 1. T7111 Synchronous Packet Data Formatter Simplified Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin
AD0	9	RD	11
AD1	8	RDY	18
AD2	7	REOFINT	25
AD3	6	RESET	15
ALE	1	RTS	20
CLK	17	RXD	23
CS	12	RXINT/DAV	26
CTS	19	TCLK	21
D4	5	TEST	16
D5	4	TXD	22
D6	3	TXINT/DRQ	27
D7	2	VDD	28
DMAACK	13	Vss	14
RCLK	24	WR	10

Figure 2. T7111 ANT Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7111 Pin Descriptions

Pin	Symbol	Type	Name/Function
1	ALE	I	**Address Latch Enable.** When high, address inputs AD0—AD3 are latched on the falling edge of ALE.
2	D7	I/O	**Data Bus Bit 7.**
3	D6	I/O	**Data Bus Bit 6.**
4	D5	I/O	**Data Bus Bit 5.**
5	D4	I/O	**Data Bus Bit 4.** Bidirectional, multiplexed
6	AD3	I/O	**Address/Data Bus Bit 3.** 4-bit address and 8-bit data bus.
7	AD2	I/O	**Address/Data Bus Bit 2.**
8	AD1	I/O	**Address/Data Bus Bit 1.**
9	AD0	I/O	**Address/Data Bus Bit 0.**
10	$\overline{WR}$	I	**Write Strobe (Active Low).** Write strobe is driven low by the microprocessor during a write access. Data is latched on the low-to-high transition of $\overline{WR}$.
11	$\overline{RD}$	I	**Read Strobe (Active Low).** Read strobe is driven low by the microprocessor during a read access. The ANT will not drive the data bus until $\overline{RD}$ is low.
12	$\overline{CS}$	I	**Chip Select (Active Low).** Must be low for the duration of a read or write pulse to ensure correct operation. ALE must be active on any transition of $\overline{CS}$. $\overline{CS}$ should only be asserted during ANT read or write cycles. $\overline{CS}$ is not required for DMA transfers.
13	DMAACK	I	**DMA Acknowledge.** DMAACK functions as a secondary chip select during DMA cycles. Its assertion state is determined by the acknowledge polarity (ACKPOL) bit in the master configuration (MC) register. When active, the ANT's data bus is enabled. If DAV is asserted, the ANT responds with a byte from the receiver queue; if DRQ is asserted, the ANT latches a byte into the transmitter queue. If neither DAV (pin 26) nor DRQ (pin 27) is asserted, DMAACK is ignored.
14	VSS	—	**Ground.**
15	RESET	I	**Reset.** When high for at least four clock cycles, all internal processes are terminated, the ANT returns to its idle state. All output pins are 3-stated while RESET remains active.
16	$\overline{TEST}$	I	**Test Mode.** Used to 3-state output pins during board testing. Held high during normal operation.
17	CLK	I	**System Clock.** 2—8 MHz system clock input.
18	RDY	O*	**Ready.** When high, indicates to 8088 and 80188 Microprocessor systems the ANT is ready to complete a read or write transfer. Also used to insert wait-states into microprocessor read and write cycles. This output should be left unconnected when using 8051 Microcontrollers.

*Indicates 3-state condition.

Table 1. T7111 Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
19	$\overline{CTS}$	I	**Clear-to-Send (Active Low).** Can be programmed to perform clear-to-send handshaking with a physical link controller when the level one control (LOC) bit in the MC register is set (1).
20	$\overline{RTS}$	O*	**Request-to-Send (Active Low).** Can be programmed to perform request-to-send handshaking with a physical link controller when the LOC bit in the MC register is set (1).
21	TCLK	I	**Transmit Data Clock.** Maximum frequency is CLK/2 (pin 17), with a maximum of 4 MHz. Data is output on the falling edge of TCLK. There is no minimum TCLK frequency.
22	TXD	O*	**Transmit Data.** Serial data output. May be inverted by setting (1) the INV bit in the transmitter control (TC) register. Data is transmitted with least significant bit first.
23	RXD	I	**Receive Data.** Serial data input. May be inverted by setting (1) the INV bit in the TC register. The first bit received is the least significant bit on the data bus.
24	RCLK	I	**Receive Data Clock.** Maximum frequency is CLK/2 (pin 17), with a maximum of 4 MHz. Data is sampled on the rising edge of RCLK. There is no minimum RCLK frequency.
25	REOFINT	O (OD)**	**Receiver End-of-Frame Interrupt.** When enabled and asserted, indicates that the receiver has detected the end of a frame. Assertion state is determined by the REOFPOL bit in the MC register. REOFINT is enabled by the REOFENB bit in the DIC register.
26	RXINT/DAV	O (OD)**	**Receiver Interrupt/Data Available.** Assertion state is determined by the D/IPOL bit in the MC register. When the DMA/I bit in the MC register is cleared (0), RXINT/DAV functions as an interrupt. RXINT is asserted when the number of bytes in the receiver queue equals or exceeds the setting of the RFL bits in the DIC register, unless it is disabled via the RDIENB bit in the DIC register. When the DMA/I bit in the MC register is set (1), RXINT/DAV functions as a DMA request. DAV is asserted when the number of bytes available is equal to the RFL; DAV is negated when the receiver queue is empty, unless it is disabled via the RDIENB bit in the DIC register. DAV is never asserted when DRQ is asserted.

*Indicates a 3-state condition.
**Open Drain – Pull-up resistor across output = 1000 Ω minimum.

Table 1. T7111 Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
27	TXINT/DRQ	O (OD)**	**Transmitter Interrupt/Data Request.** Assertion state is determined by the D/IPOL bit in the MC register. When bit DMA/I in the MC register is cleared (0), TXINT/DRQ functions as an interrupt. TXINT will be asserted when the number of empty bytes in the transmitter queue equals or exceed the setting of the TEL bits in the DIC register, unless it is disabled via the TDIENB bit in the DIC register. When bit DMA/I in the MC register is set (1), TXINT/DRQ functions as a DMA request. DRQ is asserted when a number of empty bytes equal to the TEL are available; DRQ is negated when the transmitter queue is full, unless it is disabled via the TDIENB bit in the DIC register. DRQ is never asserted when DAV is asserted.
28	VDD	—	**5 V Supply.**

*Indicates 3-state condition.
**Open Drain — Pull-up resistor across output = 1000 Ω minimum.

Registers

The T7111 Synchronous Packet Data Formatter (ANT) contains 12 user-accessible registers. Access to the internal registers is through the bidirectional, multiplexed, address/data bus (AD0—AD3, D4—D7). The four low-order address bits are used to select the 8-bit registers. All of the registers are either read-only or write-only. Writing to a read-only register may result in the loss of data or status information. Reading from a write-only register causes the ANT to return an indeterminate value on the data bus. All reserved bits in a write-only register should be made zero; all reserved bits in a read-only register contain indeterminate values.

Table 2 lists the registers and their characteristics and functions.

Table 2. T7111 Synchronous Packet Data Formatter Registers			
Address	**Symbol**	**Access Type**	**Name/Function**
0000	IS	Write	**Interframe Spacing.** The value in this register, 0—255, determines the number of flags (TC register bit IDL = 0) or octets of 1s (bit IDL = 1) transmitted between frames.
0001	TS	Read	**Transmitter Status.** Indicates status of transmitter (see Table 3). Underrun status conditions are held until the TS register is read.
0010	TC	Write	**Transmitter Control.** Controls termination of frames, loop tests, serial data inversion, and request-to-send handshaking. Inhibits CRC generation by simultaneously setting bits ABT and FC (see Table 4). On a reset, all bit values will be cleared except for IDL. Setting IDL causes the transmitter to default to its idle state.

Table 2. T7111 Synchronous Packet Data Formatter Registers (Continued)			
Address	Symbol	Access Type	Name/Function
0011	TD	Write	**Transmitter Data.** Writes a byte, with a value in the range of 0—255, to the transmitter queue. Writing to TD enables the transmitter from its idle state. The transmit queue is cleared on a hardware reset, master reset, or transmitter reset.
0100	TR	Write	**Transmitter Reset.** A write to this address resets the transmitter and clears TXINT in the interrupt register and the transmitter DMA request. The receiver and MC and DIC registers are not affected.
0101	RS	Read	**Receiver Status.** Indicates status of receiver. Overrun status conditions are held until RS is read (see Table 5). All bits are cleared on reset. Reading the RS register clears the REOF interrupt.
0110	RR	Write	**Receiver Reset.** A write to this address resets the receiver. The transmitter and the MC and DIC registers are not affected. RXINT and REOFINT in the interrupt register and the receiver DMA request are cleared.
0111	RD	Read	**Receiver Data.** Reads a byte, with a value in the range of 0—255, from the receiver queue. The receiver queue is cleared on a hardware, master, or receiver reset, or on an overrun.
1000	MC	Write	**Master Configuration.** These bits determine configuration of selected pins regarding functionality, assertion state, and transmitter and receive enabling (see Table 6). All bits are cleared on hardware reset and master reset.
1001	DIC	Write	**DMA/Interrupt Configuration.** These bits determine configuration of DMA requests and interrupts (see Table 7). All bits are cleared on hardware reset and master reset.
1010	IR	Read	**Interrupt.** Indicates which interrupts are currently active (see Table 8). Reading this register clears the REOF interrupt.
1100	MR	Write	**Master Reset.** A write to this address resets the chip.

Tables 3—8 list the register bit assignments and functions.

Table 3. TS Register Bit Assignments (Read Only)

Bit	Symbol	Name/Function		
0, 1	DF0, DF1	**Encoded Transmission Queue Status.**		
		DF1	**DF0**	**Meaning**
		0	0	No data requested. Implies queue is full or transmitter is not ready to accept new data.
		0	1	Request byte. Indicates queue has space for one more byte.
		1	0	Indicates transmitter underrun.
		1	1	Request word. Indicates queue has space for two more bytes.
2	DONE	**Done.** When bit ACR in the MC register is set, this bit is set after the last bit of a closing flag or an abort sequence is sent to indicate the completed transmission of a frame. It is the inverse of the RTS bit in the TC register and the value of the $\overline{\text{RTS}}$ pin.		
7–3	–	**Reserved.**		

Table 4. TC Register Bit Assignments (Write Only)

Bit	Symbol	Name/Function
0	COU	**Close on Underrun.** Instructs the transmitter to close the frame normally in the underrun state, i.e., with CRC and closing flag. Must be set at least two TCLK cycles before underrun occurs. If this bit is set, the FC bit is not necessary.
1	RTS	**Request-to-Send.** If the LOC bit in the MC register is set, setting this bit activates the $\overline{\text{RTS}}$ pin; clearing this bit deactivates the $\overline{\text{RTS}}$ pin.
2	INV	**Invert.** When set, transmit and receive data streams are inverted.
3	FC	**Frame Close.** Instructs the transmitter to close frame with CRC (ABT=0) or without CRC (ABT=1) after queue clears. If the COU bit is set, this bit is not necessary. Once set, this bit cannot be cleared via software. It is cleared automatically when the last data byte for this frame is transmitted.
4	ABT	**Abort.** Instructs transmitter to abort current frame. When setting abort, COU bit must be cleared. Once set, this bit cannot be cleared via software. It is cleared automatically when the abort sequence begins.
5	IDL	**Idle.** When set, instructs transmitter to enter the idle state when queue is empty. This bit is set whenever a reset occurs. In this state, octets of ones are continuously transmitted. When clear, flags (01111110) are continuously transmitted when the queue is empty.
6	FELT	**Far-End Loop Test.** Places transmitter in far-end loop test mode. All received bits are retransmitted transparently.
7	NELT	**Near-End Loop Test.** Places transmitter in near-end loop test mode. All transmitted bits are looped back to the receiver.

Table 5. RS Register Bit Assignments (Read Only)

Bit	Symbol	Name/Function
0,1	DF0, DF1	**Encoded Receiver Queue Status.** **DF1 DF0 Meaning** 0 0 Null, queue empty. 0 1 Byte available in queue. 1 0 Receiver overrun. 1 1 Two or more bytes available in queue.
2	BBC	**Bad Byte Count**. When set (1), indicates a nonintegral number of bytes have been received.
3	BFRM	**Bad Frame**. When set (1), indicates CRC is not correct. It is set when two or less bytes from a complete frame remain in the queue.
4	GFRM	**Good Frame**. When set (1), indicates CRC is correct. It is set when two or less bytes from a complete frame remain in the queue.
5	IDL	**Idle**. When set (1), indicates the idle sequence (15 ones) is detected.
6	ABT	**Abort**. When set (1), indicates the abort sequence (01111111) is detected after three or more data or CRC bytes have been received.
7	LLI	**Lost Local Interrupt**. This bit is set (1) if there is a change of status frame, idle, abort, or overrun) before the first receiver status has been read.

Table 6. MC Register Bit Assignments (Write Only)

Bit	Symbol	Name/Function
0	ACKPOL	**Acknowledge Polarity**. Determines the assertion state of the DMAACK pin. When cleared (0), DMAACK is active low; when set (1), DMAACK is active high.
1	REOFPOL	**Receiver End-of-Frame Interrupt Polarity**. Determines the assertion state of the REOF interrupt. When cleared, REOF is active low; when set (1), REOF is active high.
2	D/IPOL	**DMA/Interrupt Polarity**. Determines the assertion state of the RXINT/DAV and TXINT/DRQ pins. When cleared, both are active low; when set (1), both are active high.
3	DMA/I	**DMA/Interrupt**. Determines the function of the RXINT/DAV and TXINT/DRQ bits. When cleared, they are interrupts; when set (1), they are DMA requests.
4	ACR	**Auto-Clear RTS**. When the ACR and the LOC bits are set (1), the ANT automatically clears RTS in the TC register at the conclusion of the current frame. When ACR is clear, bit RTS must be cleared via software. If the ACR feature is used, the IS register must have a value of at least 1 to prevent shared flags between frames.
5	LOC	**Level One Control**. When cleared (0), $\overline{\text{CTS}}$ (pin 19) and $\overline{\text{RTS}}$ (pin 20) are disabled and the level one control function is not implemented. When set (1), both $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ must be active for data to be transmitted.
6	TENB	**Transmitter Enable**. When set (1), allows data to be output via TXD (pin 22). When cleared, TCLK is ignored and TXD is 3-stated.
7	RENB	**Receiver Enable**. When set (1), allows data to be input via RXD (pin 23). When cleared, the RXD input is ignored; the internal state of the receiver is not affected.

Table 7. DIC Register Bit Assignments (Write Only)

Bit	Symbol	Name/Function
1, 0	TEL1, TEL0	**Transmitter Empty Level.** Establishes the number of empty bytes in the transmitter queue that will trigger a transmitter interrupt or DMA request. Encoded as: 00 4 bytes empty (default). 01 1 or more bytes empty. 10 2 or more bytes empty. 11 3 or more bytes empty.
3, 0	RFL1, RFL0	**Receiver Fill Level.** Establishes the number of bytes in the receiver queue that will trigger a receiver interrupt of DMA request. Encoded as: 00 4 bytes available (default). 01 1 or more bytes available. 01 2 or more bytes available. 11 3 or more bytes available.
4	REOFENB	**Receiver End-of-Frame Interrupt Enable.** When MENB and REOFENB are set (1), REOFINT (pin 25) is enabled. Disabling the REOFINT does not clear the existing interrupt.
5	TDIENB	**Transmitter DMA/Interrupt Enable.** When MENB and TDIENB are set, TXINT/DRQ (pin 27) is enabled. Disabling TXINT/DRQ does not clear the existing interrupt.
6	RDIENB	**Receiver DMA/Interrupt Enable.** When MENB and RDIENB are set (1), RXINT/DAV (pin 26) is enabled. Disabling the RXINT/DAV does not clear the existing interrupt.
7	MENB	**Master Enable.** When cleared (0), disables all DMA and interrupt outputs. When set (1), along with TDIENB, RDIENB or REOFENB, all DMA and interrupt outputs are enabled.

Table 8. I Register Bit Assignments (Read Only)

Bit	Symbol	Name/Function
0—4	—	**Reserved.**
5	REOFINT	**Receiver End-of-Frame Interrupt.** When set (1), indicates the receiver end-of-frame interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore, this bit remains set if the interrupt enable bits are disabled. This bit is cleared (0) after this register, or the RS register, is read.
6	TXINT	**Transmitter Interrupt.** When set (1), indicates the transmitter queue interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore this bit remains set if the interrupt enable bits are disabled.
7	RXINT	**Receiver Interrupt.** When set (1), indicates the receiver queue interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore this bit remains set if the interrupt enabled bits are disabled.

Operation

The T7111 Synchronous Packet Data Formatter operates with a system clock frequency of 2—8 MHz. The frequency of operation is dependent upon the host microprocessor operating frequency, but does not have to be synchronous with it. See **Read/Write Cycles** for a complete description. Serial data is transmitted on TXD (pin 22) and output on the high-to-low transition of TCLK. Serial data is able to be transmitted when $\overline{RTS}$ and $\overline{CTS}$ are active (low) if the LOC bit in the MC register is set. Otherwise, these pins are ignored. Serial data is received from RXD (pin 23) and sampled on the rising edge of RCLK (see Figure 3).

16-bit Polynomial Cyclic Redundancy Check (CRC-CCITT) and Generation with Inhibit Option. As the transmitter shifts serial data out for a frame, it computes the 16-bit CRC-CCITT pattern. The frame close (FC) bit in the transmitter control (TC) register is set by the host processor after the last data byte is written to the TD register, unless the COU bit has been set. Both the DF0 and DF1 bits in the transmitter status (TS) register are cleared (00), no data requested, to stop the transmitter from requesting data. When the last data byte has been transmitted, and the CRC has begun, the transmitter is ready to accept new data, and sets the DF0 and DF1 status bits (11), word requested. After the CRC pattern is transmitted, a flag is appended to the pattern and data for a new frame, if available, is transmitted. The CRC pattern is not appended to the data if the abort bit is set at the same time as the FC. The transmitter closes the frame with a flag after the last data byte. When the CRC option is not in use, the IDL bit in the TC register must be cleared.

As the receiver shifts the serial data input for a frame, it computes the CRC pattern. When the closing flag is received, the last two data bytes received are assumed to be CRC, and are cleared from the queue. If no more than two bytes from the frame remain in the queue, the receiver sets either the GFRM or BFRM status bit, depending on whether or not the CRC matches. If the BFRM bit is set, the remaining data must still be read out from the queue.

Abort/Idle Detection and Transmission. When the receiver recognizes the abort sequence (seven successive 1s), data from the current frame and the CRC are cleared. Data from a following frame is written to the queue after a flag is recognized. If an abort sequence is received when less than three complete bytes have been received, the abort bit is not set. If three or more bytes have been received, but there is outstanding data, or an outstanding end-of-frame condition from a previous frame in the queue, the lost local interrupt (LLI) bit is set. When the receiver recognizes the idle sequence (15 successive 1s), the IDL bit in the RS register is set. It remains set as long as the link remains idle.

When the ABT bit in the TC register is set, the transmitter is instructed to abort the current frame. The transmitter shifts out the rest of the current data byte and then transmits the abort sequence. The queue and the CRC generator are cleared and the transmitter is ready to accept data from a new frame. If no new data is written and the IDL bit in the TC register is set, the transmitter is in the idle state where it continuously transmits octets of 1s until data is available. If no new data is written and the IDL bit is cleared, the transmitter transmits flags until data is available.

The value of the IDL bit also determines the interframe spacing pattern. If it is set, a number of octets of 1s equal to the interframe spacing value are transmitted between the closing and opening flags of successive frames. When the transmitter is idling and data is written to the TD register, a number of octets of 1s equal to the interframe spacing value are transmitted before that frame. The first byte written signals the start of the interframe spacing count.

Transmitter Underrun and Receiver Overrun Detection. During transmission of a frame, the transmitter underruns if neither the frame close (FC) bit nor the COU bit in the TC register is set by the time the last data byte is shifted out. The abort sequence follows the last byte shifted out during underrun. If the queue is empty, the transmitter transmits flags (IDL = 0) or octets of 1s (IDL = 1) following the abort sequence.

The underrun condition is reflected in the transmitter status bits. Writes to the FC and ABT bits, and to the TD register are ignored until the status is read. After the status has been read, the transmission queue status bits, DF(0, 1), are set to word requested. If the ACR bit is set, RTS will be deactivated at the end of the abort sequence.

If the six byte limit on the receive queue is exceeded, i.e., data is received faster than it is read out, the receiver will enter the overrun state. The receiver queue status bits, DF0 and DF1, reflect the overrun condition.

On an overrun, the receiver queue is cleared and cannot be read until the RS register is read. Received data from a subsequent frame can be written to the queue. If a second overrun occurs before the first status is read, no more data is accepted until after the status is read and LLI is set. After the overrun status is read, the status reflects the number of bytes currently available in the queue.

Automatic Flag Transmission and Detection with Programmable Interframe Spacing. When data is written to the transmit queue, the transmitter automatically generates an opening flag before it transmits the data. When the FC bit in the TC register is set, a closing flag is appended to the frame after the CRC pattern. If the queue is not empty when the closing flag is sent, the next frame begins immediately. If the interframe spacing value is zero, a single flag serves the dual role of closing and opening flag for the two frames. If two separate flags are required, the interframe spacing value should be set to one. When IDL = 0, the number of flags equal to the interframe spacing value are transmitted after the closing flag and before the data for the next frame. If IDL = 1, a number of octets of 1s equal to the interframe spacing value are transmitted after the closing flag and before the opening flag for the next frame. After the transmitter is reset, if data is in the transmit queue, it transmits one flag before the first frame, and appends the IS value of flags or octets of 1s after the closing flag. When two successive flags occur, a full sixteen bits are transmitted, i.e., 0111111001111110.

The receiver recognizes the pattern 01111110 as a flag. Two successive flags may or may not share the intermediate zero bit and still be recognized, i.e., 0111111001111110 or 011111101111110. When the receiver queue is empty and it recognizes a flag, it begins to format the subsequent bits into bytes until it recognizes another flag or an abort sequence. The bytes are stored in the six byte receiver queue. When the closing flag is recognized, the last two bytes are cleared from the queue for the CRC pattern. The GFRM, BFRM, or BBC bits in the receiver status (RS) register are set when two or less bytes from the frame remain in the receiver queue. If a second frame is completed before the status from the first frame has been read, the LLI bit in the RS register is set, and the data from the second frame is cleared from the queue.

Zero Bit Insertion and Deletion. When five successive 1s occur in either the data or CRC to be transmitted, the transmitter automatically inserts a zero bit after the fifth 1, regardless of the value of the next bit. When five successive 1s followed by a zero are received, the zero is assumed to have been inserted by the transmitter and is ignored. This eliminates the possibility of misinterpreting data or CRC patterns as flag, abort, or idle patterns.

Request-to-Send/Clear-to-Send Level One Functions. The $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ pins can be programmed to perform request-to-send/clear-to-send handshaking with a physical link controller. When the level one control (LOC) bit in the MC register is set, the specified protocols are performed. The host processor must set, by software, the RTS bit in the TC register when it is ready to begin transmission of a new frame. The $\overline{\text{RTS}}$ pin is activated when the RTS bit is set.

The RTS bit is cleared, causing the $\overline{\text{RTS}}$ pin to become inactive upon a hard reset (pin 15 asserted), a software reset, or a transmitter reset. In addition to the reset conditions, if auto-clear RTS is active

(ACR = 1), the RTS bit is cleared and the $\overline{RTS}$ pin is deactivated when one of the following conditions occurs:

- end of the closing flag of a normal frame
- end of the abort sequence of an aborted frame
- end of the abort sequence after an underrun.

If the ACR feature is used, the interframe spacing register must be set to a value of at least one. This is necessary to ensure separate closing and opening flags. RTS is cleared at the end of the closing flag. When the transmitter is reactivated, a number of flags equal to the setting of the IS register are transmitted before the first data byte. If the abort bit is set while the transmitter is sending the opening flag of the frame, the abort pattern is not transmitted. RTS clears as soon as this bit is set, causing transmission to stop. The next time RTS is set, the remaining bits of the flag are sent before the new frame begins.

If the ANT device is not in auto-clear RTS (ACR = 0) mode, the only condition that clears RTS, other than the reset conditions, is a write to that bit in the TC register.

When the LOC bit in the MC register is set, the clear-to-send ($\overline{CTS}$) input pin is enabled. When $\overline{CTS}$ is enabled, the level one controller responds to the assertion of $\overline{RTS}$ with the assertion of $\overline{CTS}$ when the physical link is available for transmission by the ANT device. The ANT device responds by transmitting as long as both $\overline{RTS}$ and $\overline{CTS}$ are active (low). If the queue is empty, the transmitter transmits either flags or octets of 1s until data is available. When $\overline{CTS}$ is enabled but inactive (high), the transmitter is disabled from transmitting anything across the serial interface. The TXD (pin 22) is 3-stated.

The DONE bit in the TS register reflects the state of the $\overline{RTS}$ pin. It is clear while $\overline{RTS}$ is asserted low; it is set when $\overline{RTS}$ is negated. It is used by the host processor to determine whether RTS may be set for the transmission of another frame. If ACR = 1, and RTS is set for another frame before it is cleared from the previous frame, RTS is cleared at the end of the first frame, but the output will not be reasserted unless set via software.

Near-End and Far-End Loop Test Modes. When the NELT bit in the TC register is set, the ANT device is in the near-end loop test mode. In this mode, all data that is transmitted on the TD line is looped back internally to the receiver. The receiver cannot distinguish between the looped back data and data received normally; therefore all status, configuration, and interrupt conditions will function as usual.

Setting the FELT bit in the TC register puts the ANT device in the far-end loop test mode. In this mode, all received data will be echoed by the transmitter in a "dumb" fashion, while the receiver functions as usual.

Read/Write Cycle. To perform a read or write operation the chip select ($\overline{CS}$) pin must be low (active) for the duration of the read or write pulse. In addition, $\overline{CS}$ may only change state when ALE is high. This ensures the integrity of the read and write operations.

On a write cycle, RDY is driven high by the ANT device as soon as $\overline{WR}$ goes low. Data is latched by the ANT device on the low-to-high transition of $\overline{WR}$. A wait state will be inserted in any read cycle that begins less than two clock cycles after a write. Another write cycle may immediately follow the previous write cycle write cycle (see Figure 4).

The ANT's read cycle begins with the falling edge of ALE. On the first rising edge of CLK, following the first falling edge of CLK, RDY is driven high. The read data is driven on the next falling edge of CLK, and is valid one clock cycle after RDY goes high. Neither RDY nor the data bus are driven until the $\overline{RD}$ signal is driven low (see Figure 5).

If $\overline{CS}$ is active and a read address is present on AD0—AD3 when the falling edge of ALE occurs, a read cycle is initiated. regardless of whether a read strobe follows. This may cause the loss of data or status information. Therefore, the device must have a unique chip select that is only activated when a read or write to the ANT is desired.

The 8051 Microcontroller requires a clock input from a crystal or a square wave source. If a crystal is used, the ANT device must be clocked asynchronously; if a square wave source is used, the ANT device may be clocked synchronously or asynchronously. Since the 8051 Microcontroller does not have wait-state capability, the ANT device is required to respond quickly to an 8051 Microcontroller read cycle. The relationship between the period of the microcontroller's clock (t8051) and the the ANT's clock (tANT) is given by:

$$tANT \leq (16/3)T8051 - 175 \text{ ns}$$

For example, to be compatible with an 8051 Microcontroller operating with a 12 MHz clock, the ANT device requires an input clock of at least 3.75 MHz.

The 8088 Microprocessor requires a square wave clock input with a 33% duty cycle. The ANT device can be supplied with the same clock input and operate synchronously with the microprocessor. The ANT device is compatible with a 33% duty cycle clock at 8 MHz as specified for the 8088 Microprocessor, i.e., minimum clock high time of 44 ns.

If the ANT device operates with the same system clock as the microprocessor, it is not necessary to insert wait states into the 8088 Microprocessor read or write cycles. When using an independent clock, wait states may be inserted depending upon relative frequencies and phase differences between the clocks.

The 80188 Microprocessor requires a clock input from either a crystal or a square wave source. The microprocessor provides a 50% duty cycle square wave output of one-half the frequency of the clock input. If the microprocessor's clock output is the ANT's system clock input, the ANT device can operate with a frequency of up to 8 MHz without inserting wait states into the 80188 Microprocessor read or write cycles.

DMA Read/Write. The 8237 and 8257 DMA Controllers must be configured for the extended write mode for compatibility with the T7111 ANT. When the DMA/I bit in the MC register is set, RXINT/DAV and TXINT/DRQ function as DMA request pins. Their assertion state, along with that of DMAACK, is determined by the status of D/IPOL (bit 2), and ACKPOL (bit 0), respectively, in the MC register. The data available (DAV) and data request (DRQ) pins are never asserted at the same time. The assertion is determined by a revolving priority scheme, where the DMA serviced most recently has the lower priority. DAV is asserted when the receiver queue fill level is equal to or greater than the setting of the receiver fill level (RFL) bits (0,1) in the DMA/interrupt configuration (DIC) register. It remains asserted until the queue is empty. DRQ is asserted when the transmitter queue has room to accommodate a number of bytes equal to or greater than the setting of the transmitter empty level (TEL) bits (2, 3) in the DIC register. It remains asserted until the queue is full.

After DAV is asserted, if a DMAACK is received, the ANT device drives a byte of data from the receiver queue onto the bus after the read strobe ($\overline{RD}$) signal is cleared (0). After the high-to-low transition of the read strobe, the ready (RDY) signal is driven high (active) on the first rising edge after the first falling edge of the system clock (CLK) after $\overline{RD}$ is asserted. Data is valid by the next rising edge of CLK (see Figure 6).

If DRQ is asserted and a DMAACK signal is received, the ANT device latches a byte of data from the bus into the transmitter queue on the low-to-high transition of the write strobe ($\overline{WR}$) signal. The RDY

signal is driven high as soon as $\overline{WR}$ goes low (see Figure 7). DMAACK must be active for the duration of the read or write pulse to ensure correct operation. $\overline{CS}$ and the address bus inputs are not needed for DMA transfers.

Interrupts. The ANT device may be programmed to provide three separate interrupts: receiver, transmitter, and receiver end-of-frame. The interrupts are enabled by setting the appropriate bits in the DIC register: RDIENB (bit 6), TDIENB (bit 5) and REOFENB (bit 4), respectively. The assertion state of the bits is determined by the value of the appropriate bits in the MC register. REOFINT becomes active upon reception of the last bit of the closing flag of a frame, the last bit of an abort sequence, or upon overrun, providing there are no outstanding data bytes or status bits from a previous frame. If data or status is outstanding, the second frame is lost and the LLI bit in the receiver status (RS) register is set. REOFINT remains asserted until the I register or the RS register is read, unless disabled via the DIC register.

When the DMA/I bit in the MC register is clear (0), RXINT/DAV and TXINT/DRQ function as interrupts. RXINT is asserted when the receiver queue fill level is equal to or greater than the setting of the RFL bits in the DIC register. RXINT is not asserted when the queue overruns, but REOFINT is asserted. TXINT is asserted upon underrun or when the transmitter queue has enough empty slots to accommodate a number of bytes equal to or greater than the setting of the TEL bits in the DIC register. Once the FC bit has been set, TXINT will be negated until the transmission of that frame is completed. TXINT remains asserted if the queue underruns. When servicing the TXINT, the TS register must be read before data is written into the TD register.

Reset. The reset signal must be held high for at least four clock cycles to reset the ANT device. All registers are cleared on reset, except the IDL bit in the TC register. The receive and transmit queues are cleared also. All output pins are 3-stated for as long as the reset signal is held high. The ANT device is guaranteed to be fully reset within 3 clock cycles after the high-to-low transition of reset. A write to the master reset address (1100) has the same effect as a hardware reset. The ANT device is fully reset within 3 clock cycles of the low-to-high transition of the $\overline{WR}$ pulse.

A write to the receiver reset address (0110) resets the receiver only. The RS register and the receive queue are cleared. The transmitter, MC, and DIC registers are not affected. The receiver queue and end-of-frame interrupts in the interrupt register and the receiver DMA request are also cleared. The receiver is fully reset within 3 cycles of the low to high transition of the $\overline{WR}$ pulse.

A write to the transmitter reset address (0100) resets the transmitter. The TS register and transmitter queue are cleared along with the transmitter interrupt in the interrupt register and the the transmitter DMA request. The receiver and the MC and DIC registers are not affected by this write. The transmitter is fully reset within 3 cycles of the low-to-high transition of the $\overline{WR}$ pulse.

CHARACTERISTICS

Clocks

System Clock Input:	2—8 MHz
Transmit Data Clock:	Maximum frequency = CLK/2, no minimum frequency
Receive Data Clock:	Maximum frequency = CLK/2, no minimum frequency

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current	I_{DD}	—	40	mA	T_A = 0 °C
Input Current					
High Level (Logic 1)	I_{IH}	—	7.5	μA	V_{IH} = 5.5 V
Low Level (Logic 0)	I_{IL}	—	7.5	μA	V_{IL} = 0 V
Input Current — Bidirectional Pins					
High Level (Logic 1)	I_{IH}	—	−37.5	μA	V_{IH} = 5.5 V
Low Level (Logic 0)	I_{IL}	—	37.5	μA	V_{IL} = 0 V
Output 3-State Leakage Current					
High Level (Logic 1)	I_{OZH}	—	−30	μA	V_{OH} = 5.5 V
Low Level (Logic 0)	I_{OZL}	—	30	μA	V_{OL} = 0 V
Input Voltage					
High Level (Logic 1)	V_{IH}	2.0	—	V	—
Low Level (Logic 0)	V_{IL}	—	0.8	V	—
Output Voltage					V_{DD} = 4.5 V
High Level (Logic 1)	V_{OH}	2.4	—	V	I_{OH} = −2.4 mA
Low Level (Logic 0)	V_{OL}	—	0.4	V	I_{OL} = 2.4 mA
Power Dissipation	PD	—	80	mW	V_{DD} = 5.5 V T = 70 °C CLK = 8 MHz TCLK = RCLK = 4 MHz

Maximum Ratings

DC Supply Voltage (V_{DD}) ..... 7 V
Input Voltage Range (V_I) ..... (V_{SS} − 0.5) to (V_{DD} + 0.5) V
Ambient Operating Temperature Range (T_A) ..... 0 to 70 °C
Storage Temperature Range (Tstg) ..... −40 to +125 °C

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Timing Characteristics for Serial Transmit and Receive Data Cycle (See Figure 3)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLLCLL	CLK Period	125	500	ns
tTCHTCH	TCLK Period	2tCLLCLL	–	ns
tTCHTCL	TCLK High	40	–	ns
tTCLTCH	TCLK Low	60	–	ns
tTCHRTL	TCLK High to $\overline{\text{RTS}}$ Low	–	30	ns
tTCHRTH	TCLK High to $\overline{\text{RTS}}$ High	–	50	ns
tCTLTCL	$\overline{\text{CTS}}$ Set-Up to TCLK Low	25	–	ns
tCTHTCL	$\overline{\text{CTS}}$ Set-Up to TCLK Low	25	–	ns
tTCLTDV	TCLK Low to Data Valid	–	50	ns
tRCHRCH	RCLK Period	2tCLLCLL	–	ns
tRDVRCH	RXD Set-Up to RCLK High	20	–	ns
tRCHRDX	RXD Hold After RCLK High	10	–	ns

Timing Characteristics for ANT Write Cycle (See Figure 4)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLLCLL	CLK Period	125	500	ns
tCLHCLL	CLK High	44	–	ns
tCLLCLH	CLK Low	48	–	ns
tCSLALL	$\overline{\text{CS}}$ Set-Up to ALE Low	10	–	ns
tWRHCSH	$\overline{\text{CS}}$ Hold After $\overline{\text{WR}}$ High	20	–	ns
tWRLWRH	$\overline{\text{WR}}$ Pulse Width	30	–	ns
tWRLRYH	$\overline{\text{WR}}$ Low to RDY High	–	50	ns
tWRHRYZ	$\overline{\text{WR}}$ High to RDY High-Z	–	20	ns
tDBVALL	Address Set-Up to ALE Low	30	–	ns
tALLDBX	Address Hold After ALE Low	0	–	ns
tDBVWRH	Data Set-Up to $\overline{\text{WR}}$ High	30	–	ns
tWRHDBX	Data Hold After $\overline{\text{WR}}$ High	10	–	ns

Timing Characteristics for ANT Read Cycle (See Figure 5)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLLCLL	CLK Period	125	500	ns
tCLHCLL	CLK High	44	—	ns
tCLLCLH	CLK Low	48	—	ns
tCSLALL	$\overline{CS}$ Set-Up to ALE Low	10	—	ns
tREHCSH	$\overline{CS}$ Hold After $\overline{RD}$ High	20	—	ns
tCLHRYH	CLK High to RDY High	—	40	ns
tREHRYZ	$\overline{RD}$ High to RDY High-Z	—	40	ns
tALLDBX	Address Hold After ALE Low	0	—	ns
tDBZREL	Data Bus High-Z to $\overline{RD}$ Low	0	—	ns
tRELDBX	$\overline{RD}$ Low to Data Bus Driven	—	60	ns
tCLLDBV	CLK Low to Data Valid	—	60	ns
tREHDBZ	$\overline{RD}$ High to Data Bus High-Z	—	30	ns
tRELRYL	$\overline{RD}$ Low to RDY Low	—	40	ns

Timing Characteristics for DMA Read Cycles (See Figure 6)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLLCLL	CLK Period	125	500	ns
tCLHDAH	CLK High to DAV High	—	120*	ns
tRELDAL	$\overline{RD}$ Low to DAV Low	—	45	ns
tDAHDMH	DAV High to DMAACK High	0	—	ns
tDMHREL	DMAACK High to $\overline{RD}$ Low	20	—	ns
tRELREH	$\overline{RD}$ Pulse Width	2tCLLCLL+60	—	ns
tREHDML	DMAACK Hold after $\overline{RD}$ High	10	—	ns
tRELREL	DMA Read Interval	3tCLLCLL	—	ns
tRELRYL	$\overline{RD}$ Low to RDY Low	—	40	ns
tCLHRYH	CLK High to RDY High	—	40	ns
tRELDBV	$\overline{RD}$ Low to Data Valid	tCLLCLL	2tCLLCLL+60	ns
tREHRYZ	$\overline{RD}$ High to RDY High-Z	—	40	ns
tREHDBZ	$\overline{RD}$ High to Data High-Z	—	30	ns
tRELDBX	$\overline{RD}$ to Data Driven	—	60	ns
tCLLDBV	CLK Low to Data Valid	—	60	ns

*Pull-up resistor = 1 kΩ

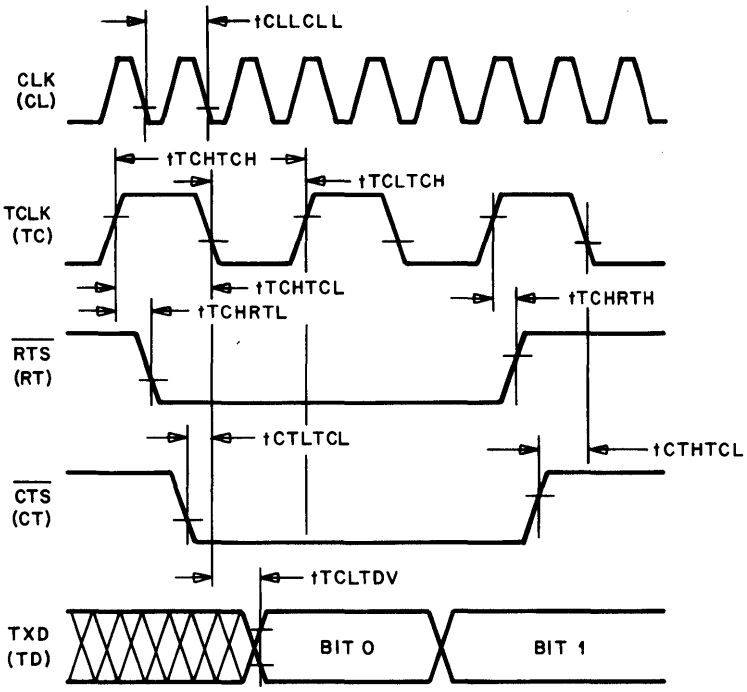
Timing Characteristics for DMA Write Cycles (See Figure 7)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLLCLL	CLK Period	125	500	ns
tCLHDRH	CLK High to DRQ High	–	120*	ns
tWRLDRL	$\overline{WR}$ Low to DRQ Low	–	40	ns
tDRHDMH	DRQ High to DMAACK High	0	–	ns
tDMHWRL	DMAACK High to $\overline{WR}$ Low	20	–	ns
tWRLWRH	$\overline{WR}$ Pulse Width	30	–	ns
tWRHWRH	DMA Write Intervals	3tCLLCLL	–	ns
tWRHDML	DMAACK Hold After $\overline{WR}$ High	10	–	ns
tWRLRYH	$\overline{WR}$ Low to RDY High	–	50	ns
tWRHRYZ	$\overline{WR}$ High to RDY High-Z	–	20	ns
tDBVWRH	Data Set-Up to $\overline{WR}$ High	30	–	ns
tWRHDBX	Data Hold After $\overline{WR}$ High	10	–	ns

*Pull-up resistor = 1 kΩ

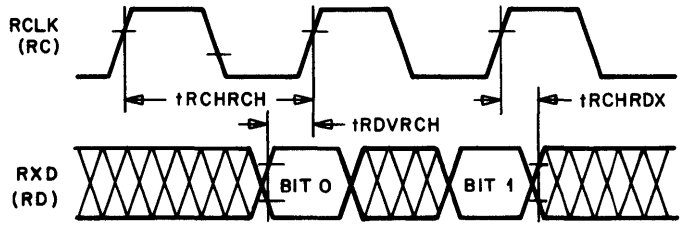
Timing Characteristics for Interrupts				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLHRFL	CLK High to REOFINT Low	–	60	ns
tCLHRFH	CLK High to REOFINT High	–	130*	ns
tCLHRIL	CLK High to RXINT Low	–	50	ns
tCLHRIH	CLK High to RXINT High	–	110*	ns
tCLHTIL	CLK High to TXINT Low	–	50	ns
tCLHTIH	CLK High to TXINT High	–	110*	ns

*Pull-up resistor = 1 kΩ

Timing Diagrams



A. Transmit Data Cycle



B. Receive Data Cycle

Figure 3. Serial Transmit and Receive Data Cycle

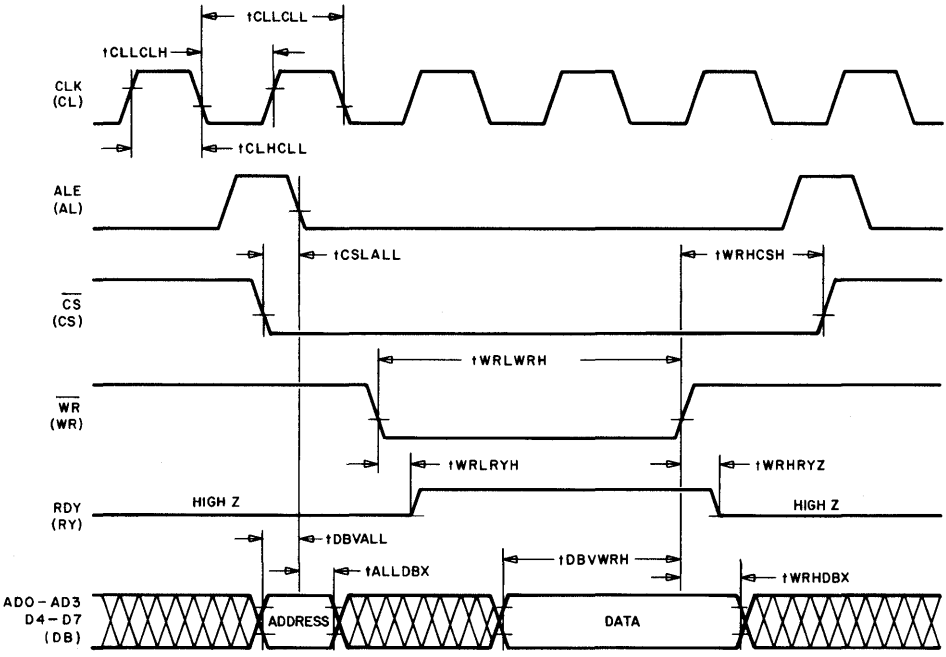


Figure 4. Write Cycle

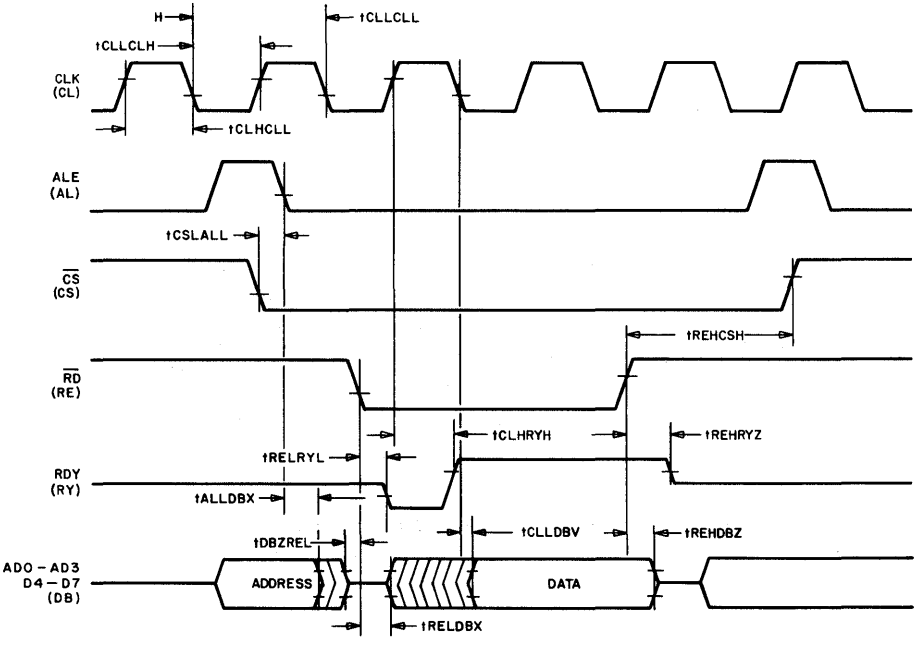
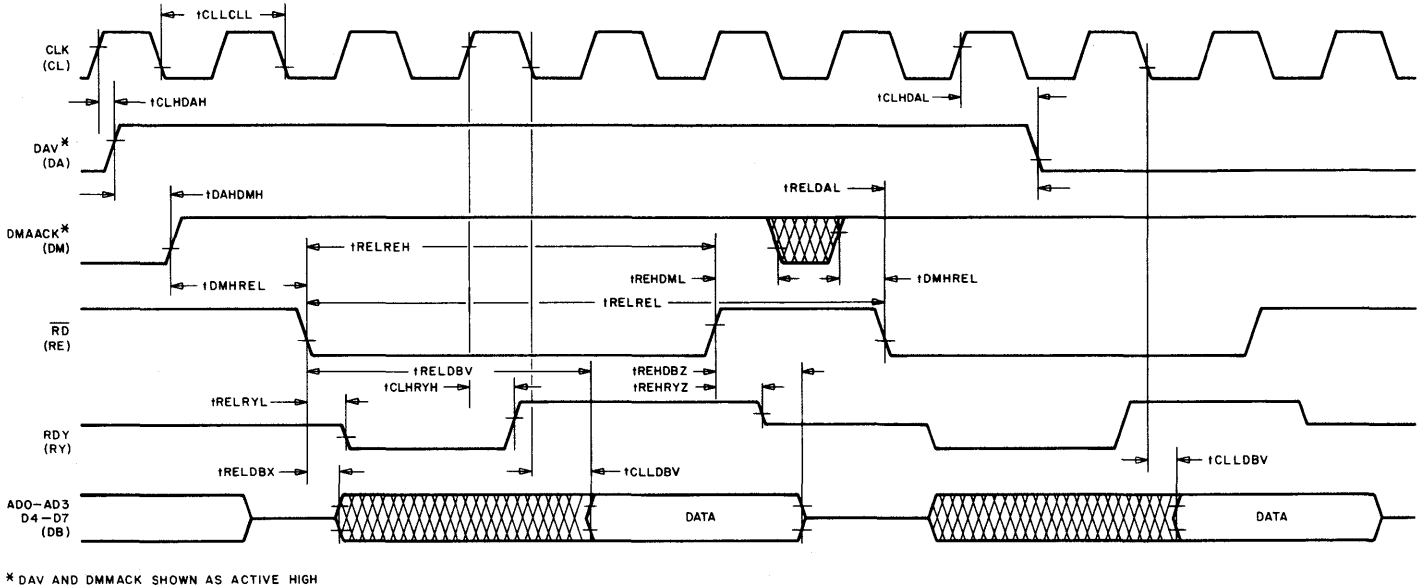


Figure 5. Read Cycle



*DAV AND DMMACK SHOWN AS ACTIVE HIGH

Figure 6. Consecutive DMA Read Cycles

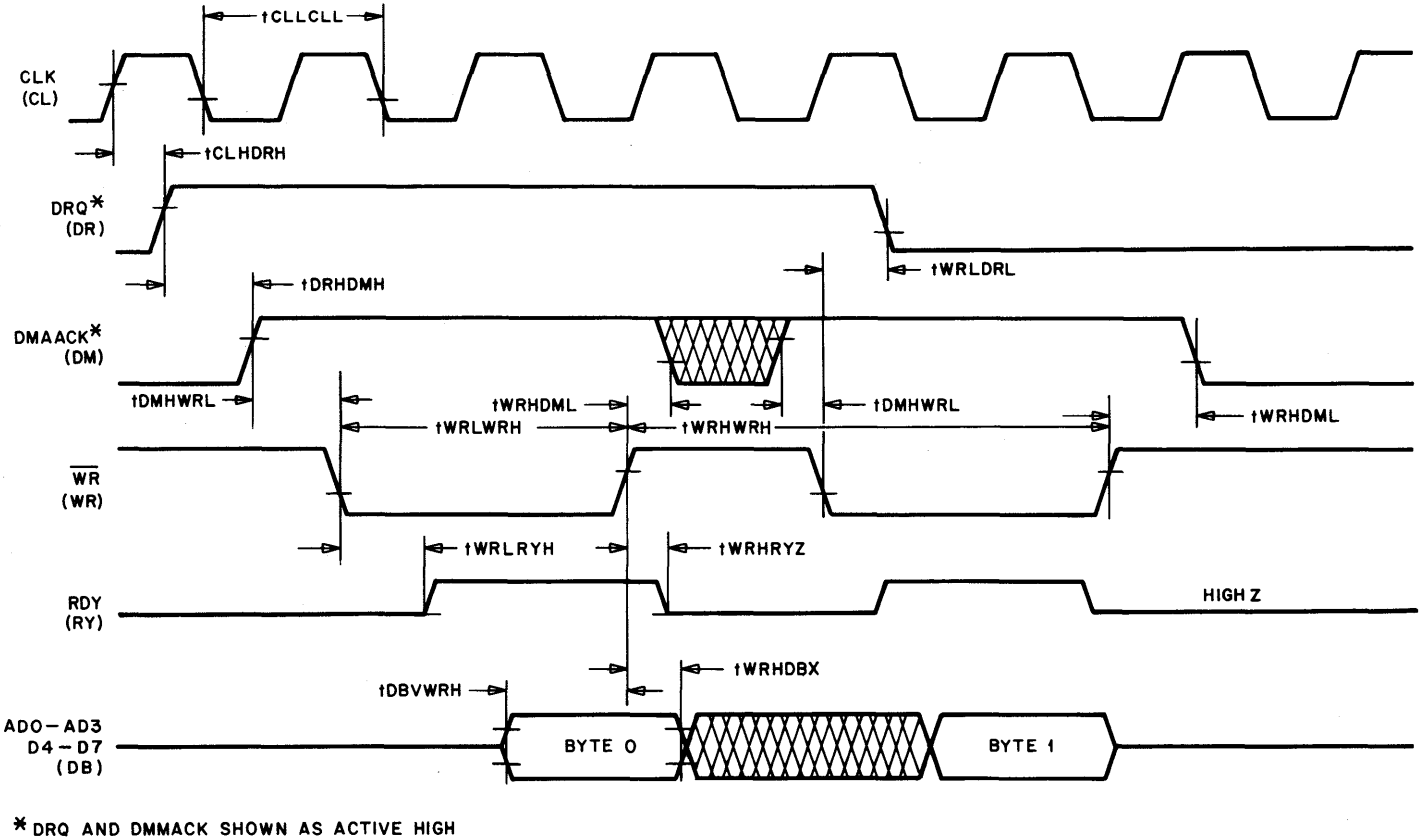


Figure 7. Consecutive DMA Write Cycles

FEATURES

The information contained herein is preliminary and subject to change.

- Full-duplex asynchronous transmitter/receiver
- Six receive and four transmit data buffers
- Programmable data format
  - 8 data bits
  - 7 data bits plus parity
  - Odd, even, one, zero, no parity
  - 1 or 2 stop bits (transmit)
- Parity, framing, and overrun error detection
- Speed matching (autobaud capability)
- 10-bit start/stop serial data
- DTR/DSR general-purpose I/O pins
- Transmit/receive FIFO status bits indicate FIFO levels
- On-chip baud rate generator
- TTL-compatible with 3-statable outputs
- Flexible polling capabilities
- Interrupt on empty level of transmit FIFO
- Interrupt on fill level of receive FIFO
- Interrupt on receive break detect
- Interrupt on error conditions
- Single 5 V power supply

DESCRIPTION

The T7112 Asynchronous Receiver/Transmitter Interface (ARTI) integrated circuit is an asynchronous, single channel, full-duplex receiver/transmitter interface for terminals and modems. The ARTI device is compatible with the bus protocol and timing specifications of the 8051 microcontroller and the 8088 and 80188 microprocessors. It may be used in a polled or interrupt driven system. The transmitter has a quadruple buffer and the receiver has six buffers to reduce the interrupt overhead and the potential for overruns. The speed matching feature of this device allows it to detect and automatically adjust to the received baud rate. The device is implemented in low-power CMOS technology and is available in a 24-pin plastic DIP (T7112-PC) or a 28-pin SOJ (T7112-EC).

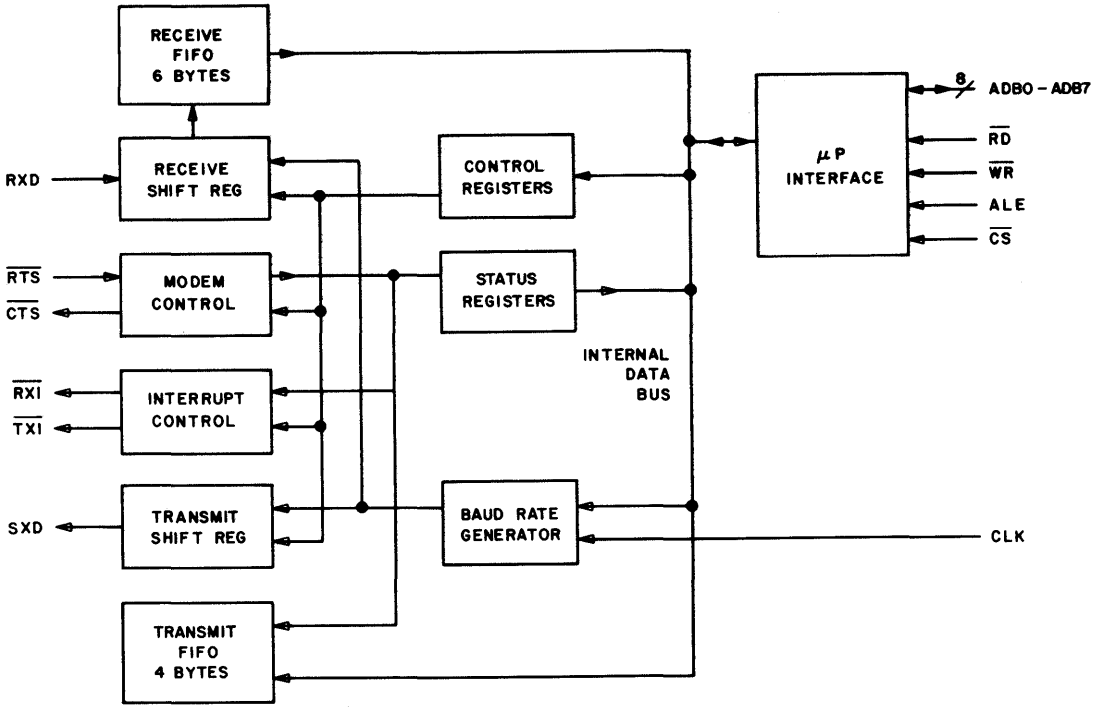


Figure 1. T7112 ARTI Block Diagram

USER INFORMATION

Pin Descriptions

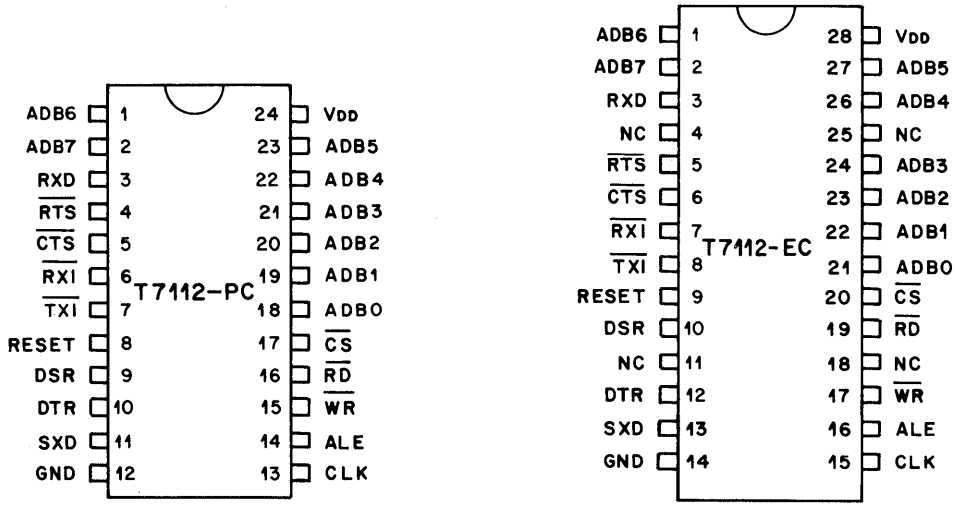


Figure 2. T7112-PC and T7112-EC Pin Function Diagrams

Table 1. T7112 Pin Descriptions

Symbol	Type	Name/Function
ADB0—ADB7	I/O	**Address/Data Bus Bits 0—7.** These eight leads are the microprocessor address/data bus and are bidirectional.
RXD	I	**Receive Data.** Serial receive data input.
$\overline{\text{RTS}}$	I	**Request to Send.** When the ARTI is in the DCE mode with the CTS/RTS control enabled, this active low input requests transmission of data to the ARTI. When the ARTI is in the DTE mode, this input enables transmission from the ARTI. When the CTS/RTS control is not enabled, the RTS is an inverting general-purpose input.
$\overline{\text{CTS}}$	O	**Clear to Send.** When the ARTI is configured in the DCE mode with CTS/RTS control enabled, this active-low output indicates that the ARTI is ready to receive data. When enabled in the DTE mode, this output indicates there is transmit data to be sent. When the CTS/RTS control is disabled, the CTS output is a general-purpose inverting output.

Table 1. T7112 Pin Descriptions (Continued)

Symbol	Type	Name/Function
$\overline{RXI}$	O	**Receive Interrupt Output.** This output is active low and remains active for at least one master clock period. It is 3-stated when not on. It must be pulled high with an external resistor to achieve proper logic levels. It may be wire ANDed with the $\overline{TXI}$ output for a common interrupt to the microprocessor.
$\overline{TXI}$	O	**Transmit Interrupt Output.** This out is active low and remains active for at least one mast clock period. It is 3-stated when not on. It must be pulled high with an external resistor to achieve the proper logic levels. It may be wire ANDed with the $\overline{RXI}$ output for a common interrupt to the microprocessor.
RESET	I	This active high input resets the ARTI. All outputs are 3-stated and ADB0—ADB7 are configured as inputs.
DSR	O	**Data Set Ready.** General-purpose noninverting output from the ARTI.
DTR	I	**Data Terminal Ready.** General-purpose noninverting input to the ARTI.
SXD	O	**Serial Transmit Data.**
GND	—	**Ground Reference.**
CLK	I	**Master Clock Input.**
ALE	I	**Address Latch Enable.** In all modes, this signal indicates a valid address is on the address/data bus.
$\overline{WR}$	I	**Write Input.** Active low.
$\overline{RD}$	I	**Read Input.** Active low.
$\overline{CS}$	I	**Chip Select.** Active low.
V_{DD}	—	**5 V Positive Power Supply.**

Overview

The T7112 ARTI provides a communication link between an 8-bit microprocessor (8088, 80188, or 8051) and a serial asynchronous peripheral. The operation is similar to a classical UART except there are FIFOs at both the transmit and the receive side, instead of the usual single register. Programmable interrupt capability is provided. Set-up of the ARTI device is done by the processor writing to control registers. In addition to data, the ARTI device provides registers to be read that contain error status, set-up status, and FIFO status.

Write Registers

Write Register 0 (Table 3) contains the transmit data byte from the microprocessor. Bit D7 is ignored if the parity is enabled. These bits are cleared (0) by a RESET.

Table 2. ARTI Write/Read Registers*

ARTI Write Registers

D7	D6	D5	D4	D3	D2	D1	D0	Register	Address (Hex)
d7	d6	d5	d4	d3	d2	d1	d0	0	00
RXEN	TXEN	PAREN	EV/ODD	PEO/10	P1/0	BRGEN	CTS	1	01
DTE/ DCE	CTS/ RTSHAND	BKGEN	INTEN	TXIEN	RXIEN	STBT	1	2	02
br7	br6	br5	br4	br3	br2	br1	br0	3	03
DSR	RESET	TXRST	RXRST	SPMAT	br10	br9	br8	4	04
TDFB	TDFA	RDFC	RDFB	RDFA	ERRINT	RTSINT	BKINT	5	05

ARTI Read Registers

D7	D6	D5	D4	D3	D2	D1	D0	Register	Address (Hex)
d7	d6	d5	d4	d3	d2	d1	d0	0	00
RXCH	RFSC	RFSB	RFSA	TXCH	TFSb	TFSa	1	1	01
BKDET	RTS	$\overline{\text{RXINT}}$	$\overline{\text{TXINT}}$	RXOR	TXUR	FRERR	PARERR	2	02
br7	br6	br5	br4	br3	br2	br1	br0	3	03
DTR	AS	1	1	SPMAT	br10	br9	br8	4	04

*The default condition for all bits is 0, except for the following:
RDFA=1, $\overline{\text{RXINT}}$=1, $\overline{\text{TXINT}}$=1, TXCH=1, TXUR=1.

Table 3. Write Register 0 (Address = 00 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
d7	d6	d5	d4	d3	d2	d1	d0	Transmit Data Byte

Write Register 1 (Table 4) contains a control byte. The receiver is enabled when RXEN is set (1) and disabled when RXEN is cleared (0). The receiver does not load a byte of data into the FIFO if RXEN is changed to 0 while that byte of data is being received. If RXEN is changed from a 0 to 1 while a valid character is in the receive shift register, that data byte is loaded into the receive FIFO. If another byte of data begins to be received before RXEN = 1, the previous byte is lost. RXEN must be set (1) if DTE/DCE of write register 2 is 0 and CTS/RTSHAND of write register 2 is 1. A hardware reset (RESET input = 1) or software reset (RESET bit D6 of register 4) clears (0) this bit, but RXRST does not.

Table 4. Write Register 1 (Address = 01 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
RXEN	TXEN	PAREN	EV/ODD	PEO/10	P1/0	BRGEN	CTS	Control

The transmitter is enabled when TXEN is set (1) and disabled when TXEN is cleared (0). The transmitter finishes sending a character if this bit is cleared (0) while in the process of sending the character. This bit must be set (1) when DTE/DCE and CTS/RTSHAND of write register 2 are set (1). A RESET clears (0) this bit, but TXRST does not.

The PAREN bit enables parity when set (1) and disables parity when cleared (0). This bit controls parity generation for transmit data and parity checking for receive data. Also, when this bit is set (1), the D7 data bit in the transmit FIFO is ignored and replaced by the appropriate parity bit. A RESET clears (0) this bit.

When EV/ODD is set (1), this bit generates even parity for transmit data if PAREN and PEO/10 of this register are set (1). Received data is also checked for even parity in this mode. When EV/ODD is cleared (0), odd parity is generated and verified if PAREN and PEO/10 are set (1). A RESET clears (0) this bit.

When PEO/10 is set (1), this bit generates even or odd parity if PAREN of this register is set (1). When cleared (0), and PAREN is 1, then a 1 or 0 parity bit is generated and verified. A RESET clears (0) this bit.

When parity is enabled and PEO/10 of this register is a 0, then the parity bit generated and verified will be a 1 or 0 according to the state of the P1/0 bit. A RESET clears (0) this bit.

The PAREN, EV/ODD, PEO/10, and P1/0 bits that determine the parity settings are summarized in Table 5.

Table 5. Parity Bits				
PAREN	EV/ODD	PEO/10	P1/0	Mode
0	X	X	X	No Parity
1	X	0	0	Zero Parity
1	X	0	1	One Parity
1	0	1	X	Odd Parity
1	1	1	X	Even Parity

The BRGEN bit enables the internal baud rate generator when set (1) and disables the baud rate generator when cleared (0). A RESET clears (0) this bit.

The CTS bit is inverted and appears at the $\overline{\text{CTS}}$ output pin if it is in EIA flow control mode or manual mode (CTS/RTSHAND of write register 2 is cleared (0)). A RESET clears (0) this bit.

Write Register 2 (Table 6) contains a control byte. When the DTE/DCE bit is set (1) and CTS/RTSHAND of this register is set (1), then the CTS/RTS I/O acts as a DTE interface. The $\overline{\text{RTS}}$ input to the ARTI device goes low when the external device can receive data. The $\overline{\text{CTS}}$ output from the ARTI device goes low in this mode when there is one or more bytes of data in the transmit FIFO and the TXEN bit is set (1). When the DTE/DCE bit is cleared (0) and CTS/RTSHAND of this register is set (1), then the CTS/RTS I/O acts as a DCE interface. In this mode, the $\overline{\text{RTS}}$ input of the ARTI device goes low when the external device requests to transmit data to the ARTI device. The $\overline{\text{CTS}}$ output of the

ARTI device goes low in response to the $\overline{RTS}$ input going low when the RXEN bit is set (1) and there is room in the receive FIFO. When CTS/RTSHAND is cleared (0) and DTE/DCE is set (1) the ARTI device is in EIA flow control mode. In this mode $\overline{CTS}$ is a general-purpose output under control of register 1 bit D0. The transmitter waits until $\overline{RTS}$ is asserted. The receiver operates as in manual mode. A RESET clears (0) this bit.

Table 6. Write Register 2 (Address = 02 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
DTE/DCE	CTS/RTSHAND	BKGEN	INTEN	TXIEN	RXIEN	STBT	1	Control

When the CTS/RTSHAND bit is set (1), the $\overline{RTS}$ input and $\overline{CTS}$ output of the ARTI device cause transmitter and receiver control as previously described. When CTS/RTSHAND is cleared (0) and DTE/DCE is cleared (0), the $\overline{RTS}$ is a general-purpose inverting input and the $\overline{CTS}$ is a general-purpose inverting output from the ARTI device. The transmitter continues to send data until it is disabled or the FIFO is empty. The receiver continues receiving data until it is disabled. Table 7 summarizes the control mode settings. A RESET clears (0) this bit.

Table 7. Control Modes

DTE/DCE	CTS/RTSHAND	Mode
0	0	MANUAL
0	1	DCE
1	0	EIA
1	1	DTE

When the BKGEN bit is set (1), a break is generated from the transmitter, if the appropriate transmitter controls have been enabled. If this bit is set (1) in the process of transmitting a character, the break begins after the stop bit of that character has been transmitted. The break is removed when this bit is cleared (0) or a hardware or software generated reset occurs. Data may be loaded into the transmit FIFO even if this bit is set (1). Breaks are sent in multiples of 10 bits. Data may be loaded into the transmit FIFO even if this bit is set (1). A RESET clears (0) this bit.

INTEN, when set (1), enables the $\overline{TXI}$ and $\overline{RXI}$ interrupt outputs from the ARTI device if they have been previously set (1). When cleared (0), all interrupts are disabled. A RESET clears (0) this bit.

TXIEN, when set (1), enables the transmit interrupts. This includes the condition for the transmit queue interrupt status set in write register 5 and the $\overline{RTS}$ input interrupt if set in write register 5. A RESET clears (0) this bit.

RXIEN, when set (1), enables the receive interrupts. This includes the condition for the receive queue interrupt status, break detect, receive parity error, and receive frame error interrupt enables all set in write register 5. A RESET clears (0) this bit.

When the STBT bit is set (1), two stop bits will be generated by the transmitter. When cleared (0), one stop bit will be generated. This bit does not affect the definition of framing error on the receiver. The receiver only looks for a 1 stop bit. A RESET clears (0) this bit.

The D0 bit must be set (1). A RESET sets (1) this bit.

Table 8. Write Register 3 (Address = 03 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
br7	br6	br5	br4	br3	br2	br1	br0	Lower byte of baud rate generator

Write Register 3 of Table 8 stores the lower eight of eleven bits for the baud rate generator. These bits are cleared (0) by a RESET.

Write Register 4 of Table 9 contains reset, control, and baud rate generator bits. DSR is the noninverted DSR output of the ARTI device. This bit is set (1) by a RESET.

Table 9. Write Register 4 (Address = 04 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
DSR	RESET	TXRST	RXRST	SPMAT	br10	br9	br8	Reset, control,and baud rate generator

The RESET bit when set (1), has the same effect as a high on the RESET input pin of the ARTI device, except that the ARTI device outputs are not 3-stated and the microprocessor bus (ADB0—ADB7) operates normally. This bit is self-clearing after the intended software reset has been completed. This bit is cleared (0) when a high level on the RESET input pin is detected. Four master clock cycles are required to complete the internal reset function.

When TXRST is set (1), it causes a transmitter reset. The transmit queues, status bits, and shift register are cleared (0) but the control bits are not. This bit is self-clearing with a wait of at least four master clock cycles needed. A RESET clears (0) this bit.

When RXRST is set (1), it causes a receiver reset. The receiver queues, status bits, and shift register are cleared. This bit is self-clearing with a wait of at least four master clock cycles needed. A RESET clears (0) this bit.

SPMAT is set (1) in speed matching mode and it will be cleared (0) by the falling edge of the start-bit pulse. The speed matching interrupt is a latched type. If interrupts are enabled, this bit, although self-clearing after the interrupt occurs, must be written as a 0 to clear the latched speed matching interrupt output. A hardware RESET or a software reset clears (0) this bit.

Bits D2 through D0 contain br10, br9, and br8. These are the upper three (most significant) bits of the internal baud rate generator counter. These bits are cleared (0) by a RESET.

Table 10. Write Register 5 (Address = 05 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
TDFB	TDFA	RDFC	RDFB	RDFA	ERRINT	RTSINT	BKINT	Queues and interrupts

Write Register 5 of Table 10 contains interrupt bits and queues. TDFB and TDFA determine the status of the transmit data queue that will cause the $\overline{\text{TXI}}$ interrupt output and $\overline{\text{TXINT}}$ status bit from the ARTI device to go low if the interrupts are enabled. A RESET clears (0) these bits. Table 11 describes the $\overline{\text{TXI}}$ interrupt corresponding to the TDFA and TDFB bits.

Table 11. $\overline{TXI}$ Interrupts		
TDFb	**TDFa**	**$\overline{TXI}$ Interrupt**
0	0	Interrupt if queue is empty
0	1	Interrupt if three or more bytes can be written
1	0	Interrupt if two or more bytes can be written
1	1	Interrupt if one or more bytes can be written

RDFC, RDFB, and RDFA determine when the $\overline{RXI}$ interrupt output and the $\overline{RXINT}$ status bit of the ARTI device will go low if the $\overline{RXI}$ interrupt is enabled. A RESET clears (0) bits RDFC and RDFB and sets (1) bit RDFA. Table 12 describes the $\overline{RXI}$ interrupt corresponding to these bits.

Table 12. $\overline{RXI}$ Interrupts			
RDFC	**RDFB**	**RDFA**	**$\overline{RXI}$ Interrupt**
0	0	0	Enables the receive interrupt at the end of start bit during speed matching.
0	0	1	Interrupt if one or more bytes are available.
0	1	0	Interrupt if two or more bytes are available.
0	1	1	Interrupt if three or more bytes are available.
1	0	0	Interrupt if four or more bytes are available.
1	0	1	Interrupt if five or more bytes are available.
1	1	0	Interrupt if six bytes are available (full).
1	1	1	Used as a test mode in factory testing.

ERRINT enables the error interrupt when set (1). An error interrupt causes the $\overline{RXI}$ interrupt output and the $\overline{RXINT}$ status bit of the ARTI device to go low if there was a parity error, framing error, or if the receive queue was in an overrun condition (six bytes were stored to fill the receive queue and another receive byte overwrote the last byte). A RESET clears (0) this bit.

RTSINT, when set (1), causes the $\overline{TXI}$ interrupt output and the $\overline{TXINT}$ status bit of the ARTI device to go low when the $\overline{RTS}$ input to the ARTI device goes low in the DCE mode. A RESET clears (0) this bit.

BKINT, when set (1), causes the $\overline{RXI}$ interrupt output and the $\overline{RXINT}$ status bit of the ARTI device to go low when a break is detected by the receiver. A RESET clears (0) this bit.

Read Registers

Read Register 0 (Table 13) contains the receive data byte. This is the most significant data byte from the receive queue when read by the microprocessor. A RESET clears (0) these bits.

Table 13. Read Register 0 (Address = 00 Hex)								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**
d7	d6	d5	d4	d3	d2	d1	d0	Receive data byte

Read Register 1 (Table 14) contains the status of the transmit and receive queues. RXCH, when set (1), indicates that one or more receive bytes are available. A RESET clears (0) this bit.

Table 14. Read Register 1 (Address = 01 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
RXCH	RFSC	RFSB	RFSA	TXCH	TFSb	TFSa	1	Transmit and receive queue status

RFSA, RFSB, and RFSC indicate the number of receive bytes in the receive queue. They indicate to bits RDFC, RDFB, and RDFA of write register 5 (Table 10) how many bytes are available for the interrupt settings. A RESET clears (0) these bits.

TXCH, when set (1), indicates that there is one or more bytes of transmit queue space available. A RESET sets (1) this bit (transmit FIFO is empty after a RESET).

TFSa and TFSb indicate the number of available queue bytes that are empty in the transmit buffers. Table 15 summarizes the bit settings of TFSa and TFSb. A RESET clears (0) these bits.

Table 15. Available Transmit Queue Bytes		
TFSb	TFSa	Number of Empty Bytes
0	0	4
0	1	3
1	0	2
1	1	1

Read Register 2 (Table 16) contains status bits. BKDET, when set (1), indicates that the receiver has detected a break condition. (A break condition is reception of ten or more low logic levels in a row.) The RXEN control bit of write register 1 (Table 4) must be set (1) to detect a break condition. A RESET clears (0) this bit.

Table 16. Read Register 2 (Address = 02 Hex)								
D7	D6	D5	D4	D3	D2	D1	D0	Function
BKDET	RTS	$\overline{\text{RXINT}}$	$\overline{\text{TXINT}}$	RXOR	TXUR	FRERR	PARERR	Status Bit

RTS is the inverted $\overline{\text{RTS}}$ input to the ARTI device regardless of the control mode that was set previously.

$\overline{\text{RXINT}}$ is 0 when a receive interrupt condition exists and RXIEN is 1 regardless of whether INTEN is enabled. This permits increased polling flexibility when external interrupts are not used. A RESET sets (1) this bit.

$\overline{\text{TXINT}}$ is 0 when a transmit interrupt condition exists and TXIEN is 1 regardless of whether INTEN is enabled. This permits increased polling flexibility when external interrupts are not used. A RESET sets (1) this bit.

RXOR, when set (1), indicates a receiver overrun condition. This cannot occur in the DCE mode (Table 7). A RESET clears (0) this bit.

TXUR, when set (1), indicates that the transmitter has sent all the bytes in the transmitter queue and that the transmit shift register is empty. A RESET sets (1) this bit. The AS bit in register 4 indicates an empty shift register.

FRERR, when set (1), indicates that a valid stop bit was not detected. A RESET clears (0) this bit.

PARERR, when set (1), indicates that a parity error has occurred if the parity was previously enabled. A RESET clears (0) this bit.

Read Register 3 (Table 17) contains the lower byte of the baud rate generator.

Table 17. Read Register 3 (Address = 03 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
br7	br6	br5	br4	br3	br2	br1	br0	Lower byte of baud rate generator

This read register indicates the data stored for the baud rate generator in write register 3 (Table 8). A RESET clears (0) all of the bits.

Read Register 4 (Table 18) contains the most significant bits of the baud rate generator and the DTR input.

Table 18. Read Register 4 (Address = 04 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
DTR	AS	1	1	SPMAT	br10	br9	br8	DTR and baud rate generator

DTR reflects the noninverted logic level of the DTR input to the ARTI device.

When AS is a 1, the data is in either the transmit FIFO or the shift register. When it is a 0, the ARTI device has sent all the data (both the FIFO and the register are empty). A RESET clears (0) this bit.

When SPMAT is a 1, then the ARTI device is in speed matching mode. In this mode the transmitter is disabled and the 16-bit baud rate clock counter is initialized to 32760 base 10 automatically. This bit is self-clearing and clears (0) after a RESET. This bit is cleared (0) after the start bit is detected.

The bits D2, D1, and D0 contain br10, br9, and br8. These three bits reflect the three most significant bits stored for the baud rate generator in write register 4 (Table 8). A RESET clears (0) these bits.

Baud Rate Generator and Master Clock

The internal baud rate generator is an 11-bit binary counter used to send transmit data and sample receive data. It divides the CLK input to the ARTI device by the binary number loaded into write registers 3 and 4 plus one. Its output is actually 16 times the desired baud rate. Figure 3 is a block diagram of the baud rate generator.

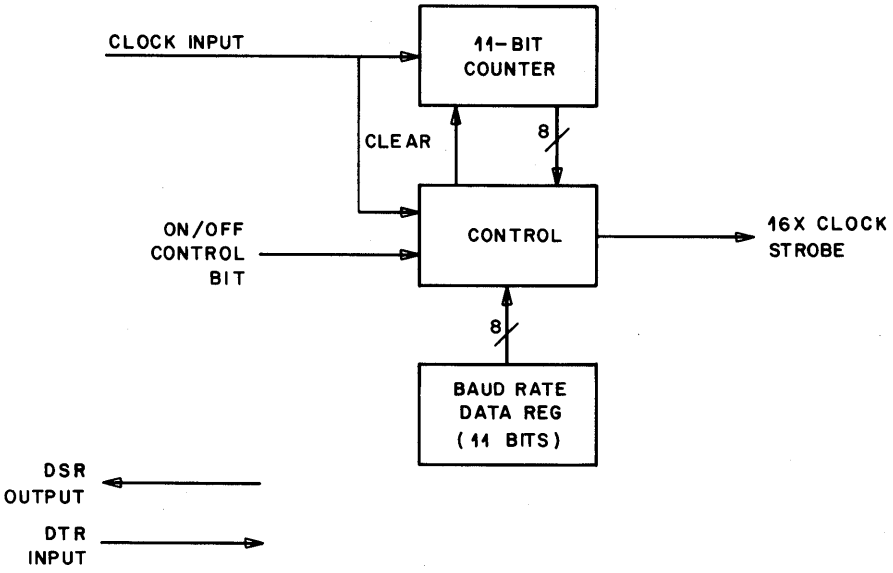


Figure 3. Baud Rate Generator

The equations for programming the baud rate registers are

$$\text{Baud Rate} = \text{CLK}/[(N+1)16]$$

or

$$\text{CLK} = \text{Baud Rate}[(N+1)16]$$

where:

- Baud Rate is desired data rate
- CLK is the input clock frequency to the ARTI device
- N is the 11-bit number of the baud rate counter but it cannot be zero.

The reason for the extra 1 in the dividend is for clearing and providing a proper strobe, since the counter is clocked from the master clock into the ARTI device.

The proper method of changing the baud rate frequency is to first disable the baud rate generator, write the new time constant to the br0—br10 data bits, and then enable the baud rate generator. The baud rate time constant may be changed while enabled. This may be useful in the speed matching mode to readjust the baud rate generator frequency.

The actual clock frequency supplied to the ARTI device must be chosen carefully because the baud rate is directly affected by this frequency and the microprocessor timing requirements are based on the relationship between the CLK input and the microprocessor control and data bus signals. When an 8088 microprocessor is used, it is suggested that the ARTI device clock be the same as the microprocessor clock. When an 8051/8031 (or 8052/8032) microprocessor is used, it is suggested that a clock frequency 75% of the 8051 crystal frequency, or greater, be used. This will ensure proper internal timing for read and write commands.

The maximum input clock frequency to the ARTI device is 8.00 MHz and the duty cycle of the clock must be at least 30%.

Transmitter

A block diagram of the transmitter section of the ARTI device is shown on Figure 4.

The order of data transmission from the ARTI device is the start bit (a logic level 0) first, then d0, d1, d2, d3, d4, d5, d6, d7 (or the parity bit), and then the stop bit(s) (a logic level 1) last.

There are four transmit registers that act as a FIFO. Transmit data written to the ARTI device from the microprocessor is steered to the most significant vacant register. As data is transmitted, bytes are shifted until the registers empty. If parity is enabled, the D7 (most significant bit) of data is changed to the proper parity before it is loaded into the transmit register.

The transmit shift register inserts a logic 0 start bit before the data byte and a logic 1 stop bit after the data byte to complete the 10-bit serial frame. One or two stop bits may be transmitted, depending on STBT in write register 2.

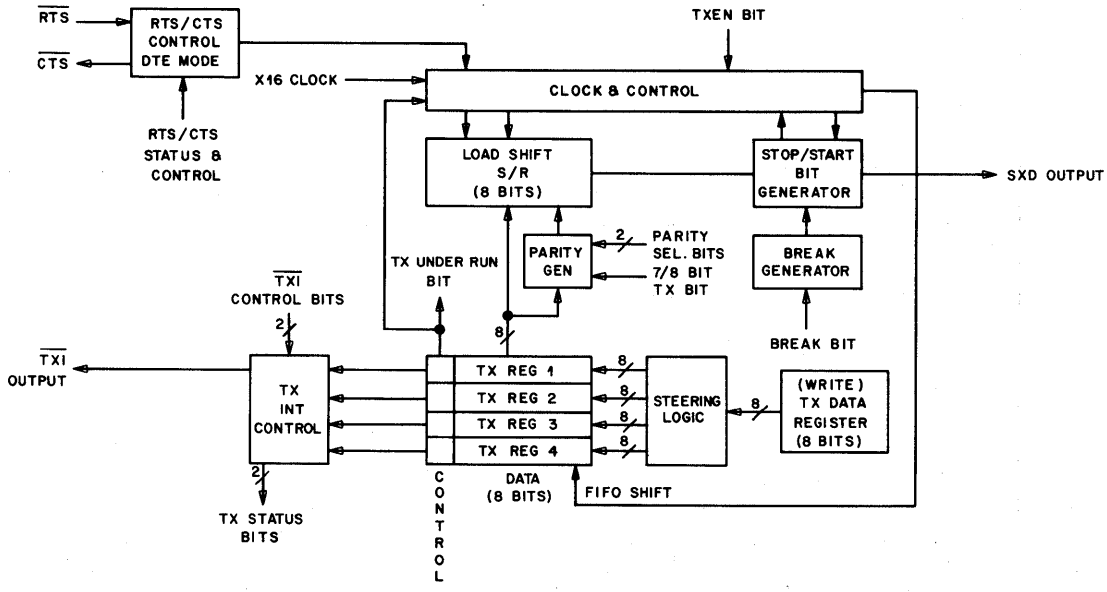


Figure 4. ARTI Transmit Circuit

Status bits associated with each register are set (1) when that register is loaded with a data byte. These status bits are used to check transmit status and for transmit interrupt control.

The break generation forces the serial data output to a 0 if the break bit is set (1) in write register 2 and there is no serial transmission in progress. If there is a character being transmitted, then the break will take place after the stop bits of that character transmission even if there are more data bytes in the transmit FIFO. The data in the FIFO is stored until the break is removed. Data may be written to the FIFO while in the break mode. BKGEN must last at least ten bit periods before being cleared by the processor. Longer break outputs are in increments of ten bit periods. That is, if the break bit was enabled by the microprocessor for 35 bit periods, the break output from ARTI would be 40 bit periods.

The clock and control section is used to control the shift register and the data registers. The clock (16 times baud rate) from the baud rate generator is used as the transmit control frequency. Each bit of data transmission is 16 baud rate clock pulses long. When a character has been transmitted, the control circuit checks for additional data to be transmitted. If there is none, the serial output goes high. If there is more data, the least significant byte of the transmit FIFO is loaded into the shift register.

Enabling serial transmission is accomplished by two methods. When CTS/RTS transmitter control is disabled, only the TXEN bit must be set (1) to enable data transmission. If the CTS/RTS transmitter control is enabled as in the DTE mode or EIA flow control mode, then the $\overline{RTS}$ input to the ARTI device must be low and the TXEN must also be set (1).

In the DTE mode, the ARTI device acts as a DTE interface to an external serial receiver. In the CTS/RTS mode, the $\overline{CTS}$ output of the ARTI device goes low when there is a byte of data to be transmitted. The external device will lower the $\overline{RTS}$ input to the ARTI device when it can accept a byte of data. The ARTI device, sensing the low $\overline{RTS}$, will then transmit the data if the TXEN bit had been set (1), or is subsequently set, (1). If the TXEN bit is cleared (0) or the $\overline{RTS}$ input goes high during data transmission, then the data transmission is stopped after the byte has been transmitted.

To abort data transmission, the TXRST bit must be set (1). This forces the SXD output high and clears the transmit registers and status bits. TXEN must be reset to a 0 by the microprocessor.

The transmit interrupt control consists of a 4- to 2-bit encoder and a comparator. When the interrupt number is less than or equal to the number of free data byte locations in the transmit registers, the $\overline{TXI}$ output and the $\overline{TXINT}$ status bit of the ARTI device go low if the interrupts were enabled. The two outputs of the encoder can be read directly in read register 1 to indicate the number of free data byte locations.

Receiver

The receiver block diagram is shown on Figure 5.

The order of data reception to the ARTI device is the start bit (logic level 0) first, then d0, d1, d2, d3, d4, d5, d6, d7 (or the parity bit), and then the stop bit(s) (logic level 1) last.

The receiver basically consists of a shift register and six receive registers.

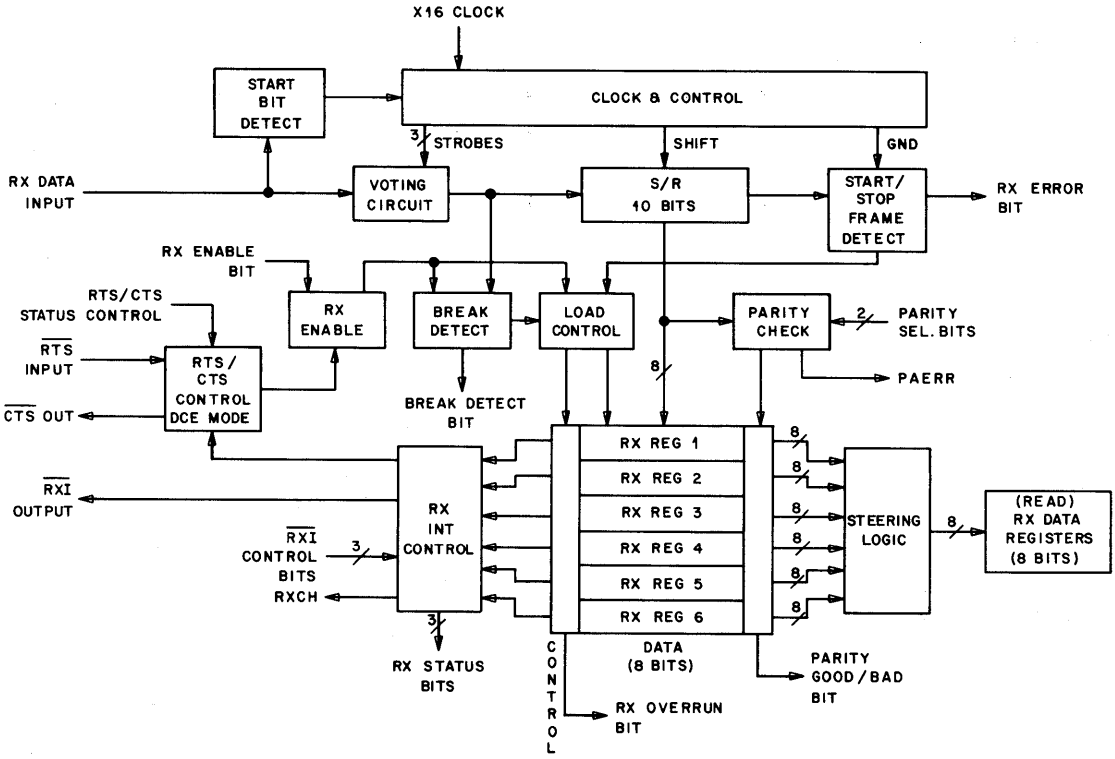


Figure 5. ARTI Receive Circuit

The RXD input of the ARTI device goes to a voting circuit. The voting circuit samples each receive bit in the middle of the bit period. This sampling involves latching the receive data at each of the middle three clock strobes and comparing the three latched logic levels. A majority wins. For example, if two highs and a low were detected, then the output of the voting circuit would be a high. This type of sampling increases the noise immunity of the receiver.

To begin data reception, a start bit detector is used. This circuit merely detects the presence of a low at the input to the receiver. The output from the start bit detector enables the clock and control circuit and the voting circuit.

After the voting circuit, the receive data is loaded into the receive shift register. The clock and control circuit controls the rate of loading in the serial data. The shift register is 10 bits long to permit start- and stop-bit verification before the received data byte is loaded into the receive registers.

The receive enable circuit determines whether data should be transferred from the receive shift register to the receive FIFO. If in the manual mode, EIA flow control, or DTE mode, a byte will be properly received and stored in FIFO if RXEN=1 and a valid start bit is received. In the CTS/RTS handshake DCE mode, data will be loaded only if an empty register is available. In all cases, if RXEN is a 0, then loading is inhibited.

In the CTS/RTS handshake mode, the ARTI device acts as a DCE interface to an external serial transmitter. When the external transmitter wants to transmit a byte of data, it lowers the $\overline{RTS}$ input to the ARTI device. The ARTI device lowers the $\overline{CTS}$ output when it is able to accept data, RXEN is set (1), and less then six bytes of data are stored in the receive registers. The external serial transmitter then transmits data to the ARTI device. The receiver is disabled if all six bytes of the receive register are full in this mode.

After a byte is received, the stop bit is checked for a 1. If parity was not enabled, then the byte is loaded into the least significant byte of the receive register if the stop bit was valid. If the stop bit was not valid, the error bit associated with that byte is set (1) but the byte is still loaded. If the $\overline{RXI}$ interrupt was enabled for frame error conditions, then the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit will go low. If read register 2 is read and the erroneous data byte is the most significant in the receive register, then the FRERR bit is set (1). After reading the erroneous data, this bit is reset.

If parity was enabled, then the PARERR bit is set (1) in read register 2 if the erroneous data byte was the most significant in the receive register. Also, if the $\overline{RXI}$ interrupt was enabled for error conditions, the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit would go low to indicate the parity error. The data byte is still loaded into the receive data register.

If an attempt is made to store more than six bytes in the receive registers, then the RXOR bit in read register 2 will be set (1). This cannot occur when the ARTI device is in the DCE mode with the RTS/CTS mode enabled, because in that mode of operation the receiver is disabled when the receive queue is full. A receive overrun condition will cause the $\overline{RXI}$ interrupt output and the $\overline{RXINT}$ status bit to go low for at least one master clock period if the ERRINT interrupt has been enabled.

On a receive overrun condition, the least significant byte (last byte received) in the receive FIFO is written over by the new receive data and the RXOR status bit is set (1). The most significant bytes of the receive FIFO are not affected by the overrun condition and are not changed until the overrun condition is cleared by reading a byte of data from the FIFO or by a receiver reset.

The break detect circuit senses when a break has occurred. A break is defined as 10 or more low-level bit periods in a row. Although during normal data reception a break would cause 10 zeros to be loaded into the receive shift register, the break detect circuit inhibits error conditions from being set. It does not load the data from the shift register into the data register, but it does set the BKDET status bit. Once a break is detected, the only way to reset the BKDET bit is the valid reception of a 1. The break circuitry also prevents the first reception of a 1 after a break from causing the control circuitry to think that a valid stop bit was detected and thus loading a byte of data into the receive register.

Associated with each byte of receive data is a status bit that goes to a 6- to 3-bit encoder. This 3-bit number indicates how many data bytes are in the receive register and may be read in read register 1 as the RXc, RXb, and RXa status bits.

These 3 bits are also the input to the receive interrupt control circuit. When the 3 bits are equal to or greater than those programmed in write register 5, and the $\overline{RXI}$ interrupt is enabled, then the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit of the ARTI device will go low for at least one master clock period.

The RXCH bit in read register 1 is set when one or more bytes of data have been stored in the receive FIFO.

Data bytes may be read at any time via the microprocessor interface to the ARTI device. The data byte that is read is the most significant byte of the receive queue. The steering logic ensures that the proper byte is read even though a byte may be ready to be transferred from the receive shift register to the receive FIFO.

Microprocessor Interface

The microprocessor interface of Figure 6 is detailed in the timing section. This interface consists of the read ($\overline{RD}$), write ($\overline{WR}$), chip select ($\overline{CS}$), address latch enable (ALE), and the eight address/data bus (ADB0—ADB7) signals. The timing of the ARTI device allows the use of an 8 MHz 8088 microprocessor without wait states as long as the attached timing requirements are met. It is strongly suggested that the ARTI device run from the same clock as the 8088 microprocessor to ensure proper read and write access timing.

An 8051 or 8052 microcontroller may be used with the ARTI device as long as the ARTI clock frequency is less then 75% of the 8051 clock frequency.

Speed Matching

Speed matching is a unique feature available in the ARTI device. It is designed to permit the microprocessor to quickly determine the baud rate of a receive serial input stream RXD.

The approach measures the duration of RXD's first low pulse and assumes it was one start bit. Thus the algorithm requires d0 (the first data bit received) to be a 1.

To set the ARTI device in speed matching mode the microprocessor must set write register 4, bit D3 to one. The 1 to 0 transition on RXD automatically clears the SPMAT bit to 0. It is recommended that TXRST (bit D5) also be set (1) to prevent unexpected data transmission before the baud rate is determined. Optionally an interrupt can be programmed in write register 5, bits D5—D3.

The result of the measurement can be a combination of three events or potentially an error condition. If the RXD low pulse is greater than 72 system clock (CLK) periods and is less than 32775 CLK periods, then an estimate of N will be loaded into the baud rate generator. This can be read through read registers 3 and 4 just after RXD goes high. Furthermore, this estimate will be used to receive the subsequent data bits.

The second event is a programmable, latched receiver interrupt ($\overline{RXI}$). The interrupt occurs at the end of the RXD's first low pulse. It thereby indicates that the baud rate generator is available for reading and possibly updating the baud registers while the serial input stream is being received. To program the ARTI device to provide this interrupt , clear bits D5—D3 to 000 in write register 5. The speed matching interrupt is a latched type. If interrupts are enabled, this bit,although self-clearing after the interrupt occurs, must be written as a 0 to clear the latched speed matching interrupt output. Using this interrupt to update the baud registers while the serial input stream is being received is recommended for applications in which RXD suffers from more than 3% jitter and correct first character reception is important. Correcting the measured estimate of N in the baud rate generator can insure proper reception of later bits. The speed matching interrupt is cleared by writing a zero to bit D3 of register 4.

The third event is a break detection. This event is mutually exclusive of the first two. When in speed matching mode, a break is detected if the first RXD low pulse exceeds 32776 system clock periods in duration. The break is signaled according to the ARTI device's current break handling configuration. No estimate of the N is loaded into the baud rate generator in this case. In addition the end of RXD = low will not be signaled by the interrupt pulse described above.

An error condition can result if the first low pulse of RXD is less than 72 system clock periods in duration. The ARTI device will load the baud rate generator, but with a useless value (N = all ones or N $\leq$ 4). The interrupt will occur if programmed. The rest of the data word will not be received correctly. Unusually short RXD pulses can load the baud rate generator with 0, thereby disabling the transmitter and receiver.

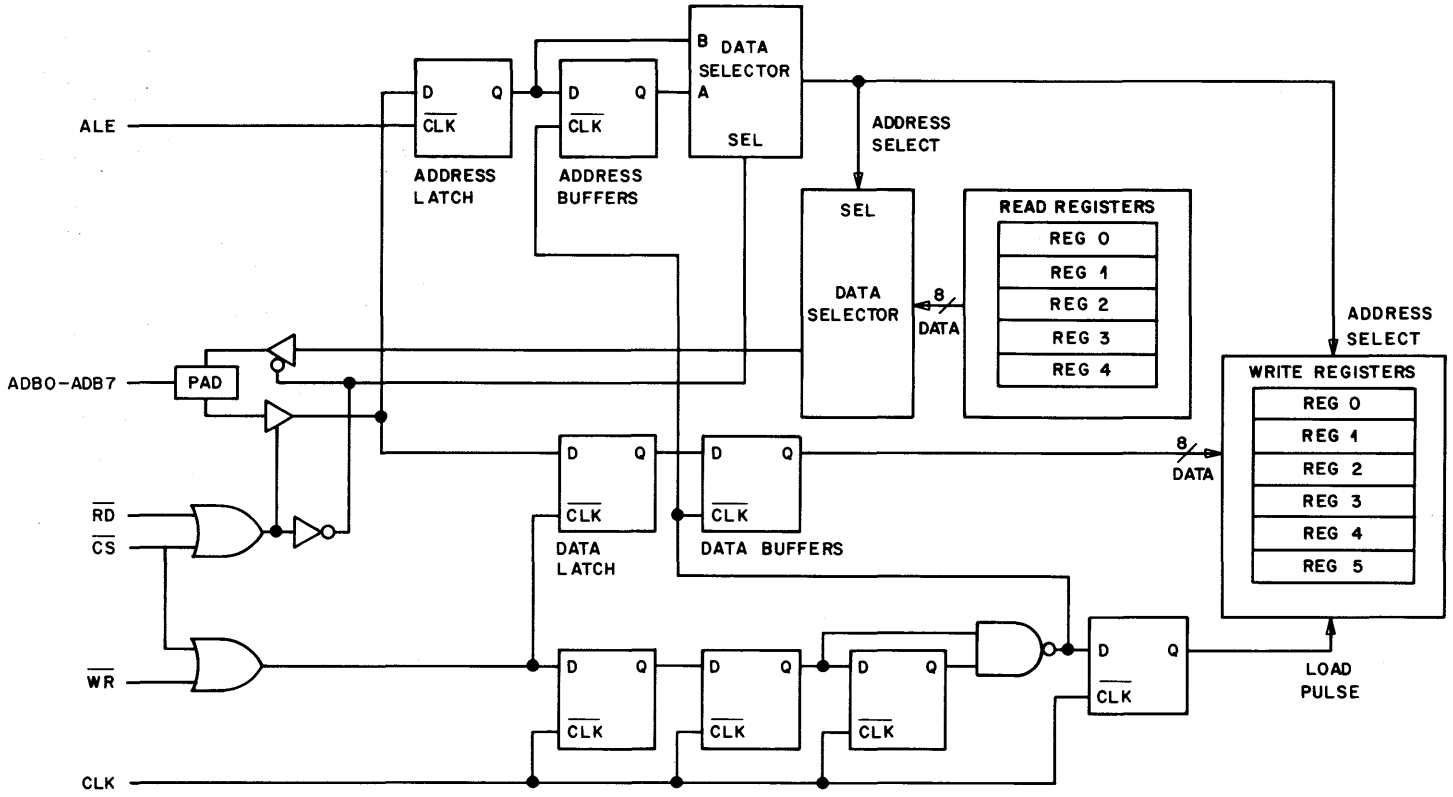


Figure 6. Microprocessor Interface

Testing

All outputs of the ARTI device are 3-stated when the RESET input is at a high logic level. The address/data bus signals are configured as inputs in this condition. This test mode is used during GenRad in-circuit PWB testing to prevent damage to the ARTI output buffers while being back-driven.

The RESET input to the ARTI clears both receive and transmit registers, the status bits, and sets the control bits to their default conditions. The RESET function is typically used during circuit power-up.

In addition, there exists certain test modes which should not be active during normal operation. Test A: Bit 0 of write register 2=1 and Test B: Bit 3 of write register 4=1.

CHARACTERISTICS

Electrical Characteristics

T_C = 0 to 70 °C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Parameter		Symbol	Min	Max	Unit	Test Condition
Input Voltage	Low	V_{IL}	0.0	0.8	V	–
	High	V_{IH}	2.0	V_{DD}	V	–
Output Voltage	Low	V_{OL}	–	0.4	V	I_{OL} = 2.4 mA
	High	V_{OH}	2.4	–	V	I_{OH} = −0.4 mA
Input Load Current		I_{LC}	0.0	−10	μA	–
3-State Output Leakage Current		IO	−40	40	μA	–
Input Capacitance		CI	–	20	pF	–
Bus Capacitance		Ctotal	–	125	pF	–
Rise Time		tr	–	20	ns	–
Fall Time		tf	–	20	ns	–
Power Dissipation		PD	–	150	mW	–

Maximum Ratings

Storage Temperature Range (Tstg) ..... −55 to +125 °C
Operating Temperature Range (T_C) ..... 0 to 70 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

ARTI/8088 (80188)* Microprocessor Interface Timing (See Figure 7)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCLCL	CLK Cycle Period	125	500	ns
tCHCL	CLK Low Time	68	–	ns
tCLCH	CLK High Time	44	–	ns
tCSL	Chip Select Delay	–	100	ns
tCLLH	ALE Active Delay	–	50 (35)	ns
tCHLL	ALE Inactive Delay	–	55 (35)	ns
tLHLL	ALE Width	58 (90)	–	ns
tCLAV	Address Valid Delay	10 (5)	60 (55)	ns
tAVAL	Address Valid to ALE Low	28 (30)	–	ns
tLLAX	Address Hold to ALE Inactive	34 (30)	–	ns
tCLAX	Address Hold Time	10	–	ns
tDVCL	Data in Set-up Time	20	–	ns
tCLRL	$\overline{RD}$ Active Delay	10	100 (70)	ns
tAZRL	Address Float to Read Active	0	–	ns
tCVCTV	Control Active Delay 1	10	70	ns
tCLDX	Data in Hold Time	10	–	ns
tWHDX	Data Hold After $\overline{WR}$	38 (85)	–	ns
tCLRH	$\overline{RD}$ Inactive Delay	10	80 (55)	ns
tCVCTX	Control Inactive Delay	10 (5)	70 (55)	ns
tWLWH	$\overline{WR}$ Width	210	–	ns
tRLRH	$\overline{RD}$ Width	200	–	ns
tRHAV	$\overline{RD}$ Inactive to Next Address	–	85	ns

*Numbers in parenthesis for 80188 microprocessor only.

ARTI/8051 Microcontroller Interface Timing (See Figures 8 and 9)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tLLRL	ALE Low to $\overline{RD}$ Low	137.5	217.5	ns
tLLWL	ALE Low to $\overline{WR}$ Low	137.5	217.5	ns
tRLRH	$\overline{RD}$ Pulse Width	375	–	ns
tRHLH	$\overline{RD}$ High to ALE High	22.5	102.5	ns
tWHLH	$\overline{WR}$ High to ALE High	22.5	102.5	ns
tCSL	Chip Select Delay	–	100	ns
tAVLL	Address Valid to ALE Low	7.5	–	ns
tLLAX	Address Hold After ALE Low	27.5	–	ns
tRLAZ	RD Low to Address Float	–	10	ns
tRLDV	RD Low to Valid Data In	–	147.5	ns
tRHDX	Data Hold After $\overline{RD}$	0	–	ns
tRHDZ	Data Float After $\overline{RD}$	–	55	ns
tDVWL	Data Valid to $\overline{WR}$ Transition	2.5	–	ns
tWLWH	$\overline{WR}$ Pulse Width	275	–	ns
tWHQX	Data Hold After $\overline{WR}$	12.5	–	ns

Timing Diagrams

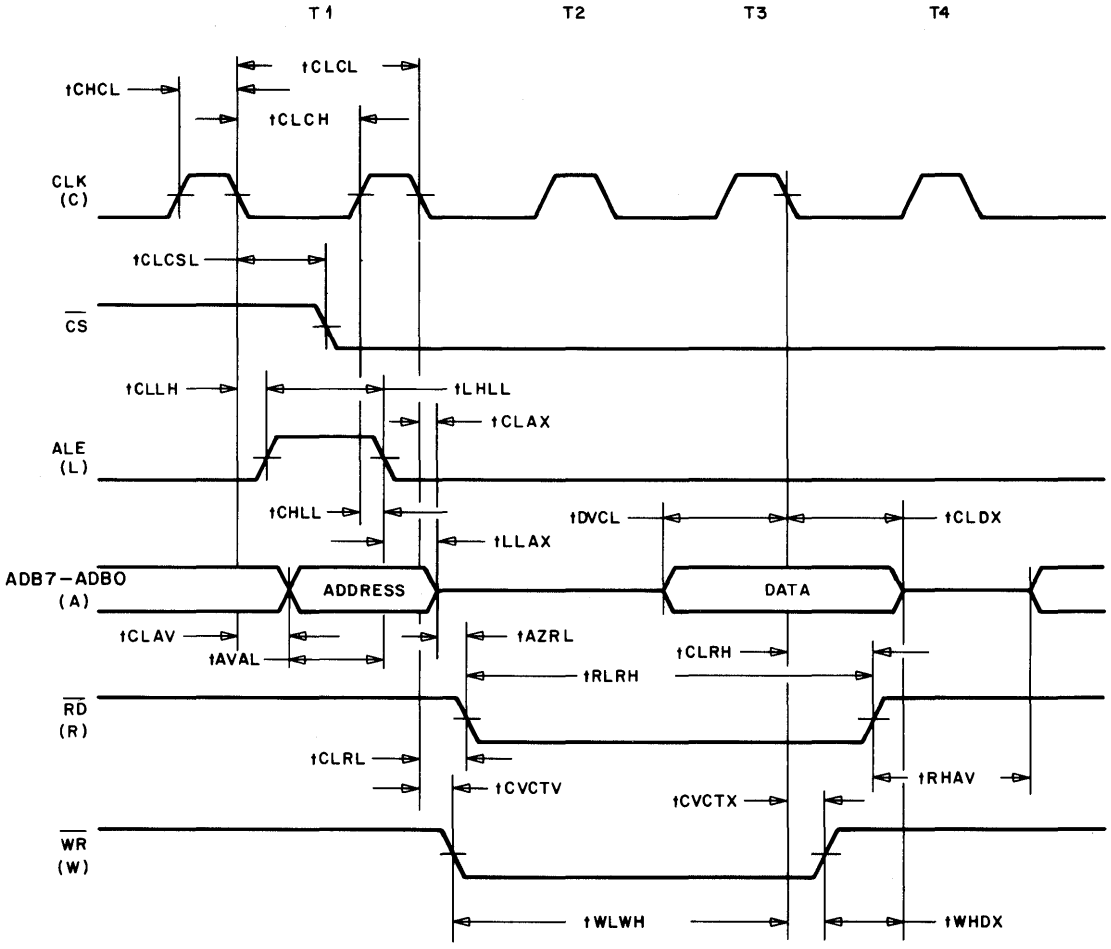


Figure 7. ARTI/8088 (80188) Microprocessor Interface Timing

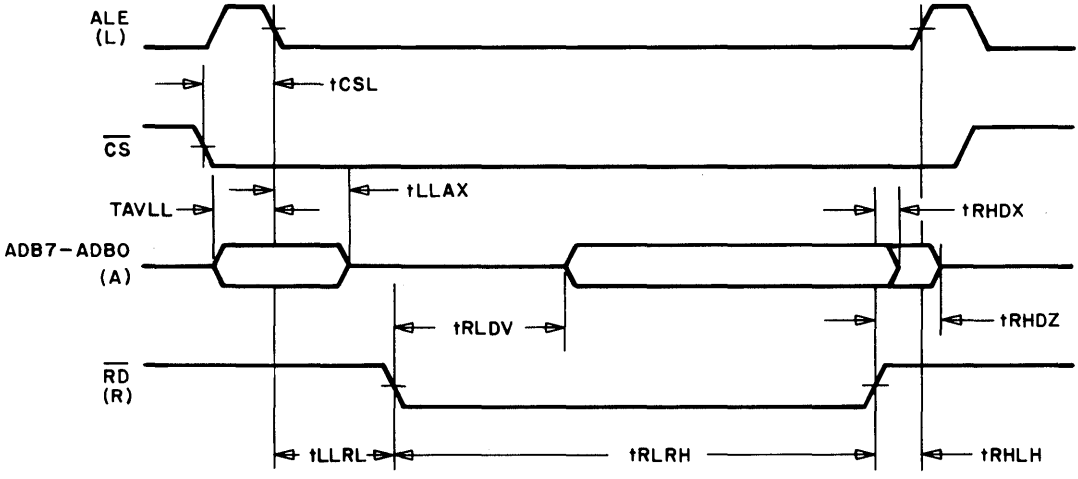


Figure 8. Read Cycle

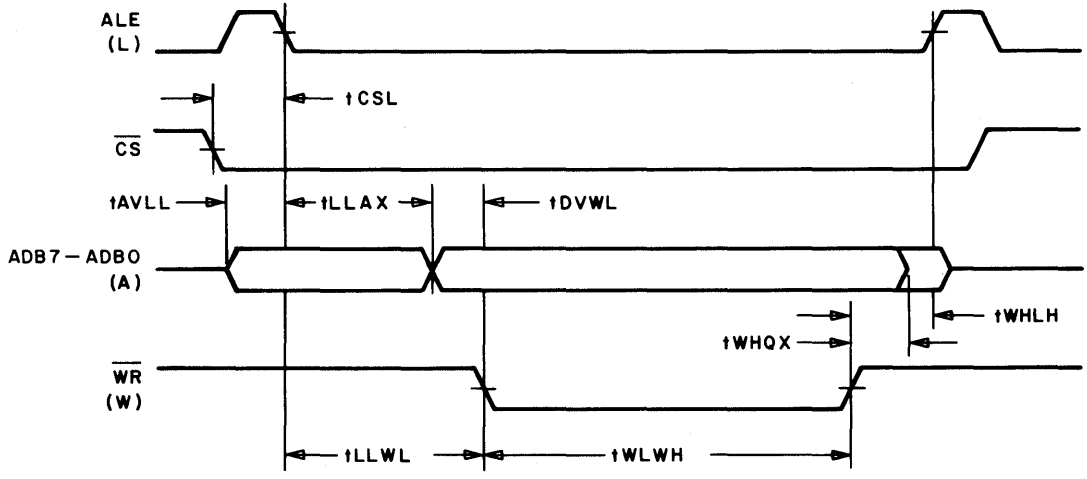


Figure 9. Write Cycle

The information contained herein is advance and subject to change.

FEATURES

- Supports CCITT I.430 recommendations for ISDN Basic Access (2B+D) at the S/T reference point in terminal equipment
- Built-in deeply buffered HDLC formatter for D channel
- Interchangeable B channels
- Optional B channel inversion
- Power-up reset
- Programmable 0.128 second – 2.048 second multifunction TIMER
- Local and remote loopback test modes
- All outputs are 3-statable
- Parallel microprocessor interface with separate address and data leads, programmable interrupt polarity, and maskable interrupts
- Programmable clock and synchronization signals allow for interfacing with codecs, HDLC controllers, and rate adapters
- Transmitter interfaces to a 2.5:1 transformer. Receiver interfaces to a 2.5:1 transformer
- TTL/CMOS-compatible I/O
- Crystal or clock input acceptable. No external circuitry required for crystal

DESCRIPTION

The T7250A User Network Interface for Terminal Equipment (UNITE) provides the line interface in terminal equipment used for basic access service offered by the Integrated Services Digital Network (ISDN). The device conforms to all CCITT I.430 recommendations for point to multipoint configurations. Priority, contention resolution, multiframing, and activation/deactivation processes are fully supported. I.430 impedance and voltage requirements can be met with a simple line interface circuit. An HDLC formatter and a sophisticated queue manager are provided to simplify the D channel interface.

The T7250A device is manufactured using CMOS technology and is available in either a 40-pin plastic DIP or in a 44-pin plastic leaded chip carrier. The 44-pin chip carrier provides two additional features that the 40-pin DIP package does not have: a 16 kHz or an 8 kHz clock and a 6.144 MHz or 192 kHz system clock. The T7250A device uses a 5 V supply and has a nominal power consumption of 55 mW.

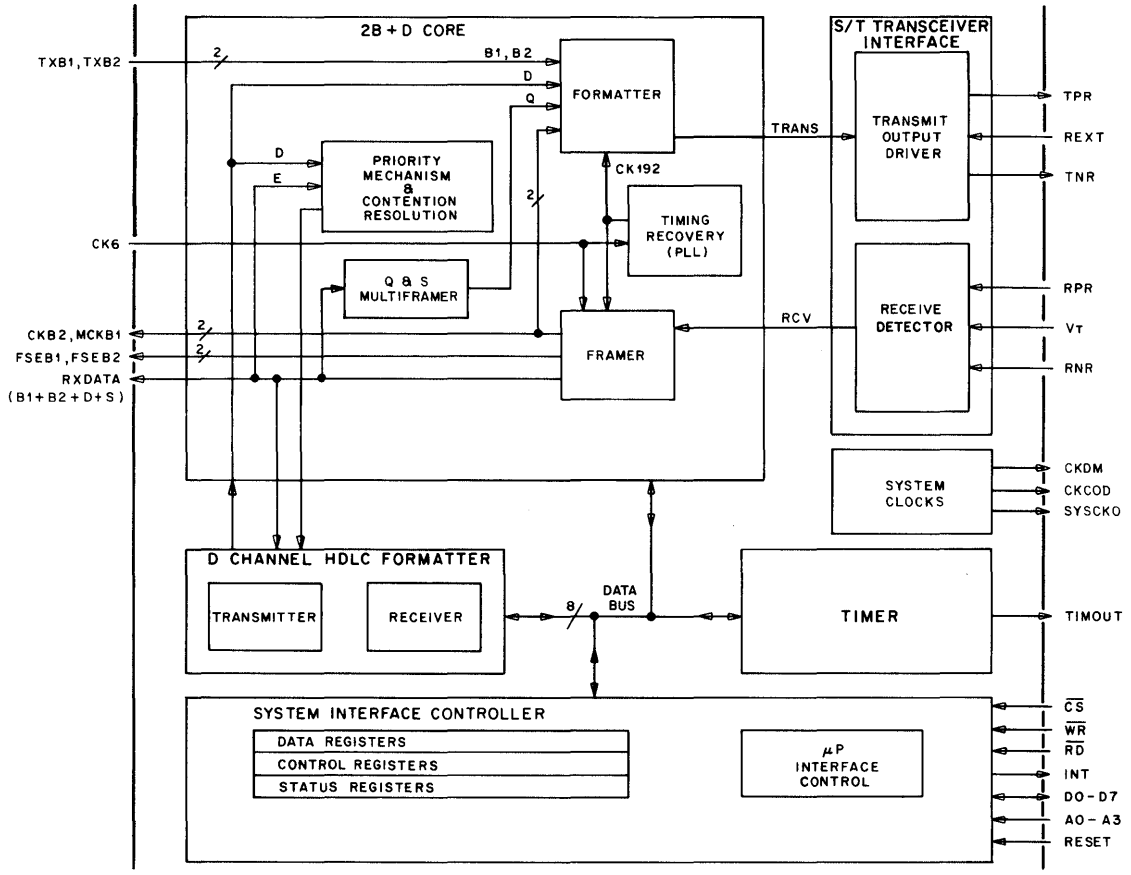


Figure 1. T7250A User Network Interface Block Diagram

USER INFORMATION

Pin Descriptions

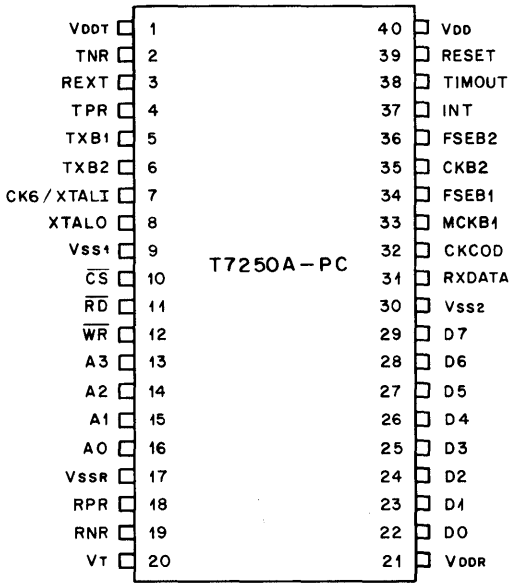


Figure 2. Pin Function Diagram For 40-Pin DIP

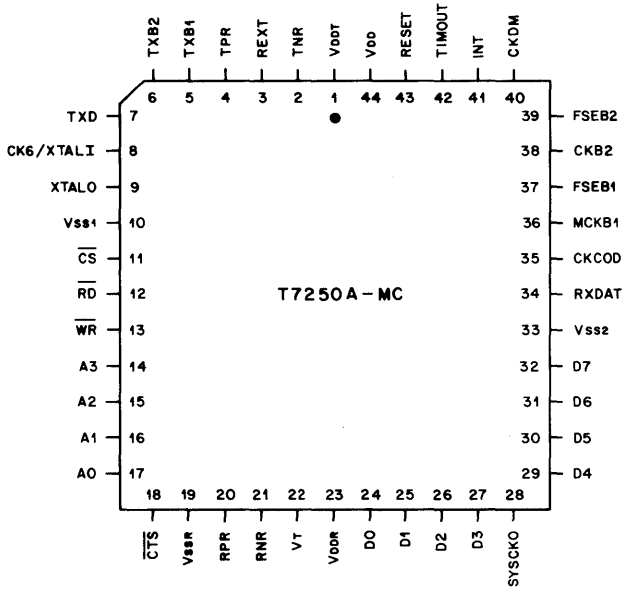


Figure 3. Pin Function Diagram For 44-Pin PLC

Table 1. T7250A Pin Descriptions – 40-Pin DIP and 44-Pin PLCC

Pin (DIP)	Pin (PLCC)	Symbol	Type	Name/Function
1	1	VDDT	—	**5 V Supply (Transmitter).** Power supply for the subscriber line transmitter. It is recommended that this be connected to the digital supply. A 1.0 μF decoupling capacitor should be tied from VDDT to digital ground.
2	2	TNR	O	**Transmit Negative Rail.** Transmitter negative output in alternate bipolar code.
3	3	REXT	I	**Resistor, External.** Connect to VDDT through a 2 kΩ ± 1% resistor.
4	4	TPR	O	**Transmit Positive Rail.** Transmitter positive output in alternate bipolar code.
5	5	TXB1	I	**Transmit B1.** B1 data that is to be transmitted to the network. Input data is valid on the falling edge of the 192 kHz clock, CK192, in reference to FSEB1.
6	6	TXB2	I	**Transmit B2.** B2 data that is to be transmitted to the network. Input data is valid on the falling edge of the 192 kHz clock, CK192, in reference to FSEB2.

Table 1. T7250A Pin Descriptions – 40-Pin DIP and 44-Pin PLCC (Continued)				
Pin (DIP)	**Pin (PLCC)**	**Symbol**	**Type**	**Name/Description**
–	7	TXD	O	**Internal Transmit D Channel Serial Data.** This signal is provided for test visibility only. The data that appears on this signal is the data from the internal HDLC transmitter to the internal S/T transmitter.
7	8	CK6/XTALI	I	**6 MHz Clock.** This is the 6.144 MHz ± 200 ppm reference clock used for the phase locked loop and other internal device logic. A crystal input or a clock is acceptable. Crystals should be compatible, with on-chip parallel resonant 12 pF load capacitance. No external circuitry is required. Input level from an external 6.144 MHz clock must be CMOS compatible.
8	9	XTALO	O	**Crystal Out.** This provides the feedback to the crystal, if a crystal is used. An optional 10 pF capacitor to ground may reduce power consumption.
9	10	V_{SS1}	–	**Digital Ground 1.** Logic and input buffer ground, not internally connected to V_{SS2}.
10	11	$\overline{CS}$	I	**Chip Select.** $\overline{CS}$ is used by the microprocessor to select the T7250A device for reading or writing when this signal is active low. The TIMOUT and SYSCKO signals are 3-stated when 1) $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
11	12	$\overline{RD}$	I	**Read.** A low on this pin when $\overline{CS}$ is low enables the T7250A device to drive the data bus. This signal is used to read data from the registers. The T7250 device drives the data bus with data from the register that is addressed by A0–A3. When $\overline{RD}$, $\overline{WR}$, are low the S/T receiver is looped back to the transmitter. The TIMOUT and SYSCKO signals are 3-stated when 1) $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
12	13	$\overline{WR}$	I	**Write.** A low on this pin when $\overline{CS}$ is low enables the T7250A device to accept data from the microprocessor. Data on D0–D7 is latched into the register addressed by A0–A3 on the rising edge of $\overline{WR}$. When $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low the S/T receiver is looped back to the transmitter. The TIMOUT and SYSCKO signals are 3-stated when 1) $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
13–16	14–17	A3–A0	I	**Address Bus.** These four address pins are used to select 1 of the sixteen internal registers. See Table 2 for register definitions.

Table 1. T7250A Pin Descriptions – 40-Pin DIP and 44-Pin PLCC (Continued)				
Pin (DIP)	**Pin (PLCC)**	**Symbol**	**Type**	**Name/Function**
–	18	$\overline{\text{CTS}}$	O	**Clear to Send.** This active low signal is provided for test visibility only. This is the internal signal from the S/T interface controller that indicates to the HDLC transmitter that it may transmit data.
17	19	VSSR	–	**Analog Ground (Receiver).** Analog ground for the subscriber line receiver. Not internally connected to other grounds.
18	20	RPR	I	**Receive Positive Rail.** Receiver positive input in alternate bipolar code.
19	21	RNR	I	**Receive Negative Rail.** Receiver negative input in alternate bipolar code.
20	22	VT	I	**Voltage Threshold for the Receiver.** A 0.1 μF decoupling capacitor should be tied from VT to analog ground to provide a clean voltage reference level for the receiver.
21	23	VDDR	–	**5 V Analog Supply (Receiver).** Analog power supply for the subscriber line receiver. A 0.1 μF decoupling capacitor should be tied from VDDR to analog ground.
22–25 26–29	24–27 29–32	D0–D3 D4–D7	I/O I/O	**Data Bus.** These eight bidirectional data lines are used to read or write on chip registers using the $\overline{\text{RD}}$, $\overline{\text{WR}}$ strobes. On a read cycle, data is received by the microprocessor on these lines. On a write cycle, data is transmitted by the microprocessor on these lines. When $\overline{\text{CS}}$ is not active, the D0–D7 pins are placed in a high impedance state (3-state).
–	28	SYSCKO	O	**System Clock Output.** This signal is programmable via R4, bit 5 (Syscko) to be either a 6.144 MHz clock (Syscko=0, default) or a 192 kHz clock (Syscko=1). Both clocks are free running. SYSCKO is 3-stated when 1) $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{CS}}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
30	33	VSS2	–	**Digital Ground 2.** Output buffer ground. Not internally connected to VSS1.
31	34	RXDATA	O	**Receive Data.** The 2B+D data received from the network side at 192 kb/s. B1 (64 kb/s) and B2 (64 kb/s) channel data are separated by using the individual frame strobe/enable B signals (FSEB1 or FSEB2) and/or the clocks (MCKB1 or CKB2). MCKB1, CKB2, FSEB1, and FSEB2 are all synchronized to the 2.048 MHz Codec clock. S and E bits also appear on this lead.
32	35	CKCOD	O	**Clock for Codec.** The clock signal on this pin is 2.048 MHz. All B channel clocks and strobes are synchronized to the 2.048 MHz clock.

Table 1. T7250A Pin Descriptions – 40-Pin DIP and 44-Pin PLCC (Continued)				
Pin (DIP)	**Pin (PLCC)**	**Symbol**	**Type**	**Name/Function**
33	36	MCKB1	O	**Master Clock or B1 Clock.** The signal on this pin can be programmed to be either CK192 (192 kHz) or CKB1 (192 kHz clock is enabled only for the B1 channel), depending on the value of the software bit clkmux (bit 2, Register 4). When clkmux is one (default), MCKB1 is CKB1. MCKB1 is synchronized to the 2.048 MHz Codec clock. MCKB1 clock can be inverted by setting R0, bit 2 (C1pol=1).
34	37	FSEB1	O	**Frame Strobe or Enable B1.** This pin is programmable via the B1f bit in the control register 4 (bit 4). The signal can either be the 8 kHz frame strobe signal for the T7500 Codec device used on the B1 channel, or an Enable B1 gating signal which is high during the 8 bits of B1, indicating the active period for B1 channel data. Timing of the enable signal is programmable via the control signal Codec1 (R4, bit 7). Available options are shown on Figure 11.
35	38	CKB2	O	**Clock for B2 Channel.** This is an output clock signal. It is a 192 kHz clock that is enabled only in the B2 time slot of RXDATA. CKB2 is synchronized to the 2.048 MHz Codec clock. CKB2 clock can be inverted by setting R0, bit 3 (C2pol=1).
36	39	FSEB2	O	**Frame Strobe or Enable B2.** The output on this pin is programmable via the B2f bit in the control register 4 (bit 3). The signal can either be the 8 kHz frame strobe signal for the T7500 Codec device used on the B2 channel, or an enable B2 gating signal which is high during the 8 bits of B2, indicating the active period for B2 channel data. Timing of the enable signal is programmable via the control signal Codec2 (R4, bit 6). Available options are shown on Figure 11.
–	40	CKDM	O	**D Channel Clock.** This is programmable to be an 8 kHz or 16 kHz clock. When R0, bit 1 (Ckdm) is zero (default), this is a free running 16 kHz signal that is used internally for clocking the D Channel. This clock does not have a 50% duty cycle. It is a 2.6 μs low going pulse that occurs at a 16 kHz rate corresponding to the location of the D bits. When Ckdm is a one, CKDM is a free running 8 kHz 50% duty cycle clock.

Table 1. T7250A Pin Descriptions – 40-Pin DIP and 44-Pin PLCC (Continued)

Pin (DIP)	Pin (PLCC)	Symbol	Type	Name/Function
37	41	INT	O	**Interrupt.** Eight conditions can cause an interrupt signal of programmable polarity to be generated. Registers 9 and 10 provide interrupt control and status. Register 9 allows the microprocessor to selectively mask any of the interrupts. Register 10 identifies eight interrupt conditions: 0. D channel access has been lost via mismatch 1. The received I.430 "info state" has changed 2. Q channel multiframe has been completed 3. S word available 4. D channel transmission has been completed 5. D channel transmit queue is at or below a specified level 6. D channel receive queue is at or above a specified level 7. D channel end of frame has been received R4, bit 1 controls the interrupt polarity. Default is active high. See Table 4, Register 9 for details.
38	42	TIMOUT	O	**Timer Timeout.** This signal occurs when a programmable timer times out and on power-up. The power-up pulse becomes high when power first exceeds 2.8 V, and remains high for 1—15 ms. On a timer timeout, the pulse is of programmed polarity for a minimum of 57 μs. Register 4, bit 0 controls the polarity of this signal. Default is active high. Refer to Register 13 for details of the various modes of timer operation. TIMOUT is 3-stated when 1) $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
39	43	RESET	I	**Reset.** A high on this pin resets the device and forces a 3-state condition on all outputs except TIMOUT. The RESET pulse must be at least 175 ns. The TIMOUT and SYSCKO signals are 3-stated when 1) $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are low, 2) RESET is high, and 3) TIMOUT is not activated.
40	44	V_{DD}	—	**5 V Supply (Digital).** A 1.0 μF decoupling capacitor should be tied from V_{DD} to digital ground.

Architecture

The T7250A device provides the user network interface for terminal equipment. It operates from a 6.144 MHz clock, which can either be a crystal input or a clock input. There are six major blocks: the system interface controller, the system clocks, the 2B+D core, the HDLC formatter, the S/T transceiver, and the timer. Figure 1 shows a high level block diagram of the T7250A device.

System Interface Controller

The system interface controller conveys status and provides control for the T7250A. It maintains the register set and provides a microprocessor interface.

The microprocessor interface allows parallel asynchronous access to all control, data, and status registers. Separate address and data lines are available so that most general-purpose microprocessors can be interfaced easily.

All control and status registers are readable. There are two types of reads: a latched read or a dynamic read. The default is a latched read, but register 0 (R0), bit 4 allows the microprocessor to specify when reads should be dynamic. In the latched mode, the status is frozen when $\overline{RD}$ is activated. In the dynamic mode, changes in status are reflected on the data bus while $\overline{RD}$ is activated.

Wait states should not be required. Internally, 350 ns (worst case) is required for a write cycle, but the external interface only requires a write pulse of 50 ns.

The T7250A device has a programmable interrupt output, INT, to alert the microprocessor if it needs to be serviced. The polarity of INT is programmable and all interrupts are maskable. An interrupt status register reveals the source of the interrupt even if the interrupt is masked. Reading the status register resets the interrupt automatically. Once an interrupt is cleared, it is not regenerated until the condition has been cleared and reinstated.

System Clocks

The system clocks block provides several system level clocks - SYSCKO, CKCOD, and CKDM. SYSCKO is programmable via R4, bit 5 (Syscko) to be either a 6.144 MHz clock (Syscko=0) or a 192 kHz clock (Syscko=1). CKCOD is a 2.048 MHz clock that is an ideal master clock for codecs. All B channel clocks and frame timing signals are internally synchronized to CKCOD to reduce noise to peripheral devices. CKDM is programmable via R0, bit 1 (Ckdm) to be either the 16 kHz D channel clock (Ckdm=0) or an 8 kHz clock (Ckdm=1). All system clocks are free running at all times.

2B+D Core

The 2B+D Core is responsible for timing recovery, framing, transmit formatting, contention resolution, priority handling, S and Q channel multiframing. It also supports activation/deactivation procedures.

A digital phase lock loop extracts timing from a transformer coupled signal that is received from the NT. It derives a 192 KHz clock that is used for sampling all data, both transmit and receive.

The 2B+D Core also derives framing from received data. It creates separate clocks for B1 data, B2 data, Q data, S data, and D data. The B and D channel clocks are accessible for system use. The exact operation is programmable for maximum flexibility and ease of interface to peripheral devices. A B2 channel clock is always provided (CKB2). The user may specify via R0, bit 2 (C2pol=1) that the clock be inverted. This allows for interfacing with peripheral devices that transmit data on the falling edge of the clock and sample data on the rising edge of the clock (most HDLC controllers). Another clock can be programmed to be either a B1 clock or a continuous 192 kHz clock (MCKB1). As with the B2 clock, the user may specify that MCKB1 be inverted (Register 0, Bit 3).

Programmable frame timing signals (FSEB2 and FSEB1) are also provided. These signals provide the 8 kHz synchronization signal that is required by codecs. FSEB2 and FSEB1 are programmable via Register 4 bits 3 and 4 (B2f and B1f) to be either a frame strobe (Bxf=1) or an enable signal (Bxf=0). The timing of the enable signal is programmable via Register 4 bits 6 and 7. These 8 kHz frame timing signals are only present when a valid INFO state is being received. In effect, they automatically disable codecs when framing is lost.

Data received from the NT is provided on a single lead, RXDATA. The clocks and frame timing signals allow peripheral devices to extract the appropriate data. D channel data that is provided on RXDATA contains all HDLC formatting information. Normally, D channel data is accessed through R3 of the microprocessor interface.

The transmit formatter combines data and control as specified by I.430 and forms the 48 bit frame. Q and D channel data to be transmitted to the NT are entered through the microprocessor interface. Dedicated leads are provided for inputting B channel data to be transmitted to the NT. The multiplexed stream is sent to the S/T transceiver for transmission.

The 2B+D Core supports contention resolution that is required for passive bus operations. It continuously monitors the received D-echo bit and compares it to the previously transmitted D bit. If they match, the terminal is allowed to continue its transmission. If they do not match, the terminal is not allowed to transmit on the D channel. When the mismatch occurs, R10, bit 0 is set. The microprocessor can specify that it should be interrupted when this condition occurs. The S/T interface controller returns to the D channel monitoring state.

The 2B+D Core supports the CCITT I.430 priority mechanism. There are two classes of priority. Signaling information can be given priority over other types of information by selecting the high priority class. R8, bit 2 (pry) controls this function. The priority within a class also varies. The priority is automatically lowered within a priority class following a successful transmission. This gives all competing terminals fair access. The priority level is automatically restored when all terminals have had a chance to transmit. R8, bit 4 (lpry) is status that indicates the current priority within a class.

Multiframing is supported by the 2B+D Core. A multiframe was defined to provide synchronization for 4-bit Q channel in the TE to NT direction and a 20 bit S channel in the NT to TE direction. The S bits are synchronized within a multiframe by the M bit (26th bit of the I.430 NT to TE frame), which goes true once every twenty frames. Multiframe synchronization requires that INFO 2 or INFO 4 is being received, and that the M bit goes true exactly and only 20 frames from the previous M bit true. R7, bit 7(mse) provides status that indicates whether multiframe synchronization exists. The multiframe also provides Q channel synchronization. Q bits are identified by appropriately timed inversions of the FA/N pair, as specified in I.430. Q synchronization requires that INFO 2 or INFO 4 is being received, multiframe synchronization is established, and that the received FA, N bit inversions (FA=1, N=0) occur exactly and only five frames from the previous FA and N bit inversions. Bit 7 of R11(qse) provides status that indicates whether the FA/N Q channel synchronization exists. Two status bits (st0 and st1) are available in R7, bits 5 and 6, which also provide S and Q status. st0 and st1 indicate how many bits remain to be sent in the current multiframe, provided Q synchronization is true.

Two modes of operation exist for the S channel. When ssm (R8, bit 5) = 0, power-up default, all S bits are provided. In this mode, R7 provides five bit groups of received S bits. New data becomes available and the ss interrupt (R10, bit 3) can be generated during frames 1, 6, 11, and 16 of the 20 frame multiframe. For example, the S bits displayed by the frame 6 interrupt are from frames 1, 2, 3, 4, 5 where the S bit from frame 5 will be SB4 = R7, bit 4. S bits are cleared at system reset.

A second mode is also provided for the S channel. When ssm = 1, the S channel is considered as 4 groups of 5 bits, synchronized to the 20 frame multiframe. A state machine is envoked that performs a vote on each 5 bit group received and stores the resultant value. The 5 bit groups are identical to those described

in the ssm=0 mode. A 1 is stored if three or more of the 5 bits are 1s. At the end of the multiframe, the resultant 4 bit S word becomes available to the processor and the ss interrupt is generated. The first group (frames 1—5) is stored in SB0 = R7, bit 0.

Data nibbles to be transmitted on the Q channel are written to R11, bits 0—3. When data is written to R11, the enflg (bit 4) should be set. The nibble will be off-loaded internally in time, and the enflg bit will be cleared to indicate that a new nibble may be written to R11. The qdone interrupt can be set at the end of a Q nibble transmission. The qdone interrupt can serve to indicate when another nibble can be added. qdone interrupt is not generated if all 1s are being transmitted (default). If M or Q synchronization is lost, then Q channel automatically transmits 1s provided FA=1 in the received frame. For FA=0 (normal), 0s are transmitted in the Q position, as required by I.430.

CCITT I.430 link activation and deactivation procedures are also supported. The T7250A device continuously monitors and reports the receive information state through bits 0—3 of Register 1. The microprocessor can specify that it be interrupted when the receive information state changes. The T7250A device also allows the microprocessor to control the transmitted information state through bits 0 and 1 of Register 2. This allows the microprocessor to perform the link activation and deactivation procedures if desired.

The 2B+D Core also handles a B1 exchange B2 feature and B channel data inversion features. R8 bit 1 allows the user to specify that B1 and B2 information should be internally exchanged. This permits designers to connect a peripheral device to either channel without limiting its operation to the channel. R8, bits 6 and 7 (b1i and b2i) allows for inverting B2 and B1 data, respectively. This feature is useful for transmission on restricted channels.

Figure 10 provides a timing diagram that depicts the relationship of data on the line interface to data at the system interface. Figure 11 is a timing diagram that shows the various clocks and frame timing strobes that can be obtained from the UNITE.

HDLC Formatter

The HDLC formatter supports standard HDLC (high level data link control) formatting functions which include flag generation and detection, zero bit insertion/deletion, and error control using the CCITT-16 polynomial cyclic redundancy check (CRC). D channel data transfers are made through the microprocessor interface. Sixteen bytes of buffering are provided in both directions of transmission.

The HDLC transmitter performs flag generation, zero bit insertion, and calculates the CRC. The CRC is calculated in parallel to other processes as data is shifted out. Whenever five successive 1s occur in either the data or the CRC to be transmitted, the transmitter will automatically insert a zero bit after the fifth 1, regardless of the value of the next bit. This prevents the possibility of misinterpreting data or CRC as flags, aborts, or idles.

A D channel transmission is started by writing data to the sixteen byte transmit queue. The HDLC transmitter requests access to the link. The transmission begins after the S/T transceiver acknowledges by asserting the internal signal clear to send ($\overline{\text{CTS}}$). The internal signals can be accessed on the 44 pin PLCC.

Multiple frames can be written to the queue. All frames must be explicitly tagged with a transmitter frame complete (TFC). TFC should be asserted after the last byte of data has been written to the queue. If the last data byte that is transmitted is not tagged with TFC, then an underrun occurs. R14, bits 0—4 provide queue status indicating how many bytes can be added to the queue. The transmission will end without a stop flag, which causes an abort. Transmitter queue status is available which will indicate that an underrun occurred (UNDABT-R14, bit 5).

There are two HDLC transmitter interrupts. The TDONE interrupt becomes set after the transmitter has completed the transmission, including the last bit of the closing flag. The TE interrupt is set when the transmitter queue has reached the programmed level of emptiness (number of bytes available in the queue). Sixteen levels may be specified.

The HDLC transmitter provides the capability for transmitting a soft abort via R2, bit 2. The abort is transmitted in place of the specified data byte in the queue. An immediate abort can be achieved by resetting the transmitter. The HDLC transmitter also provides the capability of inverting all transmitted data.

The HDLC receiver detects flags, does zero bit deletion, and calculates the CRC. Formatting is done until the HDLC receiver recognizes another flag or an abort sequence. Zero bit deletion occurs whenever five successive 1s followed by a zero are received. The sixteen bit CRC pattern is computed in parallel to other activities as the serial data for the frame is shifted in. A receive queue manager keeps track of the queue status and updates the receive status register.

On power-up and reset, all data is ignored until a new frame occurs. A frame begins when a flag that is followed by data is detected. The interframe time fill may be flags or 1s. Also, two consecutive frames may share a flag. Formatting is done until another flag is detected or until an abort sequence (01111111) is detected.

The queue manager keeps track of the queue status and updates the receive status register. The receive status register (Register 5) indicates the following:

- Bit 7 indicates end of frame (EOF) status. This bit is a one if there is an end of frame anywhere in the queue.
- Bit 6 provides IDLE status. IDLE is set (1) when 15 consecutive ones have been received.
- Bit 5 indicates, when a one, that an OVERRUN occurred since the last read of the status register.
- Bits 0—4 indicate the number of bytes in the queue up to the first EOF. CRC bytes are not reported. Binary encoding is used. If no EOF is in the queue, the frame tells how many bytes are in the queue.

The queue manager also creates an EOF status byte for each frame and stores it in the queue. The following are included in each EOF status byte:

- Bad CRC (Bit 7) – A high (1) indicates that a transmission error occurred.
- Abort (Bit 6) – A high (1) indicates frame was aborted. An abort should not be reported when a flag is followed by seven 1s.
- Overrun (Bit 5) – A high (1) indicates that an overrun occurred (the sixteen bit queue size was exceeded).
- Bad Byte Count (Bit 4) – A high (1) indicates that the bit count received after zero bit deletion, was not a multiple of eight (i.e., an integer number of bytes).
- Bits 0—3 will be zero.

A frame that is closed normally also causes an EOF. A good frame is implied by an EOF status of all zeros. The receive queue level count in bits 0 through 4 of Register 5 includes the EOF status byte for the frame. The CRC bytes are not included in the queue. The last byte of a frame is always the status word.

When overrun occurs, an overrun status is set in the receive status register (R5) the receiver should be reset. When the overrun condition is cleared, the HDLC controller clears the CRC and waits for another frame (flag).

Two maskable interrupts, receive full (RF) and receive end of frame (REOF), are generated by the receiver. If the RF interrupt is enabled, then an interrupt is generated when the receive queue reaches a programmed level of fullness. Sixteen levels (1—16) may be specified. If the REOF interrupt is enabled, then an interrupt is generated when an REOF occurs.

S/T Transceiver

The S/T transceiver supports encoding and decoding of the 2B+D inverted alternate space inversion (ASI) line code format over four wires. A logical "1" is represented by the absence of a pulse, and a binary "zero" is represented by a positive or negative pulse alternately. Figure 4 provides a conceptual view and Table 2 shows a truth table of the encoding and decoding scheme. All timing is extracted from the bit and frame timing information that is received from the NT.

The S/T interface transmitter is a voltage limited current driver. When used with a simple line interface circuit, it conforms to the voltage limitations and impedance characteristics specified in CCITT I.430 for passive bus operation.

Table 2. Transmission Code

Positive Rail	Negative Rail	Current	Logic
Z	Z	0	1
1	0	+1	0
0	1	−1	0
Z	Z	0	1

*Z is for high impedance.

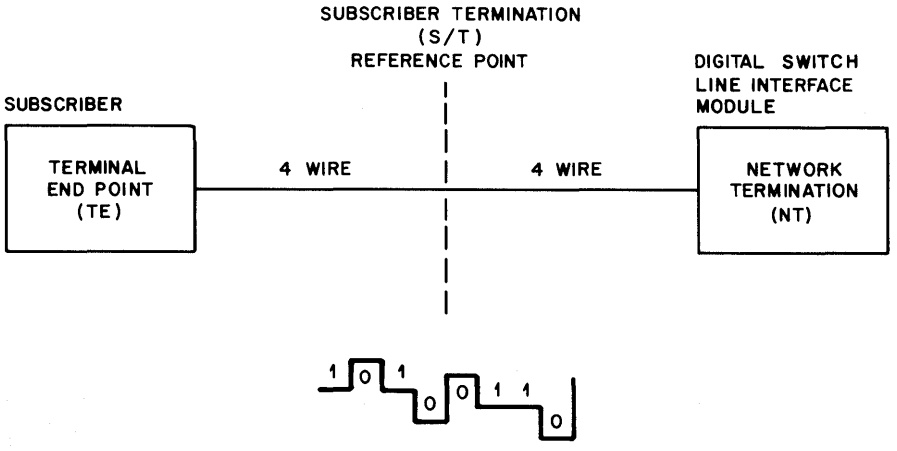


Figure 4. ISDN Basic Access Transmission Code

Timer

The T7250A device also has a built-in, general-purpose timer that can be configured for several modes of operation. The time interval is programmable from 0.127 seconds to 2.032 seconds, with a resolution of 0.127 seconds. The output of the timer goes to a pin called TIMOUT. TIMOUT is always asserted for a minimum of 55 μs. Assertion polarity defaults to active high, but can be programmed via a control register (R4, bit 0) to be active low.

The timer can be configured as a programmable timer, a programmable one-shot, an immediate one shot, or it can be completely disabled. The programmable timer mode produces a periodic TIMOUT pulse. The immediate one shot produces an immediate TIMOUT pulse. The programmable one-shot produces a TIMOUT pulse that is delayed by 127 usec times one more than the programmed offset. Four bits are used to encode the timer configuration. The timer is reset (restarted) when a designated code is written to register 13. The timer continues counting for its present state then it reloads when a non-designated code is written to register 13; the timer continues in its previous state.

Registers

The on-chip registers occupy sixteen locations in the memory map of the controlling microprocessor system. The location and function of each register are shown in Table 3. Separate address and data lines allow virtually any 8-bit or 16-bit microprocessor to be used. The registers are accessed under the control of the following signals address selects (A0—A3), chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), and the 8 bit bidirectional data bus (D0—D7).

Control registers can be written to or read by the microprocessor at any time. The ten control registers are R0, R2, R4, R6, R8, R9, R11, R12, R13, R14, and R15. Register 0 (R0) controls read modes and test modes. R2 controls the transmitter. R4 is a hardware configuration control register. This register allows the user to specify the desired timing of system interface signals. R6 is the control register for the buffer full and buffer empty interrupt trigger levels. R8 contains S/T interface controls. R9 contains interrupt mask controls. R11 controls multiframing. R12 controls loopback and transmit 1s functions. R13 provides timer mode control. R15 provides reset control. SPARE OR RESERVED BITS MUST BE PROGRAMMED TO ZERO.

All control registers are automatically initialized on power-up or reset. The HDLC transmitter and receiver and all interrupts are disabled so that the chip is quiet until it is awakened by the microprocessor. The system interface defaults to a viable configuration. The B channels and Codec clock interfaces come up in the mode suitable for the AT&T T7500 PCM Codec with Filters. FSEB1 and FSEB2 are the frame strobes but are disabled until INFO2 or INFO4 is received. All 1s are being transmitted and received on both B channels, which silences the codec. CKCOD is 2.048 MHz. The timer output (TIMOUT) polarity is active high. The interrupt, INT, is active high. B1 and B2 channel information are not interchanged. The S/T interface priority mechanism is activated and the priority class is signaling. The clock output on MCKB1 is selected to be the continuous 192 kHz clock. The timer defaults to be a 2.048 second timer.

Data registers provide read or write access to "D" channel transmit/receive data bytes. Data can be written to the 16 byte transmit queue by writing to register 3 (R3). Data can be read from the 16 byte receive queue by reading register 3. S channel data is accessed through register 7. Q channel data is specified through register 11.

Status registers are read only, and allow the microprocessor to inspect the status of various on-chip parameters. The status registers are R1, R5, R10, and R14. R1 provides line interface status. R5 provides D channel HDLC receiver status. R10 provides status information that reveals the source of the interrupt. R14 provides HDLC transmit queue status. R15 provides software resets, priority status, and transmit bad CRC control.

Registers 8 and 11 are mixed with both status and control (read and write). R11 provides Q channel transmission status.

Table 3 provides a register map showing the layout of all register bits. Table 4 details the functions of register bits.

Table 3. Register Map

Name	R/W*	T*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Chip/Hardware Configuration Register							
R0	R/W	C	0	0	0	Dynrd	C1pol	C2pol	Ckdm	0
			Line Interface Status							
R1	R/W	S	–	–	–	–	rss1	rss0	r1	r0
			Transmitter Control Register							
R2	W	C	ENR	ENT	RINV	TINV	TFC	TABT	tss1	tss0
R3	R/W	D	D CHANNEL DATA BYTE							
			Hardware Configuration Register							
R4	R/W	C	Codec1	Codec2	Syscko	B1f	B2f	Clkmux	Ipol	Tpol
			HDLC Receiver Status							
R5	R	S	EOF	RIDL	OVERRUN	RCV QUEUE STATUS				
			Interrupt Trigger Levels For D Channel Queues							
R6	R/W	C	RECEIVE FULL LEVEL				TRANSMIT EMPTY LEVEL			
			Multiframe Status and S Channel Queues							
R7	R	D	mse	st1	st0	S channel data				
			S/T Interface Control							
R8	R/W	M	b1i	b2i	ssm	lpry	prye	pry	b1xb2	clrmm
			Interrupt Masks							
R9	R/W	C	REOFIE	RFIE	TEIE	TDIE	ssie	qdie	richgie	mmie
			Interrupt Status							
R10	R	S	REOF	RF	TE	TDONE	ss	qdone	richg	mm
			Q Channel Data and Status							
R11	R/W	M	qse	–	doneq	enflg	Q Channel Data			
			Loopback and Transmit 1's Control							
R12	R/W	C	tlb1	tlb2	lld	llb1	llb2	rld	rlb1	rlb2
			Timer Configuration Control							
R13	R/W	C	Timer Mode				Timer Offset			
			Transmitter Queue Status							
R14	R/W	M	0	0	UNDABT	XMIT QUEUE STATUS				
			Software Resets							
R15	W	C	0	0	0	TCRCB	0	TRES	RRES	Mres
R15	R	S	–	–	–	TCRCB	ecd	ecc	ecb	eca

*R/W – Read/write control; T – Type of register; C – Control register; S – Status register; M – Both control and status; D – Data register

Note: Upper-case letters in Tables 3 and 4 specify control and status parameters for D channel HDLC. Lower-case letters specify control and status parameters for 2B+D core. Bits named with an upper-case letter followed by lower-case letters are system configuration parameters.

Table 4. Register Bit Definitions

Name	Bit(s)	Symbol	Name/Function
R0	0	–	**Reserved.** Program to zero for normal operation.
R0	1	Ckdm	**D Channel Clock Mux.** This bit controls the frequency of the clock that is output on CKDM (pin 40 of the PLCC). When Ckdm = 0 (default), CKDM is the 16 kHz D-Channel clock. When Ckdm = 1, CKDM is a 50% duty cycle 8 kHz free running clock.
R0	2	C2pol	**CKB2 Clock Polarity.** This bit controls the phase of CKB2 (pin 38 of PLCC) relative to the internal clock that is used for sampling and transmitting data. C2pol should be programmed to zero when the CKB2 is connected to devices that transmit on the rising edge and sample data on the falling edge (most codecs). C2pol should be programmed to one when CKB2 is connected to a device that transmits on the falling edge and sample data on the rising edge (most HDLC controllers).
R0	3	C1pol	**MCKB1 Clock Polarity.** This bit controls the phase of MCKB1 (pin 36 of PLCC) relative to the internal clock that is used for sampling and transmitting data. C1pol should be programmed to zero when MCKB1 is connected to devices that transmit on the rising edge and sample data on the falling edge (most codecs). C1pol should be programmed to one when MCKB1 is connected to a device that transmits on the falling edge and samples data on the rising edge (most HDLC controllers).
R0	4	Dynrd	**Dynamic Read.** When set, this bit specifies that all reads are dynamic. The µP can continuously monitor status bits as long as read is low. When zero (default), all reads will be latched.
R0	5–7	–	**Not Described.** Program to zero for normal operation.
R1 R1	0 1	r0 r1	**Previous Received Information Pattern.** r0 and r1 reflect the received information pattern that caused the received information change "richg" (R10, bit 1) interrupt. r0 and r1 are encoded the same as rss0 and rss1. When r0 and r1 are different from rss0 and rss1, the received information pattern has changed since the interrupt.
R1 R1	2 3	rss0 rss1	**Current Received Information Pattern.** Contains the CURRENT information pattern being received from the NT. **rss1 rss0 Definition** 0 0 Info 0 0 1 Info 2 1 0 Info 4 1 1 Lost framing Info 0 is no signal (64 successive 1s). Info 2 is normal framing with all B and D bits set to binary zero; the A bit is zero. Info 4 is normal framing with synchronized 2B+D data and D echo; the A bit is 1. See CCIT I.430 (section 6.2.2). Lost framing is assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of code violations.

Table 4. Register Bit Definitions (Continued)

Name	Bit(s)	Symbol	Name/Function
R1	4—7	—	**Not Described.** Program to zero. Bits 4—7 are internal status not intended for system applications.
R2 R2	0 1	tss0 tss1	**Transmit Serial Stream.** (To NT). These bits control what information pattern is being transmitted to the NT. **tss1 tss0 Definition** 0 0 Info 0 (default) 0 1 Info 1 1 x Info 3 Where Info 0 is no signal (64 consecutive 1s), Info 1 is a continuous signal with a pattern of positive 0, negative 0, and six 1s, and Info 3 is synchronized frames with operational data on B and D channels. See CCITT I.430 (section 6.2.2).
R2	2	TABT	**Transmit Abort (D Channel).** Setting this bit instructs the internal HDLC transmitter to abort the frame. It writes over the previous byte in the queue. The transmitter will finish shifting out the data in the queue, then transmit the abort sequence (01111111). TABT is cleared on power-up and reset.
R2	3	TFC	**Transmit Frame Complete (D Channel).** Setting this bit instructs the internal HDLC transmitter to close the frame normally after the last data byte. The 16-bit CRC and the closing flag are appended. This bit should be set within 500 μs of writing the last data byte of the frame to the queue. (Default = 0)
R2	4	TINV	**Transmit Inverted Data (D Channel).** If this bit is set, transmitted D-bit data streams are inverted. (Default = 0)
R2	5	RINV	**Invert Received Data (D Channel).** If this bit is set, received D-bit data streams are inverted. (Default = 0)
R2	6	ENT	**Enable Transmit (D Channel).** Setting this bit enables the HDLC transmitter (for TE to NT transmission). When the transmitter is disabled, 1s are transmitted. On power-up and reset, the transmitter is disabled.
R2	7	ENR	**Enable Receive (D Channel).** Setting this bit enables the HDLC receiver (for NT to TE reception). On power-up and reset, the receiver is disabled.
R3	0—7	DBYTE	**D Channel Data.** The D channel data byte to be transmitted is loaded through this register (on write). Also, the D channel data byte received is accessed through this register.
R4	0	Tpol	**Timeout Polarity.** When set, this bit causes the polarity of the timeout signal on TIMOUT to be active high. Tpol equal to zero specifies that TIMOUT should be active low. This bit is set on power-up and reset. **CAUTION:** TIMOUT will always default to active high on power-up and reset. System designers need to consider what effect this will have. TIMOUT will also be asserted (high) on power-up for 1 to 15 ms.

Table 4. Register Bit Definitions (Continued)			
Name	**Bit(s)**	**Symbol**	**Name/Function**
R4	1	Ipol	**Interrupt Polarity.** Setting this bit specifies that the hardware interrupt signal, INT, is active high (default). If this bit is zero, the INT signal is active low.
R4	2	Clkmux	**Clock Multiplexor.** When this bit is set to 1 (default), the hardware clock output signal on MCKB1 is CK192 (192 kHz). Otherwise, the clock signal is CKB1, a 192 kHz clock that is active only during B1 time slot.
R4	3	B2f	**B2 Framing.** Setting this bit (default) forces the hardware signal on FSEB2 to be a frame strobe (see Table 1). If b2f = 0, FSEB2 puts out a gating signal (envelope) for the duration of B2 channel data. The timing of the envelope is defined by bit 6 of R4.
R4	4	B1f	**B1 Framing.** Setting this bit (default) forces the hardware signal on FSEB1 to be frame synchronization (see Table 1). If b1f = 0, FSEB1 puts out a gating signal (envelope) for the duration of B1 channel data. The timing of the envelope is defined by bit 7 of R4.
R4	5	Syscko	**System Clock.** When zero (default), this bit specifies that the output SYSCKO (pin 28 of the PLCC) should be a 6.144 MHz clock. When set, this bit specifies that SYSCKO should be a 192 KHz clock. For minimum power consumption, program this bit to a one.
R4	6	Codec2	**B2 Codec Option.** This bit specifies the timing relationship between the B2 envelope (FSEB2 when R4, bit 3 is zero) and the start of the first bit of B2 data. Setting this bit specifies that FSEB2 will occur one-half clock cycle before the first bit of B2, on the falling edge of the 192 kHz clock. If this bit is cleared (default), FSEB2 occurs with the first bit of B2 on the rising edge of the 192 kHz clock. This function does not impact the timing of FSEB2 when it is programmed to be a strobe(i.e., when R4, bit 3 is set).
R4	7	Codec1	**B1 Codec Option.** This bit specifies the timing relationship between the B1 framing sync and the first bit of B1 data. Setting this bit specifies that FSEB2 will occur one-half clock cycle before the start of the first bit of B1 on the falling edge of the 192 kHz clock. If this bit is cleared (default) FSEB1 occurs with the first bit of B1 on the rising edge of the 192 kHz clock. This function does not impact the timing of FSEB1 when it is programmed to be a strobe (i.e., when R4, bit 4 is set).
R5	0—4	RECEIVE QUEUE STATUS	**Receive Queue Status (D Channel).** These bits tell how many bytes are available to the first EOF. If no EOF, the number of bytes in the queue is provided. Binary encoding is used and bit 0 is the LSB.
R5	5	OVERRUN	When set, this bit indicates that overrun has occured. The bit is cleared when the status is read.

Table 4. Register Bit Definitions (Continued)

Name	Bit(s)	Symbol	Name/Function
R5	6	RIDL	**Receive Idle (D Channel).** This condition is set when the idle sequence of fifteen contiguous 1s is detected.
R5	7	EOF	**End of Frame (D Channel).** This flag is set when an EOF exists in the queue. When EOF is set, the receive queue status reflects the number of bytes to the first EOF status.
R6	0—3	TRANSMIT EMPTY QUEUE INTERRUPT LEVEL	**Transmit Empty Interrupt Trigger Level (D Channel).** These bits specify the minimum number of empty bytes in the transmitter queue that will trigger a transmit empty (TE) interrupt. Encoding is in binary, bit 0 is the LSB. A code of 0000 means buffer empty.
R6	4—7	RECEIVE FULL QUEUE INTERRUPT LEVEL	**Receive Fill Interrupt Trigger Level (D Channel).** These bits specify the minimum number of bytes in the receiver queue that will trigger a receive full interrupt (RF). Encoding is in binary and bit 0 is LSB. A code of 0000 means buffer full (16 bytes are available).
R7	0—4	SDATA	**S Channel Data.** When ssm = 0 (Register 8, bit 5 is a zero) these bits provide 5 bits of S channel data. The five data bits, SB4—SB0, (R7, bit 4—0) display the previous five received S bits, where SB0 is the first received bit. When ssm = 1, bits 0—3 provide the four bits of S channel data that results from the four votes over the 20 frame multiframe. Frames 1 to 5 S bits are voted on and presented in SB0, while frames 16 to 20 are presented in SB3, SB4 is zero when ssm=1.
R7 R7	5 6	st0 st1	**Multiframe State Machine Bits.** These bits indicate how many bits remain to be sent in the present multiframe provided Q sync is true. They also indicate which quadrant the "S" bits are in provided multiframe sync is true. st1 st0 Q Bits to Send S-Bit Group 0 0 None or 4 16—1 0 1 One 1—6 1 0 Two 6—11 1 1 Three 11—16 These states change in frames 1, 6, 11, and 16 at the rise of qbm. The st1 and st0 bits become valid at qbm time of multiframe 16 after mse goes true.
R7	7	mse	**Multiframe Synchronization Established.** mse goes high (true) when M bit synchronization has occurred. Requirements are that frame synchronization is established and that received frame bit 26, M Bit, goes true exactly and only 20 frames from the previous M Bit true. mse will go true at the middle of 28th receive frame and will go false with the same timing for missed expected M bit or M bit at wrong frame. mse also goes false immediately with loss of frame synchronization.

Table 4. Register Bit Definitions (Continued)

Name	Bit(s)	Symbol	Name/Function
R8	0	clrmm	**Clear Mismatch.** If zero (default), the mm flag operates normally. When a mismatch occurs, the transmitter automatically forces all 1s on the D channel. A microprocessor read will clear the mm flag. A 1 on clrmm forces the mismatch flag, mm, to zero. Setting this bit disables the D channel contention resolution; thus, this bit must be zero for ISDN I.430 operation.
R8	1	b1xb2	**Exchange B1 with B2.** When 1, data received on the B1 channel from the NT will be transmitted to the TE (on RXDATA) on B2 channel and vice versa. Data from TXB2 will be transmitted to the NT on B1 channel, while data from TXB1 will be transmitted on B2. No exchange occurs if this bit is set to zero (default).
R8	2	pry	**Priority.** This bit represents the priority class for D channel access. A zero specifies high priority (signaling); a one specifies low priority (data) class. See the CCITT I.430. This bit is cleared on power-up and reset.
R8	3	prye	**Priority Enable.** When set (default), the priority mechanism for passive bus operation is active. The device waits for idle echo D bit (i.e., E bit) such that $C \geq X$, where C equals the count of consecutive E bits set (1) and X equals the priority number (8, 9, 10, or 11) for the terminal endpoint. Eight is the highest priority. D channel messages are sent when $C \geq X$. When this bit is cleared, messages are only sent on demand, invalidating networking. This bit must be set for ISDN I.430 operation. See CCITT I.430 (6.1.4).
R8	4	lpry	**Low Priority Status.** This bit indicates the current priority within a priority class; 1 for low priority, 0 for high priority. The user cannot change this bit, it can only be monitored. This bit is set when a D channel message is successfully transmitted to the network. It is cleared as soon as priority requirements are satisfied.
R8	5	ssm	**S Channel State Machine Mode.** When set, the S channel state machine is enabled. The voting mechanism is performed on groups of five bits. The resultant four bit S word is provided. When zero (default), all S channel bits are passed to the processor.
R8	6	b2i	**B2 Invert.** One specifies that all B2 data, both transmit and receive, should be inverted. When 0 (default), data is not inverted.
R8	7	b1i	**B1 Invert.** One specifies that all B1 data, both transmit and receive, should be inverted. When 0 (default), data is not inverted.
R9	0	mmie	**Mismatch Interrupt Enable.** When the mismatch interrupt enable bit is set, the hardware interrupt signal INT is generated if there is a D echo bit mismatch. See Register 10, bit 0, described following. mmie is cleared on power-up and reset.

Table 4. Register Bit Definitions (Continued)			
Name	**Bit(s)**	**Symbol**	**Name/Function**
R9	1	richgie	**Received Information Change Interrupt Enable.** When this interrupt enable bit is set, the hardware interrupt signal INT is generated when the received information pattern from the NT side changes. See Register 10, bit 1, described following. richgie is cleared on power-up and reset.
R9	2	qdie	**Q Done Interrupt Enable.** When this interrupt enable bit is set, the hardware interrupt signal, INT, is generated when a Q data nibble has been transmitted. See Register 10, bit 2, described following. qdie is cleared on power-up and reset.
R9	3	ssie	**S Channel Interrupt Enable.** When this interrupt enable bit is set, the hardware interrupt signal, INT, is generated when a new S word is available.
R9	4	TDIE	**Transmit Done Interrupt Enable (D Channel).** When this interrupt enable bit is set, the hardware interrupt signal, INT, is generated when the TDONE status bit is set (i.e., after the last bit of the closing flag). See Register 10, bit 7, described following. TDIE is cleared on power-up and reset.
R9	5	TEIE	**Transmit Empty Interrupt Enable (D Channel).** If this interrupt enable bit is set, the hardware interrupt signal INT is generated when HDLC transmit buffers have reached the programmed level of emptiness. See Register 10, bit 5, described following. TEIE is cleared on power-up and reset.
R9	6	RFIE	**Receive Fill Interrupt Enable (D Channel).** When this interrupt enable bit is set, the hardware interrupt signal INT is generated when HDLC receive buffers have reached their programmed level of fullness. See Register 10, bit 6, described following. RFIE is cleared on power-up and reset.
R9	7	REOFIE	**Receive End Of Frame Interrupt Enable (D Channel).** When this interrupt enable bit is set, the hardware interrupt signal INT is generated when an end of frame is detected by the HDLC receiver. See Register 10, bit 4, described following. REOFIE is cleared on power-up and reset.
R10	0	mm	**Mismatch.** This bit becomes set when the received E bit (D channel echo bit) does not equal the previously sent D bit while a D channel message is being transmitted (i.e., while CTS is active). A hardware interrupt is generated only if the corresponding interrupt enable bit is set in Register 9. This status bit is cleared after it is read by the microprocessor.

Table 4. Register Bit Definitions (Continued)			
Name	**Bit(s)**	**Symbol**	**Name/Function**
R10	1	richg	**Received Information Changed.** If set (1), the received information pattern has changed. Bits r0 and r1 (bits 4 and 5 of R1) contain the new information pattern which caused the richg bit to be set. Since rss0 and rss1 (bits 2 and 3 of R1) contain the current received information pattern, if the received information pattern changes after richg = 1, the microprocessor will be able to detect that change. A hardware interrupt is generated if the corresponding interrupt enable bit is set in Register 9. This status bit is cleared after it is read by the microprocessor.
R10	2	qdone	**Q-Done.** Q transmission just completed.
R10	3	ss	**S Channel Word Available.** This status is set when a group of S bits is available. The group is either 4 or 5 bits, depending on the value of ssm (Register 8, Bit 5). This status is only set when Multiframe synchronization is present.
R10	4	TDONE	**Transmit Done (D Channel).** This status bit is set when transmission of the current HDLC frame has been completed, either after the last bit of the closing flag or after the last bit of an abort sequence. A hardware interrupt is generated only if the corresponding interrupt enable bit is set in Register 9. This status bit is cleared on a microprocessor read of Register 10.
R10	5	TE	**Transmit Empty (D Channel).** If this bit is set, the HDLC transmit buffers are at the programmed level of emptiness. A hardware interrupt is generated if the corresponding interrupt enable bit is set in Register 9. This status bit is cleared after it is read by the microprocessor.
R10	6	RF	**Receive Full (D Channel).** This bit is set when the HDLC receive buffers are at the programmed level of fullness. A hardware interrupt is generated if the corresponding interrupt enable bit is set in R9. This status bit is cleared after it is read by the microprocessor.
R10	7	REOF	**Receive End of Frame (D Channel).** This bit indicates that receiver has finished receiving a frame. It becomes active upon reception of the last bit of the closing flag of a frame or the last bit of an abort. A hardware interrupt is generated if the corresponding interrupt enable bit is set in R9. This status bit is cleared after it is read by the microprocessor and after a receiver reset (RESET pin asserted, Mres, or RRES).
R11	0–3	qdata	**Q Channel Data.** Bit 0 is transmitted first. These four bits are transmitted during the 20 frames of a multiframe, one bit each 5 frames. qdata may be written when enflg (R11, bit 4) is low.
R11	4	enflg	**Enable/Flag.** This dual purpose bit is written high when writing qdata. This bit is internally reset to indicate new qdata may be written.

Table 4. Register Bit Definitions (Continued)			
Name	**Bit(s)**	**Symbol**	**Name/Function**
R11	5	doneq	**DONE Q Nibble.** Status bit which, when high, indicates a 4 bit Q word has been transmitted. This signal will stay high until a new 4-bit q word is loaded for transmission.
R11	6	—	**Not Described.** Program to zero. Internal status not intended for system applications.
R11	7	qse	**Q Bit Synchronizaation Established.** qse requires frame sync, M bit sync, and received frame FA,N bits flipped (FA = 1, N = 0) exactly and only five frames from the previous FA and N bits flipped. qse will go true at the end of receive frame bit 15 and falls immediately with loss of M bit or frame sync.
R12	0	rlb2	**Remote Loop B2 Channel.** When 1, the received B2 channel is looped back to the network terminator (NT). When zero (default), there is no loopback.
R12	1	rlb1	**Remote Loop B1 Channel.** When 1, the received B1 channel is looped back to the NT. When zero (default), there is no loopback.
R12	2	rld	**Remote Loop D Channel.** When 1, D channel data received from the NT is looped back to NT. When zero (default), there is no loopback.
R12	3	llb2	**Local Loop B2 Channel.** A value of 1 loops the B2 channel data received on the TXB2 input back through the RXDATA output, and a steady stream of 1s is sent to the network side. When zero, there is no loopback. The default values of llb2 and of t1b2 are both one, which, in effect, sets all data received from the network on RXDATA to a 1. This can be used to silence Codecs.
R12	4	llb1	**Local Loop B1 channel.** A value of 1 loops the B1 channel data received on the TXB1 input back through the RXDATA output, and a stream of 1s is sent to the NT. When zero, there is no loopback. The default values of llb1 and t1b1 are both zero, which in effect sets all data received from the network on RXDATA to a 1.
R12	5	lld	**Local Loop D Channel.** A value of 1 loops the D channel HDLC transmit data back to the terminal. A continuous stream of 1s is sent from the terminal to the network termination. **Note:** it is necessary to ignore mismatches (R8, bit 0, CLRMM=1) during local loopback D. When zero (default), there is no loopback.
R12	6	t1b2	**Transmit 1s on B2.** Setting this bit to 1 sends a stream of 1s on the B2 channel. When zero, this bit allows normal B2 channel traffic. The default values of t1b2 and llb2 are both 1, which in effect sets all data received from the network on RXDATA to a 1. This can be used to silence Codecs.
R12	7	t1b1	**Transmit 1s on B1.** Setting this bit sends a stream of 1s on the B1 channel. When zero, this bit allows normal B1 channel traffic. The default values of t1b1 and llb1 are both 1, which in effect sets all data received from the network on RXDATA to a 1.

Table 4. Register Bit Definitions (Continued)

Name	Bit(s)	Symbol	Name/Function
R13	0 1 2 3	Tm0 Tm1 Tm2 Tm3	**Timer Offset.** The internal timer is programmable from 0.127 seconds to 2.032 seconds, with a resolution of 0.127 seconds. These bits specify the timeout interval as follows: **Tm3 Tm2 Tm1 Tm0 Definition** 1 1 1 1 2.032 second (default) . . . straight binary count 0 0 0 0 0.127 seconds
R13	4 5 6 7	Tm4 Tm5 Tm6 Tm7	**Timer Mode.** These bits specify how the timer will be used. **Tm7 Tm6 Tm5 Tm4 Definition** 0 0 1 0 Programmable timer (default) 0 1 1 0 Programmable one-shot 1 0 1 0 Timer disabled 1 1 1 0 Immediate pulse on TIMOUT all others Ignored The timer is restarted when a valid code is written.
R14	0 1 2 3 4	HDLC TRANSMIT QUEUE STATUS	**HDLC TRANSMIT QUEUE STATUS.** These bits tell how many bytes can be added to the transmit queue. The bits are encoded in binary. Bit 0 is the LSB.
R14	5	UNDABT	**Underrun Abort.** A one indicates that an abort was transmitted on the D channel due to transmitter queue underrun. This occurs when the last byte in the queue is not tagged with TRANSMIT FRAME COMPLETE (TFC-R2, bit 3). The bit is cleared when the status is read.
R14	6, 7	–	**Not described.**
R15	0	Mres (control)*	**Master Reset.** Setting this bit resets the HDLC controller and the S/T interface controller. The timer and control register settings are not affected. Control registers are not reset since the microprocessor interface is assumed sane if this bit was accessed. Asserting the RESET pin, or power-up will reset the microprocessor interface.

* Bits 0—2 in Register 15 are used in two modes (control and status). Writes to bits 0—2 control software resets. Priority status is provided when register 15 is read.

Table 4. Register Bit Definitions (Continued)

Name	Bit(s)	Symbol	Name/Function
R15	1	RRES (control)*	**Receiver Reset (D Channel HDLC).** Setting this software bit resets the HDLC receiver. The receiver queue and related status are cleared. The receive end of frame (REOF) and receive queue full (RF) status bits and interrupts are cleared.
R15	2	TRES (control)*	**Transmitter Reset (D Channel HDLC).** Setting this software bit resets the HDLC transmitter. The transmit queues related status are initialized. TDONE, and TE are deactivated. TRES should be used to clear the transmitter when a mismatch occurs.
R15	0—3	eca—ecd (status)*	**Priority Mechanism Counter.** Contains a count of the number of consecutive logical ones on the D channel.
R15	4	TCRCB	**Transmit CRC Bad.** Setting this bit forces the HDLC transmitter to produce a bad CRC. This bit should be programmed to zero (default) for normal operation.
R15	5—7	0	**Not described.** Bits 5—7 must be programmed to zero for normal operation.

*Bits 0—2 in Register 15 are used in two modes (control and status). Writes to bits 0—2 control software resets. Priority status is provided when register 15 is read.

Integrated Voice Data Application

A 6.144 MHz crystal provides the clock. The T7500 Codec (in Figure 5) is used for voice on the B1 channel. The B2 channel is connected to an AT&T T7111 (HDLC controller) for data transmission. Also shown are the S/T interface connections and power and ground considerations for the T7250A device. With the hardware configuration as shown, B1 data transmission or B2 voice transmission can be achieved by telling the T7250A to exchange B1 and B2 channel information.

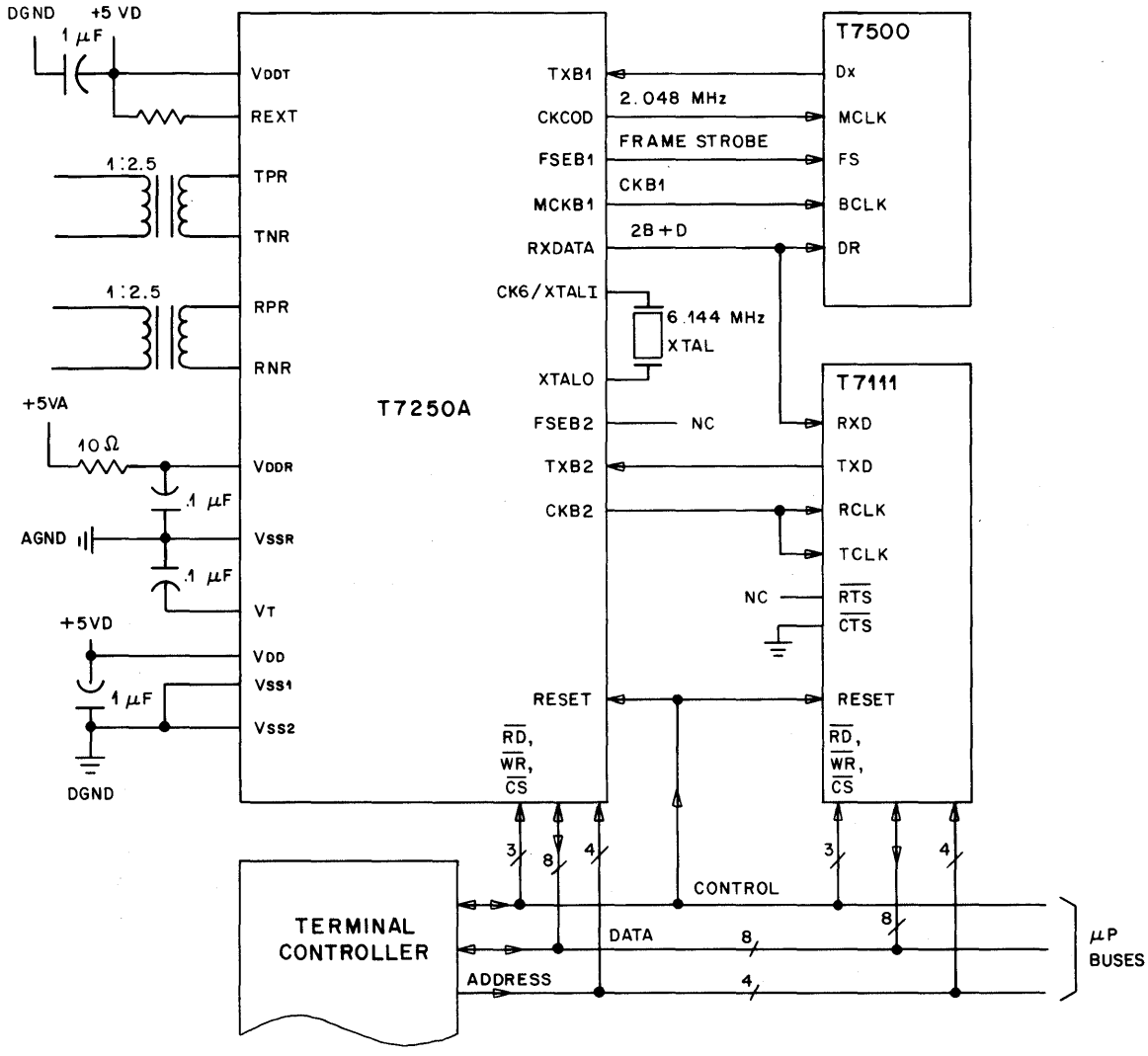


Figure 5. Connection Diagram for Integrated Voice/Data Application.

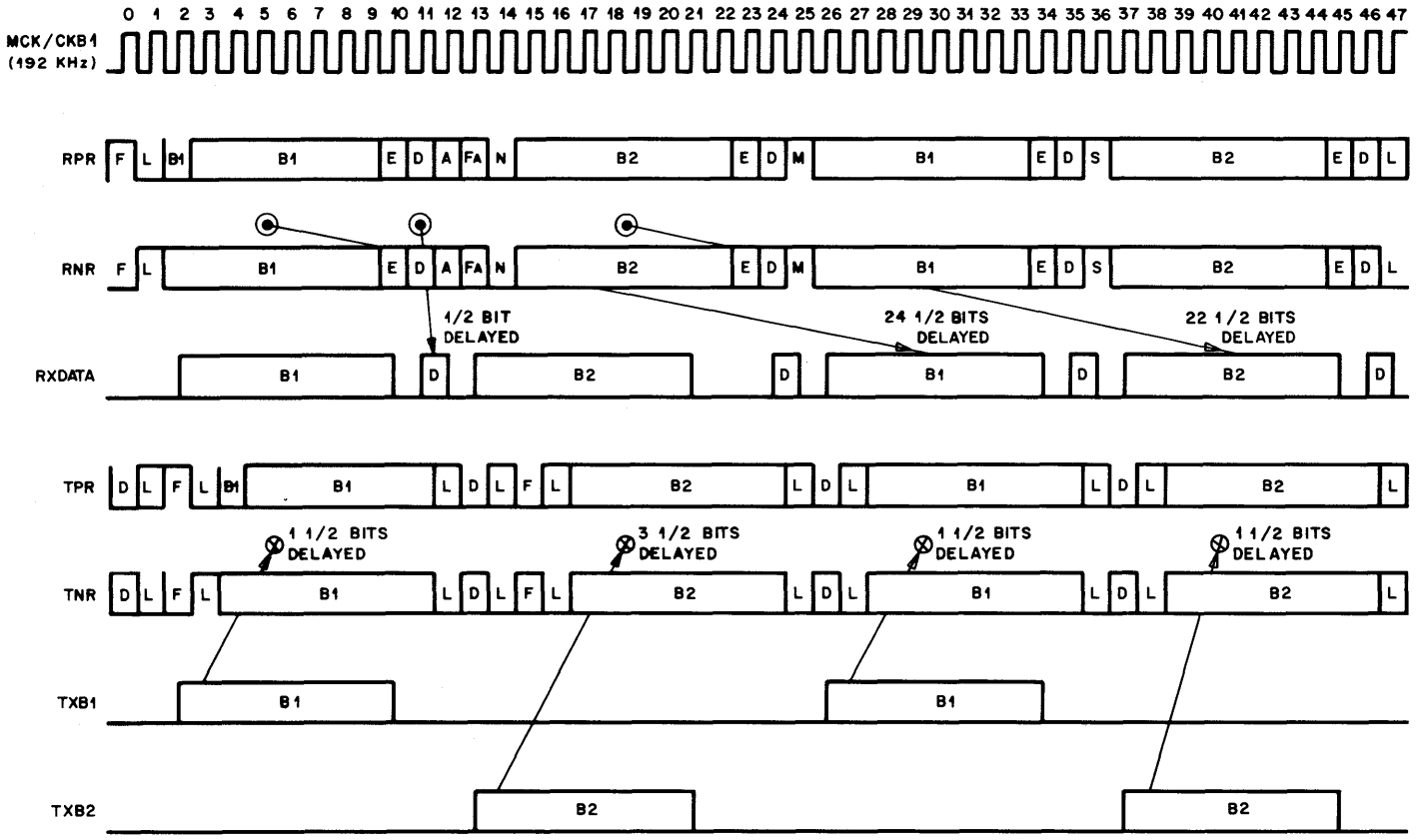


Figure 6. Bit Alignments on the S/T Interface Relative to the System Interface

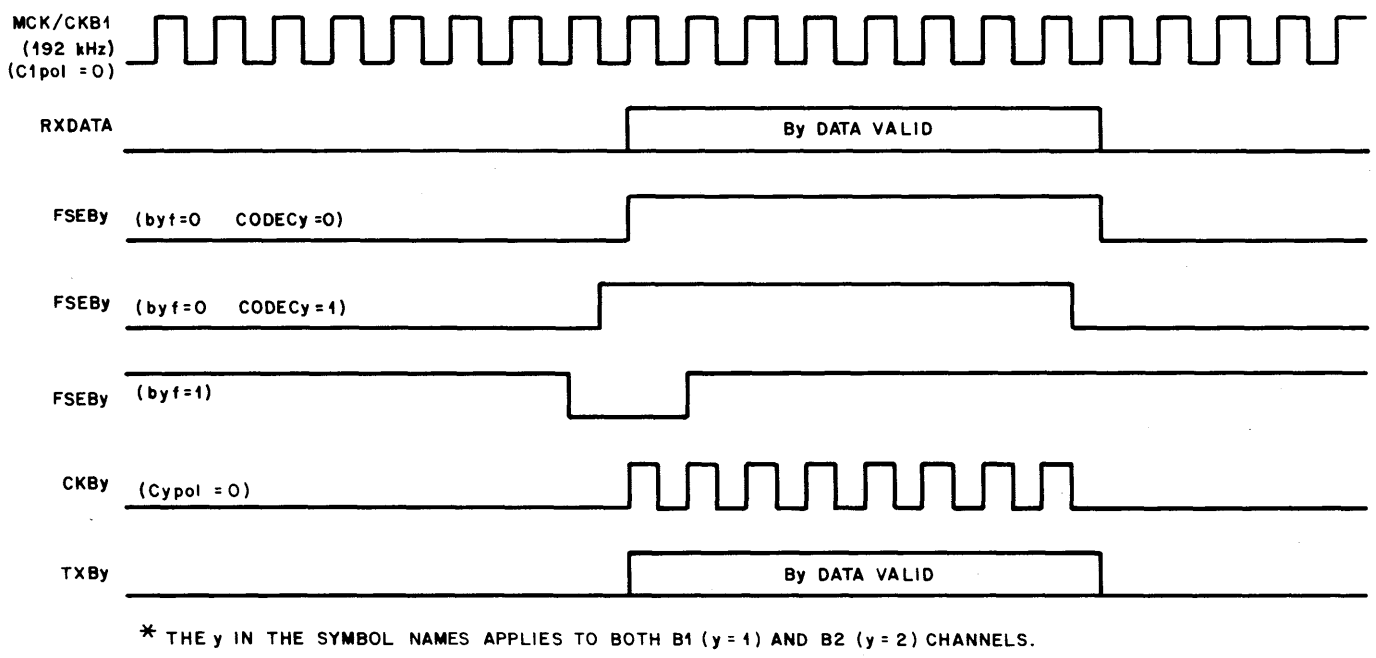


Figure 7. Functional Bit Alignment Timing on the System Interface

The information contained herein is advance and subject to change.

FEATURES

- Network termination (NT) device for four-wire ISDN Basic Access (I.430) subscriber lines at the S/T reference point
- Full-duplex 2B+D interface for point-to-point and point-to-multipoint (passive bus) configurations
- Basic access B1, B2, and D channels separated from and combined into 192 kb/s stream
- Two independent transmit/receive serial highways with assignable time slots for voice or data transfer
- User-defined organization of serial highways through programmable offset and edge-selection bits
- Compatible with AMD and Intel dual PCM highways for 32 and 64 time-slot operation
- Parallel microprocessor interface with either multiplexed or demultiplexed address/data lines and maskable interrupts for easy interface to any microprocessor
- Memory-mapped registers to control time-slot assignment, activation/deactivation, local/remote loopback modes, and interrupts
- Capability for direct microprocessor control of B1, B2, or D channel through the microprocessor interface
- Memory-mapped registers to control time-slot assignments, interrupts, activation/deactivation, and loopback modes
- Fully adaptive timing employed by analog receiver for both point-to-point and passive bus configurations, with automatic level switching between sampling thresholds
- Multiframing support, with access to the "S" (NT-to-TE) and "Q" (TE-to-NT) channels through microprocessor registers
- On-chip digital phase locked loop for 192 kHz clock derivation from a user supplied 6.144 MHz clock
- No HDLC termination of B1, B2, and D channels
- Low-power CMOS with TTL-compatible digital inputs/outputs
- Power-down mode, controlled via the microprocessor interface, to reduce power dissipation to < 15 mW
- Fifteen different loopback configurations
- Outputs 3-state for bed-of-nails testing

DESCRIPTION

The AT&T T7252 ISDN Basic Access User Network Interface Termination for Switches (UNITS) is a silicon integrated circuit that provides level 1 network termination (NT) functions in the integrated services digital network (ISDN). An expected application of the T7252 device is in digital-switch line cards connecting to terminal equipment (TE) at the S/T ISDN reference point. A basic access loop may be terminated at the TE with the AT&T T7250A device (UNITE). Other applications for the UNITS are: network terminators (NT1/2), remote multiplexers or concentrators. The UNITS device provides full-duplex 2B + D communication at 192 kb/s over a four-wire 26-gauge digital subscriber loop. Channels B1 and B2 are 64 kb/s voice or data channels; the D channel is a 16 kb/s control or data channel. All point-to-point and point-to-multipoint (passive bus) configurations, as defined in the June, 1986 version of CCITT Recommendation I.430, are supported. UNITS communicates with the switching network over a user-configured TDM (Time Division Multiplexed) highway. A generic microprocessor interface is also provided.

The UNITS device is manufactured in low-power 1.25 micron CMOS technology and is available in a 44-pin plastic leaded chip carrier or 40-pin plastic DIP (with reduced functionality). It requires a single 5 V supply and has a maximum power dissipation of less than 100 mW. The UNITS device has an operating temperature between 0 °C and 70 °C and is TTL compatible with 3-state outputs.

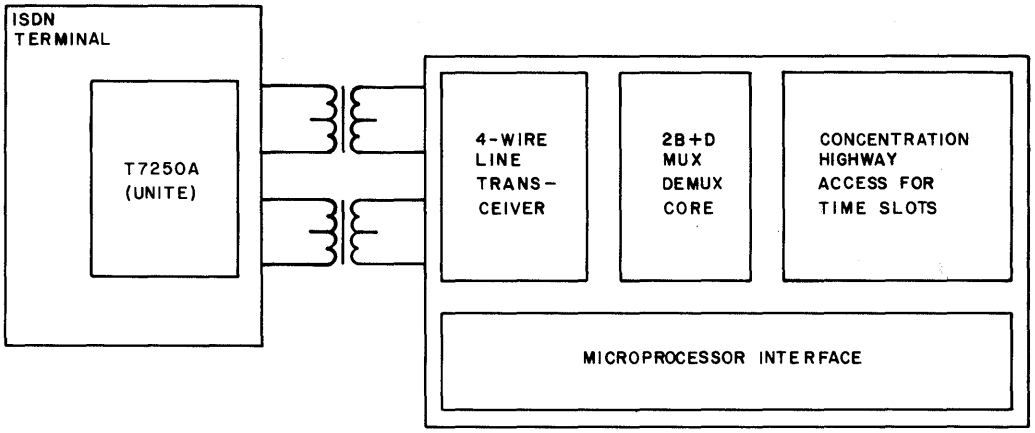


Figure 1. T7252 UNITS Block Diagram

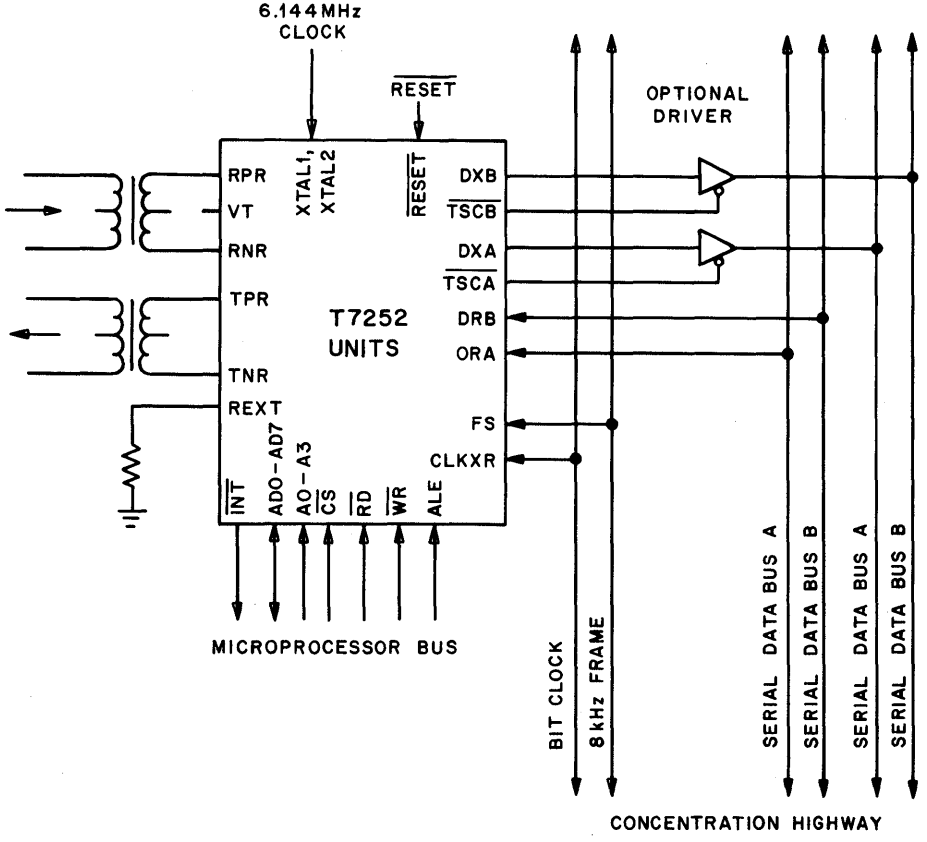


Figure 2. T7252 System Application

The information contained herein is advance and subject to change.

FEATURES

- U-interface for two wire operation for both central office (CO) and network termination (NT) applications
- 144 kb/s full duplex using echo cancellation (EC)
- Alternate mark inversion (AMI) line code as used in AT&T *5ESS* Switch
- Extended loop range with tolerance to bridged taps
- Digital I/O via the AT&T K-interface
- On-chip balanced line driver
- Balanced continuous time filters
- Adaptive equalization and automatic gain control (AGC)
- Power-down option
- LED driver to signal loss of framing
- Decision feedback equalizer (DFE) to remove intersymbol interference
- Phase lock loop (PLL) clock recovery
- EC and DFE freeze and reset pins

DESCRIPTION

The AT&T T7260 and T7261 ISDN U-Interface Basic Access Transceiver chip set is a pair of silicon integrated circuits providing full-duplex 2B + D communication on a 2-wire digital subscriber loop. The T7260 and T7261 devices perform line transceiver functions at either the central office (CO) or at the network termination (NT) and operate at a data transfer rate of 144 kb/s. Adaptive echo cancellation and equalization techniques provide a line loss budget of over 40 dB along with good tolerance to bridged taps allowing extended coverage of nonloaded loops. The T7260 device requires both a 5 V and −5 V supply. The T7261 device requires only a 5 V supply. Both are manufactured in CMOS technology and are packaged in 44-pin plastic leaded chip carriers (PLCC).

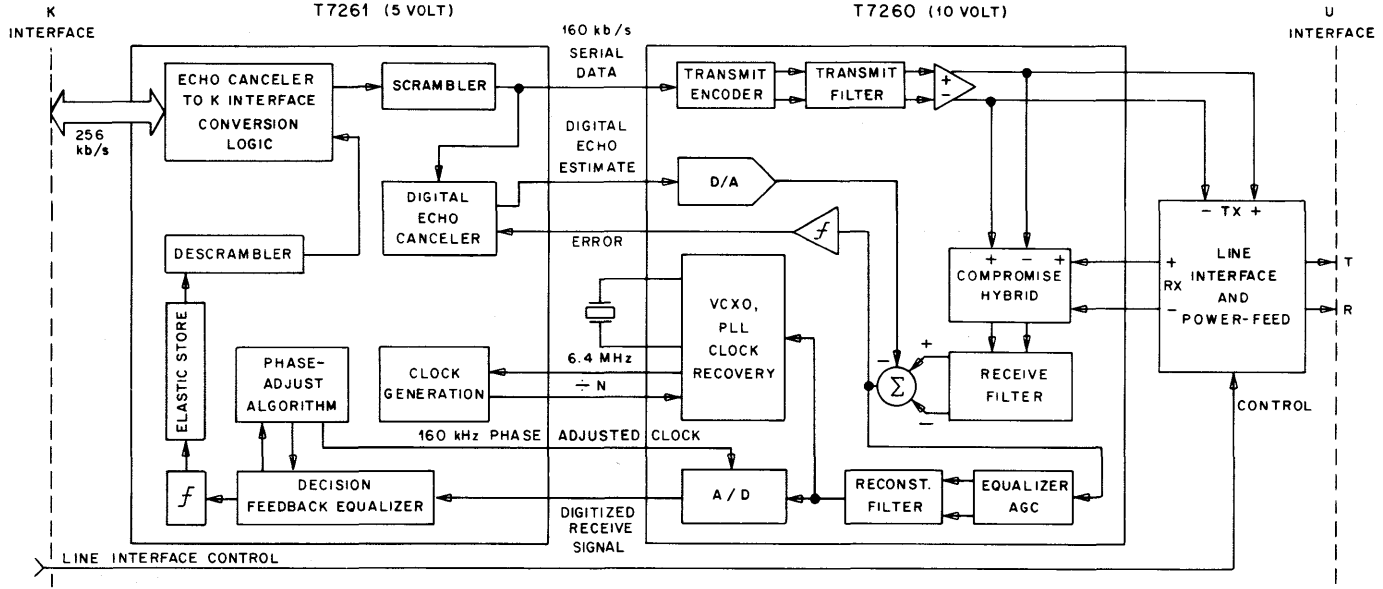


Figure 1. T7260/T7261 ISDN U-Interface Basic Access Transceiver Chip Set Block Diagram

The information contained herein is preliminary and subject to change.

FEATURES

- Pin-programmable for 1 MHz to 50 MHz operation
- Optical and wire applications
- Single 5 V supply

DESCRIPTION

The T7032 Clock Recovery Circuit integrated circuit operates over a 1 MHz to 50 MHz frequency range and provides clock recovery, data retiming, and a polynomial-based descrambler. The descrambler may be disabled for those applications where no data scrambler is used. This device accepts TTL data from a receiver (optical or electrical), recovers the clock, and retimes the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuit requires a single 5 V supply. The T7032 Clock Recovery Circuit is manufactured using CMOS technology and it is available in a 300 mil, 20-pin plastic DIP. It was developed for use with the *ODL* 50 Lightwave Data Link, but it may also be used for general-purpose clock recovery and retiming in other systems.

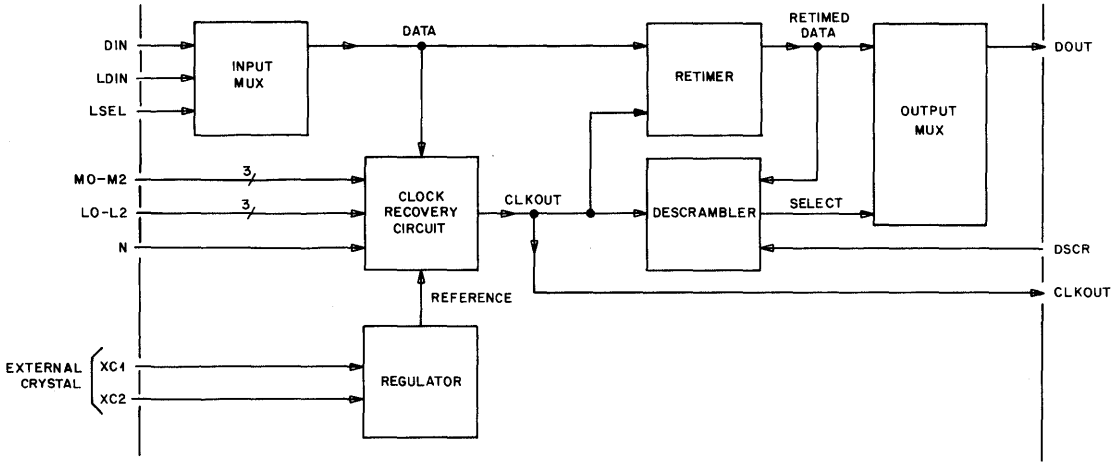
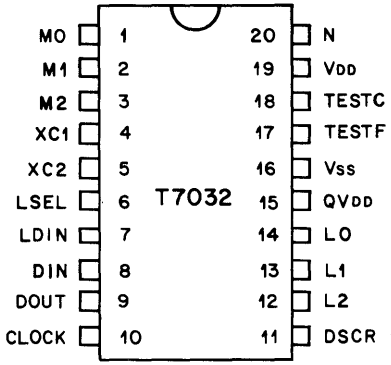


Figure 1. T7032 Clock Recovery Circuit Block Diagram

USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin
CLOCK	10	M1	2
DIN	8	M2	3
DOUT	9	N	20
DSCR	11	QVDD	15
L0	14	TESTC	18
L1	13	TESTF	17
L2	12	VDD	19
LDIN	7	VSS	16
LSEL	6	XC1	4
M0	1	XC2	5

Figure 2. T7032 Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. T7032 Pin Descriptions

Pin	Symbol	Type	Name/Function
1 2 3	M0 M1 M2	I	**Frequency Selects.** M0—M2.*
4,5	XC1, XC2	I	**XTAL1 and XTAL 2.** Connect a 3.579545 MHz crystal between these pins.
6	LSEL	I	**Alternate Data Select.** Tie to 0 V to select data on DIN (pin 8); tie to 5 V for data on LDIN (pin 7).
7	LDIN	I	**Alternate Data In.**
8	DIN	I	**Data In.**
9	DOUT	O	**Data Out.** Descrambled serial data output.
10	CLKOUT	O	**Clock Out.**
11	DSCR	I	**Descrambler.** Tie to 0 V for normal data; tie to 5 V for descrambled data.
12 13 14	L2 L1 L0	I	**Frequency Selects.** L0—L2.*

*Frequency select pins set operating frequency range of circuit. See Table 2 for frequency selection.

Table 1. T7032 Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
15	QVDD	—	**Quiet VDD 5 V Supply.** Extra care may be required when filtering this voltage.
16	VSS	—	**Ground.** 0 V.
17	TESTF	I	**Test F Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
18	TESTC	I	**Test C Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
19	VDD	—	**5 V Supply.**
20	N	I	**Frequency Select.***

Note: A circuit board ground plane is required for optimum performance.
*Frequency select pins set operating frequency range of circuit. See Table 2 for frequency selection.

Overview

The on-chip clock recovery circuit consists of a digital-frequency-lock loop and a phase-lock loop which extract the clock from the positive-going edges of the input data. This recovered clock is used with the input data in the retimer section to synchronize the output data (DOUT) with the positive edge of the clock output (CLKOUT). As a pin-selectable option (DSCR), the retimed data can be fed to a seven-stage descrambler and the descrambled data appears at DOUT (pin 9).

To insure accurate frequency selection, the T7032 Clock Recovery Circuit uses an external 3.58 MHz crystal in its oscillator reference section. The operating frequency of the device is then determined by seven frequency select pins on the circuit which are made high (5 V) or low (0 V). (See Table 2.) Special care is required for filtering the 5 V supply VDD on pin 15 (QVDD) since voltage variations on this pin may cause excessive jitter on the clock and data outputs.

DIN and LDIN are equivalent inputs when selected. LDIN can be selected for the data loopback mode of system operation. For normal operation, TESTC (pin 18) and TESTF (pin 17) must be tied to 5 V. These pins are used only for testing during manufacture.

There are six octave selections that can be chosen from the frequency band selections in Table 2. Nine frequency bands can be selected from each octave. For optimal performance, a frequency of operation that is within the bands set by the seven frequency select pins must be selected.

Noise Properties

Noisy data under worst-case conditions produces a small eye opening and a large amount of phase jitter on the data input. Under these conditions, the T7032 Clock Recovery Circuit recovers the average clock and retimes the data with reduced jitter. Figures 3 and 4 illustrate the improvement of data quality through the circuit. At the limit of sensitivity, the clock recovery circuit imposes a typical noise penalty (noise factor) of <1 dB.

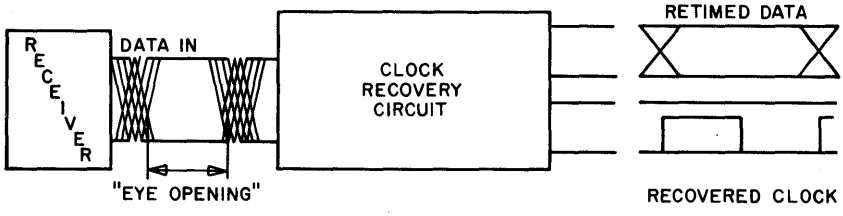


Figure 3. Clock Recovery With Noisy Data

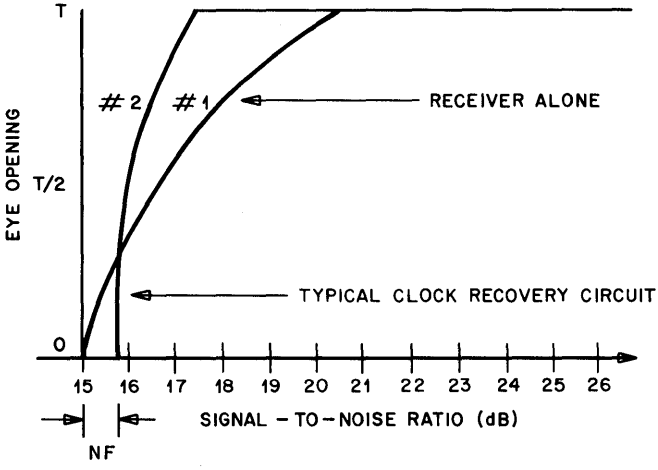


Figure 4. Eye-Opening Versus Signal-to-Noise Ratio

Table 2. Frequency Band Selections (MHz)								
							Frequency	
M2	M1	M0	L2	L1	L0	N	Min	Max
Octave 6								
0	0	0	0	0	0	1	46.3626	51.2715
0	0	0	0	0	1	0	41.9403	46.3626
0	0	0	0	0	1	1	38.5908	41.9403
0	0	0	0	1	0	0	35.4895	38.5908
0	0	0	0	1	0	1	33.0611	35.4895
0	0	0	0	1	1	0	30.7495	33.0611
0	0	0	0	1	1	1	28.9096	30.7495
0	0	0	1	0	0	0	27.1293	28.9096
0	0	0	1	0	0	1	24.8300	27.1293
Octave 5								
0	0	1	0	0	0	1	23.1720	25.6254
0	0	1	0	0	1	0	20.9617	23.1720
0	0	1	0	0	1	1	19.2876	20.9617
0	0	1	0	1	0	0	17.7376	19.2876
0	0	1	0	1	0	1	16.5239	17.7376
0	0	1	0	1	1	0	15.3685	16.5239
0	0	1	0	1	1	1	14.4490	15.3685
0	0	1	1	0	0	0	13.5592	14.4490
0	0	1	1	0	0	1	12.4100	13.5592
Octave 4								
0	1	0	0	0	0	1	11.5766	12.8024
0	1	0	0	0	1	0	10.4724	11.5766
0	1	0	0	0	1	1	9.6360	10.4724
0	1	0	0	1	0	0	8.8617	9.6360
0	1	0	0	1	0	1	8.2553	8.8617
0	1	0	0	1	1	0	7.6781	8.2553
0	1	0	0	1	1	1	7.2187	7.6781
0	1	0	1	0	0	0	6.7741	7.2187
0	1	0	1	0	0	1	6.2000	6.7741
Octave 3								
0	1	1	0	0	0	1	5.7883	6.4012
0	1	1	0	0	1	0	5.2362	5.7883
0	1	1	0	0	1	1	4.8180	5.2362
0	1	1	0	1	0	0	4.4308	4.8180
0	1	1	0	1	0	1	4.1276	4.4308
0	1	1	0	1	1	0	3.8390	4.1276
0	1	1	0	1	1	1	3.6093	3.8390
0	1	1	1	0	0	0	3.3871	3.6093
0	1	1	1	0	0	1	3.1000	3.3871

Table 2. Frequency Band Selections (MHz) (Continued)								
							Frequency	
M2	M1	M0	L2	L1	L0	N	Min	Max
Octave 2								
1	0	0	0	0	0	1	2.8942	3.2006
1	0	0	0	0	1	0	2.6181	2.8942
1	0	0	0	0	1	1	2.4090	2.6181
1	0	0	0	1	0	0	2.2154	2.4090
1	0	0	0	1	0	1	2.0638	2.2154
1	0	0	0	1	1	0	1.9195	2.0638
1	0	0	0	1	1	1	1.8047	1.9195
1	0	0	1	0	0	0	1.6935	1.8047
1	0	0	1	0	0	1	1.5500	1.6935
Octave 1								
1	0	1	0	0	0	1	1.4564	1.6106
1	0	1	0	0	1	0	1.3175	1.4564
1	0	1	0	0	1	1	1.2123	1.3175
1	0	1	0	1	0	0	1.1149	1.2123
1	0	1	0	1	0	1	1.0386	1.1149
1	0	1	0	1	1	0	0.9660	1.0386
1	0	1	0	1	1	1	0.9082	0.9660
1	0	1	1	0	0	0	0.8522	0.9082
1	0	1	1	0	0	1	0.7800	0.8522

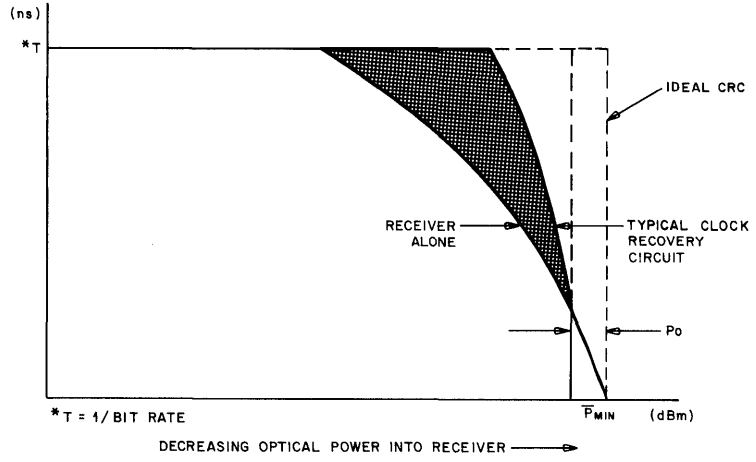
CHARACTERISTICS

A circuit board ground plane is required for optimum performance.

Optical Parameters

Operating Temperature, T_A = 0 to 70 °C

Parameter	Symbol	Min	Max	Unit
Optical Power Penalty				
50 Mb/s and 10^{-9} BER	P_O	—	1	dB
Clock Output rms Jitter				
$2^7 - 1$ Pseudo-Random Word	°rms	—	5.5	°rms
$2^{23} - 1$ Pseudo-Random Word	°rms	—	11.5	°rms



Note: The optical parameters shown are based on *ODL* 50 Lightwave Data Link characteristics.

Figure 5. Eye Width vs. Average Incident Optical Power

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter		Symbol	Min	Max	Unit
Output Voltage	I_{OL} = 4 mA	V_{OL}	–	0.4	V
	I_{OH} = −0.4 mA	V_{OH}	2.4	–	V
Output Current	High	I_{OS}	−25	–	mA
Power Supply Current Drain		I_{DD}	–	60	mA
Input Voltages	Low	V_{IL}	–	0.8	V
DIN, LDIN, LSEL	High	V_{IH}	2.0	–	V
All Other Inputs	Low	V_{IL}	–	0.5	V
	High	V_{IH}	4.5	–	V
Noise Factor*		NF	–	1	dB

*See Figure 4.

Maximum Ratings

DC Supply Voltage (V_{DD}) 6V
Short-Circuit Output Current (I_{OS}) ..... 100 mA
Power Dissipation (PD) ..... 0.5 W
Storage Temperture Range (Tstg) ..... −40 to +125 °C
Lead Soldering Temperature and Time ..... 240 °C/10s

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temepratures up to 300°C.

External Reference Crystal Requirements

Frequency: 3.579545 MHz ± 0.05%, 0 to 70 °C
Series Resistance: 150 Ω
Calibrated at 16 pF series capacitance.

Timing Characteristics

Parameter	Min	Max	Unit
Data Input Risetime	–	5	ns
Data Output Transition*	–	5	ns
Data Output Jitter**	0	7	°rms
Clock Skew (Relative to Data Output)	−3	0	ns

*Transition time is in terms of 10% and 90% values.
**Jitter is in terms of the 50% value for 1010... data input.

Timing Diagram

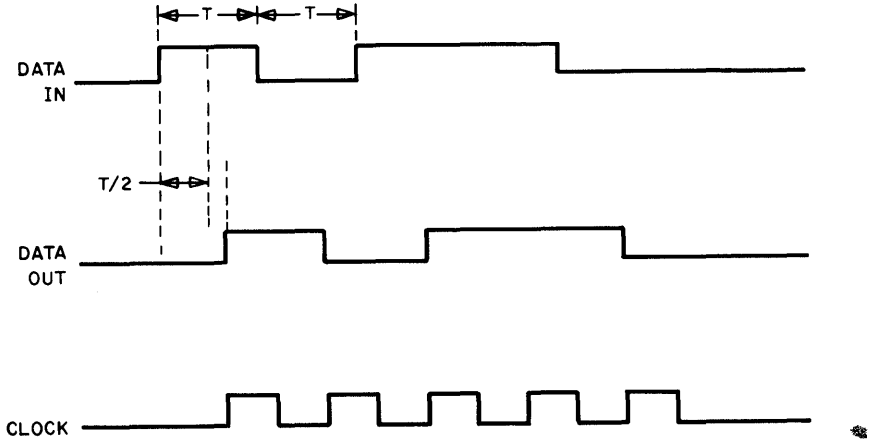


Figure 6. Timing Waveforms

The following are abstracts of available application and technical notes. To receive a copy of any note described in these abstracts, contact your AT&T Account Manager or call:

1-800-372-2447

AN-13 RS-232C COMPATIBLE DATA ENCRYPTION UNIT (AP86-36 SMOS)*

The AN-13 application note describes the design and operation of a low-cost, RS-232C compatible, data encryption unit (DEU) used to encrypt or decrypt digital data. The design of the DEU is based on the AT&T T7000A Digital Encryption Processor (DEP) and the AT&T T7001 Random Number Generator (RNG).

Many advanced electronic communication systems use an unprotected public medium as the communication link between users. These systems are easy to access and can be broken into by an unauthorized user for the purpose of eavesdropping or tampering with the data being sent on the line. The main function of the DEU is to provide secure data communication over a nonsecured public communications link. This is accomplished by encrypting the data before transmission.

The National Bureau of Standards has defined a format for encryption called the Data Encryption Standard (DES). Communication systems that use the DES provide a reasonably high level of security. The T7000A DEP is a high-speed hardware implementation of the DES. In addition to implementing the four DES modes, this programmable device allows multiple or multiplexed ciphering, or the user may program his own unique encryption method. The T7001 RNG generates a truly random (not pseudorandom) output which can be used as encryption keys or initial values.

Overview of both the T7000A and T7001 devices are presented and a description of the DEU and its operation is provided in detail. The AN-13 application note appendices contain all the information needed to construct this project.

AN-15 CONFIGURING THE T7100 X.25 PROTOCOL CONTROLLER (XPC-8) (AP86-33 SMOS)*

The T7100A integrated circuit is an X.25 level 2 Protocol Controller (XPC-8). It implements the balanced link access procedure (LAPB) for data interchange over a synchronous full duplex link as defined in X.25. The XPC-8 is in compliance with CCITT X.25 1980 and ISO 7776 (at the draft international standard [DIS] level). The protocol controller is byte oriented with a maximum transmit and receive data rate of 250 kb/s.

The XPC-8 is configured for a specific X.25 application by writing appropriate values for the system parameters into the parameter registers when the XPC-8 is in a setup state.

The AN-15 application note contains information needed to perform the initialization of the XPC-8. It describes the architecture of the device, different operating modes, major features, and typical initialization code in C language.

*Document identification number.

AN-16 POLLED AND INTERRUPT MODE OPERATIONS OF THE T7111 SYNCHRONOUS PACKET DATA FORMATER (AP86-34 SMOS)*

The AT&T T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines using high-level data link control (HDLC) bit-synchronous protocol with 8-bit microprocessor or microcontroller systems. The ANT is a single channel, full duplex, packet data formatter. It has a programmable register set to configure both host and serial link interfaces.

The AN-16 application note contains information to utilize the ANT in a variety of system environments. It describes the major features, architecture of the device, and the operation and typical system applications of the T7111 ANT when used in the polled and interrupt modes.

AN-17 USING THE AT&T T7010 SWITCHED CAPACITOR MODEM AND T7011 MODEM INTERFACE CHIP (AP86-37 SMOS)*

The AT&T T7010 Switched Capacitor Modem (SCM) integrated circuit is a full-duplex data modem. The SCM is a general-purpose modem for use in stand-alone intelligent data sets or for use in data terminals that interface directly with telephone lines. Designed for low microprocessor overhead, this microprocessor peripheral can be used to transmit full-duplex data on 2-wire switched voice telephone lines and on point-to-point circuits. The SCM supports a variety of transmission standards including 0—300 b/s frequency shift keying (FSK) for AT&T Standard 103, and 1200 b/s differential phase shift keying (DPSK) for AT&T Standard 212A and CCITT V.22. Transmit and filtering functions compatible with 2400 b/s CCITT V.22 bis are included. It is available in a dual-cavity 40-pin ceramic DIP.

The AT&T T7011 Modem Interface Chip (MIC) is recommended as a companion to the T7010 SCM. The MIC is a microprocessor peripheral providing the interconnection required between the SCM and a telephone line. A single T7011 MIC using both analog and digital circuitry, implements several peripheral functions that would otherwise require several ICs. Examples of these functions are two- to four-wire conversion (hybrid), dual-tone multifrequency (DTMF) signaling, call progress tone detection and automatic gain control (AGC) controlled speaker output for aural monitoring of call progress. The MIC has a microprocessor interface that is used to control and monitor the MIC's operation. It is available in a 24-pin plastic DIP.

The AN-17 application note contains information needed to program the SCM for designing a standard modem or a complex modem that will fit many applications. It describes the architecture, major features, different operating modes, and describes how the host processor can customize the handshaking and communications to a particular application.

AN-18 DMA MODE OPERATION OF THE T7111 SYNCHRONOUS PACKET DATA FORMATTER (AP86-46 SMOS)*

The AT&T T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines using high-level data link control (HDLC) bit-synchronous protocol with 8-bit microprocessor or microcontroller systems. The ANT is a single channel, full duplex, packet data formatter. It has a programmable register set to configure both host and serial link interfaces.

The AN-18 application note contains information to utilize the ANT in a variety of system environments. It describes the major features, architecture of the device, and the operation and typical system applications of the T7111 ANT when used with a 8237 or 8257 DMA Controller.

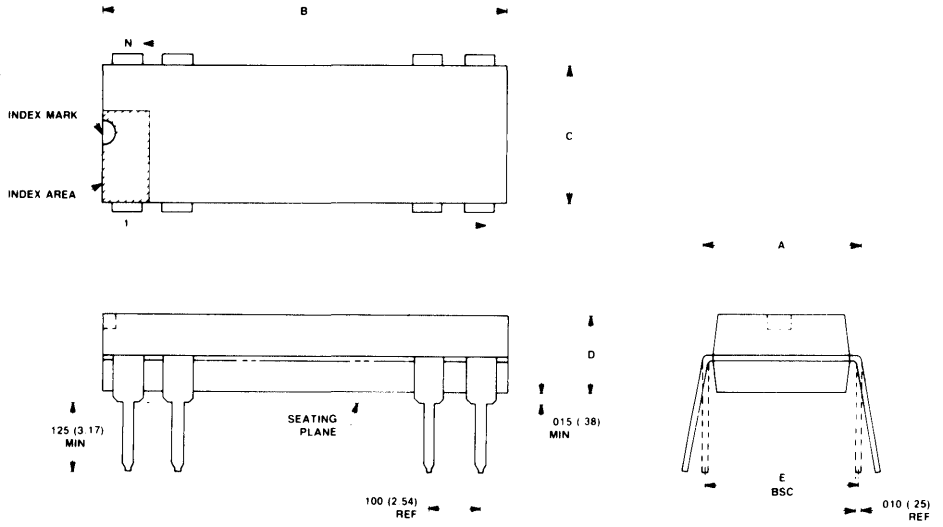
INTERFACING THE T7110 SPYDER-S TO A DS1 SIGNAL (TN86-095 SMOS)*

The interfacing of the T7110 SPYDER-S with Serial Interface to a DS1 Signal technical note discusses guidelines for interfacing the AT&T T7110 Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S) to a T1/DS1 line at a 1,544 Mb/s serial data rate. Such an interface would be required in a digital multiplexed interface (DMI) application or in an ISDN primary rate user-network interface.

Table 1. Communication Devices by Device Number			
Device	**Name**	**Package**	**Figure**
T7000A-PC	Digital Encryption Processor	40-Pin Plastic DIP	1
T7001-PC	Random Number Generator	32-Pin Plastic DIP	1
T7010-BC	Switched Capacitor Modem	40-Pin Ceramic Nonhermetic (Dual Cavity) DIP	4
T7011-PC	Modem Interface Chip	24-Pin Plastic DIP	1
T7018-MC	Modem Analog Controller	68-Pin Plastic Leaded Chip Carrier	6
T7019-EC	Analog Companion Chip	28-Pin Small-Outline Package (SOJ Configuration)	3
T7019-PC		28-Pin Plastic DIP	1
T7032-PC	Clock Recovery Circuit	20-Pin Plastic DIP	1
T7100A-BC	X.25 Protocol Controller	48-Pin Ceramic DIP	2
T7102-NE	X.25/X.75 Protocol Controller	70-Pin Ceramic Pin Grid Array	7
T7110-MC	Synchronous Protocol Data Formatter with Serial Interface (SPYDER)	68-Pin Plastic Leaded Chip Carrier	
T7111-EC	Synchronous Packet Data Formatter (ANT)	28-Pin Small-Outline Package (SOJ Configuration)	3
T7111-PC		28-Pin Plastic DIP	1
T7112-EC	Asynchronous Receive/ Transmit Interface (ARTI)	28-Pin Small-Outline Package (SOJ Configuration)	3
T7112-PC		24-Pin Plastic DIP	1
T7113-EC	CRC Checker	28-Pin Small-Outline Package (SOJ Configuration)	3
T7113-PC		28-Pin Plastic DIP	1
T7250A-MC	User Network Interface for Terminal Equipment (UNITE)	44-Pin Plastic Leaded Chip Carrier	5
T7250A-PC		40-Pin Plastic DIP	1
T7252-MC	ISDN Basic Access User Network Interface Termination for Switches (UNITS)	44-Pin Plastic Leaded Chip Carrier	5
T7252-PC		40-Pin Plastic DIP	1
T7260-MC	U-interface Basic Access Transceiver Chip Set (Analog)	44-Pin Plastic Leaded Chip Carrier	5
T7261-MC	U-interface Basic Access Transceiver Chip Set (Digital)	44-Pin Plastic Leaded Chip Carrier	5

Table 1. Communication Devices by Device Number (Continued)			
Device	**Name**	**Package**	**Figure**
T7500-EC	PCM Codec with Filters	20-Pin Small-Outline Package (SOJ Configuration)	3
T7500-PC		18-Pin Plastic DIP	1
T7501-EC	PCM Codec with Filters	20-Pin Small Outline Package (SOJ Configuration)	3
T7501-PC		18-Pin Plastic DIP	1
T7513-EC	PCM Codec with Filters	20-Pin Small-Outline Package (SOJ Configuration)	3
T7513-PC		20-Pin Plastic DIP	1
T7520-CC	High Precision PCM Codec with Filters	24-Pin Ceramic DIP	2
T7521-CC	High Precision PCM Codec with Filters	24-Pin Ceramic DIP	2
T7522-CC	High Precision PCM Codec with Filters	24-Pin Ceramic DIP	2

Table 2. Communication Devices by Number of Pins			
Pins	**Package**	**Device**	**Figure**
18	Plastic DIP	T7500-PC, T7501-PC	1
20	Plastic DIP	T7032-PC, T7513-PC	1
	Small-Outline SOJ	T7513-EC, T7500-EC, T7501-EC	3
24	Plastic DIP	T7011-PC, T7112-PC	1
	Ceramic DIP	T7520-CC, T7521-CC, T7522-CC	2
28	Plastic DIP	T7111-PC	1
	Small-Outline SOJ	T7111-EC, T7112-EC	3
40	Plastic DIP	T7000A-PC, T7250A-PC	1
	Ceramic (Dual-Cavity)	T7010-BC	4
44	Plastic Leaded Chip Carrier	T7250A-MC, T7252-MC, T7260-MC, T7261-MC	5
48	Ceramic DIP	T7100A-BC	2
68	Plastic Leaded Chip Carrier	T7110-MC	6
70	Ceramic Pin Grid Array	T7102-NC	7



Note: Dimensions are in inches and (millimeters).

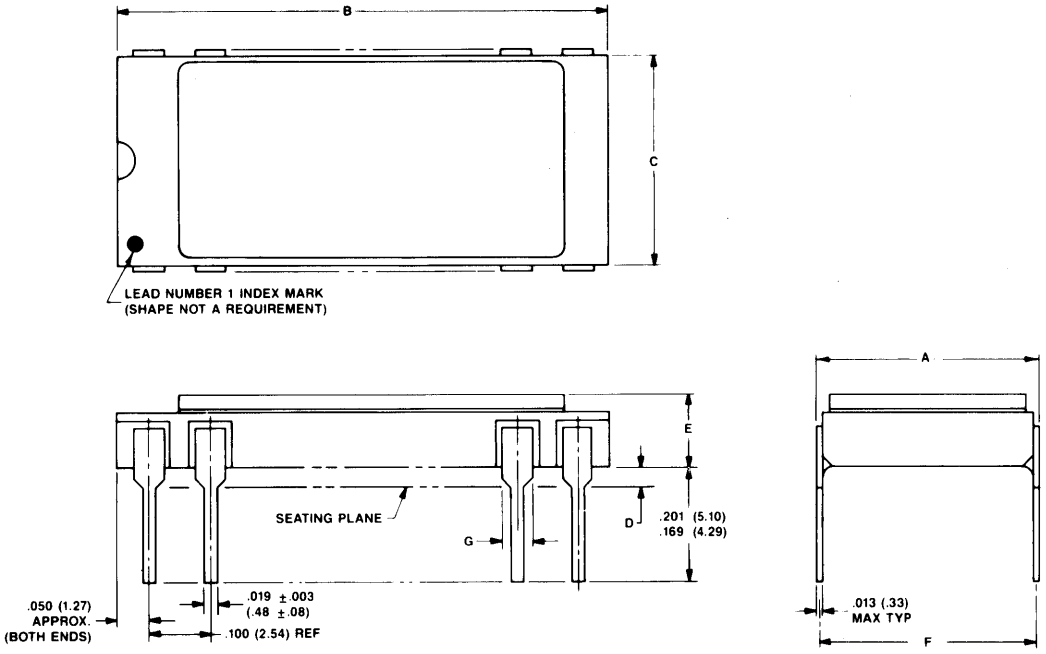
Figure 1. Postmolded Plastic DIPs

Table 3. Postmolded Plastic DIP Dimensions*

No. Pins	A Max	B Max	C Max	D Max	E BSC	F Max	Notes
18	.320 (8.13)	.920 (23.37)	.255 (6.48)	.145 (3.68)	.300 (7.62)	.400 (10.16)	1, 2, 3
20	.320 (8.13)	1.040 (26.42)	.255 (6.48)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1, 2, 3
24	.615 (15.62)	1.270 (32.26)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3
28	.615 (15.62)	1.470 (37.34)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3
40	.615 (15.62)	2.070 (52.58)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3

*Dimensions are in inches and (millimeters).

Notes:
1. Meets JEDEC standards.
2. Index mark may be semicircular notch or a circular dimple located in index area.
3. Actual dimensions may vary depending on location of assembly, but all meet limits shown in table.
4. Package does not have a JEDEC-approved pin-out.



Note: Dimensions are in inches and (millimeters).

Figure 2. Ceramic DIP – Cavity Up (Facing Away From Printed Wiring Boards)

Table 4. Ceramic DIP Dimensions*

No. Pins	A Max	B Max	C Nom	D Approx	E Max	F Nom	G Min
24**	.620 (15.75)	1.212 (30.78)	.590 (14.99)	.050 (1.27)	.135 (3.43)	.600 (15.24)	.040 (1.02)
48	.620 (15.75)	2.420 (61.47)	.590 (14.99)	.050 (1.27)	.135 (3.43)	.600 (15.24)	.040 (1.02)

Note: Maximum chip size is for chip with pads on two sides.
*Dimensions are in inches and (millimeters).
**Caution: For T7520, T7521, and T7522 Codecs, the cavity cover is internally connected to AGND.

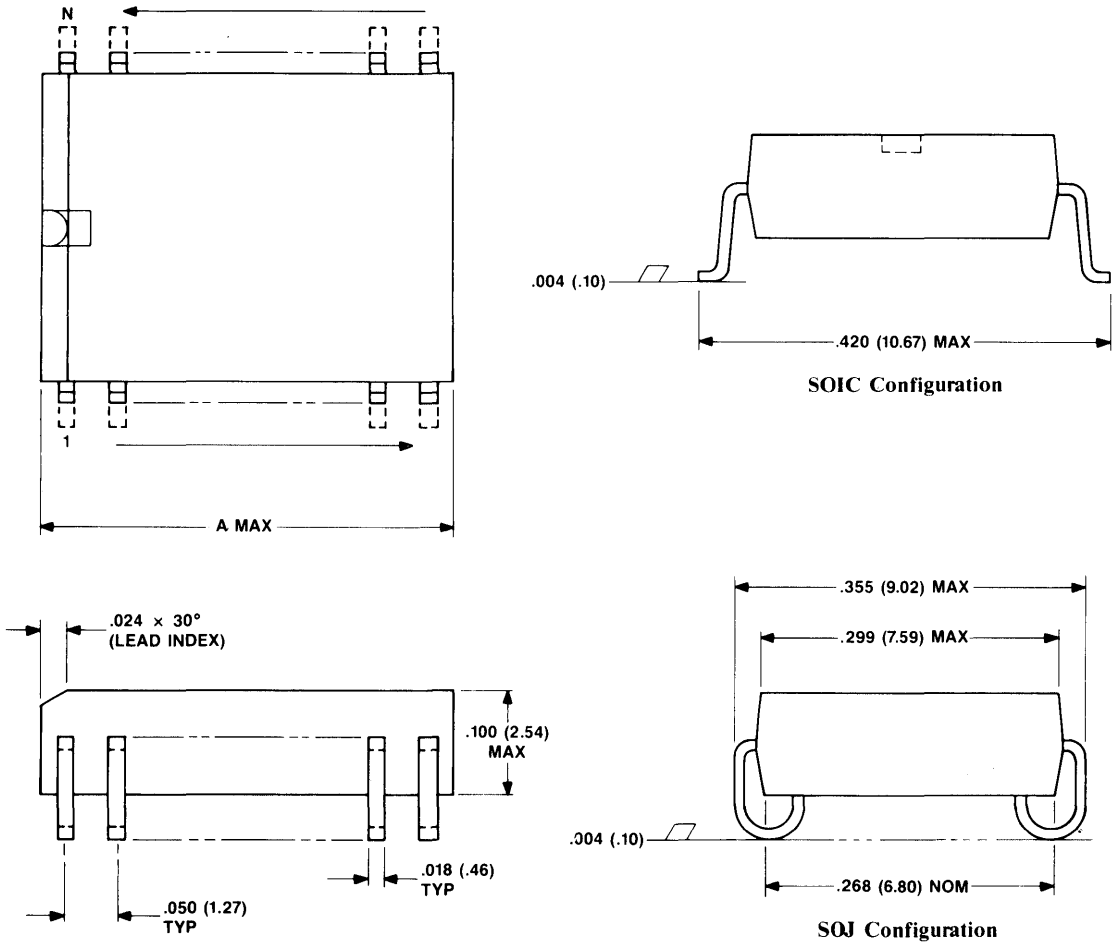


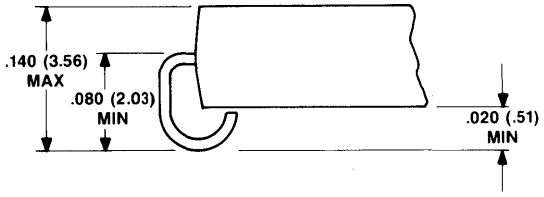
Figure 3a. Plastic Small-Outline Package

Small Outline Package Dimensions

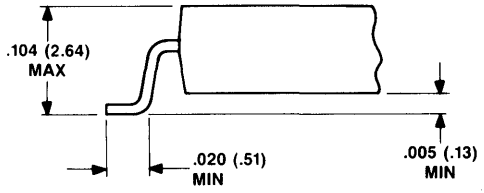
No. Leads	A Max	Lead Configuration*	Max Chip Size L x W
20	.508 (12.90	$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	.340 (8.64) × .190 (4.83)
28	.708 (17.98)	$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	.350 (8.879) × .190 (4.83)

*Package may be provided in any of the indicated lead configurations dependent on location of assembly.

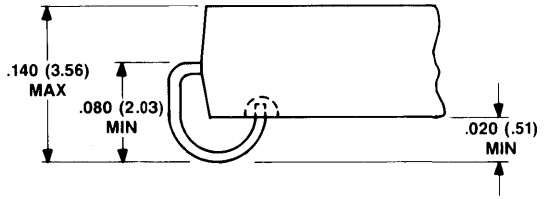
Notes:
$\overline{C}$, $\overline{D}$ meet JEDEC registered outline TMS 013.
Index mark may be a notch, dimple, or bevel located in zone identified on outline.
Actual dimensions may vary depending on location of assembly but all dimensions meet limits shown in table.
Dimensions are in inches and (millimeters).



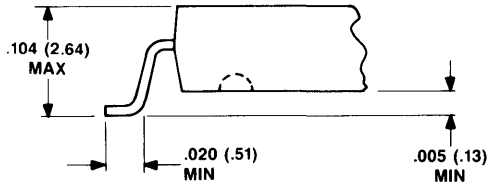
A. Detail SOJ



C. Detail SOIC



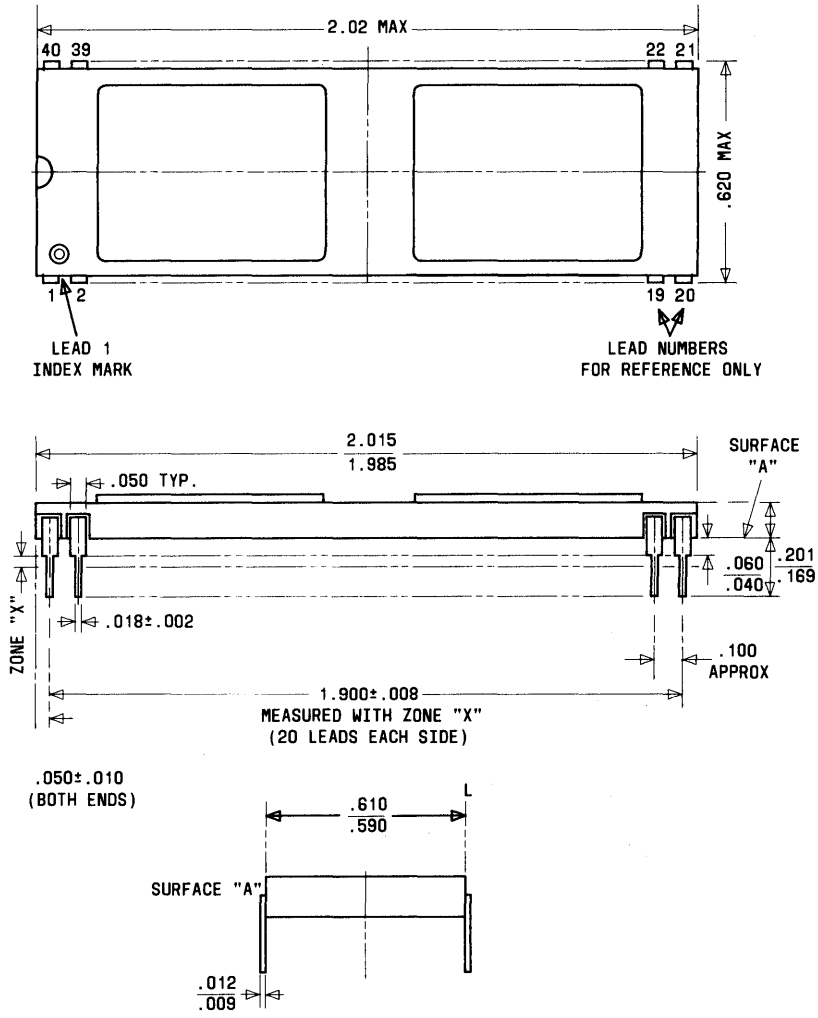
B. Detail SOJ



D. Detail SOIC

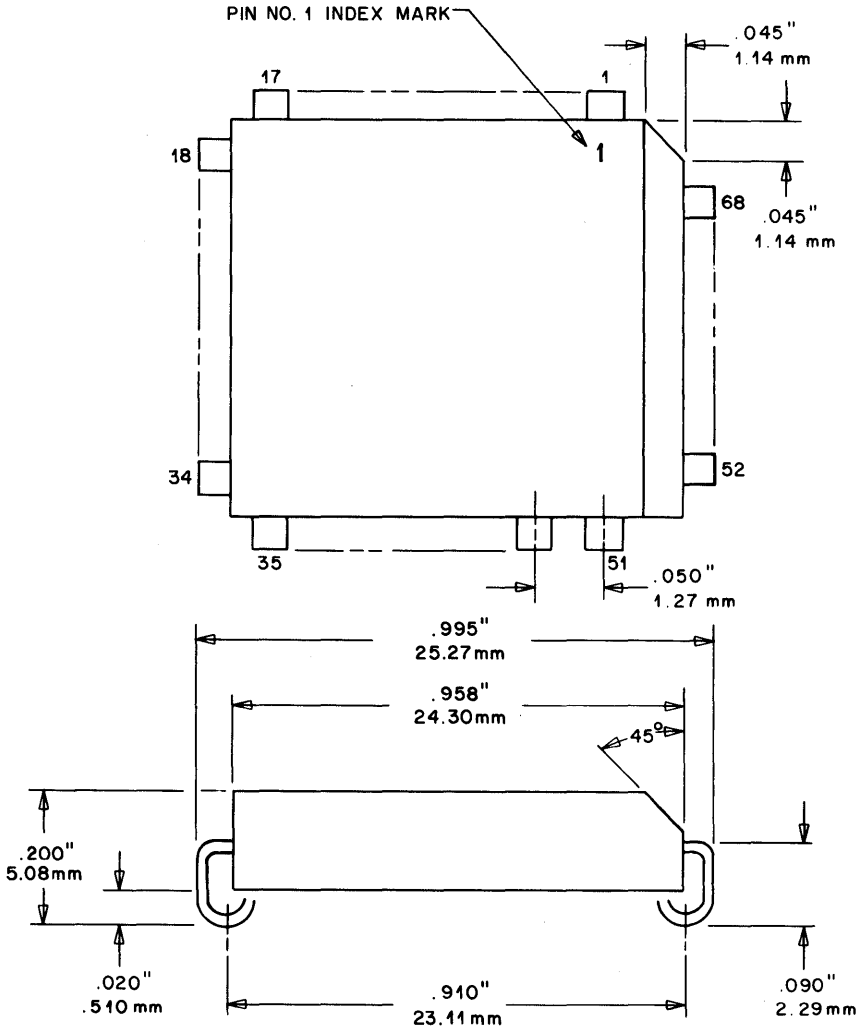
Note: Dimensions are in inches.

Figure 3b. Plastic Small-Outline Lead Configuration Packages



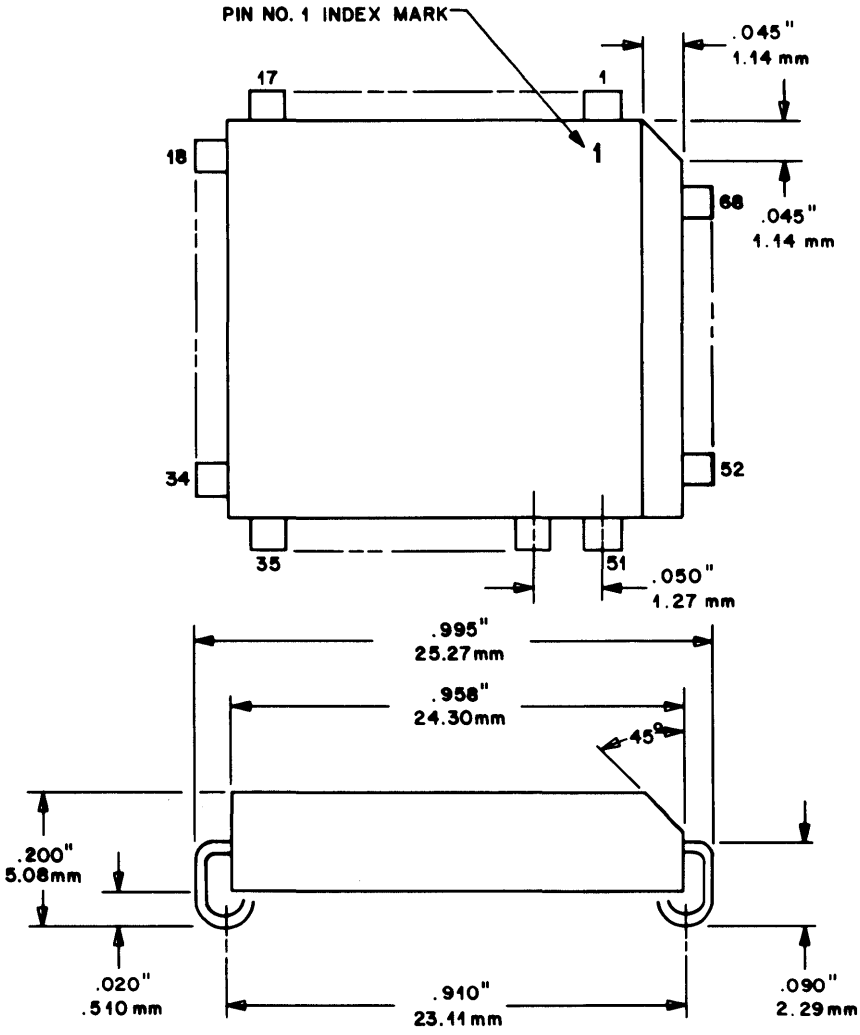
Note: Dimensions are in inches.

Figure 4. 40-Pin Ceramic Dual Cavity DIP



Notes:
1. All meet JEDEC standards.
2. Pin 1 index mark may be a dimple or numeric located in zone indicated.
3. Dimensions are in inches and (millimeters).

Figure 5. 44-Pin Plastic Leaded Chip Carrier



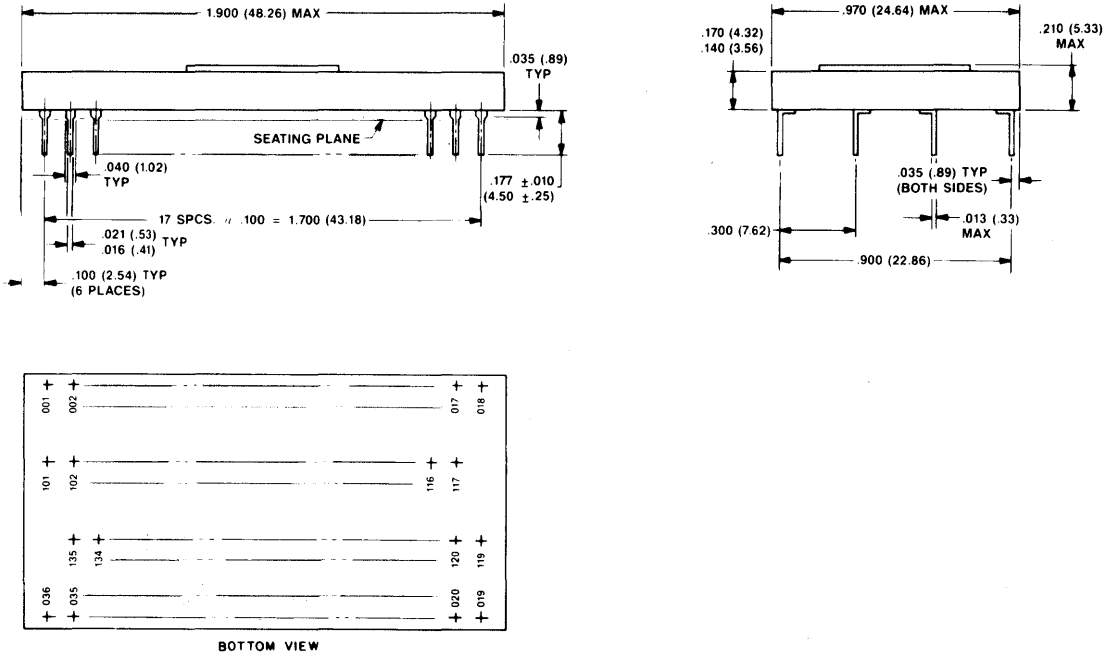
NOTES:

ALL MEET JEDEC STANDARDS.

PIN 1 INDEX MARK MAY BE A DIMPLE OR NUMERIC. LOCATED IN ZONES INDICATED.

DIMENSIONS ARE IN INCHES AND MILLIMETERS.

Figure 6. 68-Pin Plastic Leaded Chip Carrier



Note: Dimensions are in inches and (millimeters).

Figure 7. 70-Pin Ceramic PGA Package – Cavity Up (Facing Away From Printed Wiring Board)

The device numbers required for ordering are given below. To order devices, or to obtain additional information, please contact your AT&T Account Manager or call **1-800-372-2447.**

Table 1. Communication Devices Ordering Identification

Device	Name	Package
T7000A-PC	Digital Encryption Processor	40-Pin Plastic DIP
T7001-PC	Random Number Generator	32-Pin Plastic DIP
T7010-BC	Switched Capacitor Modem	40-Pin Ceramic Nonhermetic (Dual Cavity) DIP
T7011-PC	Modem Interface Chip	24-Pin Plastic DIP
T7018-MC	Modem Analog Controller	68-Pin Plastic Leaded Chip Carrier
T7019-EC	Analog Companion Chip	28-Pin Small-Outline Package (SOJ Configuration)
T7019-PC		28-Pin Plastic DIP
T7032-PC	Clock Recovery Circuit	20-Pin Plastic DIP
T7100A-BC	X.25 Protocol Controller	48-Pin Ceramic DIP
T7102-NC	X.25/X.75 Protocol Controller	70-Pin Ceramic Pin Grid Array
T7110-MC	Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S)	68-Pin Plastic Leaded Chip Carrier
T7111-EC	Synchronous Packet Data Formatter (ANT)	28-Pin Small-Outline Package (SOJ Configuration)
T7111-PC		28-Pin Plastic DIP
T7112-EC	Asynchronous Receive/ Transmit Interface (ARTI)	28-Pin Small-Outline Package (SOJ Configuration)
T7112-PC		24-Pin Plastic DIP
T7250A-MC	User Network Interface for Terminal Equipment (UNITE)	44-Pin Plastic Leaded Chip Carrier
T7250A-PC		44-Pin Plastic DIP
T7252-MC	ISDN Basic Access User Network Interface Termination for Switches (UNITS)	44-Pin Plastic Leaded Chip Carrier
T7252-PC		44-Pin Plastic DIP
T7260-MC	U-interface Basic Access Transceiver Chip (Analog)	44-Pin Plastic Leaded Chip Carrier
T7261-MC	U-interface Basic Access Transceiver Chip (Digital)	44-Pin Plastic Leaded Chip Carrier

Table 1. Communication Devices Ordering Identification (Continued)		
Device	**Name**	**Package**
T7500-EC	PCM CODEC with Filters	20-Pin Small-Outline Package (SOJ Configuration)
T7500-PC		18-Pin Plastic DIP
T7501-EC	PCM Codec with Filters	20-Pin Small-Outline Package (SOJ Configuration)
T7501-PC		18-Pin Plastic DIP
T7513-EC	PCM CODEC with Filters	20-Pin Small-Outline Package (SOJ Configuration)
T7513-PC		20-Pin Plastic DIP
T7520-CC	High-Precision PCM CODEC with Filters	24-Pin Ceramic DIP
T7521-CC	High-Precision PCM CODEC without Filter	24-Pin Ceramic DIP
T7522-CC	High-Precision PCM CODEC with Filters	24-Pin Ceramic DIP

T-Number Codes

AT&T has implemented a uniform coding matrix for all new or redesigned MOS communication IC products. The codes are based on an industry-compatible coding format that gives a condensed reference to device characteristics. One code is used for all component users, resulting in a simplified and more efficient inventory and ordering system. Examples of the new coding format (condensed form) and its interpretation are shown on Figure 1. A coding matrix key is shown on Figure 2.

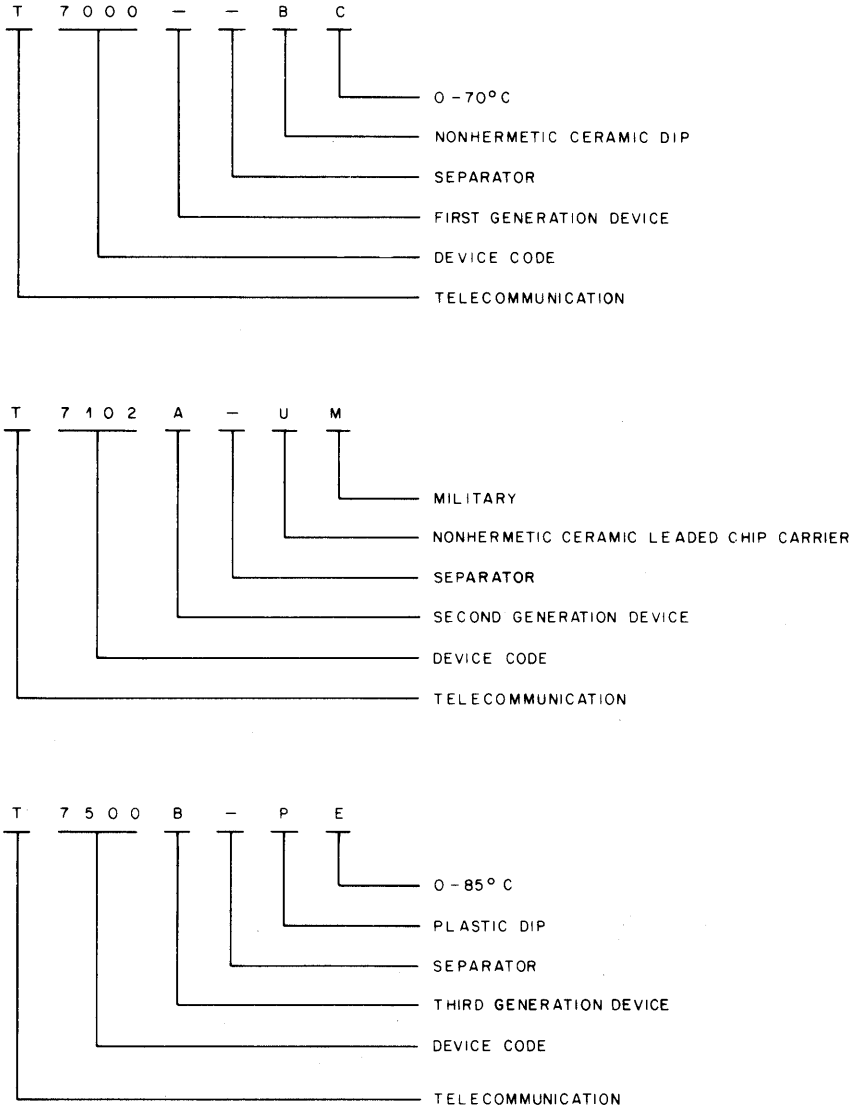


Figure 1. Coding Examples

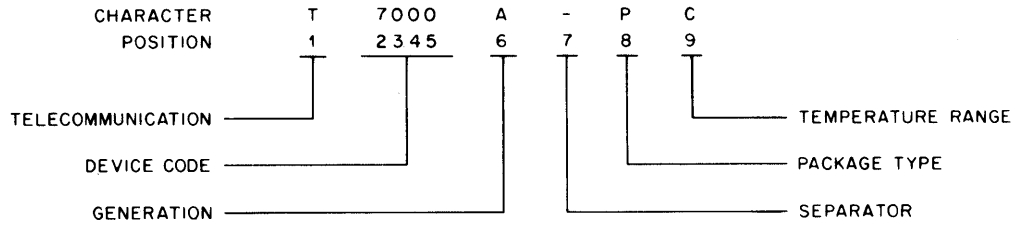


Figure 2. Coding Matrix Key

Position Number	Description	Character/Identification
1	Device	T = Telecommunication
2—5	Device Code	Four digit number identifies device
6	Generation	Dash (-) represents first generation, A—E represent subsequent generations; e.g., A=2nd, B=3rd, etc. A new generation is defined as being pin, function and software compatible with the original device. This device may provide some additional functions, have ac/dc characteristic differences, or have a significant design change.
7	Separator	- (If both positions 6 and 7 are dashes, only one dash is shown.)
8	Package Type	B = Nonhermetic, ceramic DIP C = Hermetic, ceramic DIP E = Small outline G = Dual-cavity, ceramic DIP J = Nonhermetic, leadless chip carrier K = Hermetic, leadless chip carrier L = Hermetic, ceramic, leaded chip carrier M = Plastic, leaded chip carrier N = Nonhermetic, ceramic pin grid array P = Plastic DIP R = Hermetic, ceramic pin grid array T = Plastic, leadless chip carrier U = Nonhermetic, ceramic, leaded chip carrier
9	Temperature Range	C = 0 to 70 °C (commercial) E = 0 to 85 °C (extended) M = Military L = −40 to +85 °C (outside plant/loop)

A/D – Analog to digital.

A/D Converter – A device that converts a continuously varying signal, such as voltage or frequency, to a digital representation suitable for use by digital equipment.

ADPCM – Adaptive differential pulse code modulation.

Algorithm – A defined set of rules and processes used to find a solution to a problem.

ANSI – American National Standards Institute.

Assert – To drive a signal to its active state.

Asynchronous Data Transmission – Data transmission in which there is no predetermined time interval for signal elements.

AT&T – American Telephone & Telegraph Company.

Balance Network – An adjustable impedance used to terminate one port of a hybrid such that the hybrid characteristics approach the ideal when used to provide 2-wire to 4-wire conversion.

Basic Access – Refers to a multiplexed communication link to an ISDN where the link has a channel structure consisting of two B channels for voice or data and one D channel for control. Primarily intended for terminal interfaces.

Baud – A unit of digital signaling rate. The signaling rate in bauds is equal to the reciprocal of the length in seconds of the signal element when all signal elements have equal length. If signal elements are not of equal length, as in start-stop character asynchronous operation, the signaling rate in bauds is expressed as the reciprocal of the length of the shortest signal element.

Bit – An abbreviation for binary digit. A bit can be one of the two binary characters, 1 or 0. A unit of information. One bit of information is sufficient to specify one of two equally likely possibilities.

Bit Stream – The transmission method in which bits are continuously transmitted serially and character separation is accomplished by the terminal equipment.

b/s – Bits per second.

Bridge – An arrangement for establishing and controlling one-way or two-way conference connections among a number of remotely located customers.

Burst – Several events occurring at the same moment in time.

Bus – One or more conductors over which information is carried from any of several sources to any of several destinations.

Byte – A group of eight bits constituting a single entity and a discrete item of information.

CBC – Cipher block chaining.

CC – Cluster Controller.

CCITT – Consultative Committee for International Telephone and Telegraph. See **International Telephone and Telegraph Consultative Committee.**

CEC – Cascadable echo canceler.

Central Office – A switching system that connects lines to lines and lines to trunks. The term is sometimes used to refer to a telephone company building in which a switching system is located and to include other equipment, such as transmission system terminals, that may be located in such a building.

CFB – Cipher feedback.

CFR – See **Conferencer**.

CEPT – Conference of European Post and Telecommunication Administrations.

Channel – A transmission path between two points. The term channel may refer to a one-way path or, when paths in the two directions of transmission are always associated, to a 2-way path. It is usually the smallest subdivision of a transmission system by means of which a single type of communication service is provided; i.e., a voice channel, teletypewriter channel, or data channel.

Chip Carrier – An intermediate form of package used for integrated circuits. It is a leadless package used as a plug-in type of device for mounting LSI chips on circuit boards. Some of its advantages include easing prototyping, design changes, programing and field repairs, and testing. It minimizes chip damage from static charges or leakage current during soldering or handling and lowers inventory costs because chips are easier to store than a whole circuit board.

Circuit Switching – Providing a complete end-to-end path between two terminals for the duration of the communication. The path is connected by switching equipment during the call set-up and maintained for the duration of the communication.

Circuit Switched Digital Capability – The capability of transmitting alternate baseband voice and 56 kb/s digital data using circuit switching facilities.

C-Message Weighting – A curve or filter response that approximates the human ear's response to different frequencies. The curve shows that a tone at 200 Hz is 25dB less disturbing than a 1000 Hz tone of the same power.

CMOS – Complementary metal-oxide semiconductor.

Codec (coder/decoder) – An A/D/A converter that digitally codes and decodes analog signals. A codec is necessary to interface voice-telephone circuits with time-division multiplex systems.

Common Mode Rejection – The ability of a device, usually a differential amplifier, to produce a zero output when a like voltage is applied simultaneously to both differential input terminals.

Compandor – An abbreviation for compressor-expandor. A device used to compress the range of talker volumes at the input to a carrier system (in particular, to increase low-level talker volumes) and to expand the received volumes at the output of the carrier system (to provide the complementary function and to make the transmission system transparent). This technique improves the signal-to-noise ratio for low-level talkers and provides a substantially reduced received noise level during the so-called quiet intervals.

Compression – The use of a logarithmic type of conversion to reduce a signal's dynamic range so that the small signal characteristics are maintained.

Concentrator – A store and forward device which connects a number of low-speed circuits to a smaller group of high-speed circuits for economical transmission.

Conferencer (CFR) – A circuit capable of interconnecting multiple channels into discrete and independent conferences (connections).

Contention – The process of terminal users requesting or bidding to transmit when there is competition for the communication line.

CPU – Central processing unit.

CRC – Cyclic redundancy check.

Crosspoint Array – An arrangement of switching elements used in some switching networks, characterized by incoming and outgoing talking paths arranged at right angles to each other, with switching elements at intersections.

CSDC – See **Circuit Switched Digital Capability**.

CT – Concentrator.

D/A – Digital to analog.

D/A Converter – A device that converts a digital signal into a continuous analog signal.

Data Base – An integrated collection of data that supports multiple applications.

Data Communication – The function of transmitting information from one point to another.

Data Communication Equipment – Equipment used to provide the functions required to establish, maintain, and terminate a connection and provide signal conversion and coding between a user and the common carrier's line.

Datagram – A packet network capability in which a complete message is contained within a packet's data field.

Data Terminal Equipment – Any piece of equipment at which a communication path begins or ends.

dB – Decibel. A dimensionless unit used to express the ratio between input and output voltages, powers, currents, or sound intensities.

dBm – A logarithmic measure of power with respect to a reference power of 1 milliwatt.

dBm0 – Power level in dBm referred to the zero-transmission-level point (OTLP). Used as a reference point in contrast to dBm which is the absolute power level reference point.

dBrnC – A power level in dB relative to a noise reference of −90 dBm, as measured with a noise meter, weighted by a special frequency function called C-message weighting that expresses average subjective reaction to interference as a function of frequency.

DCE – See **Data Communication Equipment**.

DEA – Data encryption algorithm.

DEP – Digital encryption processor.

DES – Data encryption standard.

DEU – Data encryption unit.

DFI – Digital facility interface. The interface between a switching or transmission facility designed specifically to handle digital signals.

Digital Facility Interface – The interface between a switching or transmission facility designed specifically to handle digital signals.

DIP – Dual in-line package.

DIS – Draft international standard.

DMA – Direct memory access. A method for external devices to directly access memory for reads or writes without passing through the CPU. During DMA the CPU is removed from the address and data buses (3-state), control is transferred to the external device, and CPU operation is temporarily suspended. Maximum DMA transfer rate is limited by the speed of the memory devices being used.

DMI – Digital multiplexed interface.

DPRAM – Dual-port random access read/write memory.

Driver – A device used to increase the current drive from its input to a higher value suitable for driving multiple outputs.

Droop – A characteristic of a pulse waveform in which the pulse height falls below its nominal value.

DSX – Digital cross-connect.

DTE – See **Data Terminal Equipment**.

Dual-rail – Two unipolar signals used to represent one bipolar waveform. Each rail corresponds to one side, either positive or negative, of a bipolar signal.

ECB – Electronic code book.

Echo – An attenuated signal derived from a primary signal by reflection at one or more impedance discontinuities and delayed relative to the primary signal.

Echo Canceler – A device that controls echo signals in either direction of a 4-wire circuit by forming a replica of the echo and subtracting it from the returned signal.

EIA RS-422 – The standard interface between data communication equipment and data processing terminal equipment adopted by the Electronic Industries Association (EIA). It has been accepted by most manufacturers of data transmission equipment.

Encoder – A device that produces an output in a desired coded form usually to hide the meaning of the message except to certain individuals who know the enciphering scheme.

Encrypt – To scramble information to prevent understanding of the information by unauthorized personnel.

Electronic Switching System (ESS) – A class of switching systems in which the control functions are performed principally by electronic devices. There are two types currently in use: time-division and space-division.

EMI – Electromagnetic interference/noise.

End Office – A local switching center where loops are terminated for purposes of interconnection to each other and to trunks.

Envelope Delay Distortion – Departure from a constant value of the envelope delay versus frequency characteristic. Envelope delay is the derivative with respect to frequency of the phase characteristic of the transfer function and should not be confused with differential delay, which is the difference in delay at two frequencies.

Equalization – The procedure applied to transmission media or channels to insure that the amplitude and phase (or envelope delay) characteristics of a transmitted signal are preserved at the receiving end of the connection.

Error Rate – A measure of the performance of a digital transmission system. It can be specified as a bit error rate (the probability of error per bit transmitted), as a block error rate (the probability of one or more errors in a specified-length block of bits), or in other forms such as percent error-free seconds.

ESD – Electrostatic discharge.

ESS – Electronic switching system.

Facility – Any one of the elements of the physical telephone system that are needed to provide service. Thus, switching systems, cables, and microwave transmission systems are examples of facilities. Facility is sometimes used in a more restricted sense to mean transmission facility.

Fall Time – The interval of time required for the trailing edge of a pulse to decay from 90 percent to 10 percent of the peak pulse amplitude.

FCC – See **Federal Communications Commission.**

FCS – Frame check sequence.

FDM – See **Frequency Division Multiplexing.**

FDX – See **Full-Duplex Transmission.**

Federal Communications Commission (FCC) – A board of seven commissioners, appointed by the President of the United States of America under the Communications Act of 1934, having the power to regulate interstate and foreign communications originating in the United States by wire and radio.

Feeder Cable – A loop cable emanating from a central office and usually placed in an underground conduit system with access available at periodically placed manholes.

FEP – Front-end processor.

FIFO – A first-in/first-out memory used when it is necessary to read out information in the same order that it was written into memory. It can be contrasted to a random access read/write memory (RAM) for transmission from one unit to another.

Filter – A circuit designed to pass selected signals while blocking all other signal components.

Foreign Exchange (FX) Service – A service connecting a subscriber's main station or private branch exchange with a central office other than that which normally serves the subscriber.

Format – A specified arrangement of data that permits identification of control and information fields by their location in the transmitted data stream.

Frame – In a time-division multiplexed system, a frame consists of a sequence of time slots, each containing a sample from one of the voice or data channels served by the system. Each time slot occupies the same sequence position in successive frames. In both DS1 and CEPT formats, a frame is repeated every 125 μs, corresponding to an 8 kHz sampling rate, and each time slot consists of 8 bits. In DS1 operation, a frame contains 24 time slots (192 bits) preceded by one framing bit. In CEPT operation, a frame contains 32 time slots (256 bits) with time slots 0 and 16 reserved for signaling and frame alignment. DS1 operation corresponds to a data transfer rate of 1.544 Mb/s (193 bits/125 μs), while CEPT operation is at a 2.048 Mb/s rate (256 bits/125 μs).

Framing – The process of establishing a reference so that time slots or elements within the frame can be identified.

Frequency Division Multiplexing (FDM) – A method of serving a number of simultaneous calls using a common transmission path with a different frequency band for each call.

Frequency Offset – A frequency shift that occurs when a signal is sent over an analog carrier facility when the modulating and demodulating frequencies are not identical. A channel with frequency offset does not preserve the waveform of the transmitted signal.

Frequency-Shift Keying (FSK) – A modulation technique for transmitting digital information having two or more discrete states. Each of the discrete states is represented by an associated frequency. The most common form is binary FSK, which uses two frequencies to represent the two binary states.

FSK – See **Frequency-Shift Keying**.

Full-Duplex Transmission (FDX) – A method of operating a communications circuit so that each end can simultaneously transmit and receive.

FX – See **Foreign Exchange Service**.

Gain – The amount of amplification produced by a device, measured as the ratio of output signal to input signal. Power amplification is measured in decibels and voltage amplification in volts per volt.

Gain Tracking Error – The maximum variation of gain over a range of input signals, calculated from a unity gain condition.

Gaussian Noise – Noise having uniformly distributed frequency and amplitude characteristics. Also known as white noise.

Glitch – An unwanted, extraneous, unpredictable noise pulse or spike that can cause hardware or software problems.

Half-Duplex Transmission – A method of operating a communications circuit so that each end can transmit or receive, but not simultaneously. Thus, normal operation is alternate, one-way-at-a-time, transmission.

Handset – A combination of a telephone transmitter and a telephone receiver mounted in a handle.

Handshaking – A term describing the alternation of send and acknowledge signals for establishing and confirming communication between two data communication devices.

Harmonic Distortion – The result of nonlinearities in the communication channel that cause harmonics of the input frequencies to appear in the output.

HDLC – See **High Level Data Link Control**.

Hermetically Sealed – A sealing procedure that protects the sealed device from chemicals, moisture, and other contaminants in compliance with testing according to Method 1014 of MIL-STD-883.

HIC – See **Hybrid Integrated Circuit**.

High Level Data Link Control (HDLC) – A standard data link communications protocol used for serial bit synchronous data transfer.

Hunting, Terminal or Trunk – The function performed by switching equipment in automatically searching for an idle line or trunk when the initially selected line is busy.

Hybrid – A network having four ports and designed to transmit an input signal equally between adjacent ports with no signal coupling to the opposite port. Hybrids are used to couple 4-wire circuits to 2-wire circuits.

Hybrid Integrated Circuit (HIC) – An electronic circuit that contains both silicon integrated circuits and circuitry fabricated by film deposition techniques.

I^2L – Integrated injection logic.

Impulse Noise – Short burst of high-level noise resulting from coupling of transients into a channel. Typical sources of impulse noise are lightning and switching system transients. Impulse noise, which sounds like a click, is not usually detrimental to voice communications, but can be detrimental to data transmissions.

Inband Signaling – Signaling that uses the same path and frequencies as that used for voice or data messages.

Insertion Loss – The ratio of power measured at a receiver before insertion of a transmission system to the power measured after insertion. Insertion loss is normally expressed in decibels (dB).

INTELSAT – See **International Telecommunications Satellite Consortium**.

Intercept Service – A service in which an improperly directed telephone call is redirected to an operator or recording. The caller is informed why the call could not be completed and, if possible, given the correct number.

Interface – A common boundary between two systems or pieces of equipment that insures proper connection between equipment.

International Direct Distance Dialing (IDDD) – The automatic establishment of international calls by signals from the calling device of either a customer or operator.

International Telecommunications Satellite Consortium (INTELSAT) – An international organization established in 1964 to govern a global commercial communications system. The Communications Satellite Corporation (COMSAT) acts as manager for INTELSAT and also represents the United States of America.

International Telephone and Telegraph Consultative Committee (CCITT) – One of two committees that supports the International Telecommunications Union (ITU) by conducting studies on technical and operating questions and recommending standards (the other committee is the International Radio Consultative Committee – CCIR). The ITU is an agency of the United Nations whose purpose is to encourage international cooperation and development of radio, telegraph, cable, telephone, and television communications.

IS – Intelligent switch.

ISDN – Integrated system digital networks.

ISO – International Standards Organization.

kb/s – kilo bits per second.

Kbytes – 1024 bytes.

Key Telephone Set – A telephone set with buttons or keys located on or near the telephone. It is used with associated equipment to provide features such as call holding, multiline pick-up, signaling, intercommunications, and conferencing.

Key Telephone Systems – Interconnection of key telephone sets without using central office or PBX facilities.

Keypulsing Signal – In multifrequency signaling, a signal keyed by the operator that is used to prepare distant equipment for receiving digits.

LAC – Local area concentrator.

LAN – Local area network.

LAP – Link access procedure.

LAPB – Balanced link access procedure.

Line – A pair of wires carrying direct current between a central office and a customer's terminal (see **Loop**). In carrier systems, line refers to the portion of a transmission system that extends between two terminal locations. This includes the transmission media and associated line repeaters.

Line Equipment – Equipment located in a central office associated with a particular line.

Loop – A channel between a customer's terminal and a central office. The most common form of loop, a pair of wires, is also called a line.

LSB – Least significant bit.

LSOXIL – Low power Schottky oxide isolated logic.

LSTTL – Low power Schottky transistor, transistor logic.

MAC – Message authentication code.

Mb/s – Mega bits per second.

Message – A set of information, typically digital and in a specific code, transmitted from a source to a destination. A header, containing address and handling information, may be part of the message.

Message Switching Network – A network in which the source provides messages which include destination and handling information. Typically, the message is in digital form and is stored at one or more points in the network; the storage time may be long (days) or short (microseconds). This contrasts with a line switching network where an unbroken channel is provided from source to destination, with no intermediate store and forward capabilities.

MIC – Modem interface chip.

Modem – A contraction of the words modulator and demodulator, signifying a piece of equipment that performs both of these functions. In this context, modulation refers to the process of converting parallel digital data into a serial bit stream for transmission over the analog telephone network. Demodulation refers to the process of converting the received serial bit stream back into parallel digital form.

MOS – Metal-oxide semiconductor.

MUX – Multiplexor.

NBS – National Bureau of Standards.

NCTE – See **Network Channel Terminating Equipment**.

Negate – To drive a singla to its inactive state.

Negative Logic – In a logic circuit, the mode of operation where the less positive voltage is selected as the 1-state, and the more positive voltage is selected as the 0-state.

Network – The aggregate facilities of a communications system consisting of transmissions, switching, and station equipment. Also used to describe a single electrical or electronic circuit that is packaged as a single piece of equipment, such as an equalization network.

Network Channel Terminating Equipment – Any channel terminating equipment.

Noise – An unwanted disturbance introduced into a communications circuit.

Nonlinear Distortion – Amplitude distortion caused by nonlinearities in a communications channel.

OFB – Output feedback.

Off-Hook – Station switchhook contacts closed, resulting in a request-for-service or in-use state.

On-Hook – Station switchhook contacts open, indicating an equipment-idle state.

Outstate T1 – T1 carrier implemented for service areas in excess of the normally recommended 50-mile T1 carrier limitation.

Packet-Switching – The transfer of a message using fixed size data packets which include address and handling information. Thus, each message may consist of one or more data packets.

PAM – See **Pulse Amplitude Modulation.**

PBX – See **Private Branch Exchange.**

PBX Tie Trunk – A trunk between two PBXs.

PC – Personal Computer.

PCM – See **Pulse Code Modulation.**

Phase Jitter – Phase variations in a channel caused by incidental frequency modulation of the transmitted signals. This occurs when the carrier supply frequencies in a frequency-division-multiplexed carrier system are not perfectly constant.

Phase-Shift Keying (PSK) – A modulation technique for transmitting digital information in which the data is conveyed by selecting discrete phase changes of the carrier.

Positive Logic – In a logic circuit, the mode of operation in which the more positive voltage is selected as the 1-state and the less positive voltage is selected as the 0-state.

Primary Access – Refers to a multiplexed communication link to an ISDN where the link has a channel structure consisting of either 23 or 30 B channels for voice or data and one D channel for control. Primarily intended for PBX and computer interfaces.

Private Branch Exchange (PBX) – A private switching system, either manual or dial, located on a customer's premises. Telephones served by the PBX are called stations.

Private Branch Exchange (PBX) Tie Trunk – A trrunk between two PBXs.

Private Line – A circuit leased by a customer for the exclusive use of connecting two or more terminals directly to each other without the need for any central office switched connections.

Protocol – An accepted set of rules or procedures that permit the orderly transfer of data between two communication devices.

PSK – See **Phase-Shift Keying.**

PTC – Protocol converter.

Pulse Amplitude Modulation (PAM) – A modulation technique in which the pulse amplitude is directly related to the analog signal amplitude. It is used in time-division multiplexed systems in which successive pulses represent samples from individual voiceband channels.

Pulse Code Modulation (PCM) – Conversion of an analog signal, such as voice, to a digital format in terms of a series of binary-coded pulses representing the quantized amplitude of the analog signal.

QAM – see **Quadrature Amplitude Modulation.**

Quadrature Amplitude Modulation (QAM) – A modulation system in which two independent signals are impressed on carriers of the same frequency that are 90° out of phase with respect to one another. QAM is attractive for high bandwidth utilization in data communication.

Quantizer – A component of a digital communications system that outputs a discrete value corresponding to the amplitude of each successive input sample. The possible output values consist of a finite set of discrete non-overlapping intervals covering the expected range of input amplitudes.

Quantizer Noise – The error that results from assigning a finite number of levels to a continuous signal.

RAM – Random access read/write memory.

RCC – Radio common carrier.

Regenerator – A repeater or amplifier that reshapes, by local generation, line signals used in digital transmission systems.

Register – A part of an automatic switching system that receives and stores signals from a calling device for interpretation and action.

Repeater – In analog circuits, an amplifier inserted in the transmission medium to compensate for attenuation and distortion introduced by the medium. In digital circuits, a device inserted in the transmission medium to regenerate a digital signal (see **Regenerator**).

Return Loss – The ratio of the incident wave to the reflected wave at the terminal of a transmission line or circuit. Where a 4-wire circuit is connected to a 2-wire circuit through a hybrid, return loss is the ratio of the wave entering the hybrid on one side of the 4-wire circuit to the reflected wave leaving the hybrid on the other side of the 4-wire circuit.

Ringer – A device, usually part of a telephone set, that responds to a 20-Hz signal to produce a ringing sound.

Ringing – The process of alerting the called party by the application of an intermittent 20-Hz signal to the appropriate line.

RNG – Random number generator.

ROM – Random access read-only memory.

RS – Receive synchronizer.

RSM – Remote switching module.

SCM – Switched capacitor modem.

SDLC – See **Synchronous Data Link Control.**

Seizure – The action of a switching system in selecting an outgoing trunk or other component for a particular call.

Selector – In step-by-step switching systems, an automatic switching mechanism actuated by DC pulses to select one of ten groups of intraoffice circuits, after which it hunts and connects to an idle circuit in the group.

Signaling – The transmission of address, supervision, or other switching information between stations and switching systems.

Singing – A continuous whistle or howl caused by oscillation in a telephone circuit. It occurs when the sum of the gains in the circuit exceeds the sum of all the circuit losses.

Slip – An advance or delay of a digital bit stream by an amount equal to or greater than one signal element.

SOJ – Small-outline, J-lead. This is the type of device package used for surface mounting.

Span Line – A T1 line section with repeaters installed connecting the two central offices. A T1 Carrier System is composed of a tandem combination of span lines, plus a digital channel bank at each terminal.

SPYDER – Synchronous protocol data formatter.

SPYDER-S – Synchronous protocol data formatter with serial interface.

Start-Stop – A timing and framing technique used in data transmission systems, especially teletypewriter systems data are transmitted asynchronously in the form of serial characters, each composed of a start element, information bits, and a stop element, with fixed bit transmittal timing.

Switching – The process of connecting together appropriate lines and trunks to form a desired communication path between two station sets. Included are the functions of sending and receiving signals, circuit status monitoring, address to routing translation, and trouble recording.

Switching System – An electromechanical or electronic system for connecting lines to lines, lines to trunks, or trunks to trunks. The term includes PBX switching systems (manual and automatic), local switching systems, and toll switching systems (see **Switching**).

Synchronous Data Link Control – An advanced line control discipline for communication between terminals and computers. It is a key element of systems network architecture.

T1 Carrier – A 1.544 Mb/s signal used to transmit 24 separate channels of pulse code modulated (PCM) voice or digital data. Each channel consists of eight bits. All 24 eight-bit channels are grouped together to form a unit of 192 bits. For synchronization (framing), every group of 192 bits is preceded by one framing bit. The complete group of 193 bits is called a frame.

Telegraph – The transmission systems, switching systems, and services that are oriented toward narrow band, private-line data services at speeds up to 150 b/s. The most common service of this type is teletypewriter.

Telephone Set – The terminal equipment on a user's premises for voice telephone service. This includes the transmitter, receiver, switchhook, dial, ringer, and associated circuits.

Teletypewriter – An electromechanical typewriter that generates a coded signal corresponding to the character typed on the keyboard. This signal may be sent over appropriate transmission facilities to control a similar remote teletypewriter.

Teletypewriter Exchange Service (TWX) – A service connecting a teletypewriter to a TWX switching system.

Terminal – Equipment at the end of a communications circuit.

TDM – See **Time Division Multiplexing**.

Time Division Multiplexing – A data communications technique for transmitting a number of independent channels using a common communications path. Each channel is sampled, and assigned a specific time interval in the transmitted frame (see **T1 Carrier**).

Time Slot – A fixed time interval in a transmitted frame. Each time slot consists of one sample from a channel.

Tip and Ring – The two conductors associated with a 2-wire cable pair. The terms derive their names from the physical characteristics of an operator's manual cordboard plug, in which these two conductors terminated.

TLP – Transmission level point.

0TLP – Zero transmission level point.

Transmission Facility – An element of a communications system that performs the function of transmission; for example, a line, coaxial cable, or microwave radio system.

Trunk – A communication channel between two switching systems.

TSI – Time slot interchanger.

TTL – Transistor-transistor logic.

Twisted Pair – A pair of wires used in transmission circuits that are twisted together to minimize coupling to other circuits.

TWX – See **Teletypewriter Exchange Service.**

UART – See **Universal Asynchronous Receiver Transmitter.**

Unipolar Signal – A digital signal technique that uses positive (or negative) excursion and ground as the two binary signal states.

UNITE – User-to-network interface in terminal equipment.

Universal Asynchronous Receiver Transmitter – A device that accepts parallel input data and transmits it serially.

VLSI – Very large scale integration.

Word – An ordered set of characters expressing a unit of information.

X.25 – A CCITT international standard protocol for intranetwork packet switching. The standard defines the interface between data terminal equipment and data communication equipment for terminals operating in the packet mode on public data networks.

X.75 – A CCITT international standard protocol for internetwork packet switching networks.

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