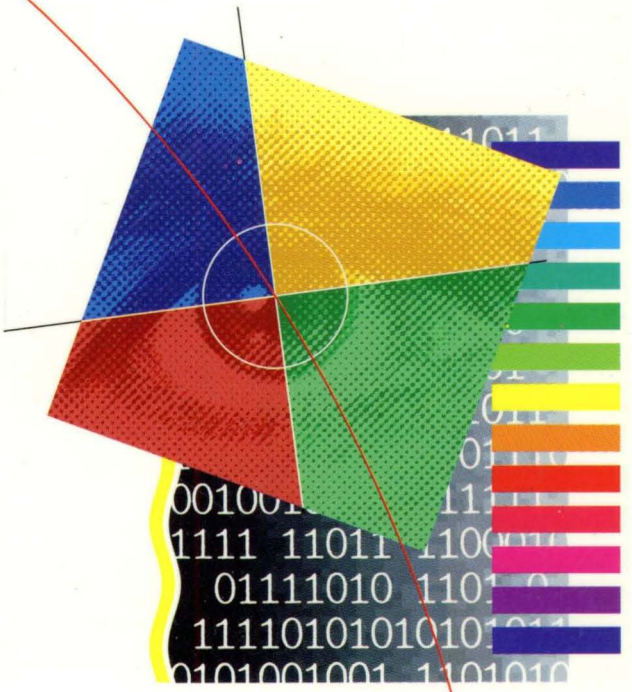
PRODUCT DATABOOK



B R O O K T R E E

Product Index

*New products

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PRODUCT DATABOOK 1989

Thank you for your interest in Brooktree products.

Our commitment is to provide a steady stream of innovative products that offer the highest quality, lowest cost/performance solutions and back them with comprehensive support services. These include timely and accurate technical information and responsive, experienced applications assistance.

At Brooktree, listening to customer's requirements is what we do first. Solving customer problems is what we do best.

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Company Facts

Brooktree began operations in 1983 following the development of an advanced architecture for data conversion. The architecture, invented by company co-founder and chief scientist Henry Katzenstein, permits the combination of high-performance analog and digital circuitry on a single monolithic integrated circuit which can be manufactured using standard bipolar or CMOS processes.

Brooktree Corporation is a privately held company located in San Diego, California. A 72,000 sq. ft. facility houses all design, test, and quality assurance activities as well as marketing, sales, and administration. Brooktree has established a worldwide network of distributors and factory representatives, with offices in the United States, Europe, and the Far East.

The company's products are manufactured under agreements with several domestic and international foundry sources. Second-source agreements are in effect with a number of suppliers.

Since its first volume shipments in 1985, Brooktree has achieved leadership share in the workstation graphics market, and a large share of the emerging market for PC graphics applications.

Products

Our first product, introduced in early 1985, was a 75 MHz 8-bit CMOS video digital-to-analog converter (VIDEODAC). By mid-1985, Brooktree had introduced six CMOS video digital-to-analog converter products (our VIDEODAC line) to the high-performance graphics market. Further system level integration led to our family of RAMDACs, which combine triple VIDEODACs, color palette RAMs, and pixel input multiplexers on a single chip. Recently introduced products include a 360 MHz bipolar RAMDAC and several next-generation CMOS RAMDACs.

In 1988, Brooktree entered the image acquisition market with it's first CMOS flash video A/D converter. Further system level integration led to our family of Image Digitizers, which combine one or more A/D converters and many additional functions required to digitize a video signal. Additional products are under development to enable image acquisition to be a "drop-in" solution.

Products for the automatic test equipment and instrumentation markets include the industry's first octal 8-bit monolithic DAC and programmable timing verniers which achieve delay resolutions of as little as 20 picoseconds.

Strategy

Brooktree will combine the elements of its high-performance mixed signal design capabilities and proprietary test technology to provide a unique family of application-specific products. We will continue to develop highly-integrated products for use in computer graphics and imaging while introducing enabling technologies aimed at solving problems in the automatic test equipment and instrumentation markets.

Data Sheet Designations

Advance Information

This is the first official information released about a potential product. The datasheet contains basic information about the product and contains the target parametric and functional specifications. It usually precedes sample devices by approximately six months. This datasheet has the phrase "Advance Information" in the upper left corner on the front page.

Preliminary Information

This datasheet is released with sample devices. It contains a more extensive discussion of device operation and provides more complete parametric information. The functional operation is fully defined and the parametric information is the result of early testing of the initial devices. Not all of the parametric specifications may be fully tested or characterized. This datasheet has the phrase "Preliminary Information" in the upper left corner on the front page.

Final datasheet

This datasheet evolves from the Preliminary Information datasheet. It is a result of test information collected from fully characterized devices. This datasheet is distinguished by the absence of any designation, except the part number, at the top of the front page.

Device Designations

Engineering Sample

Devices which have exhibited most of the functionality for which it was designed. Engineering samples are used to enable selected customers to evaluate the device as early as possible.

While some of the AC and DC parameters may be tested, the accuracy or completeness of the testing is not guaranteed. In addition, the product has not been put through Brooktree's quality and reliability testing. They have standard marking with an additional "ES" marked on top of the package. These devices have a Preliminary datasheet under document control.

Pre-Qual

These devices have production silicon, testing, and burn-in. Most characterization is done, but the device must still pass a QA life-test qual. These devices have standard marking with an additional "PQ" marked on top of the package. These devices have a Preliminary datasheet under document control.

Full Production

These devices have production silicon, testing, burn-in, and have successfully passed a QA life-test qual. These devices have standard marking with no additional designators. These devices have a Final datasheet under document control.

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Introduction

The value of a product is measured by how well it is designed, manufactured and tested and how well it continues to perform over time. This value can be represented in quantitative terms by stating levels of quality and reliability. Brooktree determines these quality levels by performing industry recognized evaluation and monitoring programs for all products it manufactures.

Quality is a critical aspect of product success, and we have established an aggressive schedule of measuring, testing and monitoring the product to assure our customer that each device will perform to the highest quality and reliability standards. We have made substantial investments in experienced personnel and in state-of-the-art capital equipment for our design, manufacturing and quality assurance departments.

Product Quality

Quality is a measure of product conformance to the specifications. This is determined by measuring the percentage of defects in a given sample size. The Quality Assurance program includes material inspections which employ industry-standard Lot Tolerance Percent Defective (LTPD) and Acceptable Quality Level (AQL) sampling plans. These sampling procedures assure with a high degree of confidence that a lot will not be approved for shipment if certain levels of quality are not met. For sampling plans, the operating characteristic curve illustrated in Figure 1 shows the relationship of lot quality versus probability of acceptance. Point A on the curve is termed AQL; it signifies the lot quality in percent defective (0.065%) that will give a high probability (95%) of lot acceptance. Point B on the curve is termed LTPD and signifies the unsatisfactory level of quality where the lot will be rejected 90% of the time. Brooktree performs quality conformance testing using an acceptance sampling method based on MIL-STD-105D and MIL-M-38510H.

Manufacturing process control is accomplished through the efforts of the Document Control Department. An effective plan for document sign-off and distribution ensures that updated documents are reviewed and are made available immediately to affected operations.

Brooktree's Quality Assurance program imposes strict requirements on vendors, and monitors their performance through inspection of incoming materials and regular audits of the vendor's facilities and quality methods. Figure 2 is a generalized standard product manufacturing flow which illustrates the manufacturing steps and quality assurance

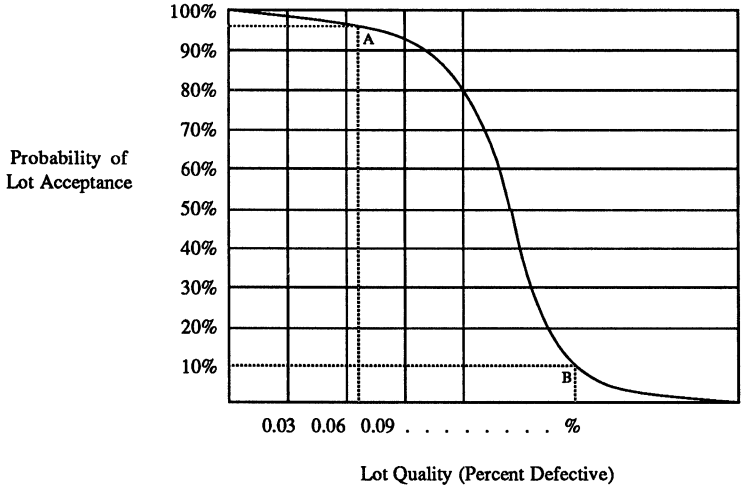

Figure 1. Lot Quality vs. Probability of Acceptance.

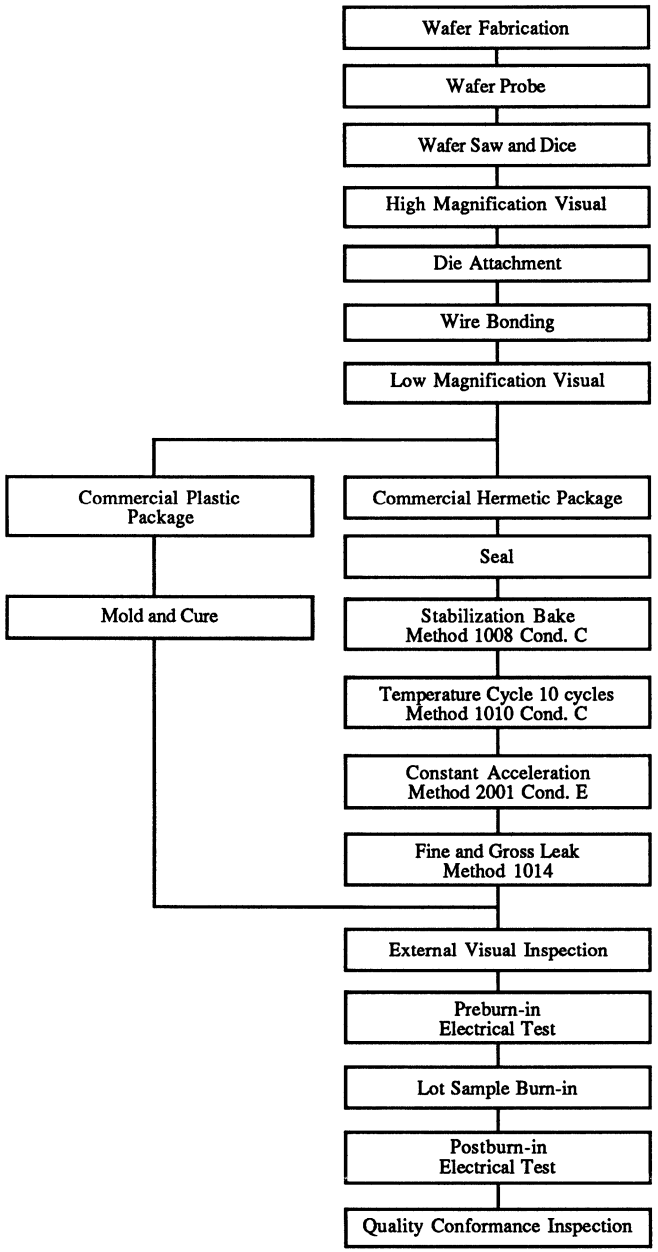

Figure 2. Standard Product Manufacturing Flow.

monitors used for all our products. The Brooktree quality assurance program conforms to the program guidelines as specified in MIL-Q-9858.

Product Reliability

Reliability is quality over time, a measurement of how long the product continues to perform to original specifications. This must be guaranteed by using a worst-case design methodology, precisely controlled wafer-processing, and manufacturing assembly and testing to highest quality standards.

Verification of product reliability is accomplished through accelerated life testing and physical and environmental stress testing. The stress tests performed for product qualification are listed in Tables 1 and 2. These tests are repeated at six-month intervals to verify continuing process and product integrity. Strict engineering change control procedures are used to assure a controlled process.

Screening is performed to eliminate early-failure devices and to conform to military requirements. Military grade products are tested in conformance to MIL-STD-883C; refer to the Military Section of this manual for further details. The basic method used to estimate product life is accelerated environmental testing. These tests expose the product to stresses greater than expected in actual use. The number of device failures that occur can be related to the magnitude of the stress applied. The common practice is to express the results in failures in 10^9 hours, or FITs (one FIT is equal to one failure per billion device hours of operation. It can also be expressed in the common notation of 0.0001% failures per 1000 hours).

Figure 3 is an idealized graph of device failure rate vs time, often called the Bathtub Curve. Three distinct regions are of importance. **Region A** is characterized by high failure rates that show up in early usage and then decrease with time. This area of early life failures needs to be eliminated prior to product being shipped to the final consumer. The early life failure rate is minimized by screening procedures, the most common of which is burn-in testing performed at the device and/or system level. **Region B** is characterized by a constant failure rate, and indicates the normal operating region that will assure maximum useful service and reliability. **Region C** indicates the wearout region where device failure rate increases. The wearout region is seldom reached in well-designed semiconductor integrated circuits under normal operating conditions. Results of accelerated life testing are extrapolated to estimates of in-service reliability through use of the Arrhenius model.

Product Development

Quality and Reliability planning begins with the product development cycle. It is vital that every possible effort to increase the reliability is made during the development cycle. This is achieved by defining specific design goals, using proven reliable materials and manufacturing methods, and implementing controlled production processes with accurate testing and monitoring.

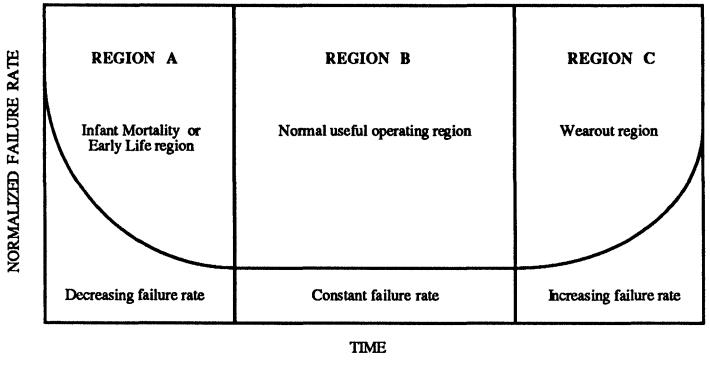

Figure 3. Device Failure Rate vs. Time.

Design

Brooktree's engineering department has established a comprehensive design methodology developed to produce reliable devices. Product definition begins with experienced system designers who can accurately specify the electrical interface and functional boundary requirements. This assures that all new devices will have specifications and worst case operating and environmental conditions identified before design begins.

Design engineers use schematic capture and simulation software to verify the operation of the design over temperature, power supply and processing variations. Design reviews require designers to demonstrate to the Quality Assurance department that their design will meet or exceed reliability rules, including allowable amount of electrostatic discharge (ESD), latch-up protection (CMOS products), and current density (to prevent metal migration). Computer simulation of each circuit design is done using a worst case methodology.

Conformance to strict layout rules gives products immunity to process variation while maximizing reliability. An extensive set of checks is provided by several state-of-the-art CAD tools that assure the design layout is correct and that wafers can be consistently processed with confidence in yield and reliability.

Wafer Probe

Wafer probe is performed at Brooktree to ensure the tightest quality and reliability controls early in the life of the product. Wafer probe test conditions and limits are guard banded to ensure early removal of defective devices. Correlation between the final test programs and probe programs is an effective gate to prevent a non-functional device from entering the assembly operation. Rejected dice are marked with an ink dot to allow easy identification after the individual die is scribed from the wafer.

Device Assembly

The Quality Assurance department monitors the performance of various processing steps by requiring mandatory sampling of each lot moving through critical quality operations. We have instituted eight sampling points or gates in the assembly area: wafer inspection, material inspection, 1st QA die visual (high magnification), die attach control, 2nd QA die visual (low magnification), QA hermeticity check, QA final inspection and QA outgoing audit. Daily monitoring and audits of equipment and operators ensure that the final product meets all predefined quality criteria.

Device Packaging

Brooktree packaging uses standard, semi-custom and custom packages. Package outlines and foot prints comply with JEDEC and SEMI standards whenever possible. Since product performance is affected by packaging design, custom packages are constructed when necessary to preserve the reliability and performance of the enclosed device.

Final Testing

Final electrical testing is performed at Brooktree using state-of-the-art test equipment and techniques. Test parameters and test conditions are such that proper performance is guaranteed to data sheet requirements. Test limits are guard banded to compensate for tester inaccuracy, thereby minimizing measurement correlation errors between the factory and customer. To comply with quality conformance requirements, QA verifies proper processing, proper electrical performance over specified operating temperatures and voltage ranges, and visual criteria.

Qualification

All products we manufacture are labeled to show the classification of the products reliability for consumer use. Each product datasheet contains a designation as to the product development and specification parameters status. The product datasheet designations are Advanced, Preliminary and Final. When the device has been fully characterized to all the specifications and datasheet parameters, and has completed the environmental tests outlined in Tables 1 and 2, it is labeled production worthy and labeled a Final Data Sheet.

Failure Analysis

Even under the strictest of standards, failures do occur. To control this situation and learn from it, the failure analysis group identifies reliability problems and performs corrective action on failures from in-house stress testing as well as customer field returns. Brooktree provides customers with specific feedback so that the customer can be assured that appropriate action has been taken.

Description	Methods and Conditions*	Sample / Max. Reject	Notes
High Temperature Operating Life Electrical	2000 hours, TA = 125° C. *** TA = Tmax	280 (<400 FIT) **** 	electrical at 16, 48, 168, 500, 1000, 1500, 2000 hours
High Temperature Storage Electrical	2000 hours, TA = 200° C. TA = Tmax	55 / 0 	electrical at 500, 1000, 1500, 2000 hours
Temperature Cycle Electrical	Method 1010, condition C, -65° C. / +150° C., 500 cycles TA = Tmax	116 / 0 	
Thermal Shock Electrical	Method 1011, condition B, -55° C. / +125° C., 200 cycles TA = Tmax	116 / 0 	electrical every 500 cycles
Pre-conditioning Temperature Cycle Temperature Cycle Electrical	-40° C. / +150° C., 20 cycles 0° C. / +125° C. 3000 cycles TA = Tmax	153 / 0 	
Pre-conditioning Temperature Cycle Pre-conditioning Temperature/Humidity Steady-State Temperature/Humidity Electrical	-65° C. / +150° C., 10 cycles 85° C. / 85% RH, 24 hours, unbiased 85° C. / 85% RH, 1500 hours, biased TA = Tmax	195 / 1 	plastic package only electrical at 500, 1000, 1500 hours
Pressure Cooker Electrical	125° C., 2.3 atm, 288 hours TA = Tmax	77 / 1 	plastic package only
Destructive Physical Analysis	SEM - surface and cross section	3 sets	1 set from each of 3 wafer lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 wafer lots (each lot shall be processed with a minimum of 1 week separating it and the other two wafer lots.

***Power supplies shall be set to 0.5v less than the absolute maximum specified supply voltage; TA shall be reduced, if necessary, to guarantee TJ to be less than 175° C. for ceramic packages, or less than 150° C. for plastic packages.

****FIT shall be calculated using the Ahhrenius acceleration model and the following assumptions:
Ea = 0.5 eV if no failures; if failures, Ea to be determined based upon failure mechanism.
Ts = 55° C. (derating temperature)
confidence level = 60%

Table 1. Wafer Foundry Tests**.

Description	Methods and Conditions*	Sample / Max. Reject	Notes
External Lead Plating Thickness Solderability	Method 2003	4 / 0 4 units / all leads	
Resistance to Solvents	Method 2015	4 / 0	
Internal Visual Bond Strength Die Shear	Method 2010 Method 2011 Method 2019	4 / 0	
External Lead Integrity Fine Leak Gross Leak	Method 2004, condition B Method 1014 , condition A or B Method 1014 , condition C	34 / 2	 for CERDIP only for CERDIP only
Temperature Cycle Electrical	Method 1010, condition C, -65° C. / +150° C., 500 cycles TA = Tmax	116 / 0	
Thermal Shock Electrical	Method 1011, condition B, -55° C. / +125° C., 200 cycles TA = Tmax	116 / 0	
Preconditioning Temperature Cycle Temperature Cycle Electrical	-40° C. / +150° C., 20 cycles 0° C. / +125° C., 3000 cycles TA = Tmax	153 / 0	 electrical every 500 cycles
Steady-State Temp. and Humidity Visual	85° C. / 85% RH, 1500 hours, biased	50 / 0	empty (dummy) packages may be used
Mechanical Shock Vibration Constant Acceleration Fine Leak Gross Leak Electrical	Method 2002, condition B Method 2007, condition A Method 2001, condition E, Y1 axis only Method 1014, condition A or B Method 1014, condition C TA = Tmax	34 / 2	

Table 2. Monolithic Hermetic Package Assembly Tests**.

Description	Methods and Conditions*	Sample / Max. Reject	Notes
Salt Atmosphere Fine Leak Gross Leak	Method 1009 Method 1014, condition A or B Method 1014, condition C	34 / 2	
Resistance to Soldering Heat Fine Leak Gross Leak Electrical	15 sec dip to with 1/8" of body in solder at 260° C. Method 1014, condition A or B Method 1014, condition C	22 / 0	
Destructive Physical Analysis	SEM - surface and cross-section	3 sets	1 set from each of 3 assembly lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 assembly lots (each lot shall be processed with a minimum of 1 week separating it and the other two assembly lots.

Table 2. Monolithic Hermetic Package Assembly Tests**. (Continued)

Description	Methods and Conditions*	Sample / Max. Reject	Notes
External Lead Plating Thickness Solderability	Method 2003	4 / 0 4 units / 2 leads	
Resistance to Solvents	Method 2015	4 / 0	
X-Ray		4 / 0	
Mechanical Shock Electrical	Method 2002, condition B TA = Tmax	25 / 1	
Temperature Cycle Electrical	Method 1010, condition C, -65° C. / +150° C., 500 cycles TA = Tmax	116 / 0	
Thermal Shock Electrical	Method 1011, condition B, -55° C. / +125° C., 200 cycles TA = Tmax	116 / 0	
Preconditioning Temperature Cycle Temperature Cycle Electrical	-40° C. / +150° C., 20 cycles 0° C. / +125° C., 3000 cycles TA = Tmax	153 / 0	 electrical every 500 cycles
Preconditioning Temperature cycle Preconditioning Temperature/Humidity Steady-State Temperature/Humidity Electrical	-65° C. / +150° C. 10 cycles 85° C. / 85% RH, 24 hours, unbiased 85° C. / 85% RH, 1500 hours, biased TA = Tmax	195 / 1	 electrical at 500, 1000, and 1500 hours
Pressure Cooker Electrical	125° C., 2.3 atm, 288 hours TA = Tmax	77 / 1	

Table 3. Monolithic Plastic Package Assembly Tests**.

Description	Methods and Conditions*	Sample / Max. Reject	Notes
Salt Atmosphere	Method 1009	34 / 2	
High Temperature Operating Life Electrical	TA = 125° C. (TJ < 150° C.), 1500 hours TA = Tmax	150 (< 400 FIT) ***	electrical at 500, 1000, 1500 hours
Preconditioning Pressure Cooker Infra-Red Reflow (IR) Pressure Cooker Electrical	125° C., 2.3 atm, 72 hours 3 cycles 125° C., 2.3 atm, 200 hours TA = Tmax	45 / 0	PLCC packages only
Preconditioning Pressure Cooker Infra-Red Reflow (IR) Temperature Cycle Electrical	125° C., 2.3 atm, 72 hours 3 cycles Method 1010, condition C -65° C. / +150° C., 500 cycles TA = Tmax	45 / 0	PLCC packages only
Preconditioning Temperature Cycle Preconditioning Temperature/Humidity Vapor Phase Solder Pressure Cooker Electrical / Visual	Method 1010, condition C, -65° C. / +150° C., 20 cycles 85° C. / 85% RH, 72 hours, unbiased 125° C., 2.3 atm, 200 hours TA = Tmax	45 / 0	PLCC packages only
Resistance to Soldering Heat Electrical	15 sec dip to within 1/8" of body in solder at 260 °C. TA = 25 °C.	22 / 0	
Destructive Physical Analysis	SEM - surface and cross-section	3 sets	1 set from each of 3 assembly lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 wafer lots (each lot shall be processed with a minimum of 1 week separating it and the other two wafer lots.

***FIT shall be calculated using the Ahhrenius acceleration model and the following assumptions:
Ea = 0.5 eV if no failures; if failures, Ea to be determined based upon failure mechanism.
Ts = 55° C. (derating temperature)
confidence level = 60%

Table 3. Monolithic Plastic Package Assembly Tests**. (Continued)

Terms and Definitions

Activation Energy

The excess energy over the ground state which must be acquired by an atomic or molecular system in order for a specific process to occur. In semiconductor materials this energy is usually equal to 0.96 eV.

Arrhenius Model (Acceleration Factor)

The Arrhenius Model defines a relationship between the failure rate and time that is commonly used in correlating accelerated life environmental testing to useful lifetime. The equation is used to calculate failure rates based on lower junction temperatures and normal operating environmental conditions.

The acceleration factor is the reaction rate of a process at one temperature compared with the reaction rate of the same process at another temperature. The acceleration factor equation determines the multiplication factor of time that the change in temperature caused on the reaction process.

$$AF = e^{[\,E/K\,(1/T_1 - 1/T_2)\,]}$$

Where:
AF = Acceleration Factor
e = natural logarithm base of 2.71828
E = the activation energy for semiconductor material
K = Boltzmann's Constant (8.61×10^{-5} eV / Kelvin)
T_1 = Lower temperature in Degrees Kelvin
T_2 = Higher temperature in Degrees Kelvin

Example: The AF for a temperature change from 85° C. to 125° C. is 393.8. This factor is the time multiplication factor: 1 hour at 125° C. is equivalent to 393.8 hours (over 16 days) at 85° C.

Bias

The electrical connection to the device pins that allows specified signals, loading, and power supply voltage to be applied. Often referred to as "electrical bias."

Biased Humidity

An environmental test where the subject device is exposed to high humidity and temperature conditions (85% relative humidity and 85° C.) while having the device under an electrical bias. This procedure is designed to measure the device's susceptibility to electrolysis or electrolytic corrosion. The acceleration factor for a humidity change from 50% to 85% has been standardized as approximately 10. In analyzing bias humidity and temperature results, the acceleration factors of humidity and temperature are estimated separately.

Burn-In

A thermal and electrical stress test designed to eliminate early failures. The early device failures (infant mortality) are detected and removed, thus enhancing reliability.

Environmental Tests

Several tests that determine the long-term stability and reliability of products. The product is exposed to various conditions and extremes of temperature, humidity, pressure or mechanical stress that stimulates potential faults to appear, and accelerate detection of device failures.

Failure in Time (FIT)

A standard reliability unit that measures the device failure rate as a function of device hours. One FIT is equal to one device failure per billion device hours of operation (1 FIT = 0.0001% failures / 1000 hours).

Infant Mortality

Initial failures of devices that occur in early life operation. This is the region of the device failure rate curve where the device failure rate decreases with time. Product reliability is enhanced when environmental screening eliminates these early failures region.

Terms and Definitions (continued)

Pressure Cooker

A test that subjects the device to an atmosphere of high temperature moisture under a pressure of approximately two atmospheres. This test exposes susceptibility to galvanic corrosion due to chemical instability of the encapsulating materials.

Qualification

The test procedures as defined by the Quality Assurance Department that a product must survive before being considered a reliable manufacturing product.

*Quality**

The extent to which a product successfully serves the purpose of the user, during usage, is called "fitness for use." This concept of fitness for use is popularly called quality. Several parameters can be used to characterize product quality. Quality of design is a technical measure of the level or degree of excellence of the product to meet it's intended needs of the user. Three activities that compose the quality of design are; Quality of market research, Quality of concept, and Quality of specification. Quality of conformance is the extent to which the product conforms to the design, and can be measured by testing to the product specification. Conformance also is termed Quality of manufacturing or Quality of production. The quality of products over time is characterized by the time-oriented factors such as; availability, reliability, and maintainability.

Quality Assurance (QA)

The activity of providing, to all concerned, the evidence needed to establish confidence and assurance that all the activities which affect product quality are being performed adequately.

Reliability

Quality of products over time can be stated by the products ability to perform without failure. The classic definition is "the probability of a product performing without failure a specified function under given conditions for a specified period of time."

Reliability Growth

The continuing efforts to reduce failure rates result in continued improvements (or growth) in reliability. This takes place in the design and manufacturing phases, and when additional product improvements are needed as determined from field performance data.

Sampling

Inspection method to determine lot quality by careful examination of a small number of devices from the lot. A sampling plan is used to set the sample size, based on the desired quality level.

Screening

The process of subjecting all products to non-destructive stresses to accelerate and identify early failures.

Stress

An extreme environmental, electrical or physical condition applied to a device to evaluate the device performance or to accelerate reaction rates.

Temperature Cycling

A test that determines the thermal expansion compatibility of materials used in device packaging. The test exposes the device to temperature extremes, typically a low temperature of -65° C. to a high temperature of +150° C. The device is under no electrical bias.

Thermal Shock

This is a temperature cycling test in which the temperature transitions are very rapid, less than 10 seconds. The device is immersed in suitable liquid baths, each having extreme high and low temperatures to expose failures such as device cracking, and package leaking.

*QUALITY CONTROL HANDBOOK, Third Edition McGraw Hill 1974, JURAN, Joseph M., Frank M. Gryna Jr., and R.S. Bingham Jr.

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3

Product Index

Product Index (continued)

Product Index (continued)

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Table of Contents

VIDEODAC Selection Guide

D/A Organization	Speed (MHz)	Part Number	Page	DL Error (LSB)	IL Error (LSB)	
triple 4-bit	75, 30	Bt103	4 - 33	± 1/16	± 1/8	monolithic CMOS
single 8-bit	400	Bt107	4 - 61	± 1/2	± 1/2	2:1 muxed inputs
single 8-bit	75	Bt102	4 - 19	± 1/4	± 1/2	programmable setup
single 8-bit	50, 30	Bt106	4 - 47	± 1	± 1	monolithic CMOS
triple 8-bit	250	Bt109	4 - 75	± 1/2	± 1/2	10KH ECL
triple 8-bit	50, 30	Bt101	4 - 5	± 1	± 1	monolithic CMOS

	Display Resolution				
DAC Size	Low (640 x 480)	Medium (1k x 800)	High (1280 x 1024)	Medium High (1600 x 1200)	Ultra High (2k x 2k)
4-bit	Bt103	Bt103			
8-bit	Bt101 Bt102 Bt106	Bt102	Bt109	Bt109	Bt107

Bt101

50 MHz

Monolithic CMOS

Triple 8-bit

VIDEODAC™

4

Distinguishing Features

- 50, 30 MHz Operation
- Triple 8-bit D/A Converters
- ± 1 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Outputs
- TTL Compatible Inputs
- +5v CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

Product Description

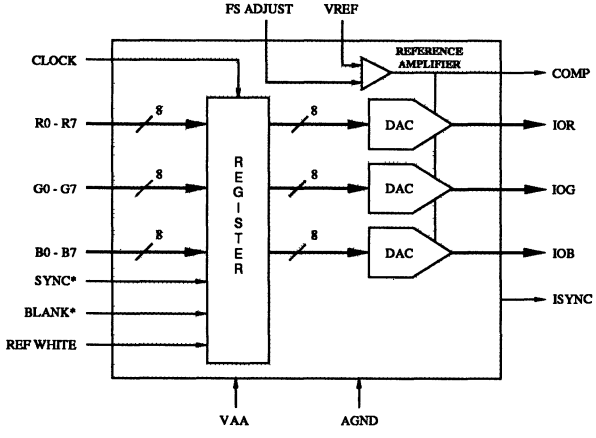
The Bt101 is a triple 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog outputs to the reference white level, regardless of the data inputs.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt101 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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Circuit Description

As illustrated in the functional block diagram, the Bt101 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0 - R7, G0 - G7, and B0 - B7) are latched into the device and presented to the three 8-bit D/A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, forces the inputs of each D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output levels.

The ISYNC current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If ISYNC is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG, and IOB outputs will have the same full scale output current.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 ohms for generation of RS-343A video into a 37.5-ohm load. The VREF input requires an external 1.2v (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converters on the Bt101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt101 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

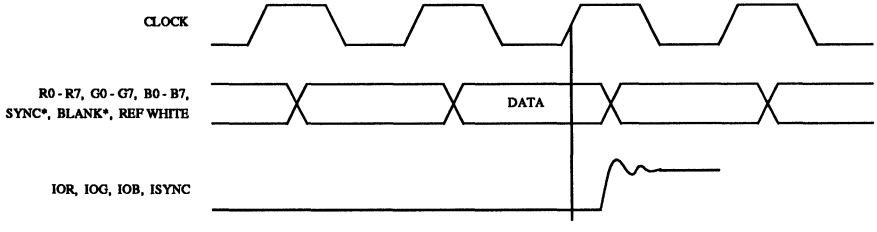
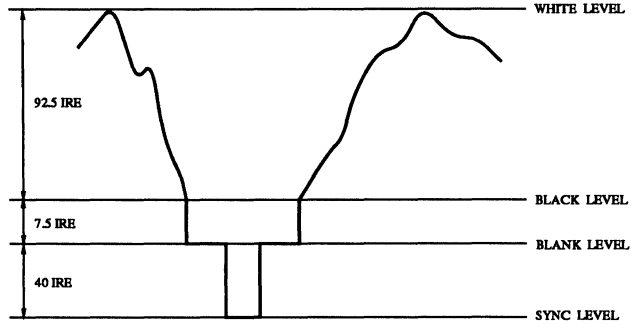


Figure 1. Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	1	$xx
WHITE	26.67	19.05	0	1	1	$FF
DATA	data + 9.05	data + 1.44	0	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	0	1	data
BLACK	9.05	1.44	0	1	1	$00
BLACK - SYNC	1.44	1.44	0	0	1	$00
BLANK	7.62	0	x	1	0	$xx
SYNC	0	0	x	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG.

Table 1. Video Output Truth Table.

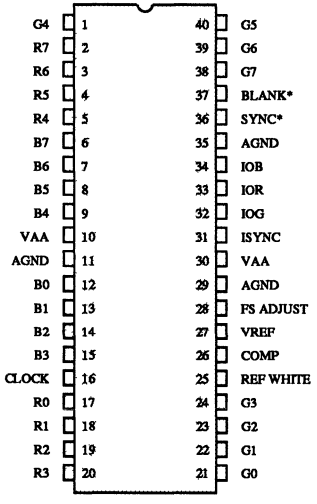
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0 - R7, G0 - G7, B0 - B7, and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R0 - R7, G0 - G7, and B0 - B7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R0 - R7, G0 - G7, B0 - B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0 - R7, G0 - G7, B0 - B7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. Typically, this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logical zero on the SYNC* input results in no current being output onto this pin, while a logical one results in the following current being output: ISYNC (mA) = 3,442 * VREF (v) / RSET (ohms) If sync information is not required on the green channel, this output should be connected to AGND.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG (assuming ISYNC is connected to IOG) is: RSET (ohms) = 12,046 * VREF (v) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 8,604 * VREF (v) / RSET (ohms)

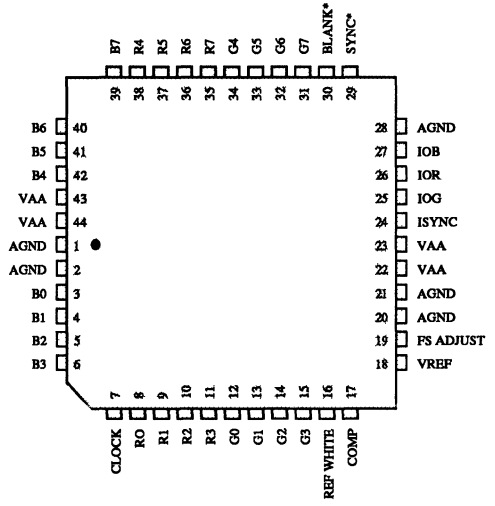
Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the nearest VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.

40-pin DIP Package



44-pin Plastic J-Lead (PLCC) Package



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt101 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt101 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101.

The analog ground plane area should encompass all Bt101 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt101, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt101.

Power Planes

The Bt101 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt101 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each of the two groups of VAA pins to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt101 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt101 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt101 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

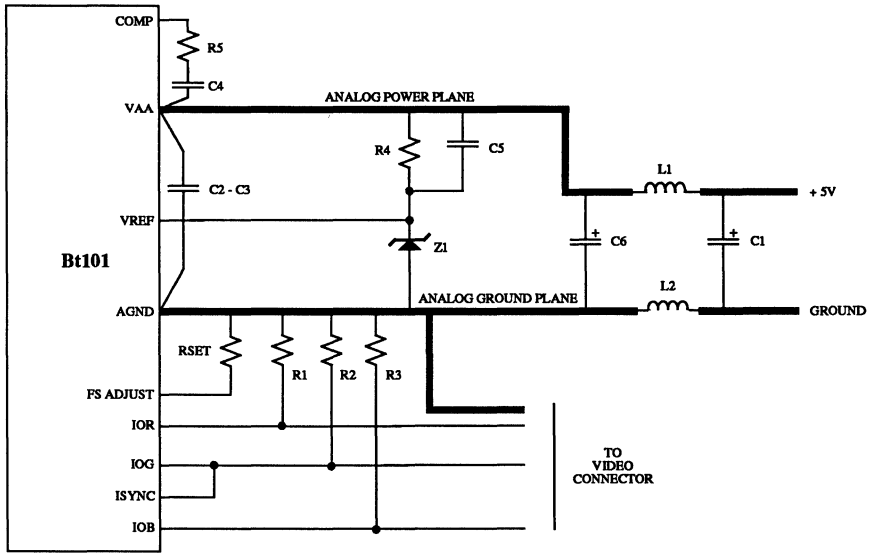
Analog Signal Interconnect

The Bt101 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt101 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1000-ohm 1% metal film resistor	Dale CMF-55C
R5	15-ohm 1% metal film resistor	Dale CMF-55C
RSET	549-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt101.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with an RSET value of about 774 ohms. If the Bt101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/(20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

COMP Resistor

To optimize the settling time of the Bt101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt101 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one. ISYNC should be connected to AGND. All three outputs will have the same full scale output current.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,958 * VREF (v) / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (v) / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full scale" control.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt101KC30, Bt101KPJ		0		+ 70	°C.
Bt101BC		- 25		+ 85	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL		± 0.3	± 1	LSB
Differential Linearity Error	DL		± 0.3	± 1	LSB
Gray Scale Error			± 1	± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2		%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v, ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		50 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time	TSU	6			8			ns
Data and Control Hold Time	TH	2			2			ns
Clock Cycle Time	TCYC	20			33.3			ns
Clock Pulse Width High Time	TCLKH	8			10			ns
Clock Pulse Width Low Time	TCLKL	8			10			ns
Analog Output Delay	TDLY		25			25		ns
Analog Output Rise/Fall Time	TVRF			8			9	ns
Analog Output Settling Time	TS		12			15		ns
Clock and Data Feedthrough*			- 28			- 28		dB
Glitch Impulse*			100			100		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew			0	3		0	3	ns
Differential Gain Error	DG		1.8			1.8		% Gray Scale
Differential Phase Error	DP		1.2			1.2		Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current**	IAA		120	175		100	140	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v, ISYNC connected to IOG. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 15 ohms. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

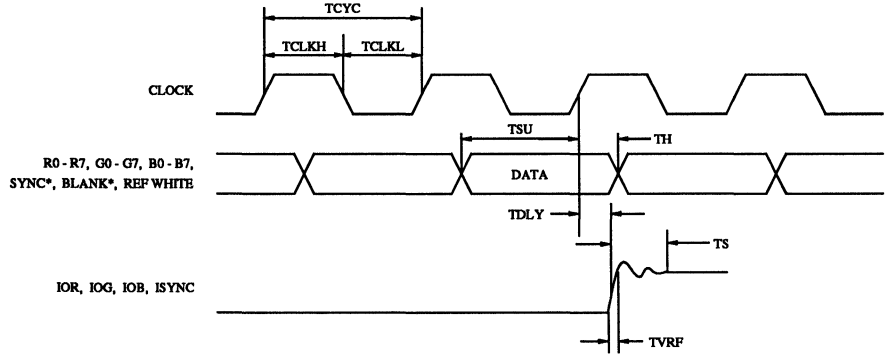
*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt101BC	50 MHz	40-pin 0.6" CERDIP	-25° to +85° C.
Bt101KC30	30 MHz	40-pin 0.6" CERDIP	0° to +70° C.
Bt101KPJ	30 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt101EVM	Evaluation Board for the Bt101		

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

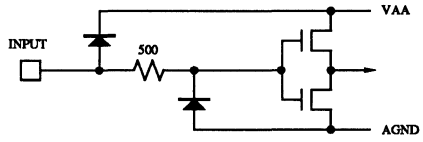


Figure 5. Equivalent Circuit of the Digital Inputs.

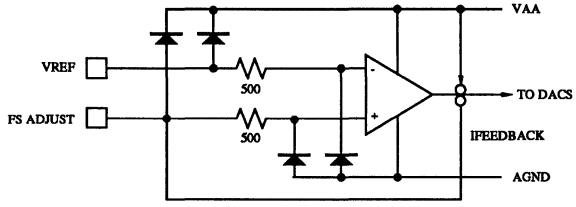


Figure 6. Equivalent Circuit of the Reference Amplifier.

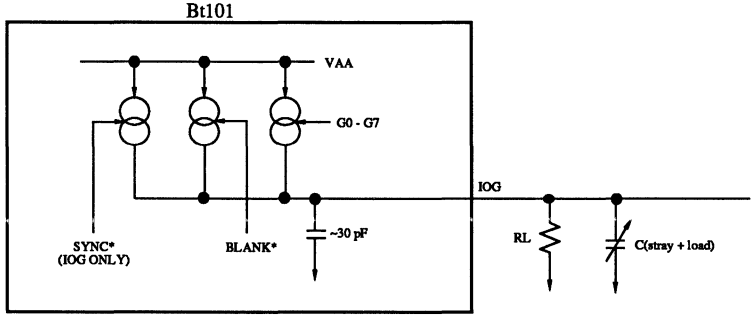


Figure 7. Equivalent Circuit of the Current Output (IOG).

Bt102

75 MHz

Monolithic CMOS

8-bit

VIDEODAC™

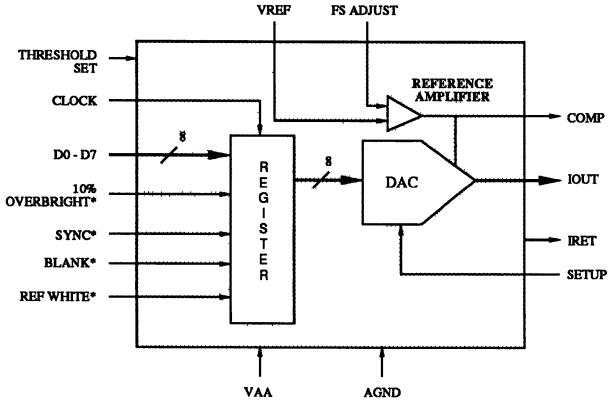
Distinguishing Features

- 75 MHz Pipelined Operation
- ± 1/4 LSB Differential Linearity Error
- ± 1/2 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- 0, 7, or 10 IRE Programmable Setup
- +5v CMOS Monolithic Construction
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 550 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Conventional D/A Applications

Functional Block Diagram



Product Description

The Bt102 is an 8-bit multi-function VIDEODAC, designed specifically for color graphics and conventional D/A converter applications.

Available control inputs include sync, blank, reference white, and 10% overbright. Additional features include a threshold set input to configure the digital inputs to be either TTL or CMOS compatible, and a setup input to specify one of three available setups in the analog output.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, reference white, and 10% overbright inputs are pipelined to maintain synchronization with the input data.

The Bt102 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1/4 LSB and ± 1/2 LSB, respectively, over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
(800) VIDEO IC
TLX: 383 596
FAX: (619) 452-1249
L102001 Rev. D

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt102 contains a single 8-bit D/A converter, input registers, and a reference amplifier.

The THRESHOLD SET input controls the logic thresholds of the digital inputs. If it is left floating, the logic thresholds are TTL compatible; if connected to VAA, the thresholds are CMOS compatible.

On the rising edge of each clock cycle, as shown below in Figure 1, eight bits of data (D0 - D7) are latched into the device and presented to the 8-bit D/A converter. The REF WHITE* input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF, regardless of the value of the D0 - D7 inputs.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC*, BLANK*, and 10% OVERBRIGHT* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs modify the output level.

The SETUP input is used to control the difference between the black and blanking level. Available setups include 10 IRE (SETUP = VAA), 7 IRE (SETUP = float), and 0 IRE (SETUP = AGND). A setup of 0 IRE specifies that the blanking level is the same as the black level.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. The VREF input requires an external 1.2v(typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt102 uses a segmented architecture in which bit currents are routed to either the output or IRET by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt102 is capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

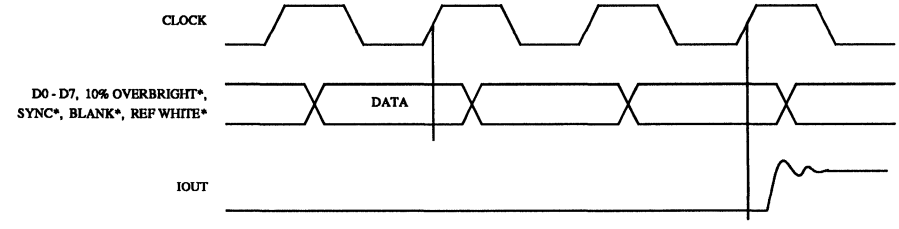
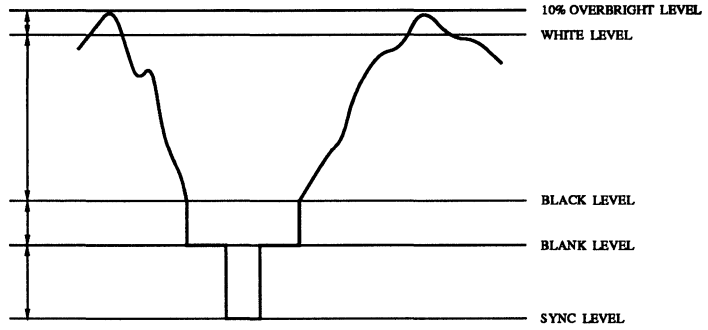


Figure 1. Input/Output Timing.

Circuit Description (continued)

RSET = 1130		RSET = 1110		RSET = 1050	
SETUP = VAA		SETUP = FLOAT		SETUP = AGND	
IRE	MA	IRE	MA	IRE	MA
9.5	28.90 27.01	10	28.74 26.81	10.75	29.00 26.97
90		92.9		100	
10	9.59 7.65	7.1	9.09 7.72	0	8.23 8.23
39.5		40.5		44	
	0.00		0.00		0.00



Note: 75-ohm doubly-terminated load, VREF = 1.235v. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	10% OVERBRIGHT*	REF WHITE*	SYNC*	BLANK*	DAC Input Data
WHITE +10%	28.74	0	1	1	1	$FF
WHITE	26.81	1	0	1	1	$xx
WHITE	26.81	1	1	1	1	$FF
DATA + 10%	data + 11.0	0	1	1	1	data
DATA	data + 9.09	1	1	1	1	data
DATA - SYNC	data + 1.37	1	1	0	1	data
BLACK	9.09	1	1	1	1	$00
BLACK - SYNC	1.37	1	1	0	1	$00
BLANK	7.72	x	x	1	0	$xx
SYNC	0	x	x	0	0	$xx

Note: Typical with white level current = 26.81 mA. RSET = 1110 ohms, VREF = 1.235v, SETUP = float.

Table 1. Video Output Truth Table.

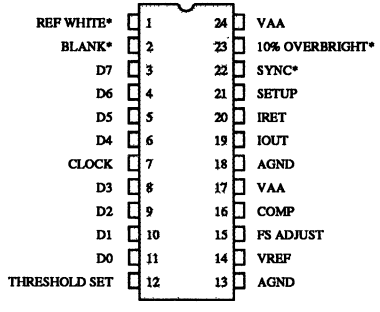
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL/CMOS compatible). A logical zero drives the output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0 - D7, REF WHITE*, and 10% OVERBRIGHT* inputs are ignored.
SYNC*	Composite sync control input (TTL/CMOS compatible). A logical zero on this input switches off a current source on the output equal to approximately 30% of the full scale current (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE*	Reference white control input (TTL/CMOS compatible). A logical zero on this input forces the output to the white level, regardless of the D0 - D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
10% OVERBRIGHT*	Overbright control input (TTL/CMOS compatible). A logical zero on this input causes the output current to increase by approximately 10 IRE units as shown in Table 1 and Figure 2. It is latched on the rising edge of CLOCK.
D0 - D7	Data inputs (TTL/CMOS compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL/CMOS compatible). The rising edge of CLOCK latches the D0 - D7, SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL or CMOS buffer.
SETUP	Setup control input. This pin controls the difference between the black level and the blanking level. Available setups include 10 IRE units (SETUP = VAA), 7 IRE units (SETUP = float), and 0 IRE units (SETUP = AGND).
THRESHOLD SET	Threshold control input. This pin controls the logic thresholds of the digital inputs. If connected to VAA through a 0.1 µF ceramic capacitor, the logic thresholds are TTL compatible. If connected directly to VAA, the thresholds are CMOS compatible.
IOUT	Current output. This high impedance current source is capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3).
IRET	Current return. This pin must be connected to AGND through a ferrite bead, as illustrated in Figure 3.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 3). Note that the IRE relationships in Figure 3 are maintained regardless of the full scale output current. The relationship between RSET and the white level output current is: RSET (ohms) = K1 * VREF (v) / IOUT (mA) The amount of additional current generated to achieve the overbright level is: IOUT (mA) = K2 * VREF (v) / RSET (ohms) K1 and K2 are defined as follows:

	SETUP		
	float	VAA	AGND
K1	24,096	24,713	22,930
K2	1,735	1,729	1,726



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt102 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt102 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt102.

The analog ground plane area should encompass all Bt102 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt102, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt102.

Power Planes

The Bt102 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt102.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt102 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt102 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt102 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt102 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

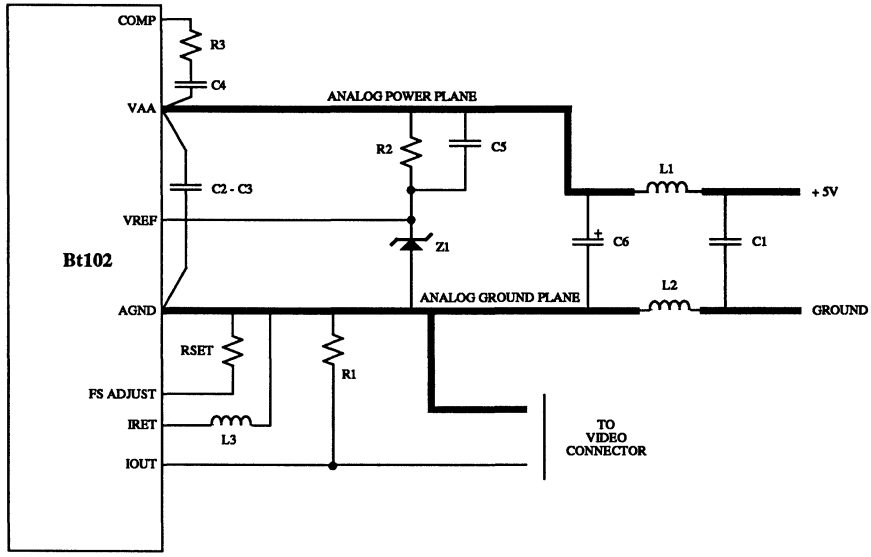
Analog Signal Interconnect

The Bt102 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog output should have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt102 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1	75-ohm 1% metal film resistor	Dale CMF-55C
R2	1000-ohm 1% metal film resistor	Dale CMF-55C
R3	27-ohm 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt102.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with the SETUP pin floating and an RSET value of about 1594 ohms. If the Bt102 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/(20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may always be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full scale output current is:

IOUT (mA) = K * VREF (v) / RSET (ohms)

where K is equal to 17,714; 17,158; or 15,933 for SETUP = VAA, float, and AGND, respectively.

Using Multiple Devices

If located close together on the same PC board, multiple Bt102 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt102 must still have it's individual RSET resistor, IOUT termination resistor (R1 in Figure 3), IRET ferrite bead (L3 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R3 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to the high current return.

Non-Video Applications

The Bt102 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero, while REF WHITE*, 10% OVERBRIGHT*, and BLANK* should be a logical one. SETUP should be connected to AGND. The output current will be determined solely by the D0 - D7 inputs.

The relationship between RSET and the full scale output current in this configuration is as follows:

RSET (ohms) = 15,933 * VREF (v) / IOUT (mA)

The BLANK* input may optionally be used as a "force to zero" control, and the REF WHITE* input may optionally be used as a "force to full scale" control.

COMP Resistor

To optimize the settling time of the Bt102, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 27 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	- 25		+ 85	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			± 1/2	LSB
Differential Linearity Error	DL			± 1/4	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
TTL Compatible Mode					
Input High Voltage	VIH				
CLOCK		3.0		VAA + 0.5	Volts
Other		2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH	- 200		- 1200	µA
Input Low Current (Vin = 0.4v)	IIL	- 200		- 1200	µA
Input Capacitance	CIN		10		pF
CMOS Compatible Mode					
Input High Voltage	VIH	3.5		AGND + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 3.5v)	IIH			2	µA
Input Low Current (Vin = 1.5v)	IIL			2	µA
Input Capacitance	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20.5	mA
Output Current					
Overbright Relative to White		1.60	1.93	2.40	mA
White Level Relative to Blank		17.90	19.09	20.31	mA
White Level Relative to Black		16.80	17.72	18.61	mA
Black Level Relative to Blank					
SETUP = float		1.10	1.37	1.70	mA
SETUP = AGND		0	5	50	µA
SETUP = VAA		1.6	1.93	2.4	mA
Blanking Level		7.2	7.72	8.3	mA
Sync Level		0	5	50	µA
LSB Size			69.5		µA
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	ROUT		33		K ohms
Output Capacitance	COUT		20		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with SETUP = float, RSET = 1110 ohms, VREF = 1.235v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			75	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	4 1			ns ns
Clock Cycle Time Clock Pulse Width Low Clock Pulse Width High	TCYC TCLKH TCLKL	13.33 5 6			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time* to ± 1/2 LSB to ± 1 LSB Clock and Data Feedthrough* Glitch Impulse*	TDLY TVRF TS		20 6 15 12 - 20 100		ns ns ns ns dB pV - sec
Differential Gain Error Differential Phase Error	DG DP		1 1		% Gray Scale Degree
Pipeline Delay		3	3	3	Clocks
VAA Supply Current**	IAA		110	175	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1110 ohms, VREF = 1.235v. THRESHOLD SET = TTL mode, SETUP = float. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 27 ohms. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

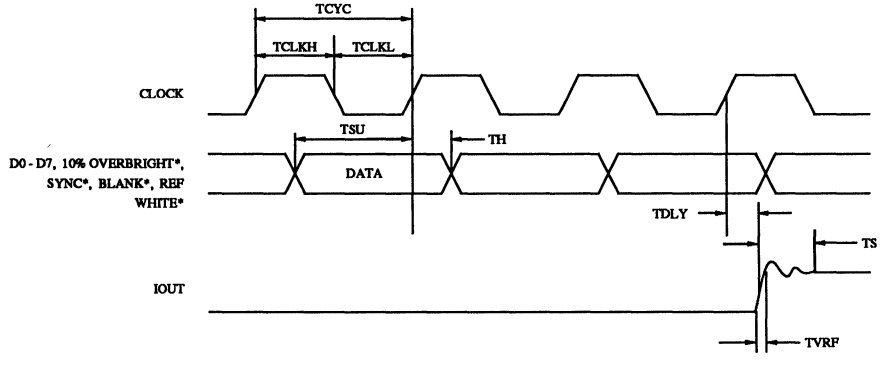
*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 150 MHz.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt102BC	75 MHz	24-pin 0.3" CERDIP	-25° to +85° C.
Bt102EVM	Evaluation Board for the Bt102		

Timing Waveforms



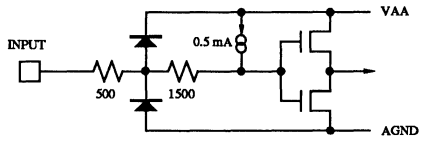
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB or ± 1 LSB.

Note 3: Output rise/fall time measured between the 20% and 80% points of full scale transition.

Figure 4. Input/Output Timing.

Device Circuit Data



High speed operation is accomplished through pipelining and a unique (patent pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

The 0.5 mA bias current is disabled when THRESHOLD SET is connected to VAA, resulting in a standard high-impedance CMOS input.

Figure 5. Equivalent Circuit of the Digital Inputs.

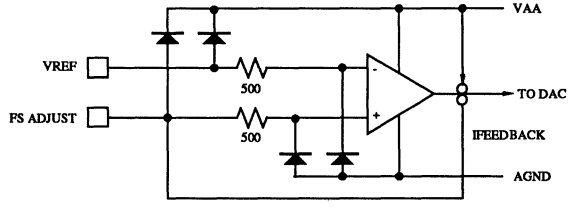


Figure 6. Equivalent Circuit of the Reference Amplifier.

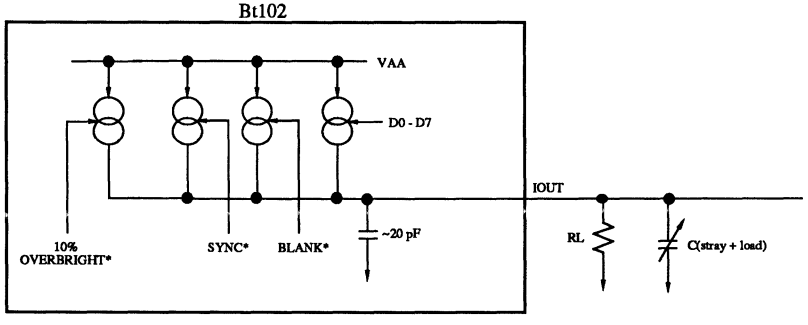


Figure 7. Equivalent Circuit of the Current Output.

Bt103

75 MHz

Monolithic CMOS

Triple 4-bit

VIDEODAC™

Distinguishing Features

- 75, 30 MHz Operation
- Triple 4-bit D/A Converters
- ± 1/16 LSB Differential Linearity Error
- ± 1/8 LSB Differential Linearity Error
- RS-343A/RS-170 Compatible Outputs
- TTL Compatible Inputs
- +5v CMOS Monolithic Construction
- 28-pin DIP Package
- Typical Power Dissipation: 800 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

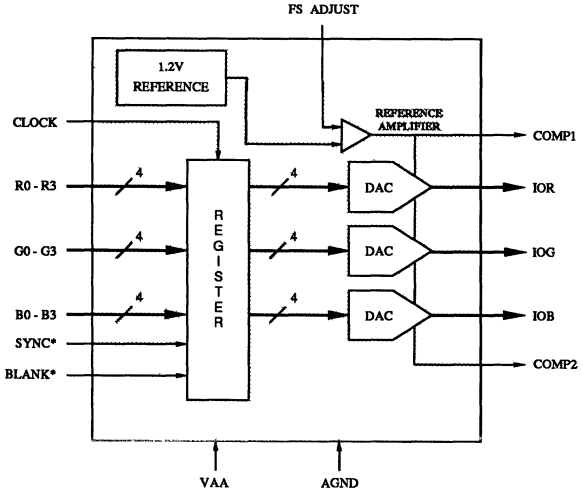
Product Description

The Bt103 is a triple 4-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync and blank, both pipelined to maintain synchronization with the color data. An on-chip voltage reference simplifies design, and a single external resistor controls the full scale output current.

The Bt103 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1/16 LSB and ± 1/8 LSB, respectively, over the full temperature range.

Functional Block Diagram



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L103001 Rev. D

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt103 contains three 4-bit D/A converters, input registers, voltage reference, and a reference amplifier.

As shown below in Figure 1, on the rising edge of each clock cycle, 12 bits of color information (R0 - R3, G0 - G3, and B0 - B3) are latched into the device and presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK and pipelined to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 499 ohms for generation of RS-343A video into a 37.5-ohm load.

The D/A converters on the Bt103 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt103 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

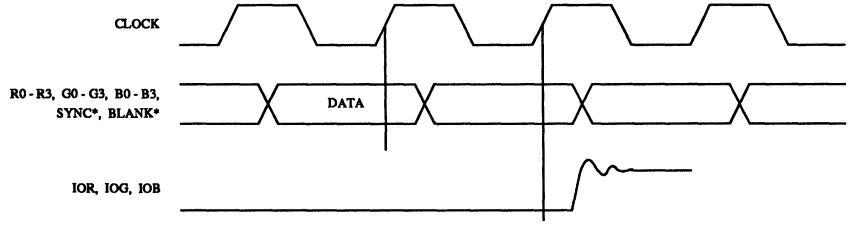
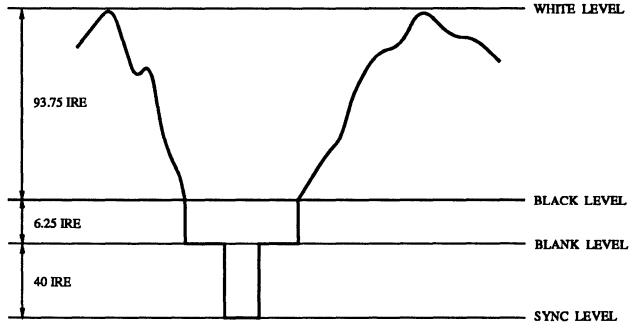


Figure 1. Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.19	0.045	8.81	0.330
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 499 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR (mA)	IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	19.05	1	1	$F
DATA	data + 8.81	data + 1.19	data + 1.19	1	1	data
DATA - SYNC	data+ 1.19	data + 1.19	data + 1.19	0	1	data
BLACK	8.81	1.19	1.19	1	1	$0
BLACK - SYNC	1.19	1.19	1.19	0	1	$0
BLANK	7.62	0	0	1	0	$x
SYNC	0	0	0	0	0	$x

Note: Typical with full scale IOG = 26.67 mA. RSET = 499 ohms.

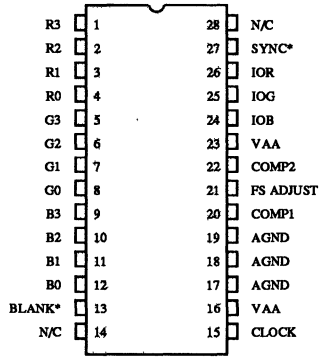
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0 - R3, G0 - G3, and B0 - B3 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0 - R3, G0 - G3, B0 - B3	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0 - R3, G0 - G3, B0 - B3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = 13,308 / IOG (mA) The full scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 9,506 / RSET (ohms)

Pin Descriptions (continued)

Pin Name	Description
COMP1, COMP2	Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins (Figure 3). The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.



Note: N/C pins may be left floating without affecting the performance of the Bt103.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt103 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt103 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt103.

The analog ground plane area should encompass all Bt103 ground pins, power supply bypass circuitry for the Bt103, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt103.

Power Planes

The Bt103 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt103.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt103 power pins and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt103 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt103 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt103 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

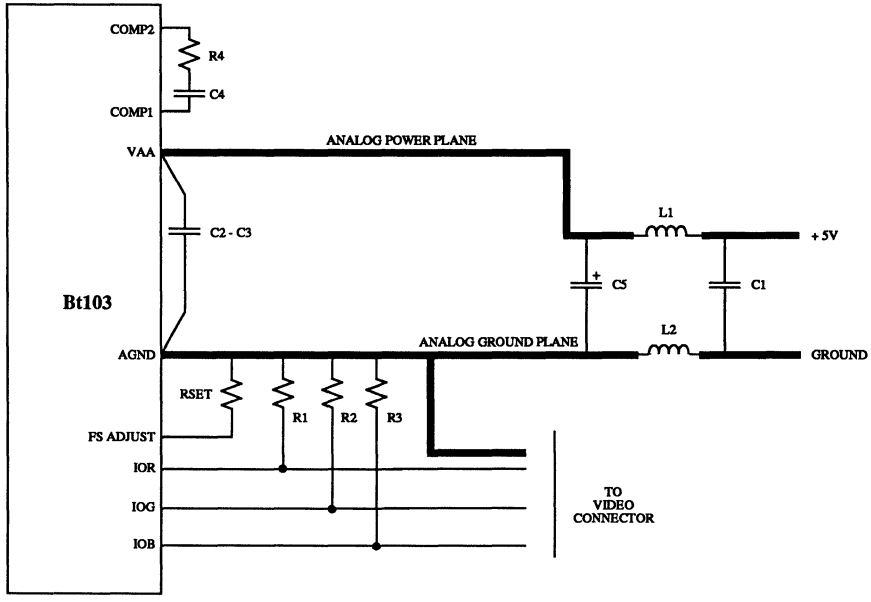
Analog Signal Interconnect

The Bt103 should be located as close as possible to the output connectors to minimize noise pickup, and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt103 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2, C3, C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	22-ohm 1% metal film resistor	Dale CMF-55C
RSET	499-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt103.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with an RSET value of about 713 ohms. If the Bt103 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/ (20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

COMP Resistor

To optimize the settling time of the Bt103, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 22 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt103 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero and BLANK* should be a logical one. All three outputs will have the same full scale output current.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 8,912 / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 594 / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt103KC30		0		+ 70	°C.
Bt103BC		- 25		+ 85	°C.
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		499		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1/8	LSB
Differential Linearity Error	DL			± 1/16	LSB
Gray Scale Error				± 10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH	- 200		- 1200	µA
Input Low Current (Vin = 0.4v)	IIL	- 200		- 1200	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		16.88	19.05	20.69	mA
White Level Relative to Black		15.86	17.62	19.38	mA
Black Level Relative to Blank		1.02	1.19	1.31	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			1.175		mA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		20		pF
Internal Voltage Reference	VREF		1.2		Volts
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 ohms. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		75 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			75			30	MHz
Data and Control Setup Time	TSU	4			10			ns
Data and Control Hold Time	TH	1			2			ns
Clock Cycle Time	TCYC	13.3			33.3			ns
Clock Pulse Width High Time	TCLKH	5			10			ns
Clock Pulse Width Low Time	TCLKL	5			10			ns
Analog Output Delay	TDLY		12			12		ns
Analog Output Rise/Fall Time	TVRF			4			9	ns
Analog Output Settling Time*	TS		12			15		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			50			50		pV - sec
DAC to DAC Crosstalk			- 25			- 25		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		2	2	2	2	2	2	Clocks
VAA Supply Current**	IAA			175			110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 ohms. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 22 ohms. Output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

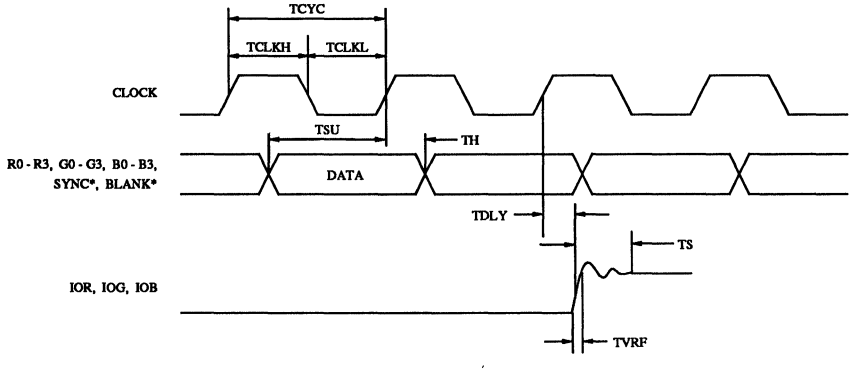
*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt103BC	75 MHz	28-pin 0.6" CERDIP	-25° to +85° C.
Bt103KC30	30 MHz	28-pin 0.6" CERDIP	0° to +70° C.
Bt103EVM	Evaluation Board for the Bt103		

Timing Waveforms



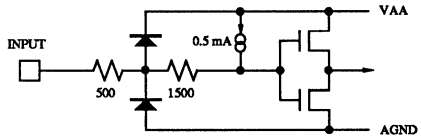
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/8 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

Device Circuit Data



High speed operation is accomplished through pipelining and a unique (patent pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

Figure 5. Equivalent Circuit of the Digital Inputs.

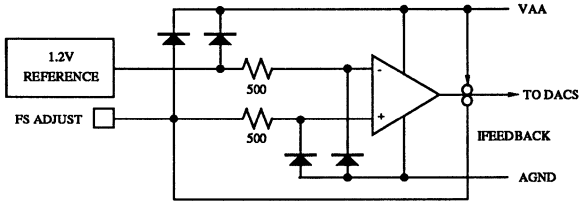


Figure 6. Equivalent Circuit of the Reference Amplifier.

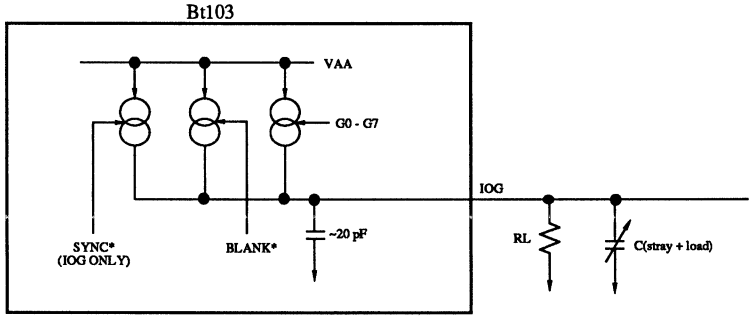


Figure 7. Equivalent Circuit of the Current Output (IOG).

Bt106

50 MHz

Monolithic CMOS

8-bit

VIDEODAC™

Distinguishing Features

- 50, 30 MHz Operation
- ± 1 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- TTL Compatible Inputs
- +5v CMOS Monolithic Construction
- 20-pin DIP Package
- Typical Power Dissipation: 400 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

Product Description

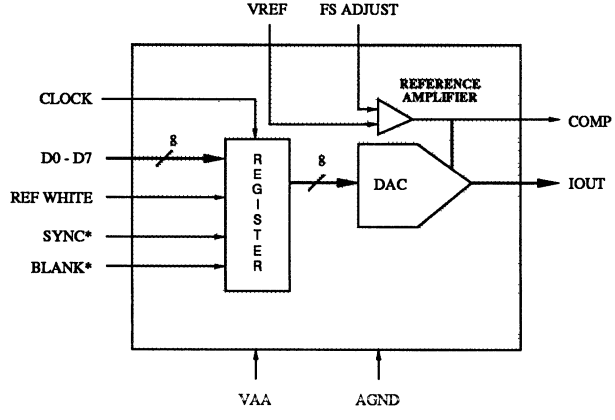
The Bt106 is an 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog output to the reference white level, regardless of the data inputs.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt106 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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San Diego, CA 92121
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FAX: (619) 452-1249
L106001 Rev. F

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt106 contains an 8-bit D/A converter, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, eight bits of data are latched into the device and presented to the 8-bit D/A converter. The REF WHITE input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog output, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output level.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 ohms for generation of RS-343A video into a 37.5-ohm load. The VREF input requires an external 1.2v (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt106 uses a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt106 is capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

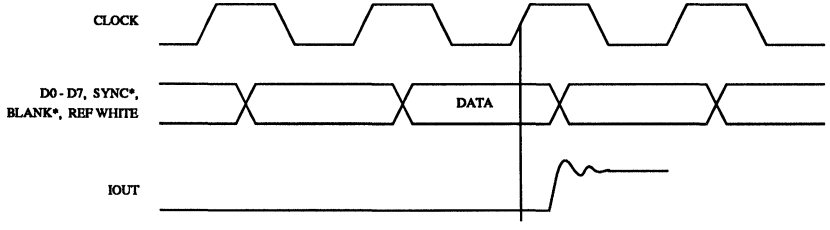
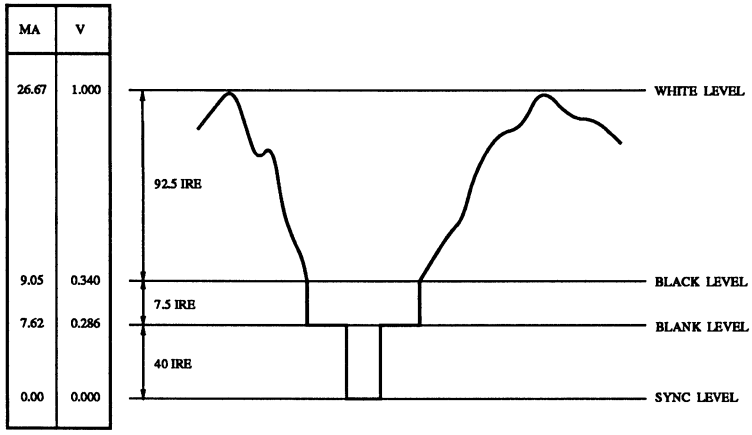


Figure 1. Input/Output Timing.

Circuit Description (continued)



Note: 75-ohm doubly-terminated load, RSET = 542 ohms, VREF = 1.2v. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	1	$xx
WHITE	26.67	0	1	1	$FF
DATA	data + 9.05	0	1	1	data
DATA - SYNC	data + 1.44	0	0	1	data
BLACK	9.05	0	1	1	$00
BLACK - SYNC	1.44	0	0	1	$00
BLANK	7.62	x	1	0	$xx
SYNC	0	x	0	0	$xx

Note: Typical with full scale IOUT = 26.67 mA. RSET = 542 ohms, VREF = 1.2v.

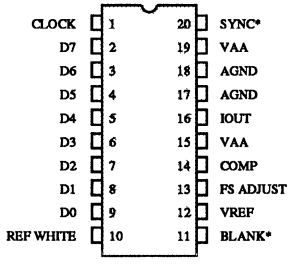
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOUT output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0 - D7 and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the output to the white level, regardless of the D0 - D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
D0 - D7	Data inputs (TTL compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the D0 - D7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer.
IOUT	Current output. This high impedance current source is capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3).
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current is: RSET (ohms) = 12,046 * VREF (v) / IOUT (mA)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The Bt106 has an internal pull-up resistor between VAA and VREF. As the value of this resistor may vary slightly due to process variations, the use of a resistor network to generate the reference is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt106 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt106 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt106.

The analog ground plane area should encompass all Bt106 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt106, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt106.

Power Planes

The Bt106 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt106.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt106 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt106 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt106 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt106 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

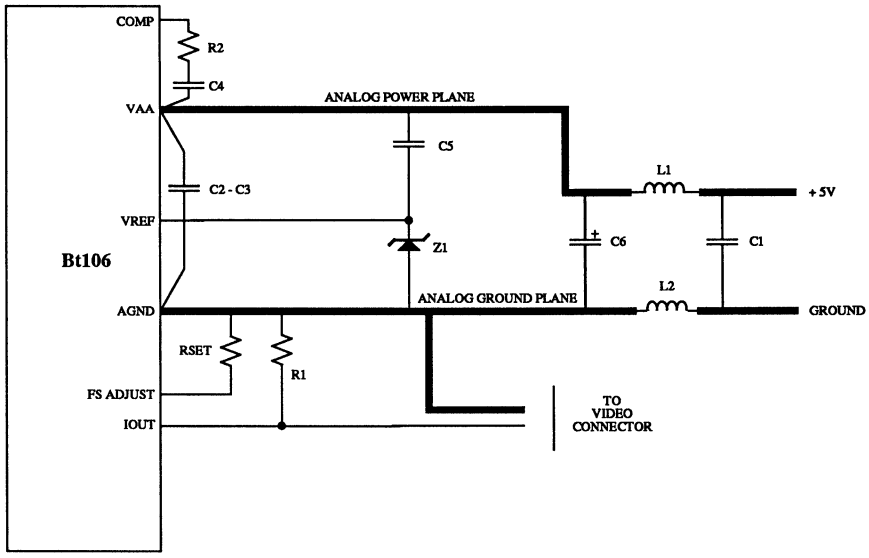
Analog Signal Interconnect

The Bt106 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog output should have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt106 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	75-ohm 1% metal film resistor	Dale CMF-55C
R2	12-ohm 1% metal film resistor	Dale CMF-55C
RSET	549-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt106.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with an RSET value of about 774 ohms. If the Bt106 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/ (20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full scale output current is:

IOUT (mA) = 8,604 * VREF (v) / RSET (ohms)

Using Multiple Devices

If located close together on the same PC board, multiple Bt106 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt106 must still have it's individual RSET resistor, IOUT termination resistor (R1 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R2 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to high current return.

Non-Video Applications

The Bt106 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,958 * VREF (v) / IOUT (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (v) / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full scale" control.

COMP Resistor

To optimize the settling time of the Bt106, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 12 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt106KC30		0		+ 70	°C.
Bt106BC		- 25		+ 85	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		50 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	8 2			8 2			ns ns
Clock Cycle Time Clock Pulse Width High Time Clock Pulse Width Low Time	TCYC TCLKH TCLKL	20 8 8			33.3 10 10			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time* Clock and Data Feedthrough* Glitch Impulse*	TDLY TVRF TS		25 20 - 33 50	8		25 25 - 33 50	9	ns ns ns dB pV - sec
Differential Gain Error Differential Phase Error	DG DP		1.8 1.2			1.8 1.2		% Gray Scale Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current**	IAA		80	100		60	75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. COMP resistor = 12 ohms. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

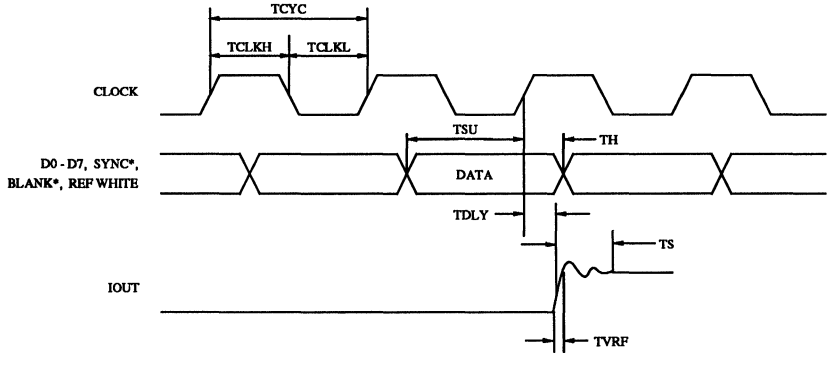
*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt106BC	50 MHz	20-pin 0.3" CERDIP	-25° to +85° C.
Bt106KC30	30 MHz	20-pin 0.3" CERDIP	0° to +70° C.
Bt106EVM	Evaluation Board for the Bt106		

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

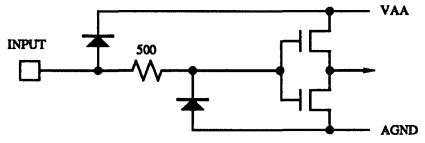


Figure 5. Equivalent Circuit of the Digital Inputs.

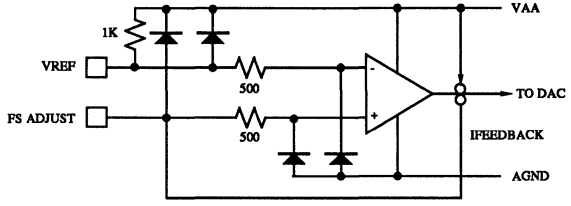


Figure 6. Equivalent Circuit of the Reference Amplifier.

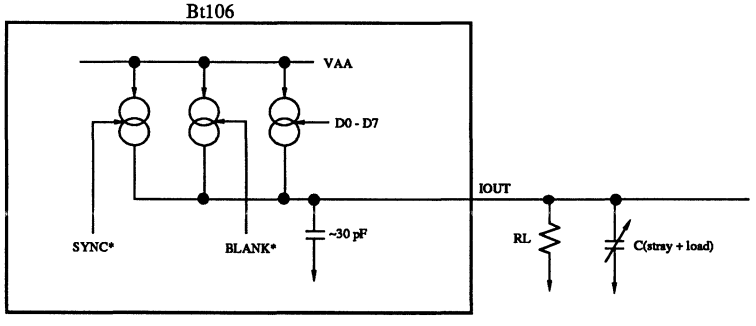


Figure 7. Equivalent Circuit of the Current Output.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt107

400 MHz

10KH/100K ECL

8-bit Multiplexed Input

VIDEODAC™

Distinguishing Features

- 400 MHz Pipelined Operation
- ± 1/2 LSB Differential Linearity Error
- ± 1/2 LSB Integral Linearity Error
- 500 ps Typical Rise/Fall Time
- RS-343A Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- Handles 25-Ohm Output Loads
- 10KH and 100K ECL Compatible I/O
- 2:1 Multiplexed Pixel Inputs
- 32-pin Flatpack Package
- Typical Power Dissipation: 1 W

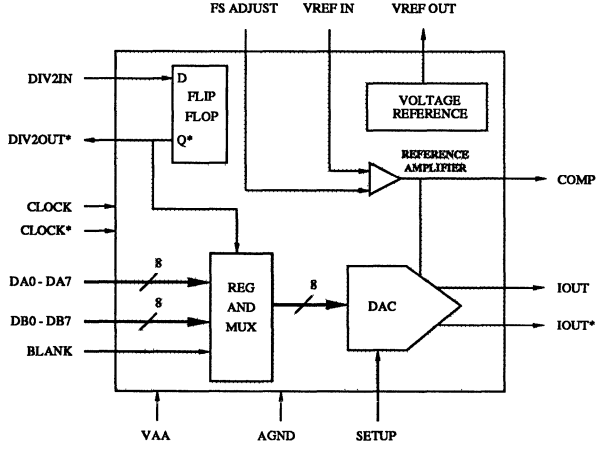
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Radar Processing
- Instrumentation

Related Products

- Bt424, Bt492

Functional Block Diagram



Product Description

The Bt107 is an 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Multiplexed pixel inputs enable pixel data to be latched into the Bt107 at a 200 MHz data rate, while maintaining the 400 MHz output rate necessary for high resolution graphics. On-chip circuitry divides the pixel clock by two, generating the 200 MHz clock signal.

An on-chip voltage reference is available or an external reference may be used. A single external resistor controls the full scale output current.

The Bt107 generates an RS-343A compatible video signal, and is capable of driving either doubly-terminated 75-ohm or 50-ohm coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1/2 LSB over the full temperature range.

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Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt107 contains a single 8-bit D/A converter, 2:1 multiplexed input register, a voltage reference, and a reference amplifier.

Pixel data on the DA0 - DA7 (even data) and DB0- DB7 (odd data) are latched on the falling edge of DIV2OUT*, as illustrated in Figure 1.

DIV2IN is defined to be 1/2 the CLOCK rate. To simplify system design, the Bt107 outputs a DIV2OUT* signal, which when connected to the DIV2IN pin, generates a clock equal to 1/2 the CLOCK rate. For a color system requiring three Bt107s, the DIV2OUT* signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Care should be taken to keep signal paths short and equal for each connection. The unused DIV2OUT* signals from the remaining Bt107s can be used to clock external lookup table RAMs.

The BLANK input is also latched on the falling edge of DIV2OUT*, and overrides the DA0 - DA7 and DB0 - DB7 data. Blanking information is output synchronously with the even pixel data.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1092 ohms for generation of RS-343A video into a 37.5-ohm load, or 729 ohms for generation of RS-343A video into a 25-ohm load. The on-chip voltage reference(VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt107s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25-ohm resistor to AGND(assuming a doubly-terminated 50-ohm load). The IOUT* output is used to generate the video signal.

The D/A converter on the Bt107 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt107 are capable of directly driving either a 37.5-ohm or 25-ohm load, such as a doubly-terminated 75-ohm or 50-ohm coaxial cable.

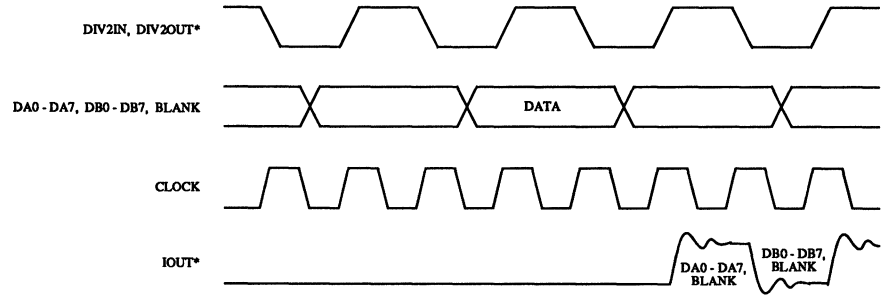
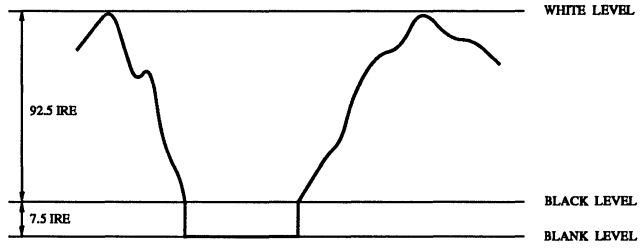


Figure 1. Input/Output Timing (DIV2IN connected to DIV2OUT).*

Circuit Description (continued)

MA RSET = 729	MA RSET = 1092	V
00.00	00.00	0.000
- 26.40	- 17.60	- 0.660
- 28.56	- 19.05	- 0.714



Note: RSET = 729 ohms (50-ohm doubly-terminated load) or 1092 ohms (75-ohm doubly-terminated load), VREF IN = -1.21v. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform (IOUT).*

Description	RSET = 729 ohms IOUT* (mA)	RSET = 1092 ohms IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	- 26.40	- 17.62	0	$00
BLANK			1	$xx
SETUP = AGND	- 26.40	- 17.62		
SETUP = float	- 28.56	- 19.05		

Note: Typical with VREF IN = -1.21v.

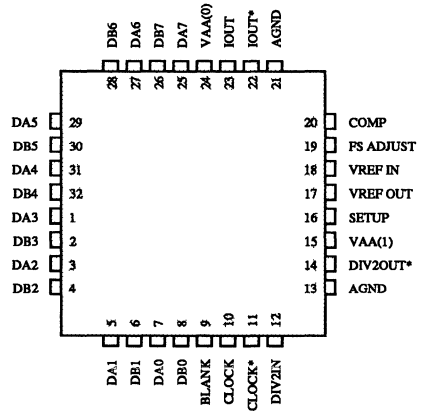
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logic one drives the analog output to the blanking level, as illustrated in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the DA0 - DA7 and DB0 - DB7 inputs are ignored. Blanking information is output synchronously with the even pixel data.
DA0 - DA7, DB0 - DB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT*. Even data represents the first (leftmost) pixel on the display screen. DAx represent the even pixel data, and DBx represent the odd pixel data. Coding is binary.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). It is typically the pixel clock rate of the video system. The Bt107 may be operated with a single-ended clock by connecting CLOCK* to a -1.3v VBB, however, common mode noise immunity at high clock rates may degrade.
DIV2IN	CLOCK/2 input (ECL compatible). This clock must be 1/2 the CLOCK rate. It is used to latch the BLANK, DAx and DBx inputs. See Figure 1.
DIV2OUT*	CLOCK/2 output (ECL compatible). When connected to the DIV2IN pin, this output is 1/2 the CLOCK rate. When not connected to DIV2IN, it generates a signal that is DIV2IN synchronized to CLOCK and inverted. DIV2OUT* must be terminated to -2v.
IOUT, IOUT*	Differential video current outputs. These high impedance current sources are capable of directly driving either a doubly-terminated 50-ohm or 75-ohm coaxial cable (Figure 3). Both outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. **Warning: It is important that a ferrite bead be used to connect the VAA(1) power pin to the analog power plane as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA(1) pin will result in unstable operation.**
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.
SETUP	Pedestal control input. If connected to AGND, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If left floating, the 7.5 IRE blanking pedestal is enabled. See Figure 2.

Pin Descriptions (continued)

Pin Name	Description
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current is: RSET (ohms) = K * VREF IN (v) / IOUT (mA) where K = 17,205 if SETUP = float or 15,915 if SETUP = AGND. Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing and depending on whether the internal or an external reference is used.
VREF OUT	Voltage reference output. This output provides a -1.2v (typical) reference, and may be connected to the VREF IN inputs of up to three Bt107s. When driving multiple Bt107s, use 100-ohm interconnect resistance to minimize noise pick-up. If it is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 4, or the VREF OUT pin must supply this input with a -1.2v (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and VAA(0), as shown in Figure 3. The decoupling capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt107 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt107 and any associated analog circuitry should have it's own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt107.

The analog ground plane area should encompass all Bt107 ground pins, power supply bypass circuitry for the Bt107, any external voltage reference circuitry, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt107.

Power Planes

The Bt107 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt107.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt107 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation due to high-frequency oscillations.

Digital Signal Interconnect

The digital inputs to the Bt107 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

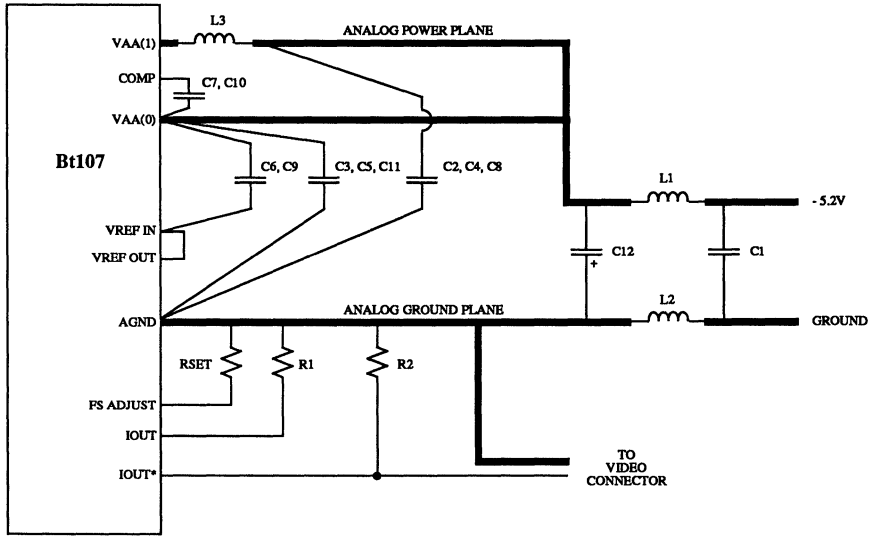
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4 - C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8 - C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1	24.9-ohm 1% metal film resistor	Dale CMF-55C
R2	49.9-ohm 1% metal film resistor	Dale CMF-55C
RSET	732-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt107. R1, R2, and RSET values assume doubly-terminated 50-ohm load on IOUT*.

Figure 3. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Terminated Inputs

All digital inputs of the Bt107 should be terminated using normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical zero state.

External Voltage Reference

An external voltage reference may be used with the Bt107, as shown in Figure 4. In this instance, the VREF OUT pin should be left floating.

Note that the VREF IN pin still requires bypass capacitors to VAA(0) (C6 and C9 in Figure 3).

Package Heatsink

The stud heatsink is electrically isolated and should be connected to AGND for minimal noise.

Using Multiple Bt107s

For color applications, three Bt107s may be used, as illustrated in Figure 5. This example generates 256 simultaneous colors from a 16.8 million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers and color palette RAM (Bt404s are used in this illustration). The Bt502s interface the color palette RAM to the TTL compatible MPU bus. If more than 256 colors are desired, additional Bt404s may be wired in parallel to expand each color palette RAM to 1024 x 8.

Note the DIV2OUT* - DIV2IN connections, generating CLOCK*/2 and ensuring the three Bt107s operate in a synchronous fashion. When analyzing the timing window for DIV2IN, be sure to include the propagation delay of the CLOCK and DIV2OUT* signals through the transmission lines of the physical layout on the PC board.

When DIV2OUT is to be used for system CLOCK, it is recommended that DIV2OUT* be buffered before distribution to the rest of the system to allow for adequate noise margins.

The Bt107s may share the voltage reference and analog power/ground planes, but each Bt107 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, VAA(1) ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2* line length. Low E stripline is recommended, and the propagation delays between CLOCK and DIV2* should match as closely as possible.

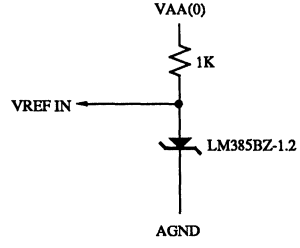


Figure 4. External Voltage Reference.

Application Information (continued)

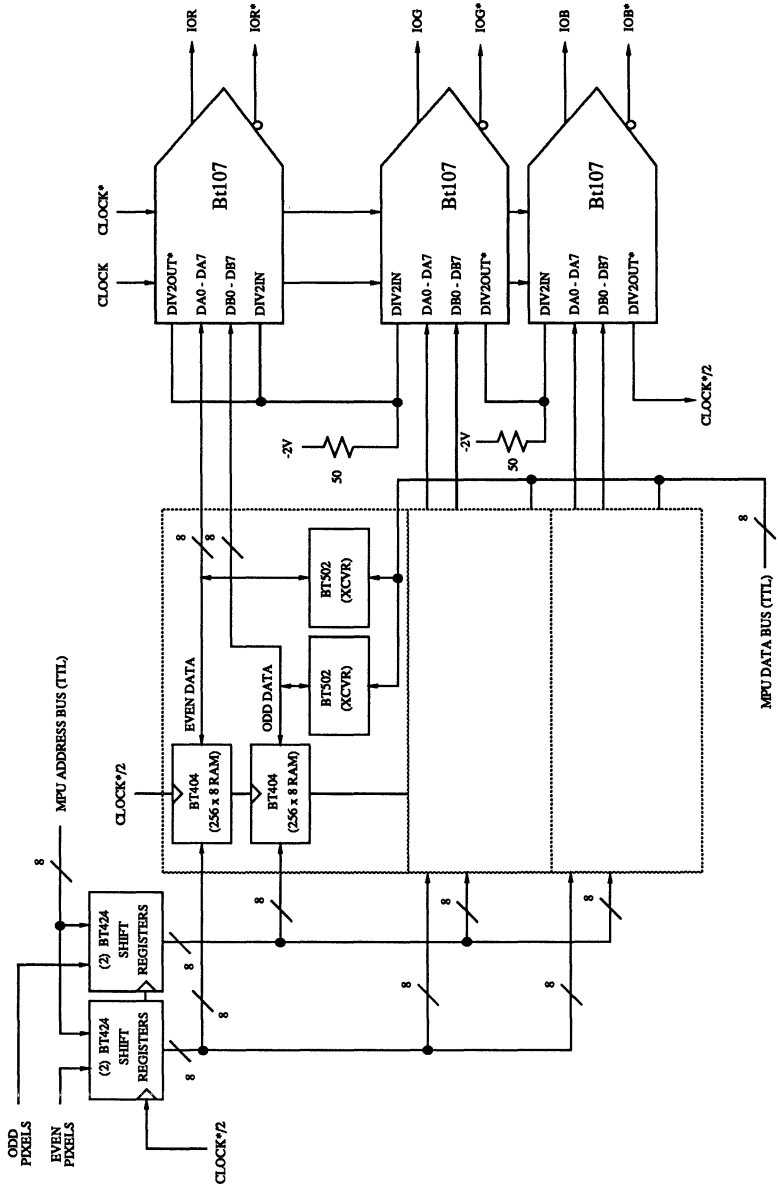


Figure 5. Using Multiple Bt107s.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	- 4.2	- 5.2	- 5.5	Volts
Ambient Operating Temperature	TA	- 25		+ 85	°C.
Output Load	RL		25		Ohms
Reference Voltage	VREF IN	- 1.13	- 1.2	- 1.3	Volts
FS ADJUST Resistor	RSET		729		Ohms

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			- 6.5	Volts
Voltage on any Digital Pin		AGND + 0.5		VAA - 0.5	Volts
Analog Output Short Circuit Duration to any Common			indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Vapor Phase Soldering (1 minutes)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			± 1/2	LSB
Differential Linearity Error	DL			± 1/2	LSB
Gray Scale Error					
Using Internal Reference				± 10	% Gray Scale
Using External Reference				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	- 1160		- 710	mV
Input Low Voltage	VIL	- 1870		- 1480	mV
Input High Current	IIH				
(Vin = VIHmax)					
Data				30	µA
All Other Inputs				150	µA
Input Low Current	IIL				
(Vin = VILmin)					
Blank				150	µA
All Other Inputs				5	µA
Input Capacitance	CIN			10	pF
(f = 1 MHz, Vin = VIHmax)					
Digital Output					
Output High Voltage	VOH	- 1060	- 955	- 880	mV
Output Low Voltage	VOL	- 1810	- 1705	- 1620	mV
Analog Output					
Gray Scale Current Range				- 40	mA
Output Current					
White Level		0	- 5	- 50	µA
Black Level Relative to White		- 25.08	- 26.40	- 27.72	mA
Blank Level Relative to Black					
SETUP = AGND		0	0	0	mA
SETUP = float		- 2.05	- 2.16	- 2.28	mA
LSB Size			- 103.5		µA
Output Compliance	VOC	- 1.2		+ 1.5	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance	COUT		9		pF
(f = 1 MHz, IOUT = 0 mA)					
Reference Input Current	IREF IN			10	µA
Reference Output Voltage	VREF OUT	- 1.14	- 1.22	- 1.3	Volts
Reference Output Current	IREF OUT	- 200			µA
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 KHz)	PSRR		0.03	0.5	%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -28.56 mA full scale output current, VREF IN = -1.21v, SETUP = float. All digital inputs have 50 ohms to -2.0v. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			400	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	1 0			ns ns
Clock Cycle Time Clock Pulse Width High Clock Pulse Width Low	TCYC TCLKH TCLKL	2.5 1 1			ns ns ns
DIV2OUT Delay*** DIV2IN Setup Time DIV2IN Hold Time	DDLY DSU DH	1.5 0 1		2.2	ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time Clock and Data Feedthrough* Glitch Impulse* Non-Harmonic Spurious	TDLY TVRF TS		 350 tbd 10 - 45	2 700 2	ns ps ns dB LSB - ns dBc
Pipeline Delay		2	2	2	Clocks
VAA Supply Current**	IAA			225	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -28.56 mA full scale output current, VREF IN = -1.21v, SETUP = float. ECL input values are -0.95 to -1.69 volts, with input rise/fall times ≤ 1 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. All digital inputs have 50 ohms to -2.0v, unless other specified. Analog output load ≤ 10 pF. See timing notes in Figure 6.

*Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 800 MHz.

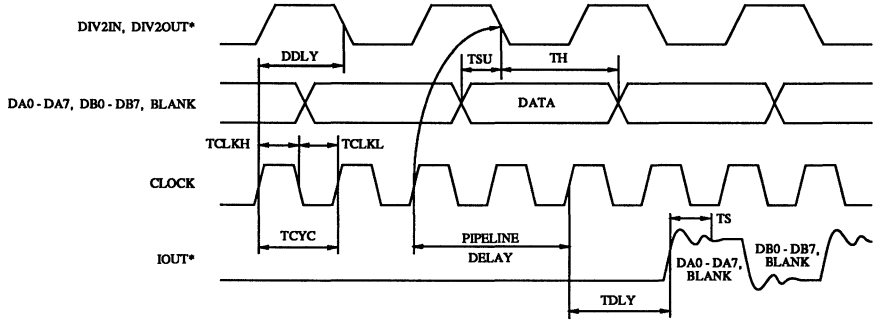
**At Fmax. IAA (typ) at VAA = -4.5v. IAA (max) at VAA = -5.5v.

***Tested with one ECL load.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt107BF400	400 MHz	32-pin Ceramic Flatpack w/heatsink	-25° to +85° C.

Timing Waveforms



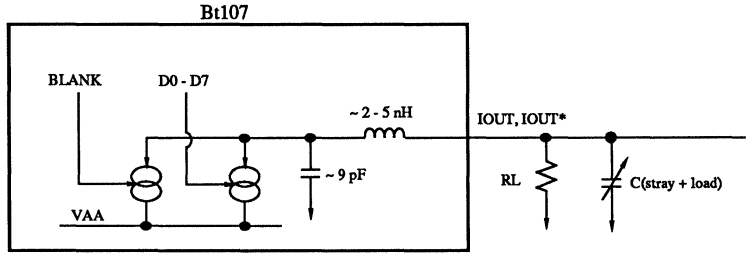
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Input/Output Timing (DIV2IN connected to DIV2OUT).*

Device Circuit Data



The output network of the Bt107 may be modeled as a three pole low pass filter. Settling time is tested on a sample basis with C(stray + load) tuned for optimum performance.

Figure 7. Equivalent Output Circuit of the Bt107.

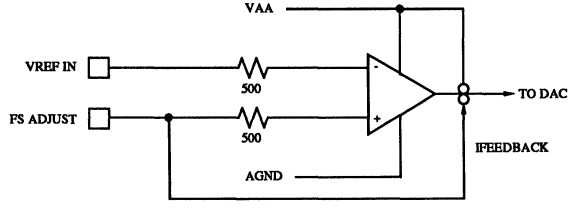


Figure 8. Equivalent Circuit of the Reference Amplifier.

Bt109

250 MHz

10KH ECL

Triple 8-bit

VIDEODAC™

Distinguishing Features

- 250 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- ± 1/2 LSB Differential Linearity Error
- ± 1/2 LSB Integral Linearity Error
- 350 ps Typical Rise/Fall Time
- RS-343A Compatible Outputs
- 10KH ECL Compatible Inputs
- 40-pin DIP Package
- Pin Compatible with TDC1318
- Typical Power Dissipation: 2 W

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt424
- Bt468

Product Description

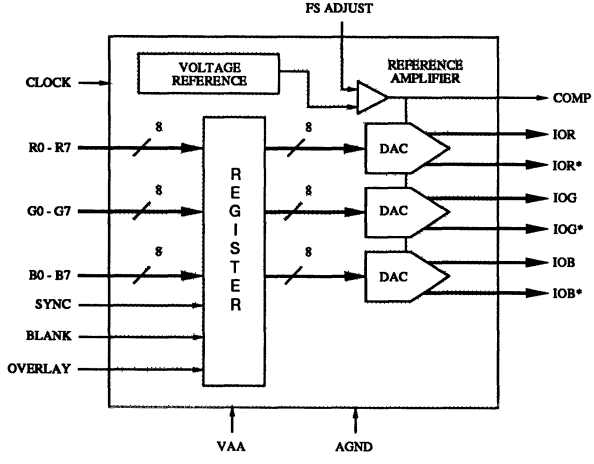
The Bt109 is a triple 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync, blank, and overlay, all registered to maintain synchronization with the pixel data.

An internal 1.2v voltage reference and a single external resistor control the full scale output current.

The Bt109 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1/2 LSB over the full temperature range.

Functional Block Diagram



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Circuit Description

As illustrated in the functional block diagram, the Bt109 contains three 8-bit D/A converters, input registers, a voltage reference, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0 - R7, G0 - G7, and B0 - B7) are latched into the device and presented to the three 8-bit D/A converters.

The OVERLAY input, also latched on the rising edge of CLOCK, forces the analog outputs to the overlay level, regardless of the data inputs. This also permits blanking of the IOUT* outputs for analog summing.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC and BLANK inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC, BLANK, and OVERLAY inputs modify the output levels.

The full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1100 ohms for generation of RS-343A video into a 37.5-ohm load.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOR, IOG, and IOB outputs through 37.5-ohm resistors to AGND (assuming IOR*, IOG*, and IOB* are driving a doubly-terminated 75-ohm load). The IOR*, IOG*, and IOB* outputs are then used to generate the video signals.

The D/A converters on the Bt109 use a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt109 are capable of directly driving a doubly-terminated 75-ohm coaxial cable or a singly-terminated 50-ohm coaxial cable.

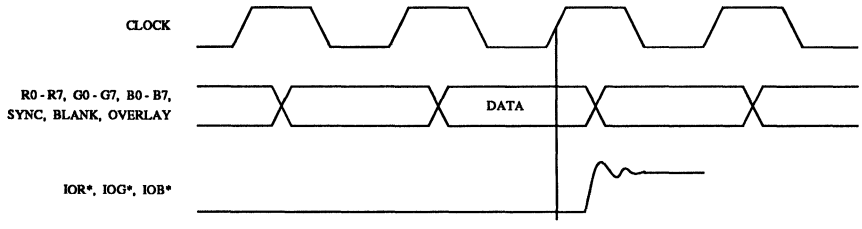
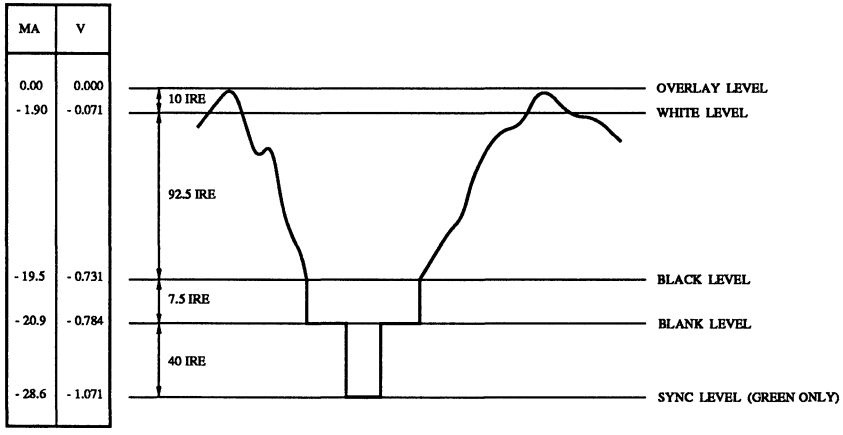


Figure 1. Input/Output Timing.

Circuit Description (continued)



Note: 75-ohm doubly-terminated load, RSET = 1100 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG* (mA)	IOR*, IOB* (mA)	OVERLAY	SYNC	BLANK	DAC Input Data
OVERLAY	0	0	1	0	0	$xx
WHITE	- 1.90	- 1.90	0	0	0	$FF
DATA	data - 1.90	data - 1.90	0	0	0	data
BLACK	- 19.50	- 19.50	0	0	0	$00
BLANK	- 20.90	- 20.90	x	0	1	$xx
SYNC	- 28.60	- 20.90	x	1	1	$xx

Note: Typical with full scale IOG* = -28.60 mA. RSET = 1100 ohms. Note that SYNC does not override data, as with the TDC1318.

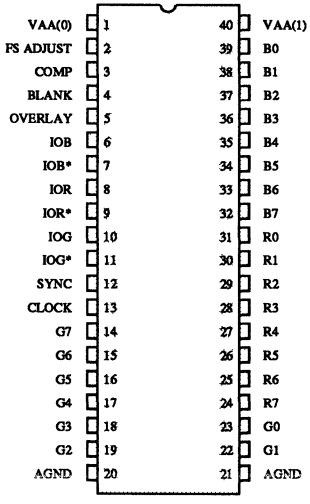
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logical one on this input drives the analog outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK is a logical one, the data and OVERLAY inputs are ignored.
SYNC	Composite sync control input (ECL compatible). A logical one on this input switches on a 40 IRE current source on the green output (see Figure 2). SYNC does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
OVERLAY	Overlay control input (ECL compatible). A logical one on this input overrides the data inputs and forces the analog outputs to the overlay level. It is latched on the rising edge of CLOCK.
R0 - R7, G0 - G7, B0 - B7	Red, green, and blue data inputs (ECL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (ECL compatible). The rising edge of CLOCK latches the R0 - R7, G0 - G7, B0 - B7, SYNC, BLANK, and OVERLAY inputs. It is typically the pixel clock rate of the video system.
IOR, IOG, IOB, IOR*, IOG*, IOB*	Red, green, and blue differential video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. **Warning: It is important that a ferrite bead be used to connect the VAA(1) power pin to the analog power plane as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA(1) pin will result in unstable operation.**
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG* is: RSET (ohms) = 31,460 / IOG (mA) The full scale output current on IOR* and IOB* for a given RSET is defined as: IOR, IOB (mA) = 22,990 / RSET (ohms) Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt109 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt109 and any associated analog circuitry should have it's own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt109.

The analog ground plane area should encompass all Bt109 ground pins, power supply bypass circuitry for the Bt109, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt109.

Power Planes

The Bt109 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt109.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt109 power pins and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 μF, 0.01 μF, and 0.001 μF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation due to high-frequency oscillations.

If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt109 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

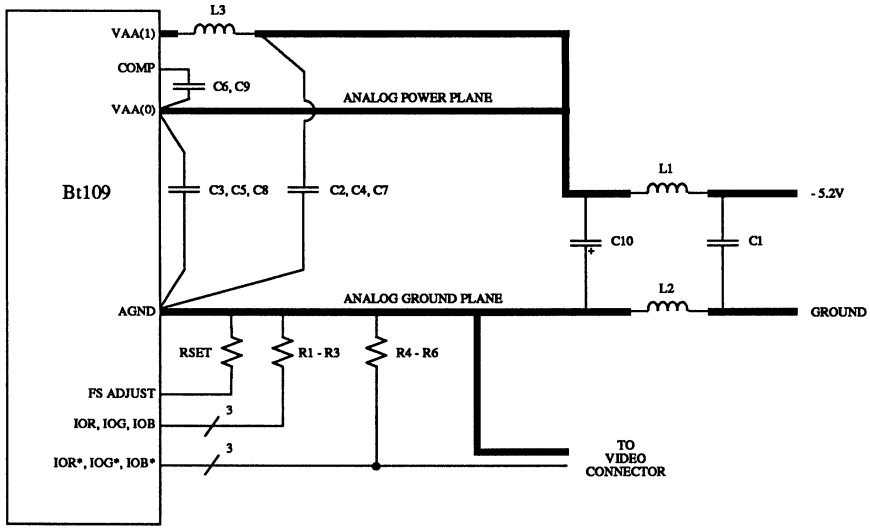
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4 - C6	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C7 - C9	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C10	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	37.4-ohm 1% metal film resistor	Dale CMF-55C
R4, R5, R6	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	1100-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt109.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Terminated Inputs

All digital inputs of the Bt109 should be terminated using normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical zero state.

Non-Video Applications

The Bt109 may be used in non-video applications by disabling the video-specific control inputs. The SYNC, BLANK, and OVERLAY inputs should be a logical zero. All three outputs will have the same full scale output current.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 19,360 / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 2,090 / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	- 4.9	- 5.2	- 5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
FS ADJUST Resistor*	RSET		1100		Ohms

*FS ADJUST set to 1.125 mA

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			- 6.5	Volts
Voltage on any Digital Pin		AGND + 0.5		VAA - 0.5	Volts
Analog Output Short Circuit Duration to any Common			indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	- 1170 - 1130 - 1070		- 840 - 810 - 735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	- 1950 - 1950 - 1950		- 1480 - 1480 - 1450	mV mV mV
Input High Current (Data, Sync) (Vin = VIHmax)	IIH	0 +25 +70			25 25 25	µA µA µA
Input High Current (Overlay) (Vin = VIHmax, VILmin)	IIH	0 +25 +70			210 210 210	µA µA µA
Input High/Low Current (Blank) (Vin = VIHmax, VILmin)	IIH / IIL	0 +25 +70			160 160 160	µA µA µA
Input Low Current (Data, Sync, Overlay) (Vin = VILmin)	IIL	0 +25 +70			5 5 5	µA µA µA
Input Capacitance (f = 1 MHz, Vin = VIHmax) BLANK All Others	CIN				 20 7	 pF pF
Internal Voltage Reference	VREF			- 1.2		Volts

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1/2	LSB
Differential Linearity Error	DL			± 1/2	LSB
Gray Scale Error				± 10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Analog Outputs					
Gray Scale Current Range:					
Black Level Relative to White				- 20	mA
Blank Level Relative to White				- 30	mA
Output Current					
Overlay Level		0	- 5	- 50	µA
White Level		- 1.70	- 1.90	- 2.10	mA
Black Level Relative to White		- 15.86	- 17.62	- 19.38	mA
Blank Level Relative to Black		- 0.95	- 1.44	- 1.90	mA
Blank Level Relative to White		- 16.81	- 19.05	- 21.28	mA
Sync Level Relative to Blank		- 6.29	- 7.62	- 8.96	mA
LSB Size			- 69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.2		+ 1.5	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 KHz)	PSRR			0.5	%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -17.62 mA full scale output current (no sync information).

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

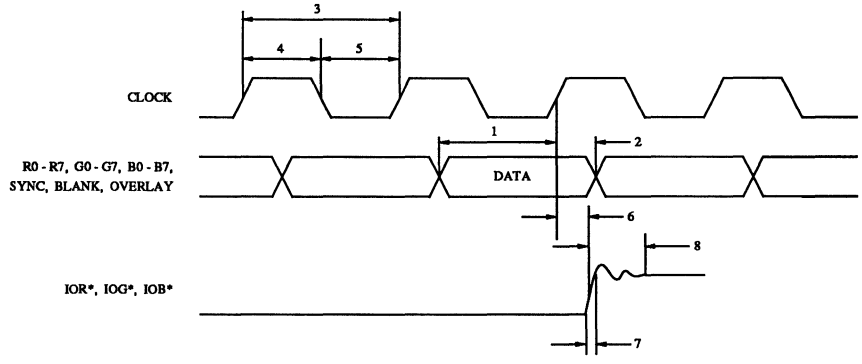
Parameter	Symbol	Min	Typ	Max	Units
Clock Rate				250	MHz
Data and Control Setup Time Data and Control Hold Time	1 2	1.5 0			ns ns
Clock Cycle Time Clock Pulse Width High Clock Pulse Width Low	3 4 5	4 1.6 1.6			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time Glitch Impulse	6 7 8		 0.5 4 50	3 1	ns ns ns pV - sec
VAA Supply Current	IAA			400	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -17.62 mA full scale output current (no sync information). ECL input values are -0.89 to -1.69 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt109KC	250 MHz	40-pin 0.6" Ceramic Cavity Down DIP	0° to +70° C.

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

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Table of Contents

RAMDAC Selection Guide

D/A Organization	Speed (MHz)	Part Number	Page	RAM Size	Overlay Size	
triple 4-bit	170, 110	Bt454	5 - 67	16 x 12	1 x 12	muxed pixel inputs
triple 4-bit	125, 110, 80	Bt451	5 - 19	256 x 12	4 x 12	Bt458 pin compatible
triple 4-bit	70, 50, 30	Bt450	5 - 5	16 x 12	3 x 12	
triple 6-bit	80, 66, 50, 35	Bt471	5 - 167	256 x 18	15 x 12	Bt478 pin compatible
triple 6-bit	66, 50, 35	Bt476	5 - 167	256 x 18	-	Bt478 pin compatible
single 8-bit	360	Bt492	5 - 237	256 x 8	16 x 8	2:1 muxed pixel inputs
single 8-bit	170, 135, 110, 80	Bt461	5 - 133	1024 x 8	256 x 8	muxed pixel inputs
single 8-bit	125, 110, 80	Bt457	5 - 19	256 x 8	4 x 8	Bt458 pin compatible

	Display Resolution				
DAC Size	Low (640 x 480)	Medium (1k x 800)	High (1280 x 1024)	Medium High (1600 x 1200)	Ultra High (2k x 2k)
4-bit	Bt450	Bt450 Bt451	Bt451 Bt454	Bt454	
6-bit	Bt471 Bt476	Bt471 Bt476			
8-bit	Bt453 Bt473 Bt478 Bt479	Bt453 Bt457 Bt458 Bt459 Bt460 Bt461 Bt473 Bt478 Bt479	Bt457 Bt458 Bt459 Bt460 Bt461	Bt458 Bt461 Bt468	Bt492

RAMDAC Selection Guide (continued)

D/A Organization	Speed (MHz)	Part Number	Page	RAM Size	Overlay Size	
triple 8-bit	200, 170	Bt468	5 - 165	256 x 24	15 x 24	muxed pixel inputs
triple 8-bit	135, 110, 80	Bt460	5 - 131	512 x 24	15 x 24	on-chip cursor
triple 8-bit	135, 110, 80	Bt459	5 - 85	256 x 24	15 x 24	on-chip cursor
triple 8-bit	170, 125, 110, 80	Bt458	5 - 19	256 x 24	4 x 24	muxed pixel inputs
triple 8-bit	80, 66, 50, 35	Bt479	5 - 211	1024 x 24	15 x 24	Window RAMDAC
triple 8-bit	80, 66, 50, 35	Bt478	5 - 167	256 x 24	15 x 24	PS/2 RAMDAC
triple 8-bit	80, 66, 50, 35	Bt473	5 - 187	(3) 256 x 8	(3) 15 x 8	true-color RAMDAC
triple 8-bit	66, 40	Bt453	5 - 51	256 x 24	3 x 24	

	Display Resolution				
DAC Size	Low (640 x 480)	Medium (1k x 800)	High (1280 x 1024)	Medium High (1600 x 1200)	Ultra High (2k x 2k)
4-bit	Bt450	Bt450 Bt451	Bt451 Bt454	Bt454	
6-bit	Bt471 Bt476	Bt471 Bt476			
8-bit	Bt453 Bt473 Bt478 Bt479	Bt453 Bt457 Bt458 Bt459 Bt460 Bt461 Bt473 Bt478 Bt479	Bt457 Bt458 Bt459 Bt460 Bt461	Bt458 Bt461 Bt468	Bt492

Bt450

70 MHz

Monolithic CMOS

16 x 12 Color Palette

RAMDAC™

Distinguishing Features

- 70, 50, 30 MHz Operation
- Triple 4-bit D/A Converters
- 16 x 12 Dual Port Color Palette RAM
- 3 x 12 Dual Port Overlay Palette
- RS-343A/RS-170 Compatible Outputs
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 28-pin DIP Package
- Typical Power Dissipation: 900 mW

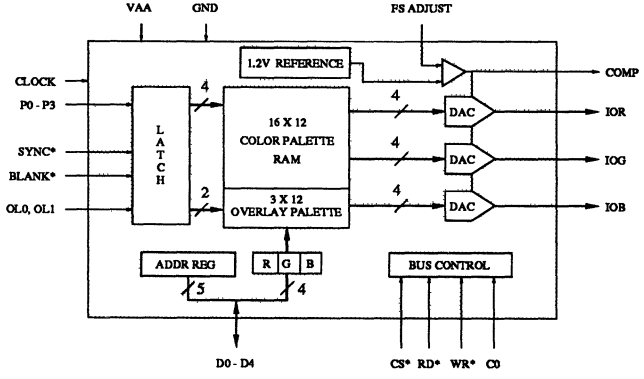
Applications

- Graphics Terminals
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt454, Bt451
- Bt453, Bt476, Bt478

Functional Block Diagram



Product Description

The Bt450 is a triple 4-bit video RAMDAC, designed specifically for high resolution color graphics, supporting up to 19 simultaneous colors from a 4096 color palette.

Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt450 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1/16 LSB and ± 1/8 LSB, respectively, over the full temperature range.

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L450001 Rev. D

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt450 has an internal 16 x 12 color palette RAM, three 12-bit overlay registers, and three 4-bit D/A converters, allowing the display of up to 19 simultaneous colors from a 4096 color palette. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

The C0 input specifies whether the MPU is accessing the address register (logical zero), or the color palette RAM location or overlay register specified by the address register (logical one).

The 5-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. During color write cycles, color data is input from D0 - D3, with D0 being the least significant bit. D4 is ignored. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 to select the color palette RAM and overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 12-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. During color read cycles, color data is output onto D0 - D3, with D0 being the least significant bit. D4 is a logical zero. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 to select the color palette RAM and overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

The address register increments to $13 following a blue read or write cycle to location $12.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 1. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other five bits of the address register (ADDR0 - 4) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 1.

Figure 1 illustrates the MPU read/write timing.

Frame Buffer Interface

The P0 - P3, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 2. The addressed location provides 12 bits of color information to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt450 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

Circuit Description (continued)

	Value	C0	CS*	RD*	WR*	Addressed by MPU
ADDRa, b (counts modulo 3)	00	1				red value
	01	1				green value
	10	1				blue value, increment ADDR0 - 4
ADDR0 - 4 (counts binary)	$xx	0	0	1	0	write to address register
	$00 - $0F	1	0	1	0	write to color palette RAM
	$10	1	0	1	0	write to overlay color 1
	$11	1	0	1	0	write to overlay color 2
	$12	1	0	1	0	write to overlay color 3
	$xx	0	0	0	1	read address register
	$00 - $0F	1	0	0	1	read color palette RAM
	$10	1	0	0	1	read overlay color 1
	$11	1	0	0	1	read overlay color 2
	$12	1	0	0	1	read overlay color 3
	$xx	x	0	0	0	invalid operation
	$xx	x	1	x	x	3-state D0 - D4

Table 1. Address Register (ADDR) Operation.

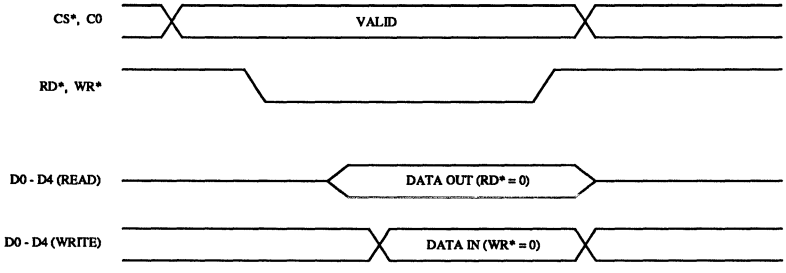


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

OL1	OL0	P0 - P3	Addressed by frame buffer
0	0	$0	color palette RAM location $0
0	0	$1	color palette RAM location $1
:	:	:	:
0	0	$F	color palette RAM location $F
0	1	$x	overlay color 1
1	0	$x	overlay color 2
1	1	$x	overlay color 3

Table 2. Pixel and Overlay Control Truth Table.

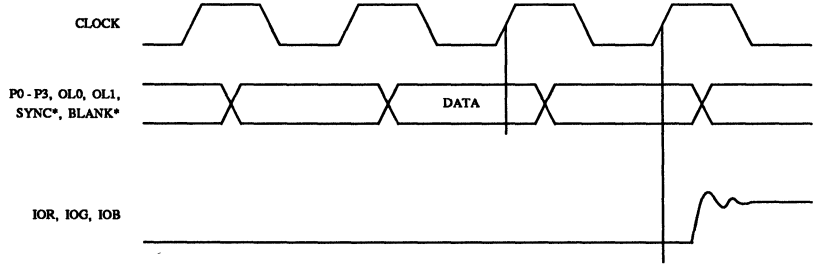
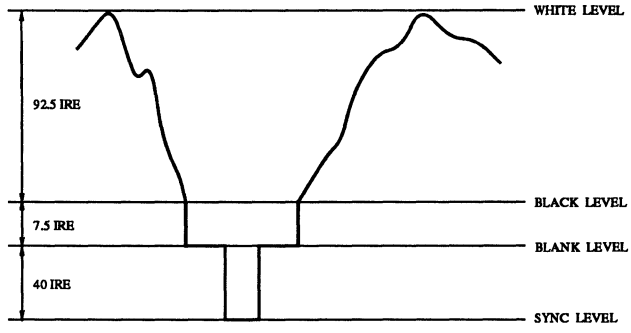


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 499 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full scale IOG = 26.67 mA. RSET = 499 ohms.

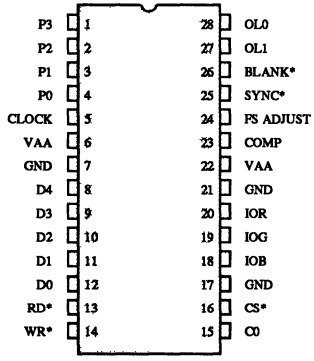
Table 3. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P3, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer.
P0 - P3	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 16 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 2. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = 13,308 / IOG (mA) The amount of full scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = 9,506 / RSET (ohms)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin(Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. Note that the Bt450 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0	Command control input (TTL compatible). C0 specifies whether the MPU is accessing the address register (logical zero) or the color palettes (logical one).
D0 - D4	Data bus (TTL compatible). Data is transferred into and out of the device over this five bit bidirectional data bus. D0 is the least significant bit.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt450 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt450 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt450, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt450.

Power Planes

The Bt450 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within three inches of the Bt450.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt450 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the two VAA pins to GND. These capacitors should be placed as close as possible to the device. It is important to note that while the Bt450 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt450 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt450 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

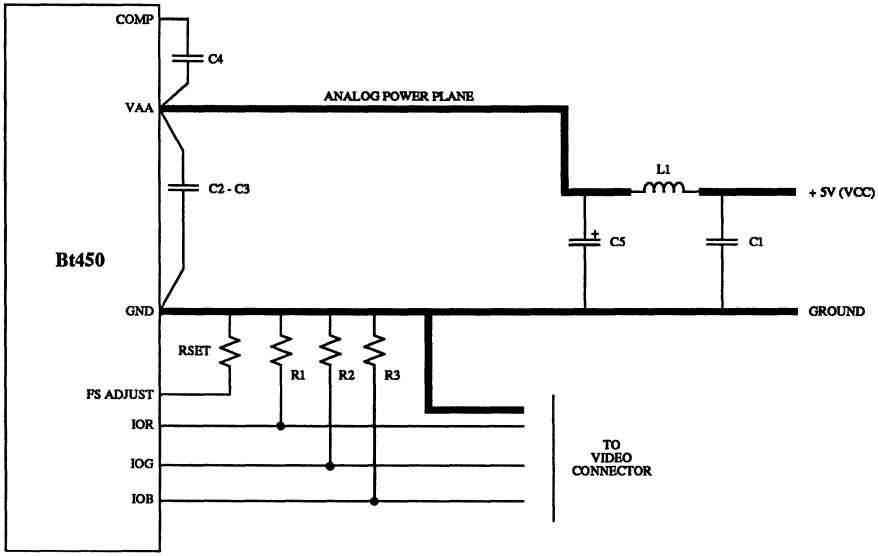
Analog Signal Interconnect

The Bt450 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt450 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	499-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt450.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C.
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		499		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1/8	LSB
Differential Linearity Error	DL			± 1/16	LSB
Gray Scale Error				± 10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			10	µA
Input Low Current (Vin = 0.4v)	IIL			- 10	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ				µA
Output Capacitance	CDOUT		20		pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			1.175		mA
DAC to DAC Matching			2		%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		30		pF
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 ohms. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

Parameter	Symbol	Min/Typ/ Max				Units
Clock Rate	Fmax	max	70	50	30	MHz
CS*, C0 Setup Time	1	min	35	35	35	ns
CS*, C0 Hold Time	2	min	35	35	35	ns
RD*, WR* High Time	3	min	25	25	25	ns
RD* Asserted to Data Bus Driven	4	min	10	10	10	ns
RD* Asserted to Data Valid	5	max	100	100	100	ns
RD* Negated to Data Bus 3-Stated	6	max	30	30	30	ns
WR* Low Time	7	min	50	50	50	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	10	10	10	ns
Pixel and Control Setup Time	10	min	4	5	10	ns
Pixel and Control Hold Time	11	min	1	2	5	ns
Clock Cycle Time	12	min	14.3	20	33.3	ns
Clock Pulse Width High Time	13	min	5	7	10	ns
Clock Pulse Width Low Time	14	min	5	7	10	ns
Analog Output Delay	15	typ	15	15	25	ns
Analog Output Rise/Fall Time	16	max	7	7	7	ns
Analog Output Settling Time	17	max	20	20	25	ns
Clock and Data Feedthrough*		typ	- 30	- 30	- 30	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	- 25	- 25	- 25	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay	18		2	2	2	Clocks
VAA Supply Current**	IAA	typ	175	140	110	mA
		max	220	175	135	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 ohms. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 130 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Timing Waveforms

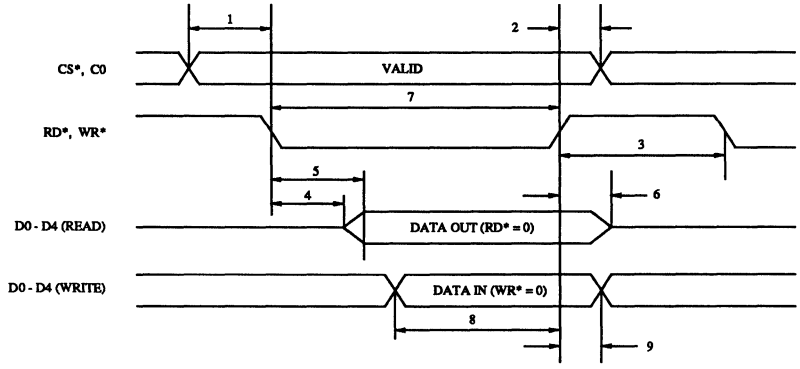
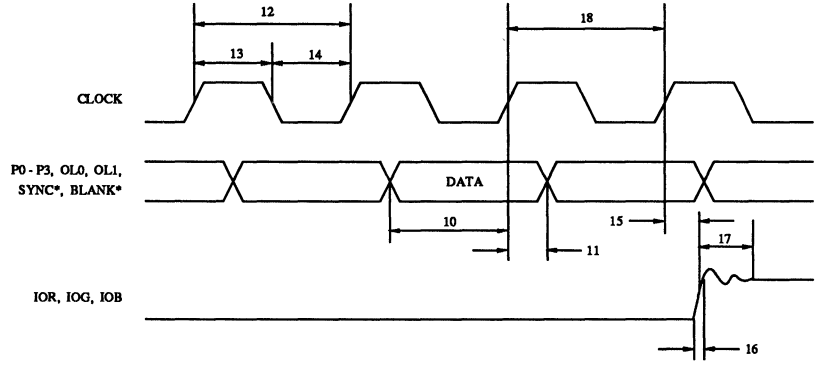


Figure 5. MPU Read/Write Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/8 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt450KC70	70 MHz	28-pin 0.6" CERDIP	0° to +70° C.
Bt450KC50	50 MHz	28-pin 0.6" CERDIP	0° to +70° C.
Bt450KC30	30 MHz	28-pin 0.6" CERDIP	0° to +70° C.

Device Circuit Data

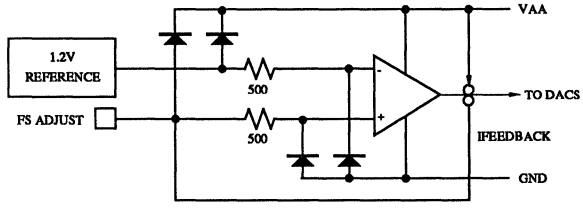


Figure 7. Equivalent Circuit of the Reference Amplifier.

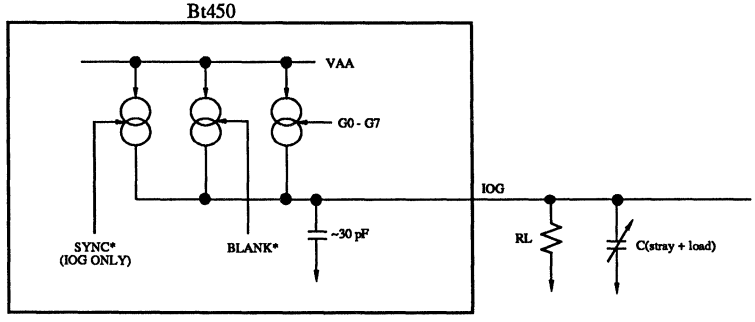


Figure 8. Equivalent Circuit of the Current Output (IOG).

Bt451 Bt457 Bt458

125 MHz / 170 MHz

Monolithic CMOS

256 Color Palette

RAMDAC™

Distinguishing Features

- 170, 125, 110, 80 MHz Operation
- Multiplexed TTL Pixel Ports
- 256 Word Dual Port Color Palette
- 4 Dual Port Overlay Registers
- RS-343A Compatible Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- 84-pin PLCC or PGA Package
- +5v CMOS Monolithic Construction

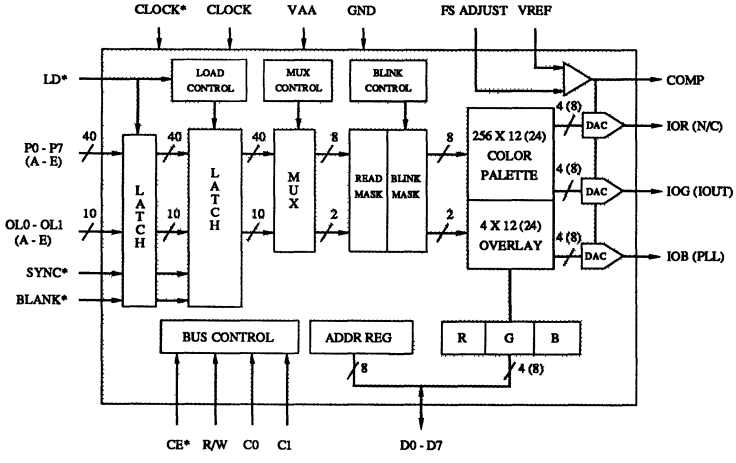
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt461, Bt468

Functional Block Diagram



Product Description

The Bt451, Bt457, and Bt458 are pin-compatible and software-compatible RAMDACs designed specifically for high performance, high resolution color graphics. The architecture enables the display of 1280 x 1024 bit mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 32 MHz) to the frame buffer, while maintaining the 125 MHz video data rates required for sophisticated color graphics.

The Bt451 has a 256 x 12 color lookup table with triple 4-bit video D/A converters.

The Bt458 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters.

The Bt457 is a single-channel version of the Bt458 and has a 256 x 8 color lookup table with a single 8-bit video D/A converter. It includes a PLL output to enable sub-pixel synchronization of multiple Bt457s.

On chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt451/457/458 generates RS-343A compatible red, green, and blue video signals, and are capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt451/457/458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0 - 7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt451/458 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (12-bit word for the Bt451) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. Note that the Bt451 uses only the four most significant bits of color data (D4 - D7) and ignores D0 - D3.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data. Note that the Bt451 outputs only four bits of color data onto D4 - D7 and forces D0 - D3 to a logical zero.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0 - 7) are accessible to the MPU.

ADDR0 - 7	C1	C0	Addressed by MPU
$xx	0	0	address register
$00 - $FF	0	1	color palette RAM
$00	1	1	overlay color 0
$01	1	1	overlay color 1
$02	1	1	overlay color 2
$03	1	1	overlay color 3
$04	1	0	read mask register
$05	1	0	blink mask register
$06	1	0	command register
$07	1	0	control/test register

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Bt457 Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette RAM or the overlay registers. The address register then increments to the next location which the MPU may modify by simply writing another color.

Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (eight bits each of red, green, blue) may be read or written to three Bt457s in a single MPU cycle. In this application, the CE* inputs of all three Bt457s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, etc.).

When accessing the color palette RAM, the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a read or write cycle to overlay register 3.

Bt457 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt457 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt457s share a common 8-bit data bus. The CE* inputs of all three Bt457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0 - 7) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt451/457/458 incorporate internal latches and multiplexers. As illustrated in Figure 1, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either four or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with four or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt451/457/458 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

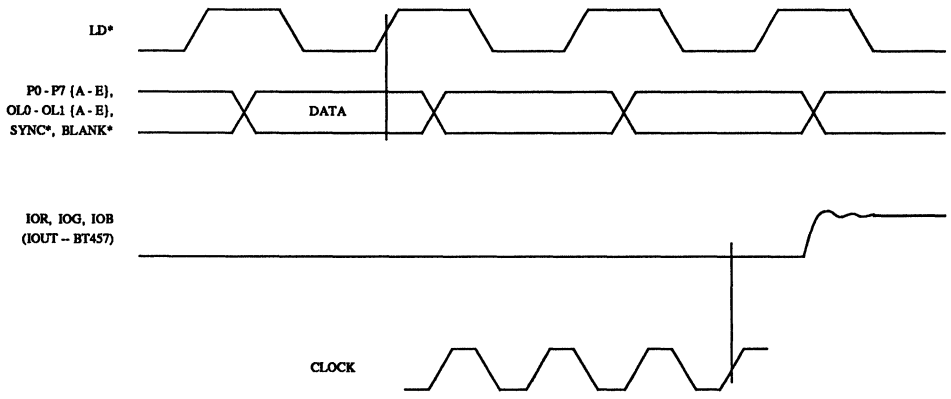


Figure 1. Video Input/Output Timing.

Circuit Description (continued)

Color Selection

Each clock cycle, eight bits of color information (P0 - P7) and two bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e. in the middle of the screen), the Bt451/457/458 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Video Generation

Every clock cycle, the selected color information from the color palette RAMs or overlay registers are presented to the D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) on the Bt451 and Bt458 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

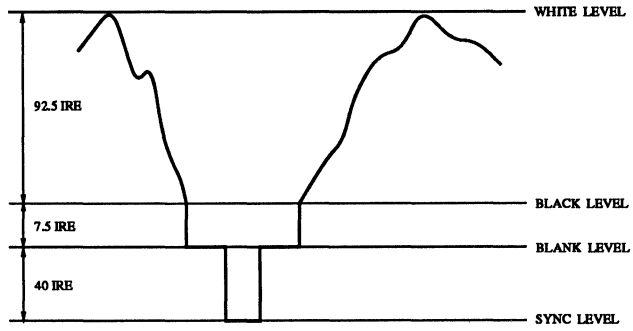
The D/A converters on the Bt451, Bt457, and Bt458 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

CR6	OL1	OL0	P0 - P7	Addressed by frame buffer
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

IOR, IOB		IOG (IOUT)	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 523 ohms, VREF = 1.235v. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (IOUT) (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 523 ohms, VREF = 1.235v. Note that the Bt451 uses only the upper four DAC input data bits.

Table 3. Video Output Truth Table.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR7 Multiplex select

(0) 4:1 multiplexing
(1) 5:1 multiplexing

This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate.

Note that it is possible to reset the pipeline delay of the Bt457/458 to a fixed 8 clock cycles. In this instance, each time the input multiplexing is changed, the Bt457/458 must again be reset to a fixed pipeline delay.

CR6 RAM enable

(0) use overlay color 0
(1) use color palette RAM

When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR5, CR4 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).

CR3 OL1 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL1 {A - E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A - E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.

CR2 OL0 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL0 {A - E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A - E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers (continued)

Command Register (continued)

CR1	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A - E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A - E} inputs.
CR0	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A - E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A - E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A - E}) and D7 corresponds to bit plane 7 (P7 {A - E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A - E}) and D7 corresponds to bit plane 7 (P7 {A - E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Bt451/458 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper four bits (D4 - D7) are ignored.

The contents of the test register are defined as follows:

D7 - D4	color information (4-bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting one, and only one, of the (red, green, blue) enable bits. These bits specify which four bits of color information the MPU wishes to read (R0 - R3, G0 - G3, B0 - B3, R4 - R7, G4 - G7, or B4 - B7). When the MPU reads the test register, the four bits of color information from the DAC inputs are contained in the upper four bits, and the lower four bits contain the (red, green, blue, low or high nibble) enable information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper four bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4 - D7 containing R4 - R7 color bits, and D0 - D3 containing (red, green, blue, low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Note that since the Bt451 has 4-bit D/A converters, bit D3 of the test register will always be a logical zero.

Internal Registers (continued)

Bt457 Control/Test Register

The control/test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converter. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper four bits (D4 - D7) are ignored.

The contents of the test register are defined as follows:

D7 - D4	color information
D3	low (logical one) or high (logical zero) nibble
D2	blue channel enable
D1	green channel enable
D0	red channel enable

To use the control/test register, the MPU writes to it, specifying the low or high nibble of color information. When the MPU reads the register, the four bits of color information from the DAC inputs are contained in the upper four bits, and the lower four bits contain whatever was previously written to the register. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green, and blue enable bits are used to specify the mode of writing color data to, and reading color data from, the Bt457. If all three enable bits are a logical zero, each write cycle to the color palette RAM or overlay registers loads eight bits of color data. During each read cycle of the color palette RAM or overlay registers, eight bits of color data are output onto the data bus. If a 24-bit data bus is available, this enables three Bt457s to be accessed simultaneously.

If any of the red, green, blue enable bits are a logical one, the Bt457 assumes the MPU is reading and writing color information using red, green, blue cycles, such as are used on the Bt451 and Bt458. Setting the appropriate enable bit configures the Bt457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logical one, and a red, green, blue write cycle occurred, the Bt457 would input data only during the green write cycle. If a red, green, blue read cycle occurred, the Bt457 would output data only during the green read cycle. Note that CE* must be a logical zero during each of the red, green, blue cycles. One, and only one, of the enable bits must be a logical one. This mode of operation is useful where only an 8-bit data bus is available, and the software drivers are written for RGB operation.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LD*	Load control input (TTL compatible). The P0 - P7 {A - E}, OL0 - OL1 {A - E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the A.C. Characteristics section.
P0 - P7 {A-E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to eight bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output, at which point the cycle repeats.
OL0 - OL1 {A-E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:

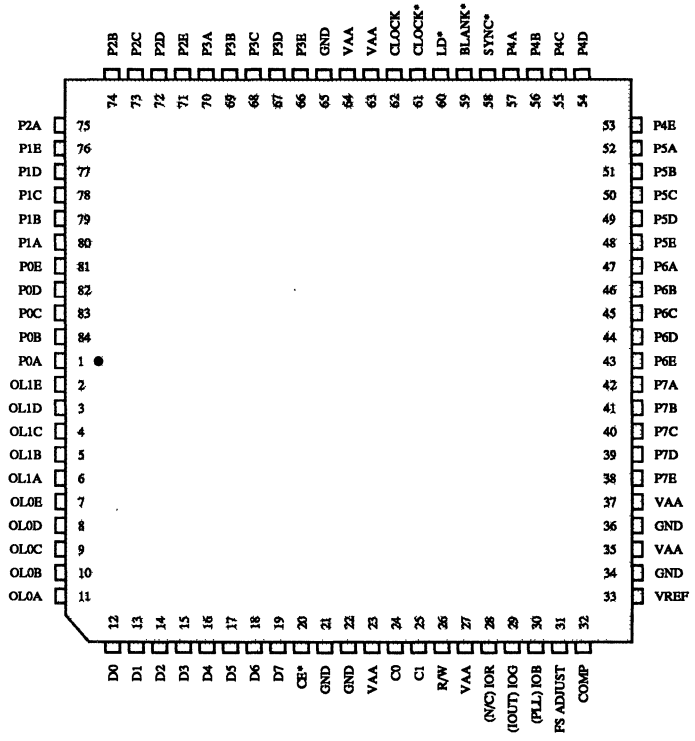
OL1	OL0	CR6 = 1	CR6 = 0
0	0	color palette RAM	overlay color 0
0	1	overlay color 1	overlay color 1
1	0	overlay color 2	overlay color 2
1	1	overlay color 3	overlay color 3

	When accessing the overlay palette, the P0 - P7 {A - E} inputs are ignored. Overlay information bits (up to two bits per pixel) for either four or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). The Bt457 outputs IOUT rather than IOR, IOG, and IOB.
PLL	Phase lock loop current output -- Bt457 only. This high impedance current source is used to enable multiple Bt457s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one on the BLANK* input results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (v) / RSET (ohms) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 ohms).

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 3). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG (or IOUT for the Bt457) is: RSET (ohms) = 11,294 * VREF (v) / IOG (mA) The full scale output current on IOR and IOB (for the Bt451 and Bt458) for a given RSET is: IOR, IOB (mA) = 8,067 * VREF (v) / RSET (ohms)
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.235v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 volt) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued) -- 84-Pin J-Lead Package



Note: Bt457 pin names are in parentheses.

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Pin Descriptions (continued) -- 84-pin PGA Package

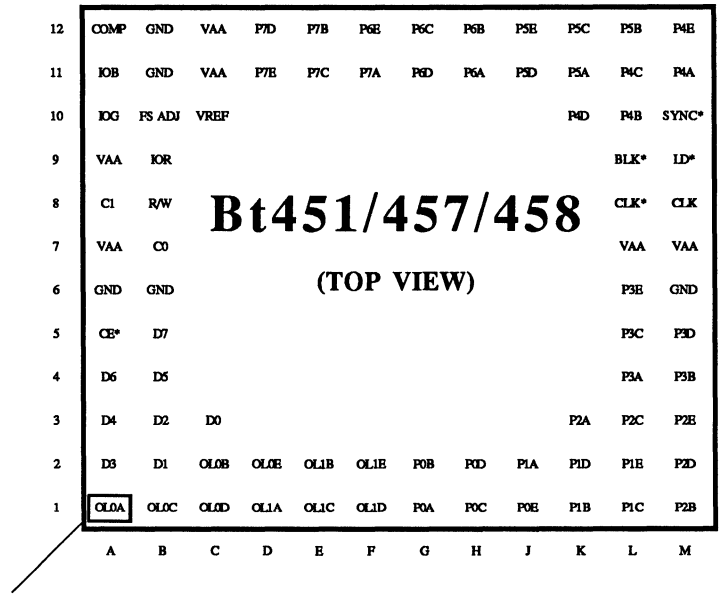
Signal	Pin Number
BLANK*	L9
SYNC*	M10
LD*	M9
CLOCK*	L8
CLOCK	M8
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J1
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P3E	L6
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12

Signal	Pin Number
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
IOG (IOUT)	A10
IOB (PLL)	A11
IOR (N/C)	B9

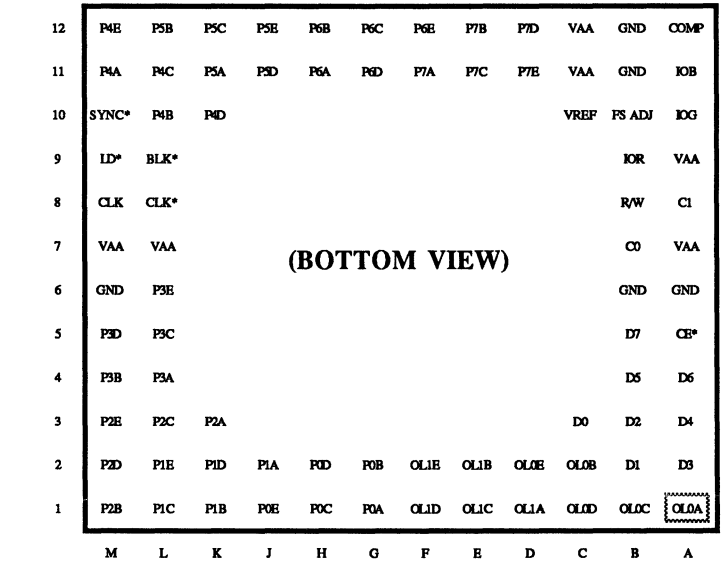
Signal	Pin Number
VAA	C12
VAA	C11
VAA	A9
VAA	L7
VAA	M7
VAA	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJUST	B10
VREF	C10
CE*	A5
R/W	B8
C1	A8
C0	B7
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

Note: Bt457 pin names are in parentheses.

Pin Descriptions (continued) -- 84-pin PGA Package



	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	GND	VAA	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	VAA	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	VREF							P4D	P4B	SYNC*
9	VAA	IOR									BLK*	LD*
8	C1	R/W									CLK*	CLK
7	VAA	C0									VAA	VAA
6	GND	GND									P3E	GND
5	CE*	D7									P3C	P3D
4	D6	D5									P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B



	M	L	K	J	H	G	F	E	D	C	B	A
12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	VAA	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	VAA	GND	IOB
10	SYNC*	P4B	P4D							VREF	FS ADJ	IOG
9	LD*	BLK*									IOR	VAA
8	CLK	CLK*									R/W	C1
7	VAA	VAA									C0	VAA
6	GND	P3E									GND	GND
5	P3D	P3C									D7	CE*
4	P3B	P3A									D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A

Pin	Bt451/458	Bt457
A10	IOG	IOUT
A11	IOB	PLL
B9	IOR	N/C

PC Board Layout Considerations

PC Board Considerations

It is recommended that a four layer PC board be used with the Bt451/457/458. The layout should be optimized for lowest noise on the Bt451/457/458 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt451/457/458 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt451/457/458, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt451/457/458.

Power Planes

The Bt451/457/458 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt451/457/458.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt451/457/458 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor should be used to decouple each of the three groups of VAA pins to GND. These capacitors should be placed as close as possible to the device. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the Bt451/457/458 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt451/457/458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground plane.

Due to the high clock rates involved, long clock lines to the Bt451/457/458 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

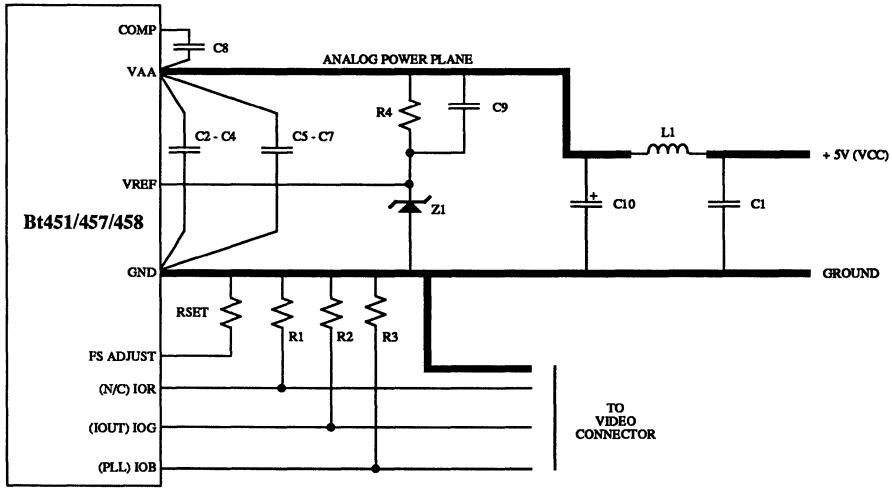
Analog Signal Interconnect

The Bt451/457/458 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch. Also, the external voltage reference circuitry should be as close as possible to the Bt451/457/458 to avoid noise pickup.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt451/457/458 to minimize reflections.

PC Board Layout Considerations (continued)



Note: Bt457 pin names in parentheses.

Location	Description	Vendor Part Number
C1 - C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5 - C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1000-ohm 1% metal film resistor	Dale CMF-55C
RSET	523-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385Z-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt451/457/458. R3 not used with Bt457 (see Applications Section).

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt451/457/458 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 volts. Note that the CLOCK and CLOCK* inputs require termination resistors (220-ohm resistor to VCC and a 330-ohm resistor to GND). The termination resistors should be as close as possible to the Bt451/457/458.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt451/457/458 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

It is recommended that the Bt438 or Bt439 Clock Generator Chips be used to generate the clock and load signals. Both support the 4:1 and 5:1 input multiplexing of the Bt451/457/458, and will also optionally set the pipeline delay of the Bt457 and Bt458 to eight clock cycles. Figures 4 and 5 illustrate using the Bt438 with the Bt451/457/458.

In applications using a single Bt457, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 ohms).

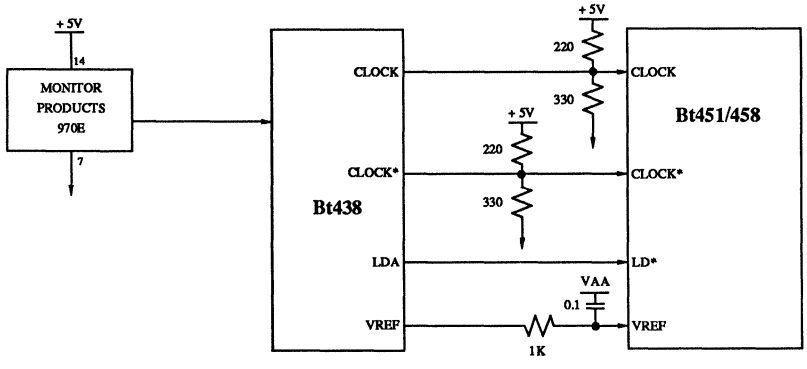


Figure 4. Generating the Bt451/458 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay (Bt457, Bt458)

The pipeline delay of the Bt457/458, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt457/458 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt457/458.

To reset the Bt457/458, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt457/458 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt457/458s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

In standard operation, the Bt457/458 need be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

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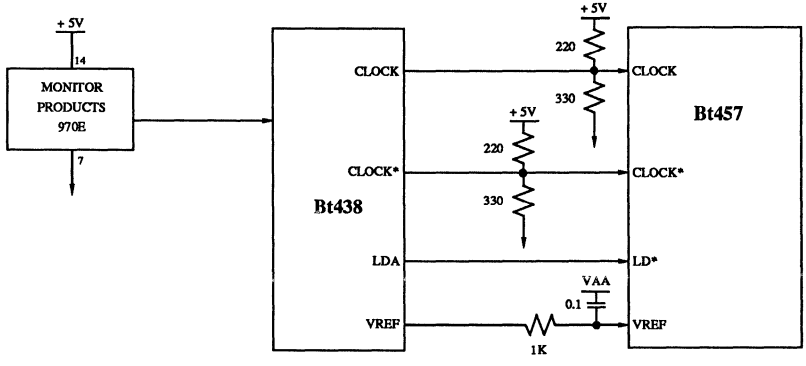

Figure 5. Generating the Bt457 Clock Signals (Monochrome Application).

Application Information (continued)

Bt457 Color Display Applications

For color display applications where up to four Bt457s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1, and 5:1 input multiplexing of the Bt457, synchronizes them to sub-pixel resolution, and will also optionally set the pipeline delay of the Bt457 to eight clock cycles. The Bt439 may also be used to interface the Bt457 to a TTL clock. Figure 6 illustrates using the Bt439 with the Bt457.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt457, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt457s, and adjusts the phase each of the CLOCK and CLOCK* signals to the Bt457s to minimize the PLL phase difference.

If sub-pixel synchronization of multiple Bt457s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt457s are connected together and driven by a single Bt438 (with distributed branch termination on each clock). The VREF inputs of the Bt457s must still be isolated by 1K-ohm resistors, as shown in Figure 6, and have a 0.1 µF bypass capacitor to VAA. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 ohms).

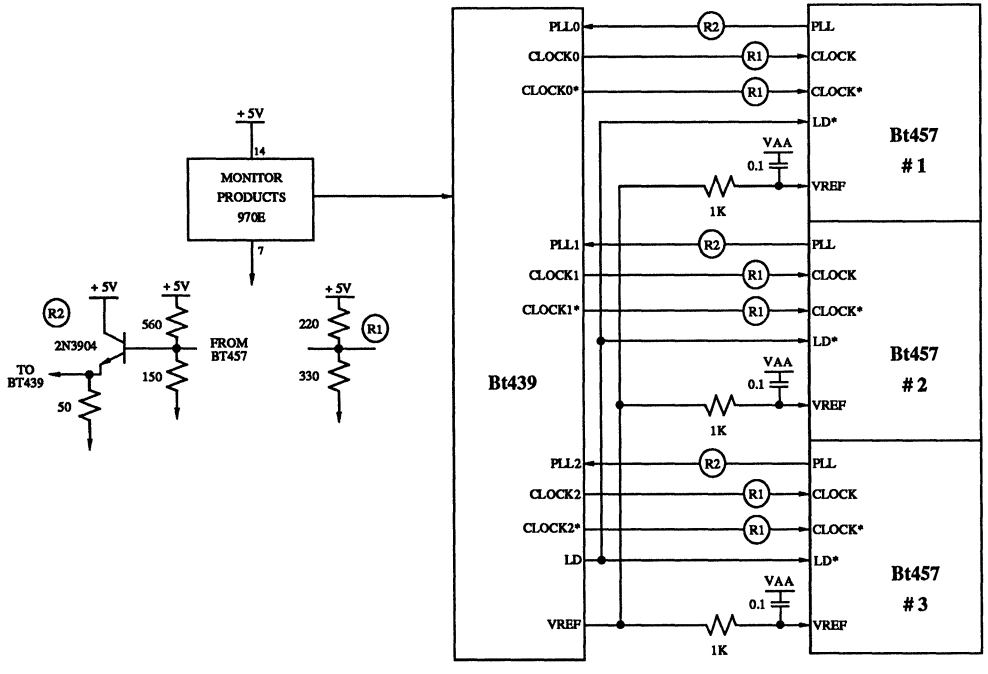

Figure 6. Generating the Bt457 Clock Signals (Color Application).

Application Information (continued)

Using Multiple Bt457s

If located close together on the same PC board, multiple Bt457s may be connected to a single analog power plane. In addition, a single voltage reference may drive multiple devices.

Each Bt457 must still have it's individual RSET resistor, IOUT termination resistor, power supply bypass capacitors, and COMP capacitor.

Bt457 Non-Video Applications

The Bt457 may be used in non-video applications by disabling the video-specific control signals. SYNC* should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,457 * VREF (v) / Iout (mA)

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 610 * VREF (v) / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin.

Initializing the Bt451/458

Following a power-on sequence, the Bt451/458 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt458 to a fixed pipeline delay of 8 clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e. from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt451/458 as follows:

4:1 multiplexed operation
no overlays
no blinking

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

Application Information (continued)

Initializing the Bt457 (Monochrome)

Following a power-on sequence, the Bt457 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457 to a fixed pipeline delay of 8 clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e. from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457 as follows:

4:1 multiplexed operation
no overlays
no blinking
color data written/read every cycle

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write data to RAM (location $00)	01
Write data to RAM (location $01)	01
:	:
Write data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write data to overlay (location $00)	11
Write data to overlay (location $01)	11
:	:
Write data to overlay (location $03)	11

Initializing the Bt457 (Color) 24-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. A 24-bit MPU data bus is available for accessing all three Bt457s in parallel.

The operation and initialization is the same as for the Bt457 being used in a monochrome application.

Initializing the Bt457 (Color) 8-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. An 8-bit MPU data bus is available for accessing the Bt457s.

Note that while accessing the command, read mask, blink mask, and control/test, and address register, each Bt457 must be accessed individually. While accessing the color palette RAM or overlay registers, all three Bt457s are accessed simultaneously.

Following a power-on sequence, the Bt457s must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457s to a fixed pipeline delay of 8 clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e. from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457s as follows:

4:1 multiplexed operation
no overlays
no blinking
initialize each Bt457 as a red, green, or blue device

Control Register Initialization	C1, C0
Red Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $01 to test register	10
Green Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $02 to test register	10

Application Information (continued)

Blue Bt457

Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $04 to test register	10

Color Palette RAM Initialization

Write $00 to all three address registers	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization

Write $00 to all three address registers	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

5

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8 (4)	8 (4)	8 (4)	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1 (1/8)	LSB
Differential Linearity Error	DL			± 1 (1/16)	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
(except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance	CIN		4	10	pF
(f = 1 MHz, Vin = 2.4v)					
Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA - 1.0		VAA + 0.5	Volts
Input Low Voltage	VKIL	GND - 0.5		VAA - 1.6	Volts
Input High Current (Vin = 4.0v)	IKIH			1	µA
Input Low Current (Vin = 0.4v)	IKIL			- 1	µA
Input Capacitance	CKIN		4	10	pF
(f = 1 MHz, Vin = 4.0v)					
Digital Outputs (D0 - D7)					
Output High Voltage	VOH	2.4			Volts
(IOH = -800 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 6.4 mA)					
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size					
Bt451			1.175		mA
Bt457, Bt458			69.1		µA
DAC to DAC Matching*			2	5	%
Output Compliance	VOC	- 1.0		+ 1.2	Volts
Output Impedance	RAOUT		50		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Does not apply to the Bt457.

A.C. Characteristics

		170 MHz Devices			125 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			170			125	MHz
LD* Rate	LDmax			42.5			31.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	10			10			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5.88			8			ns
Clock Pulse Width High Time	13	2.6			3.2			ns
Clock Pulse Width Low Time	14	2.6			3.2			ns
LD* Cycle Time	15	23.52			32			ns
LD* Pulse Width High Time	16	9			13			ns
LD* Pulse Width Low Time	17	9			13			ns
Analog Output Delay	18		20			20		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV - sec
Glitch Impulse*			50			50		pV - sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							mA
Bt451			n/a	n/a		310	400	
Bt458Kxx			n/a	n/a		375	445	
Bt458Lxx			310			225	330	
Bt457			n/a	n/a		200	220	

See test conditions on next page.

A.C. Characteristics

		110 MHz Devices			80 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			27.5			20	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	10			10			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			4			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	9.09			12.5			ns
Clock Pulse Width High Time	13	4			5			ns
Clock Pulse Width Low Time	14	4			5			ns
LD* Cycle Time	15	36.36			50			ns
LD* Pulse Width High Time	16	15			20			ns
LD* Pulse Width Low Time	17	15			20			ns
Analog Output Delay	18		20			20		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV - sec
Glitch Impulse*			50			50		pV - sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							mA
Bt451			295	385		265	355	
Bt458Kxx			360	430		330	400	
Bt458Lxx			210	315		200	285	
Bt457			190	210		170	190	

See test conditions on next page.

A.C. Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are VAA - 0.8 to VAA - 1.8 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 40 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1k-ohm resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**Does not apply to the Bt457.

***At Fmax. IAA (typ) at VAA = 5.0v, TA = 20° C. IAA (max) at VAA = 5.25v, TA = 0° C.

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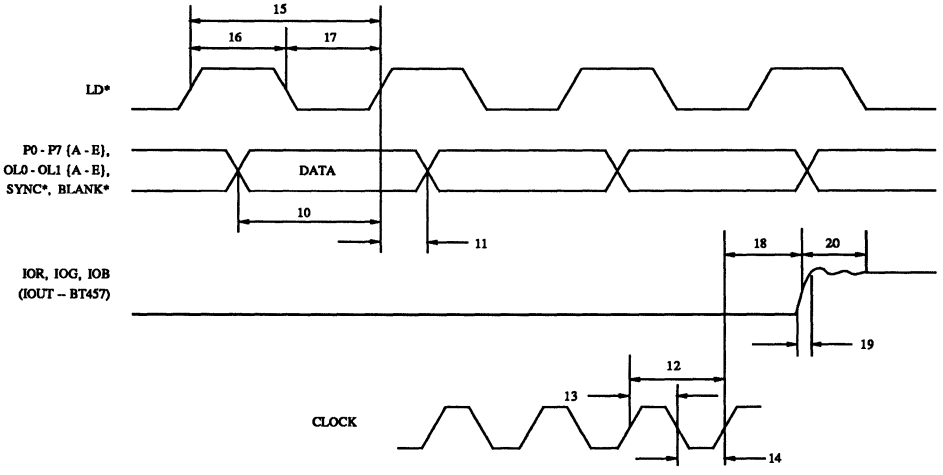


Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ± 1 LSB for the Bt457/458 or ± 1/8 LSB for the Bt451.

Note 3: Output rise/fall time measured between 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing.

Timing Waveforms (continued)

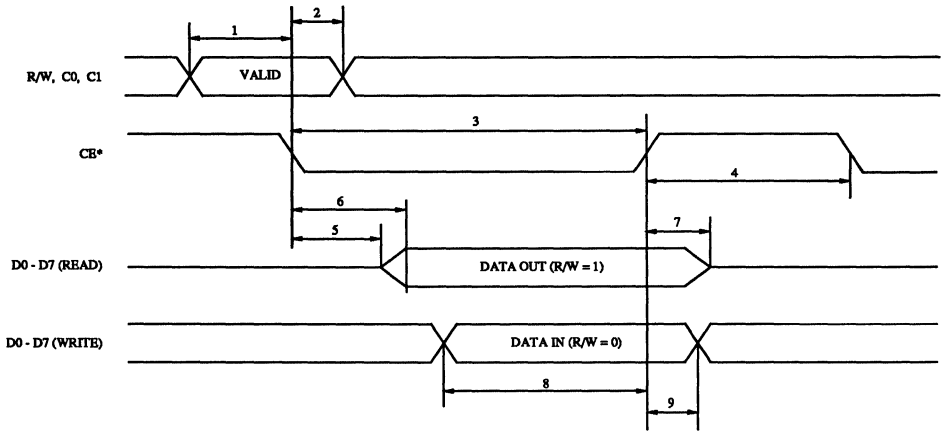


Figure 8. MPU Read/Write Timing.

Ordering Information

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LG170	256 x 24	triple 8-bit	170 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt458KG125	256 x 24	triple 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt458KG110	256 x 24	triple 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt458KG80	256 x 24	triple 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C.

Ordering Information (continued)

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LPJ170	256 x 24	triple 8-bit	170 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt458LPJ125	256 x 24	triple 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt458LPJ110	256 x 24	triple 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt458LPJ80	256 x 24	triple 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt451KG125	256 x 12	triple 4-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt451KG110	256 x 12	triple 4-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt451KG80	256 x 12	triple 4-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt451KPJ125	256 x 12	triple 4-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt451KPJ110	256 x 12	triple 4-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt451KPJ80	256 x 12	triple 4-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt457KG125	256 x 8	single 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt457KG110	256 x 8	single 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt457KG80	256 x 8	single 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C.
Bt457KPJ125	256 x 8	single 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt457KPJ110	256 x 8	single 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C.
Bt457KPJ80	256 x 8	single 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C.

Ordering Information (continued)

Model Number	
Bt451EVM	Evaluation Board for the Bt451 (includes a Bt451KG125)
Bt457EVM	Evaluation Board for the Bt457 (includes a Bt457KG125)
Bt458EVM	Evaluation Board for the Bt458 (includes a Bt458KG125)

Bt453

66 MHz

Monolithic CMOS

256 x 24 Color Palette

RAMDAC™

Distinguishing Features

- Macintosh II Compatible
- 66, 40 MHz Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343A/RS-170 Compatible Outputs
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 1 W

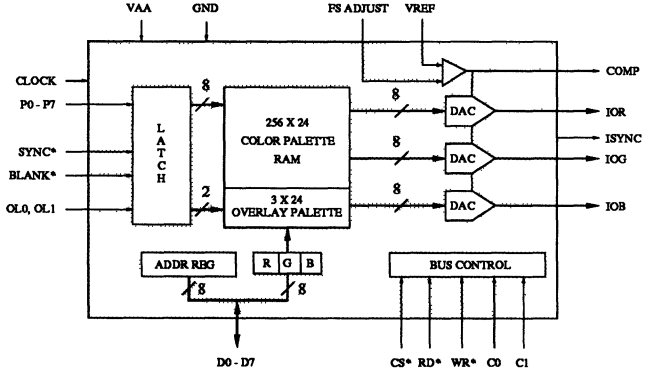
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt478

Functional Block Diagram



Product Description

The Bt453 RAMDAC is designed specifically for high resolution color graphics.

The Bt453 has a 256 x 24 color lookup table with triple 8-bit video D/A converters, supporting up to 259 simultaneous colors from a 16.8 million color palette. Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering.

Both the differential and linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

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Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

Note that anytime the CS* input is a logical zero, the video outputs are forced to the black level. When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the six most significant bits of the address register (ADDR2 - 7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2.

Figure 1 illustrates the MPU read/write timing.

C1	C0	Addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0	1	color palette RAM
	xxxx xx00	1	1	reserved
	xxxx xx01	1	1	overlay color 1
	xxxx xx10	1	1	overlay color 2
	xxxx xx11	1	1	overlay color 3

Table 2. Address Register (ADDR) Operation.

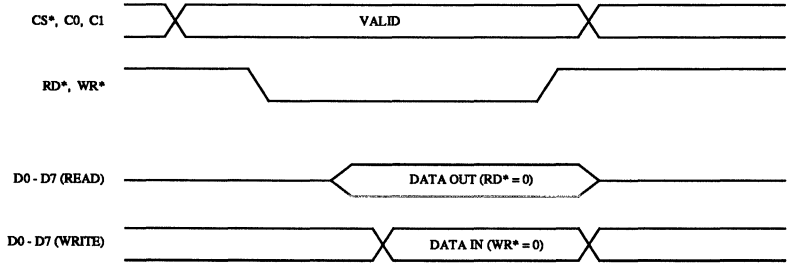


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

While CS* is a logical one, the P0 - P7, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The addressed location provides 24 bits of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 4 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt453 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

OL1	OL0	P0 - P7	Addressed by frame buffer
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
:	:	:	:
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2
1	1	$xx	overlay color 3

Table 3. Pixel and Overlay Control Truth Table.

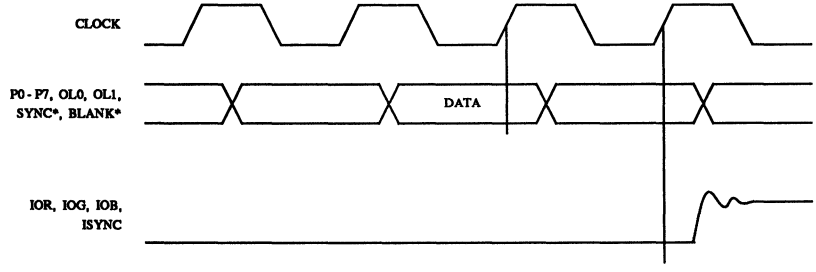
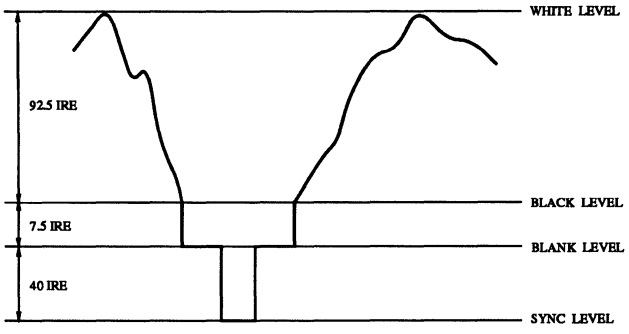


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 280 ohms, VREF = 1.235v. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 280 ohms, VREF = 1.235v. ISYNC connected to IOG.

Table 4. Video Output Truth Table.

Pin Descriptions

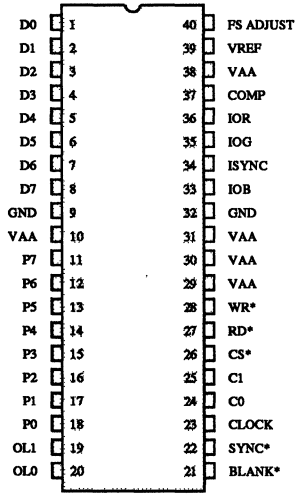
Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 4. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. This high impedance current source is typically connected directly to the IOG output (Figure 4), and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is: ISYNC (mA) = 1,728 * VREF (v) / RSET (ohms) If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is (assuming ISYNC is connected to IOG): RSET (ohms) = 6,047 * VREF (v) / IOG (mA) The relationship between RSET and the full scale output current on IOR and IOB is: IOR, IOB (mA) = 4,319 * VREF (v) / RSET (ohms)

Pin Descriptions (continued)

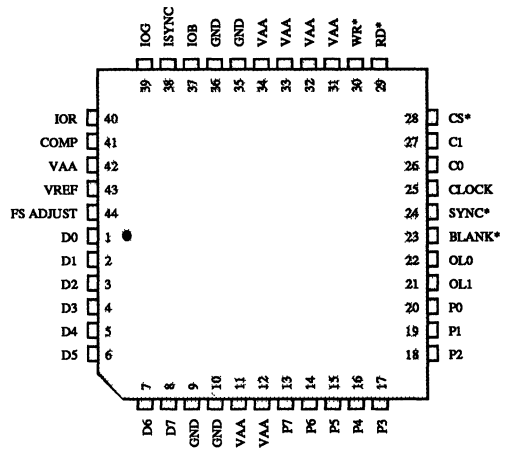
Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.2v (typical) reference. The Bt453 has an internal pull-up resistor between VREF and VAA. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black level. Note that the Bt453 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

40-pin DIP Package



44-pin Plastic J-Lead (PLCC) Package



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt453 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt453 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt453, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt453.

Power Planes

The Bt453 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within three inches of the Bt453.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt453 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the three groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt453 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt453 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt453 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

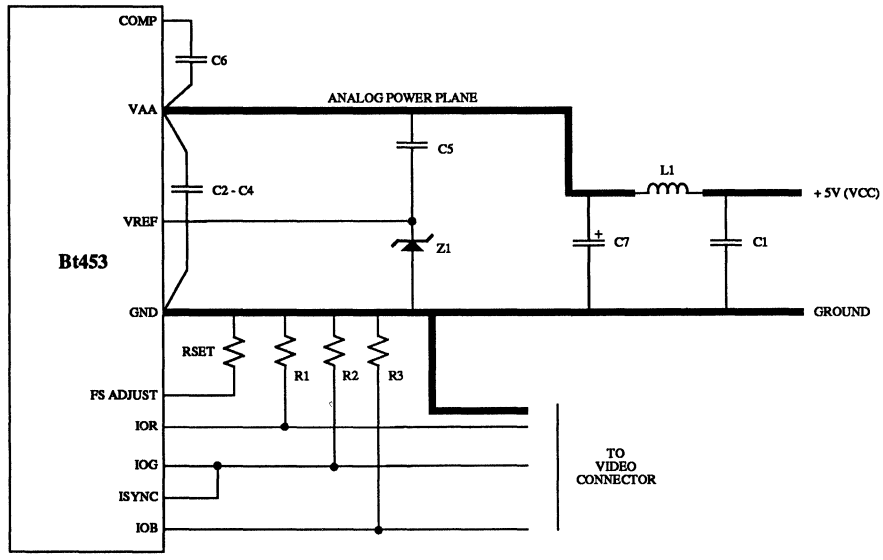
Analog Signal Interconnect

The Bt453 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt453 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C6	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C7	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	280-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt453.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts
FS ADJUST Resistor	RSET		280		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			10	µA
Output Capacitance	CDOUT		20		pF
Analog Outputs					
Gray Scale Current Range		15		22	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching (25°- 70° C.)			2	5	%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		30		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.12	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 ohms, VREF = 1.235v, ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		66 MHz Devices			40 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			66			40	MHz
CS*, C0, C1 Setup Time	1	35			35			ns
CS*, C0, C1 Hold Time	2	35			35			ns
RD*, WR* High Time	3	25			25			ns
RD* Asserted to Data Bus Driven	4	5			5			ns
RD* Asserted to Data Valid	5			100			100	ns
RD* Negated to Data Bus 3-Stated	6			15			15	ns
WR* Low Time	7	50			50			ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	5			5			ns
Pixel and Control Setup Time	10	5			7			ns
Pixel and Control Hold Time	11	2			3			ns
Clock Cycle Time	12	15			25			ns
Clock Pulse Width High Time	13	5			7			ns
Clock Pulse Width Low Time	14	5			7			ns
Analog Output Delay	15		20	30		20	30	ns
Analog Output Rise/Fall Time	16		3			3		ns
Analog Output Settling Time*	17		25			25		ns
Clock and Data Feedthrough*			- 48			- 48		dB
Glitch Impulse*			50			50		pV - sec
DAC to DAC Crosstalk			- 22			- 22		dB
Analog Output Skew			1	2		1	2	ns
Pipeline Delay	18	2	2	2	2	2	2	Clocks
VAA Supply Current**	IAA		220	275		190	250	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 ohms, VREF = 1.235v, ISYNC connected to IOG. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Timing Waveforms

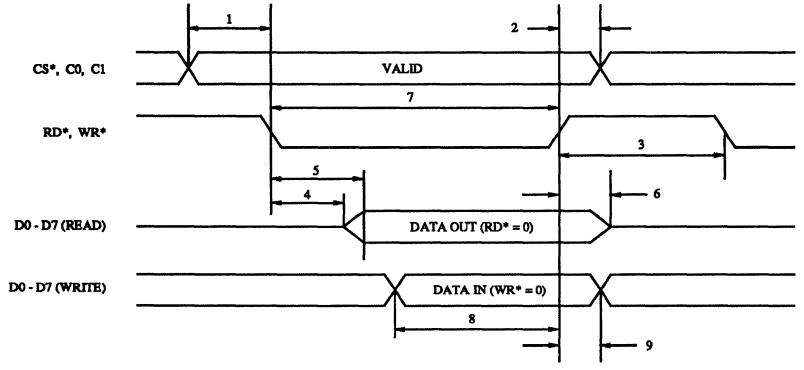
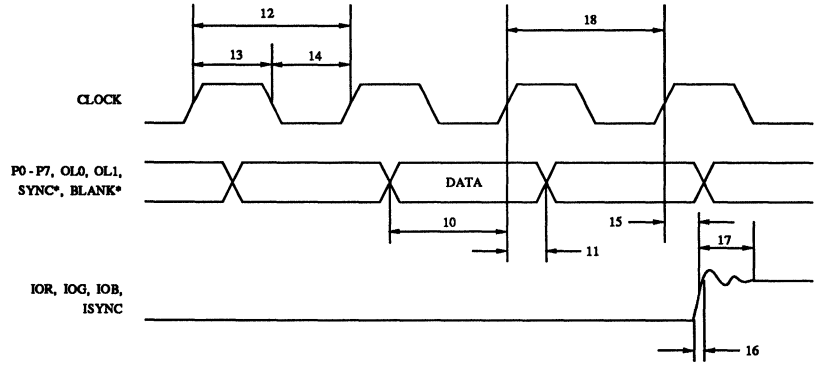


Figure 5. MPU Read/Write Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt453KP66	66 MHz	40-pin 0.6" Plastic DIP	0° to +70° C.
Bt453KPJ66	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt453KC66	66 MHz	40-pin 0.6" CERDIP	0° to +70° C.
Bt453KC	40 MHz	40-pin 0.6" CERDIP	0° to +70° C.
Bt453KP	40 MHz	40-pin 0.6" Plastic DIP	0° to +70° C.
Bt453KPJ	40 MHz	44-pin Plastic J-Lead	0° to +70° C.

Device Circuit Data

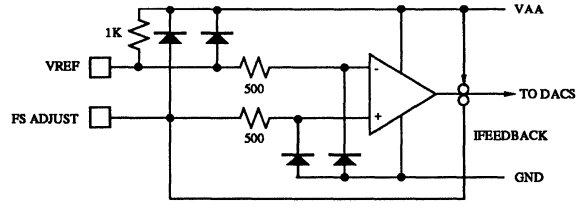


Figure 7. Equivalent Circuit of the Reference Amplifier.

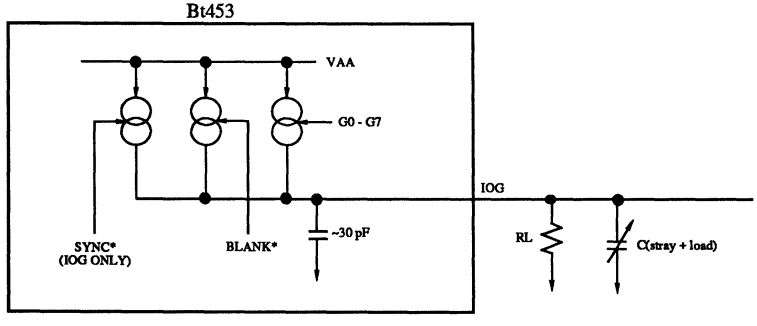


Figure 8. Equivalent Circuit of the Current Output (IOG).

Bt454

170 MHz

Monolithic CMOS

16 x 12 Color Palette

RAMDAC™

Distinguishing Features

- 170, 110 MHz Operation
- 4:1 Multiplexed TTL Pixel Ports
- Triple 4-bit D/A Converters
- 16 x 12 Dual Port Color Palette
- 1 x 12 Dual Port Overlay Palette
- RS-343A Compatible Outputs
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 1 W

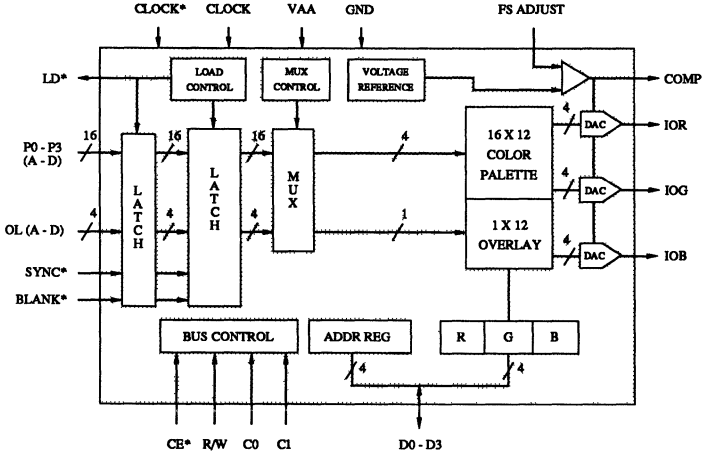
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Desktop Publishing

Related Products

- Bt451

Functional Block Diagram



Product Description

The Bt454 is a triple 4-bit video RAMDAC, designed specifically for high performance, high resolution color graphics. The architecture enables the display of 1600 x 1200 bit mapped color graphics (up to 4 bits per pixel plus one bit of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 42.5 MHz) to the frame buffer, while maintaining the 170 MHz video data rates required for sophisticated color graphics.

The Bt454 supports up to 17 simultaneous colors from a 4096 color palette. On chip features include a temperature compensated precision voltage reference, divide by four of the clock for load generation, color overlay capability, and a dual-port color palette RAM.

The Bt454 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1/4 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt454 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay register allow color updating without contention with the display refresh process.

As shown in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which color palette RAM entry or overlay register will be accessed by the MPU. The address register is used to address the internal RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data to the color palette RAM, the MPU loads the address register with the desired RAM location to be modified. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue write cycle, the address register increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data from the color palette RAM, the MPU loads the address register with the desired RAM location to be read. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $0 following the blue read or write cycle to location $F.

To read from or write to the overlay register, the MPU, using C0 and C1 to select the overlay register, performs three successive read or write cycles (4 bits each of red, green, and blue). ADDR0 - 3 are not used.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 1. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other four bits of the address register (ADDR0 - 3) are accessible to the MPU, and are used to address the color palette RAM locations.

When reading or writing the color values, the RAM or overlay register is accessed each time a 4-bit color value is read or written.

Although the color palette RAM and overlay register are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU, it is possible for one or more of the pixels on the display screen to be disturbed.

Figure 1 illustrates the MPU read/write timing when accessing the device.

Circuit Description (continued)

	Value	C1	C0	CE*	R/W	Addressed by MPU
ADDRa, b (counts modulo 3)	00		1			red value
	01		1			green value
	10		1			blue value
ADDR0 - 3 (counts binary)	$x	0	0	0	0	write to address register
	$0 - $F	0	1	0	0	write to color palette RAM
	$x	1	0	0	0	D0 - D3 ignored, 0 --> ADDRa, b
	$x	1	1	0	0	write to overlay register
	$x	0	0	0	1	read address register
	$0 - $F	0	1	0	1	read color palette RAM
	$x	1	0	0	1	0 --> D0 - D3, 0 --> ADDRa, b
	$x	1	1	0	1	read overlay register
	$x	x	x	1	x	3-state D0 - D3

Table 1. Address Register (ADDR) Operation.

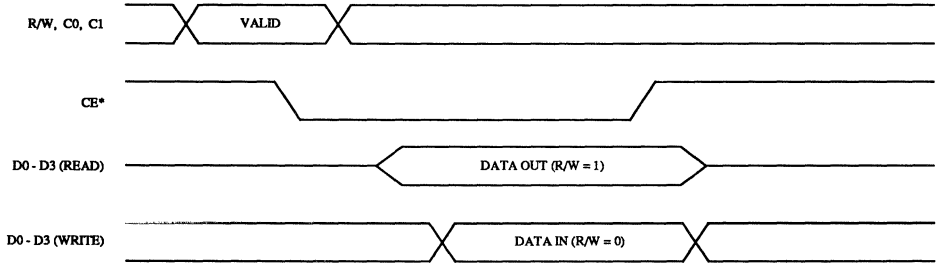


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 42.5 MHz), the Bt454 incorporates internal latches and multiplexers. As illustrated in Figure 2, the SYNC*, BLANK*, P0 - P3 {A - D}, and OL {A - D} inputs are latched on the rising edge of LDOUT. Note that with this configuration, the sync and blank timing will be recognized only with four pixel resolution. Typically, the LDOUT signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs of the frame buffer.

The overlay inputs may have pixel timing, facilitating the use of an additional bit plane in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

The Bt454 generates the LDOUT signal internally by dividing the clock by four. LDOUT is the setup and hold time reference for the pixel, overlay, sync, and blank inputs. It is recommended that LDOUT be buffered to clock the shift registers of the video DRAMs.

Once the pixel and overlay data are latched by LDOUT, they are internally multiplexed at the pixel clock rate. On each clock cycle, the Bt454 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four pixels have been output, at which point the cycle repeats.

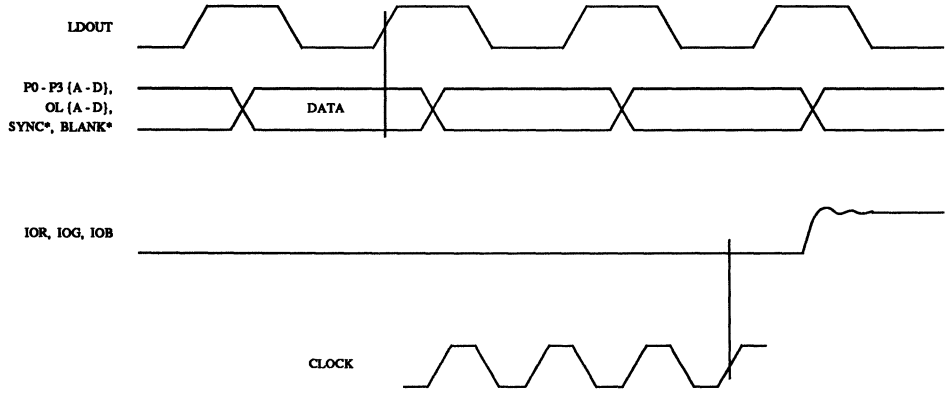


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Each clock cycle, four bits of color information (P0 - P3) and one bit of overlay information (OL) for each pixel are used to determine whether a color palette entry in the RAM or whether the overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Every clock cycle, the selected 12 bits of color information (4 bits each of red, green, and blue) are presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt454 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full scale output current against temperature and power supply variations.

CRT Monitor Interface

The analog outputs are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable, when soldered directly to a PC board. When the device is socketed, it is recommended that only a singly-terminated 75-ohm load be used (unless air flow or heat sinking are available). Note that when driving a singly-terminated 75-ohm load, the RSET value must be adjusted.

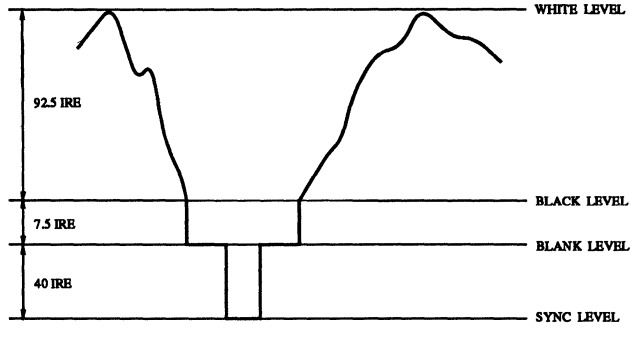
5

OL	P0 - P3	Addressed by frame buffer
0	$0	color palette entry $0
0	$1	color palette entry $1
:	:	:
0	$F	color palette entry $F
1	$x	overlay color

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 523 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full scale IOG = 26.67 mA. RSET = 523 ohms.

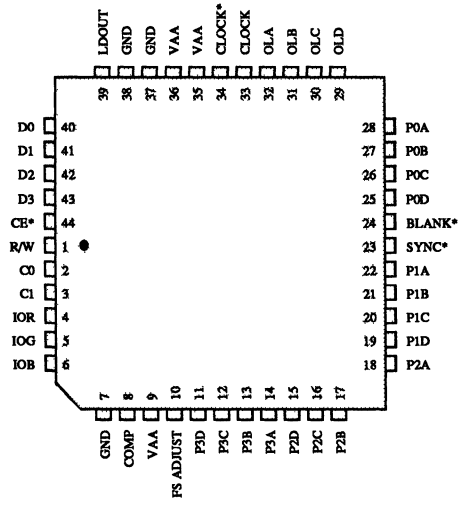
Table 3. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LDOUT. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LDOUT. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LDOUT	Load control output (TTL compatible). The P0 - P3 {A - D}, OL {A - D}, BLANK*, and SYNC* inputs are latched on the rising edge of LDOUT. LDOUT is internally generated by dividing the clock by four.
P0 - P3 {A - D}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 16 entries in the color palette RAM is to be used to provide color information. Four consecutive pixels (up to four bits per pixel) are input through this port. They are latched on the rising edge of LDOUT. P0 is the LSB. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four pixels have been output, at which point the cycle repeats.
OL {A - D}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LDOUT, specify which palette is to be used for color information. A logical zero indicates the color palette RAM is to provide color information, while a logical one indicates the overlay register is to provide color information. When accessing the overlay palette, the P0 - P3 {A - D} inputs are ignored. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
GND	Analog ground. All GND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = 13,948 / IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = 9,963 / RSET (ohms)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible low frequency power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 volt) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D3	Data bus (TTL compatible). Data is transferred into and out of the device over this four bit bidirectional data bus. D0 is the least significant bit.



PC Board Layout Considerations

PC Board Considerations

It is recommended that a four layer PC board be used with the Bt454. The layout should be optimized for lowest noise on the Bt454 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt454 ground pins, power supply bypass circuitry for the Bt454, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt454.

Power Planes

The Bt454 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within three inches of the Bt454.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt454 power pins and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor should be used to decouple each of the two groups of VAA pins (pins 35, 36; 9) to GND. These capacitors should be placed as close as possible to the device. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the Bt454 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt454 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt454 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

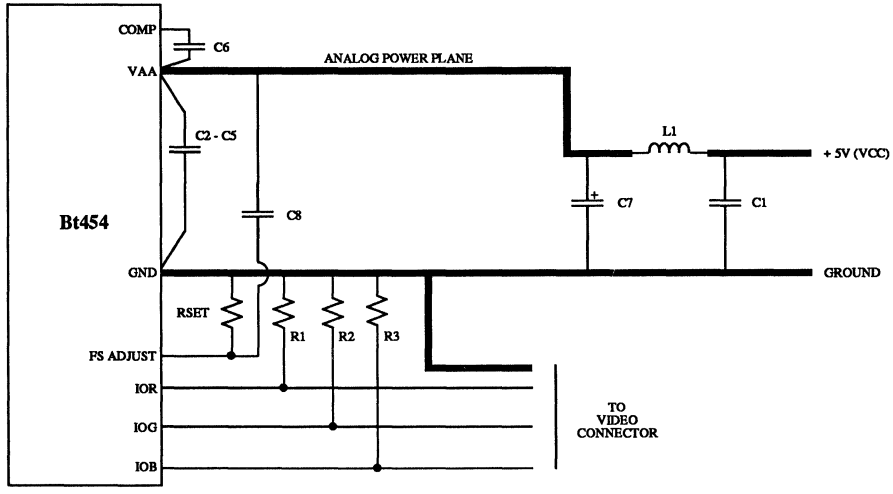
Analog Signal Interconnect

The Bt454 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt454 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C7	10 µF tantalum capacitor	Mallory CSR13G106KM
C2, C3, C6, C8	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C4, C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	523-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt454.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

LDOUT Termination

To reduce reflections on the LDOUT signal, it should be terminated at the point furthest from the Bt454. A 330-ohm resistor to VCC and a 470-ohm resistor to GND should work in most cases.

TTL Clock Interfacing

Figure 5 illustrates interfacing the Bt454 to a TTL clock. The MC10H116 is operated from a single +5v supply. The resistor network attenuates the TTL levels to MECL input levels. Although not shown, both the CLOCK and CLOCK* lines require termination resistors (220-ohm resistor to VCC and 330-ohm resistor to GND), located as close as possible to the Bt454.

ECL Clock Generation

Due to the high clock rates at which the Bt454 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 volts. Note that the CLOCK and CLOCK* inputs require termination resistors (220-ohm resistor to VCC and 330-ohm resistor to GND), located as close as possible to the Bt454.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt454 will not function using a single-ended CLOCK with CLOCK* connected to ground.

A 10K or 10KH ECL crystal oscillator that generates differential outputs, operating between +5v and ground, may be interfaced directly to the B454, as shown in Figure 6. If the crystal oscillator generates only a single-ended output, a MC10H116 may be used to generate the differential clock signals, as illustrated in Figure 7. If the MC10H116 is not readily available, a MC10H101, MC10H105, or MC10H107 may be used.

Although ECL works well using a single +5 volt supply, care must be taken to isolate the TTL power supply lines from the ECL power supply. Further information on ECL design may be obtained in the MECL Device Data Catalog and the MECL System Design Handbook, by Motorola.

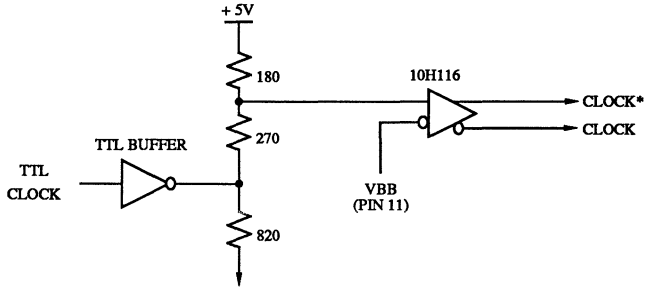


Figure 5. Interfacing the Bt454 to a TTL Clock.

Application Information (continued)

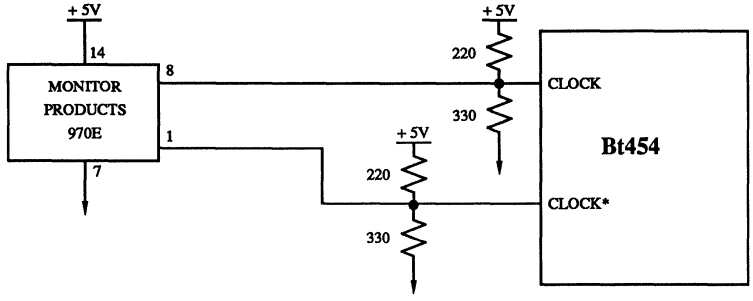


Figure 6. Interfacing to a Differential ECL Oscillator.

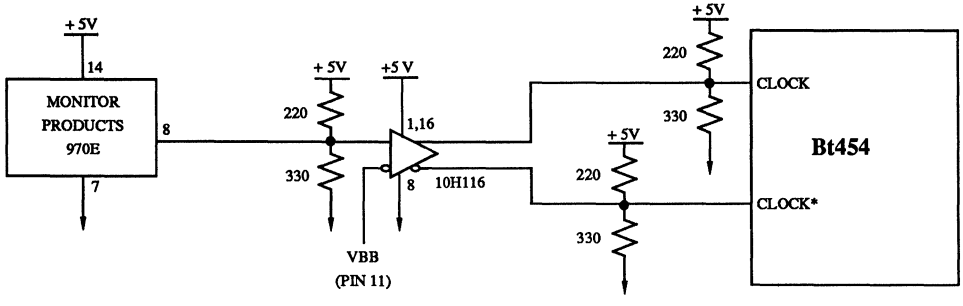


Figure 7. Interfacing to a Single-Ended ECL Oscillator.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1/4	LSB
Differential Linearity Error	DL			± 1/4	LSB
Gray Scale Error				± 10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
(except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance	CIN		10		pF
(f = 1 MHz, Vin = 2.4v)					
Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA - 1.0		VAA + 0.5	Volts
Input Low Voltage	VKIL	GND - 0.5		VAA - 1.6	Volts
Input High Current (Vin = 4.2v)	IKIH			1	µA
Input Low Current (Vin = 3.2v)	IKIL			- 1	µA
Input Capacitance	CKIN		10		pF
(f = 1 MHz, Vin = 4.2v)					
Digital Outputs					
Output High Voltage	VOH				
D0 - D3 (IOH = -400 µA)		2.4			Volts
LDOUT (IOH = -12 mA)		2.4			Volts
Output Low Voltage	VOL				
D0 - D3 (IOL = 3.2 mA)				0.4	Volts
LDOUT (IOL = 24 mA)				0.5	Volts
3-state Current (D0 - D3)	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			1.175		mA
DAC to DAC Matching				5	%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	RAOUT		50		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		20		pF
Internal Reference Voltage	VREF	1.18	1.22	1.26	Volts
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		170 MHz Devices			110 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			170			110	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	10			10			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	10			10			ns
LDOUT Pulse Width High	10	9			13			ns
LDOUT Pulse Width Low	11	9			13			ns
Clock to LDOUT	12	4	7.5	14.3	4	7.5	14.3	ns
Pixel and Control Setup Time	13	0			0			ns
Pixel and Control Hold Time	14	3			5			ns
Clock Cycle Time	15	5.88			9			ns
Clock Pulse Width High	16	2			3.6			ns
Clock Pulse Width Low	17	2			3.6			ns
Analog Output Delay	18		20			20		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time*	20			6			9	ns
Clock and Data Feedthrough*			70			70		pV - sec
Glitch Impulse*			50			50		pV - sec
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		6	6	6	6	6	6	Clocks
VAA Supply Current**	IAA		200			120	200	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are 3.2 to 4.2 volts, with input rise/fall times ≤ 2 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D3 output load ≤ 40 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v, TA = 20° C. IAA (max) at VAA = 5.25v, TA = 0° C.

Timing Waveforms

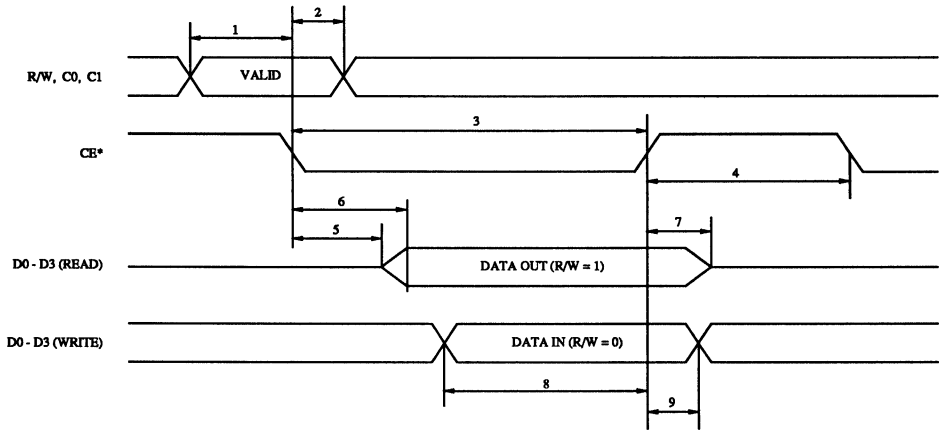
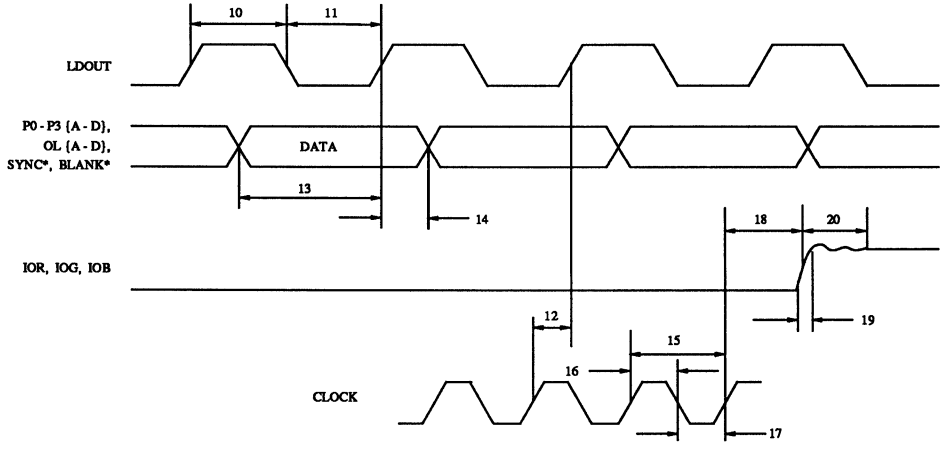


Figure 8. MPU Read/Write Timing.



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ± 1/4 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt454KPJ	110 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt454KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C.

Device Circuit Data

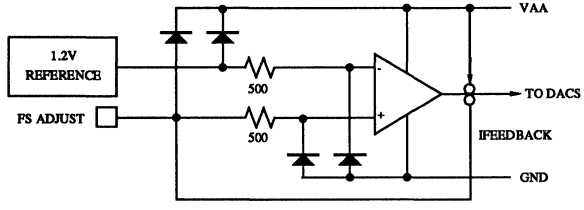


Figure 10. Equivalent Circuit of the Reference Amplifier.

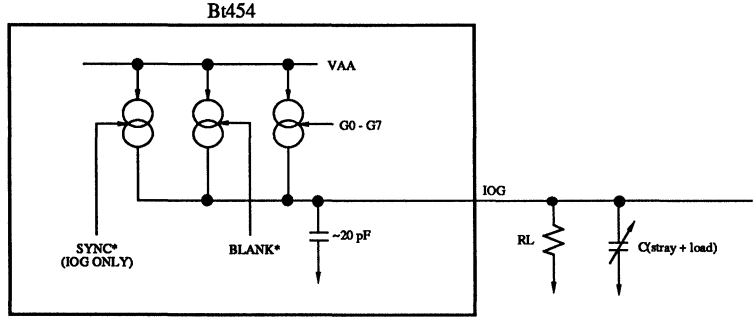


Figure 11. Equivalent Circuit of the Current Output (IOG).

Bt459

135 MHz

Monolithic CMOS

256 x 24 Color Palette

RAMDAC™

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 135, 110, 80 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- 1, 2, 4, or 8 Bits per Pixel
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X-windows Support for Overlays/Cursor
- Standard MPU Interface
- 132-pin PGA Package

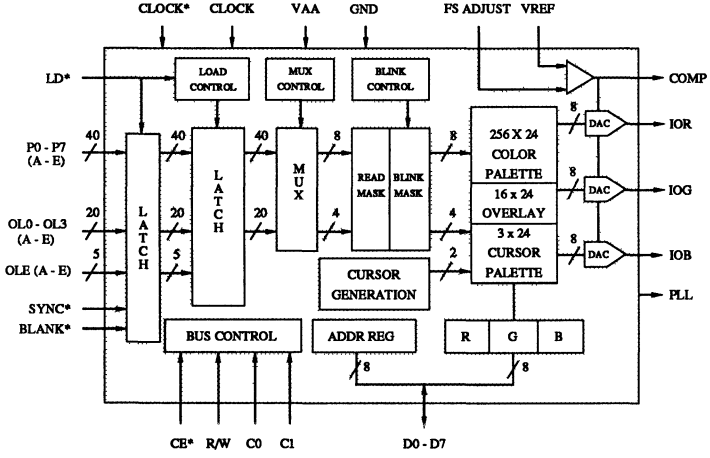
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt460, Bt461, Bt468

Functional Block Diagram



Product Description

The Bt459 triple 8-bit RAMDAC is designed specifically for high performance, high resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, and 1x to 16x integer zoom support.

Pixel data may be input as 1, 2, 4, or 8 bits per pixel. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X-windows support.

The Bt459 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt459 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

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L459001 Rev. F

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt459 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register have two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0 - 11) are accessible to the MPU. ADDR12 - ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The only time the address register resets to $0000 is after accessing location $0FFF (due to wraparound).

ADDR0 - 15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0 - 7)
$xxxx	01	address register (ADDR8 - 15)
$0000 - $00FF	10	reserved
$0100	10	overlay color 0*
:	10	:
$010F	10	overlay color 15*
$0181	10	cursor color register 1*
:	:	cursor color register 2*
$0183	10	cursor color register 3*
$0200	10	ID register ($4A)
$0201	10	command register 0
$0202	10	command register 1
$0203	10	command register 2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red signature register
$020D	10	green signature register
$020E	10	blue signature register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400 - $07FF	10	cursor RAM
$0000 - $00FF	11	color palette RAM*

*Indicates requires three read/write cycles -- RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Although the color palette RAM, overlay RAM, and cursor color registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers and cursor RAM is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt459.

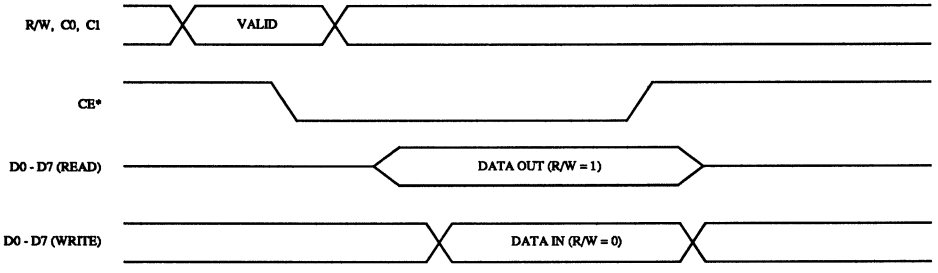


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt459 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either one, four, or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with one, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt459 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

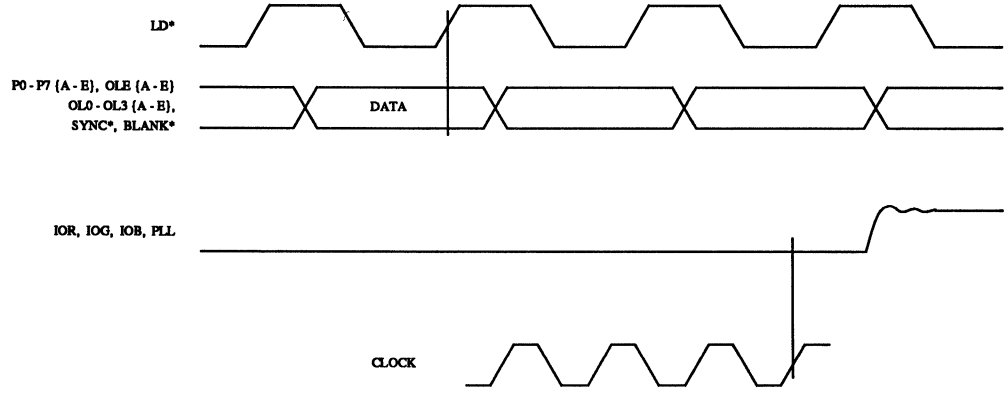


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

If 1:1 multiplexing is specified, LD* is also used for clocking the Bt459 (at a maximum of 66 MHz). The rising edge of LD* still latches the P0 - P7 {A}, OL0 - OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. Note that CLOCK must still run, but is ignored.

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0 - P7) and four bits of overlay information (OL0 - OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e. in the middle of the screen), the Bt459 monitors the BLANK* input to determine vertical retrace intervals.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 4 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register1 specifies by how many clock cycles to pan. Only the pixel inputs and underlays are panned, overlays are not. Panning is done by delaying SYNC* and BLANK*, an additional 1, 2, 3, or 4 clock cycles.

If 0 pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all four or five pixels have been output, at which point the cycle repeats (note that this assumes the interleave select is pixel {A}).

If 1 pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt459 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0 pixel panning should be specified.

Note that the cursor position does not change relative to the edge of the display screen during panning.

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1	8	32	40	1
2	4	16	20	4
4	2	8	10	16
8	1	4	5	256

Table 2. Block Mode Operation.

Circuit Description (continued)

Pixel Zoom

The Bt459 supports 1x to 16x integer zoom through the use of pixel replication. Only the P0 - P7 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, etc. 3x zooming is similar, except each pixel is output for 3 clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate. Regardless of the zoom factor, P0 - P7 data is latched every LD* cycle.

During 2x zoom, new P0 - P7 data must be presented every two LD* cycles. During 3x zoom, new P0 - P7 data must be presented every three LD* cycles. The pixel data must be held at the P0 - P7 {A - E} inputs for the appropriate number of LD* cycles until new P0 - P7 information is needed. OL0 - OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Note that in the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits pixel), 1x zoom must be specified.

Figure 3 illustrates the zoom timing.

Block Mode Operation

The Bt459 supports loading of pixel data at 1, 2, 4, or 8 bits per pixel. Only the P0 - P7 inputs are affected.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate, regardless of the block mode. Regardless of the block mode, P0 - P7 data is latched every LD* cycle.

1 Bit per Pixel (RA1 - RA7 = 0) RA0 =	2 Bits per Pixel (RA2 - RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4 - RA7 = 0) RA3 - RA0 =	8 Bits per Pixel RA7 - RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Note: Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0 - P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode.

Table 3. Block Mode Operation (RA = Color Palette RAM Address).

Circuit Description (continued)

For 8 bits per pixel, new P0 - P7 information must be presented every LD* cycle. For 4 bits per pixel, new P0 - P7 information must be presented every two LD* cycles. For 2 bits per pixel, new P0 - P7 information must be presented every four LD* cycles. For 1 bit per pixel, new P0 - P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0 - P7 inputs for the appropriate number of LD* cycles until new P0 - P7 information is needed. OL0 - OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Tables 2 and 3 show the block mode operation, and the addressing of the color palette RAM.

Figure 4 illustrates the block mode timing (4 bits per pixel).

Note that in the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0 pixel interleave must be selected.

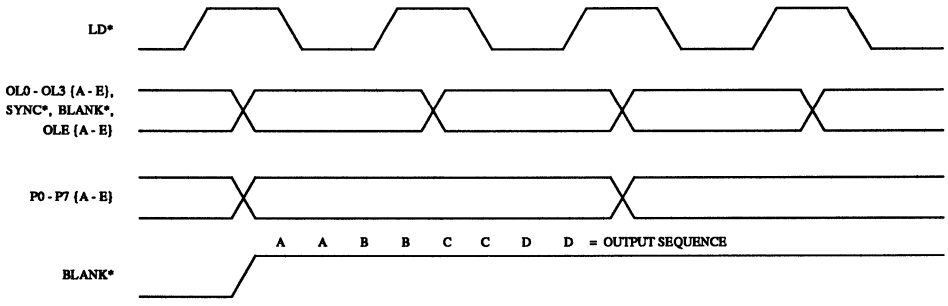


Figure 3. Zoom Input Timing.
(8 Bits per Pixel, 2x Zoom, 4:1 Multiplexing)

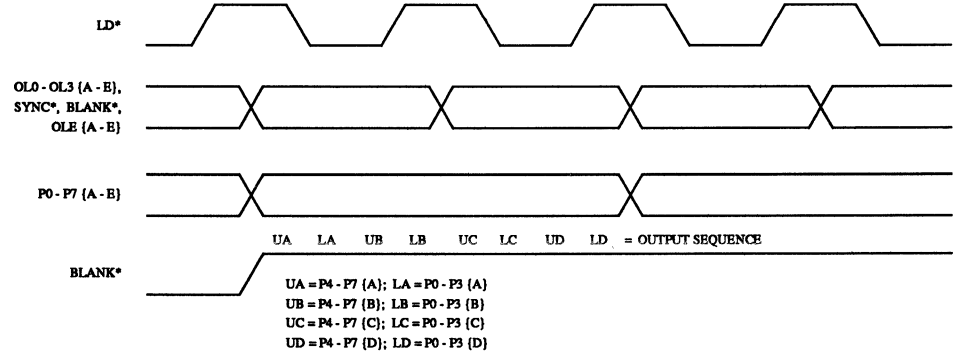


Figure 4. Block Mode Input Timing.
(4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing)

Circuit Description (continued)

On-Chip Cursor Operation

The Bt459 has an on-chip three-color 64 x 64 pixel user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done via the cursor (x,y) register. Note that the Bt459 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking.

Three Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides two bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

(0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each "plane" of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63).

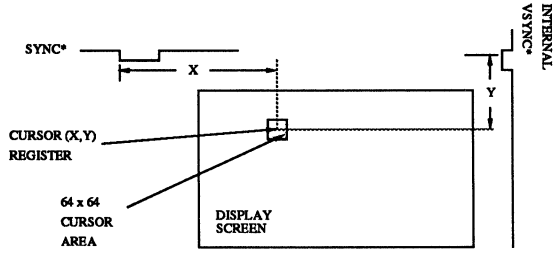


Figure 5. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking.

5

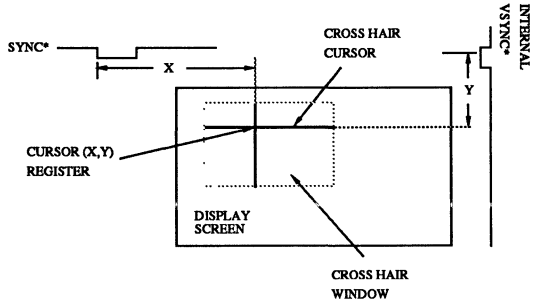


Figure 6. Cross Hair Cursor Positioning

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixel in the horizontal and vertical direction, there will be a one pixel offset from being truly centered about the cross hair cursor.

Figure 7 illustrates displaying the dual cursors.

During the 64 x 64 pixel area in which the user-definable cursor would be displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will be dependent on the cursor pattern, whether they are logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X-Windows Cursor Mode

In the X-windows mode, plane 1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Figure 12 as to the organization of the cursor RAM while in the X-windows mode.

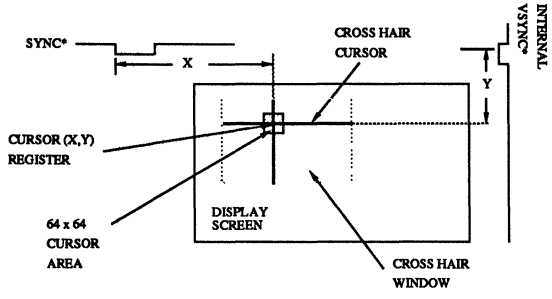


Figure 7. Dual Cursor Positioning.

Circuit Description (continued)

Overlay / Underlay Operation

The overlay inputs (OL0 - OL3 and OLE) may operate in three modes: normal overlays, X-windows overlays, or provide an underlay, as shown in Tables 4 and 5.

Overlay and underlay information may be displayed on a pixel basis. Note that overlays and underlay may both be used. If using X-windows overlays, the underlay is not available.

The priority of display operation is:

cursor
overlays
pixel data
underlays

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0 - OL3	P0 - P7	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xx	cursor color 3	
10	x	x	x	x	$x	$xx	cursor color 2	
01	x	x	x	x	$x	$xx	cursor color 1	
00	0	0	x	x	$F	$xx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$00	RAM location $00	
00	0	0	x	0	$0	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$FF	RAM location $FF	
00	x	1	1	x	$F	$xx	overlay color 15	X-windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xx	overlay color 1	
00	x	1	1	x	$0	$xx	overlay color 0	
00	x	1	0	0	$x	$00	RAM location $00	
00	x	1	0	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$FF	RAM location $FF	
00	1	0	x	x	$F	$xx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xx	overlay color 1	
00	1	0	1	x	$0	$00	overlay color 0 (underlay)	
00	1	0	0	0	$x	$00	RAM location $00	
00	1	0	x	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$FF	RAM location $FF	

Note: Refer to Figure 8 for generation of Cursor1 and Cursor0 control bits.

Table 4. Palette and Overlay Select Truth Table.

Circuit Description (continued)

In normal overlay mode, the overlay enable inputs, OLE {A - E} are ignored, and typically only 15 overlays are available. Graphics information (P0 - P7) would be displayed only when no overlay information is present (OL0 - OL3 = 0000).

In the X-windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0 - OL3. If OLE = 0, the OL0 - OL3 inputs are ignored and P0 - P7 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1, the underlay is displayed if P0 - P7 = 0; if P0 - P7 ≠ 0, then pixel data is displayed. Note that overlay color 0 is used for underlay color information.

	P0 - P7 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	yes	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	yes	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt459 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full scale output current against temperature and power supply variations.

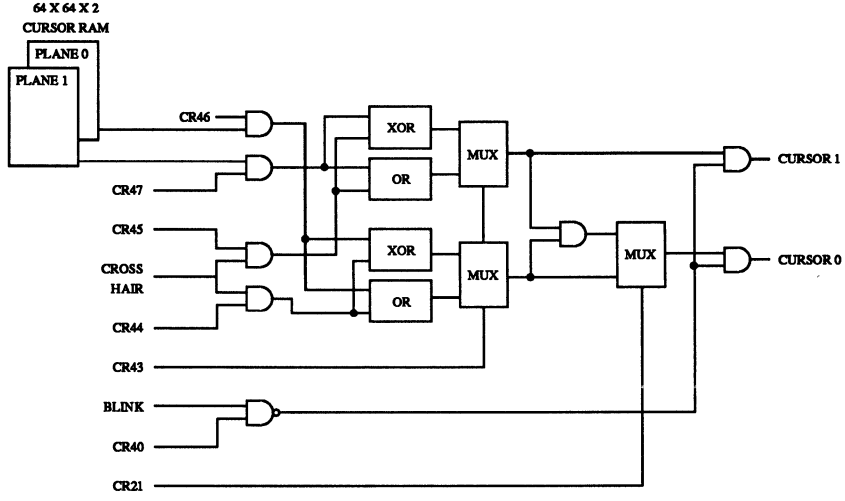
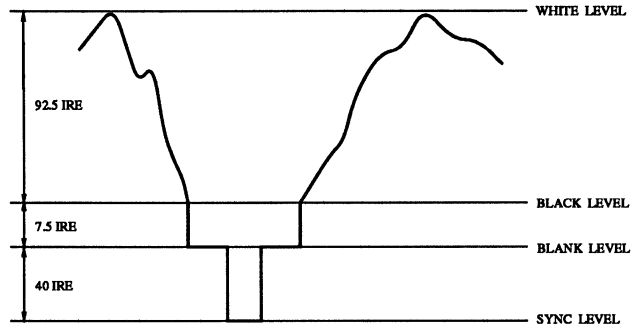


Figure 8. Cursor Control Circuitry.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 523 ohms, VREF = 1.235v. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

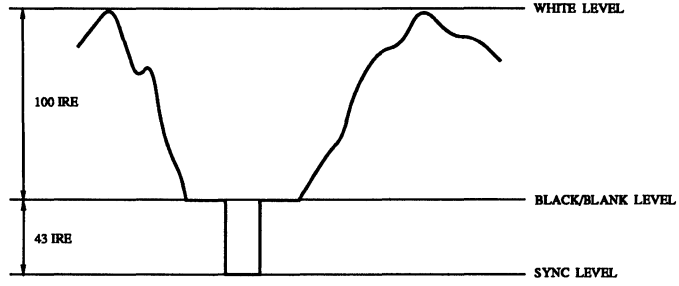
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 523 ohms, VREF = 1.235v. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 495 ohms, VREF = 1.235v. Blank pedestal = 0 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 495 ohms, VREF = 1.235v. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 5:1 multiplexing

These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored.

Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, is must remain running.

Note that it is possible to reset the pipeline delay of the Bt459 to a fixed 8 clock cycles. In this instance, each time the input multiplexing is changed, the Bt459 must again be reset to a fixed pipeline delay.

CR05 Overlay 0 enable

(0) use color palette RAM
(1) use overlay color 0

When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 4.

CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off). The counters that determine the blink rate are reset when command register0 is written to.

CR01, CR00 Block mode

(00) 8 bits per pixel
(01) 4 bits per pixel
(10) 2 bits per pixel
(11) 1 bit per pixel

These bits specify whether the pixel data is input as 1, 2, 4, or 8 bits per pixel. Note that only the P0 - P7 inputs are affected.

Internal Registers (continued)

Command Register1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17 - CR15 Pan select

(000) 0 pixels {pixel A}
(001) 1 pixel {pixel B}
(010) 2 pixels {pixel C}
(011) 3 pixels {pixel D}
(100) 4 pixels {pixel E}
(101) reserved
(110) reserved
(111) reserved

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval, and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc.

Note that only pixel and underlay information is panned. Overlay information is not panned.

In the 1:1 multiplex mode, 0 pixels should be specified.

CR14 reserved (logical zero)

CR13 - CR10 Zoom factor

(0000) 1x
(0001) 2x
:
(1111) 16x

These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, etc. For 3x zoom, pixel {A} is output for three clock cycles, etc.

In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected.

Note that only P0 - P7 are zoomed.

Internal Registers (continued)

Command Register2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt459 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt459 to emulate a single-channel RAMDAC using only the green channel. The Bt459 expects color data be to input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information. The value is loaded into or read from the green color palette RAM.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	X-windows overlay select (0) normal overlays (1) X-windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X-window environment (logical one).
CR21	X-windows cursor select (0) normal cursor (1) X-windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X-window compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37 - CR35 Interleave select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
(110) reserved
(111) reserved

These bits specify the order in which the pixels are to be output, as shown in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line.

The phrase "repeats every x" in table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1 pixel interleave select, ABCD would be repeated every 4th scan line.

In the 1:1 input multiplex mode, a value of 0 pixels (000) must be specified.

CR34 - CR32 First pixel select

(000) pixel {A}
(001) pixel {B}
(010) pixel {C}
(011) pixel {D}
(100) pixel {E}
(101) reserved
(110) reserved
(111) reserved

These bits are used to support panning in the Y direction with an interleaved frame buffer. Due to the interleave capability, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode.

These bits are ignored in the 1:1 multiplex mode.

CR31 Overlay interleave enable

(0) interleaving disabled
(1) interleave enabled

This bit specifies whether or not OL0 - OL3 and OLE are to be interleaving or not. If interleaving is enabled, the interleave factor and first pixel selection are the same as for P0 - P7. If interleaving is disabled, pixel {A} is always output first and no interleaving occurs.

CR30 Underlay enable

(0) underlay disabled
(1) underlay enabled

If command bit CR22 is a logical zero, this bit is used to enable or disable the underlay from being displayed. If CR22 is a logical one, this bit is ignored.

If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0 - P7 data is displayed. If OLE = 1, the underlay is displayed if P0 - P7 = 0, if P0 - P7 ≠ 0 then normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers (continued)

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	output sequence	scan line number	output sequence	scan line number
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers (continued)

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK*, but must must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If no zooming is done (1x zoom), the IZE* should always be a logical zero or connected directly to GND.

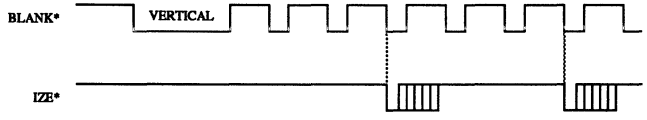


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt459, the value read by the MPU will be $4A. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A - E}) and D3 corresponds to overlay plane 3 (OL3 {A - E}). Bits D0 - D3 are logically ANDed with the corresponding overlay plane input. D4 - D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) a overlay plane from blinking at the blink rate and duty cycle specified by command register0. D0 corresponds to overlay plane 0 (OL0 {A - E}) and D3 corresponds to overlay plane 3 (OL3 {A - E}). In order for a overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4 - D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Red, Green, and Blue Signature Registers

Signature Operation

These three 8-bit signature registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a given value for the red, green, and blue signatures registers will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing", the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A - E) pixels can be captured each LD* cycle, D0 - D2 of the test register are used to specify which pixel (A - E) is to be captured.

Internal Registers (continued)

Test Register

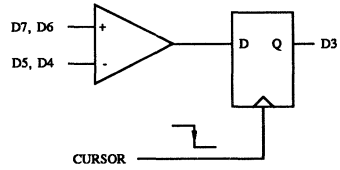
This 8-bit register is used for testing the Bt459. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is done on every fifth pixel. D0 - D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0 - D2 should select pixel A.

D3 - D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7 - D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3 - D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt459. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Note that plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is one, three, five, or seven pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4 - D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H - P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V - 32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0FC0 (-64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4 - D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H - P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4 - D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels, for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is two pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window. It is not initialized, and may be written to or read by the MPU at any time. As MPU accesses to the cursor RAM have priority over the cursor display process, the cursor RAM should not be accessed during the horizontal sync intervals to minimize contention of the cursor updating and displaying processes.

During MPU accesses to the cursor RAM, the address pointer register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM, as it appears on the display screen.

Note that in the X-windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: in both modes of operation, plane1 = D7, D5, D3, D1; plane0 = D6, D4, D2, D0.

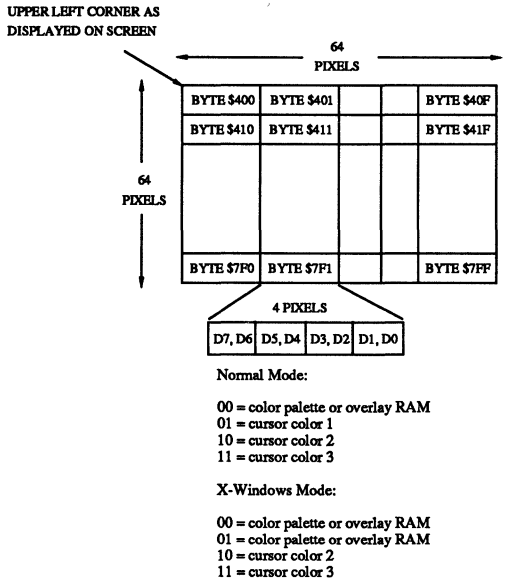


Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0 - P7 {A - E}, OL0 - OL3 {A - E}, OLE {A - E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is the output clock (1:1 multiplex mode) or is 1/4 or 1/5 of CLOCK, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the A.C. Characteristics section.
P0 - P7 {A - E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 4). Either one, four, or five consecutive pixels (up to eight bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all one, four, or five pixels have been output, at which point the cycle repeats.
OL0 - OL3 {A - E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*, and in conjunction with CR05 in command register0, specify which palette is to be used for color information, as illustrated in Table 4. When accessing the overlay palette RAM, the P0 - P7 {A - E} inputs are ignored. Overlay information (up to four bits per pixel) for either one, four, or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
OLE {A - E}	Overlay enable inputs (TTL compatible). In the X-windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates to display P0 - P7 information. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt459s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (v) / RSET (ohms) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 ohms).
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom while interleaving is not supported, this pin may be connected directly to GND.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 13). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 13). Note that the IRE relationships in Figures 9 and 10 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = K1 * VREF (v) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (v) / RSET (ohms) where K1 and K2 are defined as:

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 13. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 volt) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

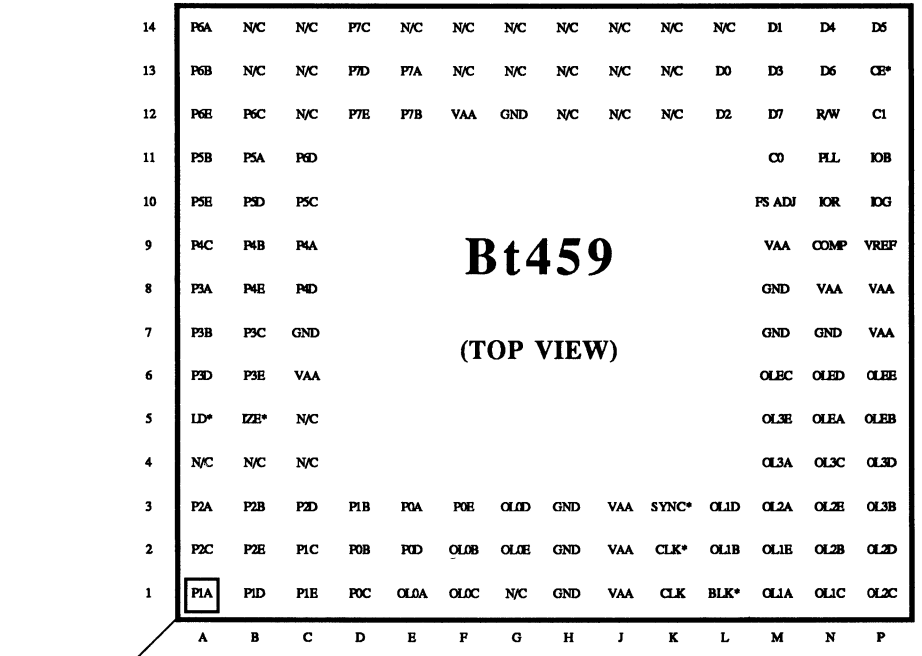
Pin Descriptions (continued)

Signal	Pin Number
BLANK*	L1
SYNC*	K3
LD*	A5
CLOCK	K1
CLOCK*	K2
IZE*	B5
P0A	E3
P0B	D2
P0C	D1
P0D	E2
P0E	F3
P1A	A1
P1B	D3
P1C	C2
P1D	B1
P1E	C1
P2A	A3
P2B	B3
P2C	A2
P2D	C3
P2E	B2
P3A	A8
P3B	A7
P3C	B7
P3D	A6
P3E	B6
P4A	C9
P4B	B9
P4C	A9
P4D	C8
P4E	B8
P5A	B11
P5B	A11
P5C	C10
P5D	B10
P5E	A10
P6A	A14
P6B	A13
P6C	B12
P6D	C11
P6E	A12
P7A	E13
P7B	E12
P7C	D14
P7D	D13
P7E	D12

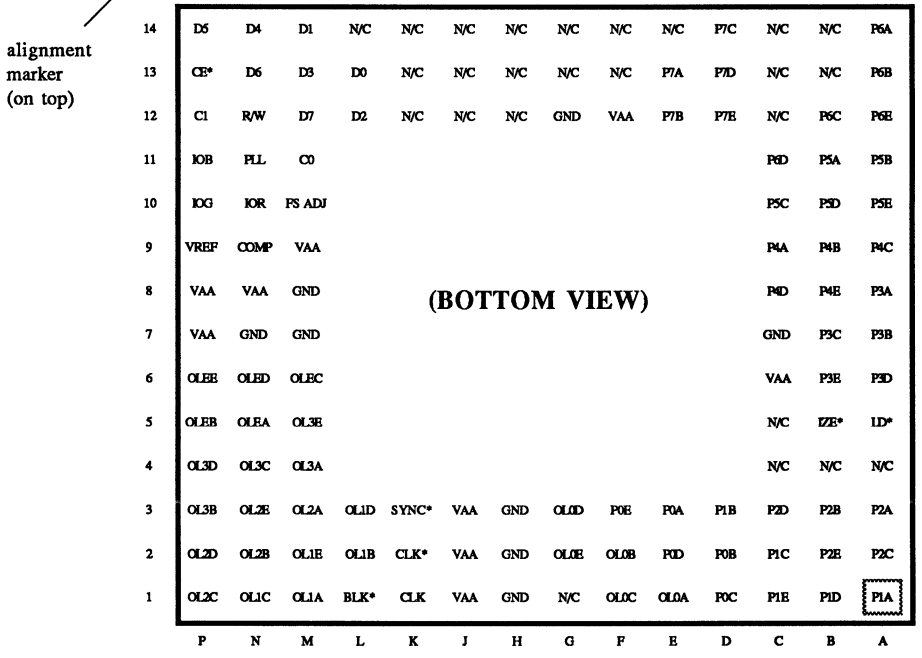
Signal	Pin Number
OL0A	E1
OL0B	F2
OL0C	F1
OL0D	G3
OL0E	G2
OL1A	M1
OL1B	L2
OL1C	N1
OL1D	L3
OL1E	M2
OL2A	M3
OL2B	N2
OL2C	P1
OL2D	P2
OL2E	N3
OL3A	M4
OL3B	P3
OL3C	N4
OL3D	P4
OL3E	M5
OLEA	N5
OLEB	P5
OLEC	M6
OLED	N6
OLEE	P6
IOG	P10
IOB	P11
IOR	N10
PLL	N11
VAA	J1
VAA	J2
VAA	J3
VAA	C6
VAA	F12
VAA	M9
VAA	P7
VAA	P8
VAA	N8

Signal	Pin Number
GND	H1
GND	H2
GND	H3
GND	C7
GND	G12
GND	M8
GND	M7
GND	N7
COMP	N9
FS ADJUST	M10
VREF	P9
CE*	P13
R/W	N12
C1	P12
C0	M11
D0	L13
D1	M14
D2	L12
D3	M13
D4	N14
D5	P14
D6	N13
D7	M12
reserved	G14
reserved	G13
reserved	F14
reserved	F13
reserved	E14
reserved	J13
reserved	J14
reserved	H12
reserved	H13
reserved	H14
reserved	C5
reserved	A4
reserved	B4
reserved	C4
reserved	C14
reserved	C13
reserved	B14
reserved	C12
reserved	B13
reserved	L14
reserved	K12
reserved	J12
reserved	K14
reserved	K13

Pin Descriptions (continued)



alignment marker (on top)



PC Board Layout Considerations

PC Board Considerations

It is recommended that a four layer PC board be used with the Bt459. The layout should be optimized for lowest noise on the Bt459 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt459 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt459, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt459.

Power Planes

The Bt459 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within three inches of the Bt459.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt459 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, three 0.1 µF ceramic capacitors in parallel with three 0.01 µF chip capacitors should be used to decouple the VAA pins to GND. These capacitors should be placed as close as possible to the device. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the Bt459 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt459 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground plane.

Due to the high clock rates involved, long clock lines to the Bt459 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

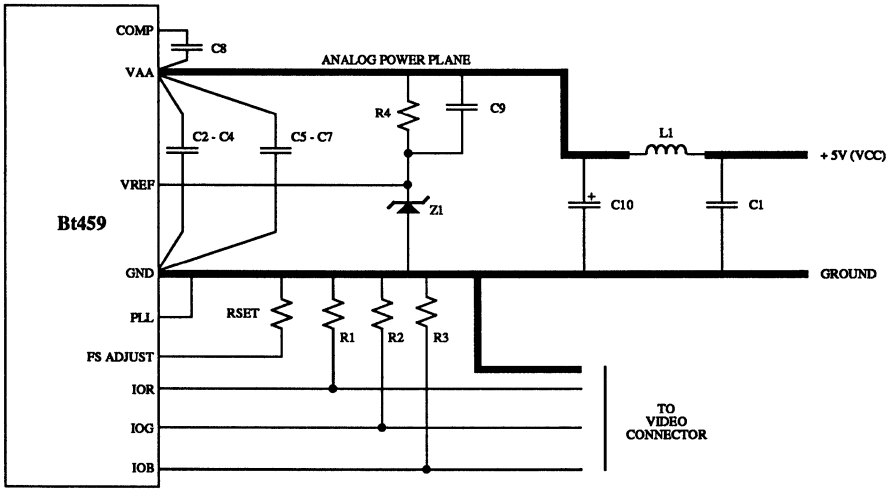
Analog Signal Interconnect

The Bt459 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch. Also, the external voltage reference circuitry should be as close as possible to the Bt459 to avoid noise pickup.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt459 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C5 - C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1000-ohm 1% metal film resistor	Dale CMF-55C
RSET	523-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385Z-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt459.

Figure 13. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt459 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 volts. Note that the CLOCK and CLOCK* inputs require termination resistors (220-ohm resistor to VCC and a 330-ohm resistor to GND). The termination resistors should be as close as possible to the Bt459.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt459 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt459 is being used, is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, and will also optionally set the pipeline delay of the Bt459 to eight clock cycles. The Bt438 may also be used to interface the Bt459 to a TTL clock. Figure 14 illustrates using the Bt438 with the Bt459.

When using a single Bt459, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 ohms).

Using Multiple Bt459s

For display applications where up to four Bt459s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, synchronizes them to sub-pixel resolution, and will also optionally set the pipeline delay of the Bt459 to eight clock cycles. The Bt439 may also be used to interface the Bt459 to a TTL clock. Figure 14 illustrates using the Bt439 with the Bt459.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt459, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt459s, and adjusts the phase each of the CLOCK and CLOCK* signals to the Bt459s to minimize the PLL phase difference.

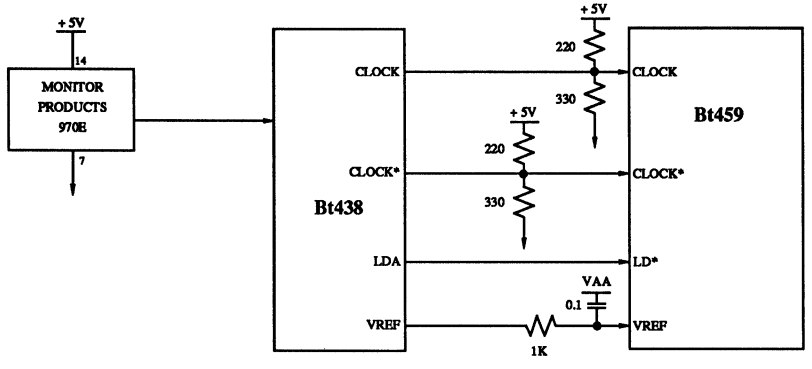


Figure 14. Generating the Bt459 Clock Signals.

Application Information (continued)

If sub-pixel synchronization of multiple Bt459s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt459s are connected together and driven by a single Bt438 (with distributed branch termination on each clock). The VREF inputs of the Bt459s must still be isolated by 1K-ohm resistors, as shown in Figure 15, and have a 0.1 µF bypass capacitor to VAA. The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt459s would not be used and should be connected to GND (either directly or through a resistor up to 150 ohms).

If located close together on the same PC board, multiple Bt459s may be connected to a single analog power plane. In addition, a single voltage reference may drive multiple devices. Each Bt459 must still have it's individual RSET resistor, IOUT termination resistor, power supply bypass capacitors, and COMP capacitor.

5

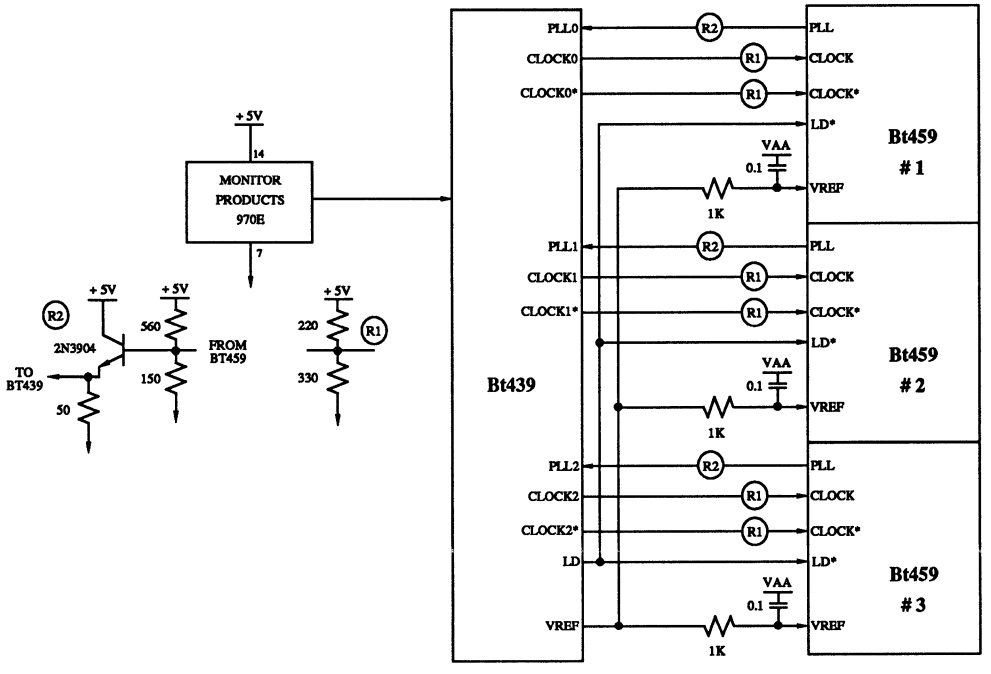


Figure 15. Generating the Clock Signals for Multiple Bt459s.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt459, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt459 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt459.

To reset the Bt459, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt459 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt459s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

Interleave Operation

To support interleaved frame buffers, the Bt459 may be configured for various interleave factors, as shown in Table 8. Table 9 shows an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 shows the same operation with pixel {B} selected as the starting pixel (the display has been panned down 3 scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown starting at the left-most displayed pixel.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information (continued)

Initializing the Bt459

Following a power-on sequence, the Bt459 must be initialized. This sequence will configure the Bt459 as follows:

4:1 multiplexed operation
no overlays, no blinking, no interleave
64 x 64 block cursor, no cross hair cursor
8 bits per pixel, no panning, no zoom
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to command register 1	10
Write $C0 to command register 2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern	
Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization	
Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization	
Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA - 1.0		VAA + 0.5	Volts
Input Low Voltage	VKIL	GND - 0.5		VAA - 1.6	Volts
Input High Current (Vin = 4.0v)	IKIH			1	µA
Input Low Current (Vin = 0.4v)	IKIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0v)	CKIN		4	10	pF
Digital Outputs (D0 - D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 0.5		+ 1.2	Volts
Output Impedance	RAOUT		50		K ohms
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
$\overline{\text{SYNC*}}/\overline{\text{BLANK*}}$ = 1		0	5	50	µA
Output Compliance		- 1.0		+ 2.5	Volts
Output Impedance			50		K ohms
Output Capacitance			8	15	pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF		500		µA
Power Supply Rejection Ratio	PSRR		0.5		% / % ΔVAA
(COMP = 0.1 µF, f = 1 KHz)					

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Clock Rate	Fmax	max	135	110	80	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	tbd	50	50	MHz
4:1 multiplexing		max	33.75	27.5	20	MHz
5:1 multiplexing		max	27	22	16	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	15	ns
CE* Low Time	3	min	50	50	50	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	10	10	10	ns
CE* Asserted to Data Valid	6	max	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	3	3	3	ns
Pixel and Control Setup Time	10	min	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	ns
Clock Cycle Time	12	min	7.4	9.09	12.5	ns
Clock Pulse Width High Time	13	min	3.2	4	5	ns
Clock Pulse Width Low Time	14	min	3.2	4	5	ns
LD* Cycle Time	15					
1:1 multiplexing		min	15.15	20	20	ns
4:1 multiplexing		min	29.63	36.36	50	ns
5:1 multiplexing		min	37.04	45.45	62.5	ns
LD* Pulse Width High Time	16					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns
LD* Pulse Width Low Time	17					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns

See test conditions on next page.

A.C. Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Analog Output Delay	18	typ	12	12	12	ns
Analog Output Rise/Fall Time	19	typ	1.5	1.5	2	ns
Analog Output Settling Time	20	max	8	8	12	ns
Clock and Data Feedthrough*		typ	tbd	tbd	tbd	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	6	6	6	Clocks
		max	10	10	10	Clocks
VAA Supply Current**	IAA	typ	240	220	200	mA
		max	300	300	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are VAA - 0.8 to VAA - 1.8 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 40 pF. See timing notes in Figure 17. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1k-ohm resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v, TA = 20° C. IAA (max) at VAA = 5.25v, TA = 0° C.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt459KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C.
Bt459KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C.
Bt459KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C.

Timing Waveforms

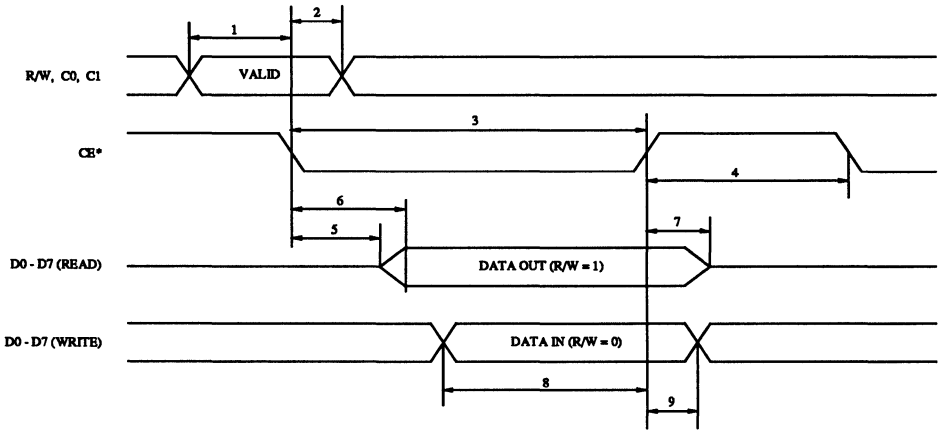
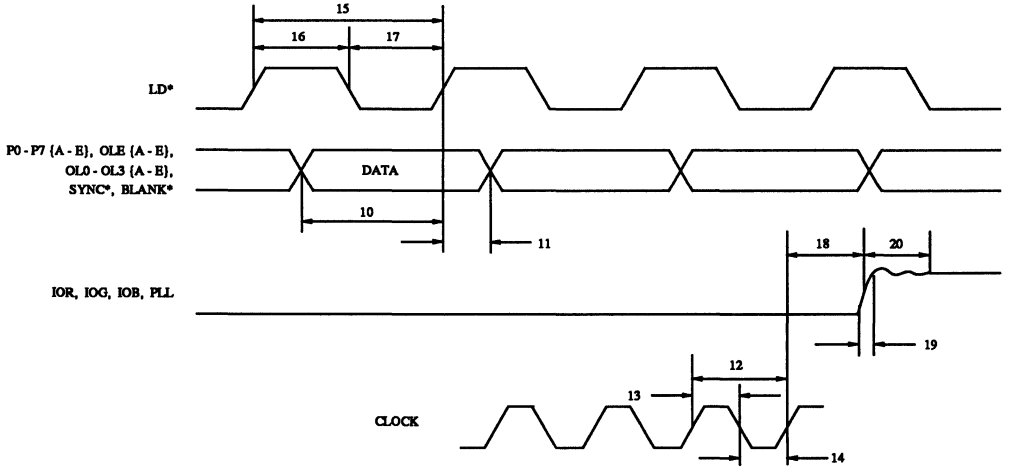


Figure 16. MPU Read/Write Timing.



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ± 1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full scale transition.

Figure 17. Video Input/Output Timing.

Bt460

135 MHz

Monolithic CMOS

512 x 24 Color Palette

RAMDAC™

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Distinguishing Features

- 135, 110, 80 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 512 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- 1, 2, 4, 8, or 9 Bits per Pixel
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X-windows Support for Overlays/Cursor
- Standard MPU Interface
- 132-pin PGA Package

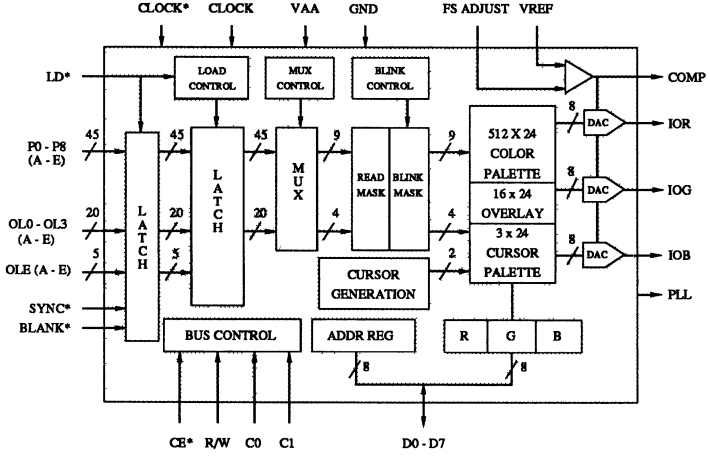
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt459, Bt461, Bt468

Functional Block Diagram



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L460001 Rev. A

Product Description

The Bt460 triple 8-bit RAMDAC is designed specifically for high performance, high resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On chip features include a 512 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, and 1x to 16x integer zoom support.

Pixel data may be input as either 9 bits per pixel or as 8 bits per pixel. For 8 bits per pixel, the cursor clip window uses the ninth bit to select the lower or upper 256 entries in the palette. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X-windows support.

The Bt460 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt460 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Brooktree®

Bt461

170 MHz

Monolithic CMOS

1024 x 8 Color Palette

RAMDAC™

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 170, 135, 110, 80 MHz Operation
- Multiplexed TTL Pixel Ports
- Single 8-bit D/A Converter
- 1024 x 8 Primary Color Palette RAM
- 256 x 8 Alternate Color Palette RAM
- 32 x 8 Overlay Color Palette RAM
- RS-343A Compatible Output
- Pixel Panning Support
- Programmable Setup (0 or 7.5 IRE)
- Bit Plane Read and Blink Masks
- Two Load Color Palette Modes
- Standard MPU Interface
- 132-pin PGA Package
- +5v CMOS Monolithic Construction

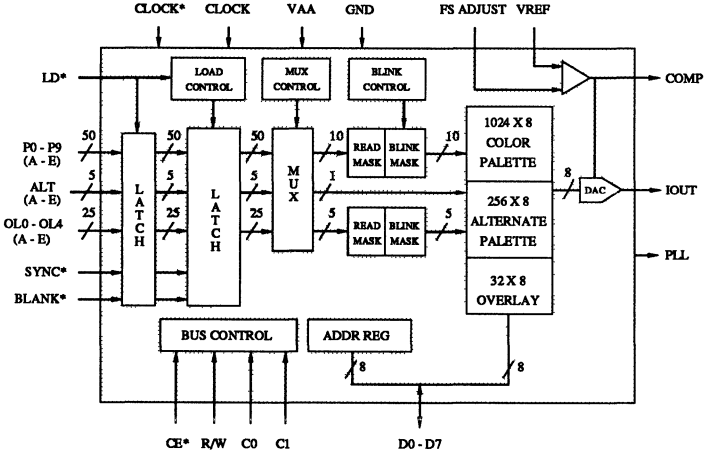
Applications

- High Resolution Color Graphics
- True Color Graphics Systems
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt439
- Bt459, Bt460, Bt468

Functional Block Diagram



Product Description

The Bt461 is a single channel RAMDAC designed specifically for high performance, high resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 45 MHz) to the frame buffer, while maintaining the 170 MHz video data rates required for sophisticated color graphics.

On chip features include a 1024 x 8 dual-port color palette RAM, a 256 x 8 dual-port alternate color palette RAM, 32 x 8 overlay color palette RAM, programmable 3:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

Color data may be written to and read from the Bt461 by the MPU each cycle or using red, green, blue cycles. The MPU interface operates asynchronously to the pixel data, simplifying system design.

The PLL current output enables the synchronization of multiple Bt461s with sub-pixel resolution.

The Bt461 generates a RS-343A compatible video signal, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt461 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 10-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

There are two ways of reading and writing color data to the device, as controlled by command register0. The first mode (normal mode), loads color data into the device each write cycle, and outputs color data from the device each read cycle. The second mode ($\overline{RGB}$ mode) loads color data into the device using red, green, blue write cycles, and output data from the device using red, green, blue read cycles. The device is configured to respond only to the color cycle specified by the command register.

Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or the overlay palette RAM. The address register then increments to the next location which the MPU may modify by simply writing another color. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (eight bits each of red, green, blue) may be read or written to three Bt461s in a single MPU cycle. In this application, the CE* inputs of all three Bt461s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, etc.).

When accessing the primary color palette RAM, the address register resets to $0000 after a read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each read or write cycle.

ADDR0 - 9	C1	C0	Addressed by MPU
$xxxx	0	0	address register low (ADDR0 - 7)
$000X	0	1	address register high (ADDR8 - 9)
$0000 - $00FF	1	0	alternate color palette RAM
$0100	1	0	overlay color 0
:	:	:	:
$011F	1	0	overlay color 31
$0200	1	0	ID register
$0201	1	0	command register 0
$0202	1	0	command register 1
$0203	1	0	command register 2
$0204	1	0	pixel read mask register low
$0205	1	0	pixel read mask register high
$0206	1	0	pixel blink mask register low
$0207	1	0	pixel blink mask register high
$0208	1	0	overlay read mask register
$0209	1	0	overlay blink mask register
$020C	1	0	test register
$0000 - $03FF	1	1	primary color palette RAM

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or overlay RAM. After the blue write cycle, the address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt461 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt461s share a common 8-bit data bus. The CE* inputs of all three Bt461s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the primary color palette RAM, the address register resets to $0000 after a blue read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register have two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 10 bits of the address register (ADDR0 - 9) are accessible to the MPU.

Command register0 is used to specify whether the device loads or outputs data during the red, green, or blue cycle. This mode is useful if only an 8-bit data bus is available, and the software drivers are written for RGB operation.

Note that CE* must be a logical zero during each of the red, green, blue read/write cycles.

Additional Information

Although the color palette RAMs and overlay RAM are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations. ADDR0 and ADDR8 correspond to D0. ADDR10 - ADDR15 are always a logical zero.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt461.

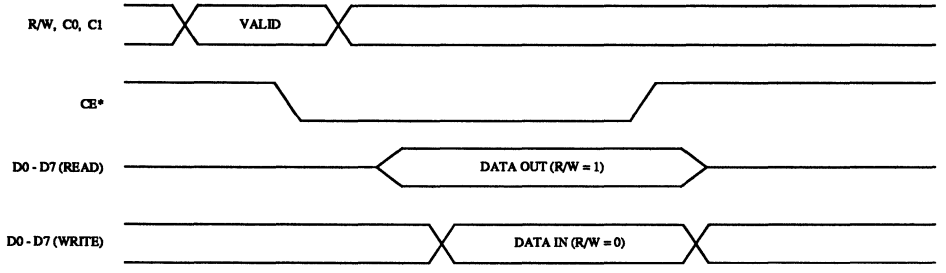

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt461 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either three, four, or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with three, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

Typically, the {A} pixel is output first, followed by the {B} pixel, etc, until all three, four, or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by three, four, or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 3:1 multiplexing is specified, only one rising edge of LD* should occur every three clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

Note that 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.

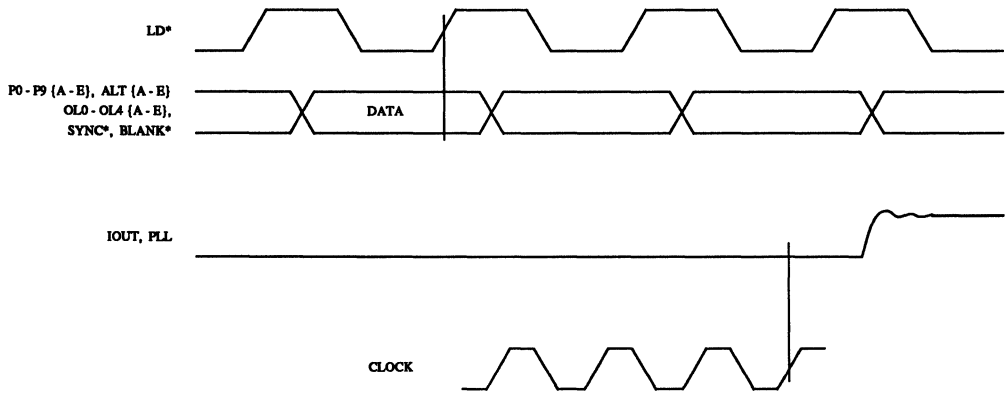

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 10 bits of color information (P0 - P9, ALT) and five bits of overlay information (OL0 - OL4) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e. in the middle of the screen), the Bt461 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

Alternate Color Palette RAM

Note that the pixel read mask and blink mask registers can also be used when the pixel inputs are addressing the alternate color palette RAM.

If the ALT enable bit in command register0 is a logical one, the alternate color palette RAM may be accessed on a pixel basis. A logical one on an ALT {A - E} input forces the P0 - P7 {A - E} inputs to address the alternate color palette RAM. P8 and P9 {A - E} are ignored in this instance. If the ALT enable bit in command register0 is a logical zero, the ALT {A - E} inputs are ignored, as shown below in Table 2.

Pixel bypassing of the primary color palette RAM may be implemented by using the ALT inputs. In this instance, the alternate color palette RAM should be loaded so that each byte contains its corresponding address ($00 - $FF), or with a gamma correction factor. The ALT inputs would then specify, on a pixel basis, whether or not to bypass the primary color palette RAM.

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CR04	ALT	CR05	OL0 - OL4	P0 - P9	Addressed by frame buffer
x	x	x	$1F	$xxx	overlay color 31
:	:	:	:	:	:
x	x	x	$01	$xxx	overlay color 1
x	x	1	$00	$xxx	overlay color 0
0	x	0	$00	$000	primary RAM location $000
0	x	0	$00	$001	primary RAM location $001
:	:	:	:	:	:
0	x	0	$00	$3FF	primary RAM location $3FF
1	1	0	$00	$x00	alternate RAM location $00
:	:	:	:	:	:
1	1	0	$00	$xFF	alternate RAM location $FF

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

Pixel Panning

To support pixel panning, command register1 specifies by how many clock cycles to pan.

If 0 pixel panning is specified, pixel (A) is output first, followed by pixel (B), etc., until all three, four, or five pixels have been output, at which point the cycle repeats.

If 1 pixel panning is specified, pixel (B) will be first, followed by pixel (C), etc. Pixel (A) will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel (A) will be output. Pixels (B), (C), (D), and (E) will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt461 during the first LD* cycle that BLANK* is a logical zero.

The pixel, overlay, and ALT inputs are all panned.

Video Generation

Every clock cycle, the selected 8 bits of color information are presented to the 8-bit D/A converter.

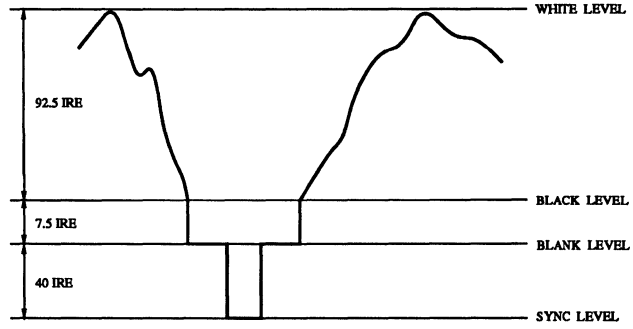
The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converter produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 3 and 4 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converter on the Bt461 uses a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full scale output current against temperature and power supply variations.

Circuit Description (continued)

CR27 = 0		CR27 = 1	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 523 ohms, VREF = 1.235v. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

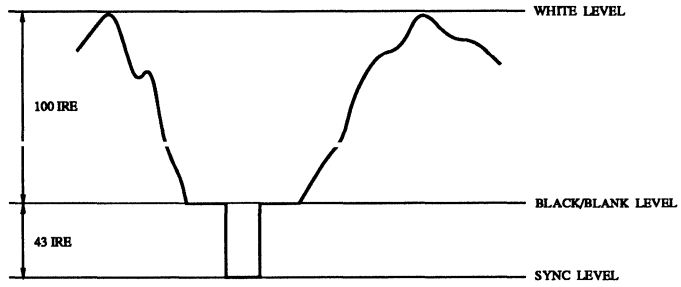
Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOUT = 26.67 mA. RSET = 523 ohms, VREF = 1.235v. Blank pedestal = 7.5 IRE.

Table 3. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

CR27 = 0		CR27 = 1	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 495 ohms, VREF = 1.235v. Blank pedestal = 0 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOUT = 26.67 mA. RSET = 495 ohms, VREF = 1.235v. Blank pedestal = 0 IRE.

Table 4. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) 3:1 multiplexing
(01) 4:1 multiplexing
(10) reserved
(11) 5:1 multiplexing

These bits specify whether 3:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 3:1 is specified, the {D} and {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/3 the CLOCK rate. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate.

Note that it is possible to reset the pipeline delay of the Bt461 to a fixed 8 clock cycles. In this instance, each time the input multiplexing is changed, the Bt461 must again be reset to a fixed pipeline delay.

Note that 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.

CR05 Overlay 0 enable

(0) use color palette RAMs
(1) use overlay color 0

When the overlay bits are $00, this bit specifies whether to use the color palette RAMs or overlay color 0 to provide color information.

CR04 ALT enable

(0) disable alternate palette
(1) enable alternate palette

This bit specifies whether the alternate color palette RAM is enabled (logical one) or disabled (logical zero) from being addressed by the ALT {A - E} and P0 - P7 {A - E} inputs.

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).

CR01 reserved (logical zero)

CR00 reserved (logical zero)

Internal Registers (continued)

Command Register1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17 - CR15 Pan select

(000) 0 pixels {pixel A}
(001) 1 pixel {pixel B}
(010) 2 pixels {pixel C)
(011) reserved
(100) 3 pixels {pixel D}
(101) 4 pixels {pixel E}
(110) reserved
(111) reserved

These bits specify the number of pixels to be panned. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc. These bits are typically modified only during the vertical retrace interval.

Note that the pixel, overlay, and ALT inputs are all panned.

CR14 - CR10 reserved (logical zero)

Internal Registers (continued)

Command Register2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the video waveform (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video waveform. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt461 each write cycle, and color data is output each read cycle. If (01), (10), or (11) is specified, the Bt461 expects color data be to input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses the SYNC* or BLANK* input for generating PLL information.
CR22	reserved (logical zero)	
CR21	reserved (logical zero)	
CR20	Test enable (0) disable test register (1) enable test register	A logical one enables the P9 {A - E} inputs to serve as a trigger for the test register. A logical zero enables normal operation.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt461, the value read by the MPU will be $4D. Data written to this register is ignored.

Pixel Read Mask Register

The 16-bit pixel read mask register is configured as two 8-bit registers (pixel read mask low and pixel read mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM.

pixel read mask register high								pixel read mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Pixel Blink Mask Register

The 16-bit pixel blink mask register is configured as two 8-bit registers (pixel blink mask low and pixel blink mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register0.

pixel blink mask register high								pixel blink mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

In order for a bit plane to blink, the corresponding bit in the pixel read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A - E}) and D4 corresponds to overlay plane 4 (OL4 {A - E}). Each register bit is logically ANDed with the corresponding overlay plane input. Bits D5 - D7 are always a logical zero. This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) a overlay plane from blinking at the blink rate and duty cycle specified by command register0. D0 corresponds to overlay plane 0 (OL0 {A - E}) and D4 corresponds to overlay plane 4 (OL4 {A - E}). In order for a overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. Bits D5 - D7 are always a logical zero. This register may be written to or read by the MPU at any time and is not initialized.

Test Register

The test register enables the MPU to verify that the pixel and overlay ports are addressing the color palette RAM and overlay registers correctly at full speed.

P9 {A - E} is the fast port trigger when CR20 is a logical one. P0 - P8 {A - E}, ALT {A - E}, and OL0 - OL4 {A - E} address the primary color palette RAM, alternate palette RAM, and overlay registers. A logical one on P9A latches the {A} color data into the test register as it is passes from the color palette to the D/A converter. A logical one on P9B latches the {B} color data into the test register as it is passes from the color palette to the D/A converter, etc.

To test the entire color palette, bit D1 in the pixel read mask register high (P9) must be a logical zero to test the lower 512 entries. Next, bit D1 in the pixel read mask register high (P9) must be a logical one to test the higher 512 entries. There should be only a single "one" on the P9 inputs per test read cycle.

A recommended test read cycle is four LD* cycles long. The test register may be written whenever the test mode is disabled or while in the test mode when no "ones" are present on the P9 inputs. The test registers are not initialized.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 3 and 4. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input typically switches off a 40 IRE current source on the IOUT output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 3 and 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0 - P9 {A - E}, OL0 - OL4 {A - E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/3, 1/4, or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the A.C. Characteristics section.
P0 - P9 {A-E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the primary or alternate color palette RAMs is to be used to provide color information (see Table 2). Either three, four, or five consecutive pixels (up to ten bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all three, four, or five pixels have been output, at which point the cycle repeats.
OL0 - OL4 {A-E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*, and in conjunction with CR05 in command register0, specify which palette is to be used for color information, as illustrated in Table 2. When accessing the overlay palette RAM, the P0 - P9 {A - E} and ALT {A - E} inputs are ignored. Overlay information bits (up to five bits per pixel) for either three, four, or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
ALT {A-E}	Palette select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and specify which color palette RAM is to be used for color information, as illustrated in Table 2. When accessing the alternate color palette RAM, the P8 - P9 {A - E} inputs are ignored. Unused inputs should be connected to GND.
IOUT	Analog current output. This high impedance current source is capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 5).
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt461s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one on the SYNC* or BLANK* input (as specified by CR23 in command register2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (v) / RSET (ohms) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 ohms).

Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 5). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 5). Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOUT for a 7.5 IRE blanking pedestal is: RSET (ohms) = 11,294 * VREF (v) / IOUT (mA) The relationship between RSET and the full scale output current on IOUT for a 0 IRE blanking pedestal is: RSET (ohms) = 10,684 * VREF (v) / IOUT (mA)
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 5, must supply this input with a 1.235v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 5. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 volt) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

Signal	Pin Number
BLANK*	L1
SYNC*	K3
LD*	A5
CLOCK	K1
CLOCK*	K2
P0A	E3
P0B	D2
P0C	D1
P0D	E2
P0E	F3
P1A	A1
P1B	D3
P1C	C2
P1D	B1
P1E	C1
P2A	A3
P2B	B3
P2C	A2
P2D	C3
P2E	B2
P3A	A8
P3B	A7
P3C	B7
P3D	A6
P3E	B6
P4A	C9
P4B	B9
P4C	A9
P4D	C8
P4E	B8
P5A	B11
P5B	A11
P5C	C10
P5D	B10
P5E	A10
P6A	A14
P6B	A13
P6C	B12
P6D	C11
P6E	A12
P7A	E13
P7B	E12
P7C	D14
P7D	D13
P7E	D12

Signal	Pin Number
P8A	G14
P8B	G13
P8C	F14
P8D	F13
P8E	E14
P9A	J13
P9B	J14
P9C	H12
P9D	H13
P9E	H14
ALTA	L14
ALTB	K12
ALTC	K13
ALTD	K14
ALTE	J12
OL0A	E1
OL0B	F2
OL0C	F1
OL0D	G3
OL0E	G2
OL1A	M1
OL1B	L2
OL1C	N1
OL1D	L3
OL1E	M2
OL2A	M3
OL2B	N2
OL2C	P1
OL2D	P2
OL2E	N3
OL3A	M4
OL3B	P3
OL3C	N4
OL3D	P4
OL3E	M5
OL4A	N5
OL4B	P5
OL4C	M6
OL4D	N6
OL4E	P6
IOUT	P10
reserved	P11
PLL	N10

Signal	Pin Number
VAA	J1
VAA	J2
VAA	J3
VAA	C6
VAA	F12
VAA	M9
GND	H1
GND	H2
GND	H3
GND	C7
GND	G12
GND	M8
COMP	N9
FS ADJUST	M10
VREF	P9
CE*	P13
R/W	N12
C1	P12
C0	M11
D0	L13
D1	M14
D2	L12
D3	M13
D4	N14
D5	P14
D6	N13
D7	M12
reserved	G1
reserved	N11
reserved	M7
reserved	N7
reserved	P7
reserved	P8
reserved	N8
reserved	B5
reserved	C5
reserved	A4
reserved	B4
reserved	C4
reserved	C14
reserved	C13
reserved	B14
reserved	C12
reserved	B13

Pin Descriptions (continued)

Bt461

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	P9E	P9B	ALTD	ALTA	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	P9D	P9A	ALTC	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	P9C	ALTE	ALTB	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	N/C	N/C
10	P5E	P5D	P5C									FS ADJ	PLL	IOUT
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	N/C	N/C
7	P3B	P3C	GND									N/C	N/C	N/C
6	P3D	P3E	VAA									OL4C	OL4D	OL4E
5	LD*	N/C	N/C									OL3E	OL4A	OL4B
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	ALTA	ALTD	P9B	P9E	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	ALTC	P9A	P9D	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	ALTB	ALTE	P9C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	N/C	N/C	C0									P6D	P5A	P5B
10	IOUT	PLL	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	N/C	N/C	GND									P4D	P4E	P3A
7	N/C	N/C	N/C									GND	P3C	P3B
6	OL4E	OL4D	OL4C									VAA	P3E	P3D
5	OL4B	OL4A	OL3E									N/C	N/C	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

PC Board Layout Considerations

PC Board Considerations

It is recommended that a four layer PC board be used with the Bt461. The layout should be optimized for lowest noise on the Bt461 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt461 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt461, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt461.

Power Planes

The Bt461 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 5. This bead should be located within three inches of the Bt461.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt461 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, three 0.1 µF ceramic capacitors in parallel with three 0.01 µF chip capacitors should be used to decouple the VAA pins to GND. These capacitors should be placed as close as possible to the device. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the Bt461 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt461 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground plane.

Due to the high clock rates involved, long clock lines to the Bt461 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

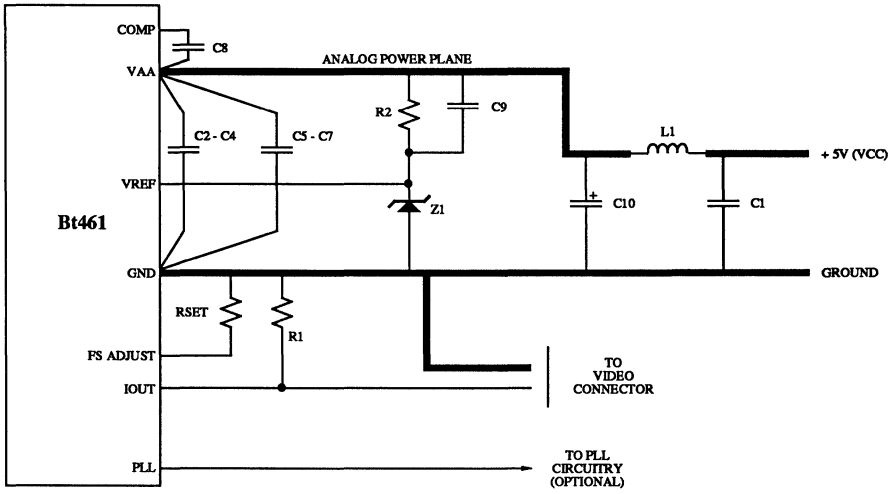
Analog Signal Interconnect

The Bt461 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch. Also, the external voltage reference circuitry should be as close as possible to the Bt461 to avoid noise pickup.

The video output signal should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog output should have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt461 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C5 - C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75-ohm 1% metal film resistor	Dale CMF-55C
R2	1000-ohm 1% metal film resistor	Dale CMF-55C
RSET	523-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385Z-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt461.

Figure 5. Typical Connection Diagram and Parts List.

Application Information

Non-Video Applications

The Bt461 may be used in non-video applications by disabling the video-specific control signals. Set bits CR26 and CR27 in command register2 to a zero (disabling the BLANK* and SYNC* inputs). SYNC* should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,457 * VREF (v) / Iout (mA)

Using Multiple Bt461s

If located close together on the same PC board, multiple Bt461s may be connected to a single analog power plane. In addition, a single voltage reference may drive multiple devices.

Each Bt461 must still have it's individual RSET resistor, IOUT termination resistor (R1 in Figure 5), power supply bypass capacitors (C2 - C7 in Figure 5) and COMP capacitor (C8 in Figure 5).

Clock Interfacing

Due to the high clock rates at which the Bt461 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 volts. Note that the CLOCK and CLOCK* inputs require termination resistors (220-ohm resistor to VCC and a 330-ohm resistor to GND). The termination resistors should be as close as possible to the Bt461.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt461 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by three, four, or five (depending on whether 3:1, 4:1, or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt461, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt461 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt461.

To reset the Bt461, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt461 to an eight clock cycle pipeline delay also resets the blink counter circuitry. If the Bt461 is periodically reset (i.e., every vertical sync interval), the on-chip blink counter will not function correctly. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

In standard operation, the Bt461 need be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Monochrome Display Applications

For monochrome display applications where a single Bt461 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461, and will also optionally set the pipeline delay of the Bt461 to seven clock cycles. The Bt438 may also be used to interface the Bt461 to a TTL clock. Figure 6 illustrates using the Bt438 with the Bt461.

In applications using a single Bt461, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 ohms).

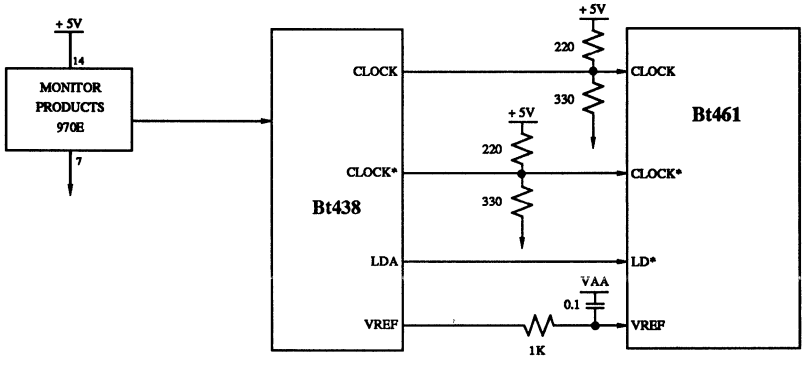


Figure 6. Generating the Bt461 Clock Signals (Monochrome Application).

Application Information (continued)

Color Display Applications

For color display applications where up to four Bt461s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461, synchronizes them to sub-pixel resolution, and will also optionally set the pipeline delay of the Bt461 to eight clock cycles. The Bt439 may also be used to interface the Bt461 to a TTL clock. Figure 7 illustrates using the Bt439 with the Bt461.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt461, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt461s, and adjusts the phase of the CLOCK and CLOCK* signals to each Bt461 to minimize the PLL phase difference.

If sub-pixel synchronization of multiple Bt461s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt461s are connected together, and driven by a single Bt438 (with distributed branch termination on each clock). The VREF inputs of the Bt461s must still be isolated by 1K-ohm resistors, as shown in Figure 7, and have a 0.1 µF bypass capacitor to VAA. The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 ohms).

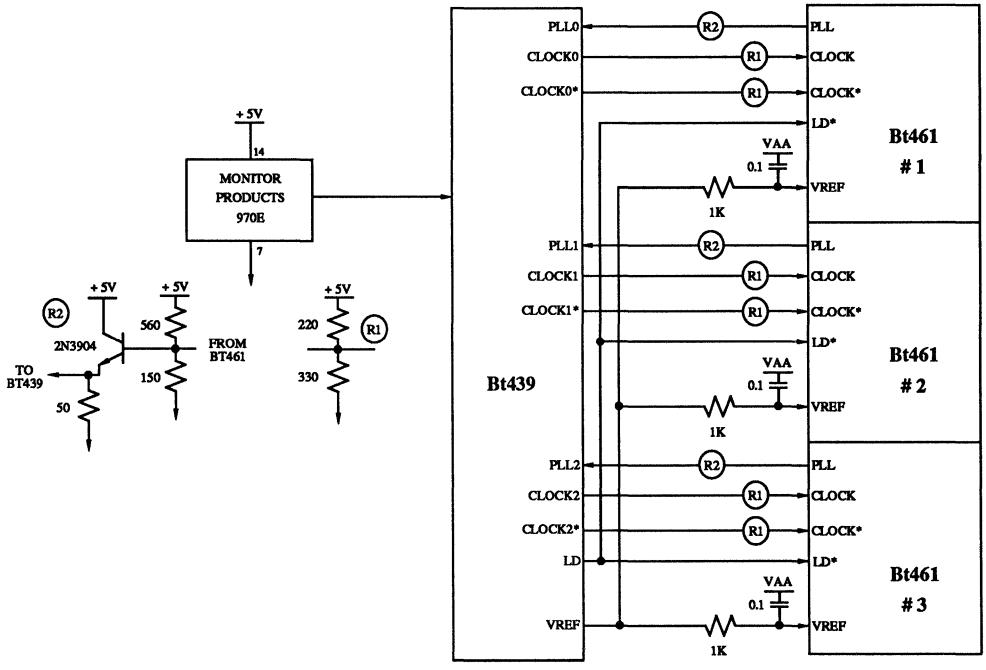


Figure 7. Generating the Bt461 Clock Signals (Color Application).

Application Information (continued)

Initializing the Bt461 (Monochrome)

Following a power-on sequence, the Bt461 must be initialized. This sequence will configure the Bt461 as follows:

4:1 multiplexed operation
no overlays
no pixel masking, no blinking, no panning
color data written/read every cycle
sync enabled on IOUT, 7.5 IRE blanking pedestal

Control Register Initialization	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $02 to address register low	00
Write $00 to command register 1	10
Write $03 to address register low	00
Write $C0 to command register 2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Color Palette RAM Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write data to RAM (location $000)	11
Write data to RAM (location $001)	11
:	:
Write data to RAM (location $3FF)	11

Overlay Color Palette Initialization	
Write $00 to address register low	00
Write $01 to address register high	01
Write data to overlay (location $00)	10
Write data to overlay (location $01)	10
:	:
Write data to overlay (location $1F)	10

Alternate Color Palette Initialization	
Write $00 to address register low	00
Write $00 to address register high	01
Write data to alternate (location $00)	10
Write data to alternate (location $01)	10
:	:
Write data to alternate (location $FF)	10

Initializing the Bt461 (Color) 24-bit MPU Data Bus

In this example, three Bt461s are being used in parallel to generate true color. A 24-bit MPU data bus is available for accessing all three Bt461s in parallel.

The operation and initialization is the same as for the Bt461 being used in a monochrome application.

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Application Information (continued)

Initializing the Bt461 (Color) 8-bit MPU Data Bus

In this example, three Bt461s are being used in parallel to generate true color. An 8-bit MPU data bus is available for accessing the Bt461s.

Note that while accessing the command, read mask, blink mask, and control/test, and address register, each Bt461 must be accessed individually. While accessing the color palette RAM, alternate RAM, or overlay registers, all three Bt461s may be accessed simultaneously.

Following a power-on sequence, the Bt461s must be initialized. This sequence will configure the Bt461s as follows:

4:1 multiplexed operation
no overlays
no blinking, no panning
initialize each Bt461 as a red, green, or blue device
sync on all outputs, 7.5 IRE blanking pedestal

Control Register Initialization

Red Bt461	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $02 to address register low	00
Write $00 to command register 1	10
Write $03 to address register low	00
Write $D0 to command register 2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Green Bt461

Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $02 to address register low	00
Write $00 to command register 1	10
Write $03 to address register low	00
Write $E0 to command register 2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Blue Bt461

Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $02 to address register low	00
Write $00 to command register 1	10
Write $03 to address register low	00
Write $F0 to command register 2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Application Information (continued)

Color Palette RAM Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $3FF)	11
Write green data to RAM (location $3FF)	11
Write blue data to RAM (location $3FF)	11

Alternate Color Palette Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to alternate (location $00)	10
Write green data to alternate (location $00)	10
Write blue data to alternate (location $00)	10
Write red data to alternate (location $01)	10
Write green data to alternate (location $01)	10
Write blue data to alternate (location $01)	10
:	:
Write red data to alternate (location $FF)	10
Write green data to alternate (location $FF)	10
Write blue data to alternate (location $FF)	10

Overlay Color Palette Initialization

Write $00 to all three address low registers	00
Write $01 to all three address high registers	00
Write red data to overlay (location $00)	10
Write green data to overlay (location $00)	10
Write blue data to overlay (location $00)	10
Write red data to overlay (location $01)	10
Write green data to overlay (location $01)	10
Write blue data to overlay (location $01)	10
:	:
Write red data to overlay (location $1F)	10
Write green data to overlay (location $1F)	10
Write blue data to overlay (location $1F)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output					
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA - 1.0		VAA + 0.5	Volts
Input Low Voltage	VKIL	GND - 0.5		VAA - 1.6	Volts
Input High Current (Vin = 4.0v)	IKIH			1	µA
Input Low Current (Vin = 0.4v)	IKIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0v)	CKIN		4	10	pF
Digital Outputs (D0 - D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output	IOUT				
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	- 1.0		+ 1.2	Volts
Output Impedance	RAOUT		50		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		- 1.0		+ 2.5	Volts
Output Impedance			50		K ohms
Output Capacitance (f = 1 MHz, PLL = 0 mA)			15		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		170 MHz Devices			135 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			170			135	MHz
LD* Rate	LDmax			42.5			45	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	10			10			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5.88			7.4			ns
Clock Pulse Width High Time	13	2			3.2			ns
Clock Pulse Width Low Time	14	2			3.2			ns
LD* Cycle Time	15	23.5			22.2			ns
LD* Pulse Width High Time	16	8			8			ns
LD* Pulse Width Low Time	17	8			8			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			6			8	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current**	IAA		400	tbd		360	400	mA

See test conditions on next page.

A.C. Characteristics (continued)

		110 MHz Devices			80 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			36.7			26.7	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	10			10			ns
CE* Asserted to Data Valid	6			75			100	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			50			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			4			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	9.09			12.5			ns
Clock Pulse Width High Time	13	4			5			ns
Clock Pulse Width Low Time	14	4			5			ns
LD* Cycle Time	15	27.27			37.5			ns
LD* Pulse Width High Time	16	10			12			ns
LD* Pulse Width Low Time	17	10			12			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			3		ns
Analog Output Settling Time	20			8			12	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current**	IAA		340	380		310	340	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 ohms, VREF = 1.235v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are VAA - 0.8 to VAA - 1.8 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 40 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1k-ohm resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v, TA = 20° C. IAA (max) at VAA = 5.25v, TA = 0° C.

Timing Waveforms

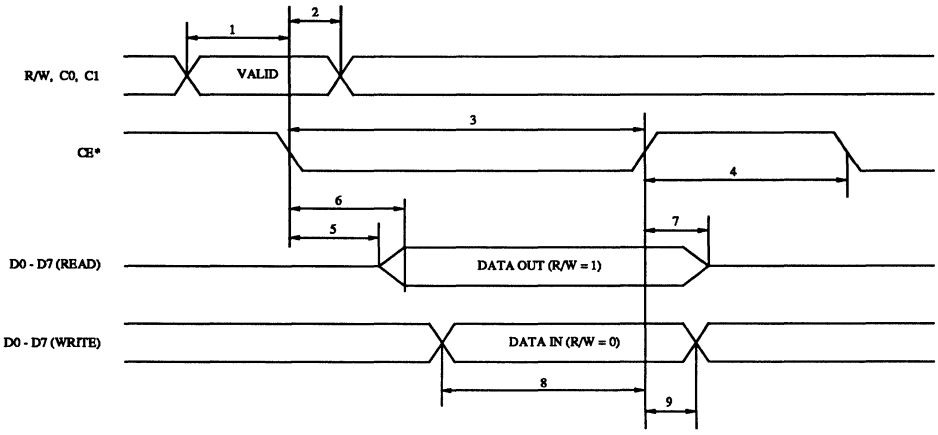
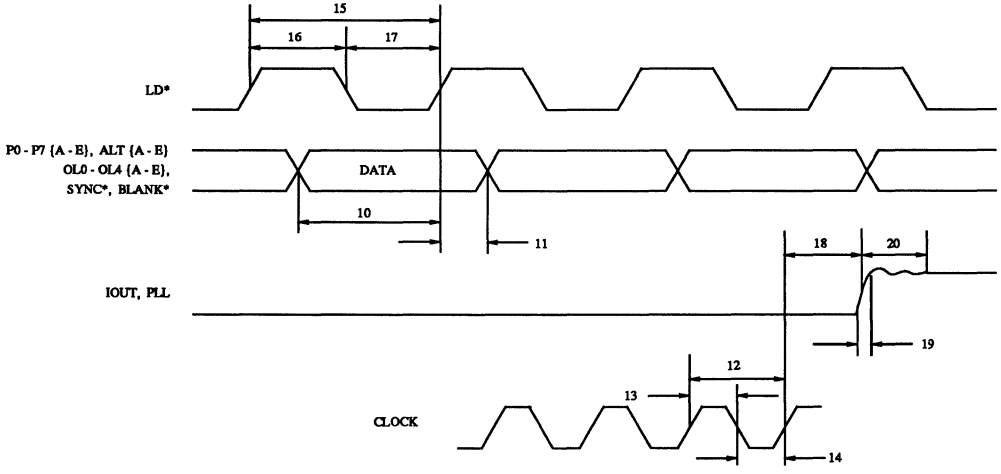


Figure 8. MPU Read/Write Timing.



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ± 1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt461KG170	170 MHz	132-pin Ceramic PGA	0° to +70° C.
Bt461KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C.
Bt461KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C.
Bt461KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C.

Device Circuit Data

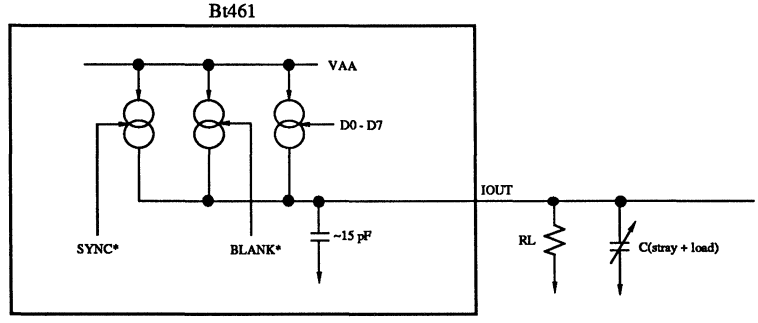


Figure 10. Equivalent Circuit of the Current Output.

Bt468

200 MHz

Monolithic CMOS

256 x 24 Color Palette

RAMDAC™

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Distinguishing Features

- 200, 170 MHz Operation
- 8:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- Pixel Panning Support
- On-Chip User-Definable Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X-windows Support for Overlays/Cursor
- Standard MPU Interface
- 144-pin PGA Package
- +5v CMOS Monolithic Construction

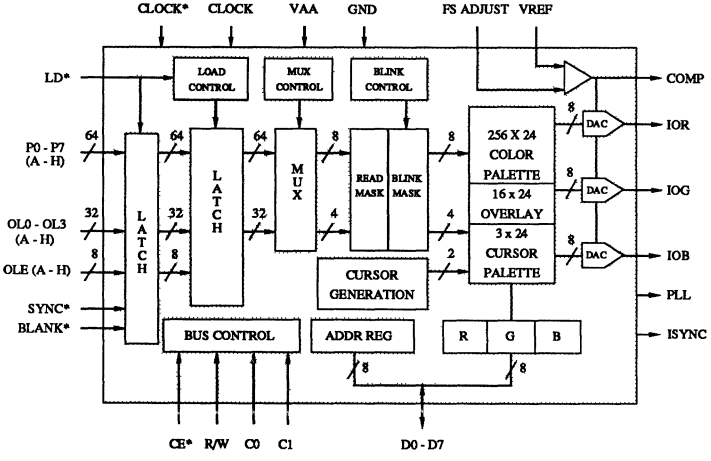
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439

Functional Block Diagram



Product Description

The Bt468 triple 8-bit RAMDAC is designed specifically for high performance, high resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing to the frame buffer, while maintaining the 200 MHz video data rates required for sophisticated color graphics.

On chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X-windows support.

The Bt468 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution. The ISYNC current output enables separate sync generation for those monitors requiring separate sync.

The Bt468 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 50-ohm or 75-ohm coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

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L468001 Rev. A

Brooktree®

Bt471 Bt476 Bt478

80 MHz

256 Color Palette

Personal System/2®

RAMDAC™

Distinguishing Features

- Personal System/2® Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 6-bit or 8-bit D/A Converters
- 256 Word Color Palette RAM
- RS-343A/RS-170 Compatible Outputs
- 15 Overlay Registers (Bt471/478)
- Sync on all Three Channels (Bt471/478)
- Programmable Pedestal (Bt471/478)
- External Voltage or Current Reference
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 44-pin PLCC or 28-pin DIP Package

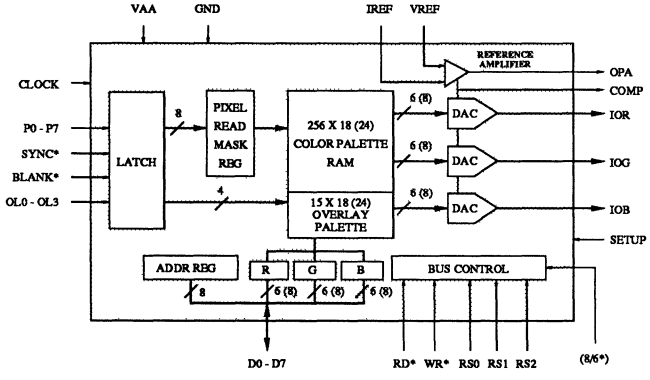
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt473, Bt479

Functional Block Diagram



Product Description

The Bt471/476/478 are pin-compatible and software-compatible RAMDACs designed specifically for Personal System/2® compatible color graphics. The Bt476 is also available in a 28-pin DIP package that is pin compatible with the IMSG176.

The Bt471 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The Bt478 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6-bit or 8-bit D/A converter operation. The Bt476 is similar to the Bt471, but has no overlays or sync information on the analog outputs.

Additional features on the Bt471 and Bt478 include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference.

The Bt471/476/478 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering.

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Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt471/476/478 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 - RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the overlay location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	reserved

Table 1. Control Input Truth Table.

Circuit Description (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4 - 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e. block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0 - 7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	i 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

Bt471/476 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Bt478 Data Bus Interface

On the Bt478, the 8/6* control input is used to specify whether the MPU is reading and writing 8-bits (8/6* = logical one) or 6-bits (8/6* = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the Bt471/476), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Note that in the 6-bit mode, the Bt478's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Frame Buffer Interface

The P0 - P7 and OL0 - OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 - P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the Bt471/476) of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE ($\overline{\text{SETUP}}$ = $\overline{\text{GND}}$) or 7.5 IRE ($\overline{\text{SETUP}}$ = $\overline{\text{VAA}}$) blanking pedestal is to be used. Note that the Bt476 generates only a 0 IRE blanking pedestal (Figure 2).

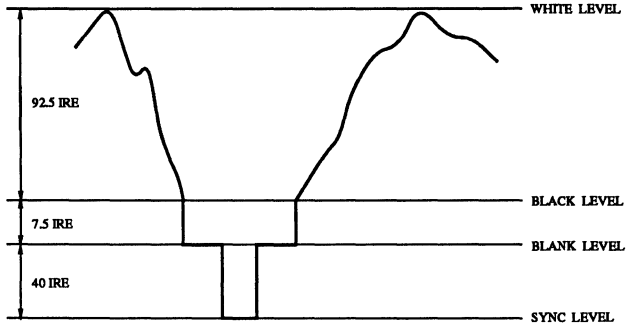
The analog outputs of the Bt471/476/478 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

OL0 - OL3	P0 - P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

Circuit Description (continued)

BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = VAA. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 1. Composite Video Output Waveforms (SETUP = VAA).

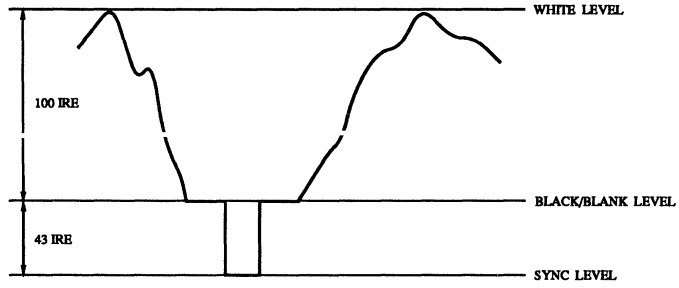
Description	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = VAA. VREF = 1.235v, RSET = 147 ohms.

Table 4. Video Output Truth Table (SETUP = VAA).

Circuit Description (continued)

BT476 OR BT471/478 W/O SYNC		BT471/478 WITH SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = GND. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND).

Description	Bt476 Iout (mA)	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = GND. VREF = 1.235v, RSET = 147 ohms.

Table 5. Video Output Truth Table (SETUP = GND).

Pin Descriptions

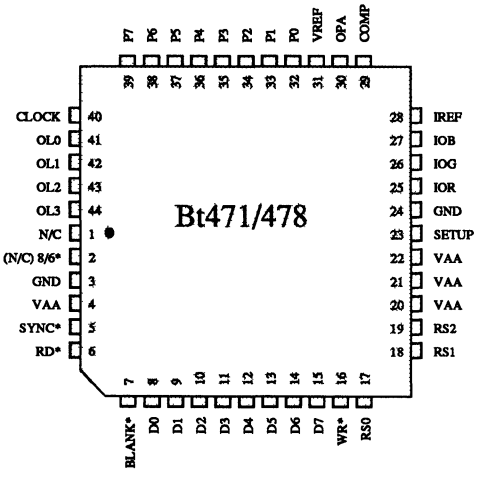
Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P7, OL0 - OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IREF	Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current. When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: RSET (ohms) = K * 1,000 * VREF (v) / Iout (mA) K is defined in the table below for doubly-terminated 75-ohm loads. It is recommended that a 147-ohm RSET resistor be used. When using an external current reference (Figures 4 and 5), the relationship between IREF and the full scale output current on each output is: IREF (mA) = Iout (mA) / K

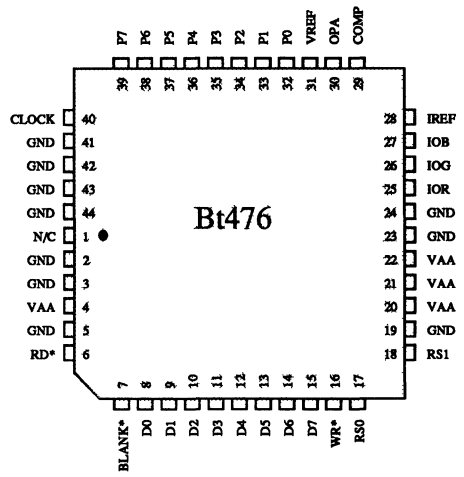
Part	Mode	Pedestal	K
Bt478	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
	6-bit	0 IRE	3.000
	8-bit	0 IRE	3.025
Bt471	(6-bit)	7.5 IRE	3.170
		0 IRE	3.000
Bt476	(6-bit)	0 IRE	2.100

Pin Descriptions (continued)

Pin Name	Description
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figures 3 and 4).
COMP	Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2v (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to VAA, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
WR*	Write control input (TTL compatible). D0 - D7 data is latched on the rising edge of WR*, and RS0 - RS2 are latched on the falling edge of WR* during MPU write operations.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0 - RS2 are latched on the falling edge of RD* during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 - RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
8/6*	8-bit/6-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles). Note: this pin should be connected to GND when using the Bt476.

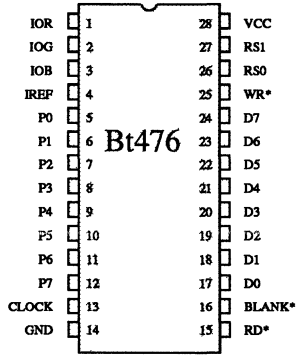
Pin Descriptions (continued) -- 44-Pin Plastic J-Lead (PLCC)





Names in parentheses are pin names for the Bt471.
N/C pins may be left unconnected without affecting the performance of the Bt471/476/478.

Pin Descriptions -- 28-Pin DIP



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt471/476/478 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt471/476/478 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the Bt471/476/478, the analog output traces, and all the digital signal traces leading up to the Bt471/476/478.

Power Planes

The Bt471/476/478 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 3, 4, and 5. This bead should be located within three inches of the Bt471/476/478.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt471/476/478 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt471/476/478 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high-frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt471/476/478 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt471/476/478 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

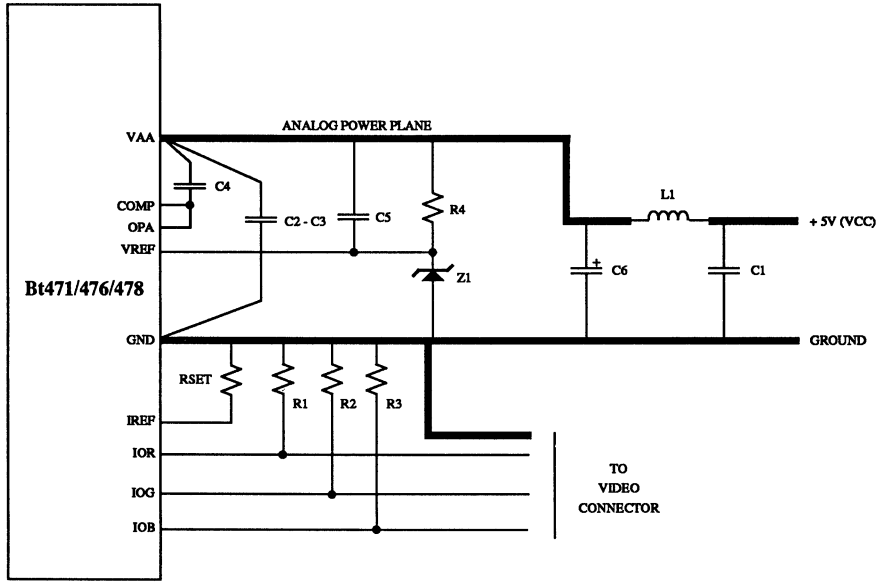
Analog Signal Interconnect

The Bt471/476/478 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt471/476/478 to minimize reflections.

PC Board Layout Considerations (continued) -- 44-Pin Plastic J-Lead (PLCC)

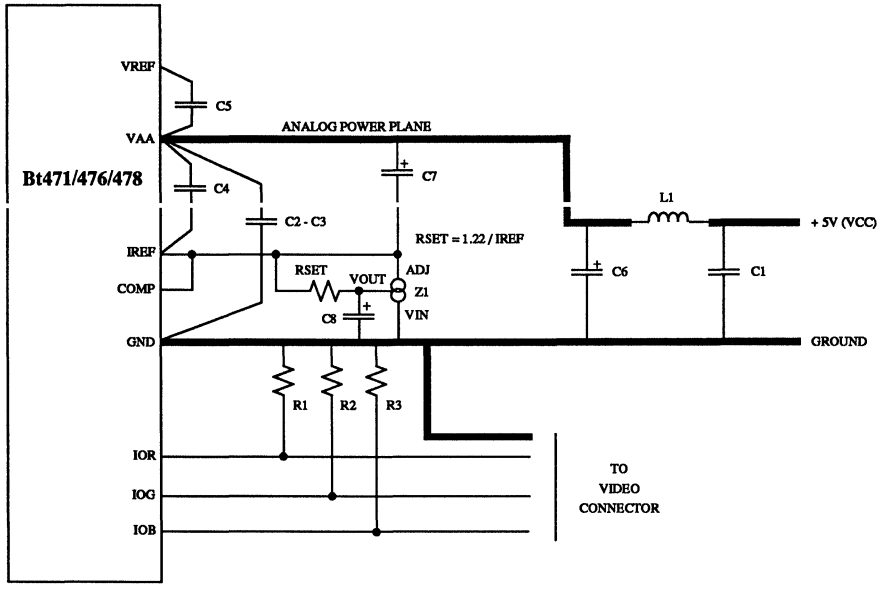


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1k-ohm 5% resistor	
RSET	147-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 3. Typical Connection Diagram and Parts List. (External Voltage Reference)

PC Board Layout Considerations (continued) -- 44-Pin Plastic J-Lead (PLCC)

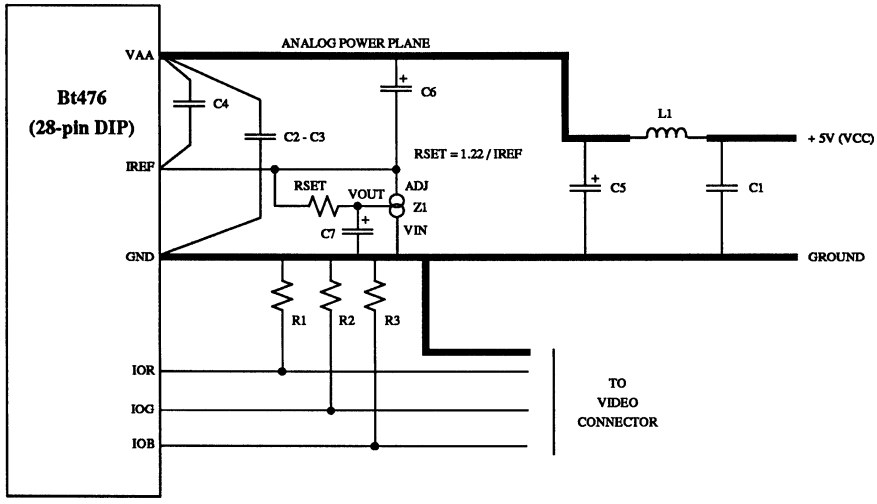


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7	47 µF capacitor	Mallory CSR13F476KM
C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 4. Typical Connection Diagram and Parts List. (External Current Reference)

PC Board Layout Considerations (continued) -- 28-Pin DIP



Location	Description	Vendor Part Number
C1 - C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF capacitor	Mallory CSR13G106KM
C6	47 µF capacitor	Mallory CSR13F476KM
C7	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt476.

Figure 5. Typical Connection Diagram and Parts List. (External Current Reference)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		- 2	- 8.39	- 10	mA
PS/2 Compatible		- 3	- 8.88	- 10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt478		8	8	8	Bits
Bt471/476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt478				± 1	LSB
Bt476				± 1/2	LSB
Bt471				± 1/4	LSB
Differential Linearity Error	DL				
Bt478				± 1	LSB
Bt476				± 1/2	LSB
Bt471				± 1/4	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = VAA		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
Bt476		0	0	0	µA
Blank Level					
Bt471/478		6.29	7.62	8.96	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA
LSB Size					
Bt478 (8/6* = logical one)			69.1		µA
Bt471/476			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.5	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	%/% ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v, SETUP = VAA, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = -8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Since the Bt471 and Bt476 have 6-bit DACs (and the Bt478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

Analog Output Levels -- PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = VAA		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
Bt476		0	5	50	µA
Blank Level					
Bt471/478		6.6	8	9.4	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 ohms, VREF = 1.235v, SETUP = VAA, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = -8.88 mA.

A.C. Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on next page.

A.C. Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			-30			-30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			-23			-23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
Average VAA Supply Current**	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v, SETUP = VAA, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = -8.39 mA. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA (max).

Timing Waveforms

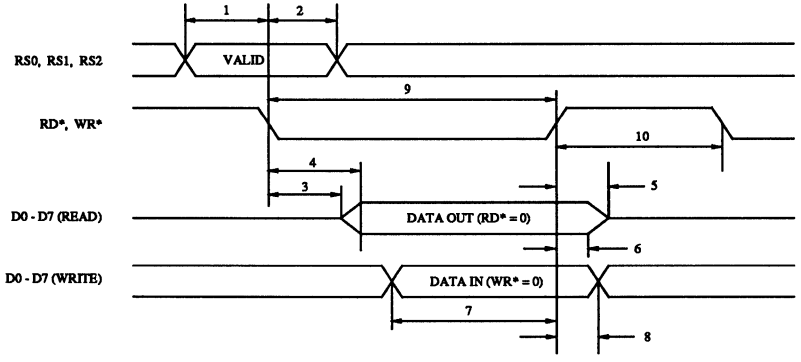
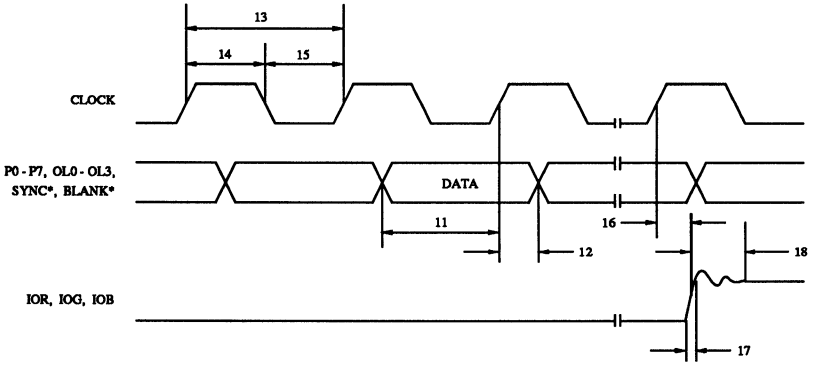


Figure 6. MPU Read/Write Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB (Bt478), ± 1/4 LSB (Bt471), or ± 1/2 LSB (Bt476).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Sync Generation	Speed	Package	Ambient Temperature Range
Bt471KPJ80	256 x 18	15 x 18	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt471KPJ66	256 x 18	15 x 18	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt471KPJ50	256 x 18	15 x 18	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt471KPJ35	256 x 18	15 x 18	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt476KPJ66	256 x 18	-	no	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt476KPJ50	256 x 18	-	no	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt476KPJ35	256 x 18	-	no	35 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt476KP66	256 x 18	-	no	66 MHz	28-pin 0.6" Plastic DIP	0° to +70° C.
Bt476KP50	256 x 18	-	no	50 MHz	28-pin 0.6" Plastic DIP	0° to +70° C.
Bt476KP35	256 x 18	-	no	35 MHz	28-pin 0.6" Plastic DIP	0° to +70° C.
Bt478KPJ80	256 x 24	15 x 24	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt478KPJ66	256 x 24	15 x 24	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt478KPJ50	256 x 24	15 x 24	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt478KPJ35	256 x 24	15 x 24	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt473

80 MHz

Monolithic CMOS

Triple 8-Bit

True-Color RAMDAC™

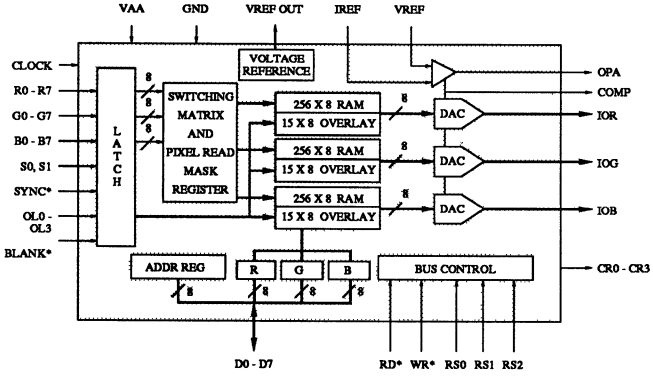
Distinguishing Features

- Bt471/478 Software Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 15 x 8 Overlay Registers
- RS-343A/RS-170 Compatible Outputs
- Sync on all Three Channels
- Programmable Pedestal (0 or 7.5 IRE)
- On-Chip Voltage Reference
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 68-pin PLCC Package
- Typical Power Dissipation: 900 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt473 true-color RAMDAC is designed specifically for true-color computer graphics. It has three 256 x 8 color lookup tables with triple 8-bit video D/A converters to support 24-bit true-color operation. In addition, 8-bit pseudo-color 8-bit true color, and 15-bit true color operations are supported.

Features include a programmable pedestal (0 or 7.5 IRE) and optional on-chip voltage reference. 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is a pixel read mask register and sync generation on all three channels.

Either an external current reference, an external voltage reference, or the internal voltage reference may be used.

The Bt473 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 - RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAMs
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

Circuit Description (continued)

red, green, and blue), using RS0 - RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4 - 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e. block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

8-Bit / 6-Bit Operation

The command register specifies whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt473's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Color Modes

Four color modes are supported by the Bt473: 24-bit true-color, 15-bit true-color, 8-bit true-color, and 8-bit pseudo-color. The mode of operation is determined by the S0 and S1 inputs, in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the R0 - R7, G0 - G7, B0 - B7, and OL0 - OL3 pixel and overlay data inputs.

Table 3 lists the modes of operation.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	0	1	red value
	01	x	0	1	green value
	10	x	0	1	blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0	0	1	color palette RAMs
	xxxx 0000	1	0	1	reserved
	xxxx 0001	1	0	1	overlay color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

OL3 - OL0	S1, S0	CR7, CR6	Mode	R7 - R0	G7 - G0	B7 - B0
1111 : 0001	xx : xx	xx : xx	overlay color 15 : overlay color 1	$xx : $xx	$xx : $xx	$xx : $xx
0000	00	00	24-bit true-color	R7 - R0	G7 - G0	B7 - B0
0000	00	01	24-bit true-color	R7- R0	G7 - G0	B7 - B0
0000	00	10	24-bit true-color	R7- R0	G7 - G0	B7 - B0
0000	00	11	reserved	reserved	reserved	reserved
0000	01	00	24-bit true-color bypass	R7 - R0	G7 - G0	B7 - B0
0000	01	01	24-bit true-color bypass	R7 - R0	G7 - G0	B7 - B0
0000	01	10	24-bit true-color bypass	R7 - R0	G7 - G0	B7 - B0
0000	01	11	reserved	reserved	reserved	reserved
0000	10	00	8-bit pseudo-color (red)	P7 - P0	ignored	ignored
0000	10	01	8-bit pseudo-color (green)	ignored	P7 - P0	ignored
0000	10	10	8-bit pseudo-color (blue)	ignored	ignored	P7 - P0
0000	10	11	reserved	reserved	reserved	reserved
0000	11	00	8-bit true-color bypass (red)	rrrgggbb	ignored	ignored
0000	11	01	8-bit true-color bypass (green)	ignored	rrrgggbb	ignored
0000	11	10	8-bit true-color bypass (blue)	ignored	ignored	rrrgggbb
0000	11	11	15-bit true color	0rrrrrgg	gggbbbbb	ignored

Table 3. Color Operation Modes.

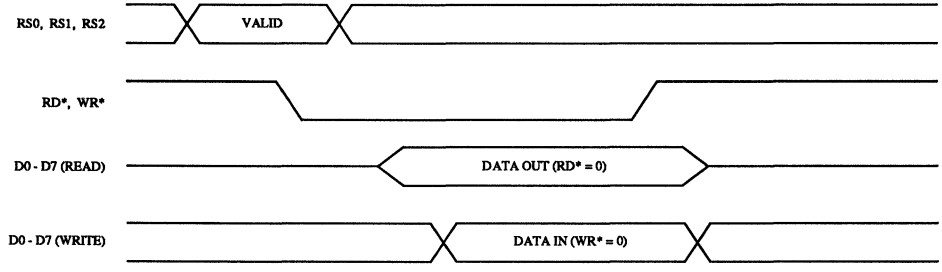


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

24-Bit True-Color Mode

24 bits of RGB color information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0 - R7, G0 - G7, and B0 - B7 inputs. R0 - R7 address the red color palette RAM, G0 - G7 address the green color palette RAM, and B0 - B7 address the blue color palette RAM. Each RAM provides eight bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

24 bits of pixel information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0 - R7, G0 - G7, and B0 - B7 inputs. R0 - R7 drive the red DAC directly, G0 - G7 drive the green DAC directly, and B0 - B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

8 bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information (P0 - P7) are input via the R0 - R7, G0 - G7 or B0 - B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same eight bits of pixel data (P0 - P7). Each RAM provides eight bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Mode

8 bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information are input via the R0 - R7, G0 - G7 or B0 - B7 inputs, as specified by CR7 and CR6:

R0 - R7 Inputs Selected	G0 - G7 Inputs Selected	B0 - B7 Inputs Selected	Input Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As seen in the table, three bits of red, three bits of green, and two bits of blue data are input. The three MSBs of the red and green DACs are driven directly by the inputs, while the two MSBs of the blue DAC are driven directly. The five LSBs for the red and green DACs, and the six LSBs for the blue DAC, are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

15-Bit True-Color Mode

15 bits of pixel information may be input into the Bt473 every clock cycle. The 15 bits of pixel information (5 bits of red, 5 bits of green, and 5 bits of blue) are input via the R0 - R7 and G0 - G7 inputs:

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The three LSBs are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

Overlays

The overlay inputs, OL0 - OL3, have priority regardless of the color mode, as shown in Table 3.

Circuit Description (continued)

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0 - R7, G0 - G7, and B0 - B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0 depending on the mode). Bit D0 also corresponds to data bus bit D0.

Programmable Setup

The command register specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be used.

Video Generation

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt473 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

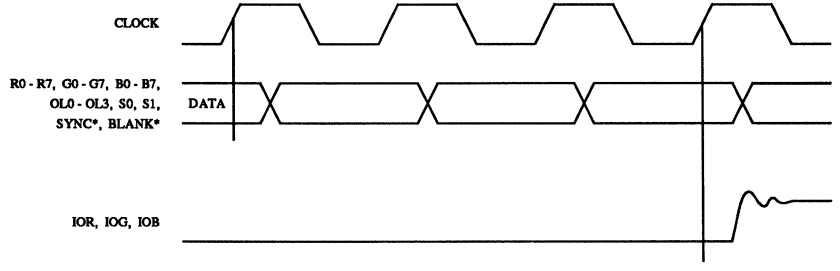
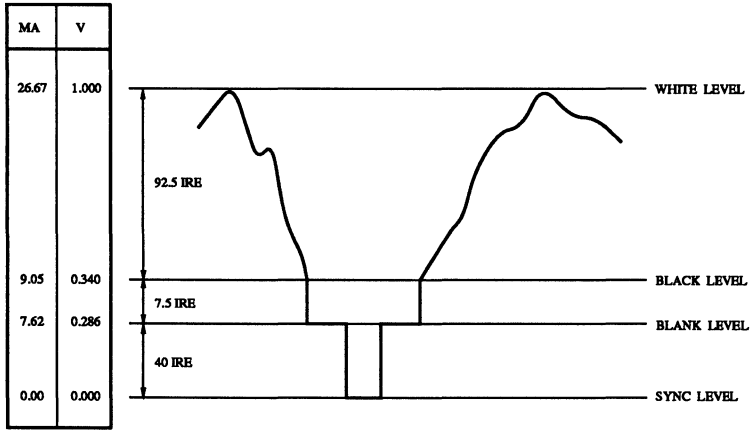


Figure 2. Video Input/Output Timing.

Circuit Description (continued)



Note: 75-ohm doubly-terminated load, SETUP = 7.5 IRE, VREF = 1.235v, RSET = 140 ohms. RS-343A levels and tolerances assumed on all levels.

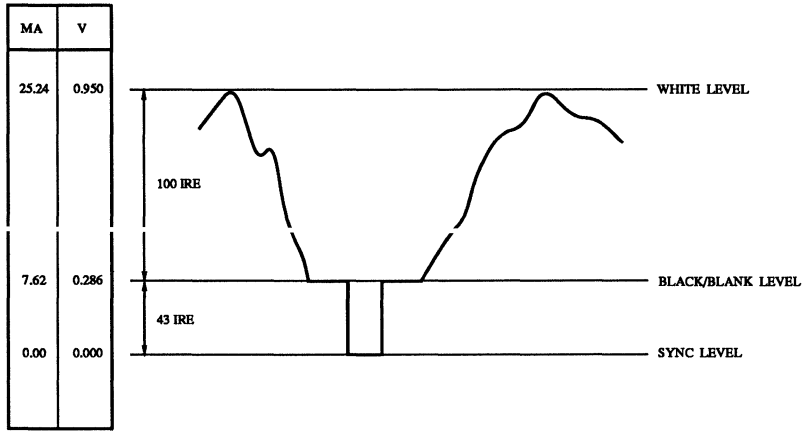
Figure 3. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, VREF = 1.235v, RSET = 140 ohms.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 75-ohm doubly-terminated load, SETUP = 0 IRE, VREF = 1.235v, RSET = 140 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	25.24	1	1	$FF
DATA	data + 7.62	1	1	data
DATA - SYNC	data	0	1	data
BLACK	7.62	1'	1	$00
BLACK - SYNC	0	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, VREF = 1.235v, RSET = 140 ohms.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 is the least significant bit and corresponds to D0.

CR7, CR6	Color mode select	These bits are used to control the various color modes, as shown in Table 3.
CR5	Setup select (0) 0 IRE (1) 7.5 IRE	Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal.
CR4	8-bit / 6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles).
CR3 - CR0	CR3 - CR0 outputs	These bits are output onto the CR3 - CR0 pins.

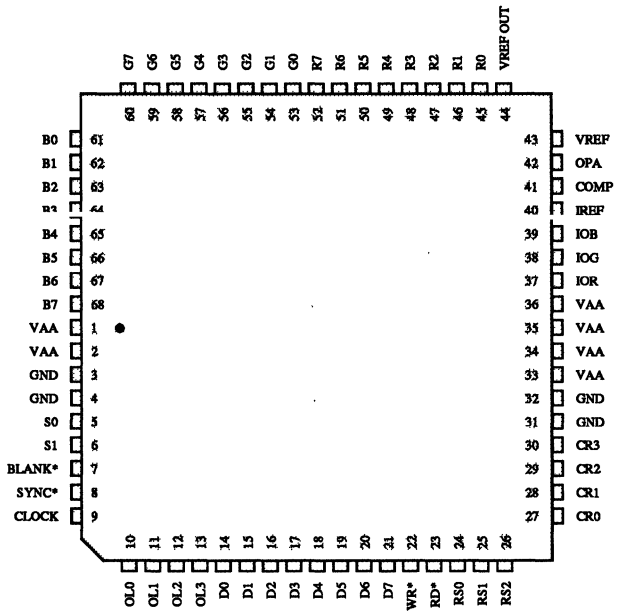
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0 - R7, G0 - G7, B0 - B7, S0, S1, OL0 - OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer.
R0 - R7, G0 - G7, B0 - B7	Red, green, and blue pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the red, green, and blue color palette RAMs is to be used to provide color information. They are latched on the rising edge of CLOCK. R0, G0, and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color mode select inputs (TTL compatible). These inputs specify the mode of operation as shown in Table 3. They are latched on the rising edge of CLOCK.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the R0 - R7, G0 - G7, B0 - B7, S0, and S1 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figures 5, 6, and 7).
IREF	When using a voltage reference (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: for SETUP = 7.5 IRE: RSET (ohms) = 3,195 * VREF (v) / Iout (mA) for SETUP = 0 IRE: RSET (ohms) = 3,025 * VREF (v) / Iout (mA) When using an external current reference (Figure 7), the relationship between IREF and the full scale output current on each output is: for SETUP = 7.5 IRE: IREF (mA) = Iout (mA) / 3.195 for SETUP = 0 IRE: IREF (mA) = Iout (mA) / 3.025

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. If an external voltage reference is used (Figures 5 and 6), this pin should be connected to OPA. If an external current reference is used (Figure 7), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. If a voltage reference is used (Figures 5 and 6), it must supply this input with a 1.2v (typical) reference. If an external current reference is used (Figure 7), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to VAA, as shown in Figures 5, 6, and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If a voltage reference is used (Figures 5 and 6), this pin must be connected to COMP. When using an external current reference (Figure 7), this pin should be left floating.
VREF OUT	Voltage reference output. This output provides a 1.2v (typical) reference, and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. See Figures 5 and 6. Up to four Bt473s may be driven by this output.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
WR*	Write control input (TTL compatible). D0 - D7 data is latched on the rising edge of WR*, and RS0 - RS2 are latched on the falling edge of WR* during MPU write operations. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0 - RS2 are latched on the falling edge of RD* during MPU read operations. See Figure 1.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 - RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
CR0 - CR3	Control outputs (TTL compatible). These outputs are used to control application-specific features. The output values are determined by the command register.

Pin Descriptions (continued)



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt473 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt473 ground pins, any voltage reference circuitry, power supply bypass circuitry for the Bt473, the analog output traces, and all the digital signal traces leading up to the Bt473.

Power Planes

The Bt473 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5, 6, and 7. This bead should be located within three inches of the Bt473.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt473 power pins and any current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt473 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high-frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt473 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

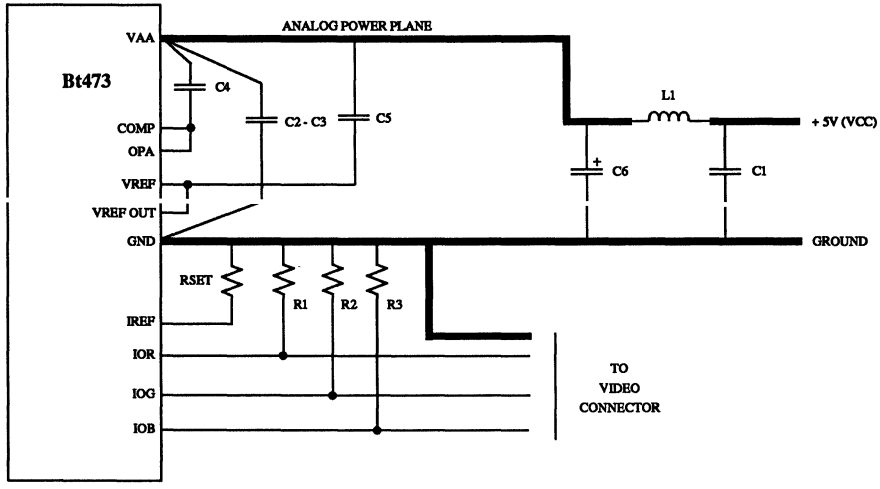
Analog Signal Interconnect

The Bt473 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt473 to minimize reflections.

PC Board Layout Considerations (continued)

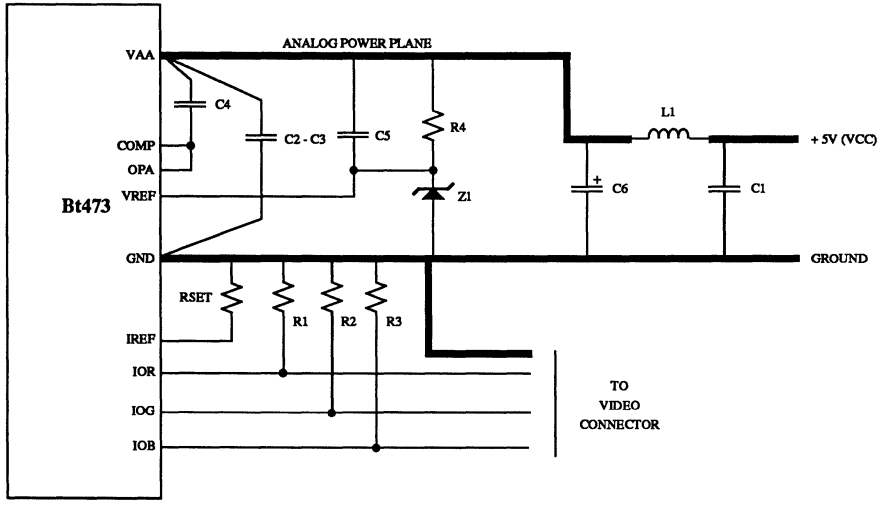


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	140-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 5. Typical Connection Diagram and Parts List. (Internal Voltage Reference)

PC Board Layout Considerations (continued)

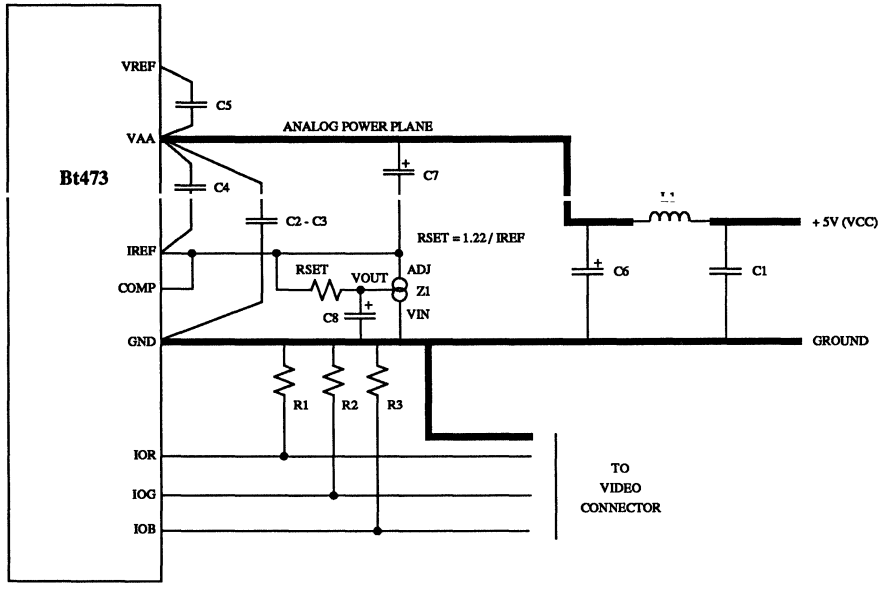


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1000-ohm 1k-ohm 1% resistor	Dale CMF-55C
RSET	140-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 6. Typical Connection Diagram and Parts List. (External Voltage Reference)

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7	47 µF capacitor	Mallory CSR13F476KM
C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 7. Typical Connection Diagram and Parts List. (External Current Reference)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		- 3	- 8.39	- 10	mA
PS/2 Compatible		- 3	- 8.88	- 10	mA

5

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
Using External Reference				±5	% Gray Scale
Using Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA+0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current (D0 - D7)	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.5	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Reference Input Current	IREF IN		10		µA
Reference Output Voltage	VREF OUT	1.08	1.2	1.32	Volts
Reference Output Current	IREF OUT		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	%/% ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 ohms, VREF = 1.235v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ± 10% rather than the ± 5% specified above.

Analog Output Levels -- PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 ohms, VREF = 1.235v or external current reference with IREF = -8.88 mA.

A.C. Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0 - CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	12.5			15.15			ns
Clock Pulse Width High Time	15	4			5			ns
Clock Pulse Width Low Time	16	4			5			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time*	19		13			13		ns
Clock and Data Feedthrough*			-30			-30		dB
Glitch Impulse*			150			150		pV - sec
DAC to DAC Crosstalk			-23			-23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on next page.

A.C. Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0 - CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	20			28			ns
Clock Pulse Width High Time	15	6			7			ns
Clock Pulse Width Low Time	16	6			9			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time*	19		13			13		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			150			150		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 ohms, VREF = 1.235v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA (max).

Timing Waveforms

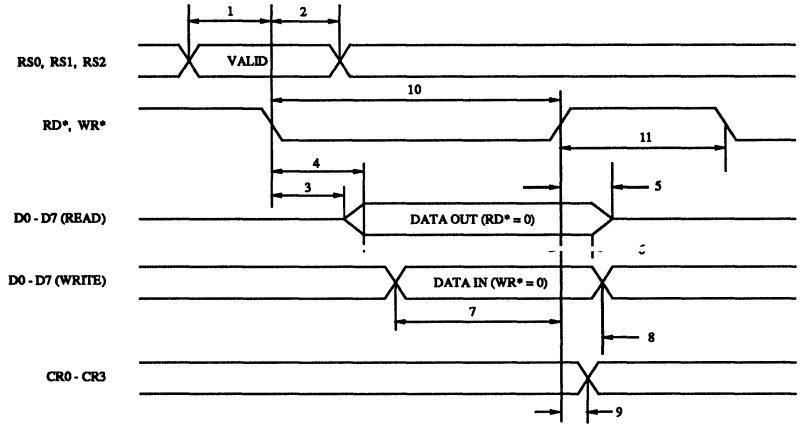
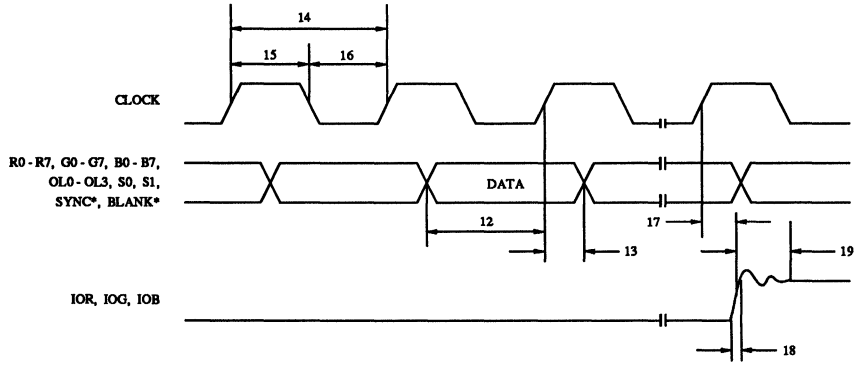


Figure 8. MPU Read/Write Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt473KPJ80	80 MHz	68-pin Plastic J-Lead	0° to +70° C.
Bt473KPJ66	66 MHz	68-pin Plastic J-Lead	0° to +70° C.
Bt473KPJ50	50 MHz	68-pin Plastic J-Lead	0° to +70° C.
Bt473KPJ35	35 MHz	68-pin Plastic J-Lead	0° to +70° C.

Bt479

80 MHz

1024 x 24 Color Palette

Personal System/2®

RAMDAC™

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

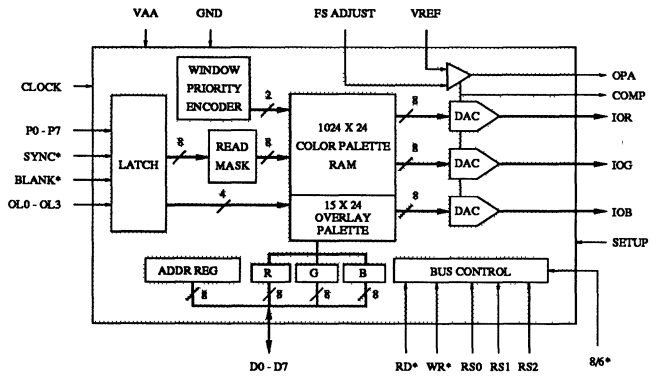
Distinguishing Features

- Personal System/2® Compatible
- Bt471/476/478 Pin Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- 1024 x 24 Color Palette RAM
- 16 Window Priority Encoder
- RS-343A/RS-170 Compatible Outputs
- 15 Overlay Registers
- Sync Enable/Disable for Each Channel
- Programmable Pedestal
- External Voltage or Current Reference
- Standard MPU Interface
- 44-pin PLCC Package

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt479 RAMDAC is designed specifically for Personal System/2® compatible color graphics.

It supports up to 1,024 simultaneous colors out of a 16.8 million color palette through the 1K x 24 color palette RAM and triple 8-bit D/A converters.

The Bt479 may also be configured to display up to 16 windows (plus background) using four unique 256 color palettes. An on-chip 16 window priority encoder provides window display priority, color palette selection, and window placement (with pixel resolution).

The 8/6* pin enables the Bt479 to emulate the Bt471 RAMDAC, including being software-compatible and pin-compatible with the Bt471.

Additional features include up to 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is sync generation on all three channels (with each channel independently enabled or disabled), a programmable pedestal (0 or 7.5 IRE) and use of either an external voltage or current reference.

The Bt479 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
(800) VIDEO IC
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L479001 Rev. A

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt479 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 - RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. Four additional bits in the command register are used to specify which one of the four 256-color palettes are being accessed by the MPU as shown in Table 2. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) and optionally the command register with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register (ADDR0 - ADDR7) then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) and optionally the command register with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register (ADDR0 - ADDR7) is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register (ADDR0 - ADDR7) then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register (ADDR0 - ADDR7) is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Circuit Description (continued)

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4 - 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e. block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

6-Bit Mode

The Bt479 is configured as a Bt471 RAMDAC if 8/6* is a logical zero. In this mode, only color palette RAM_0 is used, in addition to all 15 overlay colors. The operation of the pixel and overlay inputs are shown in Table 3. Six bits of color information are input and output each write/read cycle, with D5 being the MSB and D0 the LSB. D6 and D7 are ignored during write cycles, and are a logical zero during read cycles.

Note that in the 6-bit mode, the Bt479's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Pixel Read Mask Register

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 - P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask bits in the command register are bit-wise logically ANDed with the OL0 - OL3 inputs. The addressed RAM/overlay location provides 24 bits of color information to the three D/A converters.

Window Priority Encoder

If 8/6* and W/C* are both a logical one, up to 16 prioritized windows are available. Each window may use one of the four 256-color palettes. The operation of the pixel and overlay inputs in this mode are shown in Table 4.

Each window is controlled by the four window control registers. The location of each window is specified by it's top/left and bottom/right (x,y) coordinates. Which one of the four 256-color palettes to use is also specified. To arbitrate overlapping windows, the priority of the window is the window number, with window_0 having the highest priority, window_15 the lowest priority.

The Bt479 monitors the SYNC* input to determine the current display position (with pixel resolution). The window positions and sizes are compared to the current display position to determine which windows are being displayed. The window being displayed with the highest priority selects which one of the four 256-color palettes is used. P0 - P7 then select which one of the 256 entries in the color palette is displayed.

If no window is being displayed for the current pixel, color palette RAM_0 is used.

Circuit Description (continued)

Contiguous 1K Color Palette RAM

If 8/6* is a logical one and W/C* is a logical zero, the window priority encoder is disabled and the entire 1K color palette RAM may be addressed directly by the frame buffer. The operation of the pixel and overlay inputs in this mode are shown in Table 5.

OL2 and OL3 select which one of the four 256 color palettes to use while P0 - P7 select the entry within the 256 color palette. OL0 and OL1 select one of three overlay colors.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 - P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask bits in the command register are bit-wise logically ANDed with the OL0 - OL3 inputs. The addressed RAM/overlay location provides 24 bits of color information to the three D/A converters.

Frame Buffer Interface

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used.

The analog outputs of the Bt479 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register low (RAM write mode)
0	1	1	address register low (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register low (overlay write mode)
1	1	1	address register low (overlay read mode)
1	0	1	overlay registers
1	1	0	control registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	CR07 - CR04	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00		x	0	1	red value
	01		x	0	1	green value
	10		x	0	1	blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0000	0	0	1	color palette RAM_0 *
	$00 - $FF	0001	0	0	1	color palette RAM_1 *
	$00 - $FF	0010	0	0	1	color palette RAM_2 *
	$00 - $FF	0011	0	0	1	color palette RAM_3 *
	$x0	xxxx	1	0	1	flood color*
	$x1	xxxx	1	0	1	overlay color 1 *
	:	:	:	:	:	:
	$xF	xxxx	1	0	1	overlay color 15 *
	$00	xxxx	1	1	0	window(0) x1 low
	$01	xxxx	1	1	0	window(0) x1 high
	$02	xxxx	1	1	0	window(0) x2 low
	$03	xxxx	1	1	0	window(0) x2 high
	$04	xxxx	1	1	0	window(0) y1 low
	$05	xxxx	1	1	0	window(0) y1 high
	$06	xxxx	1	1	0	window(0) y2 low
	$07	xxxx	1	1	0	window(0) y2 high
	$08	xxxx	1	1	0	window(1) x1 low
	$09	xxxx	1	1	0	window(1) x1 high
	$0A	xxxx	1	1	0	window(1) x2 low
	$0B	xxxx	1	1	0	window(1) x2 high
	$0C	xxxx	1	1	0	window(1) y1 low
	$0D	xxxx	1	1	0	window(1) y1 high
	$0E	xxxx	1	1	0	window(1) y2 low
	$0F	xxxx	1	1	0	window(1) y2 high
	:	:	:	:	:	:
	$78	xxxx	1	1	0	window(15) x2 low
	$79	xxxx	1	1	0	window(15) x2 high
	$7A	xxxx	1	1	0	window(15) x2 low
	$7B	xxxx	1	1	0	window(15) x2 high
	$7C	xxxx	1	1	0	window(15) y2 low
	$7D	xxxx	1	1	0	window(15) y2 high
	$7E	xxxx	1	1	0	window(15) y2 low
	$7F	xxxx	1	1	0	window(15) y2 high
	$80	xxxx	1	1	0	vertical count low
	$81	xxxx	1	1	0	vertical count high
	$82	xxxx	1	1	0	command register_0
	$83	xxxx	1	1	0	command register_1
	$84	xxxx	1	1	0	flood register low
	$85	xxxx	1	1	0	flood register high

*Indicates requires three read/write cycles -- R, G, B. CR07 - CR04 are command register_0 bits D7 - D4.

Table 2. Address Register (ADDR) Operation (8/6 = Logical One).*

Circuit Description (continued)

OL3 - OL0	P0 - P7	Addressed by frame buffer
0000	$00	color palette RAM_0 location $00
0000	$01	color palette RAM_0 location $01
:	:	:
0000	$FF	color palette RAM_0 location $FF
0001	$xx	overlay color 1
0010	$xx	overlay color 2
:	:	:
1111	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table. (8/6 = Logical Zero)*

OL1, OL0	OL3, OL2	P0 - P7	Addressed by frame buffer
00	00	$00	color palette RAM_0 location $00
00	00	$01	color palette RAM_0 location $01
:	:	:	:
00	00	$FF	color palette RAM_0 location $FF
00	01	$00	color palette RAM_1 location $00
00	01	$01	color palette RAM_1 location $01
:	:	:	:
00	01	$FF	color palette RAM_1 location $FF
00	10	$00	color palette RAM_2 location $00
00	10	$01	color palette RAM_2 location $01
:	:	:	:
00	10	$FF	color palette RAM_2 location $FF
00	11	$00	color palette RAM_3 location $00
00	11	$01	color palette RAM_3 location $01
:	:	:	:
00	11	$FF	color palette RAM_3 location $FF
01	xx	$xx	overlay color 1
10	xx	$xx	overlay color 2
11	xx	$xx	overlay color 3

Table 4. Pixel and Overlay Control Truth Table. (8/6 = Logical One, 1K x 24 Color Palette)*

Circuit Description (continued)

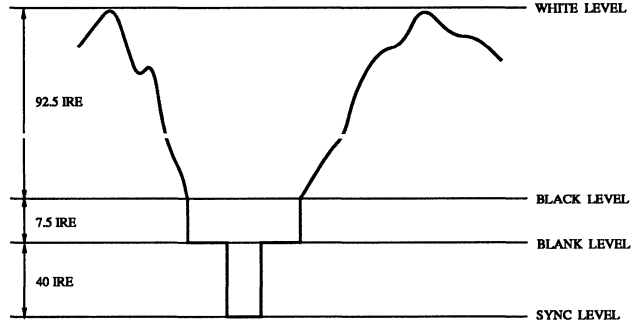
OL3 - OL0	Palette*	P0 - P7	Addressed by frame buffer
0000	0	$00	color palette RAM_0 location $00
0000	0	$01	color palette RAM_0 location $01
:	:	:	:
0000	0	$FF	color palette RAM_0 location $FF
0000	1	$00	color palette RAM_1 location $00
0000	1	$01	color palette RAM_1 location $01
:	:	:	:
0000	1	$FF	color palette RAM_1 location $FF
0000	2	$00	color palette RAM_2 location $00
0000	2	$01	color palette RAM_2 location $01
:	:	:	:
0000	2	$FF	color palette RAM_2 location $FF
0000	3	$00	color palette RAM_3 location $00
0000	3	$01	color palette RAM_3 location $01
:	:	:	:
0000	3	$FF	color palette RAM_3 location $FF
0001	x	$xx	overlay color 1
0010	x	$xx	overlay color 2
:	:	:	:
1111	x	$xx	overlay color 15

*As determined by the window priority encoder.

Table 5. Pixel and Overlay Control Truth Table. (8/6* = Logical One, Four Prioritized 256 x 24 Color Palettes)

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = VAA. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 1. Composite Video Output Waveforms (SETUP = VAA).

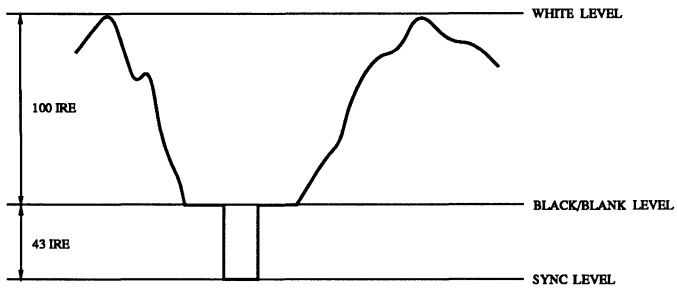
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = VAA. VREF = 1.235v, RSET = 147 ohms.

Table 6. Video Output Truth Table (SETUP = VAA).

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = GND. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND).

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = GND. VREF = 1.235v, RSET = 147 ohms.

Table 7. Video Output Truth Table (SETUP = GND).

Internal Registers

Window_0 - Window_15 x1 and x2 Registers

The 16-bit (x1) and (x2) registers are used to specify the left and right sides of each window, by specifying the number of clock cycles from the falling edge of SYNC* to the left or right side of the window. The lower value of (x1) or (x2) specifies the left side, the higher value of (x1) or (x2) specifies the right side. If (x1) and (x2) are equal, the window is not displayed. These registers are ignored if 8/6* is a logical zero.

The window (x1) register is made up of the window (x1) low register (WX1LR) and the window (x1) high register (WX1HR); the window (x2) register is made up of the window (x2) low register (WX2LR) and the window (x2) high register (WX2HR). They are not initialized and may be written to or read by the MPU at any time.

WX1LR and WX1HR are cascaded to form a 12-bit window (x1) register. Similarly, WX2LR and WX2HR are cascaded to form a 12-bit window (x2) register.

	Window (x1) High (WX1HR)				Window (x1) Low (WX1LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (x2) High (WX2HR)				Window (x2) Low (WX2LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

D4 - D7 of window (x1) high register specifies which color palette to use for the corresponding window:

D7 - D4	Palette
0000	color palette RAM_0
0001	color palette RAM_1
0010	color palette RAM_2
0011	color palette RAM_3
0100	reserved
:	:
1111	reserved

D4 - D7 of window (x2) high register are always a logical zero.

Values from $0000 to $0FFF may be written into the x1 and x2 registers.

For both (x1) and (x2), the MPU must write 8 bits to the low register, followed by 8 bits to the high register. During the high register write cycle, the 12 bits of (x) information are loaded into the registers.

Internal Registers (continued)

Window_0 - Window_15 y1 and y2 Registers

The 16-bit (y1) and (y2) registers are used to specify the top and bottom of each window, by specifying the number of scan lines from a vertical sync being detected on SYNC* to the top or bottom of the window. The lower value of (y1) or (y2) specifies the top, the higher value of (y1) or (y2) specifies the bottom. If (y1) and (y2) are equal, the window is not displayed. These registers are ignored if 8/6* is a logical zero.

The window (y1) register is made up of the window (y1) low register (WY1LR) and the window (y1) high register (WY1HR); the window (y2) register is made up of the window (y2) low register (WY2LR) and the window (y2) high register (WY2HR). They are not initialized and may be written to or read by the MPU at any time.

WY1LR and WY1HR are cascaded to form a 12-bit window (y1) register. Similarly, WY2LR and WY2HR are cascaded to form a 12-bit window (y2) register.

	Window (y1) High (WY1HR)				Window (y1) Low (WY1LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

	Window (y2) High (WY2HR)				Window (y2) Low (WY2LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

D4 - D7 of window (y2) high and (y1) high registers are always a logical zero.

Values from $0000 to $0FFF may be written into the y1 and y2 registers.

For both (y1) and (y2), the MPU must write 8 bits to the low register, followed by 8 bits to the high register. During the high register write cycle, the 12 bits of (y) information are loaded into the registers.

Vertical Count Register

This 16-bit vertical count register specifies the number of clock cycles SYNC* must be a logical zero for it to be recognized by the Bt479 to be a vertical sync interval. Values from $0000 (1) to $0FFF (256) may be specified.

The 8-bit vertical count low and high registers are cascaded to form the 16-bit vertical count register. The MPU must write 8 bits to the low register, followed by 8 bits to the high register. During the high register write cycle, the 12 bits of vertical count information are loaded into the registers. D4 - D7 of the vertical high count register are always a logical zero.

These registers may be written to or read by the MPU at any time and are not initialized. They are ignored if 8/6* is a logical zero.

Internal Registers (continued)

Pixel Read Mask Register

This 8-bit register is bit-wise logically ANDed with the P0 - P7 inputs prior to addressing the overlay and color palettes. D0 corresponds to P0 and D7 corresponds to P7. This register may be written to or read by the MPU at any time and is not initialized.

Command Register_0

This 8-bit register may be written to or read by the MPU at any time and is not initialized. It is ignored if 8/6* is a logical zero.

D0 - D3 are bit-wise logically ANDed with the OL0 - OL3 inputs prior to address the overlay and color palettes. D0 corresponds to OL0 and D3 corresponds to OL3. D4 - D7 are used to specify which one of the four color palette RAMs are to be accessed by the MPU as follows:

D7 - D4	Color Palette
0000	color palette RAM_0
0001	color palette RAM_1
0010	color palette RAM_2
0011	color palette RAM_3
0100	reserved
:	:
1111	reserved

Command Register_1

This 8-bit register may be written to or read by the MPU at any time and is not initialized. It is ignored if 8/6* is a logical zero.

D0 specifies whether to configure the color palette RAM as 1K x 24 (logical zero) or a four unique 256 x 24 color palette RAMs (logical one).

D1 specifies whether 6-bit (logical zero) or 8-bit (logical one) color data is written or read from the Bt479. This enables each color palette RAM_0, color palette RAM_1, color palette RAM_2, color palette RAM_3, and the overlay registers to contain either 6-bit or 8-bit color data. For 6-bit operation, six bits of color information are input and output each write/read cycle, with D5 being the MSB and D0 the LSB. D6 and D7 are ignored during write cycles, and are a logical zero during read cycles. For 8-bit operation, eight bits of color information are input and out each write/read cycle, with D7 being the MSB and D0 the LSB.

D2, D3, and D4 are sync enable bits for the red (D2), green (D3), and blue (D4) channels. A logical one enables sync information to be output on the video channel, and a logical zero disables sync information from being output. This enables the Bt479 to be used in applications where sync information is not present in the output video (since the window priority encoder requires sync information to determine window placement).

D5 - D7 are always a logical zero.

Internal Registers (continued)

Flood Registers

The two 8-bit flood registers low and high are used to fill a window (or windows) with the color in the flood color register. Setting a bit to a logical one fills the corresponding window with the flood color.

Flood Register Low	Corresponding Window Number
D0	0
D1	1
D2	2
D3	3
D4	4
D5	5
D6	6
D7	7
Flood Register High	
D0	8
D1	9
D2	10
D3	11
D4	12
D5	13
D6	14
D7	15

These registers may be written to or read by the MPU at any time and are not initialized.

These registers are typically used when moving windows. The old window position is filled with the flood color until the system has had time to move the graphics information from the old window location to the new window location.

Pin Descriptions

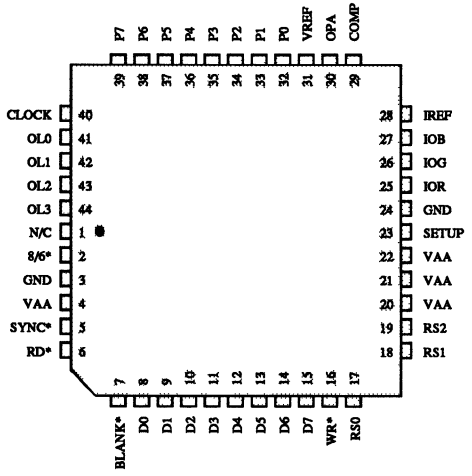
Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input optionally switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P7, OL0 - OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer.
P0 - P7, OL0 - OL3	Pixel and overlay select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 1024 entries in the color palette RAM or 15 overlay registers is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 and OL0 are the LSBs. Unused inputs should be connected to GND.
IREF	Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current. When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: RSET (ohms) = K * 1,000 * VREF (v) / Iout (mA) When using an external current reference (Figure 4), the relationship between IREF and the full scale output current on each output is: IREF (mA) = Iout (mA) / K K is defined in the table below along with corresponding RSET values for doubly-terminated 75-ohm loads.

	Sync Enabled		Sync Disabled	
Setup	0 IRE	7.5 IRE	0 IRE	7.5 IRE
K=	3.025	3.195	3.000	3.170

IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figures 3 and 4).
COMP	Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
OPA	Reference amplifier output. If an external voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.
VREF	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2v (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to VAA, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
WR*	Write control input (TTL compatible). D0 - D7 data is latched on the rising edge of WR*, and RS0 - RS2 are latched on the falling edge of WR* during MPU write operations.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0 - RS2 are latched on the falling edge of RD* during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 - RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
8/6*	8-bit/6-bit select input (TTL compatible). A logical zero forces the Bt479 to function as a Bt471 RAMDAC. D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles). A logical one enables the Bt479 to input and output 8-bit color data (D7 is the most significant data bit during color read/write cycles) and access the additional color palette RAM and windowing functions.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt479 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt479 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the Bt479, the analog output traces, and all the digital signal traces leading up to the Bt479.

Power Planes

The Bt479 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 3 and 4. This bead should be located within three inches of the Bt479.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt479 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt479 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high-frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt479 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt479 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

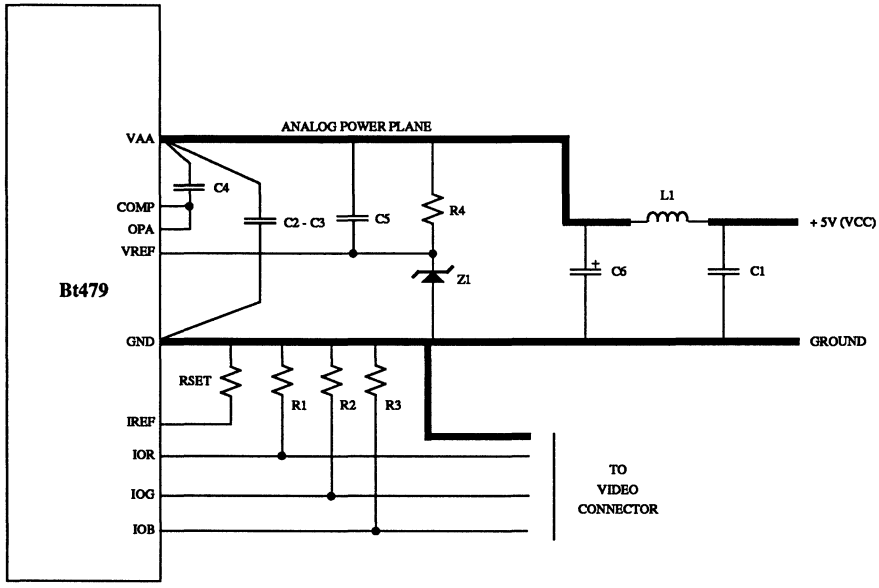
Analog Signal Interconnect

The Bt479 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt479 to minimize reflections.

PC Board Layout Considerations (continued)

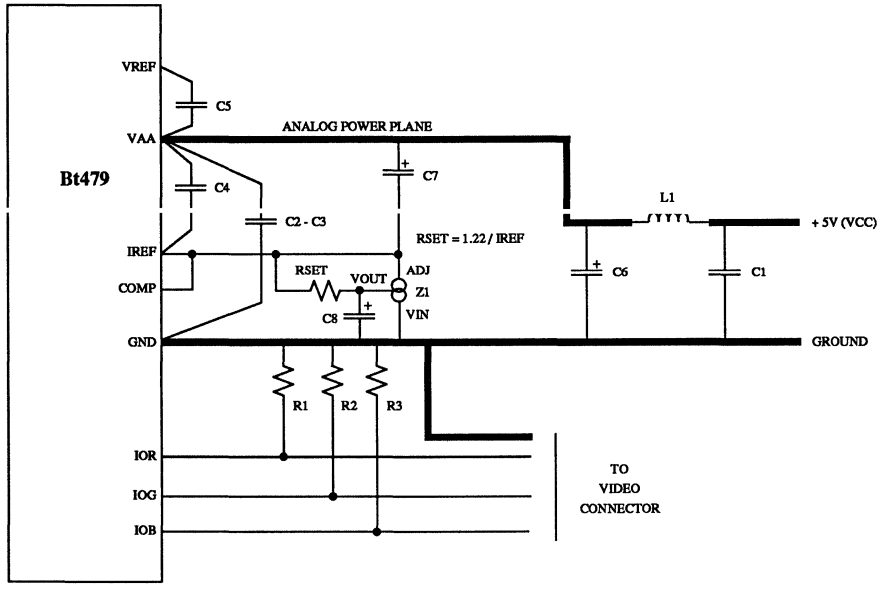


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1k-ohm 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt479.

Figure 3. Typical Connection Diagram and Parts List. (External Voltage Reference)

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7	47 µF capacitor	Mallory CSR13F476KM
C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt479.

Figure 4. Typical Connection Diagram and Parts List. (External Current Reference)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		- 3	- 8.39	- 10	mA
PS/2 Compatible		- 3	- 8.88	- 10	mA

5

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (2 minutes)	TVSOL			tbd	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = VAA		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.5	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IREF IN		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Analog Output Levels -- PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = VAA		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 ohms, VREF = 1.235v or external current reference with IREF = -8.88 mA.

A.C. Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			-30			-30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			-23			-23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		tbd	tbd		tbd	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		tbd	tbd		tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v, SETUP = VAA, 8/6* = logical one. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA (max).

Timing Waveforms

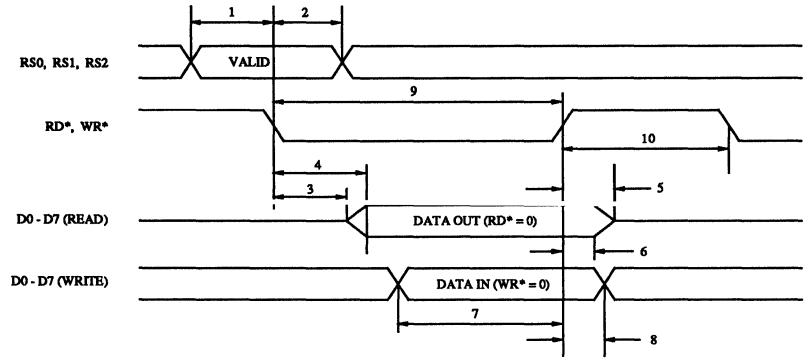
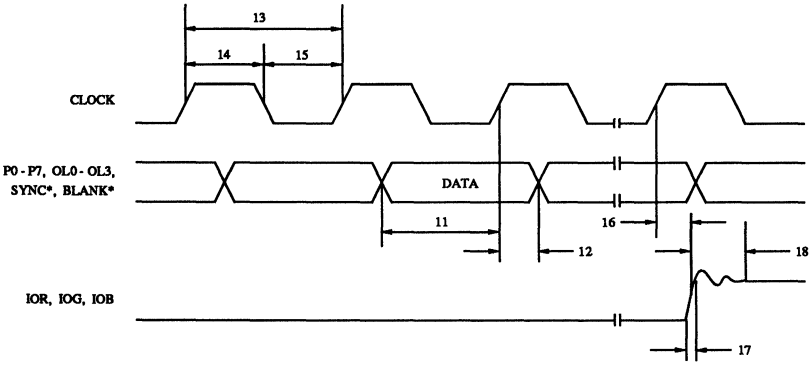


Figure 5. MPU Read/Write Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt479KPJ80	80 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt479KPJ66	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt479KPJ50	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt479KPJ35	35 MHz	44-pin Plastic J-Lead	0° to +70° C.

Bt492

360 MHz

100K ECL Compatible

256 x 8 Color Palette

RAMDAC™

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 360 MHz Pipelined Operation
- 256 x 8 Color Palette RAM
- 16 x 8 Overlay RAM
- 350 ps Typical Rise/Fall Time
- RS-343A Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- Drives 1v Into 25-Ohm Output Loads
- 100K ECL Compatible Pixel Inputs
- ÷2 of Clock for Load Generation
- TTL Compatible MPU Interface
- 68-pin Ceramic PGA Package with Heatsink and Alignment Pin
- Typical Power Dissipation: 3.5 W

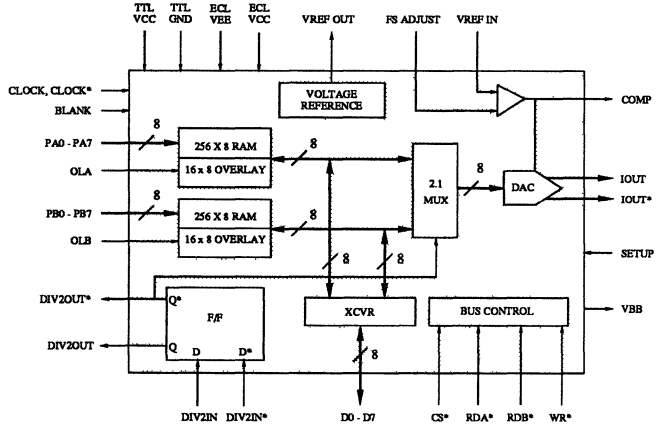
Applications

- Graphics Terminals
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt424

Functional Block Diagram



Product Description

The Bt492 is an 8-bit RAMDAC, designed specifically for high performance, high resolution color graphics.

The 2:1 multiplexed pixel inputs enable interfacing to 180 MHz pixel data, simplifying interfacing to the frame buffer. On-chip divide by 2 of the clock is provided, generating the 180 MHz differential load clocks. The pixel, DIV2IN, and blank inputs, and the DIV2OUT and DIV2OUT* outputs, are 100K ECL compatible. The blanking signal is pipelined to maintain synchronization with the pixel data.

The MPU interface signals (D0 - D7, CS*, RDA*, RDB*, and WR*) are TTL compatible. During MPU accesses to the RAM, the address is input through the pixel ports (PA0 - PA7, PB0 - PB7).

An on-chip voltage reference is available or an external reference may be used. A single external resistor controls the full scale output current.

The Bt492 generates an RS-343A compatible video signal, and is capable of driving either doubly-terminated 75-ohm or 50-ohm coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1/2 LSB over the full temperature range.

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Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt492 has two 256 x 8 RAMs, a 2:1 multiplexer, a single 8-bit DAC, and MPU interface.

MPU data is input and output via the D0 - D7 data lines. During MPU accesses to the color palette RAMs, the RAMs are addressed via the PAx, PBx, and OLx inputs and the internal pipeline registers are transparent. During MPU write cycles (WR* = 0), data is written to both RAMs. The MPU may read either RAM via the RDA* and RDB* control inputs.

BLANK should be asserted during MPU accesses to prevent the data values associated with the MPU address from appearing at the analog outputs. Following an MPU cycle, BLANK should be asserted for at least one valid pixel cycle before the PAx and PBx inputs can be properly routed to the analog outputs.

Frame Buffer Interface

Pixel data on the PA0 - PA7 and OLA inputs (even data) and PB0 - PB7 and OLB inputs (odd data) are latched on the falling edge of DIV2OUT*, as illustrated in Figure 2.

The OLx inputs determine whether the Px0 - Px7 inputs address the 256 x 8 color palette RAM (OLx = 0) or the 16 x 8 overlay palette RAM (OLx = 1). When addressing the overlay RAM, Px4 - Px7 are ignored. The outputs of the RAMs are then multiplexed at the pixel clock rate and drive the 8-bit video D/A converter.

DIV2IN is defined to be 1/2 the CLOCK rate. To simplify system design, the Bt492 outputs a DIV2OUT* signal, which when connected to the DIV2IN pin, generates a clock equal to 1/2 the CLOCK rate. For a color system requiring three Bt492s, the DIV2OUT signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Care should be taken to keep signal paths short and equal for each connection. The unused DIV2OUT signals from the remaining Bt492s can be used to clock the shift registers driving the Bt492 pixel inputs.

The BLANK input is also latched on the falling edge of DIV2OUT* and overrides the PA0 - PA7, OLA, PB0 - PB7, and OLB inputs. Blanking information is output synchronously with the even pixel data.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and ECL VCC. RSET has a typical value of 1092 ohms for generation of RS-343A video into a 37.5-ohm load, or 729 ohms for generation of RS-343A video into a 25-ohm load. The on-chip voltage reference (VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt492s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25-ohm resistor to ECL VCC (assuming a doubly-terminated 50-ohm load). The IOUT* output is used to generate the positive video signal.

The D/A converter on the Bt492 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt492 are capable of directly driving either a 37.5-ohm or 25-ohm load, such as a doubly-terminated 75-ohm or 50-ohm coaxial cable.

Circuit Description (continued)

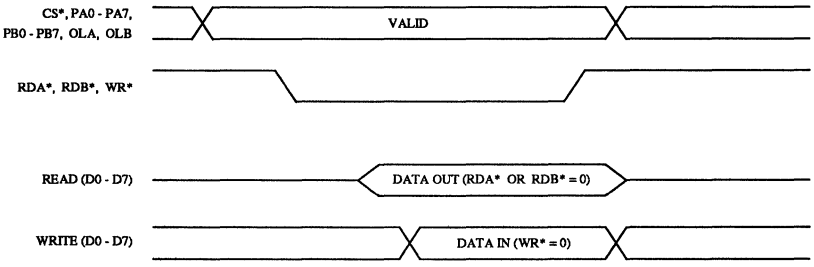


Figure 1. MPU Read/Write Timing.

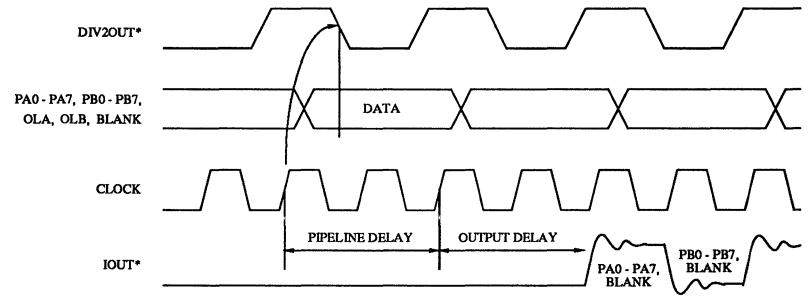
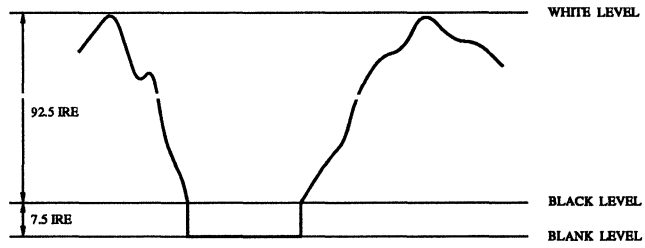


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

MA RSET = 729	MA RSET = 1092	V
00.00	00.00	0.000
- 26.40	- 17.60	- 0.660
- 28.56	- 19.05	- 0.714



Note: RSET = 729 ohms (50-ohm doubly-terminated load) or 1092 ohms (75-ohm doubly-terminated load), VREF IN = -1.2v. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms (IOUT).*

Description	RSET = 729 ohms IOUT* (mA)	RSET = 1092 ohms IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	- 26.40	- 17.62	0	$00
BLANK			1	$xx
SETUP = ECL VCC	- 26.40	- 17.62		
SETUP = float	- 28.56	- 19.05		

Note: Typical with VREF IN = -1.2v.

Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logic one drives the analog output to the blanking level, as illustrated in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the PA0 - PA7, PB0 - PB7, OLA, and OLB inputs are ignored. Blanking information is output synchronously with the even pixel data.
PA0 - PA7, PB0 - PB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT* while CS* is a logical one. PAx represent the even pixel data, and PBx represent the odd pixel data. Even data represents the first (leftmost) pixel on the display screen. Coding is binary. PA0 and PB0 are the LSBs.
OLA, OLB	Even and odd overlay data inputs (ECL compatible). When OLA or OLB are a logical one, the 4 MSBs of the corresponding pixel inputs (Px4 - Px7) are ignored and the 4 LSBs are used to select one of 16 available data words in the overlay palette. They are latched on the falling edge of DIV2OUT* while CS* is a logical one. If left floating, they will pull themselves to DVEE.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). They are typically the pixel clock rate of the video system.
DIV2IN, DIV2IN*	Differential CLOCK/2 inputs (ECL compatible). These clocks must be 1/2 the CLOCK rate. They may be configured for single-ended operation by connecting DIV2IN* to VBB.
DIV2OUT*, DIV2OUT	CLOCK/2 differential outputs (ECL compatible). When DIV2OUT* is connected to the DIV2IN pin, these outputs are 1/2 the CLOCK rate. When not connected to DIV2IN, they generate a signal that is DIV2IN synchronized to CLOCK and inverted.
IOUT, IOUT*	Differential video current outputs. These high impedance current sources are capable of directly driving either a doubly-terminated 50-ohm or 75-ohm coaxial cable (Figures 4 and 5). Both outputs, whether used or not, should have the same output load for best settling time.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 µF ceramic chip capacitor must be connected between this pin and AVEE (Figures 4 and 5). The COMP capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum.
SETUP	Pedestal control input. If connected to ECL VCC, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If left floating, the 7.5 IRE blanking pedestal is enabled. See Figure 3.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and ECL VCC controls the magnitude of the full scale video signal (Figures 4 and 5). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current is: RSET (ohms) = K * VREF IN (v) / IOUT (mA) where K = 17,205 if SETUP = float or 15,915 if SETUP = ECL VCC. Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing and depending on whether the internal or an external reference is used.

Pin Descriptions (continued)

Pin Name	Description
VREF OUT	Voltage reference output. This output provides a -1.2v (typical) reference, and may be connected to the VREF IN inputs of up to three Bt492s. When driving multiple Bt492s, use 100-ohm interconnect resistance to minimize noise pick-up. If it is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 6, or the VREF OUT pin must supply this input with a -1.2v (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and ECL VCC, as shown in Figures 4 and 5. The decoupling capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable MPU data to be written to or read from the device. When it is a logical one, D0 - D7 are three-stated. While CS* is a logical zero, the PA0 - PA7, PB0 - PB7, OLA, and OLB inputs are used to address the color palette RAM and overlay RAM, and the internal pipeline registers are configured to be transparent.
RDA*, RDB*	Read control input (TTL compatible). To read data from RAM A, both CS* and RDA* must be a logical zero. To read data from RAM B, both CS* and RDB* must be a logical zero. MPU addressing on PAx, PBx, and OLx must be valid while RDA* or RDB* is a logical zero. CS*, RDA*, and RDB* must not be a logical zero simultaneously.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. MPU addresses on PAx and PBx are accepted on the falling edge of WR* or CS*, whichever occurs first. Data is accepted on the rising edge of WR* or CS*, whichever occurs first. MPU addressing on PAx, PBx, and OLx must be valid while WR* is a logical zero. RDx* and WR* must not be a logical zero simultaneously.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
VBB	-1.3v output. A 0.01 µF decoupling capacitor to ECL VCC reduces threshold jitter.
TTL VCC	TTL power. All TTL VCC pins must be connected together.
TTL GND	TTL ground. All TTL GND pins must be connected together.
ECL VCC	ECL ground. All ECL VCC pins must be connected together. See Figures 4 and 5.
DVEE	ECL digital power. All DVEE pins must be connected together. See Figures 4 and 5.
AVEE	ECL analog power. All AVEE pins must be connected together. See Figures 4 and 5. **Warning: It is important that a ferrite bead be used to connect the AVEE power pins to the analog power plane as illustrated in Figures 4 and 5.**
Alignment Pin	The alignment pin is connected to the metallic cavity lid which is electrically isolated.

Pin Descriptions (continued)

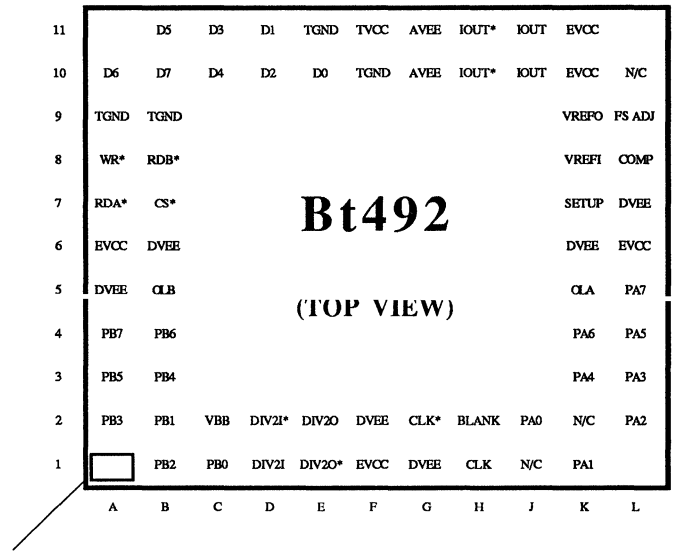
Signal	Pin Number
CLOCK	H1
CLOCK*	G2
DIV2IN	D1
DIV2IN*	D2
DIV2OUT	E2
DIV2OUT*	E1
BLANK	H2
PA0	J2
PA1	K1
PA2	L2
PA3	L3
PA4	K3
PA5	L4
PA6	K4
PA7	L5
OLA	K5
PB0	C1
PB1	B2
PB2	B1
PB3	A2
PB4	B3
PB5	A3
PB6	B4
PB7	A4
OLB	B5

Signal	Pin Number
D0	E10
D1	D11
D2	D10
D3	C11
D4	C10
D5	B11
D6	A10
D7	B10
CS*	B7
RDA*	A7
RDB*	B8
WR*	A8
IOUT	J10, J11
IOUT*	H10, H11
SETUP	K7
COMP	L8
VREF IN	K8
VREF OUT	K9
FS ADJUST	L9
N/C	K2
N/C	J1
N/C	L10

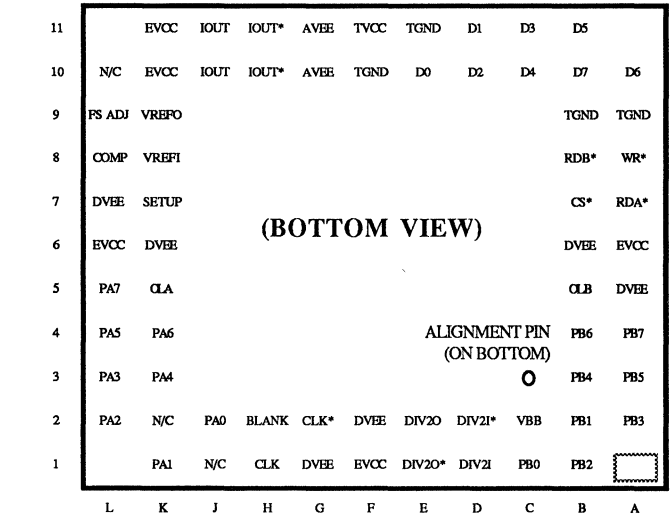
Signal	Pin Number
VBB	C2
TTL VCC	F11
TTL GND	F10
TTL GND	E11
TTL GND	A9
TTL GND	B9
ECL VCC	A6
ECL VCC	F1
ECL VCC	L6
ECL VCC	K10
ECL VCC	K11
DVEE	A5
DVEE	B6
DVEE	F2
DVEE	G1
DVEE	K6
DVEE	L7
AVEE	G10
AVEE	G11
alignment pin (LID)	C3

5

Pin Descriptions (continued)



alignment marker (on top)



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt492 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of AVEE and ECL VCC pins should be minimized so as to minimize inductive ringing.

Sockets

Only flush mount sockets should be used, such as the Advanced Interconnect KS06985TG.

Ground Planes

The ground plane should encompass all Bt492 ground pins, any voltage reference circuitry, power supply bypass circuitry for the Bt492, the analog output traces, and all the digital signal traces leading up to the Bt492.

Power Planes

The Bt492 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 4 and 5. This bead should be located within three inches of the Bt492.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt492 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the AVEE power pins and the analog power plane, as illustrated in Figures 4 and 5. The ferrite bead must be located as close as possible to the AVEE pins.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the AVEE pins as illustrated in Figures 4 and 5.

Digital Signal Interconnect

The digital inputs to the Bt492 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

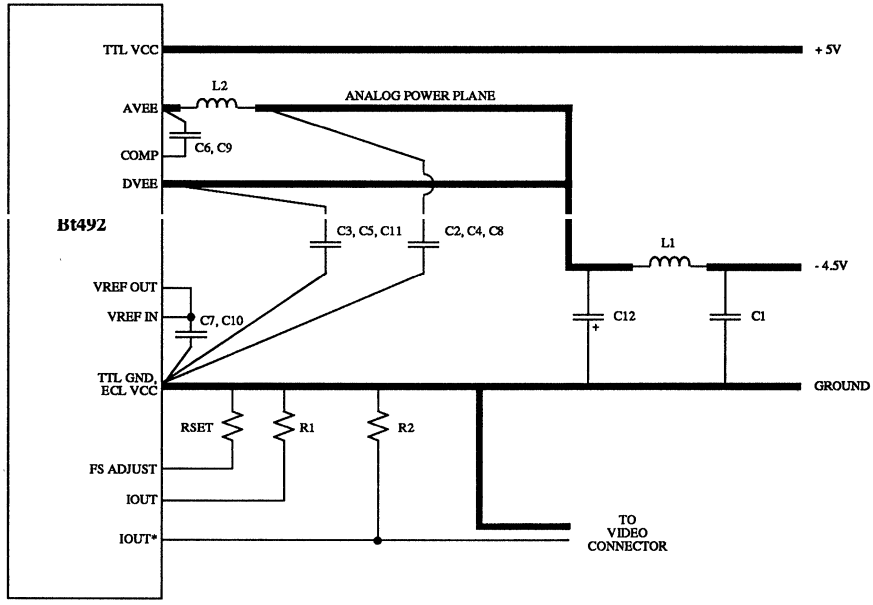
Any termination resistors for the digital inputs should be connected to the regular PCB power or termination and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)

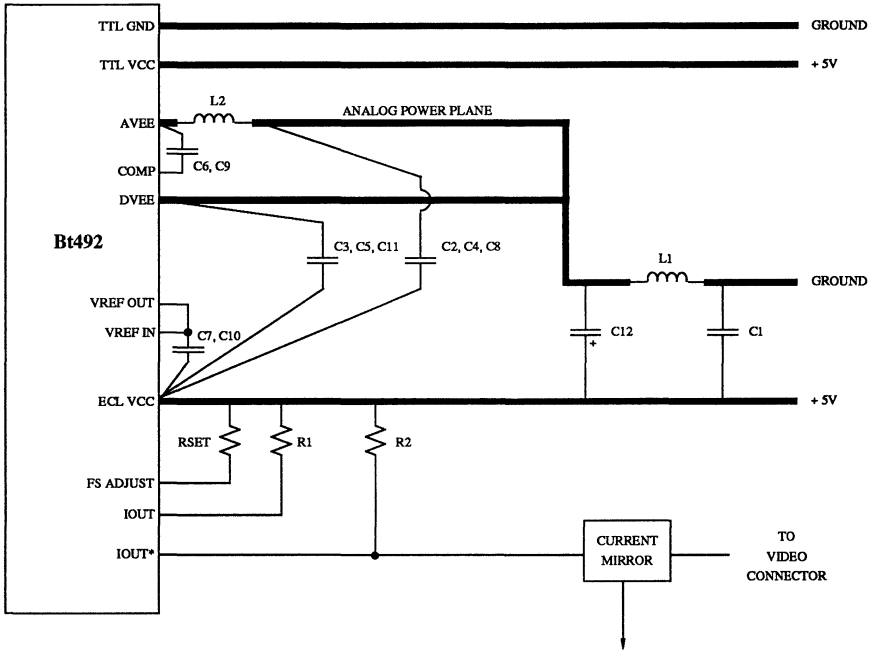


Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4 - C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8 - C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9-ohm 1% metal film resistor	Dale CMF-55C
R2	49.9-ohm 1% metal film resistor	Dale CMF-55C
RSET	732-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly-terminated 50-ohm load on IOUT*.

Figure 4. Typical Connection Diagram and Parts List. (Dual Supply Operation)

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4 - C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8 - C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9-ohm 1% metal film resistor	Dale CMF-55C
R2	49.9-ohm 1% metal film resistor	Dale CMF-55C
RSET	732-ohm 1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly-terminated 50-ohm load on IOUT*.

Figure 5. Typical Connection Diagram and Parts List. (Single Supply Operation)

Application Information

Terminated ECL Inputs

All ECL inputs of the Bt492 should be terminated using normal ECL termination practices. In addition, all of the ECL digital inputs have internal pull-down junctions. Thus, if an ECL digital input is left floating, it assumes the logical zero state.

External Voltage Reference

An external voltage reference may be used with the Bt492, as shown in Figure 6. In this instance, the VREF OUT pin should be left floating.

Note that the VREF IN pin still requires bypass capacitors to ECL VCC.

Single Supply Operation

The Bt492 may be operated from a single +5v supply by connecting the power supply pins as shown:

TTL VCC = +5v
TTL GND = 0v
ECL VCC = +5v
DVEE, AVEE = 0v

The current mirror on the analog output is required to reference the video signal to ground rather than +5v.

Using Multiple Bt492s

For color applications, three Bt492s may be used, as illustrated in Figure 7. This example generates 256 simultaneous colors from a 16.8 million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers (Bt424s). The MPU TTL address bus is also interfaced to the Bt492 pixel inputs via the Bt424s.

Note the DIV2OUT - DIV2IN connections, generating CLOCK/2 and ensuring the three Bt492s operate in a synchronous fashion. When analyzing the timing window for DIV2IN, be sure to include the propagation delay of the CLOCK and DIV2OUT signals through the transmission lines of the physical layout on the PC board.

The Bt492s may share the voltage reference and analog power/ground planes, but each Bt492 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, AVEE ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2 line length. Low dielectric stripline is recommended, and the propagation delays between CLOCK and DIV2 should match as closely as possible.

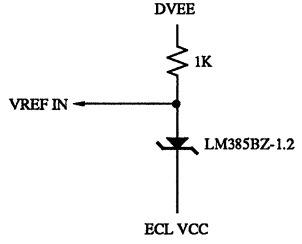


Figure 6. External Voltage Reference.

Application Information (continued)

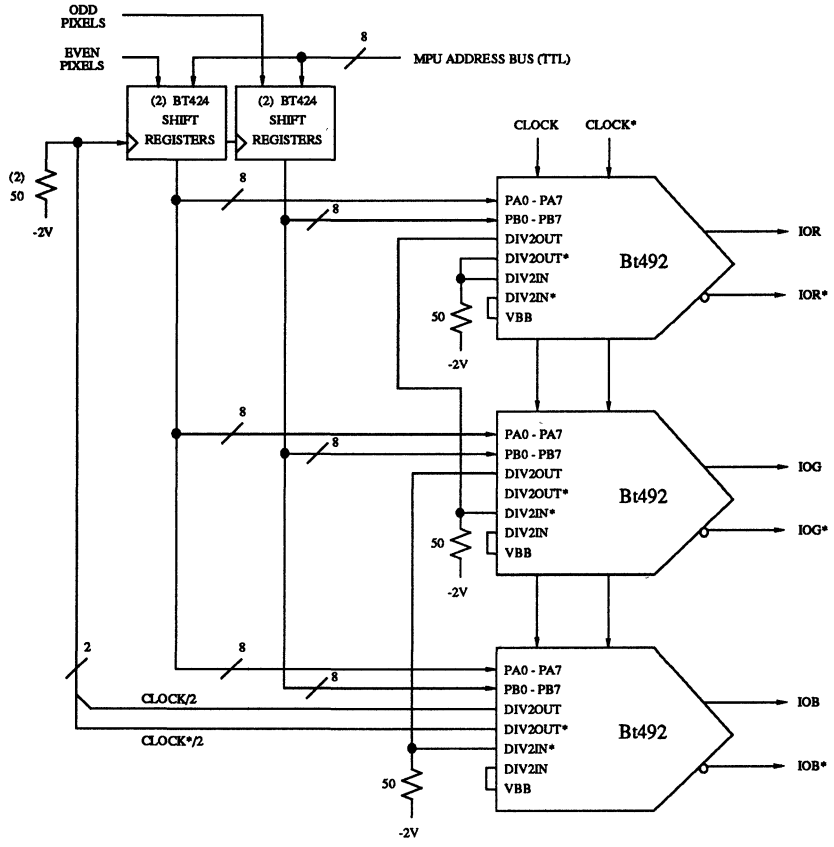


Figure 7. Using Multiple Bt492s.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
ECL Power Supply	DVEE, AVEE	- 4.2	- 4.5	- 5.5	Volts
ECL Ground	ECL VCC		0		Volts
TTL Power Supply	TTL VCC	4.75	5	5.25	Volts
TTL Ground	TTL GND		0		Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		25		Ohms
Reference Voltage	VREF IN	- 1.17	- 1.23	- 1.29	Volts
FS ADJUST Resistor	RSET		729		Ohms

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL Supply (measured to ECL VCC)	DVEE, AVEE			- 6.5	Volts
TTL Supply (measured to GND)	TTL VCC			+ 7.0	Volts
Voltage on any ECL Input Pin		ECL VCC		DVEE	Volts
Voltage on any TTL Pin		TTL GND - 0.5		TTL VCC + 0.5	Volts
Analog Output Short Circuit Duration to any Common			indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4 inch from pin)	TSOL			260	°C.
Junction-to-Ambient					
Still Air				28	°C. / W
400 LFM				13	°C. / W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			± 1/2	LSB
Differential Linearity Error	DL			± 1/2	LSB
Gray Scale Error					
Internal Reference				± 10	% Gray Scale
External Reference				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
TTL Digital Inputs					
Input High Voltage	VIH	2.0		TTL VCC + 0.5	Volts
Input Low Voltage	VIL	TTL GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			70	µA
Input Low Current (Vin = 0.4v)	IIL			- 700	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		6		pF
TTL Digital Outputs					
Output High Voltage (IOH = -2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.4	Volts
3-State Current	IOZ	- 50		50	µA
Output Capacitance	CDOUT		8		pF
ECL Digital Inputs					
Input High Voltage	VIH	- 1165		- 880	mV
Input Low Voltage	VIL	- 1810		- 1475	mV
Input High Current	IIH			220	µA
Input Low Current	IIL	0.5			µA
Input Capacitance (f = 1 MHz, Vin = VIHmax)	CIN		6		pF
CLOCK, CLOCK* Differential Input Voltage		± 400			mV
ECL Digital Outputs					
Output High Voltage	VOH	- 1025		- 880	mV
Output Low Voltage	VOL	- 1810		- 1620	mV
Output Capacitance	CDOUT		7		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Output					
Gray Scale Current Range		- 10		- 40	mA
Output Current*					
White Level		0	- 5	- 50	µA
Black Level Relative to White		- 25.08	- 26.40	- 27.72	mA
Blank Level Relative to Black					
SETUP = ECL VCC		0	0	0	mA
SETUP = float		- 2.05	- 2.16	- 2.28	mA
Blank Level Relative to White		- 27.13	- 28.56	- 30	mA
LSB Size			- 103.5		µA
Output Compliance	VOC	- 1.2		+ 1.5	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Reference Input Current	IREF IN			10	µA
Reference Output Voltage	VREF OUT	- 1.175	- 1.235	- 1.295	Volts
Reference Output Current	IREF OUT	- 200			µA
VREF OUT Tempco			± 75		ppm
VBB Output Voltage (load = 500 µA)	VBB	- 1260	- 1320	- 1380	mV
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 KHz)	PSRR		0.1		%/% ΔAVEE

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -28.56 mA full scale output current, VREF IN = -1.21v, SETUP = float. All ECL inputs have 50 ohms to -2.0v. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

*When using internal reference, RSET may need to be adjusted to meet these limits.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			360	MHz
CS* and Address Setup Time	1	10			ns
CS* and Address Hold Time	2	20			ns
RDx* Asserted to Data Bus Driven	3	10			ns
RDx* Asserted to Data Valid	4			30	ns
RDx* Negated to Data Bus 3-Stated	5			10	ns
WR* Pulse Width Low	6	75			ns
Write Data Setup Time	7	45			ns
Write Data Hold Time	8	10			ns
Pixel and Control Setup Time	9	0			ns
Pixel and Control Hold Time	10	1			ns
Clock Cycle Time	11	2.8			ns
Clock Pulse Width High	12	1			ns
Clock Pulse Width Low	13	1			ns
DIV2OUT Delay**	14	0.5		1.5	ns
DIV2IN Setup Time (to rising edge of CLOCK)	15	0.5			ns
DIV2IN Hold Time (to rising edge of CLOCK)	16	0.5			ns
Analog Output Delay	17		4		ns
Analog Output Rise/Fall Time				1	ns
Analog Output Settling Time	18		3	5	ns
Clock and Data Feedthrough*			tbd		dB
Glitch Impulse*			5		LSB - ns
Pipeline Delay		3	3	3	Clocks
DVEE + AVEE Supply Current	IEE			635	mA
TTL VCC Supply Current	ICC			65	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for -28.56 mA full scale output current, VREF IN = -1.21v, SETUP = float. ECL input values are -0.95 to -1.69 volts, with input rise/fall times ≤ 1 ns, measured between the 20% and 80% points. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. All ECL inputs have 50 ohms to -2.0v, unless other specified. Analog output load ≤ 10 pF. See timing notes in Figure 10.

*Settling time does not include clock and data feedthrough. -3 dB test bandwidth = 720 MHz.

**Tested with three ECL loads.

Timing Waveforms

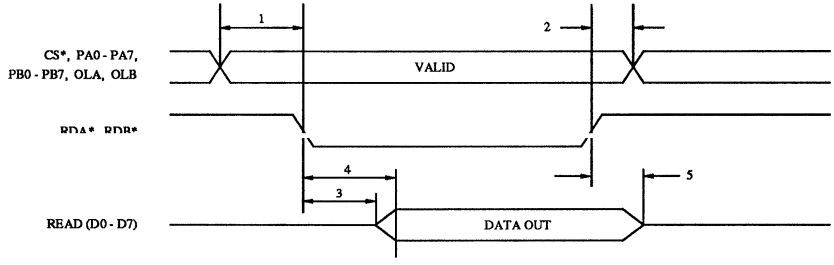


Figure 8. MPU Read Timing.

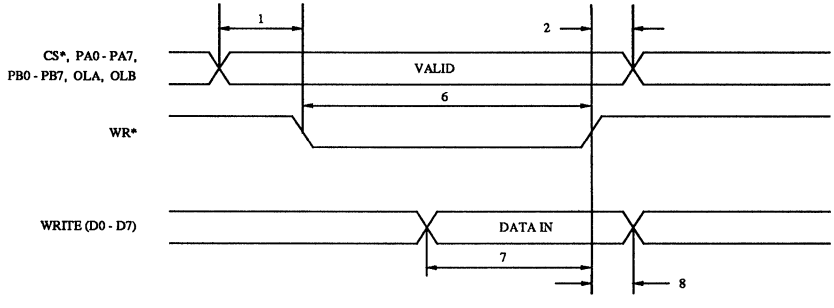
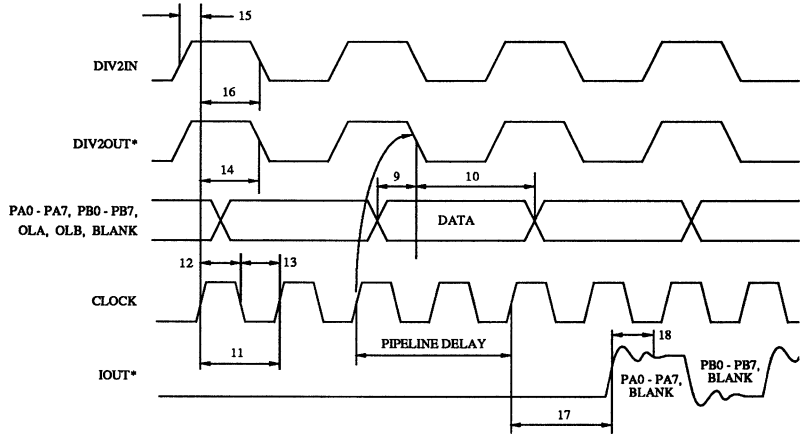


Figure 9. MPU Write Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt492KG360	360 MHz	68-pin Ceramic PGA with Alignment Pin and Heatsink	0° to +70° C.

Timing Waveforms (continued)



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1%.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 10. Video Input/Output Timing.

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Table of Contents

Bt424

250 MHz

40-bit Multi-Tap

TTL/ECL Compatible

Video Shift Register

Distinguishing Features

- 250 MHz Operation
- Overlay Support
- TTL Pixel Inputs
- TTL MPU Address Interface
- ECL Shift Register Outputs
- Shift Enable and Output Enable Controls
- Optional Single +5v Operation
- 68-pin PGA Package with Alignment Pin
- Typical Power Dissipation: 1.25 W

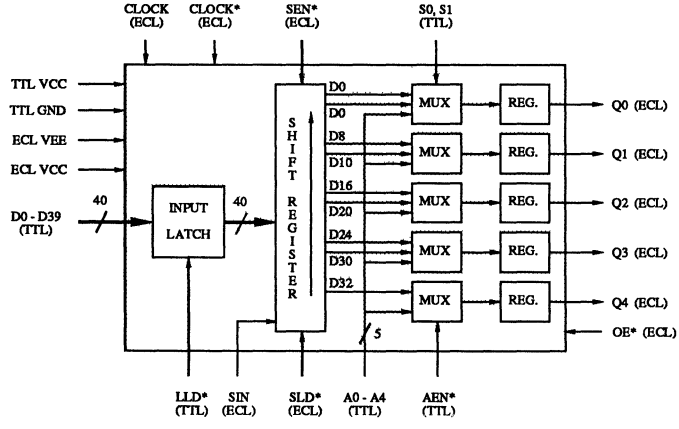
Customer Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading
- Increases System Reliability

Possible Configurations

- One 40-bit Shift Register
- Two 16-bit or 20-bit Shift Registers
- Five 8-bit Shift Registers
- Four 10-bit Shift Registers

Functional Block Diagram



Product Description

The Bt424 is a 40-bit multi-tap shift register. It is designed specifically for high-resolution graphics systems.

TTL pixel data from the frame buffer is typically loaded at either 1/8 or 1/10 the clock rate (up to about 32 MHz) using the TTL compatible LLD* signal. Data is then transferred from the input latch to the shift register using the ECL compatible load signal (SLD*). The double-buffering of incoming pixel data simplifies system timing.

The shift register is clocked by the ECL compatible CLOCK and CLOCK* inputs, and features ECL compatible serial input (SIN) and shift enable (SEN*) controls.

The Bt424 performs TTL to ECL translation of the MPU address (A0 - A4), eliminating external address translators. The MPU address interface enables the MPU address(A0 - A4) to be output onto the Q0 - Q4 pins, overriding the shift register data. This interface is controlled by the TTL compatible address enable (AEN*) signal.

The Bt424 has separate TTL and ECL supply pins, enabling operation from a single +5v supply, or a +5v and -5.2v supply.

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Circuit Description

As illustrated in the functional block diagram, the Bt424 contains a 40-bit input latch, a 40-bit shift register, and control logic.

General Shift Register Operation

The 40-bit shift register has multiple taps, as illustrated in the functional block diagram. As illustrated in Figure 3, on the rising edge of LLD*, D0 - D39 are latched into the input latch. Data is transferred from the input latch to the shift register synchronously on the rising edge of CLOCK while SLD* is a logical zero. Note that while LLD* is a logical zero, the input latch is transparent, as illustrated in Figure 4.

The multiplexers select one of two taps from the 40-bit shift register or a MPU address input. The output of the multiplexers are registered synchronously to CLOCK and output onto the Q0 - Q4 pins.

The SEN* input may be used to synchronously enable (logical zero) or disable (logical one) the shift register from clocking. This is useful for implementing hardware zooming in a graphics application. Figure 5 shows the shift timing and SEN* timing.

The OE* input is used to enable (logical zero) or disable (logical one) the outputs asynchronously to CLOCK, as shown in Figure 6.

Single 40-bit Shift Register Operation

When used as a 40-bit shift register, only the Q0 output is used, and the Q1 - Q4 outputs are ignored. D0 is the first bit output, followed by D1, etc. SLD* and LLD* should occur once every 40 clock cycles. The state of the S0 and S1 inputs are not important, and may be connected to TTL GND.

Note that single shift registers of any length (up to 40-bits) may be implemented by simply loading the parallel data at the appropriate time. For example, a 32-bit shift register may be implemented by loading parallel data once every 32 clock cycles.

Dual 20-bit Shift Register Operation

When used as a dual 20-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D20 is the first bit output, followed by D21, etc. SLD* and LLD* should occur once every 20 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Dual 16-bit Shift Register Operation

When used as a dual 16-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D16 is the first bit output, followed by D17, etc. SLD* and LLD* should occur once every 16 clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Quad 10-bit Shift Register Operation

When used as a quad 10-bit shift register, all output except Q4 are used (which is ignored). For Q0, D0 is the first bit output, followed by D1, etc. For Q1, D10 is the first bit output, followed by D11, etc. For Q2, D20 is the first bit output, followed by D21, etc. For Q3, D30 is the first bit output, followed by D31, etc. SLD* and LLD* should occur once every 10 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Quint 8-bit Shift Register Operation

When used as a quint 8-bit shift register, all outputs are used. For Q0, D0 is the first bit output, followed by D1, etc. For Q1, D8 is the first bit output, followed by D9, etc. For Q2, D16 is the first bit output, followed by D17, etc. For Q3, D24 is the first bit output, followed by D25, etc. For Q4, D32 is the first bit output, followed by D33, etc. SLD* and LLD* should occur once every 8 clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Circuit Description (continued)

MPU Address Interface

The Bt424 accepts TTL compatible MPU addresses(A0 - A4) and translates them to ECL compatible levels, eliminating the need for external TTL/ECL translators along the address path.

While AEN* is a logical one, pixel data from the shift register is output onto the Q0 - Q4 pins. While AEN* is a logical zero, A0 - A4 are output onto the Q0 - Q4 pins. Figure 7 illustrates the MPU address timing. Note that Q0 - Q4 are always output following the rising edge of CLOCK regardless of the value of AEN*.

S0, S1 Select Inputs

S0 and S1 specify the configuration of the Bt424 as follows:

S1	S0	Function
0	0	quad 10-bit
x	1	quint 8-bit
1	0	quad 8-bit, 8-bit overlay port

Table 1. S0, S1 Control Inputs.

Figure 1 shows using the Bt424 in a typical graphics system. In this instance, the RAMDAC has separate (nonmultiplexed) pixel and overlay data inputs. Therefore, all three Bt424s are configured for the same mode of operation (either quad 10-bit or quint 8-bit depending on the specific application).

Figure 2 shows a basic configuration using the Bt424 with a RAMDAC that has multiplexed pixel and overlay inputs. The OL input of the RAMDAC specifies whether pixel (OL = 0) or overlay (OL = 1) data is present on P0 - P7.

The Bt424s interfaced to bit planes 0 - 7 are configured to support overlays (S1 = 1, S0 = 0). D0 - D7, D8 - D15, D16 - D23, and D24 - D31 are configured as four 8-bit pixel input ports, while D32 - D39 are configured as an 8-bit overlay active input port. If D32 - D39 contain a logical one on any bit, the Q0 - Q3 outputs are disabled and forced to a logical zero, enabling overlay information to be wire-ORed onto the Q0 - Q3 outputs.

The Bt424 interfaced to the overlay bit planes is configured as a quint 8-bit shifter, and serializes the overlay information. The Q0 - Q3 outputs are wire-ORed onto the pixel data bus to the RAMDAC. The D32 - D39 inputs are serialized to generate the overlay enable (OL) control signal for the RAMDAC. Note that if no overlay information is being displayed, the Q0 - Q4 outputs are a logical zero, allowing normal pixel data to be displayed.

Eight 4-input TTL OR gates are required to generate the overlay active signals to the Bt424s. D0, D8, D16, and D24 are ORed together to generate D32, etc.

Power Supply Operation

The Bt424 may operate from a +5v and -5.2v power supply or from a single +5v power supply, as illustrated below:

	Nominal Voltages Applied	
Supply Pin	Single Supply System	Dual Supply System
TTL VCC	+ 5.0v	+ 5.0v
TTL GND	0v	0v
ECL VCC	+ 5.0v	0v
ECL VEE	0v	- 5.2v

Table 2. Power Supply Operation.

Inputs and outputs are temperature and voltage compensated.

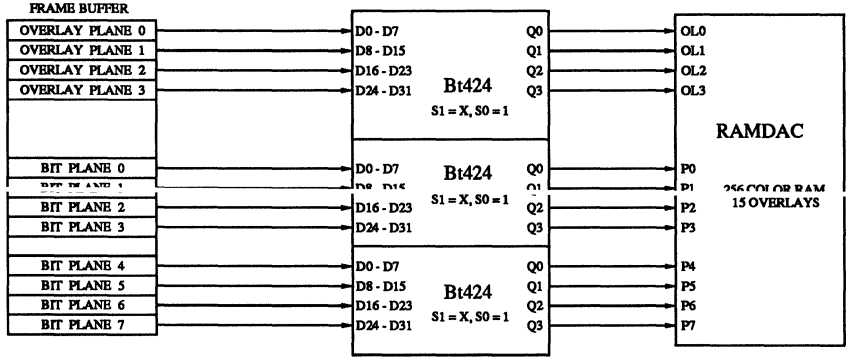


Figure 1. Using the Bt424 with Separate Pixel and Overlay Inputs. (256 Colors, 15 Overlays)

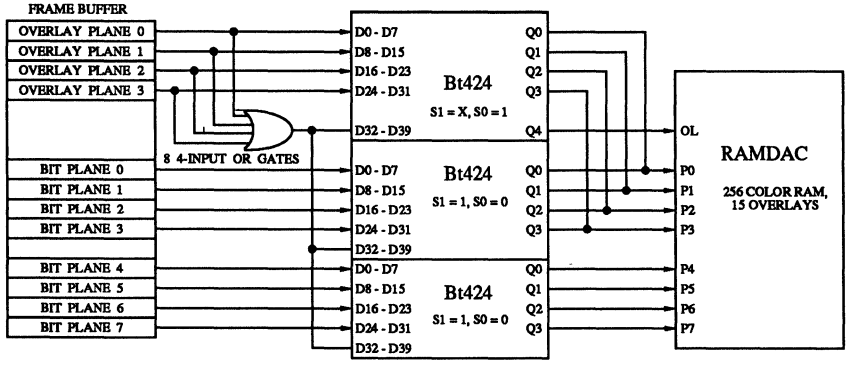


Figure 2. Using the Bt424 with Multiplexed Pixel/Overlay Inputs. (256 Colors, 15 Overlays)

Pin Descriptions

Pin Name	Description
D0 - D39	Parallel data inputs (TTL compatible). These inputs are latched into the input latch on the rising edge of LLD*, asynchronous to CLOCK.
SIN	Shift data input (ECL compatible). This input is latched on the rising edge of CLOCK, and may be used to serially load the shift register. If not used, it should be connected to ECL GND.
SEN*	Shift enable control input (ECL compatible). This input may be used to synchronously start or stop the shift register from clocking. A logical zero enables shifting, a logical one disables shifting.
LLD*	Input latch load control input (TTL compatible). The rising edge of LLD* is used to latch D0 - D39 into the input latch. While LLD* is a logical zero, the input latch is transparent.
SLD*	Shift register load control input (ECL compatible). SLD* is used to transfer data from the input latch to the shift register synchronously to CLOCK. Data is transferred on the rising edge of CLOCK while SLD* is a logical zero.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The clock rate is typically the pixel clock rate of the video system. The Bt424 may be used with a single ended clock by connecting CLOCK* to VBB (-1.3v)
Q0 - Q4	Shift register outputs (ECL compatible). These pins output either D0 - D39 data (AEN* = logical one) or A0 - A4 data (AEN* = logical zero). Data is output following the rising edge of CLOCK.
OE*	Output enable control input (ECL compatible). A logical one forces the Q0 - Q4 outputs to a logical zero, while a logical zero enables data to be output onto Q0 - Q4. The Q0 - Q4 outputs are enabled and disabled asynchronously to CLOCK.
S0, S1	Select control inputs (TTL compatible). These inputs control the operation of the device as specified in Table 1.
A0 - A4	Address inputs (TTL compatible). These are typically address inputs from the MPU, used to address the color palette RAM during MPU read/write cycles to the color palette RAM.
AEN*	Address enable control input (TTL compatible). While AEN* is a logical zero, A0 - A4 are output onto Q0 - Q4 following the rising edge of CLOCK. If AEN* is a logical one, A0 - A4 are ignored.
TTL VCC	Power supply pins for the TTL compatible circuitry.
TTL GND	Ground pins for the TTL compatible circuitry.
ECL VEE	Power supply pins for the ECL compatible circuitry.
ECL VCC	Ground pins for the ECL compatible circuitry.

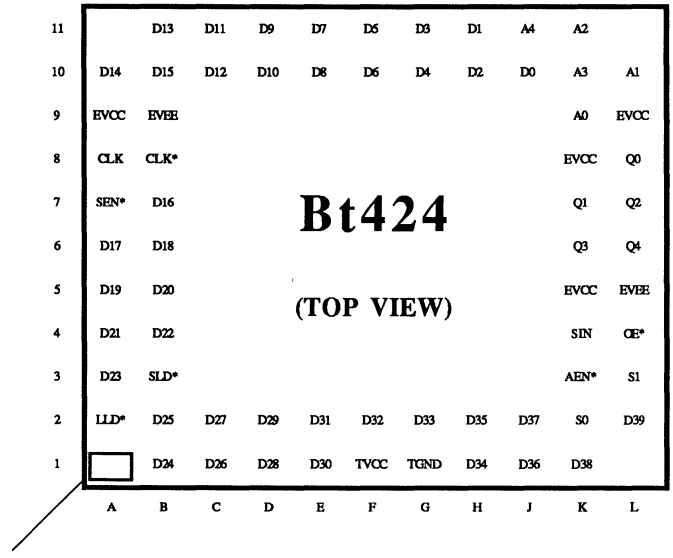
Pin Descriptions (continued)

Signal	Pin Number
CLOCK	A8
CLOCK*	B8
LLD*	A2
SLD*	B3
SEN*	A7
SIN	K4
S0	K2
S1	L3
AEN*	K3
A0	K9
A1	L10
A2	K11
A3	K10
A4	J11
Q0	L8
Q1	K7
Q2	L7
Q3	K6
Q4	L6
OE*	L4

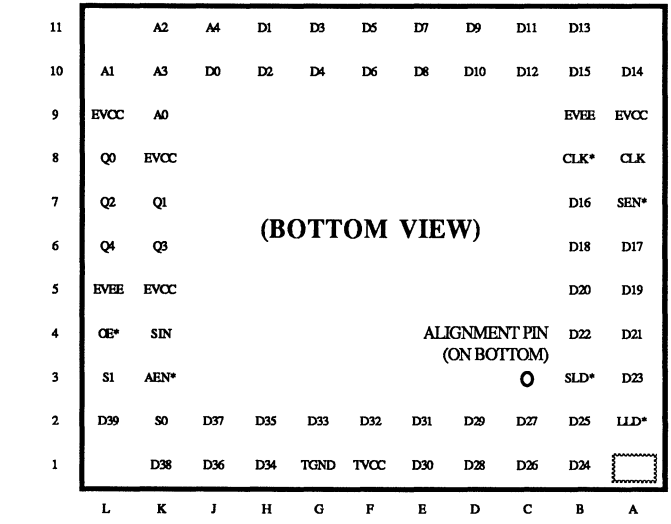
Signal	Pin Number
D0	J10
D1	H11
D2	H10
D3	G11
D4	G10
D5	F11
D6	F10
D7	E11
D8	E10
D9	D11
D10	D10
D11	C11
D12	C10
D13	B11
D14	A10
D15	B10
D16	B7
D17	A6
D18	B6
D19	A5
D20	B5
D21	A4
D22	B4
D23	A3
D24	B1

Signal	Pin Number
D25	B2
D26	C1
D27	C2
D28	D1
D29	D2
D30	E1
D31	E2
D32	F2
D33	G2
D34	H1
D35	H2
D36	J1
D37	J2
D38	K1
D39	L2
TTL VCC	F1
TTL GND	G1
ECL VEE	B9
ECL VEE	L5
ECL VCC	A9
ECL VCC	K5
ECL VCC	K8
ECL VCC	L9

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L
11		D13	D11	D9	D7	D5	D3	D1	A4	A2	
10	D14	D15	D12	D10	D8	D6	D4	D2	D0	A3	A1
9	EVCC	EVEE								A0	EVCC
8	CLK	CLK*								EVCC	Q0
7	SEN*	D16								Q1	Q2
6	D17	D18								Q3	Q4
5	D19	D20								EVCC	EVEE
4	D21	D22								SIN	OE*
3	D23	SLD*								AEN*	S1
2	LLD*	D25	D27	D29	D31	D32	D33	D35	D37	S0	D39
1		D24	D26	D28	D30	TVCC	TGND	D34	D36	D38	



	L	K	J	H	G	F	E	D	C	B	A
11		A2	A4	D1	D3	D5	D7	D9	D11	D13	
10	A1	A3	D0	D2	D4	D6	D8	D10	D12	D15	D14
9	EVCC	A0								EVEE	EVCC
8	Q0	EVCC								CLK*	CLK
7	Q2	Q1								D16	SEN*
6	Q4	Q3								D18	D17
5	EVEE	EVCC								D20	D19
4	OE*	SIN								D22	D21
3	S1	AEN*								SLD*	D23
2	D39	S0	D37	D35	D33	D32	D31	D29	D27	D25	LLD*
1		D38	D36	D34	TGND	TVCC	D30	D28	D26	D24	

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	Volts
ECL Device Ground	ECL VCC	0	0	0	Volts
TTL Power Supply	TTL VCC	+ 4.75	+ 5.0	+ 5.25	Volts
ECL Power Supply	ECL VEE	- 4.9	- 5.2	- 5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				- 8.0	Volts
TTL VCC (measured to TTL GND)				+ 7.0	Volts
Voltage on any ECL Pin		0		ECL VEE	Volts
Voltage on any TTL Pin		TTL GND - 0.5		TTL VCC + 0.5	Volts
Q0 - Q4 Output Current				- 30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	- 1165		- 880	mV
Input Low Voltage*	VIL	- 1810		- 1475	mV
Output High Voltage*	VOH	- 1025		- 880	mV
Output Low Voltage*	VOL	- 1810		- 1620	mV
Input High Current (Vin = VIHmax)	IIH			500	µA
Control (SLD, SIN, SEN)				500	µA
Clock (Clock, Clock*)				50	µA
Input Low Current (Vin = VILmin)	IIL			400	µA
Control (SLD, SIN, SEN)				400	µA
Clock (Clock, Clock*)				15	µA
ECL VEE Supply Current	IEE			240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0 - Q4 loading of 50 ohms to -2.0v.

*Relative to ECL VCC.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

TTL D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC + 0.5	Volts
Input Low Voltage*	VIL	TTL GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			70	µA
Input Low Current (Vin = 0.4v)	IIL			- 0.7	mA
TTL VCC Supply Current	ICC			75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0 - Q4 loading of 50 ohms to -2.0v.

*Relative to TTL GND.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Clock Cycle Time	1	4			ns
Clock Pulse Width High Time	2	1.5			ns
Clock Pulse Width Low Time	3	1.5			ns
LLD* Pulse Width Low Time	4	7			ns
LLD* Setup Time	5	8			ns
SLD Setup Time	6	2			ns
SLD Hold Time	7	0			ns
D0 - D39 Setup Time to LLD*	8	10			ns
D0 - D39 Setup Time to Clock	9	15			ns
D0 - D39 Hold Time to LLD*	10	0			ns
D0 - D39 Hold Time to Clock	11	0			ns
Q0 - Q4 Output Delay	12	1.5		4	ns
SEN* Setup Time	13	2			ns
SEN* Hold Time	14	0			ns
SIN Setup Time	15	1.5			ns
SIN Hold Time	16	0.5			ns
OE* Pulse Width Low Time	17	4			ns
OE* Enable Time	18			3.5	ns
OE* Disable Time	19			4	ns
A0 - A4 Setup Time	20	12			ns
A0 - A4 Hold Time	21	0			ns
AEN* Setup Time	22	5			ns
AEN* Hold Time	23	0			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0 - Q4 loading of 50 ohms to -2.0v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are -0.89 to -1.69 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt424KG	68-pin Ceramic PGA with Alignment Pin	0° to +70° C.

Timing Waveforms

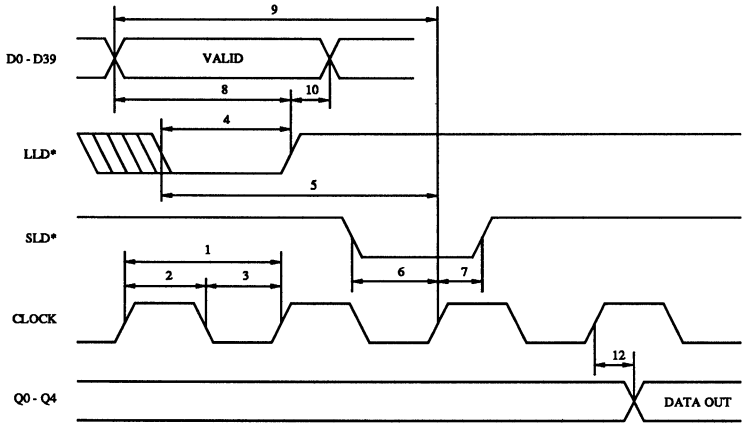


Figure 3. Load Latch and Register Timing.

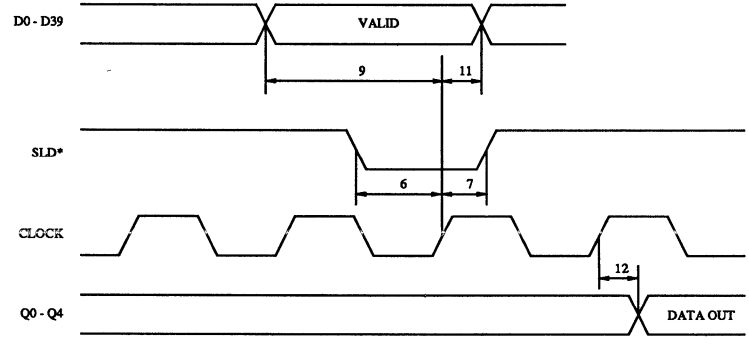


Figure 4. Transparent Latch Timing (LLD = Logical Zero).*

Timing Waveforms (continued)

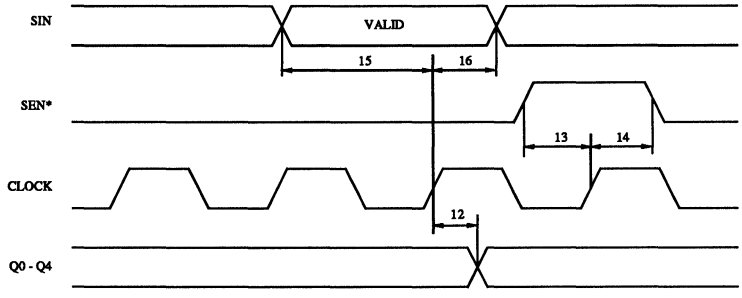


Figure 5. Shift Timing (SLD = Logical One).*

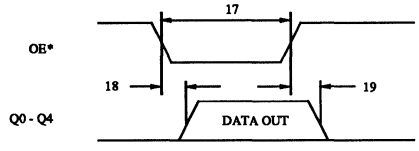


Figure 6. Output Enable Timing.

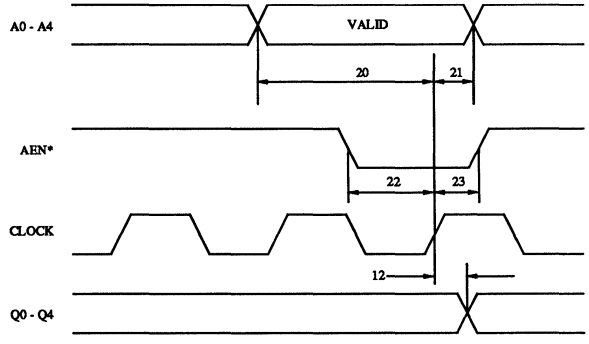


Figure 7. Address Enable Timing.

Bt431

Monolithic CMOS

64 x 64 Pixel

Cursor Generator

Distinguishing Features

- 64 x 64 Pixel User Definable Cursor
- Full Screen/Window Cross Hair Cursor
- Pixel Positioning of Cursors
- Supports Pixel Rates up to 175 MHz
- 1:1, 4:1, and 5:1 Output Multiplexing
- TTL Compatible Inputs/Outputs
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 450 mW

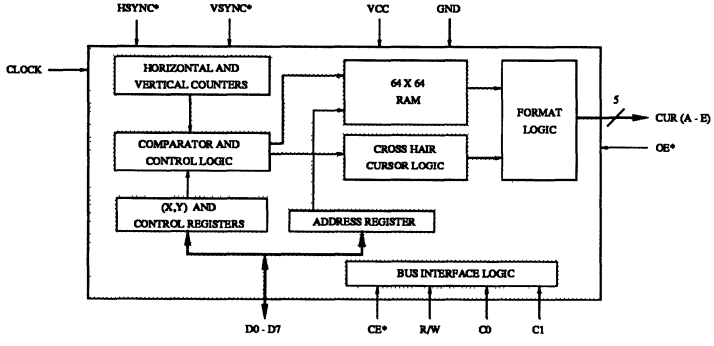
Applications

- High Resolution Color Graphics
- Image Processing

Customer Benefits

- Reduces Component Count
- Reduces PCB Area Requirements
- Simplifies Cursor Implementation
- Allows Fast Cursor Movement
- Simplifies Software Interface

Functional Block Diagram



Product Description

The Bt431 cursor generator provides a 64 x 64 pixel user-definable cursor and a cross hair cursor for high resolution, noninterlaced, monochrome or color graphics systems. The cross hair cursor may be implemented as a full screen or full window cross hair cursor. Both cursors may be displayed simultaneously, with logical OR and exclusive-OR operations supported. Either cursor may be moved off the top, bottom, left, or right side of the display without wrap-around.

The cursors may be positioned with pixel resolution, and may be individually enabled or disabled from being displayed. A standard MPU bus interface is supported, simplifying system design.

The Bt431 may be programmed to output cursor information for one, four, or five horizontally consecutive pixels, enabling it to be interfaced to either the multiplexed or nonmultiplexed overlay inputs of Brooktree RAMDACs.

An external shift register may be used with the Bt431 to support pixel rates up to 175 MHz.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt431 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and cursor RAM.

The MPU interface signals consist of D0 - D7, CE*, R/W, C0, and C1. Table 1 illustrates the truth table for the control inputs, and Figure 1 illustrates the MPU read/write timing of the device.

Two 8-bit address registers (address register0 and address register1), cascaded to form a 16-bit address pointer register, are used to address the internal control registers and cursor RAM, as illustrated in Table 2. During read/write cycles to the cursor RAM, the 9 least significant bits of the address pointer register (ADDR0 - ADDR8) are incremented following each read or write cycle to the cursor RAM. Thus, the MPU may load the address pointer register with the desired starting cursor RAM address, and burst load new cursor RAM data by writing up to 512 bytes of data to the device. Following a read or write cycle to RAM location $01FF, the address pointer register resets to $0000.

During accesses to the control registers, ADDR0 - ADDR8 are incremented after any read or write cycle to a register. While accessing the control registers, the address pointer register will reset to $0000 only following a write cycle to location $01FF. The address register is not incremented when read or written to.

RAMDAC Interface

The Bt431 is designed to generate cursor information using the overlay input ports of Brooktree RAMDACs.

The Bt431 may be interfaced directly to RAMDACs with 4:1 or 5:1 multiplexed overlay ports, supporting display resolutions up to 1280 x 1024 pixels. In this instance, the CUR (A - E) outputs of the Bt431 would connect directly to the overlay inputs of the RAMDAC, and the CLOCK input of the Bt431 would typically be connected directly to the LD* or LDOUT pin of the RAMDAC. The Bt431 must be programmed to output either four or five horizontally consecutive pixels of cursor information each CLOCK cycle. This enables the Bt431 to output cursor information at an effective 125 MHz rate.

To support RAMDACs with nonmultiplexed overlay inputs, the Bt431 may be programmed to output a single pixel of cursor information each CLOCK cycle. In this configuration, the CURA output of the Bt431 would connect directly to the one of the overlay inputs of the RAMDAC. This configuration limits the cursor information to an effective 35 MHz rate. The CLOCK input of the Bt431 is typically connected directly to the CLOCK input of the RAMDAC.

The Bt431 may be configured for 4:1 or 5:1 output multiplexing, and an external shift register used (with appropriate control logic) to interface to RAMDACs whose input pixel rate is greater than 35 MHz. In this configuration, the CLOCK must be driven at 1/4 or 1/5 the pixel clock rate. Pixel rates up to 175 MHz may be supported using this technique.

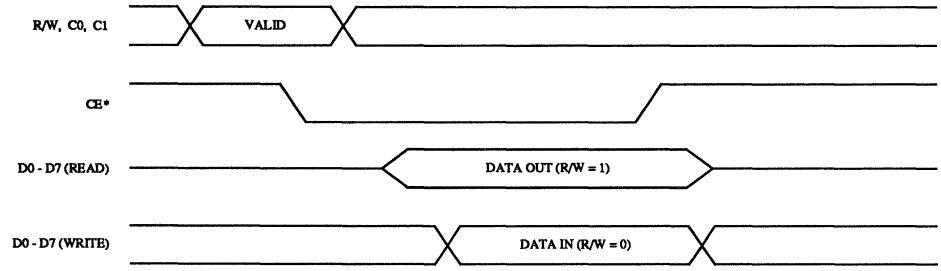


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

R/W	C1	C0	
0	0	0	write address register0
0	0	1	write address register1
0	1	0	write to RAM location specified by address pointer register
0	1	1	write to control register specified by address pointer register
1	0	0	read address register0
1	0	1	read address register1
1	1	0	read RAM location specified by address pointer register
1	1	1	read control register specified by address pointer register

Table 1. MPU Control Truth Table.

	Address Pointer Register (ADDR15 - ADDR0)		
C0	Address Register1 (D7 - D0)	Address Register0 (D7 - D0)	Register/RAM location addressed
0	0000 0000	0000 0000	cursor RAM location $000
0	0000 0000	0000 0001	cursor RAM location $001
:	:	:	:
0	0000 0000	1111 1111	cursor RAM location $0FF
0	0000 0001	0000 0001	cursor RAM location $100
0	0000 0001	0000 0001	cursor RAM location $101
:	:	:	:
0	0000 0001	1111 1111	cursor RAM location $1FF
1	xxxx xxxx	xxxx 0000	command register
1	xxxx xxxx	xxxx 0001	cursor (x) low register
1	xxxx xxxx	xxxx 0010	cursor (x) high register
1	xxxx xxxx	xxxx 0011	cursor (y) low register
1	xxxx xxxx	xxxx 0100	cursor (y) high register
1	xxxx xxxx	xxxx 0101	window (x) low register
1	xxxx xxxx	xxxx 0110	window (x) high register
1	xxxx xxxx	xxxx 0111	window (y) low register
1	xxxx xxxx	xxxx 1000	window (y) high register
1	xxxx xxxx	xxxx 1001	window width low register
1	xxxx xxxx	xxxx 1010	window width high register
1	xxxx xxxx	xxxx 1011	window height low register
1	xxxx xxxx	xxxx 1100	window height high register

Table 2. Address Pointer Register.

Circuit Description (continued)

64 x 64 Cursor Positioning

When the cursor RAM is being displayed, the contents of the cursor RAM are output onto the CUR (A - E) outputs. A logical one in the cursor RAM results in a logical one being output onto the appropriate CUR (A - E) output during the appropriate clock cycle. The cursor pattern may be changed by changing the contents of the cursor RAM.

The 64 x 64 cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 RAM (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 RAM (assuming the rows start with 0 for the top-most pixel and increment to 63).

Note that the Bt431 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen.

The cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and external pixel data, and whether 1:1, 4:1, or 5:1 output multiplexing is being done.

The cursor (y) position is relative to the first falling edge of HSYNC* that is at two or more clock cycles after the falling edge of VSYNC*.

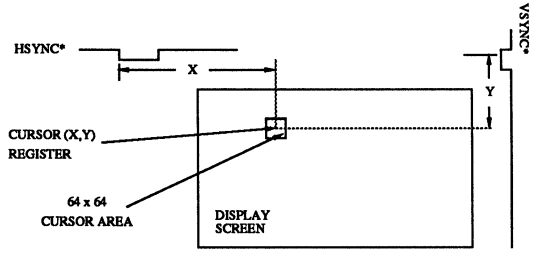


Figure 2. 64 x 64 Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor Positioning

Cursor positioning for the cross hair cursor is also done through the cursor (x,y) register.

The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, a logical one is output onto the appropriate CUR (A - E) output during the appropriate clock cycle.

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and the external pixel data, and whether 1:1, 4:1, or 5:1 output multiplexing is being done.

The cursor (y) position is relative to the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC*.

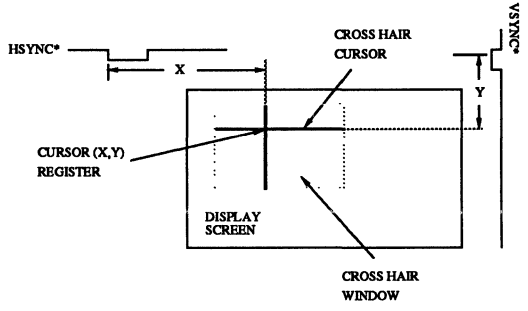


Figure 3. Cross Hair Cursor Positioning

Circuit Description (continued)

Dual Cursor Positioning

Both the 64 x 64 cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

During the 64 x 64 pixel area in which the user-definable cursor would be displayed, the contents of the cursor RAM may be logically ORed or exclusive-ORed with the cross hair cursor information.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31,31) of the cursor RAM. As the user-definable cursor contains an even number of pixel in the horizontal and vertical direction, there will be a one pixel offset from being truly centered about the cross hair cursor.

Figure 4 illustrates displaying the dual cursors, and Figure 5 illustrates the video input/output timing of the Bt431.

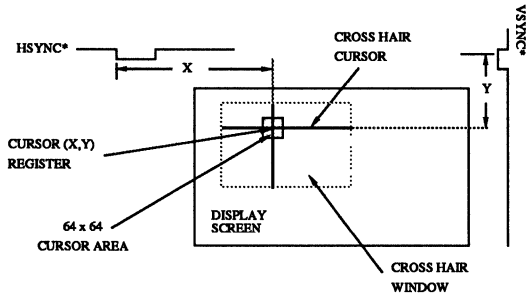


Figure 4. Dual Cursor Positioning.

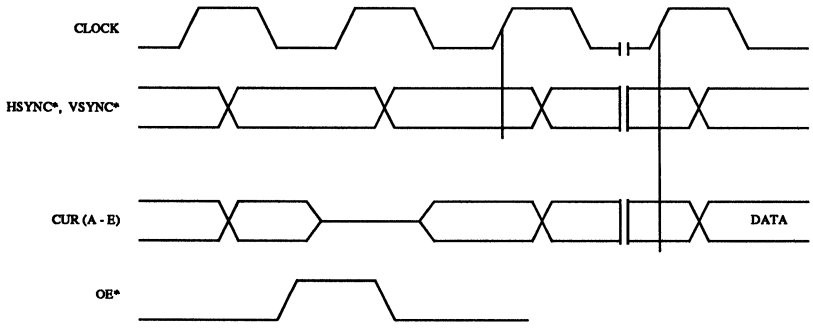


Figure 5. Video Input/Output Timing.

Internal Registers

Cursor (x,y) Register

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4 - D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + D + H - P

where

P = 37 if 1:1 output multiplexing, 52 if 4:1 output multiplexing, 57 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video.

The P value is 1/2 cursor RAM width + (internal pipeline delay in clock cycles * 1, 4, or 5 depending on multiplex selection)

Values from $0000 to $0FFF may be written into the cursor (x) register.

Internal Registers (continued)

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V - 32

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0FC0 (-64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

The cursor (x,y) registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary "tearing" of the cursor may occur.

Internal Registers (continued)

Cursor RAM

This 64 x 64 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window. It is not initialized, and may be written to or read by the MPU at any time. As MPU accesses to the cursor RAM have priority over the cursor display process, the cursor RAM should not be accessed during the horizontal sync intervals to minimize contention of the cursor updating and displaying processes.

During MPU accesses to the cursor RAM, the address pointer register is used to address the cursor RAM, as illustrated below. Figure 6 illustrates the internal format of the cursor RAM, as it appears on the display screen.

Address Pointer Register Value	Address RAM Location
$0000	byte $000
$0001	byte $001
:	:
$01FF	byte $1FF

As shown below, bit D7 is the left-most pixel within a segment of eight pixels. This enables the software generation of cursor patterns without bit swapping to obtain the desired pattern.

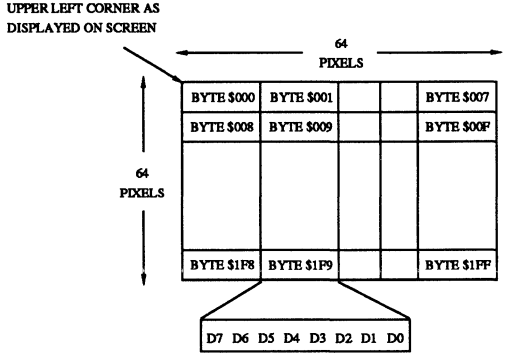


Figure 6. Cursor RAM as Displayed on the Screen.

Internal Registers (continued)

Window (x,y) Register

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register(WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4 - D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + D + H - P

where

P = 5 if 1:1 output multiplexing, 20 if 4:1 output multiplexing, 25 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video.

The P value is the number of internal pipeline delays times 1, 4, or 5 depending on the multiplex selection.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

The window (x,y) registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary repositioning of the cross hair cursor may occur.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4 - D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 output multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels, for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is two pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

The window width and height registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte and the last (fourth) byte of information. Otherwise, temporary "resizing" of the cross hair cursor may occur.

Internal Registers (continued)

Command Register

The command register is used to control various functions of the Bt431. It is not initialized, and may be written to or read by the MPU at any time.

D7 — Reserved. This bit should always be a logical zero.

D6 — 64 x 64 cursor enable. A logical one enables the contents of the cursor RAM to be output during times that user-definable cursor information is to be displayed. A logical zero disables the cursor RAM information from being output.

D5 — Cross hair cursor enable. A logical one enables cross hair cursor information to be output. A logical zero disables the cross hair cursor information from being output.

D4 — Cursor format control. If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.

D3, D2 — Multiplex control. These two bits specify whether one, four, or five bits of cursor information are output every clock cycle, as follows:

(00) 1:1 multiplexing
(01) 4:1 multiplexing
(10) 5:1 multiplexing
(11) reserved

D1, D0 — Cross hair cursor thickness. These two bits specify whether the horizontal and vertical thickness of the cross hair is one, three, five, or seven pixels, as follows:

(00) 1 pixel
(01) 3 pixels
(10) 5 pixels
(11) 7 pixels

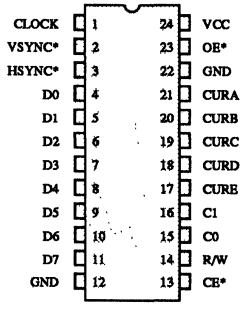
The horizontal and vertical segments are centered about the value in the cursor (x,y) register.

Pin Descriptions

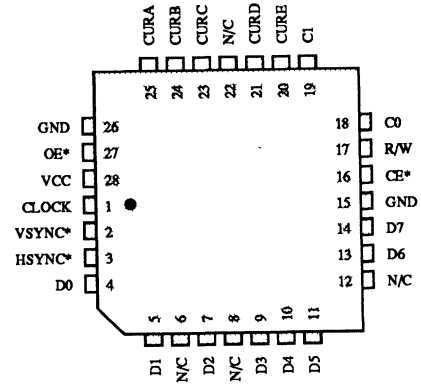
Pin Name	Description
VSYNC*	Vertical sync control input (TTL compatible). A logical zero indicates that the display is currently in the vertical sync interval. It is latched on the rising edge of CLOCK.
HSYNC*	Horizontal sync control input (TTL compatible). A logical zero indicates that the display is currently in the horizontal sync interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK is used to latch the VSYNC* and HSYNC* inputs, and to output cursor information onto the CUR (A - E) outputs. It is recommended that the CLOCK input be driven by a dedicated TTL buffer. If programmed for 1:1 output multiplexing, CLOCK should be the pixel clock rate. When programmed for 4:1 or 5:1 output multiplexing, CLOCK should be 1/4 or 1/5 the pixel clock rate, respectively.
CUR (A - E)	Cursor outputs (TTL compatible). During the pixel times that cursor information is to be displayed, either cross hair cursor information or the contents of the cursor RAM are output onto these pins. If programmed for 4:1 output multiplexing, the CURE output will always be a logical zero. If programmed for 1:1 output multiplexing, the CURB, CURC, CURD, and CURE outputs will always be a logical zero. When programmed for 4:1 or 5:1 multiplexing, CURA corresponds to the left-most pixel, followed by CURB, etc., repeating every four or five pixels.
OE*	Output enable control input (TTL compatible). A logical one asynchronously three-states the CUR (A - E) outputs, and a logical zero asynchronously enables cursor data to be output on the cursor outputs.
R/W	Read/write control input (TTL compatible). A logical zero indicates that the MPU is writing data to the device and a logical one indicates that the MPU is reading data from the device. See Figure 1.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. See Figure 1.
C0, C1	Control inputs (TTL compatible). These inputs specify the operation the MPU is performing. See Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
VCC	Power.
GND	Ground.

Pin Descriptions (continued)

24-pin DIP Package



28-pin Plastic J-Lead
(PLCC) Package



June 1989
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Note: N/C pins may be left floating without affecting the performance of the Bt431.

Application Information

Power-up Initialization

Following a power-up sequence, the Bt431 must be initialized. The following sequence is recommended:

1. Write $0000 to address pointer register
2. Do 13 write cycles to control registers
3. Write $0000 to address pointer register
4. Do 512 write cycles to the cursor RAM

Prior to the above sequence, the MPU may perform diagnostic checks on the device, such as checking that the RAM and control registers may be written to and read back.

Loading the cursor RAM

When changing the cursor pattern, it is recommended that the following sequence be used to load the cursor RAM:

1. Write $0000 to address pointer register
2. Do 512 write cycles to the cursor RAM

Moving the Cursor:

It is recommended that the following sequence be used to update the cursor (x,y) register:

1. Write $0001 to address pointer register
2. Read cursor (x) low
3. Read cursor (x) high
4. Read cursor (y) low
5. Read cursor (y) high
6. Calculate new (x,y) value
7. Write $0001 to address pointer register
8. Write new cursor (x) low
9. Write new cursor (x) high
10. Write new cursor (y) low
11. Write new cursor (y) high

The above sequence also applies to updating the window (x,y) register, except $0005 should be written to the address pointer register.

Changing the Window Size

To change the size of the cross hair window, it is recommended that the following sequence be used:

1. Write $0009 to address pointer register
2. Read window width low
3. Read window width high
4. Read window height low
5. Read window height high
6. Calculate new window width/height
7. Write $0009 to address pointer register
8. Write new window width low
9. Write new window width high
10. Write new window height low
11. Write new window height high

Using Multiple Devices

Multiple Bt431's may be used to generate more than one cursor, or to generate a multi-color cursor.

If using multiple devices to generate more than one cursor, the cursor outputs may be logically gated together, or each Bt431 may interface to a separate overlay input of the RAMDAC. If separate overlay inputs are used, the cursors will be automatically prioritized depending on which overlay is used for each cursor.

To generate a multi-color cursor (for example, using two Bt431s to generate a three color cursor), each Bt431 must interface to a separate overlay input of the RAMDAC. Either a separate cursor (x,y) calculation for each Bt431 may be performed, or the same cursor (x,y) calculation used with the cursor information appropriately offset in the cursor RAM.

Interfacing to the Bt453 and Bt458

Figure 7 illustrates interfacing a single Bt431 to the Bt453 RAMDAC and Figure 8 illustrates interfacing to the Bt458 RAMDAC.

Interfacing to the Bt451, Bt454, Bt457, and Bt461 RAMDACs are similar to interfacing to the Bt458, due to the multiplexed overlay inputs of these devices. When interfacing to the Bt454, the CLOCK pin of the Bt431 should be connected to the LDOUT pin of the Bt454, and the Bt431 configured for 4:1 output multiplexing. Interfacing to the Bt450, Bt473, and Bt471/476/478 RAMDACs is similar to interfacing to the Bt453.

Application Information (continued)

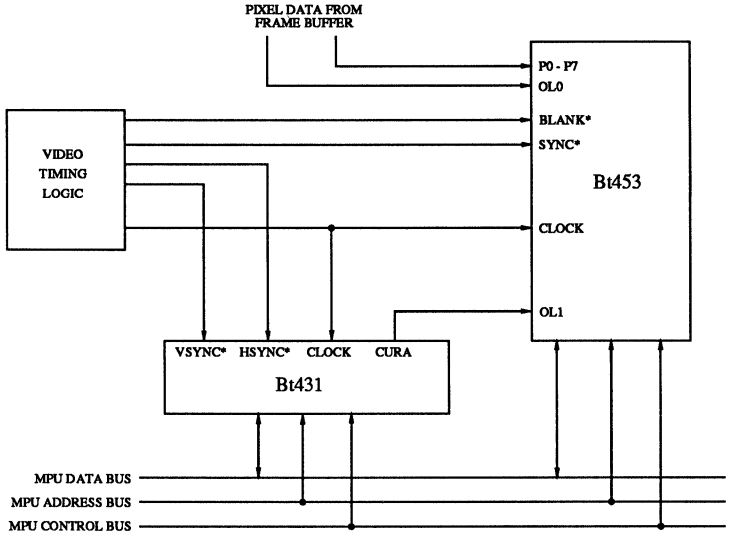


Figure 7. Interfacing to the Bt453.

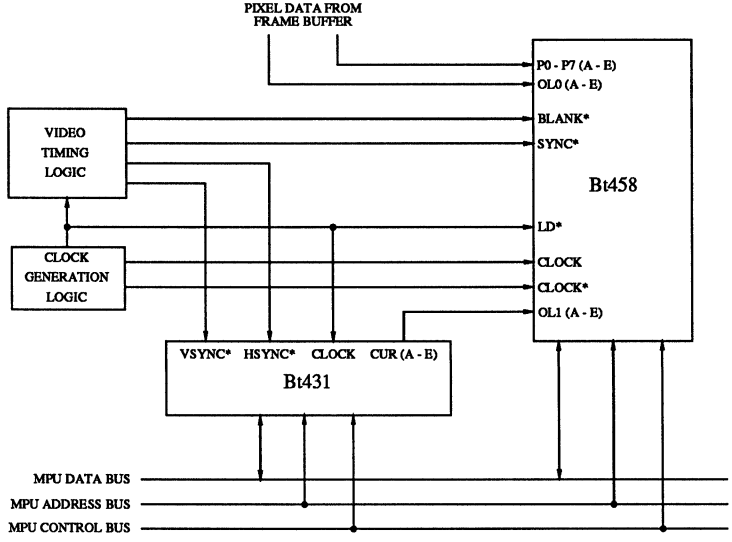


Figure 8. Interfacing to the Bt458.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND - 0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance	CIN				pF
(f = 1 MHz, Vin = 2.4v)			7		
Digital Outputs (D0 - D7)					
Output High Voltage	VOH	2.4			Volts
(IOH = -400 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 3.2 mA)					
3-state Current	IOZ			50	µA
Output Capacitance	COUT		20		pF
Digital Outputs (CURA - CURE)					
Output High Voltage	VOH	2.4			Volts
(IOH = -400 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 1.6 mA)					
3-state Current	IOZ			100	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate (per 1, 4, or 5 Pixels)	Fmax			35	MHz
C0, C1, R/W Setup Time	1	10			ns
C0, C1, R/W Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	10			ns
CE* Asserted to Data Valid	6			100	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	4	2.5		ns
VSYNC*, HSYNC* Setup Time	10	10			ns
VSYNC*, HSYNC* Hold Time	11	5			ns
VSYNC*, HSYNC* Low Time		4			Clocks
VSYNC*, HSYNC* High Time		4			Clocks
Clock Cycle Time	12	28.6			ns
Clock Pulse Width High	13	10			ns
Clock Pulse Width Low	14	10			ns
Pipeline Delay	15			5	Clocks
Output Delay	16			20	ns
Three-State Disable Time	17			15	ns
Three-State Enable Time	18			15	ns
VCC Supply Current*	ICC			100	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CURA - CURE output load ≤ 10 pF, D0 - D7 output load ≤ 130 pF.

*At Fmax. ICC (typ) at VAA = 5.0v. ICC (max) at VAA = 5.25v.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt431KC	24-pin 0.3" CERDIP	0° to +70° C.
Bt431KPJ	28-pin Plastic J-Lead	0° to +70° C.

Timing Waveforms

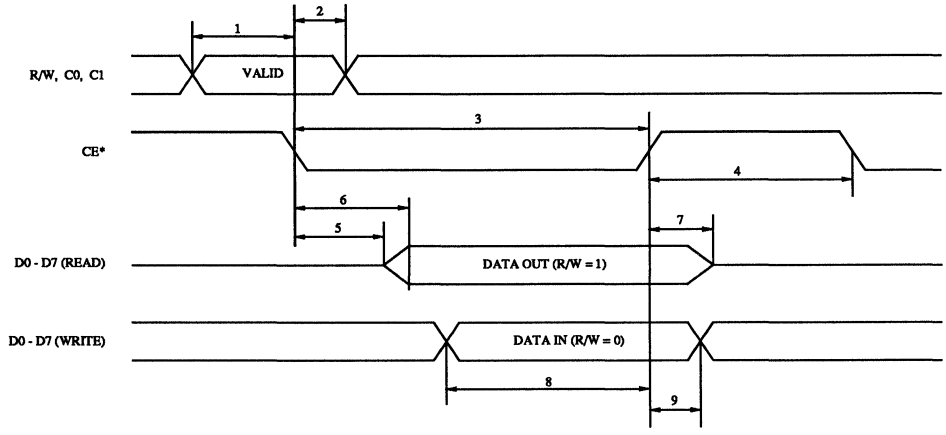


Figure 9. MPU Read/Write Timing.

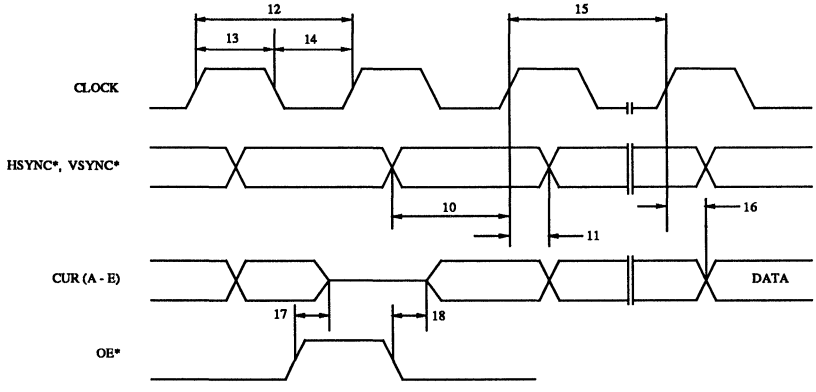


Figure 10. Video Input/Output Timing.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt438

250 MHz
Clock Generator Chip
for CMOS RAMDACs™

Distinguishing Features

- 250 MHz Operation
- Differential ECL Clock Generation
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- 1.2v Voltage Reference Output
- Single +5v Power Supply
- 20-pin DIP or 28-pin PLCC Package
- Typical Power Dissipation: 325 mW

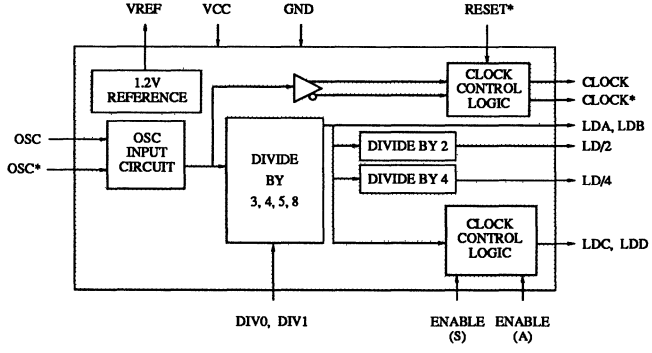
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability

Related Products

- Bt451, Bt457, Bt458, Bt459
- Bt461, Bt468

Functional Block Diagram



Product Description

The Bt438 is a clock generator for the high speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5v supply to the RAMDAC, generating the necessary clock and control signals.

The clock output may be divided by 3, 4, 5, or 8 to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438 also optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2v voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

6

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L438001 Rev. G

Brooktree®

Circuit Description

The Bt438 is designed to interface to a 10KH ECL crystal oscillator and generate the clock signals required by the RAMDACs. The OSC and OSC* inputs are designed to interface to a 10KH ECL oscillator operating from a single +5v power supply.

The CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5v power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LDA and LDB signals. LDA is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero.

Note that both ENABLE (A) and ENABLE (S) should not be a logical zero simultaneously. If this occurs, synchronous control of LDC and LDD, via ENABLE (S), is not guaranteed.

While both ENABLE (S) and ENABLE (A) are a logical one, LDC and LDD will be free-running and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally non-clocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt438, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt438 to set the pipeline delay of the RAMDACs to a specified number of clock cycles (the exact number is dependent on the RAMDAC). Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt438 also generates a 1.2v (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

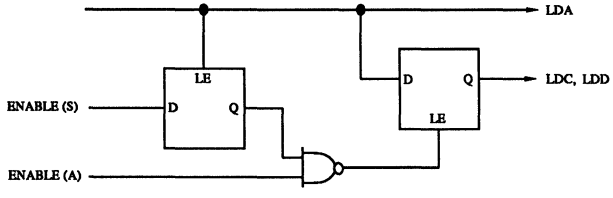


Figure 1. ENABLE Control Implementation.

Circuit Description (continued)

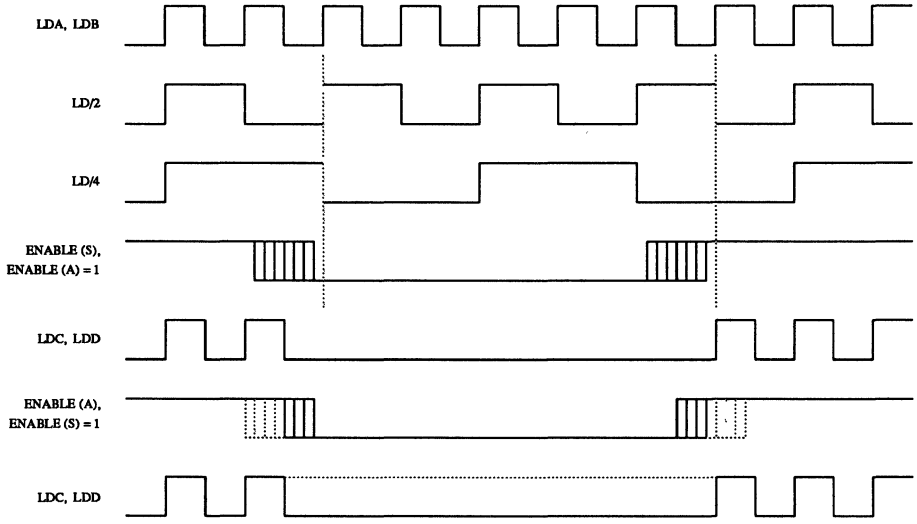


Figure 2. Load Output Timing.

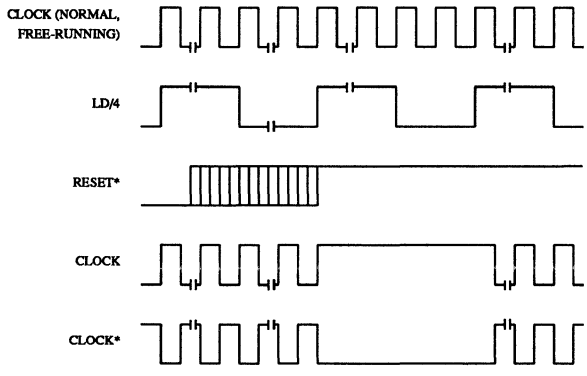


Figure 3. RESET Timing.*

Pin Descriptions

Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2v (typical) reference, and may be used to drive the VREF input of up to four RAMDACs.
OSC, OSC*	Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5v supply.
CLOCK, CLOCK*	Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and they are capable of driving up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5v supply.
DIV0, DIV1	Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified in below:

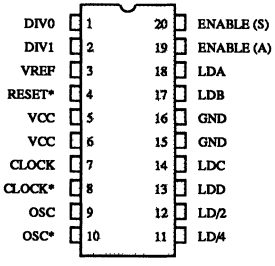
DIV1	DIV0	Division Factor	Clock Cycles Low	Clock Cycles High
0	0	+3	1	2
0	1	+4	2	2
1	0	+5	2	3
1	1	+8	4	4

LDA, LDB	Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 3, 4, 5, or 8, as determined by the DIV0 and DIV1 inputs. Each output may drive up to 20 video DRAMs without external buffering.
LD/2	Load output (TTL compatible). LD/2 is generated by dividing LDA by two. This output may drive up to 20 video DRAMs without external buffering.
LD/4	Load output (TTL compatible). LD/4 is generated by dividing LDA by four. This output may drive up to 20 video DRAMs without external buffering.
LDC, LDD	Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs. Each output may drive up to 20 video DRAMs without external buffering.
ENABLE (S)	Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
ENABLE (A)	Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs. Care should be taken to avoid glitches on this asynchronous input.

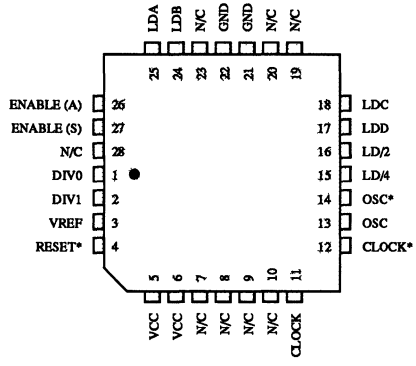
Pin Descriptions (continued)

Pin Name	Description
RESET*	Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free-running. Care must be taken to avoid glitches on this edge triggered input.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.

20-pin DIP Package



28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to the RAMDAC when using a differential crystal oscillator. The Bt438 should be located as close as possible to the RAMDAC. The termination resistors for the OSC and OSC* inputs should be located as close as possible to the Bt438.

Termination resistors are also required on the CLOCK and CLOCK* lines, located as close as possible to the RAMDAC.

Figure 5 illustrates interfacing to a single-ended crystal oscillator, while Figure 6 shows interfacing to a TTL clock for applications less than 75 MHz.

The Bt438 may drive the CLOCK and CLOCK* inputs of up to four RAMDACs if they are located as close as possible to each other. Only one set of 220/330 termination resistors should be used, and these positioned at the RAMDAC furthest away from the Bt438.

Due to the inability to insure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1k-ohm (typical) resistor must be used to isolate the VREF output of the Bt438 from the VREF input of the RAMDAC. This isolates noise from the Bt438 voltage reference from being coupled onto the RAMDAC VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA, as specified in the data sheet.

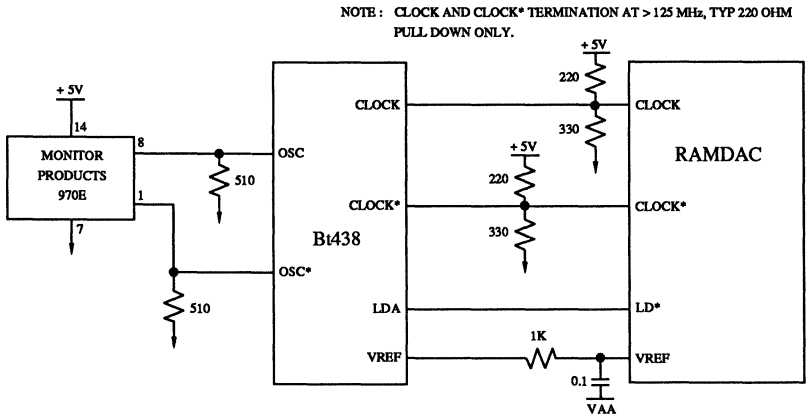


Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)

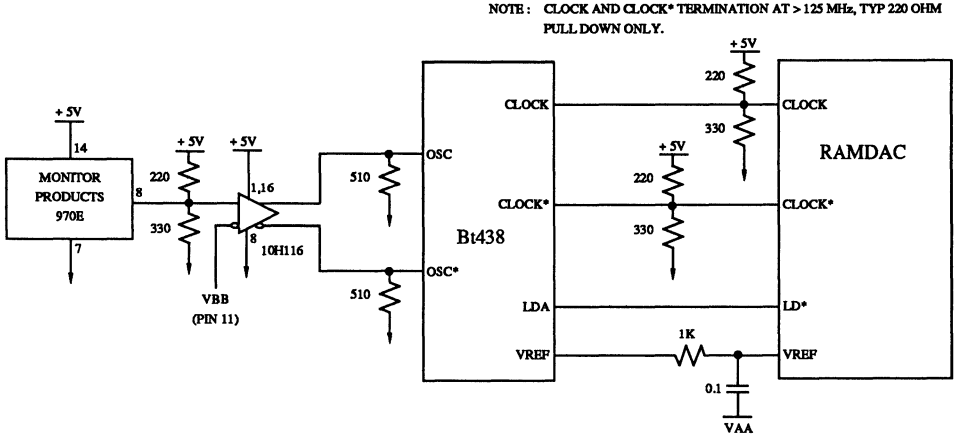


Figure 5. Interfacing to a Single-Ended Crystal Oscillator.

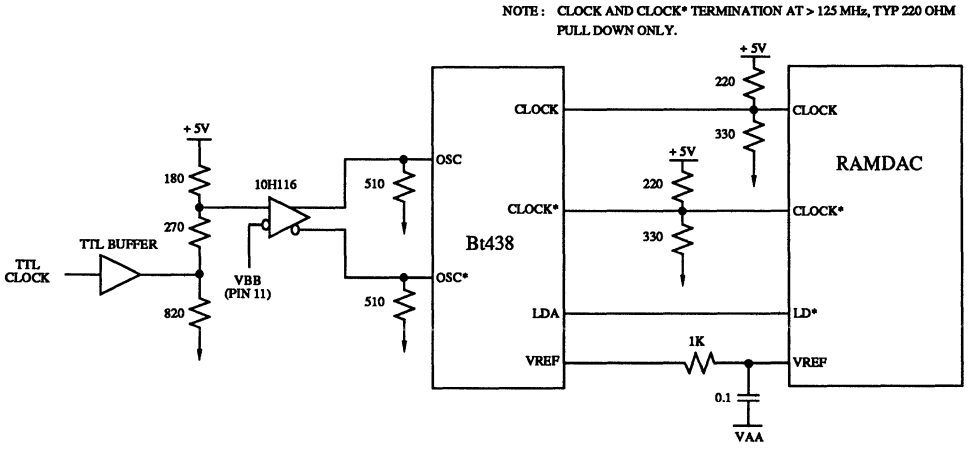


Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
OSC/OSC* Duty Cycle		40			%

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND - 0.5		VCC + 0.5	Volts
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			10	µA
Input Low Current (Vin = 0.4v)	IIL			- 0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		4		pF
ECL Inputs (at 25° C.)					
Input High Voltage	VIH	VCC - 1.1		VCC - 0.8	Volts
Input Low Voltage	VIL	GND - 0.5		VCC - 1.5	Volts
Input High Current (Vin = 4.0v)	IIH			15	µA
Input Low Current (Vin = 0.4v)	IIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0v)	CIN		4		pF
Load Outputs					
Output High Voltage (IOH = - 2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.8	Volts
Output Capacitance			10		pF
Clock Outputs (at 25° C.)					
Output High Voltage	VOH	VCC - 1.0		VCC - 0.8	Volts
Output Low Voltage	VOL	VCC - 2.0		VCC - 1.6	Volts
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage	VREF				
(Bt438 Rev. B)*		1.25	1.32	1.35	Volts
(Bt438 Rev. C)		1.2	1.235	1.26	Volts
Output Current	IREF		100		µA
VCC Supply Current**	ICC		65	85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 ohms to VCC - 2 volts.

*RSET of the RAMDAC should be adjusted due to the output voltage of the Bt438 Rev. B being higher than the recommended VREF for the RAMDAC. IOG (mA) = $\frac{11294 \text{ VREF}}{\text{RSET}}$, IOG (typ) = 26.7 mA.

**Measured without 50 ohms to VCC - 2 volts on CLOCK and CLOCK*.

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A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate	Fmax			250	MHz
LDA Output Delay (note 1)	1		4		ns
LDA, LDB Pulse Width Low (note 3)		5			ns
LDA to LDB Output Skew (note 2)			0		ns
LDA to LDC Output Skew (note 2)			1.5		ns
LDA to LD/2 Output Skew (note 2)			1.5		ns
LDA to LD/4 Output Skew (note 2)			1.5		ns
LDC to LDD Output Skew (note 2)			0		ns
RESET* Active Low Time	2	15			ns
RESET* Setup Time	3	10			ns
ENABLE (S) Setup Time	4	12			ns
ENABLE (S) Hold Time	5	-2			ns
ENABLE (A) Setup Time	6	12			ns
ENABLE (A) Hold Time	7	-2			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 ohms to VCC - 2 volts. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between 10% and 90% points. ECL input values are 3.2 to 4.2 volts, with input rise/fall times ≤ 1 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs.

Note 1: Output load = 50 pF.
Note 2: LD outputs equally loaded with 50 pF. Unequal loading may result in additional output skew.
Note 3: LD outputs not used in + 3 over 200 MHz.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt438KC	20-pin 0.3" CERDIP	0° to +70° C.
Bt438KPJ	28-pin Plastic J-Lead	0° to +70° C.

Timing Waveforms

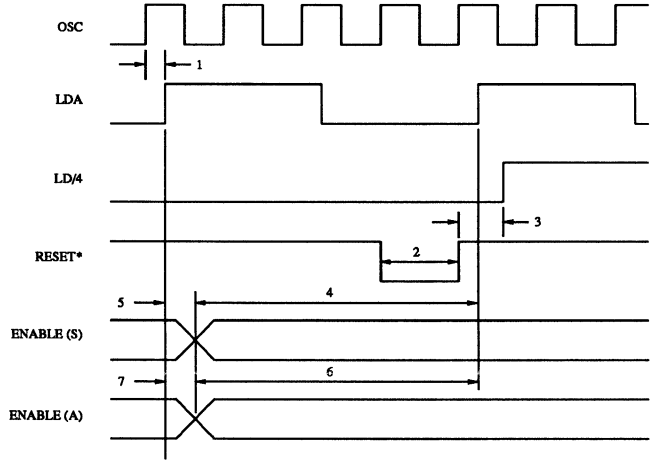


Figure 7. Input/Output Timing.

Bt439

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

200 MHz Clock Generator and Synchronizer Chip for CMOS RAMDACs™

Distinguishing Features

- 200 MHz Operation
- 4 Differential ECL Clock Outputs
- Synchronizes Multiple CMOS RAMDACs
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- Reduces Skew Between Devices to < 2 ns
- 1.2v Voltage Reference Output
- Single +5v Power Supply
- 28-pin DIP Package

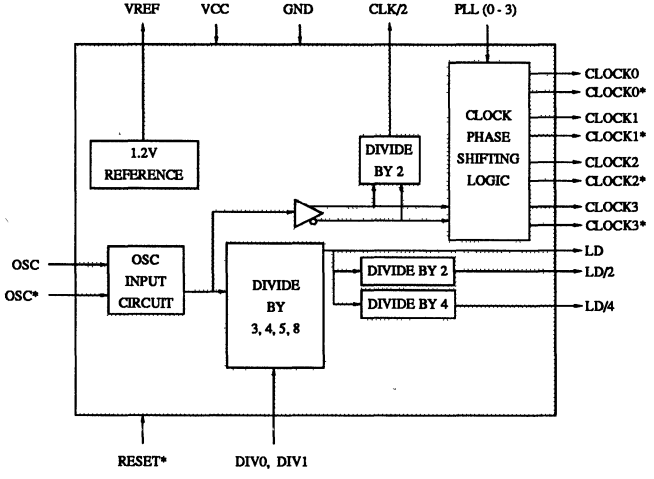
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability
- Eases Design of True Color Systems

Related Products

- Bt457, Bt461

Functional Block Diagram



Product Description

The Bt439 is clock generator chip for the high speed Brooktree single-channel CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5v supply to the RAMDACs, generating the necessary clock and control signals.

Up to four CMOS RAMDACs may be synchronized with sub-pixel resolution. The Bt439 accepts a PLL signal from each RAMDAC, and adjusts the differential clocks to each RAMDAC to minimize the phase difference between the PLL signals.

The clock output may be divided by 3, 4, 5, or 8 to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

The Bt439 optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay. An on-chip voltage reference is provided, and may be used to provide the reference voltage for up to four RAMDACs.

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L439001 Rev. D

Brooktree®

Circuit Description

The Bt439 is designed to interface to a 10K ECL crystal oscillator and generate the clock signals required by up to four CMOS RAMDACs. The OSC and OSC* inputs are designed to interface to a 10K ECL oscillator operating from a single +5v power supply.

All of the CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5v power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LD signal. LD is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively. Figure 1 shows the load output timing of the Bt439.

The RESET* input is designed to enable the Bt439 to set the pipeline delay of the RAMDACs to a fixed pipeline delay of eight clock cycles. Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 2 shows the operation of the RESET* input.

The Bt439 also generates a 1.2v (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

Synchronizing Multiple RAMDACs

The Bt439 is designed specifically to synchronize multiple CMOS RAMDACs that generate a PLL output signal. Typically, only single-channel RAMDACs will generate the PLL signal. The synchronization is necessary due to wide variations in output delays for CMOS devices due to the CMOS processing.

Following a reset input, the Bt439 sets the pipeline delay of all the RAMDACs to 8 clock cycles. It then monitors the PLL inputs, PLL0 - PLL3. On the rising edge of the last PLL input to go high, the Bt439 latches the relative time differences between the PLL inputs.

The Bt439 then stops the clocks to all the RAMDACs, with CLOCK low and CLOCK* high. The time differences between the PLL inputs are used to adjust the clock phases by selecting appropriate taps from internal delay lines (one set of delay lines for each clock signal). The Bt439 then restarts the clocks.

RESET Timing Sequence*

The following will occur when the RESET* input is asserted and remains low for at least 15nS:

The LD, LD/2, and LD/4 outputs will be forced high (CLK/2 low) within 9 nS of the falling edge of RESET* and will remain so as long as RESET* is active low. Any programmed skew between the CLKx outputs will be zeroed at this point (anticipating a re-timing sequence), which may result in some non-valid CLKx pulses. For this reason, the RESET* input should be activated only during the Blanking interval to avoid visible timing transients from the palette DACs.

When RESET* rises outside the prescribed setup/hold time before a rising OSC input, the LD output will toggle high-to-low after the fourth subsequent rising OSC input.

LD/2 will toggle high-to low coincident with the first rising edge of LD. LD/4 will toggle high-to-low on the second rising edge of LD.

On the next rising edge of LD/4 all the ECL CLKx true outputs will be forced high (CLKx low) for one cycle of the LD/4, and will fall generally (1.5*OSC period-6nS) after the following rising LD/4 and resume toggling.

RESET* transitions occurring within the setup/hold interval will delay the corresponding response one cycle of OSC. In this way correct response to an asynchronous RESET* is assured. See Figure 1.

Circuit Description (continued)

Pixel Alignment Sequence

A RESET* timing sequence must precede each Pixel Alignment sequence and should be completed within a Blanking interval to avoid corruption of the Pixel Alignment sequence which is triggered by the beginning of the ensuing active line. A Pixel Alignment sequence proceeds as follows:

The first falling PLLx input after a RESET* timing sequence initiates a delay-sampling process for the duration of the active (eg non-blanked) interval, which terminates with the last rising PLLx input (eg beginning of subsequent Blank interval). The CLKx outputs maintain minimal delay through the duration of this active line, hence any systematic delays between the PLL generators will not be corrected during this active line. Those applications which call for asserting RESET* on a line-by-line basis may consider toggling Blank in the back porch interval after normal blanking to maintain CLKx alignment on each line (at least one LD* clock cycle should occur before the first rising PLL edge).

The first rising edge of CLK/2 following the last rising PLLx input initiates a Pixel Alignment sequence which takes up to 2 periods of CLK/2 to complete. During this sequence, the CLKx outputs are held low (false) and the TTL outputs are inhibited from toggling. No false or short CLKx pulses result because of controlled time delays on chip. The proper skew compensation for each CLKx channel is latched in the internal delay lines. Concluding this sequence, the CLKy corresponding to the last (slowest) PLLy input will resume toggling with about 2 nS additional skew relative to OSC while the CLKz associated with the first (fastest) PLLz will resume with up to (Δ + (err)) nS extra delay relative to CLKy. The TTL outputs resume toggling with a consistent relationship relative to the CLK, which is consistent with the palette DAC pipeline delay preservation requirement. Note that this will stretch the low LD clock duration by up to 5 pixels which may momentarily affect any dependent synchronization timing counters.

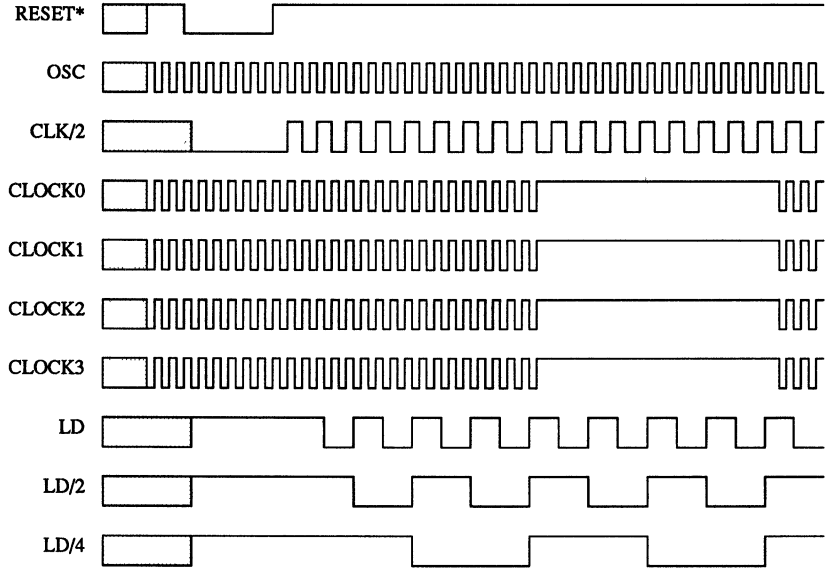


Figure 1. RESET Timing Sequence*

Circuit Description (continued)

The slowest PLLy-CLKy channel defaults to the minimum delay setting. If the slowest PLLy input lags the other active PLLx inputs by an interval exceeding the alignment span of the Bt439, then the faster PLLx channels will default to the maximum delay setting. Hence, occurrence of any active PLLx input outside the alignment span will render skew compensation on the other channels inoperative. Unused PLLx inputs are internally pulled high and hence are not sampled, leaving their corresponding CLKx channel in the minimum delay condition. See Figure 2.

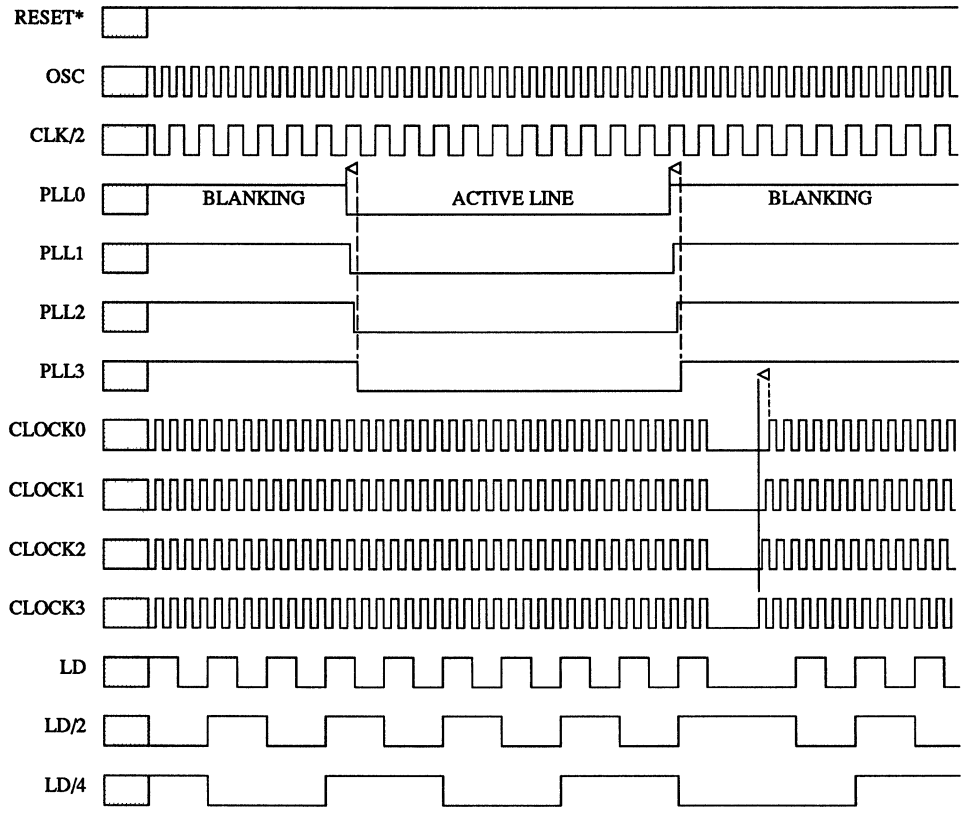


Figure 2. Pixel Alignment Sequence

Pin Descriptions

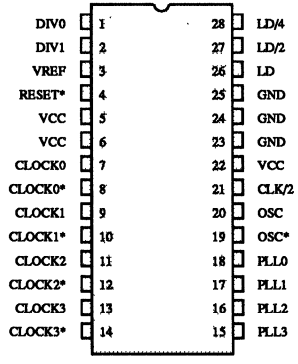
Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2v (typical) reference, and may be used to drive the VREF input of up to four RAMDACs.
OSC, OSC*	Differential ECL oscillator inputs (+5v ECL compatible). These inputs are designed to interface to a 10K ECL crystal oscillator operating from a single +5v supply.
CLOCK(0 - 3), CLOCK(0 - 3)*	Differential clock outputs (+5v ECL compatible). These outputs connect directly to the CLOCK and CLOCK* inputs of up to four RAMDACs. The output levels are equivalent to 10K ECL logic operating from a single +5v supply.
DIV0, DIV1	Divide control inputs (TTL compatible). These inputs specify the division factor for the generation of the LD signal, as specified in below:

DIV1	DIV0	Division Factor	Clock Cycles Low	Clock Cycles High
0	0	+3	1	2
0	1	+4	2	2
1	0	+5	2	3
1	1	+8	4	4

LD	Load output (TTL compatible). LD is generated by dividing CLOCK by 3, 4, 5, or 8, as determined by the DIV0 and DIV1 inputs. It may drive up to 20 video DRAMs without external buffering.
LD/2	Load output (TTL compatible). LD/2 is generated by dividing LD by two. This output may drive up to 20 video DRAMs without external buffering.
LD/4	Load output (TTL compatible). LD/4 is generated by dividing LD by four. This output may drive up to 20 video DRAMs without external buffering.

Pin Descriptions (continued)

Pin Name	Description
RESET*	Reset control input (TTL compatible). See RESET* Timing Sequence. Care must be taken to avoid glitches on this edge triggered input.
PLL0 - PLL3	Phase inputs. These inputs are used to determine the relative phases of the RAMDAC outputs. Each RAMDAC to be synchronized must generate a unique PLL signal. Unused PLL inputs should be connected to VCC through a 1K pullup resistor.
CLK/2	Clock/2 output (+5v ECL compatible). The OSC input is divided by two and output onto this pin. It may be used as a general purpose clock for external circuitry.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.



Application Information

Interfacing to the RAMDAC

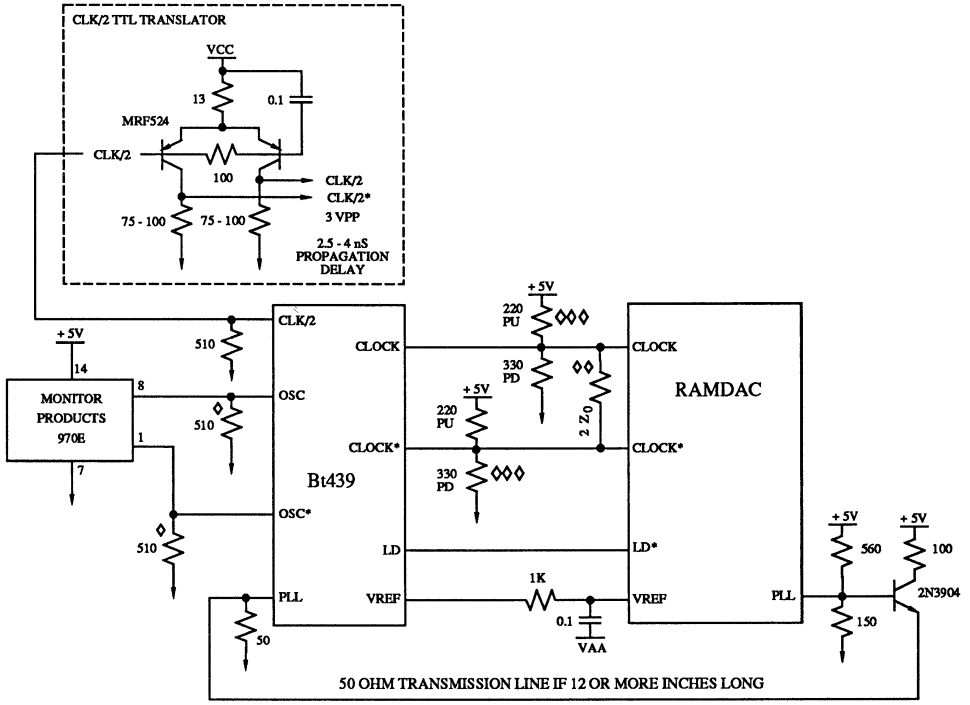
Figure 3 illustrates interfacing the Bt439 to a CMOS RAMDAC when using a differential crystal oscillator. The Bt439 should be located as close as possible to the RAMDACs. The termination resistors for the OSC and OSC* inputs should be located as close as possible to the Bt439.

Termination resistors are also required on the CLOCK and CLOCK* lines, located as close as possible to the RAMDAC. For clock lines > 4", pulldowns at the Bt439 as well as balance lined termination at the palette are recommended. For striplines of Zo, characteristic impedance separated by > 2d dielectric spacing, a balanced termination of 2Zo is appropriate.

Figure 4 illustrates interfacing to a single-ended crystal oscillator, while Figure 5 shows interfacing to a TTL clock for applications less than 75 MHz.

A 1k-ohm (typical) resistor must be used to isolate the VREF output of the Bt439 from the VREF input of the RAMDAC. This isolates noise from the Bt439 voltage reference from being coupled onto the RAMDAC VREF pin. The VREF input of each RAMDAC must still have a decoupling capacitor to VAA, as specified in the data sheet.

Due to the limited drive capability of the PLL output of the RAMDACs, the buffer circuitry should be located as close as possible to the RAMDAC.



◊ 510 OHM RESISTOR NEEDED IF THERE ARE NO INTERNAL PULL DOWNS IN OSCILLATOR.

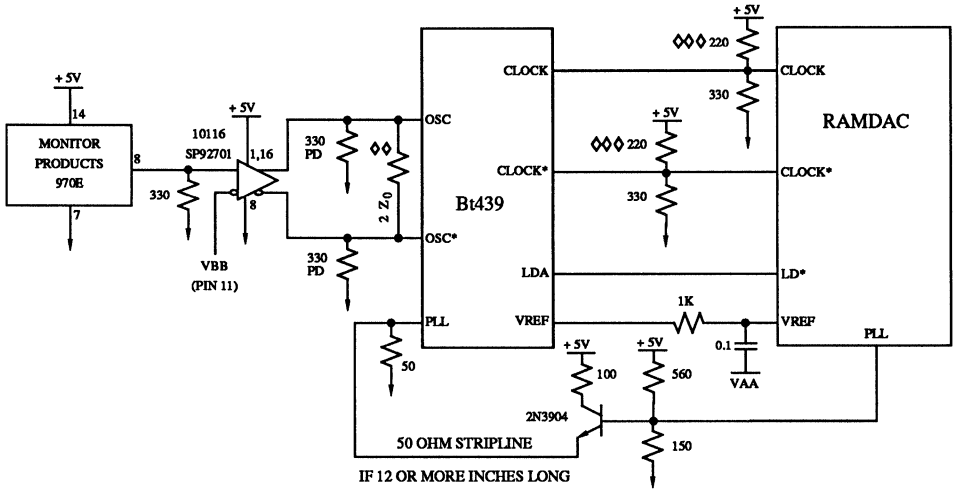
◊◊ OPTIONAL BALANCED TERMINATION FOR HIGH IMPEDANCE DIFFERENTIAL LINES > 4 INCHES; OMIT 220 OHM PULL UP IF USED.

◊◊◊ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.

Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6.

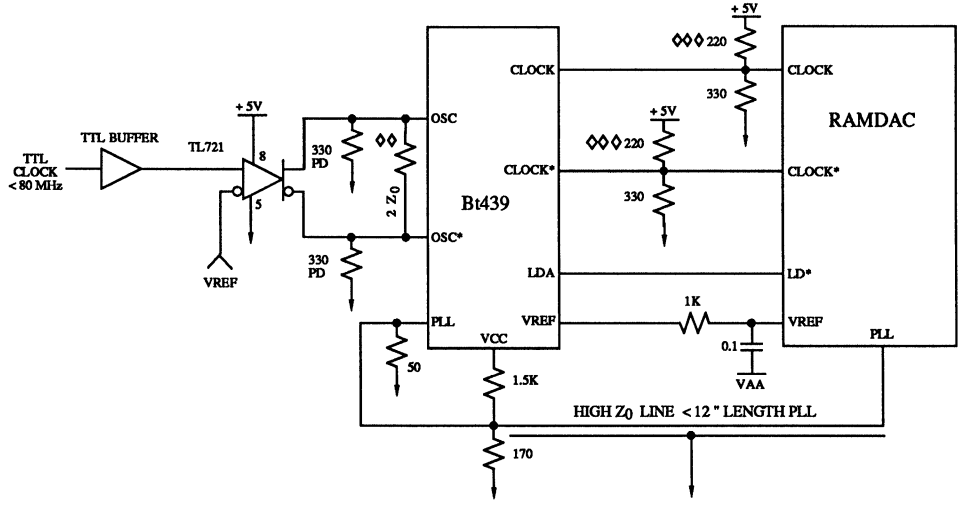
Figure 3. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)



◇◇ OPTIONAL BALANCED TERMINATION FOR CLOCK LINES > 4 INCHES. Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6
◇◇◇ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.

Figure 4. Interfacing to a Single-Ended Crystal Oscillator.



◇◇ OPTIONAL BALANCED TERMINATION FOR CLOCK LINES > 4 INCHES. Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6
◇◇◇ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.

Figure 5. Interfacing to a TTL Clock < 80 MHz.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature - Still Air	TA	0		+ 70	°C.
OSC/OSC* Duty Cycle		40			%

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND - 0.5		VCC + 0.5	Volts
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			10	µA
Input Low Current (Vin = 0.4v)	IIL	- 0.7			mA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
ECL Inputs (at 25° C.)					
Input High Voltage	VIH	VCC - 1.1		VCC - 0.8	Volts
Input Low Voltage	VIL	VCC - 2		VCC - 1.5	Volts
Input High Current (Vin = 4.0v)	IIH		4	15	µA
Input Low Current (Vin = 0.4v)	IIL	- 15	0		µA
Input Capacitance (f = 1 MHz, Vin = 4.0v)	CIN		10		pF
Load Outputs					
Output High Voltage (IOH = - 2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.8	Volts
Output Capacitance			10		pF
Clock Outputs (at 25° C.)					
Output High Voltage	VOH	VCC - 1.035		VCC - 0.8	Volts
Output Low Voltage	VOL	VCC - 2.0		VCC - 1.6	Volts
Output Capacitance	COUT		10		pF
Voltage Reference					
Output Voltage @ IREF = -100 µA	VREF	1.2	1.235	1.26	Volts
PLL Inputs					
Input High Voltage	VIH	1.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.5	Volts
Input High Current (Vin = 1.2v)	IIH		0	10	µA
Input Low Current (Vin = 0.5v)	IIL	- 700	- 180		µA
Input Capacitance			tbd		pF
VCC Supply Current*	ICC		300	400	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK, CLOCK*, and CLK/2 outputs have 50 ohms to VCC - 2 volts.

Measured without 50 ohms to VCC - 2 volts on CLOCK, CLOCK, and CLK/2. At VCC = + 5.25

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate (note 1)	Fmax			200	MHz
LD Output Delay (note 2)	1	6	10	12	ns
LD Pulse Width	2	9			ns
LD to LD/2 Output Skew (note 3)		0	1.5	3	ns
LD to LD/4 Output Skew (note 3)		0	1.5	3	ns
CLK/2 Output Delay	3		2		ns
RESET* Active Low Time	4	15			ns
RESET* Setup Time	5	10			ns
Alignment Span	6	5			ns
Residual Alignment Error (note 4)			1.5	2	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK, CLOCK*, and CLK/2 outputs have 50 ohms to VCC - 2 volts. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between 10% and 90% points. ECL input values are (VCC - 0.9) to (VCC - 1.6) volts, with input rise/fall times ≤ 1 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs.

Note 1: ÷ 3 Mode LD outputs valid only to 100 MHz without significant distortion.
Note 2: Output load = 50 pF. Derate 1 ns for each additional 50 pF loading.
Note 3: Load outputs equally loaded with 50 pF. Unequal loading may result in additional output skew.
Note 4: Maximum deviation of any two dependent PLL inputs after alignment sequence (PLL inputs within span before alignment)

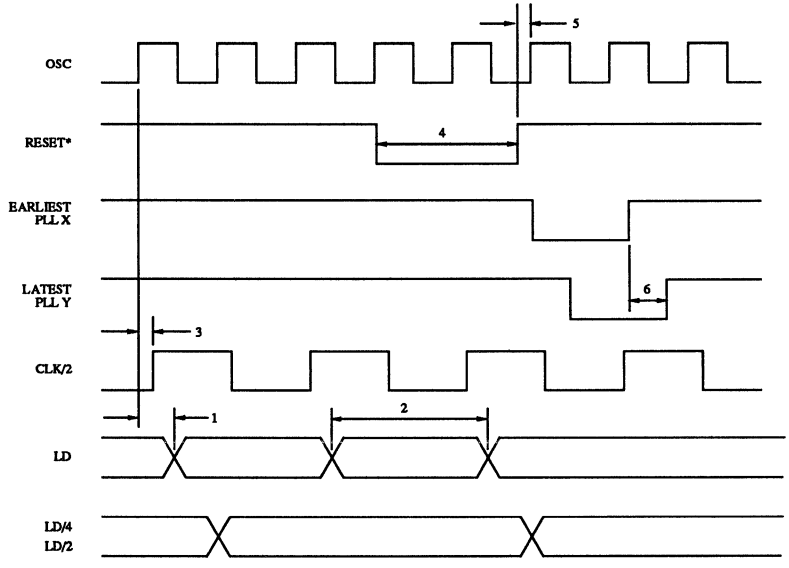


Figure 6. Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range Still Air
Bt439KC	28-pin 0.6" CERDIP	0° to +70° C.

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Table of Contents

Bt208

18 MSPS

Monolithic CMOS

8-bit Flash

Video A/D Converter

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- No Video Amplifier Required
- ± 1/4 LSB Typical DL Error
- ± 1/2 LSB Typical IL Error
- External Zero and Clamp Control
- Overflow Output
- On-Chip Reference
- Output Enable Control
- TTL Compatible
- +5v CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 500 mW

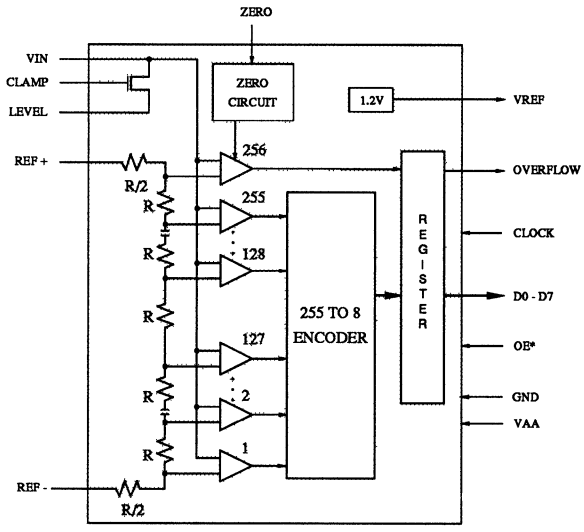
Applications

- Image Processing
- Video Digitizing

Related Products

- Bt251, Bt253
- Bt261

Functional Block Diagram



Product Description

The Bt208 is an 8-bit flash A/D converter designed specifically for video digitizing applications. A flash converter topology is utilized which has 256 high speed comparators in parallel to digitize the analog input signal.

Flexible input ranges enable RS-170, RS-170A, RS-343A, PAL, and SECAM video signals to be digitized without requiring a video amplifier.

The TTL compatible output data and OVERFLOW are registered synchronously with the clock signal. OE* three-states the D0 - D7 outputs asynchronously to CLOCK.

The ZERO input is used to zero the comparators, while CLAMP performs DC restoration of the video signal (by forcing the VIN input to the voltage on the LEVEL pin) if AC-coupled to the video signal.

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Circuit Description

As illustrated in the functional block diagram, the Bt208 contains 256 high-speed comparators, a 255 to 8 encoder, output register, and a resistor divider network. 255 of the comparators are used to digitize the analog signal, the additional comparator is used to generate the OVERFLOW bit.

General Operation

The Bt208 converts an analog signal in the range of REF- ≤ Vin ≤ REF+, generating a binary number from $00 to $FF, and an OVERFLOW output (see Table 1).

The values of REF+ and REF- are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Applications Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt208. The sample is taken following the falling edge of CLOCK. While CLOCK is low, the 255 to 8 encoding is performed. The binary data and OVERFLOW are registered and output onto the D0 - D7 and OVERFLOW pins on the next rising edge of CLOCK.

Comparator Zeroing

The ZERO input is used to periodically zero the comparators. The comparators have an initial threshold mismatch due to manufacturing tolerances. Zeroing charges capacitors in the comparators that offset this threshold mismatch. Due to capacitor discharging, they must be periodically zeroed.

While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, D0 - D7 and OVERFLOW are not updated. They retain the data loaded before the ZERO cycle.

Input Signal Clamping

CLAMP and LEVEL are used only in applications where the video signal is AC-coupled to VIN. While CLAMP is a logical one, the VIN input is forced to the voltage level of the LEVEL pin to DC restore the video signal.

In applications where the video signal is DC-coupled to VIN, the LEVEL pin should float, be connected to VIN, or (only on the 28-pin PLCC package) CLAMP should always be a logical zero.

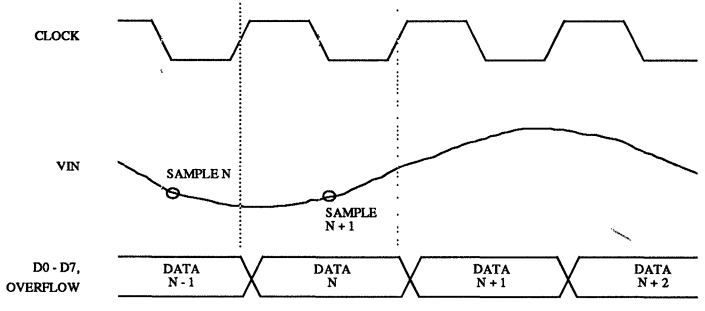
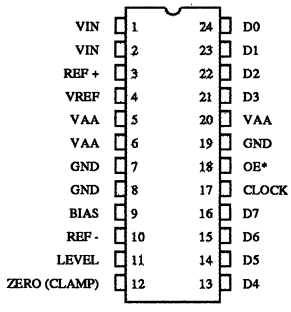


Figure 1. Input/Output Timing.

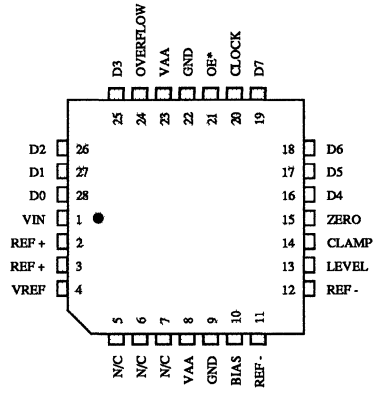
Pin Descriptions

Pin Name	Description
D0 - D7	Data outputs (TTL compatible). D0 is the least significant data bit. These outputs are latched and output following the rising edge of CLOCK. Coding is binary. For optimum performance, D0 - D7 should have minimal loading. If driving a large capacitive load, an external buffer is recommended.
OE*	Output enable control input (TTL compatible). Negating OE* three-states D0 - D7 asynchronously to CLOCK. The OVERFLOW output is not affected by the state of OE*.
OVERFLOW	Overflow output (TTL compatible). OVERFLOW is latched and output following the rising edge of CLOCK. OE* does not affect the OVERFLOW output signal. OVERFLOW is not available on the DIP package.
CLOCK	Clock input (TTL compatible). It is recommended that this pin be driven by a dedicated TTL buffer to minimize sampling jitter.
REF+	Top of ladder voltage reference (voltage input). REF+ sets the VIN voltage level that generates $FF on the D0 - D7 outputs. All REF+ pins must be connected together as close to the device as possible. A decoupling capacitor is NOT recommended on REF+.
REF-	Bottom of ladder voltage reference (voltage input). Typically, this input is connected to GND. REF- sets the VIN voltage level that generates $00 on the D0 - D7 outputs. All REF- pins must be connected together as close to the device as possible.
VIN	Analog signal inputs (voltage input). All VIN pins must be connected together as close to the device as possible.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators are zeroed. ZERO is latched on the rising edge of CLOCK. Note that on the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, zeroing and clamping occur simultaneously.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN inputs are forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. Note that on the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, ZERO and CLAMP are asserted simultaneously.
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be used for clamping while CLAMP is a logical one. It is typically connected to GND in applications where the video signal is AC-coupled to VIN. In applications where the video signal is DC-coupled to VIN, the LEVEL pin should float or be connected to VIN.
VREF	Voltage reference output pin. This pin provides a 1.2v (typical) output. A decoupling capacitor is NOT recommended on VREF.
VAA	+5v power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected together as close to the device as possible.
BIAS	Bias control pin. This pin should be left floating.

Pin Descriptions (continued)



24-pin 0.3" DIP Package



28-pin Plastic J-Lead (PLCC) Package

Note: N/C pins are reserved and must remain floating.

Vin* (v)	Overflow	D0 - D7	OE*
> 0.998	1	$FF	0
0.996	0	$FF	0
0.992	0	$FE	0
:	:	:	:
0.500	0	$81	0
0.496	0	$80	0
0.492	0	$7F	0
:	:	:	:
0.004	0	$01	0
< 0.002	0	$00	0
		3-state	1

*with REF+ = 1.000v and REF- = 0.000v. Ideal center values. 1 LSB = 3.9063 mV.

Table 1. Output Coding.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt208 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt208 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt208, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt208.

Power Planes

The Bt208 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within three inches of the Bt208.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt208 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

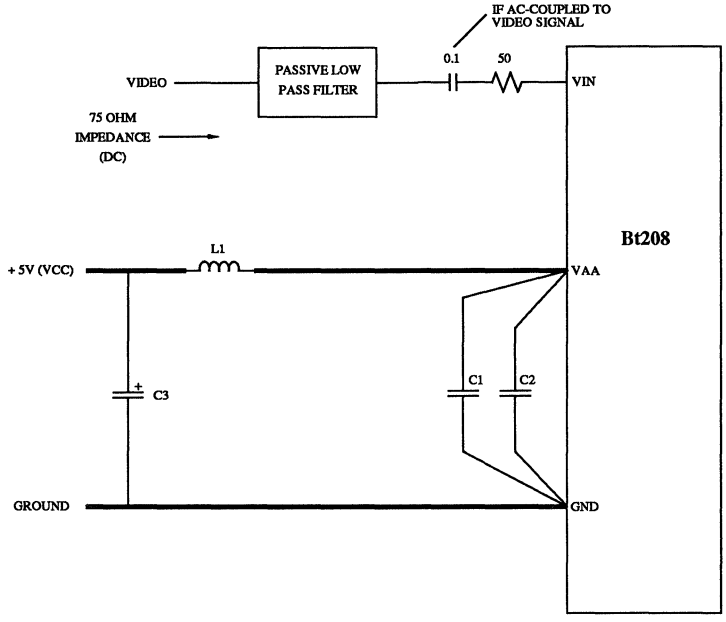
For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the two power pin groups to GND. These capacitors should be placed as close as possible to the device.

Signal Interconnect

The digital signals of the Bt208 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt208.

Figure 2. Typical Connection Diagram and Parts List.

Application Information

Using the Internal Reference

The Bt208 has a 1.2v on-chip reference available (VREF). VREF may be divided down and used to drive the REF+ input as shown in Figure 3. The 200-ohm potentiometer serves three purposes: to allow adjustment for different video signal levels, to allow for video level tolerances, and to adjust for tolerance of the internal reference.

Note that VREF should supply at least 5 mA of current to maintain voltage stability over temperature. Thus, VREF should drive a resistive load between 90 and 240 ohms.

Using An External Reference

Figure 4 illustrates using a 1.2v LM385 to generate a 0v to 1.2v reference. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5v supply.

As REF+ should be driven by a high AC impedance source, a 100-ohm resistor should be placed between REF+ and the output of the op-amp, as shown in Figure 4.

AC-Coupled Vs. DC-Coupled Input

The Bt208 may be either AC- or DC-coupled to the video signal, as shown in Figures 5 and 6. The 75-ohm resistor to ground provides the typical 75-ohm termination required by video signals. The 50-ohm resistor provides isolation from any clock kickback noise on VIN from being coupled onto the video signal.

Zeroing

As the comparators on the Bt208 must be periodically zeroed, it is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt208 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt208.

As long as the recommended zeroing interval is maintained, the Bt208 will meet linearity specifications. The longer between zeroing intervals, the more the linearity error increases.

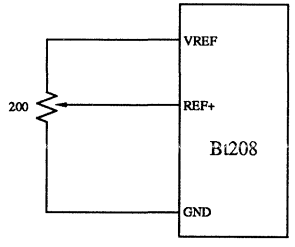


Figure 3. Using the Internal Reference.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0v	0.9v - 1.1v
RS-170 w/sync	1.4v	1.2v - 1.6v
RS-170A w/o sync	1.0v	0.9v - 1.1v
RS-170A w/sync	1.4v	1.0v - 1.8v
RS-343A w/o sync	0.7v	0.6v - 0.85v

Table 2. Video Signal Tolerances.

Application Information (continued)

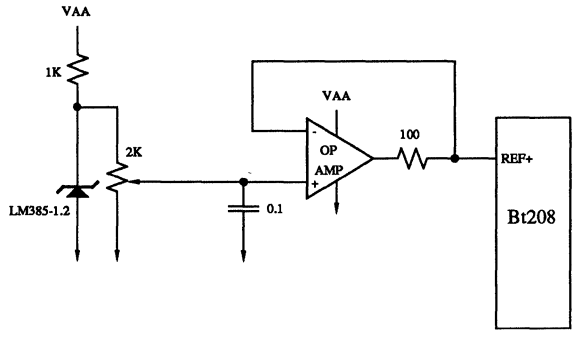


Figure 4. Using An External Reference.

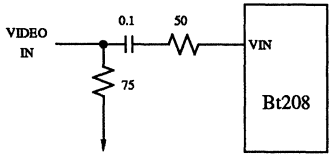


Figure 5. Typical AC-Coupled Input Circuitry (No Input Filtering).

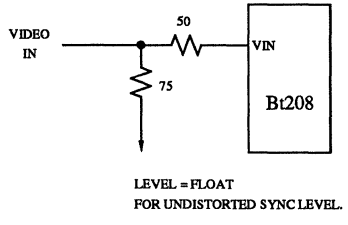


Figure 6. Typical DC-Coupled Input Circuitry (No Input Filtering).

Application Information (continued)

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2v, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2v input range.

When digitizing with a full scale range less than 0.7v, the Bt208's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting REF+ equal to 0.6v and REF- equal to 0v, 0.6v video signals may be digitized; however the integral linearity (IL) error will increase to about ± 1.8 LSB. The SNR will drop to about 40 dB (from 43 dB). With REF+ equal to 0.5v and REF- equal to 0v, 0.5v video signals may be digitized with an IL error of about ± 2 LSB. The SNR will drop to about 39 dB (from 43 dB).

SNR and Error Rate Vs. Clock Timing

Figure 7 illustrates the error rate vs. clock low time, while Figure 8 illustrates the SNR vs. clock high time. Below about 17 MHz, the Bt208 performs adequately with a 50% duty cycle (30 ns low and 30 ns high times).

Above 17 MHz, by adjusting the clock duty cycle a trade-off between error rate and SNR is possible.

An error is defined as being a sample that is more than 8 LSBs (out of 255) from the expected value, where the previous and following samples are less than (or equal to) 8 LSBs from the expected value.

Output Noise

Although the Bt208 does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increases.

The output noise of the Bt208 may be reduced by adjusting the duty cycle of the clock -- this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2" VCR.

PC Board Sockets

It is recommended that the Bt208 not be used with a socket, and have a 0.15" standoff. Use of a socket increases the output noise due to digital output ringing.

Application Information (continued)

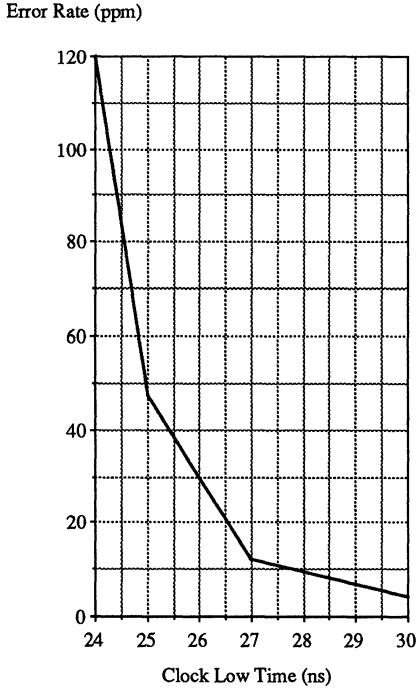


Figure 7. Error Rate vs. Clock Low Time.

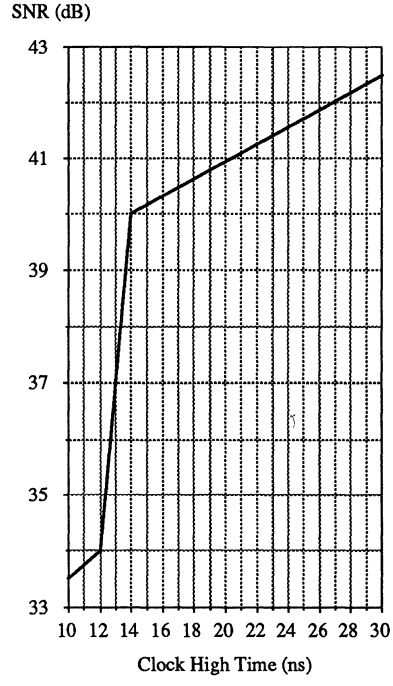


Figure 8. SNR vs. Clock High Time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.00	5.5	Volts
Voltage References					
Top	REF+	0.7	1	2.0	Volts
Bottom	REF-	0	0	1.3	Volts
Difference (Top - Bottom)		0.7	1	1.2	Volts
Analog Input Amplitude	VIN	0.7	1	1.2	Volts
Analog Input Range	VIN		REF- to REF+		Volts
LEVEL Input Voltage		GND - 0.3	REF-	REF+	Volts
Time Between Zeroing Intervals			60	150	µS
Ambient Operating Temperature	TA	0		+ 70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Input Voltage	VIN	GND - 0.3		VAA + 0.5	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error (note 1)	IL		± 0.5	± 1	LSB
Differential Linearity Error	DL		± 0.25	± 1	LSB
Output Noise (note 2)			± 1		LSB
Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C.
Coding					Binary
No Missing Codes			guaranteed		
VIN Analog Inputs (note 3)					
CLAMP = 0					
Input Impedance	RIN	10			M ohms
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
REF+ Reference Input					
Input Current	IREF+		1		mA
Input Impedance	RREF+		1		K ohms
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			-1	µA
Input Capacitance	CIN		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Clock Kickback (note 4)			160		pV - sec
Digital Outputs					
Output High Voltage (IOH = -50 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Three-State Current	IOZ			10	µA
Output Capacitance	COUT			10	pF
Internal Voltage Reference	VREF		1.2		Volts
Regulation (at 6 mA)			5		mV
Output Current	IREF			15	mA
Power Supply Rejection Ratio (not including reference)	PSRR		0.004		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float, BIAS = float.

Note 1: Using best-fit linearity. Averaged value evaluated using a closed loop system.

Note 2: Clock duty cycle adjusted for minimum output noise for a DC input. For a DC input, output noise may increase if clock duty cycle is not adjusted.

Note 3: LEVEL = GND.

Note 4: Measurement of noise coupled onto VIN due to clocking (Rs = 75 ohms). Typically occurs over a 5 ns interval.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			18	MHz
Clock Cycle Time	1	55.5			ns
Clock Low Time	2	35			ns
Clock High Time	3	20			ns
Data Output Delay	4			25	ns
OE* Asserted to D0 - D7 Valid	5			25	ns
OE* Negated to D0 - D7 3-Stated	6			25	ns
ZERO Setup Time	7	tbd			ns
ZERO Hold Time	8	tbd			ns
ZERO, CLAMP High Time (note 1)		1			Clock
Aperture Delay	9		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW	6			MHz
Transient Response (note 2)				1	Clock
Overload Recovery (note 3)				1	Clock
Zero Recovery Time (note 4)				1	Clock
RMS Signal to Noise Ratio	SNR				
Fin = 4.2 MHz, Fs = 10.7 MHz			43		dB
Fin = 4.2 MHz, Fs = 14.32 MHz			42		dB
Fin = 2.75 MHz, Fs = 6.75 MHz			44		dB
Fin = 5.75 MHz, Fs = 13.5 MHz			41		dB
Fin = 4.2 MHz, Fs = 17.72 MHz			41		dB
Differential Gain Error (note 5)	DG		2		%
Differential Phase Error (note 5)	DP		1		Degree
Supply Current (note 6) (Excluding IREF+)	IAA		100	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float, BIAS = float. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0 - D7 and OVERFLOW output load ≤ 25 pF.

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.

Note 2: For full-scale step input, full accuracy attained in specified time.

Note 3: Time to recover to full accuracy after a > 1.2v input signal.

Note 4: Time to recover to full accuracy following a zero cycle.

Note 5: 4x NTSC subcarrier, unlocked.

Note 6: IAA (typ) at VAA = 5.0v, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.5v, Fin = 6 MHz, Fs = 18 MHz.

Ordering Information

Model Number	Maximum Clock Rate	Package	Ambient Temperature Range
Bt208KP	18 MSPS	24-pin 0.3" Plastic DIP	0° to +70° C.
Bt208KPJ	18 MSPS	28-pin Plastic J-Lead	0° to +70° C.

Timing Waveforms

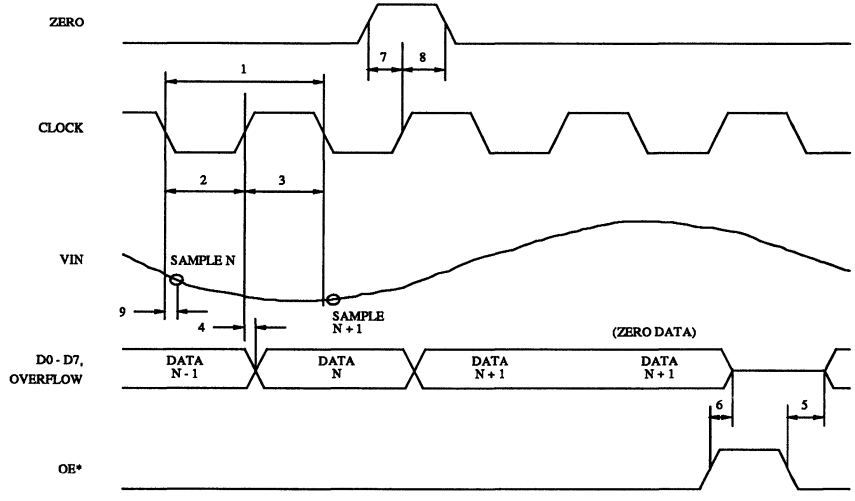


Figure 9. Input/Output Timing.

Linearity Test Circuit

Procedure:

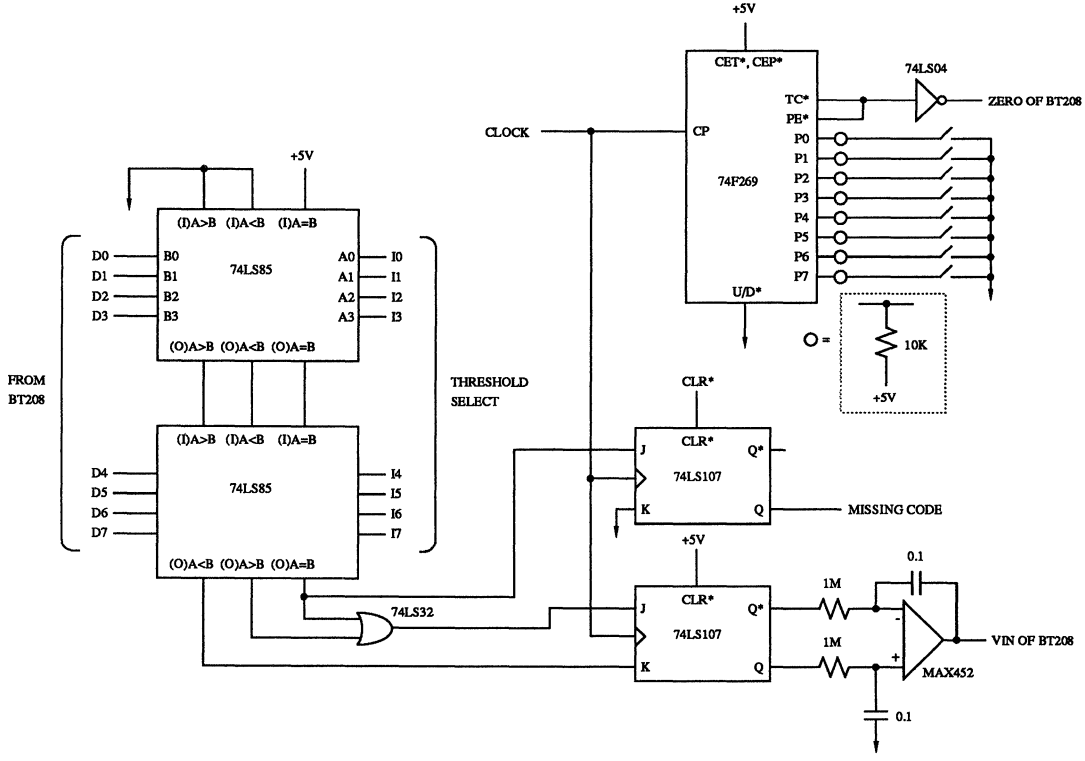
1. Set threshold select value to 0.
2. Measure Vin at integrator output.
3. Repeat steps 1 and 2 for codes 1 - 254.
4. Plot linearity as:

For I = 1 to 253:

$$IL(I) = 100*\left(\frac{I}{254} - \frac{VOLT(I) - VOLT(0)}{VOLT(254) - VOLT(0)}\right)$$

For I = 1 to 254:

$$DL(I) = 100*\left(\frac{VOLT(I) - VOLT(I-1)}{VOLT(254) - VOLT(0)} - \frac{1}{254}\right)$$



Bt251

15 MSPS

Monolithic CMOS

Single Channel

8-Bit Image Digitizer

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 4 Software Selectable Analog Inputs
- DC- or AC-Coupled Video Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- 8-bit Flash A/D Converter
- 256 x 8 Lookup Table
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5v CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 750 mW

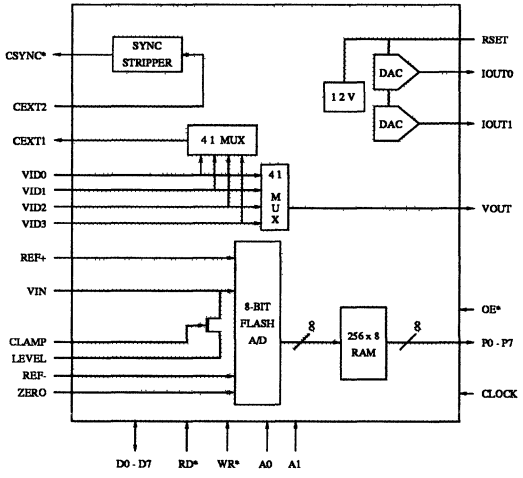
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt208, Bt253
- Bt261

Functional Block Diagram



Product Description

The Bt251 Image Digitizer is designed to digitize standard video signals (RS-170, RS-170A, RS-343A, RS-330, PAL, or SECAM). The architecture of the Bt251 enables the addition of external circuitry for filtering, gain, etc., along the signal path. A standard MPU interface is provided for accessing various control functions.

Four analog inputs are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking independently of the video input being digitized. A TTL-compatible composite sync signal is output to interface to the genlock circuitry.

The output of the 8-bit A/D converter addresses a 256 x 8 lookup table RAM, enabling real-time image manipulation prior to data storage, including thresholding, contrast enhancement, etc. The digitized data outputs may be three-stated synchronously to clock via the OE* control.

Optional MPU controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D. Zeroing and clamping signals are available to control the A/D timing for application specific designs. The clamping level is externally set via the LEVEL pin.

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Circuit Description

MPU Interface

As shown in the functional block diagram, the Bt251 supports a standard MPU interface (D0 - D7, RD*, WR*, A0, and A1). MPU operations are asynchronous to the clock.

An internal 8-bit address register, in conjunction with A0 and A1, is used to specify which control register or RAM location the MPU is accessing, as shown in Table 1. All registers and RAM locations may be written to or read by the MPU at any time; however, while digitizing a video signal, the MPU should not access the RAM as this will corrupt the digitized data.

The address register increments after each MPU read or write cycle. After writing to location $FF, the address register resets to $00. ADDR0 corresponds to D0 and is the least significant bit.

Flash A/D Converter

The Bt251 uses an 8-bit flash A/D converter to digitize the video signal. The A/D digitizes analog signals in the range of REF- ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF-) to $FF (Vin ≥ REF+).

VIN may be either DC- or AC-coupled to the video signal. If AC-coupled, the CLAMP and LEVEL controls may be used to DC restore the video signal.

Analog Input Selection

The Bt251 supports four analog input sources, VID0 - VID3. The MPU specifies which one is to be digitized via the command register. Any required gain to standard video levels should be done prior to driving the VIDx inputs to ensure reliable sync detection.

The selected video signal is output onto VOUT. VOUT may be connected directly to VIN if no filtering or gain of the video signal is required.

If digitizing a video signal containing color subcarrier information, such as RS-170A, PAL, or SECAM, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low pass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on VOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be connected together through the equivalent of 200 ohms.

A1	A0	ADDR7 - ADDR0	Addressed by MPU
0	0	xxxx xxxx	address register
0	1	0000 0000	RAM location $00
0	1	0000 001	RAM location $01
:	:	:	:
0	1	1111 1111	RAM location $FF
1	0	xxxx xx00	command register
1	0	xxxx xx01	IOUT0 data register
1	0	xxxx xx10	IOUT1 data register
1	0	xxxx xx11	reserved
1	1	xxxx xxxx	reserved

Table 1. Address Register Operation.

Circuit Description (continued)

A/D Reference Generation

Typically, REF+ is connected to a 0.7v to 1.2v reference, while REF- is connected to GND, as shown in Figure 1. This mode of operation may be used when the only operation is to digitize video signals with an amplitude of 0.7v to 1.2v with no adjustment of gain or offset.

The gain and offset of the video signal may effectively be done via the MPU adjustable outputs IOUT0 and IOUT1, as shown in Figure 2. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented.

IOUT0 and IOUT1 are current outputs (0 to 1 mA) generated by two 6-bit D/A converters. A 1200-ohm RSET resistor generates a 1 mA full scale output current. 1000-ohm resistors to GND generate a 0v to 1v level that drive the REF+ and REF- inputs through voltage followers. The top and bottom references may thus be adjusted with 16 mV resolution.

A/D Zeroing

The ZERO input is used to zero the comparators, and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the P0 - P7 outputs are not updated. They retain the data loaded before the ZERO cycle.

A/D Input Clamping

If VIN is AC-coupled to the video signal, the CLAMP and LEVEL controls may be used to DC restore the video signal. While CLAMP is a logical one, the video signal is clamped to the voltage level present on the LEVEL pin. Typically, LEVEL should be connected to GND.

If VIN is DC-coupled to the video signal, LEVEL should float or CLAMP should always be a logical zero.

Lookup Table RAM

A 256 x 8 lookup table RAM is provided on-chip to implement simple imaging operations such as gamma manipulation, simple contrast enhancement, inverting of data, or a non-linear transfer function of the A/D converter. Data from the A/D is used to address the RAM; the addressed data is output onto P0 - P7.

The RAM may be effectively bypassed by loading each location with it's corresponding address. As the lookup table RAM is not dual-ported, MPU accesses have priority over digitized data passing through the RAM. During MPU accesses to the RAM, P0 - P7 are undefined.

Sync Detect Circuitry

The Bt251 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clock and there are no pipeline delays.

The MPU specifies from which analog input to detect sync. The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The MPU selects one of four levels of sync threshold by selecting how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

Circuit Description (continued)

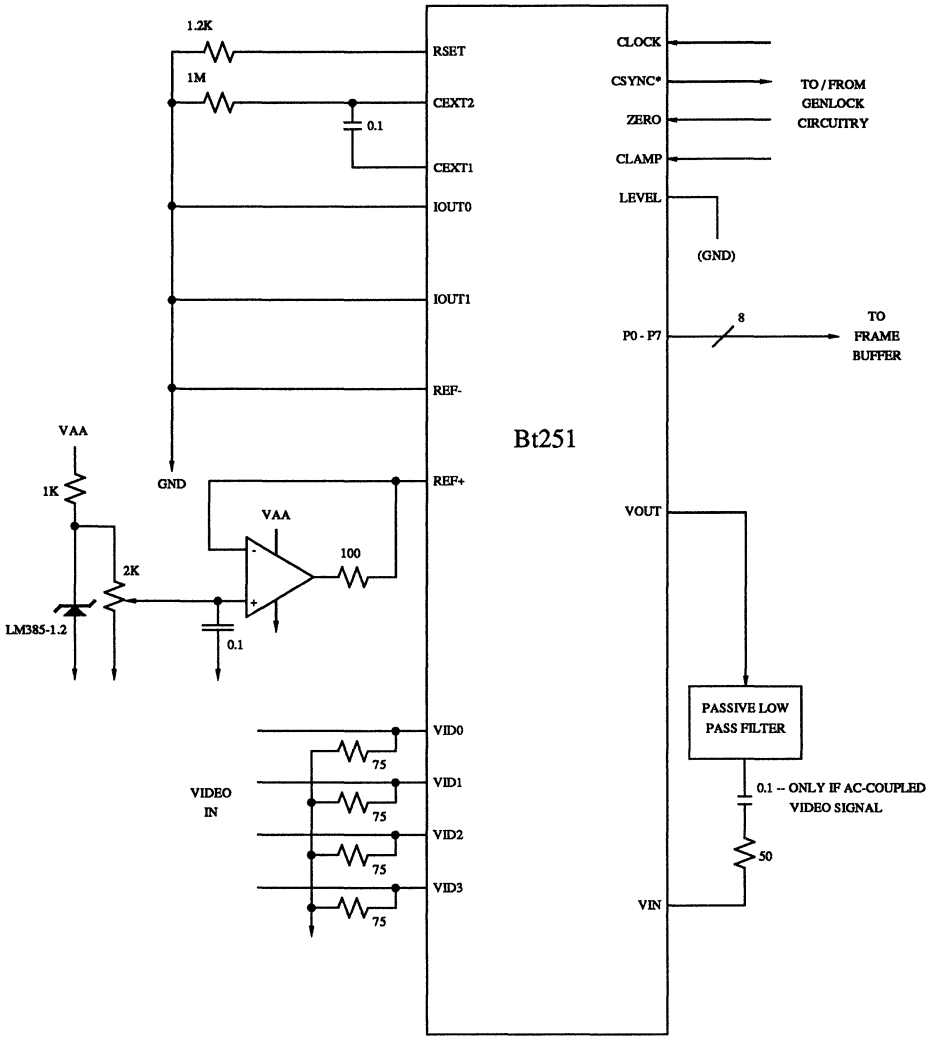


Figure 1. Typical Bt251 External Circuitry. (Fixed Top and Bottom References)

Circuit Description (continued)

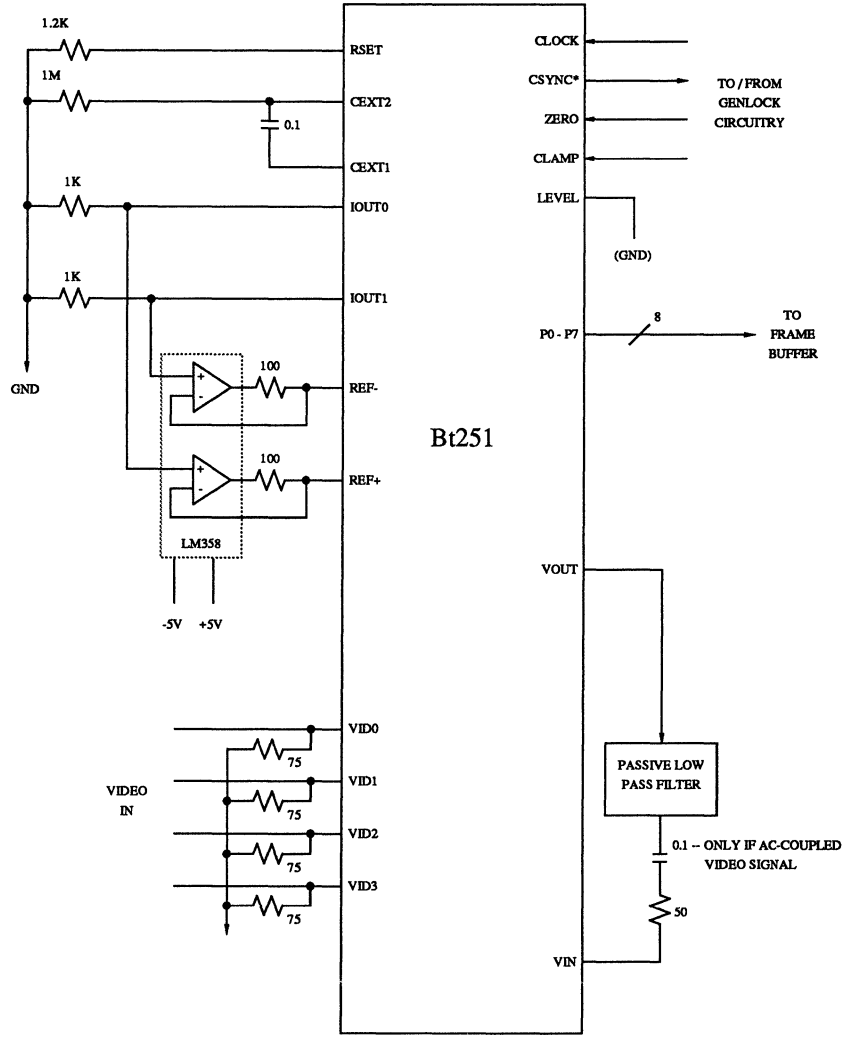


Figure 2. Typical Bt251 External Circuitry. (Variable Top and Bottom References)

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7, D6	Digitize select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify which analog input is to be digitized. The selected signal is output onto VOUT.
D5, D4	Sync strip select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify from which analog input sync information is to be detected. The selected signal is output onto CEXT1. It is converted to TTL levels and output onto CSYNC*.
D3, D2	Sync detect level select (00) 50 mV (01) 75 mV (10) 100 mV (11) 125 mV	These bits specify how much above the sync tip to slice CEXT2 for sync detection.
D1, D0	reserved (logical zero)	

IOUT Data Registers

These two 8-bit registers specify the output current on the IOUT0 and IOUT1 outputs, from 0 mA ($00) to 1 mA ($FC). The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must be programmed to be a logical zero.

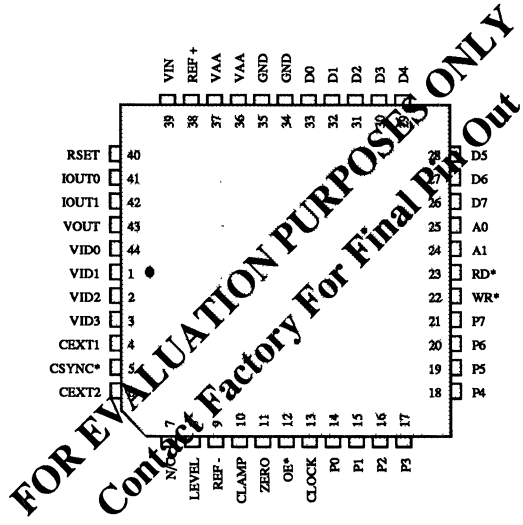
These registers may be written to or read by the MPU at any time, and are not initialized. D0 is the least significant bit.

Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full scale adjust control. An external 1200-ohm resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figures 1 and 2.
IOUT0, IOUT1	Current outputs. The amount of output current is specified by the IOUT data registers. External 1000-ohm resistors are typically connected between each pin and GND. See Figures 1 and 2. The relationship between full-scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (ohms)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M-ohm resistor must also be connected between CEXT2 and GND. See Figures 1 and 2.
A/D Functions	
REF+	Top of resistor ladder (voltage input). REF+ sets the VIN voltage level that generates $FF from the A/D converter. A decoupling capacitor is NOT recommended on REF+.
REF-	Bottom of resistor ladder (voltage input). REF- sets the VIN voltage level that generates $00 from the A/D converter.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. ZERO is latched on the rising edge of CLOCK. During zeroing cycles, P0 - P7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN input is forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should always be a logical zero.
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be for DC restoration while CLAMP is a logical one. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.
Input Selection Functions	
VIN	A/D converter input. The analog signal to be digitized should be connected to this analog input pin. It may be either DC- or AC-coupled to the video signal being digitized.
VID0 - VID3, VOUT	Analog inputs and analog output. VID0 - VID3 are connected to the video signals to be digitized. The signal selected to be digitized is output onto VOUT.
Timing Functions	
CLOCK	Clock input (TTL compatible). CLOCK should be driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected on the VID0 - VID3 input specified by the command register, converted to TTL levels, and output onto this pin. It is output asynchronously to the clock and there are no pipeline delays.

Pin Descriptions (continued)

Pin Name	Description
Digital Control Functions	
P0 - P7	Digitized video data outputs (TTL compatible). Digitized video data is output onto these pins following the rising edge of CLOCK. P0 is the least significant bit. They are three-stated if OE* is a logical one.
OE*	Output enable control input (TTL compatible). A logical one three-states the P0 - P7 outputs asynchronously to CLOCK.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0 - D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0 - D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0 - D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0, A1	Address control inputs (TTL compatible). A0 and A1 are used to specify the operation the MPU is performing as indicated in Table 1. They are latched on the falling edge of either RD* or WR*.
Power and Ground	
VAA	+5v power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt251 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt251 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt251, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt251.

Power Planes

The Bt251 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt251.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt251 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

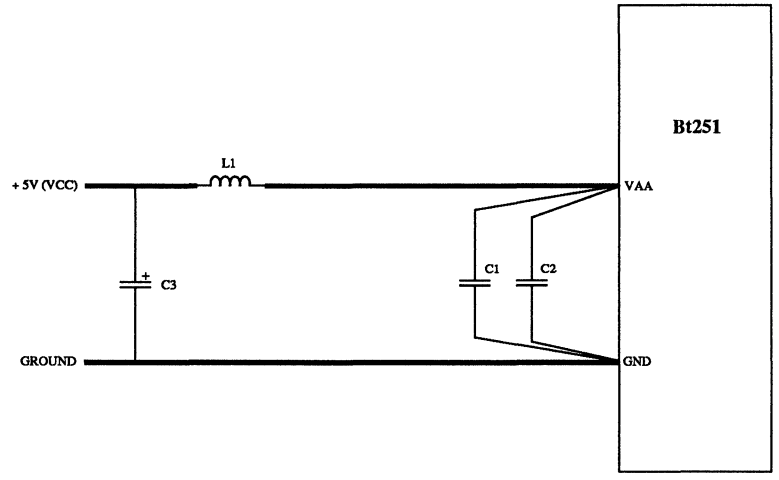
Each group of VAA pins should have a 0.1 µF ceramic bypass capacitor to GND, located as close as possible to the device.

Signal Interconnect

The digital signals of the Bt251 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt251.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Zeroing

As the comparators on the Bt251 must be periodically zeroed, it is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt251 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt251.

As long as the recommended zeroing interval is maintained, the Bt251 will meet linearity specifications. The longer between zeroing intervals, the more the linearity error increases.

AC-Coupled Vs. DC-Coupled VIN

VIN may be either AC- or DC-coupled to the video signal, as shown in Figures 1 and 2. The 50-ohm resistor provides isolation from any clock kickback noise on Vin from being coupled onto the video signal. The 75-ohm resistors to ground provide the typical 75-ohm termination required by video signals.

Increasing the Resolution of DACs

With a 1000-ohm resistor connected between each DAC output (IOUT0, IOUT1) and GND, the resolution of the ladder adjustment is 16 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 4 shows a circuit that allows adjustment of the REF+ inputs from 0.714v to 1v with 4.5 mV resolution. With the DAC data = $00, 0.714v is output; if the DAC data = $FC, 1v is output.

As the recommended maximum DAC output is 1 mA, if a 0.286v adjustable range is desired, R1 || R2 must equal 286 ohms. The minimum output voltage desired determines the ratio of R1 and R2:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF-) may be adjusted from 0v to 0.287v with 4.5 mV resolution by using a 287-ohm resistor to ground rather than a 1000-ohm resistor. As long as the minimum range is 0v, the resistor to ground may be used to adjust the total range, and thus the resolution.

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Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0v	0.9v - 1.1v
RS-170 w/sync	1.4v	1.2v - 1.6v
RS-170A w/o sync	1.0v	0.9v - 1.1v
RS-170A w/sync	1.4v	1.0v - 1.8v
RS-343A w/o sync	0.7v	0.6v - 0.85v

Table 2. Video Signal Tolerances.

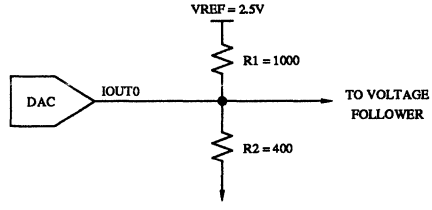

Figure 4. Increasing DAC Output Resolution.

Application Information (continued)

Driving REF+ and REF-

As REF+ and REF- should be driven by a high AC impedance source, a 100-ohm resistor should be placed between REF+ and the output of the voltage follower and between REF- and the output of the voltage follower, as shown in Figure 2.

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2v, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2v input range.

When digitizing with a full scale range less than 0.7v, the Bt251's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting REF+ equal to 0.6v and REF- equal to 0v, 0.6v video signals may be digitized; however the integral linearity error will increase to about ± 1.8 LSB. The SNR will decrease by about 3 dB. With REF+ equal to 0.5v and REF- equal to 0v, 0.5v video signals may be digitized with an IL error of about ± 2 LSB. The SNR will decrease by about 4 dB.

Output Noise (DC vs. SNR)

Measurement of A/D output noise under DC input conditions is not indicative of performance under video operating conditions. The SNR measurement more truly reflects device performance in video applications.

Uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2" VCR.

PC Board Sockets

It is recommended that the Bt251 not be used with a socket, and have a 0.15" standoff. Use of a socket increases the output noise due to digital output ringing.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Voltage References					
Top	REF+	0.7	1	2.0	Volts
Bottom	REF-	0	0	1.3	Volts
Difference (Top - Bottom)		0.7	1	1.2	Volts
VID0 - VID3 Input Amplitude		0.7			Volts
VIN Input Amplitude		0.7	1	1.2	Volts
VIN Input Range			REF- to REF+		Volts
LEVEL Input Voltage		GND - 0.3	REF-	REF+	Volts
Zeroing Interval			60	150	µS
Ambient Operating Temperature	TA	0		+ 70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Input Voltage	VIN	GND - 0.3		VAA + 0.5	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (note 1)	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C.
A/D Coding					Binary
No Missing Codes			guaranteed		
VIN Analog Input (note 2)					
CLAMP = 0					
Input Impedance	RIN	10			M ohms
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
VID0 - VID3 Analog Inputs (note 3)					
Input Impedance to VOUT					
Input Selected			100		Ohms
Input Deselected			10		M ohms
Input Capacitance			tbd		pF
REF+ Reference Input					
Input Current			1		mA
Input Impedance			1		K ohms
Clock Kickback (note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance	CIN		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (IOH = -50 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.8	Volts
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0 and IOUT1 Outputs					
DAC Output Current		0		1	mA
DAC Output Impedance			100		K ohms
DAC Output Capacitance			20		pF
DAC Output Compliance		-1		+2	Volts
Power Supply Rejection Ratio (not including reference)	PSRR		tbd		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float.

Note 1: Best-fit linearity. Averaged value evaluated using a closed loop system (see Bt208 linearity test circuit). Linearity is tested with RAM transparent.

Note 2: LEVEL = GND.

Note 3: VOUT connected to GND.

Note 4: Measurement of noise coupled onto VIN due to clocking (Rs = 75 ohms). Typically occurs over a 5 ns interval.

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Vin* (v)	P0 - P7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

*with REF+ = 1.000v and REF- = 0.000v. Ideal center values. 1 LSB = 3.9063 mV. RAM transparent.

Table 3. A/D Coding.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate (note 1)	Fs			15	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time Clock Low Time Clock High Time	1 2 3	66.7 35 20			ns ns ns
P0 - P7 Output Delay OE* Asserted to P0 - P7 Valid OE* Negated to P0 - P7 3-Stated	4 5 6			tbd tbd tbd	ns ns ns
ZERO Setup Time ZERO Hold Time ZERO, CLAMP High Time (note 2)	7 8	tbd tbd 1			ns ns Clock
Aperture Delay Aperture Jitter Full Power Input Bandwidth	9 BW	 6	10 50		ns ps MHz
Transient Response (note 3) Overload Recovery (note 4) Zero Recovery Time (note 5)				1 1 1	Clock Clock Clock
RMS Signal to Noise Ratio Fin = 4.2 MHz, Fs = 10.7 MHz Fin = 4.2 MHz, Fs = 14.32 MHz Fin = 2.75 MHz, Fs = 6.75 MHz Fin = 5.75 MHz, Fs = 13.5 MHz	SNR		 43 42 44 41		 dB dB dB dB
Analog Multiplexer Crosstalk All Hostile Crosstalk Single Channel Crosstalk Adjacent Input Crosstalk			 tbd tbd tbd		 dB dB dB
IOUT0, IOUT1 Settling Time to ± 1 LSB			100		ns
Differential Gain Error (note 6) Differential Phase Error (note 6)	DG DP		2 1		% Degree
Supply Current (note 7) (Excluding REF+)	IAA		150	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
A0, A1 Setup Time	10	tbd			ns
A0, A1 Hold Time	11	tbd			ns
RD*, WR* High Time	12	tbd			ns
RD* Asserted to Data Bus Driven	13	tbd			ns
RD* Asserted to Data Valid	14			tbd	ns
RD* Negated to Data Bus 3-Stated	15			tbd	ns
WR* Low Time	16	tbd			ns
Write Data Setup Time	17	tbd			ns
Write Data Hold Time	18	tbd			ns
Pipeline Delay		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0 - D7, P0 - P7, CSYNC* output load ≤ 50 pF. VOUT, IOUT0, IOUT1 output load ≤ 25 pF.

Note 1: Typical error rate of 10^{-6} at 15 MHz.

Note 2: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.

Note 3: For full-scale step input, full accuracy attained in specified time.

Note 4: Time to recover to full accuracy after a > 1.2v input signal.

Note 5: Time to recover to full accuracy following a zero cycle.

Note 6: 4x NTSC subcarrier, unlocked.

Note 7: IAA (typ) at VAA = 5.0v, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25v, Fin = 7.5 MHz, Fs = 15 MHz.

Timing Waveforms

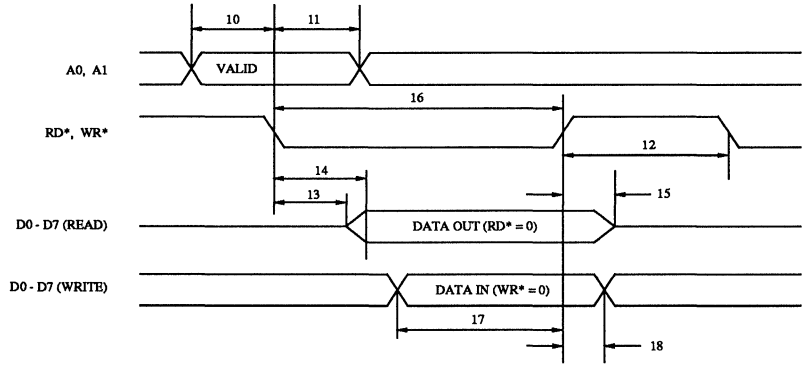

Figure 5. MPU Read/Write Timing.

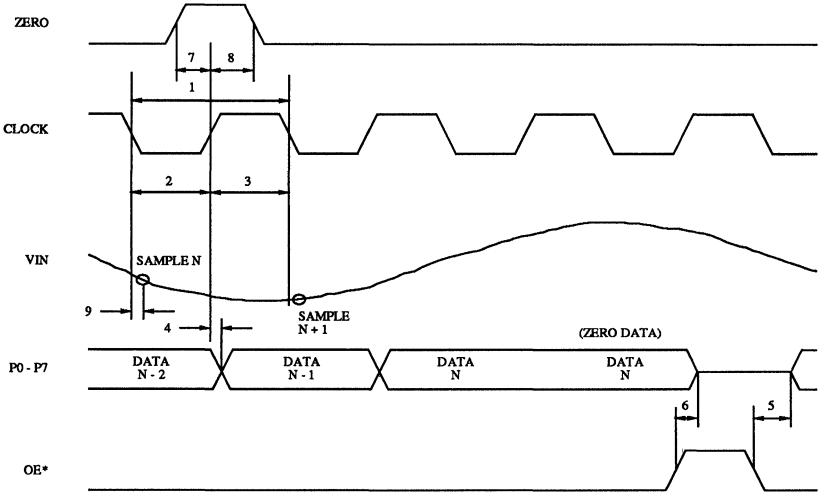

Figure 6. Video Input/Output Timing.

Test Circuits

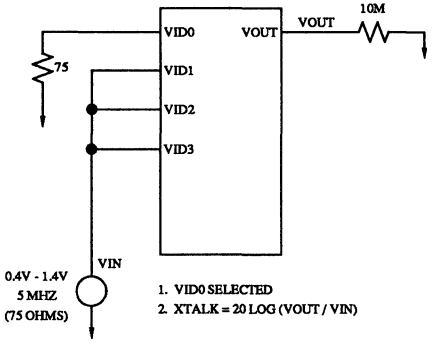

Figure 7. All Hostile Crosstalk Test Circuit.

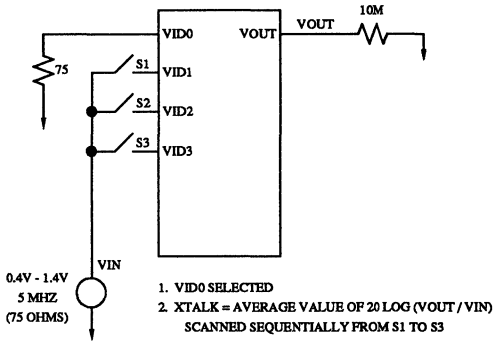

Figure 8. Single Channel Crosstalk Test Circuit.

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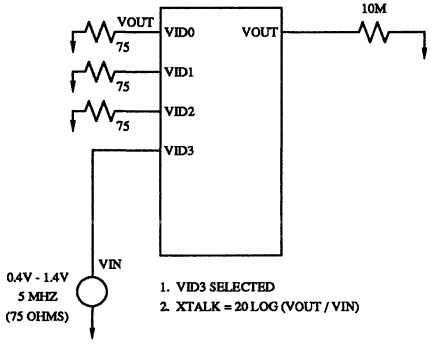
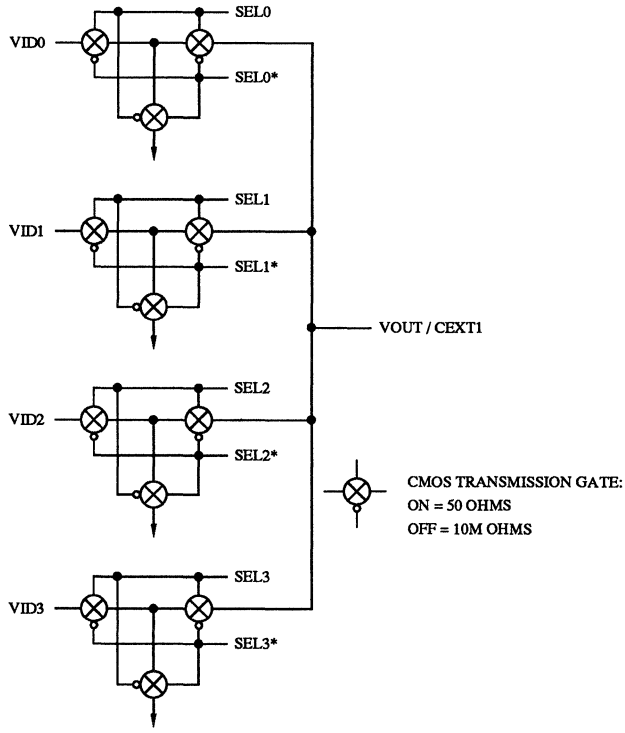


Figure 9. Adjacent Input Crosstalk Test Circuit.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt251KPJ	44-pin Plastic J-Lead	0° to +70° C.

Analog Multiplexer Circuit



Bt253

15 MSPS

Monolithic CMOS

Triple Channel

8-Bit Image Digitizer

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Distinguishing Features

- Three 8-bit Video A/D Converters
- 2 Sets Software Selectable Analog Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5v CMOS Monolithic Construction
- 84-pin PLCC Package
- Typical Power Dissipation: 1 W

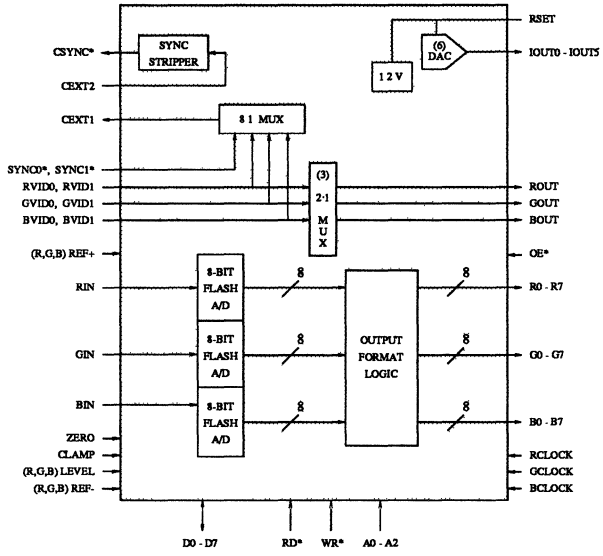
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt208, Bt251
- Bt261

Functional Block Diagram



Product Description

The Bt253 Image Digitizer is designed to digitize three channels of video signals, such as RGB, YIQ, YUV, etc., generating up to 24 bits of color pixel information. The architecture also supports single channel digitization of RS-343A, NTSC, PAL, and SECAM video signals, generating 8 bits of gray-scale pixel information.

24-bit true-color, 15-bit true-color, 8-bit true-color, and 8-bit pseudo-color modes are supported. A standard MPU interface is provided for accessing various control functions.

Six analog inputs (2 for each A/D) are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking. A TTL-compatible composite sync signal is output to interface to genlock circuitry. Two additional sync inputs are also provided to support red, green, blue, sync video interfaces.

Optional MPU controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D converters. Zeroing and clamping signals are available to control the A/D timing for application specific timing. The clamping levels are externally set via the red, green, and blue LEVEL pins.

Each A/D converter has its own clock input, top/bottom references, and LEVEL pin.

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Circuit Description

MPU Interface

As shown in the functional block diagram, the Bt253 supports a standard MPU interface (D0 - D7, RD*, WR*, and A0 - A2). MPU operations are asynchronous to the clocks.

A0 - A2 address the internal registers, as shown in Table 1.

Flash A/D Converters

The Bt253 uses three 8-bit flash A/D converters to digitize the video signals. Each A/D digitizes analog signals in the range of REF- ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF-) to $FF (Vin ≥ REF+).

Each A/D converter has it's own top and bottom reference: RREF+ and RREF- for the red A/D, GREF+ and GREF- for the green A/D, and BREF+ and BREF- for the blue A/D. Each A/D converter also has it's own clock input: RCLOCK for the red A/D, GCLOCK for the green A/D, and BCLOCK for the blue A/D.

RIN, GIN, and BIN may be either DC- or AC-coupled to the video signals. If AC-coupled, the CLAMP and (R,G,B) LEVEL controls may be used to DC restore the video signals.

Figure 1 shows the internal A/D architecture in detail.

Analog Signal Selection

The Bt253 supports two analog input sources for each A/D converter: RVID0 and RVID1, GVID0 and GVID1, and BVID0 and BVID1. The MPU specifies which ones are to be digitized via the command register. Any required gain to standard video levels should be done prior to driving the xVID0 and xVID1 inputs to ensure reliable sync detection.

The selected video signals are output onto ROUT, GOUT, and BOUT. ROUT, GOUT, and BOUT may be connected directly to RIN, GIN, and BIN, respectively, if no filtering or gain of the video signal is required.

If digitizing a video signal containing color subcarrier information (such as RS-170A, PAL, or SECAM) to generate 8 bits of gray-scale information, the green A/D converter should be used and the Bt253 configured for the pseudo-color mode. A filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A lowpass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on ROUT, GOUT, and BOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be connected together through the equivalent of 200 ohms.

A2, A1, A0	Addressed by MPU
000	command register
001	IOUT0 data register
010	IOUT1 data register
011	IOUT2 data register
100	IOUT3 data register
101	IOUT4 data register
110	IOUT5 data register
111	reserved

Table 1. Register Addressing.

Circuit Description (continued)

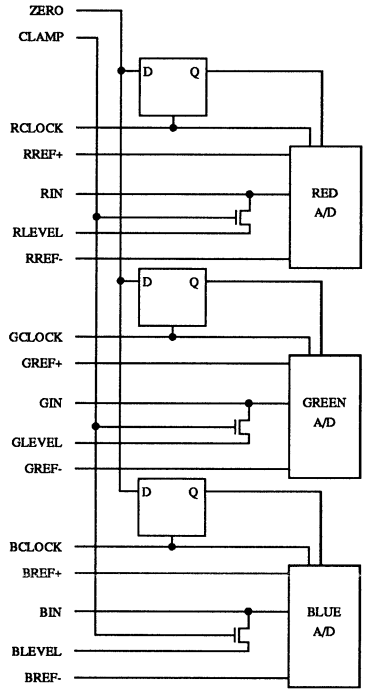


Figure 1. Internal A/D Architecture.

Circuit Description (continued)

A/D Reference Generation

Typically, RREF+, GREF+, and BREF+ are connected to a 0.7v to 1.2v reference, while RREF-, GREF-, and BREF- are connected to GND, as shown in Figure 2. This mode of operation may be used when the only operation is to digitize video signals with an amplitude of 0.7v to 1.2v with no adjustment of gain or offset.

The gain and offset of the video signals may effectively be done via the MPU adjustable outputs IOUT0 - IOUT5, as shown in Figure 3. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented.

IOUT0 - IOUT5 are current outputs (0 to 1 mA) generated by six 6-bit D/A converters. 1000-ohm resistors to GND generate a 0v to 1v level that drives the (R,G,B)REF+ and (R,G,B)REF- inputs through voltage-followers. The top and bottom references may thus be adjusted with 16 mV resolution.

A/D Zeroing

The ZERO input is used to zero the comparators, and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the R0 - R7, G0 - G7, and B0 - B7 outputs are not updated. They retain the data loaded before the ZERO cycle.

Note that each A/D converter uses its own clock to latch the ZERO signal. Thus, ZERO must be asserted for at least one clock cycle of the slowest clock.

A/D Input Clamping

If RIN, GIN, and BIN are AC-coupled to the video signals, the CLAMP and (R,G,B) LEVEL controls may be used to DC restore the video signals. While CLAMP is a logical one, the video signals are clamped to the voltage level present on the (R,G,B) LEVEL pins.

If RIN, GIN, and BIN are DC-coupled to the video signals, all three LEVEL pins should float or CLAMP should always be a logical zero.

Sync Detect Circuitry

The Bt253 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clocks and there are no pipeline delays.

The MPU specifies from which input to detect sync. The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The MPU selects how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

Two additional sync inputs are provided (SYNC0* and SYNC1*) to support red, green, blue, sync systems. SYNC0* and SYNC1* may be either TTL or normal video signal levels.

Color Output Modes

The Bt253 outputs several modes of color information, as shown in Table 2.

R0 - R7, G0 - G7, and B0 - B7 are three-stated while OE* is a logical one.

Circuit Description (continued)

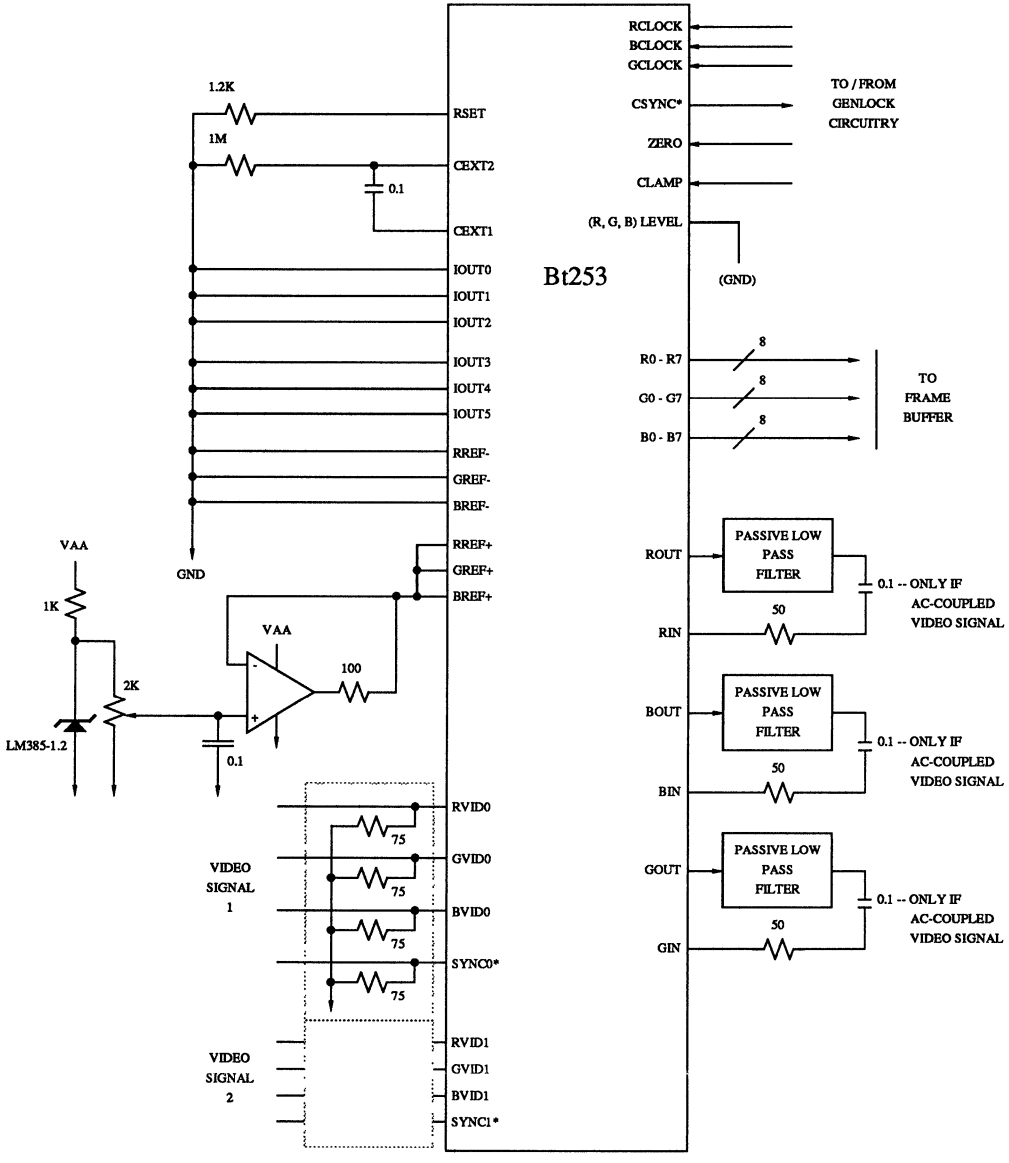


Figure 2. Typical Bt253 External Circuitry. (Fixed Top and Bottom References)

Circuit Description (continued)

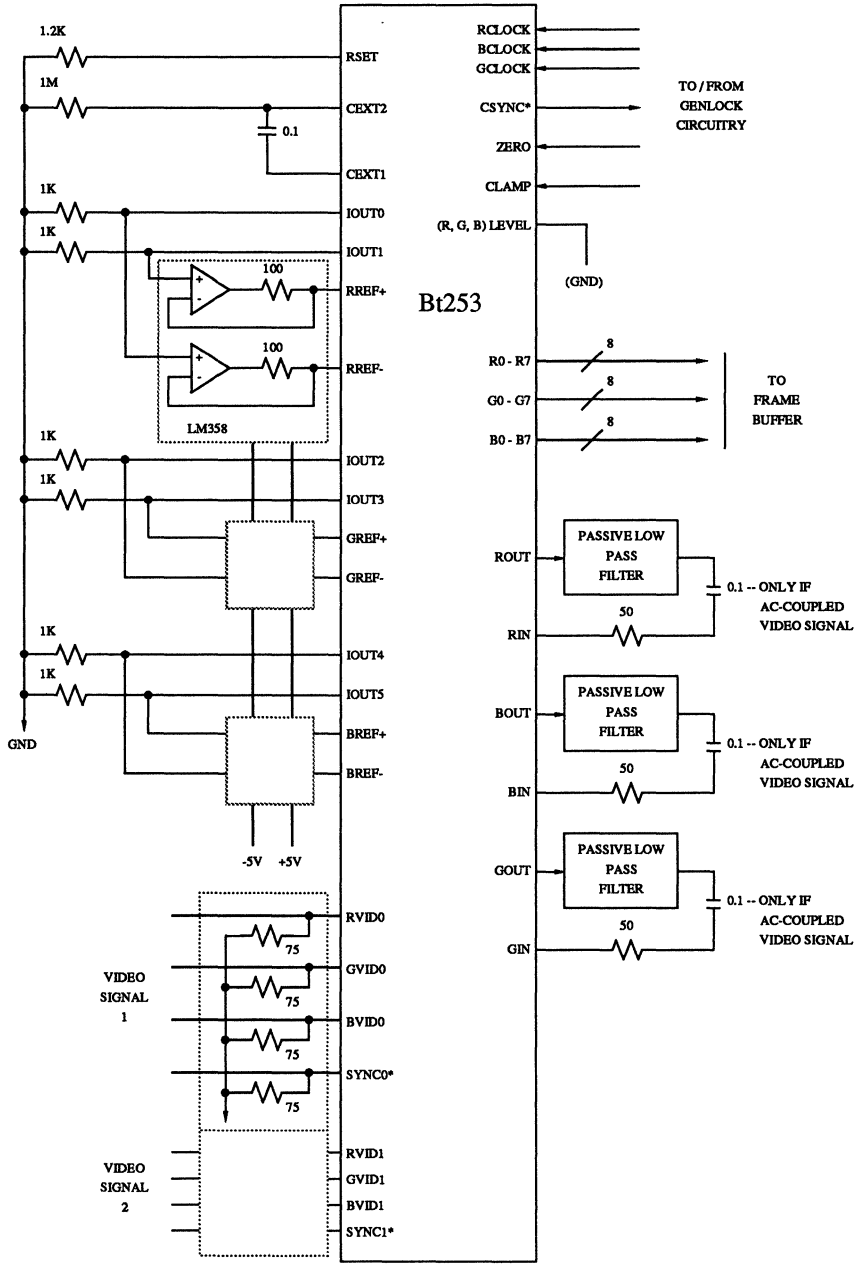


Figure 3. Typical Bt253 External Circuitry. (Variable Top and Bottom References)

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7	Digitize select (0) xVID0 (1) xVID1	This bit specifies which analog input is to be digitized. The selected signals are output onto ROUT, GOUT, and BOUT.
D6 - D4	Sync select (000) RVID0 (001) RVID1 (010) GVID0 (011) GVID1 (100) BVID0 (101) BVID1 (110) SYNC0* (111) SYNC1*	Composite sync information detected on the selected input is output onto CSYNC*.
D3, D2	Color output select (00) 24-bit true-color (01) 15-bit true-color (10) 8-bit true-color (11) 8-bit pseudo-color	Color output mode select. See Table 2. In mode (11), the red and blue A/D converters are ignored.
D1	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register.
D0	Sync detect level select (0) 50 mV (1) 125 mV	This bit specifies how much above the sync tip to slice CEXT2 for sync detection.

Internal Registers (continued)

IOUT Data Registers

These six 8-bit registers specify the output current on the IOUT0 - IOUT5 outputs, from 0 mA ($00) to 1 mA ($FC). The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must programmed to be a logical zero.

These registers may be written to or read by the MPU at any time, and are not initialized. D0 is the least significant bit.

	24-Bit True Color	15-Bit True Color	8-Bit True Color	8-Bit Pseudo Color
Output Pins	Mode (00)	Mode (01)	Mode (10)	Mode (11)
R7	R7	0	R7	G7
R6	R6	R7	R6	G6
R5	R5	R6	R5	G5
R4	R4	R5	G7	G4
R3	R3	R4	G6	G3
R2	R2	R3	G5	G2
R1	R1	G7	B7	G1
R0	R0	G6	B6	G0
G7	G7	G5	R7	G7
G6	G6	G4	R6	G6
G5	G5	G3	R5	G5
G4	G4	B7	G7	G4
G3	G3	B6	G6	G3
G2	G2	B5	G5	G2
G1	G1	B4	B7	G1
G0	G0	B3	B6	G0
B7	B7	0	R7	G7
B6	B6	0	R6	G6
B5	B5	0	R5	G5
B4	B4	0	G7	G4
B3	B3	0	G6	G3
B2	B2	0	G5	G2
B1	B1	0	B7	G1
B0	B0	0	B6	G0

Table 2. Color Output Configurations.

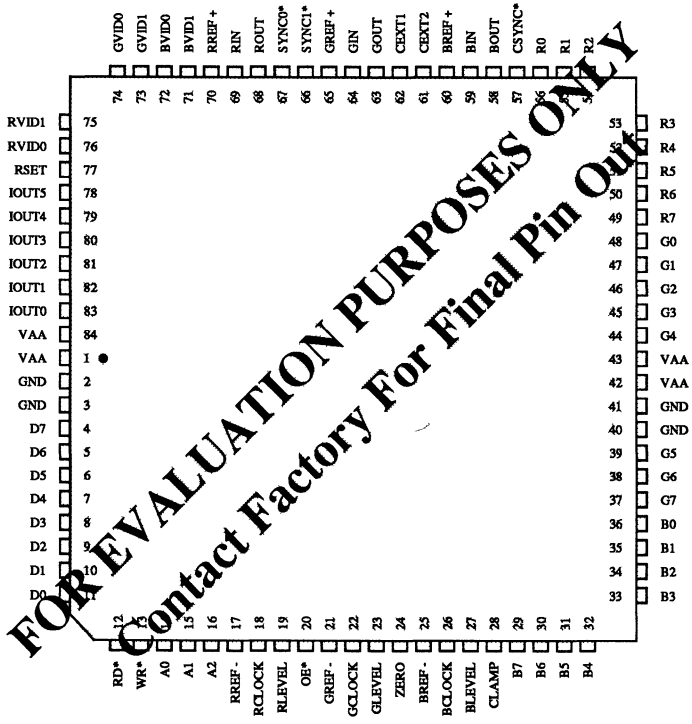
Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full scale adjust control. An external 1200-ohm resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figures 2 and 3.
IOUT0 - IOUT5	Current outputs. The amount of output current is specified by the IOUT data registers. External 1000-ohm resistors are typically connected between these pins and GND. See Figures 2 and 3. The relationship between full scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (ohms)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M-ohm resistor must also be connected between CEXT2 and GND.
A/D Functions	
RREF+, GREF+, BREF+	Red, green, and blue top of resistor ladder (voltage input). These set the Vin voltage level that generates $FF from the appropriate A/D converter. Decoupling capacitors are NOT recommended for the REF+ pins.
RREF-, GREF-, BREF-	Red, green, and blue bottom of resistor ladder (voltage input). These set the Vin voltage level that generates $00 from the appropriate A/D converter.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. The red A/D latches ZERO on the rising edge of RCLOCK, the green A/D latches ZERO on the rising edge of GCLOCK, and the blue A/D latches ZERO on the rising edge of BCLOCK. During zeroing cycles, R0 - R7, G0 - G7, and B0 - B7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the RIN, GIN, and BIN inputs are forced to the voltage level on the (R, G, B) LEVEL pins to perform DC restoration of the video signals. In applications where RIN, GIN, and BIN are DC-coupled to the video signals, the LEVEL pins should float or CLAMP should always be a logical zero. CLAMP is asynchronous to the clocks.
RLEVEL, GLEVEL, BLEVEL	Red, green and blue level control inputs (voltage inputs). These inputs are used to specify what voltage level is to be used for DC restoration while CLAMP is a logical one. In applications where RIN, GIN, and BIN are DC-coupled to the signals, the LEVEL pins should float or CLAMP should always be a logical zero.
Input Selection Functions	
RIN, GIN, BIN	A/D converter inputs. The analog signals to be digitized should be connected to these analog input pins.
RVID0, RVID1, ROUT	Red channel analog inputs and analog output. RVID0 and RVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto ROUT.
GVID0, GVID1, GOUT	Green channel analog inputs and analog output. GVID0 and GVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto GOUT.

Pin Descriptions (continued)

Pin Name	Description
BVID0, BVID1, BOUT	Blue channel analog inputs and analog output. BVID0 and BVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto BOUT.
Timing Functions	
RCLOCK, GCLOCK, BCLOCK	Clock inputs (TTL compatible). Each clock input should be driven by a dedicated TTL buffer to minimize sampling jitter. The clock signals, if not the same clock rate, should be synchronous and a multiple of each other.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected on the xVID0 or xVID1 input (as specified by the command register), converted to TTL levels, and output onto this pin. SYNC0* or SYNC1* may also be selected to be output onto this pin. It is output asynchronously to the clocks and there are no pipeline delays.
SYNC0*, SYNC1*	Sync inputs. Sync information may be input via these pins and output onto CSYNC*. SYNC0* and SYNC1* may be either TTL or normal video signal levels.
Digital Control Functions	
R0 - R7, G0 - G7, B0 - B7	Digitized video data outputs (TTL compatible). R0 - R7 are output following the rising edge of RCLOCK, G0 - G7 are output following the rising edge of GCLOCK, and B0 - B7 are output following the rising edge of BCLOCK. They are three-stated if OE* is a logical one. R0, G0, and B0 are the least significant bits.
OE*	Output enable control input (TTL compatible). A logical one three-states R0 - R7, G0 - G7, and B0 - B7 asynchronously to the clocks.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0 - D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0 - D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0 - D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0 - A2	Address control inputs (TTL compatible). A0 - A2 address the internal registers as shown in Table 1. They are latched on the falling edge of RD* or WR*.
Power and Ground	
VAA	+5v power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected as close to the device as possible.

Pin Descriptions (continued)



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PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt253 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt253 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt253, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt253.

Power Planes

The Bt253 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within three inches of the Bt253.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt253 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

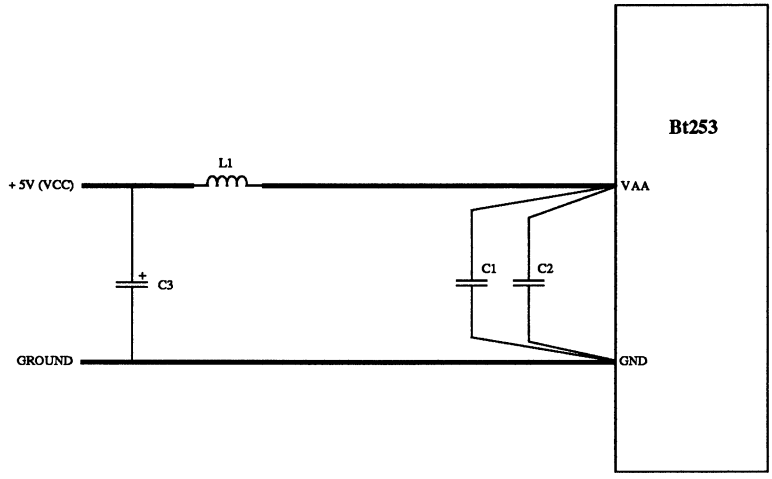
Each group of VAA pins should have a 0.1 μF ceramic bypass capacitor to GND, located as close as possible to the device.

Signal Interconnect

The digital signals of the Bt253 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt253.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

Zeroing

As the comparators on the Bt253 must be periodically zeroed, it is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt253 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt253.

As long as the recommended zeroing interval is maintained, the Bt253 will meet linearity specifications. The longer between zeroing intervals, the more the linearity error increases.

AC-Coupled Vs. DC-Coupled Inputs

RIN, GIN, and BIN may be either AC- or DC-coupled to the video signal, as shown in Figures 2 and 3. The 50-ohm resistors provide isolation from any clock kickback noise on RIN, GIN, and BIN from being coupled onto the video signal. The 75-ohm resistors to ground provide the typical 75-ohm termination required by video signals.

Increasing the Resolution of DACs

With a 1000-ohm resistor connected between each DAC output (IOUTx) and GND, the resolution of the ladder adjustment is 16 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 5 shows a circuit that allows adjustment of the REF+ inputs from 0.714v to 1v with 4.5 mV resolution. With the DAC data = $00, 0.714v is output; if the DAC data = $FC, 1v is output.

As the maximum DAC output is 1 mA, if a 0.286v adjustable range is desired, R1 || R2 must equal 286 ohms. The minimum output voltage desired determines the ratio of R1 and R2:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF-) may be adjusted from 0v to 0.287v with 4.5 mV resolution by using a 287-ohm resistor to ground rather than a 1000-ohm resistor. As long as the minimum range is 0v, the resistor to ground may be used to adjust the total range, and thus the resolution.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0v	0.9v - 1.1v
RS-170 w/sync	1.4v	1.2v - 1.6v
RS-170A w/o sync	1.0v	0.9v - 1.1v
RS-170A w/sync	1.4v	1.0v - 1.8v
RS-343A w/o sync	0.7v	0.6v - 0.85v

Table 3. Video Signal Tolerances.

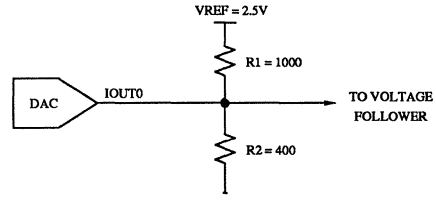


Figure 5. Increasing DAC Output Resolution.

Application Information (continued)

Driving REF+ and REF-

As (R,G,B)REF+ and (R,G,B)REF- should be driven by a high AC impedance source, a 100-ohm resistor should be placed between REF+ and the output of the voltage follower and between REF- and the output of the voltage follower, as shown in Figure 3.

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2v, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2v input range.

When digitizing with a full scale range less than 0.7v, the Bt253's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting REF+ equal to 0.6v and REF- equal to 0v, 0.6v video signals may be digitized; however the integral linearity error will increase to about ± 1.8 LSB. The SNR will decrease by about 3 dB. With REF+ equal to 0.5v and REF- equal to 0v, 0.5v video signals may be digitized with an IL error of about ± 2 LSB. The SNR will decrease by about 4 dB.

Output Noise (DC vs. SNR)

Measurement of A/D output noise under DC input conditions is not indicative of performance under video operating conditions. The SNR measurement more truly reflects device performance in video applications.

Uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2" VCR.

PC Board Sockets

It is recommended that the Bt253 not be used with a socket, and have a 0.15" standoff. Use of a socket increases the output noise due to digital output ringing.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Voltage References					
Top	xREF+	0.7	1	2.0	Volts
Bottom	xREF-	0	0	1.3	Volts
Difference (Top - Bottom)		0.7	1	1.2	Volts
VID0 - VID3 Input Amplitude		0.7			Volts
(R,G,B) IN Input Amplitude		0.7	1	1.2	Volts
(R,G,B) IN Input Range			REF- to REF+		Volts
(R,G,B) LEVEL Input Voltage		GND - 0.3	REF-	REF+	Volts
Zeroing Interval			60	150	µS
Ambient Operating Temperature	TA	0		+ 70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Input Voltage	RIN, GIN, BIN	GND - 0.3		VAA + 0.5	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (note 1)	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C.
A/D to A/D Matching			tbd		%
A/D Coding					Binary
No Missing Codes			guaranteed		
(R,G,B) IN Inputs (note 2)					
CLAMP = 0					
Input Impedance	RIN	10			M ohms
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
(R,G,B) VID0,1 Inputs (note 3)					
Input Impedance to (R,G,B) OUT					
Input Selected			100		Ohms
Input Deselected			10		M ohms
Input Capacitance			tbd		pF
(R,G,B) REF+ Reference Inputs					
Input Current			1		mA
Input Impedance			1		K ohms
Clock Kickback (note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance	CIN		10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (IOH = -50 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.8 1	Volts
Three-State Current	IOZ			- 1	µA
Output Capacitance	COUT		10		pF
IOUT0 - IOUT5 Outputs					
DAC Output Current		0		1	mA
DAC Output Impedance			100		K ohms
DAC Output Capacitance			20		pF
DAC to DAC Matching				tbd	%
DAC Output Compliance		- 1.0		+ 2	Volts
Power Supply Rejection Ratio (f = 1 KHz)	PSRR		tbd		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1v and (R,G,B)REF- = GND. REF- ≤ Vin ≤ REF+, (R,G,B) LEVEL = float.

Note 1: Best-fit linearity. Averaged value evaluated using a closed loop system (see Bt208 linearity test circuit).

Note 2: (R,G,B)LEVEL = GND.

Note 3: ROUT, GOUT, BOUT connected to GND.

Note 4: Measurement of noise coupled onto RIN, GIN, and BIN due to clocking (Rs = 75 ohms). Typically occurs over a 5 ns interval.

Vin* (v)	(R,G,B) 0 - 7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

*with (R,G,B)REF+ = 1.000v and (R,G,B)REF- = 0.000v. Ideal center values.
1 LSB = 3.9063 mV.

Table 4. A/D Coding.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate (note 1)	Fs			15	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time Clock Low Time Clock High Time	1 2 3	66.7 35 20			ns ns ns
R,G,B(0 - 7) Output Delay OE* Asserted to Pixel Data Valid OE* Negated to Pixel Data 3-Stated	4 5 6			tbd tbd tbd	ns ns ns
ZERO Setup Time ZERO Hold Time ZERO, CLAMP High Time (note 2)	7 8	tbd tbd 1			ns ns Clock
Aperture Delay Aperture Jitter Full Power Input Bandwidth	9 BW	 6	tbd tbd		ns ps MHz
Transient Response (note 3) Overload Recovery (note 4) Zero Recovery Time (note 5)				1 1 1	Clock Clock Clock
RMS Signal to Noise Ratio Fin = 4.2 MHz, Fs = 10.7 MHz Fin = 4.2 MHz, Fs = 14.32 MHz Fin = 2.75 MHz, Fs = 6.75 MHz Fin = 5.75 MHz, Fs = 13.5 MHz	SNR		 tbd tbd tbd tbd		 dB dB dB dB
Analog Multiplexer Crosstalk All Hostile Crosstalk Single Channel Crosstalk Adjacent Input Crosstalk			 tbd tbd tbd		 dB dB dB
IOUT0 - IOUT5 Settling Time to ± 1 LSB			100		ns
Differential Gain Error (note 6) Differential Phase Error (note 6)	DG DP		2 1		% Degree
Supply Current (note 7) (Excluding REF+)	IAA		tbd	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
A0 - A2 Setup Time	10	tbd			ns
A0 - A2 Hold Time	11	tbd			ns
RD*, WR* High Time	12	tbd			ns
RD* Asserted to Data Bus Driven	13	tbd			ns
RD* Asserted to Data Valid	14			tbd	ns
RD* Negated to Data Bus 3-Stated	15			tbd	ns
WR* Low Time	16	tbd			ns
Write Data Setup Time	17	tbd			ns
Write Data Hold Time	18	tbd			ns
Pipeline Delay		1	1	1	Clock

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1v and (R,G,B)REF- = GND. REF- ≤ Vin ≤ REF+, (R,G,B) LEVEL = float. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0 - D7 output load ≤ 50 pF. CSYNC*, R0 - R7, G0 - G7, and B0 - B7 output load ≤ 20 pF. ROUT, GOUT, BOUT, IOUT0 - IOUT5 output load ≤ 25 pF.

Note 1: Typical error rate of 10^{-6} at 15 MHz.

Note 2: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.

Note 3: For full-scale step input, full accuracy attained in specified time.

Note 4: Time to recover to full accuracy after a > 1.2v input signal.

Note 5: Time to recover to full accuracy following a zero cycle.

Note 6: 4x NTSC subcarrier, unlocked.

Note 7: IAA (typ) at VAA = 5.0v, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25v, Fin = 7.5 MHz, Fs = 15 MHz.

Timing Waveforms

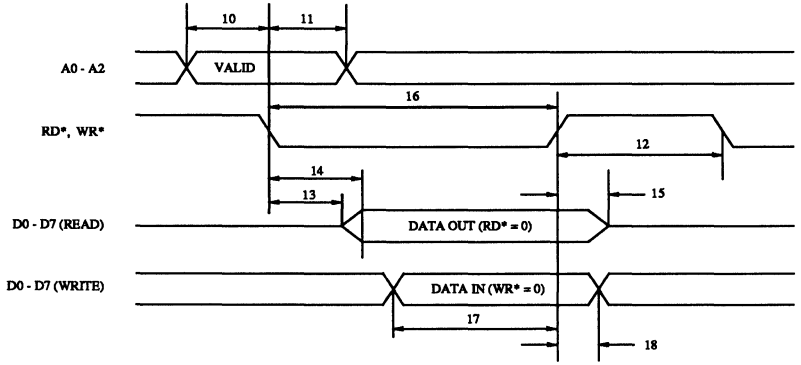


Figure 6. MPU Read/Write Timing.

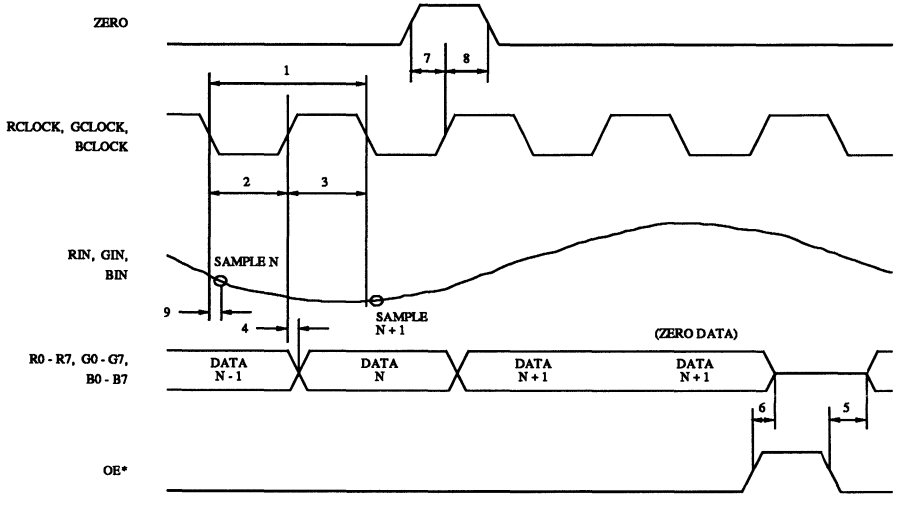


Figure 7. Video Input/Output Timing.

Test Circuits

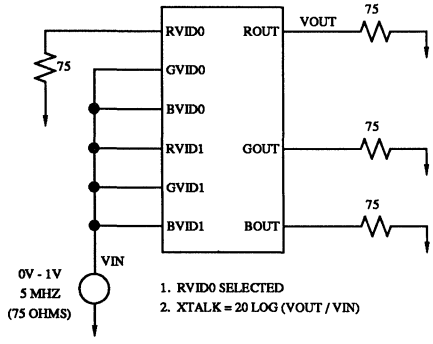


Figure 8. All Hostile Crosstalk Test Circuit.

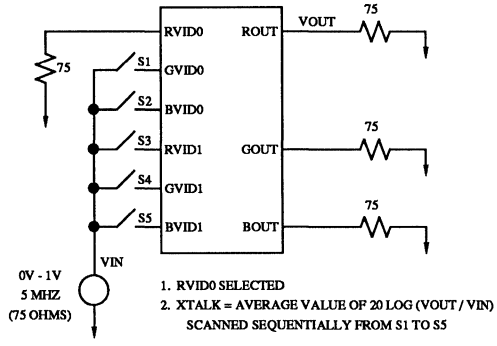


Figure 9. Single Channel Crosstalk Test Circuit.

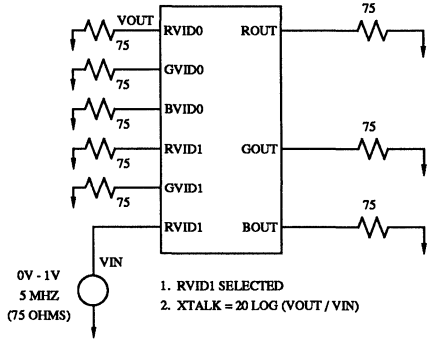
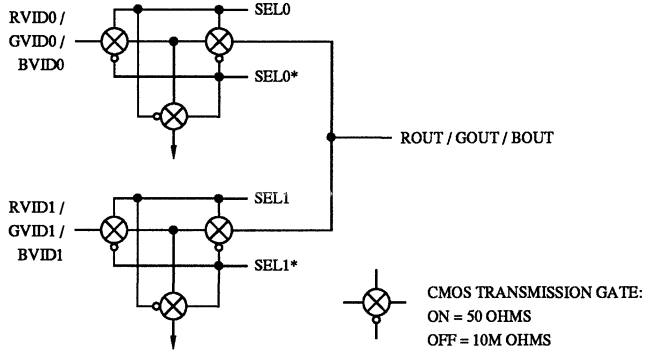


Figure 10. Adjacent Input Crosstalk Test Circuit.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt253KPJ	84-pin Plastic J-Lead	0° to +70° C.

Analog Multiplexer Circuit



Bt261

30 MHz Pixel Clock

Monolithic CMOS

HSYNC Genlock

Controller

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Distinguishing Features

- Programmable Video Timing
- Flexbile Configurations
- Programmable Sync Noise Gating
- External VCO Support
- Standard MPU Interface
- TTL Compatible
- + 5v Monolithic CMOS
- 28-pin PLCC Package
- Typical Power Dissipation: 500 mW

Applications

- Image Processing
- Video Digitizing
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt208, Bt251, Bt253

Product Description

The Bt261 HSYNC Genlock Controller is designed specifically for image capture applications.

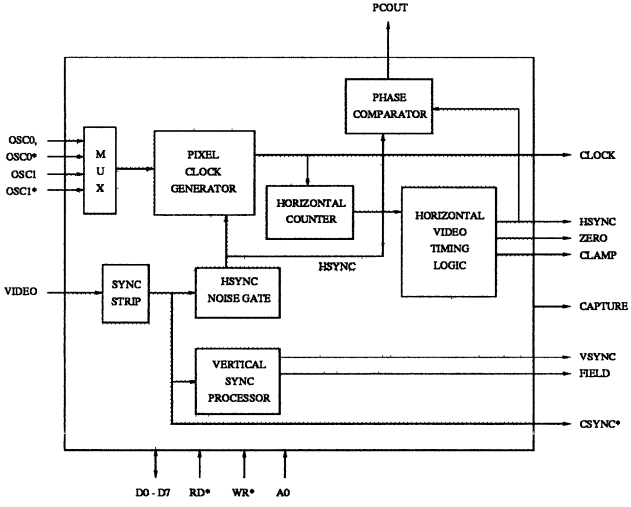
Either composite video or TTL composite sync information is input via VIDEO. An internal sync separator separates horizontal and vertical sync information. Programmable horizontal and vertical video timing enables recovery of both standard and non-standard timing information.

A high speed clock (OSC) is divided down to generate the pixel clock. CLOCK is synchronized to the falling edge of each recovered horizontal sync. The OSC inputs may be configured to be either TTL or ECL compatible. Thus, four TTL clocks may be used, two TTL clocks and one differential ECL clock, or two differential ECL clocks. The ECL clock inputs are designed to be driven by 10KH ECL using a single +5v supply. The higher the OSC clock rate, the lower the pixel clock jitter.

Alternately, an external VCO may be used in conjunction with the on-chip phase comparator for implementation of PLL-based genlock designs.

The CLAMP and ZERO outputs are programmed by the MPU for DC restoration of the video signal and zeroing the Image Digitizer or A/D converter at the appropriate time.

Functional Block Diagram



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L261001 Rev. A

Brooktree®

Bt701

CCITT T.4 and T.6 High Speed Bi-Level Image Decompression Accelerator

Advance Information

This document contains information on a product under development. Specifications are subject to change without notice.

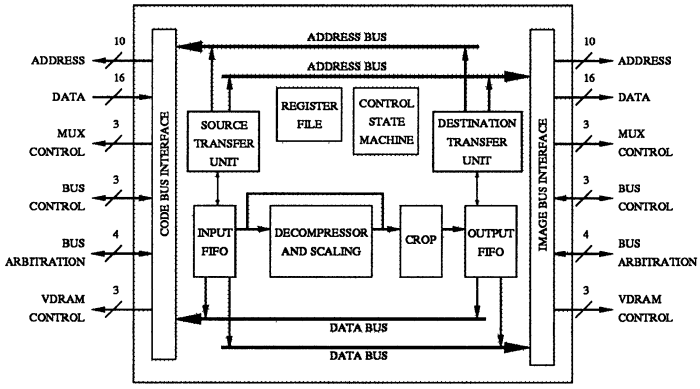
Distinguishing Features

- Provides CCITT Recommendation T.4 and T.6 Decompression Modes
- 60M bps Decompression Rate using the CCITT Standard Documents
- On-Chip Cropping of Decompressed Images
- 1:2 Scale-up and 2:1 Scale Down of Resultant Images
- Dual Port Device with Full DMA Master Interface
- Direct Pin Interface to 256K, 1M, and 4M to Standard and Video DRAMs
- BitBlt on Output for Interface Directly to Frame Buffers
- 100-pin Quad Plastic Flat Pack

Applications

- Raster Image Displays for Document Storage and Retrieval Systems.
- Laser Printers Which Handle CCITT Compressed Images.

Functional Block Diagram



Product Description

The Bt701 is a single-chip implementation of Brooktree's proprietary flow-through CCITT image decompressor architecture combined with two high performance bus interfaces and post-processing functions. The Bt701 is ideal for applications requiring high speed image decompression such as high-speed printers and displays for document storage and retrieval systems. The Bt701 is designed to increase the performance and reduce the cost of display and printer subsystems which employ CCITT Group 3 and Group 4 data compression and decompression.

The Bt701's dual ports can function as full DMA masters allowing the Bt701 to read coded image data and to write resultant raster image data without MPU intervention. Since the Bt701 is a dual port device, the source and destination for data transfers can occur on separate buses which optimizes the devices throughput.

The Bt701 provides post processing functions such as cropping the decompressed image to user specified boundaries and image scaling. The decompressed image can be scaled up by a factor of 1:2 or scaled down by a factor of 2:1.

The Bt701 can create decompressed image data at an average rate of 60 megabits-per-second. This speed makes the Bt701 ideal for interactive systems which demand fast user response times.

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8

Table of Contents

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Getting the Best Performance From Video Digital-to-Analog Converters

When using high speed analog and digital logic, proper component selection, hardware, and printed circuit board layout becomes paramount in obtaining stable and noise-free performance.

Because VIDEODACs and RAMDACs contain part digital and part analog circuitry, the analog output signal is subject to degradation from power supply noise, ground loops, radiated pickup, and magnetic coupling. The mixture of digital and analog circuitry often requires some unique solutions due to the harmonic content of the waveforms. This application note will provide guidelines for both the design engineer and the printed circuit board designer to obtain the best performance from a VIDEODAC or RAMDAC.

For additional and more detailed product-specific layout considerations, refer to the specific product datasheet.

Ground Planes

In designing a board with high speed TTL logic, one should always use a ground plane under digital signal traces to minimize radiated noise and crosstalk.

Best performance from VIDEODACs is obtained by separating this ground plane into two separate areas, which are designated as digital ground and analog ground, with at least a 1/8" gap between the areas. The digital ground plane should encompass the area under all the digital logic including signal traces leading up to the DAC but excluding any ground pins on the DAC. The analog ground plane area should include all ground pins on the DAC, all reference circuitry (external reference if used, current setting resistors, etc.), the output traces and output connector(s).

The digital and analog ground plane areas should be connected at the lowest impedance source. For highly integrated devices, such as RAMDACs, it is recommended a common ground plane be used for both the digital and analog circuitry.

Power Planes

It is good design practice for dense PCB layout with high speed logic to include a power plane layer to minimize voltage drops, aid power supply decoupling, and improve noise margins.

For best DAC performance, the power plane should be separated into two areas, designated as analog and digital power, which lay on top of the analog and digital ground planes, respectively. The digital power plane will supply power to all digital logic on the board and the analog power plane will supply all power pins of the DAC, together with power for any reference circuitry.

It is important that portions of the digital power plane area do not overlay portions of the analog ground plane area and that portions of the analog power plane area do not overlap portions of the digital ground plane. This will prevent PCB plane-to-plane noise coupling. Finally, as with the ground planes, the analog and digital power plane areas should be tied together at a single point with a wire through a ferrite bead (such as Fair-Rite part no. 2743001111).

Power and ground return connections from the board to an external power supply should be made to the digital power and ground areas to minimize the DC current flowing through the ferrite beads connecting the analog and digital areas together.

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Rev. C

Supply Decoupling

Printed Circuit Boards

A four layer sandwich structure, with power and ground planes inside the board and signals on the top and bottom of the board, provides good high frequency decoupling by virtue of the distributed capacitance between the power and ground planes.

The addition of 0.1 µF ceramic capacitors at a density of one cap per one or two square inches is usually enough for lower frequency decoupling. For best DAC performance, a 0.1 µF ceramic capacitor should be placed as close to each DAC power pin as possible for bypassing the analog power and ground plane areas. For operation beyond 75 MHz, a 0.1 µF ceramic capacitor paralleled with a 0.001 µF chip capacitor is recommended.

If the display has "ghosting" problems, additional capacitance in parallel with the power supply and COMP capacitors may fix the problem.

Breadboards

In breadboards with a ground plane and point to point wiring for power, best DAC performance is achieved with chip capacitors in the 0.01 µF to 0.1 µF range connected between the power pins and ground (see discussion about sockets on next page). Also, in breadboards with point to point power wiring, a ferrite choke such as Ferroxcube part no. VK20019/4B should be placed between the DAC power pins and the power source for the digital logic. Breadboards with a prefabricated ground plane should have this plane cut into analog and digital areas as indicated in the earlier discussion on ground planes with a single point ferrite bead connection.

Signal Interconnect

Digital Inputs

The digital input signals to the DAC should be kept isolated as possible from the analog output(s) and other analog reference inputs to the DAC. Also, the digital input signals should run over the digital ground and power plane areas of the board (see earlier discussion on power and ground planes).

To minimize data undershoot, ringing, and resultant data feedthrough noise, interconnect distances should be kept as short as possible to the DAC inputs (less than 3 inches). Data feedthrough noise is also proportional to edge speed, so in lower speed applications, use of lower speed logic will reduce data related noise on the DAC output. Also one should avoid running long clock lines to the DAC since this is another source of noise pickup.

Finally, in some applications, use of parallel termination resistors at the DAC inputs can reduce digital noise. The terminating resistors, if used, should be the low inductance film type, and should be connected to the digital ground and power planes.

Analog Inputs

The DAC should be located as close as possible to its output connector(s) to minimize noise pickup on the analog output traces. Also it is usually more difficult to control the characteristic impedance on boards and minimizing the output line length will minimize reflections due to impedance mismatch. DAC reference circuitry should be kept close to the DAC to avoid stray pickup. DAC output signals should overlay the analog ground plane and not the analog power plane to maximize high frequency power supply rejection.

It is important to note that while DACs contain circuitry to reject power supply noise, this rejection decreases with increasing frequency. As an example, with a 0.01 µF compensation capacitor the power supply rejection on CMOS DACs flattens out to 20 dB at frequencies around 1 KHz. This means that if the user powers the DAC from a 20 KHz switching power supply with 100 mv of noise at 20 KHz and harmonics, that about 10 mV of this supply noise will be on the DAC output. If the designer does not use linear supplies, close attention should be paid to reducing supply noise and consider using a three terminal regulator for DAC power.

Bypass Capacitors

Probably the single most important external components which affect the noise performance of a DAC are the capacitors used to bypass the power supplies.

It is important to realize that at the frequencies generated by the logic that one wishes to bypass, most capacitors look like inductors. For example a 0.1 μF capacitor with 1/4 inch of lead length will self resonate at around 10 MHz and beyond this frequency will look inductive. Therefore the criterion for measuring the effectiveness of a given bypass capacitor is to note its lead inductance. In addition, bypass capacitors should be installed in printed circuit boards with the very shortest leads possible consistent with reliable operation.

Probably the most effective capacitor is the distributed capacitance between power and ground planes. However this capacitance is usually too small to sustain large current surges without excessive voltage change. Ceramic chip capacitors are the next most effective for bypassing applications and are highly recommended. The drawback of using chip capacitors in PCB applications are their tendency to crack in high shock and wide temperature ranges.

The third most effective capacitor type is the radial lead ceramic capacitor. Although they tend to be 5x to 10x larger then chip capacitors, they can still be acceptable when used in conjunction with ground and power planes. Capacitors which will not be effective for DAC bypassing include electrolytic and axial lead types.

In summary, there is no one right answer to bypassing which will suit all applications. However, the principle to keep in mind is that bypassing capacitors in conjunction with the distributed power supply plane inductance will determine the effectiveness of the decoupling.

Avoiding Latch-Up

Latch-up is a common concern with CMOS devices, where power supply differentials or sequences can induce the CMOS device to draw excessive current. Observe the following precautions to avoid latch-up in CMOS devices:

1. Tie all VAA pins together at the package pins.

2. Hold all logic inputs low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants which could ring indefinitely upon power.

Attenuation Beads

Ferrite beads are recommended to suppress interference due to the fast switching times of the DACs and decoupling noise on the power plane from getting to the DAC output. Some recommended attenuation beads are Ferroxcube part no. VK20019-4B, Fair-Rite part no. 2743001111, and Phillips part no. 431202036690. Figures 1 and 2 are the impedance and typical damping curves for several Ferroxcube brand wide band chokes.

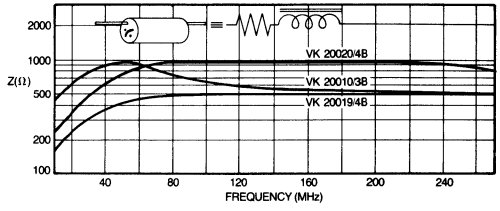

Figure 1. Impedance Curves of Wide-Band Chokes.

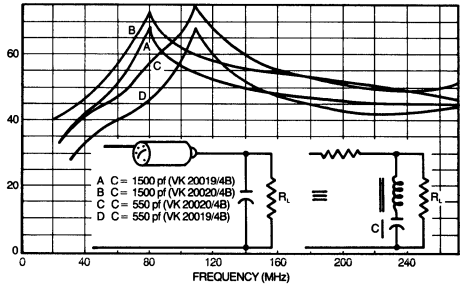

Figure 2. Typical Damping curves for VK Chokes with Additional Parallel Ceramic Capacitors.

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Note: The purpose of attenuator beads in the DAC ground path is to isolate DAC currents from high frequency system logic ground noise. The DAC must still have a low impedance return path to system ground to minimize logic threshold uncertainty and electromagnetic radiation. Bypassing the analog output sheaths to chassis ground is one method of accomplishing this.

Analog Output Protection

CMOS VIDEODACs and RAMDACs have no intrinsic protection on the analog outputs against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low capacitance, fast switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

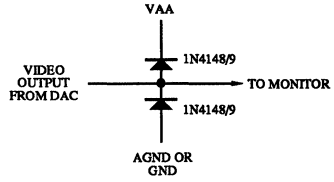

Figure 3. Output Protection Circuit.

Video DAC Essentials

A raster based graphics display terminal is comprised of a graphics controller, a frame buffer to hold the refresh data, optional color lookup tables, video DACs, and a CRT monitor. The video DAC subsystem has special requirements and performance parameters that will define the overall quality of the graphics presentation.

A simplified block diagram of a color graphics terminal using a color lookup table and three video DACs is shown in Figure 1. A monochrome or black and white monitor will use one lookup table and one video DAC. The interface to the computer system is the graphics display controller. The graphics controllers generates all the timing and interface signals to the video RAM, the color lookup tables, the video DACs and the deflection circuitry for the CRT.

The new generation of monolithic integrated circuits includes the color lookup RAM and the DAC, either as a single group or as a triple RAM and DAC combination (RAMDAC). The video amplifiers in the CRT block diagram are used to amplify the DAC output levels to the 40 to 200 volt levels required for the grids of the cathode ray tube. The deflection circuit block is used for the horizontal scanning and retrace portion of the video signal.

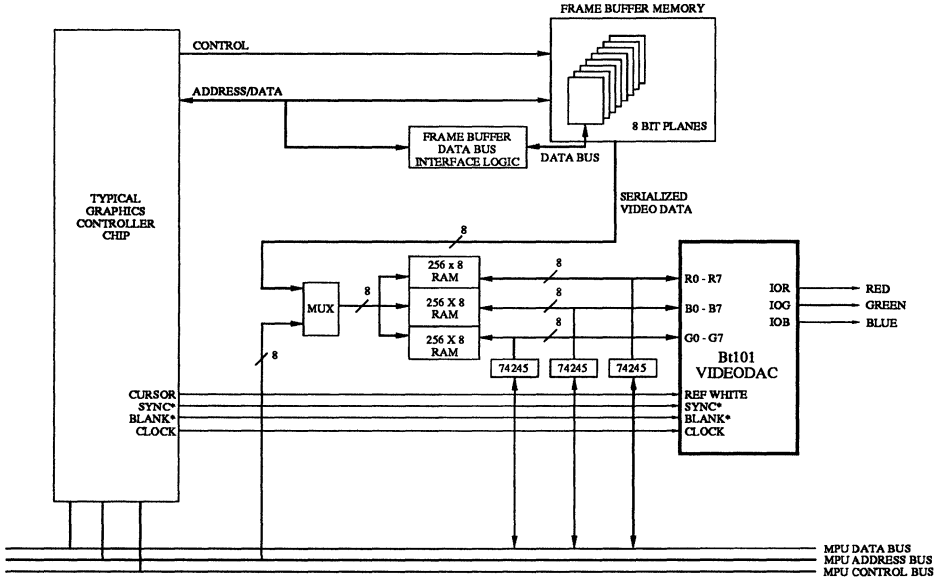

Figure 1. Simplified Block Diagram of a Color Graphics Terminal.

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Video Waveform

As raster scan video monitors are commonly used for computer graphics, a standard input signal (EIA standard RS-343A) has been defined. This standard defines the voltage level for each component of the video signal, as illustrated below in Figure 2. Note that the entire video signal is divided into three segments: sync, setup, and intensity information. A color CRT monitor requires three of these signals, one each for red, green, and blue.

In a color graphics system, the green video signal has a peak-to-peak amplitude of 1.0 volts. The red and blue video signals have a peak-to-peak amplitude of either 1.0 volts or 0.714 volts, depending on whether they have sync information present or not. Typically, sync information is present only on the green channel.

Sync information is defined to be 0.286v ± 0.05v, or 40+ IRE units. Sync is used to provide horizontal and vertical synchronization information to the CRT monitor. Separate sync monitors will have a fourth channel dedicated just to sync information.

The setup, which is the difference between the blank level and the reference black level, is defined as 7.5 ± 2.5 IRE units, or 0.054 ± 0.018 volts. At this level the CRT beam is visibly shut off, allowing it to retrace across the screen at the blank level to begin the next scan line.

DAC Bits	DAC Output Steps	Color Palette
1	2	8
2	4	64
3	8	512
4	16	4096
5	32	32,768
6	64	262,144
7	128	2,097,152
8	256	16,777,216

Table 1.

Intensity information, the interval between reference black and reference white, is assigned 92.5 ± 2.5 IRE units, or 0.660 ± 0.018 volts. It is typically composed of 16 discrete levels when 4-bit DACs are used, or 256 discrete levels when 8-bit DACs are used.

Thus, the DACs ultimately determine the number of colors available. Although many current systems use 4-bit DACs, most new designs are using 6- or 8-bit DACs to increase the number of available colors.

Table 1 illustrates the total number of available colors (color palette) for various DAC resolutions when used in a color graphics system. To substantially reduce system costs, most systems, compress data through the use of lookup table RAMs, allowing the user to display typically only 16 or 256 simultaneous colors of the total available color palette.

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

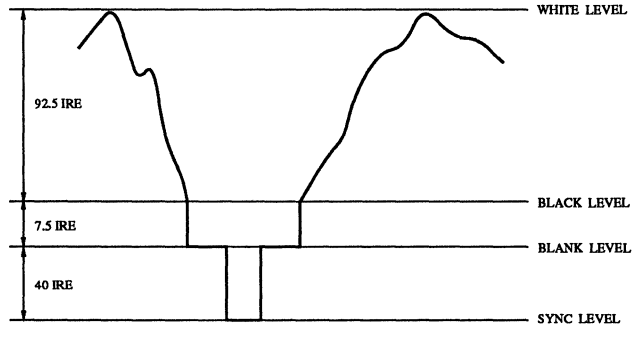

Figure 2. Standard Voltage Levels of RS-343A.

Video DAC

The video DAC converts the digital information to analog signals for the color guns in the CRT. A video DAC has several important parameters that will determine the overall performance of the display system. The update rate of the DAC sets the speed at which the pixels or dots can be displayed across the screen. The overall system speed is determined by the time it takes to scan across the screen and the time the monitor is blanked for retrace. Table 2 illustrates some of the common graphics resolutions and their video line rates.

Logic Interface

The type of logic interface can determine the overall system speed and the number of power supplies required. For a TTL type of system, the Schottky S series or the FAST series of logic must be used to obtain speeds up to 75 MHz. The regular Schottky families, such as LS or ALS, can be used in most cases up to 40 MHz. If the DAC is also compatible with CMOS logic levels, the 74HC series of gates can be used to 40 MHz. For speeds higher than 80 MHz, ECL logic is typically used. Either the 10K, 10KH, or 100K series will perform up to 125, 250, and 300 MHz respectively.

Resolution	Video Rate	Line Rate	# of 256K RAMs per Bit Plane
512 x 512	20 MHz	31.5 KHz	1
640 x 400	20 MHz	24 KHz	1
640 x 480	25 MHz	31.5 KHz	2
768 x 576	35 MHz	37 KHz	2
1024 x 800	75 MHz	52 KHz	4
1024 x 1024	95 MHz	63 KHz	4
1152 x 900	95 MHz	58 KHz	4
1280 x 1024	110 MHz	65 KHz	5
1600 x 1200	165 MHz	75 KHz	8
2048 x 1536	250 MHz	100 KHz	12

Table 2. Common Graphics Resolutions and Line Rates. (60 Hz Non-Interlaced Refresh Rate)

DAC Resolution

DAC resolution is a measure of how many individual steps there are between end points and a measure of how accurate each step relates to the next one. A 4-bit DAC output will have 16 discrete levels at 41.2 mV intervals, while an 8-bit DAC will have 256 discrete levels at 2.5 mV intervals (assuming 0.66 volts of color information). A typical video DAC will have a differential non-linearity of ±1 LSB or ±2.51 mV which determines the width of each step. The end result is a higher resolution and a smaller differential non-linearity value, which produces a more accurate control over the CRT beam intensity and the color quality.

In a TTL and CMOS system, only a single 5 volt power supply will be required. An ECL system will require a termination plane and a -5.2 volt power supply, while an ECL-TTL system will need a +5 volt, a VT, and -5.2 volt power supply.

DAC Termination

The video DACs output signal must interface properly with a video monitor and be able to drive a 75 ohm coax (the standard input impedance for the video monitors). Since the DAC is a current source, and the relation V = IR determines the signal level, the output is terminated into a 75 ohm load to develop the output voltage levels. As speeds increase, ringing and reflections in the cable may distort the waveform causing the termination at the monitor to be insufficient in maintaining the signal quality.

If termination is at the source and at the load, some video DACs will allow double termination. In such an instance, a 75-ohm resistor is placed near the output pin of the DAC to ground and the terminating impedance of the monitor serves as the load resistor. A diagram of the connections are shown in Figure 3.

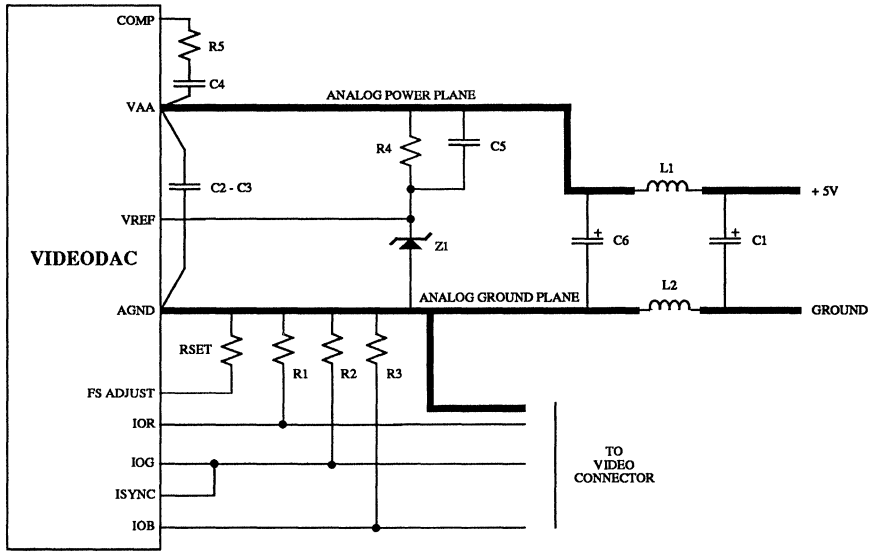

Figure 3. Typical Connection Circuit.

Glitch Impulse

Glitch impulse is a term used to define the area under the voltage-time curve of a single DAC step until the level has settled out to within the specified error band of the final value (the linearity error). Glitch impulse is important where subtle code changes can produce significant level changes, and is different from settling impulse which involves large amplitude changes.

Depending on the type of internal logic design in the DAC, the glitch energy can be very low (< 50 pV-sec) for a segmented architecture to as much as 250 pV-sec for a R-2R network. For many DACs, maximum glitch energy will occur when a transition is made between segments (which have the worst switching skew), where the count goes from 0111 1111 to 1000 0000. This is where all the internal registers will change and the current sources are turning on and off. Low glitch energy is necessary to avoid pixel color change or blurred pixels across the CRT. Figure 4 shows a typical DAC output glitch.

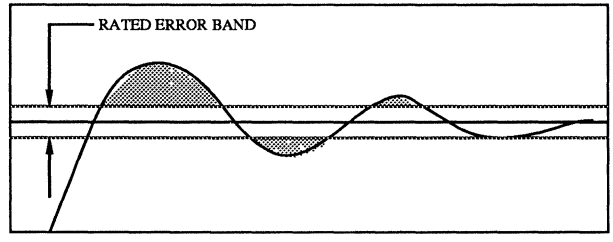

Figure 4. DAC Output Glitch.

In a video system, if the glitch energy is sufficiently low and repetitively consistent across all codes, it will be integrated over a period of time and will have no effect on the CRT screen. Other glitches generated by the DAC, such as data feedthrough and DAC-to-DAC noise may have a cumulative effect since the waveforms may not be repetitive. Therefore, good design practices in PC board design, power supply decoupling, and avoiding running digital signal lines near the DAC analog circuitry and output to the monitor should be observed. A suggested component placement is shown in Figure 5.

DAC-to-DAC skews greater than 1/4 pixel interval results in perceived color shift and resolution loss.

Rise/Fall Times

How fast a DAC output can switch from one voltage step to the next voltage step is measured from the 10% to 90% transition of the output waveform. In video applications, the faster the DAC the smaller this number will be. For a 30 MHz DAC, 3 to 10 ns would be typical, while for a 125 MHz DAC, 1 to 3 ns would be common. For very high speed DACs in the 250 MHz or greater speed range, rise and fall times under 1 ns are necessary. The output voltage slew rate is also a function of the load capacitance/termination and the addition of small values of capacitance can some times be used to reduce overshoot and ringing when very fast DACs are used.

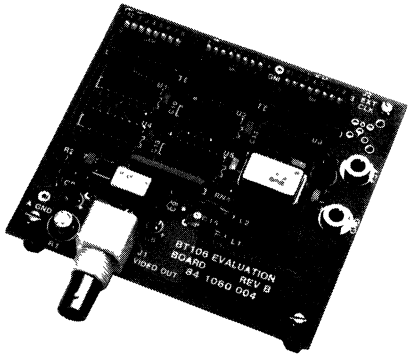

Figure 5. Typical Evaluation Module.

Settling Time

Settling time is a measurement of how fast a DAC output voltage from the mid-transition, settles to the desired value within an error band (e), typically ± 1/2 LSB.

In video applications, settling time is of moderate importance, since the CRT phosphors are being excited and the eye will not respond to the very small differences in light intensity of the pixel on the screen. Settling times greater than a pixel interval result in loss of color rendition or palette resolution.

Settling time is an important parameter if the DAC is being used in an instrumentation environment where it is necessary to have very accurate voltages as the input code is changed. Figure 6 describes both rise/fall time and settling measurements.

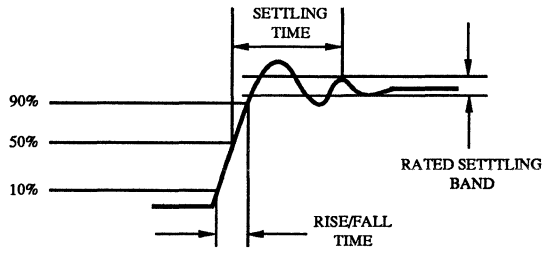

Figure 6. Rise/Fall Time and Settling Measurements.

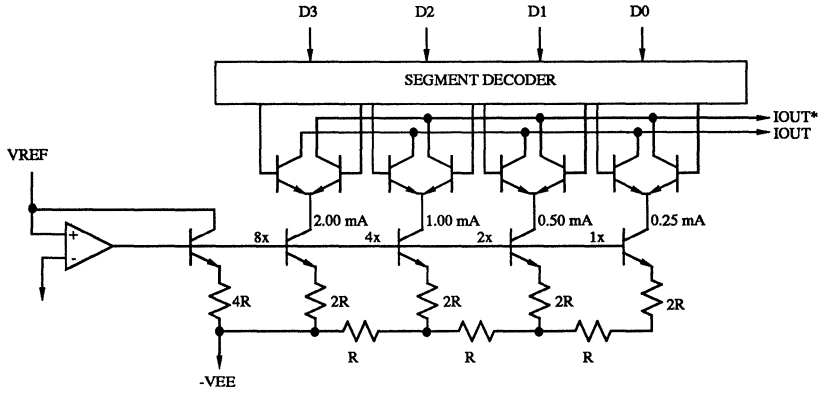

Figure 7. Typical R-2R DAC Network (4-Bit DAC).

DAC Internal Architecture

To generate the individual current steps, the simplest form of a DAC will use a R-2R summing resistor network. For an 8-bit DAC, eight current sources are used in a binary fashion to generate 256 output steps. While minimal components, the weaknesses of this design are: 1) the resistor ladder tolerances are critical, 2) the individual current steps range from large to small values, and 3) the temperature tracking of resistor pairs. Due to device tolerances, in order to obtain less than ± 1 LSB integral linearity error and ± 1 LSB of differential linearity error, it is necessary to match the resistors by laser trimming resistor links.

Figure 7 illustrates a typical R-2R DAC network. An improved type of circuit architecture, called a segmented DAC, offers low glitch energy and no trimming of resistors to obtain the needed accuracy. The segmented DAC utilizes the fact that monolithic transistors and resistors of the same geometry can match closely to each other and that cumulative geometry errors can be effectively averaged over the monolithic device area.

Some segmented DACs may use 256 individual current source transistors or a combination of segmentation for the higher order bits and a R-2R network for the lower order bits where speed, tolerance, and area determines the partition. Figure 8 shows a fully segmented DAC circuit topology.

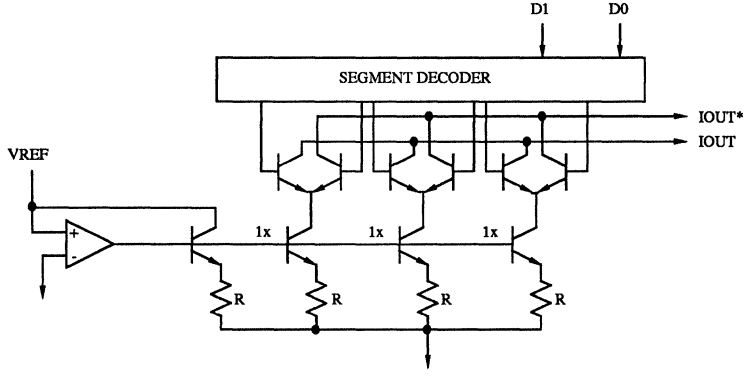

Figure 8. Segmented DAC Topology (2-Bit DAC).

Comparison of NTSC, PAL and SECAM Video Formats

There are several international standards for specifying the amplitude and video components of a waveform for use with television and video monitors which use a subcarrier for color or chrominance information.

In North America and Japan, the NTSC format is the standard, while PAL and SECAM video formats are used in Europe. A comparison of the various video levels is shown in Table 1 for reference, and Figure 1 is a drawing of a composite video waveform. The newer international standards specify a voltage amplitude of 0.714 volts between the blanking level and the white level for the video portion of the waveform (blanked video signal) and is defined as having 100 IRE units. The black to blank level (typically referred to as the setup) is used to shut off the beam during the retrace time and varies between the formats. The total amplitude is about 140 IRE units (143 IRE units for PAL and SECAM) from sync tips to reference white for monochrome, with a saturated subcarrier.

An older standard known as RS170A is also used in the United States and differs from RS343A level for the voltage level from blank to white. The RS170A blanked video level is 1.00 volts as compared to the RS343A, PAL, and SECAM levels of 0.714 volts.

8

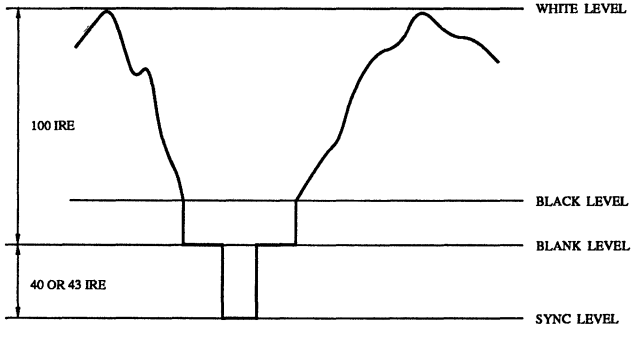

Figure 1. Composite Video Waveform.

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The monochrome version of the RS-170A standard (RS-170) does not have a subcarrier for color or chrominance information.

The sync levels (40 IRE units for NTSC and 43 IRE units for PAL and SECAM) are sufficiently close enough in tolerance that the 40 IRE levels of the Brooktree VIDEODACs and RAMDACs will meet the PAL and SECAM tolerance.

The RS-343A standard is commonly used for computer graphics, and of the four standards previously mentioned, it and RS-170 are the only ones that do not use a subcarrier for color or chrominance information. Rather, three separate signals (red, green, and blue) are generated, each containing intensity and blanking information. Typically, only the green channel contains sync information.

To assist users who need to determine the output current when terminated into 75 ohm and 37.5 ohm (doubly-terminated 75-ohm) loads, a comparison chart is shown in Table 1. Brooktree DACs are specified to drive doubly-terminated 75-ohm loads, while many competitor DACs can only drive a singly-terminated 75-ohm load and develop the proper video output voltage level.

	Video Output Levels	IRE Units	Volts	mA (typ.) (75-ohm load)	mA (typ.) (37.5-ohm load)
NTSC RS-343A*	Blank to White	100 IRE	0.714 ± 0.1	9.52	19.04
	Blank to Black	7.5 ± 5 IRE	typ. 0.054	0.714	1.43
	Blank Level		0	0	0
	Blank to Sync	typ. 40 IRE	- 0.286 ± 0.05	- 3.81	- 7.62
NTSC RS-170*	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
NTSC RS-170A**	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
PAL**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 IRE	0v	0	0
	Blank Level		0v	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19
SECAM**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 to 7 IRE	0 to 0.049	0	0
	Blank Level		0	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19

*no color or chrominance subcarrier -- requires three channels for RGB.
**uses color or chrominance subcarrier -- Bt102 is suggested VIDEODAC.

Table 1. Comparison Of Video Formats.

Other items of interest when comparing the various video formats are the number of lines per frame, field frequency, and normal video bandwidth:

	RS-170A	PAL	SECAM
Number of lines per frame	525	625	625
Field frequency	60	50	50
Luminance Bandwidth (MHz)	4.2	5	6
Chrominance Subcarrier (MHz)	3.58	4.43	4.3 to 4.4
Chrominance Bandwidth (MHz)	0.5 to 1.5	1.3	1.3

Table 2. Comparison of Video Formats.

Since chrominance subcarrier formats generate output levels between blank and sync levels (to generate color burst information during the back porch time), the sync and blank control inputs to most DACs cannot be used in such applications. The 20 IRE gap between sync and the most negative color burst level represents a 15% loss in gray scale range just to encode the sync.

This can be improved by asserting sync information through an external current sink rather than through the DAC data bits. Figure 2 shows a circuit using a transistor array (3227) biased off a negative supply voltage. The delay through the external sync switch should roughly match that through the DAC including any pipeline delays. Fast CMOS switches (4316 type) can perform the same function using resistor summing (rather than current summing), with some attendant degradation in output impedance match or return loss (3% or 30 dB is common for industrial grade, while 10% or 20 dB suffices for consumer applications).

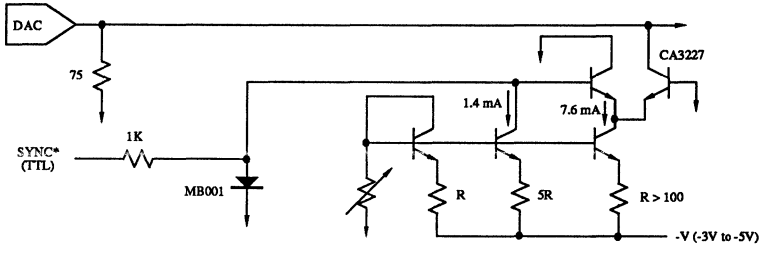

Figure 2. External Sync Circuit for NTSC RS-170A, PAL, and SECAM.

Component Analog Video Formats

In recent years, the trend has been toward component analog video (CAV) formats, much like the RGB format of most computer graphics systems.

The major video equipment CAV formats currently in use are summarized in Table 3 at a standard color saturation level of 75%, which is the common "legal" limit to the chrominance subcarrier's amplitude range in the NTSC format.

GBR is the matrix decoded version of NTSC with sync added to all three channels, which may be extended to 700 mV gray scale at 100% saturation with a PLUGE offset for monitor black/white adjust. Reversal of the non-complex RGB to GBR format is consistent with the green signal corresponding to the Y or luminance signal in the other color difference (B - Y and R - Y) formats.

The BetaCam and MII are the popular Sony and Matsushita formats respectively, each of which come in 3 or 2 wire versions and involve the Component Time Division Multiplexed (CTDM or CTCM) nomenclature in the latter case.

The Society for Motion Picture and Television Engineers (SMPTE) and the European Broadcasting Union (EBU) have adopted their own color difference formats in order to remove brand name association. Most CAV formats sample the color difference components at half the rate or bandwidth of the luminance signal (the common 4:2:2 hierarchy, not to be confused with the RS-422 interface). Most CAV formats have no use for the 7.5 IRE setup used in NTSC, which represents a 7.5% loss in dynamic range. Hence, the newer CAV standards (GRB and SMPTE/EBU) call for no setup pedestal.

Format	Video Output Function	Signal Amplitude (Volts)	Comments
GRB	G, R, B Sync	+ 0.700 - 0.300	at 100% saturation, 0% setup three wire = (G + sync), (R + sync), (B + sync)
BetaCam*	Y Sync R - Y, B - Y	+ 0.714 - 0.286 ± 0.350	at 75% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
BetaCam*	Y Sync CTDM R - Y CTDM B - Y Sync	+ 0.714 - 0.286 ± 0.350 ± 0.350 - 0.630	at 100% saturation, 7.5% setup on Y only two wire = (Y + sync), CTDM [(R - Y), (B - Y + sync)]
MII†	Y Sync R - Y B - Y	+ 0.700 - 0.300 ± 0.324 ± 0.324	at 100% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
MII†	Y Sync CTCM R - Y CTCM B - Y Sync	+ 0.700 - 0.300 ± 0.350 ± 0.250 - 0.650	at 75% saturation, 7.5% setup on Y only two wire = (Y + sync), CTCM [(R - Y), (B - Y + sync)]
SMPTE	Y Sync PB PR	+ 0.700 - 0.300 ± 0.350 ± 0.350	at 100% saturation, 0% setup three wire = (Y + sync), PB, PR

*Trademark of Sony Corporation.
†Trademark of Matsushita Corporation.

Table 3. Popular Component Analog Video Output Formats.

Using the Overlay Palettes on Brooktree RAMDACs

What are Overlay Palettes?

Brooktree RAMDACs usually include an overlay palette, consisting of one or more registers, in addition to the normal color palette RAM. For triple RAMDACs, each overlay register contains 12 or 24 bits of color information (for triple 4-bit or triple 8-bit D/A converters, respectively). For single RAMDACs, each overlay register contains 8 bits of color information (assuming an 8-bit D/A converter).

To support the overlay palette, besides the normal pixel input ports, the RAMDACs have palette selection inputs, OLx. These inputs specify, on a pixel basis, whether color information is to be provided by the color palette RAM or one of the overlay registers.

Why are Overlays Useful?

In many instances, the graphics application software is primarily concerned with the generation and manipulation of images in the frame buffer. The system software, on the other hand, is usually responsible for cursor movement, menu insertion and deletion, and user messages, with minimal concern about the graphics image.

The use of one or two additional bit planes for overlays enables the system software to control user interface graphics independently of the graphics image. Graphics performance is improved, as the image in the frame buffer need not be modified each time the cursor is moved or a menu is displayed or removed. The problem of cursor avoidance during the image drawing process is also solved by implementing the cursor using an overlay approach.

Generating Overlay Information

Overlay information may be generated by using additional bit planes in the frame buffer, which would be interfaced directly to the overlay inputs of the RAMDAC. Thus, the designer is able to keep the graphics data and overlay data in separate memory, simplifying software and increasing graphics performance.

If a VLSI graphics processor is used, the cursor output may be connected to the one of the overlay inputs of the RAMDAC. Thus, whenever the graphics controller outputs cursor information, the appropriate overlay register is automatically selected. Additional bit planes or external hardware may still be used for menus, grids, alphanumeric overlays, etc., by using any other overlay inputs of the RAMDAC.

Some high performance graphics systems implement hardware cursors using discrete or VLSI logic. Again, the cursor information may interface directly to one of the overlay inputs of the RAMDAC. Additional bit planes or hardware, connected to the other overlay inputs may be used for any additional overlay functions. Four bits of overlay can emulate an enhanced graphic adaptor window atop the main graphics image.

Summary

Overlays provide a means of simplifying the implementation of user interface mechanisms such as cursors, menus, and any type of graphics or text information that is to be displayed independent of the main graphics image.

The separation of system user interface software and graphics generation software will usually increase graphics performance and simplify software interfacing to the graphics system.

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Expanding Personal System/2® Graphics With the Bt471/476/478 Family

The new IBM Personal System/2 introduces more graphics display versatility to personal computer software and calls for more versatile digital-to-analog converters to take advantage of the greater software power. The Bt471/476/478 family of pin compatible RAMDACs support the basic capabilities of the IBM hardware as well as several added performance features which help differentiate board-level products in the compatible PC and expansion board markets.

The Bt471/476/478 family features more palette colors, higher speeds, overlay planes, simultaneous composite video and read-back, and surface mount packaging. These features afford the board designer flexibility and component savings for positioning his product in a dynamic marketplace.

Performance Features

Enhancements to the IBM hardware implementation (based on their Video Graphics Array) include:

A. Programmable choice of 262K or 16.7 million color palette. On the Bt478, a single pin programs the length of the palette word to be either 6 or 8 bits per color channel. For business graphics or false color renderings 6 bits is adequate, but for pleasing pictures of subtly shaded objects, 8 bits per channel is now standard on most Computer Aided Engineering (CAE) workstations and in the new Apple Macintosh II. More precise color segmentation can compensate for monitor inconsistencies (such as gamma effect) and reduce the "cartoon" appearance of color-limited palettes.

B. A 4-bit overlay port on the Bt471 and Bt478 makes special effects, such as cursors, borders, or even full EGA windows easy to implement on pixel-by-pixel boundaries, without the additional microprocessor burden of updating the pixel read mask for special effects.

C. A fully synchronous read-mask feature eliminates the need to externally synchronize the MPU write strobe to the pixel clock.

D. Support of both sync and MPU read-back on the Bt471 and Bt478 provides direct compatibility with RS-343 monitors without sacrificing future software system or self testing capabilities. The IMSG171 device offers one or the other of these features, but not both, in one unit. Selectable setup levels (0 or 7.5 IRE) allow the user to optimize the retrace intensity for each monitor assuring international hardware compatibility.

E. The Bt471/476/478 family also offers a choice of more stable voltage references, or a cheaper current reference that is 100% compatible with the existing PS/2® hardware.

F. More robust output capability for driving doubly terminated cables greater distances (or looped thru more monitors) with crisper transitions and lower reflection "ghosts". Brooktree guarantees linearity in terms of peak errors (not RMS) under doubly-terminated conditions. The coaxial medium between the DAC output and the monitor input calls for superior pulse fidelity to reduce amplitude ringing and monitor mistermination which can make pixels appear fuzzy, jittery or to have shadows.

G. An efficient 44-pin PLCC surface mount package occupies less board area than the 28-pin DIP counterpart. The lower PLCC profile improves power supply feedthrough and grounding as well by lowering package inductance 50%.

H. The Bt476 offers a pin-compatible solution to the IMSG176, and is available in both the 44-pin PLCC and the 28-pin DIP package.

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Implementing Enhanced Graphic Overlays

The new PS/2 graphics format is distinguished by its higher vertical resolution, variable frame rate, and its 8-bit pixel architecture. To take advantage of multi-frequency monitors, the IBM 8514A resorts to interlacing at higher resolutions to provide near megapixel displays at a reasonable price, supporting interlaced 1024 x 768 resolution at a 43.5 Hz refresh rate. Since interlacing compromises display phosphor response to reduce flicker, faster pixel rates are desirable to achieve 60 Hz refresh rates without flicker or smearing. Non-interlaced 60 Hz formats of 1024 x 768 or 1024 x 1024 can be supported by the 80 MHz Bt471/478.

The non-interlaced formats keep the full 640 pixel horizontal resolution of the previous CGA, EGA and PGC formats while giving the preferred 4:3 aspect with 480 vertical lines at a frame rate of 60 to 70 hertz (320 x 200 with pixel replication). The 8-bit pixel word size provides for 256 simultaneous colors from a palette of 262K colors (6 bits per channel) or 16.7 million colors (8 bits per channel with the Bt478).

As the power of the VGA to do complex graphic operations in real time becomes fully supported by the software industry, it will be possible to mix various formats on screen to create sophisticated windows, cursors and overlays. The independent palette access provided by the overlay ports on the Bt471/478 will enable parallel generation of graphic effects without imposing additional MPU limitations.

The use of a read mask in the IMSG171 to generate special effects is fully supported (internally synchronous) in the Bt471/476/478, but it's update rate is limited by the MPU write cycle time of 3 to 4 pixel clocks. This means that the mask effect will appear no finer than several pixels on the screen. This may save palette RAM size but prohibits high resolution overlays such as an EGA style window over a large part of the viewing screen. In situations where pixel frequency must be agile and independent of the MPU clock, the synchronous buffering of the Bt471/476/478 prevents corruption of the palette contents, something that can occur with asynchronous IMSG171s when the pixel clock is not locked to the MPU clock.

The four overlay inputs to the color palette can be loaded and invoked in the same manner as the standard palette. An additional register select pin(RS2) is provided for loading and reading back the overlay values. In the read mode the overlay inputs override the P0 - P7 pixel inputs, so any unused pixel and overlay inputs should be tied low. This parallel palette access simplifies cursor or cross hair generation to where a single chip (such as the Bt431) can manage this function with direct connection to the overlay inputs of the Bt471 or the Bt478.

With proper synchronization and raster scaling through the feature connector common on EGA cards, direct superposition of an EGA image over a VGA display is possible without burdening the VGA interface. This multi-path approach to high resolution windows is inherently faster and more interactive than software driven techniques and compares with hardware window features found on the more sophisticated graphics systems processors. This technique can be done on a pixel-by-pixel or bit-by-bit basis so that the full resolution capability of the multi-frequency monitor can be used.

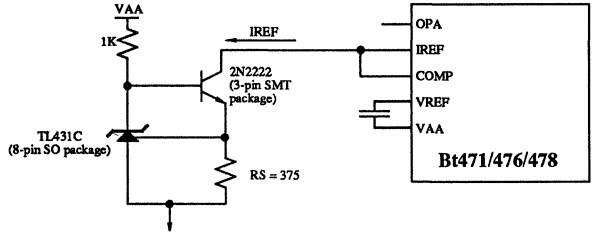

Figure 1. External Current Reference.

Suitable References

The quality of the image produced by the DAC can depend on the stability and regulation of it's reference. The Bt471/476/478 family offers the user a choice of current or voltage references so that either drop-in compatibility or optimum performance can be provided. The 28-pin DIP version of the Bt476 supports the only current reference.

The Bt471/476/478 family uses the voltage reference in a closed feedback loop control circuit which provides each individual current cell with a stable voltage reference. This common voltage reference can be externally decoupled at the compensation pin to minimize noise disturbance due to current switching. The combination of closed-loop stability, direct reference decoupling, and compatibility with low temperature coefficient voltage references gives the Bt471/476/478 superior amplitude stability and noise immunity. This results cleaner images on the graphics display monitor.

Figure 1 shows a typical current reference circuit for the Bt471/476/478. All these components are available in surface mount packages, but you will note the current reference approach requires 2 or 3 additional passive components. The simplest 4 mA current reference available, a Motorola MCL1304 or Siliconix CR430 type JFET device, offers only ±15% to ±25% accuracy, which would only be tolerable in analog-EGA applications or where the monitor contrast adjustment could compensate.

Setup and Sync

While the IBM-PC graphics standards have always provided for separate TTL synchronization lines, traditional analog monitors work with composite synchronization super-imposed on the green video channel. The Bt471/478 devices provide composite sync on all channels by asserting a low pulse on the SYNC* pin, which turns off an internal 40 IRE pedestal on each video channel.

Blank assertion in the composite format is more reliable (form a noise standpoint) if a 7.5 IRE pedestal distinguishes the black and blank voltage levels. This setup level provides for blacker-than-black CRT beam retraces which reduce visible retrace lines on bright displays. For this reason a selectable setup pedestal is provided to optimize the sync and blank interface for most multi-frequency analog monitors and various international raster video formats (NTSC, PAL, SECAM, CCIR, etc).

Optimum Termination

The analog interface between the RAMDAC and the display monitor must have transmission line properties to assure proper pixel definition on the display. Where TTL monitors can tolerate pulse ringing and cable echoes due to their binary nature, analog displays must settle to within 1% amplitude accuracy well within the pixel duration to render 6- or 8-bit color values faithfully. Double termination of the coaxial cable with the characteristic impedance of the cable is desirable in that it lowers the lumped time-constant at the DAC node and attenuates signal reflections from the monitor (or loop through nodes), which can produce pixel smearing or ghosting with cables longer than 2 meters.

A lower termination resistance at the DAC node neutralizes the connector and cable capacitance but forces the DAC to put out as much as 30 milliamps to produce 1v peak to peak at the monitor input. A lower time constant produces faster transitions and settling, which means crisper pixels on the display with truer color rendition.

Figures 2 and 3 depict the 64 code steps of the IMSG171 and Bt471 driving a 75-ohm doubly-terminated load. A Tektronix 2465 scope was used in the expanded sweep mode to highlight the mid-scale glitch that occurs during the binary 31 to 32 code transition. The characteristic 1/4 - 1/2 - 3/4 scale glitches of the IMSG171 are evident on the 700 mV amplitude waveform.

The expanded scale is calibrated to give graticle square areas of 500 pV-sec (100 mV * 5 ns). The mid-scale glitch of the IMSG171 consists of clock feedthrough with an approximate impulse area approaching 200 pV-sec, while the Bt471 mid-scale glitch area is less than 50 pV-sec. Clock feedthrough has no visible aberration on the monitor since it represents an equal amount of energy every pixel. However, glitch impulse may be visible since it occurs only on specific code transitions.

Resolution

The Bt478 offers an upgrade path to 8 bits of resolution in the same pin compatible package as the Bt471 and Bt476. Figures 4 and 5 show a comparison between 6 bits and 8 bits of resolution for a 3D solid model.

The gray scale shading can been seen limited and annoying to the eye on the 6-bit rendering offering only 64 shades, while the 8-bit image offers 256 gray shades and fine shading. The 8-bit photo clearly shows the smooth shading required for 3D modeling or professional slide presentations.

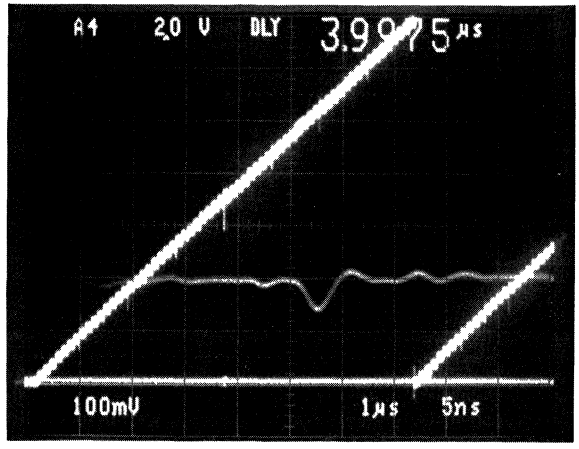

Figure 2. IMSG171 Output Waveform.

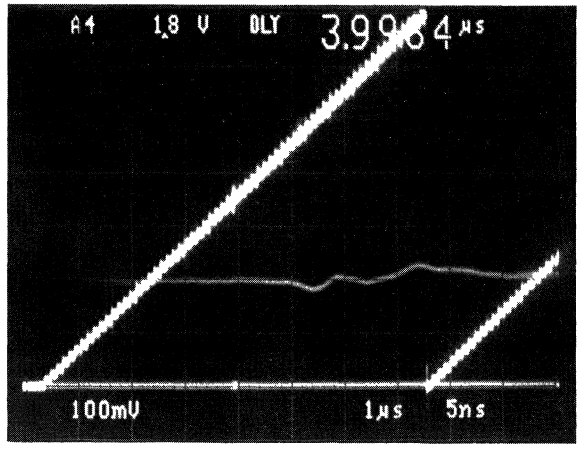

Figure 3. Bt471/478 Output Waveform.

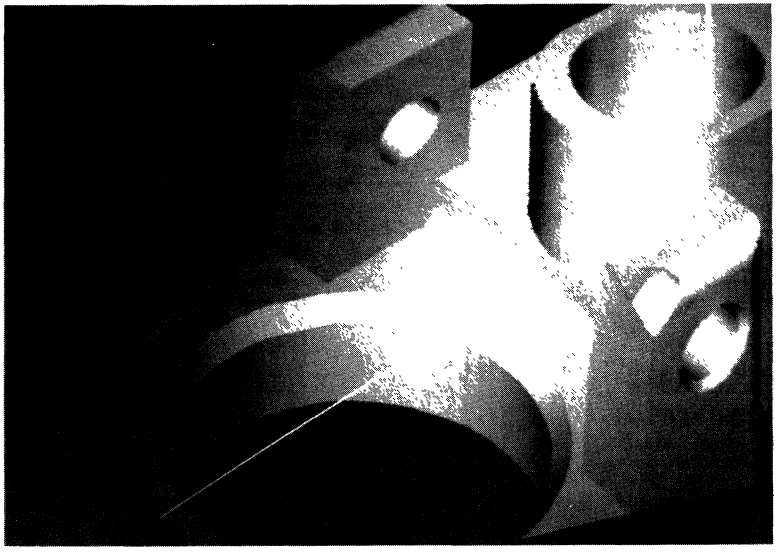

Figure 4. 6-Bit Resolution Example.

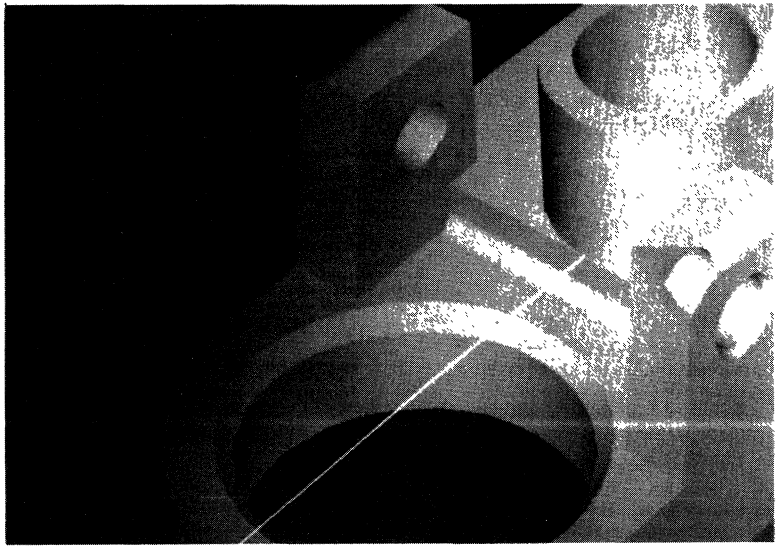

Figure 5. 8-Bit Resolution Eample.

Packaging

The IMSG171 is photographed side by side with the Bt471/478 in Figure 6. The Bt471/478 is shown in the ceramic 44-pin package and occupies considerably less area than the IMSG171 in the 28-pin DIP.

Note the internal chip capacitor in the specially-tooled 28-pin DIP package of the IMSG171. The chip capacitor mounted in the cavity serves to compensate for the DIP package inductance. This is less effective in terms of glitch suppression than the inherently lower inductance of the 44-pin PLCC package.

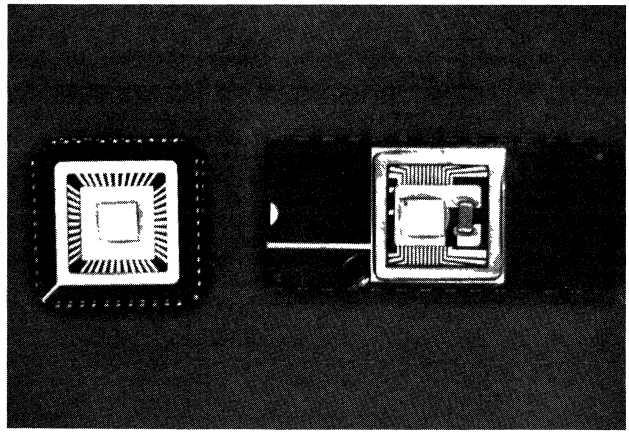

Figure 6. Packaging Comparison.

PC Board Layout Tips

Printed wiring board design considerations for analog output devices can be more critical than for pure digital. Four-or-more layer boards are better for lower power and ground noise as well as for segregating the analog outputs and reference from the digital inputs. This becomes even more important as speed migration from 25 MHz to 75 MHz dictates faster devices which generate more power supply spikes and radiation. Migrating from 6 bits per channel to 8 bit quantization compounds the need for low inductance power and ground returns if true color rendition and low electromagnetic emissions are to be achieved.

The effect of supply and ground noise and digital edges on the palette DAC is to produce image-dependent artifacts on the display which are especially perceptible when images are superimposed. Even the best CMOS DACs couple about 10% of any supply noise to the analog output. Care should be taken to limit supply noise at the DAC (in the bandwidth of the analog channel, typically the pixel rate) to 10 times the amplitude of the least significant bit.

Multiple ground planes make it possible to isolate the DAC current return to the system supply from other digital circuitry while maintaining low plane-plane potentials which affect the digital noise margins and contribute to electromagnetic emissions. It is desirable to reduce DAC ground noise to less than 10 mV during the active display line for clean looking 6-and 8-bit displays.

Performance Comparision Chart of Bt471/476/478 vs IMSG171

	Bt471	Bt476	Bt478	IMSG171
IBM PS/2 Compatible	YES	YES	YES	YES
Number of Displayable Colors	256 + 15	256	256 + 15	256
Maximum Number of Bit Planes	12 (8 + 4)	8	12 (8 + 4)	8
Total Palette Size	256K	256K	256K or 16M	256K
Frequency (MHz)	35 / 50 / 66 / 80	35 / 50 / 66	35 / 50 / 66 / 80	35 / 50
Palette Read-Back	YES	YES	YES	YES
On-Board Sync	YES	NO	YES	NO
Full Scale Reference	Voltage + Current	Voltage + Current	Voltage + Current	Current
RS-343A and CCIR Standards	YES	YES	YES	NO
Integral Linearity	0.25 LSB (0.5%)	0.5 LSB (1%)	1 LSB (0.5%)	0.5 LSB (1%)
Differential Linearity	0.25 LSB (0.5%)	0.5 LSB (1%)	1 LSB (0.5%)	monotonic
Glitch Impulse	75 pV-sec	75 pV-sec	75 pV-sec	200 pV-sec
Overlay Capability	YES	NO	YES	NO
Rise/Fall Time	3 ns	3 ns	3 ns	8 ns**
Memory Technology	Fully Static	Fully Static	Fully Static	Req. Constant Clock***
Compatible Family	YES	YES	YES	Almost*
Monolithic	YES	YES	YES	On Board Chip Cap
Surface Mountable	YES	YES	YES	NO
Package	44-pin PLCC	44-pin PLCC or 28-pin DIP	44-pin PLCC	28-pin DIP

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* Due to limited number of pins in the INMOS pin-out, trade-offs have been made between products. For example, the pin that allows the color palette to be read in the IMSG171/3/6 is used for SYNC in the IMSG170/2/4 thereby inhibiting the ability to read back the color palette on the later parts. Also, the 6-bit data used in the IMSG170/1/2/3 can not be used directly with the 8-bit IMSG174/6 because the 6 bits are located in the LSBs and would result in an output 1/4 the brightness. Brooktree has a 6/8-bit pin that allows 6-bit code written for either the Bt471/476 or the IMSG170/1/2 to run on the 8 bit Bt478.

**single 75-ohm termination
***psuedo-static RAM cell

NOTE: Comparisons are based on the Brooktree Bt471/476/478 specification sheet L478001 Rev. L and the IMSG171 specification sheet 42-1008-00 dated April 1987.

Troubleshooting Your Brooktree CMOS VIDEODAC or RAMDAC

Power Supply Considerations

The noise on the power pins must be kept to a minimum. Brooktree devices offer some power supply rejection, however, this noise rejection decreases with frequency. In particular, about 10% of any frequency components over about 1 MHz will be coupled onto the output. The VREF and COMP pins should be checked to assure noise is minimized. This can be accomplished by keeping PCB and lead lengths to decoupling capacitors short and wide. Decoupling VREF and COMP pins to VAA is vital to reducing switching noise and overshoot on the DAC output.

Another useful technique is to mount a three terminal regulator close to the power supply pins to provide immunity to power supply transients, and use the fact that the regulator will provide excellent power supply ripple rejection. When operating from a switching supply with greater than 100 mV of noise, a two stage VAA decoupling filter is advisable. A CLC pie filter combination ahead of the attenuator bead should have a time constant value much less than the switching frequency to be effective. With a VAA filter approach, care should be taken to assure VAA power is applied before the inputs to prevent latch-up.

Always probe the power supply signals with an oscilloscope probe at the device pins. The DAC can have significantly more noise than is seen on the supply bus. Probe ground (AC coupled) less than one inch on DAC ground. Measure VREF noise relative to VAA.

Decoupling Capacitors

One of the most common problems is choosing the proper power supply decoupling capacitors and keeping the leads short enough. Refer to recommended capacitor types in individual datasheets. All capacitors exhibit a self-resonant point at which they no longer look like capacitors, but inductors. This resonant point is a function of frequency, capacitor material, lead length, and the PCB trace length of the power and ground traces where the capacitor is soldered into. Above self resonance, a capacitor looks like a series resonant inductor (with approximately 1 nH per 0.1 inch of lead length).

For example, a 0.1 µF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz. A 0.01 µF ceramic radial lead may resonate around 40 to 60 MHz while a 0.01 µF ceramic chip capacitor may resonant around 400 MHz.

As power supply transient frequencies approach the resonant point, the capacitor offers less effective filtering. At resonance, it is neither a capacitor nor inductor. Past resonance, it becomes an inductor, and may exhibit transmission line effects.

To overcome these problems, the parallel connection of a 0.1, 0.01, and 0.001 µF capacitors will generally overcome the most difficult transients. For the lower frequencies, a 10 µF tantalum capacitor is the best choice, mounted near the power and ground pins.

Attenuator Beads

The purpose of the ferrite attenuator beads is two-fold. First, they isolate fast transients (i.e., less than 1 ns) on the regular PCB power and ground planes from the device. They will reduce any fast transients and act as increasing AC resistance with frequency. These frequency vs. impedance characteristics are diagramed in Application Note 1. Therefore a decoupling capacitor close to the bead and the DAC power pin for long lead length is needed. Second, the ferrite beads also isolate high-frequency noise generated by the VIDEODAC or RAMDAC from being coupled back onto the main PCB power and ground planes.

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Experience has found that the ferrite beads are usually not required where the video bandwidth is less than one tenth the time constant of the logic. As an approximation, if the clock rate is less than 10 MHz beads are usually not necessary, but become increasingly important for frequencies above 50 MHz.

Many of Brooktree devices have signal edges on the order of 2 or 3 ns, which produces harmonic components in the 300 MHz to 500 MHz range. The beads attenuate these components from the PCB supply planes.

When using Surface Mount Technology (SMT) beads, watch the current rating. Bipolar DACs may use ferrite breads on their power pins for stability, while CMOS DACs are for noise rejection. Attenuator beads in the DAC ground return must have tens of ohms resistance at high frequency to be an effective attenuator. However, this can produce ground potentials of greater than the intrinsic noise margin when DAC currents are greater than 100 mA. Therefore ground beads are not recommended for DACs with dynamic currents of greater than 100 mA.

Digital Input Considerations

Some of the newer TTL logic families have very fast rise/fall times. It is possible for these fast transients to couple onto the analog outputs, resulting in excessively noisy analog signals.

Possible solutions are to put a 33 to 100 ohm limiting resistor in series with the digital inputs at their source, or use a resistor terminating network (220/330 ohm) at the expense of additional power. A slower logic family, such as ALS, LS, may be used if possible to reduce the input rise/fall times where pixel rates are less than 25 MHz. Noise on three-state lines should be avoided through termination.

ESD and Latchup Considerations

Correct ESD handling procedures are required to prevent damage which can produce symptoms of catastrophic failure or an erratic device behavior with somewhat leaky inputs.

Latchup can be prevented by assuring all power pins are at the same potential, that VAA is applied before the inputs voltage (power-up sequencing), and that there is no overshoot/undershoot on the input/outputs (schottky clamping diodes can limit these excursions).

No Video Information

Verify all power pins should have the correct voltage.

If a constant DC output is generated, it indicates that the DACs are probably not functioning correctly. The voltage on the VREF pin should be checked first to verify that the external voltage reference (if required) is operational. Decoupling of VREF to VAA near the DAC is vital to reduce switching noise on the DAC output.

The voltage on FS ADJUST should be very close to the VREF voltage. If the device contains an on-chip reference, the measured voltage at the FS ADJUST pin should be approximately equal to the specified internal reference voltage. Offsets of greater than 10 mV may indicate damage to the internal op-amp.

The COMP pin must be coupled to VAA through a ceramic capacitor and the lead lengths keep to an absolute minimum. The voltage on the COMP pin is nominally 3v to 4v. A voltage close to 0v or 5v indicates a bad COMP capacitor, a COMP trace shorted to power or ground, or a bad device. The output traces for video information should be checked for shorts to power and ground supplies.

The control, pixel, and overlay input setup and hold times should be verified. To ensure reliable operation over the full temperature and power supply range, the CLOCK input should be buffered by a single dedicated buffer that assures fast edges, with glitch free levels.

Incorrect Analog Output Information

If sync and blank information are output, but they are not the correct levels, verify the RSET resistor value, the voltage on VREF and FS ADJUST (they should match), and the output load. When looking at the voltage levels on the video outputs, the oscilloscope probe must have 75-ohm termination, to form the other termination of the doubly-terminated 75-ohm load.

If the sync and blank levels are correct, the analog section of the device is probably operational, and the problem is probably the microprocessor or pixel data interface.

Ensure that all of the control registers and color palette RAM are properly initialized following power-up. The contents of the control registers and RAM may be read back by the MPU to verify their contents. The chip select or chip enable input should always be a logical one, except when the MPU is accessing the device.

Nonlinear Gray Scale Analog Output

If the gray scale video appears to be nonlinear or compressed at one end of the gray scale, the compliance limits of the device are probably being exceeded.

Voltage levels on the analog outputs outside the compliance limits forces the DACs to operate in a nonlinear fashion. The greater the exceeded voltages, the more nonlinear the D/A operation will be. Incorrect output loading, a wrong value for the RSET resistor, or an incorrect reference voltage are the primary causes.

Noisy Analog Output

Excessively noisy analog outputs indicates that either the power supply pins, the COMP pin, or the VREF input have an excessive amount of power supply noise that is not being decoupled, or there is excessive undershoot/overshoot on the digital inputs.

Refer to Application Note 1 or contact the Brooktree technical hotline for further assistance at:

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RAMDAC Initialization

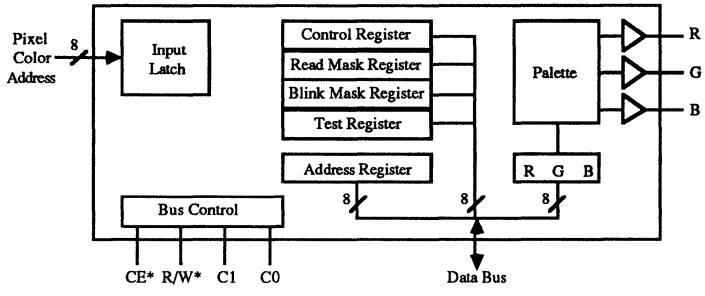

Figure 1. Bt458 Ports

Brooktree RAMDACs need to be initialized through the microprocessor port after power-on. This application note gives step-by-step instructions to the software programmer.

The initialization procedure differs slightly depending on how many control registers the RAMDAC contains. This application note uses the Bt458 as an example. Figure 1. shows the four Bt458 control registers, the pixel port (fast port), MPU port and bus control (slow port), and the DAC outputs. The microprocessor initializes the Bt458 through the MPU port. The following procedure explains a typical initialization of the Bt458.

Initialization Procedure

1. Initialize the control registers:

- Write 0,0 to C1,C0 ; set to write address register
- Put 06H on data bus ; address of command register
- Pull R/W* low ; write mode
- Strobe CE* ; write address to address register
- Write 1,0 to C1,C0 ; set to write command register
- Put 40H on data bus ; data to command register
- R/W* low, Strobe CE* ; write to command register

Note: 40H in the command register configures the device as follows:

- 4:1 mux
- Enable color palette RAM
- Blink rate = 16/48
- Blink disable
- Forces overlay inputs to logical zero

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Repeat the control register sequence using the following values to initialize the other command registers. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	04H	; write read mask address
• 1, 0	FFH	; FF hex to read mask register
• 0, 0	05H	; write blink mask address
• 1, 0	00H	; 00 hex to blink mask
• 0, 0	07H	; write test register address
• 1, 0	00H	; 00 hex to test register

2. Write the color palette starting with location 00 hex. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	00H	; write palette address 00H
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

Note: At this point, the palette address pointer auto-increments to address 01H. One must rewrite the address pointer to access locations other than 01H.

C1,C0	Data Bus	
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

3. To read back the palette or control registers, use the same sequencing but set R/W* high.

4. To write/read the overlay palette; set C1,C0 to 1,1 and continue as in step **2.**

Conclusion

This application note explains a basic program flow for initializing a Bt458 RAMDAC. The Brooktree databook contains further information concerning operation of this and other RAMDACs.

Bt458 INITIALIZATION PROGRAMMING SEQUENCE

TABLE OF OPERATIONS

	STEP	CE*	R/W*	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
Command Register	1	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE ADDRESS REGISTER
	2	↑	X	X	X	0	0	0	0	0	1	1	0	DATA 06H INTO ADDRESS REGISTER
	3	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO CONTROL REGISTER
	4	↑	X	X	X	0	1	0	0	0	0	0	0	DATA 40H INTO CONTROL REGISTER
Read Mask	5	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	6	↑	X	X	X	0	0	0	0	0	1	0	0	DATA 04H TO ADDRESS REGISTER
	7	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO READ MASK
	8	↑	X	X	X	1	1	1	1	1	1	1	1	DATA FFH TO READ MASK
Blink Mask	9	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	10	↑	X	X	X	0	0	0	0	0	1	0	1	DATA 05H TO ADDRESS REGISTER
	11	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO BLINK MASK
	12	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO BLINK MASK
Test Register	13	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	14	↑	X	X	X	0	0	0	0	0	1	1	1	DATA 07H TO ADDRESS REGISTER
	15	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO TEST REGISTER
	16	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO TEST REGISTER
Write Color Palette	17	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	18	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	19	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE RED
	20	↑	X	X	X	RED VALUE								DATA TO RED PALETTE
	21	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE GREEN
	22	↑	X	X	X	GREEN VALUE								DATA TO GREEN PALETTE
	23	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE BLUE
	24	↑	X	X	X	BLUE VALUE								DATA TO BLUE PALETTE
Read OVL0	25	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	26	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	27	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	28	↑	X	X	X	RED VALUE								RED VALUE AVAILABLE
	29	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	30	↑	X	X	X	GREEN VALUE								GREEN VALUE AVAILABLE
	31	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	32	↑	X	X	X	BLUE VALUE								BLUE VALUE AVAILABLE

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Building a 4K Lookup Table with the Bt457

Palette Applications

The need for a 4K lookup table for graphics is found in such applications as medical imaging, solids modeling and electronic publishing. A discrete implementation using three Bt457 single channel RAMDACs, twenty-four 4K x 4 static rams and miscellaneous MSI circuitry is all that is needed to implement this application.

The circuitry for one of the three channels is shown in Figure 1. This would be duplicated for each of the Red, Green and Blue channels. Each channel interfaces to the twelve plane frame buffer with two F374 devices. Four sets of 12-bit pixels are supplied to the registers from the frame buffer. Since the RGB planes use the same address, these registers can be used for all three channels.

The register's outputs are sent to the address inputs of the 4K x 4 static rams. Eight of these are needed for each of the three channels. The output data is then input into another set of F374 registers. The data has now been reduced to eight bits, which is used as pixel data. Four sets (A-D) of 8-bit pixel data is provided to the pixel inputs of the DACs for color generation. This provides 4:1 multiplexing of the Bt457 input.

Mapping the Bt457 internal LUT RAM allows the pixel data to be used as 8-bit data for the D/A converter, or the Bt457 RAMs can be programmed so that gamma correction, image manipulation or window palette switching can be performed.

MPU Interface

The microprocessor interface to the color palette is provided by a 12-bit address bus and an 8-bit data bus for each of the channels.

The address bus is presented to the RAMs by way of 2 F244 devices. These provide an output enable such that during a display, the F374s are always enabled and the F244s are disabled. The same address would be provided to each of the look-up tables.

The MPU data interface is a bit different. First, a bidirectional bus is needed so that the data stored in the color palette can be read back by the MPU. For this reason F245 devices are used. Second, each of the RGB channels is provided with it's own 8-bit Data bus. By using a 32-bit bus the red, green, and blue palettes can be written simultaneously. A counter can be included to generate the addresses so that the 4K addresses can be auto-incremented. The direction of the data bus is determined by the value on the RD* line. 8-bits are also needed for the RAMDAC MPU interface.

If direct color generation is needed, the Bt457 palette wouldn't be used as a lookup table, and the pixel address would be the same as the data. If gamma correction, or any other image transformation is needed, then the RAMDAC would need to be programmed accordingly.

Performance

The limiting factor in building the 4K solution discretely is the overall performance of the video generator. The screen resolution is directly related to the speed of the MSI circuitry and the static RAMs. The delay of the pipelines is as follows:

F374 Clock to Q	10 ns
Static RAM access(read)	20 ns
F374 Setup Time	2 ns
Interconnect delay	4 ns
Total delay	36 ns

Because 4:1 multiplexing is used, the time for each pixel generated is 36/4 = 9 ns. This corresponds to a clock frequency of 111 MHz. With this implementation a 1280 x 1024 resolution system (with 60Hz refresh) can be achieved. To increase the performance of the system, use of faster VRAMs (33 MHz), or a 2:1 multiplexing between the VRAMs and LUT is required.

An 8:1 LUT architecture could also be used. This would require multiplexing the output of the LUT to the Bt457 and also a significant cost increase due to a doubling in the amount of SRAMs.

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Another approach to increase the resolution of the system is to use faster RAMs as they become available. By using SRAMs with a 15 ns access time, the given architecture can achieve a video rate of 129 MHz.

True Color Application

A true color (36 plane) system can be achieved by multiplexing data from a frame buffer with the LUT output as shown in the diagram. The F374 outputs would be disabled via True Color Select, and the true color data would be enabled on the red, green , and blue channels.

Summary

Using the Brooktree Bt457 RAMDAC, a 4K color palette system can be created with the use of standard MSI products and CMOS Static RAMs. The 4K palette provides enough simultaneous color for modeling applications and medical imagery. It can be easily implemented using the methods described in this application note.

This information is intended for stimulating design interest and has not been breadboarded. Brooktree accepts no liability for designs contained in this application note. All users are cautioned to verify their own design.

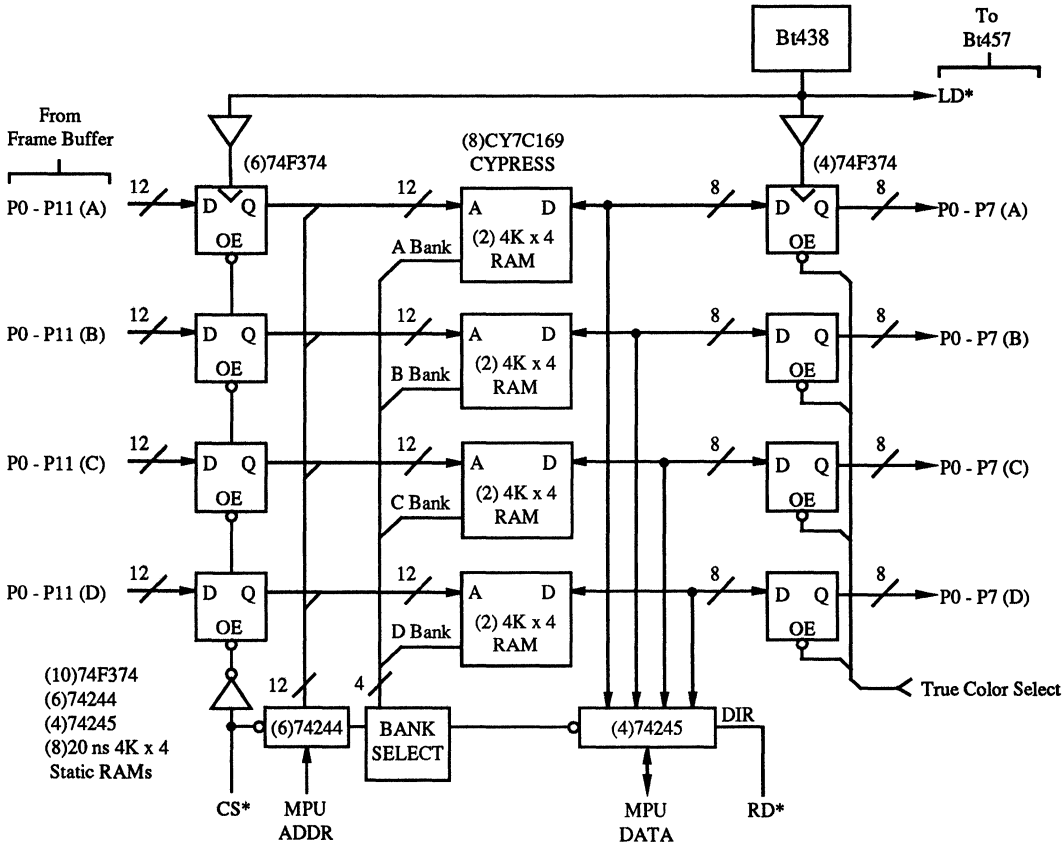

Figure 1. 4K Lookup Table Solution using the Bt457

Bt471/476/478 Power Saving Features

This application note will discuss various circuit configurations which will allow significant savings in power requirements when used with the Bt471/476/478. Laptop computers which support VGA graphics capabilities represent an application that can benefit from utilizing these power saving configurations. When operated from battery power in the portable mode, laptops use liquid crystal displays which do not require the VGA RAMDAC to be active. In such circumstances, the Bt471/476/478 power saving modes can be used to reduce supply requirements and extend battery life by powering down.

The Bt471/476/478 may be powered down in the following ways:

Power Down Mode	Registers/Memory Accessible
• VREF - shut down the DACs.	Yes
• IREF - shut down the DACs.	Yes
• Stop the clock.	No

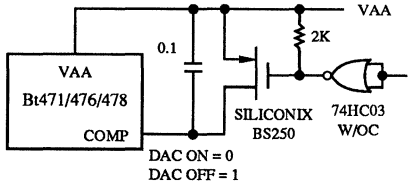

Figure 1. DAC Shutdown Using the COMP Pin.

Siliconix alternate sources:
Philips #BS250
Topaz #VP106

BS250 Typical Parameters:
IDSS @ VGS = 0v = - 0.5 mA
VGS @ ID = 1 mA = - 2.75v
BVDSS @ VGS = 0v = - 20v

VREF Power Down Mode

The VREF implementation provides an order of magnitude improvement in amplitude stability and noise immunity over an IREF implementation. For this reason, using a voltage reference is recommended over a current reference.

To eliminate the full scale output current and associated supply current to the DACs, open circuit the RSET resistor or pull the COMP pin up to VAA. Figure 1 shows a circuit for pulling the COMP pin to VAA. The 0.1 µF capacitor acts as a bypass capacitor between the VAA and COMP pins. This capacitor should be mounted as close as possible to the RAMDAC, with the leads kept short. The P-channel MOSFET with the source connected to VAA turns on when the gate voltage drops below four volts. The output of the 74HC03 open drain NAND gate pulls up through a 2K-ohm resistor to VAA. A logical one at the input to the NAND gate turns the DACs off.

Shutting down the DACs typically cuts the supply current by forty percent. For the Bt471, each DAC outputs three times the current flowing through the RSET resistor. To get a DAC output current of 21 mA, the current through RSET must be 7 mA (the actual value will be slightly less to achieve the 19.05 mA value specified in the databook). When the DACs are shut off, the total current saved will be 3 x 7 x 3 = 63 mA. At nominal supply voltage and room temperature, the Bt471/476/478 typically requires 130 mA. The power down current is therefore 160 - 63 = 97 mA.

Caution: Brooktree guarantees linearity specifications for output voltages up to 1.4 volts and for output currents down to one half of full scale.

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IREF Power Down Mode

For systems using a reference current (IREF), shut down the DACs by open circuiting IREF. Like the VREF mode above, the IREF current is proportional to the DAC output current. Figure 2 shows a circuit for supplying a constant current to the IREF pin. Drive the base of the NPN transistor with a low TTL logic signal to turn the DACs off. In the power down mode, the RAMDAC is fully register/memory compatible.

Powering down Bt471/476/478 typically cuts the supply current by forty percent and also saves the IREF current. For the Bt471 as discussed in the previous section the supply current is 160 - 63 - 7 = 90 mA.

Stopping the Clock

This mode is useful in applications where the designer does not need register compatibility or active video. The Bt471/476/478 static RAM does not require clocking to retain memory data. With the DACs on, this power down mode saves about 10 mA. Shutting off the clocks with the DAC powered down saves 2 to 3 mA. See Figure 3.

Summary

This application note shows several methods to reduce power consumption on Brooktree's Bt471/476/478 RAMDACs. Designers will find these power savings useful in laptop computers with VGA graphics capabilities. System designers may use the Bt471/476/478 power down capabilities to differentiate their products and improve performance.

This information is intended for stimulating design interest. Brooktree accepts no liability for designs contained in this application note. All users are cautioned to verify their own design.

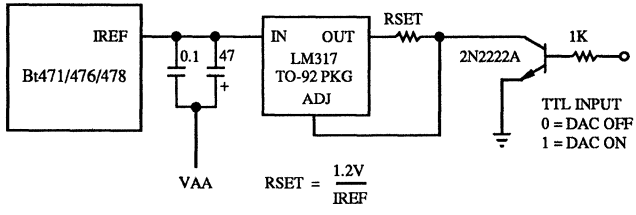

Figure 2. Open Circuit IREF.

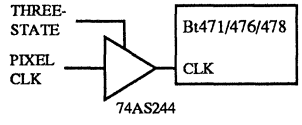

Figure 3. Clock Stopper Circuit.

Support Components

Brooktree's Technical Hotline has received many requests for assistance in identifying and locating components used with Brooktree products. Brooktree's data book and data sheets recommend components that are not always available in all areas. The following is a list of suggested manufacturers and components that will assure optimum performance of Brooktree products.

Crystal Oscillators

Many of the Brooktree CMOS RAMDACs require a positive ECL differential clock. Common 10K and 100K ECL crystal oscillators powered from +5 volts will provide this positive clock.

The following crystal oscillators come in a 14 pin DIP outline package. Pin 7 is ground, pin 14 is +5V, pin 8 is the clock output, and when a complimentary output is available, it is on pin 1.

Manufacturer/ Supplier	Model/Part Number	Description
Monitor Products 502 Via Del Monte Oceanside, CA 92054 (619) 433-4510	907EA 907EA1 907T	• For 10K ECL clocks to 200 MHz, case floating, open emitter output. • For 10K ECL clocks to 200 MHz, case floating, complimentary open emitter outputs. • For TTL clocks to 80 MHz.
Vectron Laboratories, Inc. 166 Glover Ave. Norwalk, CT 06850 (203) 853-4433 *In the U.K.:* Lyons Instruments (099-24) 67161	CO-633 CO-450	• For ECL clocks to 200 MHz • For 100K complimentary ECL clocks from 5- 400 MHz
Fox Electronics 6225 Presidential Court Fort Myers, FL 33907 (813) 482-7212	F5L F1100	• For 10KH ECL clocks to 200 MHz - Pin 7 (case ground) is an option • For TTL clocks to 80 MHz
Conner-Winfield 1865 Selmarten Road Aurora, IL 60505 (312) 851-4722	ECLA-1 ECLA-2 S15R6 S17R6	• For 10K, 8-150 MHz, case tied to pin 14 • For 100K, 8-150 MHz, case tied to pin 14 • For TTL, 0° to 70° C, 256 KHz-80 MHz • For TTL, 55° to 125° C, 256 KHz-80 MHz

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Ferrite Beads

Decoupling the power to Brooktree's products through a ferrite bead is recommended to prevent power supply noise from being coupled into the video outputs. Use of a ferrite bead is also recommended for suppressing interference caused by the fast switching times of the DACs.

Ferrite beads have a very low impedance at low frequencies which increases at higher frequencies. Refer to **AN-1** for a typical impedance curve. Beads are selected for their impedance at a standard frequency of 100 MHz, typical.

Manufacturer/ Supplier	Model/Part Number	Description
Fair-Rite Products Corporation P.O.Box J Wallkill, NY 12589 (914) 895-2055 *In the U.K.:* Apex Inductive Devices (01) 903-2944	2743001111 2743021446	• Axial lead, 71 ohms @ 100 MHz • Surface mount, 89 ohms @ 100 MHz
TDK Corporation 4711 West Golf Road #300 Skokie, IL 60076 (312) 679-8200	CB30-1210 BF45-4001	• Surface mount, 52 ohms @ 100 MHz • Axial lead, 85 ohms @ 100 MHz
Ferroxcube 5083 Kings Hwy Saugerties, NY 12477 (914) 246-2811 Canada: (416) 561-9311	5659065-3B	• 38 ohms @ 100 MHz

Sockets

For high speed operations and proper heat dissipation, it is generally recommended that Brooktree products be soldered directly to the PC board. However, when prototyping or operating at clock rates less than 50 MHz, sockets can be used. The following is a listing of commonly requested sockets.

The following sockets are recommended for use with Brooktree's PLCC packages:

Manufacturer/ Supplier	Model/Part Number	Description
AMP Inc. Harrisburg, PA 17105 (717) 564-0100 Canada: (416) 475-6222 U.K.: 44-1-954-2356 W. Germany: 49-6103-7090 Japan: 81-3-404-7171	641444-2 641746-2 641343-2 641747-2 643151-2 643066-2	• 28 pin, surface mount • 28 pin, solder tail • 44 pin, surface mount • 44 pin, solder tail • 84 pin, surface mount • 84 pin, solder tail
Burndy Corporation P.O. Box 5200 Richards Ave. Norwalk, CT 06856 (203) 838-4444	QILE28P-410T QILE44P-410T QILE84P-410T QILEXT-1	• 28 pin, solder tail • 44 pin, solder tail • 84 pin, solder tail • PLCC Removal tool
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PLCC-28-P-T PLCC-44-P-T PLCC-84-P-T	• 28 pin • 44 pin • 84 pin

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Sockets (continued):

The following sockets are recommended for use with Brooktree's PGA packages.

Manufacturer/ Supplier	Model/Part Number	Description
Augat 33 Perry Ave. Attleboro, MA 02703 (617) 222-2202 U.K.: (0908) 67665 W. Germany: (089) 576085 Japan: (03) 465-8457	PPS069-2A1130-L PPS084-2A1212-L PPS132-2A1414-L	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 144 pin PGA* *PGA package to PC board standoff distance : 0.166"
Robinson Nugent, Inc. 800 East Eighth St. New Albany, IN 47150 (812) 945-0211 Switzerland: (066) 229822	PGA-068CM3-S-TG PGA-084AM3-S-TG PGA-132AM3-S-TG	• 68 pin PGA* • 84 pin PGA* • 132 pin PGA* *PGA package to PC board standoff distance : 0.175"
Yamaichi U.S. Distributers: Nepenthe 2471 East Bayshore Rd. Suite 520 Palo Alto, CA 94303 (415) 856-9332	IC93-10803-G4	• 84 pin PGA* *PGA package to PC board standoff distance : 0.236"
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PGA69H003B1-1130T PGA84H003B1-1212T PGA132H003B1-1414T PGA145H003B1-1521T	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 144 pin PGA* *PGA package to PC board standoff distance : 0.165"

1.2V Voltage References

To meet RS170/RS343 tolerances, Brooktree DACs require a voltage reference of 1.2V ± 5%. The following devices meet this requirement.

Manufacturer/ Supplier	Model/Part Number	Description
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 721-5000	LM385Z-1.2	
Motorola Semiconductor Products 5005 East McDowell Road Phoenix, AZ 85008 (602) 244-7100 Japan: (03)440-3311 Hong Kong: 0-223111 U.K.: 0296-35252 W. Germany: (089) 92720	LM385Z-1.2	
Maxim Integrated Products 510 North Pastoria Sunnyvale, CA 94086 (408) 737-7600	ICL8069	

Video Buffers

Brooktree's DACs are intended to drive transmission line loads, which most monitors are rated as. Transmission line cable lengths greater than 10 meters can attenuate and distort high frequency pulses. Booster buffers can compensate for some cable distortion but must have 6-12 dB voltage gain into the cable load to be effective. Select buffers with ± 30 mA drive, 3 - 4 volt output swing, and full power bandwidth greater than that of the monitor. Buffers usually require negative supply voltages and thermal considerations.

Manufacturer/ Supplier	Model/Part Number	Description
Elantec 1996 Tarob Court Milpitas, CA 95035 (408) 945-1323 U.K.: 0844-68781	EL2003 EL2020	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain ≥ 1 into 50 Ω
Harris Semiconductor 2401 Palm Bay Road Palm Bay, FL 32905 (305) 724-7418	HA-5033 HA1-2542	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain 2 into 150 Ω
Comlinear Corporation 4800 Wheaton Drive P.O. Box 20600 Fort Collins, CO 80522 (303) 226-0500	CLC400	• 3dB/200 MHz Gain 2 into 100 Ω

Other Components

Metal film resistors are recommended for use with Brooktree's products because of low temperature coefficients and low current noise.

For assistance in locating other components, call the Brooktree Technical Hotline at (800) VIDEO IC.

Brooktree Product Evaluation Boards

Brooktree offers a wide range of Evaluation Module (EVM) and Device Under Test (DUT) boards to assist the designer in product evaluation. These boards are available through your sales representative or the Brooktree area sales office.

EVM boards are complete evaluation modules and include all the logic for initial evaluation of the Brooktree product. These boards are designed to offer a functional evaluation with minimal equipment, usually only a power supply and an oscilloscope are required.

DUT boards are a general purpose device test board and contain only the Brooktree product with design emphasis placed on the proper operating environment for layout and component placement. These boards will require all inputs, clocks, and power to be supplied through an external DIN connector. The power and ground layout on these boards has been optimized for best performance.

Printed circuit artwork for the EVM and DUT boards is available upon request. For further information call the Brooktree Technical Hotline at (800) VIDEO IC.

Device	Board Number	Description
Bt101	Bt101 EVM	Includes logic to generate full scale ramp and square wave outputs at full rated clock speeds.
Bt102	Bt102 EVM	Same as the Bt101 EVM
Bt103	Bt103 EVM	Same as the Bt101 EVM
Bt104/105	Bt104/105 EVM	Does not include logic. Uses a half wide DIN connector for power/data and an SMA connector for analog video out.
Bt106	Bt106 EVM	Same as the Bt101 EVM
Bt471/478	Bt471/478 EVM	This is an adapter which allows the Bt471/478KPJ to be evaluated in a 28-pin socket. Includes circuitry for an optional voltage reference. Access to overlay input via header. 4 optional jumpers.
Bt604	Bt604 EVM	Includes the necessary logic to evaluate the Bt604. Requires external trigger and -5.2V.

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Table of Contents

Bt604

Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

125 MHz
10KH ECL Compatible
Dynamically Programmed
Timing Edge Vernier

Distinguishing Features

- 125 MHz Maximum Trigger Rate
- Less than ± 1 LSB Timing Accuracy
- 15 ps Delay Resolution (4 ns Span)
- Extendable Delay Span to 40 ns
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package
- Typical Power Dissipation: 910 mW

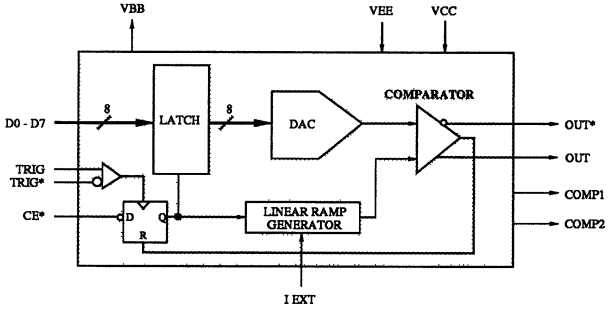
Applications

- Automatic Test Equipment
- Precision Timing Verniers
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt605, Bt606

Functional Block Diagram



Product Description

The Bt604 is a Dynamically Programmed Timing Edge Vernier, whose time delay is dynamically loaded upon each trigger of the circuit. In response to a trigger pulse, the Bt604 outputs a pulse of fixed width a programmable delay time later.

With the delay span set to 4 ns, the Bt604 features 15 ps of resolution (255 steps). The delay span is externally adjusted and is set in the range of 4 ns to 40 ns by IEXT.

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger and output pulse.

In applications for Automatic Test Equipment (ATE), the Bt604 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy, and is suitable for use in testers featuring "timing changes on-the-fly".

The Bt604 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

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Circuit Description

As illustrated in the block diagram, the Bt604 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, if CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG and latches the D0 - D7 input data which sets the DAC output voltage.

The comparator detects when the ramp reaches the DACs programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Upon resetting the ramp, the input data latch is made transparent, enabling D0 - D7 to reprogram the DAC and permitting another trigger of the Bt604.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0 - D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

$$Tspan = Tmax - Tmin$$

The output pulse delays are adjustable and are set by IEXT current flow through pin 12. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin.

Referring to Figure 4:

$$IEXT = (VEXT + 1.25v) / (REXT + 26\ ohms)$$

Output Pulse Spacing

Consecutive output pulses must be spaced no less than 8 ns apart.

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required to achieve maximum performance. The following recommendations are for maintaining the lowest linearity errors and minimizing the absolute timing variations over frequency.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

The data set-up time for trigger of the device should be extended to 5ns for on-the-fly applications. This will insure the best dynamic performance when making full scale transitions from code $FF to $00 which is when the worst case settling time conditions occur.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin - 500ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

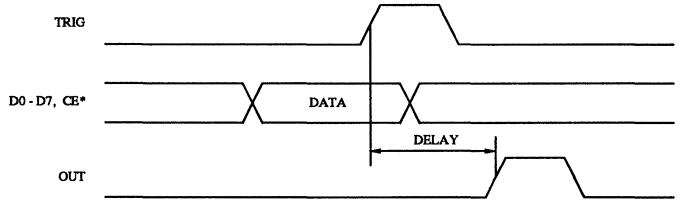


Figure 1. Input/Output Timing.

Circuit Description (continued)

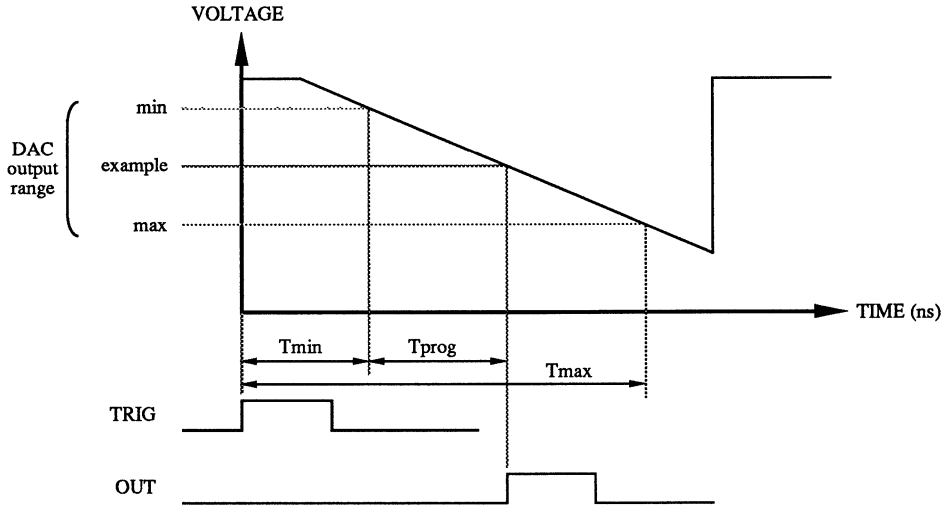


Figure 2. Linear Ramp and Output Pulse Timing.

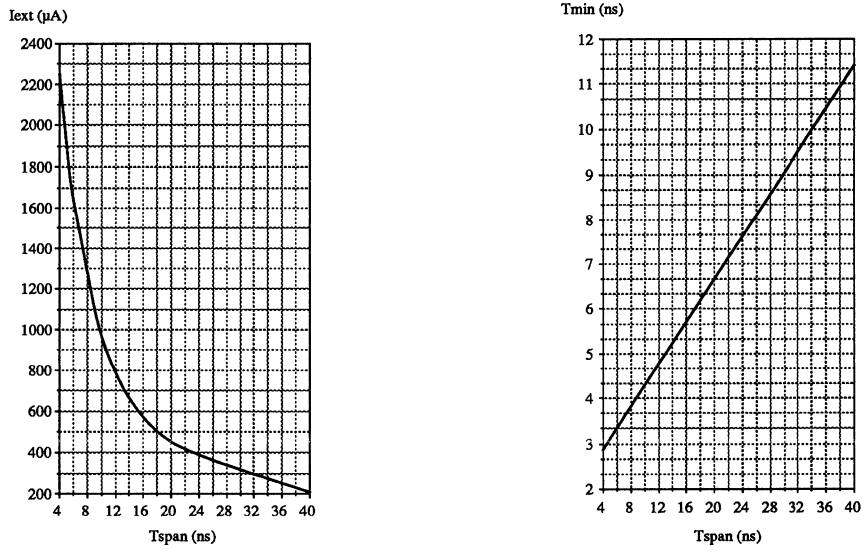
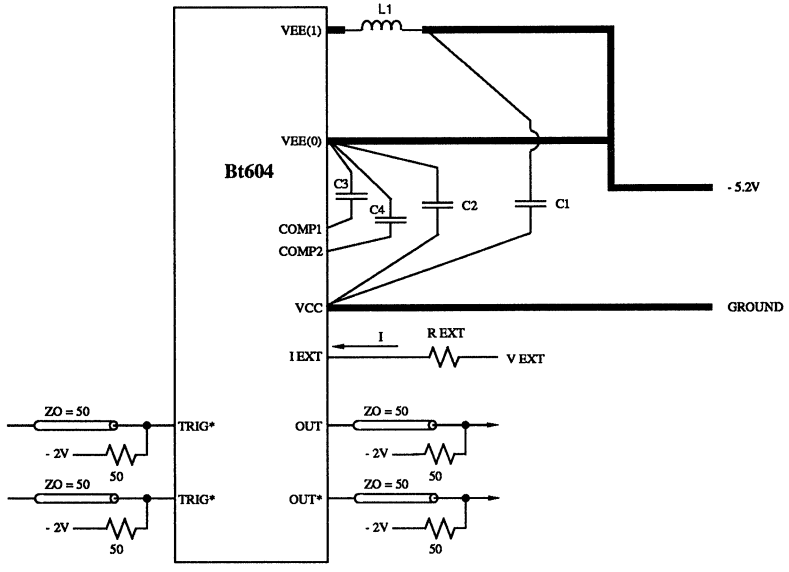


Figure 3. Typical Output Delays.

9

Circuit Description (continued)



with VEXT connected to VCC:

REXT (ohms)	Tspan (ns)
700	5
1400	10
2800	20

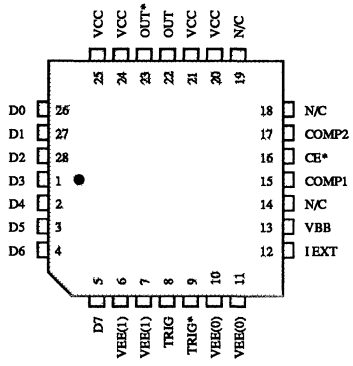
Location	Description	Vendor Part Number
C1 - C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
L1	ferrite chip bead	TDK 301210
REXT	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt604. All devices should be as close as possible to the Bt604.

Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0 - D7	Data input pins (ECL compatible). On the rising edge of TRIG, a ramp is initiated where upon D0 - D7 are latched into the device. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse. See Figure 1.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of the TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled. See Figure 1.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering is performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically -1.25v.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.
VEE	Device power. All VEE pins must be connected. **Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.**
VCC	Device ground. All VCC pins must be connected together.
VBB	-1.3v (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt604.

Application Information

Introduction

The Bt604 Timing Edge Vernier uses an external current source to set and calibrate the time delay span, Tspan. This section describes how Tspan may be set using external resistors and how an external diode may be used to improve, by a factor of approximately 3:1, the effects of temperature variations.

In applications where the output time delay may be measured, Tspan may be automatically calibrated using an external programmable current source. Also described is how this can be achieved in a cost effective manner using Brooktree's Bt110 CMOS Octal 8-bit DAC.

Tspan Temperature Compensation

The Bt604 exhibits small changes in Tspan with changes in temperature caused by temperature coefficient differences between the minimum time delay (tmin) and the maximum time delay (Tmax), where:

$$Tspan = Tmax - Tmin$$

Tspan is set with an external current source (usually a resistor to a voltage VEXT) as shown in Figure 4. The Tspan positive temperature coefficient can be partially compensated with an external network exhibiting a negative temperature coefficient consisting of two resistors and an inexpensive 1N4148 diode (see Figure 5). Resistors R1 and R2 are selected from Table 1 according to the Tspan desired. R1 and R2 are metal film resistors. R2 is selected or trimmed to obtain the desired Tspan.

The 2 mV/°C decrease in the forward voltage drop across the diode provides the necessary small changes in current. This network is most effective over a temperature range of 40 to 60 °C. Also shown in Table 1 are the temperature coefficients that can be expected over this temperature range for a 10° change in temperature. This is not a linear function in all cases. For example, with a 5 ns Tspan, Tmin may decrease from 40 to 50 °C. and then increase from 50 to 60 °C. As a result, values shown are absolute values.

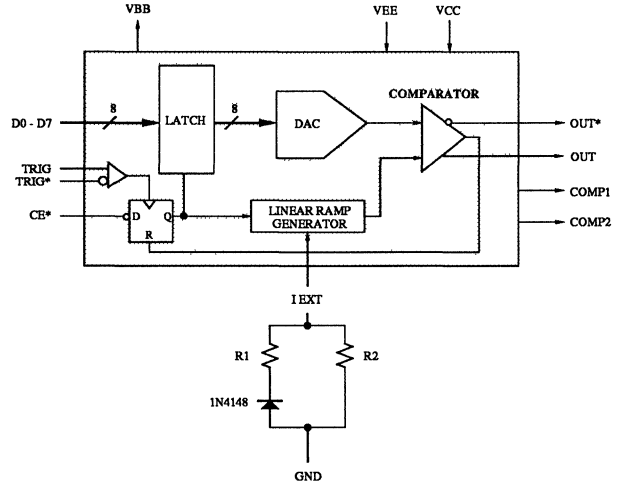


Figure 5. Typical Temperature Compensation Circuit.

Application Information (continued)

Tspan Calibration Using the Bt110

The accuracy and stability of the circuit providing the reference current (IEXT) directly affects the timing span accuracy. Computing values for R1 and R2 in Figure 5 results in a Tspan accuracy of better than ± 20%. This may require the adjustment or trimming of R2 to set Tspan to the precision required by the application. Using the Bt110 CMOS Octal 8-bit DAC can eliminate the need to trim resistors and provides a cost effective, low power solution to Tspan calibration. The block diagram of the Bt110 is shown in Figure 6.

For example, the Bt604 requires a nominal external current of 1780 µA for a Tspan of 5 ns. When the span is set of 5 ns, the Tspan/IEXT ratio is typically 2.80 ps/µA. Setting Tspan with resistor values as per Table 1 could result in a Tspan error of ± 20%, or ±1 ns. To correct for this error would require an adjustment of IEXT of ± 1 ns divided by 0.0028 ns/µA or ± 357 µA. If this IEXT adjustment is to be supplied by a DAC, then the full scale range would need to be 2 x 357 = 714 µA. An 8-bit DAC with this range would have a calibration resolution of 714 µA divided by 255 or 2.8 µA per bit. This represents a calibration resolution of 2.8 µA times 2.8 ps/µA or 7.84 ps.

This can be stated more simply as:

- Setting Tspan with resistors results in an error of ± x%.
- The Bt604 has 8 bits of resolution
- Calibrating with an 8-bit DAC results in a calibration resolution of 2x% of 1 LSB of the Bt604
- For Tspan = 5 ns
  1 LSB = 5 ns/255 = 19.6 ns
  Calibration resolution for ± x = ± 20% is
  0.4 x 19.6 = 7.84 ps

The circuit shown in Figure 7 implements the above using the Brooktree Bt110 CMOS Octal 8-bit DAC. Resistor R5 provides a voltage drop so that the ± 1v compliance range of the Bt110 is not exceeded; variations in R5 have no effect on IEXT.

The output range of the Bt110 is set by R6:

Range (µA) = 1000*VREF (v) / R6 (ohms)

where VREF into the Bt110 may be set by the internal 1.2v reference of the Bt110. Using this internal reference, the full scale gain error of the Bt110 is ± 10%. Table 2 shows resistor values for the circuit in Figure 7.

As the Bt110 has eight 8-bit DACs, it is capable of calibrating up to eight Bt604s.

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Tspan (ns)	R1 (ohms)	R2 (ohms)	Tmin Tempco (ps/°C.)	Tmax Tempco (ps/°C.)	Tspan Tempco (ps/°C.)
5	1000	1154	2.5	2.5	1.0
10	2000	2411	2.5	2.5	1.0
15	3300	3569	2.5	2.5	2.0
20	4700	4590	4.0	4.0	2.0

Table 1. Component Values for Figure 5.

Application Information (continued)

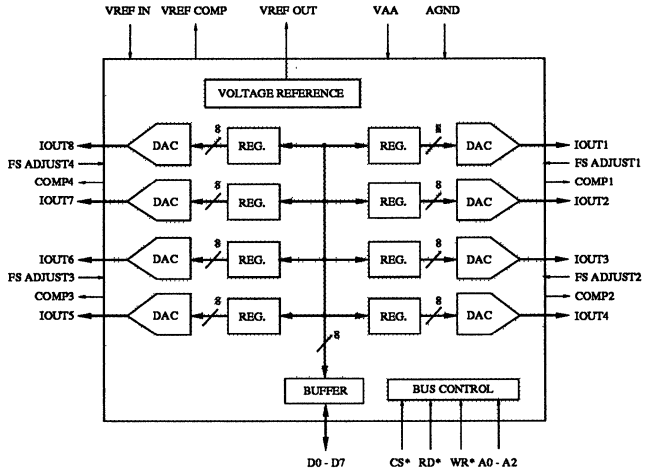


Figure 6. Block Diagram of the Bt110 Octal 8-Bit DAC.

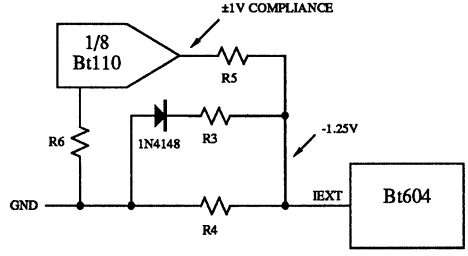


Figure 7. Tspan Calibration Using the Bt110.

Tspan (ns)	R3 (ohms)	R4 (ohms)	R5 (ohms)	R6 (ohms)	Nominal Range of Bt110 DAC (µA)
5	1000	1200	2500	1500	800
10	2000	2700	4500	2660	450
15	3300	3900	8100	4800	250
20	4700	4700	17000	10000	120

Table 2. Component Values for Figure 6.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	- 4.9	- 5.2	- 5.5	Volts
Reference Current	IEXT	150		2500	µA
Ambient Operating Temperature	TA	0		+ 70	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				- 8.0	Volts
Voltage on any Digital Pin		0		VEE	Volts
Output Current				- 30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	- 1170 - 1130 - 1070		- 840 - 810 - 735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	- 1950 - 1950 - 1950		- 1480 - 1480 - 1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	- 1020 - 980 - 920		- 840 - 810 - 735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	- 1950 - 1950 - 1950		- 1630 - 1630 - 1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 +25 +70		20 15 10		µA µA µA
Input Low Current (Vin = VILmin)	IIL	0 +25 +70	0.5 0.5 0.5			µA µA µA
Output Delay Spans Differential Linearity Error Integral Linearity Error	 DL IL				 ± 0.5 ± 1.0	 LSB LSB
VEE Supply Current	IEE			175		mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". OUT and OUT* loading with 50 ohms to -2.0v.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (note 1) Trigger Width High	Fmax Twi	 2		125	MHz ns
Output Pulse Width High Time Output Pulse Rise/Fall Time Output Pulse Spacing	Two Ts	 8	3 550	 750	ns ps ns
Output Delay Span Resolution Tempco (5 ns Span) Power Supply Rejection	 Tspan Tspan / 255 ΔTspan/°C.	 4 15.7	 6 80	 40 157	 ns ps ps / °C. ps / V
D0 - D7 Setup Time D0 - D7 Hold Time	Tdsu Tdh	2.0 1.5			ns ns
CE* Setup Time CE* Hold Time	Tsu Th	2.0 1.0			ns ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". ECL input values are -0.89 to -1.69 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 ohms to -2.0v.

Note 1: Maximum Trigger Rate:

Maximum Tspan (ns)	Minimum Trigger Period (ns)	Maximum Trigger Rate (MHz)
4.0	8	125
5.5	10	100
7.5	12.5	80
9.5	15	67
13.4	20	50
17.5	25	40
21.2	30	33
29.1	40	25
37.0	50	20

Maximum Tspan = ((33*Period) - 96) / 42

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt604KPJ	28-pin Plastic J-Lead	0° to +70° C.

Timing Waveforms

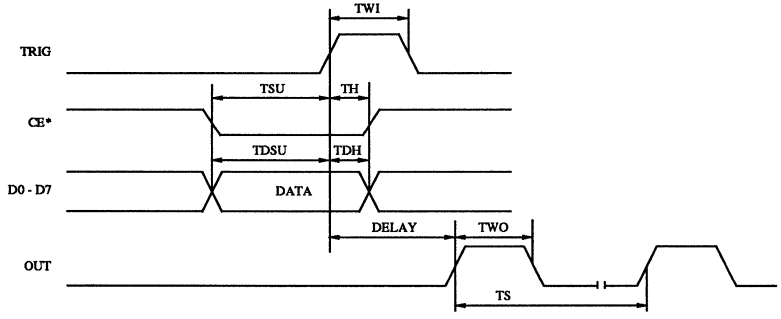


Figure 8. Input/Output Timing.

Bt605

125 MHz

10KH ECL Compatible

Programmable

Timing Edge Vernier

Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 125 MHz Maximum Trigger Rate
- Less than ± 1 LSB Timing Accuracy
- 15 ps Delay Resolution (4 ns Span)
- Extendable Delay Span to 40 ns
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package
- Typical Power Dissipation: 910 mW

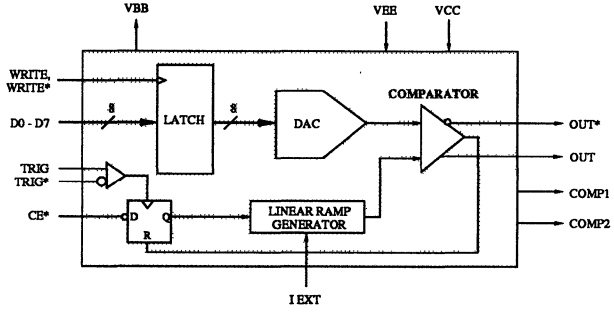
Applications

- Automatic Test Equipment
- Precision Timing Verniers
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt604, Bt606

Functional Block Diagram



Product Description

The Bt605 is a Programmable Timing Edge Vernier, whose time delay is loaded independently of triggering the circuit. In response to a trigger pulse, the Bt605 outputs a pulse of fixed width a programmable delay time later.

With the delay span set to 4 ns, the Bt605 features 15 ps of resolution (255 steps). The delay span is externally adjusted and is set in the range of 4 ns to 40 ns by IEXT.

Separate to triggering of the device, a new 8-bit value of delay is written in parallel (D0 - D7).

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger, output pulse, and write input.

In applications for Automatic Test Equipment (ATE), the Bt605 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy.

The Bt605 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

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Brooktree®

Circuit Description

As illustrated in the block diagram, the Bt605 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, the linear ramp determines the span of delay and the DAC's output sets the delay value. The programmed value of delay is written into the DAC input register via D0 - D7 and WRITE.

If CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG. The comparator detects when the ramp reaches the DACs programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Resetting the ramp permits another trigger of the Bt605.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0 - D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

$$Tspan = Tmax - Tmin$$

The output pulse delays are adjustable and are set by IEXT current flow through pin 12. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin.

Referring to Figure 4:

$$IEXT = (VEXT + 1.25v) / (REXT + 26\ ohms)$$

Output Pulse Spacing

Consecutive output pulses must be spaced no less than 8 ns apart.

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required to achieve maximum performance.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin - 500ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

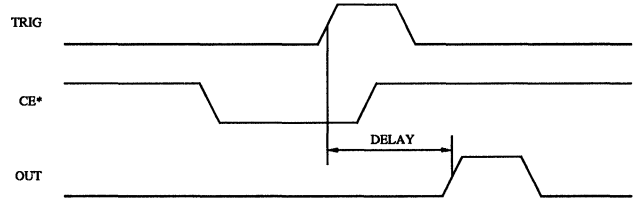


Figure 1. Delay Timing.

Circuit Description (continued)

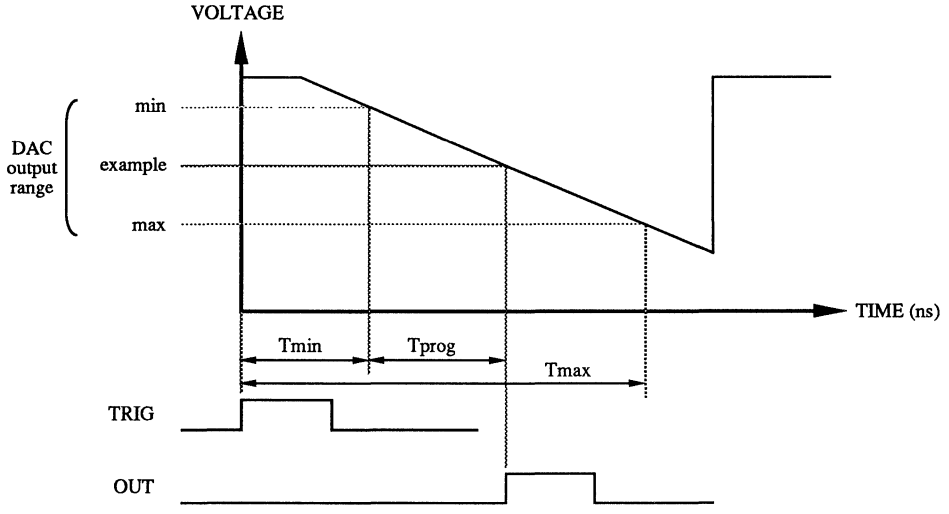


Figure 2. Linear Ramp and Output Pulse Timing.

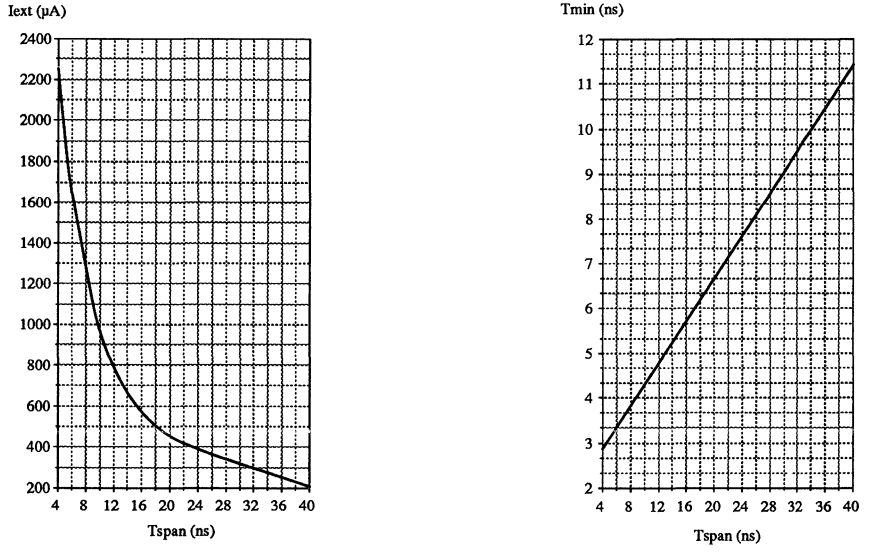
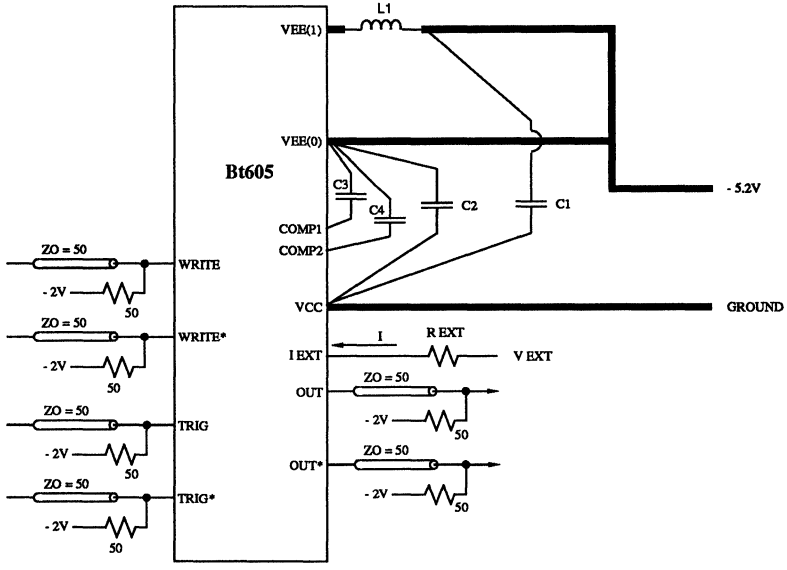


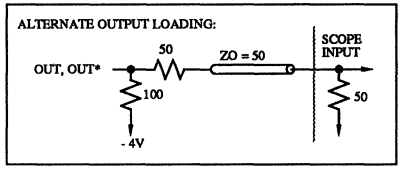
Figure 3. Typical Output Delays.

Circuit Description (continued)



with VEXT connected to VCC:

R EXT (ohms)	Tspan (ns)
700	5
1400	10
2800	20



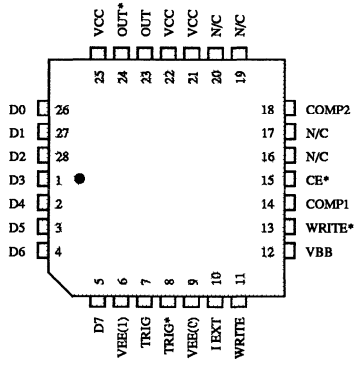
Location	Description	Vendor Part Number
C1 - C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
L1	ferrite chip bead	TDK 301210
REXT	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt605. All devices should be as close as possible to the Bt605.

Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0 - D7	Data input pins (ECL compatible). On the falling edge of WRITE, D0 - D7 are latched into the DAC input register. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.
WRITE, WRITE*	Differential write inputs (ECL compatible). These inputs control the parallel data input latch. When WRITE is a logical one, the data latch is transparent. Data is latched on the falling edge of WRITE. A single-ended write may be used by connecting WRITE* to VBB.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering is performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically -1.25v.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.
VEE	Device power. All VEE pins must be connected. **Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.**
VCC	Device ground. All VCC pins must be connected together.
VBB	-1.3v (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt605.

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The Bt605 exhibits small changes in Tspan with changes in temperature caused by temperature coefficient differences between the minimum time delay (tmin) and the maximum time delay (Tmax), where:

$$Tspan = Tmax - Tmin$$

Tspan is set with an external current source (usually a resistor to a voltage VEXT) as shown in Figure 4. The Tspan positive temperature coefficient can be partially compensated with an external network exhibiting a negative temperature coefficient consisting of two resistors and an inexpensive 1N4148 diode (see Figure 5). Resistors R1 and R2 are selected from Table 1 according to the Tspan desired. R1 and R2 are metal film resistors. R2 is selected or trimmed to obtain the desired Tspan.

The 2 mV/°C decrease in the forward voltage drop across the diode provides the necessary small changes in current. This network is most effective over a temperature range of 40 to 60 °C. Also shown in Table 1 are the temperature coefficients that can be expected over this temperature range for a 10° change in temperature. This is not a linear function in all cases. For example, with a 5 ns Tspan, Tmin may decrease from 40 to 50 °C. and then increase from 50 to 60 °C. As a result, values shown are absolute values.

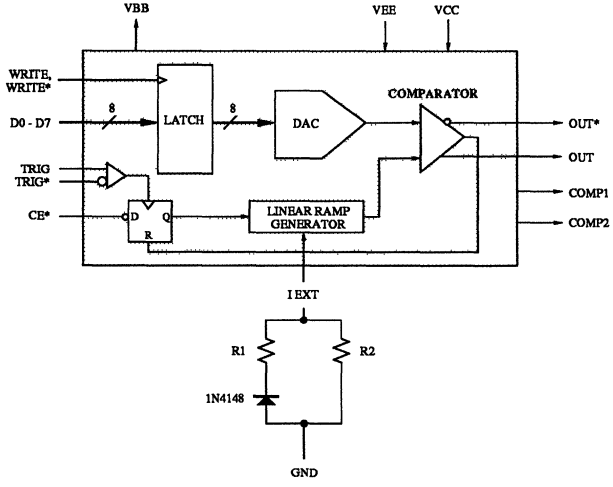

Figure 5. Typical Temperature Compensation Circuit.

Application Information (continued)

Tspan Calibration Using the Bt110

The accuracy and stability of the circuit providing the reference current (IEXT) directly affects the timing span accuracy. Computing values for R1 and R2 in Figure 5 results in a Tspan accuracy of better than ± 20%. This may require the adjustment or trimming of R2 to set Tspan to the precision required by the application. Using the Bt110 CMOS Octal 8-bit DAC can eliminate the need to trim resistors and provides a cost effective, low power solution to Tspan calibration. The block diagram of the Bt110 is shown in Figure 6.

For example, the Bt605 requires a nominal external current of 1780 µA for a Tspan of 5 ns. When the span is set of 5 ns, the Tspan/IEXT ratio is typically 2.80 ps/µA. Setting Tspan with resistor values as per Table 1 could result in a Tspan error of ± 20%, or ±1 ns. To correct for this error would require an adjustment of IEXT of ± 1 ns divided by 0.0028 ns/µA or ± 357 µA. If this IEXT adjustment is to be supplied by a DAC, then the full scale range would need to be 2 x 357 = 714 µA. An 8-bit DAC with this range would have a calibration resolution of 714 µA divided by 255 or 2.8 µA per bit. This represents a calibration resolution of 2.8 µA times 2.8 ps/µA or 7.84 ps.

This can be stated more simply as:

- Setting Tspan with resistors results in an error of ± x%.
- The Bt605 has 8 bits of resolution
- Calibrating with an 8-bit DAC results in a calibration resolution of 2x% of 1 LSB of the Bt605
- For Tspan = 5 ns
  1 LSB = 5 ns/255 = 19.6 ns
  Calibration resolution for ± x = ± 20% is
  0.4 x 19.6 = 7.84 ps

The circuit shown in Figure 7 implements the above using the Brooktree Bt110 CMOS Octal 8-bit DAC. Resistor R5 provides a voltage drop so that the ± 1v compliance range of the Bt110 is not exceeded; variations in R5 have no effect on IEXT.

The output range of the Bt110 is set by R6:

Range (µA) = 1000*VREF (v) / R6 (ohms)

where VREF into the Bt110 may be set by the internal 1.2v reference of the Bt110. Using this internal reference, the full scale gain error of the Bt110 is ± 10%. Table 2 shows resistor values for the circuit in Figure 7.

As the Bt110 has eight 8-bit DACs, it is capable of calibrating up to eight Bt605s.

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Tspan (ns)	R1 (ohms)	R2 (ohms)	Tmin Tempco (ps/°C.)	Tmax Tempco (ps/°C.)	Tspan Tempco (ps/°C.)
5	1000	1154	2.5	2.5	1.0
10	2000	2412	2.5	2.5	1.0
15	3300	3569	2.5	2.5	2.0
20	4700	4590	4.0	4.0	2.0

Table 1. Component Values for Figure 5.

Application Information (continued)

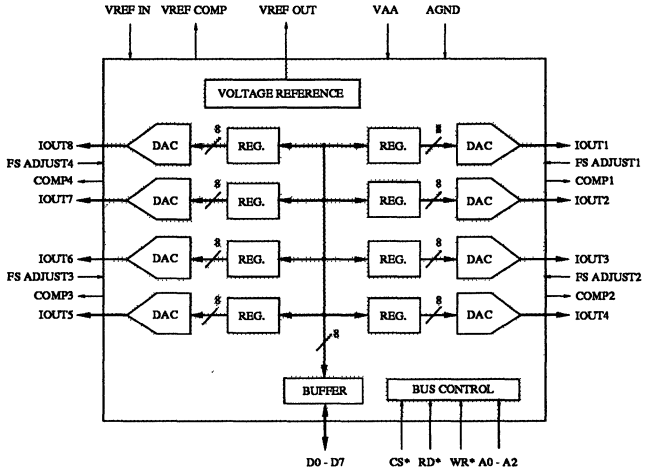


Figure 6. Block Diagram of the Bt110 Octal 8-Bit DAC.

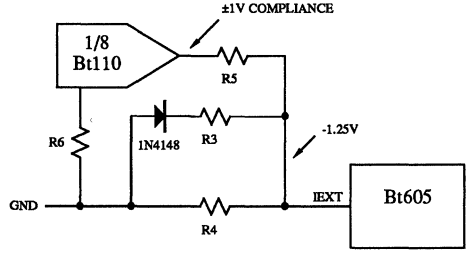


Figure 7. Tspan Calibration Using the Bt110.

Tspan (ns)	R3 (ohms)	R4 (ohms)	R5 (ohms)	R6 (ohms)	Nominal Range of Bt110 DAC (μA)
5	1000	1200	2500	1500	800
10	2000	2700	4500	2660	450
15	3300	3900	8100	4800	250
20	4700	4700	17000	10000	120

Table 2. Component Values for Figure 6.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	- 4.9	- 5.2	- 5.5	Volts
Reference Current	IEXT	150		2500	µA
Ambient Operating Temperature	TA	0		+ 70	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				- 8.0	Volts
Voltage on any Digital Pin		0		VEE	Volts
Output Current				- 30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 + 25 + 70	- 1170 - 1130 - 1070		- 840 - 810 - 735	mV mV mV
Input Low Voltage	VIL	0 + 25 + 70	- 1950 - 1950 - 1950		- 1480 - 1480 - 1450	mV mV mV
Output High Voltage	VOH	0 + 25 + 70	- 1020 - 980 - 920		- 840 - 810 - 735	mV mV mV
Output Low Voltage	VOL	0 + 25 + 70	- 1950 - 1950 - 1950		- 1630 - 1630 - 1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 + 25 + 70		20 15 10		µA µA µA
Input Low Current (Vin = VILmin)	IIL	0 + 25 + 70	0.5 0.5 0.5			µA µA µA
Output Delay Spans Differential Linearity Error Integral Linearity Error	 DL IL				 ± 0.5 ± 1.0	 LSB LSB
VEE Supply Current	IEE			175		mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". OUT and OUT* loading with 50 ohms to -2.0v.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (note 1) Trigger Width High	Fmax Twi	 2		125	MHz ns
Output Pulse Width High Time Output Pulse Rise/Fall Time Output Pulse Spacing	Two Ts	 8	3 550	 750	ns ps ns
Output Delay Span Resolution Tempco (5 ns Span) Power Supply Rejection	 Tspan Tspan / 255 ΔTspan/°C	 4 15.7	 6 80	 40 157	 ns ps ps / °C. ps / V
CE* Setup Time CE* Hold Time	Tsu Th	2.0 1.5			ns ns
WRITE Pulse Width High Time D0 - D7 Setup Time D0 - D7 Hold Time	Twh Tdsu Tdh	2 1 1.5			ns ns ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". ECL input values are -0.89 to -1.69 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 ohms to -2.0v.

Note 1: Maximum Trigger Rate:

Maximum Tspan (ns)	Minimum Trigger Period (ns)	Maximum Trigger Rate (MHz)
4.0	8	125
5.5	10	100
7.5	12.5	80
9.5	15	67
13.4	20	50
17.5	25	40
21.2	30	33
29.1	40	25
37.0	50	20

Maximum Tspan = ((33*Period) - 96) / 42

Timing Waveforms

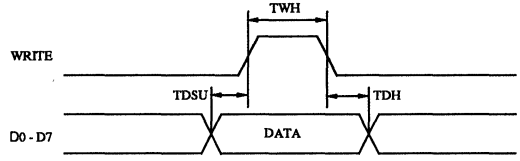


Figure 8. Parallel Load Timing.

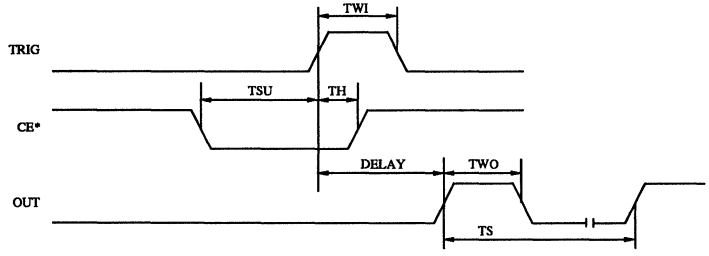


Figure 9. Delay Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt605KPJ	28-pin Plastic J-Lead	0° to +70° C.

Bt606

20 ns to 200 ns Span

10KH ECL Compatible

Programmable

Timing Edge Delay

Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 20 ns to 200 ns Delay Span Selection
- Less than ± 1 LSB Timing Accuracy
- 30 MHz Maximum Trigger Rate
- Span Programmable Externally
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package
- Typical Power Dissipation: 910 mW

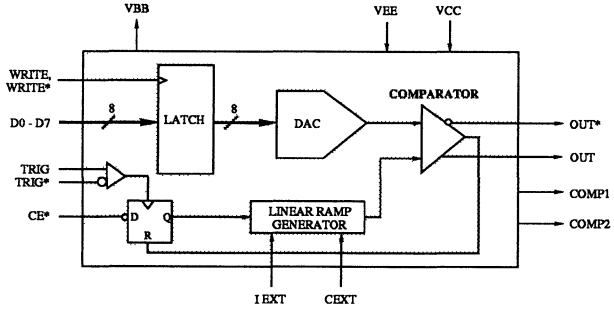
Applications

- Automatic Test Equipment
- Precision Timing Delays
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt604, Bt605

Functional Block Diagram



Product Description

The Bt606 is a Programmable Timing Edge Delay, whose time delay is loaded independently of triggering the circuit. In response to a trigger pulse, the Bt606 outputs a pulse of fixed width a programmable delay time later.

The minimum output delay span is 20 ns in 255 steps. The Bt606 is designed to be used for spans up to 200 ns, where the delay range is set by CEXT and may be further programmed and finally adjusted by IEXT.

Separate to triggering of the device, a new 8-bit value of delay is written in parallel (D0 - D7).

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger, output pulse, and write input.

In applications for Automatic Test Equipment (ATE), the Bt606 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy.

The Bt606 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

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Brooktree®

Circuit Description

As illustrated in the block diagram, the Bt606 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, the linear ramp determines the span of delay and the DAC's output sets the delay value. The programmed value of delay is written into the DAC input register via D0 - D7 and WRITE.

If CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG. The comparator detects when the ramp reaches the DACs programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Resetting the ramp permits another trigger of the Bt606.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0 - D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

$$Tspan = Tmax - Tmin$$

The actual output delay range is determined by CEXT. The output pulse delays are further adjustable by IEXT. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin for various values of CEXT.

Referring to Figure 4:

$$IEXT = (VEXT + 1.25v) / (REXT + 26\ ohms)$$

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required to achieve maximum performance.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin - 500ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

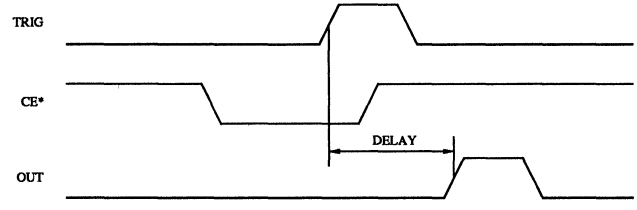


Figure 1. Delay Timing.

Circuit Description (continued)

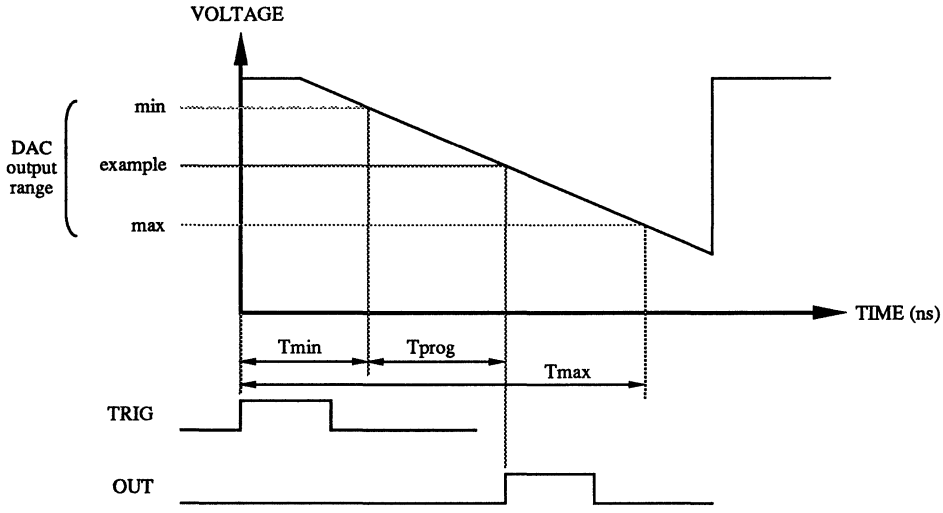


Figure 2. Linear Ramp and Output Pulse Timing.

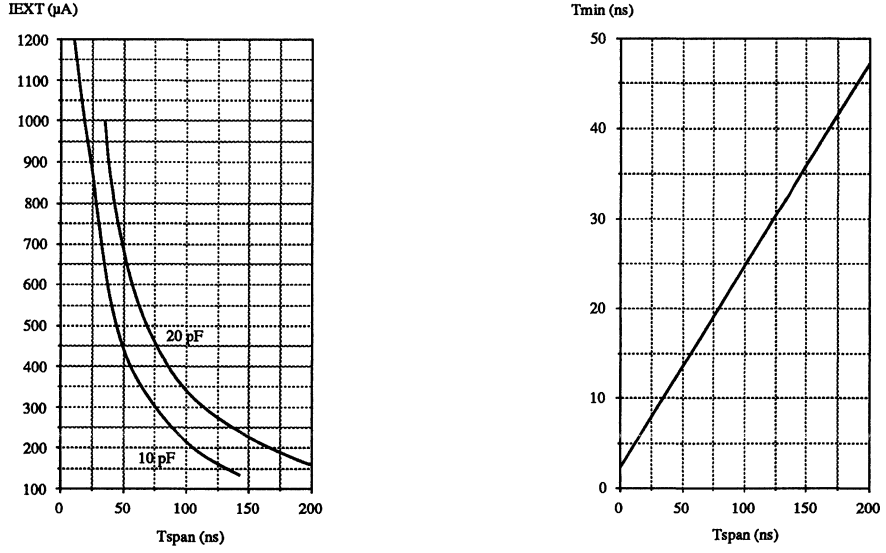
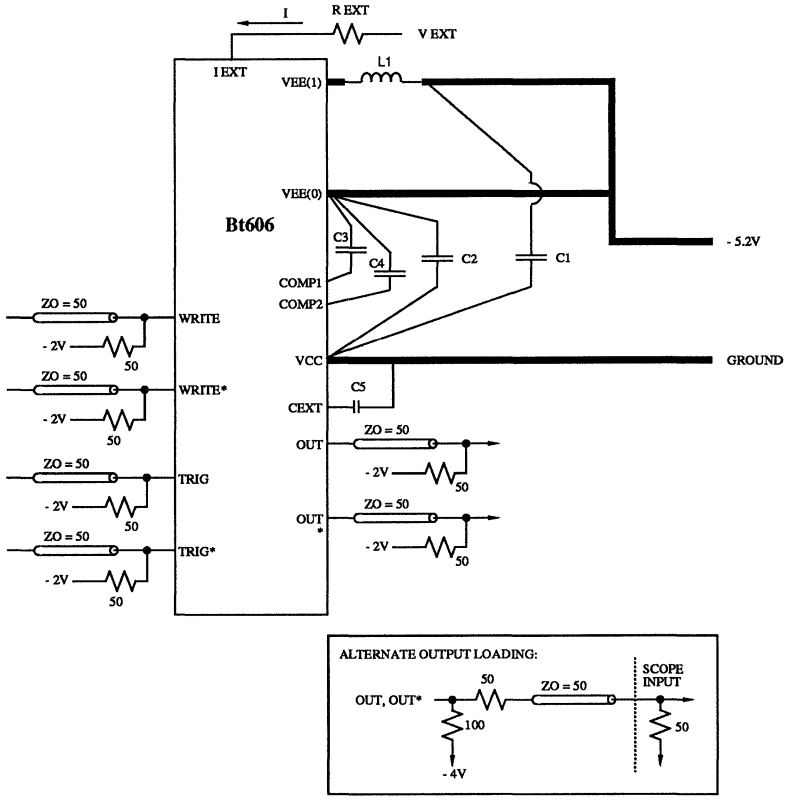


Figure 3. Typical Output Delays.

Circuit Description (continued)



Location	Description	Vendor Part Number
C1 - C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
L1	ferrite chip bead	TDK 301210
REXT	1% metal film resistor	Dale CMF-55C
C5	5 pF to 20 pF ceramic chip capacitor	

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt606. All devices should be as close as possible to the Bt606.

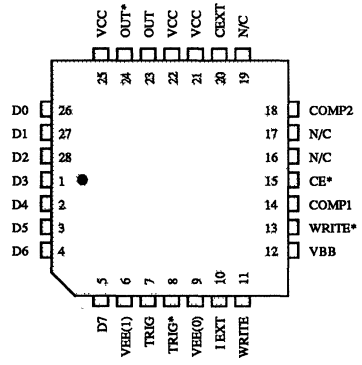
Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0 - D7	Data input pins (ECL compatible). On the falling edge of WRITE, D0 - D7 are loaded into the DAC input register. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.
WRITE, WRITE*	Differential write inputs (ECL compatible). These inputs control the parallel data input latch. When WRITE is a logical one, the data latch is transparent. Data is latched on the falling edge of WRITE. A single-ended write may be used by connecting WRITE* to VBB.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering is performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically -1.25v.
CEXT	External capacitor pin. The amount of capacitance between this pin and VCC determines the delay range.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.

Pin Descriptions (continued)

Pin Name	Description
VEE	Device power. All VEE pins must be connected. **Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.**
VCC	Device ground. All VCC pins must be connected together.
VBB	-1.3v (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt606.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	- 4.9	- 5.2	- 5.5	Volts
Reference Current	IEXT	150		2500	µA
Ambient Operating Temperature	TA	0		+ 70	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				- 8.0	Volts
Voltage on any Digital Pin		0		VEE	Volts
Output Current				- 30	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	- 1170 - 1130 - 1070		- 840 - 810 - 735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	- 1950 - 1950 - 1950		- 1480 - 1480 - 1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	- 1020 - 980 - 920		- 840 - 810 - 735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	- 1950 - 1950 - 1950		- 1630 - 1630 - 1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 +25 +70		10 10 10		µA µA µA
Input Low Current (Vin = VILmin)	IIL	0 +25 +70	0.5 0.5 0.5			µA µA µA
Output Delay Spans Differential Linearity Error Integral Linearity Error	 DL IL				 ± 0.5 ± 1.0	 LSB LSB
VEE Supply Current	IEE			175		mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". OUT and OUT* loading with 50 ohms to -2.0v.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (note 1) Trigger Width High	Fmax Twi	 2		30	MHz ns
Output Pulse Width High Time Output Pulse Rise/Fall Time	Two		3 550	 750	ns ps
Output Delay Span Resolution Tempco (20 ns Span) Power Supply Rejection	 Tspan Tspan / 255 ΔTspan/°C	 20 78.4	 tbd 80	 200 784	 ns ps ps / °C. ps / V
CE* Setup Time CE* Hold Time	Tsu Th	2.0 1.5			ns ns
WRITE Pulse Width High Time D0 - D7 Setup Time D0 - D7 Hold Time	Twh Tdsu Tdh	2.0 1.0 1.5			ns ns ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". ECL input values are -0.89 to -1.69 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 ohms to -2.0v.

Note 1: Maximum Trigger Rate:

CEXT	Tspan (ns)	Maximum Trigger Rate (MHz)	CEXT	Tspan (ns)	Maximum Trigger Rate (MHz)
10 pF	20	30	20 pF	75	8
	30	20		100	6
	40	15		125	5
	50	12		150	4.3
	60	10		175	3.7
	80	7.5		200	3.3
	100	6			

Timing Waveforms

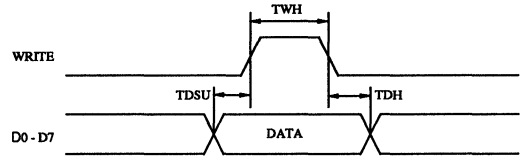


Figure 5. Parallel Load Timing.

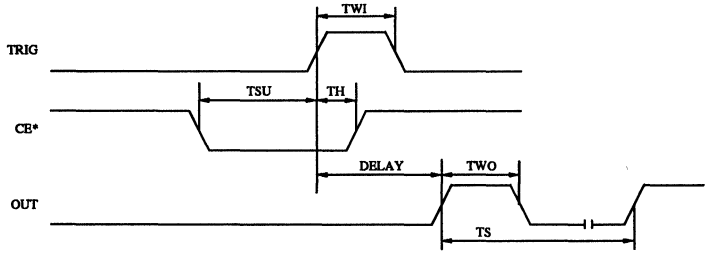


Figure 6. Delay Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt606KPJ	28-pin Plastic J-Lead	0° to +70° C.

Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

Bt687

Ultra Fast
10KH ECL Compatible
Dual Comparator

Distinguishing Features

- 1.8 ns Maximum Propagation Delay
- 0.8 ns Latch Setup Time
- 0.0 ns Latch Hold Time
- 250 MHz Bandwidth
- 38 dB Gain at 500 MHz
- ± 3.3v Common Mode Range
- +5v, -5.2v Power Supplies
- 10KH ECL Compatible
- 16-pin DIP or 20-pin LCC Package
- Typical Power Dissipation: 280 mW

Applications

- Automatic Test Equipment
- Instrumentation
- Window Comparators
- Line Receivers
- Threshold Detection

Related Products

- Bt688, Bt689

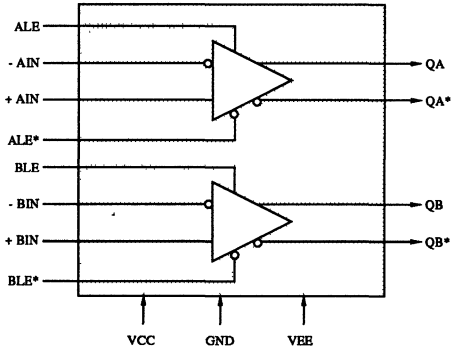
Product Description

The Bt687 is an ultra-fast dual comparator, compatible to other '687-type devices. It is manufactured with a high performance bipolar process and can drive 50-ohm terminated transmission lines.

Each comparator has a latch function, with differential inputs, for sampling of input waveforms. Outputs are latched when LE is a logical zero and LE* is a logical one.

The Bt687 has the gain and bandwidth to track very fast input signals, and offers significant improvements in timing accuracy over existing comparators.

Functional Block Diagram



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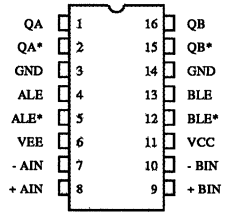
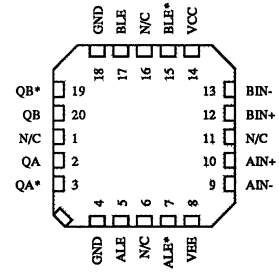
Pin Descriptions

Pin Name	Description
AIN+, AIN-, BIN+, BIN-	Differential analog inputs. AIN+ and BIN+ are noninverting while AIN- and BIN- are inverting. If a comparator is not used, the inputs must be at least one diode drop apart (within the recommended common mode range) to force the outputs to a fixed state, the LE* input should be connected to GND, the LE input may remain floating.
QA, QA*, QB, QB*	Differential outputs (ECL compatible).
ALE, ALE*, BLE, BLE*	Differential latch enable inputs (ECL compatible). In the compare mode (LE = logical one and LE* = logical zero), Q and Q* will track changes at the IN+ and IN- inputs. In the latch mode (LE = logical zero and LE* = logical one), Q and Q* will reflect the input state of IN+ and IN- just prior to switching to the latch mode. The compare mode may be continuously enabled by grounding LE and floating LE*.
GND	Ground. All GND pins must be connected together as close to the device as possible.
VCC	Positive supply, typically +5v.
VEE	Negative supply, typically -5.2v.

16-pin DIP Package



20-pin Ceramic Leadless Chip Carrier Package



Application Information

Power Supply Decoupling

Both the VCC and VEE supply pins should be separately decoupled to GND with a 0.1 μF ceramic chip capacitor in parallel with a 0.001 μF chip capacitor. The bypass capacitors should be as close as possible to the device.

A ground plane is recommended to provide a low inductance ground return path.

ECL Terminations

The Bt687 has open-emitter outputs, thus, they must be terminated through 50-ohm resistors to -2v or the equivalent. Microstrip layout techniques are recommended. The impedance at the inputs should be as low as possible, and lead lengths kept to a minimum.

Hysteresis Control

An alternate use of the latch enable inputs is as a hysteresis control. By varying the differential voltage between LE and LE*, small variations in the hysteresis may be attained.

For example, there is minimal hysteresis when the differential voltage between LE and LE* is large (e.g. LE grounded and LE* is floating). With both LE and LE* grounded, then a small (less than 10 mV) switching hysteresis may be achieved.

Delay Dispersion

Given a constant temperature and voltage environment (within the bounds of the Recommended Operating Conditions), the dispersion parameter (TSD) indicates how much propagation delay time variation can be expected for one comparator when given a wide range of input conditions.

The input conditions are defined in terms of slew rate and input threshold. A set of "typical" ECL and TTL waveforms were defined and a separate group of dispersion parameters measured for each. These sets of waveforms are shown in Figures 2 and 3.

Given any combination of input slew rate and input threshold within the bounds described in Figures 2 and 3, timing characteristics can be described as:

$$TNOM \pm TSD$$

where TNOM is the nominal delay or setup time which will vary with temperature, voltage, and package type, and will vary from part to part. In all state-of-the-art Automated Test Equipment applications, TNOM is calibrated. TSD includes factors which normally are not taken into account when doing system calibration.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	4.75	5.00	5.25	Volts
Negative Power Supply	VEE	- 4.90	- 5.20	- 5.50	Volts
Ground	GND		0		Volts
Ambient Operating Temperature	TA	- 25		+ 85	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (relative to GND)				7.0	Volts
VEE (relative to GND)				- 8.0	Volts
Input Voltages					
- AIN, + AIN, - BIN, + BIN		VEE		VCC	Volts
ALE, ALE*, BLE, BLE*		VEE		+ 1.0	Volts
Differential Input Voltage				± 6.0	Volts
Output Current				- 50	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Digital Input High Voltage*	VIH	- 25 + 25 + 85	- 1210 - 1130 - 1060		- 870 - 810 - 720	mV mV mV
Digital Input Low Voltage*	VIL	- 25 + 25 + 85	- 1950 - 1950 - 1950		- 1510 - 1480 - 1445	mV mV mV
Digital Output High Voltage*	VOH	- 25 + 25 + 85	- 1060 - 980 - 910		- 870 - 810 - 720	mV mV mV
Digital Output Low Voltage*	VOL	- 25 + 25 + 85	- 1950 - 1950 - 1950		- 1660 - 1630 - 1595	mV mV mV
Analog Input Voltage Range*	VCM		- 3.3		+ 3.3	Volts
Analog Input Offset Voltage** Tempco**	VOS VOSTC				± 5 5	mV µV / °C.
Analog Input Bias Current Analog Input Offset Current	IB IOS				± 20 ± 5	µA µA
Analog Input Resistance Analog Input Capacitance	RIN CIN		100	 2		K ohms pF
Digital Input Current (Vin = VIHmax, VILmin)	IIN				70	µA
Common Mode Rejection Ratio	CMRR		70			dB
Power Supply Rejection Ratio	PSRR		60			dB
VCC Supply Current VEE Supply Current	ICC IEE			30 25	45 38	mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with QA, QA*, QB, and QB* loading of 50 ohms to -2.0v.

*Relative to GND.

**Rs ≤ 100 ohms.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays (note 1)					
Input to Output High	TPD+			1.8	ns
Input to Output Low	TPD-			1.8	ns
Delay Dispersion (note 2)	TSD		± 75		ps
Propagation Delay Tempco					
Input to Output	TPDTC		4		pS / °C.
Latch Enable to Output	TENTC		4		pS / °C.
Propagation Delay Skew (note 3)			80		ps
Latch Enable Setup Time	TS	0.8			ns
Latch Enable Hold Time	TH	0			ns
Latch Enable Pulse Width	TPW	1.5			ns
Latch Enable to Output High	TPD+(E)			1.5	ns
Latch Enable to Output Low	TPD-(E)			1.5	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C. and QA, QA*, QB, and QB* loading of 50 ohms to -2.0v. Timing reference points at 50% for Q and Q* outputs and latch enable inputs.

Note 1: Input to Output propagation delays (at standard test levels) specify the delay measured from the time the input signal crosses the input offset voltage (VOS) to the 50% point of a HIGH or LOW output transition. Vin = 1 volt, Vod = 100 mV, Fin = 10 MHz, Tr and Tf = 1v/ns measured between the 20% and 80% points.

Note 2: Delay dispersion refers to both TTL and ECL signal dispersion.

TTL dispersion: Input to output propagation delay dispersion of a given part for 2.5v TTL signals (see Figure 2). Input threshold range is between the 20% and 80% points for slew rates between 0.25v/ns to 1v/ns for both rising and falling edges. Outputs are measured at the Q and Q* cross point.

ECL dispersion: Input to output propagation delay dispersion of a given part for 1v ECL signals (see Figure 3). Input threshold range is between the 20% and 80% points for slew rates between 0.25v/ns to 1v/ns for both rising and falling edges. Outputs are measured at the Q and Q* cross point.

Note 3: Comparator A to comparator B delay skew in a given part under the same conditions, with latches transparent.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Timing Waveforms

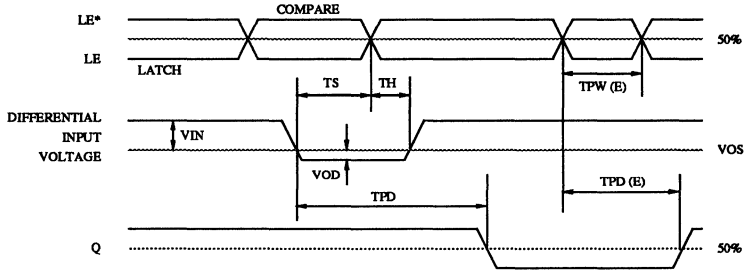


Figure 1. Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt687BC	16-pin CERDIP	-25° to +85° C.
Bt687BL	20-pin Ceramic Leadless Chip Carrier	-25° to +85° C.

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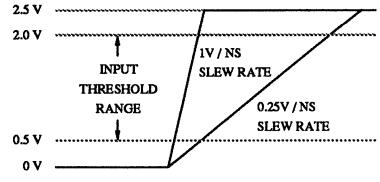
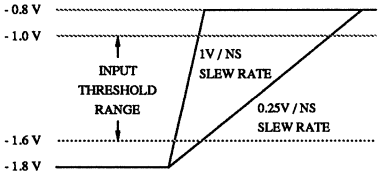
Timing Waveforms (continued)



Note: Test conditions include both rising and falling edges.

Figure 2. TTL Dispersion Test Input Conditions.



Note: Test conditions include both rising and falling edges.

Figure 3. ECL Dispersion Test Input Conditions.

Bt688

Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

High Speed

10KH ECL Compatible

Wide Input Voltage

Dual Comparator

Distinguishing Features

- +8.2v, -2.2v Common Mode Range with +8v, -6.2v Supplies
- Operates down to +5v, -5.2v Supplies
- Typical Input Bias Current < 2 µA
- 2.8 ns Maximum Propagation Delay
- 1.2 ns Latch Setup Time
- 0 ns Latch Hold Time
- 40 dB Gain at 300 MHz
- 10KH ECL Compatible
- Bt687 Pin Compatible
- 16-pin Plastic DIP or 20-pin LCC Package
- Typical Power Dissipation: 250mW to 365mW depending on Power Supplies

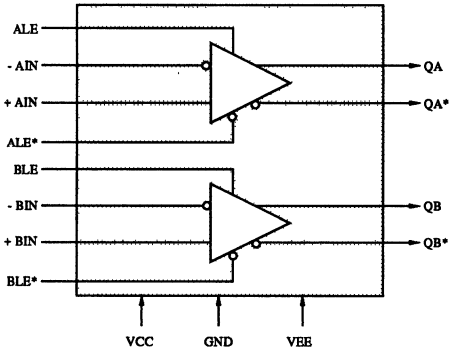
Applications

- Automatic Test Equipment
- Instrumentation
- Window Comparators
- Line Receivers
- Threshold Detection

Related Products

- Bt687
- Bt689

Functional Block Diagram



Product Description

The Bt688 is an extremely fast dual comparator, designed with a wide input voltage range allowing direct interfacing to TTL or ECL input signals. It is manufactured with a high performance bipolar process and can drive 50-ohm terminated transmission lines.

Each comparator has a latch function, with differential inputs, for sampling of input waveforms. Outputs are latched when LE is a logical zero and LE* is a logical one.

In the application of Automatic Test Equipment (ATE), the Bt688 provides the function of the Pin Electronics Comparator, having sufficient voltage range and low bias current to monitor output from ECL, TTL, and CMOS devices under test. The Bt688 eliminates the need for a buffer amplifier between the comparator and the device under test.

As a Pin Electronics Comparator (and in similar applications), the Bt688 will be more cost effective, faster and have much improved timing accuracy than solutions requiring a comparator and an additional input buffer.

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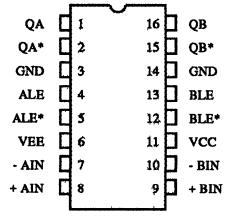
Brooktree®

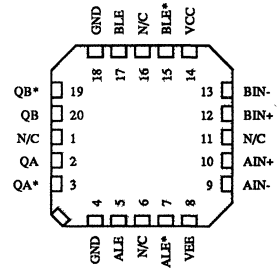
Pin Descriptions

Pin Name	Description
AIN+, AIN-, BIN+, BIN-	Differential analog inputs. AIN+ and BIN+ are noninverting while AIN- and BIN- are inverting. If a comparator is not used, the inputs must be at least one diode drop apart (within the recommended common mode range) to force the outputs to a fixed state, the LE* input should be connected to GND, the LE input may remain floating.
QA, QA*, QB, QB*	Differential outputs (ECL compatible).
ALE, ALE*, BLE, BLE*	Differential latch enable inputs (ECL compatible). In the compare mode (LE = logical one and LE* = logical zero), Q and Q* will track changes at the IN+ and IN- inputs. In the latch mode (LE = logical zero and LE* = logical one), Q and Q* will reflect the input state of IN+ and IN- just prior to switching to the latch mode. The compare mode may be continuously enabled by floating LE* and connecting LE to any valid ECL input voltage (logical one or zero).
GND	Ground. All GND pins must be connected together as close to the device as possible.
VCC	Positive supply, typically +8.0v.
VEE	Negative supply, typically -6.2v.
	Note: The Bt688 may operate over a wide range of power supply voltages.

16-pin DIP Package



20-pin Ceramic Leadless Chip Carrier Package



Application Information

Power Supply Decoupling

Both the VCC and VEE supply pins should be separately decoupled to GND with a 0.1 µF ceramic chip capacitor in parallel with a 0.001 µF chip capacitor. The bypass capacitors should be as close as possible to the device.

A ground plane is recommended to provide a low inductance ground return path.

ECL Terminations

The Bt688 has open-emitter outputs, thus, they must be terminated through 50-ohm resistors to -2v or the equivalent. Microstrip layout techniques are recommended. The impedance at the inputs should be as low as possible, and lead lengths kept to a minimum.

Hysteresis Control

An alternate use of the latch enable inputs is as a hysteresis control. By varying the differential voltage between LE and LE*, small variations in the hysteresis may be achieved. For example, there is minimal hysteresis when the differential voltage between LE and LE* is large (e.g. LE logical 1, and LE* is at logical zero). With both LE and LE* at the same potential, 10mV switching hysteresis may be achieved.

Input Protection

Figure 1 shows a means for input protection when the Bt688 is used in the application as a Pin Electronics Comparator. The Bt688 inputs have intrinsic diode clamps to the VCC and VEE supplies. All that is needed is the current limiting network as indicated to protect the inputs from overvoltage. Such schemes may be implemented with the Bt688 due to its high differential input range.

Delay Dispersion

Given a constant temperature and voltage environment (within the bounds of the Recommended Operating Conditions), the dispersion parameter (TSD) indicates how much propagation delay time variation can be expected for one comparator when given a wide range of input conditions.

The input conditions are defined in terms of slew rate and input threshold. A set of "typical" ECL and TTL waveforms were defined and a separate group of of dispersion parameters measured for each. These sets of waveforms are shown in Figures 3 and 4.

Given any combination of input slew rate and input threshold within the bounds described in Figures 3 and 4, timing characteristics can be described as:

$$TNOM \pm TSD$$

where TNOM is the nominal delay or setup time which will vary with temperature, voltage, and package type, and will vary from part to part. In all state-of-the-art Automated Test Equipment applications, TNOM is calibrated. TSD includes factors which normally are not taken into account when doing system calibration.

9

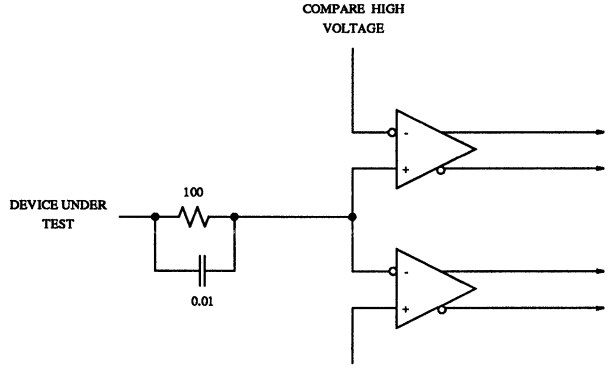


Figure 1. Typical Input Protection Circuit.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	4.5	8.0	8.5	Volts
Negative Power Supply	VEE	- 4.2	- 6.2	- 6.6	Volts
Ground	GND		0		Volts
Ambient Operating Temperature	TA	0		+ 70	°C.

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (relative to GND)				tbd	Volts
VEE (relative to GND)				- tbd	Volts
Input Voltages					
- AIN, + AIN, - BIN, + BIN		VEE - 0.7		VCC + 0.7	Volts
ALE, ALE*, BLE, BLE*		VEE		+1.0	Volts
Differential Input Voltage					
AIN, BIN				± 16.0	Volts
ALE, BLE				± 6.0	Volts
Output Current				- 50	mA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Digital Input High Voltage*	VIH	0 +25 +70	- 1170 - 1130 - 1070		- 840 - 810 - 735	mV mV mV
Digital Input Low Voltage*	VIL	0 +25 +70	- 1950 - 1950 - 1950		- 1480 - 1480 - 1450	mV mV mV
Digital Output High Voltage*	VOH	0 +25 +70	- 1020 - 980 - 920		- 840 - 810 - 735	mV mV mV
Digital Output Low Voltage*	VOL	0 +25 +70	- 1950 - 1950 - 1950		- 1630 - 1630 - 1600	mV mV mV
Analog Input Voltage Range*	VCM		VEE+ 4.0		VCC+ 0.2	Volts
Analog Input Offset Voltage** Tempco**	VOS VOSTC				±5 5	mV µV/°C.
Analog Input Bias Current (note 1) Analog Input Offset Current	IB IOS			1.8	5 2	µA µA
Analog Input Capacitance	CIN			2		pF
Digital Input Current (Vin = VIHmax, VILmin)	IIN				20	µA
Common Mode Rejection Ratio	CMRR		70			dB
Power Supply Rejection Ratio	PSRR		70			dB
VCC Supply Current VEE Supply Current	ICC IEE			16 38	24 55	mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with QA, QA*, QB, and QB* loading of 50 ohms to -2.0v.

*Relative to GND.

**Rs ≤ 100 ohms.

Note 1: IB nominal @ 5v differential with one input at 0v and the other input at 5v. Supply condition with VCC = 8.0v and VEE = - 6.2v.

IB worst case @ 10.9v differential with one input at 8.7v (Maximum Operating Condition) and the other input at - 2.2v. Supply condition with VCC = 8.5v and VEE = - 6.6v.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays (note 1)					
Input to Output High	TPD+			2.8	ns
Input to Output Low	TPD-			2.8	ns
Delay Dispersion (note 2)	TSD		± 150		ps
Propagation Delay Tempco					
Input to Output	TPDTC		7		pS / °C.
Latch Enable to Output	TENTC		7		pS / °C.
Propagation Delay Skew (note 3)			100		ps
Latch Enable Setup Time	TS	1.2			ns
Latch Enable Hold Time	TH	0			ns
Latch Enable Pulse Width	TPW	1.5			ns
Latch Enable to Output High	TPD+(E)			2.0	ns
Latch Enable to Output Low	TPD-(E)			2.0	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C. and QA, QA*, QB, and QB* loading of 50 ohms to -2.0v. Timing reference points at 50% for Q and Q* outputs and latch enable inputs.

Note 1: Input to Output propagation delays (at standard test levels) specify the delay measured from the time the input signal crosses the input offset voltage (VOS) to the 50% point of a HIGH or LOW output transition. Vin = 1 volt, Vod = 100 mV, Fin = 10 MHz, Tr and Tf = 1v/ns measured between the 20% and 80% points.

Note 2: Delay dispersion refers to both TTL and ECL signal dispersion.

TTL dispersion: Input to output propagation delay dispersion of a given part for 2.5v TTL signals (see Figure 2). Input threshold range is between the 20% and 80% points for slew rates between 0.25v/ns to 1v/ns for both rising and falling edges. Outputs are measured at the Q and Q* cross point.

ECL dispersion: Input to output propagation delay dispersion of a given part for 1v ECL signals (see Figure 3). Input threshold range is between the 20% and 80% points for slew rates between 0.25v/ns to 1v/ns for both rising and falling edges. Outputs are measured at the Q and Q* cross point.

Note 3: Comparator A to comparator B delay skew in a given part under the same conditions, with latches transparent.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Timing Waveforms

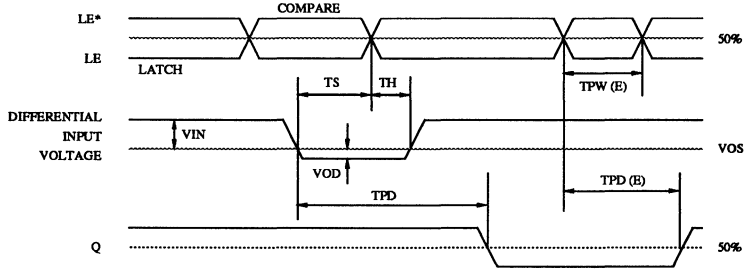


Figure 2. Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt688KP	16-pin Plastic DIP	0° to +70° C.
Bt688KL	20-pin Ceramic Leadless Chip Carrier	0° to +70° C.

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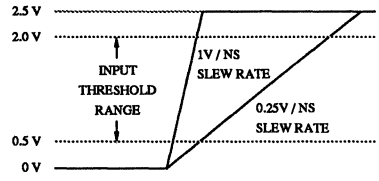
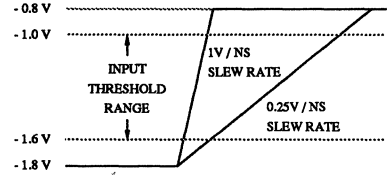
Timing Waveforms (continued)



Note: Test conditions include both rising and falling edges.

Figure 3. TTL Dispersion Test Input Conditions.



Note: Test conditions include both rising and falling edges.

Figure 4. ECL Dispersion Test Input Conditions.

Bt689

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Extremely Fast

10KH ECL Compatible

Programmable Pin

Electronics Driver/Load

Distinguishing Features

- +8v, -2v Programmable Output Voltage
- 60 mA Programmable Output Current
- Programmable as Pin Electronics Driver or Load
- > 100 MHz Operation
- 2v/ns Typical Rise/Fall Times
- Drives 50-Ohm to 100-Ohm Lines
- 10KH ECL Compatible Inputs
- 32-pin Ceramic Flatpack Package with Heatsink

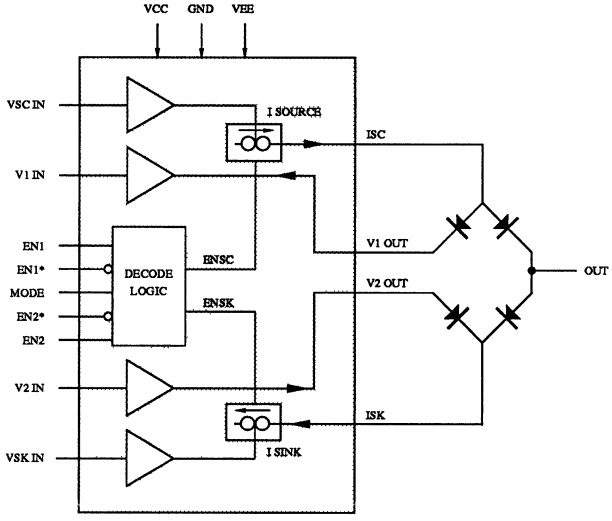
Applications

- Automatic Test Equipment
- Instrumentation

Related Products

- Bt687, Bt688

Functional Block Diagram



Product Description

The Bt689 is configurable as either a programmable Pin Electronics Driver or Pin Electronics Load circuit.

The Bt689 provides programmable source (ISC) and sink (ISK) currents (up to 60 mA) and buffered voltage outputs (V1 OUT and V2 OUT) programmable in the range -2v to +8v. All current and voltage outputs are set independently by voltages into high impedance amplifiers.

Differential ECL inputs, EN1 and EN2, switch either or both ISC and ISK on or off. The ECL compatible MODE input determines the function of EN1 and EN2.

Configured as a Pin Electronics Driver, the Bt689 can drive 50- to 100-ohm transmission lines, with programmable output voltage levels of -2v to +8v. The programmable currents permit adjustment of current drive up to 60 mA and also permit some adjustment of output rise/fall times.

Configured as a Pin Electronics Load, the Bt689 is designed to provide switched, programmable source and sink currents (up to 60 mA). The voltage compliance is programmable from -2v to +8v.

In the application of Automatic Test Equipment (ATE), the Bt689 provides the ability to construct programmable Pin Electronics Drivers and Loads having a wide voltage and current range for interfacing to ECL, TTL, and CMOS devices under test. The speed of the Bt689 allows use in testers that have greater than 100 MHz test rates.

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Bt698

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

Extremely Fast
10KH ECL Compatible
Pin Electronics
Driver and Comparator

Distinguishing Features

- Includes both a Pin Electronics Three-State Driver and Comparator
- > 100 MHz Operation
- +8, -2v Programmable Output Voltages
- 60 mA Programmable Output Current
- Programmable Rise/Fall Times up to 2v/ns
- 2.6 ns Comparator Propagation Delay
- +8.2v, -2.2v Input Voltage Range
- Programmable Comparator Hysteresis
- 32-pin Ceramic Flatpack Package with Heatsink

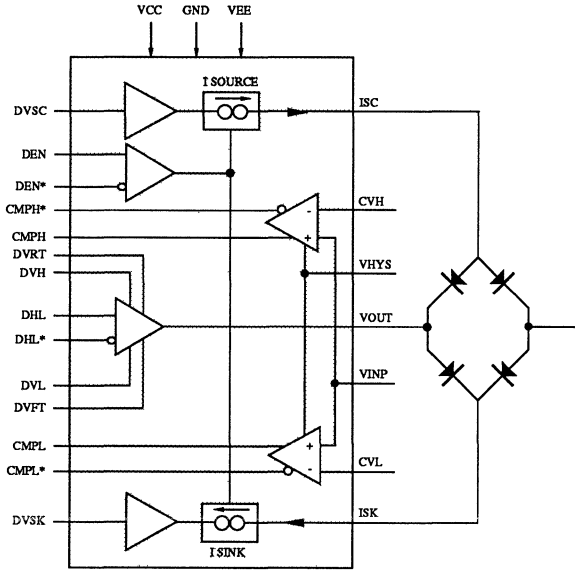
Applications

- Automatic Test Equipment
- Instrumentation

Related Products

- Bt687, Bt688
- Bt689

Functional Block Diagram



Product Description

The Bt698 includes both an extremely fast, flexible and programmable Pin Electronics Driver and Comparator.

Using an external diode bridge, the Bt698 forms a Pin Electronics Driver which can drive 50- to 100-ohm transmission lines. The differential ECL input (DHL) switches the output (VOUT) between the high (DVH) and low (DVL) levels programmable in the range of +8v to -2v. The output rise and fall times are independently programmed by input voltages DVRT and DVFT respectively, in the range of 0.2 v/ns to 2 v/ns. Programmable source (ISC) and sink (ISK) output currents (up to 60 mA) are enabled or disabled by the differential ECL input, DEN, so as to form a three-statable driver.

The Bt698 Dual Comparator's wide input common mode and high input impedance allow direct interfacing to the device under test without the need for an external buffer. The high (CVH) and low (CVL) compare levels are programmable in the range of +8.2v to -2.2v. Differential ECL outputs, CMPH and CMPL, and can drive 50-Ohm transmission lines. Compare hysteresis is programmed by VHYS.

In the application of Automatic Test Equipment (ATE), the Bt698's voltage and current ranges (power and appropriate package) may be selected to provide the desired Pin Electronics Driver and Comparator for testing ECL, TTL and CMOS devices to greater than 100 MHz test rates. Brooktree's Bt689 is compatible with the Bt698 for applications requiring a Pin Electronics Load.

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Table of Contents

Bt104/105

40 ns

Monolithic CMOS

12-bit

D/A Converter

Distinguishing Features

- 40 ns Maximum Settling Time
- Registered Data Inputs (Bt105)
- ± 1/2 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- TTL Compatible Inputs
- +5v CMOS Monolithic Construction
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 300 mW

Applications

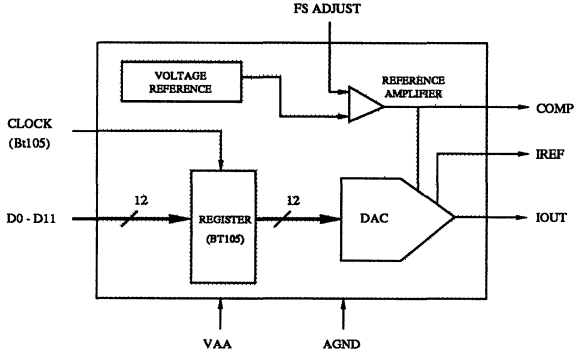
- Vector and Raster Displays
- Instrumentation
- SAR A/D Converters

Product Description

The Bt104 and Bt105 are 12-bit D/A converters designed specifically for applications requiring accurate and stable D/A conversion, while maintaining low linearity errors and glitch energy. The Bt104 has nonregistered data inputs and the Bt105 has registered data inputs.

An on-chip voltage reference is available or, for greater temperature stability and accuracy, an external reference may be used. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1/2 LSB and ± 1 LSB, respectively, over the full temperature range.

Functional Block Diagram



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Circuit Description

As illustrated in the functional block diagram, the Bt104 and Bt105 contain a single 12-bit D/A converter, a voltage reference, and a reference amplifier. The Bt105 also has a data register before the D/A converter.

Figure 1 illustrates the input/output timing of the Bt104, and Figure 2 illustrates the input/output timing of the Bt105.

Note that the output of the Bt104/105 is designed to drive into a virtual ground, such as an operational amplifier. Driving a resistive load degrades linearity.

The D/A converter on the Bt104 and Bt105 uses a segmented architecture in which bit currents are routed to either IOUT or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off.

Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip voltage reference and operational amplifier stabilizes the full scale output current against temperature and power supply variations.

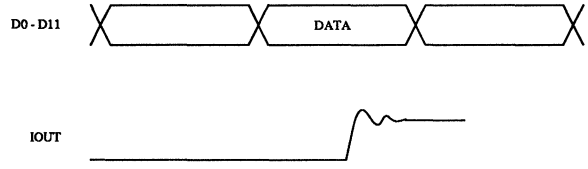

Figure 1. Bt104 Input/Output Timing.

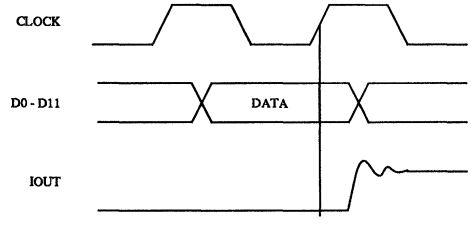

Figure 2. Bt105 Input/Output Timing.

Pin Descriptions

Pin Name	Description
D0 - D11	Data inputs (TTL compatible). D0 is the least significant data bit. On the Bt105, these inputs are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK (N/C)	Clock input (TTL compatible). The rising edge of CLOCK latches the D0 - D11 inputs on the Bt105. It is recommended that this pin be driven by a dedicated TTL buffer. This pin is not used on the Bt104 and may be left floating without affecting the performance of the Bt104.
IOUT	Analog current output. This high impedance current source is capable of sourcing up to 40 mA of current.
VAA	Analog power. All VAA pins must be connected.
AGND	Analog ground. All AGND pins must be connected.
FS ADJUST	Full scale adjust control. If the internal voltage reference is used, a resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale output current. If an external voltage reference is used, this pin should be connected to VAA. See Figures 3 and 4.
COMP	Compensation pin. A 0.01 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin. Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. See Figures 3 and 4. If an external voltage reference is used, this pin is driven by an external circuit such as shown in Figure 4.
IREF	Current reference output. If the internal voltage reference is used, this output is connected to the FS ADJUST input. If an external voltage reference is used, IREF is used, in conjunction with RSET, to provide feedback to the external reference to servo the reference. See Figures 3 and 4.

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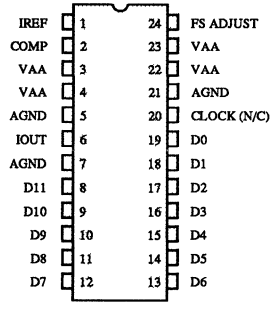


PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt104/105 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The Bt104/105 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figures 3 and 4. This bead should be located within three inches of the Bt104/105.

The analog ground plane area should encompass all Bt104/105 ground pins, any external voltage reference circuitry, power supply bypass circuitry for the Bt104/105, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces (D0 - D11 and CLOCK), excluding the ground pins, leading up to the Bt104/105.

Power Planes

The Bt104/105 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 3 and 4. This bead should be located within three inches of the Bt104/105.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt104/105 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

For the best performance, a 0.01 µF ceramic chip capacitor should be placed under the device to decouple the analog power and ground planes. In addition, two 0.01 µF ceramic capacitors should be used to decouple the two groups of VAA pins to the AGND pins. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt104/105 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt104/105 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

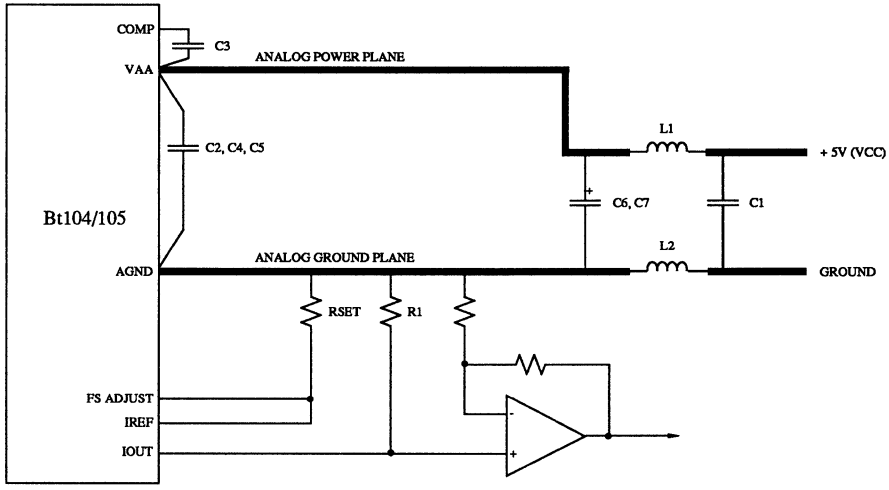
Analog Signal Interconnect

If an external output amplifier is used to convert the current output of the Bt104/105 to a voltage level, the amplifier should be placed as close as possible to the device. The amplifier power and ground pins should be connected to the analog power and ground planes.

When using an external voltage reference, the analog power and ground planes should be used to provide power and grounding to the reference circuitry.

The output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

PC Board Layout Considerations (continued)

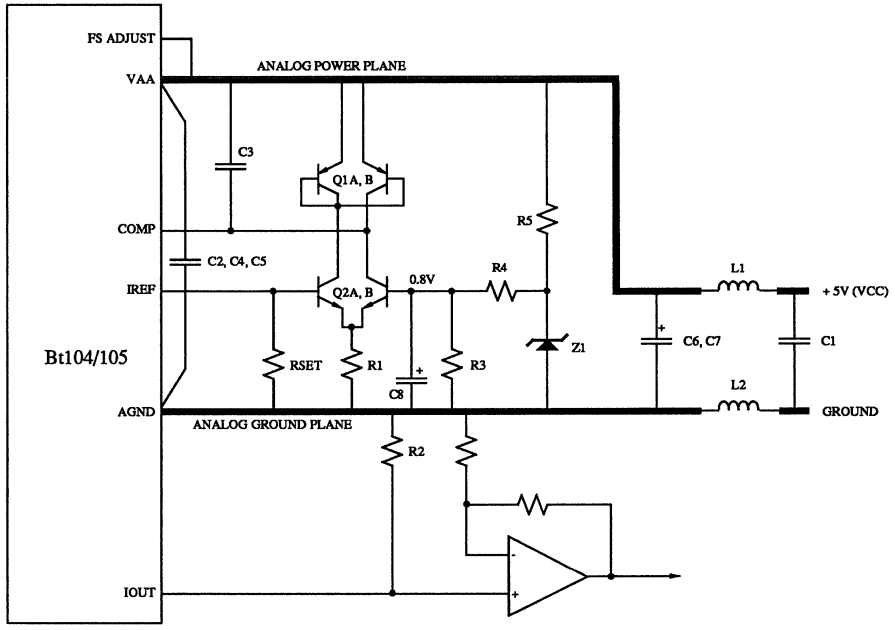


Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2, C3, C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
C6, C7	22 µF tantalum capacitor	Mallory CSR13G226KM
R1	24.9-ohm 1% metal film resistor	Dale CMF-55C
L1, L2	ferrite bead	Fair-Rite 2743001111
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt104/105.

Figure 3. Typical Connection Diagram and Parts List (Internal Reference).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2, C3, C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
C6, C7, C8	22 µF tantalum capacitor	Mallory CSR13G226KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	121-ohm 1% metal film resistor	Dale CMF-55C
R2	24.9-ohm 1% metal film resistor	Dale CMF-55C
R3	6.81K-ohm 1% metal film resistor	Dale CMF-55C
R4	3.65K-ohm 1% metal film resistor	Dale CMF-55C
R5	3.32K-ohm 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
Q1	matched transistor pair	Intersil IT131
Q2	matched transistor pair	National Semiconductor LM394
Z1	1.22V voltage reference	National Semiconductor LM313

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt104/105. Thermal coupling R2 to RSET minimizes drift.

Figure 4. Typical Connection Diagram and Parts List (External Reference).

Application Information

Using the Internal Reference

The Bt104/105 has an internal voltage reference to simplify design, as illustrated in Figure 3. The full scale output current is determined by the value of the RSET resistor. The internal reference (VREF) is typically 0.68v, but due to process variations has a tolerance of approximately ± 10%. Therefore, there will be a ± 10% tolerance from device to device, in the full scale output current for a given value of RSET.

As IREF = IOUT / 7.892 and IREF * RSET = VREF, assuming zero offset of the internal operational amplifier, then:

RSET (ohms) = 5,367 / IOUT (mA)

Using an External Reference

As illustrated in Figure 4, an external circuit may be used to increase the accuracy and temperature stability. This configuration disables the internal reference, and allows the use of an external temperature compensated reference. In this mode of operation, an external voltage reference, current mirror, and differential transistor pair servos the output current as a function of the IREF current.

The relationship of IOUT / IREF = 7.892 is internally maintained by the Bt104/105, and IREF * RSET = VREF, assuming zero offset of the operational amplifier. An external reference (VREF) from 0.2v to 0.8v may be used. The equation for finding RSET is:

RSET (ohms) = 7,892 * VREF (v) / IOUT (mA)

Therefore, the required accuracy may be traded off by the accuracy of the voltage reference tolerance, resistor tolerance, operational amplifier off tolerance, and the temperature tracking between these items.

The voltage reference should have a temperature coefficient of less than 25 ppm/°C, while the operational amplifier should have the lowest possible offset drift.

Power Dissipation Considerations

As the Bt104/105 is a CMOS device, there is a fairly linear relationship between the update rate and the power dissipation.

Estimated maximum VAA supply current (IAA) may be calculated as follows:

IAA (mA) =
(1.2 mA per MHz) + (full scale output current in mA)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		12	12	12	Bits
Accuracy					
Integral Linearity Error*	IL				
Bt104KC, Bt105KC				± 1	LSB
Bt104LC, Bt105LC				± 2	LSB
Differential Linearity Error	DL			± 1/2	LSB
Zero Error	EZ			1	µA
Full Scale (Gain) Error	EG				
Using Internal Reference				± 10	% FSR
Using External Reference				± 1	% FSR
Monotonicity					
Coding			guaranteed		Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Analog Output					
Output Current	IOUT	10		40	mA
Output Compliance	VOC	- 1.0		+ 1.0	Volts
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		25		pF
Internal Reference Voltage	VREF		0.68		Volts
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Integral linearity error is measured using a best-fit algorithm, with adjusted offset and gain.

A.C. Characteristics

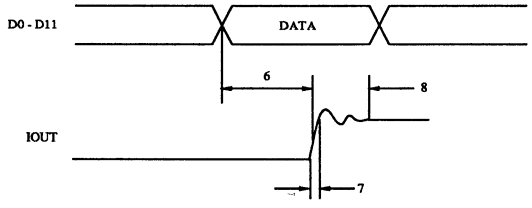
		Bt104			Bt105			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Register Clock Rate	Fmax						25	MHz
Data Setup Time	1				10			ns
Data Hold Time	2				2			ns
Clock Cycle Time	3				40			ns
Clock Pulse Width High Time	4				10			ns
Clock Pulse Width Low Time	5				10			ns
Analog Output Delay	6		25			25		ns
Analog Output Rise/Fall Time	7		8			8		ns
Analog Output Settling Time*	8							
Bt104KC, Bt105KC			25	40		25	40	ns
Bt104LC, Bt105LC			25	40		25	40	ns
Clock and Data Feedthrough*			- 25			- 25		dB
Glitch Impulse*			100			100		pV - sec
Differential Gain Error	DG		1.5			1.5		% FSR
Differential Phase Error	DP		1.5			1.5		Degrees
Pipeline Delay					1	1	1	Clock
VAA Supply Current**	IAA		68	75		68	75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 135 ohms. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load 25 ohms and ≤ 10 pF. See timing notes in Figures 5 and 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For these tests, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 50 MHz.

**at Fmax and 30 mA output current. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Timing Waveforms

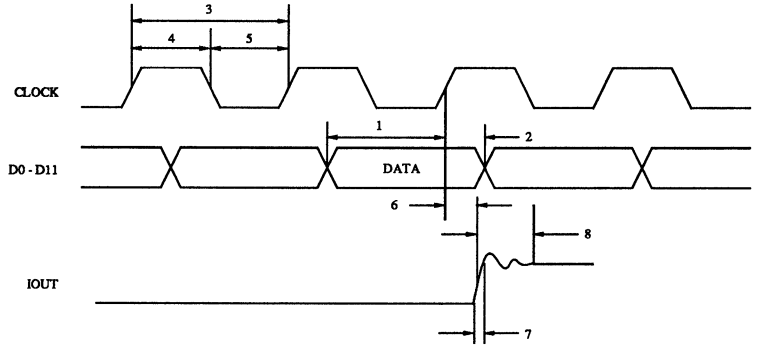


Note 1: Output delay measured from valid data to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within the specified IL error.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 5. Bt104 Input/Output Timing.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within the specified IL error.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Bt105 Input/Output Timing.

Ordering Information

Model Number	Integral Linearity Error	Package	Ambient Temperature Range
Bt104KC, Bt105KC	±1 LSB	24-pin 0.3" Ceramic Sidebraze DIP	0° to +70° C.
Bt104LC, Bt105LC	±2 LSB	24-pin 0.3" Ceramic Sidebraze DIP	0° to +70° C.

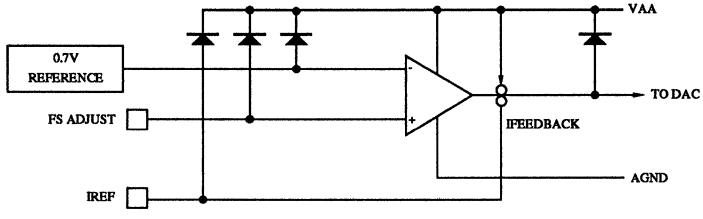


Figure 7. Equivalent Circuit of the Reference Amplifier.

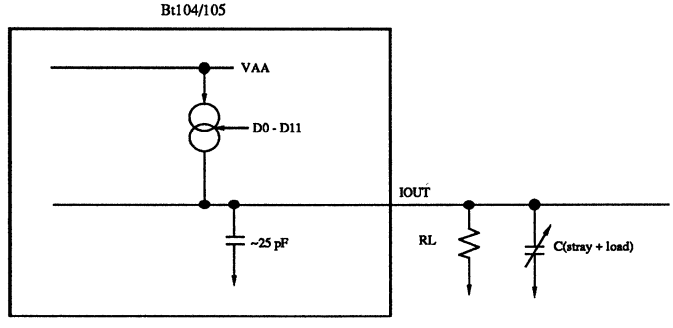


Figure 8. Equivalent Circuit of the Current Output.

Bt110

100 ns

Monolithic CMOS

Octal 8-bit

D/A Converter

Distinguishing Features

- Eight 8-bit D/A Converters
- 100 ns Settling Time to ± 1 LSB
- ± 1 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- Guaranteed Monotonic
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 150 mW

Applications

- Instrumentation
- Test Equipment
- Waveform Synthesis
- Data Aquisition Systems

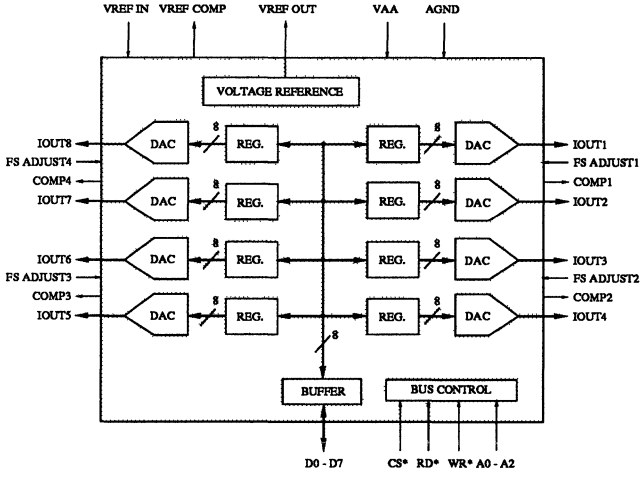
Product Description

The Bt110 is an octal 8-bit D/A converter. It provides eight independent D/A converters and has a standard MPU interface.

The D/A converters are arranged in pairs, with each pair sharing a common reference amplifier. This provides excellent matching and stability of the paired D/A converters.

An on-chip voltage reference is provided or an external reference may be used. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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Circuit Description

As illustrated in the functional block diagram, the Bt110 contains eight 8-bit D/A converters, eight nontransparent (D-type) octal data registers, and MPU bus interface logic. Also included on chip are four reference amplifiers and a voltage reference.

The Bt110 supports a conventional MPU bus interface through the use of the CS*, RD*, WR*, D0 - D7, and A0 - A2 pins. A0 - A2 specify which one of the eight internal data latches the MPU is accessing. These data latches may be written to or read by the MPU at any time. The input/output timing is illustrated in Figure 1.

The data contained in the data latches are presented to the associated D/A converter and used to specify the output current level. The MPU may read these data latches to determine what data is present at each D/A converter.

The full scale output current of each pair of D/A converters is set by an external resistor (RSET) between the FS ADJUST pin and AGND. FS ADJUST1 controls the full scale output current of IOUT1 and IOUT2, FS ADJUST2 controls the full scale output current of IOUT3 and IOUT4, FS ADJUST3 controls the full scale output current of IOUT5 and IOUT6, and FS ADJUST4 controls the full scale output current of IOUT7 and IOUT8.

The on-chip voltage reference (VREF OUT) may be used to provide the reference voltage for the VREF IN pin or an external reference circuit may be used. The on-chip reference should offer adequate performance for most applications.

Better temperature stability may be attainable by using an external voltage reference, such as the LM385BZ-1.2. The use of a resistor network to generate the reference voltage is not recommended, as any low frequency power supply noise on VREF IN will be directly coupled onto the analog outputs.

The D/A converters on the Bt110 use a segmented architecture in which bit currents are routed to either IOUT or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. The on-chip operational amplifiers stabilize the full-scale output currents against temperature and power supply variations.

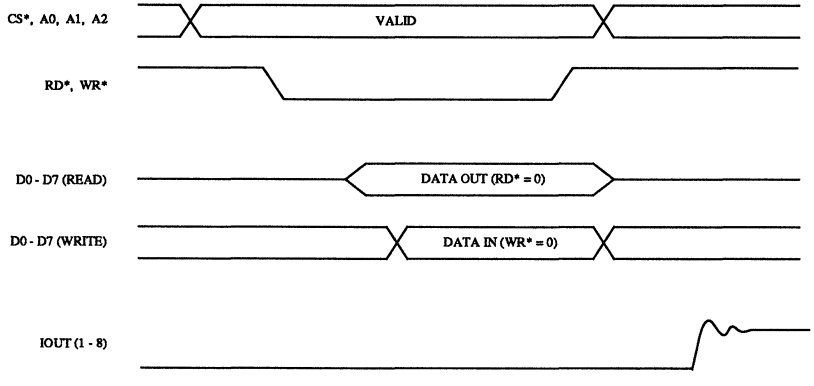


Figure 1. Input/Output Timing.

Pin Descriptions

Pin Name	Description
FS ADJUST (1 - 4)	Full scale adjust controls. A resistor (RSET) between each of these pins and AGND controls the full scale output currents. FS ADJUST1 controls the full scale output current for IOUT1 and IOUT2, FS ADJUST2 controls the full scale output current for IOUT3 and IOUT4, FS ADJUST3 controls the full scale output current for IOUT5 and IOUT6, and FS ADJUST4 controls the full scale output current for IOUT7 and IOUT8. The relationship between the full scale output current of each D/A and RSET is defined as follows: RSET (ohms) = 1000 * VREF IN (v) / IOUT (mA)
COMP (1 - 4)	Compensation pins. These pins provide compensation for the internal reference amplifiers. A 0.1 µF ceramic capacitor should be connected between each compensation pin and VAA, as illustrated in Figure 2. Decoupling the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. COMP1 provides compensation for IOUT1 and IOUT2, COMP2 provides compensation for IOUT3 and IOUT4, COMP3 provides compensation for IOUT5 and IOUT6, and COMP4 provides compensation for IOUT7 and IOUT8.
IOUT (1 - 8)	High impedance current outputs. These current outputs are designed to drive into a virtual ground, such as an operational amplifier.
VREF OUT	Voltage reference output. This output provides a 1.2v (typical) reference, and may be directly connected to the VREF IN pin. When used to provide a reference voltage to VREF IN, an external 1000-ohm resistor must be connected between VREF OUT and AGND.
VREF IN	Voltage reference input. Either an external voltage reference circuit or the VREF OUT pin is used to supply this input with a 1.2v (typical) reference. A 0.1 µF ceramic capacitor must be connected between this pin and VREF COMP.
VREF COMP	VREF IN compensation pin. A 0.1 µF ceramic capacitor must be connected between this pin and VREF IN.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
CS*	Chip select control input (TTL compatible). To enable data to be written to or read from the device, this input must be a logical zero. While it is a logical one, D0 - D7 are three-stated. Note that the Bt110 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
RD*	Read control input (TTL compatible). To enable data to be read from the device, both CS* and RD* must be a logical zero. See Figure 1.

Pin Descriptions (continued)

Pin Name **Description**

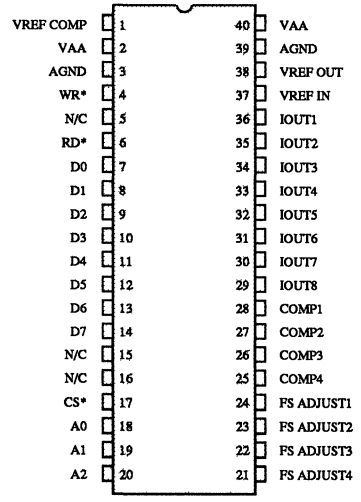
A0, A1, A2 — Select control inputs (TTL compatible). These inputs specify which internal D/A latch will be written to or read, as follows:

A2, A1, A0	D/A Output
000	IOUT1
001	IOUT2
010	IOUT3
011	IOUT4
100	IOUT5
101	IOUT6
110	IOUT7
111	IOUT8

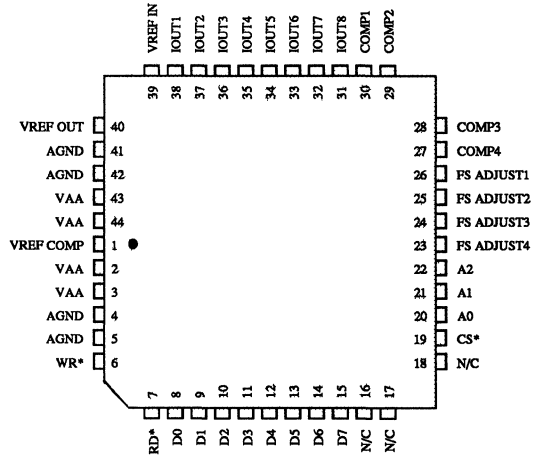
WR* — Write control input (TTL compatible). To enable data to be written to the device, both CS* and WR* must be a logical zero. Data is internally latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.

D0 - D7 — Bidirectional data bus (TTL compatible). Data is transferred into and out of the Bt110 over this eight bit data bus. D0 is the least significant bit.

40-pin DIP Package



44-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt110.

PC Board Layout Considerations

PC Board Considerations

The layout for the Bt110 should be optimized for lowest noise on the Bt110 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt110 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within three inches of the Bt110.

The analog ground plane area should encompass all Bt110 ground pins, any external voltage reference circuitry, power supply bypass circuitry for the Bt110, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt110.

Power Planes

The Bt110 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within three inches of the Bt110.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt110 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin(or group of VAA pins if they are adjacent) to the adjacent AGND pins. The capacitor should be placed as close as possible to the device.

A 0.1 µF ceramic capacitor must also be connected between each COMP pin (COMP1 - COMP4) and VAA. These capacitors should be placed as close as possible to the device.

A 0.1 µF ceramic capacitor must also be connected between the VREF COMP pin and the VREF IN pin. This capacitor should be placed as close as possible to the device.

It is important to note that while the Bt110 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt110 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

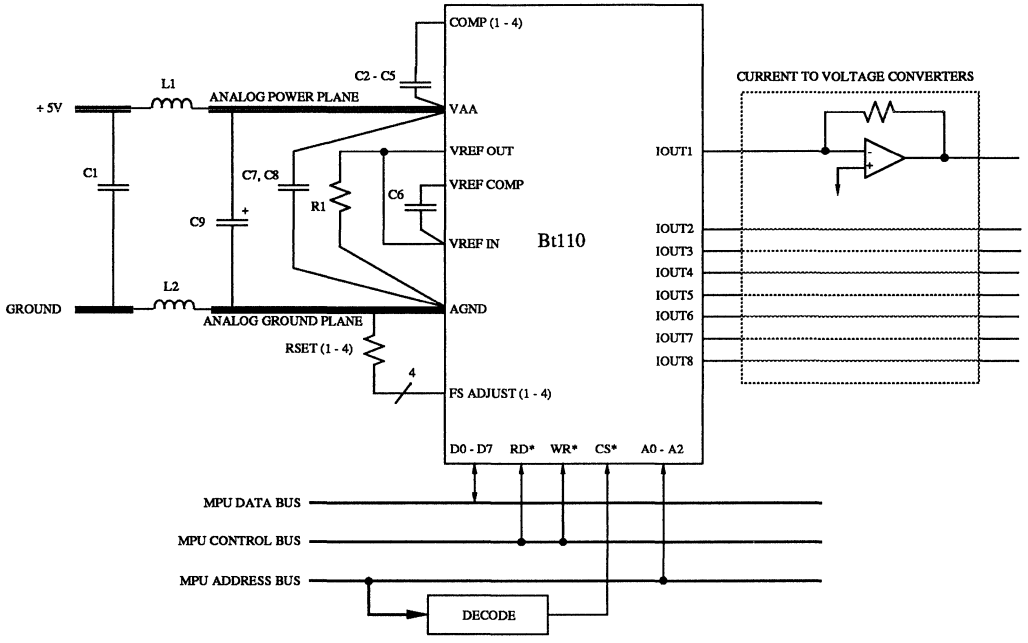
Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The Bt110 should be located as close as possible to the output amplifiers. Also, any external voltage reference circuitry should be as close as possible to the Bt110 to avoid noise pickup.

The analog output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C8	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C9	22 µF tantalum capacitor	Mallory CSR13G226KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	1000-ohm 1% metal film resistor	Dale CMF-55C
RSET (1 - 4)	1% metal film resistors	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt110.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

External Voltage Reference

For improved temperature stability, an external voltage reference may be used with the Bt110, as shown in Figure 3. In this instance, the VREF OUT pin should remain floating. The temperature stability of the internal reference is equivalent to about 1/4 LSB.

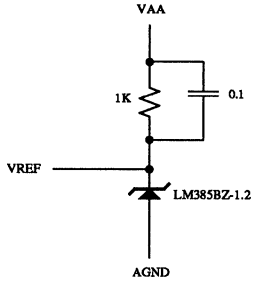


Figure 3. External Voltage Reference.

Programmable Window Comparator

The window comparator of Figure 4 is a circuit that may be used to determine whether the input voltage (Vin) lies within predefined limits. Using the Bt110, up to four programmable window comparators may be implemented.

One DAC of the matched pair is used to set the low limit and the other DAC is used to set the high limit. Thus, each pair of DACs form a window of programmable size. The output will be high while Vlow ≤ Vin ≤ Vhigh.

For a RSET value of 1200 ohms and a VREF IN voltage of 1.2v, the Bt110 outputs a full scale output current of approximately 1 mA onto IOUT1 and IOUT2. The 1K-ohm resistor generates a 0v to 1v output voltage (for DAC codes $00 to $FF), which is amplified to 0v to 5v (5x) by the LM358 dual operational amplifier. In this configuration, the LM358 is operating from a single +5v power supply.

The LM319 dual comparator is also operating from a single +5v power supply and compares the Vlow and Vhigh voltage levels to Vin. The 500-ohm pull-up resistor is necessary as the LM319 has open-collector outputs.

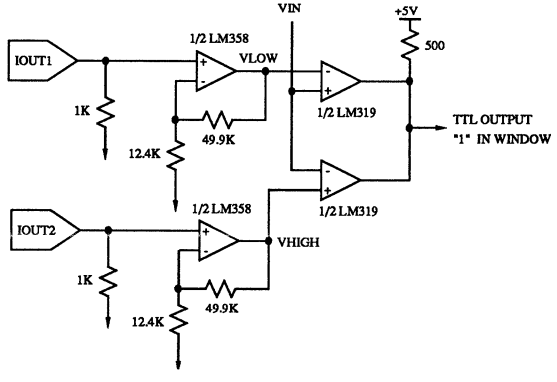


Figure 4. Programmable Window Comparator.

Application Information (continued)

Programmable Power Supply

The Bt110, when used with an external operational amplifier and power transistor, provides a way of generating voltages and currents outside of the Bt110's normal capability. Figure 5 illustrates a 0v to 10v programmable power supply.

For a RSET value of 1200 ohms and a VREF IN voltage of 1.2v, the Bt110 outputs a full scale output current of approximately 1 mA onto IOUT1. The 1K-ohm resistor is used to generate a 0v to 1v output voltage from the Bt110 (for DAC codes $00 to $FF). One of the operational amplifiers in the LM358 (A1) is used to multiply the voltage at IOUT1 by 10x, resulting in a 0v to 10v range. In this configuration, the LM358 is operating from a single +15v power supply.

The other operational amplifier in the LM358 (A2) is used as a buffer and driver for the TIP31 transistor. RS is the current limiting resistor to shut down the output in case of an overload. The correct value for RS is determined as follows:

$$RS = 0.7 / IOUTmax$$

For output voltages down to or near 0v, it is necessary to use a CMOS operational amplifier with a very low saturation voltage, or a plus/minus power supply and a bipolar operational amplifier to allow for output saturation which is typically 2v to 3v below the supply voltage.

Driving Active Devices

If the Bt110 is driving an active device whose supply is outside the 0v to 5v range, the analog output(s) should be clamped to VAA (see Figure 5).

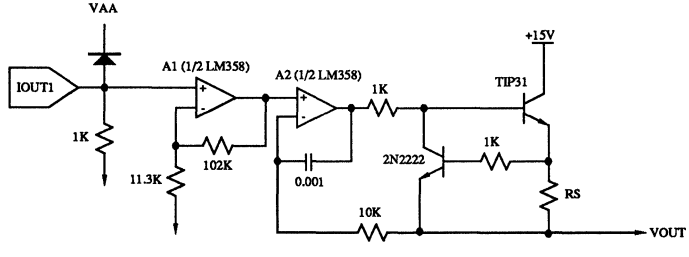


Figure 5. Programmable Power Supply.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Reference Voltage	VREF IN	1.0	1.2	1.3	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Full Scale (Gain) Error	EG				
Using Internal Reference				±10	% of FSR
Using External Reference				±5	% of FSR
Zero Error	EZ			5	µA
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Digital Outputs (D0 - D7)					
Output High Voltage (IOH = -800 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			1	µA
Output Capacitance	CDOUT		10		pF
Analog Outputs					
Output Current				1	mA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.2	Volts
Output Impedance	RAOUT		125		K ohms
Output Capacitance (IOUT1 - IOUT8 = 0 mA)	CAOUT		20		pF
Reference Output Voltage	VREF OUT	1.05	1.17	1.29	Volts
Reference Output Current	IREF OUT		1.2		mA
Reference Input Current	IREF IN			10	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.3		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 ohms, VREF IN = 1.0v. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Tmax			100	ns
CS*, A0, A1, A2 Setup Time	1	30			ns
CS*, A0, A1, A2 Hold Time	2	5			ns
WR* Low Time	3	30			ns
RD*, WR* High Time	4	20			ns
RD* Asserted to Data Bus Driven	5	10			ns
RD* Asserted to Data Valid	6			60	ns
RD* Negated to Data Bus 3-Stated	7			40	ns
Write Data Setup Time	8	20			ns
Write Data Hold Time	9	10			ns
Analog Outputs					
Analog Output Delay	10		15		ns
Analog Output Rise/Fall Time	11				
into 50 ohms				10	ns
into 1K ohms			350		ns
Analog Output Settling Time	12				
into 50 ohms				100	ns
into 1K ohms			800		ns
Data Feedthrough			- 30		dB
Glitch Impulse			75		pV - sec
DAC to DAC Crosstalk			- 25		dB
VAA Supply Current*	IAA		30	38	mA

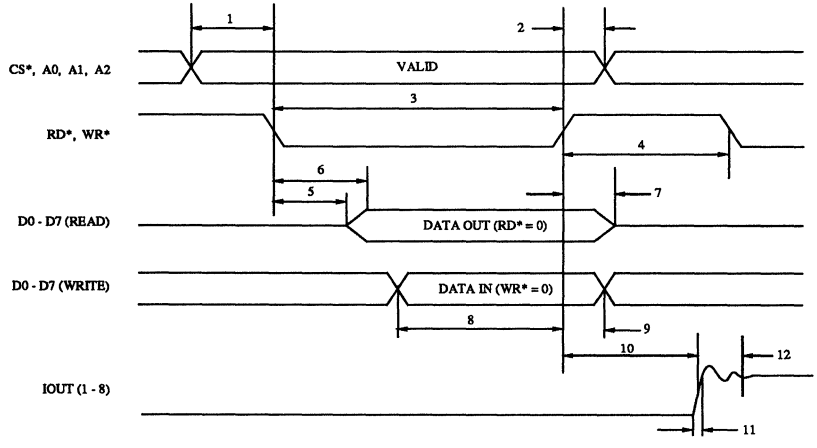
Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 ohms, VREF IN = 1.0v. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF into a virtual ground, D0 - D7 output load ≤ 130 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt110KC	40-pin 0.6" CERDIP	0° to +70° C.
Bt110KPJ	44-pin Plastic J-Lead	0° to +70° C.

Timing Waveforms



Note 1: Output delay measured from the rising edge of WR* to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Input/Output Timing.

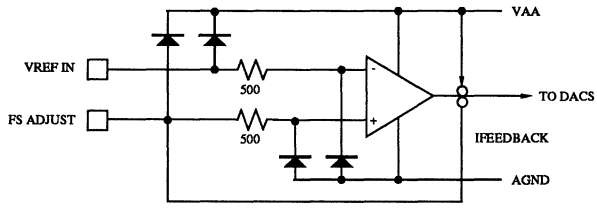


Figure 7. Equivalent Circuit of the Reference Amplifier.

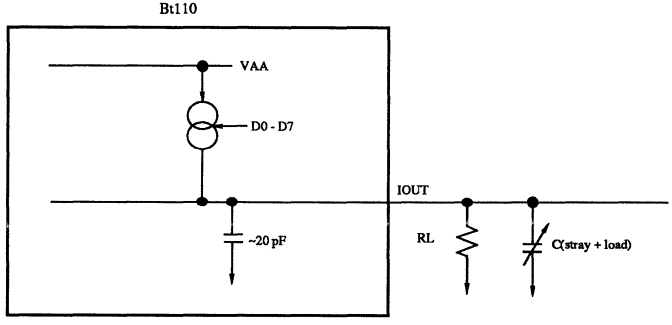


Figure 8. Equivalent Circuit of the Current Outputs.

Brooktree®

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Table of Contents

This section describes the Brooktree Military 883C Program, which was developed for the screening and processing of integrated circuits in accordance with MIL-STD-883C, Class B. The program is intended to provide the user with the ability to procure standardized, off-the-shelf integrated circuits from Brooktree Corporation that are fully compliant to MIL-STD-883C, Class B.

1.0 Applicable Documents

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

1.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits

1.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedures for Microelectronics

1.3 Detail Specifications

The detail specification for a particular 883C integrated circuit is the Brooktree Device Test Specification (DTS), an example of which is shown in Figure 1. The DTS is a detailed listing of the parameters, forcing functions, and lower/upper limits on the test tapes used to test 883C integrated circuits.

In the event of conflicting requirements, the order of precedence will be the purchase order, the DTS specification, and then the reference documents.

2.0 General Requirements

The individual requirements are specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements for the integrated circuit and electrical test methods are as specified in the detail specification.

2.1 Process Conditioning, Testing, Reliability, and Quality Assurance Screening

Process conditioning, screening, and testing are as specified in Section 4.0. Figure 2 illustrates the process flow chart for MIL-STD-883C, Class B products.

2.1.1 Qualification

The 883C integrated circuits furnished under this specification are products which have passed the qualification tests specified herein. Successful qualification for a given level results in qualification approval for that level and all lower product assurance levels of that device (reference Appendix E MIL-M-38510).

2.1.2 Alternate Qualifications

In lieu of meeting the requirements of 2.1.1, Brooktree may establish qualification by performing an initial, one time qualification test. Qualification testing shall be performed on each generic family supplied. Upon successful completion of the qualification program, the product shall remain qualified for a period not to exceed 12 months.

2.1.3 Product or Process Change

Brooktree will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability, or interchangeability of the circuit without full or partial requalification.

2.2 Quality Conformance Inspection

The 883C integrated circuits furnished under this specification are products which have been produced and tested in conformance with all the provisions of this specification for the applicable level. Devices which have been accepted as conforming to a given product assurance level may be furnished as conforming to any other level for which they meet or exceed the quality conformance requirements.

Table 1 -- DX90 Test Program

Test #	Characteristic	Symbol	Test Conditions	Final Min	Final Max	Limits QA Min	Limits QA Max	Corr Delta	Unit	Metri Max Range	Avgs	Fail Bin	VAA and VDD pass 1	VAA and VDD pass 2	Pins
9000.1	VDD continuity		V15 clamp at ±2v (note 4)	- 900	500	- 900	500	-	mV	2v	1	7	force	- 100 µA	10
9000.2	VAA continuity		V12 clamp at ±2v (note 4)	- 900	500	- 900	500	-	mV	2v	1	7	force	- 100 µA	30
9000.3	input continuity (digital pins)		V11 clamp at ±2v (note 4), force -100 µA	- 970	- 25	- 970	- 25	-	mV	2v	1	7	0v	0v	list 5
1	digital supply current	IDD	note 1	6.0	49.0	5.0	50.0	1.0	mA	120 mA	1	10	4.75v	5.25v	10
101															
201															
2	analog supply current	IAA	note 1	51.0	84.0	50.0	85.0	1.0	mA	150 mA	1	10			30
3	VREF	VREF	note 2	1.161	1.239	1.16	1.24	0.002	V	3 mA	1	11			15
4	worst case bit current (Vin = VDD)	IIH	digital inputs = VDD	- 0.8	0.8	- 1.0	1.0	0.2	µA	100 µA	1	12			list 5
5	worse case bit current (Vin = 0v)	IIL	digital inputs = 0v	- 0.8	0.8	- 1.0	1.0	0.2	µA	100 µA	1	12			list 5
6	sync voltage level	VSYNC	blank, sync, ref white low; all D0 - D7 high (note 3)	- 0.8	0.8	- 1.88	1.88	1.0	mV	0.5v	12	12			31
7	sync current	ISYNC	blank, ref white low; sync, all D0 - D7 high (note 3) using ISYNC formula	6.8	8.8	6.30	8.96	0.02	mA	0.5v	1	12			31
8	ISYNC compliance (-1.2v to +1.2v)	-	same condition using sync compliance formula	- 0.25	0.25	- 0.3	0.3	0.1	mA	2v	12	12			31
11	blank level voltage (green)	VBLANK	blank, ref white low; sync, all D0 - D7 high (note 3)	- 0.8	0.8	- 1.88	1.88	1.0	mV	0.5v	12	13			32
12	reference black current (green)	IBLACK	ref white, all D0 - D7 low; sync, blank high (note 3) using IBLACK formula	0.97	1.88	0.95	1.90	0.02	mA	1v	12	14			32
13.0	full scale error (green)	IFS	all D0 - D7 low; ref white, sync, blank high (note 3) using FS ERROR formula	- 4.4	4.4	- 5.0	5.0	0.6	% FSR	1v	12	15			32
13.1	M ratio (green)	-	same conditions as above using M RATIO formula	none	none	none	none	-	-	1v	12	-			32
13.2	M ratio error (green)	-	same conditions as above using M RATIO error formula	none	none	none	none	-	-	1v	12	-			32
14.0	intergral linearity (green)	IL	ref white low; sync, blank high (note 3) using linearity algorithm	- 0.9	0.9	- 1.0	1.0	0.08	LSB	1v	12	17			32
14.1	worst code (green)	-	code that resulted in highest absolute IL error	none	none	none	none	-	-	1v	12	-			32
15.0	differential linearity (green)	DL	same conditions as above using linearity algorithm	- 0.9	0.9	- 1.0	1.0	0.08	LSB	1v	12	17			32
15.1	worst code (green)	-	code that resulted in highest absolute DL error	none	none	none	none	-	-	1v	12	17			32
16	power supply rejection ratio at 120 Hz (green)	PSSR	data and control pins high; RS at 120 Hz 500 mV p-p using PSSR algorithm	- 0.25	0.25	- 0.3	0.3	0.05	%F%VAA	400 mV p-p	1	18			32
17	power supply rejection ratio at 1 KHz (green)	PSSR	data and control pins high; RS at 1 KHz 500 mV p-p using PSSR algorithm	- 0.45	0.45	- 0.5	0.5	0.05	%F%VAA	400 mV p-p	1	18			32
18	compliance, delta IL at 8F, 1v to 1.6v (green)	-	ref white low; sync, blank high (note 3) using data compliance algorithm	- 0.5	0.5	- 0.75	0.75	0.2	LSB	1v	38	19			32

Figure 1. Brooktree Device Test Specification (DTS) Example.

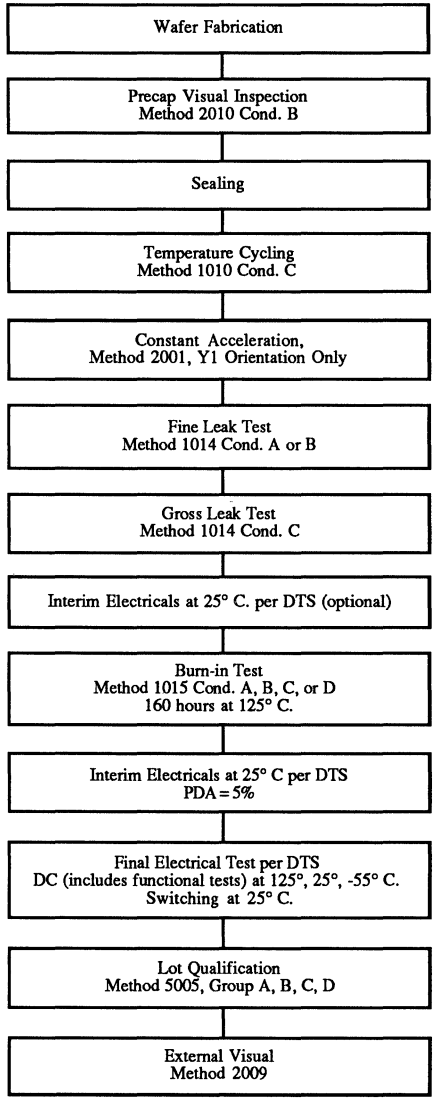


Figure 2. Product Screening Flow per MIL-STD-883C, Class B.

2.3 Marking

2.3.1 Marking Each Device

The following marking is placed on each integrated circuit:

a) Index point (see 2.3.4)
b) Part number (see 2.3.5)
c) Inspection or Identification code (see 2.3.7)
d) Manufacturer's identification (see 2.3.8)
e) Compliance Indicator "C" (see 2.3.9)
f) Country of Origin (see 2.3.10)
g) Die Fabrication Date code (see 2.3.11)

2.3.2 Marking on Initial Container

All of the marking specified in 2.3.1, except the index point, appear on the initial protection or wrapping for delivery.

2.3.3 Marking Permanence

Marking is permanent in nature and will remain legible after testing. Damage to marking caused by mechanical fixturing in Group B, C and D tests are not cause for lot rejection.

2.3.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

2.3.5 Part Number

The part number is the Brooktree generic part number with /883 attached at the end.

2.3.6 Formation of Lots

Integrated circuits are assembled into inspection lots in accordance with MIL-M-38510.

2.3.7 Inspection or Identification Code

Integrated circuits are marked by a 4-digit date code indicating the date the lot was sealed, and a 3-digit lot identification code. The codes provide for a method of traceability of product history.

2.3.8 Manufacturer's Identification

These integrated circuits are marked with the name, logo, or trademark of Brooktree Corporation.

2.3.9 Compliance Indicator "C"

The letter "C" will be marked on the topside of the device indicating the product is in compliance with MIL-STD-883C, paragraph 1.2.1.

2.3.10 Country of Origin

Each device will be marked with the country in which the product was assembled.

2.3.11 Die Fabrication Date Code

Each device will be marked with a two digit Numeric/Alpha code indicating the year and quarter in which the wafer fabrication process was completed.

3.0 Conditions and Methods of Test

Conditions and methods of test are in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

3.1 Internal Visual Inspection (Precap)

Internal visual inspection is performed per MIL-STD-883, Method 2010, Condition B.

3.2 Temperature Cycling

Temperature cycling is performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from -65° C. to +150° C.

3.3 Constant Acceleration

Constant acceleration is performed per MIL-STD-883C, Method 2001, Y1 Orientation only. Condition E will be performed unless Condition D is allowed.

3.4 Hermeticity

Hermeticity tests are performed per the following:

3.4.1 Fine Leak Testing

Fine leak testing is performed per MIL-STD-883, Method 1014, Condition A or B. The criterion for rejection is in accordance with MIL-STD-883.

3.4.2 Gross Leak Testing

Gross leak testing is performed per MIL-STD-883, Method 1014, Condition C. The rejection criterion is in accordance with MIL-STD-883.

3.5 Interim Electrical Parameters

Interim electrical parameters are the 25° C. DC parameters, specified in the detail specification. Interim electrical parameters are performed at Brooktree's option.

If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening are excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures are included in the PDA. The verified failures of Group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

3.6 Burn-in

Burn-in is performed per MIL-STD-883, Method 1015, Conditions A, B, C, or D . Burn-in condition varies with product type. Burn-in is performed for 160 hours at 125° C.

3.7 Final Electrical Parameters

Final electrical parameters are as specified in the applicable detail specification. DC testing is performed at 25° C, -55° C. and 125° C. Switching testing is performed at 25 °C. The PDA (Percent Defective Allowable) shall be 5% maximum and shall only apply to DC measurements at 25° C.

3.8 External Visual Inspection

All 883C integrated circuits receive external visual inspection per MIL-STD-883, Method 2009.

4.0 Quality Assurance Provisions

4.1 Quality Conformance Inspection

Quality conformance inspection is in accordance with Groups A and B. Inspection lot sampling is in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for a given product assurance level are rejected. Sample selection is in accordance with MIL-M-38510.

4.1.1 Group A Inspection

Group A inspection consists of the electrical parameters in the DTS and is performed on each lot. If an inspection lot is made up of a collection of sublots, each sublot is subjected to Group A, as specified. Group A may be done in-line.

4.1.2 Group B Inspection

Group B inspection consists of construction testing and is performed on each unique date code lot. This sample test sequence includes, resistance to solvents, bond strength, and solderability. Group B qualifies the inspection sublot from which the sample is selected and all devices manufactured within the same inspection lot in the same package on the same assembly line. Group B may be done in-line.

4.1.3 Group C Inspection

Group C inspection consists of die stress testing. This sample test sequence includes operating life, and end point electricals. Group C qualifies the lot from which the sample is selected and all generically similar die type for a period of one year.

Test	Quantity / (accept no.)
Subgroup 1 Static tests at 25° C.	116 (0)
Subgroup 2 Static tests at maximum rated operating temperature	116 (0)
Subgroup 3 Static tests at minimum rated operating temperature	116 (0)
Subgroup 4 Dynamic tests at 25° C.	116 (0)
Subgroup 5 Dynamic tests at maximum rated operating temperature	116 (0)
Subgroup 6 Dynamic tests at minimum rated operating temperature	116 (0)
Subgroup 7 Functional tests at 25° C.	116 (0)
Subgroup 8 Functional tests at maximum and minimum rated operating temperature	116 (0)
Subgroup 9 Switching tests at 25° C.	116 (0)
Subgroup 10 Switching tests at maximum rated operating temperature	116 (0)
Subgroup 11 Switching tests at minimum rated operating temperature	116 (0)

Table I. Group A Inspection (Electrical Tests).

Test	Method	Conditions	Quality / (accept no.) or LTPD
Subgroup 2 Resistance to solvents	2015		4 (0)
Subgroup 3 (Note 1) Solderability	2003 or 2022	Soldering temperature of 245°C ± 5° C.	10
Subgroup 5 (Note 2) Bond strength	2011	Condition C or D	15

Note 1: The LTPD for solderability test applies to the number of leads inspected, except no less than 3 devices shall be used to provide the number of leads required.

Note 2: The LTPD for bond strength test is the number of bond pulls selected from a minimum of 4 devices.

Table II. Group B Inspection.

Test	Method	Conditions	LTPD
Subgroup 1 Operating life test End point electrical parameters	1005	Test conditions to be specified (1,000 hours at 125° C.) As specified per applicable DTS* (subgroup 1 of Group A)	5

* Device Test Specification

Table III. Group C Inspection (Die Related Tests).

Test	Method	Conditions	Quality / (accept no.) or LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2			
Lead integrity	2004	Test conditions B2 (lead fatigue)	15
Leadless chip carrier package		Condition D	
Seal (fine and gross)	1014	As applicable	
Subgroup 3			
Thermal shock	1011	Test condition B -- 15 cycles	15
Temperature cycling	1010	Test condition C -- 100 cycles	
Moisture resistance	1004		
Seal (fine and gross)	1014	As applicable	
Visual examination		Criteria per 1004 and 1010	
End point electrical parameters		As specified per applicable DTS* (subgroup 1 of Group A)	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration, variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y1 axis	
Seal (fine and gross)	1014	As applicable	
Visual examination		Criteria per 1010	
End point electrical parameters		As specified per applicable DTS* (subgroup 1 of Group A)	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal (fine and gross)	1014	As applicable	
Visual examination		Criteria per 1009	
Subgroup 6			3 (0) or
Internal water vapor content	1018	5,000 ppm maximum water content at 100° C.	5 (1)
Subgroup 7			15
Adhesion of lead finish	2025		
Subgroup 8			5 (0)
Lid Torque	2024		

* Device Test Specification

Table IV. Group D Inspection (Package Related Tests).

4.1.4 Group D Inspection

Group D testing further stresses the package and the die. The Group D tests include physical dimensions, lead integrity, hermeticity, thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration variable frequency, constant acceleration, salt atmosphere, visual examination, and end point electricals (see Table IV). Group D qualifies the lot from which the sample is selected and all generically similar devices built in the same package and assembled by the same vendor for a period of one year.

5.0 Data and Reports

5.1 Certificate of Compliance

All 883C integrated circuits shipped are accompanied by a Certificate of Compliance.

5.2 Quality Conformance Reports

Quality conformance data for Group A, B, C, and D testing, and the device test specifications, is not normally provided, but is retained on file. Copies are available at no cost.

5.3 Traceability

Traceability is in accordance with MIL-M-38510. Each integrated circuit is traceable to the production lot. Reworked or repaired circuits maintain traceability.

6.0 Packaging

Packing and packaging are in accordance with MIL-M-38510.

7.0 Custom Marking

Dual marking is allowable, since the 883C integrated circuits are fully compliant with Methods 5004 and 5005 of MIL-STD-883, and are typically fully compliant to Source Control /Specification Control Drawings prepared in accordance with MIL-STD-883.

Bt101/883

MIL-STD-883C, Class B

Monolithic CMOS

30 MHz Triple 8-bit

VIDEODAC™

Distinguishing Features

- 30 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- ± 1 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Outputs
- +5v CMOS Monolithic Construction
- 40-pin Ceramic Sidebraze DIP Package
- Typical Power Dissipation: 700 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

Product Description

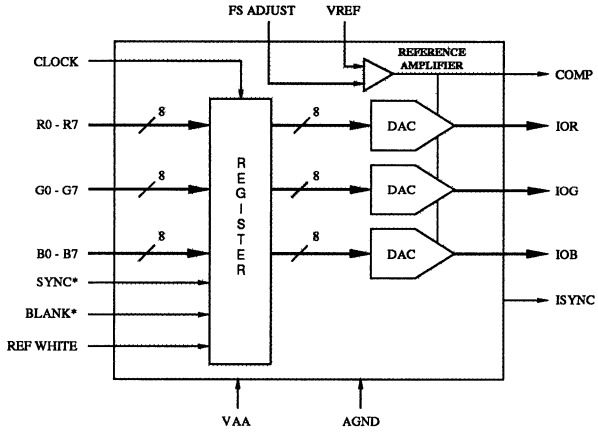
The Bt101/883 is a triple 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog outputs to the reference white level, regardless of the data inputs.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt101/883 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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L101M01 Rev. E

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt101/883 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0 - R7, G0 - G7, and B0 - B7) are latched into the device and presented to the three 8-bit D/A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, forces the inputs of each D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output levels.

The ISYNC current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If ISYNC is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG, and IOB outputs will have the same full scale output current.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 ohms for generation of RS-343A video into a 37.5-ohm load. The VREF input requires an external 1.2v (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converters on the Bt101/883 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt101/883 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

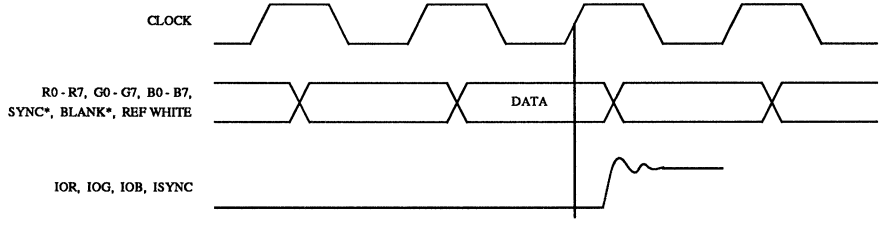
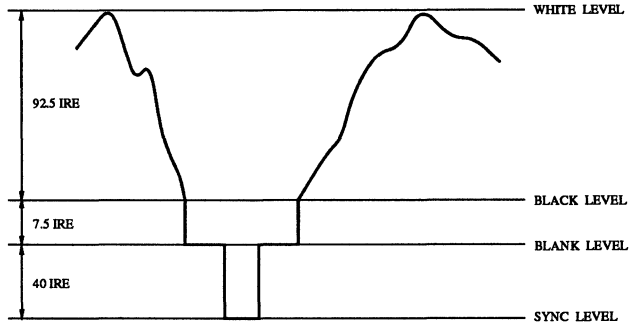


Figure 1. Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	1	$xx
WHITE	26.67	19.05	0	1	1	$FF
DATA	data + 9.05	data + 1.44	0	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	0	1	data
BLACK	9.05	1.44	0	1	1	$00
BLACK - SYNC	1.44	1.44	0	0	1	$00
BLANK	7.62	0	x	1	0	$xx
SYNC	0	0	x	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG.

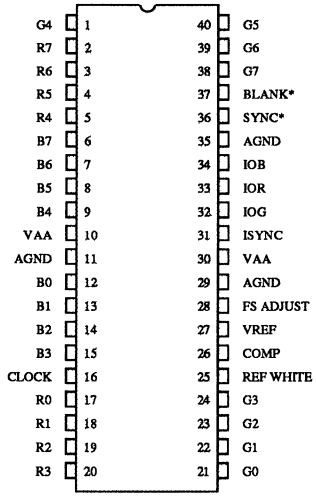
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0 - R7, G0 - G7, B0 - B7, and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R0 - R7, G0 - G7, and B0 - B7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R0 - R7, G0 - G7, B0 - B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0 - R7, G0 - G7, B0 - B7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. Typically, this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logical zero on the SYNC* input results in no current being output onto this pin, while a logical one results in the following current being output: ISYNC (mA) = 3,442 * VREF (v) / RSET (ohms) If sync information is not required on the green channel, this output should be connected to AGND.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG (assuming ISYNC is connected to IOG) is: RSET (ohms) = 12,046 * VREF (v) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 8,604 * VREF (v) / RSET (ohms)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the nearest VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt101/883 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt101/883 and any associated analog circuitry should have it's own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101/883.

The analog ground plane area should encompass all Bt101/883 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt101/883, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt101/883.

Power Planes

The Bt101/883 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101/883.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt101/883 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt101/883 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt101/883 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt101/883 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

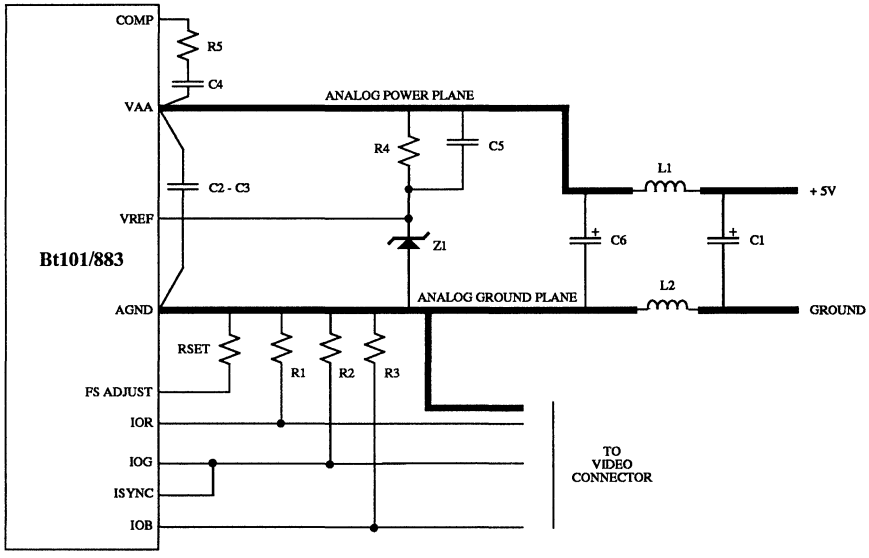
Analog Signal Interconnect

The Bt101/883 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt101/883 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description
C1	33 µF tantalum capacitor
C2, C3, C5	0.1 µF ceramic capacitor
C4	0.01 µF ceramic capacitor
C6	10 µF tantalum capacitor
L1, L2	ferrite bead
R1, R2, R3	75-ohm 1% metal film resistor
R4	1000-ohm 1% metal film resistor
R5	15-ohm 1% metal film resistor
RSET	549-ohm 1% metal film resistor
Z1	1.2v voltage reference

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with an RSET value of about 774 ohms. If the Bt101/883 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/(20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

COMP Resistor

To optimize the settling time of the Bt101/883, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt101/883 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one. ISYNC should be connected to AGND. All three outputs will have the same full scale output current.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,958 * VREF (v) / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (v) / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full scale" control.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 185	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
θ JC				25	°C. / W
θ JA				60	°C. / W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity**			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH				
CLOCK		3.0			Volts
Other		2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = VAA)	IIH			1	µA
Input Low Current (Vin = 0v)	IIL			- 1	µA
Input Capacitance*	CIN		10		pF
Analog Outputs					
Gray Scale Current Range				20.40	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size*			69.1		µA
Output Compliance	VOC			+ 1.4	Volts
Output Capacitance*	COUT		30		pF
Voltage Reference Input Current (VREF = 1.200v)	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): 100% tested at VAA = 4.75v and 5.25v, TA = -55°, 25°, and 125° C., RSET = 542 ohms ± 0.1%, VREF = 1.200v. ISYNC connected to IOG.

*Derived from characterization, not tested (TA = 25° C., VAA = 5v ± 5%).

**Guaranteed by design, not tested.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			30	MHz
Data and Control Setup Time	TSU	10			ns
Data and Control Hold Time	TH	3			ns
Clock Cycle Time	TCYC	33.3			ns
Clock Pulse Width Low	TCLKH	10			ns
Clock Pulse Width High	TCLKL	10			ns
Analog Output Delay	TDLY				
TA = -55° C.				31	ns
TA = 25° C.				31	ns
TA = 125° C.				39	ns
Analog Output Rise/Fall Time	TVRF			9	ns
Analog Output Settling Time*	TS		12		ns
Clock and Data Feedthrough*			- 28		dB
Glitch Impulse*			100		pV - sec
DAC to DAC Crosstalk*			- 23		dB
Analog Output Skew			0	3	ns
Pipeline Delay		1	1	1	Clock
VAA Supply Current**	IAA		140	175	mA

Test conditions (unless otherwise specified): 100% tested at VAA = 4.75v and 5.25v with TA = 25° C. QCI sample tested at VAA = 4.75v and 5.25v with TA = -55°, 25°, and 125° C. RSET = 542 ohms ± 0.1%, VREF = 1.200v. Input values are 0.4 to 3.5 volts for CLOCK and 0 to 3 volts for all other digital inputs, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 15 ohms. Analog output load ~ 10 pF with doubly-terminated 50-ohm line. See timing notes in Figure 4.

Note: Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 60 MHz.

*Derived from characterization, not tested (TA = 25° C, VAA = 5v ± 5%).

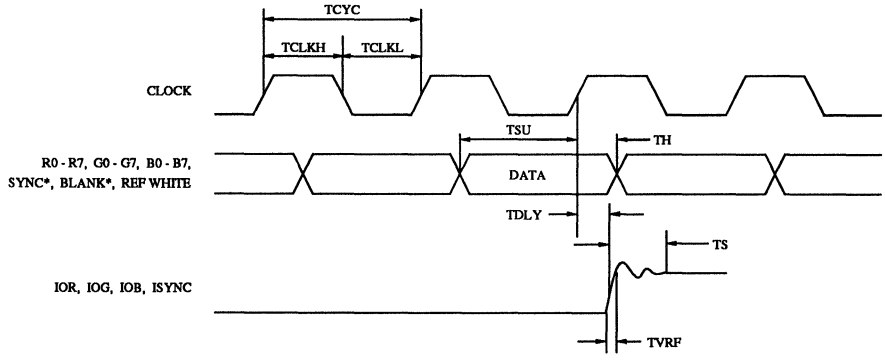
**at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v. IAA (max) 100% tested at TA = 25° C. IAA (typ) based on characterization.

Ordering Information

Model Number	MTBF* (hours)	Package	Ambient Temperature Range
Bt101SC883	1.5×10^6	40-pin 0.6" Ceramic Sidebraze DIP	-55° to +125° C.

*MTBF is calculated per MIL Handbook 217.

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

Bt102/883

MIL-STD-883C, Class B

Monolithic CMOS

50 MHz Single 8-bit

VIDEODAC™

Distinguishing Features

- 50 MHz Pipelined Operation
- ± 1/2 LSB Differential Linearity Error
- ± 3/4 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- 0, 7, or 10 IRE Programmable Setup
- +5v CMOS Monolithic Construction
- 24-pin 0.3" Sidebraze DIP Package
- Typical Power Dissipation: 550 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Conventional D/A Applications

Product Description

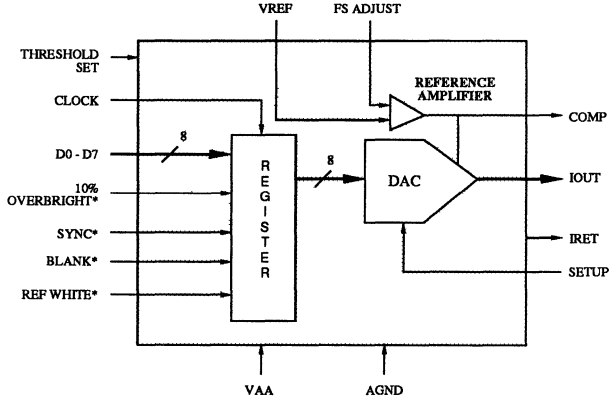
The Bt102/883 is an 8-bit multi-function VIDEODAC, designed specifically for color graphics and conventional D/A converter applications.

Available control inputs include sync, blank, reference white, and 10% overbright. Additional features include a threshold set input to configure the digital inputs to be either TTL or CMOS compatible, and a setup input to specify one of three available setups in the analog output.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, reference white, and 10% overbright inputs are pipelined to maintain synchronization with the input data.

The Bt102/883 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ± 1/2 LSB and ± 3/4 LSB, respectively, over the full temperature range.

Functional Block Diagram



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L102M01 Rev. D

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt102/883 contains a single 8-bit D/A converter, input registers, and a reference amplifier.

The THRESHOLD SET input controls the logic thresholds of the digital inputs. If it is left floating, the logic thresholds are TTL compatible; if connected to VAA, the thresholds are CMOS compatible.

On the rising edge of each clock cycle, as shown below in Figure 1, eight bits of data (D0 - D7) are latched into the device and presented to the 8-bit D/A converter. The REF WHITE* input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF, regardless of the value of the D0 - D7 inputs.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC*, BLANK*, and 10% OVERBRIGHT* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs modify the output level.

The SETUP input is used to control the difference between the black and blanking level. Available setups include 10 IRE (SETUP = VAA), 7 IRE (SETUP = float), and 0 IRE (SETUP = AGND). A setup of 0 IRE specifies that the blanking level is the same as the black level.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. The VREF input requires an external 1.2v(typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt102/883 uses a segmented architecture in which bit currents are routed to either the output or IRET by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt102/883 is capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

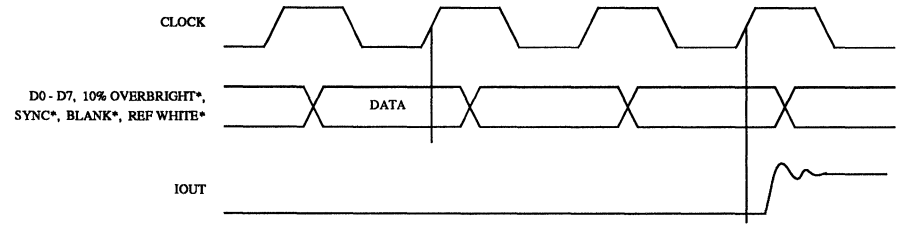
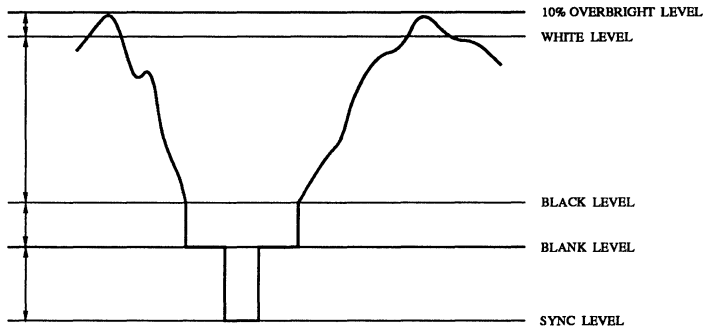


Figure 1. Input/Output Timing.

Circuit Description (continued)

RSET = 1130		RSET = 1110		RSET = 1050	
SETUP = VAA		SETUP = FLOAT		SETUP = AGND	
IRE	MA	IRE	MA	IRE	MA
9.5	28.90	10	28.74	10.75	29.00
	27.01		26.81		26.97
90		92.9		100	
	9.59		9.09		8.23
10		7.1		0	
	7.65		7.72		8.23
39.5		40.5		44	
	0.00		0.00		0.00



Note: 75-ohm doubly-terminated load, VREF = 1.235v. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	10% OVERBRIGHT*	REF WHITE*	SYNC*	BLANK*	DAC Input Data
WHITE +10%	28.74	0	1	1	1	$FF
WHITE	26.81	1	0	1	1	$xx
WHITE	26.81	1	1	1	1	$FF
DATA + 10%	data + 11.0	0	1	1	1	data
DATA	data + 9.09	1	1	1	1	data
DATA - SYNC	data + 1.37	1	1	0	1	data
BLACK	9.09	1	1	1	1	$00
BLACK - SYNC	1.37	1	1	0	1	$00
BLANK	7.72	x	x	1	0	$xx
SYNC	0	x	x	0	0	$xx

Note: Typical with white level current = 26.81 mA. RSET = 1110 ohms, VREF = 1.235v, SETUP = float.

Table 1. Video Output Truth Table.

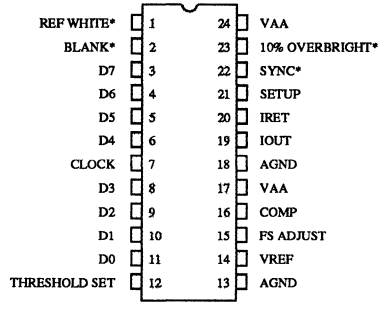
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL/CMOS compatible). A logical zero drives the output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0 - D7, REF WHITE*, and 10% OVERBRIGHT* inputs are ignored.
SYNC*	Composite sync control input (TTL/CMOS compatible). A logical zero on this input switches off a current source on the output equal to approximately 30% of the full scale current (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE*	Reference white control input (TTL/CMOS compatible). A logical zero on this input forces the output to the white level, regardless of the D0 - D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
10% OVERBRIGHT*	Overbright control input (TTL/CMOS compatible). A logical zero on this input causes the output current to increase by approximately 10 IRE units as shown in Table 1 and Figure 2. It is latched on the rising edge of CLOCK.
D0 - D7	Data inputs (TTL/CMOS compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL/CMOS compatible). The rising edge of CLOCK latches the D0 - D7, SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL or CMOS buffer.
SETUP	Setup control input. This pin controls the difference between the black level and the blanking level. Available setups include 10 IRE units (SETUP = VAA), 7 IRE units (SETUP = float), and 0 IRE units (SETUP = AGND).
THRESHOLD SET	Threshold control input. This pin controls the logic thresholds of the digital inputs. If connected to VAA through a 0.1 µF ceramic capacitor, the logic thresholds are TTL compatible. If connected directly to VAA, the thresholds are CMOS compatible.
IOUT	Current output. This high impedance current source is capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3).
IRET	Current return. This pin must be connected to AGND through a ferrite bead, as illustrated in Figure 3.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 3). Note that the IRE relationships in Figure 3 are maintained regardless of the full scale output current. The relationship between RSET and the white level output current is: RSET (ohms) = K1 * VREF (v) / IOUT (mA) The amount of additional current generated to achieve the overbright level is: IOUT (mA) = K2 * VREF (v) / RSET (ohms) K1 and K2 are defined as follows:

	SETUP		
	float	VAA	AGND
K1	24,096	24,713	22,930
K2	1,735	1,729	1,726



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt102/883 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The Bt102/883 and any associated analog circuitry should have it's own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt102/883.

The analog ground plane area should encompass all Bt102/883 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt102/883, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt102/883.

Power Planes

The Bt102/883 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt102/883.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt102/883 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt102/883 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt102/883 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt102/883 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

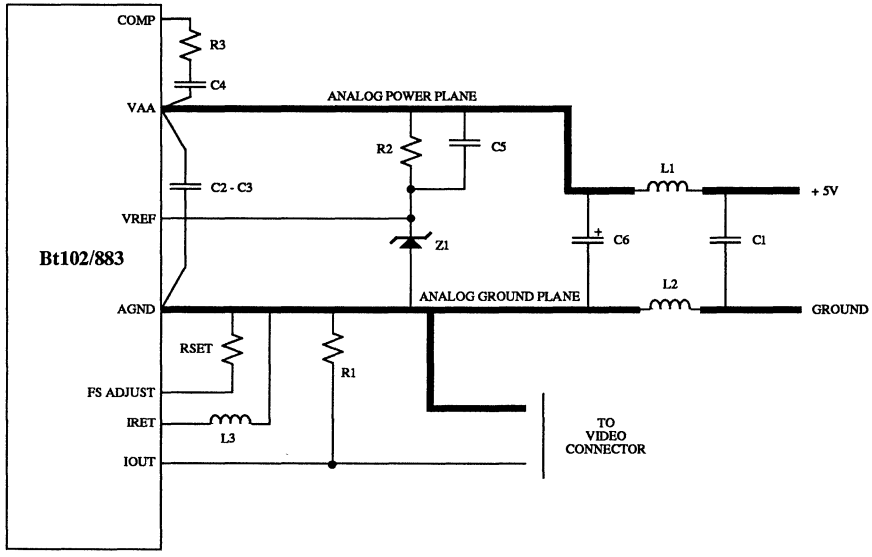
Analog Signal Interconnect

The Bt102/883 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog output should have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt102/883 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description
C1, C2, C3, C5	0.1 µF ceramic capacitor
C4	0.01 µF ceramic capacitor
C6	10 µF tantalum capacitor
L1, L2, L3	ferrite bead
R1	75-ohm 1% metal film resistor
R2	1000-ohm 1% metal film resistor
R3	27-ohm 1% metal film resistor
RSET	1% metal film resistor
Z1	1.2v voltage reference

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with the SETUP pin floating and an RSET value of about 1594 ohms. If the Bt102/883 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/ (20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may always be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full scale output current is:

IOUT (mA) = K * VREF (v) / RSET (ohms)

where K is equal to 17,714; 17,158; or 15,933 for SETUP = VAA, float, and AGND, respectively.

Using Multiple Devices

If located close together on the same PC board, multiple Bt102/883 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt102/883 must still have it's individual RSET resistor, IOUT termination resistor (R1 in Figure 3), IRET ferrite bead (L3 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R3 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to high current return.

Non-Video Applications

The Bt102/883 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero, while REF WHITE*, 10% OVERBRIGHT*, and BLANK* should be a logical one. SETUP should be connected to AGND. The output current will be determined solely by the D0 - D7 inputs.

The relationship between RSET and the full scale output current in this configuration is as follows:

RSET (ohms) = 15,933 * VREF (v) / IOUT (mA)

The BLANK* input may optionally be used as a "force to zero" control, and the REF WHITE* input may optionally be used as a "force to full scale" control.

COMP Resistor

To optimize the settling time of the Bt102/883, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 27 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 185	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
θ JC				25	°C. / W
θ JA				60	°C. / W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL				
at -55 °C.				± 3/4	LSB
at +25 and +125 °C.				± 1/2	LSB
Differential Linearity Error	DL			± 1/2	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity**			guaranteed		
Coding					Binary
Digital Inputs					
TTL Compatible Mode					
Input High Voltage	VIH				
CLOCK		3.0			Volts
Other		2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4v)	IIH	- 200		- 1200	µA
Input Low Current (Vin = 0.4v)	IIL	- 200		- 1200	µA
Input Capacitance*	CIN		10		pF
CMOS Compatible Mode					
Input High Voltage	VIH	3.5			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 3.5v)	IIH			2	µA
Input Low Current (Vin = 1.5v)	IIL			2	µA
Input Capacitance*	CIN		10		pF
Voltage Reference Input Current (VREF = 1.235v)	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): 100% tested at VAA = 4.75v and 5.25v, TA = -55°, 25°, and 125° C., RSET = 1110 ohms ± 0.1%, VREF = 1.235v.

*Derived from characterization, not tested (TA = 25°C., VAA = 5v ± 5%).

**Guaranteed by design, not tested.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Output Gray Scale Current Range				20.50	mA
Output Current (SETUP = float, RSET = 1110Ω) Overbright Relative to White White Level Relative to Blank White Level Relative to Black Black Level Relative to Blank Blank Level Sync Level LSB Size*		 1.60 17.90 16.80 1.10 7.20 0	 1.93 19.09 17.72 1.37 7.72 5 69.49	 2.40 20.31 18.61 1.70 8.30 50	 mA mA mA mA mA µA µA
Output Current (SETUP = AGND, RSET = 1050Ω) Overbright Relative to White* White Level Relative to Blank White Level Relative to Black Black Level Relative to Blank Blank Level Sync Level LSB Size*		 17.80 17.80 0 7.70 0	 2.03 18.74 18.74 5 8.23 5 73.49	 19.75 19.70 50 9.00 50	 mA mA mA µA mA µA µA
Output Current (SETUP = VAA, RSET = 1130Ω) Overbright Relative to White* White Level Relative to Blank White Level Relative to Black Black Level Relative to Blank Blank Level Sync Level LSB Size*		 18.00 16.50 1.50 7.10 0	 1.89 19.36 17.42 1.94 7.65 5 68.31	 20.60 18.30 2.30 8.30 50	 mA mA mA mA mA µA µA
Output Compliance Output Capacitance*	VOC COUT		 20	+ 1.4	Volts pF

Test conditions (unless otherwise specified): 100% tested at VAA = 4.75v and 5.25v, TA = -55°, 25°, and 125° C., VREF = 1.235v, RSET = 1110 ohms ± 0.1%, THRESHOLD SET = TTL mode.

*Derived from characterization, not tested (TA = 25° C., VAA = 5v ± 5%).

**Guaranteed by design, not tested.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			50	MHz
Data and Control Setup Time	TSU	5			ns
Data and Control Hold Time	TH	2			ns
Clock Cycle Time	TCYC	20			ns
Clock Pulse Width Low	TCLKH	7			ns
Clock Pulse Width High	TCLKL	7			ns
Analog Output Delay	TDLY				
TA = -55° C.				22	ns
TA = 25° C.				26	ns
TA = 125° C.				36	ns
Analog Output Rise/Fall Time	TVRF			6	ns
Analog Output Settling Time*	TS				
to ± 1/2 LSB			20		ns
to ± 1 LSB			15		ns
Clock and Data Feedthrough*			- 20		dB
Glitch Impulse*			100		pV - sec
Pipeline Delay		3	3	3	Clocks
VAA Supply Current**	IAA		110	175	mA

Test conditions (unless otherwise specified): 100% testing at VAA = 4.75v and 5.25v with TA = 25°C. QCI sample tested at VAA = 4.75v and 5.25v with TA = -55°, 25°, and 125°C. RSET = 1110 ohms ± 0.1%, VREF = 1.235v. THRESHOLD SET = TTL mode, SETUP = float. Input values are 0.4 to 3.5 volts on CLOCK, and 0 to 3 volts on control and data, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 27 ohms. Analog output load ~ 10 pF with doubly-terminated 50-ohm line. See timing notes in Figure 4.

Note: Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 100 MHz.

*Derived from characterization, not tested (TA = 25° C., VAA = 5v ± 5%).

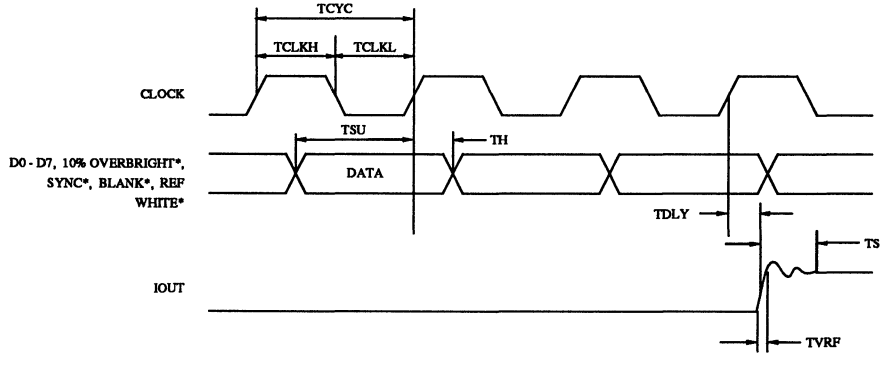
**at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v. IAA (max) 100% tested at TA = 25° C. IAA (typ) based on characterization.

Ordering Information

Model Number	MTBF* (hours)	Package	Ambient Temperature Range
Bt102TC883	2.7 x 10^6	24-pin 0.3" Ceramic Sidebraze DIP	-55° to +125° C.

*MTBF is calculated per MIL Handbook 217.

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB or ± 1 LSB.

Note 3: Output rise/fall time measured between the 20% and 80% points of full scale transition.

Figure 4. Input/Output Timing.

Bt438/883

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

MIL-STD-883C, Class B

125 MHz

Clock Generator Chip

for CMOS RAMDACs™

Distinguishing Features

- 125 MHz Operation
- Differential ECL Clock Generation
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- 1.32v Typical Voltage Reference Output
- Single +5v Power Supply
- 20-pin Ceramic Sidebraze DIP Package
- Typical Power Dissipation: 325 mW

Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability

Related Products

- Bt458/883

Product Description

The Bt438/883 is a clock generator for the high speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5v supply to the RAMDAC, generating the necessary clock and control signals.

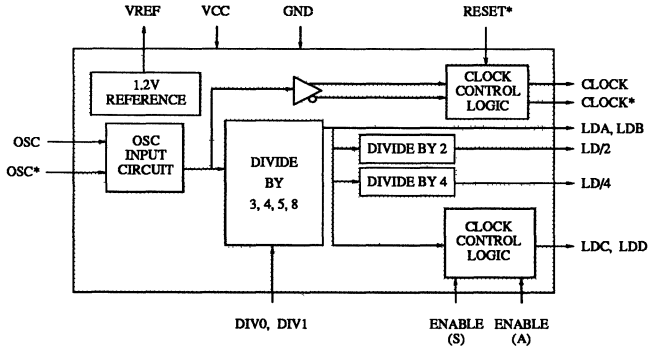
The clock output may be divided by 3, 4, 5, or 8 to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438/883 also optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay of 8 clock cycles.

An on-chip voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
(800) VIDEO IC
TLX: 383 596
FAX: (619) 452-1249
L438M01

Brooktree®

Bt453/883

MIL-STD-883C, Class B

Monolithic CMOS

256 x 24 Color Palette

40 MHz RAMDAC™

Distinguishing Features

- 40 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343A/RS-170 Compatible Outputs
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 40-pin Ceramic Sidebraze DIP Package
- Typical Power Dissipation: 950 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

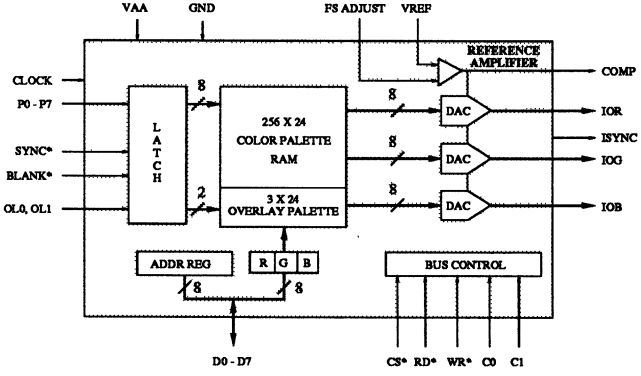
Product Description

The Bt453/883 RAMDAC is designed specifically for high resolution color graphics.

It has a 256 x 24 color lookup table with triple 8-bit video D/A converters, supporting up to 259 simultaneous colors from a 16.8 million color palette. Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453/883 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Both the differential and linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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L453M01 Rev. B

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt453/883 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

Note that anytime the CS* input is a logical zero, the video outputs are forced to the black level. When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the six most significant bits of the address register (ADDR2 - 7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2.

Figure 1 illustrates the MPU read/write timing.

C1	C0	Addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0	1	color palette RAM
	xxxx xx00	1	1	reserved
	xxxx xx01	1	1	overlay color 1
	xxxx xx10	1	1	overlay color 2
	xxxx xx11	1	1	overlay color 3

Table 2. Address Register (ADDR) Operation.

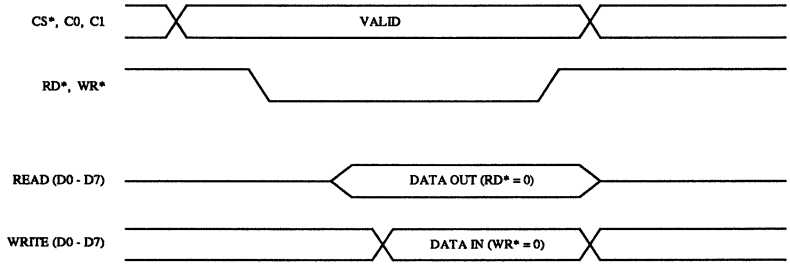


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

While CS* is a logical one, the P0 - P7, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The addressed location provides 24 bits of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 4 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt453/883 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

OL1	OL0	P0 - P7	Addressed by frame buffer
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
:	:	:	:
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2
1	1	$xx	overlay color 3

Table 3. Pixel and Overlay Control Truth Table.

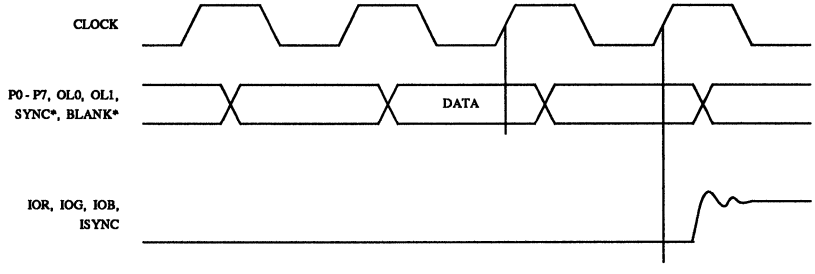
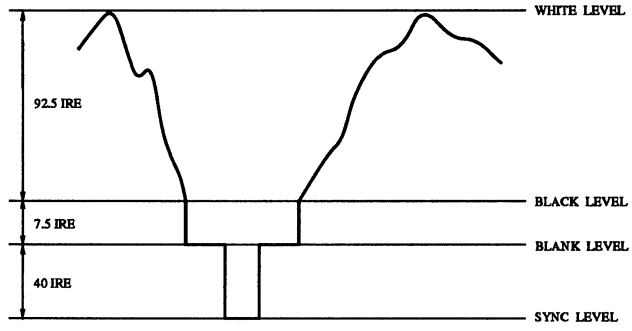


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 280 ohms, VREF = 1.235v. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 280 ohms, VREF = 1.235v. ISYNC connected to IOG.

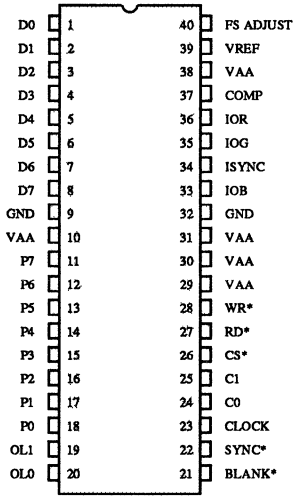
Table 4. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 4. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. This high impedance current source is typically connected directly to the IOG output (Figure 4), and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is: ISYNC (mA) = 1,728 * VREF (v) / RSET (ohms) If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is (assuming ISYNC is connected to IOG): RSET (ohms) = 6,047 * VREF (v) / IOG (mA) The relationship between RSET and the full scale output current on IOR and IOB is: IOR, IOB (mA) = 4,319 * VREF (v) / RSET (ohms)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.2v (typical) reference. The Bt453/883 has an internal pull-up resistor between VREF and VAA. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black level. Note that the Bt453/883 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt453/883 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all Bt453/883 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt453/883, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the Bt453/883.

Power Planes

The Bt453/883 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within three inches of the Bt453/883.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt453/883 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the three groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt453/883 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt453/883 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the Bt453/883 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (VCC), and not the analog power plane.

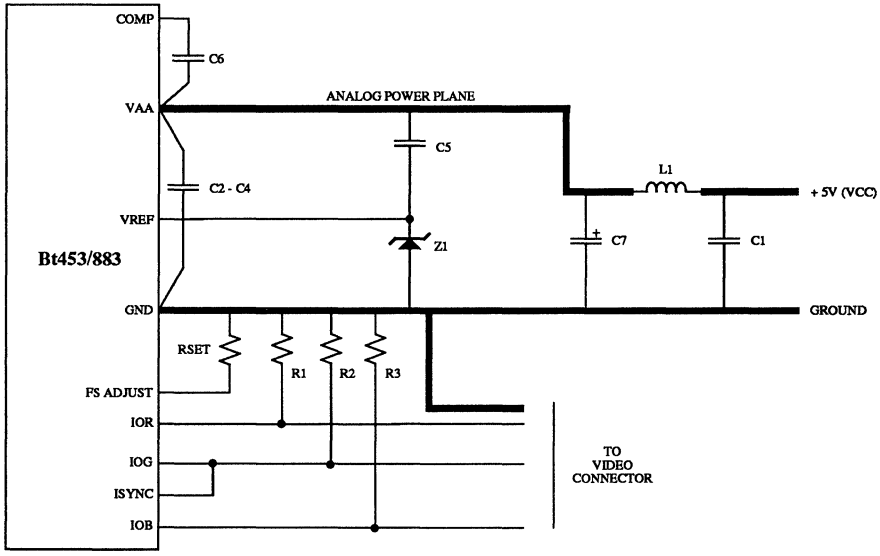
Analog Signal Interconnect

The Bt453/883 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the Bt453/883 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description
C1 - C6	0.1 µF ceramic capacitor
C7	10 µF tantalum capacitor
L1	ferrite bead
R1, R2, R3	75-ohm 1% metal film resistor
RSET	280-ohm 1% metal film resistor
Z1	1.2v voltage reference

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt453/883.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.0	5.5	Volts
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts
FS ADJUST Resistor	RSET		280		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
θ JC				18	°C. / W
θ JA				28	°C. / W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH				
CLOCK		2.4			Volts
Other		2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = VAA)	IIH			1	µA
Input Low Current (Vin = 0v)	IIL			- 1	µA
Input Capacitance**	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			10	µA
Output Capacitance**	CDOUT		20		pF
Analog Outputs***					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	1	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	1	50	µA
LSB Size**			69.1		µA
DAC to DAC Matching			3.5	7	%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Capacitance**	CAOUT		30		pF

Test conditions (unless otherwise specified): 100% tested at VAA = 4.5v and 5.5v, TA = -55°, 25°, and 125° C., RSET = 280 ± 0.1% ohms, VREF = 1.235v.

**Derived from characterization, not tested (TA = 25° C., VAA = 5v ± 10%).

***ISYNC connected to IOG.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			40	MHz
CS*, C0, C1 Setup Time	1	35			ns
CS*, C0, C1 Hold Time	2	35			ns
RD*, WR* High Time	3	25			ns
RD* Asserted to Data Bus Driven	4				
TA = 25° C., 125° C.		5			ns
TA = - 55° C.		2			ns
RD* Asserted to Data Valid	5			100	ns
RD* Negated to Data Bus 3-Stated	6			15	ns
WR* Low Time	7	50			ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	5			ns
Pixel and Control Setup Time	10	7			ns
Pixel and Control Hold Time	11	3			ns
Clock Cycle Time	12	25			ns
Clock Pulse Width High	13	7			ns
Clock Pulse Width Low	14	7			ns
Analog Output Rise/Fall Time	15			8	ns
Analog Output Settling Time**	16		25		ns
VAA Supply Current***	IAA		190	300	mA

Test conditions (unless otherwise specified): 100% testing at VAA = 4.5v and 5.5v with TA = 25°C. QCI sample tested at VAA = 4.5v and 5.5v with TA = -55°, 25°, and 125°C. RSET = 280 ohms ± 0.1%, VREF = 1.235v. Input values are 0.8 to 2.4 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ~ 75 pF with doubly-terminated 50-ohm line. D0 - D7 output load ~ 75 pF. See timing notes in Figure 6.

**Derived from characterization, not tested (TA = 25° C., VAA = 5v ± 10%).

***at Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.5v. IAA (max) 100% tested at TA = 25° C. IAA (typ) based on characterization.

Timing Waveforms

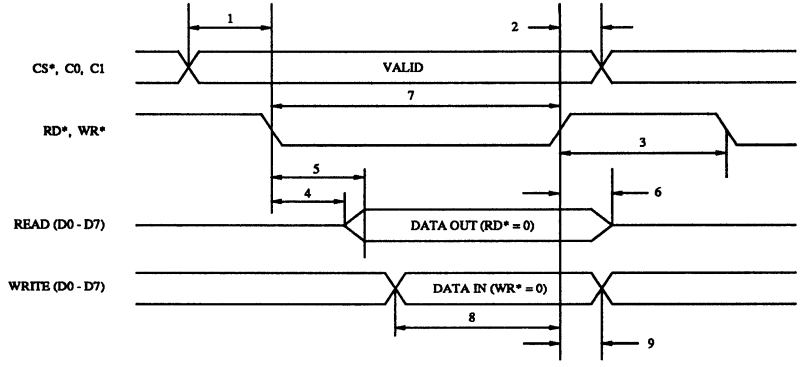
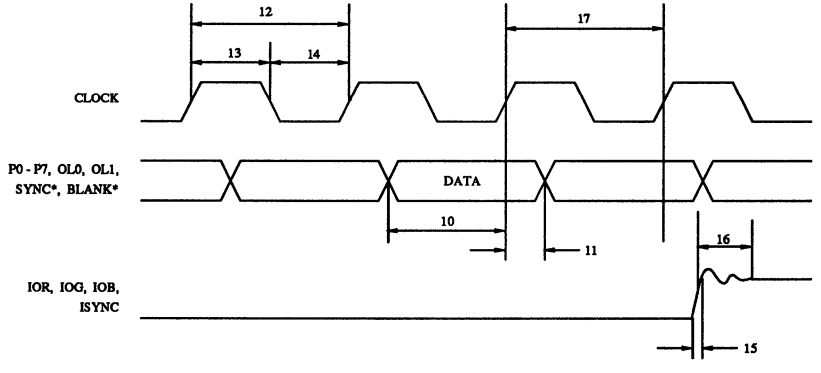


Figure 5. MPU Read/Write Timing.



Note 1: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 2: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	MTBF* (hours)	Package	Ambient Temperature Range
Bt453SC883	0.54×10^6	40-pin 0.6" Ceramic Sidebraze DIP	-55° to +125° C.

*MTBF is calculated per MIL Handbook 217.

Bt458/883

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

MIL-STD-883C, Class B

Monolithic CMOS

256 x 24 Color Palette

110 MHz RAMDAC™

Distinguishing Features

- 110 MHz Pipelined Operation
- Multiplexed TTL Pixel Ports
- Triple 8-bit D/A Converters
- 256 x 24 Dual Port Color Palette
- 4 x 24 Dual Port Overlay Registers
- RS-343A Compatible RGB Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 84-pin Ceramic PGA Package
- Typical Power Dissipation: 2 W

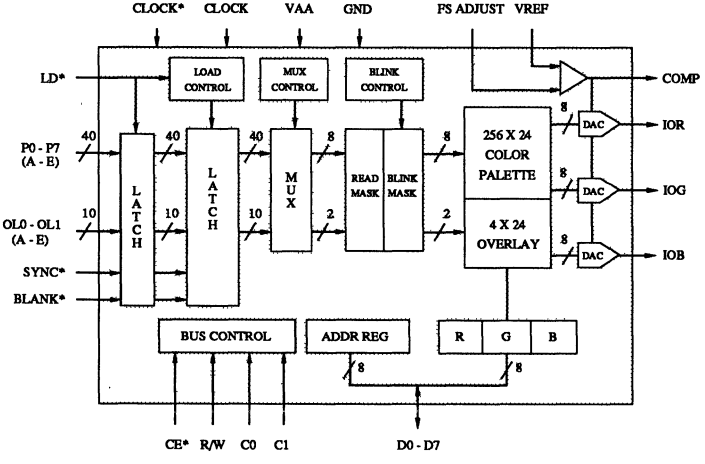
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Related Products

- Bt438/883

Functional Block Diagram



Product Description

The Bt458/883 is a triple 8-bit RAMDAC designed specifically for high performance, high resolution color graphics.

The architecture enables the display of 1280 x 1024 bit mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 28 MHz) to the frame buffer, while maintaining the 110 MHz video data rates required for sophisticated color graphics.

The Bt458/883 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. On chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt458/883 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering.

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Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
(800) VIDEO IC
TLX: 383 596
FAX: (619) 452-1249
L458M01

Brooktree®

Brooktree®

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Table of Contents

Part Numbering System

Bt458 K G 125 883

optional MIL-STD 883C, Class B processing for the S temperature range.

optional speed gradeout information. For VIDEODACs and RAMDACs, specifies MHz.

package type:

C	CERDIP
CJ	ceramic J-lead (CERQUAD)
D	ceramic sidebraze DIP
F	ceramic flatpack (with heatsink)
FN	ceramic flatpack (no heatsink)
G	ceramic PGA
L	ceramic leadless chip carrier
P	plastic DIP
PJ	plastic J-lead (PLCC)
PF	plastic Quad flatpack
S	150 mil SOIC
SW	300 mil SOIC

performance gradeout:

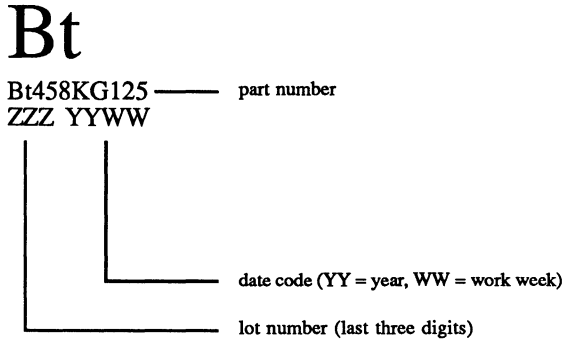
B	- 25 to + 85 °C.
K	0 to + 70 °C. (0 to + 85 °C. for 100K ECL)
L	0 to + 70 °C., Low power
S	- 55 to + 125 °C.

For other than standard grades, refer to the individual datasheet for letter designation.

basic model number

100 - 149	D/A converters
200 - 249	A/D converters
250 - 299	imaging components
300 - 399	reserved
400 - 449	graphics peripherals
450 - 499	RAMDACs
500 - 599	general components
600 - 699	ATE components
700 - 799	reserved
800 - 899	reserved
900 - 999	reserved

Device Marking (Top)



Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$PD = (TJ - TA) / \theta JA$$

where:

PD = power dissipation at ambient operating temperature
TJ = maximum junction operating temperature (typically 150 °C. is used)
TA = maximum ambient operating temperature (free air)
θ JA = typical thermal resistance of junction to ambient (°C / W)

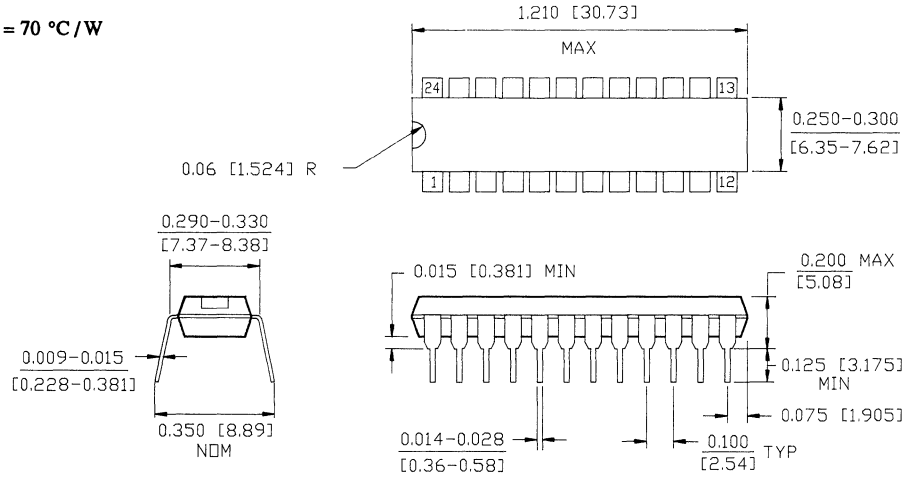
Packaging Notes

1. Unless otherwise indicated, all thermal impedances listed are typical range values or values in static free air for the package only. These impedances will vary when additional heat sinking capability is provided through PCB solder attachment or air flow.

Plastic DIP Packages

24-Pin 0.3" Plastic DIP

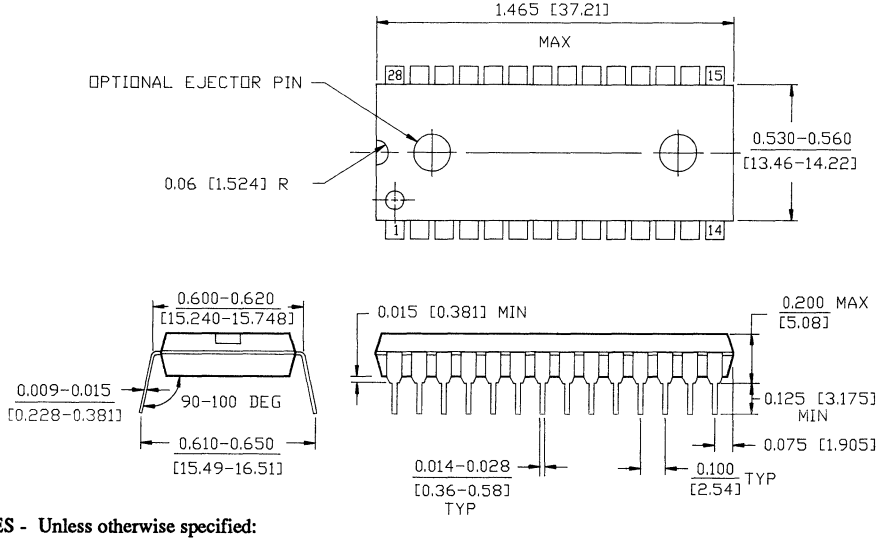
θJA = 70 °C/W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

28-Pin 0.6" Plastic DIP

θJA = 60 °C/W

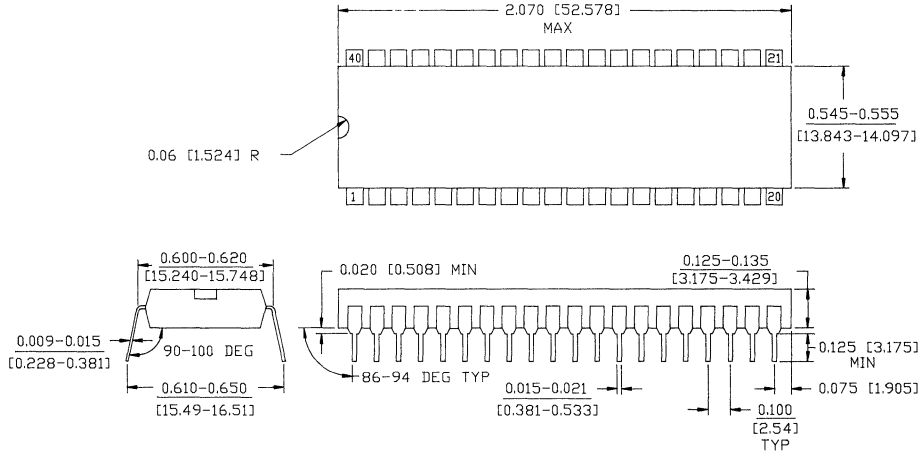


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Plastic DIP Packages (continued)

40-Pin 0.6" Plastic DIP

θJA = 50 °C/W

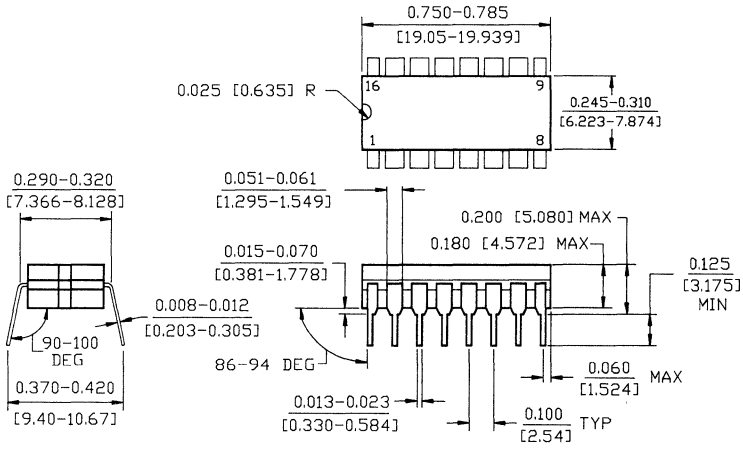


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

CERDIP Packages

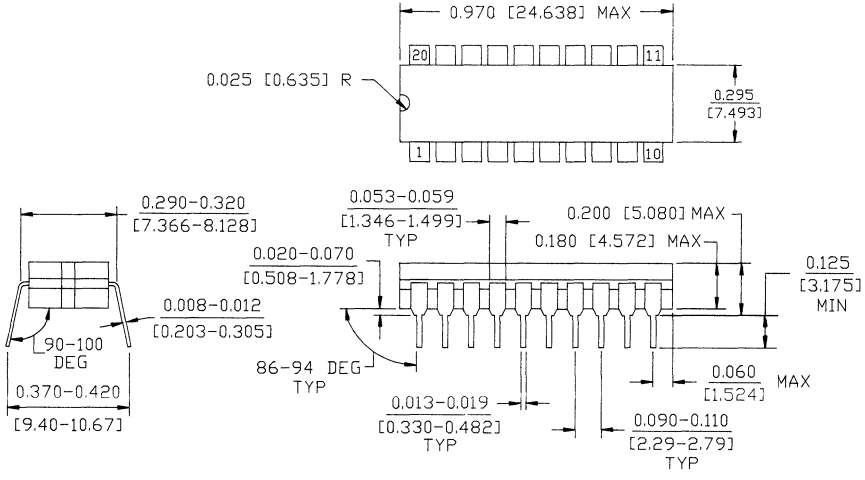
16-Pin 0.3" CERDIP

θ JA = 90 to 95 °C / W



20-Pin 0.3" CERDIP

θ JA = 85 to 90 °C / W

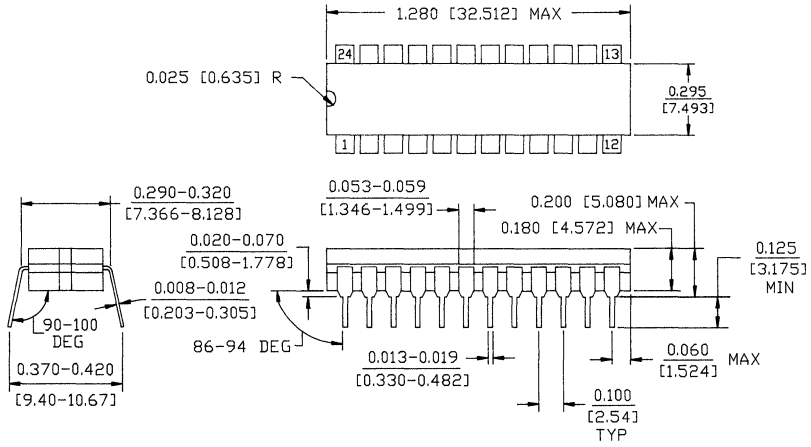


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

CERDIP Packages (continued)

24-Pin 0.3" CERDIP

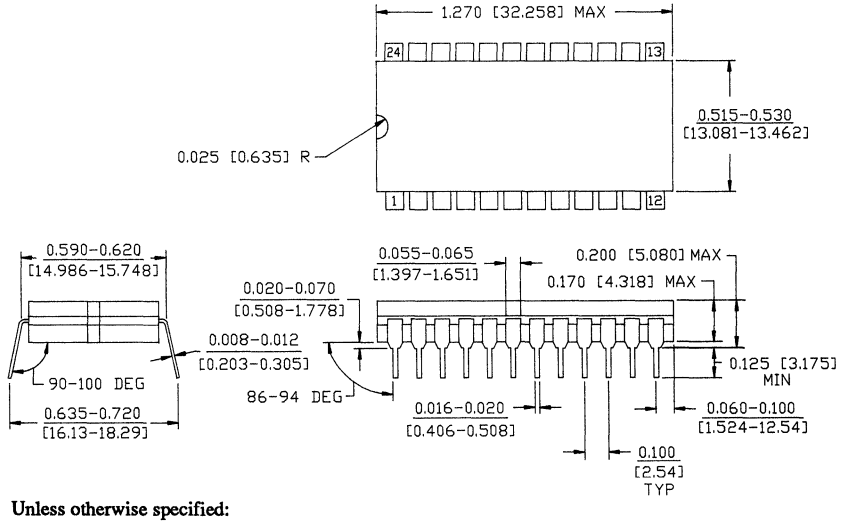
θ JA = 75 to 80 °C / W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" CERDIP

θ JA = 55 to 60 °C / W

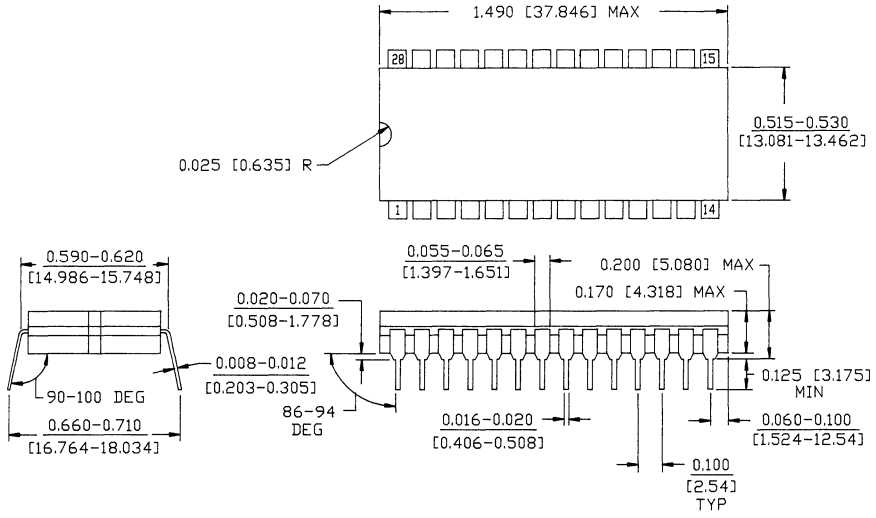


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

CERDIP Packages (continued)

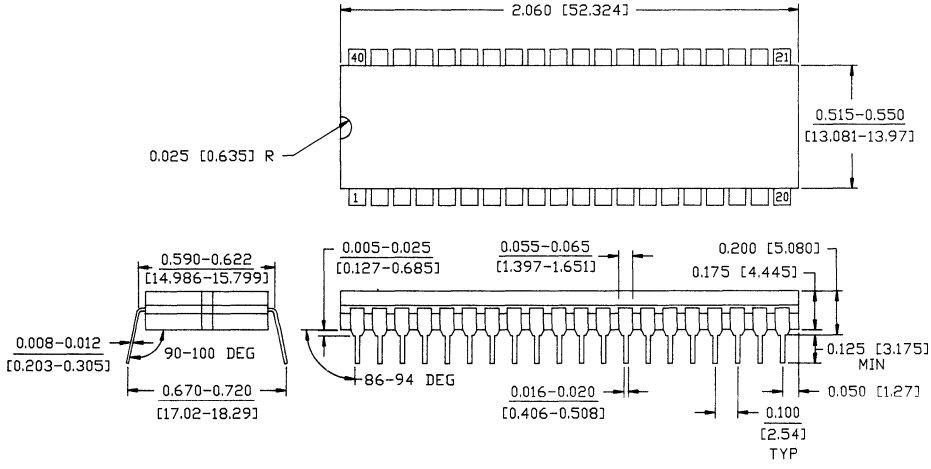
28-Pin 0.6" CERDIP

θ JA = 55 to 60 °C / W



40-Pin 0.6" CERDIP

θ JA = 50 to 55 °C / W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

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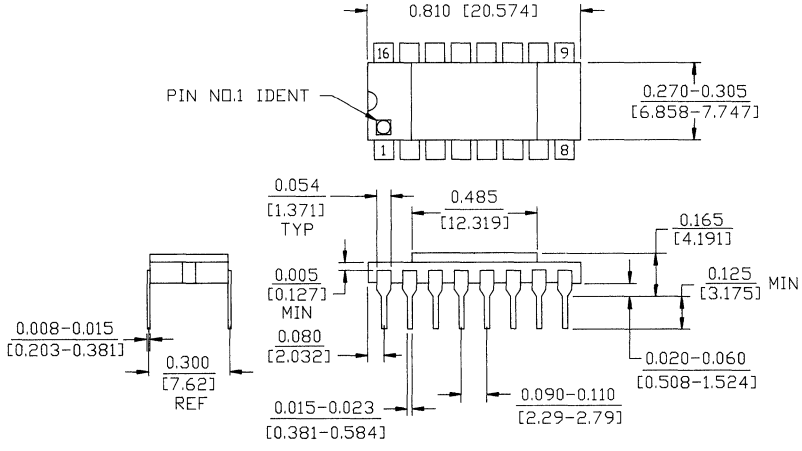
Ceramic Sidebraze DIP Packages

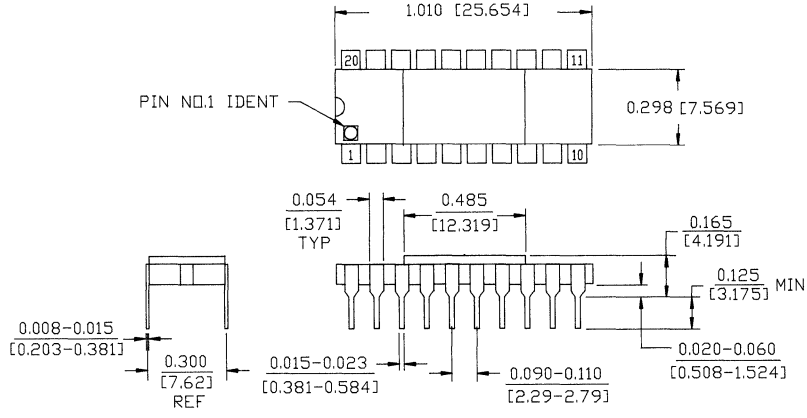
16-Pin 0.3" Ceramic Sidebraze DIP

θ JA = 95 °C / W



20-Pin 0.3" Ceramic Sidebraze DIP

θ JA = 85 to 90 °C / W



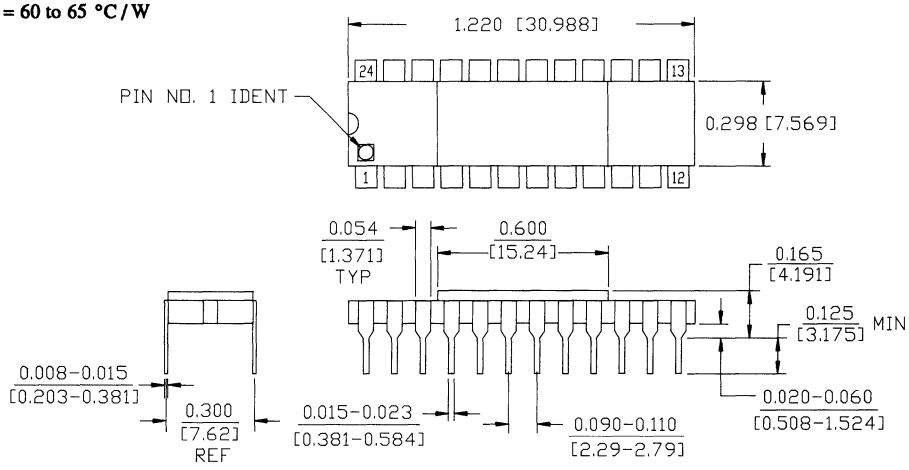
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

Ceramic Sidebraze DIP Packages (continued)

24-Pin 0.3" Ceramic Sidebraze DIP

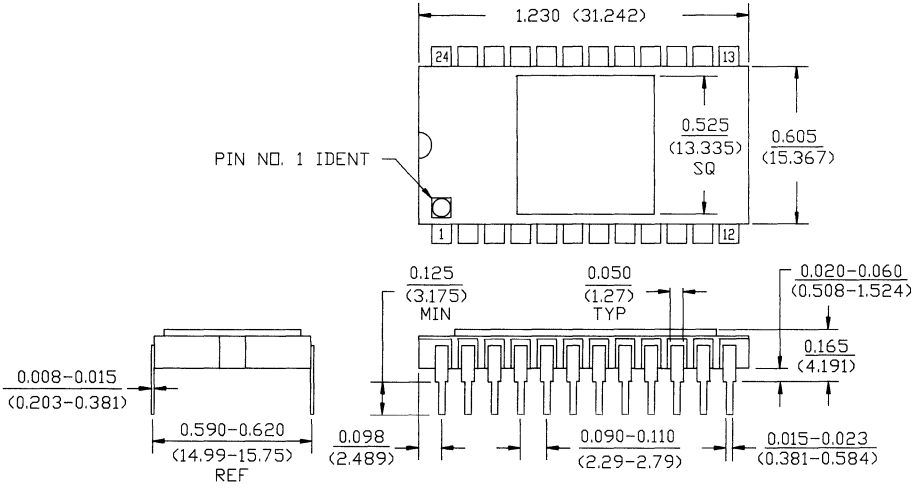
θ JA = 60 to 65 °C / W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" Ceramic Sidebraze DIP

θ JA = 55 to 60 °C / W

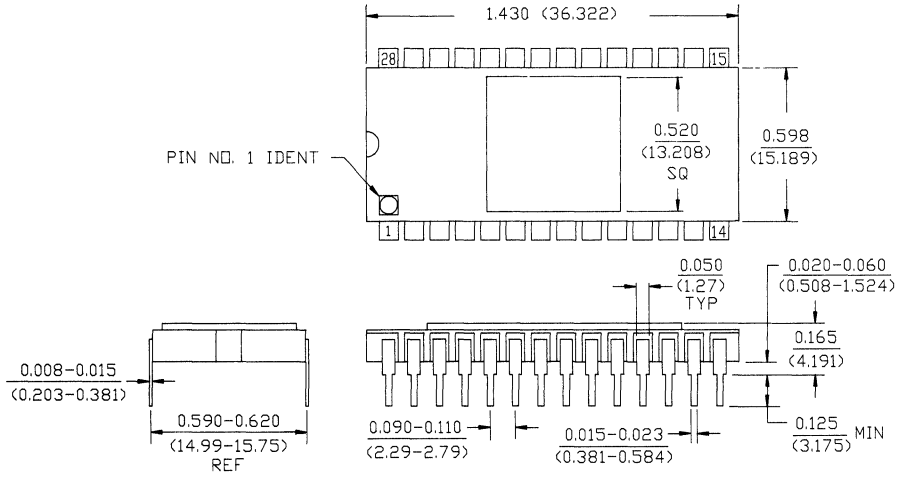


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Sidebraze DIP Packages (continued)

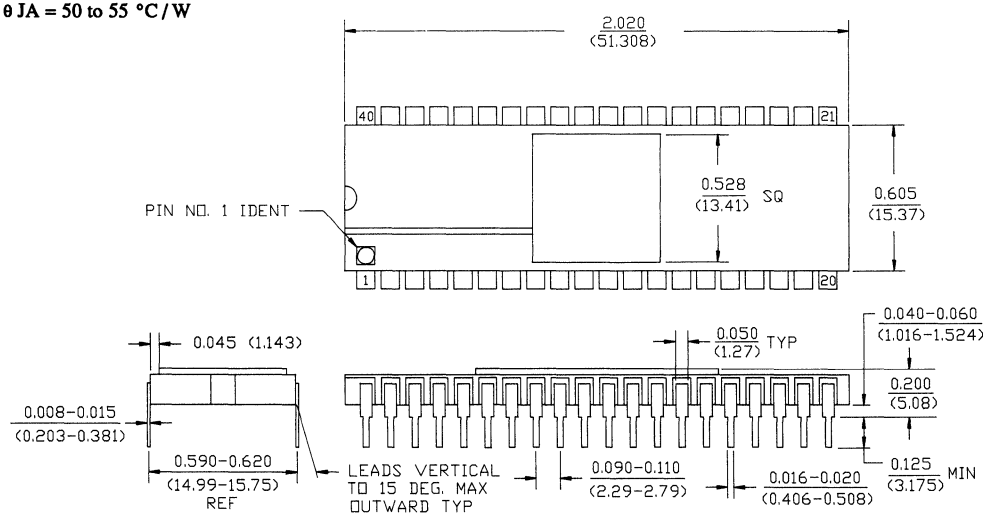
28-Pin 0.6" Ceramic Sidebraze DIP

θ JA = 55 to 60 °C / W



40-Pin 0.6" Ceramic Sidebraze DIP

θ JA = 50 to 55 °C / W



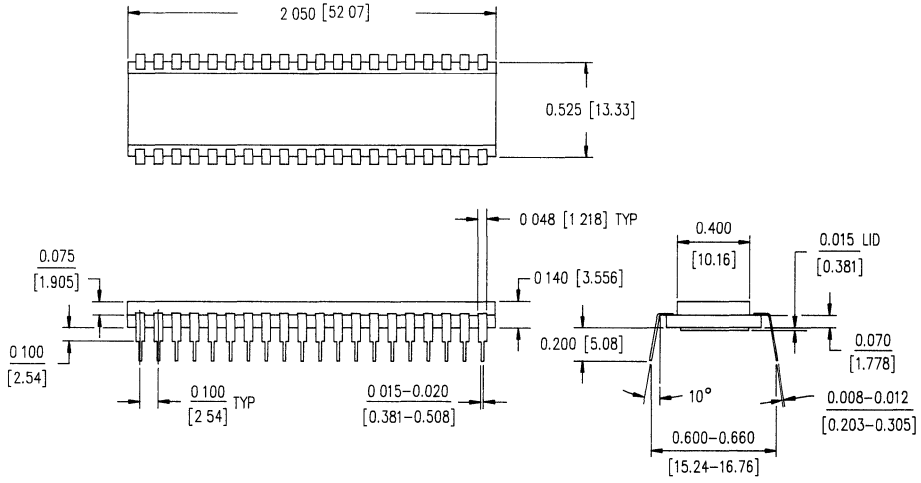
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Cavity Down DIP Packages

40-Pin 0.6" Ceramic Cavity Down DIP

θ JA = 30 to 40 °C / W

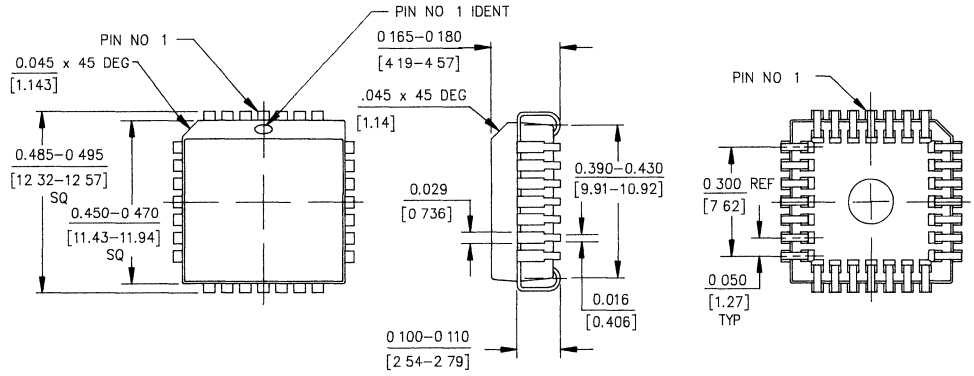


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Plastic J-Lead (PLCC) Packages

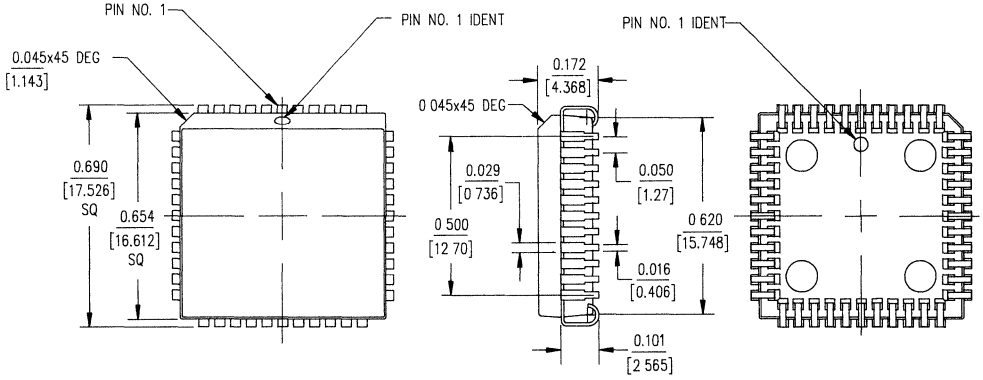
28-Pin Plastic J-Lead

θ JA = 75 to 80 °C / W



44-Pin Plastic J-Lead

θ JA = 42 to 48 °C / W

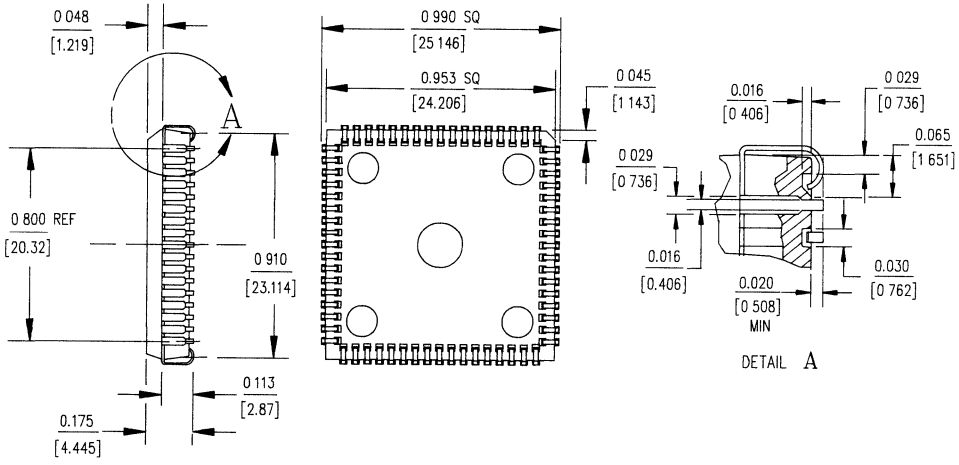


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

68-Pin Plastic J-Lead

θ JA = 42 to 48 °C / W

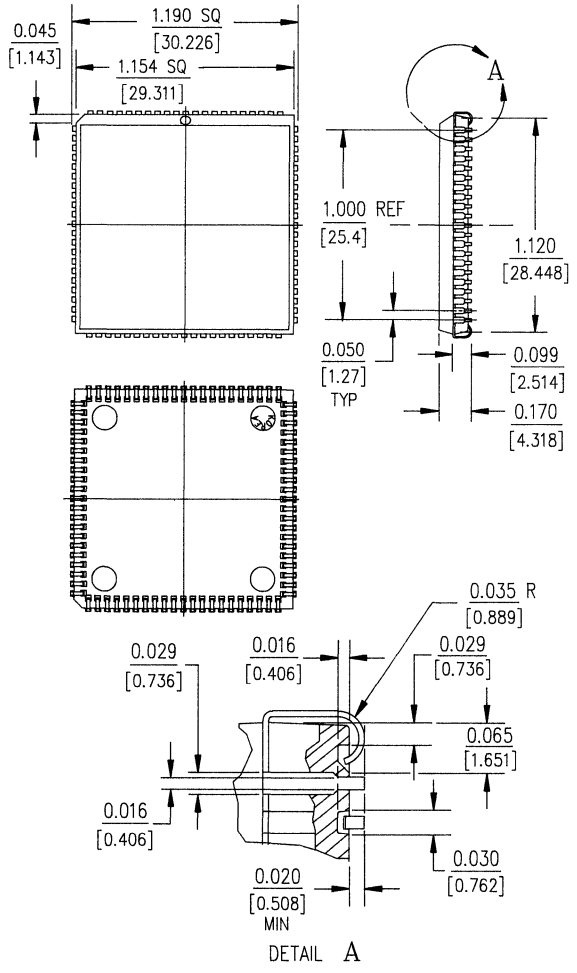


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

84-Pin Plastic J-Lead

θ JA = 42 to 48 °C / W

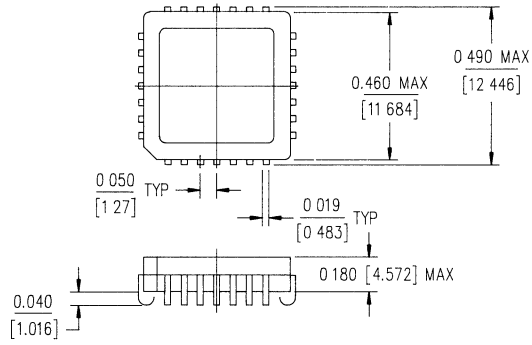


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ceramic J-Lead (CERQUAD) Packages

28-Pin Ceramic J-Lead

θ JA = 60 to 65 °C / W

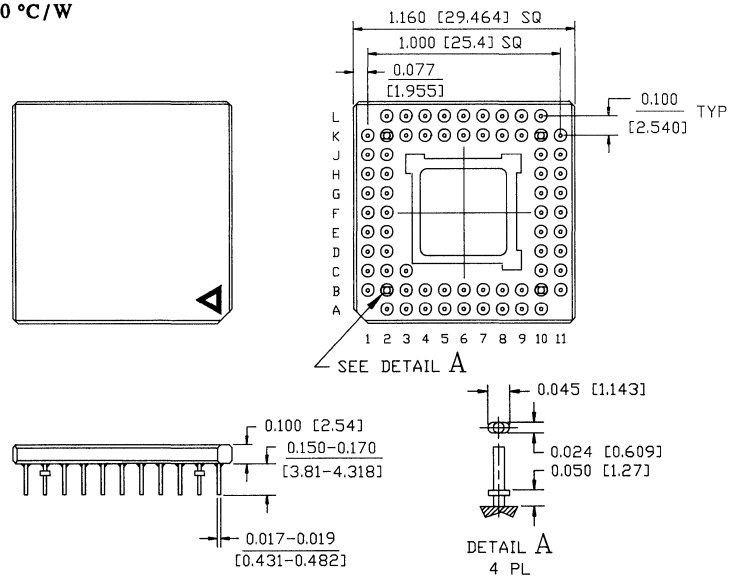


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. CERQUAD packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ceramic Pin Grid Array (PGA) Packages

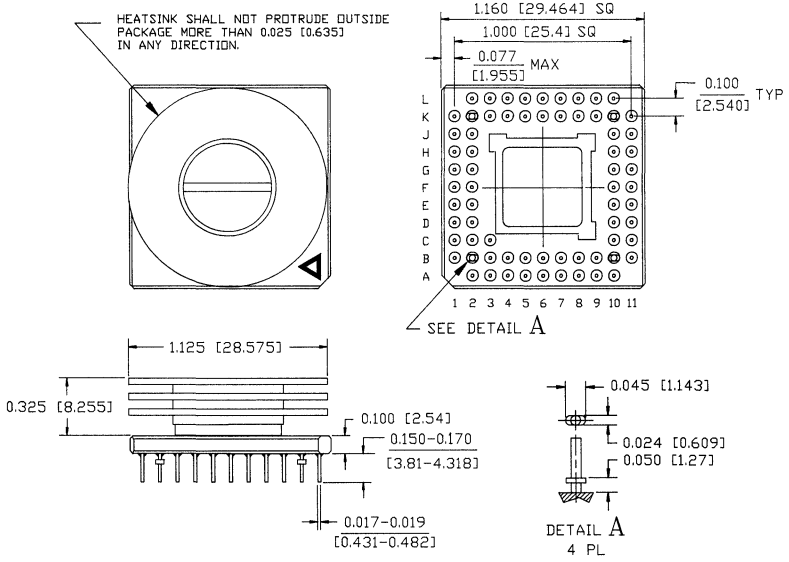
68-Pin Ceramic PGA

θ JA = 30 to 40 °C / W



68-Pin Ceramic PGA with Heatsink and Alignment Pin

θ JA = 27 to 34 °C / W



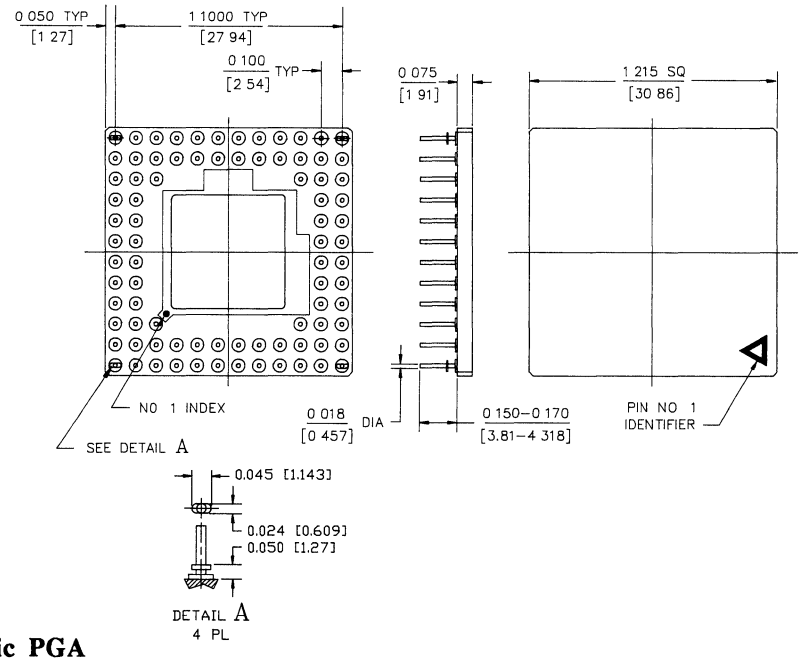
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Pin Grid Array (PGA) Packages (continued)

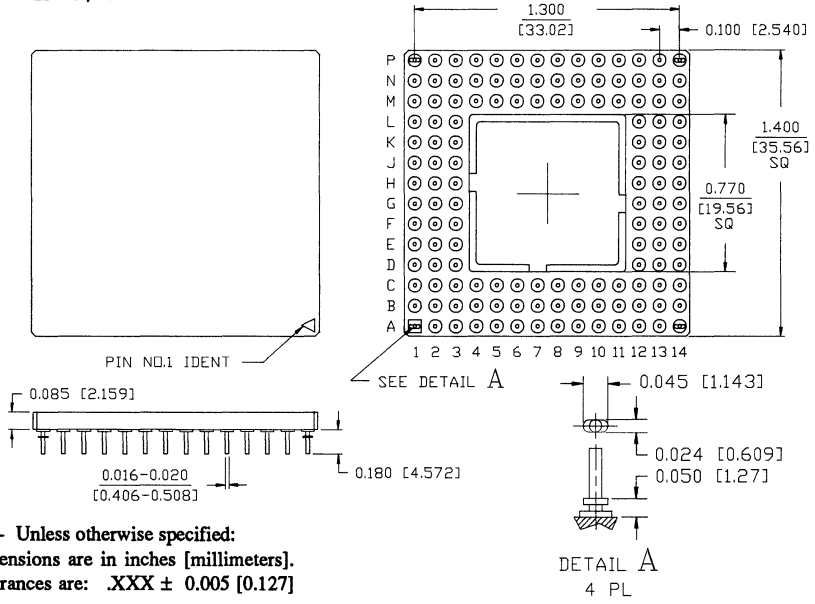
84-Pin Ceramic PGA

θ JA = 25 to 30 °C / W



132-Pin Ceramic PGA

θ JA = 20 to 25 °C / W



NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

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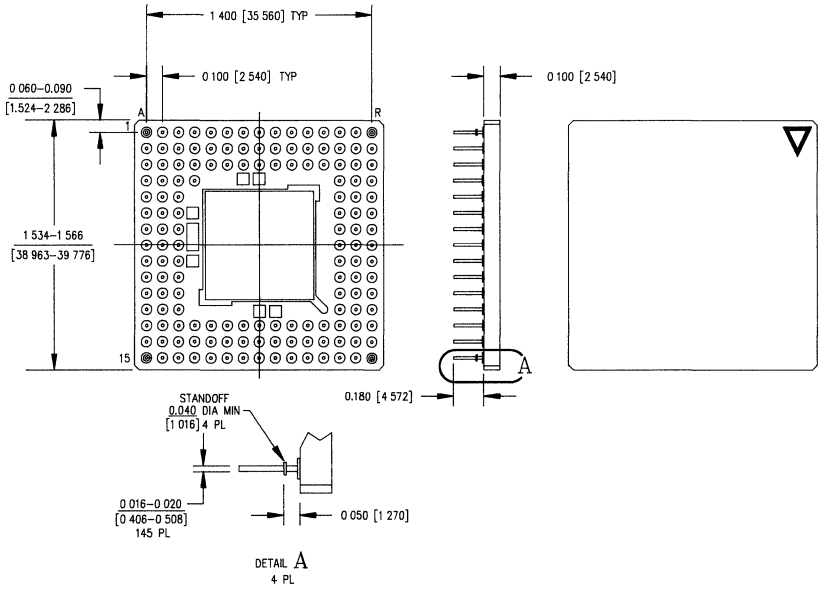
Ceramic Pin Grid Array (PGA) Packages (continued)

144-Pin Ceramic PGA with Alignment Pin

θ JA = 18 to 23 °C / W

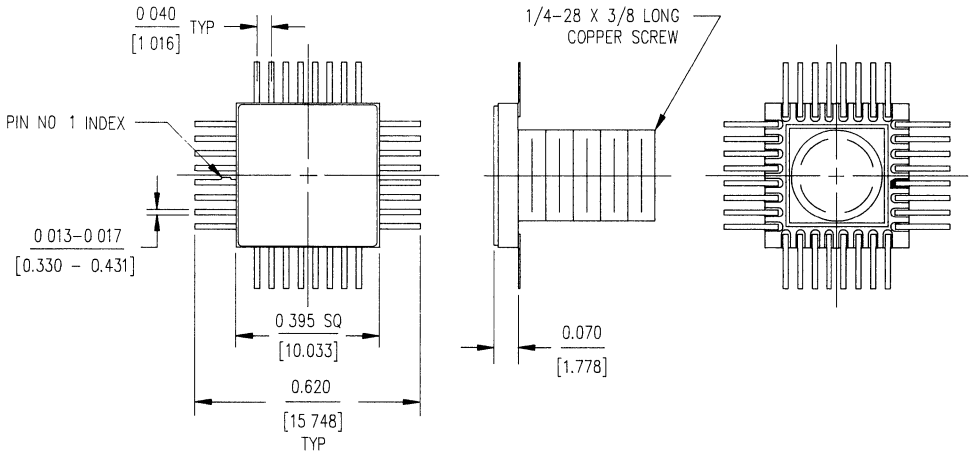


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Flatpack Packages

32-Pin Ceramic Flatpack with Heat Sink

θ JA = 20 to 25 °C / W

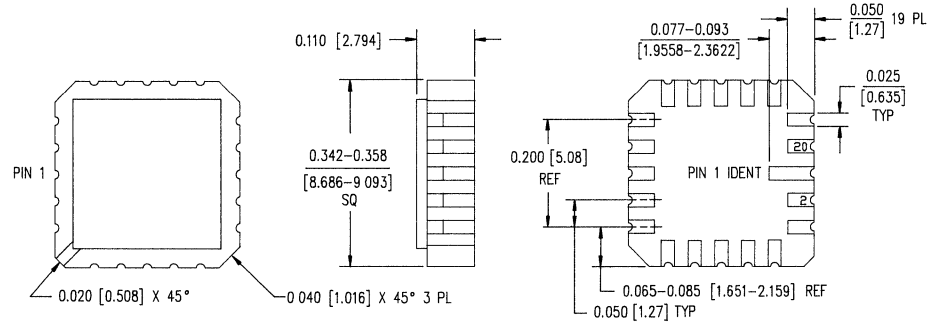


NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Leadless Chip Carrier Packages

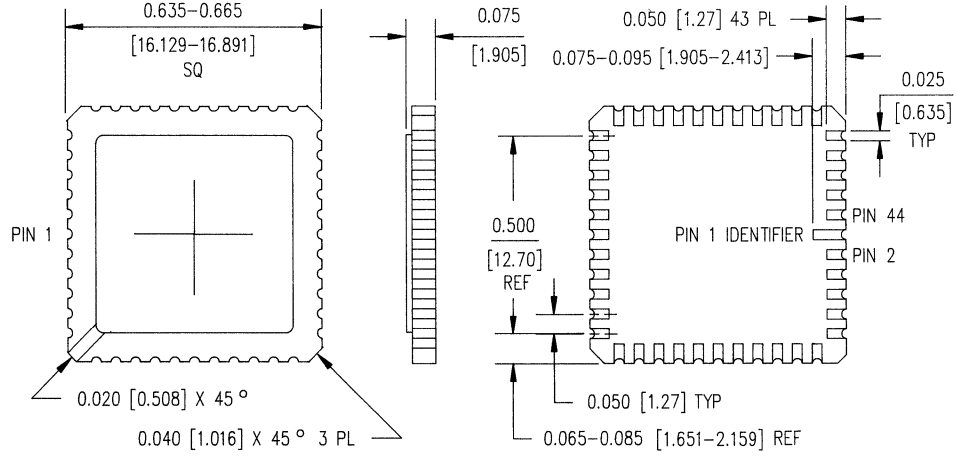
20-Pin Ceramic Leadless Chip Carrier

θJA = 90 °C/W



44-Pin Ceramic Leadless Chip Carrier

θJA = 100 °C/W



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

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Solon, OH 44139
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FAX: (216) 248-2312

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FAX: (503) 629-8645

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Anthem
Horsham Business Center
355 Business Center Drive
Horsham, PA 19044
(215) 443-5150
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158 Gaither Drive
Mt. Laurel, NJ 08054
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FAX: (609) 778-1819

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Western

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FAX: (508) 657-6008

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Quality Components
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FAX: (512) 339-9252

Quality Components
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Sugarland, TX 77478
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FAX: (713) 240-6988

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Marshall
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