82C570 CHIPSLink™
SINGLE CHIP "3270" PROTOCOL CONTROLLER

- **Implements IBM 3270 Communication Protocol**
- **Provides IBM 3278/79 and IRMA™ emulation adapter cards interface**
- **Supports both CUT and DFT modes**
- **Type A coaxial transmitter and receiver**
- **8X Digital Phase Locked Loop (DPLL)**
- **On chip 4.7 MIPS microcontroller**
- **Dual port RAM control function**
- **2.4K bytes internal microcode**
- **Provisions for external microcode**
- **Low power CMOS technology**
- **18.8696 MHz crystal oscillator**
- **84 pins PLCC package**

The 82C570 is a highly integrated IBM 3270 coaxial type A protocol controller chip. It serves as an I/O processor to emulate most of the IBM terminals and printers. It works with IBM 3276/3274/3174 control units either locally or remotely attached.

The 82C570 internal microcode supports most display terminals and printers in both CUT and DFT modes except 3279-S3G due to the large memory requirement. The programmed symbol and APA graphics for 3179/G and 3270 PC/G can only be supported in DFT mode. There are provisions for adding an additional 8K × 8 SRAM and using external microcode.

The 82C570 provides both IRMA and IBM emulation adapter compatible interface. All the IRMA and IBM emulation, file transfer and application software can run on the adapter using 82C570.

The 82C570 along with an external 120ns 8K × 8 SRAM , line driver, line receiver and pulse transformer, a complete 3270 protocol emulation adapter can be built easily.

The 82C570 is fabricated using advanced CMOS technology and is packaged in an 84 pin PLCC.

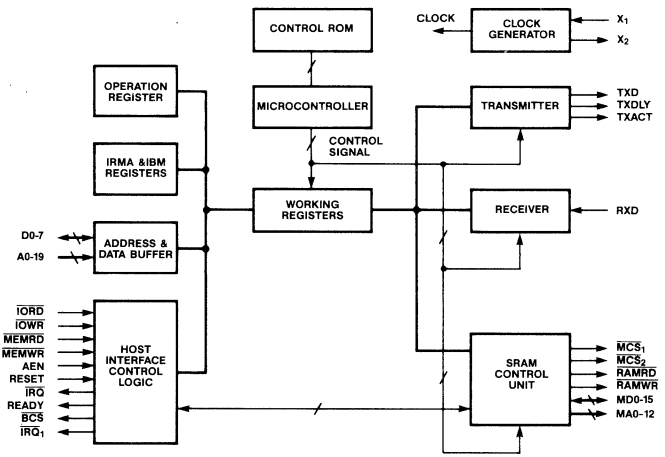
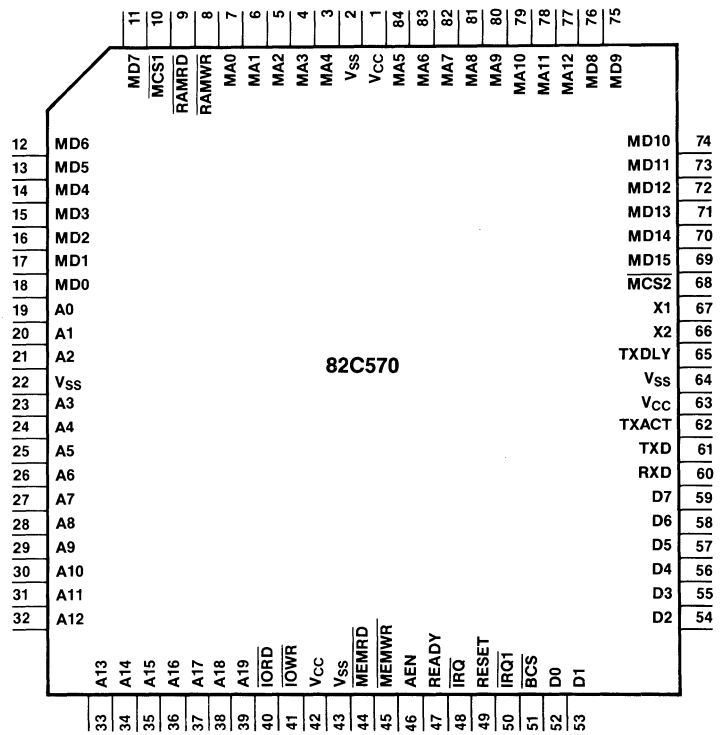


Figure 1. 82C570 Functional Block Diagram


82C570
1 VCC
2 VSS
3 MA4
4 MA3
5 MA2
6 MA1
7 MA0
8 RAMWR
9 RAMRD
10 MCS1
11 MD7
12 MD6
13 MD5
14 MD4
15 MD3
16 MD2
17 MD1
18 MD0
19 A0
20 A1
21 A2
22 VSS
23 A3
24 A4
25 A5
26 A6
27 A7
28 A8
29 A9
30 A10
31 A11
32 A12
33 A13
34 A14
35 A15
36 A16
37 A17
38 A18
39 A19
40 IORD
41 IOWR
42 VCC
43 VSS
44 MEMRD
45 MEMWR
46 AEN
47 READY
48 IRQ
49 RESET
50 IRQ1
51 BCS
52 D0
53 D1
54 D2
55 D3
56 D4
57 D5
58 D6
59 D7
60 RXD
61 TXD
62 TXACT
63 VCC
64 VSS
65 TXDLY
66 X2
67 X1
68 MCS2
69 MD15
70 MD14
71 MD13
72 MD12
73 MD11
74 MD10
75 MD9
76 MD8
77 MA12
78 MA11
79 MA10
80 MA9
81 MA8
82 MA7
83 MA6
84 MA5

82C570 Pin Description

Pin No.	Pin Type	Symbol	Pin Description
PC Bus Interface			
19-21 23-39	I I	A0-2 A3-19	System Address bit 0 to 19. These bits are used to address the memory and I/O devices. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB).
40	I	$\overline{\text{IORD}}$	Active low I/O read strobe. It is used by the system CPU to read the 82C570 internal registers.
41	I	$\overline{\text{IOWR}}$	Active low I/O write strobe. It is used by the system CPU to load the information into the internal registers.
44	I	$\overline{\text{MEMRD}}$	Active low memory read strobe. When this signal is active, the display buffer is read.
45	I	$\overline{\text{MEMWR}}$	Active low memory write strobe. When active, the display buffer is written or the external microcode is being down-loaded.
46	I	AEN	Active high address enable for DMA transfers. When this line is active, DMA controller has the control of the bus. When it is low, $\overline{\text{IORD}}$ $\overline{\text{IOWR}}$ $\overline{\text{MEMRD}}$ $\overline{\text{MEMWR}}$ are enabled for 82C570.
47	T	READY	READY is a active high output signal to indicate to the host system that a data transfer will be completed. During I/O transfer, this signal will always be tri-stated. For memory read or write operation, READY will be deasserted for a period of 220 ns - 460 ns to inform the host to insert the wait state. READY has the tri-state buffer and requires external pull up resistor. It can drive the system bus directly.
48	T	$\overline{\text{IRQ}}$	Interrupt request signal. When $\overline{\text{IRQ}}$ is active, it will go low for 100 ns - 250 ns then return to tri-state. It is designed for the edge triggered interrupt system.
49	I	RESET	Active high hardware reset signal. When reset is active, it initializes the chip and the program counter of the micro-controller is reset to address 0.
50	T	$\overline{\text{IRQ1}}$	Level interrupt request signal. When a interrupt is initiated, $\overline{\text{IRQ1}}$ will be held active low untill it is acknowledged by the system interrupt service routine. It stays tri-stated when it is inactive.
51	O	$\overline{\text{BCS}}$	Active low external 74LS245 buffer enable signal. It goes active when the internal registers or the display buffer RAM are accessed. (Either read or write.)
52-59	B	D0-7	System data bit 0 to 7. These bits are used to transfer data to and from the CPU data bus. They are 3 state bidirectional lines.

82C570 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
Serial interface			
60	I	RXD	Receive input data. It is the serial biphase Manchester II encoded bit stream from the controller unit. RXD is connected to the TTL level output of the external differential receive amplifier.
61	O	TXD	Transmit data output. It is the biphase Manchester II encoded data output from the transmitter. An external line driver is required for cable interface.
62	O	TXACT	Active high transmit active signal. It goes high while the transmitter is transmitting.
65	O	TXDLY	Delayed transmit output data. It has a delay of 1/4 bit time from TXD. TXDLY is designed for an easy implementation of the cable waveform precompensation.
Buffer RAM interface			
7-3 84-77	O O	MA0-4 MA5-12	Memory address bit 0 to 12. These bits are used to address the RAM buffer. MA0 is the least significant bit and MA12 is the most significant bit.
18-11 76-69	B B	MD0-7 MD8-15	Memory data bit 0 to bit 15. They are 3 state lines used to transfer the data between RAM, 82C570, control units and system CPU. MD0 is the least significant bit and MD15 is the most significant bit.
8	O	$\overline{\text{RAMWR}}$	Active low memory write strobe signal. It is active when system CPU, control unit or 82C570 write the buffer RAM.
9	O	$\overline{\text{RAMRD}}$	Active low memory read strobe signal.
10	O	$\overline{\text{MCS1}}$	Active low memory selection 1. It is used to enable the first RAM.
68	O	$\overline{\text{MCS2}}$	Active low memory selection 2 used for the enabling of the second RAM.
Miscellaneous			
67,66	I/O	X1, X2	Crystal oscillator input. A fundamental frequency parallel resonant crystal should be connected to this pair. Alternatively, an external clock source may be connected to X1 input by floating X2. The clock frequency should be 18.8696 MHz with an accuracy of $\pm$ 0.01%.
1,42,63	I	VCC	5 Volt power supply.
2,22,43,64	I	VSS	Power supply ground.

Note: I = Input T = 3-state output
O = Output B = Bidirectional

82C570 Functional Description

The 82C570 block diagram is illustrated in Fig 1. The chip consists of the following functional blocks:

- Serial Interface Section
- Host System Interface Logic
- SRAM Control Block
- Microcontroller
- IRMA and IBM Adapter Interface

The internal microcode supports three operation modes:

- 3278/79 Display CUT mode (78E).
  Displays in CUT mode will have 4K display buffer storage and 4K Extented Attribute Buffer (EAB) storage. This will support all the terminal types except the 3279-S3G which needs 64K programmed symbol memory.
- 3287 Printer CUT mode (87E).
  Printer in CUT mode will use 4K or 8K (configurable) bytes of the buffer for information and message storage. The 82C570 will put all the information inside the buffer and generate an interrupt after receiving the START OPERATION command.
- Distributed Function Terminal mode (DFT).
  Displays and printers in DFT mode use 8K memory for input and output storage followed by a 128 bytes of memory for data communication. The 82C570 will put all the information inside the buffer and generate an interrupt after receiving the START OPERATION command.

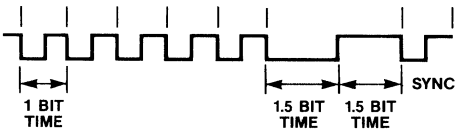
3270 Coaxial Type A Protocol Overview

The RG62AU coaxial cable is used to connect between control unit and device (terminal, printer, PC) with a maximum length of 1.5 meters. The data transmission is encoded by using the bi-phase Manchester II technique which has a fix bit rate of 2.3587 MHz.

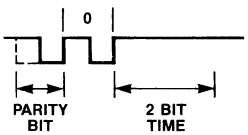
In the bi-phase Manchester II encoding, the 1st half of the bit cell consists of the complementary data and the 2nd half of the bit cell is the true data. There is always a central bit transition in the normal bit cell except in the transmission starting or ending sequence which have the code violations in the bit frame.

The transmission packet between the adapter and control unit is composed of the following: 1. Transmission Start Sequence (Code Violation Sequence). 2. One or more data frames. 3. Transmission Ending Sequence (Mini Code Violation Sequence).

At the beginning of the packet, five consecutive "1" bits followed by one and half bits high level and one and half bits low level will be transmitted by adapter or the control unit. This is called the Transmission Start Sequence. At the end of the packet, a Transmission Ending Sequence is sent to signify the the completion of the data frame. It consists of a "0" bit followed by two bits of high level without central bit transition. Fig 2 shows the Start and Ending Sequence.



(a) Transmission Start Sequence



(b) Transmission Ending Sequence

Figure 2. Transmission Start and Ending Sequence

The data frame is composed of 12 bits starting with "1" sync bit and ending with even frame parity bit. The frames have three formats: command word, data word and status word.

COMMAND WORD:

b1:	Sync Bit = 1.
b2-4:	Address Bits. Bits 2-4 = 0 for Base. Bits 2-4 = X for Feature.
b5-9:	Command ID.
b10:	Unused.
b11:	Command Bit = 1.
b12:	Frame Parity. Even parity for b1 through b11.

The command word is from control unit only. It can be read or write type. For the read type command, the chip responds with either data or status word. For a write type command, the chip responds with TT/AR (Transmit Turnaround/Auto Response). For any good command from the control unit, the chip will respond within 5μs after receiving the last bit of the ending sequence.

DATA WORD:

b1:	Sync Bit = 1.
b2-9:	Data Byte. Bit 2 is the most significant bit and bit 9 is the least significant bit.
b10:	Data byte parity. Odd parity for bit 2 through 9.
b11:	Data Bit = 0.
b12:	Frame parity. Even parity for b1 through b11.

The data word can be from control unit or the adapter. For control unit, it always follows the write command. For the adapter , it is the response of the read command.

STATUS WORD:

b1:	Sync Bit = 1.
b12:	Frame even parity.

For no keystroke returned:

TT/AR:	b2-11 = 0.
Poll request:	b6 = 1.
Operation complete:	b9 = 1.
POR complete:	b8 = 1, b10 = 1.
Feature error:	b11 = 1.

For keystroke returned:

b2-9:	Keyboard scan code.
b10:	1.
b11:	0.

The status word is returned from the chip in response to the Poll command from the control unit.

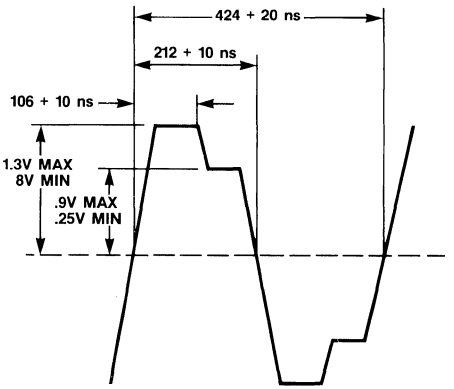
Serial Interface Section

The Serial Interface section consists of several signals that are used to connect the external analog circuit. The external transmission line driver (DP3487/MC3487) and receiver (DP3486/MC3486) and pulse transformer (PE85762) are used for the cable interface.

The TXACT goes active high while the transmitter is transmitting, it is used to enable the tri-state line driver. The transmit data (TXD) and transmit delay data (TXDLY) are also connected to the driver. The output of the driver feeds into the integrated pulse transformer which consists of the resistor and capacitor network and provides the proper signal level. The waveform at the coaxial cable is precompensated. The signals on the cable are polarized. The line receiver converts the differential cable signals (Minimum amplitude of 40mV and minimum pulse width of 185ns) to TTL level receive data RXD. Fig 3 shows the transmit and receive waveform.

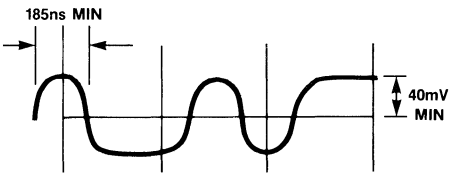
The transmitter logic includes transmit holding register, transmit shift register, parity generator, starting and ending sequence generators, Manchester encoder. The content of b11 of the transmit frame is controlled by the microcode. Bit 10 can be the data byte parity bit or programmed by the microcode.

The receiver consists of receive shift register, receive hold register, parity checker, starting and ending sequence detector, clock and data recovery circuit. The clock/data recovery circuit consists of a sophisticated 8X digital phase locked loop which can tolerate a maximum of $\pm$35ns data jitter. The reveive overrun, frame parity error and missing sync bit will cause the receive error state which disables the receiving and waits for the next starting sequence. Two receiver modes are supported: Mode 0 supports the 12 bits frame. Mode 1 supports both 8 bits (1st frame only) and 12 bits frame which may fit the 3299 multiplexor application.



ALL RISE AND FALL TIMES 30ns MAX.

(a) Transmit Waveform



(b) Receive Waveform

Figure 3. Cable Signals Waveforms

The chip has an on chip crystal oscillator. The 18.8696 MHz fundamental mode parallel resonant crystal is connected to pins X1 and X2. It requires two 20 pF capacitors to ground to prevent spurious oscillation. Alternatively, an external clock source may be connected to X1 input by floating pin X2. The 18.8696 MHz clock is used in receiver for data and clock recovery. It is divided down to generate the transmit clock for the frame encoding. It is also used in the microcontroller as the processor clock.

Host System Interface Section

The 82C570 provides a very simple method to interface with the IBM PC/XT , PC/AT and PS/2 model 30. Also together with the 82C574 microchannel interface chip, the 82C570 can support the PS/2 model 50, 60 and 80 easily.

The data bus is one byte wide to transfer the data between the host system and the I/O registers or the display memory. An external 74LS245 data beffer is recommended to use between the system data bus and D0-7. $\overline{BCS}$ is provided to turn on the buffer and the direction control is generated externally by NANDing the $\overline{MEMWR}$ and $\overline{IOWR}$ signals.

The system address bus is connected directly to the chip for the I/O and memory space decoding. The READY signal is used to control the display buffer read or write operations. Two interrupt request systems are supported: $\overline{IRQ}$ is used in the edge triggered system (IBM PC/XT/AT) and IRQ1 is used in the level interrupt system (PS/2 model 50,60,80).

The 82C570 supports both external and internal micro code operations by programming the 228H Operation Register. The detailed function of this register is described as follows:

228H Operation Register:

This register is used to control the operation of 82C570.

b7	Unused.
b6	Unused.
b5	Test 2. It is used for the chip testing purpose and should be held low in normal operation.
b4	Microcontroller Program Counter Reset Signal.
b3	Test 1. A bit to control the testing function. This bit should stay low in normal operation.
b2	External Microcode Download Control Signal.
b1	External Microcode Operation Mode.
b0	Software Reset.

All the bits are reset when RESET pin goes active. The external micro code is down-

loadable from floppy disk by executing the memory write operation with b2 (external microcode download control signal) and b1 (external microcode operation mode) high. After the completion of download process, b0 (Software Reset signal) should be turn on for a minimum period of 500 ns to initialize the chip again before doing other operation.

SRAM Control Block

The memory used by the 82C570 consists of 8K × 8 static RAMs with 120 ns access time. The Address (MA0-12), Data (MD0-7) Read/Write control (RAMRD, RAMWR), and memory chip enable signals (MCS1, MCS2) are all provided by 82C570.

If the user uses the internal microcode, only one 8K X 8 RAM is required (MCS1 is active). The lower half 4K is for data buffer and the higher half 4K is for the EAB buffer. The memory is dual ported between Host System (PC) and microcontroller. The arbitration logic is built on the chip with microcontroller having higher priority. When the Host accesses the memory, the memory Address MA0-12 are the same value as the Host Address A0-12. A12 controls the lower or higher half portion of the RAM. The READY signal controls the wait state and signifies the completion of the memory access.

If the external microcode is used, two 8K × 8 RAMs are required. MCS1 enables the first RAM and MCS2 enables the second RAM. The microcode can be downloaded from the floppy by enabling the MEMWR signal with the b1 and b2 on in register 228H. It can be read back for verification by enabling MEMRD with same b1 and b2 value. The microcode is relocated by the 82C570 with the 1st 4K of the microcode (A12 = 0) locating at the higer half of the first RAM (MCS1 active and MA12 = 1) and the 2nd 4K (A12 = 1) locating at the higher half of the second RAM (MCS2 active and MA12 = 1). To read or write the data/EAB buffer, the register 228H b1 should be high and b2 should stay low. The data buffer is located at the lower half of the first RAM (MCS1 active and MA12 = 0) with the Host address A12 = 0. The EAB buffer is located at the lower half of the second RAM (MCS2 active and MA12 = 0) with the Host address A12 = 1. The memory access is arbitrated between Host,microcontroller and microcode access. The microcontroller has the highest priority and the microcode access has the lowest priority.

Microcontroller Section

The 82C570 contains a very high speed microengine. The microcode is 16 bits wide and the data transfer between registers and memory is 8 bits wide. Each microcode command executes in 212ns except when executing from external microcode, and fetching or storing data memory in which case a microinstruction takes 414 ns.

The microcontroller is composed of an ALU, working registers (With general and special functions), zero flag, zero flag stack, program counter, program counter stack and two accumulators, two RAM address counters.

The microinstructions supportted by the microcontroller are listed as below:

- Immediate ALU Operation
- Source/Destination ALU Operation
- Conditional Branch
- Pulse Function
- Jump on Accumulator
- Return from Interrupt
- Long Jump

The detailed operation of each instruction is described in the different document: 82C570 Microcode Specification.

IRMA and IBM Adapter Interface

The 82C570 provides both IRMA and IBM adapter cards interface compatible registers. All the terminal emulation and file transfer application software written for these two boards can also run on the adapter cards using 82C570 chip.

IRMA Interface

There are 6 I/O addressible registers and 13 IRMA commands defined in this interface. To initiate a command, the host CPU puts the command codes in IRMA0 register and the associated arguments in IRMA1-3 registers. The command request flag is set by writing any data to I/O address 226H. During idle, the microcontroller keeps on polling this flag bit. Once the set flag is detected, it starts to execute the command and reset this command flag. After the command is processed, the microcontroller put the execution results and status back to the IRMA0-3 registers.

The description of the registers is listed as follows:

220H-223H IRMA0-IRMA3 registers. These four registers are the communication box between host system and control unit. They contain the command codes and the arguments after being written by the CPU. The command execution results and status are put back to these registers after the command processing.

226H Not defined. The command request flag is set by executing an I/O write to this address.

227H Status Flag register. When the CPU reads this register, b7 indicates the attention request flag and b6 indicates command request flag. b5-b0 are "0" and unused. The attention request flag is cleared by executing an I/O write to this address. It is set when the main status bits are changed from "0" to "1" with the attention mask bits set in the corresponding bits.

Main Status Register:

b7	Auxiliary Status change occured.
b6:	Trigger occured.
b5:	Key buffer empty.
b4:	Unused.
b3:	Reset command from control unit.
b2:	Unused.
b1:	Buffer modified. The buffer write commands set this bit.
b0:	Cursor address loaded.

Bits 7, 6, 3, 1, 0 can be cleared by PC using Clear Main Status Bits command.

Auxiliary Register:

b7:	Unused.
b6:	Unit Polled. This bit is set by a Poll command and reset after being read by the microcontroller.
b5:	Sound alarm.
b4:	Display inhibited.
b3:	Cursor inhibited.
b2:	Reverse cursor enabled.
b1:	Cursor blink enable.
b0:	Keyboard click enable.

B0 through B5 are set and reset by the control unit.

The IRMA commands supported by the internal microcode are listed as follows:

Code (b3-b0)	Command Definition
0	Read Buffer Data
1	Write Buffer Data
2	Read Status/Cursor Position
3	Clear Main Status Bits
4	Send Keystroke
5	Send Selector Pen Location
6	Execute Power-on-Reset
7	Load Trigger Data and Mask
8	Load Trigger Address
9	Load Attention Mask
A	Set Terminal Type
C	Read Terminal Information
E	Return revision ID and OEM number

Read Buffer Data:

For this command, IRMA0-3 registers contain the command code and the buffer address. The main status , buffer data and the corresponding EAB data are returned at the end of the execution.

Registers	Write	Read
IRMA0	Command 0	Main Status
IRMA1	ADDR (L)	X
IRMA2	ADDR (H)	EAB Data
IRMA3	X	Buffer Data

Write Buffer Data:

The operation of this command is similiar to Read Buffer Data command except that it executes the writing of buffer.

Registers	Write	Read
IRMA0	Command 1	Main Status
IRMA1	ADDR (L)	X
IRMA2	ADDR (H)	X
IRMA3	Data for Write	X

Read Status/Cursor Position:

This command reads the cursor address and the main/Aux status registers.

Register	Write	Read
IRMA0	Command 2	Main Status
IRMA1	X	Cursor Address Low
IRMA2	X	Cursor Address High
IRMA3	X	Aux Status

Clear Main Status Bits:

This command is used to clear the main status bits. Five bits (b7,6,3,1,0) can be reset by the PC. The status bits are cleared if the corresponding clear mask bits are "1". The returned status bits are the status after the command has been executed.

Register	Write	Read
IRMA0	Command 3	Main Status
IRMA1	X	X
IRMA2	X	X
IRMA3	Bits Clear Mask	X

Send Keystroke Command:

This command causes the chip to send a key scan code to the control unit. It resets bit 5 (Key buffer empty) of the main status register to "0".

Register	Write	Read
IRMA0	Command 4	Main Status
IRMA1	X	X
IRMA2	X	X
IRMA3	Key Scan Code	X

Send Selector Pen Location:

This command causes the light pen position to be sent to the control unit.

Register	Write	Read
IRMA0	Command 5	Main Status
IRMA1	Row on Screen	X
IRMA2	Field ID on Screen	X
IRMA3	X	X

Execute Power on Reset:

This command causes the chip appears to the control unit that it has been reset.

Register	Write	Read
IRMA0	Command 6	Main Status
IRMA1	X	X
IRMA2	X	X
IRMA3	X	X

Load Trigger Data and Mask:

This command loads the trigger data and trigger mask registers. The trigger occurred bit will be set if the the buffer address matches the trigger address and the buffer data bits match the corresponding trigger data bits. (Only the bits with the value of "1" in the mask register are compared.)

Register	Write	Read
IRMA0	Command 7	Main Status
IRMA1	Data Pattern	X
IRMA2	Mask Pattern	X
IRMA3	X	X

Load Trigger Address:

This command sets the buffer position for the data/mask comparison. The trigger occured bit should be reset by this command.

Register	Write	Read
IRMA0	Command 8	Main Status
IRMA1	ADDR (L)	X
IRMA2	ADDR (H)	X
IRMA3	X	X

Load Attention Mask:

This command loads the attention mask register. Whenever the main status bits change from "0" to "1", the Attention Request flag is set if the corresponding attention mask register bits are set to "1".

Register	Write	Read
IRMA0	Command 9	Main Status
IRMA1	X	X
IRMA2	X	X
IRMA3	Mask Pattern	X

Set Terminal Type:

This command is used to set the terminal type. If a new type is assigned, the POR status is issued and the new terminal type is stored, otherwise no action is taken.

Register	Write	Read
IRMA0	Command A	Main Status
IRMA1	X	X
IRMA2	X	X
IRMA3	New Terminal ID	X

Read Terminal Information:

This command is used to get the terminal conditions.

Register	Write	Read
IRMA0	Command C	Main Status
IRMA1	X	Starting EAB Page Number
IRMA2	X	Starting Internal Variable Page Number
IRMA3		Current Terminal Type

Return Revision ID and OEM Number:

A unique number is assgned for the application.

Register	WriteRead	
IRMA0	Command E	Main Status
IRMA1	X	Low 2 BCD digits of Revision Number
IRMA2	X	High 2 BCD digits of Revision Number
IRMA3	X	OEM Number

IBM Interface

For IBM application software interface, the 82C570 provides 11 registers with I/O mapped addresses from 2D0-2DA for the communication between host CPU and the control unit.

Table 1

I/O Address	Registers	POR contents 7	6	5	4	3	2	1	0	PC Read	PC Write
02D0	PC Adapter Interrupt Status	0	0	X	1	X	X	X	X	Data	Reset Mask
02D1	Visual/Sound	X	0	Z	Z	Z	Z	Z	Z	Data	Reset Alarm
02D2	Cursor Address Low	X	X	X	Z	Z	Z	Z	Z	Data	
02D3	Cursor Address High	Z	E	Z	E	Z	Z	Z	Z	Data	
02D4	PC Adapter Control	1	0	0	Z	Z	0	0	0	Data	Data
02D5	Scan Code	X	X	X	X	X	X	X	X		Data
02D6	Terminal ID	X	X	X	X	X	X	X	X		Data
02D7	Segment	1	1	0	0	1	1	1	0	Data	Data
02D8	Page Change Low	X	X	X	X	X	X	X	X	Data	Reset Mask
02D9	Page Change High	X	X	X	X	X	X	X	X	Data	Reset Mask
02DA	87E Status	X	X	X	X	X	X	X	X	Data	Reset Mask

Note: 0 - hardware reset
1 - hardware set
Z - internal microcode reset
E - internal microcode set
X - Undetermined

PC Adapter Interrupt Status Register:

b0	Keystroke Accepted (78E mode) Start Operation Command (DFT and 87E modes). In 78E mode, this bit is set by the chip when a keystroke is acknowledged by the control unit and reset by PC. In 87E and DFT modes, this bit is set by the chip when a Start Operation command is decoded and reset by PC.
b1	Reset Command (All modes). This bit is set when a Reset command is decoded and reset by PC.
b2	In 78E mode, this bit represents "Visual/Sound Registers Updated". It is set when the Load Control Register command is decoded or when the sound alarm enable/disable clicker has been decoded in a Poll command. In 87E mode, this bit is set when the enable/disable operation has been decoded in a Poll command. In DFT mode, the decoding of the Diagnostic Reset command sets this bit.
b3	Read Terminal ID Command. This bit is used in DFT mode only. The decoding of the Read Terminal ID command sets this bit.
b4	Base Buffer Modified Complete. This bit is used in 78E mode. It is set at the termination of a Write Data, Clear and Insert commands.
b5	Load I/O Address Command. This bit is set when the the Load I/O Address High or Low commands are reveived in the 78E mode. When set, it will generate the interrupt to the PC if the mask bit is off and bit 3 (Inhibit cursor bit) of the Visual/Sound register is off if the conditional inhibit disable bit (Bit 6 in the PC adapter register) is set.
b6	Buffer Being Modified. This bit is used in 78E mode only. It is set at the beginning of the Write Data, Clear and Insert command. It is reset at the end of the command when Base Buffer Modified Complete bit is set.
b7	Interrupt Generated. This bit is set when one of the interrupt status bits b0-b5 is on and the interrupt mask bit is off. It is reset by the PC when it resets the interrupt bits or when the mask bit is on.

Visual/Sound Register:

b0	Characters per line. 132 characters per line if this bit is "1". 80 characters per line for "0".
b1	Inhibit feature step of the buffer address counter.
b2	Inhibit display.
b3	Inhibit cursor.
b4	Reverse cursor.
b5	Blink cursor.
b6	Sound alarm.
b7	Click enable.

This register is set and reset by the control unit except b6 which is reset by the Host by writing anything to this register. The loading of this register causes b2 (Visual/Sound Updated bit) of the PC Adapter Interrupt Status register to be set.

Cursor Address Low Register:

This register is readable only. It contains the value of low byte buffer address counter.

Cursor Address High Register:

Similiar to Cursor Address Low register, the register is readable only and contains the value of high byte buffer address counter.

PC Adapter Control Register:

This register can be read and written by PC.

b0	Coaxial Cable Enable. It is set (Enabled) by the PC and reset by PC or Reset signal. The writing of 220H register will also set this bit. When it is reset, the chip is disabled and unable to respond to the control unit. POR response will be returned for the first Poll command after the coaxial cable is enabled.
b1	78E, 87E/DFT mode. If "1", the chip operates in DFT mode. If "0", it operates in 78E or 87E mode.
b2	87E/78E mode. The chip is configurated as 87E mode if b1 = "0" and b2 = "1". It is configurated as 78E mode if b2 = "0" and b1 = "0".
b3	Keystroke Available. This bit is used in 78E mode only. When set ,it indicates that the scan code has been loaded by PC. It is reset by the Poll Acknowledge and Reset commands.
b4	Request Poll. When set by the PC, it causes the poll request bit to be returned for the next poll response. It is reset by the Poll Acknowledge command. This bit is used in 87E and DFT modes only.
b5	Test bit. The test function is not implemented by the internal microcode.
b6	"Reset Cursor" for 87E mode. It resets the buffer address counter to 0 when it is active. "Conditional Interrupt Disable" for 78E mode. When this bit is set, the decoding of Load I/O Address command interrupts are disabled if bit 3 (inhibit cursor bit) of the Visual/Sound register is set.
b7	Disable Interrupts. This bit is set when Reset signal is active. It can be set and reset by PC. When active, it inhibits all interrupts (B0 to B5 in the PC Adapter Interrupt Status register) to the PC. The interrupt status bits can be set even with this mask bit on.

Scan Code Register:

This register holds the keystroke code to be sent to the control unit. This register should not be changed if bit 3 of the PC-Adapter Control register (keystroke abailable bit) is set. The contents sent to the control unit is the one's complement value of this register.

Terminal ID Register:

This register represents the terminal ID. It is programmed by the Host before enabling the coaxial cable. The content of the data sent to the control unit is the one's complement of this register.

For DFT and 87E modes: "01" H should be programmed. For 78E mode:

bit 4-7 Keyboard ID.
bit 1-3 3278/3279 Models.
010 for model 2
011 for model 3
111 for model 4
110 for model 5

Segment Register:

Bit 0 of this register controls the enabling of the buffer memory access. A "0" allows the memory read/write. The memory access is prohibited if this bit is "1".

Bit 1 to 7 of the Segment Register is written by PC for the desired memory block address. It is used for the memory relocation. Bit 1 to 7 are compared with PC address bit 13 to 19. Only a match in the comparison will enable the memory access. The Reset default value of the register is "CE".

Page Change Low Register:

This register indicates the change of each 256 bytes of the lower 2K buffer space. During the write command from the control unit, the bit will be set if any modification of the corresponding 256 byte page buffer happens. The bit gets reset when the Host (PC) writes to this register and the corresponding data bus bit is "1".

The buffer locations that correspond to each bit are listed as follows:

bit	buffer locations
0	0 - 255
1	256 - 511
2	512 - 767
3	768 - 1023
4	1024 - 1279
5	1280 - 1535
6	1536 - 1791
7	1792 - 2047

Page Change High Register:

Similiar to Page Change Low Register, this register indicates the change of each 256 bytes of the higher 2K buffer space. The bits are set and reset the same way as Page Change Low Register.

The following table shows the buffer locations corresponding to each data bus bit:

bit	buffer locations
0	2048 - 2303
1	2304 - 2559
2	2560 - 2815
3	2816 - 3071
4	3072 - 3327
5	3328 - 3583
6	3584 - 3839
7	3840 - 4095

87E Status Register:

This register is dedicated for 87E mode operation only. Bits are set by the control unit and reset under mask by PC.

b0-4	Unused.
b5	87E sound alarm. It is set by the Poll command.
b6	Disable operation. This bit is set by Poll or Poll Acknowledge command.
b7	Enable operation. Set by Start Operation, Poll or Poll Acknowledge commands.

Features and Commands Supported by Internal Microcode

Base Feature

The 82C570 internal microcode supports most of the base feature commands. Table 2 lists all the commands supported. The description of the commands is as follows:

Poll:

This command doesn't use the address portion of the command word. The functions of the frame bit 2 and bit 3 are assigned as follows:

b2	b3	78E mode function	87E mode function
1	1	Enable keyboard clicker.	Enable operation.
0	1	Disable keyboard clicker.	Disable operation.
1	0	Sound alarm.	Sound alarm.
0	0	None of the above.	None of the above.

The following status frames are returned to the control unit in response to the Poll command:

Response	Frame Bits 2	3	4	5	6	7	8	9	10	11
POR complete	0	0	0	0	0	0	1	0	1	0
TT/AR	0	0	0	0	0	0	0	0	0	0
Keystroke available	2-9 Scan Code								1	0
Base status	0	0	0	0	x	0	0	x	0	x

The base status bit 6 is set for poll request (For DFT and 87E modes only). Bit 9 is active if the operation is complete. The feature error will set bit 11. The priority of the multiple poll responses is listed as below:

1. Feature error. 2. POR complete. 3. Poll request. 4. Operation complete. 5. Keystroke available. 6. Any other feature status.

Reset:

The decoding of this command sets bit 1 (Reset command decoded bit) of the PC Adapter Interrupt Status register. Both data and EAB buffers will not be cleared. The buffer address counter is set to "0050H" for 78E and DFT modes, and "0000" for 87E mode. TT/AR is returned to the control unit. The chip can accept two or more Reset command (Without intervening Poll commands) and responds with a single POR response to a subsequent Poll.

Read Data:

The return of this command is the data at the location of current buffer address counter. The address counter is incremented by one at the completion of the command.

Load Address Counter High:

The decoding of this command causes the chip to load the next data frame into the high byte of the buffer address counter. In 78E mode, it sets the bit 5 of the PC-Adapter Interrupt Status.

Read Address Counter High:

The 82C570 responds to this command by sending the content of the high byte buffer address counter. It is supported in both 78E and 87E modes only.

Clear:

This command clears all or part of the data buffer to null (0). The clear operation terminates at the location where the data value matches with the pattern byte (The data frame that follows the command) in conjunction with the Mask Register, or terminates at address 0 if no match has been found. All the locations from the starting address up to the matched location (Not included) are cleared. The address counter contains the matching location address. The corresponding locations of the EAB are also cleared to nulls under the control of the EAB Mask register.

In 78E mode, bit 6 (Buffer being modified) of the PC Adapter Interrupt Stsatus register is set at the beginning the command. At the completion of the command, this bit is reset and bit 4 (Base buffer modified complete) of the register is set.

Start Operation:

This command is supported in both DFT and 87E modes. In DFT mode, TT/AR is returned , bit 0 (Start Operation command) of the Adapter Interrupt Status register is set at the decoding of the command. For 87E mode, the response is same except that no action is taken if there is any pending status. Bit 7 (Enable operation) of the 87E Status register is also set in this mode.

Read Terminal ID:

The response of this command is the return of the following data byte:

78E mode:	b2-5	Keyboard ID.
	b6-8	Terminal ID.
	b9	0
87E mode:	b2-8	0
	b9	1
DFT mode:	b2-8	0
	b9	1

In DFT mode, the decoding of this command sets bit 3 (Read Terminal ID command) of the PC Adapter Interrupt Status register. In 87E and 78E modes, it reset bit 9 and bit 11 (operation complete and feature error) of the status word.

Load Control Register:

This commands loads the next data frame into the Visual/Sound Register (2D1) or IRMA Auxiliary Register.

The function of each bit is listed as follows:

Frame Bits	Function
2	80 characters per line if this bit is "0". 132 characters if "1".
5	Inhibit feature step of the buffer address counter.
6	Inhibit display.
7	Inhibit cursor display.
8	Reverse image cursor.
9	Cursor blinking.

In 78E mode, bit 2 of the PC Adapter Interrupt Status (Visual/Sound Register Updated) will be set to "1" at the completion of this command.

Read Multiple:

The Read Multiple will cause the chip to return one or more data words from buffer memory beginning at the current buffer address counter. The counter increments by one each time the buffer is accessed. The maximum number the chip can read depends on the Secondary Control Register bit 0. If this bit is "0", the read will terminate when the two low order bits of the buffer address counter becomes "00" which gives a maximum of 4 bytes of reading data. If it is "1", the read will terminate when the five low order bits of the counter becomes "00000" and give a maximum of 32 bytes of data.

Write Data:

The decoding of the Write Data command will cause the chip to put all the following data frames into the buffer memory untill another command is received. The buffer address counter increments by one for every data written. In 78E mode, the 1st data word following the command sets bit 6 (Buffer being modified) of the PC Adapter Interrupt Status register. At the completion of the command, bit 4 of the register (Base buffer modified complete) is set.

Read Status:

In 78E and 87E modes, the return of this command is as follows:

Frame bit 1:	Sync bit
bit 2-3:	0
bit 4:	"1" for not busy
bit 5-6:	0
bit 7:	"1" for feature error
bit 8:	"1" for operation complete
bit 9-11:	0
bit 12:	Frame parity

Insert:

This command causes the chip to accept the following data frame and put it in the buffer storage at the current address counter location. The old starage data is shifted one location ahead. This process continues for each successive location untill a null (00) character or attribute is found, or the address counter steps to zero.

The EAB (Extented attribute buffer) is also shifted with the contents of the EAB Mask register being inserted at the initial location.

In 78E mode, bit 6 of the PC Adapter Interrupt Status Register (Buffer being modified) is asserted at the beginning of command. At the completion of the command, this bit is deasserted and bit 4 (base buffer modified complete) is set.

Search Forward:

This command is supported in 78E and 87E modes only. The command causes the chip to search for each buffer storage starting with the current address counter. This process will keep on going untill a match in the pattern byte (The data frame that follows the command). The bit comparison happens only on the bit with corresponding mask bit equal to "1". The address counter increments by one after each comparison. The address counter contains the value of the buffer address of the first matched data. The search will terminate at address 0 if no match is found.

Poll Acknowledge:

This command is sent by the control unit when it receives the non-zero status. TT/AR is returned by the chip after receiving this command. If the chip receives a second Poll command instead of Poll Acknowledge, it will return the same status. In the case taht a new status is available before the first returned status is acknowledged, the new status will be stacked by the chip.

In 78E mode, if the sending of the keystroke is acknowledged by the control unit, the receiving of this command will set bit 0 (Keystroke Accepted) of the Interrupt Status register.

If this command contains the sound alarm or enable/disable clicker in 78E mode or enable/disable operation in 87E mode , it will set bit 2 (Visual/Sound Register Updated) of the Interrupt Status register.

Search Backward:

The operation of Search Backward command is similiar to Search Forward command except that the address counter decrements by one after each comparison. If no byte match is found the search will terminate at one location past address 0. (Address counter bits 0 to 11 are set to "1").

Load Address Low:

Similiar to Load Address High command, this command causes the chip to load the next data frame into the low byte of the buffer address counter. In 78E mode, the decoding of the command sets bit 5 of the PC-Adapter Interrupt Status register.

Read Address Low:

Similiar to Read Address High commnad, the content of buffer address low counter is returned in response to this command.

It is ignored in DFT mode.

Load Mask:

This command causes the chip to load the next byte into the mask register. The mask register is used with Search and Clear commands. A "1" bit in the mask enables the bit in the buffer to compare with the pattern byte. Load Mask command is spported in 78E and 87E modes only.

Load Secondary Control Register:

The decoding of this command interprets the data byte following the command as the control bit for the Read Multiple command. If b0 is "0", the termination of Read Multiple command will be 0 to 4 bytes. If it is "1", the termination will be 0 to 32 bytes.

Diagnostic Reset:

This command is supported in DFT mode only. It is ignored in both 78E and 87E modes. In DFT mode, the response of this command will be the return of TT/AR and the setting of bit 2 in PC Adapter Interrupt Status register.

Table 2

Command Name	Command Code B5-B9	R/W	CUT Mode Display	CUT Mode Printer	DFT
Poll	00001	R	Y	Y	Y
Reset	00010	W	Y	Y	Y
Read Data	00011	R	Y	Y	Y
Load Address Counter High	00100	W	Y	Y	Y
Read Address Counter High	00101	R	Y	Y	N
Clear	00110	W	Y	Y	N
Start Operation	01000	W	N	Y	Y
Read Terminal ID	01001	R	Y	Y	Y
Load Control Register	01010	W	Y	N	N
Read Multiple	01011	R	Y	N	Y
Write Data	01100	W	Y	Y	Y
Read Status	01101	R	Y	Y	N
Insert	01110	W	Y	N	N
Search Forward	10000	W	Y	Y	N
Poll Acknowledge	10001	R	Y	Y	Y
Search Backward	10010	W	Y	Y	N
Load Address Counter Low	10100	W	Y	Y	Y
Read Address Counter Low	10101	W	Y	Y	N
Load Mask	10110	W	Y	Y	N
Load Secondary Control Register	11010	W	Y	N	Y
Diagnostic Reset	11100	W	N	N	Y

Selector Pen Feature:

Table 3 lists the selector pen feature supported by 82C570 internal microcode. The explanation of each command is as follows:

POLL: The status response is the same as in the base feature.

READ ROW COUNT: The response of this command will send the row count indicating the display row detected.

READ FEATURE ID: 25H will be returned as the feature ID.

Table 3

Command Name	Command Code b6-b9	R/W	CUT Mode Display	CUT Mode Printer	DFT
Poll	0001	R	Y	N	N
Read Row Count	0011	R	Y	N	N
Read Feature ID	01X1	R	Y	N	N
Read Selector Pen Field Count	1111	R	Y	N	N

Extended Character Set Feature:

Table 4 lists the extended character set feature supported by 82C570 internal microcode. The description of each command is as follows:

Read Data:

The operation of this command is similiar to base Read Data command except that the buffer address counter is incremented after the data reading only when bit 1 = "0" (Inhibit Feature Step of I/O Address Counter) in the Visual/Sound Register.

Read Feature ID:

"79"H is returned which means color and no program symbol is supported.

Read Multiple:

If bit 5 of the Control Register is "1", TT/AR is returned and no other action is taken. If this bit is "0", the operation is similiar to base Read Multiple command.

Write Alternate:

The data bytes following the command are writen into the display data buffer and the EAB buffer alternately, starting with the data buffer. The writing of EAB buffer is "under mask" just like the Write Under Mask command. The address counter will increment by one after the byte is writen into EAB if bit 1 of the Visual/Sound Register is "0".

Load EAB Mask:

This command stores the following data byte into the EAB Mask Register (One of the 15 working registers in the microcontroller). It is used in the base Clear command, feature Write Under Mask and Write Alternate commands.

Write Under Mask:

The operation of this command is "NEW EAB = (NOT (MASK) AND (OLD EAB)) OR (DATA BYTE))". A "1" bit in the data byte (The data frame that follows the command) always sets the corresponding EAB bit. The New EAB bit will be "0" only under two conditions: 1) Mask bit = "1" and the corresponding data bit is "0". 2) Mask bit = "0", Old EAB bit is "0" and the corresponding data bit is "0". At the completion of the writing, the buffer address counter will increment by one if bit 1 of the Visual/Sound Register is "0".

Read Status:
"20"H is returned for the decoding of this command.

Table 4

Command Name	Command Code b6-b9	R/W	CUT Mode Display	CUT Mode Printer	DFT
Read Data	0011	R	Y	N	N
Load EAB Mask	0101	W	Y	N	N
Read Feature ID	01X1	R	Y	N	N
Write Alternate	1010	W	Y	N	N
Read Multiple	1011	R	Y	N	N
Write Under Mask	1100	W	Y	N	N
Read Status	1101	R	Y	N	N

82C570 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C570 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C570 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Power Supply Current	I_{CC}		50	mA
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input High Voltage (except X1)	V_{IH}	2.0	V_{CC}+0.5	V
Input High Voltage for X1	V_{IH}	3.5	V_{CC}+0.5	V
Output Low Voltage (note 1)	V_{OL}		0.4	V
Output High Voltage (note 1)	V_{OH}	2.4		V
Input Leakage Current For V_{IN} = 0 to V_{CC}	I_{IL}	-10	10	μA
Output Tri-State Leakage Current For V_O = 0 to V_{CC}	I_{OL}	-10	10	μA

Note 1: I_{OL} = 12mA I_{OH} = -4mA for pins IRQ READY.
I_{OL} = 24mA I_{OH} = -4mA for IRQ1 pin.
I_{OL} = 4mA I_{OH} = -2mA for all other pins.

Capacitance (T_A = 25°C, V_{CC} = 0)

Parameter	Symbol	Min.	Max.	Units
Input Capacitance For F_C = 1 MHz	C_{IN}		10	pF
Output Capacitance	C_{OUT}		20	pF
I/O Capacitance	$C_{I/O}$		20	pF

82C570 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 60 pF for all the outputs)

Sym	Parameter	Min	Max	Units
Processor Interface Timing				
t1	Address Set-Up to Command Active	25		ns
t2	AEN Set-Up to Command Active	25		ns
t3	AEN Hold from Command Inactive	0		ns
t4	Address Hold from Command Active	10		ns
t5	I/O Command Pulse Width	100		ns
t6	Data Read Delay time		80	ns
t7	Data Hold from $\overline{\text{IORD}}$ Inactive	8		ns
t8	$\overline{\text{BCS}}$ Asserts Delay time		30	ns
t9	$\overline{\text{BCS}}$ Deasserts Delay time	10	30	ns
t10	Data Set-Up to $\overline{\text{IOWR}}$ Inactive	50		ns
t11	Data Hold from $\overline{\text{IOWR}}$ Inactive	0		ns
t12	READY Asserts Delay from $\overline{\text{MEMRD}}$/$\overline{\text{MEMWR}}$ Active	220	460	ns
t13	Data Valid before Ready Asserts	80		ns
t14	Data Hold from $\overline{\text{MEMRD}}$ Inactive	10		ns
t15	READY Deasserts Delay from $\overline{\text{MEMRD}}$/$\overline{\text{MEMWR}}$ Active		30	ns
t16	READY Tri-state Delay from $\overline{\text{MEMRD}}$/$\overline{\text{MEMWR}}$ Inactive		30	ns
t17	Data Set-Up to READY Active	80		ns
t18	Data Hold from $\overline{\text{MEMWR}}$ Inactive	0		ns
Buffer RAM Interface timing				
t21	RAM Write cycle time	135		ns
t22	RAM Write cycle Address Hold from $\overline{\text{MCS1}}$/$\overline{\text{MCS2}}$ Inactive	10		ns
t23	RAM Write cycle Address Hold from $\overline{\text{RAMWR}}$ Inactive	10		ns
t24	$\overline{\text{RAMWR}}$ Pulse Width	85		ns
t25	Address Valid to $\overline{\text{RAMWR}}$ Active	20		ns
t26	Data Valid to End of Write	60		ns
t27	Data Hold from End of Write	5		ns

82C570 AC Characteristics (Continued)
(T_D = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 60 pF for all the outputs)

Sym	Parameter	Min	Max	Units
Buffer RAM Interface timing (Continued)				
t28	$\overline{MCS1}$/$\overline{MCS2}$ Active to End of Write	120		ns
t29	Address Valid to End of Write	120		ns
t30	RAM Read cycle time	135		ns
t31	Address Access time		120	ns
t32	Data Valid from $\overline{MCS1}$/$\overline{MCS2}$ Active		120	ns
t33	Data Valid from $\overline{RAMRD}$ Active		120	ns
t34	Output Hold from Address changes	0		ns
Serial interface timing				
t41	TXDLY Delay time from TXD	100	110	ns
t42	Transmit Data bit cell time	423.92	424.0048	ns
t43	Transmit Data half bit cell time	209	215	ns
t44	TXD first high going Delay from TXACT Active	205	220	ns
t45	Maximum Receive Input Data Jitter DPLL can tolerate		±35	ns
Miscellaneous timing				
t51	X1 Rise time		5	ns
t52	X1 Fall time		5	ns
t53	X1 High time	20	30	ns
t54	X1 Low time	20	30	ns
t55	X1 Cycle time	52.9899	53.0005	ns
t56	RESET Active time	1		μs
t57	$\overline{IRQ}$ Pulse Width	100	250	ns
t58	$\overline{IRQ1}$ Deasserts from $\overline{IOWR}$ Inactive		60	ns

Notes: AC measurements are done at: TTL output: High level = 2.0 V Low level = 0.8 V. Input swing is at least 0.4 V to 2.4 V with 3-10 ns rise and fall times.
High time is measured at 3.0V
Low time is measured at 0.6V

Crystal Specification

The crystal required in the X1, X2 inputs should meet the following requirements.

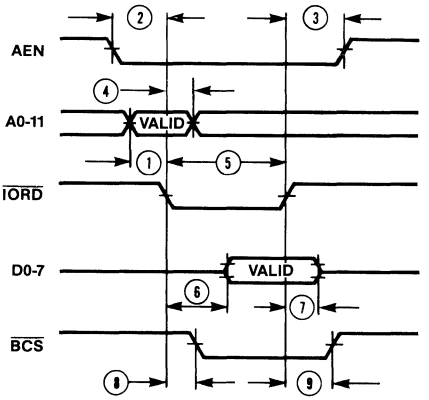
Resonant Frequency
(CL = 20 pF)..... 18.8696 MHz
Type ..... Fundamental Mode
Circuit.....Parallel Resonance
Load Capacitance (CL)..... 20 pF
Shunt Capacitance (CO) ..... 7 pF Max.
Equivalent
Series Resistance (R1) .....25 Ohm Max.
Motional Capacitance (C1) ... 0.02 pF Max.
Drive Level ..... 2 mW
Accuracy .. at 18.8696MHz ±0.002% at 25°C
..... at 18.8696MHz ±0.005%
for 0-70°C

Also, instead of the crystal at the X1, X2 inputs, an alternate TTL input may be connected at X1 input and floating X2.

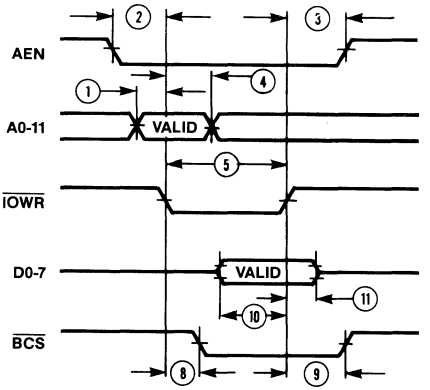
82C570 Timing Diagrams

Processor Interface Timing

I/O Read

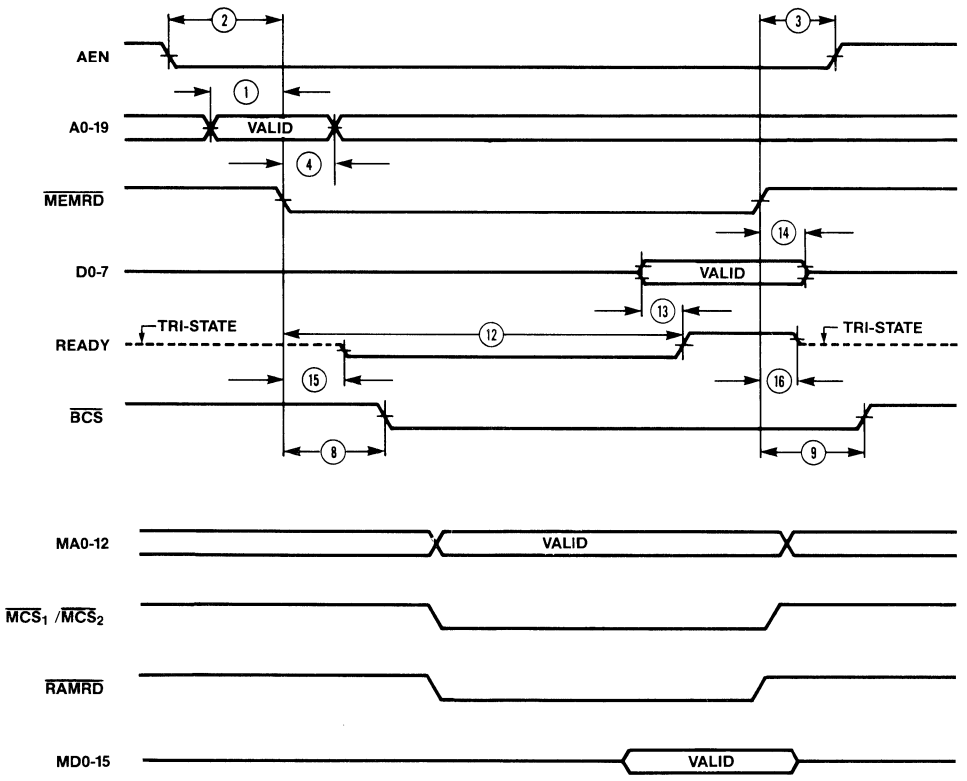


I/O Write



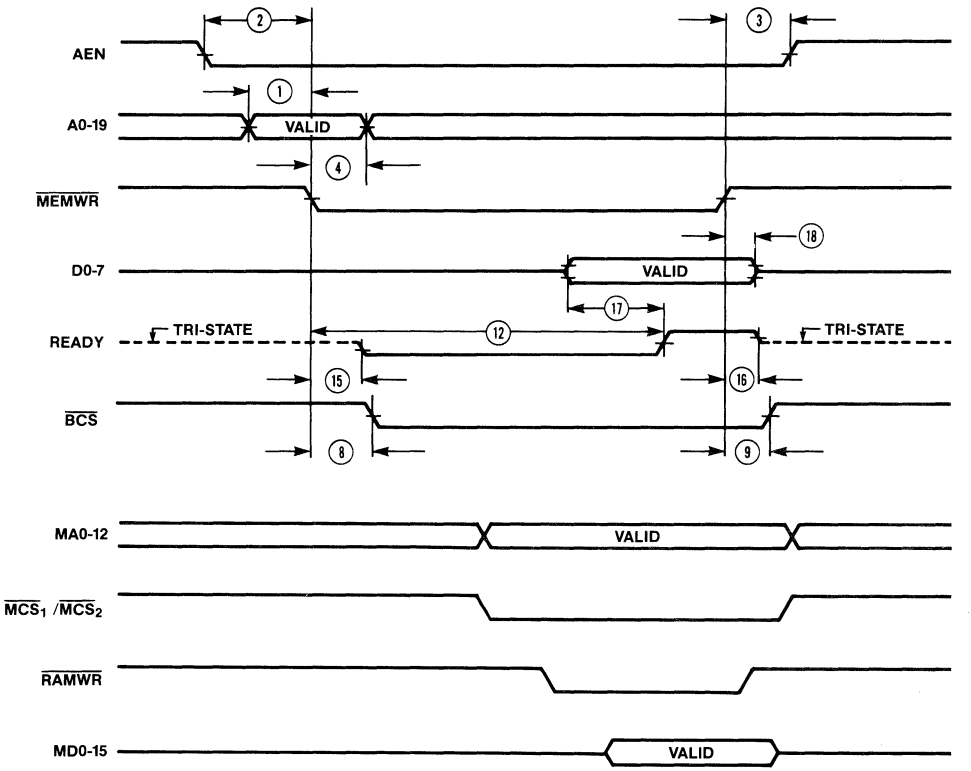
82C570 Timing Diagrams (Continued)

Memory Read



82C570 Timing Diagrams (Continued)

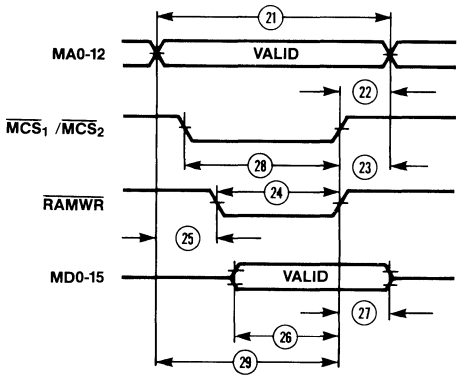
Memory Write



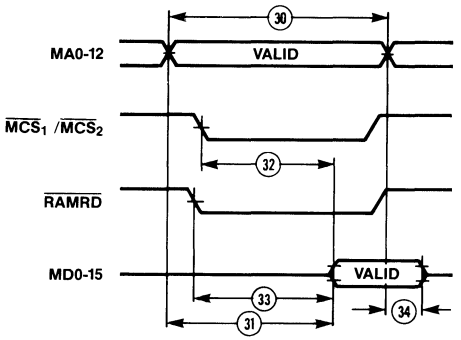
82C570 Timing Diagrams (Continued)

Buffer RAM Interface Timing

Write Cycle



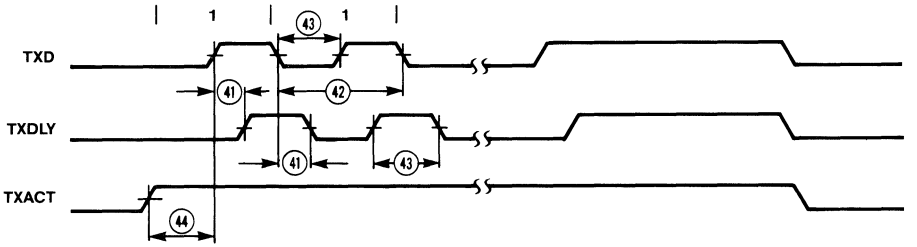
Read Cycle

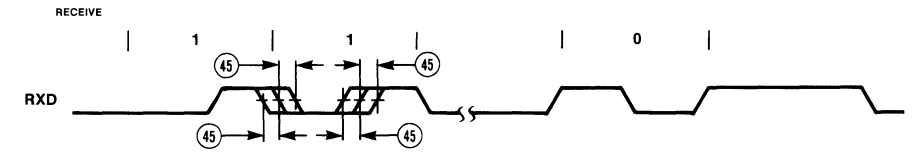


82C570 Timing Diagrams (Continued)

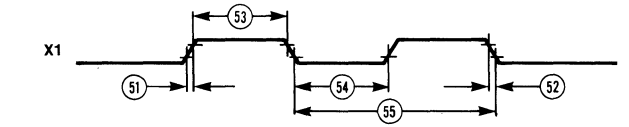
Serial Interface Timing

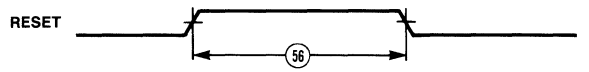
Transmit

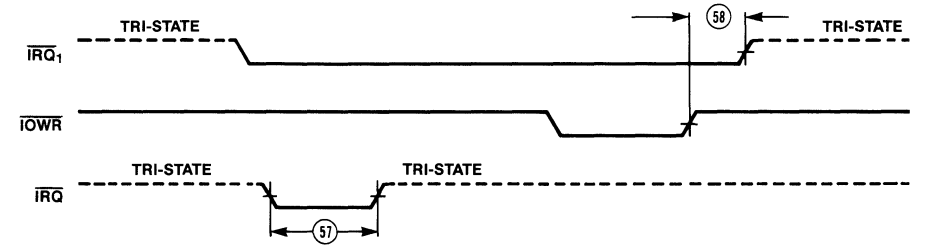




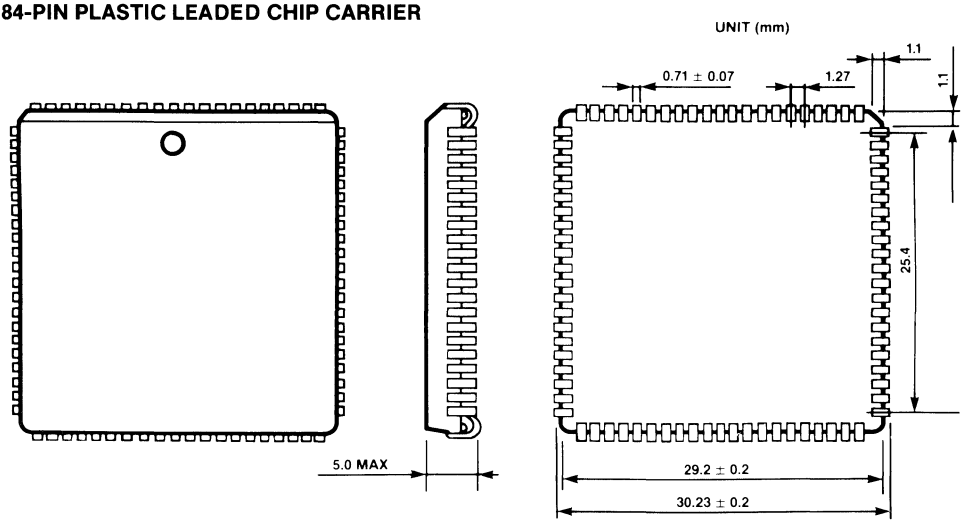
Miscellaneous Timing







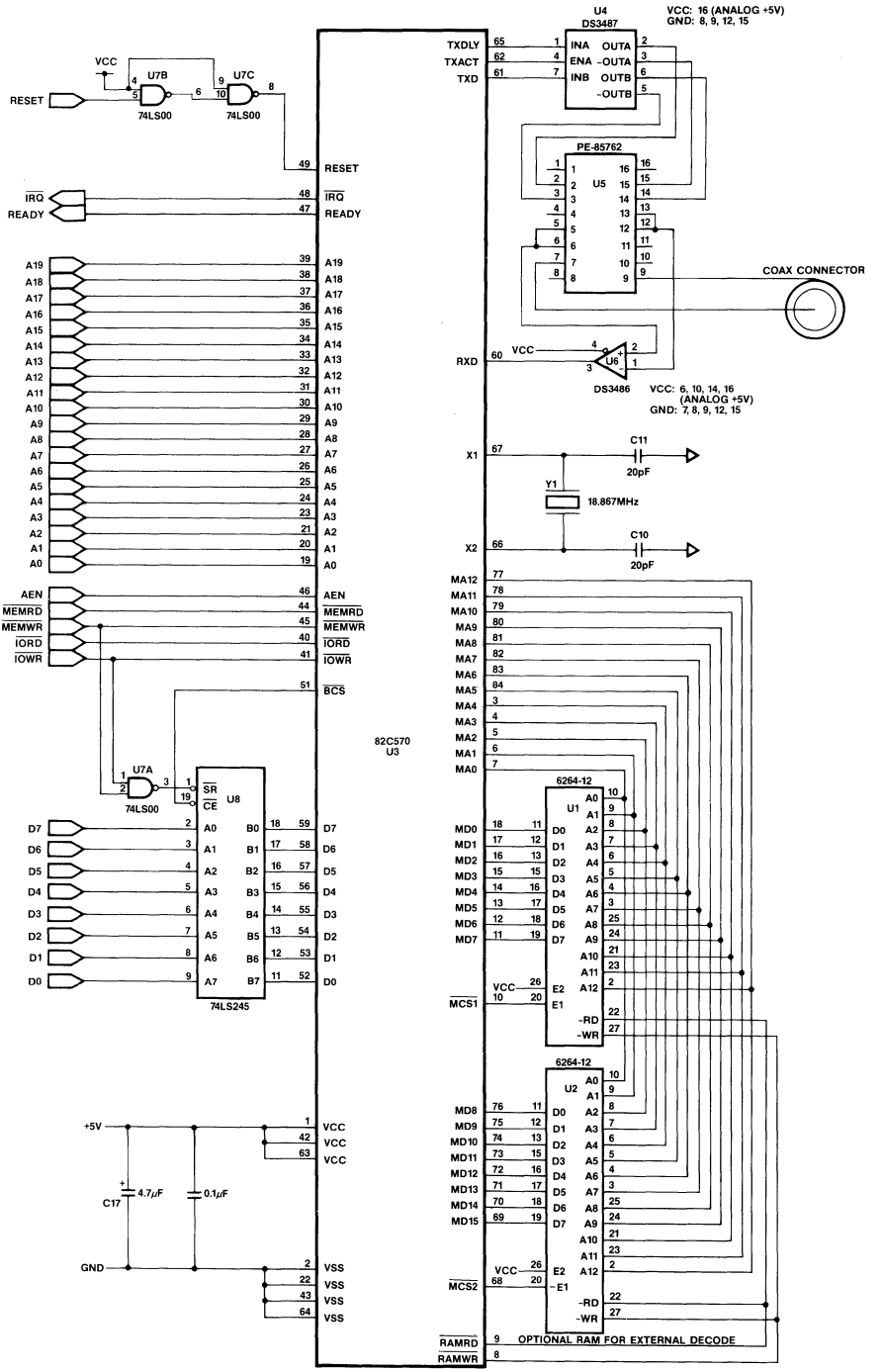
84-PIN PLASTIC LEADED CHIP CARRIER



Ordering Information

Order Number	Package Type
P82C570	PLCC-84

Note:
1. PLCC = Plastic Leaded Chip Carrier



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