82C301, 82C302, 82A303, 82A304, 82A305, 82A306
CS8230: AT/386 CHIPSet™

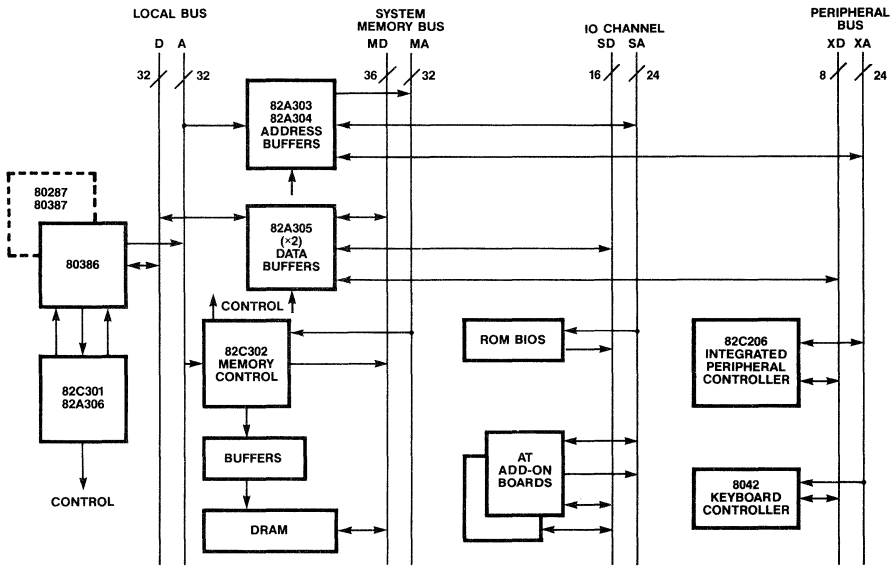
- **100% IBM™ PC AT compatible**
- **Flexible architecture allows usage in any iAPX 386™ design**
- **Operates in Page mode with Interleave memory subsystem**
- **16 MHz zero wait operation**
- **Independent clock to support correct AT bus timing**
- **1MB to 16MB of DRAM memory support**
- **A complete PC AT requires only 40 IC's plus memory**

The CS8230 AT/386 CHIPSet™ is a seven chip VLSI implementation of most of the system logic to control an iAPX 386 based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIP's 82C206, Integrated Peripherals Controller, provides a complete PC AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet™ consists of one 82C301 Bus Controller, one 82C302 Page/ Interleave MemoryController, one each of 82A303 and 82A304 Address Bus Interfaces, two 82A305 Data Bus Interfaces, and a 82A306 Control Signal Buffer.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram below. The 82C301 and 82A306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock, and allows for dynamic selection of the processor clock between the 16 MHz clock and the AT bus clock. The



AT/386 System Block Diagram

82A306 provides buffers for bus control signals in addition to other miscellaneous logic functions.

The 82C302 Page/Interleave Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 1 MB to 16 MB of DRAMs with combinations of 256Kbit and 1Mbit DRAMs. The processor can operate at 16 MHz with zero wait state memory accesses by using 100 nsec DRAMs.

The 82A303 and 82A304 interface between all address buses, generate RAS/CAS addresses for the system memory and the addresses needed for proper data path conversion. Two 82A305 are used to interface between the local, system memory, and AT data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths.

System Overview

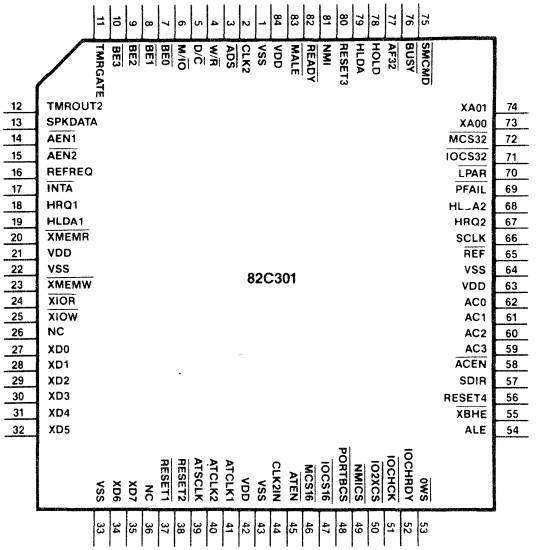
The CS 8230 is designed for use in 80386-based systems and provides complete support for the IBM PC AT bus. There are four buses supported by the CS 8230 as shown in the AT/386 system block diagram: CPU local bus (A and D), system memory bus (MA and MD), IO Channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface to DRAM's controlled by the 82C302. The IO channel bus refers to the bus supporting the AT bus adapters which could be either a 8 bit devices or 16 bit devices. The X bus refers to the peripheral bus to which the DMA controllers and timers are attached in an IBM PC AT. The X bus has only an 8-bit data path. The term "AT bus" is used to refer to the IO channel bus and X bus. Provisions are also made for user extension of the IO channel to 32 bit bus.

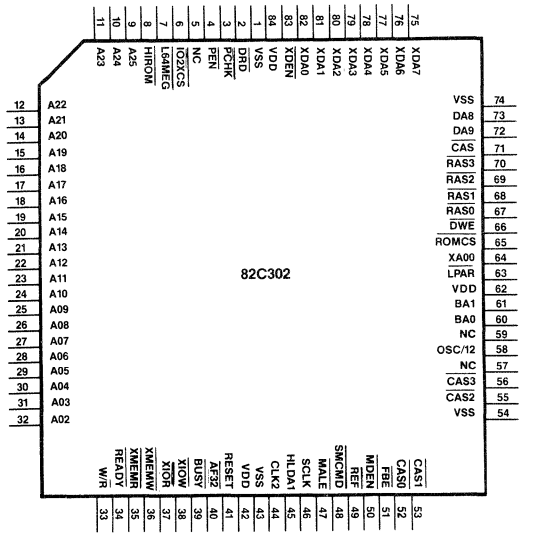
Notation and Glossary

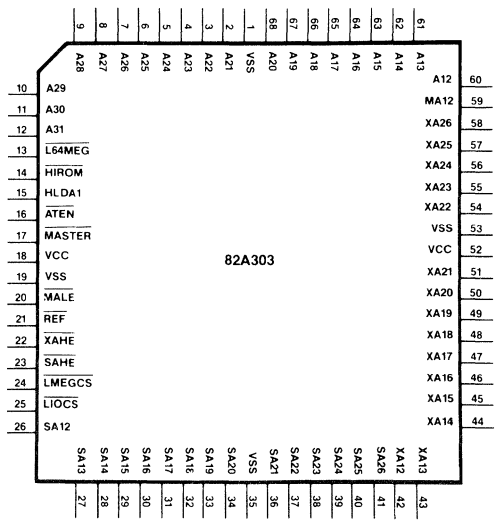
The following notations are used to refer to the configuration and diagnostic registers internal to the 82C301 and 82C302.

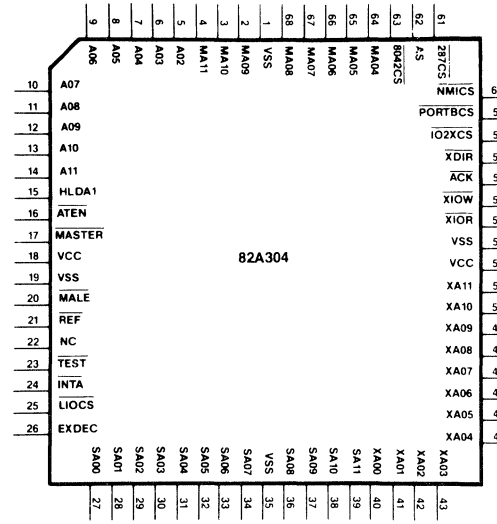
REGnH denotes the internal register with the index n in hexadecimal notation.

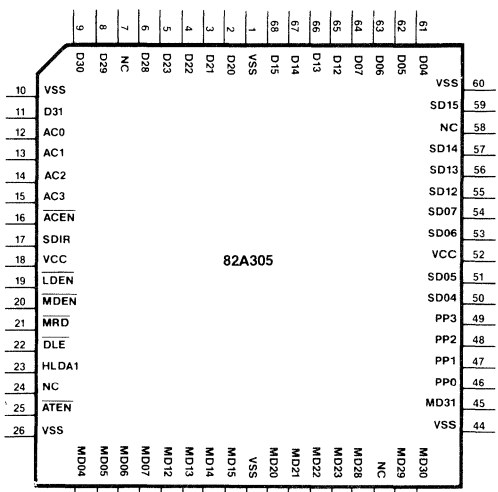
REGnH<x:y> denotes the bit field from bits y to x of the internal register with the index n in hexadecimal notation.

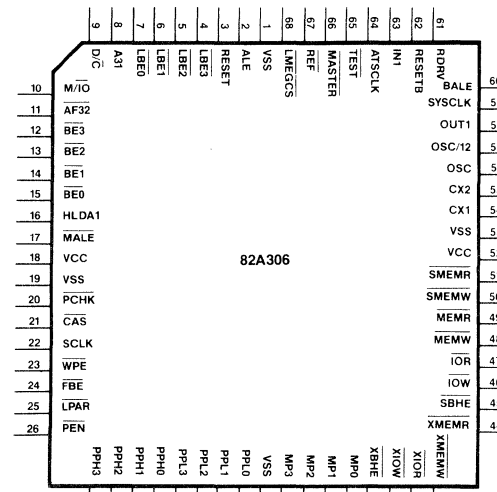

82C301
1 VSS
2 CLK2
3 ADS
4 W/R
5 D/C
6 M/IO
7 BE0
8 BE1
9 BE2
10 BE3
11 TMRGATE
12 TMROUT2
13 SPKDATA
14 AEN1
15 AEN2
16 REFREQ
17 INTA
18 HRQ1
19 HLDA1
20 XMEMR
21 VDD
22 VSS
23 XMEMW
24 XIOR
25 XIOW
26 NC
27 XD0
28 XD1
29 XD2
30 XD3
31 XD4
32 XD5
33 VSS
34 XD6
35 XD7
36 NC
37 RESET1
38 RESET2
39 ATSCLK
40 ATCLK2
41 ATCLK1
42 VDD
43 VSS
44 CLK2IN
45 ATEN
46 MCS16
47 IOCS16
48 PORTBCS
49 NMICS
50 IO2XCS
51 IOCHCK
52 IOCHRDY
53 0WS
54 ALE
55 XBHE
56 RESET4
57 SDIR
58 ACEN
59 AC3
60 AC2
61 AC1
62 AC0
63 VDD
64 VSS
65 REF
66 SCLK
67 HRQ2
68 HL_A2
69 PFAIL
70 LPAR
71 IOCS32
72 MCS32
73 XA00
74 XA01
75 SMCMD
76 BUSY
77 AF32
78 HOLD
79 HLDA
80 RESET3
81 NMI
82 READY
83 MALE
84 VDD


82C302
1 VSS
2 DRD
3 PCHK
4 PEN
5 NC
6 IO2XCS
7 L64MEG
8 HIROM
9 A25
10 A24
11 A23
12 A22
13 A21
14 A20
15 A19
16 A18
17 A17
18 A16
19 A15
20 A14
21 A13
22 A12
23 A11
24 A10
25 A09
26 A08
27 A07
28 A06
29 A05
30 A04
31 A03
32 A02
33 W/R
34 READY
35 XMEMW
36 XMEMR
37 XIOR
38 XIOW
39 BUSY
40 AF32
41 RESET
42 VDD
43 VSS
44 CLK2
45 HLDA1
46 SCLK
47 MALE
48 SMCMD
49 REF
50 MDEN
51 FBE
52 CAS0
53 CAS1
54 VSS
55 CAS2
56 CAS3
57 NC
58 OSC/12
59 NC
60 BA0
61 BA1
62 VDD
63 LPAR
64 XA00
65 ROMCS
66 DWE
67 RAS0
68 RAS1
69 RAS2
70 RAS3
71 CAS
72 DA9
73 DA8
74 VSS
75 XDA7
76 XDA6
77 XDA5
78 XDA4
79 XDA3
80 XDA2
81 XDA1
82 XDA0
83 XDEN
84 VDD


82A303
1 VSS
2 A21
3 A22
4 A23
5 A24
6 A25
7 A26
8 A27
9 A28
10 A29
11 A30
12 A31
13 L64MEG
14 HIROM
15 HLDA1
16 ATEN
17 MASTER
18 VCC
19 VSS
20 MALE
21 REF
22 XAHE
23 SAHE
24 LMEGCS
25 LIOCS
26 SA12
27 SA13
28 SA14
29 SA15
30 SA16
31 SA17
32 SA18
33 SA19
34 SA20
35 VSS
36 SA21
37 SA22
38 SA23
39 SA24
40 SA25
41 SA26
42 XA12
43 XA13
44 XA14
45 XA15
46 XA16
47 XA17
48 XA18
49 XA19
50 XA20
51 XA21
52 VCC
53 VSS
54 XA22
55 XA23
56 XA24
57 XA25
58 XA26
59 MA12
60 A12
61 A13
62 A14
63 A15
64 A16
65 A17
66 A18
67 A19
68 A20


82A304
1 VSS
2 MA09
3 MA10
4 MA11
5 A02
6 A03
7 A04
8 A05
9 A06
10 A07
11 A08
12 A09
13 A10
14 A11
15 HLDA1
16 ATEN
17 MASTER
18 VCC
19 VSS
20 MALE
21 REF
22 NC
23 TEST
24 INTA
25 LIOCS
26 EXDEC
27 SA00
28 SA01
29 SA02
30 SA03
31 SA04
32 SA05
33 SA06
34 SA07
35 VSS
36 SA08
37 SA09
38 SA10
39 SA11
40 XA00
41 XA01
42 XA02
43 XA03
44 XA04
45 XA05
46 XA06
47 XA07
48 XA08
49 XA09
50 XA10
51 XA11
52 VCC
53 VSS
54 XIOR
55 XIOW
56 ACK
57 XDIR
58 IO2XCS
59 PORTBCS
60 NMICS
61 287CS
62 AS
63 8042CS
64 MA04
65 MA05
66 MA06
67 MA07
68 MA08


82A305
1 VSS
2 D20
3 D21
4 D22
5 D23
6 D28
7 NC
8 D29
9 D30
10 VSS
11 D31
12 AC0
13 AC1
14 AC2
15 AC3
16 ACEN
17 SDIR
18 VCC
19 LDEN
20 MDEN
21 MRD
22 DLE
23 HLDA1
24 NC
25 ATEN
26 VSS
27 MD04
28 MD05
29 MD06
30 MD07
31 MD12
32 MD13
33 MD14
34 MD15
35 VSS
36 MD20
37 MD21
38 MD22
39 MD23
40 MD28
41 NC
42 MD29
43 MD30
44 VSS
45 MD31
46 PP0
47 PP1
48 PP2
49 PP3
50 SD04
51 SD05
52 VCC
53 SD06
54 SD07
55 SD12
56 SD13
57 SD14
58 NC
59 SD15
60 VSS
61 DD4
62 DD5
63 DD6
64 DD7
65 D12
66 D13
67 D14
68 D15


82A306
1 VSS
2 ALE
3 RESET
4 LBE3
5 LBE2
6 LBE1
7 LBE0
8 A31
9 D/C
10 M/IO
11 AF32
12 BE3
13 BE2
14 BE1
15 BE0
16 HLDA1
17 MALE
18 VCC
19 VSS
20 PCHK
21 CAS
22 SCLK
23 WPE
24 FBE
25 LPAR
26 PEN
27 PPH3
28 PPH2
29 PPH1
30 PPH0
31 PPL3
32 PPL2
33 PPL1
34 PPL0
35 VSS
36 MP3
37 MP2
38 MP1
39 MP0
40 XBHE
41 XIOW
42 XIOR
43 XMEMW
44 XMEMR
45 SBHE
46 IOW
47 IOR
48 MEMW
49 MEMR
50 SMEMW
51 SMEMR
52 VCC
53 VSS
54 CX1
55 CX2
56 OSC
57 OSC/12
58 OUT1
59 SYSCLK
60 BALE
61 RDRV
62 RESETB
63 IN1
64 ATSCLK
65 TEST
66 MASTER
67 REF
68 LMEGCS

82C301 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks			
44	CLK2IN	I	CLOCK 2 INPUT from a packaged TTL crystal oscillator having twice the rated frequency of the processor.
2	CLK2	O	CLK2 output to the Clock 2 input of 80386 and the memory controller. This clock output is derived from CLK2IN and has a 50% duty cycle. The clock can also be programmed to be the same as the BCLK.
66	SCLK	O	SCLK is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock and CLK2.
41	ATCLK1	I	BUS CLOCK INPUT source from Crystal or Oscillator. This clock input is used for the AT Bus operation and is required only if the AT bus state machine clock (BCLK) will not be derived from the CLK2 input. This signal should be tied LO if not used.
40	ATCLK2	O	BUS CLOCK CRYSTAL OUTPUT is connected to the crystal oscillator circuit if a packaged oscillator is not used. A series resistor should be used to reduce the amplitude of the resonant circuit. It should be left unconnected if a packaged TTL oscillator is used.
39	ATSCLK	O	AT SYSTEM CLOCK is buffered to drive the clock signal SYSCLK on the AT bus I/O channel. It is half the frequency of BCLK and should have a nominal value in the range of 6 to 8 MHz for maintaining correct AT I/O bus timing with IBM PC AT.
Control			
37	$\overline{\text{RESET1}}$	I	Active LO. $\overline{\text{RESET1}}$ is connected to the power good signal generated by the PWRGOOD from the power supply. When LOW it will activate RESET3 and RESET4 for resetting the system.
38	$\overline{\text{RESET2}}$	I	Active LO. $\overline{\text{RESET2}}$ (8042RC) is an active LOW signal generated from the keyboard controller 8042 for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3 signal.
56	RESET4	O	Active HI. RESET4 is the System Reset used to reset the AT Bus, 82C206 IPC, 8042 keyboard controller 82C302 or 82C312 memory controller. RESET4 is synchronized with the processor clock.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
CPU Interface			
80	RESET3	O	Active HI. RESET3 is the reset to the 80386 when $\overline{\text{RESET1}}$ or $\overline{\text{RESET2}}$ is active. This is also activated when shutdown condition in the CPU is detected.
82	$\overline{\text{READY}}$	I/O	Active LO. $\overline{\text{READY}}$ is driven LO during AT bus cycles indicating that the current CPU bus cycle is to be completed. It is also asserted if 'Time Out' condition is detected. During all other cycles it is an input to 82C301. Ready is an open collector output requiring an external pull up resistor. It connects to the 80386 $\overline{\text{READY}}$ pin.
3	$\overline{\text{ADS}}$	I	Active LO. ADDRESS STATUS input connected to the 80386 $\overline{\text{ADS}}$ pin.
4	W/$\overline{\text{R}}$	I/O	READ/WRITE STATUS input from the 80386 W/$\overline{\text{R}}$ signal. It indicates a write bus cycle if it is HI and a read cycle if it is LO.
5	D/$\overline{\text{C}}$	I	DATA/CONTROL STATUS input from the 80386 D/$\overline{\text{C}}$ signal.
6	M/$\overline{\text{IO}}$	I	MEMORY/IO STATUS input from the 80386 M/$\overline{\text{IO}}$ signal.
78	HOLD	O	Active HI. HOLD REQUEST output to the 80386 HOLD input pin. This signal is used to request the CPU to relinquish the bus cycles to another requesting master such as HRQ1, HRQ2 and REFREQ.
79	HLDA	I	Active HI. HOLD ACKNOWLEDGE input connected to processor HLDA signal. When the signal is HIGH it indicates that the processor has relinquished the system bus in response to the HOLD request.
10-7	$\overline{\text{BE<3:0>}}$	B	Active LO. BYTE ENABLE signals input from the 80386 $\overline{\text{BE<3:0>}}$ during a CPU cycle. $\overline{\text{BE3}}$ controls the most significant while $\overline{\text{BE0}}$ controls the least significant byte. $\overline{\text{BE<3:0>}}$ are generated by 82C301 during DMA cycles based on the status signals XA0, XA1 and $\overline{\text{XBHE}}$.
81	NMI	O	Active HI. NON-MASKABLE INTERRUPT connects to the 80386 NMI pin and is generated by 82C301 to cause an NMI.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Decodes			
48	$\overline{\text{PORTBCS}}$	I	Active LO. PORT B CHIP SELECT is the address decode input from the 82A304 as enable for the Port B register at address 061H.
49	$\overline{\text{NMICS}}$	I	Active LO. NMI CHIP SELECT is the address decode input from the 82A304 as enable for the NMI enable bit at address 070H.
50	$\overline{\text{IO2XCS}}$	I	Active LO. IO2X CHIP SELECT is the address decode input from the 82A304 as chip select for the IO registers at 022H and 023H used to access the 82C301 internal configuration registers.
53	$\overline{\text{0WS}}$	I	Active LO. ZERO WAIT STATE acknowledge input from the IO channel. When active it causes immediate termination of the current AT bus memory or IO cycle.
IO Channel Interface			
52	IOCHRDY	I	Active HI. IO CHANNEL READY input from the AT bus. When LOW it indicates a 'not ready' condition and forces the insertion of wait states in I/O or memory accesses. When HIGH it will allow the completion of the current memory or I/O access.
51	$\overline{\text{IOCHCK}}$	I	Active LO. IO CHANNEL CHECK input from the AT bus which causes an NMI to be generated if enabled. It is used to signal an Error condition from a device residing on the AT bus.
70	$\overline{\text{LPAR}}$	I	Active LO. PARITY ERROR input from local memory system which causes an NMI to be geneated if enabled.
69	$\overline{\text{PFAIL}}$	I	Active LO. POWER FAIL WARNING signal input from the power supply.
54	ALE	O	Active HI. ADDRESS LATCH ENABLE to AT bus. This signal controls the address latches used to hold the address during a bus cycle. The signal should be buffered to drive the AT bus.
DMA Interface			
19	HLDA1	O	Active HI. HOLD ACKNOWLEDGE 1 is active when a bus cycle is granted in response to HRQ1.
68	HLDA2	O	Active HI. HOLD ACKNOWLEDGE 2 is active when a bus cycle is granted in response to HRQ2.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
18	HRQ1	I	Active HI. HOLD REQUEST 1 is active when a DMA/ Master is requesting a bus cycle. For an AT compatible architecture it should be connected to the HOLD REQUEST signal from DMA1 and DMA2.
67	HRQ2	I	Active HI. HOLD REQUEST 2 is active when a DMA/ Master is requesting a bus cycle. This should be grounded if not used.
14	$\overline{\text{AEN1}}$	I	Active LO. ADDRESS ENABLE for 8 bit DMA transfers.
15	$\overline{\text{AEN2}}$	I	Active LO. ADDRESS ENABLE for 16 bit DMA transfers.
Control Strobes			
46	$\overline{\text{MCS16}}$	I	Active LO. $\overline{\text{MCS16}}$ When active causes 16 bit memory accesses on IO channel.
72	$\overline{\text{MCS32}}$	I	Active LO. $\overline{\text{MCS32}}$ when active causes 32 bit memory accesses on IO channel.
47	$\overline{\text{IOCS16}}$	I	Active LO. $\overline{\text{IOCS16}}$ when active causes 16 bit IO accesses on IO channel.
71	$\overline{\text{IOCS32}}$	I	Active LO. $\overline{\text{IOCS32}}$ when active causes 32 bit IO accesses on IO channel.
75	$\overline{\text{SMCMD}}$	O	Active LO. SYSTEM MEMORY COMMAND when active indicates the current access cycle is a memory cycle.
Refresh			
16	REFREQ	I	Active HI. REFresh REQuest when active initiates a DRAM refresh sequence be initiated. This signal is obtained from the timer controller, 8254, in a PC AT implementation.
65	$\overline{\text{REF}}$	I/O	Active LO. REFresh is an open drain signal. It initiates a refresh cycle for the DRAMs. As an input it can be used to force a refresh cycle from an I/O device. An external pull up is required.
X Bus Interface			
20	$\overline{\text{XMEMR}}$	I/O	Active LO. X BUS MEMORY READ is a control strobe directing memory to place data on the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	$\overline{\text{XMEMW}}$	I/O	Active LO. X BUS MEMORY WRITE is a control strobe directing memory to accept data from the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.
24	$\overline{\text{XIOR}}$	I/O	Active LO. X BUS IO READ is a control strobe directing an IO port to place data on the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.
25	$\overline{\text{XIOW}}$	I/O	Active LO. X BUS IO WRITE is a control strobe directing an IO port to accept data from the data bus. It is sourced either from the 82C305 when the 80386 is the master or from the DMA.
55	$\overline{\text{XBHE}}$	I/O	Active LO. X BUS BYTE HIGH ENABLE indicates that the high byte (bits <15:08>) on the bus has valid data. It is sourced from the 82C301 when 80386 or DMA2 (16 bit) is the master.
35-34	XD<7:6>	I/O	X DATA BUS bits <7:6>
32-27	XD<5:0>	I/O	X DATA BUS bits <5:0>
57	SDIR	O	SYSTEM BUS DIRECTION controls the direction of data transfer between the IO channel and the local bus. When LO the it enables data transfer from the IO channel to local bus.
58	$\overline{\text{ACEN}}$	O	Active LO. ACTION CODE ENABLE when active validates the action code signals AC<3:0>.
59-62	AC<3:0>	O	ACTION CODE is a four-bits encoded command for bus size control and byte assembly operations performed by the 82A305s.
Memory Control			
77	$\overline{\text{AF32}}$	I	Active LO. AF32 when active indicates that a bus cycle is a local bus access without any data size conversion or AT cycle simulation treated as a 32-bit access.
76	$\overline{\text{BUSY}}$	I	Active LO. BUSY from memory controller.
83	$\overline{\text{MALE}}$	O	Active LO. Address Latch Enable for accesses to on board memory/IO. It also indicates start of a new CPU cycle.
11	TMRGATE	O	Active HI. TIMER GATE signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
12	TMROUT2	I	Active HI. TIMER OUT 2 is the output from the timer 8254. It can be read from port B.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
13	SPKDATA	O	Active HI. SPEAKER DATA is used to gate the 8254 tone signal to the speaker.
17	$\overline{\text{INTA}}$	O	Active LO. Interrupt acknowledge output to the interrupt controller.
45	$\overline{\text{ATEN}}$	O	Active LO. AT ENABLE when active indicates the current CPU access is an AT bus cycle.
73	XA00	I/O	Address bit 0. It is sourced from the 82C301 when 80386 or DMA (16 bit) is a bus master.
74	XA01	I/O	Address but 1. It is sourced from the 82C301 when 80386 is a bus master.
26,36	NC		Reserved
21,42 63,84	VDD VDD		Power
1 22,33 43,64	VSS VSS VSS		Ground

82C302 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks and Control			
44	CLK2	I	Processor Clock
46	SCLK	O	Generated CLK2/2 for reference.
41	RESET	I	Active HI. When active resets 82C302
49	$\overline{\text{REF}}$	I	Active LO. DRAM refresh control signal.
47	$\overline{\text{MALE}}$	I	Active LO. Address Latch Enable
33	W/$\overline{\text{R}}$	I	System WRITE/$\overline{\text{READ}}$ status input
48	$\overline{\text{SMCMD}}$	I	Active LO. System Memory Command. Indicates that the current command is for memory.
37	$\overline{\text{XIOR}}$	I	Active LO. I/O READ command used to qualify $\overline{\text{IO2XCS}}$.
38	$\overline{\text{XIOW}}$	I	Active LO. I/O WRITE command used to qualify $\overline{\text{IO2XCS}}$.
35	$\overline{\text{XMEMR}}$	I	Active LO. X Bus memory READ command.
36	$\overline{\text{XMEMW}}$	I	Active LO. X Bus memory WRITE command.
45	HLDA1	I	Active HI. HOLD ACKNOWLEDGE 1 input from 82C301.
63	$\overline{\text{LPAR}}$	I	Active LO. Parity error indication during a DRAM read. The failing address will be latched inside the chip for diagnostic purposes.
8	$\overline{\text{HIROM}}$	I	Active LO. High ROM address chip select asserted when the highest 16 MBytes of memory is addressed (A<31:A24>=FFH). Unlatched. This is used in conjunction with the remaining address bits to generate the $\overline{\text{ROMCS}}$ signal.
7	$\overline{\text{L64MEG}}$	I	Active LO. Low 64M address that is asserted when A<31:26>=00H. Unlatched.
65	$\overline{\text{ROMCS}}$	O	Active LO. Chip select for the BIOS EPROMs that is qualified with W/$\overline{\text{R}}$ and $\overline{\text{SMCMD}}$.
6	$\overline{\text{IO2XCS}}$	I	Active LO. IO address 22 and 23 chip selects. I/O port 22 is the index register for the configuration register set and and I/O 23 is accessed as the 8 bit configuration register selected by the index written to I/O port 22.
09-32	A<25:02>	I	Address from the CPU local bus.
64	XA00	I	Address from the X Bus

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
34	$\overline{\text{READY}}$	I/O	Active LO. System ready indicating the end of current 386 bus cycle. It goes inactive when the requested memory transfer has been completed. It becomes an input when the current bus cycle is for the AT IO expansion channel ($\overline{\text{AF32}}$ = 0).
39	$\overline{\text{BUSY}}$	O	Active LO. Indicates that the memory controller is still servicing a previous request. This should be connected to IOCHRDY through an open collector buffer. This signal should not be confused with the BUSY of 80386.
40	$\overline{\text{AF32}}$	O	Active LO, open drain. If asserted indicates that the current address is for local memory on the system board (DRAM or possibly EPROM). Otherwise the current address is assumed to be on the AT IO channel.
Memory Expansion			
61-60	BA<1:0>	O	Addresses that may be externally decoded to gate RAS to the correct block of 4 banks of DRAMs. These will always be zero.
2	$\overline{\text{DRD}}$	O	Active LO. DRAM Read controls the direction of data transfer between the DRAM and local bus. When LO it controls the transfer from the memory data bus toward CPU and from the CPU to memory otherwise.
DRAM Interface			
70-67	$\overline{\text{RAS}}$<3:0>	O	Active LO. Row Address Strobe. There is one for each bank.
71	$\overline{\text{CAS}}$	O	Active LO. Column Address Strobe. Used to latch data in the 82A305 data buffer.
56-55 53-52	$\overline{\text{CAS}}$<3:2> $\overline{\text{CAS}}$<1:0>	O	Active LO. Column Address Strobe. A strobe per bank that must be externally gated with byte enables for each byte of DRAM chips.
58	OSC/12	I	1.19MHz Clock input used for RAS pulse width time-out. Replaces CA3 on Cache controller.
66	$\overline{\text{DWE}}$	O	Active LO. DRAM Write Enable.
51	$\overline{\text{FBE}}$	O	Active LO. Force Byte Enable. Will always be inactive.
72-73	DA<9:8>	O	Remaining DRAM address bits.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
75-82	XDA<7:0>	I/O	Multiplexed bidirectional data pins for XD<7:0>. DA<7:0> are the lower address bits for the DRAM array.
83	$\overline{\text{XDEN}}$	O	Active LO. XD bus buffer Enable. $\overline{\text{XDEN}}$ is asserted during IO access cycles to 022H and 023H if 022H access is for an internal register of 82C302. $\overline{\text{XDEN}}$ is used to control the chip enable for the buffer between the XD and XDA buses.
3	$\overline{\text{PCHK}}$	O	Active LO. Parity Check Strobe.
4	$\overline{\text{PEN}}$	O	Active LO. Overall Parity Enable.
50	$\overline{\text{MDEN}}$	O	Active LO. MEMORY DATA BUFFER ENABLE. This signal is by default always LO and is connected to $\overline{\text{MDEN}}$ of 82A305.
Miscellaneous			
5,57,59	NC		Reserved
42,62,84	VDD		Power
1,43 54,74	VSS VSS		Ground

82A303 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active LO. Bus MASTER is generated by a device that is active on the expansion bus. After $\overline{\text{MASTER}}$ is force LO by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. $\overline{\text{MASTER}}$ must not be held LO for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.
15	HLDA1	I	Active HI. HOLD ACKNOWLEDGE from 82C301.
20	$\overline{\text{MALE}}$	I	Active LO. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising edge.
21	$\overline{\text{REF}}$	I	Active LO. REFRESH. Schmitt Trigger.
16	$\overline{\text{ATEN}}$	I	Active LO. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	O	Active LO. LOW IO ADDRESS CHIP SELECT is asserted when A<15:12>=0.
24	$\overline{\text{LMEGCS}}$	O	Active LO. LOW 1 MB SELECT is active when the access address decodes to the low 1MB address space: A<31:20> = 0.
13	$\overline{\text{L64MEG}}$	O	Active LO. LOW 64 MB SELECT is active when the access address decodes to the low 64MB address space: A<31:26> = 0.
14	$\overline{\text{HIROM}}$	O	Active LO. HI ROM SELECT is active when A<31:26> = 3FH.
Processor/Bus Interface			
12-2	A<31:21>	I/O	Local Address Bus
68-60	A<20:12>	I/O	
58-54	XA<26:22>	I/O	X Address Bus
51-42	XA<21:12>	I/O	
22	XAHE	I	Active LO. Enable bits 26:24 from the XA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
41-36	SA<26:21>	I/O	24mA. System Address Bus
34-26	SA<20:12>	I/O	

82A303 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	$\overline{\text{SAHE}}$	I	Active LO. Enable bits 26:24 from the SA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
59	MA12	O	Memory Address Bus Latched on the trailing edge of MALE.
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A304 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active LO. BUS MASTER is generated by a device active on the expansion bus.
15	HLDA1	I	Active HI. HOLD ACKNOWLEDGE 1 from 82C301.
20	$\overline{\text{MALE}}$	I	Active LO. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising (trailing) edge.
21	$\overline{\text{REF}}$	I	Active LO. REFRESH Schmitt trigger.
16	$\overline{\text{ATEN}}$	I	Active LO. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	I	Active LO. LOW IO ADDRESS CHIP SELECT.
54	$\overline{\text{XIOR}}$	I	Active LO. X BUS IO Read.
55	$\overline{\text{XIOW}}$	I	Active LO. X BUS IO Write
57	$\overline{\text{XDIR}}$	O	X BUS DIRECTION is used to control the drivers between the X bus and S bus. The drivers should be used such that S bus signals are driven toward X bus when $\overline{\text{XDIR}}$ is LO and in the other direction when HI.
26	EXDEC	I	Active HI. EXTENDED IO DECODE. A strapping option that when LO ignores A<11:10> and $\overline{\text{LIOCS}}$ (which is decoded based on A<15:12>) for decoding the system board IO ports. An internal pullup is provided.
58	$\overline{\text{IO2XCS}}$	O	Active LO. IO 2x SELECT is decode of IO address 022H or 023H.
63	$\overline{\text{8042CS}}$	O	Active LO. 8042 SELECT is decode of 8042 address at 060H or 064H.
59	$\overline{\text{PORTBCS}}$	O	Active LO. PORTB SELECT is decode of Port B address at 061H
60	$\overline{\text{NMICS}}$	O	Active LO. NMI SELECT is decode of NMI address at 070H.
61	$\overline{\text{287CS}}$	O	Active LO. 80287 SELECT is decode of 287 address at 0E0-0FFH.
56	$\overline{\text{ACK}}$	O	Active LO. ACKNOWLEDGE indicates that AEN1 OR AEN2 has been asserted. This signal is used to generate AEN signal on the AT I/O channel.
62	AS	O	Active HI. Address Strobe for the RTC. IO address 7xH is conditioned with XIOW.

82A304 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
24	$\overline{\text{INTA}}$	I	Active LO. INTERRUPT ACKNOWLEDGE bus cycle indication.
Processor/Bus Interface			
14-5	A<11:02>	I/O	Local address
51-40	XA<11:00>	I/O	X bus address
39-36	SA<11:08>	I/O	24mA. System address
34-27	SA<07:00>	I/O	
4-2	MA<11:09>	O	Memory address
68-64	MA<08:04>	O	
23	$\overline{\text{TEST}}$	I	Active LO. TEST when active resets the refresh counter to zero. A pullup is provided.
22	NC		Reserved
Miscellaneous			
18,52	VCC		Power
1,19	VSS		Ground
35,53	VSS		

82A305 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
15-12	AC<3:0>	I	Action Code (bus size/assembly command)
16	$\overline{\text{ACEN}}$	I	Active LO. Action Code Enable when active validates the action codes.
17	SDIR	I	System bus DIRection. When LO enables data transfers from the System to Local busn and in the other direction otherwise.
25	$\overline{\text{ATEN}}$	I	Active LO. AT bus ENable
23	HLDA1	I	Active HI. HoLD Acknowledge.
20	$\overline{\text{MDEN}}$	I	Active LO. MEMORY DATA BUFFER ENABLE. When LO enables the memory data buffers for transfer between the processor and memory subsystem. When HI disables these bus buffers. Should be connected to $\overline{\text{MDEN}}$ on the 82C302.
19	$\overline{\text{LDEN}}$	I	Active LO. Selects LD as a source for the SD bus during MASTER or DMA reads. When HI selects MD. Asserting $\overline{\text{MRD}}$ overrides $\overline{\text{LDEN}}$ and gates MD to the SD bus. A pullup is provided.
21	$\overline{\text{MRD}}$	I	Active LO. Memory Bus DIRection. When LO enables data movement for a processor read from the memory to local bus. $\overline{\text{MRD}}$ when HI enables drivers from local to memory bus.
22	$\overline{\text{DLE}}$	I	Active LO. Data Latch Enable.
Data Paths (Bit numbers are for the upper 4 bits slice of each byte and should be 4 less for the lower nibble slice).			
11, 9	D<31:30>	I/O	
8, 6	D<29:28>	I/O	
5-2	D<23:20>	I/O	Local Data Bus
68-65	D<15:12>	I/O	
64-61	D<07:04>	I/O	
45,43	MD<31:30>	I/O	
42,40	MD<29:28>	I/O	
39-36	MD<23:20>	I/O	Memory Data Bus
34-31	MD<15:12>	I/O	
30-27	MD<07:04>	I/O	
49-46	PP<03:00>	O	Memory Partial Parity

82A305 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
59,57	SD<15:14>	I/O	IO Channel Data Bus
56,55	SD<13:12>	I/O	
54-53	SD<07:06>	I/O	
51-50	SD<05:04>	I/O	
7,24	NC		Reserved.
41,58	NC		
Power Supplies			
18,52	VCC		Power
1,10	VSS		Ground
26,35	VSS		
44,60	VSS		

82A306 Pin Description

Pin No.	Symbol	Pin Type	Description
64	ATSCLK	I	AT IO channel SYSCLK input.
59	SYSCLK	O	24mA. Buffered SYSCLK to AT IO channel. Nominally one half of the bus state machine clock frequency.
Control			
54	CX1	I	14.318MHz oscillator input from crystal.
55	CX2	O	14.318MHz oscillator output to crystal.
56	OSC	O	24mA. System 14.318MHz output.
57	OSC/12	O	24mA. 14.318MHz/12 = 1.19MHz output.
17	$\overline{\text{MALE}}$	I	Active LO. Address Latch Enable for on board access.
12-15	$\overline{\text{BE<3:0>}}$	I	Active LO. BYTE ENABLE.
4-7	$\overline{\text{LBE<3:0>}}$	O	Active LO. LATCHED BYTE ENABLE on the trailing edge of $\overline{\text{MALE}}$.
24	$\overline{\text{FBE}}$	I	Active LO. FORCE BYTE ENABLE Forces all byte enables LBE active independent of $\overline{\text{MALE}}$ and the $\overline{\text{BE<3:0>}}$ inputs.
67	$\overline{\text{REF}}$	I	Active LO. REFRESH.
8	A<31>	I	Local Address Bus bit 31.
10	M/$\overline{\text{IO}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
9	D/$\overline{\text{C}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
68	$\overline{\text{LMEGCS}}$	I	Active LO. LOW MEGABYTE CHIP SELECT.
11	$\overline{\text{AF32}}$	O	Active LO, Tri-state output. $\overline{\text{AF32}}$ when active indicates a local bus memory access cycle on the system board. It is generated from M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, A<31>, and HLDA1.
66	$\overline{\text{MASTER}}$	I	Active LO. Bus MASTER input from the AT IO channel.
3	RESET	I	Active HI. RESET input. Should be connected to RESET4 of 82C301.
62	RESETB	O	Active HI. Buffered RESET to X bus.
61	RDRV	O	Active HI. 24mA. RESET to AT bus.
2	ALE	I	Active HI. ALE for AT bus.
40	$\overline{\text{XBHE}}$	I/O	Active LO. X Bus BHE.
44	$\overline{\text{XMEMR}}$	I/O	Active LO. X Bus Memory Read.
43	$\overline{\text{XMEMW}}$	I/O	Active LO. X Bus Memory Write.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
42	$\overline{\text{XIOR}}$	I/O	Active LO. X Bus IO Read.
41	$\overline{\text{XIOW}}$	I/O	Active LO. X Bus IO Write.
60	BALE	O	Active HI. 24mA. Buffered ALE to AT bus.
45	$\overline{\text{SBHE}}$	I/O	Active LO. 24mA. System bus BHE.
51	$\overline{\text{SMEMR}}$	O	Active LO. 24mA. System bus MEMory Read.
50	$\overline{\text{SMEMW}}$	O	Active LO. 24mA. System bus MEMory Write.
49	$\overline{\text{MEMR}}$	I/O	Active LO. 24mA. Memory Read.
48	$\overline{\text{MEMW}}$	I/O	Active LO. 24mA. Memory Write.
47	$\overline{\text{IOR}}$	I/O	Active LO. 24mA. IO Read.
46	$\overline{\text{IOW}}$	I/O	Active LO. 24mA. IO Write.
16	HLDA1	I	Active HI. HOLD ACKNOWLEDGE from 82C301.
22	SCLK	I	CLK2/2 clock input. Should be connected to SCLK output of 82C302.
27-30	PPH<3:0>	I	PARTIAL PARITY HIGH computed by 82A305 for the high nibble data bits.
31-34	PPL<3:0>	I	PARTIAL PARITY LOW computed by 82A305 for the low nibble data bits.
36-39	MP<3:0>	I/O	Data Parity bits for the DRAMs.
21	$\overline{\text{CAS}}$	I	Active LO. Read Parity latch enable.
20	$\overline{\text{PCHK}}$	I	Active LO. PARITY CHECK STROBE for generating LPAR from the partial parity and data parity bits.
26	$\overline{\text{PEN}}$	I	Active LO. Overall PARITY CHECK ENABLE.
23	$\overline{\text{WPE}}$	I	Active LO. WRITE PARITY ENABLE. Enables the sourcing of write parity onto the MP bus. A pullup is provided.
25	$\overline{\text{LPAR}}$	O	Active LO. LATCHED PARITY ERROR signal.
65	$\overline{\text{TEST}}$	I	Active LO. Enables testing of the OSC/12 counter. A pullup is provided.
63	IN1	I	Input to an uncommitted 24mA non-inverting buffer.
58	OUT1	O	24mA. Output of the IN1 buffer.
Power Supply			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82C301 BUS CONTROLLER

- Optional Independent AT Bus Clock
- Processor Clock Selection
- AT Bus Timing Configuration
- CPU Interface and Bus Control
- Port B Register

OVERVIEW

The 82C301 provides a clock generation circuitry to solve two basic problems. One is to provide system designers the choice of a particular AT bus clock most adequate for their applications. The other is to allow the processor to run at the full speed and optionally at a speed to match timing dependent application software. Because many AT adapter boards are designed with built in timing assumptions, independent programmable controls are provided for AT bus command timing and wait state generation for IO accesses and for 8, 16, and 32 bit memory accesses.

The 82C301 interfaces directly with the 80386 and implements the state machines required for controlling all bus accesses. It also features a status register known as Port B register used in a standard IBM PC AT.

FUNCTIONAL DESCRIPTION

The 82C301 has the following function blocks as illustrated in figure 1-1:

- Clock generation and reset control
- CPU bus access state machine
- AT bus access state machine
- Port B register and NMI logics
- Bus Arbitration and refresh logic

Clock Generation and Reset Control

The 82C301 provides three major system clocks: the processor clock CLK2, the BCLK clock for AT bus state machine of 82C301, and the AT bus clock SYSCLK. The BCLK (SYSCLK × 2) is a clock internal to the 82C301 and is used in this document to describe the system operation.

The clock generation circuitry shown in figure 1-2 contains two external clocks CLK2IN and ATCLK1 used as selectable clock sources. CLK2IN is assumed to be greater than 20MHz and should come from a packaged crystal oscillator while an oscillator circuit is provided for the ATCLK1 signal so that it can be connected to either a packaged oscillator or a crystal. This ATCLK1 input is required only if BCLK need be derived from an independent clock source other than CLK2IN. When required ATCLK1 frequency should be between 10 and 20 MHz for a typical PC AT. Notice that by design SYSCLK is always the BCLK divided by two.

The clock switching logic is guaranteed to provide a "clean" transition with no phases shorter than the minimum values or longer than the maximum values. This allows the clock selections be done dynamically.

Processor clock selection

Referring to figure 1-2, the CLK2 and SCLK signal can be selected from two sources:

—the external oscillator connected to CLK2IN,
—the AT bus state machine clock BCLK.

This selection is made by programming bit 4 of the configuration register 4 which defaults to CLK2IN upon reset. By design, if SCLK is selected as the source for BCLK, CLK2 must not be sourced from BCLK. In all but some special cases, CLK2IN should match the rated processor speed, and the BCLK can be either subdivisions of CLK2IN or ATCLK1.

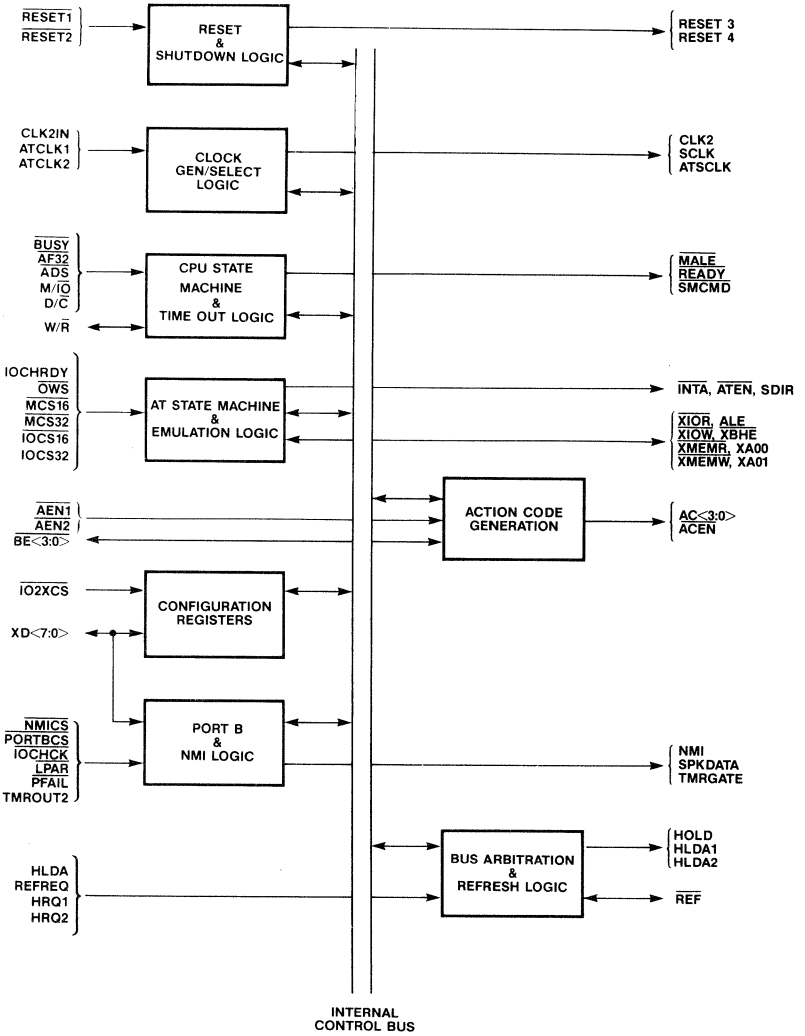


Figure 1-1. 82C301 Functional Block Diagram

AT bus clock selection

The 82C301 provides flexible software controlled selection of the clock used for the AT bus state machine. The clock can be synchronous (related but not necessarily equal) to the processor CLK2 or unrelated (requiring synchronization between the AT and processor bus state machines). While synchronization logic has been provided in all interface signals between the CPU and the AT state machines, it is highly recommended that the AT bus state machine clock (BCLK) be sourced from SCLK. An internal programmable divider has been provided allowing BCLK frequency of CLK2/2 or CLK2/3. This eliminates the need for an additional oscillator for some system designs. If the divide by 3 option is selected the resulting waveform will have an approximately 50% duty cycle.

The SYSCLK signal generated by the 82C301 is one half of the AT bus state machine clock BCLK. Since this clock is used to drive the AT bus, it is recommended that the the divide ratio be set for a SYSCLK of about 6 and 8MHz. The table 1-1 shows the combination of clock frequencies obtainable from CLK2IN with this selection scheme.

CLK2IN	SCLK Ratio	BCLK	SYSCLK
24	12 /2	12	6
32	16 /2	16	8
32	16/3 10.7	5.4	

Table 1-1. Examples of BCLK and SYSCLK derived from CLK2

Reset control

When $\overline{\text{RESET1}}$ signal is asserted 82C301 asserts RESET3 and RESET4 for a system reset. For warm restart not requiring the extensive reset, $\overline{\text{RESET2}}$ can be asserted to generate the RESET3 for resetting only the processor and some specific devices. RESET3 is also asserted when CPU shut down condition is detected. This differentiation of reset is

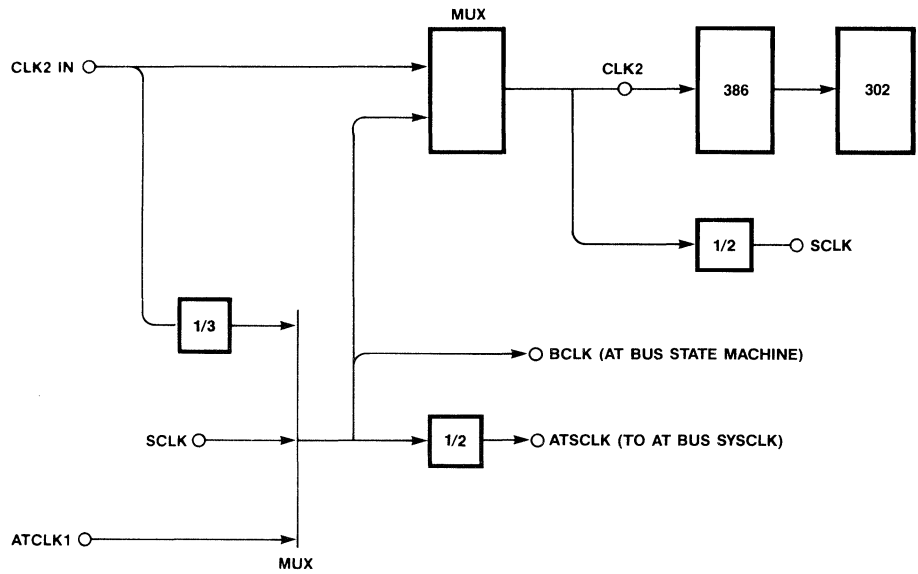


Figure 1-2. CLK2 and ATSCLK Clock Selection

provided so that some register states can be maintained through the reset if so desired.

Bus Arbitration, CPU bus and AT bus State Machines

The 82C301 performs the synchronization and control required between the local processor bus, the memory subsystem and the AT IO channel. It controls all bus activities and handles the HRQ1, HRQ2, and REFREQ by generating HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner. Upon CPU asserting HLDA the arbitration logic in turn responds by asserting HLDA1 (for HRQ1) or HLDA2 (for HRQ2), and the requesting DMA or master device has the control of the bus until it de-asserts HRQ1 (or HRQ2) to terminate the HLDA cycle. During the HLDA cycle, the 82C301 generates both SMCMD and action codes AC<3:0> to control the buffer enable and directions for the address and data buffers. Bus size conversions are not supported by 82C301 for these bus cycles and if necessary should be performed by the requesting device.

The CPU state machine and AT state machine control CPU accesses to the devices on the local bus and non-local buses respectively. The CPU state machine supports only 32 bit transfers between the 80386 and system memory (or memory mapped IO) and no bus size conversions are done. Thus BS16 input on the 80386 is not used in a CS8230 system and should be connected to a HI level. The AT state machine responsible for all non-local bus CPU accesses controls the AT bus and supports bus size matching.

All CPU access cycles are started by 82C301 asserting MALE. The CPU state machine then samples AF32 one SCLK clock cycle later. If AF32 is active, it is assumed to be a local bus cycle and the CPU state machine terminates this cycle when it detects READY signal active. In response to an MALE, if the AF32 is detected inactive the control is passed to AT state machine. At the end of the bus access cycle, the AT state machine generates READY to terminates the processor access cycle as well as the CPU state machine cycle.

CPU State Machine

Interface to the 80386 requires interpretation of the status lines upon assertion of ADS and synchronization and generation of a READY response to the CPU upon completion of the requested operation. By interpreting the CPU status lines and ADS, the 82C301 generates control signals MALE and SMCMD. In response to each ADS generated by CPU, an MALE is generated by the 82C301 to indicate the start of a new CPU access cycle. In a non-pipelined CPU cycle, MALE is generated in response to ADS being asserted by the 80386. In a pipelined cycle, MALE is generated when the assertion of READY is detected for the previous CPU cycle. If AF32 is not active one cycle after MALE is asserted, control is passed to the AT bus state machine. The CPU state machine then waits for READY becoming active to terminate the access cycle. In CS 8230 CHIPset, the READY can be generated by 82C302 which controls the system memory access.

SMCMD indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles it is generated for all memory cycles by decoding M/IO, D/C and W/R signals. During non-CPU cycles it is active when XMEMR or XMEMW is active.

NA Pipeline Control

The 82C301 supports both pipelined and non-pipelined cycles of the 80386. The NA (Next Address) input on the 80386 can be always asserted in a CS8230 system for higher performance.

Bus Timeout

An optional feature allows generation of an NMI if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32 is asserted in response to MALE and READY is not returned to the 82C301 within 128 CLK2 cycles. A control bit in the 82C301 configuration registers enables this feature.

AT Bus State Machine

The AT state machine gains the control of the buses when AF32 is detected inactive by the

CPU state machine. It uses BCLK having a frequency twice that of the IO channel clock SYSCLK. When ATCLK1 is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C301 supports 8, 16 or 32 bit transfers between the processor and 8, 16 or 32 bit memory or IO devices located on the IO channel.

An AT bus cycle is initiated by asserting ALE decoded from the CPU status signals and is terminated by asserting READY. On the falling (or trailing) edge of the ALE, MCS16, IOCS16, MCS32, IOCS32 are sampled to determine the bus size conversion required. It then enters the command cycle. The AT bus state machine provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide for timing emulation of lower speed IO channels to maintain compatibility with AT or PC/XT IO adapters and memory cards. The command cycle is terminated by detecting 0WS or IOCHRDY active.

IO Channel Speed Control

The AT state machine can be programmed to insert wait states in units of ATSCLK and to delay the generation of XIOR, XIOW, XMEMR, and XMEMW commands in one half units of ATSCLK (BCLK) within the selected wait states. The command phase delay can be selectively defined for IO cycles and for 8, 16, and 32 bit wide memory cycles by setting the corresponding fields in REG05H. REG06H controls the IO Channel wait state generation for 8, 16, and 32 bit accesses.

The bus clock BCLK is selected by setting REG06H<1:0>. It should be noted that the processor clock source should be set to CLK2IN whenever the BCLK is selected to be SCLK.

Data Conversion

The AT bus access state machine performs data conversion for CPU accesses to devices not on the local bus when AF32 is not asserted. AT bus data conversions are performed for the following types of transfers:

—32 bit to 8/16 bit,
—24 bit to 8/16 bit,
—16 bit to 8/16 bit.

Larger transfers are broken into smaller AT bus reads or writes and the action code AC<3:0> to the 82A306 is generated. Byte addresses XA<01:00> are generated to drive the lower two bits of the AT address bus.

The 82C301 responds to IOCS16, MCS16, IOCS32, and MCS32 in determining what size of data the IO channel needs. If none of the above signals are asserted, 8 bit transfers are assumed and the request is converted into 2, 3 or 4 IO channel cycles based on BE<3:0>. For either MCS16 or IOCS16, the AT bus state machine converts a 32-bit access into two 16 bit AT bus accesses.

The bus state machine also supports 32-bits transfer between the processor and memory and IO devices on the IO channel. IOCS32 and MCS32 inputs allow a device to request a 32-bits transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32 and MCS32 override IOCS16 and MCS16.

In performing these data conversions, a 4-bits action code AC<3:0> is generated to control the buffers in 82A305 for the alignment of data path, and direction control between D, MD, and SD data buses. The definition for the action codes is given in the functional description of 82A305.

Port B Register

The 82C301 provides access to Port B defined for a PC AT as shown in figure 1-3. PORTBCS enables the access to Port B register and is provided as an output from 82A304. Table 1-2 gives the Port B register bit definition.

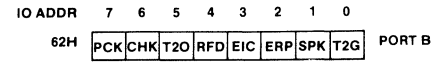


Figure 1-3. Port B register definition

Addr	Bits	Function	
62H		Port B Register	
	7	Read only.	PCK - System memory parity check.
	6	Read only.	CHK - IO channel check.
	5	Read only.	T2O - Timer 2 out
	4	Read only.	RFD - Refresh Detect.
	3	Read/write.	EIC - Enable IO channel check.
	2	Read/write.	ERP - Enable system memory parity check.
	1	Read/write.	SPK - Speaker Data
	0	Read/write.	T2G - Timer 2 Gate Speaker

Table 1-2. Port B Register Definition

CS 8230 Internal Register Access Ports

The CS 8230 have internal registers used for system configurations and for diagnostics. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of IO addresses required to access all registers needed to configure and control CS 8230 chips. Each access (either read or write) to an internal register is done by first writing its index into port 22H. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data port is being accessed again.

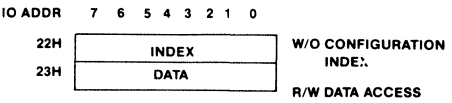


Figure 1-4. Configuration Register Access Ports

Configuration Registers

There are 3 bytes of configuration and diagnostic registers in 82C301 as shown in figure 1-5. The definitions for these registers are given in table 1-3.

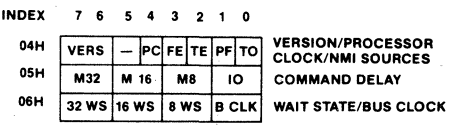


Figure 1-5. 82C301 Internal Configuration Registers

Index	Bits	Function
04H		Version/Processor clock select/NMI source
	7:6	Read only. Version 0 Initial version
	5	Reserved
	4	Processor Clock Select. If SCLK is selected as the source for BCLK, CLK2 source must not be selected as BCLK. 0 Use processor oscillator input. Default. 1 Use AT bus state machine clock (SYSCLKx2).
	3	Power Fail Warning Enable 0 Power Fail NMI not enabled. Default. 1 Power Fail NMI enabled
	2	Local Bus READY timeout NMI Enable 0 READY timeout NMI not enabled. Default. 1 READY timeout NMI enabled
	1	Read only. Power Fail warning active during last NMI arbitration. 0 Power Fail warning pin not active. Default. 1 Power Fail warning pin was active.
	0	Read only. Local bus READY timeout 0 READY timeout has not occurred. Default. 1 READY timeout has occurred
05H		Command delay The value for each one of the command delay field is defined as: 0 0 cycle delay 1 1 cycle delay 2 2 cycle delay 3 3 cycle delay
	7:6	AT Bus 32 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 32 bit memory cycle. Default is 0.
	5:4	AT Bus 16 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 16 bit memory cycle. Default is 0.

Table 1-3. 82C301 Configuration Register Definitions

Index	Bits	Function
05H	3:2	AT Bus 8 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 8 bit memory cycle. Default is 1.
	1:0	AT Bus I/O Cycle command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus IO cycle. Default is 1.
06H		Wait State/Bus Clock Source
	7:6	32 bit AT Bus wait state select 0-3 wait states per 32 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	5:4	16 bit AT Bus wait state select 0-3 wait states per 16 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	3:2	8 bit AT Bus wait state select 2-5 wait states per 8 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 5. 0 5 cycle delay 1 4 cycle delay 2 3 cycle delay 3 2 cycle delay
	1:0	Bus Clock Source Select 0 Use Proc Clock/3 for AT bus state machine. Default. 1 Use Proc Clock/2 for AT bus state machine. 2 Reserved. 3 Use ATCLK input pin for the AT bus state machine.

Table 1-3. 82C301 Configuration Register Definitions (Continued)

82C301 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C301 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C301 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 16 MHz Clock	I_{CC}		40	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA
CLK2 Output Low Voltage @ I_{OL} = 5 mA	V_{OLC}		0.45	V
CLK2 Output High Voltage @ I_{OH} = -1 mA	V_{OHC}	4.0		V

NOTE:
1. $\overline{REF}$ has I_{OL} = 16mA. CLK2, $\overline{MALE}$ have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C301 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t101	CLK2 period		31		ns
t102	CLK2 low time (at 32 MHz)	9			ns
t103	CLK2 high time (at 32 MHz)	9			ns
t104	CLK2 rise time			8	ns
t105	CLK2 fall time			8	ns
t106	SCLK delay from CLK2↑		4		ns
t107	RESET3, RESET4 set-up time		15		ns
t108	RESET3, RESET4 hold time		8		ns
t109	$\overline{\text{SMCMD}}$ delay from $\overline{\text{MALE}}$ active		7		ns
t110	$\overline{\text{AF32}}$ set-up time to CLK2↑	22			ns
t111	$\overline{\text{AF32}}$ hold time to CLK2↑	0			ns
t112	HOLD delay from CLK2↑		25		ns
t113	$\overline{\text{READY}}$ input set-up time to CLK2↑	13			ns
t114	$\overline{\text{READY}}$ input hold time from CLK2↑	5			ns
t115	$\overline{\text{ATEN}}$ active delay from CLK2↑		20		ns
t116	$\overline{\text{ATEN}}$ inactive delay from CLK2↑		20		ns
t117	$\overline{\text{MALE}}$ active delay from CLK2↑		15		ns
t118	$\overline{\text{MALE}}$ inactive delay from CLK2↓		15		ns
t119	$\overline{\text{READY}}$ output active delay from CLK2↑		20		ns
t120	$\overline{\text{READY}}$ output inactive delay from CLK2↑		20		ns
t121	ATSCLK period		125		ns
t122	ATSCLK low time		62		ns
t123	ATSCLK high time		62		ns
t124	ATSCLK rise time			8	ns
t125	ATSCLK fall time			8	ns
t126	ALE delay from ATSCLK (↑ or ↓)		5		ns
t127	$\overline{\text{XIOR}}$, $\overline{\text{XMEMR}}$, $\overline{\text{INTA}}$ active delay from ATSCLK (↑ or ↓)		10		ns
t128	$\overline{\text{XIOR}}$, $\overline{\text{XMEMR}}$, $\overline{\text{INTA}}$ inactive delay from ATSCLK↑		10		ns
t129	IOCHRDY set-up time to ATSCLK↑		17		ns

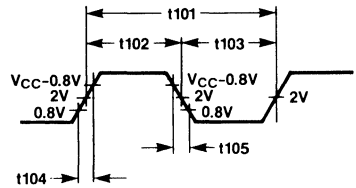
82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

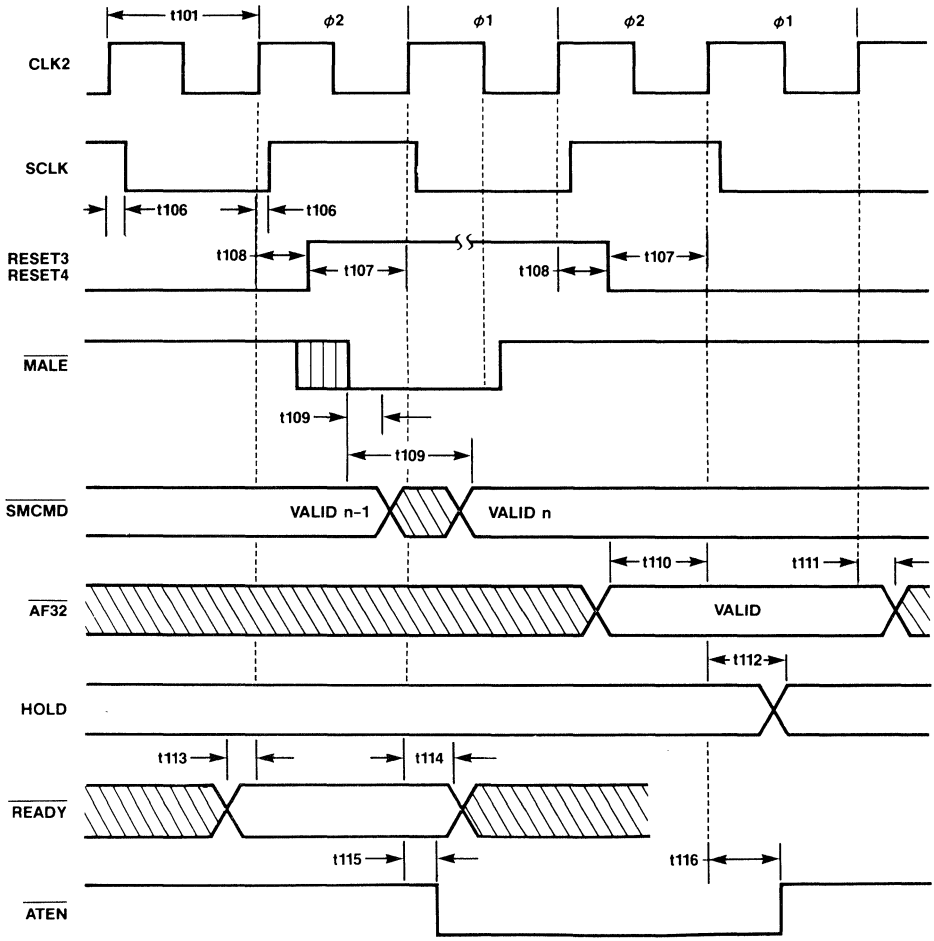
Sym	Description	Min.	Typ.	Max.	Units
t130	IOCHRDY hold time to ATSCLK↓	0			ns
t131	$\overline{MCS16}$, $\overline{IOCS16}$ set-up time to ATSCLK↑	35			ns
t132	$\overline{MCS16}$, $\overline{IOCS16}$ hold time from ATSCLK↓		25		ns
t133	$\overline{MCS32}$, $\overline{IOCS32}$ set-up time to ATSCLK↑	35			ns
t134	$\overline{MCS32}$, $\overline{IOCS32}$ hold time from ATSCLK↓		25		ns
t135	XA00, XA01, $\overline{SBHE}$ active delay from ATSCLK↓		20		ns
t136	XA00, XA01, $\overline{SBHE}$ inactive delay from ATSCLK↓		10		ns
t137	$\overline{ACEN}$ active delay (read cycle) from ATSCLK↓		20		ns
t138	$\overline{ACEN}$ inactive delay (read cycle) from ATSCLK↑		10		ns
t139	AC<3:0> active delay from ATSCLK↑		20		ns
t140	AC<3:0> inactive delay from ATSCLK↓		10		ns
t145	$\overline{XMEMR}$, $\overline{XMEMW}$ active delay from ATSCLK↑ (with zero command delay)		15		ns
t146	$\overline{ACEN}$ active delay (write cycle) from ATSCLK↑		10		ns
t147	$\overline{ACEN}$ inactive delay (write cycle) from ATSCLK↓	0			ns
t148	$\overline{0WS}$ set-up time to ATSCLK↓		17		ns
t149	$\overline{0WS}$ hold time from ATSCLK↑	0			ns
t151	$\overline{NMICS}$ set-up time to $\overline{XIOW}$ active	20			ns
t152	$\overline{NMICS}$ hold time from $\overline{XIOW}$ inactive	20			ns
t153	Data (XD7) set-up time to $\overline{XIOW}$ inactive	30			ns
t154	Data (XD7) hold time from $\overline{XIOW}$ inactive	20			ns
t155	NMI delay from $\overline{XIOW}$ inactive		25		ns
t156	$\overline{PORTBCS}$ set-up time to $\overline{XIOR}$, $\overline{XIOW}$ active	20			ns
t157	$\overline{PORTBCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive	20			ns
t158	Data (XD<7:0>) valid delay from $\overline{XIOR}$ active	15			ns
t159	Data (XD<7:0>) hold time from $\overline{XIOR}$ inactive	15			ns
t160	$\overline{IO2XCS}$ set-up time to $\overline{XIOR}$, $\overline{XIOW}$ active		10		ns
t161	$\overline{IO2XCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive		15		ns
t162	$\overline{LPAR}$, $\overline{IOCHK}$, $\overline{PFAIL}$ pulse width		15		ns
t165	REFREQ pulse width	15			ns

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

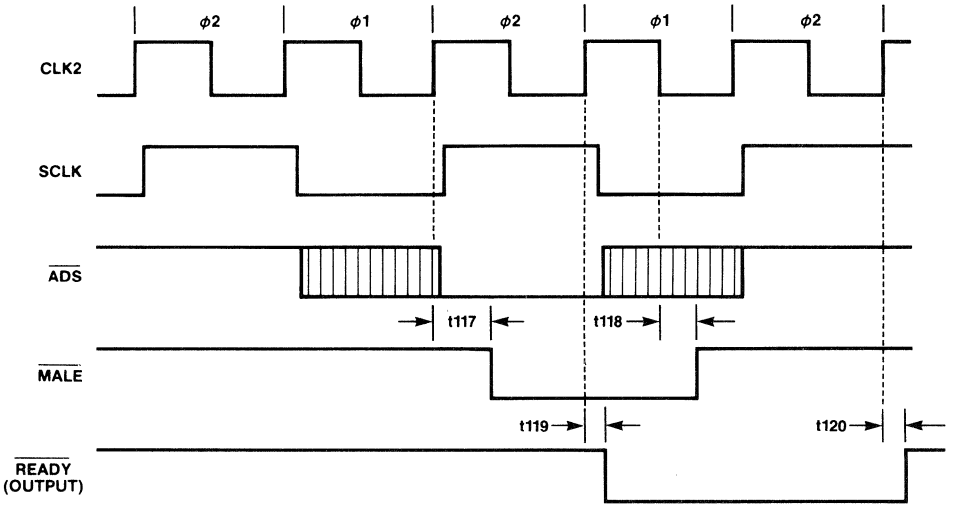
Sym	Description	Min.	Typ.	Max.	Units
t166	$\overline{REF}$ set-up time to ATSCLK↑		10		ns
t167	$\overline{XMEMR}$ active delay (refresh cycle) from ATSCLK↑		15		ns
t168	$\overline{XMEMR}$ inactive delay (refresh cycle) from ATSCLK↑		15		ns
t169	IOCHRDY set-up time (refresh cycle) to ATSCLK↑	25			ns
t170	IOCHRDY hold time (refresh cycle) from ATSCLK↑	0			ns
t171	$\overline{BE}$<3:0> active delay from XA0, XA1, $\overline{XBHE}$ valid		15		ns
t172	$\overline{BE}$<3:0> inactive delay		15		ns
t173	$\overline{SMCMD}$ active delay from $\overline{XMEMR}$, $\overline{XMEMW}$ active		20		ns
t174	$\overline{SMCMD}$ inactive delay from $\overline{XMEMR}$, $\overline{XMEMW}$ inactive		20		ns
t175	$\overline{ACEN}$ active delay from HLDA1 active		20		ns
t176	$\overline{ACEN}$ inactive delay from HLDA1 inactive		20		ns
t177	AC<3:0> active delay from XA0, XA1, $\overline{XBHE}$ not valid		TBD		
t178	AC<3:0> inactive delay from XA0, XA1, $\overline{XBHE}$ valid		TBD		
t179	AC<3:0> active delay from $\overline{XMEMR}$ active		TBD		
t180	AC<3:0> inactive delay from $\overline{XMEMR}$ inactive		TBD		

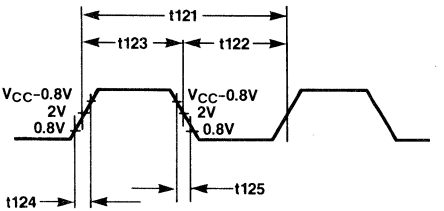
82C301 TIMING DIAGRAMS



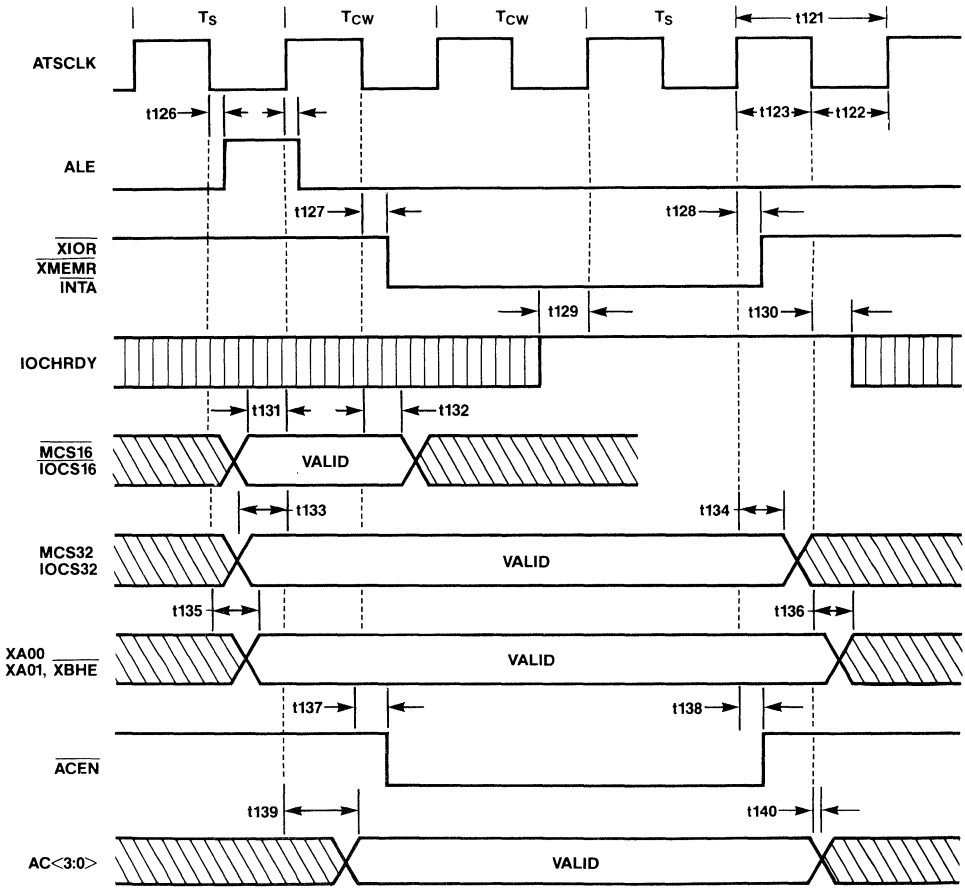


82C301 TIMING DIAGRAMS





82C301 TIMING DIAGRAMS



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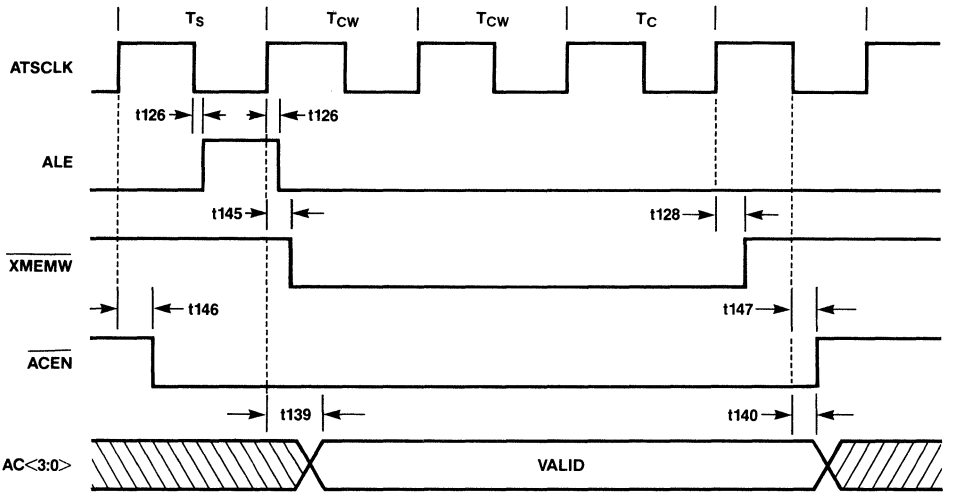
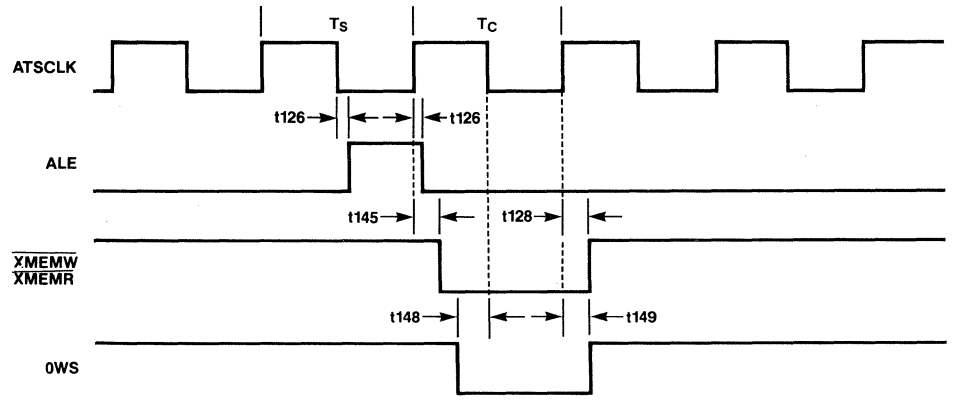
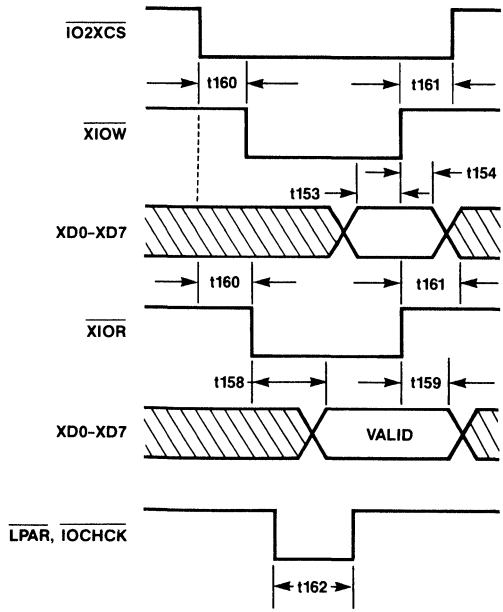
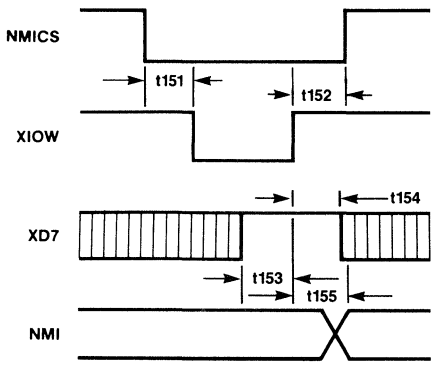
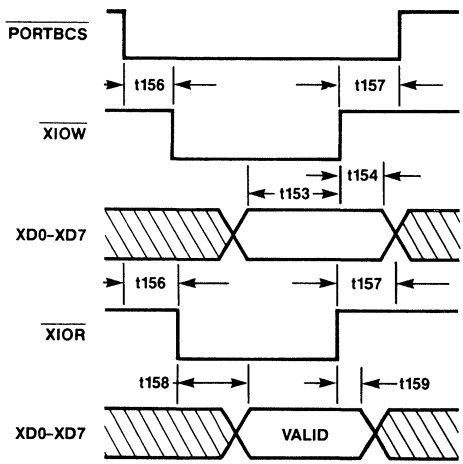




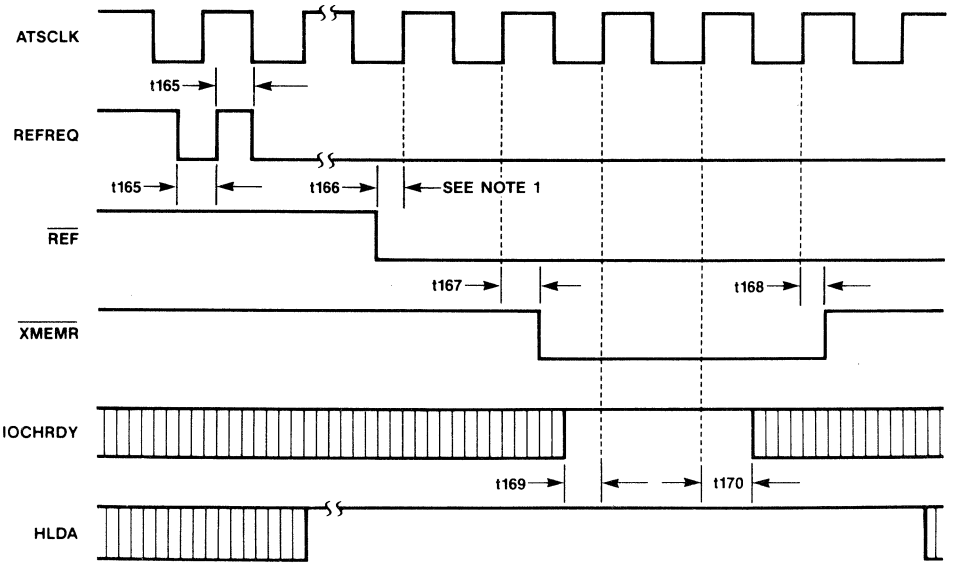
82C301 TIMING DIAGRAMS





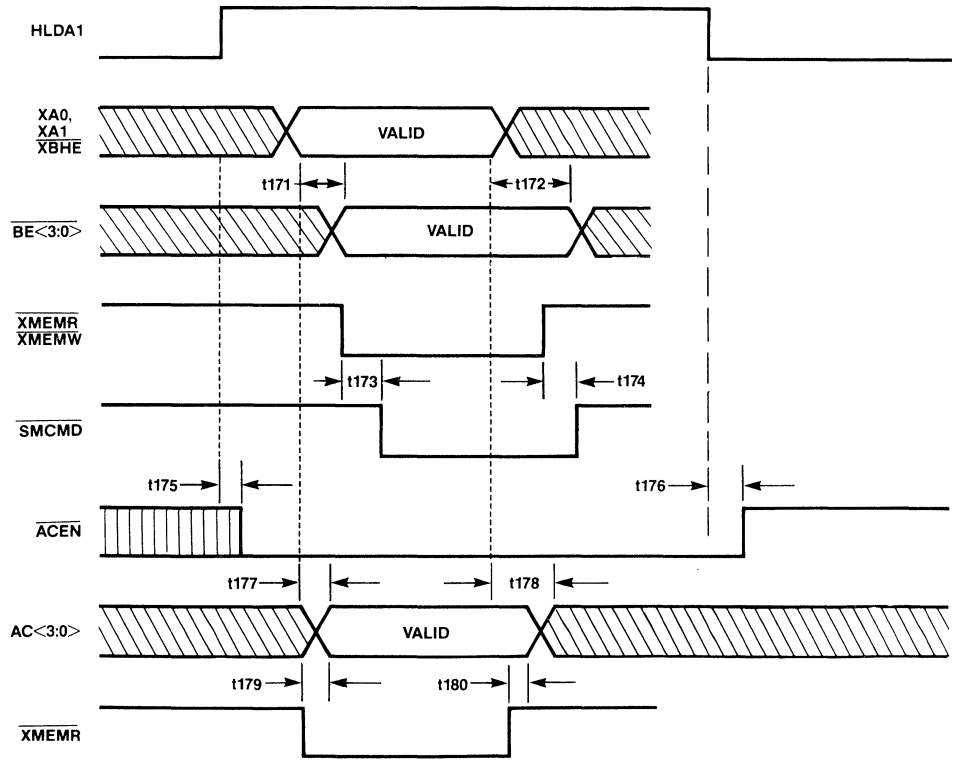


82C301 TIMING DIAGRAMS



NOTE
REF is an asynchronous signal and the setup time is specified only to guarantee starting a refresh cycle on that clock cycle instead of next one.

82C301 TIMING DIAGRAMS



82C302 PAGE/INTERLEAVE MEMORY CONTROLLER

- Page mode access with interleaved memory banks achieves higher performance than conventional DRAM arrays.
- Zero wait state access at 16MHz using 100nS DRAMs.
- Minimum configuration of 1 bank of 36 bits, 1MB using 256K *x* 1 or 4MB using 1M × 1 DRAMs.
- Maximum configuration of 4 banks of 36 bits, 4MB using 256K × 1 or 16MB using 1M × 1 DRAMs.
- Memory configurations of 1, 2 and 4 banks.
- Staggered refresh to reduce power supply noise.

OVERVIEW

The 82C302 performs the memory control functions in a 80386-based systems that utilizes page mode access DRAMs. The memory configurations can be one bank (non-interleaved) or multiple banks (2 or 4) interleaved on 2KB-page basis.

Array Configuration

The 82C302 organizes memory as banks of 36 bits consisting of 32 bits of data and 4 bits of parity. A common design may use either 36 by-1 DRAMs or 8 by-4 and 4 by-1 DRAMs. The minimum configuration can be a single bank operating in non-interleaved mode or can be one to two pairs of banks operating in two-way page interleaved mode at higher performance.

The memory controller is designed such that the memory can be up-graded from one to two banks by making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair due to the interleaved configuration. However, each pair of banks can use different DRAM types. with one or two banks of smaller DRAM types and later upgraded with additional pairs of banks of larger DRAMs.

Page Interleaved Operation

The 82C302 uses a page interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses in the other. If accesses are sequential (or at least to alternating even and odd addresses) the RAS precharge time of one set can be overlapped with the access time of the second set. Typically the hit rate (fraction of times that the required bank is available) is 50%. This is especially true since operand accesses (which tend to be more random) can be interspersed with (most likely sequential) instruction fetches.

Page mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256K × 1) that are subsequently selected using the column address. Once a row access has been made higher speed random access can be made to any bit (1 of 512) within the row. The page mode access and cycle times are typically half that of the normal access and cycle times respectively. If 36 256K × 1 DRAMs are used to implement a bank, a page would have 512 × 4 bytes = 2KB. Thus memory could be interleaved on a 2KB page rather than 4B basis. Any access to the currently active RAS page would occur in the page access rather than the normal access time and any subsequent access could be to anywhere in the same 2KB without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving. There are two reasons for this:

— The page mode access is faster than the normal access time. This permits more relaxed timing in order to achieve the same 0 wait-state "hit" access.

— The frequency of the next access being fast (same or alternate page vs. alternate address in interleaved mode) is significantly higher. This is because of the principle of locality of reference, instructions and data tend to be clustered together.

However, the complexity is somewhat higher in the page mode controller, making VLSI an ideal implementation vehicle.

FUNCTIONAL DESCRIPTION

The 82C302 performs four major functions as shown in figure 2-1:

- DRAM memory access arbitration
- DRAM memory access cycle control
- DRAM refresh
- Memory mapping

Memory Access State Machines and Arbitration

The 82C302 controls the DRAM memory access from three sources: CPU, DMA, and refresh requests. These accesses are arbitrated based on the inputs HLDA1 and REF and are handled by three state machines controlling each type of accesses. The CPU cycle state machine controls the memory operation for CPU accesses, the DMA cycle state machine for DMA accesses, and the refresh cycle state machine controls the DRAM refresh operation.

The refresh state machine is in control whenever REF is active. When HLDA1 is active the DMA state machine is in control. In all other cases, the CPU state machine is in control for valid DRAM memory accesses as defined by the memory map in the configuration registers. The arbitration is not preemptive in that the current active state machine always runs to completion before relinquishing the control. Therefore, it is possible for the HLDA1 with active XMEMW or XMEMR to prevent refresh cycles to take place.

CPU Access State Machine

The CPU initiated accesses are decoded according to the memory map defined in the configuration registers. These are the only accesses that uses the page mode operation of the DRAMs. The 82C302 maintains four page registers storing the page addresses of the most recently accessed DRAM pages of the two-way page-interleaved banks. These four registers are called active page registers. Accesses to the active pages are called "hits" and are faster because the DRAM is operated in the page mode with the RAS staying asserted.

The 82C302 supports memory configurations with either one, two, or four banks. Since one active register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration only one active page register is in use. For each active page register in use, the corresponding RAS stays asserted after the previous access. If an access does not hit any active pages, a "miss" cycle, normal DRAM access cycle is entered by first de-asserting the RAS associated with the bank accessed. Refer to the timing diagram for the timing sequence for each of these cases.

RAS and CAS Generation

The 82C302 is based on 2K byte page-interleaved organization. To maintain this organization, the following table shows the address lines used for the different organizations:

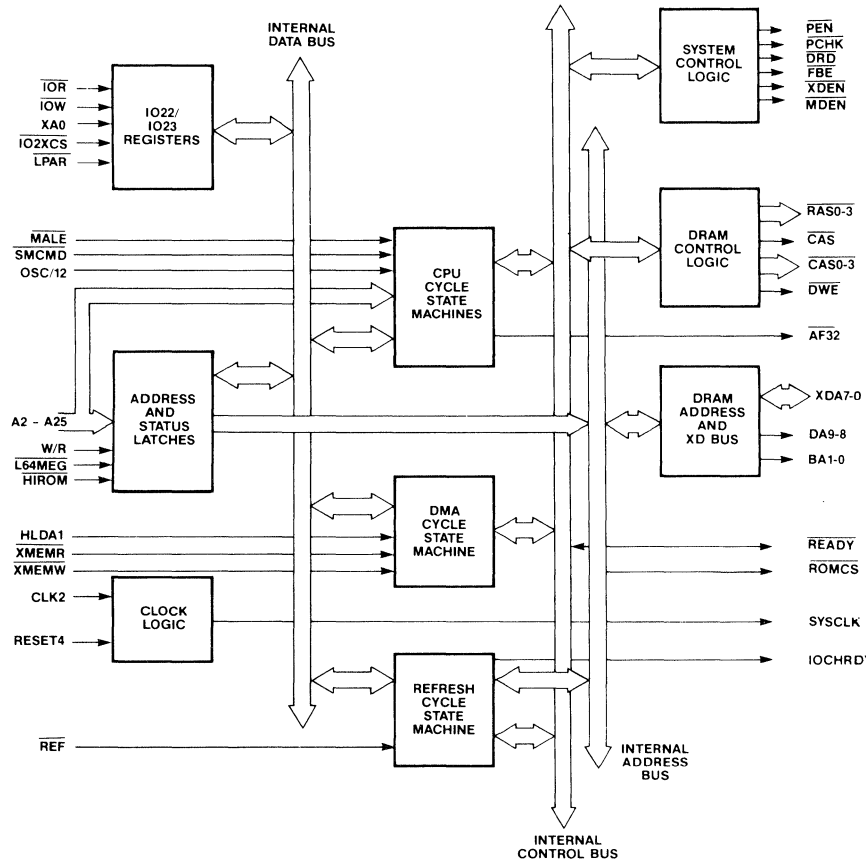


Figure 2-1. 82C302 Functional Block Diagram

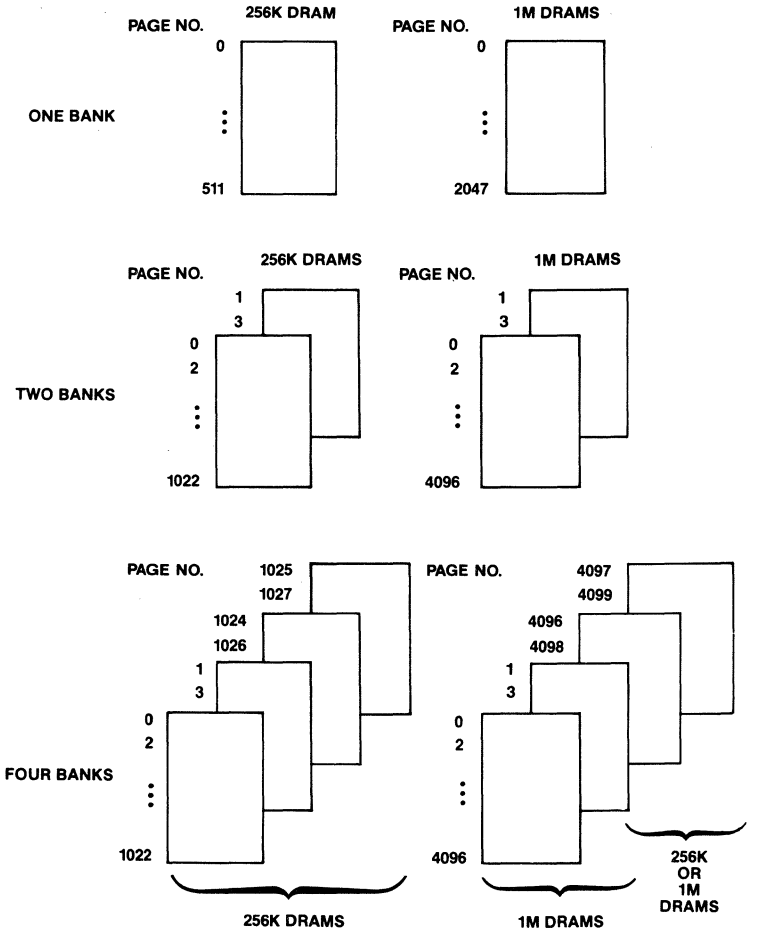


Figure 2-2. Memory Addressing

For non-interleaved operation (one bank only):

	Row	Column
256K DRAM's	A<19:11>	A<10:2>
1M DRAM's	A<21:12>	A<11:2>

For interleaved memory(two or four banks):

	Row	Column
256K DRAM's	A<20:12>	A<10:2>
1M DRAM's	A<21:12>	A<22>, A<10:2>

Table 2-1. Row and Column Address Definition

In interleaved memory cases bit A<11> determines which one of the even page banks or odd page banks is accessed in the two-way interleaved organization. For configurations using only 256K DRAM's, A<11> and A<21> are used to control RAS<3:0>; and for 1M DRAM only configurations A<11> and A<23> are used. When 256K and 1M DRAMs are used, it is required that the 1M DRAMs occupy the first two-banks and the 256K DRAMs occupy the second two-banks. This constrain is there to ensure that the there will not be a hole in the address space without actual DRAM's. Figure 2-2 shows the memory addressing scheme for the allowable memory configurations.

RAS Timeout

When using DRAM page mode, the maximum RAS pulse width must be observed. For most DRAMs this is 10 microseconds (although some have 30 or 100 microsecond limits). Timers are maintained for each bank to assure data integrity using the OSC/12 (1.19MHz = 840nS) clock available on the system board. RAS is de-asserted for each bank when its counter times out at about 10 microseconds intervals. The configuration register bit REG13H<7> can be programmed to set desired RAS time out intervals.

CPU Access Cycles Sequences

There are many basic CPU memory access patterns: memory read-hit access, memory write-hit access, memory read-miss access, and memory write-miss access, and CPU IO access to 82C301 configuration registers. These basic access sequences and timing for the critical signals are shown in the timing charts. In addition to these basic patterns, the configuration register REG13H<6> may be programmed to have one wait state inserted for supporting slow DRAM's. Note that the default setting after the system reset is for one wait state insertion.

DMA Access State Machine

DMA accesses are initiated by asserting HLDA1. The XMEMR an XMEMW determines if it is a read or a write memory access. The bytes accessed are controlled externally with the BE<3:0> signals generated by the 82C301 Bus Controller. The DMA state machine makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers. Refer to the timing charts for a DMA access cycle sequence and timing.

Dynamic RAM Access Logic

The DRAM control logic generates the necessary RAS, CAS and DWE signals for all DRAM acesses. CPU, DMA, and refresh access cycles use DA<9:8> and XDA<7:0> and bank select signals BA<1:0>. (Note that in the current version of 82C302, the signals BA<1:0> default to zero.) The system control logic provides MDEN to control the buffer chips. MDEN enables data buffers for MD bus in 82A305's for non-refresh DRAM access cycles.

Refresh Cycles

To reduce power supply noise generation due to the surges caused during RAS transitions, RAS pulses to each bank are staggered by one CLK2 cycle, as shown in Figure 2-3. Because all RAS's could be active for page mode operation, a refresh cycle requires that all RAS's be first de-asserted then asserted with the correct refresh address.

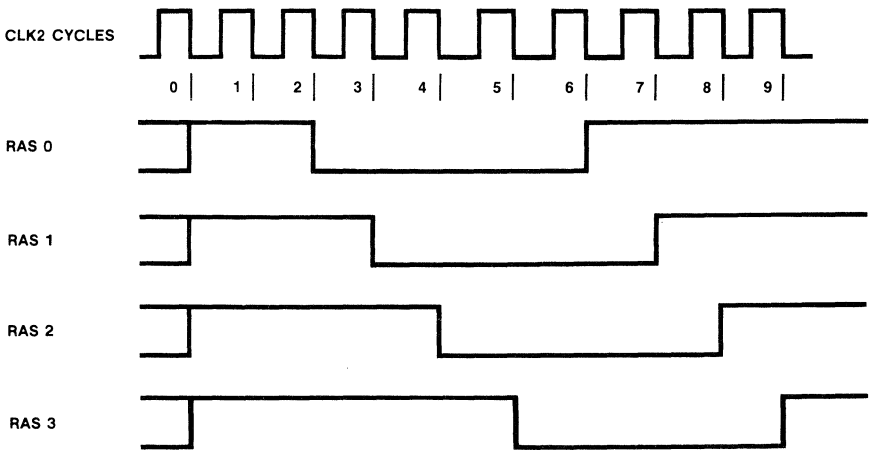


Figure 2-3. Staggered RAS pulses during refresh

Memory Mapping Logic

The configuration registers REG08H to REG13H define what is a valid local memory access, and what is a ROM memory access according to the local bus addresses. REG08H and REG09H determines how ROM areas (as defined by an IBM PC AT) between 768K to 1M address range are accessed.

For valid local memory accesses it asserts the AF32 to indicate that it has control of the local bus and also asserts the READY signal at the end of the access cycle. If an access is a ROM access, it asserts ROMCS to provide controls for the ROM's or PROM's; in this case, the READY signal must be provided to the CPU and 82C302 by another source (82C301 will provide this signal in a chip set solution).

Clock, Reset and Other Miscellaneous Logic

The RESET4 input causes all internal registers to be reset to their default values. Configuration registers not specified with a default value is not reinitialized and may not retain its old value. The system control logic generates the PCHK and PEN signals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

There are 14 bytes of configuration and diagnostic registers in the 82C302. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. Accesses to these configuration and diagnostic registers are done first by writing the index of the desired register into port 22H and then followed by an access (either read or write) to 23H for the data. XDEN is asserted for these accesses to control the buffer connecting the XD and XDA buses.

Memory Configuration Registers

The configuration registers REG08H to REG0FH are used to control how the CPU memory accesses are defined. They define all address as ROM accesses, system memory accesses (or DRAM accesses for short), other local CPU bus accesses, or as IO channel accesses . These provisions are made because the low one megabyte is both occupied by DRAM's, ROM's and also devices on the AT bus. For ROM accesses it generates the ROMCS to control the PROM access;for system memory accesses it generates the necessary DRAM controls to the system memory

under its control; it generates $\overline{AF32}$ for all other local CPU bus accesses; and it does not control the IO channel accesses.

The 82C301 provides three 256KB areas where the ROM's can be located. The low ROM space is located just below the 1MB address, the middle ROM space is located below 16MB address, and the high ROM space is below 4GB address. The low ROM is used for 8086 compatible operation, the middle ROM is for 80286, and the high ROM is for 80386. Upon system reset, the default configuration register setting causes accesses to these three ROM areas to generate $\overline{ROMCS}$. With the exception of the high ROM area which is always recognized as ROM accesses, the other two ROM areas can be mapped to be either ROM or RAM accesses.

After reset, REG08<4:3> may be programmed to make the entire middle ROM area mapped to DRAM and with write protection if desired. REG08H<2> determines if the 82C301 recognizes the addresses generated beyond 16 MB as local CPU bus cycles. REG08H<1> is used to enable REG0AH to REG0FH which controls the "Low Meg DRAM" (40000H to FFFFFH) address mapping for 256KB to 1MB addresses in 16 KB blocks. This bit defaults upon reset so that only the 0 to 256KB areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed. REG08H<0> defaults to single bank memory configuration upon reset and must be programmed to enable page/interleaved operation.

The REG09H control the address mapping and write protection for the low ROM area (from C0000H to FFFFFH) in 64KB blocks. REG0AH to REG0FH define for each 16 KB address range if it is a DRAM block in the system memory or on the IO channel.

INDEX	7	6	5	4	3	2	1	0	
08H	0	VERS		MW	MR	HM	SM	NI	IDENTIFICATION
09H	R3	R2	R1	R0	D3	D2	D1	D0	ROM CONFIGURATION
0AH	368K						256K		MEMORY ENABLE (16KB RESOLUTION)
0BH	496K						384K		•
0CH	624K						512K		•
0DH	752K						640K		•
0EH	880K						768K		•
0FH	1008K						896K		MEMORY ENABLE (16KB RESOLUTION)

Figure 2-5. Control and Address Space Map Register Summary

Index	Bits	Function
08H		Identification
	7	Controller Type Part type
		0 Interleaved Memory Controller (82C302)
	6:5	Version
		0 Initial
	4	MW - Middle Boot Space Write Protect. This bit is used in conjunction with bit 3 allowing the BIOS code to be copied into RAM and write protected at this location as well as below 1MB. It should only be used if there is RAM present at this address (16MB installed). Executing out of RAM will result in better performance than out of narrower (usually 8 or 16 bits) EPROMs.
		0 Read/Write of 256KB RAM at 16128K 00FC0000H. Default. 1 Read-Only of 256KB RAM at 16128K 00FC0000H
	3	MR - Middle Boot ROM disable
		0 The boot/BIOS ROM located just below 16MB is enabled. This is necessary for 286 compatibility. Default. 1 The boot/BIOS ROM located just below 16MB is disabled.
	2	HM - 16MB IO Channel Memory Limit
		0 $\overline{AF32}$ will not be asserted for addresses $\geq$ 16MB. This should only be used if external logic can recognize addresses above 16MB. Default. 1 $\overline{AF32}$ is asserted for addresses $\geq$ 16MB (01000000H). Since IO channel memory cannot normally be configured above 16MB, accessing above 16MB will cause a READY timeout if that feature is enabled. This is necessary during setup because memory address above 16MB that are not enabled for local memory could wrap into a valid IO channel memory location.
	1	SM - Minimum memory configuration after reset. Used during initialization.
		0 256K only enabled. Default. Ignore memory address configuration registers 0AH to 0FH. 1 Normal configuration controlled by registers 0AH to 0FH.
	0	NI - Single bank/interleave select 0 Disable interleave (single bank). Default. 1 Enable interleave

Table 2-2. Memory Configuration Register Definition

Index	Bits	Function
09H		RAM/ROM Configuration in boot area.
	7	RAM at 768K C0000-CFFFFH (EGA)
	6	RAM at 832K D0000-DFFFFH
	5	RAM at 896K E0000-EFFFFH
	4	RAM at 960K F0000-FFFFFH (BIOS)
		Bits 7:4 disable writing to RAM located in the BIOS area in 64KB blocks. BIOS data.
		0 Read/Write. Default. 1 Read-Only
	3	ROM at 768K C0000-CFFFFH (EGA)
	2	ROM at 832K D0000-DFFFFH
	1	ROM at 896K E0000-EFFFFH
	0	ROM at 960K F0000-FFFFFH (BIOS)
		Bits 3:0 enable substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks. This should be done after the BIOS code is copied from the ROM and the RAM locations have been write protected using bits 7:4.
		0 Disabled 1 Enabled. Default.
0AH		Address Map 256K 040000-05FFFFH (16K Resolution)
0BH		Address Map 384K 060000-07FFFFH
0CH		Address Map 512K 080000-09FFFFH
0DH		Address Map 640K 0A0000-0BFFFFH
0EH		Address Map 768K 0C0000-0DFFFFH
0FH		Address Map 896K 0E0000-0FFFFFH
		0 Address is on or controlled by the system board 1 Address is on the IO Channel.
		This permits 16K blocks of memory to be disabled allowing ROMs, memory expansion mechanisms (EMS or XMA) or memory mapped IO devices to reside within the lower 1MB address space.

Table 2-2. Memory Configuration Register Definition (Continued)

DRAM Array Configuration and Timing

The configuration registers REG10H to REG13H provides the DRAM type definition and starting address for each pair of banks, banks 0 and 1, and banks 2 and 3. The REG10H<7:6> and REG12H<7:6> defines if the DRAM's are enabled, uses 256K DRAM's, or uses 1M DRAM's. These bits defaults to 256K DRAM's upon reset. The REG10H<6:0> and REG12H<6:0> defines the address bits <25:20> of the starting address of the pairs of banks. Some of these bits may not be valid because the memory banks must start at some predefined boundaries. For 256K DRAM's, all bits <25:20> are valid if only single bank is enabled-it can be on any 1MB boundary; otherwise only bits <25:21> are valid starting address bits on 2MB boundaries. For 1M DRAM's, only bits <25:23> are valid forcing it on 8 MB boundaries. The REG11H<7> and REG13H<7> define the RAS precharge time required when a page miss occurs so that DRAM's of different speeds can be supported for each pair of banks. The REG11H<6> and REG13H<6> define the wait state to be inserted to meet the DRAM speed. These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions on the DRAM speed and the memory configuration. Refer to Table 2-3 for details of the bit definitions.

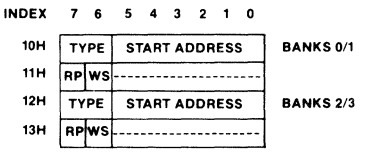


Figure 2.6. DRAM Configuration/Timing Register Summary

Index	Bits	Function
10H		bank 0/1 Type/Start Address
12H		bank 2/3 Type/Start Address
	7:6	DRAM Type
		0 none (bank disabled)
		1 256K words, default value for REG10H and REG12H
		2 1M words
		3 Reserved
	5:0	Starting Address 25:20 The DRAM type determines which address bits are valid in the address recognition process. This field of REG10H defaults to zero after reset.
		25:20 256K DRAM's. 1MB boundary 1MB per bank, single bank only. Valid for the first register only.
		25:21 256K DRAM's. 2MB boundary 1MB per bank, two banks required for interleaved operation.
		25:23 1M DRAM's. 8MB boundary 4MB per bank, two banks required for interleaved operation.

Table 2-3. DRAM Configuration and Timing Register Definition

Index	Bits	Function
11H		banks 0/1 Timing
13H		banks 2/3 Timing
	7	DRAM RAS precharge. Specifies the amount of time for RAS precharge when a page miss occurs. 0 3 CLK2 times (93 nS at 16MHz) 1 5 CLK2 times (155nS at 16MHz). Default.
	6	Access wait states Specifies the number of wait states in SCLK units to allow the use of slower DRAMs. 0 0 wait-states 1 1 wait-states. Default.
	5:0	Reserved

Table 2-3. DRAM Configuration and Timing Register Definition (Continued)

Diagnostic Access Register

REG28H<7> controls the parity check enable and defaults to "disable" after reset. This bit generates the $\overline{\text{PEN}}$ signal for enabling the parity check by 82A306. When parity errors occur REG28H<1:0> and REG29H<7:0> will latch the error address <25:16>.

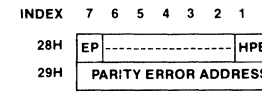


Figure 2.7. Diagnostic Access Register Summary

Index	Bits	Function
28H		Error Source/Address (MSBs)
	7	Parity check disable 0 Enabled 1 Disabled
	6:2	Not used, returns unpredictable value.
	1:0	High Parity Error Address bits <25:24>
29H		Parity Error Address (LSBs)
	7:0	Error address bits <23:16>

Table 2-4. Diagnostic Access Registers Definition

82C302 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C302 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C302 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTE:
1. SYSCLK, $\overline{DWE}$, $\overline{RAS}$<3:0>, $\overline{CAS}$, $\overline{CAS}$<3:0> have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all $I_{OL} = I_{OH}$ for the pin.

82C302 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t200	CLK2 input cycle time (t0 used as reference)	31		42	ns
t201	CLK2 fall time	2		5	ns
t202	CLK2 rise time	2		5	ns
t203	CLK2 low time	10			ns
t204	CLK2 high time	10			
t205	RESET hold time	6			ns
t206	RESET set-up time	5			ns
t207	SCLK delay time	6	12	22	ns
DMA Sequence					
t210	$\overline{RASi}$ de-assertion time from HLDA1		13		ns
t211	$\overline{RASi}$ active delay from commands active		16		ns
t212	Address set-up time to commands active	35			ns
t213	Address hold time from commands inactive	0			ns
t214	$\overline{AF32}$ active time from commands active		26		ns
t215	$\overline{DRD}$ active time from commands active	10			ns
t216	Row address set-up time to $\overline{RAS}$ active	10			ns
t217	Row address hold time from $\overline{RAS}$ active	0.5t0			ns
t218	$\overline{CASi}$ active delay from $\overline{RAS}$ active for DMA memory read cycle	1.0t0			ns
t219	$\overline{CASi}$ active delay from $\overline{RAS}$ active for DMA memory write cycle	1.5t0			ns
t220	$\overline{DWE}$ active delay from $\overline{RAS}$ active	0.5t0			ns
t221	$\overline{READY}$ active delay from $\overline{RAS}$ active	1.5t0			ns
t222	$\overline{RASi}$ de-assertion time from commands inactive		13		ns
t223	Column address hold time from commands active		29		ns
t224	$\overline{CASi}$ de-assertion from commands inactive		22		ns
t225	$\overline{AF32}$ tri-state delay from commands inactive		21		ns
t226	$\overline{DWE}$ de-assertion time from commands inactive		11		ns
t227	$\overline{READY}$ de-assertion time from commands inactive		16		ns
t228	$\overline{DRD}$ de-assertion time from commands inactive		12		ns

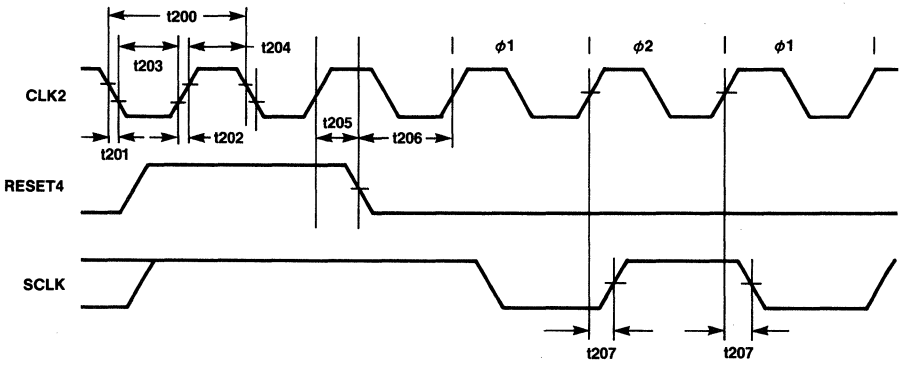
82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
ROMCS Sequence					
t235	$\overline{\text{ROMCS}}$ active delay from CLK2↑		27		ns
t236	$\overline{\text{ROMCS}}$ inactive delay from CLK2↑		22		ns
t237	$\overline{\text{READY}}$ input set-up time to CLK2↓	8			ns
t238	$\overline{\text{READY}}$ input hold time from CLK2↑	0			ns
Refresh Sequence					
t240	IOCHRDY going low from $\overline{\text{REF}}$ active		14		ns
t241	IOCHRDY floating from CLK2↑		18		ns
t242	$\overline{\text{RAS0}}$ precharge time		3t0		ns
t243	$\overline{\text{RASi}}$ (i = 0 to 3) pulse width		4t0		ns
t244	$\overline{\text{RAS(i+1)}}$ active delay from $\overline{\text{RASi}}$ active		1t0		ns
t245	Refresh address set-up time to $\overline{\text{RASi}}$		3t0		ns
t246	Refresh address hold time from $\overline{\text{RASi}}$		2t0		ns
t247	$\overline{\text{RASi}}$ inactive delay from CLK2↑		14		ns
t248	$\overline{\text{RASi}}$ active delay from CLK2↑		15		ns
IO Read/Write Sequence					
t250	$\overline{\text{IO2XCS}}$ set-up time to $\overline{\text{XIOR}}$↓ or $\overline{\text{XIOW}}$↓	10			ns
t251	XA0 set-up time to $\overline{\text{XIOR}}$↓ or $\overline{\text{XIOW}}$↓	10			ns
t252	$\overline{\text{IO2XCS}}$ hold time from $\overline{\text{XIOR}}$↑ or $\overline{\text{XIOW}}$↑	15			ns
t253	XA0 hold time from $\overline{\text{XIOR}}$↑ or $\overline{\text{XIOW}}$↑	15			ns
t254	$\overline{\text{XDEN}}$ active delay from $\overline{\text{XIOR}}$↓ or $\overline{\text{XIOW}}$↓		15		ns
t255	$\overline{\text{XDEN}}$ inactive delay from $\overline{\text{XIOR}}$↑ or $\overline{\text{XIOW}}$↑		12		ns
t256	XDA<7:0> input set-up time to $\overline{\text{XIOW}}$↑	10			ns
t257	XDA<7:0> input hold time to $\overline{\text{XIOW}}$↑	8			ns
t258	XDA<7:0> output valid delay from $\overline{\text{XIOR}}$↓		37		ns
t259	XDA<7:0> hold time from $\overline{\text{XIOR}}$↑		14		ns
CPU to Memory Sequence					
t260	$\overline{\text{MALE}}$ active set-up time to CLK2↑		TBD		
t261	$\overline{\text{MALE}}$ inactive delay from CLK2↓		TBD		
t262	Address/Status set-up time to CLK2↑		TBD		

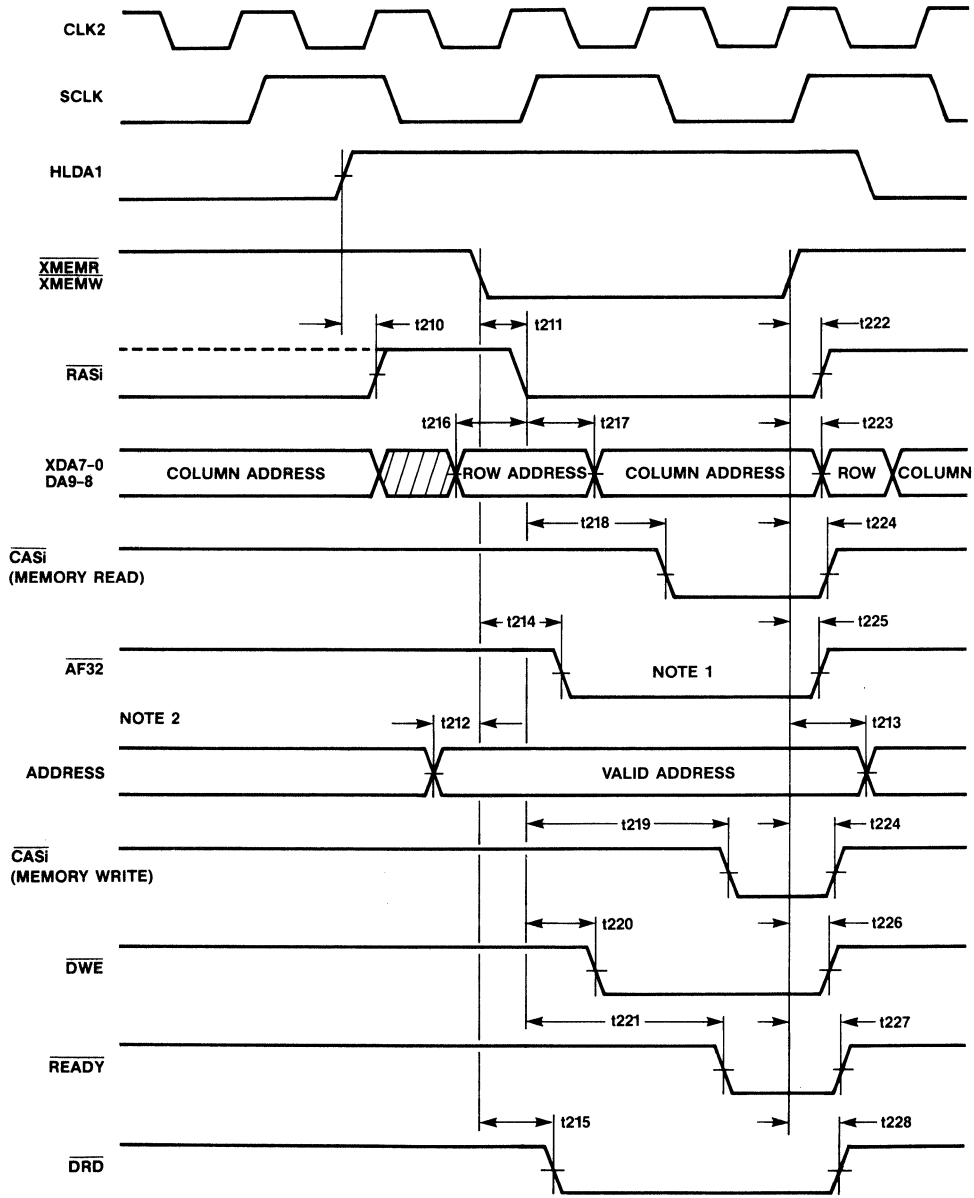
82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t263	Address/Status hold time from $\overline{\text{MALE}}$↑		TBD		
t264	$\overline{\text{L64MEG}}$, $\overline{\text{HIROM}}$ set-up time to CLK2↑		TBD		
t265	$\overline{\text{L64MEG}}$, $\overline{\text{HIROM}}$ hold time to $\overline{\text{MALE}}$↑		TBD		
t266	$\overline{\text{SMCMD}}$ active delay from $\overline{\text{MALE}}$↓		TBD		
CPU Cycle Timing					
t270	$\overline{\text{AF32}}$ active delay from CLK2↓		26		ns
t271	$\overline{\text{AF32}}$ inactive delay from CLK2↓		17		ns
t272	$\overline{\text{CASi}}$ active delay from $\overline{\text{MALE}}$↑ for read-hit cycle		19		ns
t273	$\overline{\text{CASi}}$ inactive delay from CLK2↑		16		ns
t274	$\overline{\text{CAS}}$ active delay from $\overline{\text{MALE}}$↑ for read-hit cycle		20		ns
t275	$\overline{\text{CAS}}$ inactive delay from CLK2↑		18		ns
t276	Column Address stable from $\overline{\text{MALE}}$↓		25		ns
t277	$\overline{\text{DRD}}$ active delay from CLK2↓		21		ns
t278	$\overline{\text{DRD}}$ inactive delay from CLK2↑		17		ns
t279	$\overline{\text{FBE}}$ active delay from CLK2↓		23		ns
t280	$\overline{\text{FBE}}$ inactive delay from CLK2↓		19		ns
t281	$\overline{\text{READY}}$ active delay from CLK2↑		20		ns
t282	$\overline{\text{READY}}$ inactive delay from CLK2↑		18		ns
t283	$\overline{\text{RASi}}$ active delay from CLK2↑		18		ns
t284	Row address set-up time to $\overline{\text{RASi}}$↓	10			ns
t285	Row address hold time from CLK2↑		12		ns
t286	$\overline{\text{CASi}}$ active delay from CLK2↑		17		ns
t287	$\overline{\text{CAS}}$ active delay from CLK2↑		18		ns
t288	$\overline{\text{RASi}}$ inactive delay from CLK2↑		17		ns
t289	$\overline{\text{RASi}}$ precharge time	3t0			ns
t290	$\overline{\text{CASi}}$ precharge time		1.5t0		ns
t291	$\overline{\text{DWE}}$ active delay from CLK2↑		16		ns
t292	$\overline{\text{DWE}}$ inactive delay from CLK2↑		17		ns

82C302 TIMING DIAGRAM (RESET SEQUENCE)



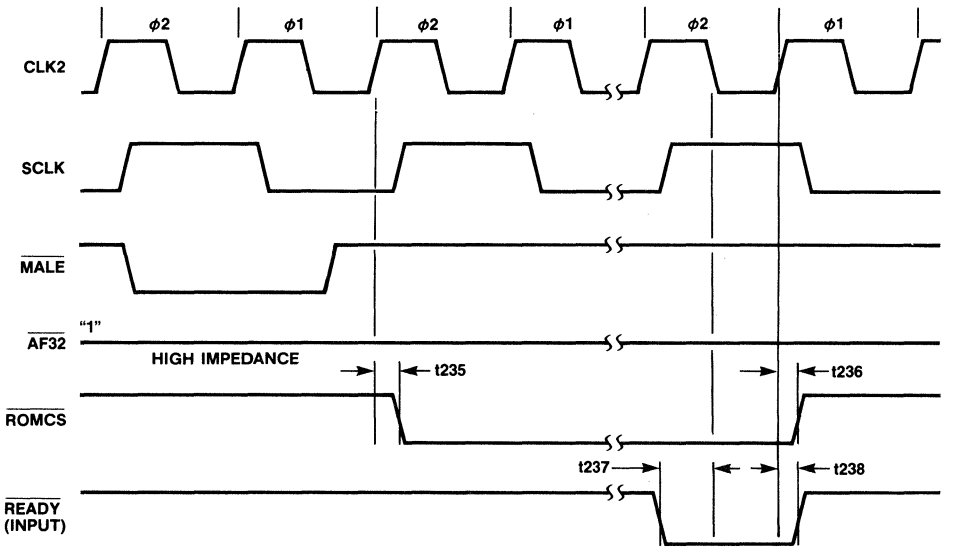
82C302 TIMING DIAGRAM (DMA CYCLES)



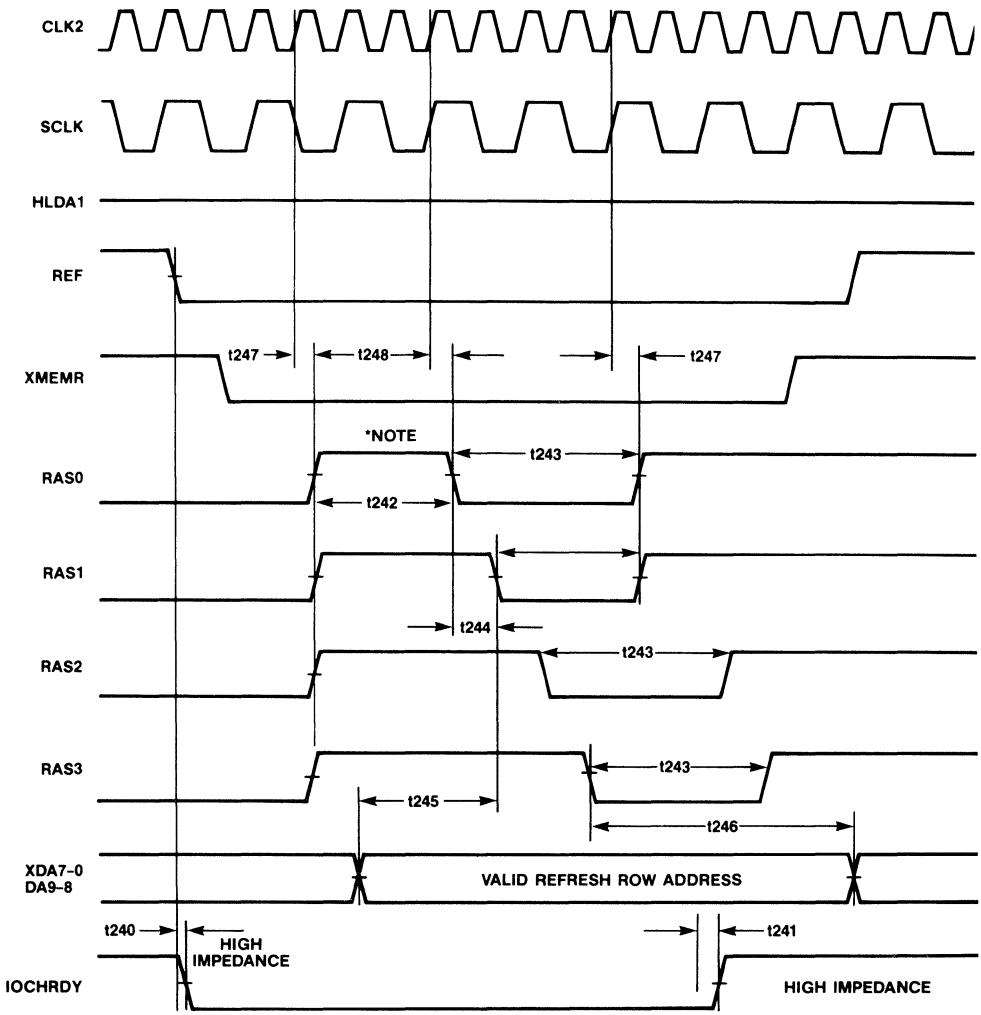
NOTE

1. During DMA cycles, only $\overline{\text{RASi}}$ will become active if $\overline{\text{AF32}}$ = 1 (not local memory)
2. The address includes $\overline{\text{L64MEG}}$ and $\overline{\text{HIROM}}$ input signals.

82C302 TIMING DIAGRAM (ROM READ CYCLE)

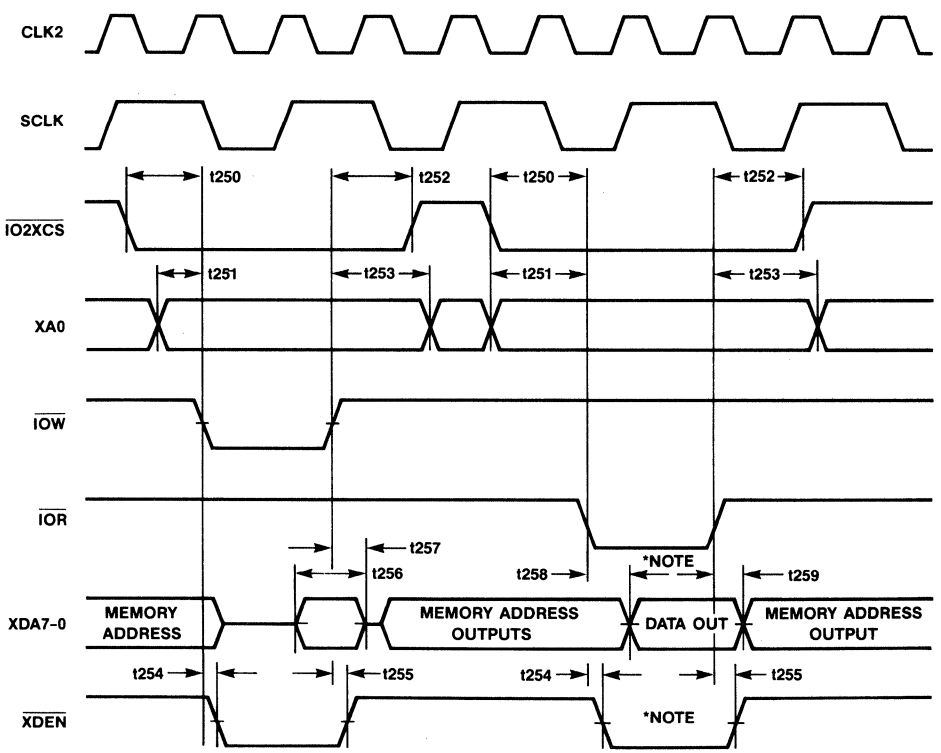


82C302 REFRESH CYCLE WAVEFORM



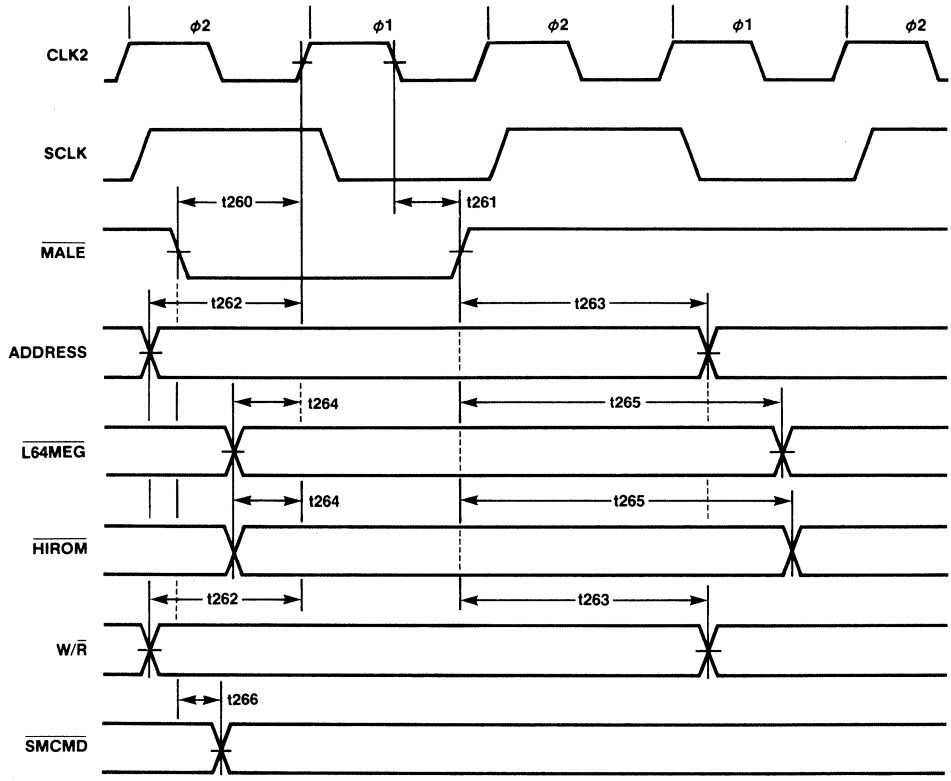
* **NOTE:** Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1.

82C302 TIMING DIAGRAM (IO READ/WRITE)

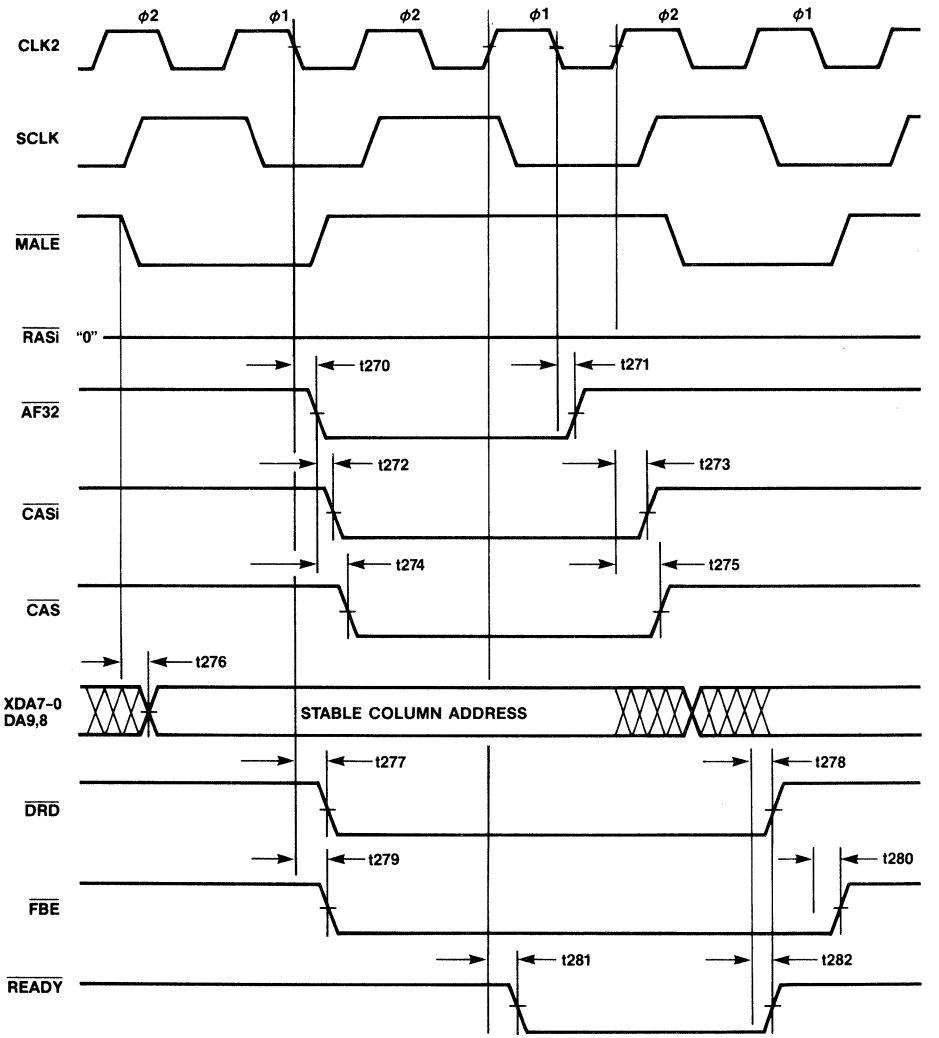


***NOTE:** No data output and XDEN is inactive if the index set up by the previous IO22 Write doesn't point to a valid IO23 register of 82C302.
Valid registers of IO23: 08H-0FH, 10H-13H, 28H-29H.

82C302 TIMING DIAGRAM (INPUT SETUP/HOLD TIME FOR CPU CYCLES)

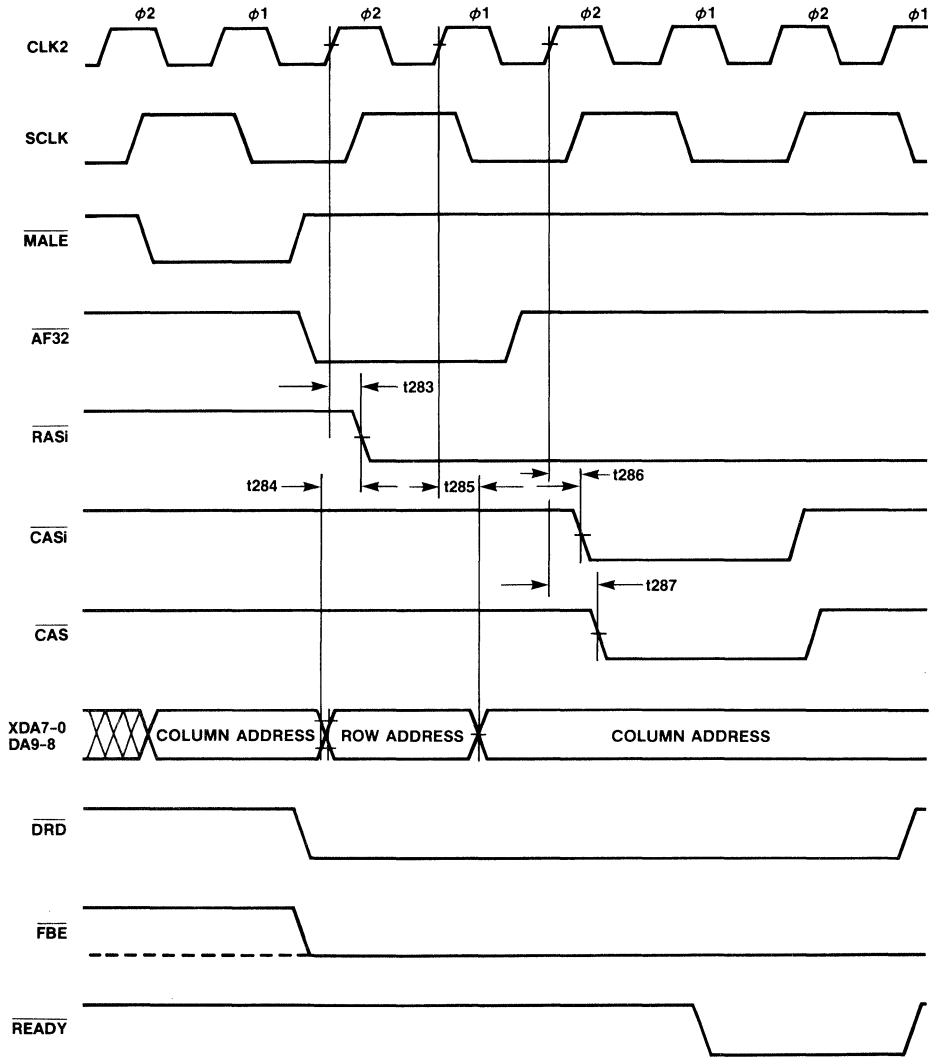


82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY CYCLE) READ HIT, ϕ WAIT STATE

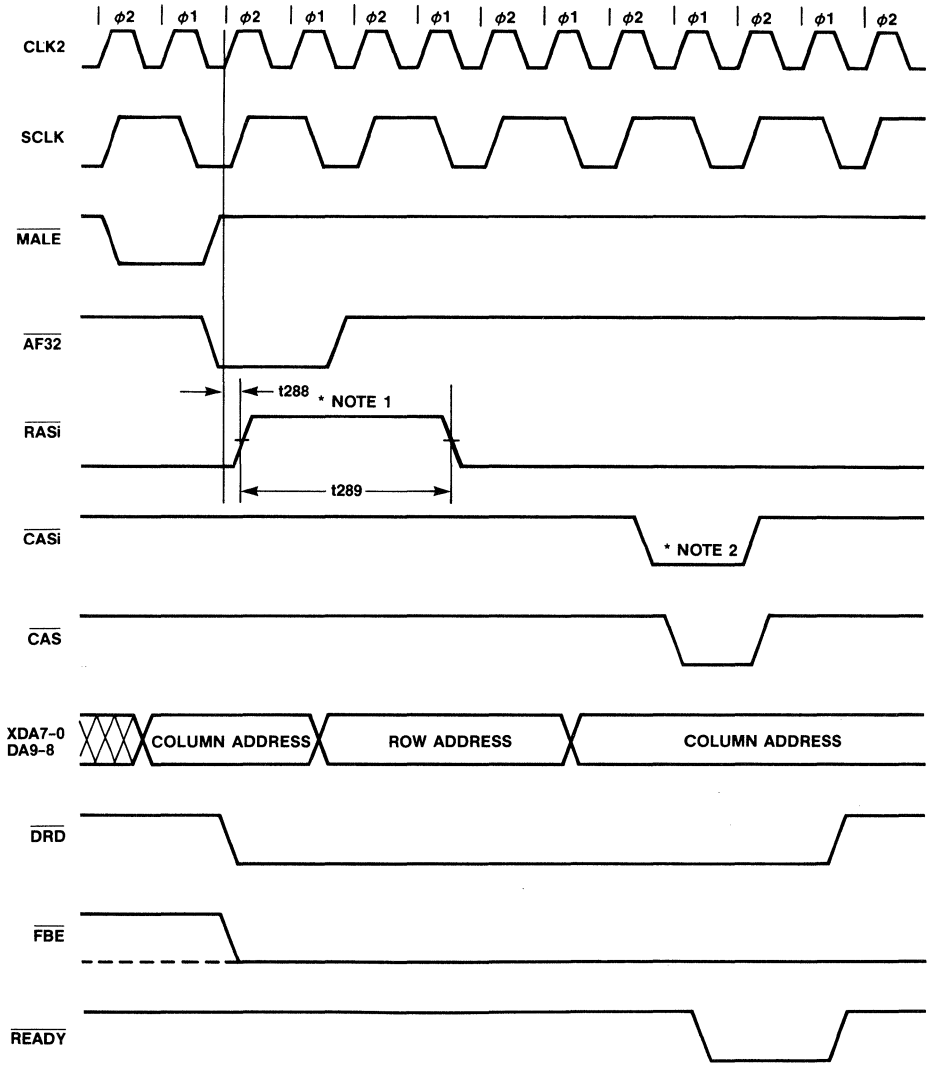


NOTE: Assume bit 6 of Register 11 (or 13) is programmed to "0".

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ CYCLE WITH RAS BEING INACTIVE



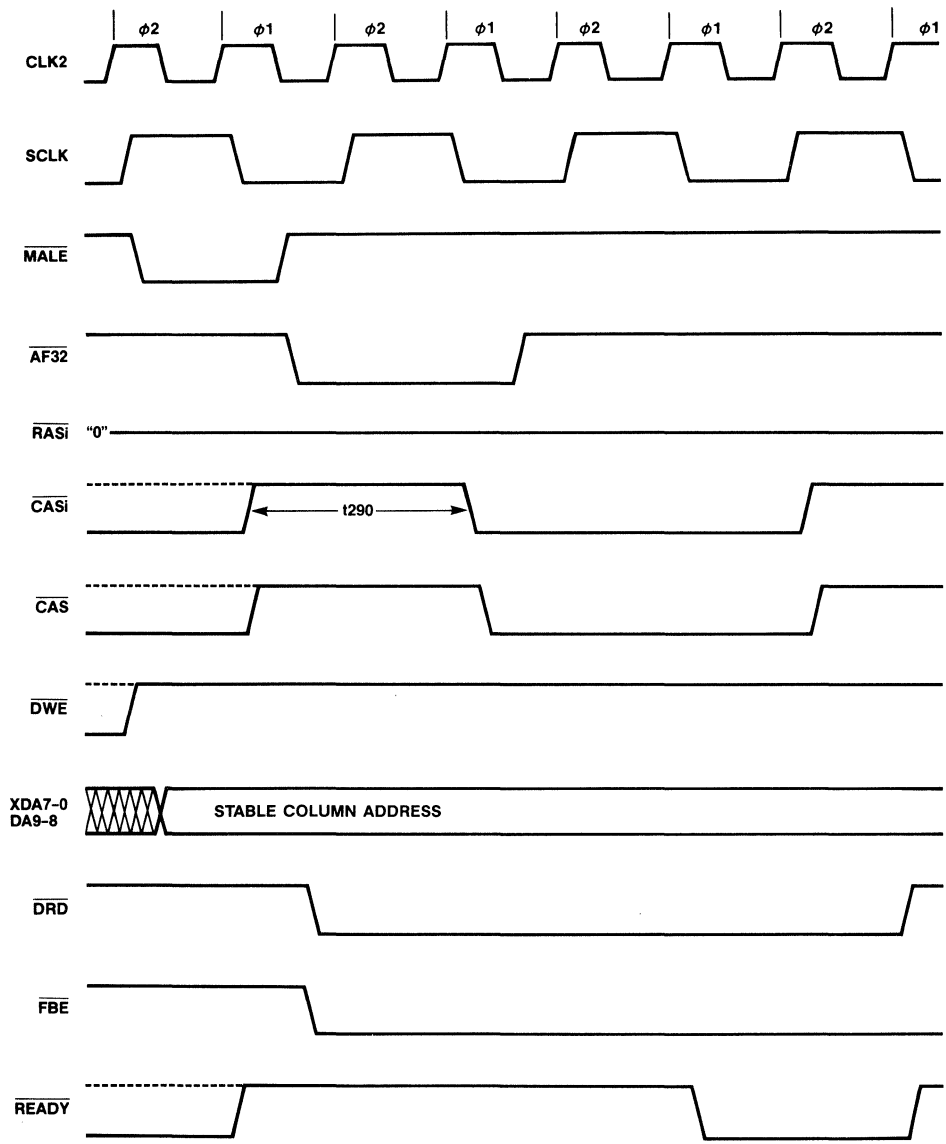
82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ MISS CYCLE



NOTES

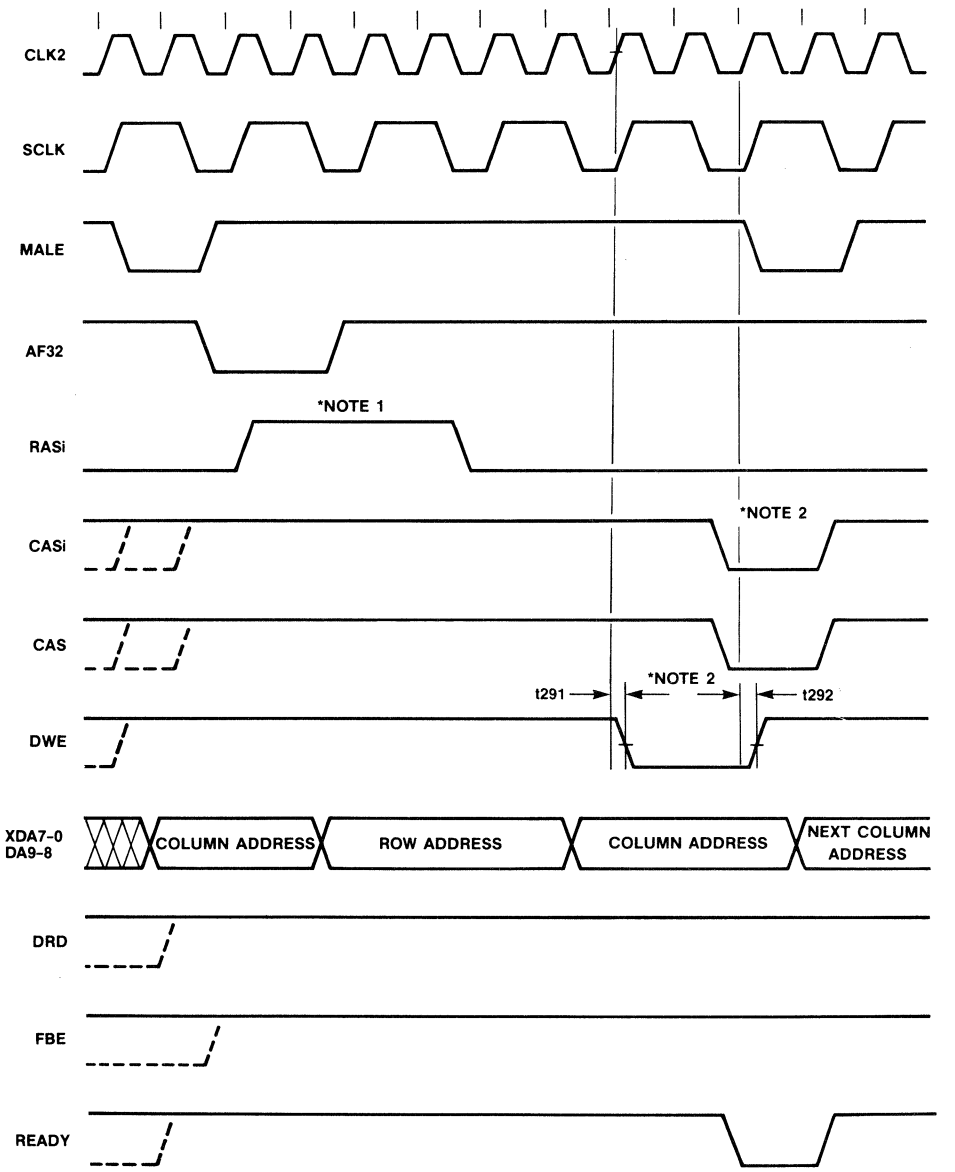
1. $\overline{\text{RASi}}$ precharge time will be increased by 2 CLK2 cycles if bit 7 of Register 11 (or 13) is programmed to "1".
2. $\overline{\text{CASi}}$ (and $\overline{\text{CAS}}$) pulse width will be increased by 2 CLK2 cycles if bit 6 of registers 11, (or 13) is programmed to "1".

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY CYCLE) READ HIT FOLLOWING A WRITE OR 1 WAIT STATE READ-HIT CYCLE



NOTE: The read cycle will be identical to this waveform (regardless whether the previous cycle is a Write or not) if bit 6 of Register 11 (or 13) is programmed to "1".

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY) WRITE MISS CYCLE



NOTES

1. $\overline{\text{RASi}}$ precharge time will be increased by 2 CLKZ cycles if bit 7 of Register 11 (or 13) is programmed to "1".
2. $\overline{\text{CASi}}$ (and $\overline{\text{CAS}}$) pulse widths will be increased by 2 CLK2 cycles if bit 6 of register 11, (or 13) is programmed to "1".

82A303 HIGH ADDRESS BUFFERS

- Buffer for bits 31:12 of the Local, X and System address buses.
- X and S address bus can be extended to 27 bits (128MB).
- Direct interface to AT Bus
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTIONS

The 82A303 as shown in figure 3-1 provides two functions:

- Generation of address decoding signals required by other chips.
- Interface between the local, X and System address bus.

Address Decode

The address decoding circuit provides as outputs LIOCS, LMEGCS, L64MEG, and HIROM. These signals are active if the address accesses satisfy the conditions defined in table 3-1. The signal decodes for LIOCS and LMEGCS are controlled by HLDA1 and latched on the trailing edge of MALE. The L64MEG and HIROM are simply decoded from the address signals.

Signal	Decode Condition
LIOCS	A<15:12> = 00H
LMEGCS	A<31:20> = 00H
L64MEG	A<31:26> = 00H
HIROM	A<31:26> = 3FH

Table 3-1. High Address Decodes Definition

Address Bus Interfaces

The 82A303 interconnects the local, X and system address buses with bidirectional drivers connecting each bus and the internal buses. Theses drivers have 24mA current drives for direct connection to the system address bus. The table 3-2 shows how the drivers are configured between the buses for each type of active bus requests. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

For all CPU sourced accesses, the addresses are latched on the trailing edge of MALE.

Active	Source	Target
HLDA1	XA	SA, A, MA
MASTER	SA	XA, A, MA
REF	-	SA driven LO
ATEN	A	XA, SA, MA
default	A	MA

Table 3-2. High Address Bus Control

27 bit Address Extensions

The standard AT implementation supports only 24-bit addresses. The CS 8230 allows for address extension on the SA and XA buses to 27 bits (128MB). This is done by grounding the enable pin XBHE for XA bus and SBHE for SA bus. Internal pullups are provided so that if the enable pins are left unconnected bits 24 to 27 of the respective bus are forced LO.

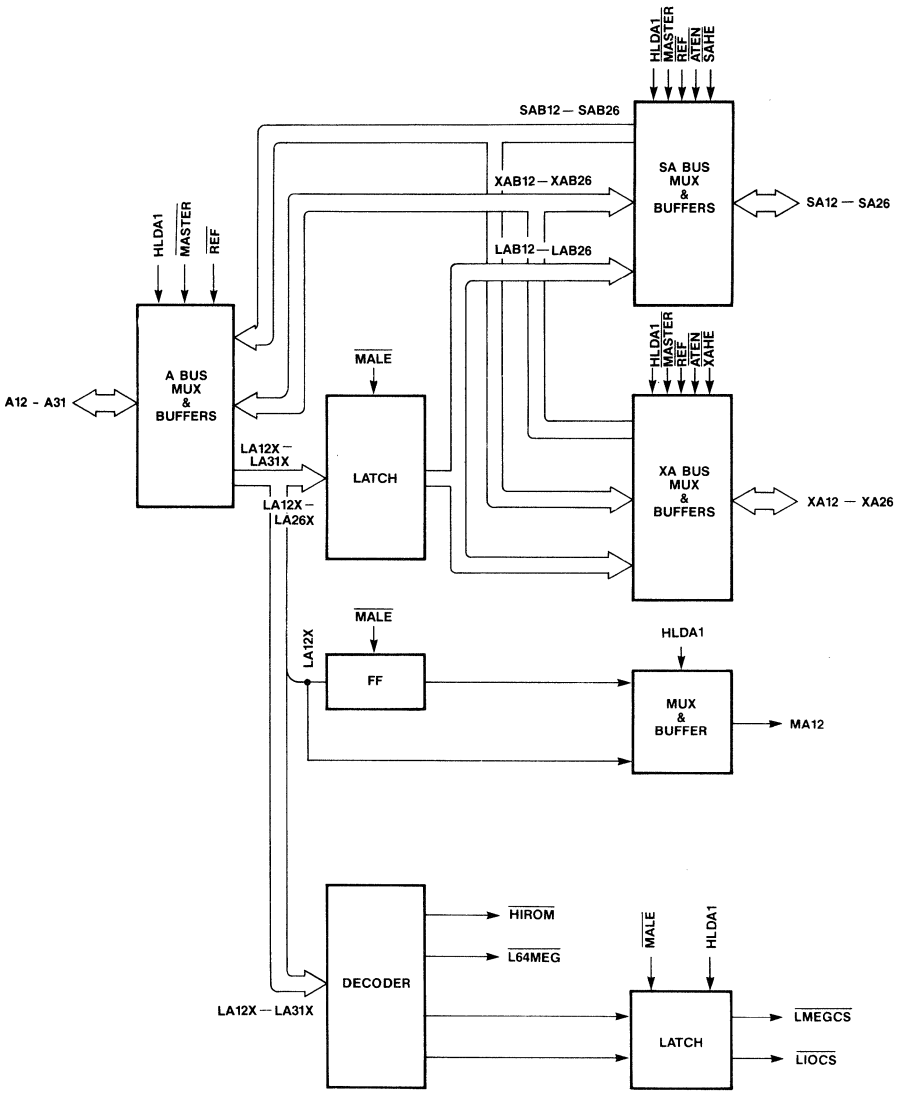


Figure 3-1. 82A303 Functional Block Diagram

82A303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A303 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12> and XA<26:21>.
2. All SA<20:12> and XA<26:21> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82A303 AC Characteristics

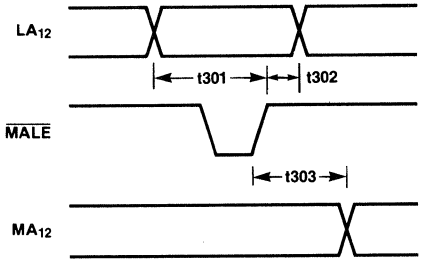
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

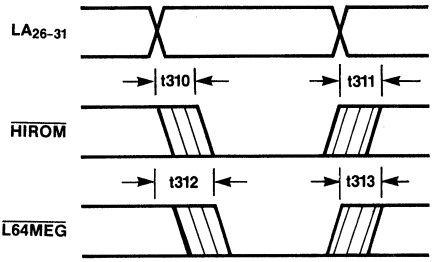
Sym	Description	Min.	Typ.	Max.	Units
t301	A to MA input set-up time to $\overline{\text{MALE}}$↑		TBD		
t302	A to MA input hold time from $\overline{\text{MALE}}$↑		TBD		
t303	MA output valid delay from $\overline{\text{MALE}}$↑	5		33	ns
t304	A to SA,XA input set-up time to $\overline{\text{MALE}}$↑		TBD		
t305	A to SA,XA input hold time from $\overline{\text{MALE}}$↑		TBD		
t306	SA output valid delay from $\overline{\text{ATEN}}$ active	8		33	ns
t307	SA tri-state delay from $\overline{\text{ATEN}}$ inactive	6		28	ns
t308	XA output valid delay from $\overline{\text{ATEN}}$ active	11		42	ns
t309	XA tri-state delay from $\overline{\text{ATEN}}$ inactive	9		38	ns
t310	$\overline{\text{HIROM}}$ decode active from A<32:26> valid	4		19	ns
t311	$\overline{\text{HIROM}}$ decode inactive from A<32:26> invalid	2		16	ns
t312	$\overline{\text{L64MEG}}$ decode active from A<32:26> valid	4		19	ns
t313	$\overline{\text{L64MEG}}$ decode inactive from A<32:26> invalid	2		17	ns
t314	$\overline{\text{LIOCS}}$ decode active from $\overline{\text{MALE}}$ active	6		26	ns
t315	$\overline{\text{LIOCS}}$ decode inactive from $\overline{\text{MALE}}$ active	4		23	ns
t316	$\overline{\text{LMEGCS}}$ decode active from $\overline{\text{MALE}}$ active	6		26	ns
t317	$\overline{\text{LMEGCS}}$ decode inactive from $\overline{\text{MALE}}$ active	4		23	ns
t318	A data valid delay from SA data valid	4		27	ns
t319	XA data valid delay from SA data valid	7		35	ns
t320	MA data valid delay from SA data valid	9		49	ns
t321	$\overline{\text{LIOCS}}$ decode active from SA data valid	13		50	ns
t322	$\overline{\text{LIOCS}}$ decode inactive from SA data invalid	10		39	ns
t323	$\overline{\text{L64MEG}}$ decode active from SA data valid	12		47	ns
t324	$\overline{\text{L64MEG}}$ decode inactive from SA data invalid	9		35	ns
t325	$\overline{\text{LMEGCS}}$ decode active from SA data valid	14		53	ns
t326	$\overline{\text{LMEGCS}}$ decode inactive from SA data invalid	10		40	ns
t327	A data valid delay from XA data valid	4		27	ns
t328	SA data valid delay from XA data valid	6		34	ns
t329	MA data valid delay from XA data valid	9		49	ns
t330	$\overline{\text{LIOCS}}$ decode active from XA data valid	13		50	ns

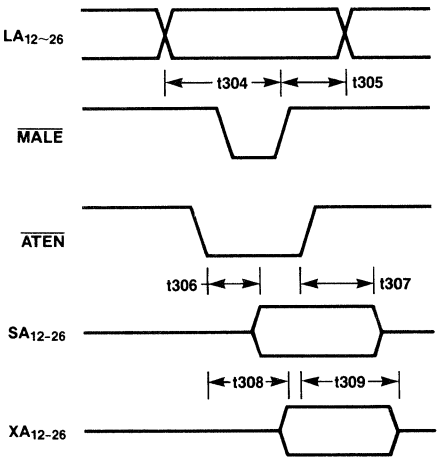
82A303 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

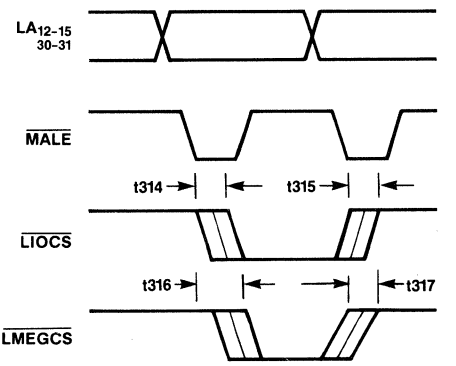
Sym	Description	Min.	Typ.	Max.	Units
t331	$\overline{\text{LIOCS}}$ decode inactive from XA data invalid	9		38	ns
t332	$\overline{\text{L64MEG}}$ decode active from XA data valid	12		47	ns
t333	$\overline{\text{L64MEG}}$ decode inactive from XA data invalid	9		35	ns
t334	$\overline{\text{LMEGCS}}$ decode active from XA data valid	14		53	ns
t335	$\overline{\text{LMEGCS}}$ decode inactive from XA data invalid	10		40	ns
t336	SA valid delay from $\overline{\text{REF}}$ active	18		64	ns
t337	SA tri-state delay from $\overline{\text{REF}}$ inactive	8		33	ns

82A303 TIMING DIAGRAMS

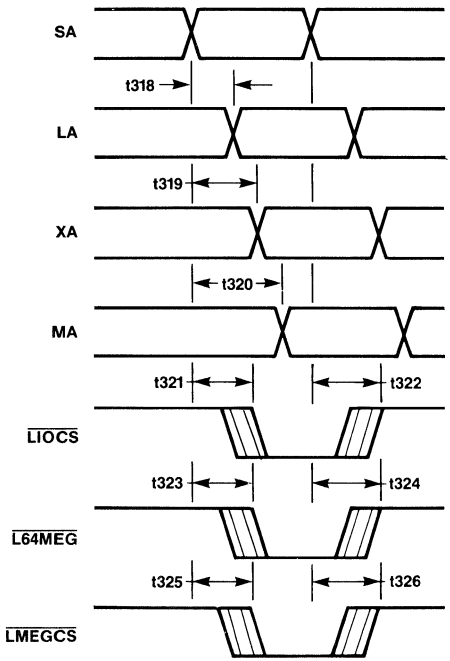


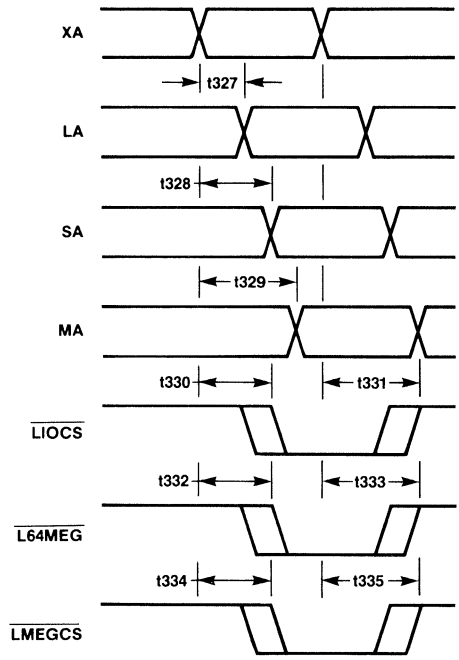


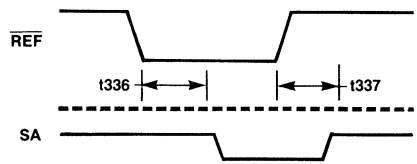




82A304 TIMING DIAGRAMS







82A304 LOW ADDRESS BUFFERS

- Buffer for bits 11:00 of the Local, X and System address buses.
- Peripheral device decode
- Direct interface to AT Bus
- Refresh Address Generation
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTIONS

Address Decode

The signals IO2XCS, 8042CS, PORTBCS, NMICS, 287CS, and AS provide the lower address decodes for the corresponding devices after being qualified by the LIOCS generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT IO addresses and is as shown in table 4-1. For applications where these devices are required to be relocated, the EXDEC can be tied LOW to ignore the LIOCS qualification and the MA<11:10> address bits.

Signal	Addresses Decoded
IO2XCS	022H, 023H
8042CS	060H, 064H
PORTBCS	061H
NMICS	070H
287CS	0E0H to 0FFH

Table 4-1. Low Address Decode Definition

Address Bus Interfaces

The 82A304 interfaces between the bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER, REF, and ATEN to drive the signals from the source to the target buses as defined by table 4-2 for each signal when active. When REF is asserted, the refresh counter is gated to the SA bus as refresh row address and is incremented. When none of the listed signals are active, the default buffers configuration is that the A bus drives the MA bus for memory accesses by CPU.

The SA<11:00> are 24mA address buffers for direct interface to the AT bus.

Active	Source	Target
HLDA1	XA	SA, MA, A
MASTER	SA	XA, MA, A
REF	Counter	SA
ATEN	A<11:2>	SA<11:2>, XA<11:2>, MA<11:4>
	XA<1:0>	SA<1:0>
default	A	MA

Table 4-2. Bus Control Definition

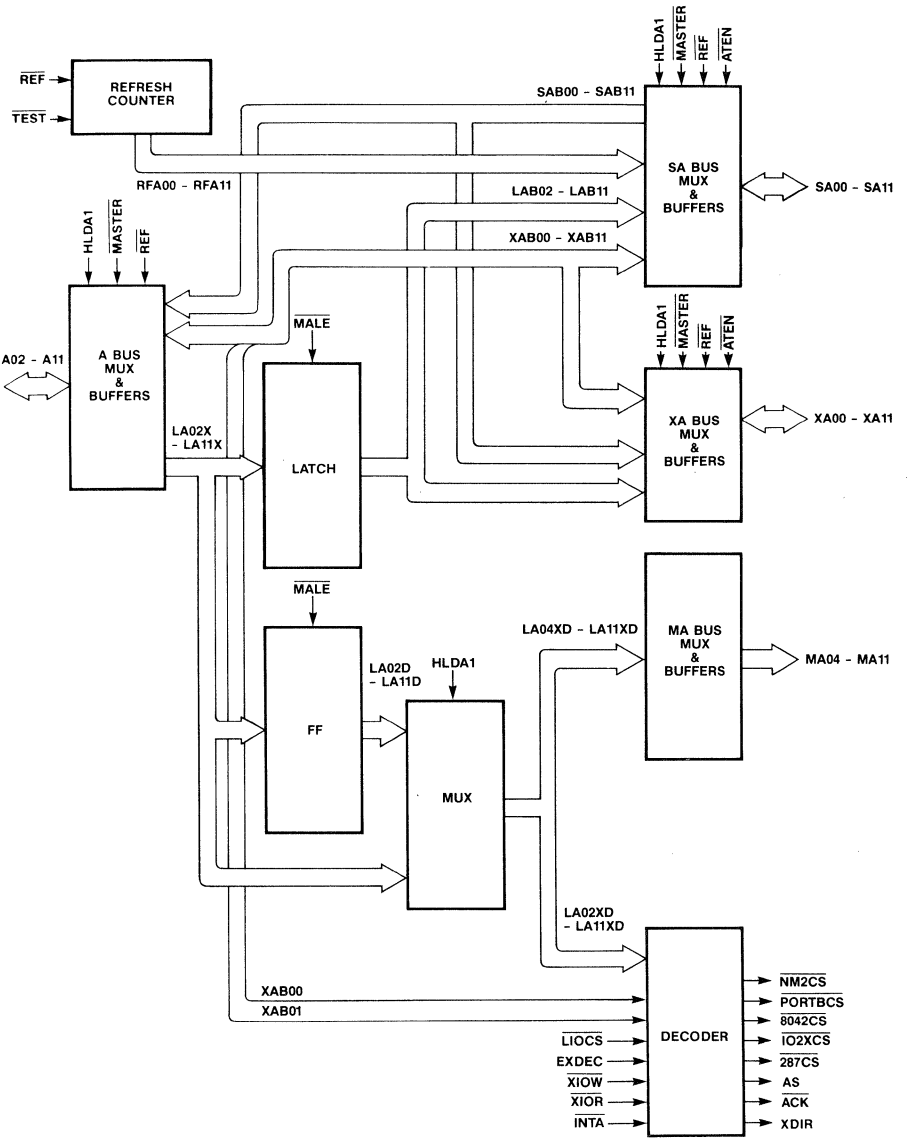


Figure 4-1. 82A304 Functional Block Diagram

82A304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<11:00>.
2. All SA<11:00> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82A304 AC Characteristics

(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t401	A to MA input set-up time to $\overline{MALE}$↑		TBD		
t402	A to MA input hold time from $\overline{MALE}$↑		TBD		
t403	MA output valid delay from $\overline{MALE}$↑	5		34	ns
t404	A to SA, XA input set-up time to $\overline{MALE}$↑		TBD		
t405	A to SA, XA input hold time from $\overline{MALE}$↑		TBD		
t406	SA output valid delay from $\overline{ATEN}$ active	8		33	ns
t407	SA tri-state delay from $\overline{ATEN}$ inactive	6		28	ns
t408	XA output valid delay from $\overline{ATEN}$ active	10		41	ns
t409	XA tri-state delay from $\overline{ATEN}$ inactive	9		37	ns
t410	$\overline{NMICS}$ decode active from $\overline{MALE}$↑	11		44	ns
t411	$\overline{NMICS}$ decode inactive from $\overline{MALE}$↑	10		40	ns
t412	$\overline{PORTBCS}$ decode active from $\overline{MALE}$↑	11		44	ns
t413	$\overline{PORTBCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns
t414	$\overline{8042CS}$ decode active from $\overline{MALE}$↑	11		44	ns
t415	$\overline{8042CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns
t416	$\overline{IO2XCS}$ decode active from $\overline{MALE}$↑	11		44	ns
t417	$\overline{IO2XCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns
t418	$\overline{287CS}$ decode active from $\overline{MALE}$↑	11		44	ns
t419	$\overline{287CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns
t420	A data valid delay from SA data valid	4		26	ns
t421	XA data valid delay from SA data valid	3		35	ns
t422	MA data valid delay from SA data valid	9		49	ns
t423	$\overline{NMICS}$ decode active from SA data valid	14		58	ns
t424	$\overline{NMICS}$ decode inactive from SA data invalid	11		46	ns
t425	$\overline{PORTBCS}$ decode active from SA data valid	15		59	ns
t426	$\overline{PORTBCS}$ decode inactive from SA data invalid	11		46	ns
t427	$\overline{8042CS}$ decode active from SA data valid	15		59	ns
t428	$\overline{8042CS}$ decode inactive from SA data invalid	11		46	ns
t429	$\overline{IO2XCS}$ decode active from SA data valid	12		59	ns
t430	$\overline{IO2XCS}$ decode inactive from SA data invalid	12		46	ns

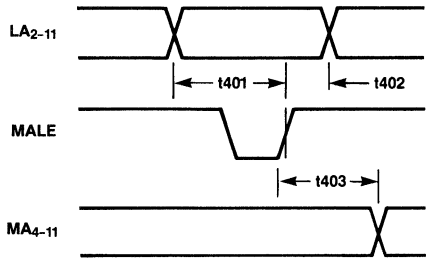
82A304 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

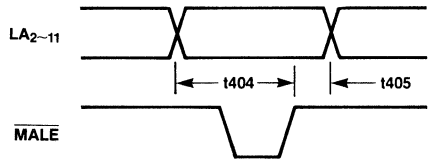
Sym	Description	Min.	Typ.	Max.	Units
t431	$\overline{287CS}$ decode active from SA data valid	16		59	ns
t432	$\overline{287CS}$ decode inactive from SA data invalid	13		46	ns
t433	$\overline{XDIR}$ decode active from SA data valid	15		59	ns
t434	$\overline{XDIR}$ decode inactive from SA data invalid	15		60	ns
t435	A data valid delay from XA data valid	4		26	ns
t436	SA data valid delay from XA data valid	7		34	ns
t437	MA data valid delay from XA data valid	9		49	ns
t438	$\overline{NMICS}$ decode active from XA data valid	14		58	ns
t439	$\overline{NMICS}$ decode inactive from XA data invalid	11		46	ns
t440	$\overline{PORTBCS}$ decode active from XA data valid	15		59	ns
t441	$\overline{PORTBCS}$ decode inactive from XA data invalid	11		46	ns
t442	$\overline{8042CS}$ decode active from XA data valid	15		59	ns
t443	$\overline{8042CS}$ decode inactive from XA data invalid	11		46	ns
t444	$\overline{IO2XCS}$ decode active from XA data valid	12		59	ns
t445	$\overline{IO2XCS}$ decode inactive from XA data invalid	12		46	ns
t446	$\overline{287CS}$ decode active from XA data valid	16		59	ns
t447	$\overline{287CS}$ decode inactive from XA data invalid	13		46	ns
t448	$\overline{XDIR}$ decode active from XA data valid	15		55	ns
t449	$\overline{XDIR}$ decode inactive from XA data invalid	15		55	ns
t450	$\overline{NMICS}$ decode active from $\overline{LIOCS}$ active	7		31	ns
t451	$\overline{NMICS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t452	$\overline{PORTBCS}$ decode active from $\overline{LIOCS}$ active	7		31	ns
t453	$\overline{PORTBCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t454	$\overline{8042CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t455	$\overline{8042CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t456	$\overline{IO2XCS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t457	$\overline{IO2XCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t458	$\overline{287CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t459	$\overline{287CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t460	$\overline{XDIR}$ decode active from $\overline{LIOCS}$ active	8		32	ns

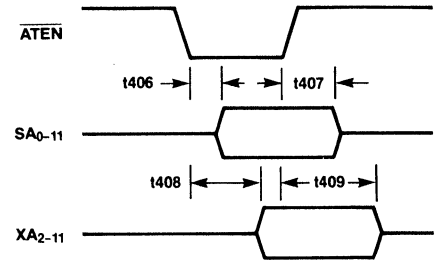
82A304 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

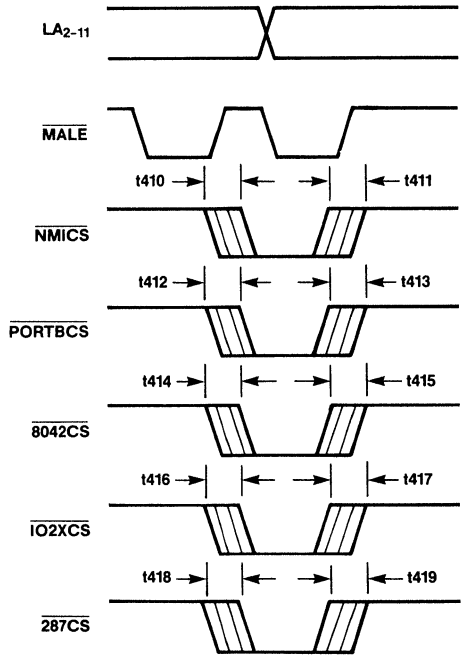
Sym	Description	Min.	Typ.	Max.	Units
t461	$\overline{\text{XDIR}}$ decode inactive from $\overline{\text{LIOCS}}$ inactive	5		26	ns
t462	$\overline{\text{XDIR}}$ decode active from $\overline{\text{INTA}}$ active	4		23	ns
t463	$\overline{\text{XDIR}}$ decode inactive from $\overline{\text{INTA}}$ inactive	2		17	ns
t464	$\overline{\text{XDIR}}$ decode active from $\overline{\text{XIOR}}$ active	6		27	ns
t465	$\overline{\text{XDIR}}$ decode inactive from $\overline{\text{XIOR}}$ inactive	4		20	ns
t466	$\overline{\text{ACK}}$ decode active from HLDA1 active	9		37	ns
t467	$\overline{\text{ACK}}$ decode inactive from HLDA1 inactive	7		32	ns
t468	$\overline{\text{ACK}}$ decode active from $\overline{\text{MASTER}}$ active	8		33	ns
t469	$\overline{\text{ACK}}$ decode inactive from $\overline{\text{MASTER}}$ inactive	6		26	ns
t470	SA data valid delay from $\overline{\text{REF}}$ active	18		64	ns
t471	SA tri-state delay from $\overline{\text{REF}}$ inactive	8		33	ns

82A304 TIMING DIAGRAMS

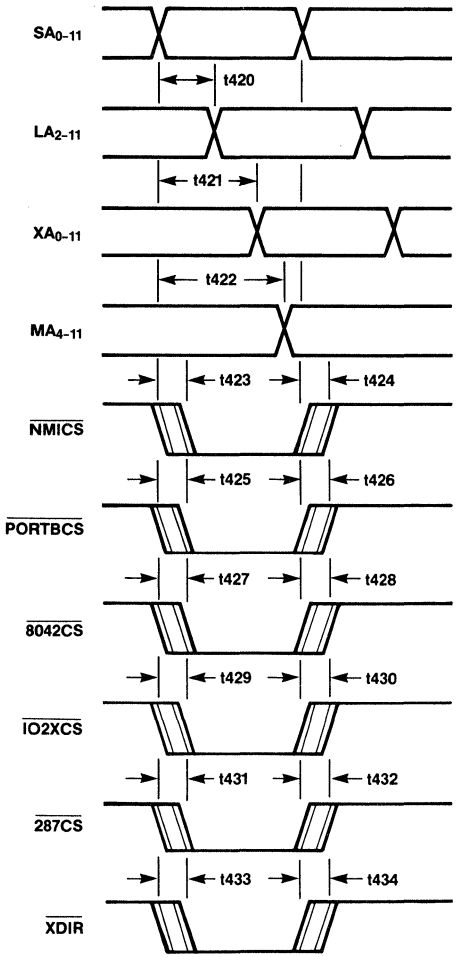


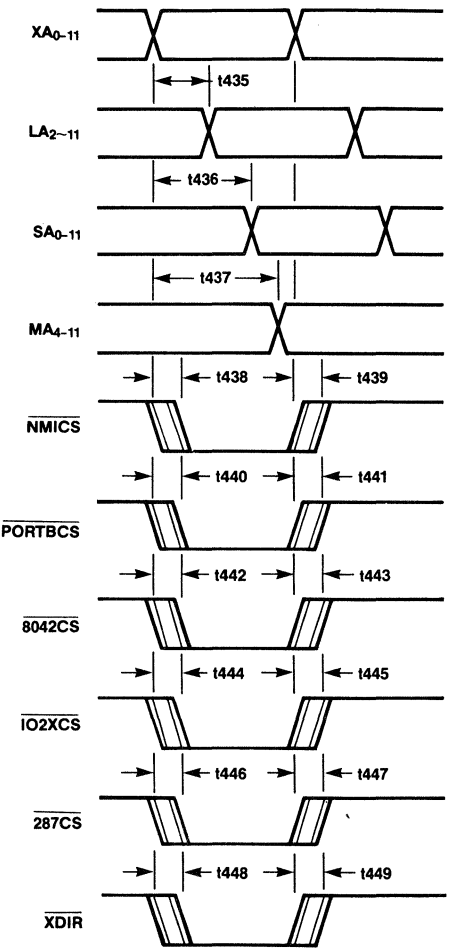




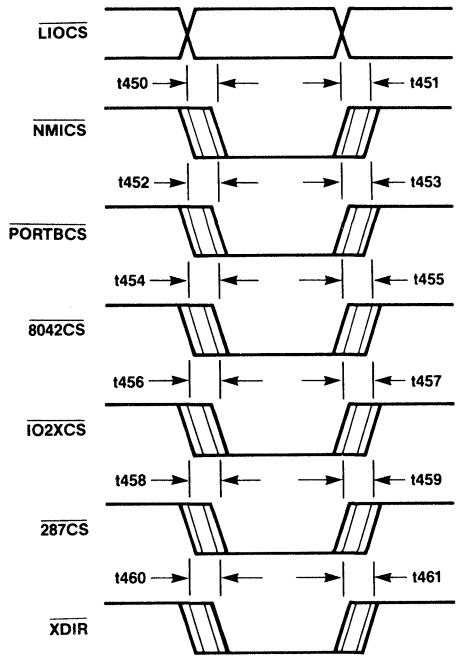


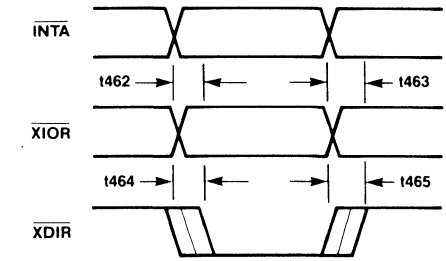
82A304 TIMING DIAGRAMS

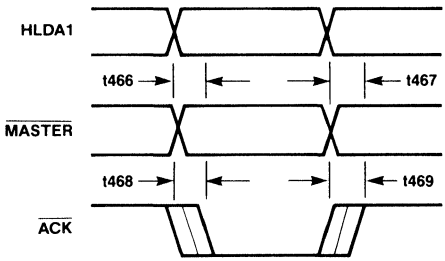


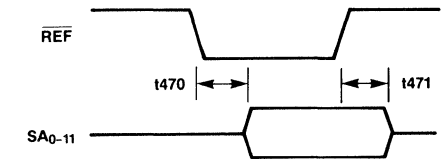


82A304 TIMING DIAGRAMS









82A305 DATA BUFFER

- Nibble Slice of Memory and AT Data Bus Interface
- Data Size Conversion
- Advanced Schottky technology

FUNCTIONAL DESCRIPTION

The 82A305 interfaces between the Local, Memory and System (AT IO channel) data busses and provides data alignment and size conversion for AT IO channel operations. It is designed as a nibble slice to reduce pin count and simplify system design and two parts are used to interface all data buses.

Bus Controls

The 82A305 controls the bus buffers according to the signals HLDA1, $\overline{ATEN}$, $\overline{MDEN}$, $\overline{LDEN}$, SDIR, $\overline{MRD}$, and AC<3:0>. The first group of signals HLDA1, $\overline{ATEN}$, $\overline{MDEN}$, and $\overline{LDEN}$ determines which buses are connected, and the second group of signals SDIR, $\overline{MRD}$, and AC<3:0> determines the direction of the buffers drivers. Table 5-1 shows the bus connections for different bus cycles.

All drivers are active for the active buses, and external bus controls are required if selective data bits need be controlled. For the DRAM interface, the $\overline{LBE}$<3:0> must be used to ensure that only the valid data bytes are written into the DRAM's during a write cycle.

Bus Cycles	From Bus	To Bus	Direction Control
$\overline{HLDA1}$=0, $\overline{ATEN}$=1	D	MD	$\overline{MRD}$=1
	MD	D	$\overline{MRD}$=0
$\overline{HLDA1}$=0, $\overline{ATEN}$=0	D	SD	SDIR=1
	SD	D	SDIR=0
HLDA1=1	SD	MD,D	$\overline{SDIR}$=0, $\overline{MRD}$=1
	MD	SD	$\overline{SDIR}$=1, $\overline{MRD}$=0
	D	SD	$\overline{SDIR}$=1, $\overline{MRD}$=1, $\overline{LDEN}$=0

Table 5-1. Bus Control Definitions

Data Conversion

The 82A305 provides the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action codes AC<3:0> are used to control how bus bits are connected between the IO channel SD bus and the CPU local bus D or the system memory MD bus. The action codes are provided by the 82C301 bus controller for CPU to AT bus access cycles and is qualified by the ACEN. The meaning of the action codes are:

AC<3:0>	FROM	TO
0	MD,D<15:0>	SD<15:0>
1	MD,D<15:8>	SD<15:8>, SD<7:0>
2	MD,D<31:16>	SD<15:0>
3	MD,D<31:24>	SD<15:8>, SD<7:0>
4	MD,D<31:0>	SD<31:0>
5	SD<7:0>	MD,D<7:0>
6	SD<7:0>	MD,D<15:8>
7	SD<7:0>	MD,D<23:16>
8	SD<7:0>	MD,D<31:24>
9	SD<15:0>	MD,D<15:0>
A	SD<15:0>	MD,D<31:16>
B	reserved	
C	SD<31:0>	MD,D<31:0>
D	reserved	
E	reserved	
F	reserved	

Table 5-2. Action Code Definition

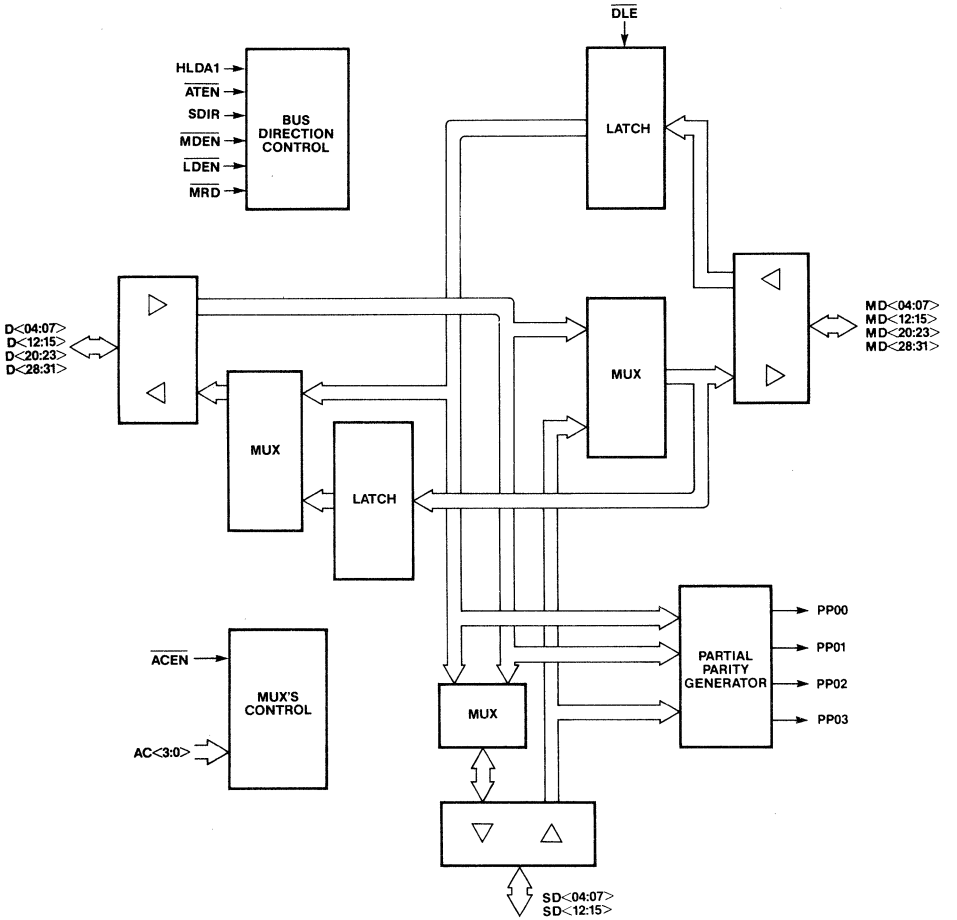


Figure 5-1. 82A305 Functional Block Diagram

82A305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 2)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

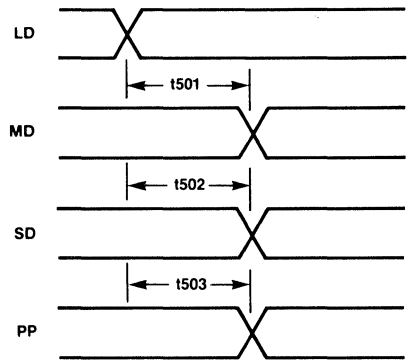
NOTES
1. All bus outputs and PP<3:0> have I_{OL} = 10mA.
2. All outputs and bidirectional pins.

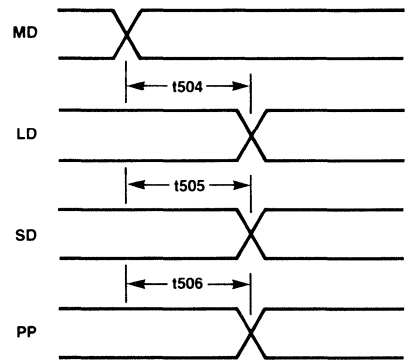
82A305 AC Characteristics

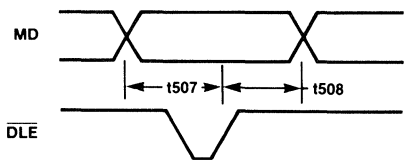
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

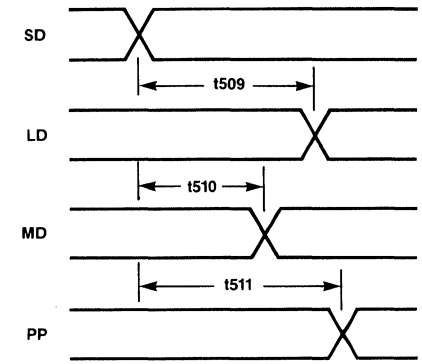
Sym	Description	Min.	Typ.	Max.	Units
t501	MD data valid delay from LD data valid	4		27	ns
t502	SD data valid delay from LD data valid	4		27	ns
t503	PP data valid delay from LD data valid	5		29	ns
t504	LD data valid delay from MD data valid	4		28	ns
t505	SD data valid delay from MD data valid	4		28	ns
t506	PP data valid delay from MD data valid	5		30	ns
t507	MD data set-up time to $\overline{DLE}$↑		TBD		
t508	MD data hold time from $\overline{DLE}$↑		TBD		
t509	LD data valid delay from SD data valid	8		38	ns
t510	MD data valid delay from SD data valid	4		27	ns
t511	PP data valid delay from SD data valid	5		33	ns
t512	SD data set-up time to $\overline{ACEN}$↑		TBD		
t513	SD data hold time from $\overline{ACEN}$↑		TBD		
t514	MD data valid delay from $\overline{MDEN}$↓	7		29	ns
t515	MD tri-state delay from $\overline{MDEN}$↑	5		23	ns
t516	LD data valid delay from $\overline{MDEN}$↓	7		30	ns
t517	LD tri-state delay from $\overline{MDEN}$↑	5		23	ns

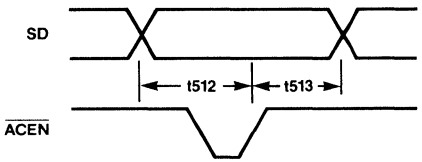
82A305 TIMING DIAGRAMS

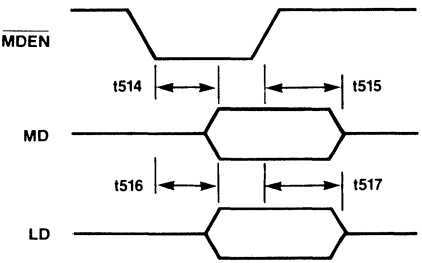












82A306 CONTROL BUFFER

- 14.318MHz oscillator and divide by 12 counter
- Byte enable latch
- Parity Checking
- Direct interface to AT Bus
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTION

14MHz Oscillator and Divider

The color reference oscillator is provided eliminating the 8224 normally used in AT compatible systems. A divide by 12 counter is also included to generate the OSC/12 (1.19MHz) signal used on the system board.

AF32 Generation

The AF32 is used in the CS 8230 system to indicate that the current bus cycle is a CPU local bus cycle.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located on the 82A306. An additional input FBE is provided to force all byte enables active during certain memory operations. A pullup resistor is provided on the FBE input for implementations not requiring this feature.

Parity Checking and Generation

The 82A306 provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH<3:0> and PPL<3:0> generated on the two (nibble wide) data buffers 82A305.

For a memory read access, read parity PPH<3:0> and PPL<3:0> are checked against the parity bits MP<3:0> read from memory. These parity bits are latched by CAS and PCHK so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes which are not valid. The OR'ed byte-wise parity error is then latched as the output LPAR if PEN input is asserted.

During a memory write access, write parity for each byte is generated from PPH<3:0> and PPL<3:0> and can be gated onto the memory parity bus MP<3:0> if enabled by WPE controlling the tri-state drivers. If an external parity generation circuit is used, an internal pullup resistor is provided for WPE to disable the write parity output buffers if left unconnected.

Bus Drivers

24mA drivers are provided for some of the control signals on the IO channel. These include SYSCLK, OSC, OSC/12, RDRV, SBHE, BALE, IOR, IOW, MEMR, MEMW, SMEMR, SMEMW and OUT1.

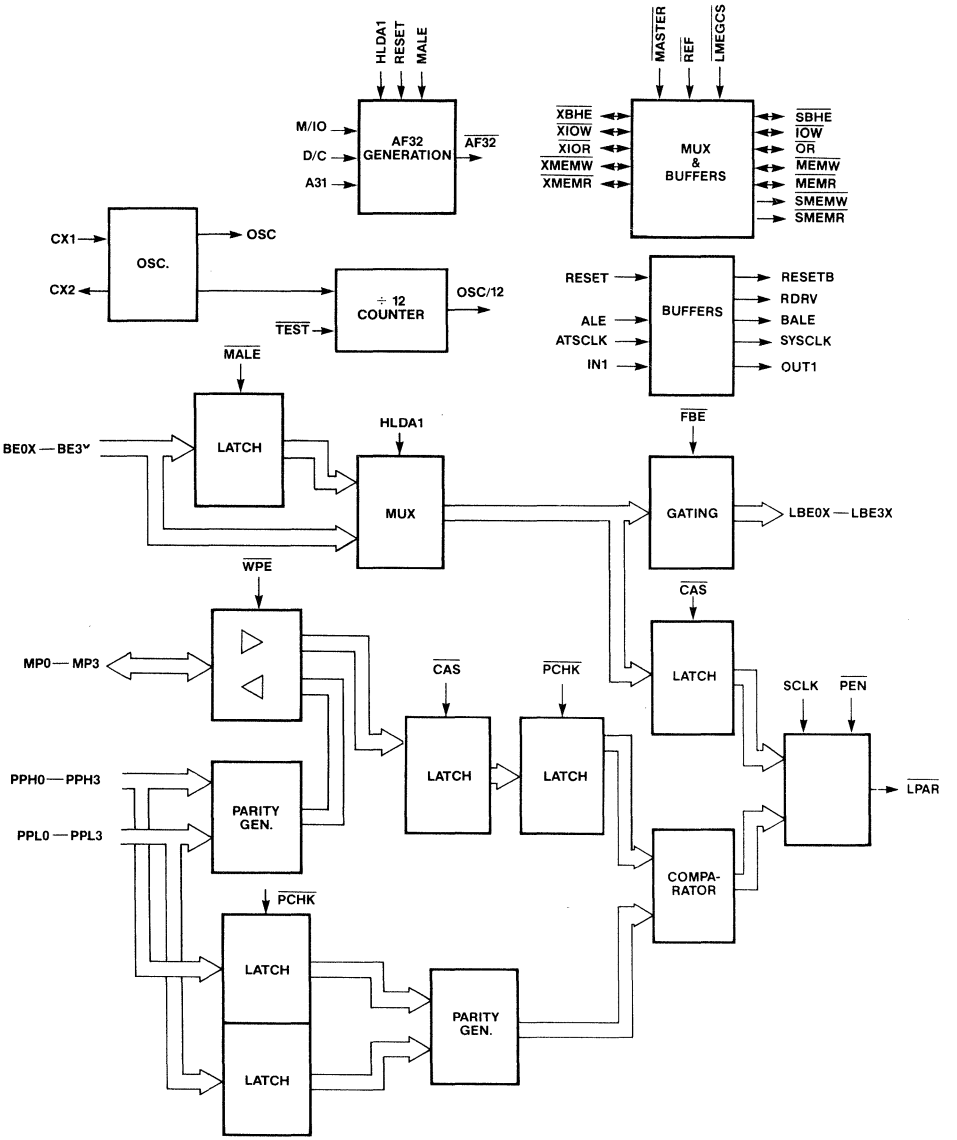


Figure 6-1. 82A306 Functional Block Diagram

82A306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. $\overline{MP<3:0>}$, $\overline{XIOW}$, $\overline{XIOR}$, $\overline{XBHE}$, $\overline{XMEMW}$, $\overline{XMEMR}$, $\overline{RESTEB}$, $\overline{LBE<3:0>}$ all have I_{OL} = 10mA.
2. $\overline{SBHE}$, $\overline{IOW}$, $\overline{IOR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{SMEMW}$, $\overline{SMEMR}$, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82A306 AC Characteristics

(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t601	OSC↓ delay from CX1↑	4		22	ns
t602	OSC↑ delay from CX1↓	5		26	ns
t603	OSC/12↑ delay from CX1↑	9		35	ns
t604	OSC/12↓ delay from CX1↓	9		37	ns
t605	$\overline{BE}$<3:0> set-up time to $\overline{MALE}$↑		TBD		
t606	$\overline{BE}$<3:0> hold time to $\overline{MALE}$↑		TBD		
t607	$\overline{LBE}$<3:0> valid delay from $\overline{MALE}$↑	7		35	ns
t608	$\overline{LBE}$<3:0> valid delay from $\overline{BE}$<3:0> valid	3		25	ns
t609	$\overline{LBE}$<3:0> LO delay from $\overline{FBE}$↓	5		25	ns
t610	$\overline{LBE}$<3:0> de-asserted from $\overline{FBE}$↑	3		19	ns
t611	PPH<3:0>, PPL<3:0> set-up time to $\overline{PCHK}$↑		TBD		
t612	PPH<3:0>, PPL<3:0> hold time to $\overline{PCHK}$↑		TBD		
t613	MP<3:0> valid delay from corresponding PPH<3:0> and PPL<3:0>	2		21	ns
t614	MP<3:0> set-up time from $\overline{CAS}$↑		TBD		
t615	MP<3:0> hold time from $\overline{CAS}$↑		TBD		
t616	$\overline{LPAR}$↑ delay from SCLK↑	4		23	ns
t617	$\overline{LPAE}$↓ delay from SCLK↑	6		24	ns
t618	$\overline{LPAR}$↑ delay from $\overline{PEN}$↑	1		13	ns
t619	$\overline{LPAR}$↓ delay from $\overline{PEN}$↓	3		19	ns
t620	$\overline{MEMW}$↓ (or $\overline{MEMR}$↓) delay from $\overline{XMEMW}$↓ (or $\overline{XMEMR}$↓)	3		19	ns
t621	$\overline{MEMW}$↑ (or $\overline{MEMR}$↑) delay from $\overline{XMEMW}$↑ (or $\overline{XMEMR}$↑)	1		14	ns
t622	$\overline{XMEMW}$↓ (or $\overline{XMEMR}$↓) delay from $\overline{MEMW}$↓ (or $\overline{MEMR}$↓)	4		21	ns
t623	$\overline{XMEMW}$↑ (or $\overline{XMEMR}$↑) delay from $\overline{MEMW}$↑ (or $\overline{MEMR}$↑)	1		14	ns
t624	$\overline{SMEMW}$↓ (or $\overline{SMEMR}$↓) delay from $\overline{XMEMW}$↓ (or $\overline{XMEMR}$↓)	5		23	ns
t625	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from $\overline{LMEGCS}$↓	4		23	ns

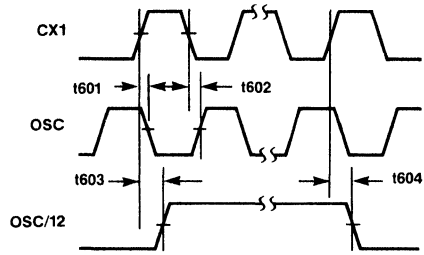
82A306 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

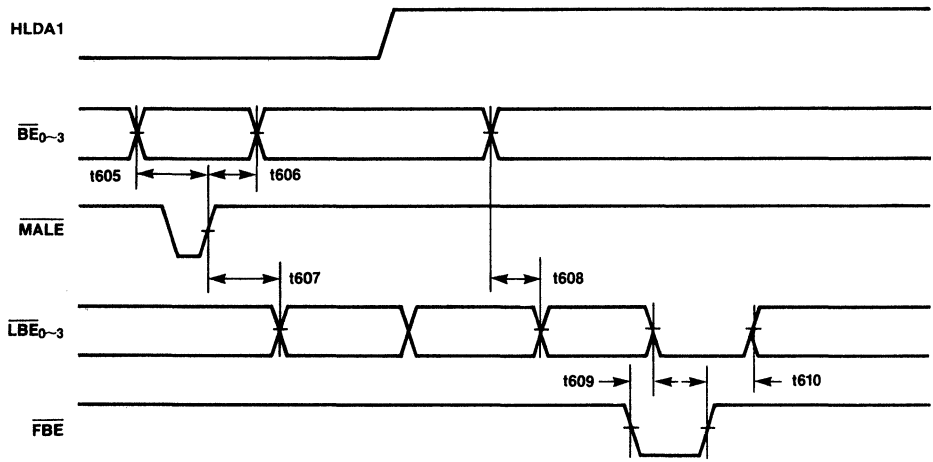
Sym	Description	Min.	Typ.	Max.	Units
t626	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to LO transition delay from $\overline{LMEGCS}$↑	6		28	ns
t627	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from $\overline{REF}$↓	6		28	ns
t628	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to LO transition delay from $\overline{REF}$↑	8		32	ns
t629	$\overline{SMEMW}$↑ (or $\overline{SMEMR}$↑) delay from $\overline{XMEMW}$↑ (or $\overline{XMEMR}$↑)	3		19	ns
t630	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{LMEGCS}$↓	4		23	ns
t631	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{LMEGCS}$↑	6		28	ns
t632	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{REF}$↓	6		28	ns
t633	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{REF}$↑	8		32	ns
t634	$\overline{SMEMW}$↓ (or $\overline{SMEMR}$↓) delay from $\overline{MEMW}$↓ (or $\overline{MEMR}$↓)	5		23	ns
t635	$\overline{SMEMW}$↑ (or $\overline{SMEMR}$↑) delay from $\overline{MEMW}$↑ (or $\overline{MEMR}$↑)	3		19	ns
t636	$\overline{IOW}$↓ (or $\overline{IOR}$↓) delay from $\overline{XIOW}$↓ (or $\overline{XIOR}$↓)	3		18	ns
t637	$\overline{IOW}$↑ (or $\overline{IOR}$↑) delay from $\overline{XIOW}$↑ (or $\overline{XIOR}$↑)	1		14	ns
t638	$\overline{XIOW}$↓ (or $\overline{XIOR}$↓) delay from $\overline{IOW}$↓ (or $\overline{IOR}$↓)	4		21	ns
t639	$\overline{XIOW}$↑ (or $\overline{XIOR}$↑) delay from $\overline{IOW}$↑ (or $\overline{IOR}$↑)	1		14	ns
t640	$\overline{SBHE}$↓ delay from $\overline{XBHE}$↓	3		18	ns
t641	$\overline{SBHE}$↑ delay from $\overline{XBHE}$↑	1		14	ns
t642	$\overline{XBHE}$↓ delay from $\overline{SBHE}$↓	4		21	ns
t643	$\overline{XBHE}$↑ delay from $\overline{SBHE}$↑	1		14	ns
t644	RESETB↓ delay from RESET↓	3		20	ns
t645	RESETB↑ delay from RESET↑	1		14	ns
t646	RDRV↓ delay from RESET↓	3		18	ns

82A306 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

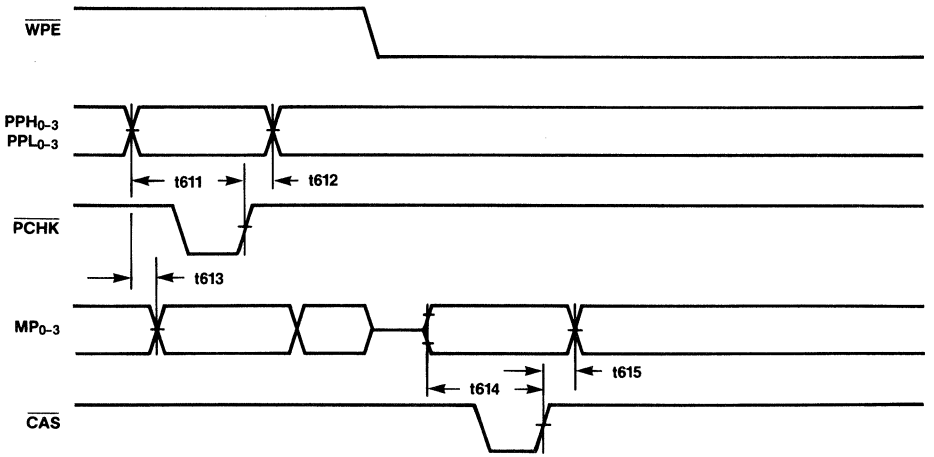
Sym	Description	Min.	Typ.	Max.	Units
t647	RDRV↑ delay from RESET↑	1		14	ns
t648	BALE↓ delay from ALT↓ SYSCLK↓ delay from ATSCLK↓ OUT1↓ delay from IN1↓	2		17	ns
t649	BALE↑ delay from ALT↑ SYSCLK↑ delay from ATSCLK↑ OUT1↑ delay from IN1↑	1		13	ns
t650	M/$\overline{IO}$, D/$\overline{C}$, A31 set-up time to $\overline{MALE}$↑		TBD		
t651	M/$\overline{IO}$, D/$\overline{C}$, A31 hold time to $\overline{MALE}$↑		TBD		
t652	$\overline{AF32}$ HI-Z to LO transition delay from $\overline{MALE}$↑	7		32	ns
t653	$\overline{AF32}$ LO to HI-Z transition delay from $\overline{MALE}$↑	6		29	ns
t654	$\overline{AF32}$ LO to HI-Z transition delay from RESET↑	6		28	ns
t655	$\overline{AF32}$ LO to HI-Z transition delay from HLDA1↑	6		29	ns

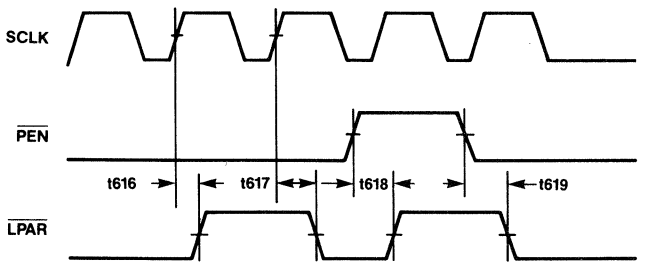
82A306 TIMING DIAGRAMS



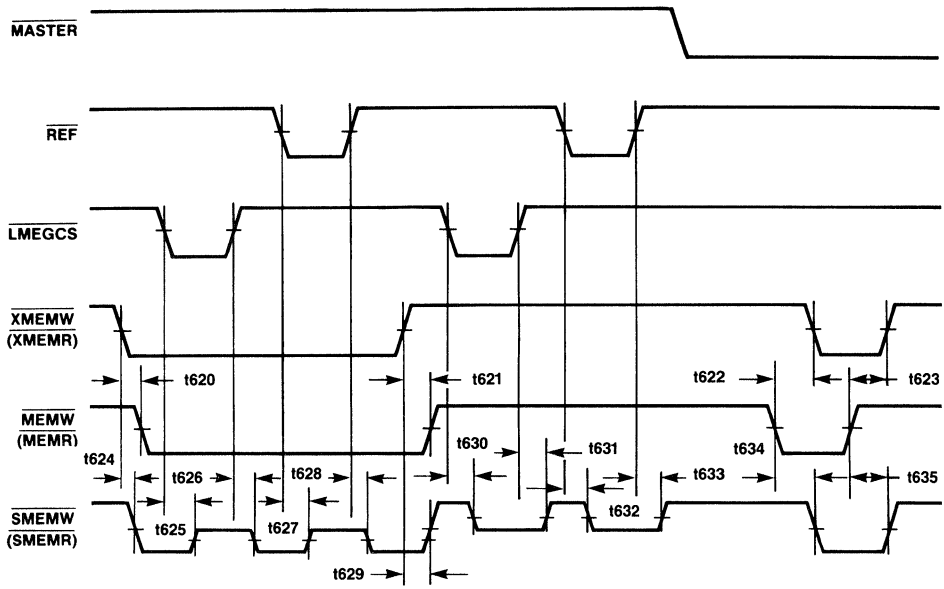


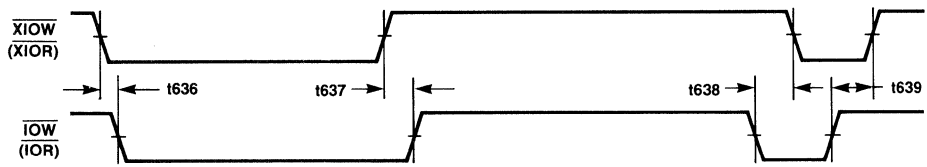
82A306 TIMING DIAGRAMS

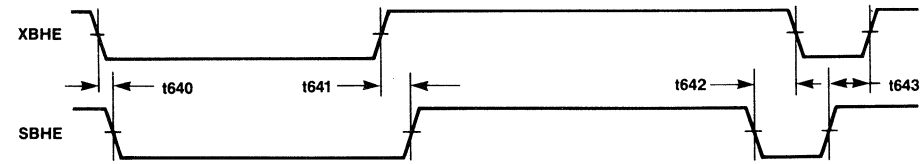




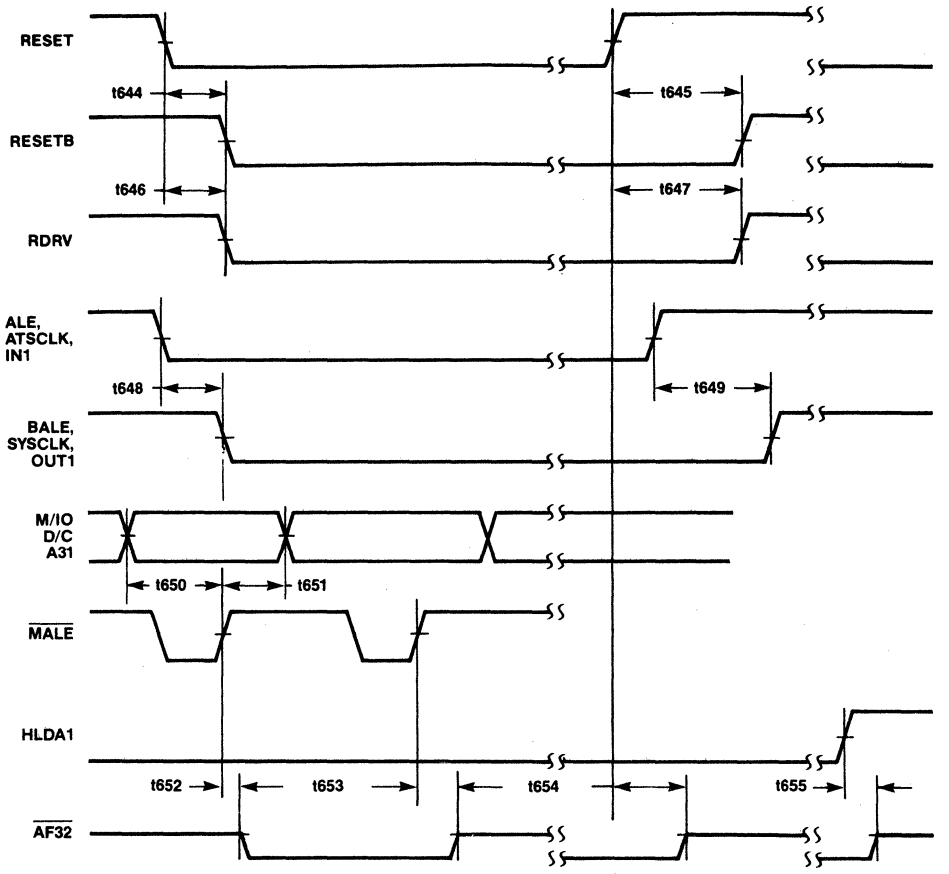
82A306 TIMING DIAGRAMS





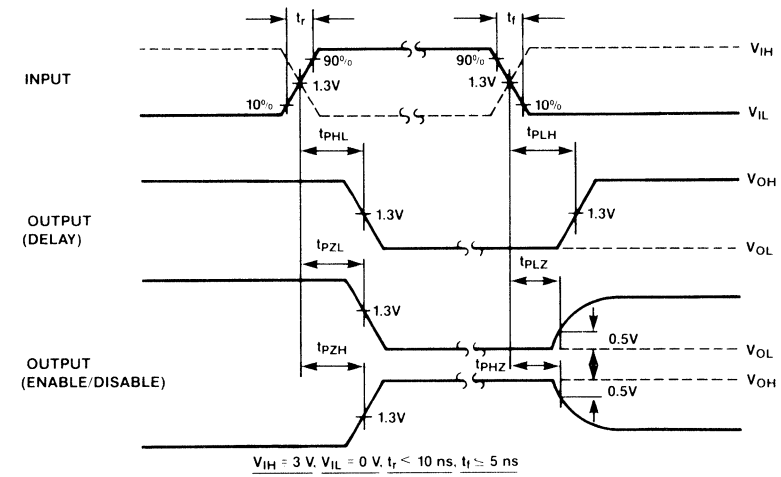


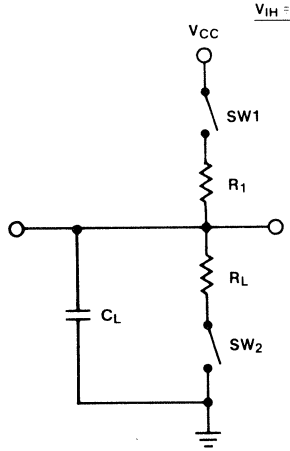
82A306 TIMING DIAGRAMS

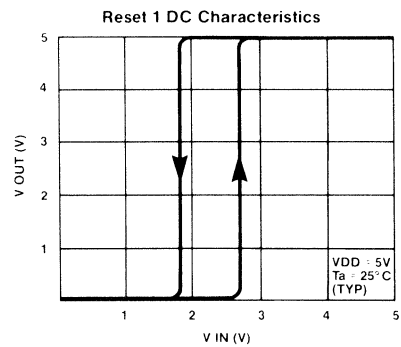


Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON ON

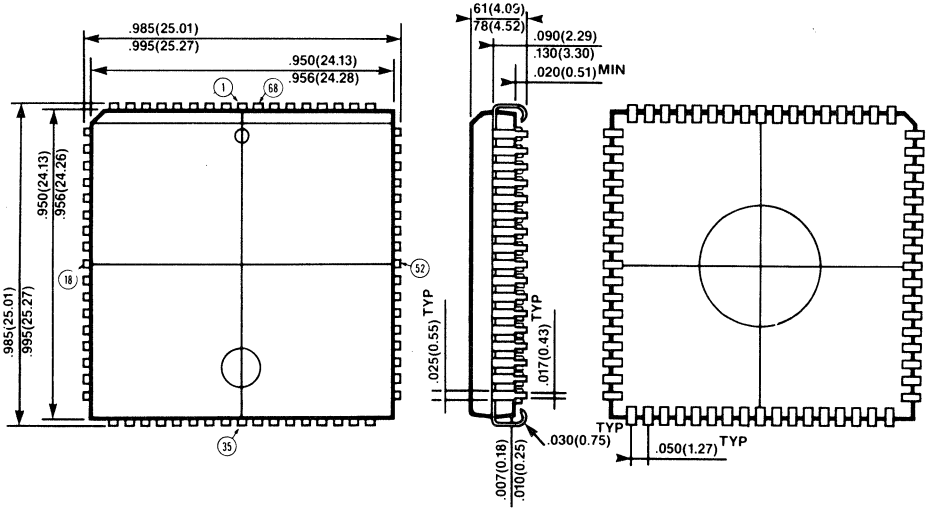






Load Circuit and AC Characteristics Measurement Waveform

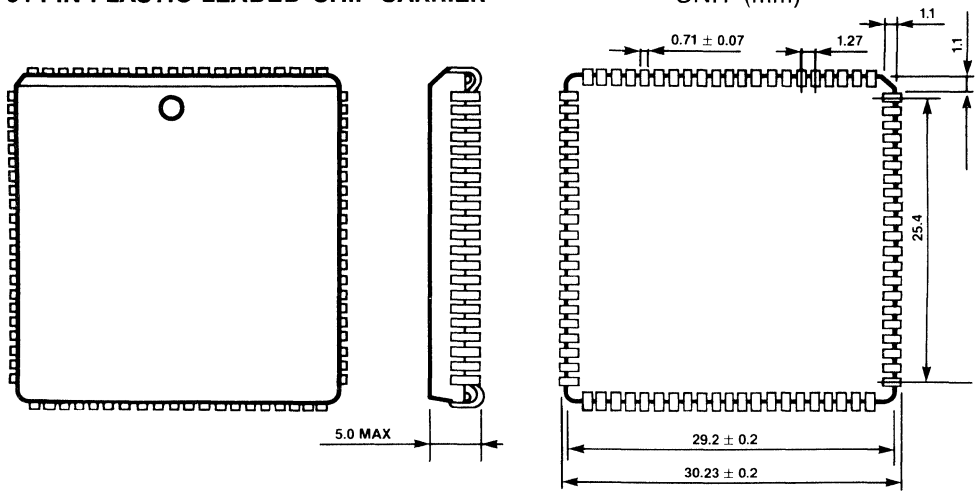
68-LEAD PLASTIC CHIP CARRIER



DIMENSIONS IN INCHES (MILLIMETERS) S = 3.6/1

84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)



82A303 Absolute Maximum Ratings

Order Number	Package Type Note 1	Remarks
P82C301	PLCC-84	C (Note 2)
P82C302	PLCC-84	C
P82A303	PLCC-68	C
P82A304	PLCC-68	C
P82A305	PLCC-68	C
P82A306	PLCC-68	C
CS8230	—	Standard CHIPSet (Note 3)

NOTES

1. PLCC = Plastic Leaded Chip Carrier 84 Pins
2. C = Commercial Range, 0° to 70°C, V_{DD} = 4.75 to 5.25 V
3. CS8230 consists of P82C301, P82C302, P82A303, P82A304, 2 of P82A305, P82A306.

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