CMOS
DATA BOOK

CYPRESS SEMICONDUCTOR

CMOS RAMs-PROMs
PLDs-LOGIC

CYPRESS
SEMICONDUCTOR

CMOS
DATA BOOK

CYPRESS SEMICONDUCTOR™

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How To Use This Book

This book has been organized by product type, beginning with Product Information. The products then follow, beginning with RAMs, then PROMs, PLDs, LOGIC, and finally the BridgeMOS™ product family. FIFO products are included in the LOGIC section. Within each section, data sheets are arranged in order of part number. Quality and Reliability aspects follow next, then a compilation of various Application Briefs, and finally Thermal Data and Packages.

A Numeric Device Index is included after the Table of Contents that identifies products by numeric order, rather than by device type which is how the manual is set up. To further help you in identifying parts, a Product Line Cross Reference is in Product Information. Use it to find the Cypress part number that is comparable to another manufacturer's part number.

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Cypress Semiconductor Background

Cypress Semiconductor was founded in April of 1983, became a public company in May 1986, and has established itself as a leader in high performance CMOS products. The Cypress CMOS product line is targeted to replace slower bipolar and NMOS products with higher reliability, high speed and low power. The initial process employed 1.2 micron geometries. Cypress has now placed into production a submicron (0.8 micron) process, further enhancing density and performance at manageable power levels.

Cypress products fall into three families: High Speed Static RAMs, Programmable Products, and Logic. Members of the Static RAM family include devices in densities of 64 bits to 64K bits and performance from 7 to 35 ns. The various organizations from 16 x 4, 256 x 4 through 64K x 1, 8K x 8, and 16K x 4 provide field applications in large mainframes, high speed controllers, communications, and graphics display.

Cypress Programmable Products consist of high speed CMOS PROMs and Programmable Logic Devices (PLDs), both employing an EPROM programming element. Like the High Speed Static RAM family, these products are the natural choice to replace older devices, manufactured in bipolar technology, because they provide superior performance at one half of the power consumption. Densities range from 4K bits to 256K in byte wide organization. To support new programmable products Cypress introduced the QuickPro programming system (CY3000). A single, IBM PC compatible board is available to program all Cypress PLDs and PROMs. The programming is updated via floppy disk, thereby allowing for quick support from Cypress Semiconductor on new products.

Logic products include a 16-bit slice, the CY7C9101, and support devices, as well as a family of FIFOs that range from 64 x 4 to 2048 x 9. FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed while the results may be processed or distributed at a speed commensurate with need.

Cypress' semiconductors are "Made in USA". Situated in California's Silicon Valley and Round Rock (Austin) Texas, Cypress houses R&D, design, wafer fabrication, assembly, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. In many other semiconductor facilities, wafers are fabricated in Class 100 environments, often under laminar flow hoods only. At the Texas Facility the entire wafer fabrication area is specified to be a class 1 environment. This means that the ambient air has less than 1 particulate of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.2 degree Fahrenheit tolerance; filtered air is completely exchanged >10 times each minute throughout the fab; critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is just as critical. Assembly is done in a clean room until the silicon die is sealed in a package. Lead frames are handled in carriers or cassettes through the entire operation. Automated robots remove and replace parts into cassettes. Using sophisticated automated equipment, parts are assembled and tested in less than five days. The Cypress assembly line is the most flexible, automated line in the United States.

The Cypress motto has always been "only the best". The best facilities, the best equipment, the best employees . . . all striving to make the best CMOS product. Cypress has grown very quickly to become "the best".

Cypress CMOS Technology

In the last decade, there has been a tremendous need for high performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor has overcome the classically held perceptions that CMOS is a moderate performance technology. That places its product lines ahead of its bipolar competitors in all three areas.

Cypress initially introduced a 1.2 micron "N" well technology with double layer poly, single layer metal and an EPROM capability. The process employs lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latchup characteristics associated with the older CMOS technologies.

To maintain our leadership position in CMOS Technology, Cypress has introduced a sub-micron technology into production. This process reduces the channel length from the current 1.2 microns to 0.8 microns. This sub-micron breakthrough makes Cypress' CMOS the most advanced production process in the world.

To further enhance the technology from the reliability direction, improvements have been incorporated in the process and design, minimizing electrostatic discharge and input signal clipping problems.

Finally, although not a requirement in the high performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages, without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latchup have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high performance MOS and bipolar products. Although in its earliest years MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2 and 0.8 micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2000 volts and 0.4 milli-joules, more than twice the energy level specified by MIL STD 883C.

Latchup, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures, and care in the physical layout of the products.

The Cypress CMOS technology has been carefully designed, creating products that are "only the best" in high speed, excellent reliability, and low power.

Military Overview

Introduction

Success at any endeavor requires a high level of dedication to the task. Cypress Semiconductor has demonstrated its dedication through its corporate commitment to support the military marketplace. The commitment starts with product design. All products that are designed on our state-of-the-art CMOS processes must meet the full −55 to +125 degree C operational criteria for military use. The commitment continues with the 1986 DESC certification of our automated U.S. facility in San Jose, California. The commitment shows in our dedication to meet and exceed the stringent quality and reliability requirements of MIL-STD-883 and MIL-M-38510. It shows in Cypress' participation in each of the military processing programs: 883C-Compliant, SMD (Standard Military Drawing) and JAN. Finally, our commitment shows in our leadership position in special packages for military use.

Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out on our industry-leading 0.8 micron CMOS process. Cypress is able to offer a family of products that are industry leaders in density, low operating current and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCC's and flatpacks so often used on military programs.

DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Level B CMOS Microcircuits (copy attached). This certification not only provided Cypress with the ability to qualify product for JAN use, but it also benefits all of our customers by acknowledging that our San Jose facility has the necessary documentation and procedures in place to manufacture product to the most stringent of quality and reliability requirements. Our wafer fabrication facility is a Class 10 manufacturing environment and our assembly facility is also a clean room. In addition, our highly automated assembly facility is entirely located in the U.S.A. and is capable of handling virtually any hermetic package configuration.

Quality and Reliability

MIL-STD-883 and MIL-M-38510 spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability and Process Flows for further details.

Military Product Offerings

Cypress offers three different levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883, Revision C.

Secondly, selected products are available to the SMD (Standard Military Drawing) program supervised by DESC. These products are not only fully 883-C compliant but they are also screened to the electrical requirements of the applicable military drawing.

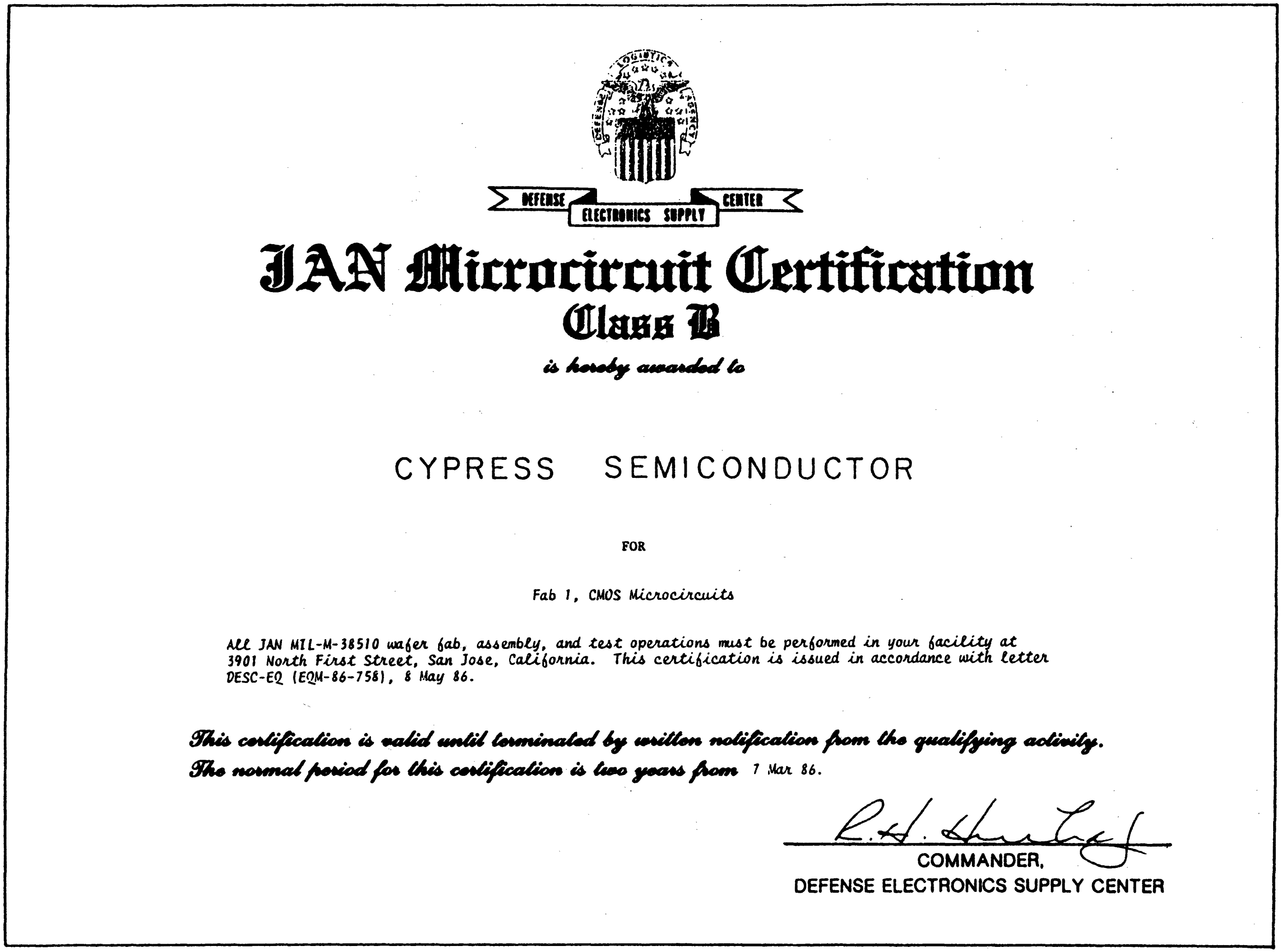
Third, selected products are available as JAN devices. These products are processed in full accordance with MIL-M-38510 and screened to the electrical requirements of the applicable JAN slash sheet.

Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader and appreciation of the variety of packages offered. Included are cerdips, windowed cerdips, leadless chip carriers (LCC's), leadless chip carriers with windows for reprogrammable products, cerpack and bottom-brazed flatpacks and pin grid arrays. As indicated above, all of these packages are assembled in the U.S. in our highly automated San Jose plant.

Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our quality and reliability programs, our support of all levels of military processing and by our leadership in special packaging.



DEFENSE LOGISTICS AGENCY

DEFENSE ELECTRONICS SUPPLY CENTER

JAN Microcircuit Certification
Class B

is hereby awarded to

CYPRESS SEMICONDUCTOR

FOR

Fab 1, CMOS Microcircuits

All JAN MIL-M-38510 wafer fab, assembly, and test operations must be performed in your facility at 3901 North First Street, San Jose, California. This certification is issued in accordance with letter DESC-EQ (EQM-86-758), 8 May 86.

This certification is valid until terminated by written notification from the qualifying activity. The normal period for this certification is two years from 7 Mar 86.

COMMANDER,
DEFENSE ELECTRONICS SUPPLY CENTER

0105–1

Product Selection Guide

	Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
SRAMs	64	16 x 4—Inverting	16	CY7C189	t_{AA} = 15, 25	55 @ 25	D, L, P
	64	16 x 4—Non-Inverting	16	CY7C190	t_{AA} = 15, 25	55 @ 25	D, L, P
	64	16 x 4—Inverting	16	CY74S189	t_{AA} = 35	90 @ 35	D, P
	64	16 x 4—Inverting	16	CY27S03A	t_{AA} = 25, 35	90 @ 25	D, L, P
	64	16 x 4—Non-Inverting	16	CY27S07A	t_{AA} = 25, 35	90 @ 25	D, L, P
	64	16 x 4—Inv. Low Power	16	CY27LS03M	t_{AA} = 65	38 @ 65	D, L
	1024	256 x 4	22	CY7C122	t_{AA} = 15, 25, 35	60 @ 25	D, L, P, S
	1024	256 x 4	24S	CY7C123	t_{AA} = 7, 12, 15	120 @ 7	D, L, P
	1024	256 x 4	22	CY9122/91L22	t_{AA} = 25, 35, 45	120 @ 25	D, P
	1024	256 x 4	22	CY93422A/93L422A	t_{AA} = 35, 45, 60	80 @ 45	D, P
	4096	4096 x 1—CS Power Down	18	CY7C147	t_{AA} = 25, 35, 45	80/10 @ 35	D, L, P
	4096	4096 x 1—CS Power Down	18	CY2147/21L47	t_{AA} = 35, 45, 55	125/25 @ 35	D, P
	4096	1024 x 4—CS Power Down	18	CY7C148	t_{AA} = 25, 35, 45	80/10 @ 35	D, L, P
	4096	1024 x 4—CS Power Down	18	CY2148/21L48	t_{AA} = 35, 45, 55	120/20 @ 35	D, P
	4096	1024 x 4	18	CY7C149	t_{AA} = 25, 35, 45	80 @ 35	D, L, P
	4096	1024 x 4	18	CY2149/21L49	t_{AA} = 35, 45, 55	120 @ 35	D, P
	4096	1024 x 4—Separate I/O	24S	CY7C150	t_{AA} = 15, 25, 35	90 @ 25	D, L, P
	8192	1024 x 8—Dual Port	48	CY7C130	t_{AA} = 35, 45, 55	120 @ 35	D, L, P
	8192	1024 x 8—Dual Port (Slave)	48	CY7C140	t_{AA} = 35, 45, 55	120 @ 35	D, L, P
	16384	2048 x 8—CS Power Down	24S	CY7C128	t_{AA} = 25, 35, 45, 55	90/20 @ 55	D, L, P, S
	16384	2048 x 8—CS Power Down	24	CY6116	t_{AA} = 35, 45, 55	120/20 @ 45	D, L
	16384	16384 x 1—CS Power Down	20	CY7C167/L	t_{AA} = 25, 35, 45	45/15 @ 25	D, L, P, S
	16384	4096 x 4—CS Power Down	20	CY7C168/L	t_{AA} = 25, 35, 45	70/15 @ 25	D, L, P, S
	16384	4096 x 4	20	CY7C169/L	t_{AA} = 25, 35, 40	70 @ 25	D, L, P
	16384	4096 x 4—Output Enable	22S	CY7C170	t_{AA} = 25, 35, 45	90 @ 45	D, L, P
	16384	4096 x 4—Separate I/O	24S	CY7C171/L	t_{AA} = 25, 35, 45	70/10 @ 25	D, L, P, S
	16384	4096 x 4—Separate I/O	24S	CY7C172/L	t_{AA} = 25, 35, 45	70/10 @ 25	D, L, P, S
	16384	2048 x 8—Dual Port	48	CY7C132	t_{AA} = 35, 45, 55	120 @ 35	D, L, P
	16384	2048 x 8—Dual Port (Slave)	48	CY7C142	t_{AA} = 35, 45, 55	120 @ 35	D, L, P
	65536	8192 x 8—CS Power Down	28S	CY7C185/L	t_{AA} = 35, 45, 55	100/20/1 @ 35	D, L, P, S
	65536	8192 x 8—CS Power Down	28	CY7C186/L	t_{AA} = 35, 45, 55	100/20/1 @ 35	D, P
	65536	16384 x 4—CS Power Down	22S	CY7C164/L	t_{AA} = 25, 35, 45	70/20/1 @ 25	D, L, P, S
	65536	16384 x 4—Output Enable	24S	CY7C166/L	t_{AA} = 25, 35, 45	70/20/1 @ 25	D, L, P, S
	65536	16384 x 4—Separate I/O	28S	CY7C161/L	t_{AA} = 25, 35, 45	70/20/1 @ 25	D, L, P, S
	65536	16384 x 4—Separate I/O	28S	CY7C162/L	t_{AA} = 25, 35, 45	70/20/1 @ 25	D, L, P, S
	65536	65536 x 1—CS Power Down	22S	CY7C187/L	t_{AA} = 25, 35, 45	70/20/1 @ 25	D, L, P, S
	262144	32768 x 8—CS Power Down	28	CY7C198	t_{AA} = 35, 45, 55	100/20 @ 35	D, P
	262144	32768 x 8—CS Power Down	28S	CY7C199	t_{AA} = 35, 45, 55	100/20 @ 35	D, P
	262144	65536 x 4—CS Power Down	24S	CY7C194	t_{AA} = 25, 35, 45	70/20 @ 25	D, P
	262144	65536 x 4—Separate I/O	28S	CY7C191	t_{AA} = 25, 35, 45	70/20 @ 25	D, P
	262144	65536 x 4—Separate I/O	28S	CY7C192	t_{AA} = 25, 35, 45	70/20 @ 25	D, P
	262144	262144 x 1—CS Power Down	24S	CY7C197	t_{AA} = 25, 35, 45	70/20 @ 25	D, P
PROMs	4096	512 x 8—Registered	24S	CY7C225	$t_{SA/CO}$ = 25/12, 30/15	90	D, L, P
	8192	1024 x 8—Registered	24S	CY7C235	$t_{SA/CO}$ = 30/15, 40/20	90	D, L, P
	8192	1024 x 8	24S	CY7C281	t_{AA} = 30, 45	90	D, L, P
	8192	1024 x 8	24	CY7C282	t_{AA} = 30, 45	90	D, L, P
	16384	2048 x 8—Registered	24S	CY7C245/L	$t_{SA/CO}$ = 25/12, 35/15	100/60	D, L, P, Q, W, S
	16384	2048 x 8	24S	CY7C291/L	t_{AA} = 35, 50	90/60	D, L, P, Q, W, S
	16384	2048 x 8	24	CY7C292/L	t_{AA} = 35, 50	90/60	D, P
	65536	8192 x 8—CS Power Down	24S	CY7C261	t_{AA} = 35, 40, 45, 55	100/30	D, L, P, Q, W, S
	65536	8192 x 8	24S	CY7C263	t_{AA} = 35, 40, 45, 55	100	D, L, P, Q, W, S
	65536	8192 x 8	24	CY7C264	t_{AA} = 35, 40, 45, 55	100	D, P
	65536	8192 x 8—Registered, Diagnostic	28S	CY7C269	$t_{SA/CO}$ = 40/20, 50/25	100	D, L, P, Q, W, S
	65536	8192 x 8—Registered, Diagnostic	32	CY7C268	$t_{SA/CO}$ = 40/20, 50/25	100	D, L, Q, W
	131072	16384 x 8—CS Power Down	28S	CY7C251	t_{AA} = 45, 55, 65	100/30	D, L, P, Q, W, S
	131072	16384 x 8	28S	CY7C253	t_{AA} = 45, 55, 65	100	D, L, P, Q, W, S
	131072	16384 x 8	28	CY7C254	t_{AA} = 45, 55, 65	100	D, P
	262144	32768 x 8—CS Power Down	28	CY7C271	t_{AA} = 55, 65, 75	100/30	D, L, P, Q, W, S

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C.

Military temperature range (−55°C to +125°C) product processed to MIL-STD-883 Revision C is also available. Speed and power selections may vary from those above.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP or LCC. PLCC and SOIC packages are available on some products.

All power supplies are V_{CC} = 5V ± 10%.

22S stands for 22-pin 300 mil. 24S stands for 24-pin 300 mil. 28S stands for 28-pin 300 mil.

F and K packages are special order only.

Package Code:

D = CERAMIC DIP
F = FLATPAK
G = PIN GRID ARRAY
J = PLCC
K = CERPAK
L = LCC
P = PLASTIC
Q = WINDOWED LCC
S = SOIC
W = WINDOWED CERDIP

Product Selection Guide (Continued)

	Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
PLDs	PALC20	16L8	20	CYPALC16L8/L	t_{PD} = 20	70/45	D, L, P, Q, W
	PALC20	16R8	20	CYPALC16R8/L	$t_{S/CO}$ = 20/15	70/45	D, L, P, Q, W
	PALC20	16R6	20	CYPALC16R6/L	$t_{PD/S/CO}$ = 20/20/15	70/45	D, L, P, Q, W
	PALC20	16R4	20	CYPALC16R4/L	$t_{PD/S/CO}$ = 20/20/15	70/45	D, L, P, Q, W
	PLDC24	22V10—Macro Cell	24S	CYPALC22V10/L	$t_{PD/S/CO}$ = 25/15/15	90/55	D, L, P, Q, W, J
	PLDC24	20G10—Generic	24S	CYPLDC20G10	$t_{PD/S/CO}$ = 25/15/15	55	D, L, P, Q, W, J
	PLDC28	7C330—State Machine	28S	CY7C330	50 MHz	120/30	D, L, P, Q, W, J
	PLDC28	7C331—Asynchronous	28S	CY7C331	25 MHz	180/90	D, L, P, Q, W, J
	PLDC28	7C332—Combinatorial	28S	CY7C332	40 MHz	180/90	D, L, P, Q, W, J
FIFOs	256	64 x 4—Cascadeable	16	CY3341	1.2, 2 MHz	45	D, P
	256	64 x 4—Cascadeable	16	CY7C401	5, 10, 15 MHz	75	D, L, P, S
	256	64 x 4—Cascadeable/OE	16	CY7C403	10, 15, 25 MHz	75	D, L, P, S
	320	64 x 5—Cascadeable	18	CY7C402	5, 10, 15 MHz	75	D, L, P, S
	320	64 x 5—Cascadeable/OE	18	CY7C404	10, 15, 25 MHz	75	D, L, P, S
	512	64 x 8—Cascadeable/OE	28S	CY7C408	15, 25, 35 MHz	120	D, L, P, S
	576	64 x 9—Cascadeable	28S	CY7C409	15, 25, 35 MHz	120	D, L, P, S
	4608	512 x 9—Cascadeable	28	CY7C412	30, 40, 65 MHz	100 @ 20 MHz	D, L, P, S
	9216	1024 x 9—Cascadeable	28	CY7C424	30, 40, 65 MHz	100 @ 20 MHz	D, L, P, S
	18432	2048 x 9—Cascadeable	28	CY7C429	30, 40, 65 MHz	100 @ 20 MHz	D, L, P, S
LOGIC		2901—4 Bit Slice	40	CY7C901	t_{CLK} = 23, 31	70	D, L, P, J
		2901—4 Bit Slice	40	CY2901	C	140	D, P
		4 x 2901—16 Bit Slice	64	CY7C9101	t_{CLK} = 30, 40	60	D, L, P, G, J
		2909—Sequencer	28	CY7C909	t_{CLK} = 30, 40	55	D, L, P, J
		2911—Sequencer	20	CY7C911	t_{CLK} = 30, 40	55	D, L, P, J
		2909—Sequencer	28	CY2909	A	70	D, P
		2911—Sequencer	20	CY2911	A	70	D, P
		2910—Controller (17 Word Stack)	40	CY7C910	t_{CLK} = 40, 50, 93	100	D, L, P, J
		2910—Controller (9 Word Stack)	40	CY2910	A	170	D, L, P, J
		16 x 16—Multiplier	64	CY7C516	t_{MC} = 38, 45, 55, 75	100 @ 10 MHz	D, L, P, G, J
		16 x 16—Multiplier	64	CY7C517	t_{MC} = 38, 45, 55, 75	100 @ 10 MHz	D, L, P, G, J
		16 x 16—Multiplier/Accumulator	64	CY7C510	t_{MC} = 45, 55, 65, 75	100 @ 10 MHz	D, L, P, G, J

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C.

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All power supplies are V_{CC} = 5V ±10%.

22S stands for 22-pin 300 mil. 24S stands for 24-pin 300 mil. 28S stands for 28-pin 300 mil.

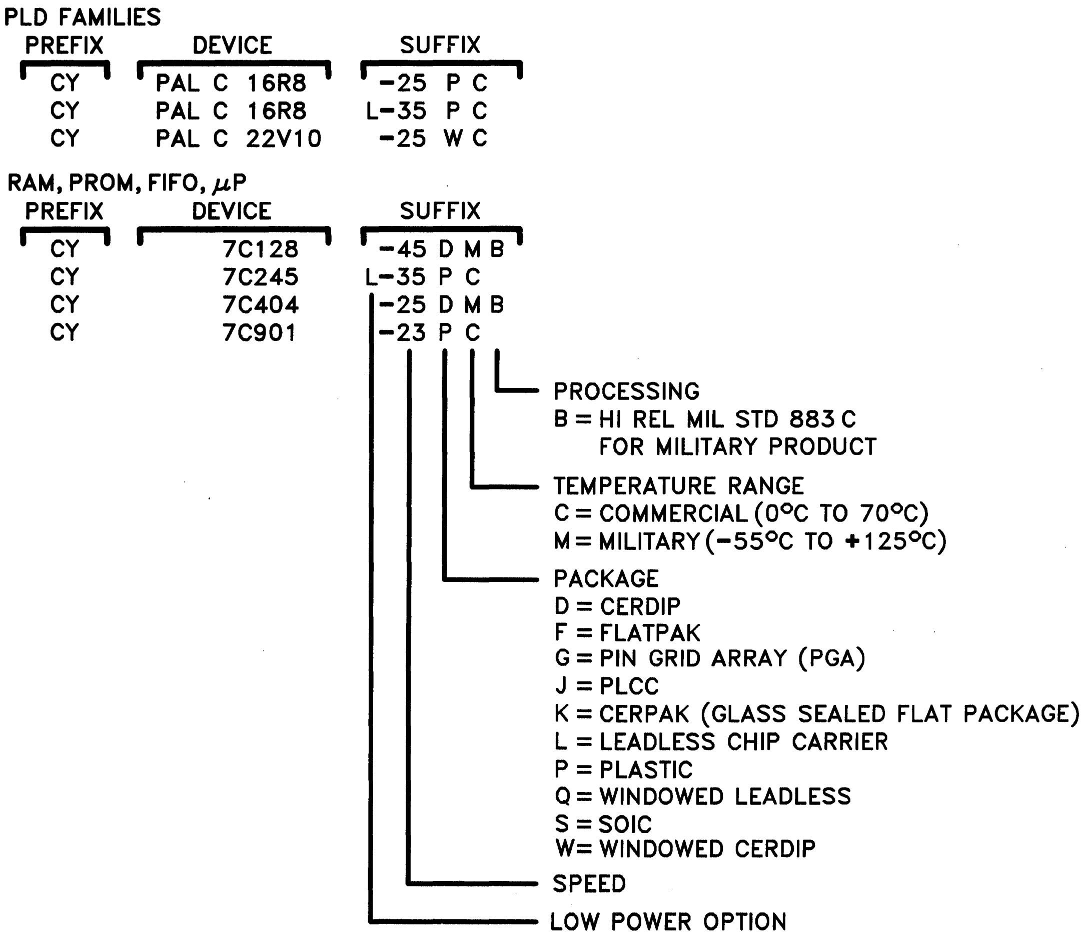
F and K packages are special order only.

Package Code:

D = CERAMIC DIP
F = FLATPAK
G = PIN GRID ARRAY
J = PLCC
K = CERPAK
L = LCC
P = PLASTIC
Q = WINDOWED LCC
S = SOIC
W = WINDOWED CERDIP

Ordering Information

Specific ordering codes are indicated in the detailed data sheets. In general, the product codes follow the format below:



PLD FAMILIES

PREFIX	DEVICE	SUFFIX
CY	PAL C 16R8	-25 P C
CY	PAL C 16R8	L-35 P C
CY	PAL C 22V10	-25 W C

RAM, PROM, FIFO, μP

PREFIX	DEVICE	SUFFIX
CY	7C128	-45 D M B
CY	7C245	L-35 P C
CY	7C404	-25 D M B
CY	7C901	-23 P C

PROCESSING
B = HI REL MIL STD 883 C
FOR MILITARY PRODUCT

TEMPERATURE RANGE
C = COMMERCIAL (0°C TO 70°C)
M = MILITARY (−55°C TO +125°C)

PACKAGE
D = CERDIP
F = FLATPAK
G = PIN GRID ARRAY (PGA)
J = PLCC
K = CERPAK (GLASS SEALED FLAT PACKAGE)
L = LEADLESS CHIP CARRIER
P = PLASTIC
Q = WINDOWED LEADLESS
S = SOIC
W = WINDOWED CERDIP

SPEED

LOW POWER OPTION

0018-1

i.e. CY7C128-35PC, CYPALC16R8L-25PC

Cypress FSCM #65786

Product Line Cross Reference

CYPRESS	CYPRESS
2147-35C	7C147-35C
2147-45C	2147-35C
2147-45C	7C147-45C
2147-45M	7C147-45M
2147-55C	2147-45C
2147-55M	2147-45M
2148-35C	21L48-35C
2148-35C	7C148-35C
2148-35M	7C148-35M
2148-45C	21L48-45C
2148-45C	2148-35C
2148-45M	7C148-45M
2148-45M	2148-35M
2148-55C	2148-45C
2148-55C	21L48-55C
2148-55M	2148-45M
2149-35C	21L49-35C
2149-35C	7C149-35C
2149-35M	7C149-35M
2149-45C	21L49-45C
2149-45M	2149-35M
2149-45M	7C149-45M
2149-55C	2149-45C
2149-55C	21L49-55C
2149-55M	2149-45M
21L48-35C	7C148-35C
21L48-45C	21L48-35C
21L48-45C	7C148-45C
21L48-55C	21L48-45C
21L49-35C	7C149-25C
21L49-45C	21L49-35C
21L49-45C	7C149-45C
21L49-55C	21L49-45C
27S03AC	7C189-25C
27S03AM	7C189-25M
27S03C	27S03AC
27S03C	74S189C
27S03M	54S189M
27S03M	27S03AM
27S07AC	7C190-25C
27S07AM	7C190-25M
27S07C	27S07AC
27S07M	27S07AM
27S07M	7C190-25M
2901CC	7C901-31C
2901CM	7C901-32M
2909AC	7C909-40C
2909AM	7C909-40M
2910AC	7C910-50C
2910AM	7C910-51M
2910C	2910AC
2910M	2910AM
2911AC	7C911-40C
2911AM	7C911-40M
3341C	3341-2C
3341M	3341-2M
3341-2C	7C401-5C+
3341-2C	7C402-5C
54S189M	27S03M
6116-45C	6116-35C
6116-55C	6116-45C
6116-55M	6116-45M
74S189C	27S03C
7C122-25C	7C122-15C+
7C122-35C	7C122-25C
7C122-35M	7C122-25M
7C123-12C	7C123-7C
7C128-35C	7C128-25C
7C128-45C	7C128-35C
7C128-45M	7C128-35M+
7C128-55C	7C128-45C+
7C128-55M	7C128-45M+
7C130-45C	7C130-35C
7C130-55C	7C130-45C
7C130-55M	7C130-45M
7C132-45C	7C132-35C
7C132-55C	7C132-45C
7C132-55M	7C132-45M
7C147-35C	7C147-25C+
7C147-45C	7C147-35C
7C147-45M	7C147-35M
7C148-35C	7C148-25C+
7C148-45C	7C148-35C
7C148-45M	7C148-35M
7C149-35C	7C149-25C+
7C149-45C	7C149-35C
7C149-45M	7C149-35M
7C150-25C	7C150-15C
7C150-35C	7C150-25C
7C150-35M	7C150-25M
7C161-35C	7C161-25C
7C161-45C	7C161-35C
7C161-45M	7C161-35M
7C162-35C	7C162-25C
7C162-45C	7C162-35C
7C162-45M	7C162-35M
7C164-35C	7C164-25C
7C164-45C	7C164-35C
7C164-45M	7C164-35M
7C166-35C	7C166-25C
7C166-45C	7C166-35C
7C166-45M	7C166-35M
7C167L-35C	7C167L-25C
7C167-25C	7C167L-25C
7C167-35C	7C167-25C
7C167-45C	7C167L-35C
7C167-45M	7C167-35M+
7C168L-35C	7C168L-25C
7C168-25C	7C168L-25C
7C168-35C	7C168-25C
7C168-45C	7C168L-35C
7C168-45M	7C168-35M+
7C169L-35C	7C169L-25C
7C169-25C	7C169L-25C
7C169-35C	7C169-25C
7C169-40C	7C169L-35C
7C169-40M	7C169-35M+
7C170-35C	7C170-25C
7C170-45C	7C170-35C+
7C170-45M	7C170-35M+
7C171L-35C	7C171L-25C
7C171-25C	7C171L-25C
7C171-35C	7C171-25C
7C171-45C	7C171L-35C
7C171-45M	7C171-35M+
7C172L-35C	7C172L-25C
7C172-25C	7C172L-25C
7C172-35C	7C172-25C
7C172-45C	7C172L-35C
7C172-45M	7C172-35M+
7C185-45C	7C185-35C
7C185-55C	7C185-45C
7C185-55M	7C185-45M
7C186-45C	7C186-35C
7C186-55C	7C186-45C
7C186-55M	7C186-45M
7C187-35C	7C187-25C
7C187-45C	7C187-35C
7C187-45M	7C187-35M
7C189-18C	7C189-15C
7C189-25C	7C189-15C+
7C190-18C	7C190-15C
7C190-25C	7C190-15C+
7C225-30C	7C225-25C
7C225-30M	7C225-25M
7C225-40C	7C225-30C
7C225-40M	7C225-35M
7C235-40C	7C235-30C
7C245L-35C	7C245-35C+
7C245L-45C	7C245L-35C
7C245-35C	7C245-25C
7C245-45C	7C245-35C
7C245-45M	7C245-35M
7C251-55C	7C251-45C
7C251-65C	7C251-55C
7C251-65M	7C251-55M
7C253-55C	7C253-45C
7C253-65C	7C253-55C
7C253-65M	7C253-55M
7C254-55C	7C254-45C
7C254-65C	7C254-55C
7C254-65M	7C254-55M
7C261-45C	7C261-35C
7C261-55C	7C261-45C
7C261-55M	7C261-45M
7C263-45C	7C263-35C
7C263-55C	7C263-45C
7C263-55M	7C263-45M
7C264-45C	7C264-35C
7C264-55C	7C264-45C
7C264-55M	7C264-45M
7C268-50C	7C268-40C+
7C268-60C	7C268-50C
7C268-60M	7C268-50M+
7C269-50C	7C269-40C+
7C269-60C	7C269-50C
7C269-60M	7C269-50M+
7C281-45C	7C281-30C
7C282-45C	7C282-30C+
7C291L-35C	7C291-35C+
7C291L-50C	7C291L-35C
7C291-35C	7C291-25C+
7C291-50C	7C291-35C
7C291-50M	7C291-35M
7C292L-35C	7C292-35C+
7C292L-50C	7C292L-35C
7C292-35C	7C292-25C+
7C292-50C	7C292-35C
7C401-10C	7C401-15C
7C401-10M	7C401-15M
7C401-5C	7C401-10C
7C402-10C	7C402-15C
7C402-10M	7C402-15M
7C402-5C	7C402-10C
7C403-10C	7C403-15C
7C403-10M	7C403-15M
7C403-15C	7C403-25C
7C403-15M	7C403-25M
7C404-10C	7C404-15C
7C404-10M	7C404-15M
7C404-15C	7C404-25C
7C404-15M	7C404-25M
7C408-15C	7C408-25C
7C408-15M	7C408-25M
7C408-25C	7C408-35C
7C408-25M	7C408-35M
7C409-15C	7C409-25C
7C409-15M	7C409-25M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
— = functionally equivalent

Product Line Cross Reference (Continued)

CYPRESS	CYPRESS
7C409-25C	7C409-35C
7C409-25M	7C409-35M
7C412-12C	7C412-15C
7C412-12M	7C412-15M
7C412-15C	7C412-25C
7C412-15M	7C412-20M
7C412-20C	7C412-25C
7C412-20M	7C412-25M
7C510-55C	7C510-45C
7C510-65C	7C510-55C
7C510-65M	7C510-55M
7C510-75C	7C510-65C
7C510-75M	7C510-65M
7C516-45C	7C516-38C
7C516-55C	7C516-45C
7C516-55M	7C516-42M
7C516-65C	7C516-55C
7C516-65M	7C516-55M
7C516-75C	7C516-65C
7C516-75M	7C516-65M
7C517-55C	7C517-45C
7C517-65C	7C517-55C
7C517-65M	7C517-55M
7C517-75C	7C517-65C
7C517-75M	7C517-65M
7C901-31C	7C901-23C+
7C901-32M	7C901-27M
7C909-40C	7C909-30C
7C909-40M	7C909-30M
7C9101-40C	7C9101-30C
7C9101-45M	7C9101-35M
7C910-50C	7C910-40C
7C910-51M	7C910-46M
7C910-93C	7C910-50C
7C910-99M	7C910-51M
7C911-40C	7C911-30C
7C911-40M	7C911-30M
9122-25C	91L22-25C
9122-25C	7C122-15C
9122-35C	9122-25C
9122-35C	91L22-35C
9122-45C	93L422C
91L22-25C	7C122-25C
91L22-35C	7C122-35C
91L22-45C	93L422AC
93422AC	9122-35C
93422AC	7C122-35C
93422AM	7C122-35M
93422C	93L422AC
93422M	93422AM
93422M	93L422AM
93L422AC	91L22-45C

CYPRESS	CYPRESS
93L422AC	7C122-35C
93L422AM	7C122-35M
93L422C	93L422AC
93L422M	93L422AM
PALC16L8L-35C	PALC16L8L-25C
PALC16L8-25C	PALC16L8L-25C
PALC16L8-30M	PALC16L8-20M
PALC16L8-35C	PALC16L8-25C
PALC16L8-40M	PALC16L8-30M
PALC16R4L-35C	PALC16R4L-25C
PALC16R4-25C	PALC16R4L-25C
PALC16R4-30M	PALC16R4-20M
PALC16R4-35C	PALC16R4-25C
PALC16R4-40M	PALC16R4-30M
PALC16R6L-35C	PALC16R6L-25C
PALC16R6-25C	PALC16R6L-25C
PALC16R6-30M	PALC16R6-20M
PALC16R6-35C	PALC16R6-25C
PALC16R6-40M	PALC16R6-30M
PALC16R8L-35C	PALC16R8L-25C
PALC16R8-25C	PALC16R8L-25C
PALC16R8-30M	PALC16R8-20M
PALC16R8-35C	PALC16R8-25C
PALC16R8-40M	PALC16R8-30M
PALC22V10L-25C	PALC22V10-25C+
PALC22V10L-35C	PALC22V10L-25C
PALC22V10-35C	PALC22V10-25C
PALC22V10-40M	PALC22V10-30M
PLDC20G10-35C	PLDC20G10-25C
PLDC20G10-40M	PLDC20G10-30M

AMD	CYPRESS
PREFIX:Am	PREFIX:CY
PREFIX:SN	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
2130-100C	7C130-55C
2130-120C	7C130-55C
2130-70C	7C130-55C
2147-35C	2147-35C
2147-45C	2147-45C
2147-45M	2147-45M
2147-55C	2147-55C
2147-55M	2147-55M
2147-70C	2147-55C
2147-70M	2147-55M
2148-35C	2148-35C
2148-35M	2148-35M
2148-45C	2148-45C

AMD	CYPRESS
2148-45M	2148-45M
2148-55C	2148-55C
2148-55M	2148-55M
2148-70C	2148-55C
2148-70M	2148-55M
2149-35C	2149-35C
2149-45C	2149-45C
2149-45M	2149-45M
2149-55C	2149-55C
2149-55M	2149-55M
2149-70C	2149-55C
2149-70M	2149-55M
2167-35C	7C167-35C
2167-35M	7C167-35M
2167-45C	7C167-45C
2167-45M	7C167-45M
2167-55C	7C167-45C
2167-55M	7C167-45M
2167-70C	7C167-45C
2167-70M	7C167-45M
2168-35C	7C168-35C
2168-45C	7C168-45C
2168-45M	7C168-45M
2168-55C	7C168-45C
2168-55M	7C168-45M
2168-70C	7C168-45C
2168-70M	7C168-45M
2169-40C	7C169-40C
2169-50C	7C169-40C
2169-50M	7C169-40M
2169-70C	7C169-40C
2169-70M	7C169-40M
21L47-45C	7C147-45C
21L47-55C	7C147-45C
21L47-70C	7C147-45C
21L48-45C	21L48-45C
21L48-55C	21L48-55C
21L48-70C	21L48-55C
21L49-45C	21L49-45C
21L49-55C	21L49-55C
21L49-70C	21L49-55C
27LS03C	27LS03C
27LS03M	27LS03M+
27LS07C	27S07C+
27LS191C	7C292-35C
27LS291C	7C291-35C
27LS291M	7C291-35M
27PS181AC	7C282-45C
27PS181AM	7C282-45M+
27PS181C	7C282-45C
27PS181M	7C282-45M+
27PS191AC	7C292-50C

AMD	CYPRESS
27PS191AM	7C292-50M+
27PS191C	7C292-50C
27PS191M	7C292-50M+
27PS281AC	7C281-45C
27PS281AM	7C281-45M+
27PS281C	7C281-45C
27PS281M	7C281-45M+
27PS291AC	7C291-50C
27PS291AM	7C291-50M+
27PS291C	7C291-50C
27PS291M	7C291-50M+
27S03AC	27S03AC
27S03AM	27S03AM
27S03C	27S03C
27S03M	27S03M
27S07AC	27S07AC
27S07AM	27S07AM
27S07C	27S07C
27S07M	27S07M
27S181AC	7C282-30C
27S181AM	7C282-45M
27S181C	7C282-45C
27S181M	7C282-45M
27S191AC	7C292-35C
27S191AM	7C292-50M
27S191C	7C292-50C
27S191M	7C292-50M
27S25AC	7C225-30C
27S25AM	7C225-35M
27S25C	7C225-40C
27S25M	7C225-40M
27S25SAC	7C225-25C
27S25SAM	7C225-35M
27S281AC	7C281-30C
27S281AM	7C281-45M
27S281C	7C281-45C
27S281M	7C281-45M
27S291AC	7C291-35C
27S291AM	7C291-50M
27S291C	7C291-50C
27S291M	7C291-50M
27S35AC	7C235-30C
27S35AM	7C235-40M
27S35C	7C235-40C
27S35M	7C235-40M
27S45AC	7C245-35C
27S45AM	7C245-45M
27S45C	7C245-45C
27S45M	7C245-45M
27S45SAC	7C245-25C
27S49AC	7C264-45C
27S49AM	7C264-55M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
— = functionally equivalent

CYPRESS SEMICONDUCTOR

Product Line Cross Reference (Continued)

AMD	CYPRESS
27S49A-45C	7C264-45C
27S49C	7C264-55C
27S49M	7C264-55M
27S51C	7C254-55C
27S51M	7C254-65M
2841AC	3341C
2841AM	3341M
2841C	3341C
2841M	3341M
2901BC	2901CC
2901BM	2901CM
2901CC	2901CC
2901CM	2901CM
2909AC	2909AC
2909AM	2909AM
2909C	2909AC
2909M	2909M
2910AC	2910AC
2910AM	2910AM
2910C	2910C
2910M	2910M
2910-1C	2910C
2910-1M	2910M
2911AC	2911AC
2911AM	2911AM
2911C	2911AC
2911M	2911M
29516AM	7C516-55M
29516C	7C516-55C
29516M	7C516-55M
29517C	7C517-55C
29517M	7C517-55M
29701C	27S07C
29701M	27S07M
29703C	27S03C
29703M	27S03M
29C01BC	7C901-31C
29C01CC	7C901-31C
29C101C	7C9101-40C
29C101M	7C9101-35M
29C10AC	7C910-93C
29L516C	7C516-75C
29L516M	7C516-75M
29L517C	7C517-75C
29L517M	7C517-75M
3341C	3341C
3341M	3341M
54S189M	54S189M
74S189C	74S189C
9122-25C	9122-25C
9122-35C	9122-35C
9122-35M	7C122-35M
9128-100C	6116-55C
9128-120M	6116-55M
9128-150C	6116-55C
9128-150M	6116-55M
9128-200C	6116-55C
9128-200M	6116-55M
9128-70C	6116-55C
9128-90M	6116-55M
9150-20C	7C150-15C
9150-25C	7C150-25C
9150-25M	7C150-25M
9150-35C	7C150-35C
9150-35M	7C150-35M
9150-45C	7C150-35C
9150-45M	7C150-35M
91L22-35C	91L22-35C
91L22-35M	7C122-35M
91L22-45C	91L22-45C
91L22-45M	7C122-35M
91L22-60C	7C122-35C+
91L50-25C	7C150-25C
91L50-35C	7C150-35C
91L50-45C	7C150-35C
93422AC	93422AC
93422AM	93422AM
93422C	93422C
93422M	93422M
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
99C164-35C	7C164-35C
99C164-45C	7C164-45C
99C164-45M	7C164-45M
99C164-55C	7C164-45C
99C164-55M	7C164-45M
99C164-70C	7C164-45C
99C164-70M	7C164-45M
99C165-35C	7C166-35C
99C165-45C	7C166-45C
99C165-45M	7C166-45M
99C165-55C	7C166-45C
99C165-55M	7C166-45M
99C165-70C	7C166-45C
99C165-70M	7C166-45M
99C641-25C	7C187-25C+
99C641-35C	7C187-35C+
99C641-45C	7C187-45C+
99C641-45M	7C187-45M
99C641-55C	7C187-45C+
99C641-55M	7C187-45M
99C641-70C	7C187-45C+
99C641-70M	7C187-45M
99C68-35C	7C168-35C
99C68-45C	7C168-45C*
99C68-45M	7C168-45M*
99C68-55C	7C168-45C*
99C68-55M	7C168-45M*
99C68-70C	7C168-45C*
99C68-70M	7C168-45M*
99C88H-35C	7C186-35C
99C88H-45C	7C186-45C
99C88H-45M	7C186-45M+
99C88H-55C	7C186-55C
99C88H-55M	7C186-55M+
99C88H-70C	7C186-55C
99C88H-70M	7C186-55M+
99C88-10C	7C186-55C*
99C88-10M	7C186-55M*
99C88-12C	7C186-55C*
99C88-12M	7C186-55M*
99C88-15C	7C186-55C*
99C88-15M	7C186-55M*
99C88-20C	7C186-55C*
99C88-20M	7C186-55M*
99C88-70C	7C186-55C*
99C88-70M	7C186-55M*
99CL68-35C	7C168-35C
99CL68-45C	7C168-45C*
99CL68-45M	7C168-45M*
99CL68-55C	7C168-45C*
99CL68-55M	7C168-45M*
99CL68-70C	7C168-45C*
99CL68-70M	7C168-45M*
99CL88-10C	7C186-55C*
99CL88-12C	7C186-55C*
99CL88-15C	7C186-55C*
99CL88-70C	7C186-55C*
99CS88-10M	7C186-55M*
99CS88-12M	7C186-55M*
99CS88-15M	7C186-55M*
99CS88-20M	7C186-55M*
99CS88-70M	7C186-55M*
PAL16L8AC	PALC16L8-25C
PAL16L8ALC	PALC16L8-25C
PAL16L8ALM	PALC16L8-30M
PAL16L8AM	PALC16L8-30M
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M+
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8LC	PALC16L8-35C
PAL16L8LM	PALC16L8-40M
PAL16L8M	PALC16L8-40M
PAL16L8QC	PALC16L8L-35C
PAL16L8QM	PALC16L8-40M+
PAL16R4ALC	PALC16R4-25C
PAL16R4ALM	PALC16R4-30M
PAL16R4AM	PALC16R4-30M
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M+
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4LC	PALC16R4-35C
PAL16R4LM	PALC16R4-40M
PAL16R4M	PALC16R4-40M
PAL16R4QC	PALC16R4L-35C
PAL16R4QM	PALC16R4-40M+
PAL16R6AC	PALC16R6-25C
PAL16R6ALC	PALC16R6-25C
PAL16R6ALM	PALC16R6-30M
PAL16R6AM	PALC16R6-30M
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6LC	PALC16R6-35C
PAL16R6LM	PALC16R6-40M
PAL16R6M	PALC16R6-40M
PAL16R6QC	PALC16R6L-35C
PAL16R6QM	PALC16R6-40M+
PAL16R8AC	PALC16R8-25C
PAL16R8ALC	PALC16R8-25C
PAL16R8ALM	PALC16R8-30M
PAL16R8AM	PALC16R8-30M
PAL16R8A-4C	PALC16R8L-35C
PAL16R8A-4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8LC	PALC16R8-35C
PAL16R8LM	PALC16R8-40M
PAL16R8M	PALC16R8-40M
PAL16R8QC	PALC16R8L-35C
PAL16R8QM	PALC16R8-40M+
PAL22V10AC	PALC22V10-25C
PAL22V10AM	PALC22V10-30M
PAL22V10C	PALC22V10-35C
PAL22V10M	PALC22V10-40M

ANALOG—DEV	CYPRESS
PREFIX:ADSP	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:E	SUFFIX:L
SUFFIX:F	SUFFIX:F
SUFFIX:G	SUFFIX:G

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
— = functionally equivalent

Product Line Cross Reference (Continued)

ANALOG—DEV	CYPRESS
1010A	7C510-65C+
1010J	7C510-75C+
1010K	7C510-75C+
1010S	7C510-75M+
1010T	7C510-75M+
7C901-27M	7C901-32M
7C901-32M	2901CM

FAIRCHILD	CYPRESS
PREFIX:F	PREFIX:CY
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
SUFFIX:QB	SUFFIX:B
1600C45	7C187-45C+
1600C55	7C187-45C+
1600C70	7C187-45C+
1600M55	7C187-45M+
1600M70	7C187-45M+
1601C45	7C187-45C*
1601C55	7C187-45C*
1601C70	7C187-45C*
1601M55	7C187-45M*
1601M70	7C187-45M*
1620C25	7C164-25C+
1620C35	7C164-35C+
1620M35	7C164-35M+
1620M45	7C164-45M+
1621C25	7C164-25C*
1621C35	7C164-35C*
1621M35	7C164-35M*
1621M45	7C164-45M*
1622C25	7C166-25C+
1622C35	7C166-35C+
1622M35	7C166-35M+
1622M45	7C166-45M+
1623C25	7C166-25C*
1623C35	7C166-35C*
1623M35	7C166-35M*
1623M45	7C166-45M*
16L8A	PALC16L8-25C
16L8A	PALC16L8-20M
16P8A	PALC16L8-20M−
16P8A	PALC16L8-25C−
16R4A	PALC16R4-20M
16R4A	PALC16R4-25C
16R6A	PALC16R6-20M
16R6A	PALC16R6-25C
16R8A	PALC16R8-25C
16R8A	PALC16R8-20M
16RP4A	PALC16R4-20M−
16RP4A	PALC16R4-25C−
16RP6A	PALC16R6-25C−
16RP6A	PALC16R6-20M−
16RP8A	PALC16R8-25C−
16RP8A	PALC16R8-20M−
3341AC	3341C
3341C	3341C
54F189	7C189-25M−
54F219	7C190-25M−
54F413	7C401-15M
54S189M	54S189M
74AC1010-40	7C510-45C
74F189	7C189-25C−
74F219	7C190-25C−
74F413	7C401-15C
74LS189	27LS03C
74S189	74S189C
93422AC	93422AC
93422AM	93422AM
93422C	93422C
93422M	93422M
93475C	2149-45C
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
93Z451AC	7C282-30C
93Z451AM	7C282-45M
93Z451C	7C282-30C
93Z451M	7C282-45M
93Z511C	7C292-35C
93Z511M	7C292-50M
93Z565AC	7C264-45C
93Z565AM	7C264-55M
93Z565C	7C264-55C
93Z565M	7C264-55M
93Z611C	7C292-25C
93Z665C	7C264-35C
93Z665M	7C264-45M
93Z667C	7C263-35C
93Z667M	7C261-45M

FUJITSU	CYPRESS
PREFIX:MB	PREFIX:CY
PREFIX:MBM	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:M	SUFFIX:P
SUFFIX:Z	SUFFIX:D
2147H-35	2147-35C
2147H-45	2147-45C
2147H-55	2147-55C
2147H-70	2147-55C
2148-55L	21L48-55C
2148-70L	21L48-55C
2149-45	2149-45C
2149-55L	21L49-55C
2149-70L	21L49-55C
7132E	7C282-45C
7132E-SK	7C281-45C
7132E-W	7C282-45M
7132H	7C282-45C
7132H-SK	7C281-45C
7132Y	7C282-30C
7132Y-SK	7C281-30C
7138E	7C292-50C
7138E-SK	7C291-50C
7138E-W	7C292-50M
7138H	7C292-35C
7138H-SK	7C291-35C
7138Y	7C292-35C
7138Y-SK	7C291-35C
7144E	7C264-55C
7144E-W	7C264-55M
7144H	7C264-55C
7144Y	7C264-45C
7226RA-20	7C225-30C
7226RA-25	7C225-30C
7232RA-20	7C235-30C
7232RA-25	7C235-30C
7238RA-20	7C245-25C
7238RA-25	7C245-35C
8167A-55	7C167-45C
8167A-70	7C167-45C
8167-70W	7C167-45M
8168-55	7C168-45C
8168-70	7C168-45C
8168-70W	7C168-45M
8171-55	7C187-45C
8171-70	7C187-45C
81C67-35	7C167-45C+
81C67-45	7C167-45C
81C67-55	7C167-45C
81C67-55W	7C167-45M
81C68A-25	7C168L-25C
81C68A-30	7C168L-25C
81C68A-35	7C168L-35C
81C68-35	7C168L-35C
81C68-45	7C168-45C
81C68-55W	7C168-45M+
81C69A-25	7C169L-25C
81C69A-30	7C169L-25C
81C69A-35	7C169L-35C
81C71-45	7C187-45C+
81C71-55	7C187-45C+
81C74-25	7C164-25C+
81C74-25	7C187-25C+
81C74-35	7C164-35C+
81C74-35	7C187-35C+
81C74-45	7C164-45C+
81C75-35	7C166-35C
81C75-45	7C166-45C
81C78-45	7C186-45C+
81C78-55	7C186-55C+
8464L-100	7C185-55C+
8464L-70	7C185-45C+

HARRIS	CYPRESS
PREFIX:1	SUFFIX:D
PREFIX:3	SUFFIX:P
PREFIX:4	SUFFIX:L
PREFIX:9	SUFFIX:F
PREFIX:HM	PREFIX:CY
PREFIX:HPL	PREFIX:CY
16LC8-5	PALC16L8L-35C−
16LC8-8	PALC16L8-40M+
16LC8-9	PALC16L8-40M+
16RC4-5	PALC16R4L-35C−
16RC4-8	PALC16R4-40M+
16RC4-9	PALC16R4-40M+
16RC6-5	PALC16R6L-35C−
16RC6-8	PALC16R6-40M+
16RC6-9	PALC16R6-40M+
16RC8-5	PALC16R8L-35C−
16RC8-8	PALC16R8-40M+
16RC8-9	PALC16R8-40M+
65162B-5	6116-55C*
65162B-8	6116-55M*
65162B-9	6116-55M*
65162C-8	6116-55M*
65162C-9	6116-55M*
65162S-5	6116-55C*
65162S-9	6116-55M*
65162-5	6116-55C*
65162-8	6116-55M*
65162-9	6116-55M*
65262B-8	7C167-45M*
65262B-9	7C167-45M*
65262C-9	7C167-45M*
65262S-9	7C167-45M*
65262-8	7C167-45M*
65262-9	7C167-45M*
6-76161A-2	7C291-50M
6-76161A-5	7C291-50C
6-76161B-5	7C291-35C
6-76161-2	7C291-50M
6-76161-5	7C291-50C

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− = functionally equivalent

Product Line Cross Reference (Continued)

HARRIS	CYPRESS
6-7681A-5	7C281-45C
6-7681-5	7C281-45C
76161A-2	7C292-50M
76161A-5	7C292-50C
76161B-5	7C292-35C
76161-2	7C292-50M
76161-5	7C292-50C
76641A-5	7C264-45C
76641-2	7C264-55M
76641-5	7C264-55C
7681A-5	7C282-45C
7681-2	7C282-45M
7681-5	7C282-45C
SUFFIX:8	SUFFIX:B

HITACHI	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HN	PREFIX:CY
SUFFIX:CG	SUFFIX:L
SUFFIX:G	SUFFIX:D
SUFFIX:P	SUFFIX:P
25089	7C282-45C
25089S	7C282-45C
25169S	7C292-50C
4847	2147-55C
4847-2	2147-45C
4847-3	2147-55C
6116ALS-12	6116-55C*
6116ALS-15	6116-55C*
6116ALS-20	6116-55C*
6116AS-12	6116-55C+
6116AS-15	6116-55C+
6116AS-20	6116-55C+
6147	7C147-45C*
6147	7C147-45C*
6147HL-35	7C147-35C*
6147HL-45	7C147-45C*
6147HL-55	7C147-55C*
6147H-35	7C147-35C+
6147H-45	7C147-45C+
6147H-55	7C147-45C+
6147-3	7C147-45C*
6147-3	7C147-45C*
6148	7C148-45C
6148HL-35	21L48-35C*
6148HL-45	7C148-45C*
6148HL-55	7C148-45C*
6148H-35	21L48-35C
6148H-45	7C148-45C+
6148H-55	7C148-45C+
6148L	7C148-45C*
6167	7C167-45C+
6167HL-45	7C167-45C*
6167HL-55	7C167-45C*
6167H-45	7C167-45C+
6167H-55	7C167-45C+
6167L	7C167-45C*
6167L-6	7C167-45C*
6167L-8	7C167-45C*
6167-6	7C167-45C+
6167-8	7C167-45C+
6168HL-45	7C168-45C*
6168HL-55	7C168-45C*
6168HL-70	7C168-45C*
6168H-45	7C168-45C+
6168H-55	7C168-45C+
6168H-70	7C168-45C+
6264L-10	7C186-55C*
6264L-12	7C186-55C*
6264L-15	7C186-55C*
6264-10	7C186-55C+
6264-12	7C186-55C+
6264-15	7C186-55C+
6267-35	7C167-35C+
6267-45	7C167-45C
6287L-55	7C187-45C*
6287L-70	7C187-45C*
6287-45	7C187-45C+
6287-55	7C187-45C+
6287-70	7C187-45C+
6787-25	7C187-25C

IDT	CYPRESS
PREFIX:IDT	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
39C01C	7C901-31C+
39C01CB	7C901-32M+
39C01D	7C901-23C+
39C01DB	7C901-27M+
39C09A	7C909-40C+
39C09AB	7C909-40M+
39C10B	7C910-50C−
39C10BB	7C910-51M−
39C11A	7C911-40C+
39C11AB	7C911-40M+
49C401	7C9101-40C−
49C401B	7C9101-45M−
6116L120B	6116-55M*
6116L150B	6116-55M*
6116L55	6116-55C*
6116L55B	6116-55M*
6116L70	6116-55C*
6116L70B	6116-55M*
6116L90	6116-55C*
6116L90B	6116-55M*
6116LA120B	6116-55M*
6116LA120TB	7C128-55M*
6116LA35	6116-35C*
6116LA35B	6116-45M*
6116LA35T	7C128-35C*
6116LA35TB	7C128-35M*
6116LA45	6116-45C*
6116LA45B	6116-45M*
6116LA45T	7C128-45C*
6116LA45TB	7C128-45M*
6116LA55	6116-55C*
6116LA55B	6116-55M*
6116LA55T	7C128-55C*
6116LA55TB	7C128-55M*
6116LA70	6116-55C*
6116LA70B	6116-55M*
6116LA70T	7C128-55C*
6116LA70TB	7C128-55M*
6116LA90	6116-55C*
6116LA90B	6116-55M*
6116LA90T	7C128-55C*
6116LA90TB	7C128-55M*
6116S120B	6116-55M+
6116S150B	6116-55M+
6116S55	6116-55C+
6116S55B	6116-55M+
6116S70	6116-55C+
6116S70B	6116-55M+
6116S90	6116-55C+
6116S90B	6116-55M+
6116SA120B	6116-55M+
6116SA120TB	7C128-55M+
6116SA35	6116-35C+
6116SA35B	6116-45M+
6116SA35T	7C128-35C+
6116SA35TB	7C128-35M+
6116SA45	6116-45C+
6116SA45B	6116-45M+
6116SA45T	7C128-45C+
6116SA45TB	7C128-45M+
6116SA55	6116-55C+
6116SA55B	6116-55M+
6116SA55T	7C128-55C+
6116SA55TB	7C128-55M+
6116SA70	6116-55C+
6116SA70B	6116-55M+
6116SA70T	7C128-55C+
6116SA70TB	7C128-55M+
6116SA90	6116-55C+
6116SA90B	6116-55M+
6116SA90T	7C128-55C+
6116SA90TB	7C128-55M+
6167L100B	7C167-45M*
6167L45	7C167L-45C*
6167L55B	7C167-45M*
6167L70B	7C167-45M*
6167L85B	7C167-45M*
6167LA25	7C167-25C*
6167LA35	7C167-35C*
6167LA35B	7C167-35M*
6167LA45	7C167-45C*
6167LA45B	7C167-45M*
6167LA55	7C167-45C*
6167LA55B	7C167-45M*
6167LA70B	7C167-45M*
6167S100B	7C167-45M
6167S45	7C167-45C
6167S55	7C167-45C
6167S55B	7C167-45M
6167S70	7C167-45C+
6167S70B	7C167-45M
6167S85B	7C167-45M
6167SA25	7C167-25C+
6167SA35	7C167-35C+
6167SA35B	7C167-35M+
6167SA45	7C167-45C+
6167SA45B	7C167-45M+
6167SA55	7C167-45C+
6167SA55B	7C167-45M+
6167SA70B	7C167-45M+
6168L100B	7C168-45M*
6168L45	7C168-45C*
6168L55	7C168-45C*
6168L55B	7C168-45M*
6168L70	7C168-45C*
6168L70B	7C168-45M*
6168L85	7C168-45C*
6168L85B	7C168-45M*
6168LA25	7C168-25C*
6168LA35	7C168-35C*
6168LA35B	7C168-35M*
6168LA45	7C168-45C*
6168LA45B	7C168-45M*
6168LA55	7C168-45C*
6168LA55B	7C168-45M*
6168LA70B	7C168-45M*
6168S100B	7C168-45M+
6168S45	7C168-45C+
6168S55	7C168-45C+

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Product Line Cross Reference (Continued)

IDT	CYPRESS	IDT	CYPRESS	IDT	CYPRESS	IDT	CYPRESS
6168S55B	7C168-45M+	7164S55	7C186-55C+	71682S55B	7C172-45M+	71981L35	7C161-35C*
6168S70	7C168-45C	7164S55B	7C186-55M+	71682S70	7C172-45C+	71981L35B	7C161-35M*
6168S70B	7C168-45M	7164S70	7C186-55C+	71682S70B	7C172-45M+	71981L45	7C161-45C*
6168S85	7C168-45C	7164S70B	7C186-55M+	71682S85B	7C172-45M+	71981L45B	7C161-45M*
6168S85B	7C168-45M	7164S85B	7C186-55M+	71682SA25	7C172-25C+	71981L55	7C161-45C*
6168SA25	7C168-25C+	71681L100B	7C171-45M*	71682SA35	7C172-35C+	71981L55B	7C161-45M*
6168SA35	7C168-35C+	71681L45	7C171-45C*	71682SA35B	7C172-35M+	71981L70	7C161-45C*
6168SA35B	7C168-35M+	71681L55	7C171-45C*	71682SA45	7C172-45C+	71981L70B	7C161-45M*
6168SA45	7C168-45C+	71681L55B	7C171-45M*	71682SA45B	7C172-45M+	71981L85B	7C161-45M*
6168SA45B	7C168-45M+	71681L70	7C171-45C*	71682SA55	7C172-45C+	71981S35	7C161-35C
6168SA55	7C168-45C+	71681L70B	7C171-45M*	71682SA55B	7C172-45M+	71981S35B	7C161-35M
6168SA55B	7C168-45M+	71681L85B	7C171-45M*	7187L30	7C187-25C*	71981S45	7C161-45C
6168SA70B	7C168-45M+	71681LA25	7C171-25C*	7187L35	7C187-35C*	71981S45B	7C161-45M
7130L100	7C130-55C*	71681LA35	7C171-35C*	7187L35B	7C187-35M*	71981S55	7C161-45C
7130L100B	7C130-55M	71681LA35B	7C171-35M*	7187L45	7C187-45C*	71981S55B	7C161-45M
7130L120B	7C130-55M	71681LA45	7C171-45C*	7187L45B	7C187-45M*	71981S70	7C161-45C
7130L55	7C130-55C*	71681LA45B	7C171-45M*	7187L55	7C187-45C*	71981S70B	7C161-45M
7130L70	7C130-55C*	71681LA55	7C171-45C*	7187L55B	7C187-45M*	71981S85B	7C161-45M
7130L90	7C130-55C*	71681LA55B	7C171-45M*	7187L70	7C187-45C*	71982L35	7C162-35C*
7130S100	7C130-55C	71681LA70B	7C171-45M*	7187L85	7C187-45C*	71982L35B	7C162-35M*
7130S100B	7C130-55M	71681S100B	7C171-45M+	7187L85B	7C187-45M*	71982L45	7C162-45C*
7130S120B	7C130-55M	71681S45	7C171-45C+	7187S30	7C187-25C+	71982L45B	7C162-45M*
7130S55	7C130-55C	71681S55	7C171-45C+	7187S35	7C187-35C+	71982L55	7C162-45C*
7130S70	7C130-55C	71681S55B	7C171-45M+	7187S35B	7C187-35M	71982L55B	7C162-45M*
7130S90	7C130-55C	71681S70	7C171-45C+	7187S45	7C187-45C+	71982L70	7C162-45C*
7132L100	7C132-55C*	71681S70B	7C171-45M+	7187S45B	7C187-45M	71982L70B	7C162-45M*
7132L100B	7C132-55M*	71681S85B	7C171-45M+	7187S55	7C187-45C+	71982L85B	7C162-45M*
7132L120B	7C132-55M*	71681SA25	7C171-25C+	7187S55B	7C187-45M	71982S35	7C162-35C
7132L55	7C132-55C*	71681SA35	7C171-35C+	7187S70	7C187-45C+	71982S35B	7C162-35M
7132L70	7C132-55C*	71681SA35B	7C171-35M+	7187S70B	7C187-45M	71982S45	7C162-45C
7132L70B	7C132-55M*	71681SA45	7C171-45C+	7187S85	7C187-45C+	71982S45B	7C162-45M
7132L90	7C132-55C*	71681SA45B	7C171-45M+	7187S85B	7C187-45M	71982S55	7C162-45C
7132L90B	7C132-55M*	71681SA55	7C171-45C+	7188L30	7C164-25C*	71982S55B	7C162-45M
7132S100	7C132-55C+	71681SA55B	7C171-45M+	7188L35	7C164-35C*	71982S70	7C162-45C
7132S100B	7C132-55M+	71681SA70B	7C171-45M+	7188L35B	7C164-35M*	71982S70B	7C162-45M
7132S120B	7C132-55M+	71682L100B	7C172-45M*	7188L45	7C164-45C*	71982S85B	7C162-45M
7132S55	7C132-55C+	71682L45	7C172-45C*	7188L45B	7C164-45M*	7198L35	7C166-35C*
7132S70	7C132-55C+	71682L55	7C172-45C*	7188L55	7C164-45C*	7198L35B	7C166-35M*
7132S70B	7C132-55M+	71682L55B	7C172-45M*	7188L55B	7C164-45M*	7198L45	7C166-45C*
7132S90	7C132-55C+	71682L70	7C172-45C*	7188L70	7C164-45C*	7198L45B	7C166-45M*
7132S90B	7C132-55M+	71682L70B	7C172-45M*	7188L70B	7C164-45M*	7198L55	7C166-45C*
7164L35	7C186-35C*	71682L85B	7C172-45M*	7188L85B	7C164-45M*	7198L55B	7C166-45M*
7164L45	7C186-45C*	71682LA25	7C172-25C*	7188S30	7C164-25C	7198L70	7C166-45C*
7164L45B	7C186-45M*	71682LA35	7C172-35C*	7188S35	7C164-35C	7198L70B	7C166-45M*
7164L55	7C186-55C*	71682LA35B	7C172-35M*	7188S35B	7C164-35M*	7198L85B	7C166-45M*
7164L55B	7C186-55M*	71682LA45	7C172-45C*	7188S45	7C164-45C	7198S35	7C166-35C
7164L70	7C186-55C*	71682LA45B	7C172-45M*	7188S45B	7C164-45M	7198S35B	7C166-35M+
7164L70B	7C186-55M*	71682LA55	7C172-45C*	7188S55	7C164-45C	7198S45	7C166-45C
7164L85B	7C186-55M*	71682LA55B	7C172-45M*	7188S55B	7C164-45M	7198S45B	7C166-45M
7164S35	7C186-35C+	71682S100B	7C172-45M+	7188S70	7C164-45C	7198S55	7C166-45C
7164S45	7C186-45C+	71682S45	7C172-45C+	7188S70B	7C164-45M	7198S55B	7C166-45M
7164S45B	7C186-45M+	71682S55	7C172-45C+	7188S85B	7C164-45M	7198S70	7C166-45C

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− = functionally equivalent

CYPRESS
SEMICONDUCTOR

Product Line Cross Reference (Continued)

IDT	CYPRESS
7198S70B	7C166-45M
7198S85B	7C166-45M
7201LA-120	7C412-12C+
7201LA-120B	7C412-12M*
7201LA-40B	7C412-25M*
7201LA-50	7C412-25C+
7201LA-50B	7C412-20M*
7201LA-65	7C412-15C+
7201LA-65B	7C412-15M*
7201LA-80	7C412-15C+
7201LA-80B	7C412-15M*
7201L-120	7C412-12C+
7201L-120B	7C412-12M*
7201L-40B	7C412-25M*
7201L-50	7C412-25C+
7201L-50B	7C412-20M*
7201L-65	7C412-15C+
7201L-65B	7C412-15M*
7201L-80	7C412-15C+
7201L-80B	7C412-15M*
7201SA-120	7C412-12C
7201SA-120B	7C412-12M
7201SA-40B	7C412-25M
7201SA-50	7C412-25C
7201SA-50B	7C412-20M
7201SA-65	7C412-15C
7201SA-65B	7C412-15M
7201SA-80	7C412-15C
7201SA-80B	7C412-15M
7201S-120	7C412-12C
7201S-120B	7C412-12M
7201S-40B	7C412-25M
7201S-50	7C412-25C
7201S-50B	7C412-20M
7201S-65	7C412-15C
7201S-65B	7C412-15M
7201S-80	7C412-15C
7201S-80B	7C412-15M
7210L100	7C510-75C+
7210L165	7C510-75C+
7210L45	7C510-45C+
7210L55	7C510-55C+
7210L65	7C510-65C+
7210L75	7C510-75C+
7210L120B	7C510-75M+
7210L200B	7C510-75M+
7210L55B	7C510-55M
7210L65B	7C510-65M
7210L75B	7C510-75M
7210L85B	7C510-75M
7216L120B	7C516-75M+
7216L140	7C516-75C+
7216L185B	7C516-75M+
7216L55	7C516-55C+
7216L55B	7C516-55M
7216L65	7C516-65C+
7216L65B	7C516-65M
7216L75	7C516-75C+
7216L75B	7C516-75M
7216L90	7C516-75C+
7216L90B	7C516-75M+
7217L120B	7C517-75M+
7217L140	7C517-75C+
7217L185B	7C517-75M+
7217L45	7C517-45C+
7217L55	7C517-55C+
7217L55B	7C517-55M
7217L65	7C517-65C+
7217L65B	7C517-65M
7217L75	7C517-75C+
7217L75B	7C517-75M
7217L90	7C517-75C+
7217L90B	7C517-75M+

INMOS	CYPRESS
PREFIX:IMS	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:P	SUFFIX:P
SUFFIX:S	SUFFIX:D
SUFFIX:W	SUFFIX:L
1400L-10	7C167-45C
1400L-70	7C167-45C
1400-35	7C167-35C
1400-35M	7C167-35M
1400-45	7C167-45C
1400-45M	7C167-45M
1400-55	7C167-45C
1400-55M	7C167-45M
1400-70M	7C167-45M
1403-35	7C167-35C+
1403-45	7C167-45C
1403-45M	7C167-45M
1403-55	7C167-45C
1403-55M	7C167-45M
1420L-10	7C168-45C
1420L-70	7C168-45C
1420-45	7C168-35C
1420-55	7C168-45C
1420-55M	7C168-45M+
1421-40	7C169-40C
1421-50	7C169-40C
1421-50M	7C169-40M+
1423-25	7C168-25C
1423-35	7C168-35C
1423-45	7C168-45C
1423-45M	7C168-45M*
1423-55M	7C168-45M*
1424-35	7C170-35C−
1424-45	7C170-45C−
1600-45	7C187-45C+
1600-55	7C187-45C+
1600-55M	7C187-45M*
1600-70	7C187-45C+
1600-70M	7C187-45M*
1620-45	7C164-45C
1620-55	7C164-45C
1620-55M	7C164-45M
1620-70	7C164-45C
1620-70M	7C164-45M

INTEL	CYPRESS
PREFIX:D	SUFFIX:D
PREFIX:L	SUFFIX:L
PREFIX:P	SUFFIX:P
SUFFIX:/B	SUFFIX:B
2147H	2147-55C
2147HL	7C147-45C
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2148H	2148-55C
2148HL	21L48-55C
2148HL-3	21L48-55C
2148H-2	2148-45C
2148H-3	2148-55C
2149H	2149-55C
2149HL	21L49-55C
2149H-1	2149-35C
2149H-2	2149-55C
2149H-3	2149-55C
51C66-25	7C167-25C−
51C66-30	7C167-25C−
51C66-35	7C167-25C−
51C66-35L	7C167-25C−
51C67-30	7C167-25C+
51C67-35	7C167-35C+
51C67-35L	7C167-35C+
51C68L-35	7C168L-35C+
51C68-30	7C168-25C+
51C68-35	7C168-35C+
M2147H-3	7C169-40M
M2148H	2148-55M
M2149H	2149-55M
M2149H-2	2149-45M
M2149H-3	2149-55M

LATTICE	CYPRESS
PREFIX:EE	PREFIX:CY
PREFIX:GAL	PREFIX:CY
PREFIX:SR	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
16K4-25	7C168-25C
16K4-35	7C168-35C
16K4-35M	7C168-35M
16K4-45	7C168-45C
16K4-45M	7C168-45M
16K8-35	7C128-35C+
16K8-55	7C128-45C+
20V8-25	PLDC20G10-25C
20V8-25L	PLDC20G10-25C
20V8-25Q	PLDC20G10-25C+
20V8-35	PLDC20G10-35C
20V8-35	PLDC20G10-30M
20V8-35L	PLDC20G10-30M
20V8-35L	PLDC20G10-35C
20V8-35Q	PLDC20G10-30M+
20V8-35Q	PLDC20G10-35C+
64E4-35	7C166-35C+
64E4-45	7C166-45C+
64E4-55	7C166-45C+
64K1-35	7C187-35C+
64K1-45	7C187-45C+
64K1-45M	7C187-45M+
64K1-55	7C187-45C+
64K1-55M	7C187-45M+
64K4-35	7C164-35C+
64K4-45	7C164-45C+
64K4-45M	7C164-45M+
64K4-55	7C164-45C+
64K4-55M	7C164-45M+
64K8-35	7C186-35C+
64K8-45	7C186-45C+
64K8-45	7C264-45C
64K8-45M	7C186-45M+
64K8-55	7C264-55C
64K8-55	7C186-55C+
64K8-55M	7C186-45M+
64K8-70	7C264-55C
L1010-45	7C510-45C+
L1010-65	7C510-65C+
L1010-65B	7C510-65M+
L1010-90	7C510-75C+
L1010-90B	7C510-75M+

MITSUBISHI	CYPRESS
PREFIX:M5M	PREFIX:CY

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
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− = functionally equivalent

Product Line Cross Reference (Continued)

MITSUBISHI	CYPRESS
SUFFIX:AP	SUFFIX:L
SUFFIX:FP	SUFFIX:F
SUFFIX:K	SUFFIX:D
SUFFIX:P	SUFFIX:P
21C67P-35	7C167-35C
21C67P-45	7C167-45C
21C67P-55	7C167-45C
21C68P-35	7C168-35C
21C68P-45	7C168-45C
21C68P-55	7C168-45C
5165L-100	7C186-55C+
5165L-120	7C186-55C+
5165L-70	7C186-55C+
5165P-100	7C186-55C+
5165P-120	7C186-55C+
5165P-70	7C186-55C+
5178P-45	7C186-45C
5178P-55	7C186-55C+
5187P-25	7C187-25C+
5187P-35	7C187-35C+
5187P-45	7C187-45C+
5187P-55	7C187-45C+
5188P-25	7C164-25C
5188P-35	7C164-35C+
5188P-45	7C164-45C+
5188P-55	7C164-45C+

MMI	CYPRESS
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:SHRP	SUFFIX:B
5381S-1	7C281-45M
5381S-2	7C281-45M
5381-1	7C282-45M
5381-2	7C282-45M
53RA1681AS	7C245-35M−
53RA1681S	7C245-45M−
53RA481AS	7C225-35M
53RA481S	7C225-40M
53RS1681AS	7C245-35M−
53RS1681S	7C245-45M−
53RS881AS	7C235-40M−
53RS881S	7C235-40M−
53S1681	7C292-50M
53S1681AS	7C291-35M
53S1681S	7C291-50M
53S881	7C282-45M
53S881A	7C282-45M
53S881AS	7C281-45M

MMI	CYPRESS
53S881S	7C281-45M
57401	7C401-10M
57401A	7C401-10M
57402	7C402-10M
57402A	7C402-10M
6381S-1	7C281-45C
6381S-2	7C281-45C
6381-1	7C282-45C
6381-2	7C282-45C
63RA1681AS	7C245-35C−
63RA1681S	7C245-35C−
63RA481AS	7C225-25C
63RA481S	7C225-30C
63RS1681AS	7C245-35C−
63RS1681S	7C245-35C−
63RS881AS	7C235-30C−
63RS881S	7C235-30C−
63S1681	7C292-50C
63S1681A	7C292-35C
63S1681AS	7C291-35C
63S1681S	7C291-50C
63S881	7C281-45C
63S881	7C282-45C
63S881A	7C282-30C
63S881A	7C281-30C
67401	7C401-10C
67401	7C401-10C
67401A	7C401-15C
67401B	7C403-25C
67401D	7C403-25C
67402	7C402-10C
67402A	7C402-15C
67402B	7C402-25C
67402D	7C404-25C
67411	7C403-25C
67412	7C402-25C
67L402	7C402-10C
C57401	7C401-10M
C57401A	7C401-10M
C57402	7C402-10M
C57402A	7C402-10M
C67401A	7C401-15C
C67401B	7C403-25C
C67402	7C402-10C
C67402A	7C402-15C
C67402B	7C404-25C
C67L401	7C401-5C
C67L401D	7C401-15C
C67L402D	7C402-15C
PAL12L10C	PLDC20G10-35C
PAL12L10M	PLDC20G10-40M
PAL14L8C	PLDC20G10-35C

MMI	CYPRESS
PAL14L8M	PLDC20G10-40M
PAL16L6C	PLDC20G10-35C
PAL16L6M	PLDC20G10-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M+
PAL16L8BM	PALC16L8-20M
PAL16L8B-2C	PALC16L8-25C
PAL16L8B-2M	PALC16L8-30M
PAL16L8B-4C	PALC16L8L-35C
PAL16L8B-4M	PALC16L8-40M+
PAL16L8C	PALC16L8-35C
PAL16L8D-4C	PALC16L8L-25C
PAL16L8D-4M	PALC16L8-30M+
PAL16L8M	PALC16L8-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4A-2C	PALC16R4-35C
PAL16R4A-2M	PALC16R4-40M
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M+
PAL16R4BM	PALC16R4-20M
PAL16R4B-2C	PALC16R4-25C
PAL16R4B-2M	PALC16R4-30M
PAL16R4B-4C	PALC16R4L-35C
PAL16R4B-4M	PALC16R4-40M+
PAL16R4C	PALC16R4-35C
PAL16R4D-4C	PALC16R4L-25C
PAL16R4M	PALC16R4-40M+
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6A-2C	PALC16R6-35C
PAL16R6A-2M	PALC16R6-40M
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6B-2C	PALC16R6-25C
PAL16R6B-2M	PALC16R6-30M
PAL16R6B-4C	PALC16R6L-35C
PAL16R6B-4M	PALC16R6-40M+
PAL16R6C	PALC16R6-35C
PAL16R6D-4C	PALC16R6L-25C
PAL16R6M	PALC16R6-40M+
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8A-2C	PALC16R8-35C
PAL16R8A-2M	PALC16R8-40M
PAL16R8A-4C	PALC16R8L-35C
PAL16R8A-4M	PALC16R8-40M

MMI	CYPRESS
PAL16R8BM	PALC16R8-20M
PAL16R8B-2C	PALC16R8-25C
PAL16R8B-2M	PALC16R8-30M
PAL16R8B-4C	PALC16R8L-35C
PAL16R8B-4M	PALC16R8-40M+
PAL16R8C	PALC16R8-35C
PAL16R8D-4C	PALC16R8L-25C
PAL16R8M	PALC16R8-40M+
PAL18L4C	PLDC20G10-35C
PAL18L4M	PLDC20G10-40M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20L2C	PLDC20G10-35C
PAL20L2M	PLDC20G10-40M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8A-2C	PLDC20G10-35C
PAL20L8A-2M	PLDC20G10-40M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4A-2C	PLDC20G10-35C
PAL20R4A-2M	PLDC20G10-40M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6A-2C	PLDC20G10-35C
PAL20R6A-2M	PLDC20G10-40M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8A-2C	PLDC20G10-35C
PAL20R8A-2M	PLDC20G10-40M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M
PLE10P8C	7C281-30C
PLE10P8C	7C282-30C
PLE10P8M	7C281-45M
PLE10P8M	7C282-45M
PLE10R8C	7C235-30C−
PLE10R8M	7C235-40M−
PLE11P8C	7C291-35C
PLE11P8M	7C291-35M
PLE11RA8C	7C245-35C−
PLE11RA8M	7C245-35M−
PLE11RS8C	7C245-35C−
PLE11RS8M	7C245-35M−

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Product Line Cross Reference (Continued)

MMI	CYPRESS
PLE9R8C	7C225-30C
PLE9R8M	7C225-35M

MOTOROLA	CYPRESS
PREFIX:MCM	PREFIX:CY
SUFFIX:P	SUFFIX:P
SUFFIX:S	SUFFIX:D
SUFFIX:Z	SUFFIX:L
1423-45	7C168-45C+
2016H-45	6116-45
2016H-55	6116-55C
2016H-70	6116-55C
2018-35	7C128-35C
2018-45	7C128-45C
2167H-35	7C167-35C
2167H-45	7C167-45C
2167H-55	7C167-45C
6147-55	7C147-45C*
6147-70	7C147-45C*
6164-45	7C186-45C+
6164-55	7C186-55C+
6164-70	7C186-55C+
6168-35	7C168-35C+
6168-45	7C168-45C+
6168-55	7C168-45C+
6168-70	7C168-45C+
61L47-55	7C147-45C*
61L47-70	7C147-45C*
61L64-45	7C186-45C+
61L64-55	7C186-55C+
61L64-70	7C186-55C+
6268-25	7C168-25C
6268-35	7C168-35C
6269-25	7C169-25C
6269-35	7C169-35C
6270-25	7C170-25C
6270-35	7C170-35C
6270-45	7C170-45C
6287-25	7C187-25C+
6287-35	7C187-35C+
6287-45	7C187-45C+
6288-25C	7C164-25C+
6288-35C	7C164-35C+
6288-35M	7C164-35M
6288-45C	7C164-45C+
6288-45M	7C164-45M
6290-25C	7C166-25C+
6290-35C	7C166-35C+
6290-35M	7C166-35M
6290-45C	7C166-45C+
6290-45M	7C166-45M
62L87-25	7C187-25C+

MOTOROLA	CYPRESS
62L87-35	7C187-35C+
76161	7C292-50C
76161A	7C292-50C
7681	7C282-45C
7681A	7C282-45C
93422	93422M
93422	93422C
93422A	93422AM
93422A	93422AC
93L422	93L422C
93L422	93L422M
93L422A	93L422AC
93L422A	93L422AM

NATIONAL	CYPRESS
PREFIX:DM	PREFIX:CY
PREFIX:IDM	PREFIX:CY
PREFIX:NMC	PREFIX:CY
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
12L10C	PLDC20G10-35C
14L8C	PLDC20G10-35C
14L8M	PLDC20G10-40M
16L6C	PLDC20G10-35C
16L6M	PLDC20G10-40M
18L4C	PLDC20G10-35C
18L4M	PLDC20G10-40M
20L2M	PLDC20G10-40M
2147H	2147-55C
2147H	2147-55M
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147H-3	2147-55M
2147H-3L	7C147-45C
2148H	2148-55C
2148HL	21L48-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148H-3L	21L48-55C
2901AC	7C901-31C
2901AM	7C901-32M
2901A-1C	7C901-31C
2901A-1M	7C901-32M
2901A-2C	7C901-31C
2901A-2M	7C901-32M
2909AC	2909AC
2909AM	2909M
2911AC	2911AC
2911AM	2911M
54S189	54S189M
54S189A	7C189-25M

NATIONAL	CYPRESS
74S189	74S189C
74S189A	27S03AC
75S07	7C190-25M
75S07A	27S07AM
77LS181	7C282-45M
77S181	7C282-45M
77S181A	7C282-45M
77S191	7C292-50M
77S191A	7C292-50M
77S191B	7C292-50M
77S281	7C281-45M
77S281A	7C281-45M
77S291	7C291-50M
77S291A	7C291-50M
77S291B	7C291-50M
77S401	7C401-10M
77S401A	7C401-10M
77S402	7C402-10M
77S402A	7C402-10M
77SR181	7C235-40M
77SR25	7C225-40M
77SR25B	7C225-40M
77SR476	7C225-40M−
77SR476B	7C225-40M−
85S07	27S07C
85S07A	7C128-45C+
85S07A	27S07AC
87LS181	7C282-45C
87S181	7C282-45C
87S191	7C292-50C
87S191A	7C292-35C
87S191B	7C292-35C
87S281	7C281-45C
87S281A	7C281-45C
87S291	7C291-50C
87S291A	7C291-35C
87S291B	7C291-35C
87S401	7C401-10C
87S401A	7C401-15C
87S402	7C402-10C
87S402A	7C402-15C
87SR181	7C235-30C
87SR25	7C225-40C
87SR25B	7C225-30C
87SR476	7C225-40C−
87SR476B	7C225-30C−
PAL16L8A2C	PALC16L8-35C
PAL16L8A2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8B2C	PALC16L8-25C
PAL16L8B2M	PALC16L8-30M

NATIONAL	CYPRESS
PAL16L8B4C	PALC16L8L-35C
PAL16L8B4M	PALC16L8-40M+
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8M	PALC16L8-40M
PAL16R4A2C	PALC16R4-35C
PAL16R4A2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B2C	PALC16R4-25C
PAL16R4B2M	PALC16R4-30M
PAL16R4B4C	PALC16R4L-35C
PAL16R4B4M	PALC16R4-40M+
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4M	PALC16R4-40M+
PAL16R6A2C	PALC16R6-35C
PAL16R6A2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B2C	PALC16R6-25C
PAL16R6B2M	PALC16R6-30M
PAL16R6B4C	PALC16R6L-35C
PAL16R6B4M	PALC16R6-40M+
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6M	PALC16R6-40M+
PAL16R8A2C	PALC16R8-35C
PAL16R8A2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B2C	PALC16R8-25C
PAL16R8B2M	PALC16R8-30M
PAL16R8B4C	PALC16R8L-35C
PAL16R8B4M	PALC16R8-40M+
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8M	PALC16R8-40M+
PAL20L10B2C	PLDC20G10-25C
PAL20L10B2M	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20L2C	PLDC20G10-35C
PAL20L2M	PLDC20G10-40M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8BC	PLDC20G10-25C
PAL20L8BM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M

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Product Line Cross Reference (Continued)

NATIONAL	CYPRESS
PAL20R4BC	PLDC20G10-25C
PAL20R4BM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6BC	PLDC20G10-25C
PAL20R6BM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8BC	PLDC20G10-25C
PAL20R8BM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M

NEC	CYPRESS
PREFIX:uPD	PREFIX:CY
SUFFIX:C	SUFFIX:P
SUFFIX:D	SUFFIX:D
SUFFIX:K	SUFFIX:L
SUFFIX:L	SUFFIX:F
2147A-25	7C147-25C
2147A-35	2147-35C
2147A-45	2147-45C
2147-2	2147-55C
2147-3	2147-55C
2149	2149-55C
2149-1	2149-45C
2149-2	2149-35C
2167-2	7C167-45C
2167-3	7C167-45C
429	7C292-50C
429-1	7C292-50C
429-2	7C292-50C
429-3	7C292-35C
4311-35	7C167L-35C
4311-45	7C167-45C
4311-55	7C167-45C
4314-35	7C168L-35C +
4314-45	7C168L-45C +
4314-55	7C168L-45C +
4361-40	7C187-35C +
4361-45	7C187-45C +
4361-55	7C187-45C +
4361-70	7C187-45C +
4362-45	7C164-45C +
4362-55	7C164-45C +
4362-70	7C164-45C +
4363-45	7C166-45C
4363-55	7C166-45C
4363-70	7C166-45C

RAYTHEON	CYPRESS
PREFIX:R296	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:S	SUFFIX:S
29631AC	7C282-45C
29631AM	7C282-45M
29631ASC	7C281-45C
29631ASM	7C281-45M
29631C	7C282-45C
29631M	7C282-45M
29631SC	7C281-45C
29631SM	7C281-45M
29633AC	7C282-45C +
29633AM	7C282-45M +
29633ASC	7C281-45C +
29633ASM	7C281-45M +
29633C	7C282-45C +
29633M	7C282-45M +
29633SC	7C281-45C +
29633SM	7C281-45M +
29681AC	7C292-50C
29681AM	7C292-50M
29681ASC	7C291-50C
29681ASM	7C291-50M
29681C	7C292-50C
29681M	7C292-50M
29681SC	7C291-50C
29681SM	7C291-50M
29683AC	7C292-50C +
29683AM	7C292-50M +
29683ASC	7C291-50C +
29683ASM	7C291-50M +
29683C	7C292-50C +
29683M	7C292-50M +
29683SC	7C291-50C +
29683SM	7C291-50M +
29VP864DB	7C264-55M
29VP864SB	7C263-55M
29VS864SB	7C261-55M
39VP864D	7C264-55C
39VP864S	7C263-55C
39VS864S	7C261-55C

SIGNETICS	CYPRESS
PREFIX:N	PREFIX:CY
PREFIX:S	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:D
SUFFIX:G	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:R	SUFFIX:F
N74S189	74S189C
N82HS641	7C264-55C
N82HS641A	7C264-45C
N82HS641B	7C264-35C
N82LS181	7C282-45C
N82S181	7C282-45C
N82S181A	7C282-45C
N82S181B	7C282-45C
N82S191A—3	7C291-50C
N82S191A—6	7C292-50C
N82S191B—3	7C291-35C
N82S191B—6	7C292-35C
N82S191—3	7C291-50C
N82S191—6	7C292-50C
S54S189	54S189M
S82HS641	7C264-55M
S82LS181	7C282-45M
S82S181	7C282-45M
S82S181A	7C282-45M
S82S191A—3	7C291-50M
S82S191A—6	7C292-50M
S82S191B—3	7C291-50M
S82S191B—6	7C292-50M
S82S191—3	7C291-50M
S82S191—6	7C292-50M

TI	CYPRESS
PREFIX:JBP	PREFIX:CY
PREFIX:PAL	SUFFIX:P
PREFIX:SN	PREFIX:CY
PREFIX:TBP	PREFIX:CY
PREFIX:TIB	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:L
SUFFIX:N	SUFFIX:D
22V10AC	PALC22V10-25C
22V10AM	PALC22V10-30M
27C291-3	7C291L-35C +
27C291-30	7C291L-35C +
27C291-5	7C291L-50C +
27C291-50	7C291L-50C +
28L166W	7C292-50C
28L86AMW	7C282-45M
28L86AW	7C282-45C
28S166W	7C292-50C
28S86AMW	7C282-45M
28S86AW	7C282-45C
38L165-35C	7C291-35C
38L165-45C	7C291-35C
38L85-45C	7C281-45C
38R165-18C	7C245-25C
38R165-25C	7C245-35C
38S165-25C	7C291-25C
38S165-35C	7C291-35C
54LS189A	27LS03M
54LS219A	7C190-25M +
54S189A	54S189M
74LS189A	27LS03C
74LS219A	27S07C +
74S189A	74S189C
HCT9510E	7C510-75C +
HCT9510E-10	7C510-75C +
HCT9510M	7C510-75M +
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8-20M	PALC16L8-20M
PAL16L8-25C	PALC16L8B-2C
PAL16L8-30M	PALC16L8-30M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4A-2C	PALC16R4-25C
PAL16R4A-2M	PALC16R4-40M
PAL16R4-20M	PALC16R4-20M
PAL16R4-25C	PALC16R4-25C
PAL16R4-30M	PALC16R4-30M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6A-2C	PALC16R6-25C
PAL16R6A-2M	PALC16R6-40M
PAL16R6-20M	PALC16R6-20M
PAL16R6-25C	PALC16R6-25C
PAL16R6-30M	PALC16R6-30M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8A-2C	PALC16R8-25C
PAL16R8A-2M	PALC16R8-40M
PAL16R8-20M	PALC16R8-20M
PAL16R8-25C	PALC16R8-25C
PAL16R8-30M	PALC16R8-30M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L10A-2C	PLDC20G10-25C
PAL20L10A-2M	PLDC20G10-30M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8A-2C	PLDC20G10-25C
PAL20L8A-2M	PLDC20G10-30M
PAL20R4AC	PLDC20G10-25C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
— = functionally equivalent

TI	CYPRESS
PAL20R4AM	PLDC20G10-30M
PAL20R4A-2C	PLDC20G10-25C
PAL20R4A-2M	PLDC20G10-30M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6A-2C	PLDC20G10-25C
PAL20R6A-2M	PLDC20G10-30M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8A-2C	PLDC20G10-25C
PAL20R8A-2M	PLDC20G10-30M

TOSHIBA	CYPRESS
PREFIX:P	SUFFIX:P
PREFIX:TMM	PREFIX:CY
SUFFIX:D	SUFFIX:D
2015A-10	7C128-55C+
2015A-12	7C128-55C+
2015A-15	7C128-55C+
2015A-90	7C128-55C+
2018-35	7C128-35C
2018-45	7C128-45C
2018-55	7C128-55C
2068-35	7C168-35C
2068-45	7C168-45C
2068-55	7C168-45C
2069-35	7C169-35C
2078-35	7C170-35C
2078-45	7C170-45C
2078-55	7C170-45C
315	2147-55C
315-1	2147-55C
5561-55	7C187-45C+
5561-70	7C187-45C+
5562-45	7C187-45C+
5562-55	7C187-45C+

TRW	CYPRESS
MPY016HA	7C516-75M
MPY016HC	7C516-75C
MPY016KA	7C516-75M
MPY016KC	7C516-75C
TDC1010A	7C510-75M
TDC1010C	7C510-75C
TMC2010A	7C510-75M+
TMC2010C	7C510-75C+
TMC2110A	7C510-75M
TMC2110C	7C510-75C
TMC216HA	7C516-75M
TMC216HC	7C516-75C+

VTI	CYPRESS
20C18-35	7C128-35C
20C19-35	7C128-35C
20C68-25	7C168-25C
20C68-35	7C168-35C
20C69-25	7C169-25C
20C69-35	7C169-35C
20C78-25	7C170-25C
20C78-35	7C170-35C
20C79-25	7C170-25C
20C79-35	7C170-35C
VL2010-65	7C510-65C
VL2010-70	7C510-65C
VL2010-90	7C510-75C
VT64KS4-35	7C164-35C+
VT64KS4-45	7C164-45C+
VT64KS4-55	7C164-45C+
VT65KS4-35	7C166-35C+
VT65KS4-45	7C166-45C+
VT65KS4-55	7C166-45C+

WEITEK	CYPRESS
1010AC	7C510-75C
1010AM	7C510-75M
1010BC	7C510-75C
1010BM	7C510-75M
1010C	7C510-75C
1010M	7C510-75M
1516AC	7C516-75C
1516AM	7C516-75M
1516BC	7C516-55C
1516BM	7C516-75M
1516C	7C516-75C
1516M	7C516-75M
2010AC	7C510-55C
2010AM	7C510-75M
2010BC	7C510-45C
2010BM	7C510-55M
2010C	7C510-75C
2010DC	7C510-55C
2010DM	7C510-75M
2010M	7C510-75M+
2516AC	7C516-55C
2516AM	7C516-75M
2516C	7C516-75C
2516DC	7C516-45C
2516DM	7C516-55M
2516M	7C516-75M+
2517AC	7C517-55C
2517AM	7C517-75M
2517C	7C517-75C
2517M	7C517-75M+

WSI	CYPRESS
PREFIX:WS	PREFIX:CY
SUFFIX:C	PREFIX:CY
SUFFIX:D	PREFIX:CY
SUFFIX:M	SUFFIX:P
SUFFIX:P	PREFIX:CY
29C01C	7C901-31C
57C128F-70	7C251-55C
57C128F-70M	7C251-55M+
57C128F-90	7C251-55C
57C128F-90M	7C251-55M+
57C191-40	7C292-35C
57C191-55	7C292-50C
57C191-55M	7C292-50M
57C191-70	7C292-50C
57C191-70M	7C292-50M
57C291-40	7C291-35C
57C291-55	7C291-50C
57C291-55M	7C291-50M
57C291-70	7C291-50C
57C291-70M	7C291-50M
57C49-55	7C264-55C+
57C49-55M	7C264-55M
57C49-70	7C264-55C+
57C49-70M	7C264-55M
57C49-90	7C264-55C+
57C49-90M	7C264-55M
59016C	7C9101-40C
59016C	7C9101-45M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
− = functionally equivalent

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Static RAMs (Random Access Memory)

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CY7C185	8192 x 8 Static RAM	2-108
CY7C186	8192 x 8 Static RAM	2-108
CY7C187	65,536 x 1 Static RAM	2-116
CY7C189	16 x 4 Static RAM	2-124
CY7C190	16 x 4 Static RAM	2-124
CY7C191	65,536 x 4 Static RAM Separate I/O	2-130
CY7C192	65,536 x 4 Static RAM Separate I/O	2-130
CY7C194	65,536 x 4 Static RAM	2-135
CY7C196	65,536 x 4 Static RAM	2-135
CY7C197	262,144 x 1 Static RAM	2-140
CY7C198	32,768 x 8 Static RAM	2-145
CY7C199	32,768 x 8 Static RAM	2-145
CY74S189	16 x 4 Static RAM	2-150
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CY93422A	256 x 4 Static RAM Separate I/O	2-155
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CYPRESS SEMICONDUCTOR

CY2147

4096 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **35 ns**
- **Low active power**
  - **690 mW (commercial)**
  - **770 mW (military)**
- **Low standby power**
  - **140 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

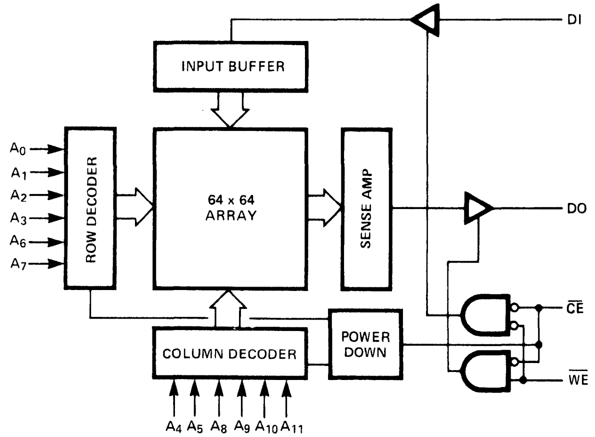
The CY2147 is a high performance CMOS static RAM organized as 4096 x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY2147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

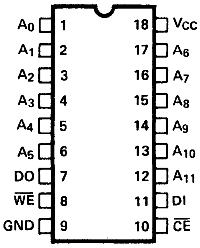
The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram


DI
INPUT BUFFER
A0
A1
A2
A3
A6
A7
ROW DECODER
64 x 64
ARRAY
SENSE AMP
DO
CE
WE
POWER
DOWN
COLUMN DECODER
A4 A5 A8 A9 A10 A11

0013-1

Pin Configuration


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DO 7
WE 8
GND 9
18 Vcc
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DI
10 CE

0013-2

Selection Guide (For higher performance and lower power refer to CY7C147 data sheet.)

		2147-35	2147-45	2147-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	125	125	125
	Military		140	140
Maximum Standby Current (mA)	Commercial	25	25	25
	Military		25	25

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		125	mA
			Military		140	
I_{SB}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		25	mA
			Military		25	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	

Notes:

1. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

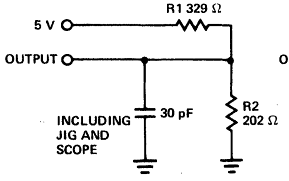


Figure 1a

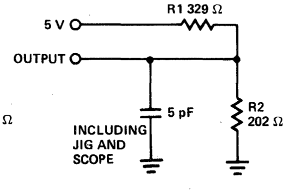


Figure 1b

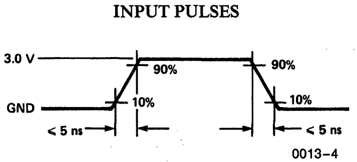
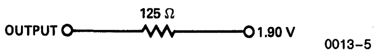


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

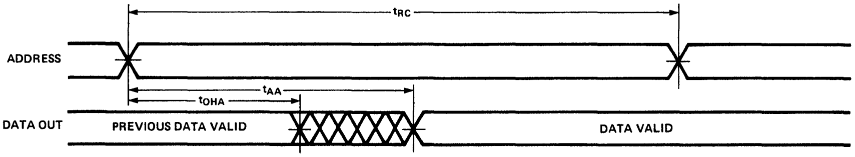
Parameters	Description	2147-35		2147-45		2147-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		30		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		45		45		ns
t_{AW}	Address Set-up to Write End	35		45		45		ns
t_{HA}	Address Hold from Write End	0		0		10		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-up to Write End	20		25		25		ns
t_{HD}	Data Hold from Write End	10		10		10		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	20	0	25	0	25	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

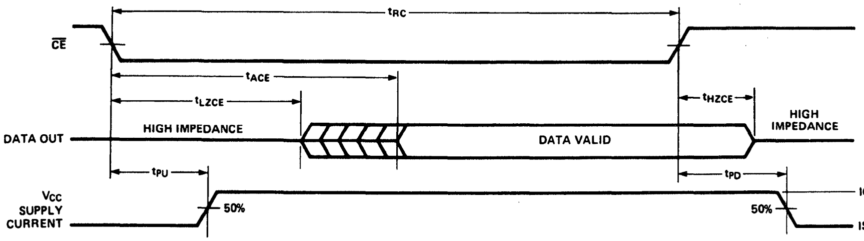
Switching Waveforms

Read Cycle No. 1 (Notes 8, 9)



0013-6

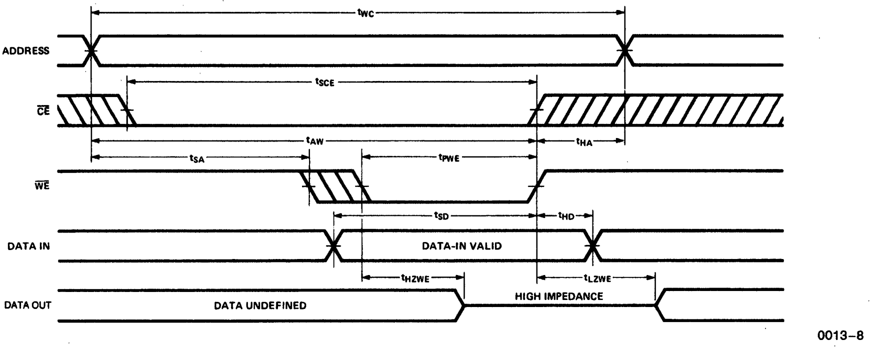
Read Cycle No. 2 (Notes 8, 10)



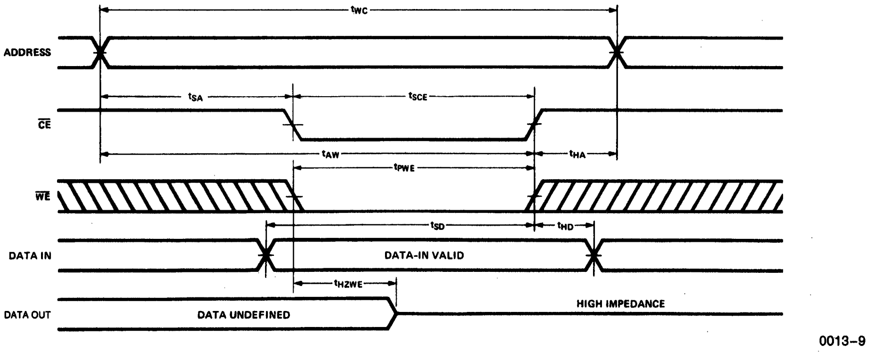
0013-7

Switching Waveforms (Continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)


ADDRESS
CE
WE
DATA IN
DATA OUT
tWC
tSCE
tAW
tHA
tSA
tPWE
tSD
tHD
DATA-IN VALID
tHZWE
tLZWE
HIGH IMPEDANCE
DATA UNDEFINED
0013-8

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 7)


ADDRESS
CE
WE
DATA IN
DATA OUT
tWC
tSA
tSCE
tAW
tHA
tPWE
tSD
tHD
DATA-IN VALID
tHZWE
HIGH IMPEDANCE
DATA UNDEFINED
0013-9

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2147-35 PC	P3	Commercial
	CY2147-35 DC	D4	
45	CY2147-45 PC	P3	Commercial
	CY2147-45 DC	D4	
	CY2147-45 DMB	D4	Military
55	CY2147-55 PC	P3	Commercial
	CY2147-55 DC	D4	
	CY2147-55 DMB	D4	Military

CYPRESS
SEMICONDUCTOR

CY2148/CY21L48
CY2149/CY21L49

1024 x 4 Static R/W RAM

Features

- **Automated power-down when deselected (2148)**
- **CMOS for optimum speed/ power**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **5 volt power supply ±10% tolerance both commercial and military**
- **TTL compatible inputs and outputs**

Functional Description

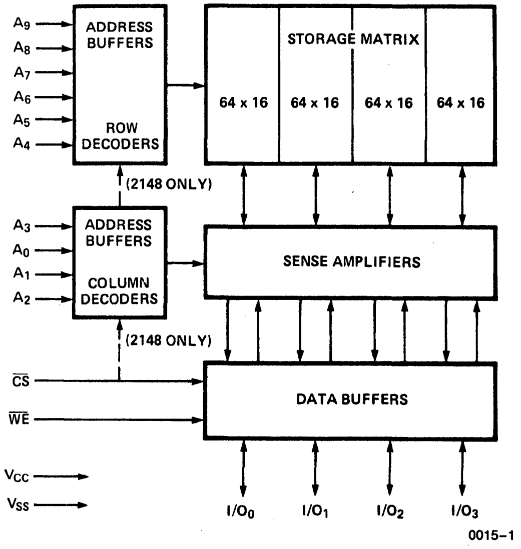
The CY2148 and CY2149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input, and three-state outputs. The CY2148 and CY2149 are identical except that the CY2148 includes an automatic ($\overline{CS}$) power-down feature. The CY2148 remains in a low power mode as long as the device remains unselected, i.e. ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY2149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

Reading the device is accomplished by selecting the device, ($\overline{CS}$) active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O_0 through I/O_3).

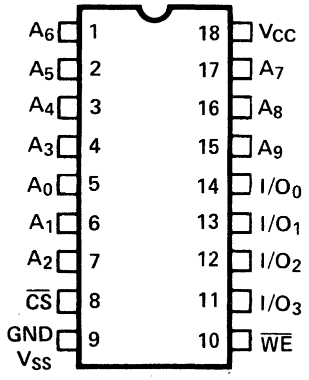
The input/output pins (I/O_0 through I/O_3) remain in a high impedance state unless the chip is selected, and write enable ($\overline{WE}$) is high.

Logic Block Diagram


A9
A8
A7
A6
A5
A4
ADDRESS BUFFERS
ROW DECODERS
STORAGE MATRIX
64 x 16
64 x 16
64 x 16
64 x 16
(2148 ONLY)
A3
A0
A1
A2
ADDRESS BUFFERS
COLUMN DECODERS
SENSE AMPLIFIERS
(2148 ONLY)
CS
WE
DATA BUFFERS
VCC
VSS
I/O0
I/O1
I/O2
I/O3

0015-1

Pin Configuration


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND VSS 9
18 VCC
17 A7
16 A8
15 A9
14 I/O0
13 I/O1
12 I/O2
11 I/O3
10 WE

0015-2

Selection Guide (For Higher Performance and Lower Power Refer to CY7C148/9 Data Sheet)

		2148/9-35	21L48/9-35	2148/9-45	21L48/9-45	2148/9-55	21L48/9-55
Maximum Access Time (ns)		35	35	45	45	55	55
Maximum Operating Current (mA)	Commercial	140	120	140	120	140	120
	Military			140		140	

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		21L48/9		2148/9		Units
				Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4V	T_A = 70°C	8		8		mA
			T_A = 125°C			8		
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ $V_O \le V_{CC}$ Output Disabled	T_A = −55°C to +125°C	−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0V, V_{CC} = 5V			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \le V_{IL}$ Output Open	T_A = 0°C to +70°C		120		140	mA
			T_A = −55°C to +125°C				140	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, $\overline{CS} \ge V_{IH}$ 2148 only	T_A = 0°C to +70°C		20		30	mA
			T_A = −55°C to +125°C				30	
I_{PO}	Peak Power-On Current	Max. V_{CC}, $\overline{CS} \ge V_{IH}$[3] 2148 only	T_A = 0°C to +70°C		30		50	mA
			T_A = −55°C to +125°C				50	
I_{OS}	Output Short Circuit Current	GND ≤ $V_O \le V_{CC}$[10]	T_A = 0°C to +70°C		±275		±275	mA
			T_A = −55°C to +125°C				±350	

Notes:

1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise current will exceed values given (CY2148 only).
4. Chip deselected greater than 55 ns prior to selection.
5. Chip deselected less than 55 ns prior to selection.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in *Figure 1b*. These parameters are sampled and not 100% tested.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms

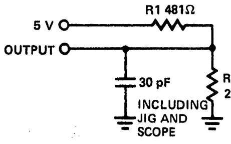
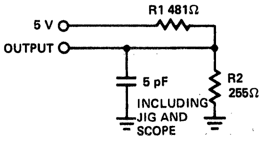
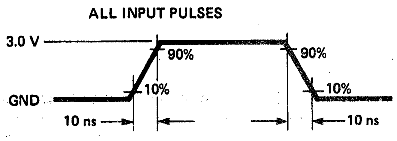


Figure 1a



0015-3

Figure 1b

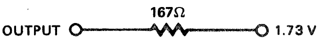


0015-5

Figure 2

Equivalent to:

THÉVINEN EQUIVALENT



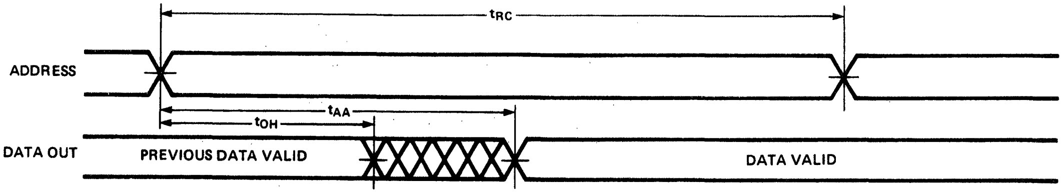
0015-4

Switching Characteristics

Parameters	Description		2148/9-35		2148/9-45		2148/9-55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55	ns
t_{ACS1}[4]	Chip Select LOW to Data Out Valid (CY2148 only)			35		45		55	ns
t_{ACS2}[5]				45		55		65	
t_{ACS}	Chip Select LOW to Data Out Valid (CY2149 only)			15		20		25	ns
t_{LZ}[6]	Chip Select LOW to Data Out On	2148	10		10		10		ns
		2149	5		5		5		
t_{HZ}[6]	Chip Select HIGH to Data Out Off		0	20	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		5		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	2148		30		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	2148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		ns
t_{WP}[2]	Write Enable LOW to Write Enable HIGH		30		35		40		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[6]	Write Enable LOW to Output in High Z		0	10	0	15	0	20	ns
t_{DW}	Data in Valid to Write Enable HIGH		20		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[2]	Chip Select LOW to Write Enable HIGH		30		40		50		ns
t_{OW}[6]	Write Enable High to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		30		35		50		ns

Switching Waveforms

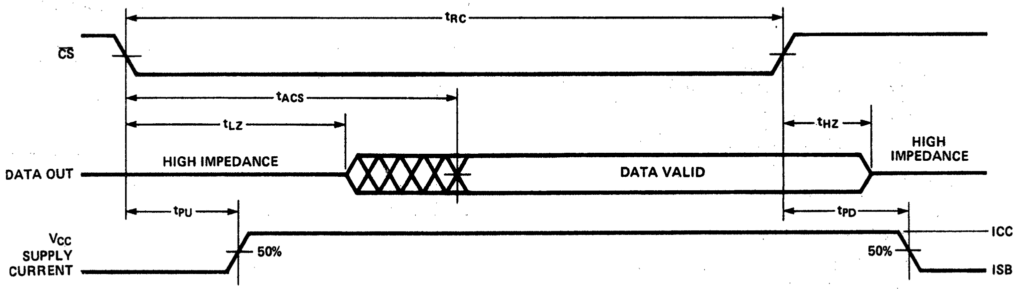
Read Cycle No. 1 (Notes 7, 8)



0015-6

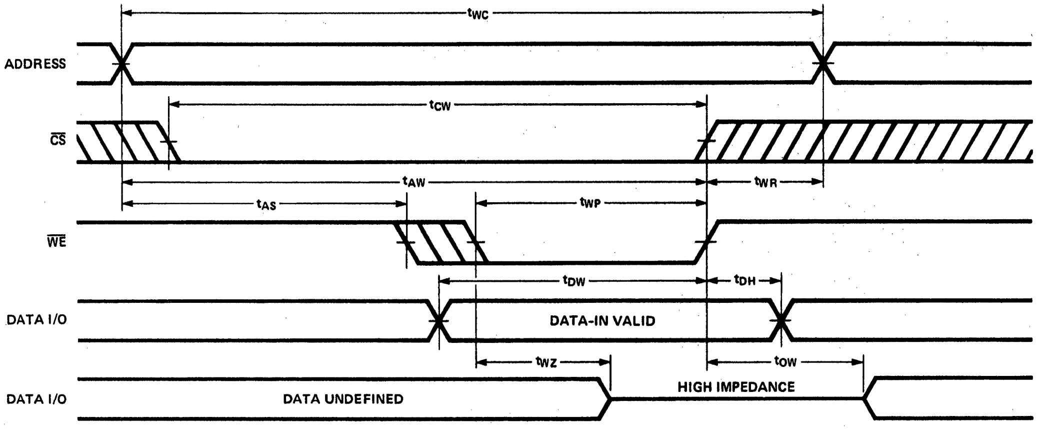
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 7, 9)


t_{RC}
$\overline{CS}$
t_{ACS}
t_{LZ}
t_{HZ}
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

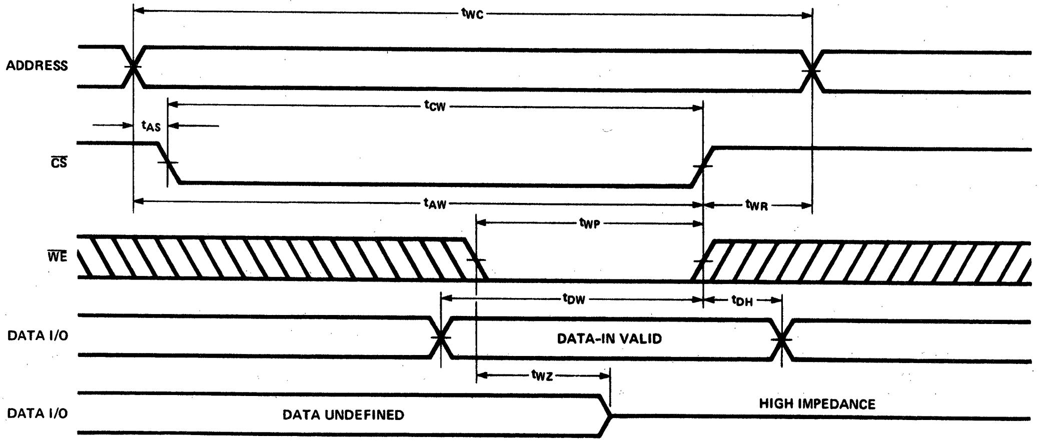
0015-9

Write Cycle No. 1 ($\overline{WE}$ Controlled)


t_{WC}
ADDRESS
t_{CW}
$\overline{CS}$
t_{AW}
t_{WR}
t_{AS}
t_{WP}
$\overline{WE}$
t_{DW}
t_{DH}
DATA I/O
DATA-IN VALID
t_{WZ}
t_{OW}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0015-8

Write Cycle No. 2 ($\overline{CS}$ Controlled)


t_{WC}
ADDRESS
t_{CW}
t_{AS}
$\overline{CS}$
t_{AW}
t_{WR}
t_{WP}
$\overline{WE}$
t_{DW}
t_{DH}
DATA I/O
DATA-IN VALID
t_{WZ}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0015-7

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a HIGH impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2148-35 PC CY2149-35 PC	P3	Commercial
	CY2148-35 DC CY2149-35 DC	D4	
	CY21L48-35 PC CY21L49-35 PC	P3	Commercial
	CY21L48-35 DC CY21L49-35 DC	D4	
45	CY2148-45 PC CY2149-45 PC	P3	Commercial
	CY2148-45 DC CY2149-45 DC	D4	
	CY2148-45 DMB CY2149-45 DMB	D4	Military
	CY21L48-45 PC CY21L49-45 PC	P3	Commercial
	CY21L48-45 DC CY21L49-45 DC	D4	
55	CY2148-55 PC CY2149-55 PC	P3	Commercial
	CY2148-55 DC CY2149-55 DC	D4	
	CY2148-55 DMB CY2149-55 DMB	D4	Military
	CY21L48-55 PC CY21L49-55 PC	P3	Commercial
	CY21L48-55 DC CY21L49-55 DC	D4	

CY6116

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—35 ns**
- **Low active power — 660 mW**
- **Low standby power — 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

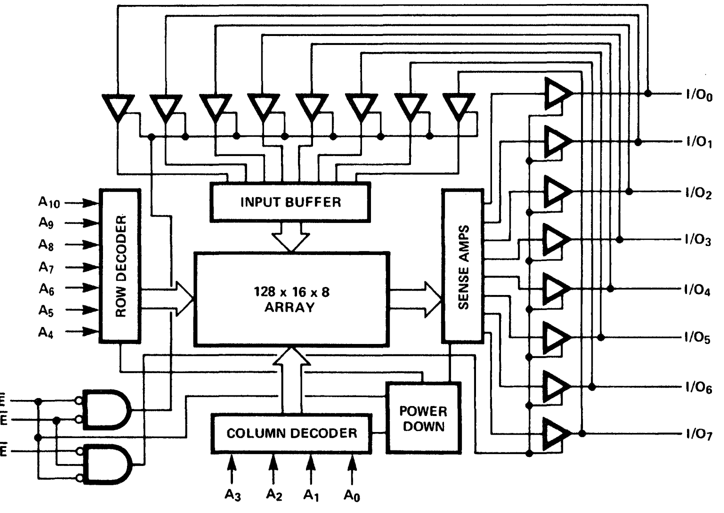
The CY6116 is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY6116 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

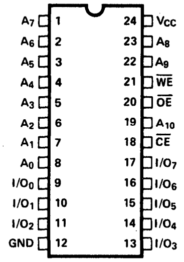
The CY6116 utilizes a die coat to ensure alpha immunity.

Logic Block Diagram

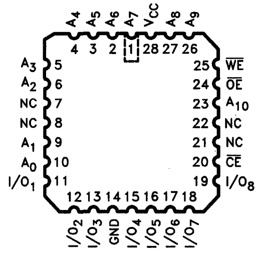

A_{10}
A_9
A_8
A_7
A_6
A_5
A_4
ROW DECODER
INPUT BUFFER
128 x 16 x 8
ARRAY
SENSE AMPS
$\overline{CE}$
$\overline{WE}$
$\overline{OE}$
COLUMN DECODER
POWER DOWN
A_3
A_2
A_1
A_0
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7

0087–1

Pin Configurations


A_7 1
A_6 2
A_5 3
A_4 4
A_3 5
A_2 6
A_1 7
A_0 8
I/O_0 9
I/O_1 10
I/O_2 11
GND 12
24 V_{CC}
23 A_8
22 A_9
21 $\overline{WE}$
20 $\overline{OE}$
19 A_{10}
18 $\overline{CE}$
17 I/O_7
16 I/O_6
15 I/O_5
14 I/O_4
13 I/O_3

0087–2


A_4 A_5 A_6 A_7 V_{CC} A_8 A_9
4 3 2 1 28 27 26
A_3 5
A_2 6
NC 7
NC 8
A_1 9
A_0 10
I/O_1 11
25 $\overline{WE}$
24 $\overline{OE}$
23 A_{10}
22 NC
21 NC
20 $\overline{CE}$
19 I/O_8
12 13 14 15 16 17 18
I/O_2 I/O_3 GND I/O_4 I/O_5 I/O_6 I/O_7

0087–3

Selection Guide

		CY6116-35	CY6116-45	CY6116-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)	Commercial	20	20	20
	Military	20	20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		CY6116-35, 45, 55		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled			10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120	mA
			Military		130	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		20	mA
			Military		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

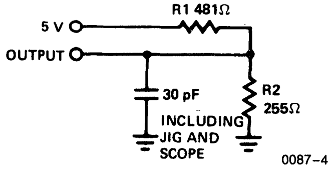

R1 481Ω
5 V
OUTPUT
30 pF
INCLUDING
JIG AND
SCOPE
R2
255Ω
0087-4

Figure 1a

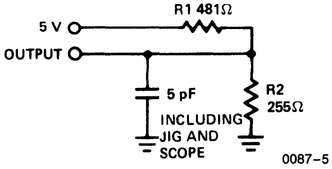

R1 481Ω
5 V
OUTPUT
5 pF
INCLUDING
JIG AND
SCOPE
R2
255Ω
0087-5

Figure 1b

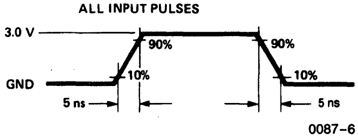
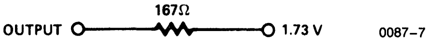

ALL INPUT PULSES
3.0 V
GND
90%
90%
10%
10%
5 ns
5 ns
0087-6

Figure 2

Equivalent to:

THÉVENIN EQUIVALENT


167Ω
OUTPUT
1.73 V
0087-7

Switching Characteristics Over Operating Range[4]

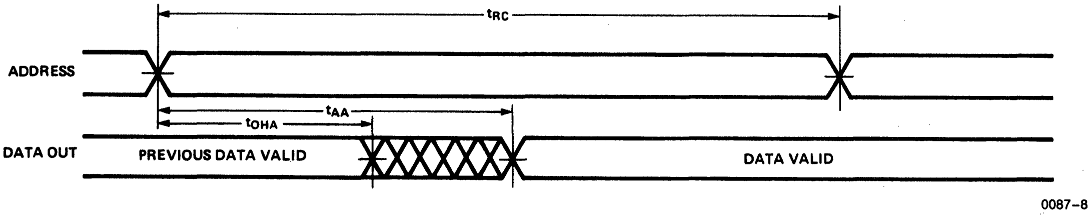
Parameters	Description	6116-35		6116-45		6116-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[5]		15		15		20	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[5, 6]		15		20		20	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		25	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	30		40		40		ns
t_{AW}	Address Set-up to Write End	30		40		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	20		20		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z		15		15		20	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		ns

Notes:

3. Data I/O Pins enter high-impedance state, as shown, when $\overline{\text{OE}}$ is held LOW during write.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are specified and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{\text{WE}}$ is HIGH for read cycle.
9. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Switching Waveforms

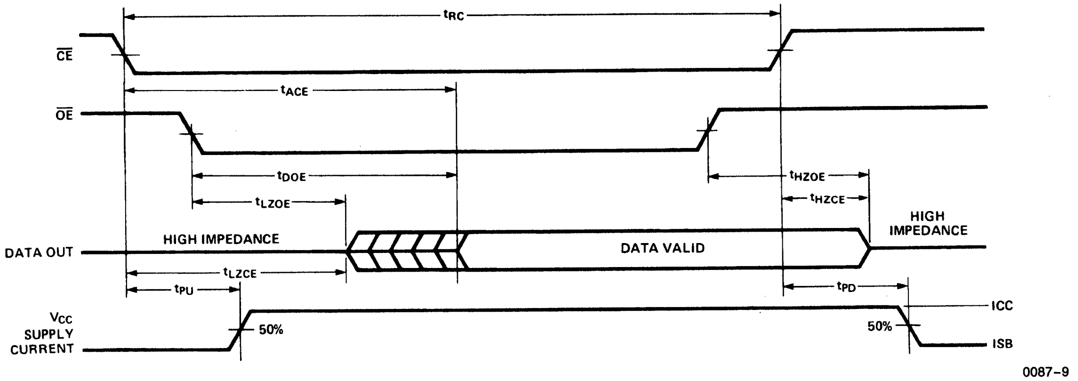
Read Cycle No. 1 (Notes 8, 9)



0087–8

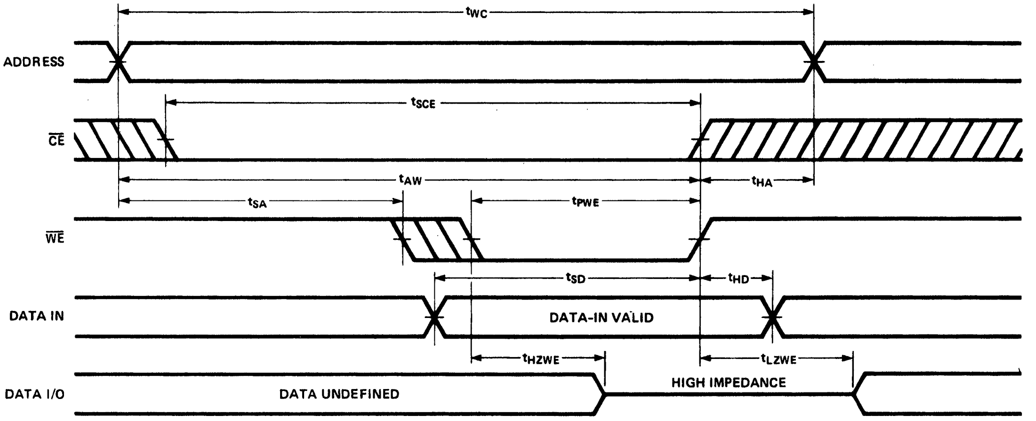
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


tRC
CE
tACE
OE
tDOE
tLZOE
tHZOE
tHZCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
tLZCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

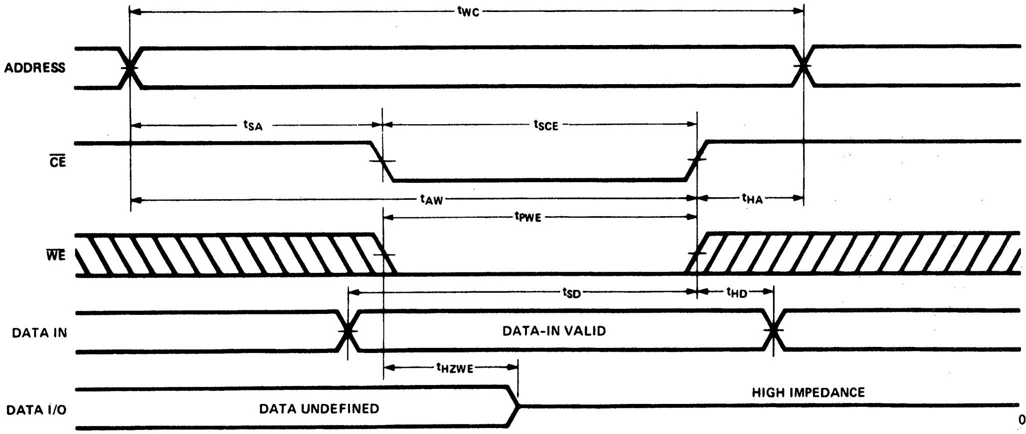
0087-9

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 3, 7)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0087-10

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Notes 3, 7)

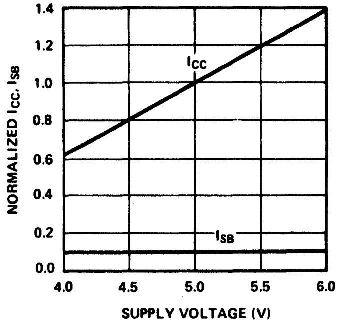

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0087-11

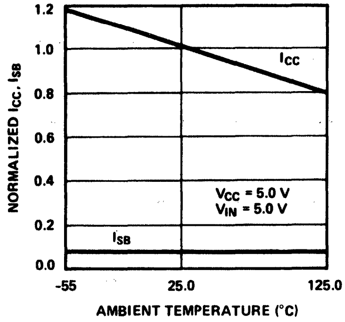
Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

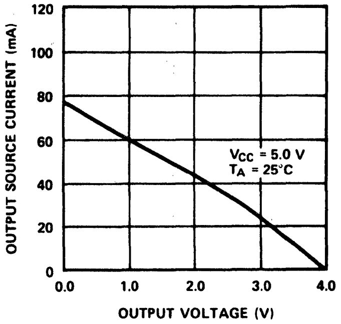
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



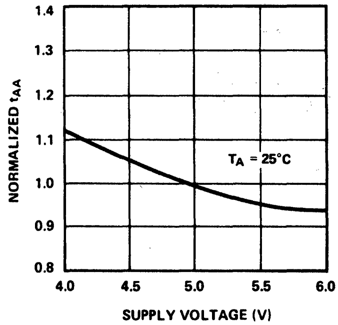
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



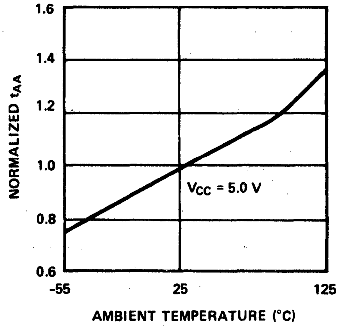
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



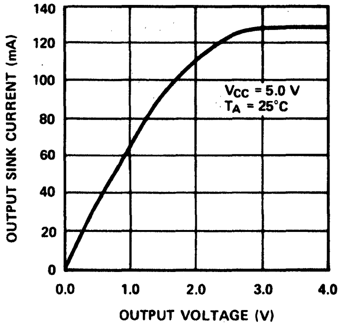
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



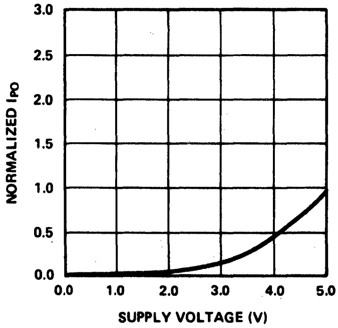
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



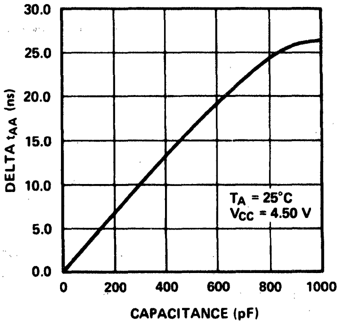
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



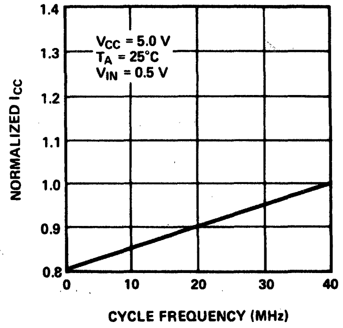
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0087-12

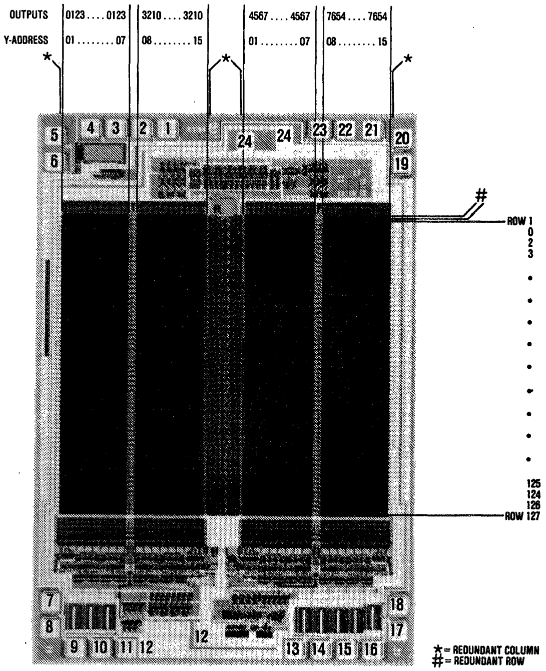
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY6116-35PC CY6116-35DC CY6116-35LC	P11 D12 L64	Commercial
	CY6116-35DMB CY6116-35LMB	D12 L64	Military
45	CY6116-45PC CY6116-45DC CY6116-45LC	P11 D12 L64	Commercial
	CY6116-45DMB CY6116-45LMB	D12 L64	Military
55	CY6116-55PC CY6116-55DC CY6116-55LC	P11 D12 L64	Commercial
	CY6116-55DMB CY6116-55LMB	D12 L64	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_3	8
A_1	Y_2	7
A_2	Y_1	6
A_3	Y_0	5
A_4	X_2	4
A_5	X_4	3
A_6	X_3	2
A_7	X_0	1
A_8	X_5	23
A_9	X_6	22
A_{10}	X_1	19

Bit Map


OUTPUTS
0123....0123
3210....3210
4567....4567
7654....7654
Y-ADDRESS
01........07
08........15
01........07
08........15
*
*
*
5
4
3
2
1
24
24
23
22
21
20
6
19
#
ROW 1
0
2
3
125
124
126
ROW 127
7
8
9
10
11
12
12
13
14
15
16
18
17
* = REDUNDANT COLUMN
# = REDUNDANT ROW

0087-13

CYPRESS SEMICONDUCTOR

CY7C122

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 330 mW (commercial)**
  - **— 495 mW (military)**
- **Separate inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2000V static discharge**
- **TTL compatible inputs and outputs**

Functional Description

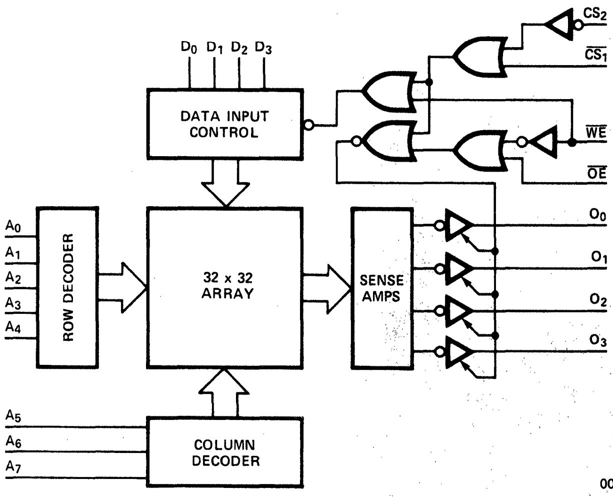
The CY7C122 is a high performance CMOS static RAM organized as 256 words x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS}_1$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select one ($\overline{CS}_1$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

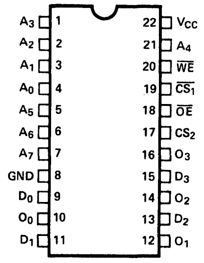
Logic Block Diagram



D0 D1 D2 D3
DATA INPUT CONTROL
CS2
CS1
WE
OE
A0
A1
A2
A3
A4
ROW DECODER
32 x 32 ARRAY
SENSE AMPS
O0
O1
O2
O3
A5
A6
A7
COLUMN DECODER

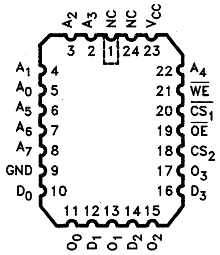
0003-1

Pin Configurations



A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
D0 9
O0 10
D1 11
22 Vcc
21 A4
20 WE
19 CS1
18 OE
17 CS2
16 O3
15 D3
14 O2
13 D2
12 O1

0003-2



A2 A3 NC NC Vcc
3 2 1 24 23
A1 4
A0 5
A5 6
A6 7
A7 8
GND 9
D0 10
22 A4
21 WE
20 CS1
19 OE
18 CS2
17 O3
16 D3
11 12 13 14 15
O0 D1 O1 D2 O2

0003-10

Selection Guide

		7C122-15	7C122-25	7C122-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military	NA	25	35
Maximum Operating Current (mA)	Commercial	90	60	60
	Military	NA	90	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential Pin 22 to Pin 8) .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State..................... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current, into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Logic Table

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	D_0–D_3		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0–O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

Notes: H = HIGH Voltage L = LOW Voltage X = Don't Care
High Z = High Impedance

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C122-15		7C122-25 7C122-35		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $I_{OH} = -5.2$ mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $I_{OL} = 8.0$ mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$			10		10	μA
V_{CD}	Input Diode Clamp Voltage				Note 2		Note 2	V
I_{OZ}	Output Current (High-Z)	$V_{OL} \leq V_{OUT} \leq V_{OH}$ Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current (Note 1)	V_{CC} = Max., V_{OUT} = GND	Commercial		−70		−70	mA
			Military		−80		−80	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		60	mA
			Military		NA		90	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz $V_{CC} = 5.0V$	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. The CMOS process does not provide a clamp diode. However, the CY7C122 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. Tested on a sample basis.

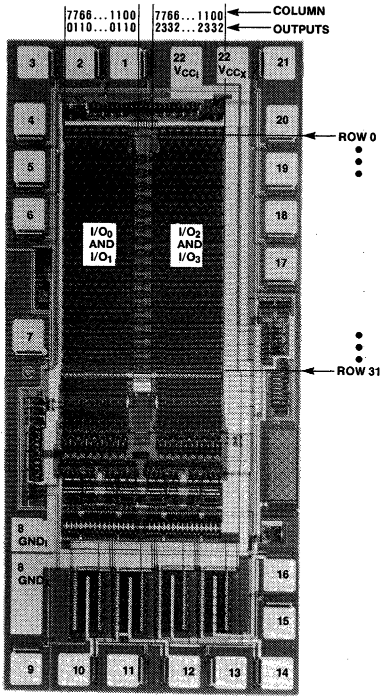
Switching Characteristics Over the Operating Range[5]

Parameters	Description	Test Conditions	CY7C122-15		CY7C122-25		CY7C122-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		15		25		35		ns
t_{ACS}	Chip Select Time			8		15		25	ns
t_{ZRCS}	Chip Select to High-Z	Note 6		12		20		30	ns
t_{AOS}	Output Enable Time			8		15		25	ns
t_{ZROS}	Output Enable to High-Z	Note 6		12		20		30	ns
t_{AA}	Address Access Time			15		25		35	ns
WRITE CYCLE									
t_{WC}	Write Cycle Time		15		25		35		ns
t_{ZWS}	Write Disable to High-Z	Note 6		12		20		30	ns
t_{WR}	Write Recovery Time			12		20		25	ns
t_W	Write Pulse Width	Note 4	11		15		25		ns
t_{WSD}	Data Setup Time Prior to Write		0		5		5		ns
t_{WHD}	Data Hold Time After Write		2		5		5		ns
t_{WSA}	Address Setup Time	Note 4	0		5		10		ns
t_{WHA}	Address Hold Time		4		5		5		ns
t_{WSCS}	Chip Select Setup Time		0		5		5		ns
t_{WHCS}	Chip Select Hold Time		2		5		5		ns

Notes:

4. t_W measured at t_{WSA} = min.; t_{WSA} measured at t_W = min.
5. Test conditions assume signal transition times of 5 ns or less for the −15 product and 10 ns or less for the −25 and −35 product. Timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in *Figure 1a.*
6. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input with load shown in *Figure 1b.*

Bit Map



0003–3

Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	4
A_1	AX1	3
A_2	AX2	2
A_3	AX3	1
A_4	AX4	21
A_5	AY0	5
A_6	AY1	6
A_7	AY2	7

AC Test Loads and Waveforms

AC Test Loads

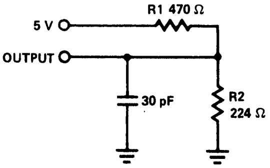
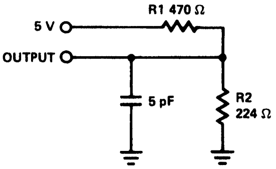

R1 470 Ω
5 V
OUTPUT
30 pF
R2
224 Ω

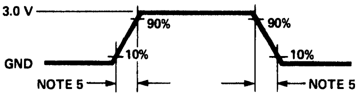
Figure 1a


R1 470 Ω
5 V
OUTPUT
5 pF
R2
224 Ω

0003-4

Figure 1b

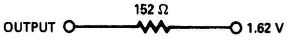
Input Pulses


3.0 V
GND
90%
10%
90%
10%
NOTE 5
NOTE 5

0003-5

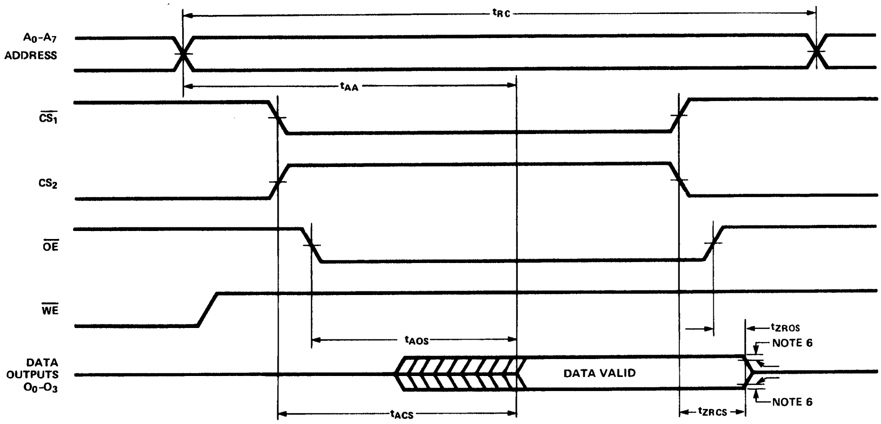
Figure 2

Equivalent to: THÉVENIN EQUIVALENT


152 Ω
OUTPUT
1.62 V

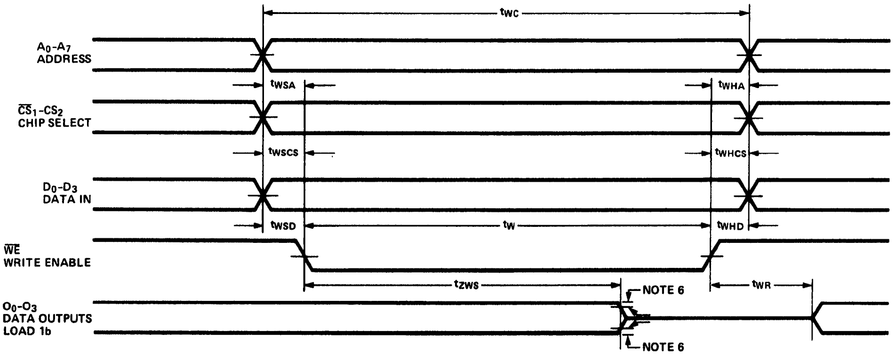
0003-6

Read Mode


tRC
A0-A7
ADDRESS
tAA
CS1
CS2
OE
WE
tAOS
tZROS
NOTE 6
DATA
OUTPUTS
O0-O3
DATA VALID
NOTE 6
tACS
tZRCS

0003-7

Write Mode


tWC
A0-A7
ADDRESS
tWSA
tWHA
CS1-CS2
CHIP SELECT
tWSCS
tWHCS
D0-D3
DATA IN
tWSD
tW
tWHD
WE
WRITE ENABLE
tZWS
NOTE 6
tWR
O0-O3
DATA OUTPUTS
LOAD 1b
NOTE 6

0003-8

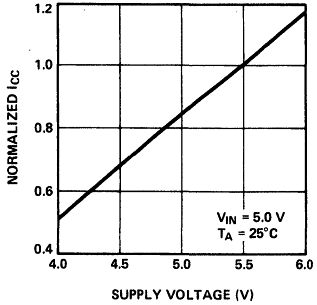
(All above measurements referenced to 1.5V unless otherwise stated.)

Note:

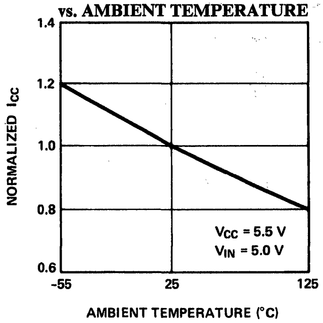
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

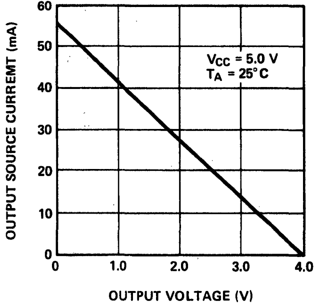
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



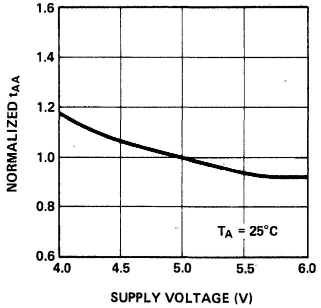
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



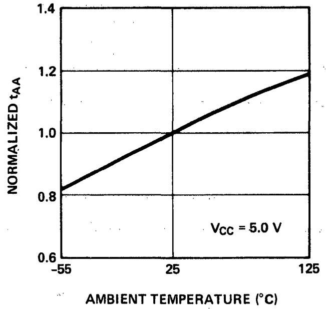
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



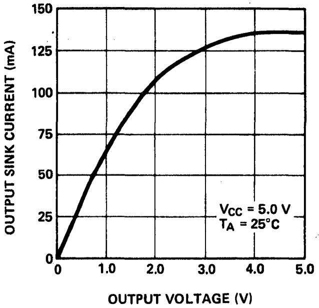
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



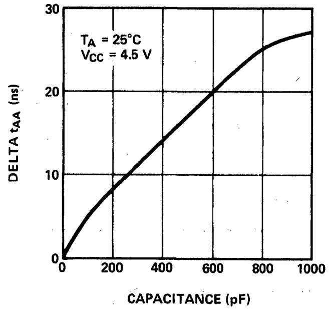
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



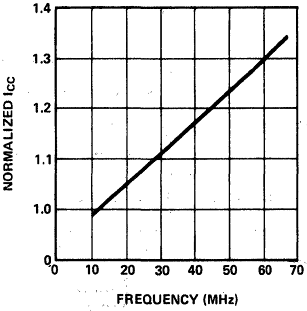
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0003-9

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C122-15PC	P7	Commercial
	CY7C122-15DC	D8	Commercial
25	CY7C122-25PC	P7	Commercial
	CY7C122-25DC	D8	Commercial
	CY7C122-25LC	L53	Commercial
	CY7C122-25DMB	D8	Military
35	CY7C122-35PC	P7	Commercial
	CY7C122-35DC	D8	Commercial
	CY7C122-35LC	L53	Commercial
	CY7C122-35DMB	D8	Military
	CY7C122-35LMB	L53	Military

CYPRESS SEMICONDUCTOR

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 7 ns (commercial)**
  - **— 15 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 825 mW (military)**
- **Separate inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **TTL compatible inputs and outputs**
- **24 pin**
- **300 MIL package**

Functional Description

The CY7C123 is a high performance CMOS static RAM organized as 256 words x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

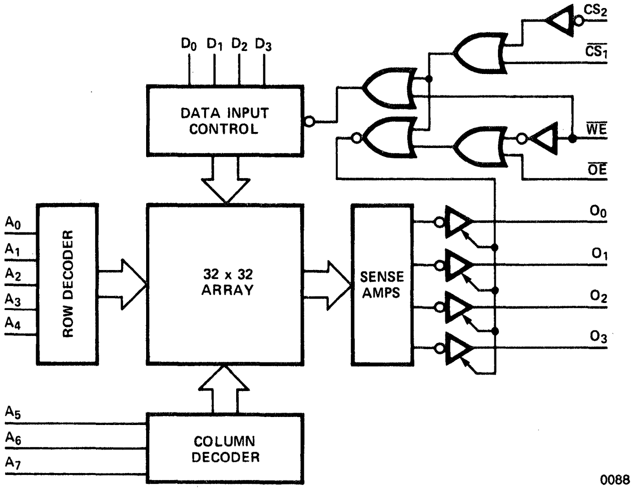
An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS}_1$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select one ($\overline{CS}_1$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

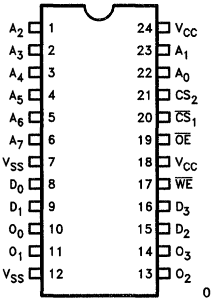
Logic Block Diagram



D0 D1 D2 D3
DATA INPUT CONTROL
CS2
CS1
WE
OE
A0
A1
A2
A3
A4
ROW DECODER
32 x 32 ARRAY
SENSE AMPS
O0
O1
O2
O3
A5
A6
A7
COLUMN DECODER

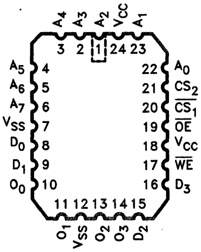
0088-1

Pin Configurations



A2 1
A3 2
A4 3
A5 4
A6 5
A7 6
VSS 7
D0 8
D1 9
O0 10
O1 11
VSS 12
24 VCC
23 A1
22 A0
21 CS2
20 CS1
19 OE
18 VCC
17 WE
16 D3
15 D2
14 O3
13 O2

0088-2



A4 A3 A2 VCC A1
3 2 1 24 23
A5 4
A6 5
A7 6
VSS 7
D0 8
D1 9
O0 10
22 A0
21 CS2
20 CS1
19 OE
18 VCC
17 WE
16 D3
11 12 13 14 15
O1 VSS O2 O3 D2

0088-3

Selection Guide

		7C123-7	7C123-12	7C123-15
Maximum Access Time (ns)	Commercial	7	12	NA
	Military	NA	NA	15
Maximum Operating Current (mA)	Commercial	120	120	NA
	Military	NA	NA	150

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
Pins 24 & 18 to Pin 7 .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.5V to +7.0V

Output Current, into Outputs (Low) .... 20 mA

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Logic Table

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS}_1$	CS_2	$\overline{WE}$	D_0–D_3		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0–O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

Notes: H = HIGH Voltage L = LOW Voltage X = Don't Care
High Z = High Impedance

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C123-7 7C123-12		7C123-15		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			10		10	μA
I_{OZ}	Output Current (High-Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH} Output Disabled		−10	+10	−10	+10	μA
I_{CC}	Power Supply Current	V_{CC} = Max.,	Commercial		120		N/A	mA
		I_{OUT} = 0 mA	Military		NA		150	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. Tested on a sample basis.

Switching Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C123-7		7C123-12		7C123-15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		7		12		15		ns
t_{AA}	Address Access Time			7		12		15	ns
t_{ACS}	Chip Select Time			7		8		10	ns
t_{DOE}	Output Enable Time			7		8		10	ns
t_{HZCS}	Chip Select to Output Hi-Z	Note 4, 5		5		6.5		8	ns
t_{HZOE}	Output Enable to Out Hi-Z	Note 4		5		6.5		8	ns
t_{LZCS}	Chip Select to Out Low-Z	Note 4, 5	2		2		2		ns
t_{LZOE}	Output Enable to Out Low-Z	Note 4	2		2		2		ns
WRITE CYCLE									
t_{WC}	Write Cycle Time		7		12		15		ns
t_{HZWE}	Write Enable to Hi-Z			5.5		7		8	ns
t_{LZWE}	Write Enable to Low-Z		2		2		2		ns
t_{PWE}	Write Pulse Width	Note 3	5		9		11		ns
t_{SD}	Data Setup to End of Write		5		9		11		ns
t_{HD}	Data Hold Time After Write		2		2		2		ns
t_{SA}	Add Setup to Start of Write	Note 3	0		0		2		ns
t_{HA}	Address Hold Time		2		3		4		ns
t_{SCS}	CS Active Low to End of Write		5		9		11		ns
t_{AW}	Add Setup to End of Write		5		9		13		ns

Notes:

3. t_{PWE} measured at t_{SA} = min.; t_{SA} measured at T_{PWE} = min.
4. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input with load shown in *Figure 1b*.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are sampled and not 100% tested.

AC Test Loads and Waveforms

AC Test Loads

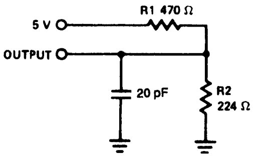

5 V
R1 470 Ω
OUTPUT
20 pF
R2
224 Ω

Figure 1a

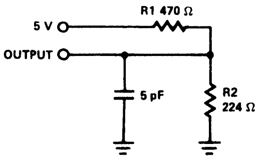
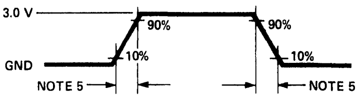

5 V
R1 470 Ω
OUTPUT
5 pF
R2
224 Ω

Figure 1b

0088-4

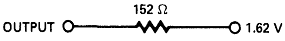
Input Pulses


3.0 V
GND
90%
10%
90%
10%
NOTE 5
NOTE 5

0088-5

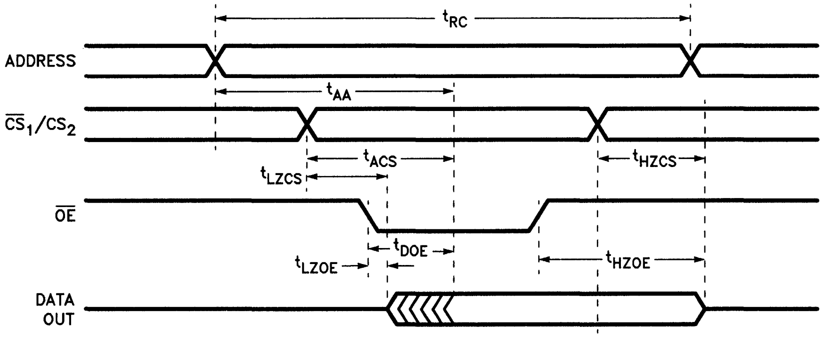
Figure 2

Equivalent to: THÉVENIN EQUIVALENT


152 Ω
OUTPUT
1.62 V

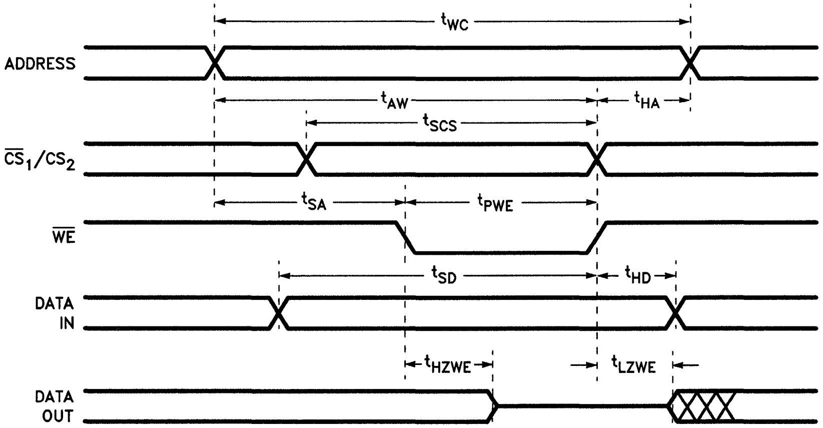
0088-6

Read Mode


t_{RC}
ADDRESS
t_{AA}
$\overline{CS}_1/CS_2$
t_{ACS}
t_{HZCS}
t_{LZCS}
$\overline{OE}$
t_{DOE}
t_{LZOE}
t_{HZOE}
DATA OUT

0088-11

Write Mode


t_{WC}
ADDRESS
t_{AW}
t_{HA}
t_{SCS}
$\overline{CS}_1/CS_2$
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
t_{HZWE}
t_{LZWE}
DATA OUT

0088-12

(All above measurements referenced to 1.5V unless otherwise stated.)

Note:

Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
7	CY7C123-7PC	P13	Commercial
	CY7C123-7DC	D14	
	CY7C123-7LC	L53	
12	CY7C123-12PC	P13	
	CY7C123-12DC	D14	
	CY7C123-12LC	L53	
15	CY7C123-15DMB	D14	Military
	CY7C123-15LMB	L53	

CYPRESS
SEMICONDUCTOR

CY7C128

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power**
  - **660 mW (commercial)**
  - **825 mW (military)**
- **Low standby power**
  - **110 mW**
- **SOIC package**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

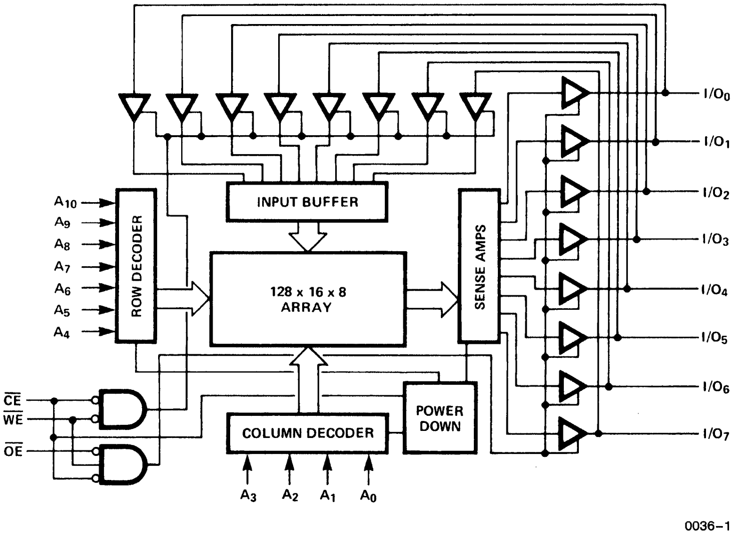
The CY7C128 is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

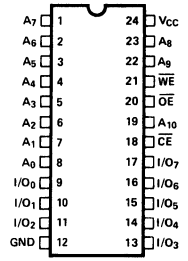
The 7C128 utilizes a die coat to ensure alpha immunity.

Logic Block Diagram

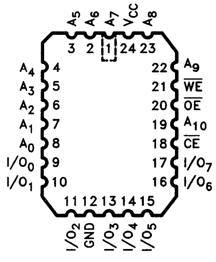

I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
INPUT BUFFER
A10
A9
A8
A7
A6
A5
A4
ROW DECODER
128 x 16 x 8 ARRAY
SENSE AMPS
CE
WE
OE
POWER DOWN
COLUMN DECODER
A3
A2
A1
A0

0036-1

Pin Configurations


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
I/O0 9
I/O1 10
I/O2 11
GND 12
24 VCC
23 A8
22 A9
21 WE
20 OE
19 A10
18 CE
17 I/O7
16 I/O6
15 I/O5
14 I/O4
13 I/O3

0036-2


A5 A6 A7 VCC A8
3 2 1 24 23
A4 4
A3 5
A2 6
A1 7
A0 8
I/O0 9
I/O1 10
22 A9
21 WE
20 OE
19 A10
18 CE
17 I/O7
16 I/O6
11 12 13 14 15
I/O2 GND I/O3 I/O4 I/O5

0036-3

Selection Guide

		7C128-25	7C128-35	7C128-45	7C128-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120	90
	Military		150	130	100
Maximum Standby Current (mA)	Commercial	20	20	20	20
	Military		20	20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(Per MIL-STD-883 Method 3015.2)

Latch-up Current.......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C128		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $I_{OH} = -4.0$ mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input HIGH Voltage	Commercial -25, Military -35		2.0	V_{CC}	V
		All Others		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ Output Disabled		−40	40	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial -25, -35, -45		120	mA
			Commercial -55		90	mA
			Military -35		150	mA
			Military -45		130	mA
			Military -55		100	mA
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Commercial		20	mA
			Military*		20	

*35 ns and 55 ns only

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz $V_{CC} = 5.0V$	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

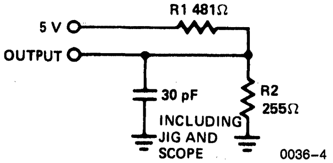

R1 481Ω
5 V
OUTPUT
30 pF
INCLUDING
JIG AND
SCOPE
R2
255Ω
0036-4

Figure 1a

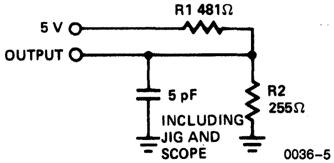

R1 481Ω
5 V
OUTPUT
5 pF
INCLUDING
JIG AND
SCOPE
R2
255Ω
0036-5

Figure 1b

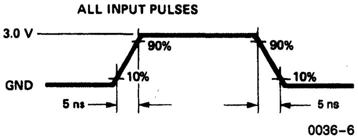
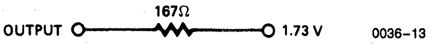

ALL INPUT PULSES
3.0 V
GND
90%
10%
90%
10%
5 ns
5 ns
0036-6

Figure 2

Equivalent to:

THÉVENIN EQUIVALENT


167Ω
OUTPUT
1.73 V
0036-13

Switching Characteristics Over Operating Range[4]

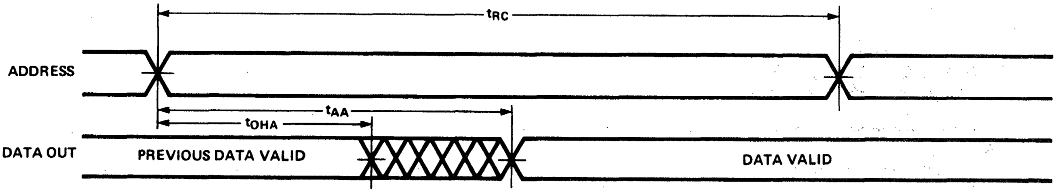
Parameters	Description	7C128-25		7C128-35		7C128-45		7C128-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		12		15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		12		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		25		25	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		50		ns
t_{AW}	Address Set-up to Write End	20		30		40		50		ns
t_{HA}	Address Hold from Write End	2		[11]		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	WE Pulse Width	12		20		20		25		ns
t_{SD}	Data Set-up to Write End	10		15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		10		15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns

Notes:

3. Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are specified and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. 0 ns for commercial, 2 ns for military.

Switching Waveforms

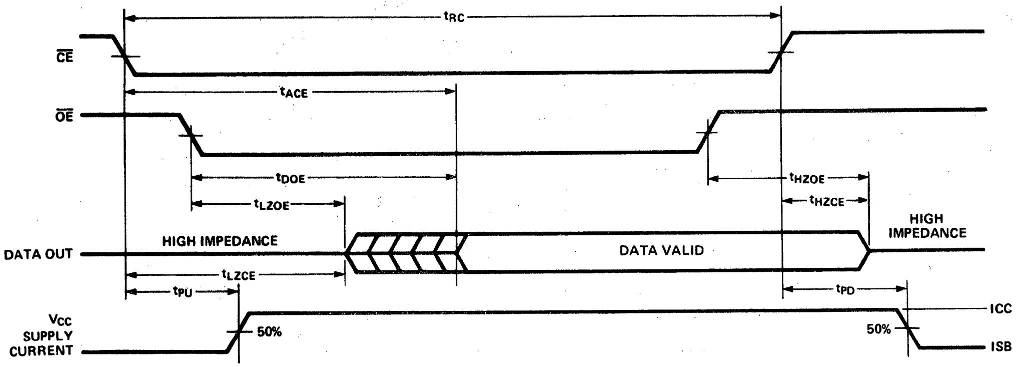
Read Cycle No. 1 (Notes 8, 9)



0036-7

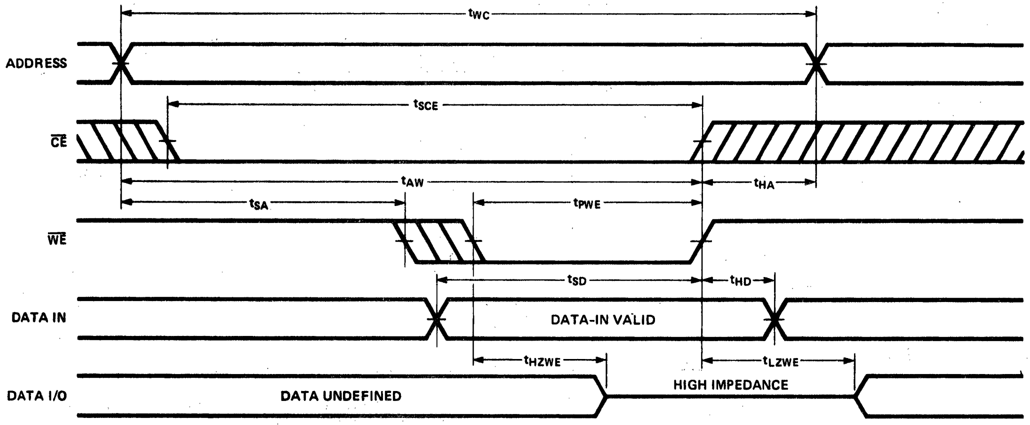
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


t_{RC}
$\overline{CE}$
t_{ACE}
$\overline{OE}$
t_{DOE}
t_{HZOE}
t_{LZOE}
t_{HZCE}
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
t_{LZCE}
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

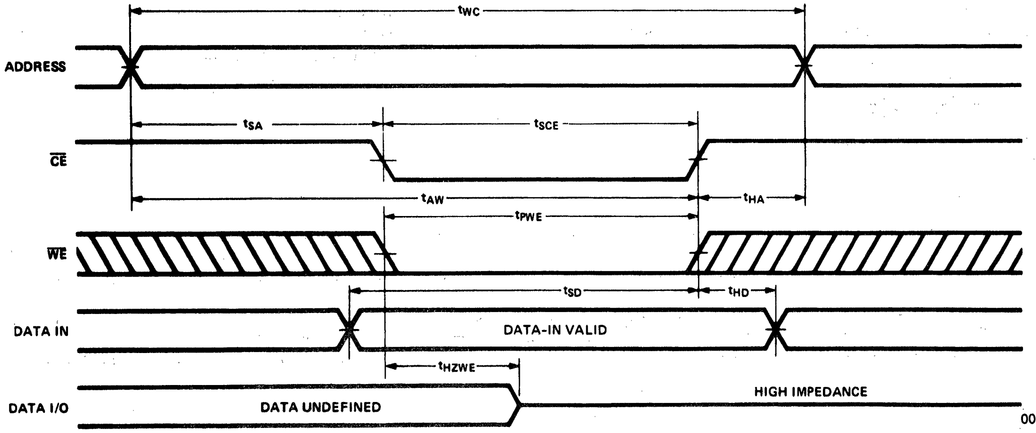
0036-8

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 3, 7)


t_{WC}
ADDRESS
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0036-9

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Notes 3, 7)

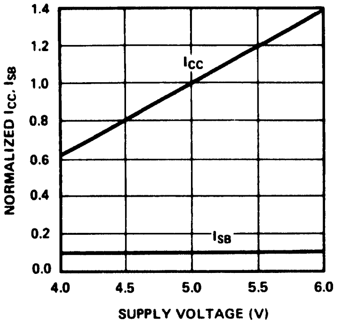

t_{WC}
ADDRESS
t_{SA}
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0036-10

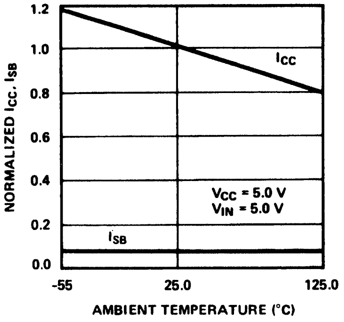
Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

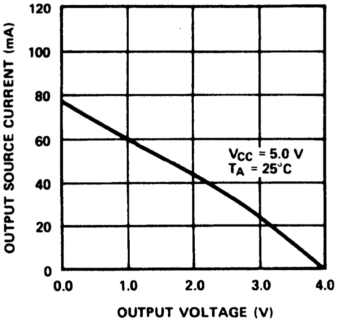
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



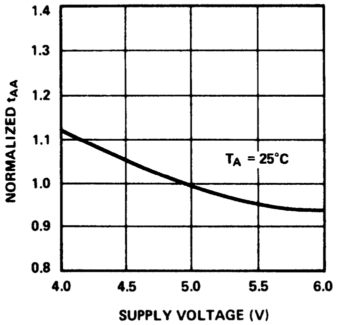
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



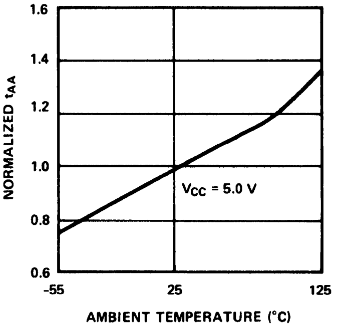
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



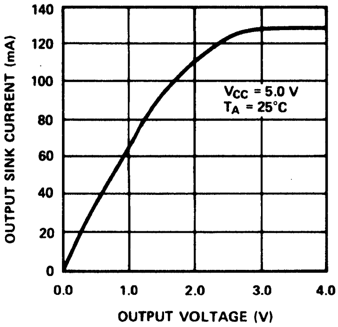
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



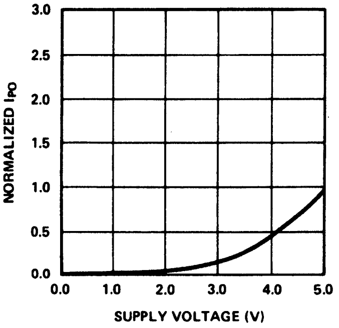
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



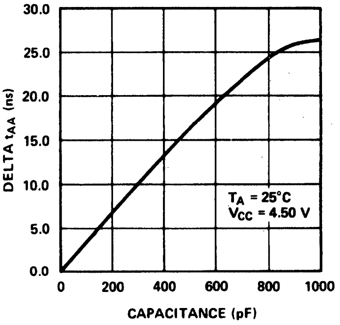
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



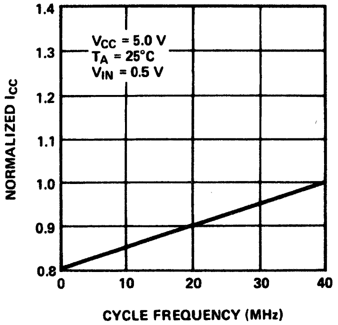
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0036-11

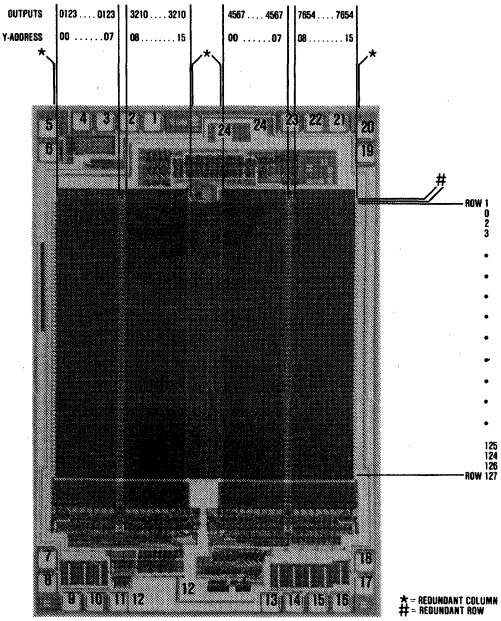
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C128-25PC CY7C128-25SC CY7C128-25DC CY7C128-25LC	P13 S13 D14 L53	Commercial
35	CY7C128-35PC CY7C128-35SC CY7C128-35DC CY7C128-35LC	P13 S13 D14 L53	Commercial
	CY7C128-35DMB CY7C128-35LMB	D14 L53	Military
45	CY7C128-45PC CY7C128-45SC CY7C128-45DC CY7C128-45LC	P13 S13 D14 L53	Commercial
	CY7C128-45DMB CY7C128-45LMB	D14 L53	Military
55	CY7C128-55PC CY7C128-55SC CY7C128-55DC CY7C128-55LC	P13 S13 D14 L53	Commercial
	CY7C128-55DMB CY7C128-55LMB	D14 L53	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_3	8
A_1	Y_2	7
A_2	Y_1	6
A_3	Y_0	5
A_4	X_2	4
A_5	X_4	3
A_6	X_3	2
A_7	X_0	1
A_8	X_5	23
A_9	X_6	22
A_{10}	X_1	19

Bit Map


OUTPUTS
0123....0123
3210....3210
4567....4567
7654....7654
Y-ADDRESS
00......07
08........15
00......07
08........15
*
*
*
#
ROW 1
0
2
3
125
124
126
ROW 127
5
4
3
2
1
24
24
23
22
21
20
6
19
7
8
9
10
11
12
12
13
14
15
16
17
18
* = REDUNDANT COLUMN
# = REDUNDANT ROW

0036–12

PRELIMINARY **CY7C130**
CY7C140

1024 x 8 Dual Port Static RAM

Features

- 0.8 micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130 easily expands data bus width to 16 or more bits using SLAVE CY7C140
- $\overline{\text{BUSY}}$ output flag on CY7C130; $\overline{\text{BUSY}}$ input on CY7C140
- $\overline{\text{INT}}$ flag for port to port communication

Functional Description

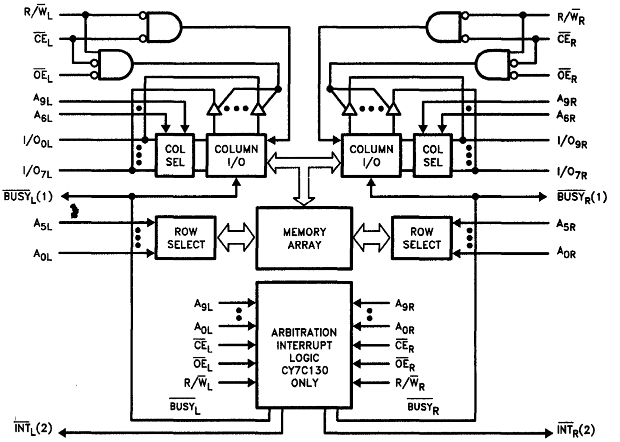
The CY7C130/CY7C140 are high speed CMOS 1K x 8 Dual Port Static RAMS. Two ports are provided permitting independent access to any location in memory. The CY7C130 can be utilized as either a stand-alone 8-bit Dual Port Static RAM or as a MASTER Dual Port RAM in conjunction with the CY7C140 SLAVE Dual Port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, Bit-Slice, or multiprocessor designs.

Each port has independent control pins; Chip Enable ($\overline{\text{CE}}$), Write Enable ($\overline{\text{WE}}$), and Output Enable ($\overline{\text{OE}}$). Two flags are provided on each port, $\overline{\text{BUSY}}$ and $\overline{\text{INT}}$. $\overline{\text{BUSY}}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{\text{INT}}$ is an interrupt flag indicating that data has been placed in a unique location by the other port. An automatic power down feature is controlled independently on each port by the Chip Enable ($\overline{\text{CE}}$) pin.

The CY7C130/CY7C140 are available in both 48-pin DIP and 52-pin LCC.

A die coat is used to insure alpha immunity.

Logic Block Diagram

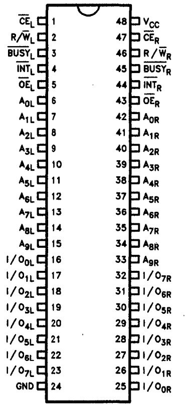

R/W̄L
CE̅L
OE̅L
A9L
A6L
I/O0L
I/O7L
BUSYL(1)
A5L
A0L
COL SEL
COLUMN I/O
ROW SELECT
MEMORY ARRAY
A9L
A0L
CEL
OEL
R/WL
BUSYL
ARBITRATION INTERRUPT LOGIC CY7C130 ONLY
A9R
A0R
CER
OER
R/WR
BUSYR
INTL(2)
R/WR
CER
OER
A9R
A6R
I/O9R
I/O7R
COLUMN I/O
COL SEL
BUSYR(1)
ROW SELECT
A5R
A0R
INTR(2)

0114-1

Notes:

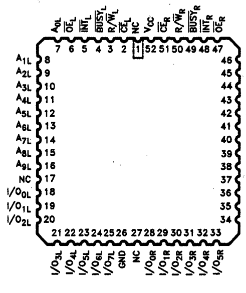
1. CY7C130 (Master): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor.
   CY7C140 (Slave): $\overline{\text{BUSY}}$ is input.
2. Open drain outputs: pullup resistor required.

Pin Configurations


CEL 1
R/WL 2
BUSYL 3
INTL 4
OEL 5
A0L 6
A1L 7
A2L 8
A3L 9
A4L 10
A5L 11
A6L 12
A7L 13
A8L 14
A9L 15
I/O0L 16
I/O1L 17
I/O2L 18
I/O3L 19
I/O4L 20
I/O5L 21
I/O6L 22
I/O7L 23
GND 24
48 VCC
47 CER
46 R/WR
45 BUSYR
44 INTR
43 OER
42 A0R
41 A1R
40 A2R
39 A3R
38 A4R
37 A5R
36 A6R
35 A7R
34 A8R
33 A9R
32 I/O7R
31 I/O6R
30 I/O5R
29 I/O4R
28 I/O3R
27 I/O2R
26 I/O1R
25 I/O0R

0114-2

DIP
Top View


A0L OEL INTL BUSYL R/WL CEL NC VCC CER R/WR BUSYR INTR OER
7 6 5 4 3 2 1 52 51 50 49 48 47
A1L 8
A2L 9
A3L 10
A4L 11
A5L 12
A6L 13
A7L 14
A8L 15
A9L 16
NC 17
I/O0L 18
I/O1L 19
I/O2L 20
46 A0R
45 A1R
44 A2R
43 A3R
42 A4R
41 A5R
40 A6R
39 A7R
38 A8R
37 A9R
36 NC
35 I/O7R
34 I/O6R
21 22 23 24 25 26 27 28 29 30 31 32 33
I/O3L I/O4L I/O5L I/O6L I/O7L GND NC I/O0R I/O1R I/O2R I/O3R I/O4R I/O5R

0114-3

LCC
Top View

Selection Guide

		7C130-35 7C140-35	7C130-45 7C140-45	7C130-55 7C140-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		150	150
Maximum Standby Current (mA)	Commercial	30	30	30
	Military		40	40

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C130-35 7C140-35		7C130-45 7C140-45		7C130-55 7C140-55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 6.0 mA			0.4		0.4		0.4	V
		I_{OL} = 8.0 mA			0.5		0.5		0.5	
		I_{OL} = 16.0 mA Note 6			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short[3] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120		120		120	mA
			Military*				150		150	
I_{SB}	Automatic $\overline{CE}$[4] Power Down Current									
I_{SB1}	Both Ports, TTL Inputs		Commercial		30		30		30	mA
I_{SB2}	One Port, TTL Input				75		75		75	mA
I_{SB3}	Both Ports, CMOS Inputs				15		15		15	mA
I_{SB4}	One Port, CMOS Inputs				65		65		65	mA
I_{SB1}	Both Ports, TTL Inputs		Military*				40		40	mA
I_{SB2}	One Port, TTL Input						100		100	mA
I_{SB3}	Both Ports, CMOS Inputs						30		30	mA
I_{SB4}	One Port, CMOS Inputs						80		80	mA

* -45 and -55 only

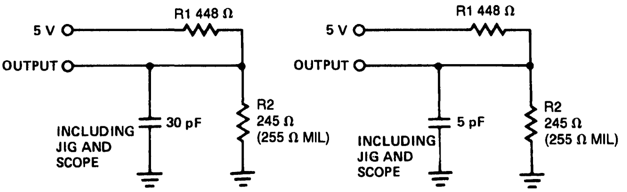
Capacitance[5]

Parameters	Description	Test Condtions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	

Notes:

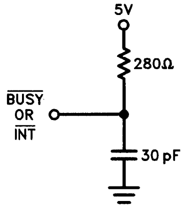
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested on a sample basis.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.

AC Test Loads and Waveforms


5 V
R1 448 Ω
OUTPUT
30 pF
INCLUDING JIG AND SCOPE
R2 245 Ω (255 Ω MIL)
5 V
R1 448 Ω
OUTPUT
5 pF
INCLUDING JIG AND SCOPE
R2 245 Ω (255 Ω MIL)

0114-5

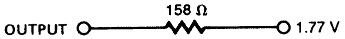
Figure 1 **Figure 2**


5V
280Ω
BUSY OR INT
30 pF

0114-4

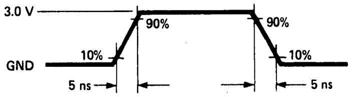
Figure 3. $\overline{\text{BUSY}}$ Output Load (CY7C130 Only)

Equivalent to: THÉVENIN EQUIVALENT


OUTPUT
158 Ω
1.77 V

0114-7

ALL INPUT PULSES


3.0 V
GND
90%
10%
90%
10%
5 ns
5 ns

0114-6

Figure 4

Switching Characteristics Over Operating Range[8]

Parameters	Description	7C130-35 7C140-35		7C130-45 7C140-45		7C130-55 7C140-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[9]		15		20		25	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[10]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[9,10]		15		20		25	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[11]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	30		35		40		ns
t_{AW}	Address Set-up to Write End	30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z		15		20		25	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		ns

Switching Characteristics Over Operating Range[8] (Continued)

Parameters	Description	7C130-35 7C140-35		7C130-45 7C140-45		7C130-55 7C140-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{WC}	Write Cycle Time	35		45		55		ns
t_{BLA}	$\overline{\text{BUSY}}$ LOW from Address Match		20		25		30	ns
t_{BHA}	$\overline{\text{BUSY}}$ HIGH from Address Mismatch		20		25		30	ns
t_{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW		20		25		30	ns
t_{BHC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WINS}	$\overline{\text{WE}}$ to $\overline{\text{INTERRUPT}}$ Set Time		15		20		25	ns
t_{EINS}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Set Time		25		35		45	ns
t_{INS}	Add to $\overline{\text{INTERRUPT}}$ Set Time		25		35		45	ns
t_{OINR}	$\overline{\text{OE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time		15		20		25	ns
t_{EINR}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time		25		35		45	ns
t_{INR}	Add to $\overline{\text{INTERRUPT}}$ Reset Time		25		35		45	ns
BUSY TIMING								
t_{WB}*	$\overline{\text{WE}}$ LOW after $\overline{\text{BUSY}}$	0		0		0		ns
t_{WH}	$\overline{\text{WE}}$ HIGH after $\overline{\text{BUSY}}$	15		15		15		ns
t_{BDD}	$\overline{\text{BUSY}}$ HIGH to Valid Data		20		25		30	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 15		Note 15		Note 15	ns
t_{WDD}	Write Pulse to Data Delay		Note 15		Note 15		Note 15	ns

* CY7C140 Only

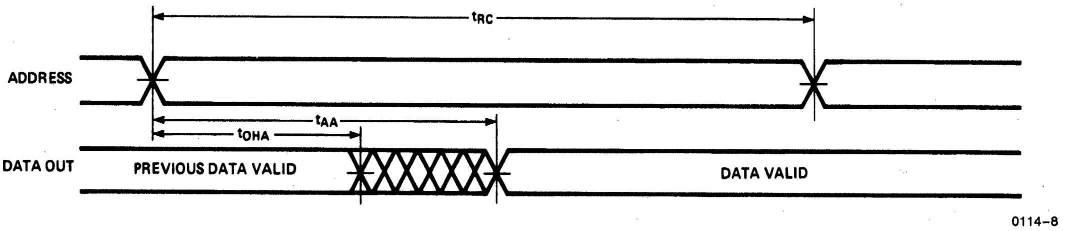
Notes:

7. Data I/O pins enter high impedance state, as shown when $\overline{\text{OE}}$ is held LOW during write.
8. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF in *Figure 2.* Transition is measured ±500 mV from steady state voltage.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are specified and not 100% tested.
11. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. $\overline{\text{WE}}$ is HIGH for read cycle.
13. Device is continuously selected $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{IL}$.
14. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
15. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{\text{BUSY}}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{\text{CE}}$ for Port B is toggled.
    D. $\overline{\text{WE}}$ for Port B is toggled.

Switching Waveforms

Read Cycle No. 1 (Notes 12, 13)

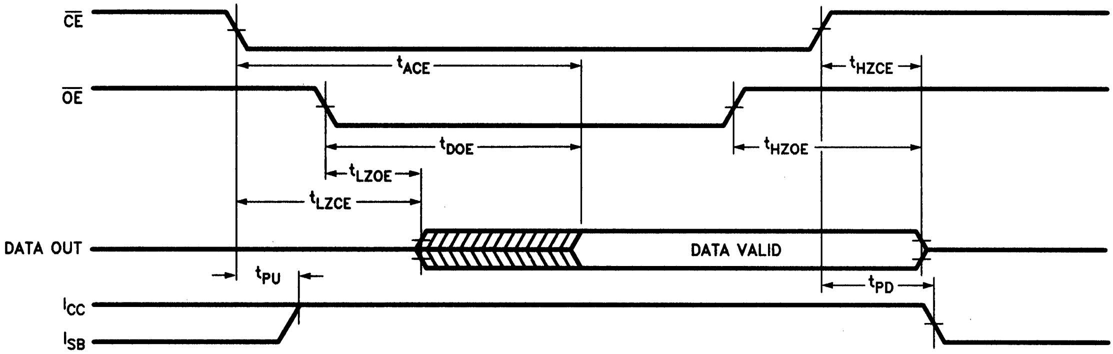
Either Port Address Access



Switching Waveforms (Continued)

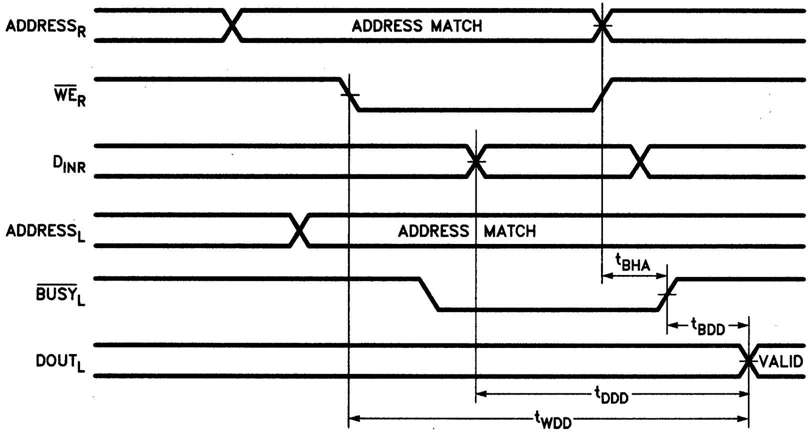
Read Cycle No. 2 (Notes 12, 14)

Either Port $\overline{\text{CE}}$/$\overline{\text{OE}}$ Access


$\overline{\text{CE}}$
$\overline{\text{OE}}$
DATA OUT
I_{CC}
I_{SB}
t_{ACE}
t_{HZCE}
t_{DOE}
t_{HZOE}
t_{LZOE}
t_{LZCE}
DATA VALID
t_{PU}
t_{PD}

0114-9

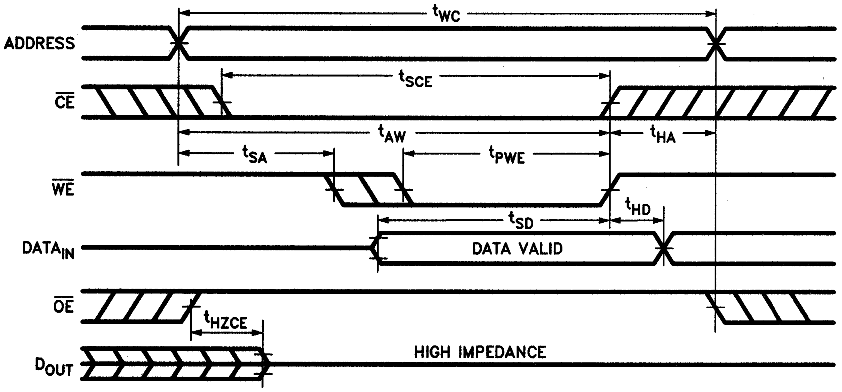
Timing Waveform of Read with $\overline{\text{BUSY}}$ (Note 12)


ADDRESS_R
ADDRESS MATCH
$\overline{\text{WE}}_R$
D_{INR}
ADDRESS_L
ADDRESS MATCH
t_{BHA}
$\overline{\text{BUSY}}_L$
t_{BDD}
DOUT_L
VALID
t_{DDD}
t_{WDD}

0114-10

Write Cycle No. 1 (Notes 7, 11)

Either Port

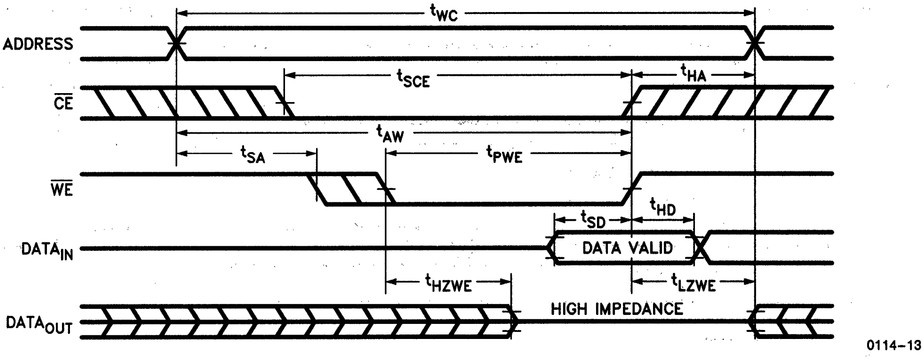

t_{WC}
ADDRESS
t_{SCE}
$\overline{\text{CE}}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{\text{WE}}$
t_{HD}
t_{SD}
DATA_{IN}
DATA VALID
$\overline{\text{OE}}$
t_{HZCE}
D_{OUT}
HIGH IMPEDANCE

0114-12

Switching Waveforms (Continued)

Write Cycle No. 2 (Notes 7, 11)

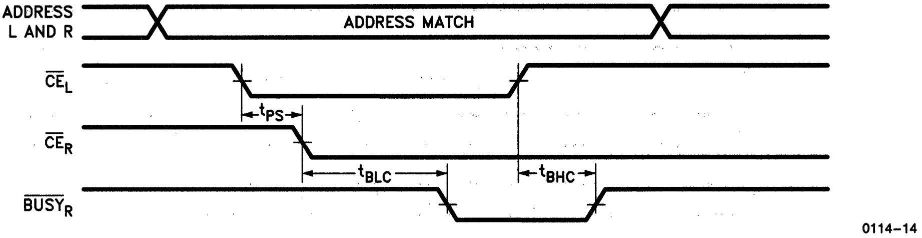
Either Port



t_{WC}
ADDRESS
t_{SCE}
t_{HA}
$\overline{CE}$
t_{AW}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{HD}
t_{SD}
$DATA_{IN}$
DATA VALID
t_{HZWE}
t_{LZWE}
HIGH IMPEDANCE
$DATA_{OUT}$
0114–13

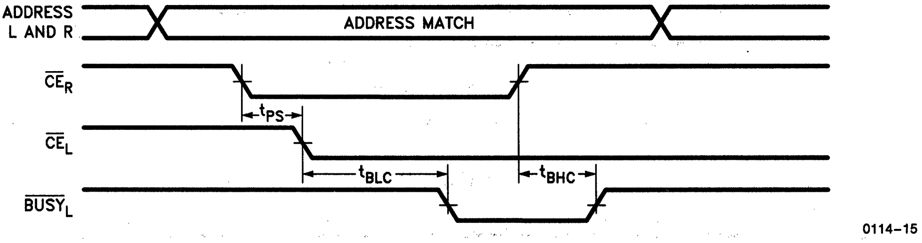
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE_L}$ Valid First:



ADDRESS L AND R
ADDRESS MATCH
$\overline{CE}_L$
t_{PS}
$\overline{CE}_R$
t_{BLC}
t_{BHC}
$\overline{BUSY}_R$
0114–14

$\overline{CE_R}$ Valid First

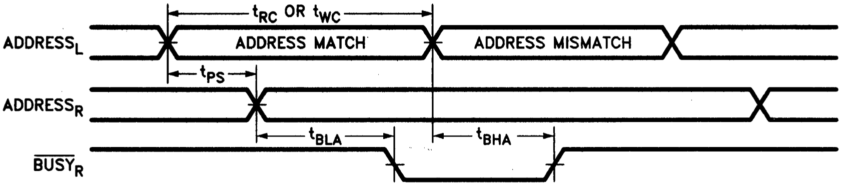


ADDRESS L AND R
ADDRESS MATCH
$\overline{CE}_R$
t_{PS}
$\overline{CE}_L$
t_{BLC}
t_{BHC}
$\overline{BUSY}_L$
0114–15

Switching Waveforms (Continued)

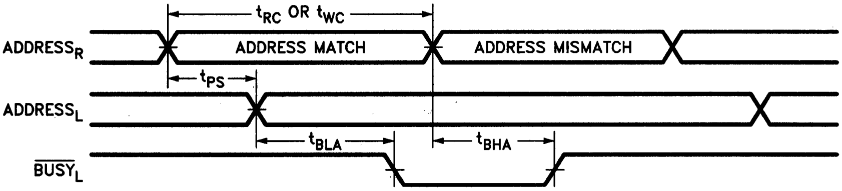
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:


tRC OR tWC
ADDRESSL
ADDRESS MATCH
ADDRESS MISMATCH
tPS
ADDRESSR
tBLA
tBHA
BUSYR

0114–16

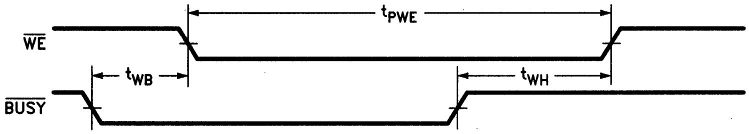
Right Address Valid First:


tRC OR tWC
ADDRESSR
ADDRESS MATCH
ADDRESS MISMATCH
tPS
ADDRESSL
tBLA
tBHA
BUSYL

0114–17

Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (Slave: CY7C140):

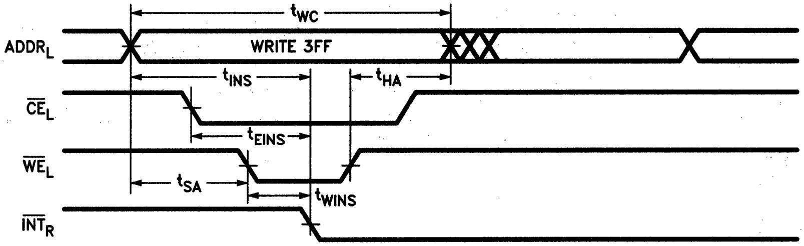

tPWE
WE
tWB
tWH
BUSY

0114–11

Switching Waveforms (Continued)

Interrupt Timing Diagrams

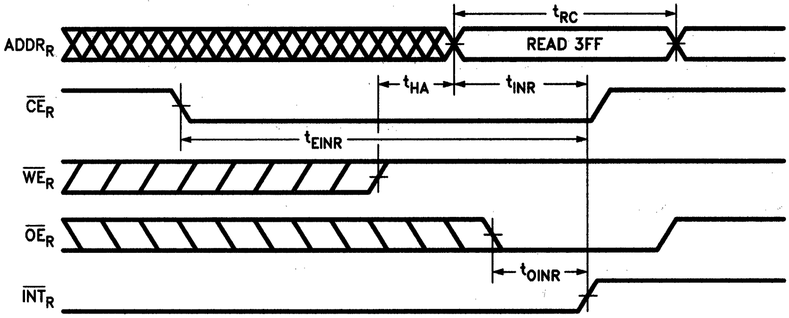
Left Side Sets $\overline{\text{INT}}_R$:



tWC
ADDRL
WRITE 3FF
tINS
tHA
CEL
tEINS
WEL
tSA
tWINS
INTR

0114–18

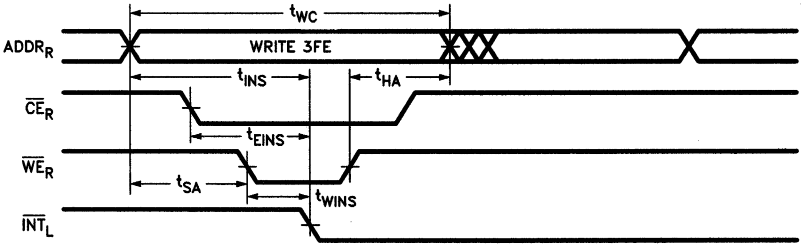
Right Side Clears $\overline{\text{INT}}_R$:



tRC
ADDRR
READ 3FF
tHA
tINR
CER
tEINR
WER
OER
tOINR
INTR

0114–19

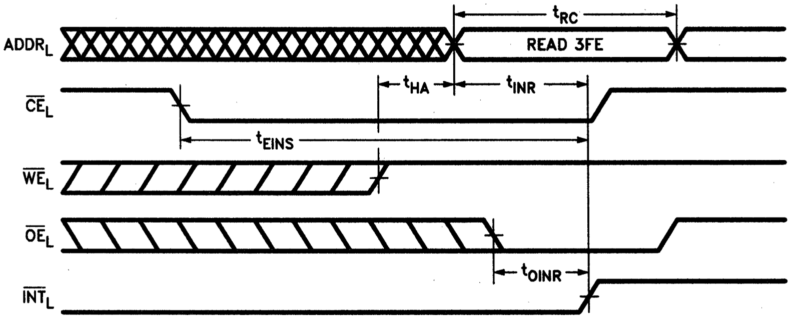
Right Side Sets $\overline{\text{INT}}_L$:



tWC
ADDRR
WRITE 3FE
tINS
tHA
CER
tEINS
WER
tSA
tWINS
INTL

0114–20

Left Side Clears $\overline{\text{INT}}_L$:



tRC
ADDRL
READ 3FE
tHA
tINR
CEL
tEINS
WEL
OEL
tOINR
INTL

0114–21

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C130-35 PC CY7C130-35 DC CY7C130-35 LC	P25 D26 L69	Commercial
45	CY7C130-45 PC CY7C130-45 DC CY7C130-45 LC	P25 D26 L69	Commercial
	CY7C130-45 LMB CY7C130-45 DMB	L69 D26	Military
55	CY7C130-55 PC CY7C130-55 DC CY7C130-55 LC	P25 D26 L69	Commercial
	CY7C130-55 LMB CY7C130-55 DMB	L69 D26	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C140-35 PC CY7C140-35 DC CY7C140-35 LC	P25 D26 L69	Commercial
45	CY7C140-45 PC CY7C140-45 DC CY7C140-45 LC	P25 D26 L69	Commercial
	CY7C140-45 LMB CY7C140-45 DMB	L69 D26	Military
55	CY7C140-55 PC CY7C140-55 DC CY7C140-55 LC	P25 D26 L69	Commercial
	CY7C140-55 LMB CY7C140-55 DMB	L69 D26	Military

CYPRESS
SEMICONDUCTOR

PRELIMINARY **CY7C132**
CY7C142

2048 x 8 Dual Port Static RAM

Features

- **0.8 micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **MASTER CY7C132 easily expands databus width to 16 or more bits using SLAVE CY7C142**
- **$\overline{\text{BUSY}}$ output flag on CY7C132; $\overline{\text{BUSY}}$ input on CY7C142**
- **$\overline{\text{INT}}$ flag for port to port communication (LCC version)**

Functional Description

The CY7C132/CY7C142 are high speed CMOS 2K x 8 Dual Port Static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C132 can be utilized as either a stand-alone 8-Bit Dual Port RAM or as a MASTER Dual Port RAM in conjunction with the CY7C142 SLAVE Dual Port device in systems requiring 16-Bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice or multiprocessor designs.

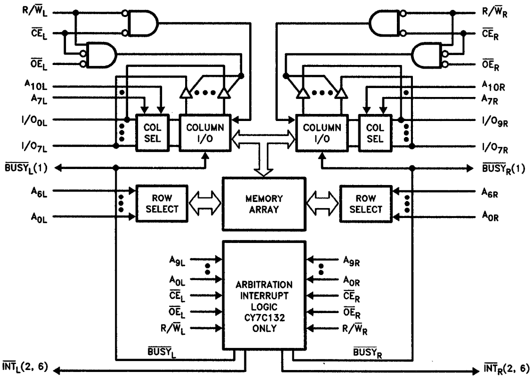
Each port has independent control pins; Chip Enable ($\overline{\text{CE}}$), Write Enable ($\overline{\text{WE}}$), and Output Enable ($\overline{\text{OE}}$). $\overline{\text{BUSY}}$ flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the LCC version. $\overline{\text{BUSY}}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC version, $\overline{\text{INT}}$ is an interrupt flag indicating that data has been placed in a unique location by the other port.

An automatic power-down feature is controlled independently on each port by the Chip Enable ($\overline{\text{CE}}$) pin.

The CY7C132/CY7C142 are available in both 48-pin DIP and 52-pin LCC.

A die coat is used to insure alpha immunity.

Logic Block Diagram



R/$\overline{\text{W}}_L$
$\overline{\text{CE}}_L$
$\overline{\text{OE}}_L$
A_{10L}
A_{7L}
I/O_{0L}
I/O_{7L}
$\overline{\text{BUSY}}_L$(1)
A_{6L}
A_{0L}
COL SEL
COLUMN I/O
ROW SELECT
MEMORY ARRAY
COLUMN I/O
COL SEL
ROW SELECT
R/$\overline{\text{W}}_R$
$\overline{\text{CE}}_R$
$\overline{\text{OE}}_R$
A_{10R}
A_{7R}
I/O_{9R}
I/O_{7R}
$\overline{\text{BUSY}}_R$(1)
A_{6R}
A_{0R}
A_{9L}
A_{0L}
$\overline{\text{CE}}_L$
$\overline{\text{OE}}_L$
R/$\overline{\text{W}}_L$
ARBITRATION INTERRUPT LOGIC CY7C132 ONLY
A_{9R}
A_{0R}
$\overline{\text{CE}}_R$
$\overline{\text{OE}}_R$
R/$\overline{\text{W}}_R$
$\overline{\text{BUSY}}_L$
$\overline{\text{BUSY}}_R$
$\overline{\text{INT}}_L$(2, 6)
$\overline{\text{INT}}_R$(2, 6)

0106-1

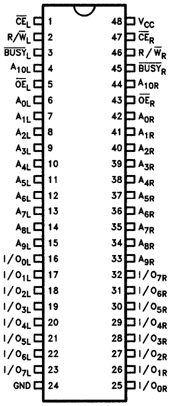
Notes:

1. CY7C132 (MASTER): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor. CY7C142 (SLAVE): $\overline{\text{BUSY}}$ is input.
2. Open drain outputs: pullup resistor required.

Selection Guide

		7C132-35 7C142-35	7C132-45 7C142-45	7C132-55 7C142-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		150	150
Maximum Standby Current (mA)	Commercial	30	30	30
	Military		40	40

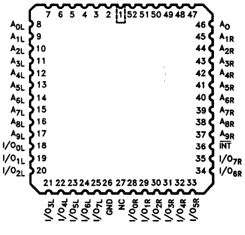
Pin Configurations



$\overline{\text{CE}}_L$ 1
R/$\overline{\text{W}}_L$ 2
$\overline{\text{BUSY}}_L$ 3
A_{10L} 4
$\overline{\text{OE}}_L$ 5
A_{0L} 6
A_{1L} 7
A_{2L} 8
A_{3L} 9
A_{4L} 10
A_{5L} 11
A_{6L} 12
A_{7L} 13
A_{8L} 14
A_{9L} 15
I/O_{0L} 16
I/O_{1L} 17
I/O_{2L} 18
I/O_{3L} 19
I/O_{4L} 20
I/O_{5L} 21
I/O_{6L} 22
I/O_{7L} 23
GND 24
48 V_{CC}
47 $\overline{\text{CE}}_R$
46 R/$\overline{\text{W}}_R$
45 $\overline{\text{BUSY}}_R$
44 A_{10R}
43 $\overline{\text{OE}}_R$
42 A_{0R}
41 A_{1R}
40 A_{2R}
39 A_{3R}
38 A_{4R}
37 A_{5R}
36 A_{6R}
35 A_{7R}
34 A_{8R}
33 A_{9R}
32 I/O_{7R}
31 I/O_{6R}
30 I/O_{5R}
29 I/O_{4R}
28 I/O_{3R}
27 I/O_{2R}
26 I/O_{1R}
25 I/O_{0R}

DIP
Top View

0106-2



$\overline{\text{OE}}_L$ 7
A_{10L} 6
$\overline{\text{INT}}_L$ 5
$\overline{\text{BUSY}}_L$ 4
R/$\overline{\text{W}}_L$ 3
$\overline{\text{CE}}_L$ 2
NC 1
V_{CC} 52
$\overline{\text{CE}}_R$ 51
R/$\overline{\text{W}}_R$ 50
$\overline{\text{BUSY}}_R$ 49
A_{10R} 48
$\overline{\text{OE}}_R$ 47
A_{0L} 8
A_{1L} 9
A_{2L} 10
A_{3L} 11
A_{4L} 12
A_{5L} 13
A_{6L} 14
A_{7L} 15
A_{8L} 16
A_{9L} 17
I/O_{0L} 18
I/O_{1L} 19
I/O_{2L} 20
46 A_0
45 A_{1R}
44 A_{2R}
43 A_{3R}
42 A_{4R}
41 A_{5R}
40 A_{6R}
39 A_{7R}
38 A_{8R}
37 A_{9R}
36 $\overline{\text{INT}}$
35 I/O_{7R}
34 I/O_{6R}
21 I/O_{3L}
22 I/O_{4L}
23 I/O_{5L}
24 I/O_{6L}
25 I/O_{7L}
26 GND
27 NC
28 I/O_{0R}
29 I/O_{1R}
30 I/O_{2R}
31 I/O_{3R}
32 I/O_{4R}
33 I/O_{5R}

LCC
Top View

0106-3

Maximum Ratings

(Above which the useful life may be inpaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 48 to Pin 24).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.5V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015.2)

Latch-up Current............................ >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C132-35 7C142-35		7C132-45 7C142-45		7C132-55 7C142-55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 6.0 mA			0.4		0.4		0.4	V
		I_{OL} = 8.0 mA			0.5		0.5		0.5	
		I_{OL} = 16.0 mA (Note 7)			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short [3] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120		120		120	mA
			Military*				150		150	
I_{SB}	Automatic $\overline{CE}$ [4] Power Down Current									
I_{SB1}	Both Ports, TTL Inputs		Commercial		30		30		30	mA
I_{SB2}	One Port, TTL Input				75		75		75	mA
I_{SB3}	Both Ports, CMOS Inputs				15		15		15	mA
I_{SB4}	One Port, CMOS Inputs				65		65		65	mA
I_{SB1}	Both Ports, TTL Inputs		Military*				40		40	mA
I_{SB2}	One Port, TTL Input						100		100	mA
I_{SB3}	Both Ports, CMOS Inputs						30		30	mA
I_{SB4}	One Port, CMOS Inputs						80		80	mA

* -45 and -55 Only

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	

Notes:

3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested on a sample basis.
6. LCC version only.
7. $\overline{BUSY}$ and $\overline{INT}$ pins only.

AC Test Loads and Waveforms

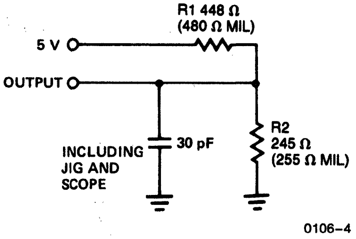

R1 448 Ω
(480 Ω MIL)
5 V
OUTPUT
INCLUDING JIG AND SCOPE
30 pF
R2
245 Ω
(255 Ω MIL)
0106-4

Figure 1

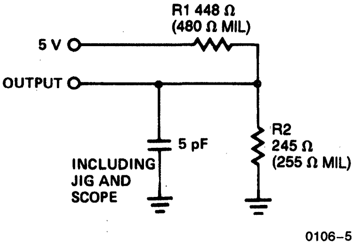

R1 448 Ω
(480 Ω MIL)
5 V
OUTPUT
INCLUDING JIG AND SCOPE
5 pF
R2
245 Ω
(255 Ω MIL)
0106-5

Figure 2

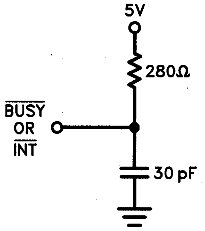
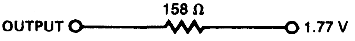

5V
280Ω
BUSY OR INT
30 pF
0106-6

Figure 3. $\overline{\text{BUSY}}$ Output Load (CY7C132 Only)

Equivalent to: THÉVENIN EQUIVALENT


158 Ω
OUTPUT
1.77 V
0106-8

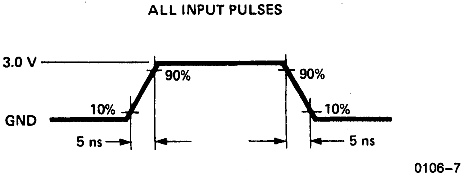

ALL INPUT PULSES
3.0 V
GND
90%
90%
10%
10%
5 ns
5 ns
0106-7

Figure 4

Switching Characteristics Over Operating Range [9]

Parameters	Description	7C132-35 7C142-35		7C132-45 7C142-45		7C132-55 7C142-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[10]		15		20		25	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[11]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[10, 11]		15		20		25	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[12]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	30		35		40		ns
t_{AW}	Address Set-Up to Write End	30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z		15		20		25	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		ns

Switching Characteristics Over Operating Range [9] (Continued)

Parameters	Description	7C132-35 7C142-35		7C132-45 7C142-45		7C132-55 7C142-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{WC}	Write Cycle Time	35		45		55		ns
t_{BLA}	$\overline{\text{BUSY}}$ LOW from Address Match		20		25		30	ns
t_{BHA}	$\overline{\text{BUSY}}$ HIGH from Address Mismatch		20		25		30	ns
t_{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW		20		25		30	ns
t_{BHC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH		20		25		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		ns
t_{WINS}	$\overline{\text{WE}}$ to $\overline{\text{INTERRUPT}}$ Set Time		15		20		25	ns
t_{EINS}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Set Time		25		35		45	ns
t_{INS}	Add to $\overline{\text{INTERRUPT}}$ Set Time		25		35		45	ns
t_{OINR}	$\overline{\text{OE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time		15		20		25	ns
t_{EINR}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time		25		35		45	ns
t_{INR}	Add to $\overline{\text{INTERRUPT}}$ Reset Time		25		35		45	ns
BUSY TIMING								
t_{WB}*	$\overline{\text{WE}}$ LOW after $\overline{\text{BUSY}}$	0		0		0		ns
t_{WH}	$\overline{\text{WE}}$ HIGH After $\overline{\text{BUSY}}$	15		15		15		ns
t_{BDD}	$\overline{\text{BUSY}}$ HIGH to Valid Data		20		25		30	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 16		Note 16		Note 16	ns
t_{WDD}	Write Pulse to Data Delay		Note 16		Note 16		Note 16	

*CY7C142 Only

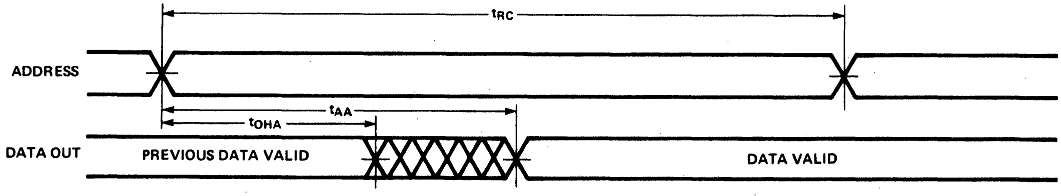
Notes:

8. Data I/O pins enter high-impedance state, as shown, when $\overline{\text{OE}}$ is held LOW during write.
9. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
10. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 2*. Transition is measured ± 500 mV from steady state voltage.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
12. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. $\overline{\text{WE}}$ is HIGH for read cycle.
14. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{IL}$.
15. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
16. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    - A. $\overline{\text{BUSY}}$ on Port B goes HIGH.
    - B. Port B's address toggled.
    - C. $\overline{\text{CE}}$ for Port B is toggled.
    - D. $\overline{\text{WE}}$ for Port B is toggled.

Switching Waveforms

Read Cycle No. 1 (Notes 13, 14)

Either Port—Address Access

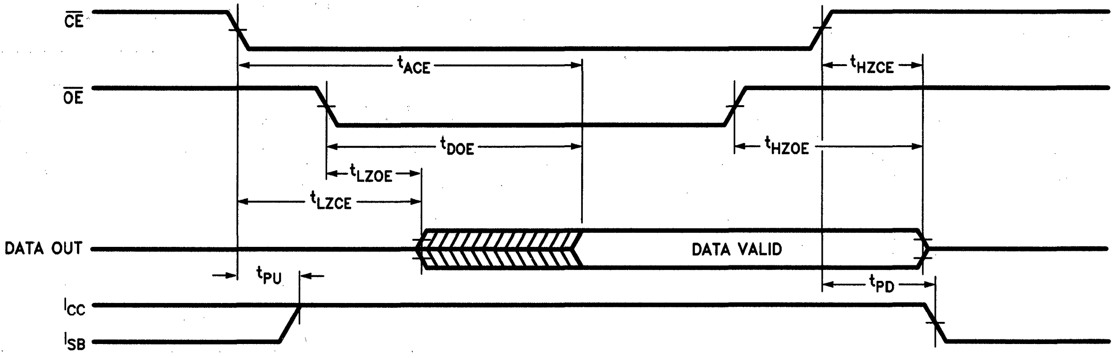


0106-9

Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 13, 15)

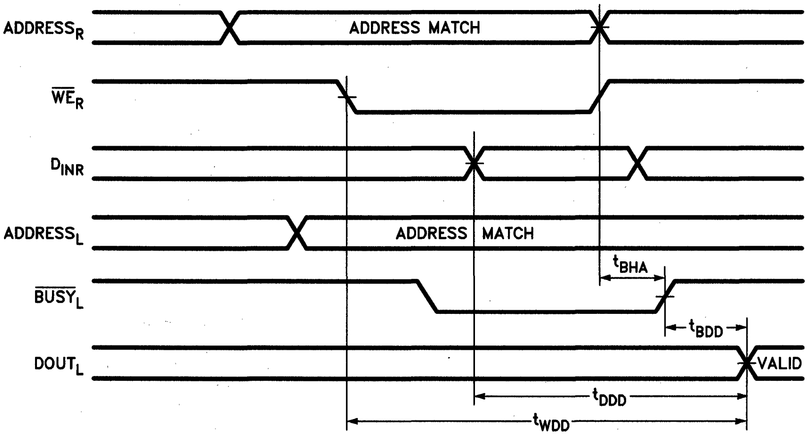
Either Port—$\overline{\text{CE}}/\overline{\text{OE}}$ Access


$\overline{\text{CE}}$
t_{ACE}
t_{HZCE}
$\overline{\text{OE}}$
t_{DOE}
t_{HZOE}
t_{LZOE}
t_{LZCE}
DATA OUT
DATA VALID
t_{PU}
t_{PD}
I_{CC}
I_{SB}

0106–10

Read Cycle No. 3 (Note 13)

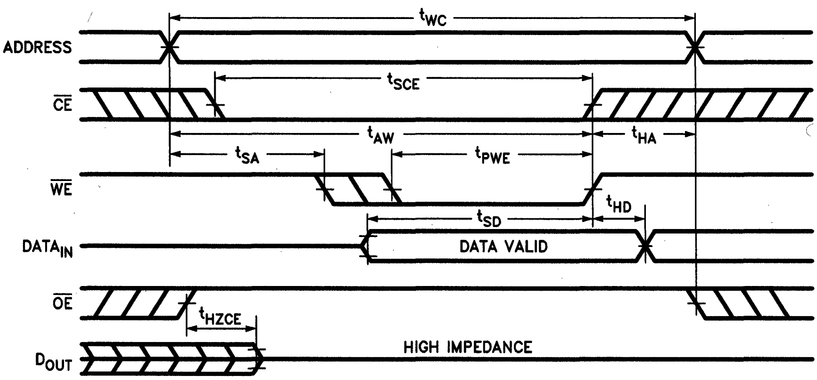
READ with $\overline{\text{BUSY}}$


ADDRESS_R
ADDRESS MATCH
$\overline{\text{WE}}_R$
D_{INR}
ADDRESS_L
ADDRESS MATCH
t_{BHA}
$\overline{\text{BUSY}}_L$
t_{BDD}
DOUT_L
VALID
t_{DDD}
t_{WDD}

0106–11

Write Cycle No. 1 (Notes 8, 12)

Either Port

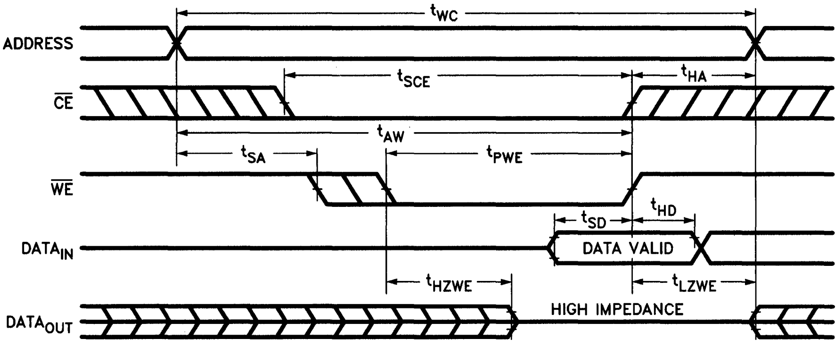

t_{WC}
ADDRESS
t_{SCE}
$\overline{\text{CE}}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{\text{WE}}$
t_{HD}
t_{SD}
DATA_{IN}
DATA VALID
$\overline{\text{OE}}$
t_{HZCE}
D_{OUT}
HIGH IMPEDANCE

0106–13

Switching Waveforms (Continued)

Write Cycle No. 2 (Notes 8, 12)

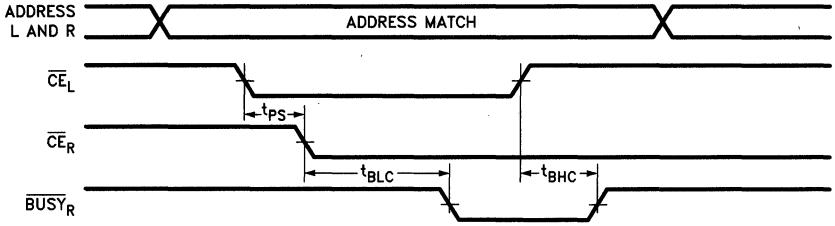
Either Port


ADDRESS
CE
WE
DATA_IN
DATA_OUT
t_WC
t_SCE
t_HA
t_AW
t_SA
t_PWE
t_SD
t_HD
DATA VALID
t_HZWE
t_LZWE
HIGH IMPEDANCE

0106-14

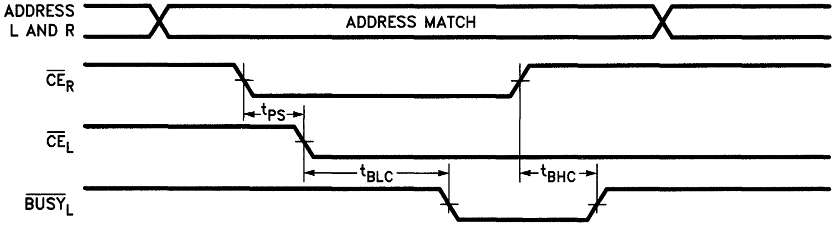
BUSY Timing Diagram No. 1 (CE Arbitration)

CE_L Valid First:


ADDRESS L AND R
ADDRESS MATCH
CE_L
t_PS
CE_R
t_BLC
t_BHC
BUSY_R

0106-15

CE_R Valid First:

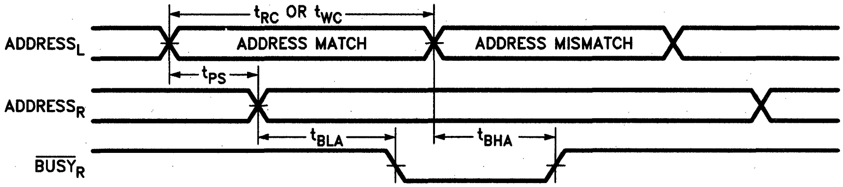

ADDRESS L AND R
ADDRESS MATCH
CE_R
t_PS
CE_L
t_BLC
t_BHC
BUSY_L

0106-16

Switching Waveforms (Continued)

BUSY Timing Diagram No. 2 (Address Arbitration)

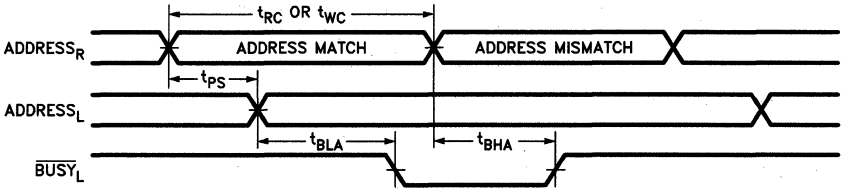
LEFT Address Valid First:


t_{RC} OR t_{WC}
ADDRESS$_L$
ADDRESS MATCH
ADDRESS MISMATCH
t_{PS}
ADDRESS$_R$
t_{BLA}
t_{BHA}
$\overline{BUSY}_R$

0106-17

BUSY Timing Diagram No. 2

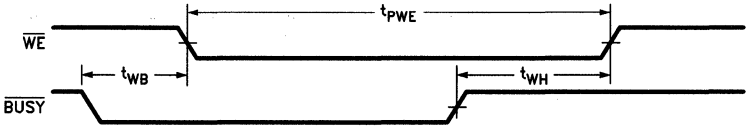
RIGHT Address Valid First:


t_{RC} OR t_{WC}
ADDRESS$_R$
ADDRESS MATCH
ADDRESS MISMATCH
t_{PS}
ADDRESS$_L$
t_{BLA}
t_{BHA}
$\overline{BUSY}_L$

0106-18

BUSY Timing Diagram No. 3

WRITE with $\overline{BUSY}$ (SLAVE: CY7C142)

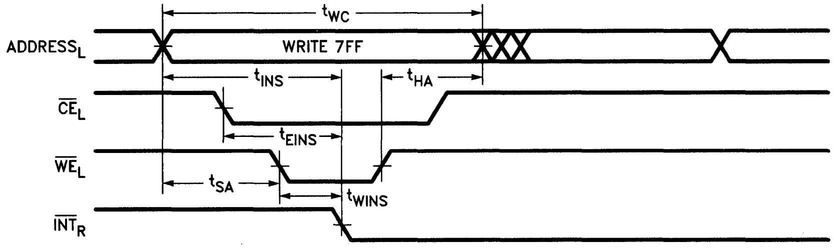

t_{PWE}
$\overline{WE}$
t_{WB}
t_{WH}
$\overline{BUSY}$

0106-12

Switching Waveforms (Continued)

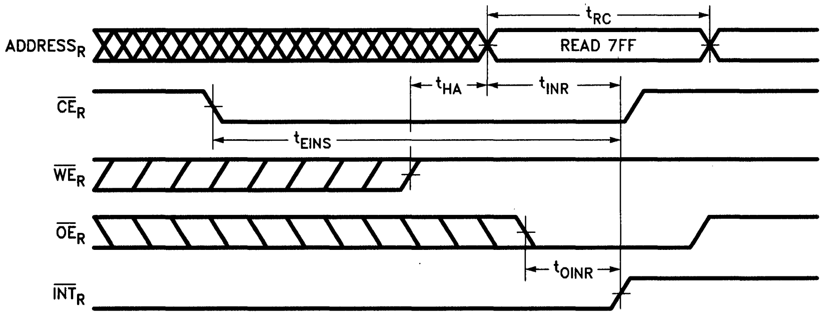
Interrupt Timing Diagram (Note 6)

LEFT Side Sets $\overline{\text{INT}}_R$:


tWC
ADDRESSL
WRITE 7FF
tINS
tHA
CEL
tEINS
WEL
tSA
tWINS
INTR

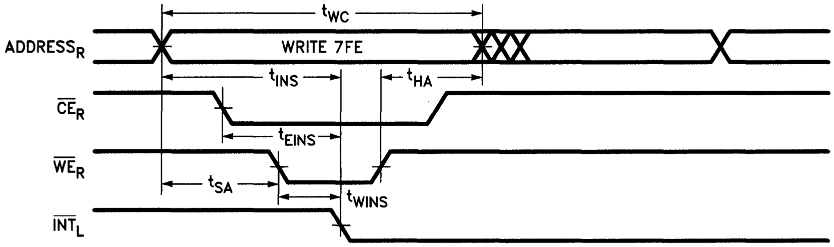
0106-19

RIGHT Side Clears $\overline{\text{INT}}_R$:


tRC
ADDRESSR
READ 7FF
tHA
tINR
CER
tEINS
WER
OER
tOINR
INTR

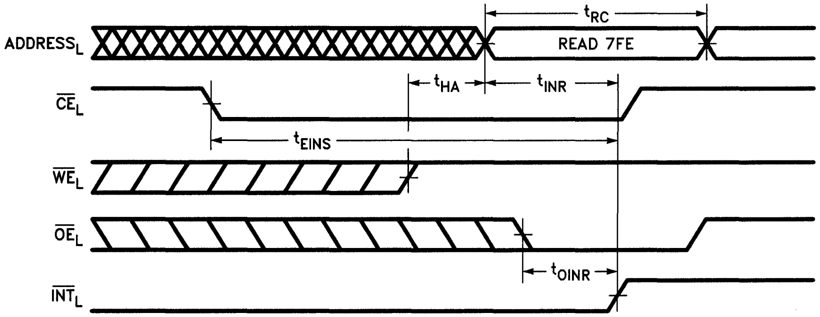
0106-20

RIGHT Side Sets $\overline{\text{INT}}_L$:


tWC
ADDRESSR
WRITE 7FE
tINS
tHA
CER
tEINS
WER
tSA
tWINS
INTL

0106-21

LEFT Side Clears $\overline{\text{INT}}_L$:


tRC
ADDRESSL
READ 7FE
tHA
tINR
CEL
tEINS
WEL
OEL
tOINR
INTL

0106-22

Ordering Information

Speed (ms)	Ordering Code	Package Type	Operating Range
35	CY7C132-35PC	P25	Commercial
	CY7C132-35DC	D26	
	CY7C132-35LC	L69	
45	CY7C132-45PC	P25	Commercial
	CY7C132-45DC	D26	
	CY7C132-45LC	L69	
	CY7C132-45LMB	L69	Military
	CY7C132-45DMB	D26	
55	CY7C132-55PC	P25	Commercial
	CY7C132-55DC	D26	
	CY7C132-55LC	L69	
	CY7C132-55LMB	L69	Military
	CY7C132-55DMB	D26	

Speed (ms)	Ordering Code	Package Type	Operating Range
35	CY7C142-35PC	P25	Commercial
	CY7C142-35DC	D26	
	CY7C142-35LC	L69	
45	CY7C142-45PC	P25	Commercial
	CY7C142-45DC	D26	
	CY7C142-45LC	L69	
	CY7C142-45LMB	L6	Military
	CY7C142-45DMB	D26	
55	CY7C142-55PC	P25	Commercial
	CY7C142-55DC	D26	
	CY7C142-55LC	L69	
	CY7C142-55LMB	L69	Military
	CY7C142-55DMB	D26	

CYPRESS
SEMICONDUCTOR

CY7C147

4096 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power**
  - **— 55 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

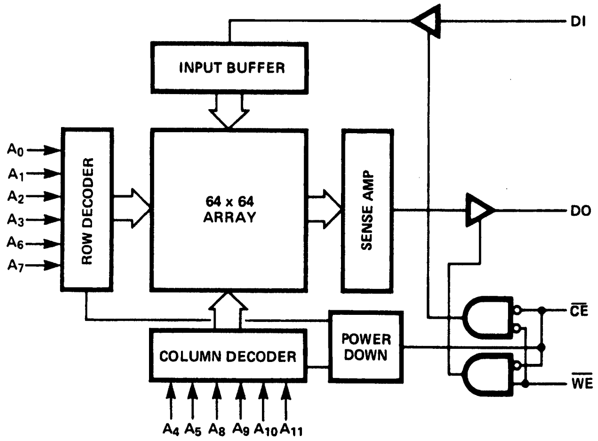
The CY7C147 is a high performance CMOS static RAM organized as 4096 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

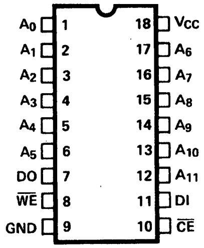
The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram

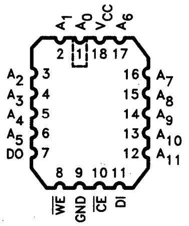

DI
INPUT BUFFER
A0
A1
A2
A3
A6
A7
ROW DECODER
64 x 64 ARRAY
SENSE AMP
DO
CE
WE
COLUMN DECODER
POWER DOWN
A4 A5 A8 A9 A10 A11

0019-1

Pin Configurations


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DO 7
WE 8
GND 9
10 CE
11 DI
12 A11
13 A10
14 A9
15 A8
16 A7
17 A6
18 Vcc

0019-2


A1 A0 VCC A6
2 1 18 17
A2 3
A3 4
A4 5
A5 6
DO 7
16 A7
15 A8
14 A9
13 A10
12 A11
8 9 10 11
WE GND CE DI

0019-3

Selection Guide

		7C147-25	7C147-35	7C147-45
Maximum Access Time (ns)	Commercial	25	35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial	90	80	80
	Military		110	110
Maximum Standby Current (mA)	Commercial	15	10	10
	Military		10	10

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C147-25		7C147-35, 45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	−50	+50	μA
I_{OS}	Output Short[1] Circuit Current	V_{CC} = Max.	V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90		80	mA
			Military				110	
I_{SB_1}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		15		10	mA
			Military				10	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	

Notes:

1. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

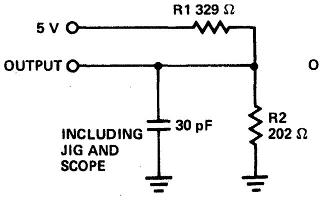


Figure 1a

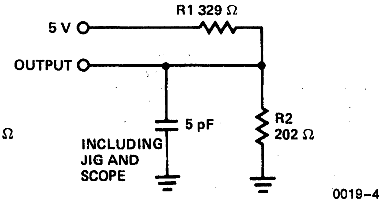


Figure 1b

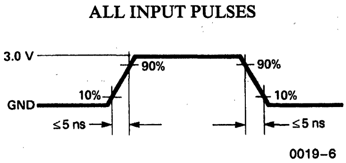
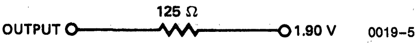


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

Parameters	Description	7C147-25		7C147-35		7C147-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACE}	$\overline{CS}$ Low to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{CE}$HIGH to High Z[5, 6]		20		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		35		45		ns
t_{AW}	Address Set-up to Write End	25		35		45		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		10		10		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		15		20		25	ns

Notes:

[4] Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.

[5] t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.

[6] At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.

[7] The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

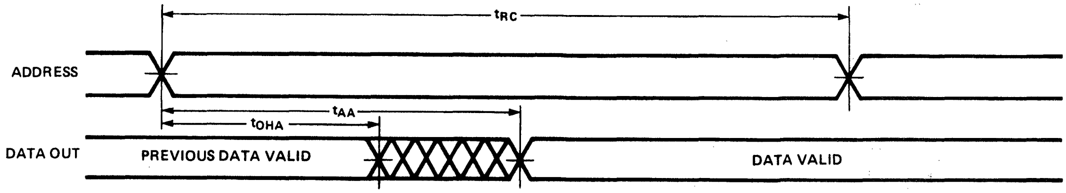
[8] $\overline{WE}$ is HIGH for read cycle.

[9] Device is continuously selected, $\overline{CE} = V_{IL}$.

[10] Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

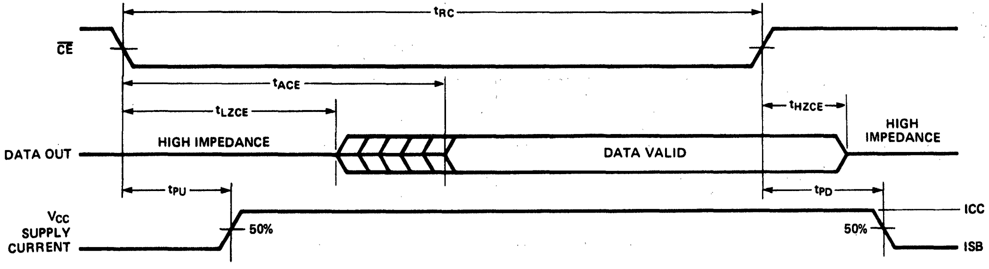
Read Cycle No. 1 (Notes 8, 9)



0019-7

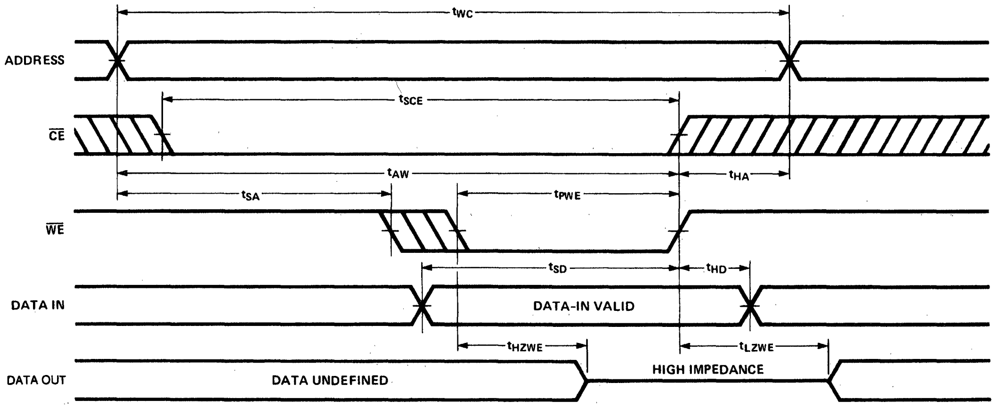
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


tRC
CE
tACE
tLZCE
tHZCE
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
DATA OUT
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

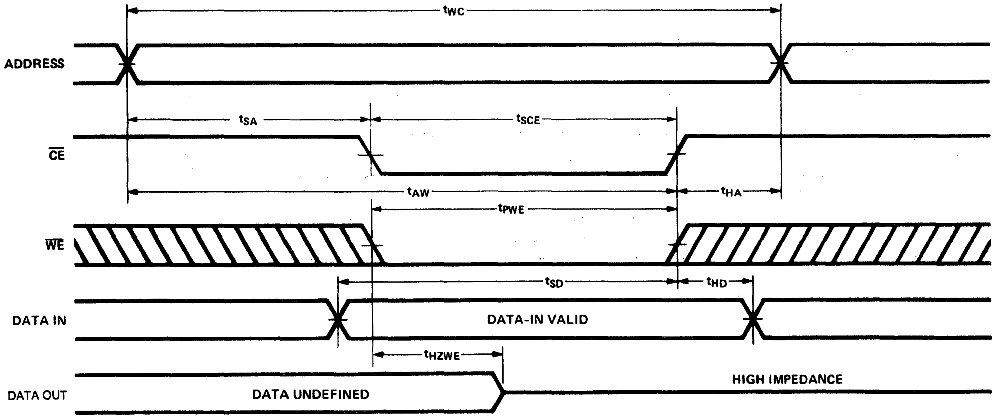
0019-8

Write Cycle No. 1 (WE Controlled) (Note 7)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

0019-9

Write Cycle No. 2 (CE Controlled) (Note 7)

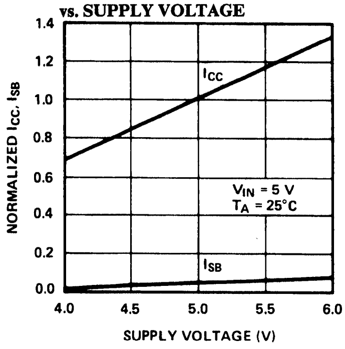

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

0019-10

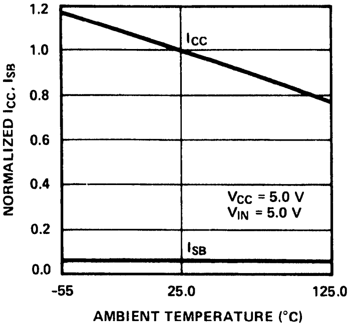
Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

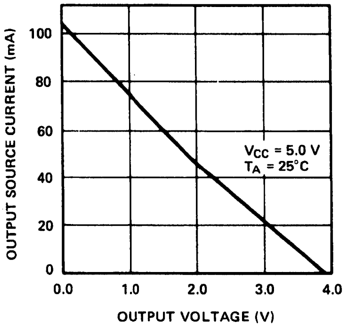
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



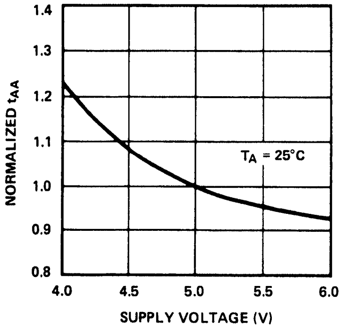
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



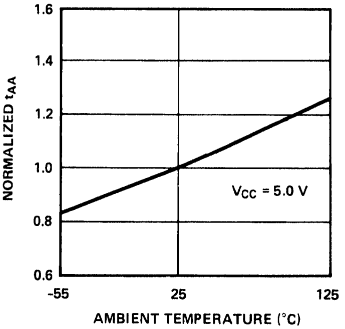
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



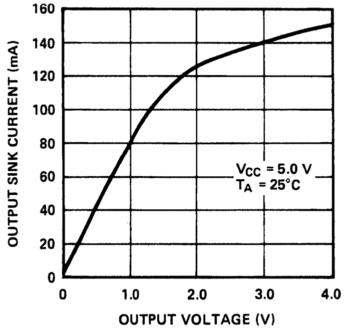
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



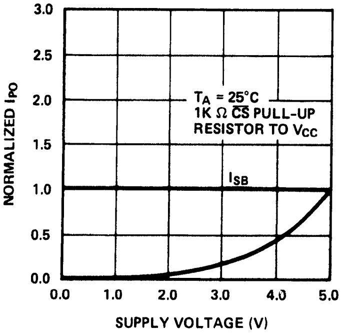
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



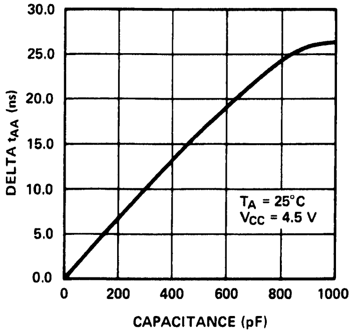
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



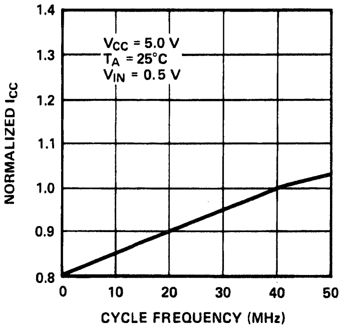
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0019-11

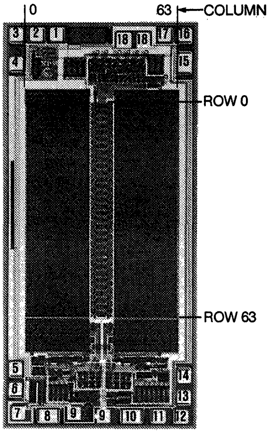
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C147-25PC	P3	Commercial
	CY7C147-25DC	D4	Commercial
	CY7C147-25LC	L50	Commercial
35	CY7C147-35PC	P3	Commercial
	CY7C147-35DC	D4	Commercial
	CY7C147-35LC	L50	Commercial
	CY7C147-35DMB	D4	Military
	CY7C147-35LMB	L50	Military
45	CY7C147-45PC	P3	Commercial
	CY7C147-45DC	D4	Commercial
	CY7C147-45LC	L50	Commercial
	CY7C147-45DMB	D4	Military
	CY7C147-45LMB	L50	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	1
A_1	X_1	2
A_2	X_2	3
A_3	X_3	4
A_4	Y_0	5
A_5	Y_1	6
A_6	X_4	17
A_7	X_5	16
A_8	Y_2	15
A_9	Y_3	14
A_{10}	Y_4	13
A_{11}	Y_5	12

Bit Map



0019–12

CYPRESS
SEMICONDUCTOR

CY7C148
CY7C149

1024 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25 ns access time**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power (7C148)**
  - **— 82.5 mW (25 ns version)**
  - **— 55 mW (all others)**
- **5 volt power supply ±10% tolerance both commercial and military**
- **TTL compatible inputs and outputs**

Functional Description

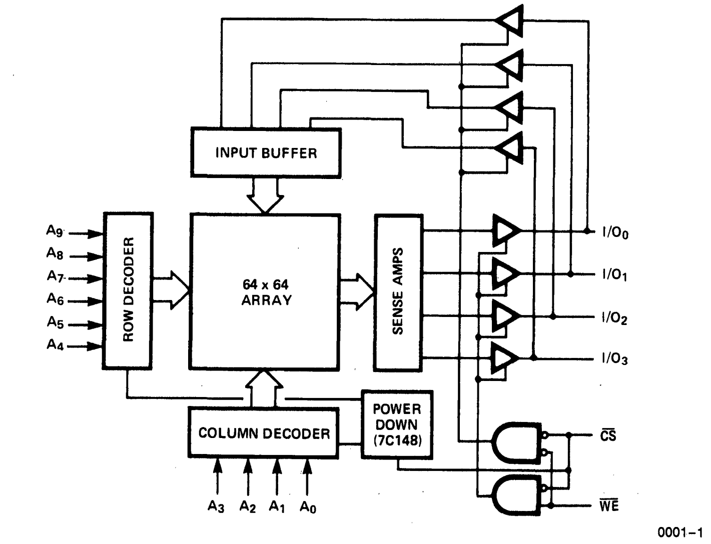
The CY7C148 and CY7C149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input, and three-state outputs. The CY7C148 and CY7C149 are identical except that the CY7C148 includes an automatic ($\overline{CS}$) power-down feature. The CY7C148 remains in a low power mode as long as the device remains unselected, i.e. ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O$_0$ through I/O$_3$) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

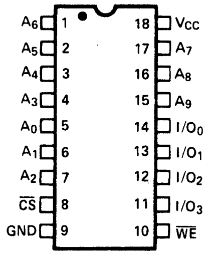
Reading the device is accomplished by selecting the device, ($\overline{CS}$) active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O$_0$ through I/O$_3$).

The input/output pins (I/O$_0$ through I/O$_3$) remain in a high impedance state unless the chip is selected, and write enable ($\overline{WE}$) is high.

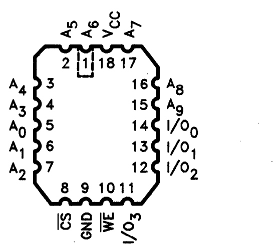
Logic Block Diagram


INPUT BUFFER
ROW DECODER
64 x 64 ARRAY
SENSE AMPS
COLUMN DECODER
POWER DOWN (7C148)
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
I/O0
I/O1
I/O2
I/O3
CS
WE
0001-1

Pin Configurations


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 Vcc
17 A7
16 A8
15 A9
14 I/O0
13 I/O1
12 I/O2
11 I/O3
10 WE

0001-2


A5
A6
VCC
A7
2 1 18 17
A4 3
A3 4
A0 5
A1 6
A2 7
16 A8
15 A9
14 I/O0
13 I/O1
12 I/O2
8 9 10 11
CS
GND
WE
I/O3

0001-3

Selection Guide

		7C148-25	7C148-35	7C148-45	7C149-25	7C149-35	7C149-45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage (Per MIL-STD-883 Method 3015.2) .... >2001V

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C148/9-25		7C148/9-35, 45		Units
				Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	$V_{OH} = 2.4V$	$V_{CC} = 4.5V$	−4		−4		mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		8		8		mA
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled		−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz $T_A = 25°C$, All Pins at 0V, $V_{CC} = 5V$			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ Output Open	Commercial		90		80	mA
			Military				110	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, $\overline{CS} \geq V_{IH}$ 7C148 only	Commercial		15		10	mA
			Military				10	
I_{PO}	Peak Power-On Current	Max. V_{CC}, $\overline{CS} \geq V_{IH}$[3] 7C148 only	Commercial		15		10	mA
			Military				10	
I_{OS}	Output Short Circuit Current	$GND \leq V_O \leq V_{CC}$[10]	Commercial		±275		±275	mA
			Military				±350	

Notes:

1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise current will exceed values given (CY7C148 only).
4. Chip deselected greater than 25 ns prior to selection.
5. Chip deselected less than 25 ns prior to selection.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in *Figure 1b*. These parameters are sampled and not 100% tested.
7. $\overline{WE}$ is high for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CS}$ transition low.
10. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms

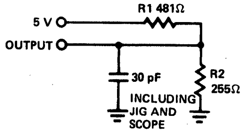


Figure 1a

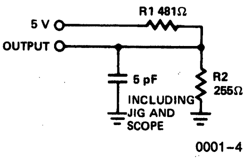
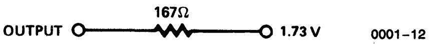


Figure 1b

Equivalent To:

THÉVENIN EQUIVALENT



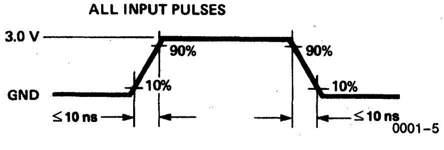


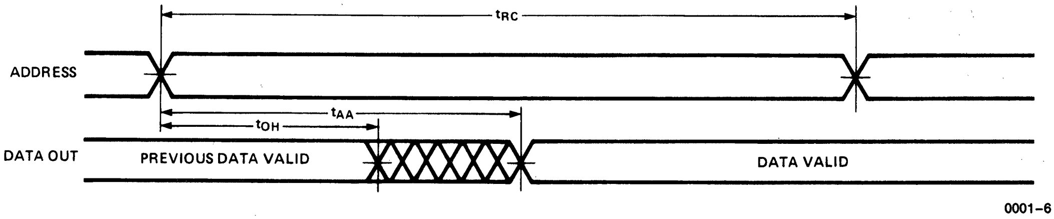
Figure 2

Switching Characteristics Over Operating Range (Note 1)

Parameters	Description		7C148/9-25		7C148/9-35		7C148/9-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1}	Chip Select Low to Data Out Valid (CY7C148 only)			25[4]		35		45	ns
t_{ACS2}				30[5]		35		45	
t_{ACS}	Chip Select Low to Data Out Valid (CY7C149 only)			15		15		20	ns
t_{LZ}[6]	Chip Select Low to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[6]	Chip Select High to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select High to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select Low to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[2]	Write Enable Low to Write Enable High		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[6]	Write Enable to Output in High Z		0	8	0	10	0	15	ns
t_{DW}	Data in Valid to Write Enable High		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable Low		0		0		0		ns
t_{CW}[2]	Chip Select Low to Write Enable High		20		30		40		ns
t_{OW}[6]	Write Enable High to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

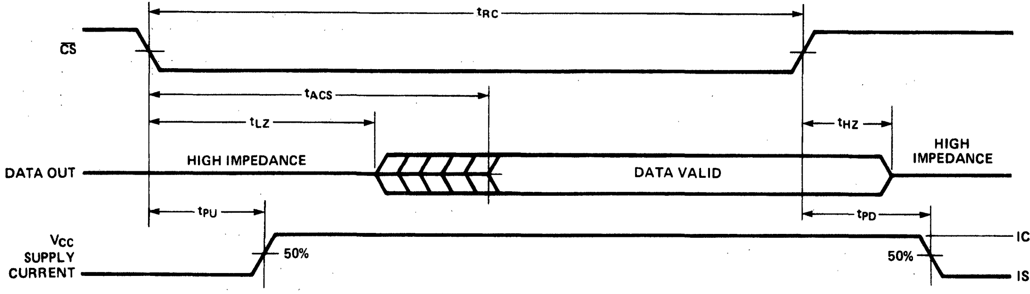
Switching Waveforms

Read Cycle No. 1 (Notes 7, 8)



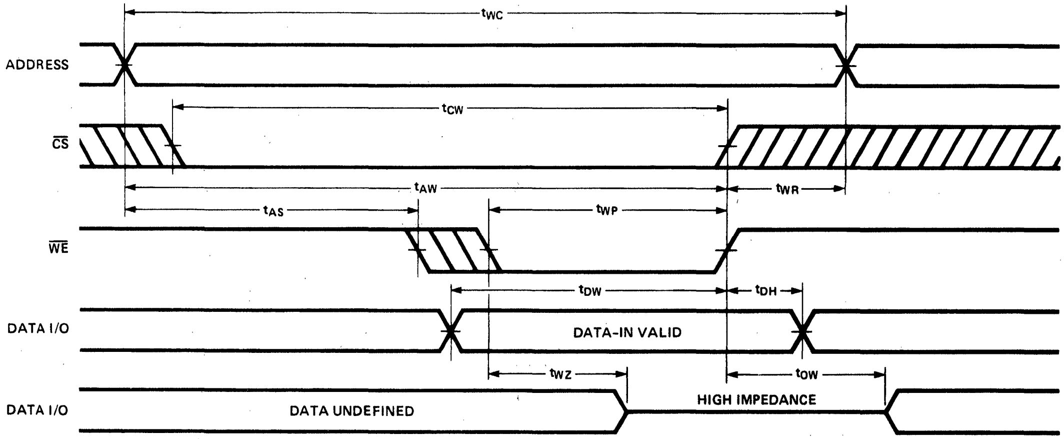
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 7, 9)


tRC
CS
tACS
tLZ
tHZ
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
tPU
tPD
Vcc SUPPLY CURRENT
50%
50%
ICC
ISB

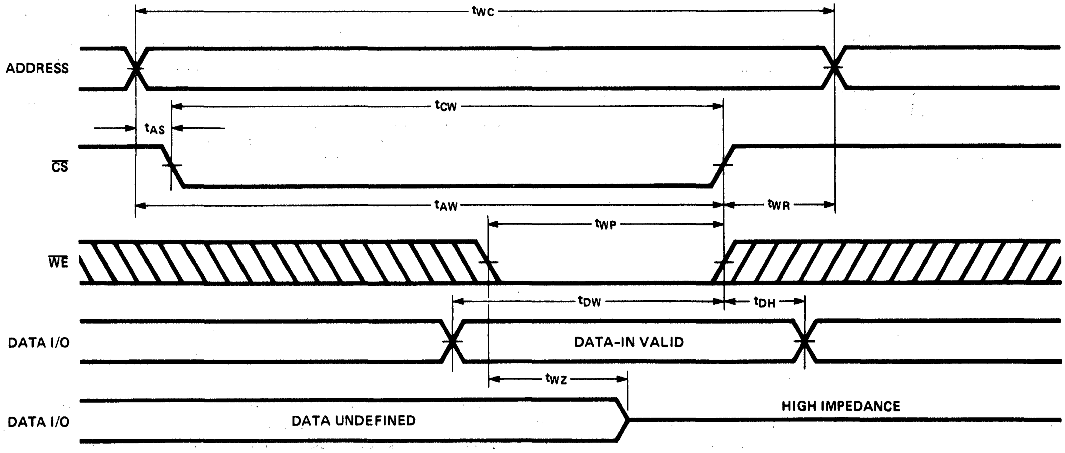
0001-7

Write Cycle No. 1 (WE Controlled)


tWC
ADDRESS
tCW
CS
tAW
tWR
tAS
tWP
WE
tDW
tDH
DATA I/O
DATA-IN VALID
tWZ
tOW
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0001-8

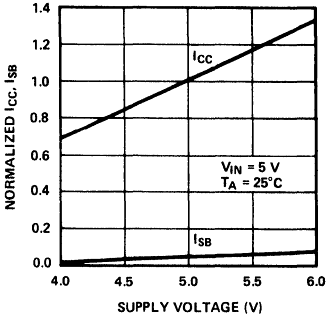
Write Cycle No. 2 (CS Controlled)

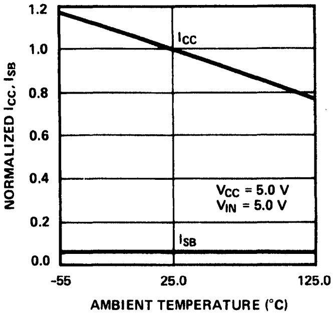

tWC
ADDRESS
tCW
tAS
CS
tAW
tWR
tWP
WE
tDW
tDH
DATA I/O
DATA-IN VALID
tWZ
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

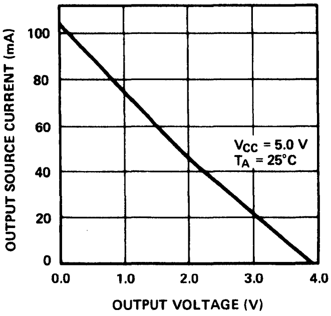
0001-9

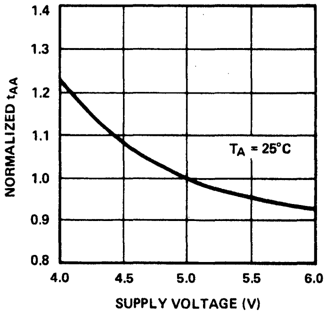
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

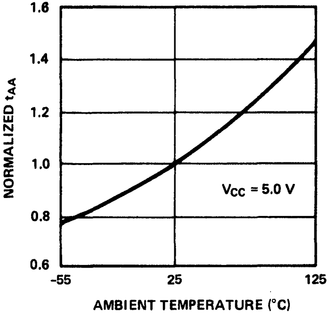
Typical DC and AC Characteristics

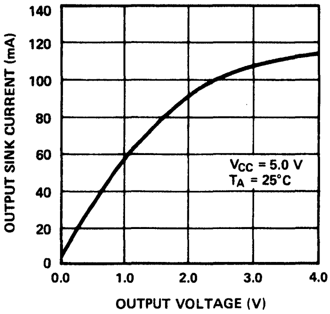

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

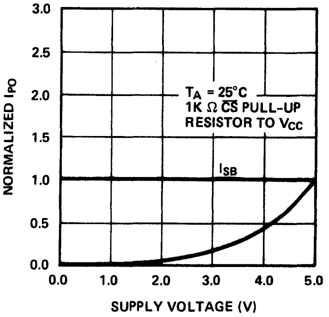

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

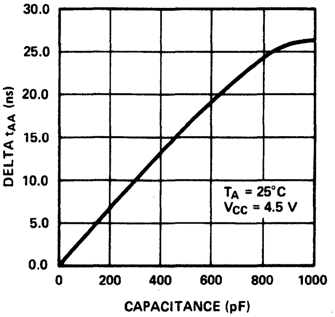

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

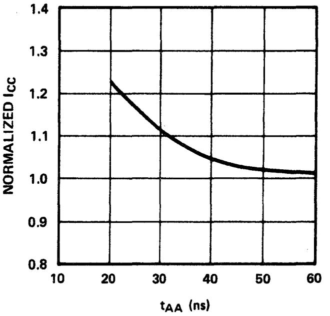

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE


NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)


TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING


NORMALIZED I_{CC} vs. ACCESS TIME

0001-10

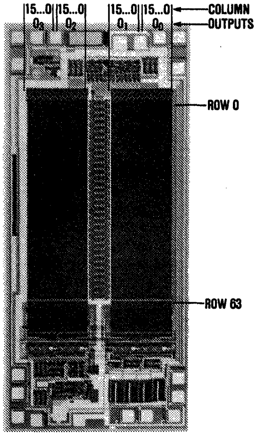
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C148-25PC CY7C149-25PC	P3	Commercial
	CY7C148-25DC CY7C149-25DC	D4	
	CY7C148-25LC CY7C149-25LC	L50	
35	CY7C148-35PC CY7C149-35PC	P3	Commercial
	CY7C148-35DC CY7C149-35DC	D4	
	CY7C148-35LC CY7C149-35LC	L50	
	CY7C148-35DMB CY7C149-35DMB	D4	Military
	CY7C148-35LMB CY7C149-35LMB	L50	
45	CY7C148-45PC CY7C149-45PC	P3	Commercial
	CY7C148-45DC CY7C149-45DC	D4	
	CY7C148-45LC CY7C149-45LC	L50	
	CY7C148-45DMB CY7C149-45DMB	D4	Military
	CY7C148-45LMB CY7C149-45LMB	L50	

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_0	5
A_1	Y_1	6
A_2	Y_2	7
A_3	Y_3	4
A_4	X_0	3
A_5	X_3	2
A_6	X_2	1
A_7	X_5	17
A_8	X_4	16
A_9	X_1	15

Bit Map



0001-11

CYPRESS SEMICONDUCTOR

CY7C150

1024 x 4 Static R/W RAM

Features

- **Memory reset function**
- **1024 x 4 static RAM for control store in high speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 550 mW (military)**
- **Separate inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL compatible inputs and outputs**

Functional Description

The CY7C150 is a high performance CMOS static RAM designed for use in cache memory, high speed graphics, and data aquisition applications. Organized as 1024 words x 4 bits, the entire memory can be reset to zero in two memory cycles.

Separate I/O paths eliminate the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are tri-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS}$ = LOW) and pulsing the reset ($\overline{RS}$) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

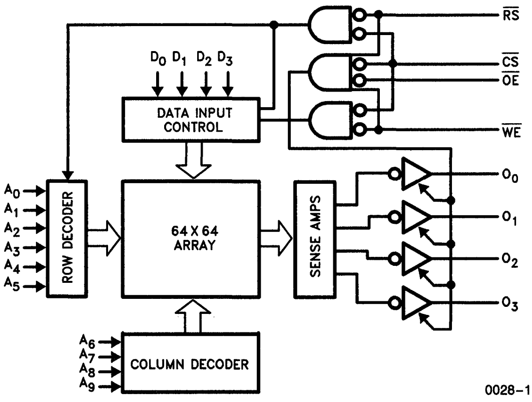
An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are LOW, the information on the four data inputs D_0 to D_3 is written into the addressed memory location and the output circuitry is preconditioned so that the write data is present at the outputs when the write cycle is completed.

Reading is performed with the chip select ($\overline{CS}$) input LOW, and the write enable ($\overline{WE}$) input HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select ($\overline{CS}$) is HIGH, Reset ($\overline{RS}$) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when Write Enable ($\overline{WE}$) is LOW.

A die coat is used to ensure alpha immunity.

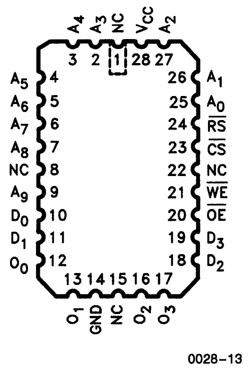
Logic Block Diagram



RS
CS
OE
WE
D0 D1 D2 D3
DATA INPUT CONTROL
A0
A1
A2
A3
A4
A5
ROW DECODER
64 X 64 ARRAY
SENSE AMPS
O0
O1
O2
O3
A6
A7
A8
A9
COLUMN DECODER

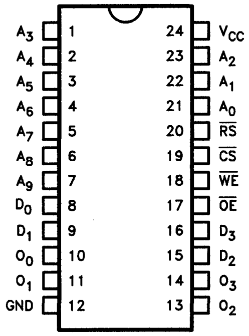
0028-1

Pin Configurations



A4 A3 NC VCC A2
3 2 1 28 27
A5 4
A6 5
A7 6
A8 7
NC 8
A9 9
D0 10
D1 11
O0 12
13 14 15 16 17
O1 GND NC O2 O3
26 A1
25 A0
24 RS
23 CS
22 NC
21 WE
20 OE
19 D3
18 D2

0028-13



A3 1
A4 2
A5 3
A6 4
A7 5
A8 6
A9 7
D0 8
D1 9
O0 10
O1 11
GND 12
24 VCC
23 A2
22 A1
21 A0
20 RS
19 CS
18 WE
17 OE
16 D3
15 D2
14 O3
13 O2

0028-2

Selection Guide

		7C150-15	7C150-25	7C150-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military		25	35
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		100	100

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C150-15, 25, 35		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	μA
I_{OS}	Output Short[1]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90	mA
			Military*		100	

*-25 and -35 only

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

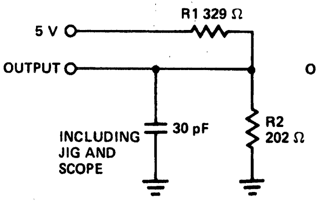

R1 329 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
30 pF
R2
202 Ω

Figure 1a

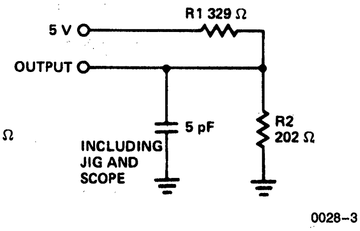

R1 329 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
5 pF
R2
202 Ω
0028-3

Figure 1b

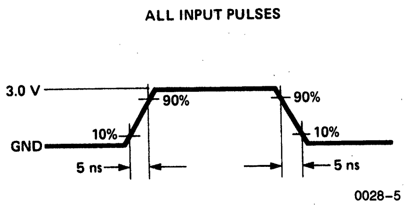
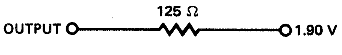

ALL INPUT PULSES
3.0 V
GND
90%
90%
10%
10%
5 ns
5 ns
0028-5

Figure 2

Equivalent To:

THÉVENIN EQUIVALENT


125 Ω
OUTPUT
1.90 V
0028-4

Switching Characteristics Over Operating Range[3]

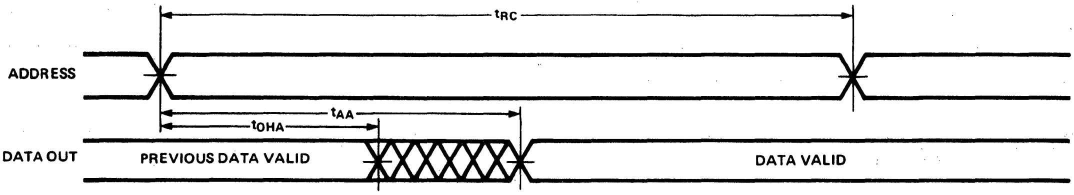
Parameters	Description	7C150-15		7C150-25		7C150-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{AA}	Address to Data Valid		15		25		35	ns
t_{OHA}	Output Hold from Address Change	2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4,5]	0	11	0	20	0	25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[5]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4,5]	0	9	0	20	0	25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	11		15		20		ns
t_{AW}	Address Set-up to Write End	13		20		30		ns
t_{HA}	Address Hold from Write End	2		5		5		ns
t_{SA}	Address Set-up to Write Start	2		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	11		15		20		ns
t_{SD}	Data Set-up to Write End	11		15		20		ns
t_{HD}	Data Hold from Write End	2		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4,5]	0	12	0	20	0	25	ns
RESET CYCLE								
t_{RRC}	Reset Cycle Time	30		50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		ns
t_{PRS}	Reset Pulse Width	15		20		30		ns
t_{HCSR}	Chip Select Hold after End of Reset	0		0		0		ns
t_{HWER}	Write Enable Hold after End of Reset	15		30		40		ns
t_{HAR}	Address Hold after End of Reset	15		30		40		ns
t_{LZRS}	Reset HIGH to Output in Low Z[5]	0		0		0		ns
t_{HZRS}	Reset LOW to Output in High Z[4,5]	0	12	0	20	0	25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZCS}, t_{HZOE}, t_{HZR} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. These parameters are specified and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ and $\overline{OE} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

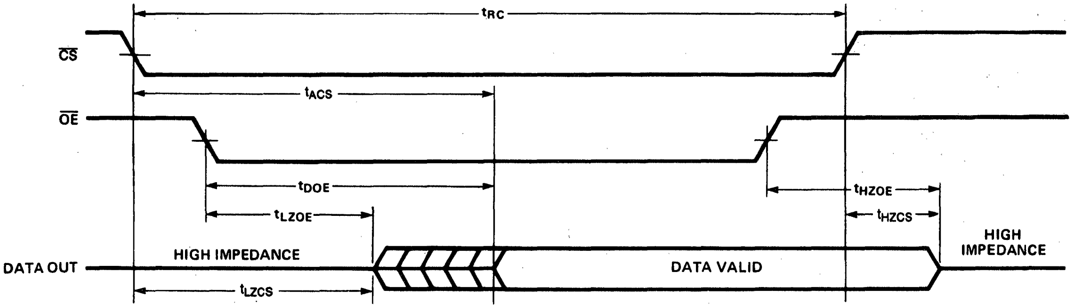
Switching Waveforms

Read Cycle No. 1 (Notes 7, 8)


t_{RC}
ADDRESS
t_{AA}
t_{OHA}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

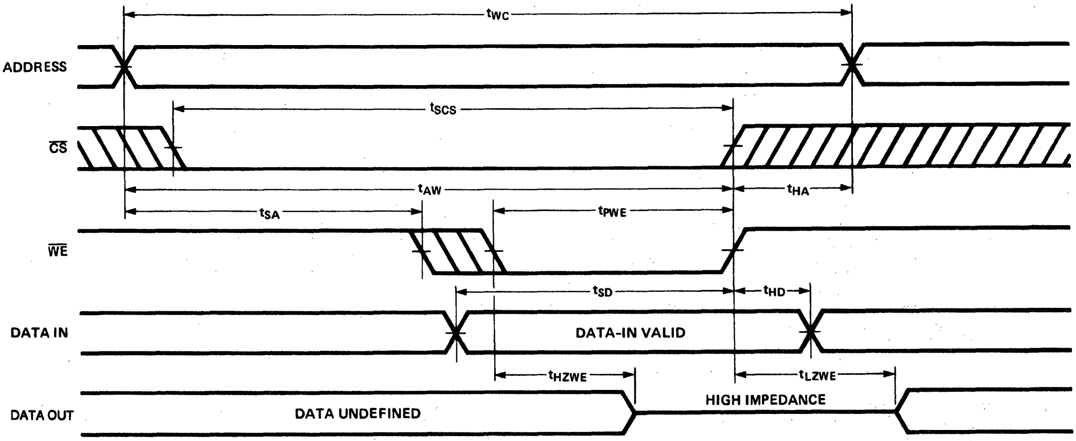
0028-6

Read Cycle No. 2 (Notes 7, 9)


t_{RC}
$\overline{CS}$
t_{ACS}
$\overline{OE}$
t_{DOE}
t_{LZOE}
t_{HZOE}
t_{HZCS}
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
t_{LZCS}

0028-8

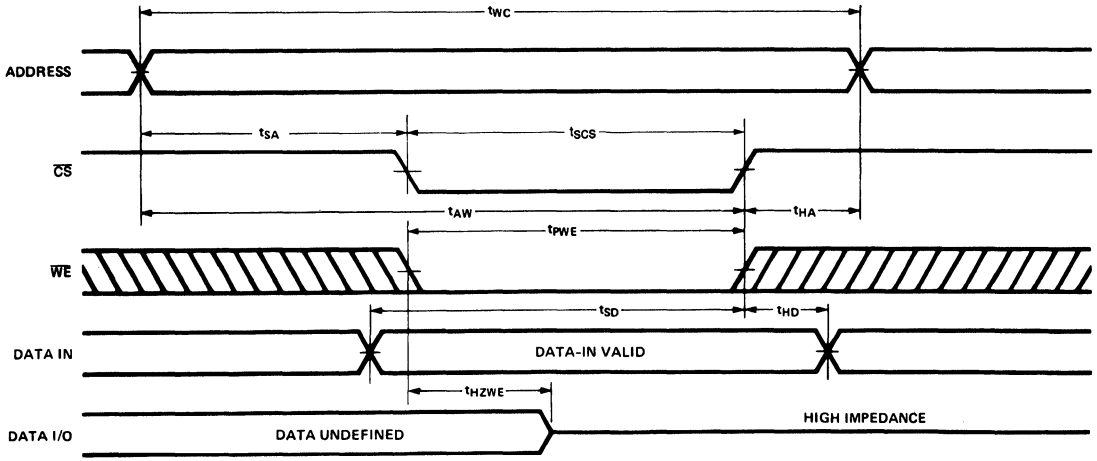
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Note 6)


t_{WC}
ADDRESS
t_{SCS}
$\overline{CS}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

0028-9

Switching Waveforms (Continued)

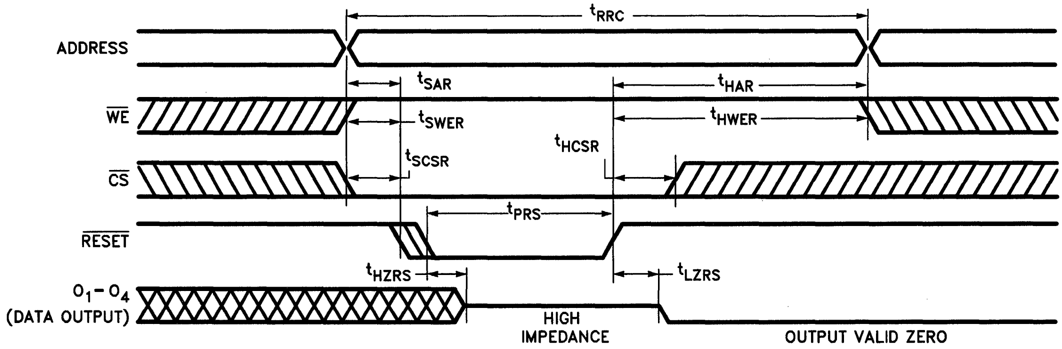
Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled) (Note 6)


tWC
ADDRESS
tSA
tSCS
CS
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0028–10

Note: If $\overline{\text{CS}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state.

Reset Cycle

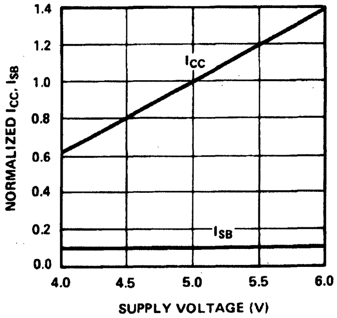

tRRC
ADDRESS
tSAR
tHAR
WE
tSWER
tHWER
tHCSR
tSCSR
CS
tPRS
RESET
tHZRS
tLZRS
O1 - O4
(DATA OUTPUT)
HIGH
IMPEDANCE
OUTPUT VALID ZERO

0028–11

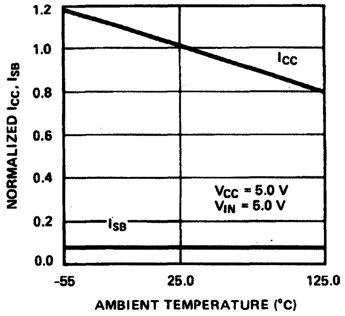
Note: Reset cycle is defined by the overlap of $\overline{\text{RS}}$ and $\overline{\text{CS}}$ for the minimum reset pulse width.

Typical DC and AC Characteristics

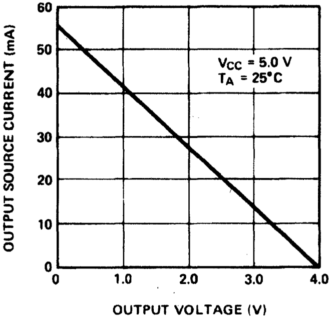
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



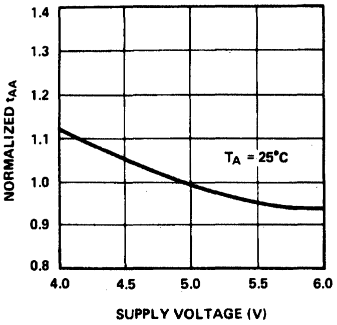
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



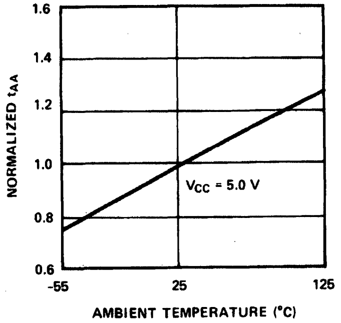
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



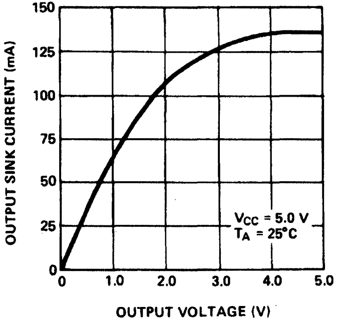
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



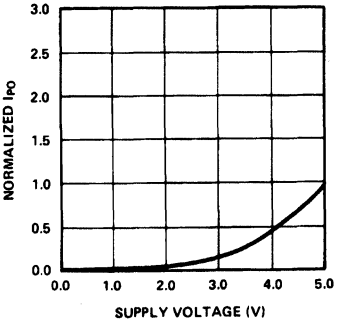
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



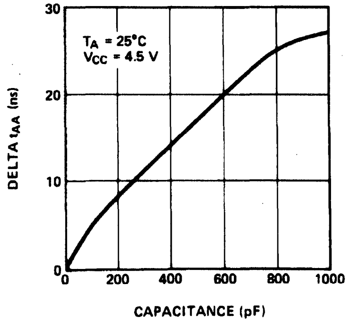
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



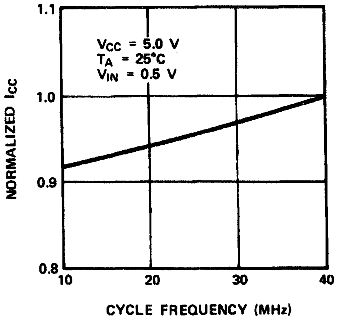
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0028-14

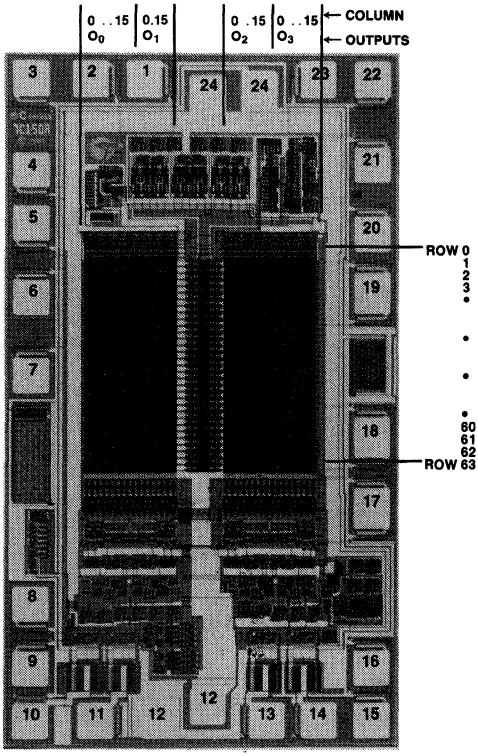
Truth Table

Inputs				Outputs	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{RS}$		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0–O_3	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C150-15PC	P13	Commercial
	CY7C150-15DC	D14	Commercial
	CY7C150-15LC	L54	Commercial
25	CY7C150-25PC	P13	Commercial
	CY7C150-25DC	D14	Commercial
	CY7C150-25LC	L54	Commercial
	CY7C150-25DMB	D14	Military
	CY7C150-25LMB	L54	Military
35	CY7C150-35PC	P13	Commercial
	CY7C150-35DC	D14	Commercial
	CY7C150-35LC	L54	Commercial
	CY7C150-35DMB	D14	Military
	CY7C150-35LMB	L54	Military

Bit Map


0 ..15
O_0
0.15
O_1
0 .15
O_2
0 ..15
O_3
← COLUMN
← OUTPUTS
3
2
1
24
24
23
22
4
21
5
20
6
19
7
18
17
8
9
16
10
11
12
12
13
14
15
ROW 0
1
2
3
60
61
62
ROW 63

0028-15

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	21
A_1	X_1	22
A_2	X_2	23
A_3	X_3	1
A_4	X_4	2
A_5	X_5	3
A_6	Y_0	4
A_7	Y_1	5
A_8	Y_2	6
A_9	Y_3	7

CYPRESS SEMICONDUCTOR

CY7C161
CY7C162

16,384 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **Transparent Write (7C161)**
- **CMOS for optimum speed/power**
- **High Speed**
  - **25 ns t_{AA}**
- **Low active power**
  - **385 mW**
- **Low standby power**
  - **110 mW**
- **TTL compatible inputs and outputs**
- **2V data retention (L version)**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C161 and CY7C162 are high performance CMOS static RAMs organized as 16,384 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 85% when deselected.

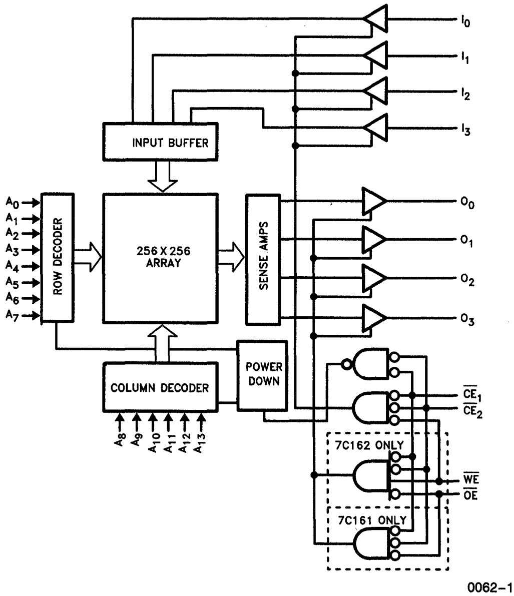
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high impedance state when write enable ($\overline{WE}$) is LOW (7C162 only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

A die coat is used to insure alpha immunity.

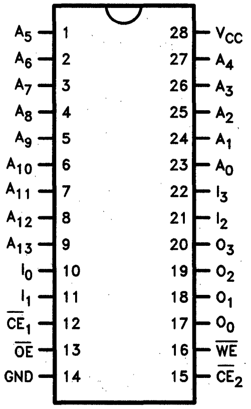
Logic Block Diagram



I0
I1
I2
I3
INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
A7
ROW DECODER
256 X 256 ARRAY
SENSE AMPS
O0
O1
O2
O3
POWER DOWN
COLUMN DECODER
A8
A9
A10
A11
A12
A13
CE1
CE2
7C162 ONLY
WE
OE
7C161 ONLY

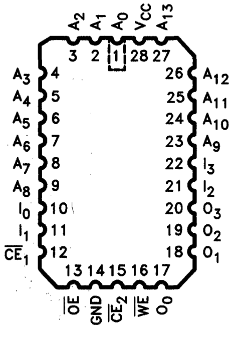
0062-1

Pin Configurations



A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
I0 10
I1 11
CE1 12
OE 13
GND 14
28 VCC
27 A4
26 A3
25 A2
24 A1
23 A0
22 I3
21 I2
20 O3
19 O2
18 O1
17 O0
16 WE
15 CE2

0062-2



A2
A1
A0
VCC
A13
3 2 1 28 27
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
I0 10
I1 11
CE1 12
26 A12
25 A11
24 A10
23 A9
22 I3
21 I2
20 O3
19 O2
18 O1
13 14 15 16 17
OE
GND
CE2
WE
O0

0062-3

Selection Guide

		7C161-25 7C162-25	7C161-35 7C162-35	7C161-45 7C162-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C161-25 7C162-25		7C161-35 7C162-35		7C161-45 7C162-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		70		50	mA
			Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military		20		20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} −0.3V V_{IN} ≥ V_{CC} −0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

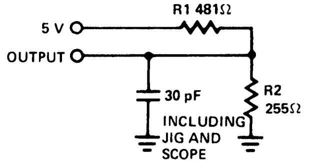


Figure 1a

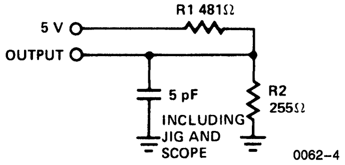


Figure 1b

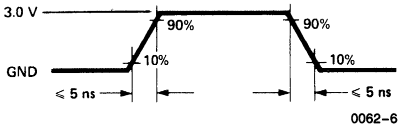
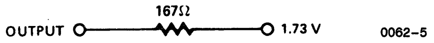


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[3, 10]

Parameters	Description	7C161-25 7C162-25		7C161-35 7C162-35		7C161-45 7C162-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[5]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4, 5]		10		15		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z		15		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		25		35		45	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5] (7C162)	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5] (7C162)		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161)		20		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C161)		20		30		35	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. These parameters are guaranteed and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$, $\overline{CE}_2$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is high for read cycle.
8. Device is continuously selected, $\overline{CE}_1, \overline{CE}_2 = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.
10. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms.

Data Retention Characteristics (L Version only)

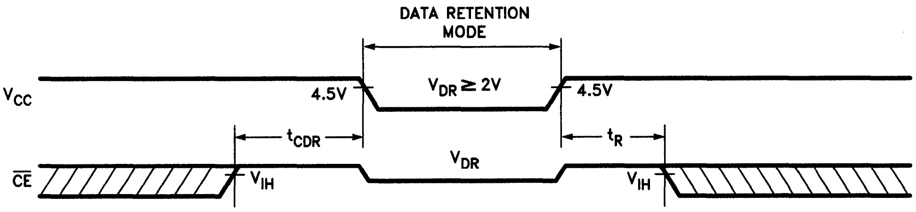
Parameters	Description	Test Conditions	CY7C161/CY7C162		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention of Data	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	V
I_{CCDR}	Data Retention Current		—	1000	μA
t_{CDR}[12]	Chip Deselect to Data Retention Time		0	—	ns
t_R[12]	Operation Recovery Time		t_{RC}[11]	—	ns
I_{LI}[12]	Input Leakage Current		—	2	μA

Notes:

11. t_{RC} = Read Cycle Time.

12. Guaranteed, not tested.

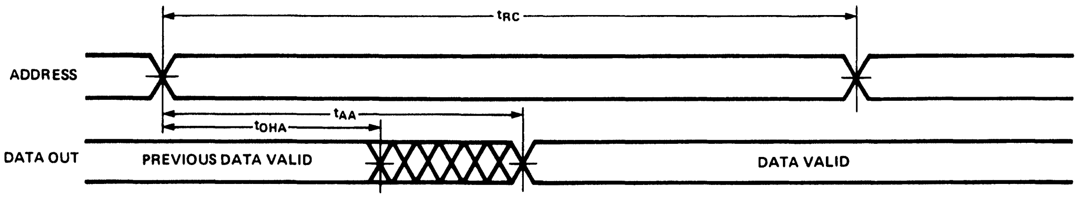
Data Retention Waveform


DATA RETENTION MODE
V_{CC}
4.5V
$V_{DR} \geq 2V$
4.5V
t_{CDR}
t_R
$\overline{CE}$
V_{IH}
V_{DR}
V_{IH}

0062-11

Switching Waveforms[10]

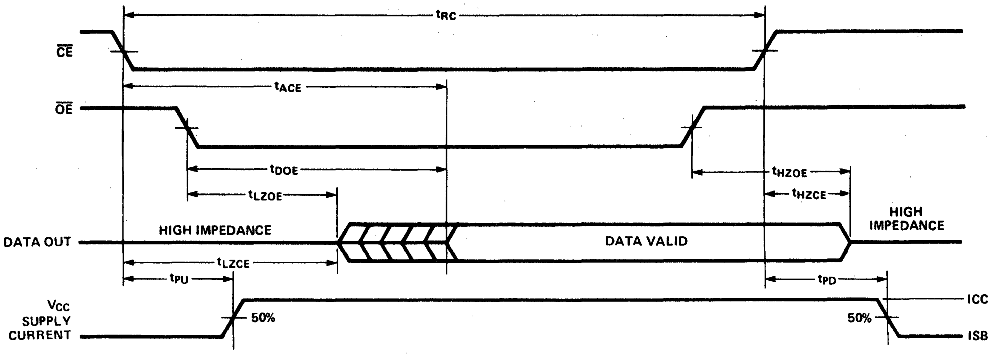
Read Cycle No. 1 (Notes 7, 8)


t_{RC}
ADDRESS
t_{AA}
t_{OHA}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

0062-7

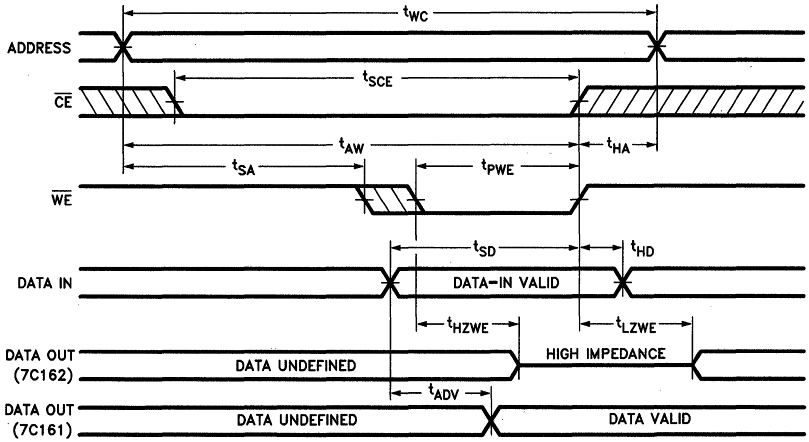
Switching Waveforms[10] (Continued)

Read Cycle (Notes 7, 9)


tRC
CE
tACE
OE
tDOE
tLZOE
tHZOE
tHZCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
tLZCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

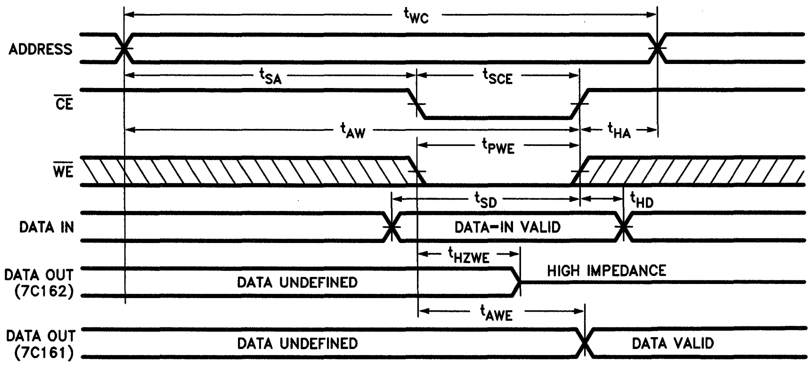
0062-8

Write Cycle No. 1 (WE Controlled) (Note 6)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA OUT (7C162)
DATA UNDEFINED
HIGH IMPEDANCE
tADV
DATA OUT (7C161)
DATA UNDEFINED
DATA VALID

0062-9

Write Cycle No. 2 (CE Controlled) (Note 6)

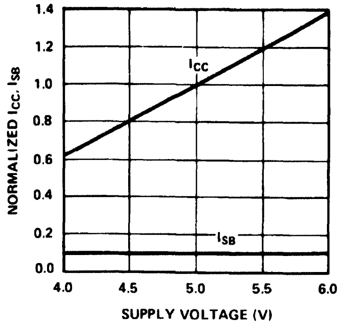

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA OUT (7C162)
DATA UNDEFINED
HIGH IMPEDANCE
tAWE
DATA OUT (7C161)
DATA UNDEFINED
DATA VALID

0062-10

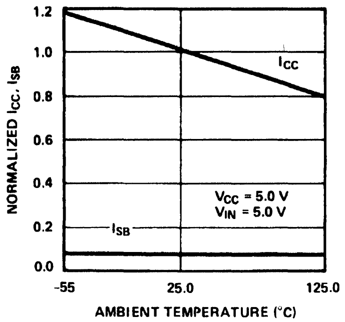
Note: If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state (7C162 only).

Typical DC and AC Characteristics

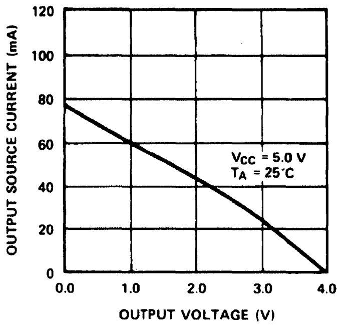
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



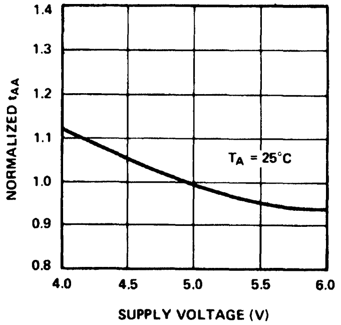
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



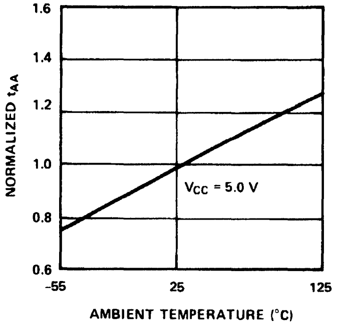
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



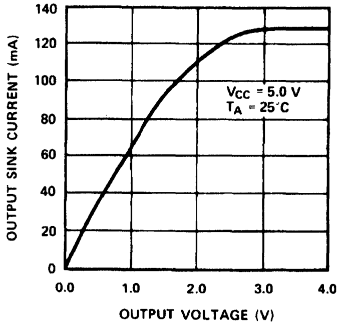
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



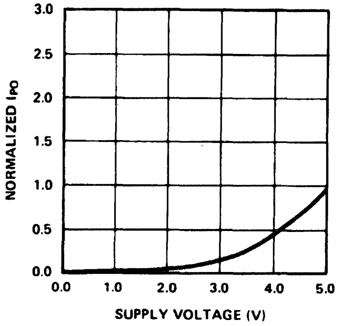
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



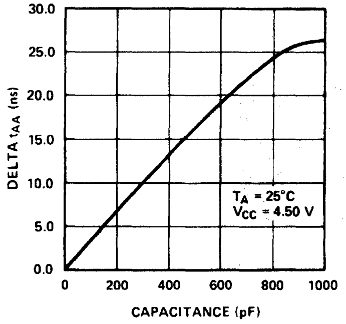
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



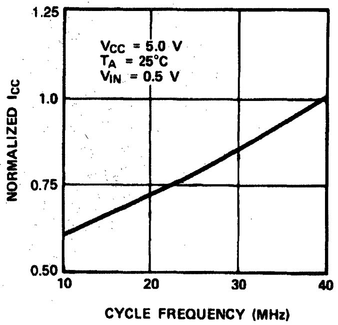
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



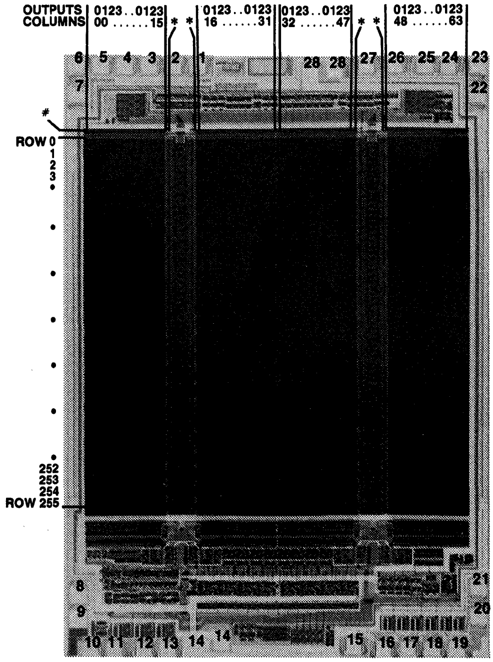
0062-12

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C161-25PC	P21	Commercial
	CY7C161L-25PC	P21	
	CY7C161-25DC	D22	
	CY7C161L-25DC	D22	
35	CY7C161-35PC	P21	Commercial
	CY7C161L-35PC	P21	
	CY7C161-35DC	D22	
	CY7C161L-35DC	D22	
	CY7C161-35LC	L54	
	CY7C161L-35LC	L54	
	CY7C161-35DMB	D22	Military
	CY7C161L-35DMB	D22	
	CY7C161-35LMB	L54	
	CY7C161L-35LMB	L54	
45	CY7C161-45PC	P21	Commercial
	CY7C161L-45PC	P21	
	CY7C161-45DC	D22	
	CY7C161L-45DC	D22	
	CY7C161-45LC	L54	
	CY7C161L-45LC	L54	
	CY7C161-45DMB	D22	Military
	CY7C161L-45DMB	D22	
	CY7C161-45LMB	L54	
	CY7C161L-45LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C162-25PC	P21	Commercial
	CY7C162L-25PC	P21	
	CY7C162-25DC	D22	
	CY7C162L-25DC	D22	
35	CY7C162-35PC	P21	Commercial
	CY7C162L-35PC	P21	
	CY7C162-35DC	D22	
	CY7C162L-35DC	D22	
	CY7C162-35LC	L54	
	CY7C162L-35LC	L54	
	CY7C162-35DMB	D22	Military
	CY7C162L-35DMB	D22	
	CY7C162-35LMB	L54	
	CY7C162L-35LMB	L54	
45	CY7C162-45PC	P21	Commercial
	CY7C162L-45PC	P21	
	CY7C162-45DC	D22	
	CY7C162L-45DC	D22	
	CY7C162-45LC	L54	
	CY7C162L-45LC	L54	
	CY7C162-45DMB	D22	Military
	CY7C162L-45DMB	D22	
	CY7C162-45LMB	L54	
	CY7C162L-45LMB	L54	

Bit Map


OUTPUTS
COLUMNS
0123..0123
00......15
*
*
0123..0123
16......31
0123..0123
32......47
*
*
0123..0123
48......63
6
5
4
3
2
1
28
28
27
26
25
24
23
7
22
#
ROW 0
1
2
3
252
253
254
ROW 255
8
9
21
20
10
11
12
13
14
14
15
16
17
18
19

0062-13

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

CY7C164
CY7C166

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **Output Enable ($\overline{OE}$) Feature (7C166)**
- **CMOS for optimum speed/ power**
- **High speed — 25 ns t_{AA}**
- **Low active power — 385 mW**
- **Low standby power — 110 mW**
- **TTL compatible inputs and outputs**
- **2V data retention (L version)**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

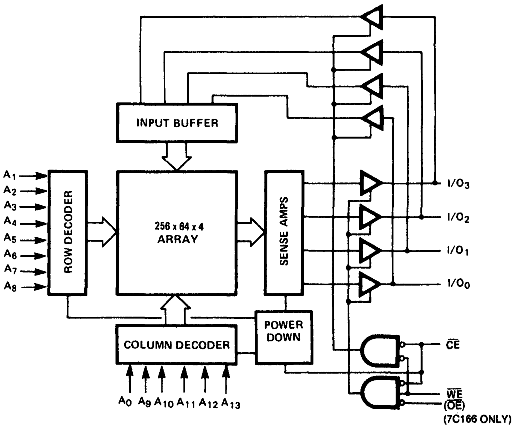
The CY7C164 and CY7C166 are high performance CMOS static RAMs organized as 16,384 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166 has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166). Data on the four input/output pins (I/O$_0$ through I/O$_3$) is written into the memory location specified on the address pins (A$_0$ through A$_{13}$).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW (or output enable ($\overline{OE}$) is HIGH for 7C166). A die coat is used to insure alpha immunity.

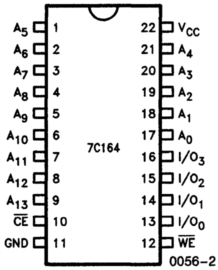
Logic Block Diagram



INPUT BUFFER
A1
A2
A3
A4
A5
A6
A7
A8
ROW DECODER
256 x 64 x 4 ARRAY
SENSE AMPS
I/O3
I/O2
I/O1
I/O0
POWER DOWN
COLUMN DECODER
A0 A9 A10 A11 A12 A13
CE
WE
(OE)
(7C166 ONLY)

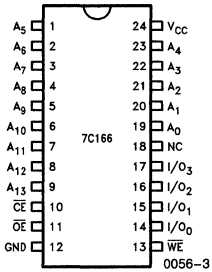
0056–1

Pin Configurations



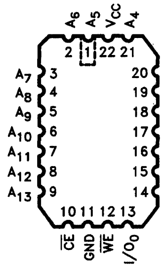
A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
CE 10
GND 11
22 VCC
21 A4
20 A3
19 A2
18 A1
17 A0
16 I/O3
15 I/O2
14 I/O1
13 I/O0
12 WE
7C164

0056–2



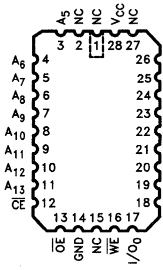
A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
CE 10
OE 11
GND 12
24 VCC
23 A4
22 A3
21 A2
20 A1
19 A0
18 NC
17 I/O3
16 I/O2
15 I/O1
14 I/O0
13 WE
7C166

0056–3



A6 A5 VCC A4
2 1 22 21
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
20 A3
19 A2
18 A1
17 A0
16 I/O3
15 I/O2
14 I/O1
10 11 12 13
CE GND WE I/O0

0056–4



A5 NC NC VCC NC
3 2 1 28 27
A6 4
A7 5
A8 6
A9 7
A10 8
A11 9
A12 10
A13 11
CE 12
26 NC
25 A4
24 A3
23 A2
22 A1
21 A0
20 I/O3
19 I/O2
18 I/O1
13 14 15 16 17
OE GND NC WE I/O0

0056–5

Selection Guide

		7C164-25 7C166-25	7C164-35 7C166-35	7C164-45 7C166-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State........................ −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C164-25 7C166-25		7C164-35 7C166-35		7C164-45 7C166-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		70		50	mA
			Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military				20		20	
I_{SB_2}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} −0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

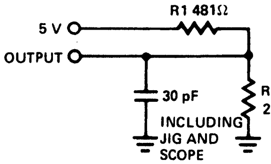


Figure 1a

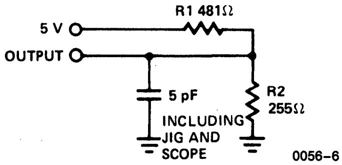


Figure 1b

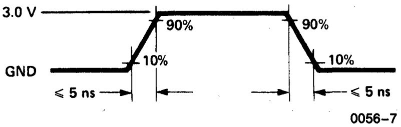
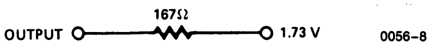


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

Parameters	Description		7C164-25 7C166-25		7C164-35 7C166-35		7C164-45 7C166-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		25		35		45		ns
t_{AA}	Address to Data Valid			25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid			25		35		45	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	7C166		15		25		30	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to LOW Z	7C166	3		3		3		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to HIGH Z	7C166		15		15		15	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[6]		5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[5, 6]			10		15		15	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up		0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down			25		35		45	ns
WRITE CYCLE[7]									
t_{WC}	Write Cycle Time		20		30		40		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End		20		30		35		ns
t_{AW}	Address Set-up to Write End		20		25		35		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width		20		25		35		ns
t_{SD}	Data Set-up to Write End		13		15		20		ns
t_{HD}	Data Hold from Write End		0		0		5		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[6]		3		3		3		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[5, 6]		0	7	0	10	0	15	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{\text{WE}}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$. (7C166: $\overline{\text{OE}} = V_{IL}$ also.)
10. Address valid prior to or coincident with $\overline{\text{CE}}$ transition low.
11. 7C166 only: Data I/O will be high impedance if $\overline{\text{OE}} = V_{IH}$.

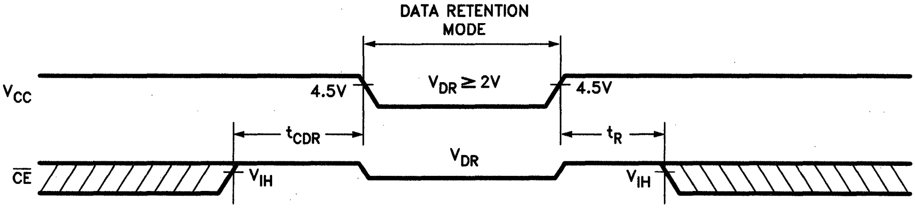
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CY7C164/CY7C166		Units
			Min.	Max.	
V_{DR}	V_{CC} For Retention of Data	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	V
I_{CCDR}	Data Retention Current		—	1000	μA
t_{CDR}[13]	Chip Deselect to Data Retention Time		0	—	ns
t_R[13]	Operation Recovery Time		t_{RC}[12]	—	ns
I_{LI}[13]	Input Leakage Current		—	2	μA

Notes:

12. t_{RC} = read cycle time.
13. Guaranteed, not tested.

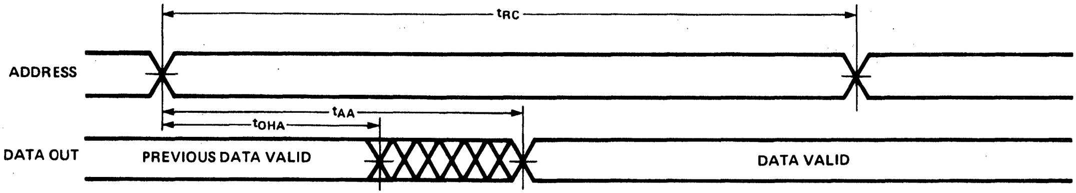
Data Retention Waveform


DATA RETENTION MODE
V_{CC}
4.5V
$V_{DR} \geq 2V$
4.5V
t_{CDR}
t_R
V_{DR}
$\overline{CE}$
V_{IH}
V_{IH}

0056-13

Switching Waveforms

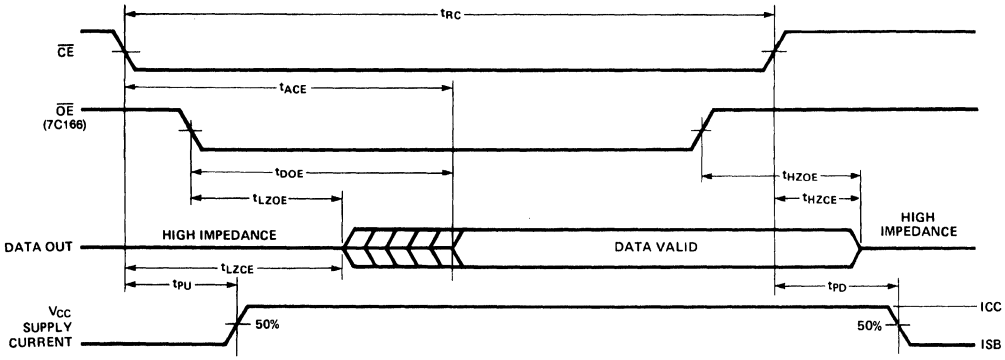
Read Cycle No. 1 (Notes 8, 9)


t_{RC}
ADDRESS
t_{AA}
t_{OHA}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

0056-9

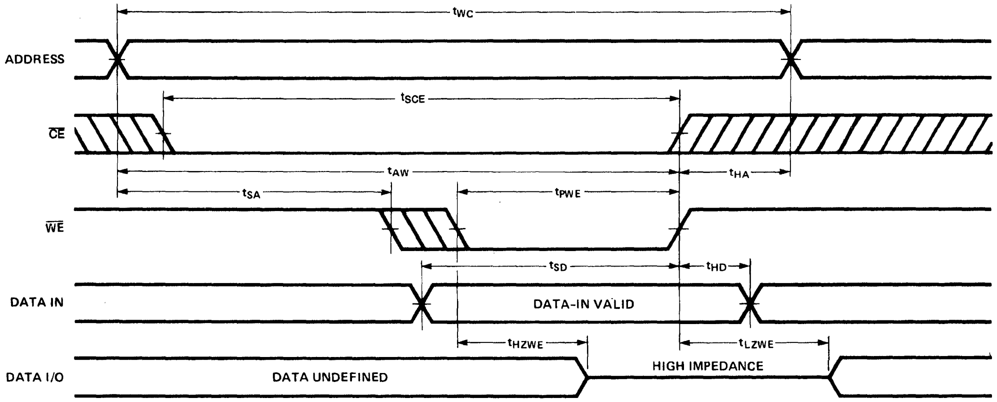
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


tRC
CE
tACE
OE
(7C166)
tDOE
tLZOE
tHZOE
tHZCE
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
tLZCE
tPU
tPD
VCC
SUPPLY
CURRENT
50%
50%
ICC
ISB

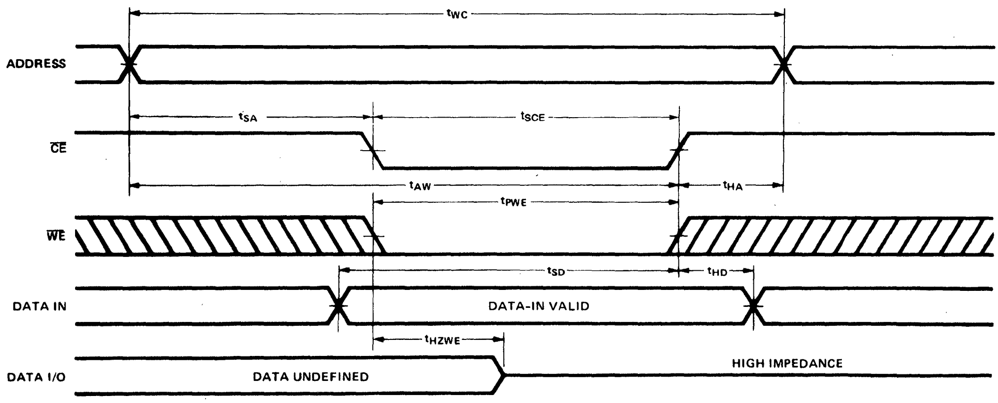
0056–10

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Notes 7, 11)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0056–11

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) (Notes 7, 11)

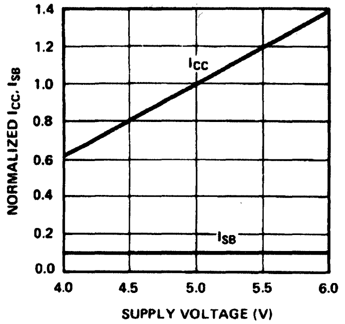

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0056–12

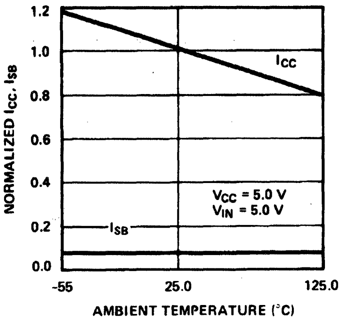
Note: If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

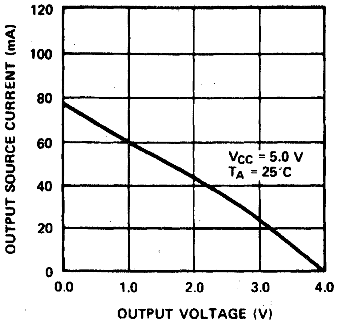
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



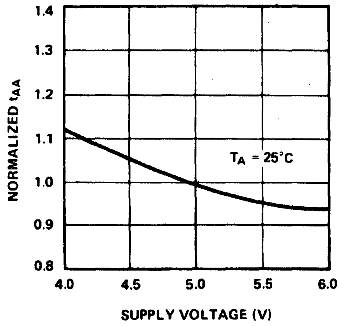
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



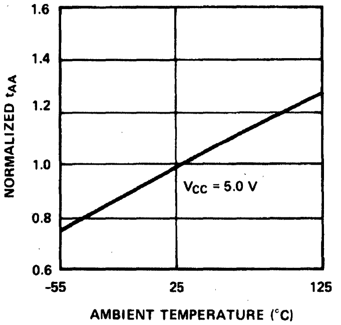
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



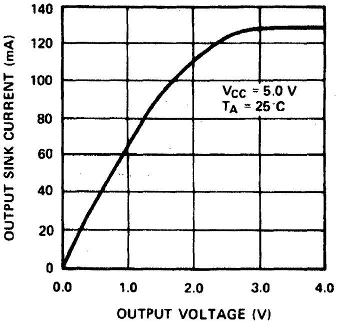
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



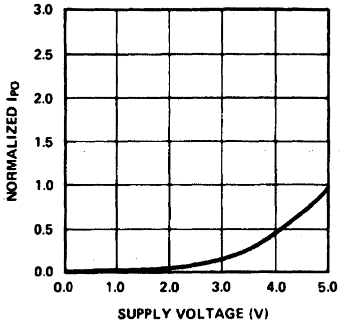
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



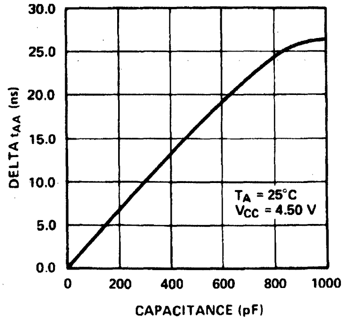
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



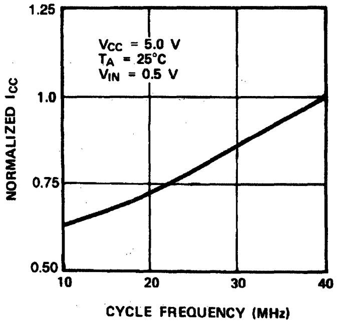
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0056–14

7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect Power Down
L	H	Data Out	Read
L	L	Data In	Write

7C166 Truth Table

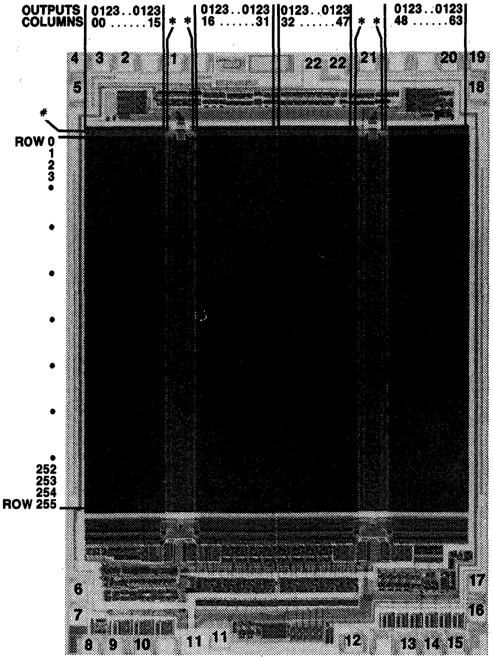
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C164-25PC CY7C164L-25PC	P9	Commercial
	CY7C164-25DC CY7C164L-25DC	D10	
35	CY7C164-35PC CY7C164L-35PC	P9	Commercial
	CY7C164-35DC CY7C164L-35DC	D10	
	CY7C164-35LC CY7C164L-35LC	L52	
	CY7C164-35DMB CY7C164L-35DMB	D10	Military
	CY7C164-35LMB CY7C164L-35LMB	L52	
45	CY7C164-45PC CY7C164L-45PC	P9	Commercial
	CY7C164-45DC CY7C164L-45DC	D10	
	CY7C164-45LC CY7C164L-45LC	L52	
	CY7C164-45DMB CY7C164L-45DMB	D10	Military
	CY7C164-45LMB CY7C164L-45LMB	L52	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C166-25PC CY7C166L-25PC	P13	Commercial
	CY7C166-25DC CY7C166L-25DC	D14	
35	CY7C166-35PC CY7C166L-35P	P13	Commercial
	CY7C166-35DC CY7C166L-35DC	D14	
	CY7C166-35LC CY7C166L-35LC	L54	
	CY7C166-35DMB CY7C166L-35DMB	D14	Military
	CY7C166-35LMB CY7C166L-35LMB	L54	
45	CY7C166-45PC CY7C166L-45PC	P13	Commercial
	CY7C166-45DC CY7C166L-45DC	D14	
	CY7C166-45LC CY7C166L-45LC	L54	
	CY7C166-45DMB CY7C166L-45DMB	D14	Military
	CY7C166-45LMB CY7C166L-45LMB	L54	

Bit Map


OUTPUTS
COLUMNS
0123..0123
00......15
*
*
0123..0123
16......31
0123..0123
32......47
*
*
0123..0123
48......63
#
ROW 0
1
2
3
252
253
254
ROW 255
1
2
3
4
5
6
7
8
9
10
11
11
12
13
14
15
16
17
18
19
20
21
22
22

0056-15

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

CYPRESS SEMICONDUCTOR

CY7C167

16,384 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power**
  - **— 248 mW (commercial)**
  - **— 275 mW (military)**
- **Low standby power**
  - **— 83 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C167 is a high performance CMOS static RAM organized as 16,384 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{\text{CE}}$) and three-state drivers. The CY7C167 has an automatic power-down feature, reducing the power consumption by 70% when deselected.

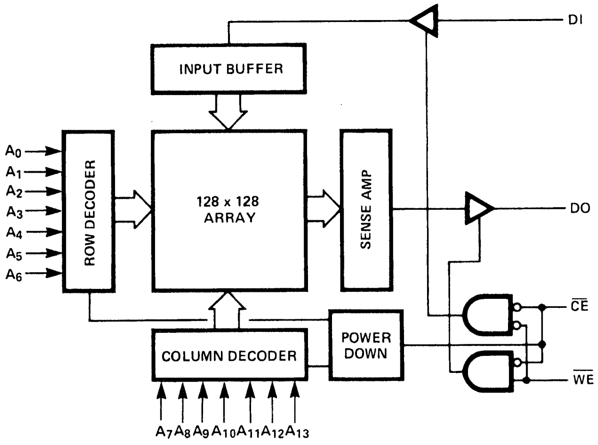
Writing to the device is accomplished when the chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{\text{CE}}$) LOW, while write enable ($\overline{\text{WE}}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ($\overline{\text{CE}}$) is HIGH or write enable ($\overline{\text{WE}}$) is LOW.

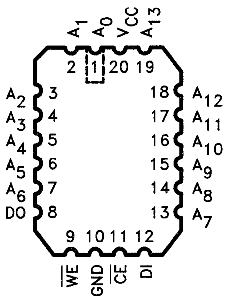
A die coat is used to insure alpha immunity.

Logic Block Diagram

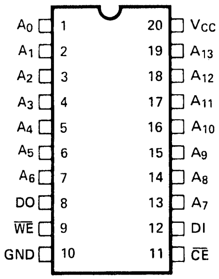

DI
INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
ROW DECODER
128 x 128 ARRAY
SENSE AMP
DO
CE
WE
COLUMN DECODER
POWER DOWN
A7 A8 A9 A10 A11 A12 A13

0017-1

Pin Configurations


A1
A0
VCC
A13
2
1
20
19
A2 3
A3 4
A4 5
A5 6
A6 7
DO 8
18 A12
17 A11
16 A10
15 A9
14 A8
13 A7
9
10
11
12
WE
GND
CE
DI

0017-2


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
DO 8
WE 9
GND 10
20 VCC
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
13 A7
12 DI
11 CE

0017-3

Selection Guide

			7C167-25	7C167-35	7C167-45
Maximum Access Time (ns)			25	35	45
Maximum Operating Current (mA)	L	Commercial	45	45	
	STD	Commercial	60	60	50
		Military		60	50

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(Per MIL-STD-883 Method 3015.2)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C167L-25, 35		7C167-25, 35		7C167-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short[1] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		45		60		50	mA
			Military*				60		50	
I_{SB}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		15		20		15	mA
			Military*				20		20	

* −35 and −45 only

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		6	
C_{CE}	Chip Enable Capacitance		5	

Notes:

1. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

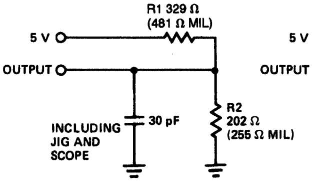

R1 329 Ω
(481 Ω MIL)
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
30 pF
R2
202 Ω
(255 Ω MIL)

Figure 1a

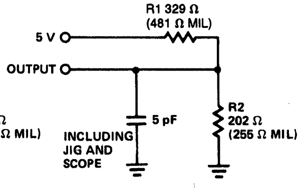
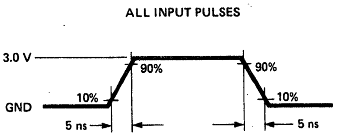

R1 329 Ω
(481 Ω MIL)
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
5 pF
R2
202 Ω
(255 Ω MIL)

Figure 1b

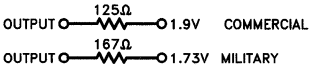
0017-4


ALL INPUT PULSES
3.0 V
GND
90%
10%
90%
10%
5 ns
5 ns

0017-6

Figure 2

Equivalent to: THÉVENIN EQUIVALENT


125Ω
OUTPUT
1.9V
COMMERCIAL
167Ω
OUTPUT
1.73V
MILITARY

0017-5

Switching Characteristics Over Operating Range[4]

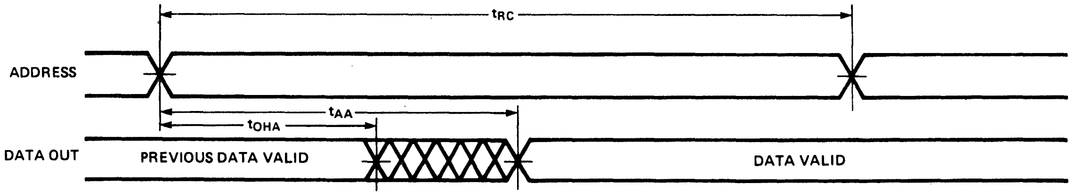
Parameters	Description	7C167-25		7C167-35		7C167-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time (Commercial)	25		30		40		ns
t_{RC}	Read Cycle Time (Military)			35		40		ns
t_{AA}	Address to Data Valid (Commercial)		25		30		40	ns
t_{AA}	Address to Data Valid (Military)				35		40	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[5, 6]		15		20		25	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		30		40		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	25		30		40		ns
t_{AW}	Address Set-up to Write End	25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	15		20		20		ns
t_{SD}	Data Set-up to Write End	15		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[5, 6]	0	15	0	20	0	20	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[6]	0	15	0	20	0	25	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ low and $\overline{\text{WE}}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{\text{WE}}$ is high for read cycle.
9. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{\text{CE}}$ transition low.

Switching Waveforms

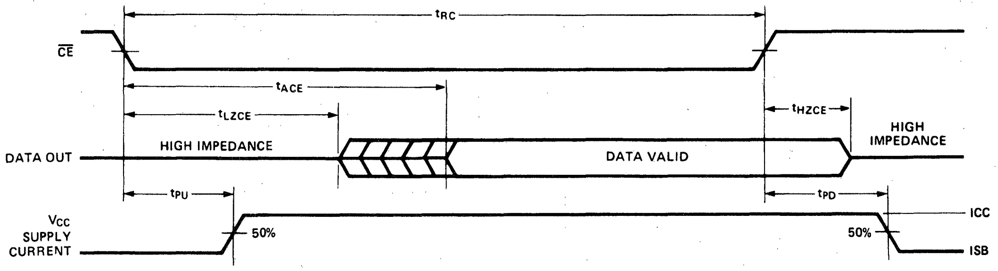
Read Cycle No. 1 (Notes 8, 9)



0017-7

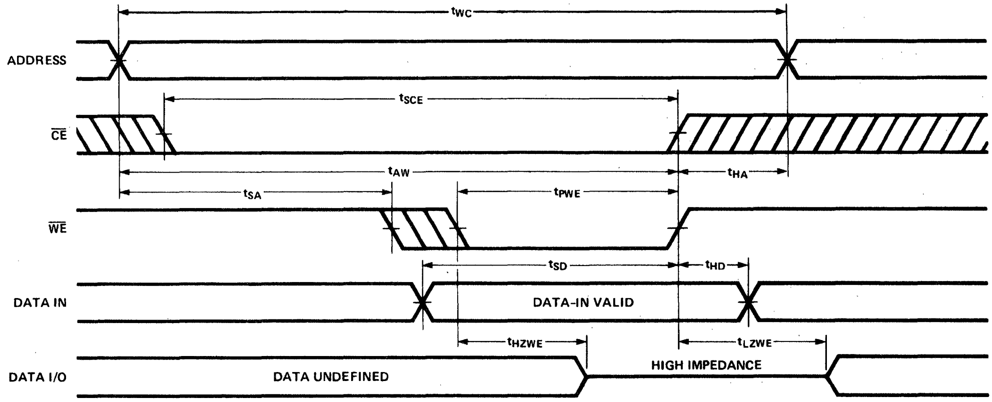
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


tRC
CE
tACE
tLZCE
tHZCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

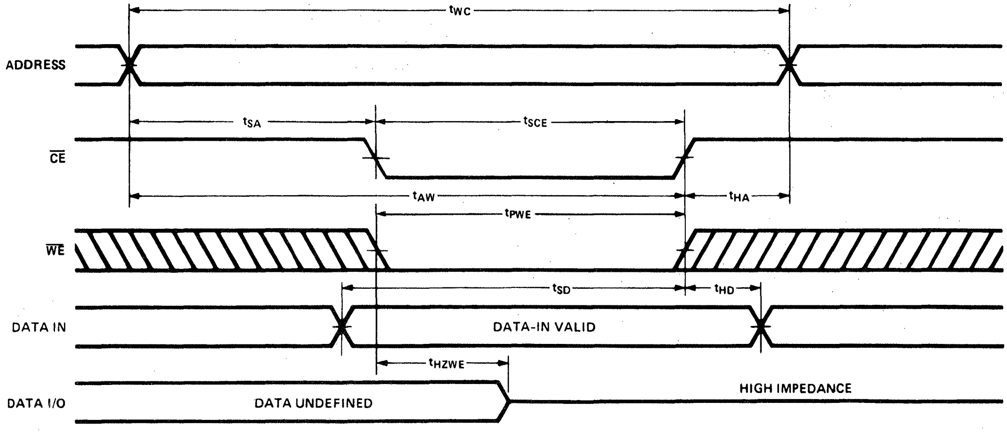
0017-8

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Note 7)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0017-9

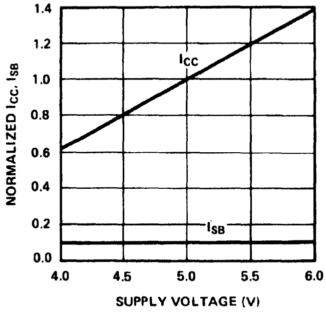
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) (Note 7)


tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

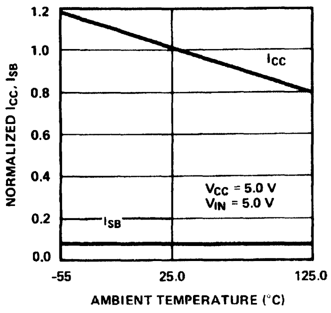
0017-10

Note: If $\overline{\text{CE}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance state.

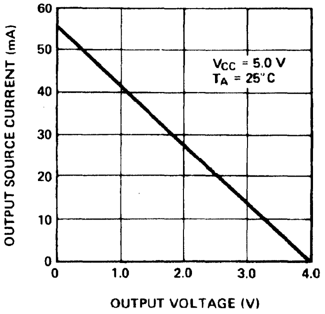
Typical DC and AC Characteristics



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

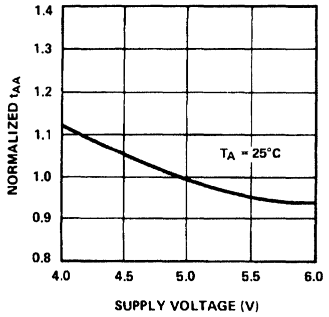


NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

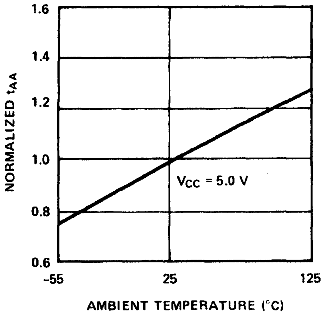


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

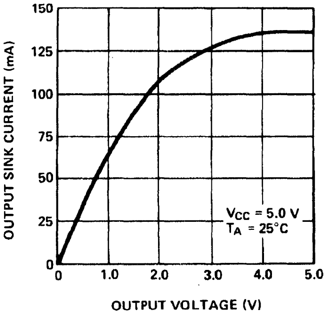
2



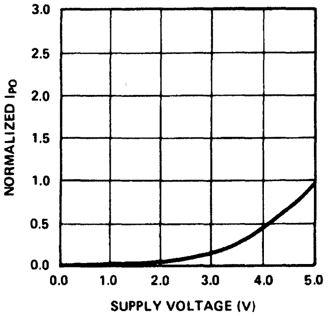
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



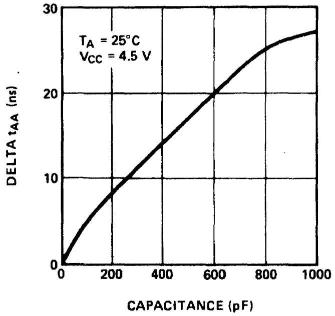
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



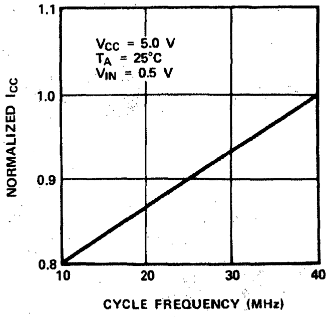
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME

0017-11

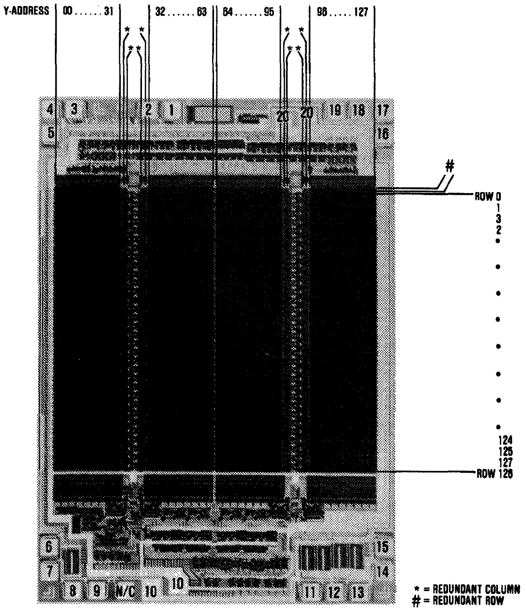
Ordering Information

Speed (ns)	I_{CC} mA	Ordering Code	Package Type	Operating Range
25	45	CY7C167L-25PC	P5	Commercial
		CY7C167L-25DC	D6	
		CY7C167L-25LC	L51	
	60	CY7C167-25PC	P5	
		CY7C167-25DC	D6	
		CY7C167-25LC	L51	
35	45	CY7C167L-35PC	P5	Commercial
		CY7C167L-35DC	D6	
		CY7C167L-35LC	L51	
	60	CY7C167-35PC	P5	
		CY7C167-35DC	D6	
		CY7C167-35LC	L51	
		CY7C167-35DMB	D6	Military
		CY7C167-35LMB	L51	
45	50	CY7C167-45PC	P5	Commercial
		CY7C167-45DC	D6	
		CY7C167-45LC	L51	
		CY7C167-45DMB	D6	Military
		CY7C167-45LMB	L51	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_2	1
A_1	X_5	2
A_2	X_6	3
A_3	Y_3	4
A_4	Y_4	5
A_5	Y_0	6
A_6	Y_1	7
A_7	Y_2	13
A_8	Y_5	14
A_9	Y_6	15
A_{10}	X_0	16
A_{11}	X_3	17
A_{12}	X_4	18
A_{13}	X_1	19

Bit Map


Y-ADDRESS
00......31
32......63
64......95
96.....127
* *
* *
* *
* *
4
3
2
1
20
20
19
18
17
5
16
6
7
15
14
8
9
N/C
10
10
11
12
13
#
ROW 0
1
3
2
124
125
127
ROW 126
* = REDUNDANT COLUMN
# = REDUNDANT ROW

0017-12

CYPRESS
SEMICONDUCTOR

CY7C168
CY7C169

4096 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected (7C168)**
- **CMOS for optimum speed/ power**
- **High Speed**
  - **— 25 ns t_{AA}**
  - **— 15 ns t_{ACE} (7C169)**
- **Low active power**
  - **— 330 mW (commercial)**
  - **— 385 mW (military)**
- **Low standby power (7C168)**
  - **— 83 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

The CY7C168 and CY7C169 are high performance CMOS static RAMs organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 77% when deselected.

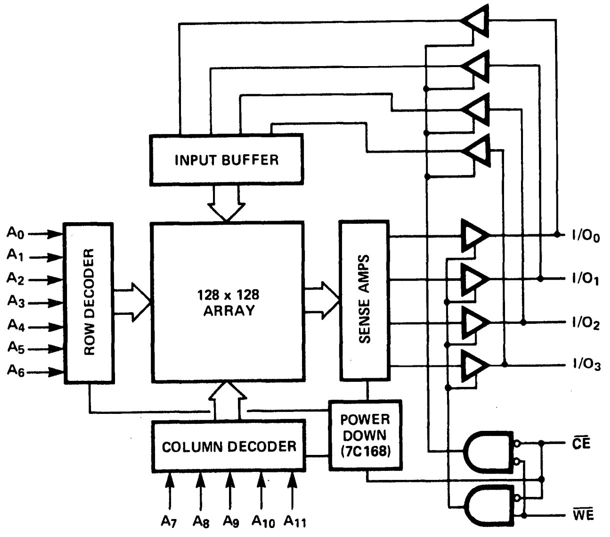
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

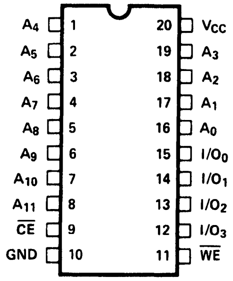
A die coat is used to insure alpha immunity.

Logic Block Diagram

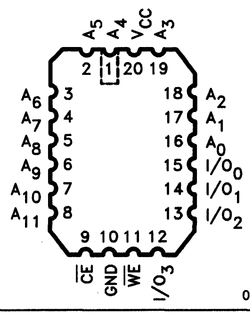

INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
ROW DECODER
128 x 128 ARRAY
SENSE AMPS
I/O0
I/O1
I/O2
I/O3
POWER DOWN (7C168)
COLUMN DECODER
CE
WE
A7 A8 A9 A10 A11

0021-1

Pin Configurations


A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
CE 9
GND 10
20 Vcc
19 A3
18 A2
17 A1
16 A0
15 I/O0
14 I/O1
13 I/O2
12 I/O3
11 WE

0021-2


A5 A4 Vcc A3
2 1 20 19
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
18 A2
17 A1
16 A0
15 I/O0
14 I/O1
13 I/O2
9 10 11 12
CE GND WE I/O3

0021-3

Selection Guide

			7C168-25 7C169-25	7C168-35 7C169-35	7C169-40	7C168-45
Maximum Access Time (ns)			25	35	40	45
Maximum Operating Current (mA)	L	Commercial	70	70		
	STD	Commercial	90	90	70	70
		Military		90	70	70

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 20 to Pin 10).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(Per MIL-STD-883 Method 3015.2)

Latch-up Current.......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C168L-25, -35 7C169L-25, -35		7C168-25, -35 7C169-25, -35		7C168-45 7C169-40		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		90		70	mA
			Military*				90		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		15		20		15	mA
			Military*				20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V	Commercial		11		11		11	mA
			Military*				20		20	

* −35 and −45 only

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

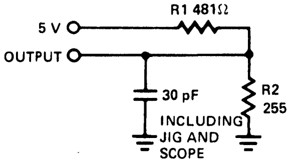


Figure 1a

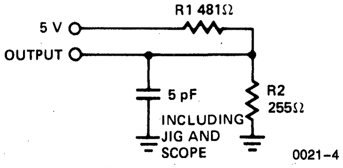


Figure 1b

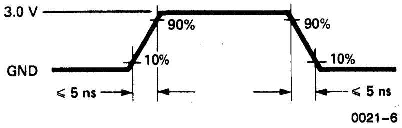
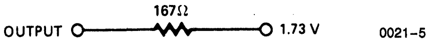


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[3]

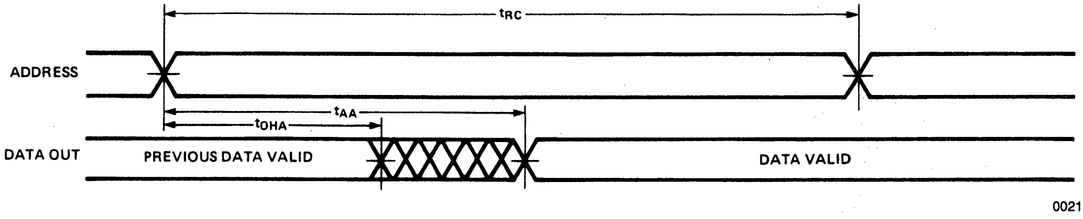
Parameters	Description		7C168-25 7C169-25		7C168-35 7C169-35		7C169-40		7C168-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
t_{RC}	Read Cycle Time		25		35		40		45		ns
t_{AA}	Address to Data Valid			25		35		40		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	7C168		25		35				45	ns
		7C169		15		25		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[5]		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4, 5]			15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)		0		0				0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down (7C168)			25		25				30	ns
t_{RCS}	Read Command Set-up		0		0		0		0		ns
t_{RCH}	Read Command Hold		0		0		0		0		ns
WRITE CYCLE[6]											
t_{WC}	Write Cycle Time		25		35		40		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		30		30		35		ns
t_{AW}	Address Set-up to Write End		20		30		40		35		ns
t_{HA}	Address Hold from Write End		0		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		20		30		35		35		ns
t_{SD}	Data Set-up to Write End		10		15		15		15		ns
t_{HD}	Data Hold from Write End		0		0		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]		6		6		6		6		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5]			10		15		20		20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CE} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

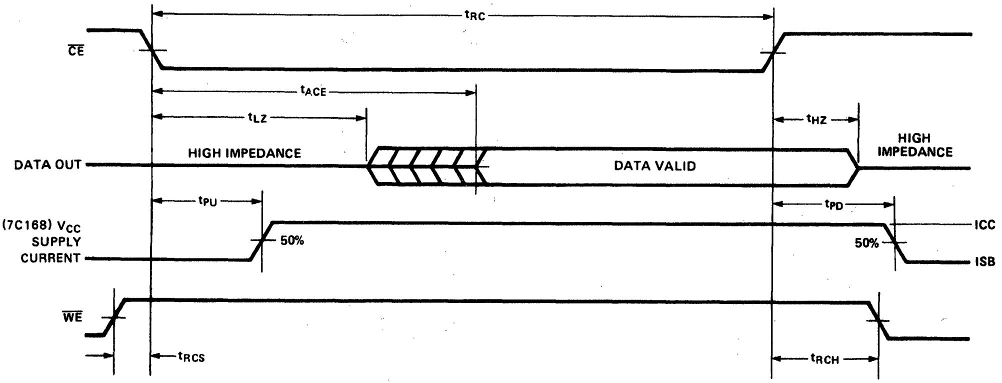
Switching Waveforms

Read Cycle No. 1 (Notes 7, 8)



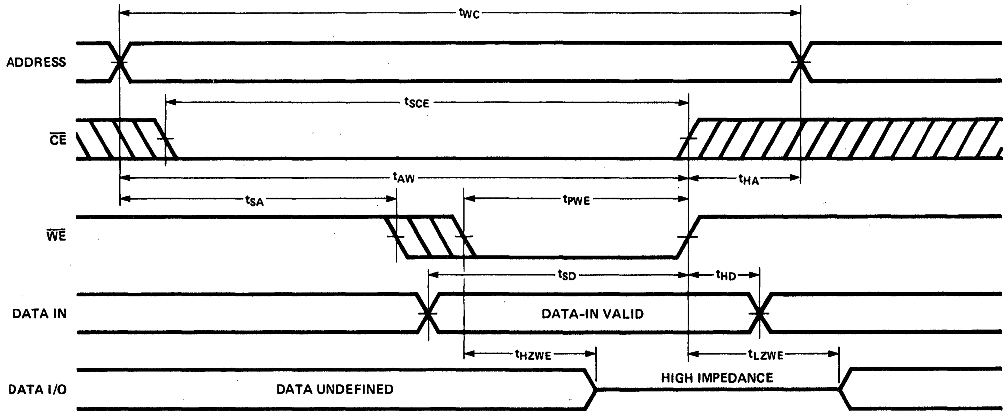
Switching Waveforms (Continued)

Read Cycle (Notes 7, 9)


t_{RC}
$\overline{CE}$
t_{ACE}
t_{LZ}
t_{HZ}
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
t_{PU}
t_{PD}
(7C168) V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB
$\overline{WE}$
t_{RCS}
t_{RCH}

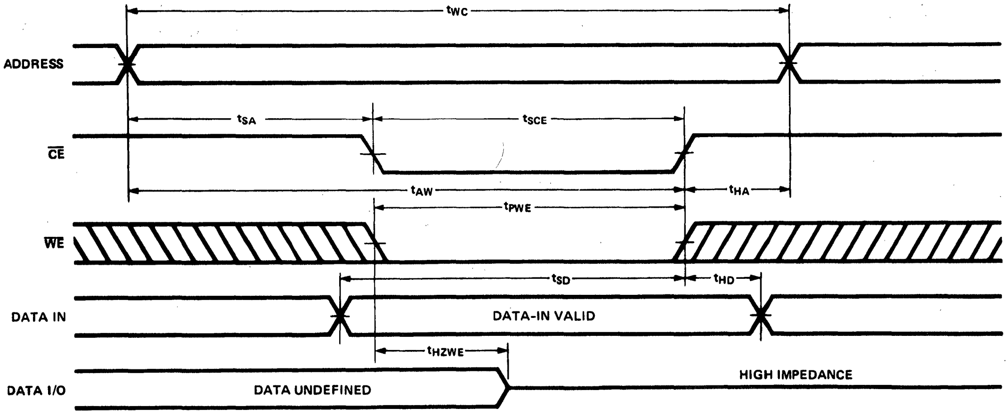
0021-8

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 6)


t_{WC}
ADDRESS
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0021-9

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 6)

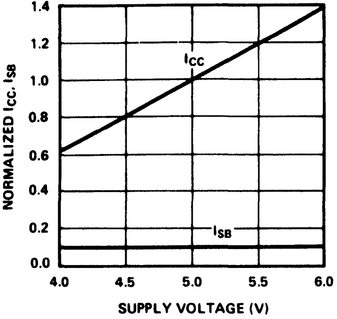

t_{WC}
ADDRESS
t_{SA}
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0021-10

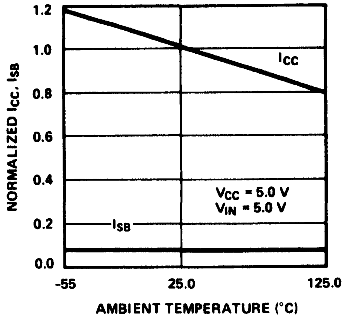
Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

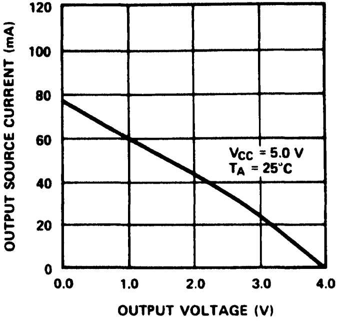
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



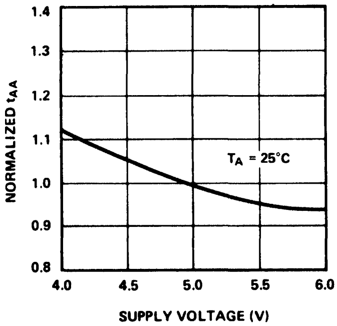
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



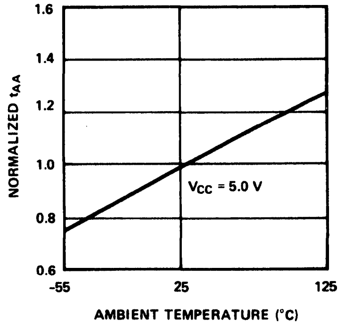
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



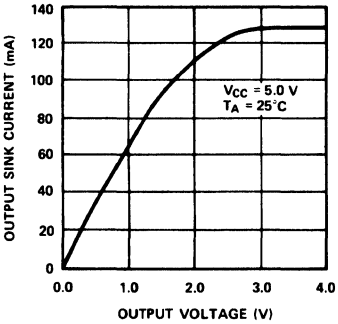
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



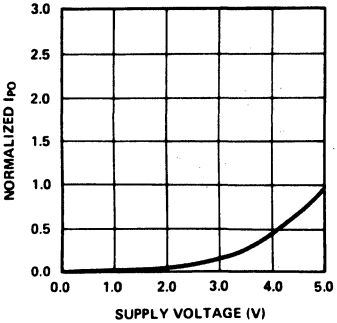
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



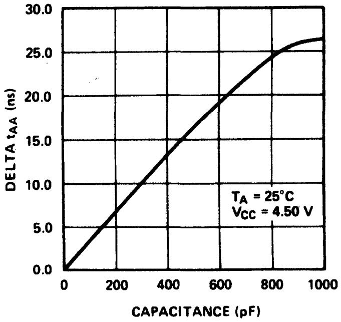
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



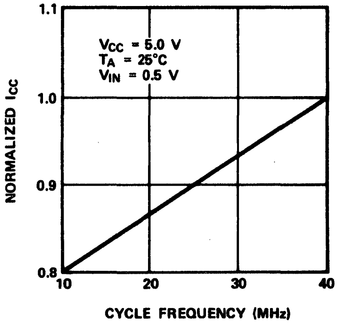
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0021-11

Ordering Information

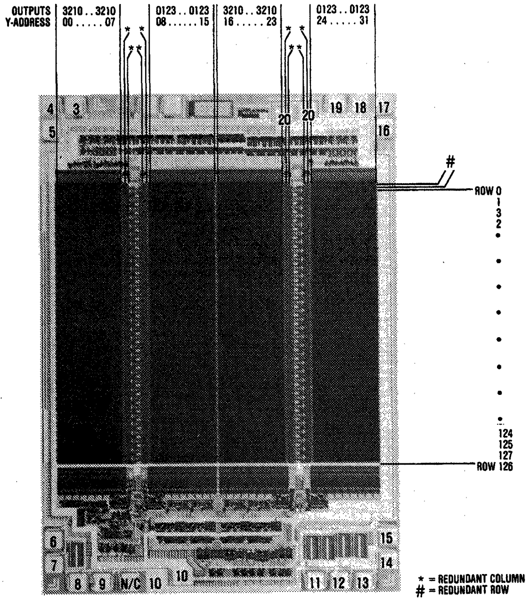
Speed (ns)	I_{CC} mA	Ordering Code	Package Type	Operating Range
25	70	CY7C168L-25PC	P5	Commercial
		CY7C168L-25DC	D6	
		CY7C168L-25LC	L51	
		CY7C168L-25SC	S5	
	90	CY7C168-25PC	P5	
		CY7C168-25DC	D6	
		CY7C168-25LC	L51	
		CY7C168-25SC	S5	
35	70	CY7C168L-35PC	P5	Commercial
		CY7C168L-35DC	D6	
		CY7C168L-35LC	L51	
		CY7C168L-35SC	S5	
	90	CY7C168-35PC	P5	
		CY7C168-35DC	D6	
		CY7C168-35LC	L51	
		CY7C168-35SC	S5	
		CY7C168-35DMB	D6	Military
		CY7C168-35LMB	L51	
45	70	CY7C168-45PC	P5	Commercial
		CY7C168-45DC	D6	
		CY7C168-45LC	L51	
		CY7C168-45SC	S5	
		CY7C168-45DMB	D6	Military
		CY7C168-45LMB	L51	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	16
A_1	X_3	17
A_2	X_4	18
A_3	X_1	19
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

Speed (ns)	I_{CC} mA	Ordering Code	Package Type	Operating Range
25	60	CY7C169L-25PC	P5	Commercial
		CY7C169L-25DC	D6	
		CY7C169L-25LC	L51	
	90	CY7C169-25PC	P5	
		CY7C169-25DC	D6	
		CY7C169-25LC	L51	
35	60	CY7C169L-35PC	P5	Commercial
		CY7C169L-35DC	D6	
		CY7C169L-35LC	L51	
	90	CY7C169-35PC	P5	
		CY7C169-35DC	D6	
		CY7C169-35LC	L51	
		CY7C169-35DMB	D6	Military
		CY7C169-35LMB	L51	
40	70	CY7C169-40PC	P5	Commercial
		CY7C169-40DC	D6	
		CY7C169-40LC	L51	
		CY7C169-40DMB	D6	Military
		CY7C169-40LMB	L51	

Bit Map


OUTPUTS
Y-ADDRESS
3210 . . 3210
00 07
0123 . . 0123
08 15
3210 . . 3210
16 23
0123 . . 0123
24 31
*
**
4
3
5
20
20
19
18
17
16
#
ROW 0
1
3
2
124
125
127
ROW 126
6
7
8
9
N/C
10
10
11
12
13
14
15
* = REDUNDANT COLUMN
# = REDUNDANT ROW

0021–12

CYPRESS
SEMICONDUCTOR

CY7C170

4096 x 4 Static R/W RAM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns t_{AA}**
  - **— 15 ns t_{ACE}**
- **Low active power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Output enable**

Functional Description

The CY7C170 is a high performance CMOS static RAM organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$), and three-state drivers.

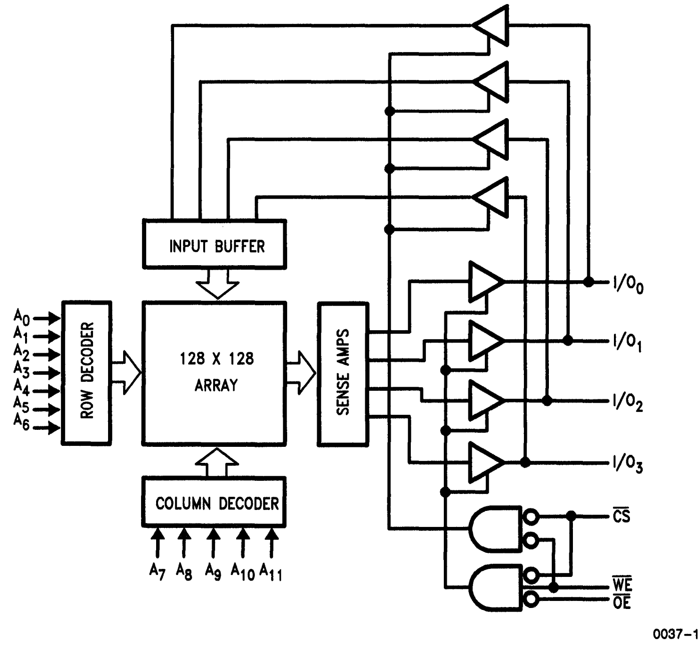
Writing to the device is accomplished when the chip enable ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

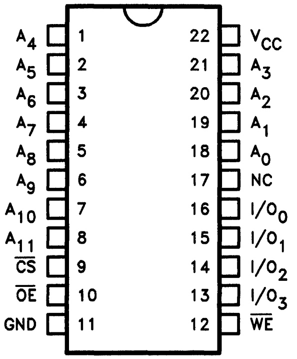
A die coat is used to insure alpha immunity.

Logic Block Diagram


INPUT BUFFER
A_0
A_1
A_2
A_3
A_4
A_5
A_6
ROW DECODER
128 X 128
ARRAY
SENSE AMPS
COLUMN DECODER
A_7 A_8 A_9 A_{10} A_{11}
I/O_0
I/O_1
I/O_2
I/O_3
$\overline{CS}$
$\overline{WE}$
$\overline{OE}$

0037-1

Pin Configuration


A_4 1
A_5 2
A_6 3
A_7 4
A_8 5
A_9 6
A_{10} 7
A_{11} 8
$\overline{CS}$ 9
$\overline{OE}$ 10
GND 11
22 V_{CC}
21 A_3
20 A_2
19 A_1
18 A_0
17 NC
16 I/O_0
15 I/O_1
14 I/O_2
13 I/O_3
12 $\overline{WE}$

0037-2

Selection Guide

		7C170-25*	7C170-35	7C170-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120

*Preliminary

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

Output Current into Outputs (Low) . . . . 20 mA

Static Discharge Voltage . . . . >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C170 Min.	7C170 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	μA
I_{OS}	Output Short[1] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90	mA
			Military		120	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

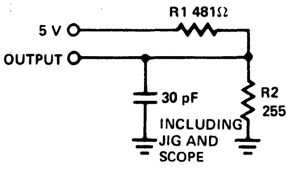

R1 481Ω
5 V
OUTPUT
30 pF
INCLUDING JIG AND SCOPE
R2 255Ω

Figure 1a

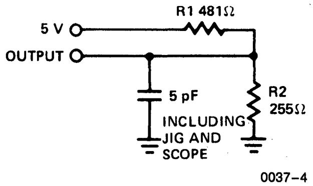

R1 481Ω
5 V
OUTPUT
5 pF
INCLUDING JIG AND SCOPE
R2 255Ω
0037-4

Figure 1b

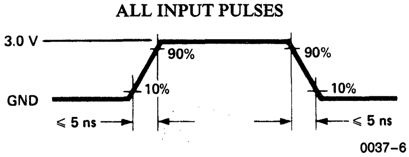
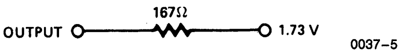

ALL INPUT PULSES
3.0 V
GND
90%
90%
10%
10%
≤ 5 ns
≤ 5 ns
0037-6

Figure 2

Equivalent to:

THÉVENIN EQUIVALENT


167Ω
OUTPUT
1.73 V
0037-5

Switching Characteristics Over Operating Range[3]

Parameters	Description	7C170-25*		7C170-35		7C170-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{\text{CS}}$ Low to Data Valid		15		25		30	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		15		15		20	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[4]		15		15		15	ns
t_{LZCS}	$\overline{\text{CS}}$ LOW to Low Z[5]	3		5		5		ns
t_{HZCS}	$\overline{\text{CE}}$ HIGH to High Z[4, 5]		15		20		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCS}	$\overline{\text{CS}}$ LOW to Write End	25		35		35		ns
t_{AW}	Address Set-up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	20		30		35		ns
t_{SD}	Data Set-up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z		10		15		20	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	6		6		6		ns

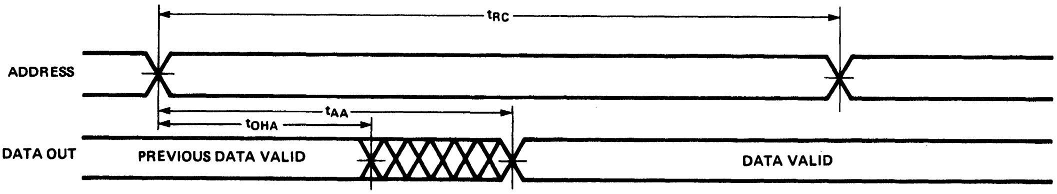
*Preliminary

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZOE}, t_{HZCS} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for all devices. These parameters are sampled and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{\text{WE}}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$ and $\overline{\text{OE}} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
10. Data I/O will be high impedance if $\overline{\text{OE}} = V_{IH}$.

Switching Waveforms

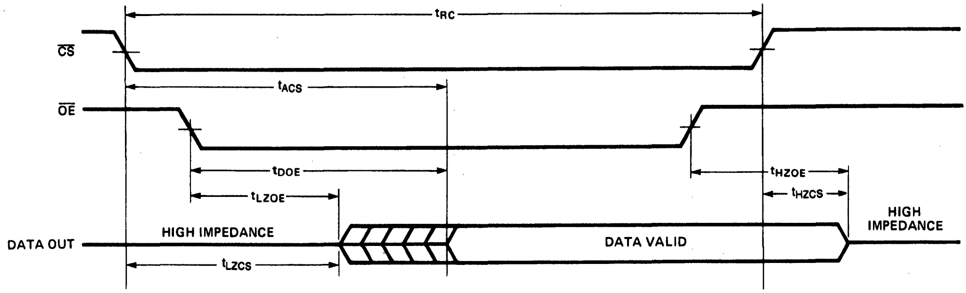
Read Cycle No. 1 (Notes 7, 8)



0037-11

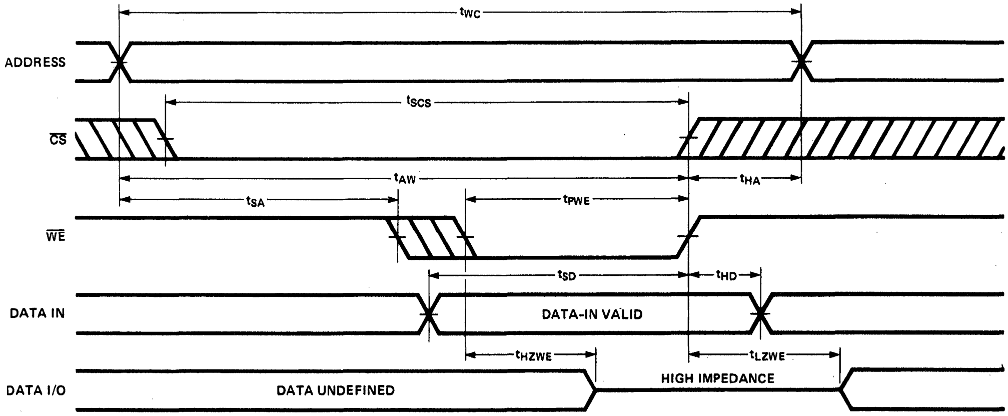
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 7, 9)


t_{RC}
$\overline{CS}$
t_{ACS}
$\overline{OE}$
t_{DOE}
t_{LZOE}
t_{HZOE}
t_{HZCS}
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
DATA OUT
t_{LZCS}

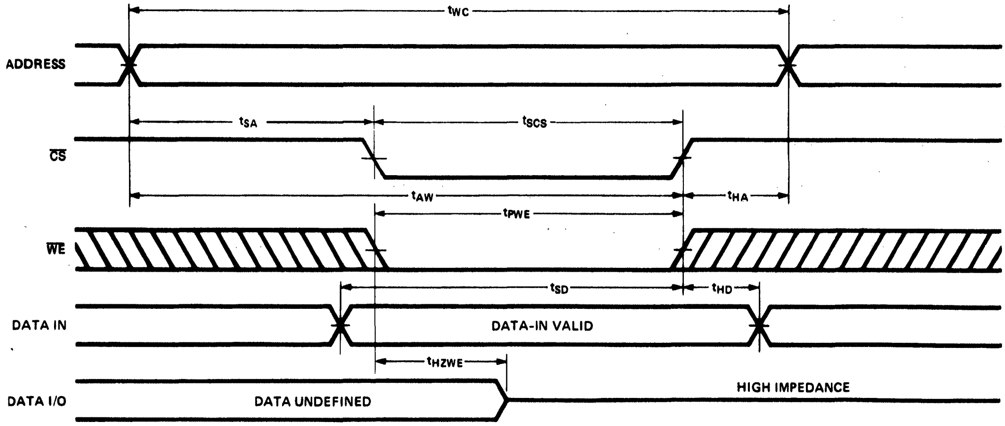
0037-7

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SCS}
$\overline{CS}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0037-8

Write Cycle No. 2 ($\overline{CS}$ Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SA}
t_{SCS}
$\overline{CS}$
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0037-9

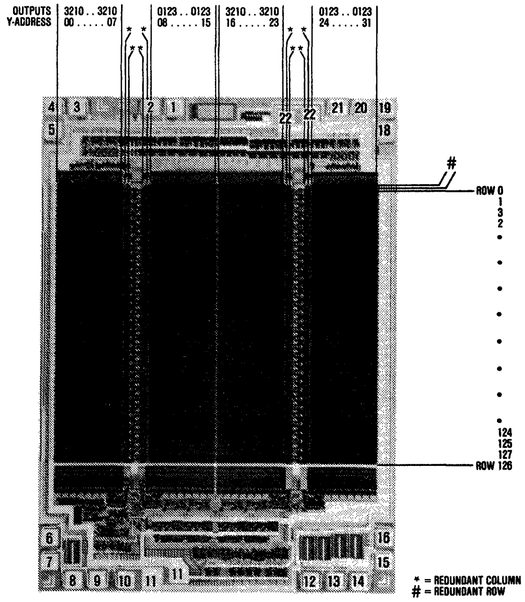
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25*	CY7C170-25PC	P9	Commercial
	CY7C170-25DC	D10	
35	CY7C170-35PC	P9	Commercial
	CY7C170-35DC	D10	
	CY7C170-35DMB	D10	Military
45	CY7C170-45PC	P9	Commercial
	CY7C170-45DC	D10	
	CY7C170-45DMB	D10	Military

*Preliminary

Bit Map


OUTPUTS
Y-ADDRESS
3210 . . 3210
00 07
0123 . . 0123
08 15
3210 . . 3210
16 23
0123 . . 0123
24 31
* *
* *
* *
* *
4
3
2
1
22
22
21
20
19
5
18
#
ROW 0
1
3
2
124
125
127
ROW 126
6
7
8
9
10
11
11
12
13
14
15
16
* = REDUNDANT COLUMN
# = REDUNDANT ROW

0037-10

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	18
A_1	X_3	19
A_2	X_4	20
A_3	X_1	21
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

CYPRESS SEMICONDUCTOR

CY7C171
CY7C172

4096 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High Speed**
  - **25 ns t_{AA}**
- **Transparent Write (7C171)**
- **Low active power**
  - **385 mW (commercial)**
  - **385 mW (military)**
- **Low standby power**
  - **83 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

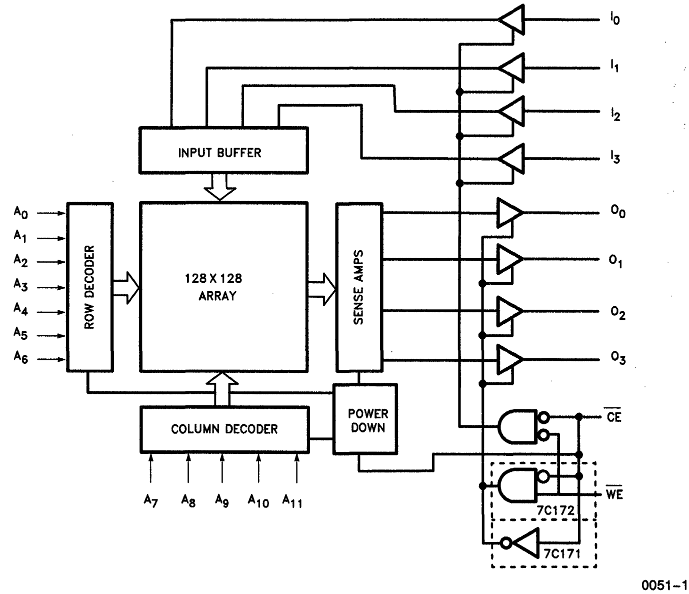
The CY7C171 and CY7C172 are high performance CMOS static RAMs organized as 4096 x 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

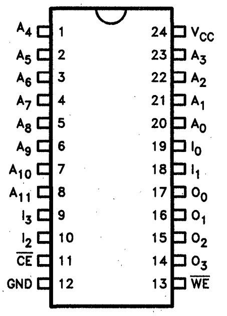
The output pins stay in high impedance state when write enable ($\overline{WE}$) is LOW (7C172 only), or chip enable ($\overline{CE}$) is HIGH. A die coat is used to insure alpha immunity.

Logic Block Diagram

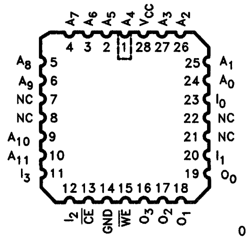

I0
I1
I2
I3
INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
ROW DECODER
128 X 128
ARRAY
SENSE AMPS
O0
O1
O2
O3
POWER DOWN
COLUMN DECODER
A7
A8
A9
A10
A11
CE
WE
7C172
7C171

0051-1

Pin Configurations


A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
I3 9
I2 10
CE 11
GND 12
24 VCC
23 A3
22 A2
21 A1
20 A0
19 I0
18 I1
17 O0
16 O1
15 O2
14 O3
13 WE

0051-2


A7 A6 A5 A4 VCC A3 A2
4 3 2 1 28 27 26
A8 5
A9 6
NC 7
NC 8
A10 9
A11 10
I3 11
25 A1
24 A0
23 I0
22 NC
21 NC
20 I1
19 O0
12 13 14 15 16 17 18
I2 CE GND WE O3 O2 O1

0051-3

Selection Guide

			7C171-25 7C172-25	7C171-35 7C172-35	7C171-45 7C172-45
Maximum Access Time (ns)			25	35	45
Maximum Operating Current (mA)	L	Commercial	70	70	
	STD	Commercial	90	90	70
		Military		90	70

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current.......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C171L-25, -35 7C172L-25, -35		7C171-25, -35 7C172-25, -35		7C171-45 7C172-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		90		70	mA
			Military*				90		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		15		20		15	mA
			Military*				20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} −0.3V	Commercial		10		15		15	mA
			Military*				20		20	

*-35 and -45 only

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

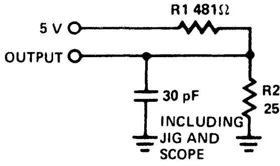


Figure 1a

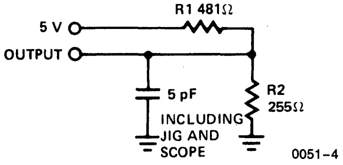


Figure 1b

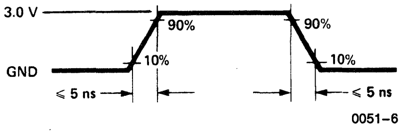
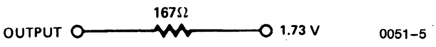


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[3]

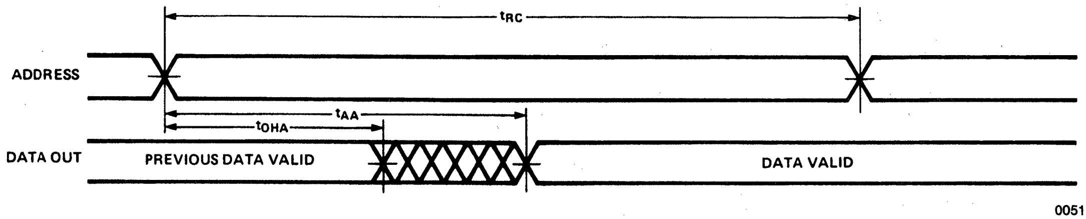
Parameters	Description	7C171-25 7C172-25		7C171-35 7C172-35		7C171-45 7C172-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[5]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[4, 5]		15		20		20	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		25		25		30	ns
t_{RCS}	Read Command Set-up	0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	25		30		35		ns
t_{AW}	Address Set-up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[5] (7C172)	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[4, 5] (7C172)		10		15		20	ns
t_{AWE}	$\overline{\text{WE}}$ LOW to Data Valid (7C171)		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171)		25		30		35	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. These parameters are specified and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ low and $\overline{\text{WE}}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{\text{WE}}$ is high for read cycle.
8. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{\text{CE}}$ transition low.

Switching Waveforms

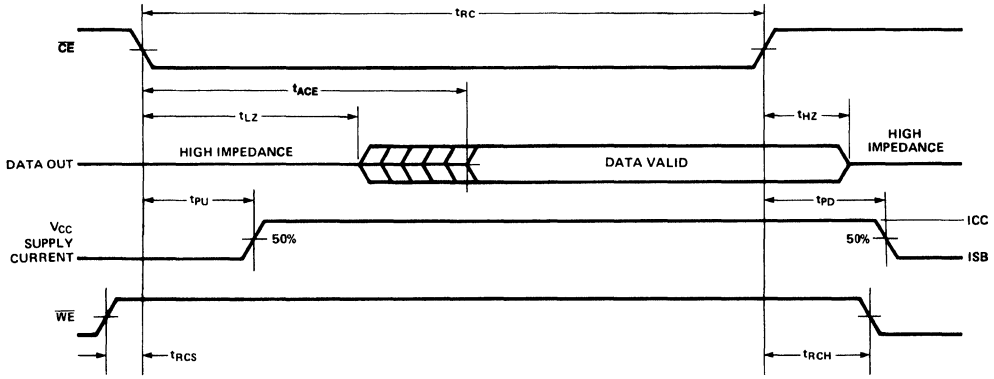
Read Cycle No. 1 (Notes 7, 8)



0051-7

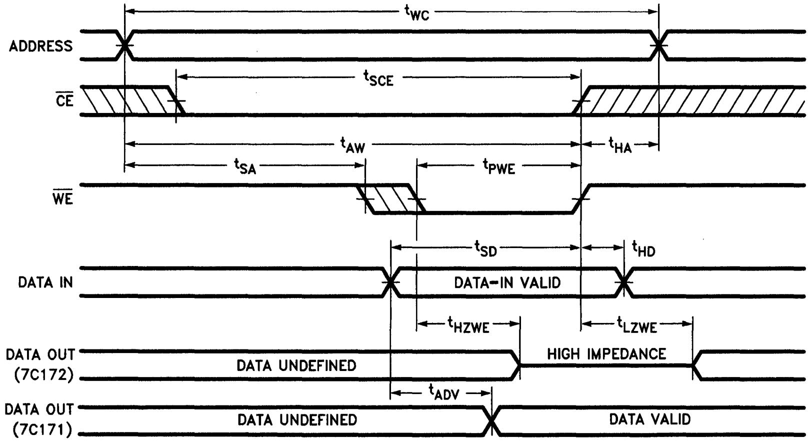
Switching Waveforms (Continued)

Read Cycle (Notes 7, 9)


tRC
CE
tACE
tLZ
tHZ
DATA OUT
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB
WE
tRCS
tRCH

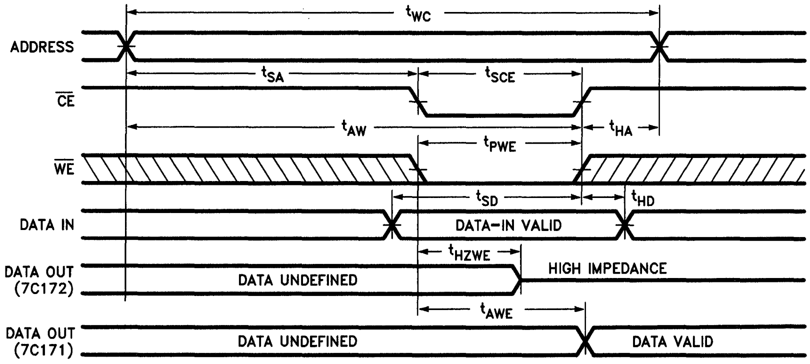
0051-8

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Note 6)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA OUT (7C172)
DATA UNDEFINED
HIGH IMPEDANCE
tADV
DATA OUT (7C171)
DATA UNDEFINED
DATA VALID

0051-9

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) (Note 6)

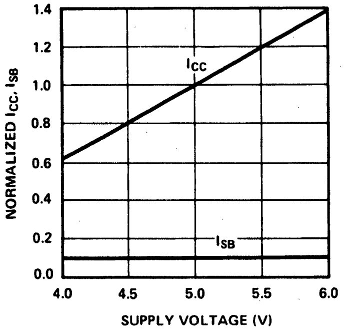

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA OUT (7C172)
DATA UNDEFINED
HIGH IMPEDANCE
tAWE
DATA OUT (7C171)
DATA UNDEFINED
DATA VALID

0051-10

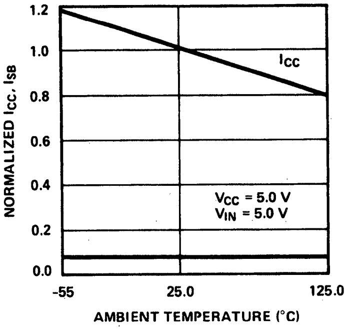
Note: If $\overline{\text{CE}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance state (7C172).

Typical DC and AC Characteristics

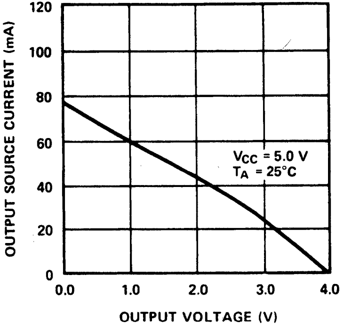
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



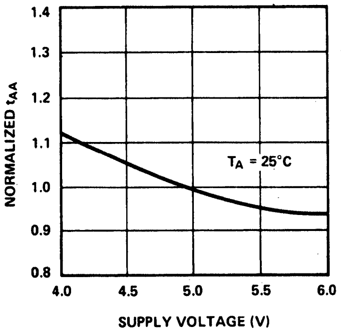
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



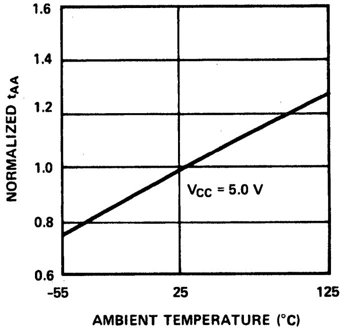
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



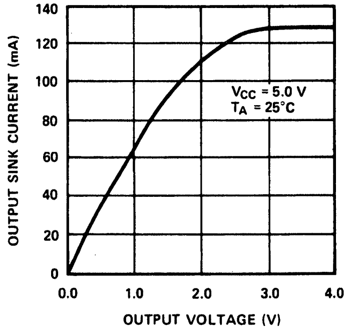
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



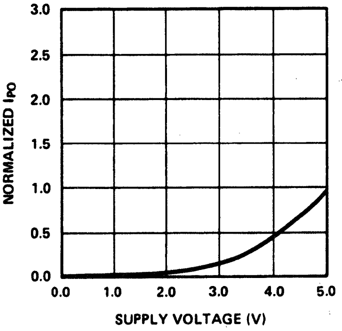
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



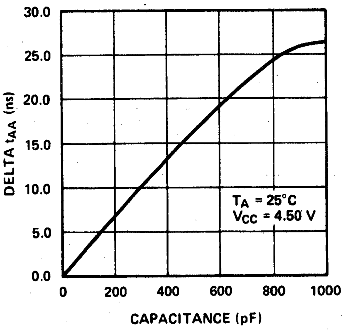
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



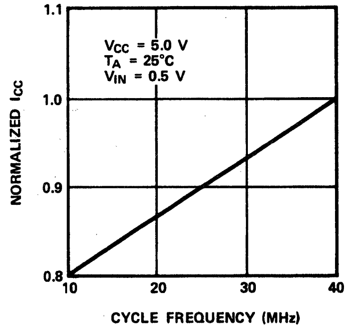
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0051-11

Ordering Information

Speed (ns)	I_{CC} mA	Ordering Code	Package Type	Operating Range
25	70	CY7C171L-25PC	P13	Commercial
		CY7C171L-25DC	D14	
		CY7C171L-25LC	L64	
	90	CY7C171-25PC	P13	
		CY7C171-25DC	D14	
		CY7C171-25LC	L64	
35	70	CY7C171L-35PC	P13	Commercial
		CY7C171L-35DC	D14	
		CY7C171L-35LC	L64	
	90	CY7C171-35PC	P13	
		CY7C171-35DC	D14	
		CY7C171-35LC	L64	
		CY7C171-35DMB	D14	Military
		CY7C171-35LMB	L64	
45	70	CY7C171-45PC	P13	Commercial
		CY7C171-45DC	D14	
		CY7C171-45LC	L64	
		CY7C171-45DMB	D14	Military
		CY7C171-45LMB	L64	

Speed (ns)	I_{CC} mA	Ordering Code	Package Type	Operating Range
25	70	CY7C172L-25PC	P13	Commercial
		CY7C172L-25DC	D14	
		CY7C172L-25LC	L64	
	90	CY7C172-25PC	P13	
		CY7C172-25DC	D14	
		CY7C172-25LC	L64	
35	70	CY7C172L-35PC	P13	Commercial
		CY7C172L-35DC	D14	
		CY7C172L-35LC	L64	
	90	CY7C172-35PC	P13	
		CY7C172-35DC	D14	
		CY7C172-35LC	L64	
		CY7C172-35DMB	D14	Military
		CY7C172-35LMB	L64	
45	70	CY7C172-45PC	P13	Commercial
		CY7C172-45DC	D14	
		CY7C172-45LC	L64	
		CY7C172-45DMB	D14	Military
		CY7C172-45LMB	L64	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	20
A_1	X_3	21
A_2	X_4	22
A_3	X_1	23
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

CYPRESS
SEMICONDUCTOR

CY7C185
CY7C186

8192 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/ power**
- **High speed—35 ns**
- **Low active power — 550 mW**
- **Low standby power — 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**
- **2V data retention (L version)**

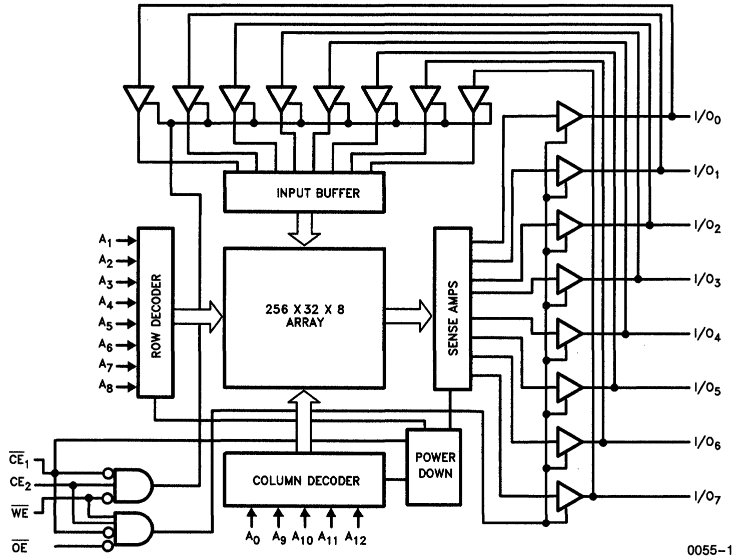
Functional Description

The CY7C185 and CY7C186 are high performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by 73% when deselected. The CY7C185 is in the space saving 300 mil wide DIP package and leadless chip carrier. The CY7C186 is in the standard 600 mil wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/ output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE_1}$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/ output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

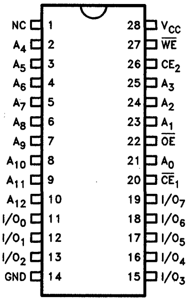
Logic Block Diagram



INPUT BUFFER
256 X 32 X 8 ARRAY
ROW DECODER
SENSE AMPS
COLUMN DECODER
POWER DOWN
A1
A2
A3
A4
A5
A6
A7
A8
CE1
CE2
WE
OE
A0 A9 A10 A11 A12
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7

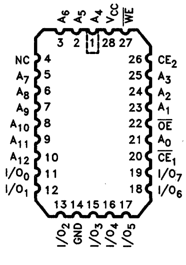
0055-1

Pin Configurations



NC 1
A4 2
A5 3
A6 4
A7 5
A8 6
A9 7
A10 8
A11 9
A12 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 CE2
25 A3
24 A2
23 A1
22 OE
21 A0
20 CE1
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3

0055-2



A6 A5 A4 VCC WE
3 2 1 28 27
NC 4
A7 5
A8 6
A9 7
A10 8
A11 9
A12 10
I/O0 11
I/O1 12
26 CE2
25 A3
24 A2
23 A1
22 OE
21 A0
20 CE1
19 I/O7
18 I/O6
13 14 15 16 17
I/O2 GND I/O3 I/O4 I/O5

0055-3

Selection Guide

		7C185-35 7C186-35	7C185-45 7C186-45	7C185-55 7C186-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	100	100	80
	Military		100	100
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C185-35 7C186-35		7C185-45 7C186-45		7C185-55 7C186-55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		100		100		80	mA
			Military				100		100	
I_{SB_1}	Automatic $\overline{CE_1}$ Power Down Current	Max. V_{CC}, $\overline{CE_1}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military				20		20	
I_{SB_2}	Automatic $\overline{CE_1}$ Power Down Current	Max. V_{CC}, $\overline{CE_1}$ ≥ V_{CC}−0.3V, V_{IN} ≥ V_{CC}−0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on sample basis.

AC Test Loads and Waveforms

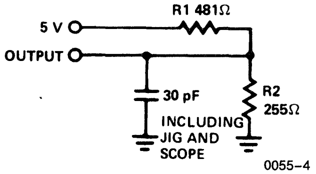


Figure 1a

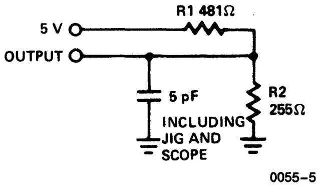


Figure 1b

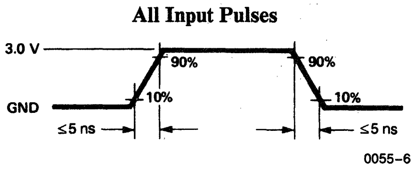
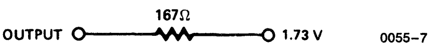


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[3]

Parameters	Description	7C185-35 7C186-35		7C185-45 7C186-45		7C185-55 7C186-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE_1}	$\overline{CE_1}$ LOW to Data Valid		35		45		55	ns
t_{ACE_2}	CE_2 HIGH to Data Valid		25		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4]		20		25		30	ns
t_{LZCE_1}	$\overline{CE_1}$ LOW to Low Z[5]	5		5		5		ns
T_{LZCE_2}	CE_2 HIGH to Low Z	3		3		3		ns
t_{HZCE}	$\overline{CE_1}$ HIGH to High Z[4, 5] CE_2 LOW to High Z		15		20		20	ns
t_{PU}	$\overline{CE_1}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE_1}$ HIGH to Power Down		20		25		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		50		ns
t_{SCE_1}	$\overline{CE_1}$ LOW to Write End	30		40		50		ns
t_{SCE_2}	CE_2 HIGH to Write End	20		25		30		ns
t_{AW}	Address Set-up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	20		25		30		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$. $CE_2 = V_{IH}$.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
10. Data I/O is HIGH impedance if $\overline{OE} = V_{IH}$.

Data Retention Characteristics (L Version only)

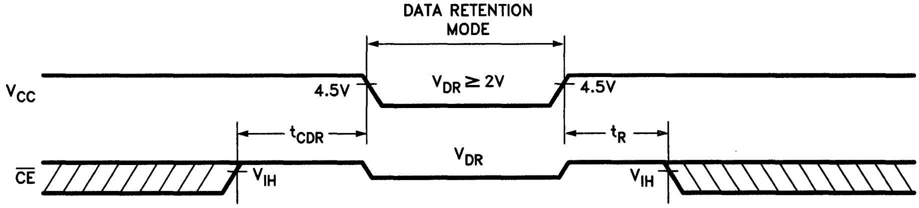
Parameters	Description	Test Conditions	Min.	Max.	Units
V_{DR}	V_{CC} for Retention of Data	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	V
I_{CCDR}	Data Retention Current		—	1000	μA
t_{CDR}[12]	Chip Deselect to Data Retention Time		0	—	ns
t_R[12]	Operation Recovery Time		t_{RC}[11]	—	ns
I_{LI}[12]	Input Leakage Current		—	2	μA

Notes:

11. t_{RC} = Read Cycle Time.

12. Guaranteed, not tested.

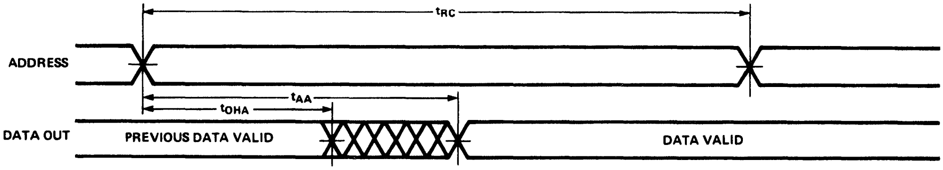
Data Retention Waveform


DATA RETENTION
MODE
V_{CC}
4.5V
$V_{DR} \geq 2V$
4.5V
t_{CDR}
t_R
V_{DR}
$\overline{CE}$
V_{IH}
V_{IH}

0055-12

Switching Waveforms

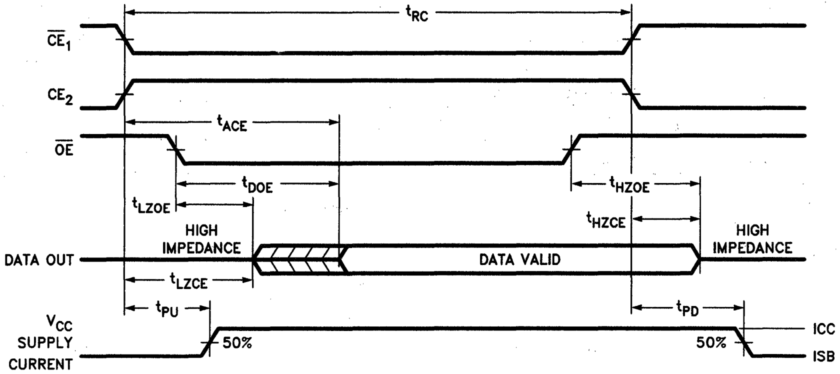
Read Cycle No. 1 (Notes 8, 9)


t_{RC}
ADDRESS
t_{AA}
t_{OHA}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

0055-8

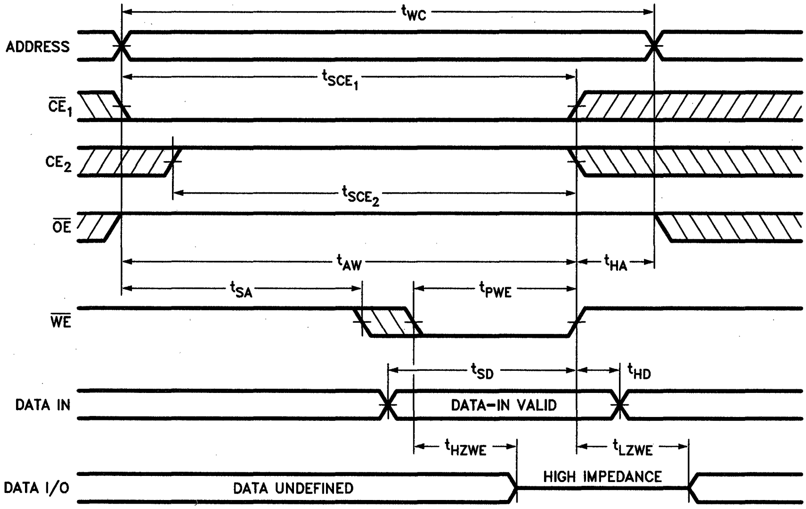
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 7, 9)


t_{RC}
$\overline{CE}_1$
CE_2
t_{ACE}
$\overline{OE}$
t_{DOE}
t_{HZOE}
t_{LZOE}
t_{HZCE}
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
t_{LZCE}
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

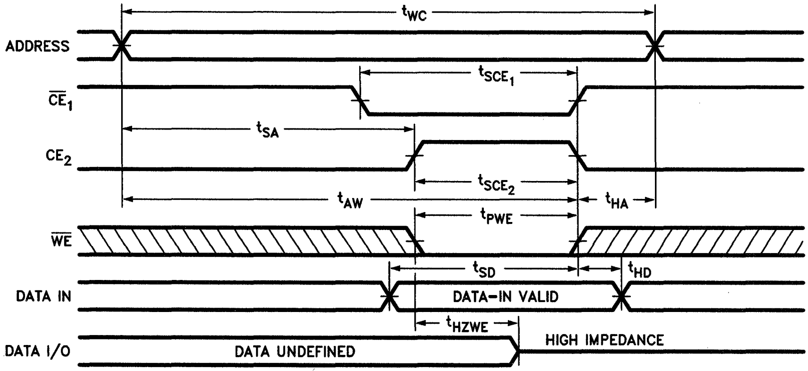
0055-9

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SCE_1}
$\overline{CE}_1$
CE_2
t_{SCE_2}
$\overline{OE}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

0055-10

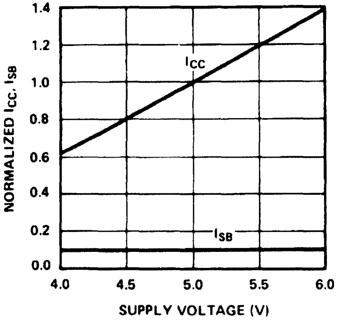
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SCE_1}
$\overline{CE}_1$
t_{SA}
CE_2
t_{SCE_2}
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
HIGH IMPEDANCE
DATA I/O
DATA UNDEFINED

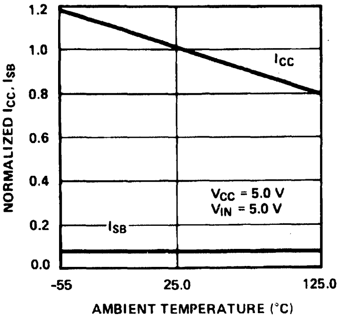
0055-11

Note: If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state.

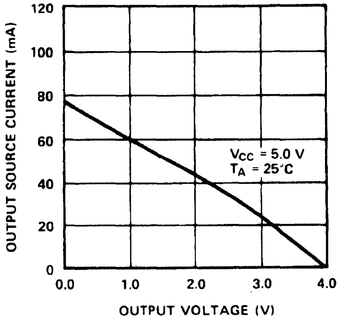
Typical DC and AC Characteristics



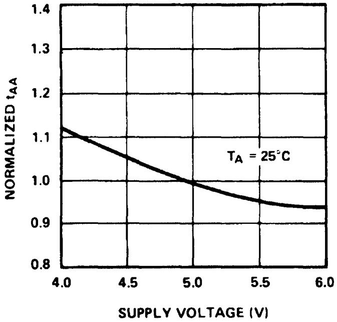
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



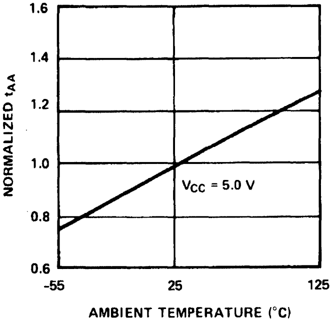
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



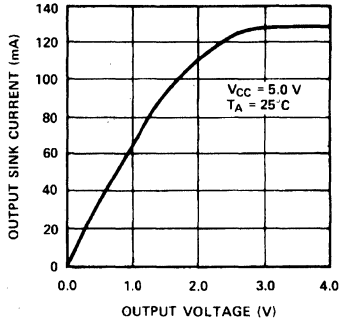
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



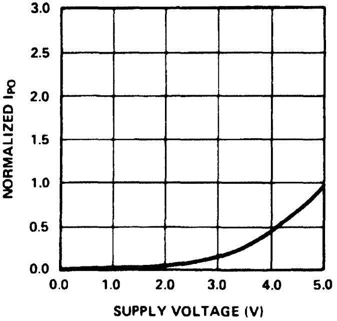
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



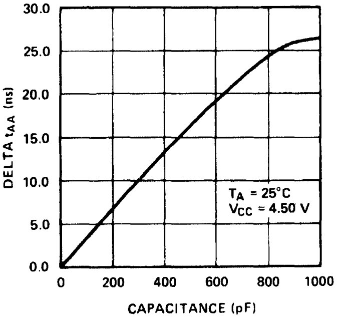
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



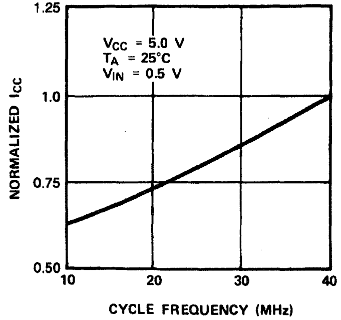
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME

0055-13

Truth Table

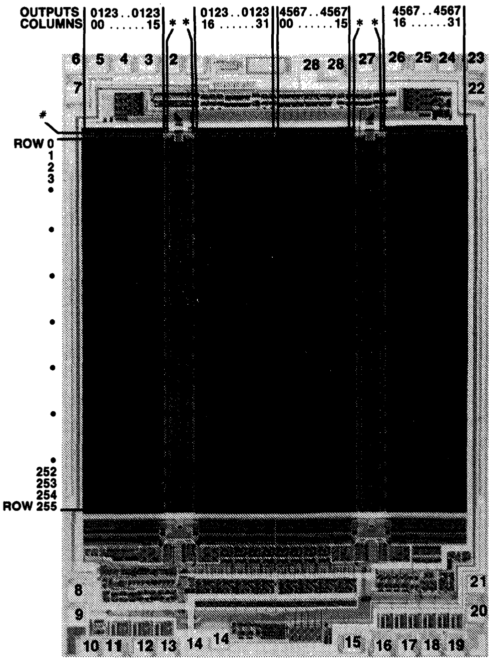
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	X	High Z	Deselect Power Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C185-35PC	P21	Commercial
	CY7C185L-35PC	P21	
	CY7C185-35DC	D22	
	CY7C185L-35DC	D22	
45	CY7C185-45PC	P21	Commercial
	CY7C185L-45PC	P21	
	CY7C185-45DC	D22	
	CY7C185L-45DC	D22	
	CY7C185-45LC	L54	
	CY7C185L-45LC	L54	
	CY7C185-45DMB	D22	Military
	CY7C185L-45DMB	D22	
	CY7C185-45LMB	L54	
	CY7C185L-45LMB	L54	
55	CY7C185-55PC	P21	Commercial
	CY7C185L-55PC	P21	
	CY7C185-55DC	D22	
	CY7C185L-55DC	D22	
	CY7C185-55LC	L54	
	CY7C185L-55LC	L54	
	CY7C185-55DMB	D22	Military
	CY7C185L-55DMB	D22	
	CY7C185-55LMB	L54	
	CY7C185L-55LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C186-35PC	P15	Commercial
	CY7C186L-35PC	P15	
	CY7C186-35DC	D16	
	CY7C186L-35DC	D16	
45	CY7C186-45PC	P15	Commercial
	CY7C186L-45PC	P15	
	CY7C186-45DC	D16	
	CY7C186L-45DC	D16	
	CY7C186-45DMB	D16	Military
	CY7C186L-45DMB	D16	
55	CY7C186-55PC	P15	Commercial
	CY7C186L-55PC	P15	
	CY7C186-55DC	D16	
	CY7C186L-55DC	D16	
	CY7C186-55DMB	D16	Military
	CY7C186L-55DMB	D16	

Bit Map


OUTPUTS
COLUMNS
0123..0123
00......15
* *
0123..0123
16......31
4567..4567
00......15
* *
4567..4567
16......31
6 5 4 3 2
28 28 27 26 25 24 23
7
22
#
ROW 0
1
2
3
252
253
254
ROW 255
8
9
21
20
10 11 12 13 14 14 15 16 17 18 19

0055-14

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

CYPRESS SEMICONDUCTOR

CY7C187

65,536 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power — 385 mW**
- **Low standby power — 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**
- **2V data retention (L version)**

Functional Description

The CY7C187 is a high performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

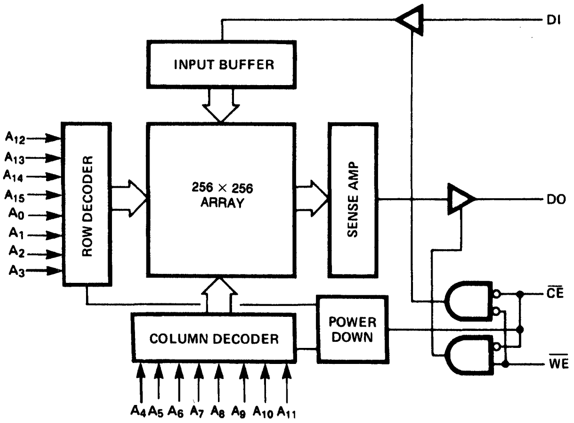
Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

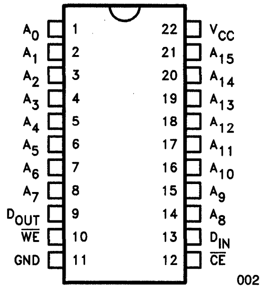
The 7C187 utilizes a Die Coat to ensure alpha immunity.

Logic Block Diagram

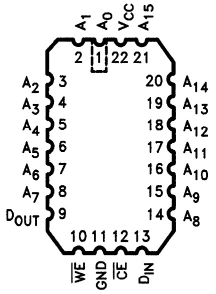

DI
INPUT BUFFER
A12
A13
A14
A15
A0
A1
A2
A3
ROW DECODER
256 × 256 ARRAY
SENSE AMP
DO
$\overline{CE}$
$\overline{WE}$
POWER DOWN
COLUMN DECODER
A4 A5 A6 A7 A8 A9 A10 A11

0029-1

Pin Configurations


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
DOUT 9
$\overline{WE}$ 10
GND 11
22 VCC
21 A15
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
13 DIN
12 $\overline{CE}$

0029-2


A1 A0 VCC A15
2 1 22 21
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
DOUT 9
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
10 11 12 13
$\overline{WE}$ GND $\overline{CE}$ DIN

0029-3

Selection Guide

		7C187-25	7C187-35	7C187-45
Maximum Access Time (ns)	Commercial	25	35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11)................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage ....>2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..........................>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions			7C187-25		7C187-35		7C187-45		Units
					Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Military		0.4		0.4		0.4	V
			I_{OL} = 12.0 mA	Commercial							
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND				−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Commercial		70		70		50	mA
				Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		Commercial		20		20		20	mA
				Military				20		20	
I_{SB_2}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		Commercial		20		20		20	mA
				Military				20		20	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

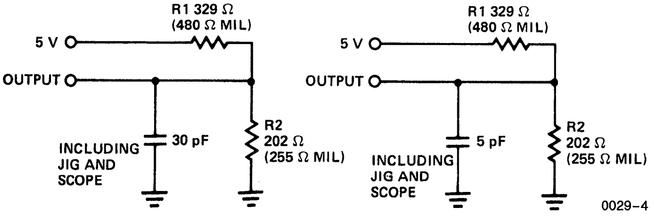

R1 329 Ω
(480 Ω MIL)
5 V
OUTPUT
INCLUDING JIG AND SCOPE
30 pF
R2
202 Ω
(255 Ω MIL)
R1 329 Ω
(480 Ω MIL)
5 V
OUTPUT
INCLUDING JIG AND SCOPE
5 pF
R2
202 Ω
(255 Ω MIL)
0029-4

Figure 1a Figure 1b

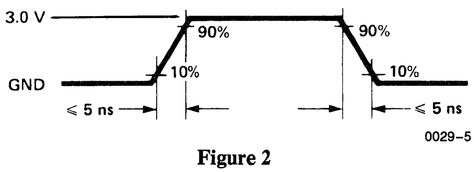
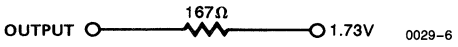
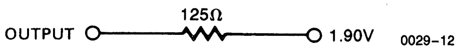

3.0 V
GND
90%
90%
10%
10%
≤ 5 ns
≤ 5 ns
0029-5

Figure 2

Equivalent to: THÉVENIN EQUIVALENT


OUTPUT
167Ω
1.73V
0029-6

Military


OUTPUT
125Ω
1.90V
0029-12

Commercial

Switching Characteristics Over Operating Range[4]

Parameters	Description	7C187-25		7C187-35		7C187-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[5, 6]	0	15	0	20	0	20	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[6]	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[5, 6]	0	15	0	20	0	20	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{\text{WE}}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Data Retention Characteristics (L Version only)

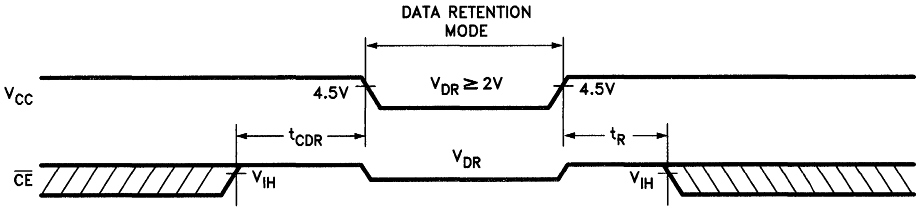
Parameters	Description	Test Conditions	CY7C187		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	V
I_{CCDR}	Data Retention Current		—	1000	μA
t_{CDR}[12]	Chip Deselect to Data Retention Time		0	—	ns
t_R[12]	Operation Recovery Time		t_{RC}[11]	—	ns
I_{LI}[12]	Input Leakage Current		—	2	μA

Notes:

11. t_{RC} = read cycle time.

12. Guaranteed, not tested.

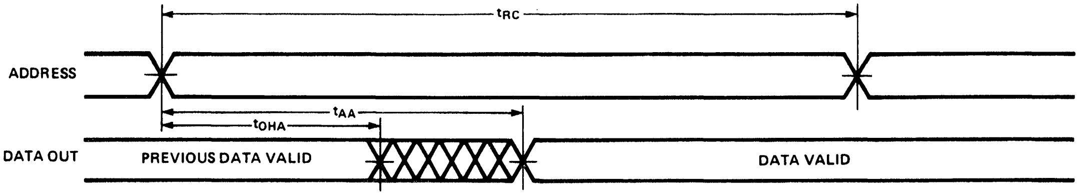
Data Retention Waveform


DATA RETENTION MODE
V_{CC}
4.5V
$V_{DR} \geq 2V$
4.5V
t_{CDR}
t_R
V_{DR}
$\overline{CE}$
V_{IH}
V_{IH}

0029-13

Switching Waveforms

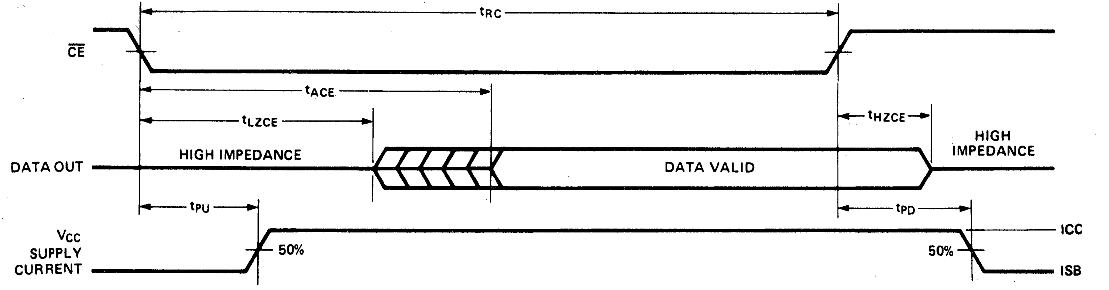
Read Cycle No. 1[8, 9]


t_{RC}
ADDRESS
t_{AA}
t_{OHA}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

0029-7

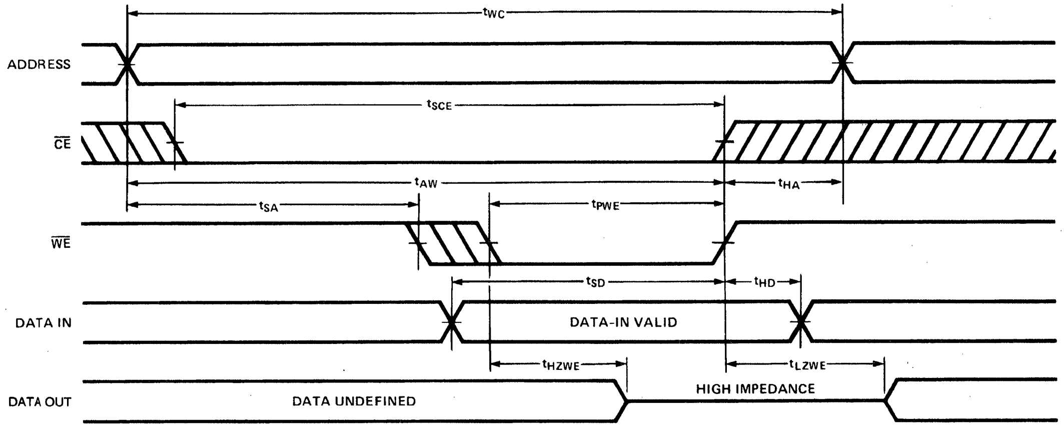
Switching Waveforms (Continued)

Read Cycle No. 2[9, 11]


tRC
CE
tACE
tLZCE
tHZCE
DATA OUT
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

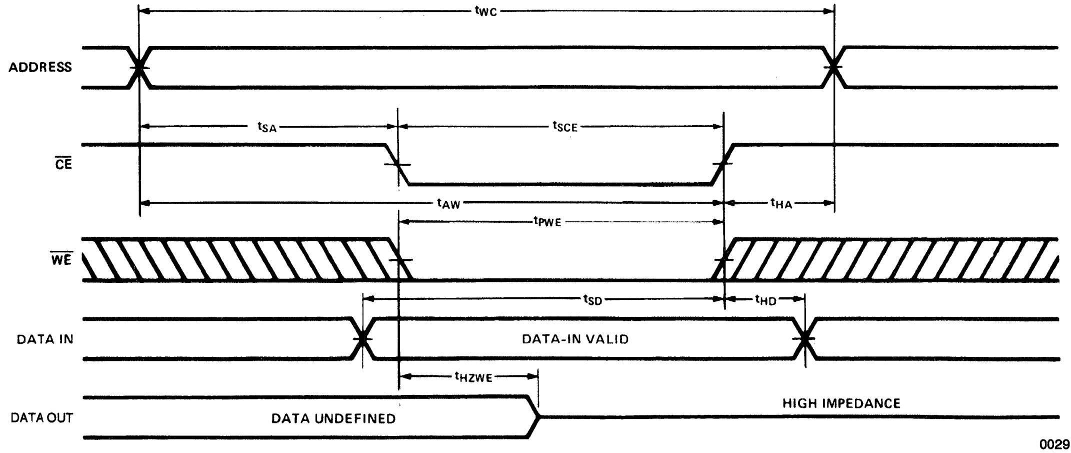
0029-8

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[8]


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

0029-9

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)[8]

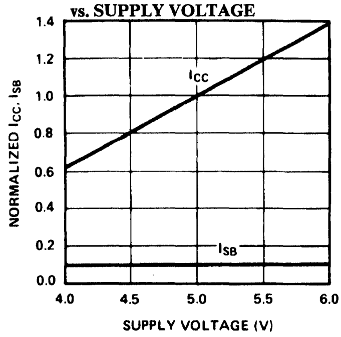

tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

0029-10

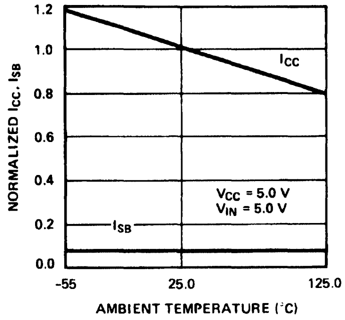
Note: If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

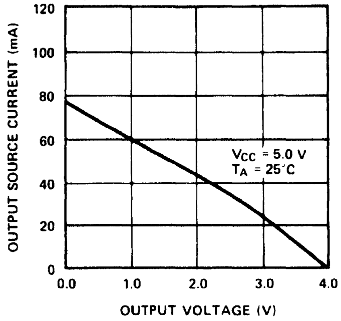
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



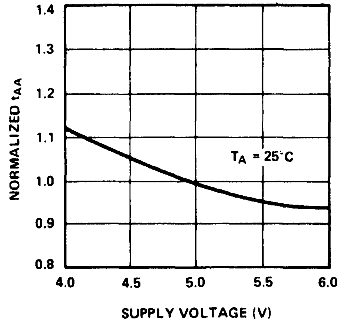
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



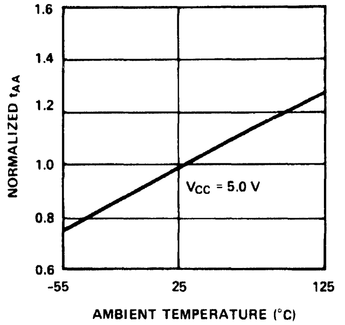
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



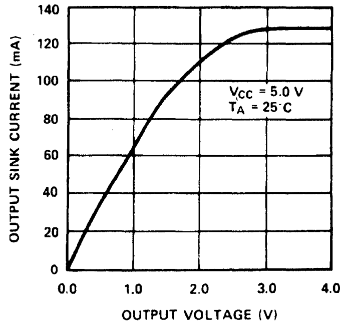
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



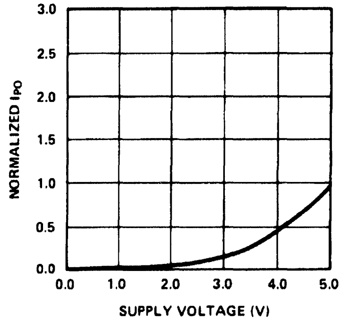
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



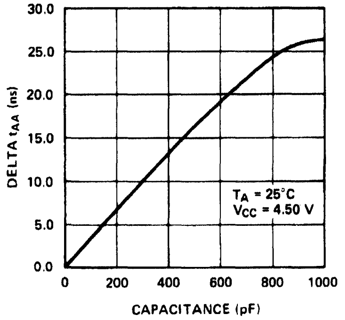
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



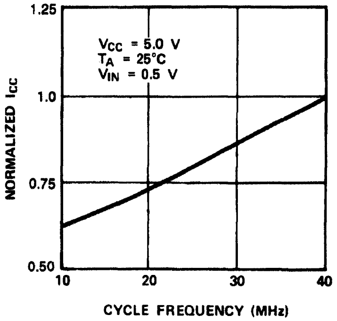
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0029-14

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect Power Down
L	H	Data Out	Read
L	L	Data In	Write

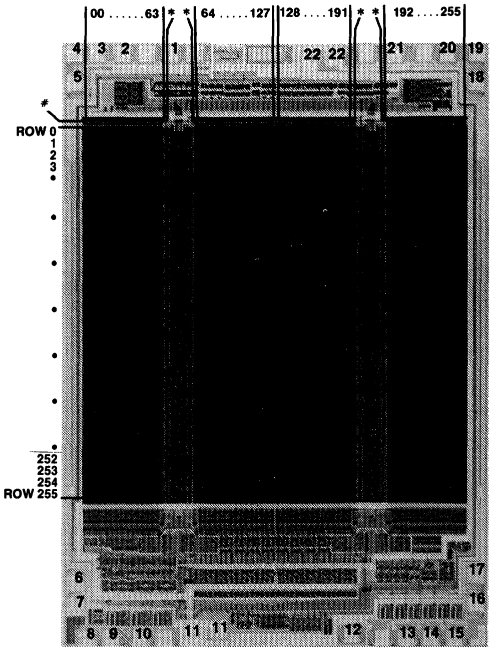
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C187-25PC	P9	Commercial
	CY7C187L-25PC	P9	
	CY7C187-25DC	D10	
	CY7C187L-25DC	D10	
35	CY7C187-35PC	P9	Commercial
	CY7C187L-35PC	P9	
	CY7C187-35DC	D10	
	CY7C187L-35DC	D10	
	CY7C187-35LC	L52	
	CY7C187L-35LC	L52	
	CY7C187-35DMB	D10	Military
	CY7C187L-35DMB	D10	
	CY7C187-35LMB	L52	
	CY7C187L-35LMB	L52	
45	CY7C187-45PC	P9	Commercial
	CY7C187L-45PC	P9	
	CY7C187-45DC	D10	
	CY7C187L-45DC	D10	
	CY7C187-45LC	L52	
	CY7C187L-45LC	L52	
	CY7C187-45DMB	D10	Military
	CY7C187L-45DMB	D10	
	CY7C187-45LMB	L52	
	CY7C187L-45LMB	L52	

Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Bit Map


00 63
*
*
64 127
128 191
*
*
192 255
4
3
2
1
22
22
21
20
19
5
18
*
ROW 0
1
2
3
252
253
254
ROW 255
6
7
8
9
10
11
11
12
13
14
15
16
17

0029-15

CYPRESS SEMICONDUCTOR

CY7C189
CY7C190

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high speed CMOS RAMs**
- **Inverting outputs CY7C189**
- **Non-inverting outputs CY7C190**
- **High speed**
  - **— 15 ns and 25 ns commercial**
  - **— 25 ns military**
- **Low power**
  - **— 303 mW at 25 ns**
  - **— 495 mW at 15 ns**
- **Power supply 5V ±10%**
- **Advanced high speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2000V static discharge**
- **Three-state outputs**
- **TTL compatible interface levels**

Functional Description

The CY7C189 and CY7C190 are extremely high peformance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting (CY7C189) and non-inverting (CY7C190) outputs.

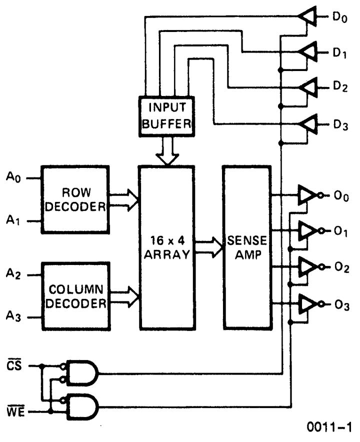
An active LOW write enable ($\overline{WE}$) signal controls the writing and reading of the memory. When the write enable ($\overline{WE}$) and chip select ($\overline{CS}$) are both LOW the information on the four data inputs (D_0–D_3) is written into the location addressed by the information on the address lines (A_0–A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0–O_3) when the write cycle is complete. This precondition operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is accomplished with an active LOW on the chip select line ($\overline{CS}$) and a HIGH on the write enable ($\overline{WE}$) line. The information stored is read out from the addressed location and presented at the outputs in inverted (CY7C189) or non-inverted (CY7C190) format.

During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

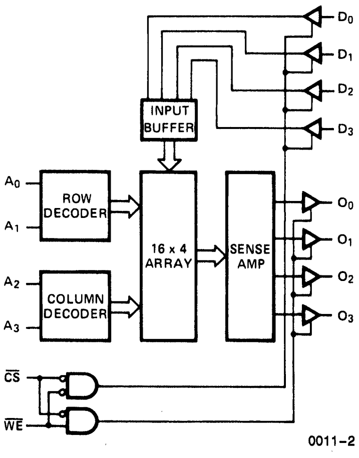
Logic Block Diagrams

CY7C189


D0
D1
D2
D3
INPUT BUFFER
A0
A1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O0
O1
O2
O3
A2
A3
COLUMN DECODER
CS
WE

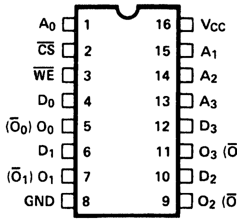
0011-1

CY7C190


D0
D1
D2
D3
INPUT BUFFER
A0
A1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O0
O1
O2
O3
A2
A3
COLUMN DECODER
CS
WE

0011-2

Pin Configuration


A0 1
CS 2
WE 3
D0 4
(O0) O0 5
D1 6
(O1) O1 7
GND 8
16 Vcc
15 A1
14 A2
13 A3
12 D3
11 O3 (O3)
10 D2
9 O2 (O2)

0011-3

(7C189)
7C190

Selection Guide

		7C189-15 7C190-15	7C189-25 7C190-25
Maximum Access Time (ns)	Commercial	15	25
	Military		25
Maximum Operating Current (mA)	Commercial	90	55
	Military		70

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potenial
(Pin 16 to Pin 8).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) ....20 mA

Static Discharge Voltage ....>2001V
(per MIL-STD-883 Method 3015.2)

Latchup Current ....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C189-15 7C190-15		7C189-25 7C190-25		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45		0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage[1]							
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		55	mA
			Military				70	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. The CMOS process does not provide a clamp diode. However the CY7C189 and CY7C190 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 5 ns (measured at 50% points).
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch).
4. Tested on a sample basis.

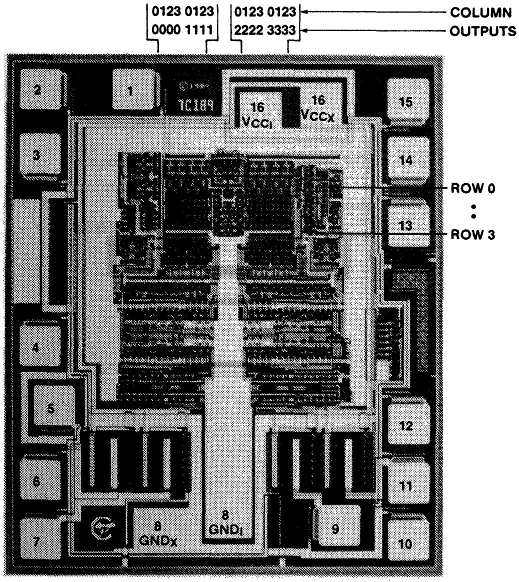
Switching Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions	7C189-15 7C190-15		7C189-25 7C190-25		Units
			Min.	Max.	Min.	Max.	
READ CYCLE							
t_{RC}	Ready Cycle Time		15		25		ns
t_{ACS}	Chip Select to Output Valid	Note 8		12		15	ns
t_{HZCS}	Chip Select Inactive to High Z	Note 7, 9		12		15	ns
t_{LZCS}	Chip Select Active to Low Z			12		15	ns
t_{OHA}	Output Hold from Address Change		5		5		ns
t_{AA}	Address Access Time	Note 8		15		25	ns
WRITE CYCLE[3, 6]							
t_{WC}	Write Cycle Time		15		20		ns
t_{HZWE}	Write Enable Active to High Z	Note 7, 9		12		20	ns
t_{LZWE}	Write Enable Inactive to Low Z			12		20	
t_{AWE}	Write Enable Inactive to Output Valid	Note 8		12		20	ns
t_{PWE}	Write Enable Pulse Width		15		20		ns
t_{SD}	Data Setup to Write End		15		20		ns
t_{HD}	Data Hold from Write End		0		0		ns
t_{SA}	Address Setup to Write Start		0		0		ns
t_{HA}	Address Hold from Write End		0		0		ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input.
8. t_{AA}, t_{ACS} and t_{AWE} are tested with $C_L = 30$ pF as in *Figure 1a.* Timing is referenced to 1.5V on the inputs and outputs.
9. t_{HZCS} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b.*

Bit Map



0011-5

Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

AC Test Loads and Waveforms

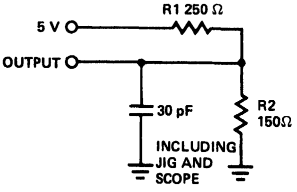

R1 250 Ω
5 V
OUTPUT
30 pF
R2 150Ω
INCLUDING JIG AND SCOPE

Figure 1a

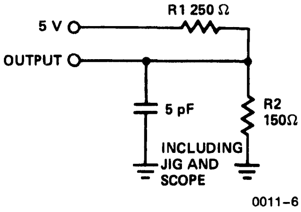
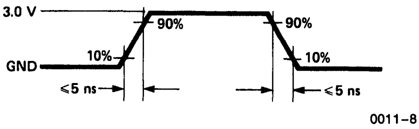
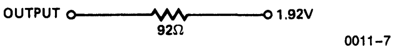

R1 250 Ω
5 V
OUTPUT
5 pF
R2 150Ω
INCLUDING JIG AND SCOPE
0011-6

Figure 1b

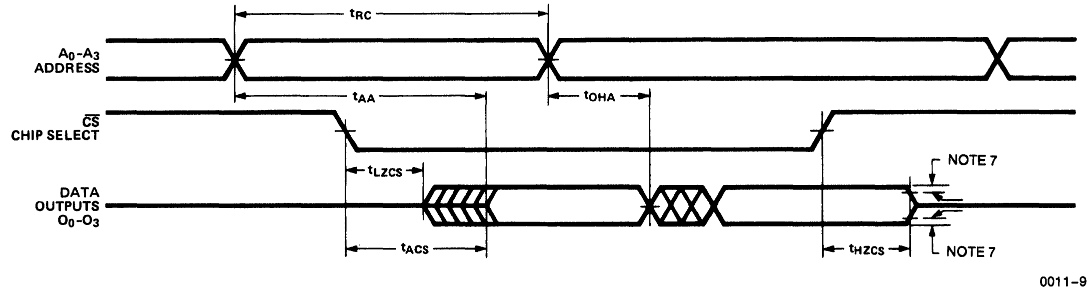
ALL INPUT PULSES


3.0 V
GND
90%
90%
10%
10%
≤5 ns
≤5 ns
0011-8

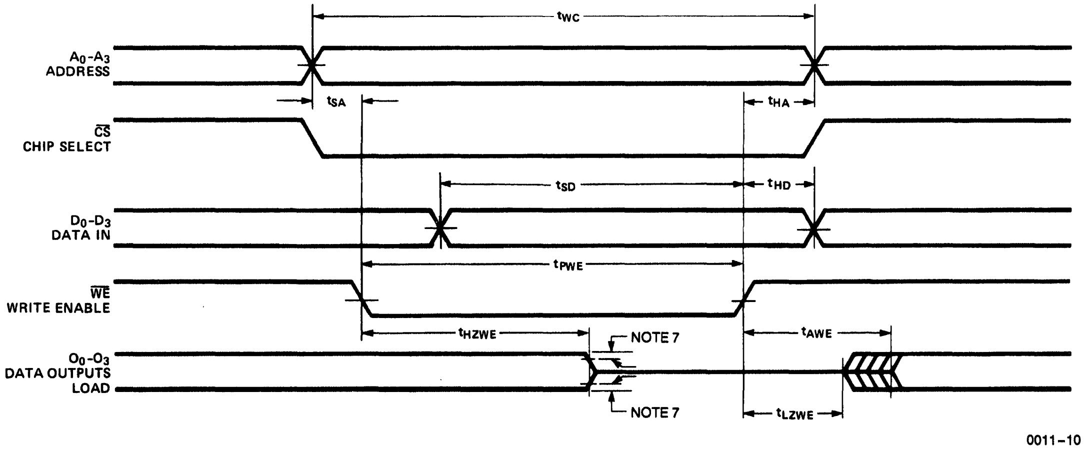
Equivalent to: THÉVENIN EQUIVALENT


OUTPUT
92Ω
1.92V
0011-7

Read Mode


t_RC
A0-A3 ADDRESS
t_AA
t_OHA
CS CHIP SELECT
t_LZCS
NOTE 7
DATA OUTPUTS O0-O3
t_ACS
t_HZCS
NOTE 7
0011-9

Write Mode


t_WC
A0-A3 ADDRESS
t_SA
t_HA
CS CHIP SELECT
t_SD
t_HD
D0-D3 DATA IN
t_PWE
WE WRITE ENABLE
t_HZWE
NOTE 7
t_AWE
O0-O3 DATA OUTPUTS LOAD
NOTE 7
t_LZWE
0011-10

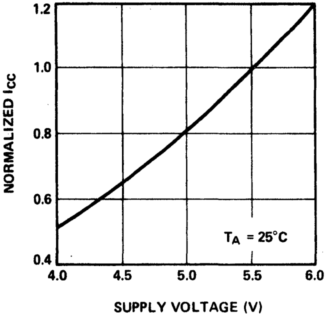
(All above measurements referenced to 1.5V.)

Note:

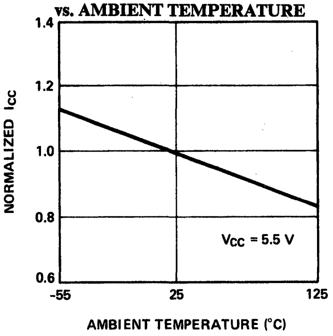
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

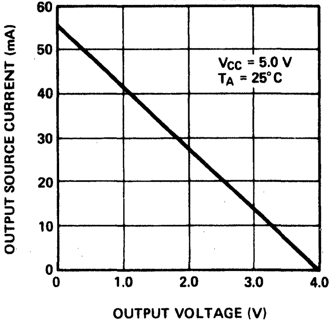
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



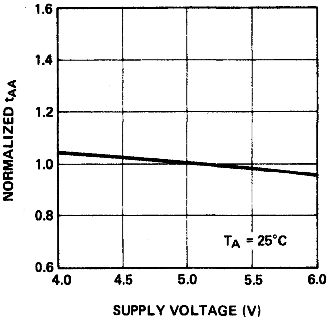
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



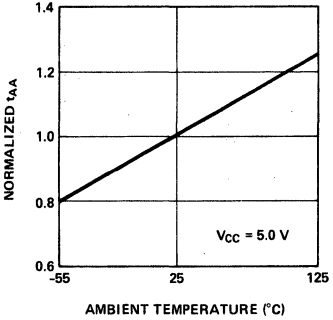
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



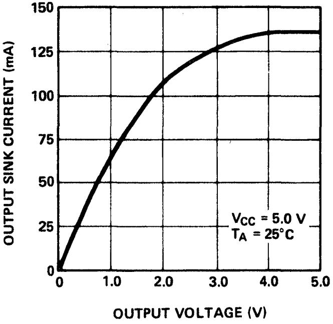
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



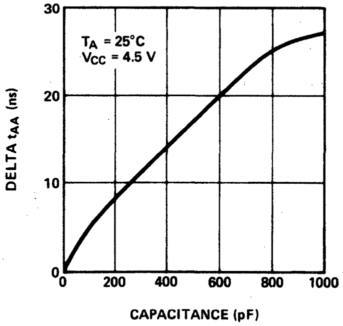
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



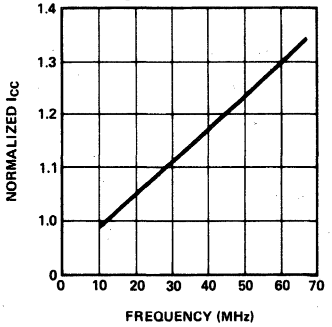
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY

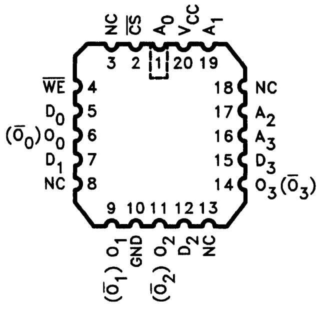


0011-11

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C189-15PC CY7C190-15PC	P1	Commercial
	CY7C189-15DC CY7C190-15DC	D2	
	CY7C189-15LC CY7C190-15LC	L61	
25	CY7C189-25PC CY7C190-25PC	P1	
	CY7C189-25DC CY7C190-25DC	D2	
	CY7C189-25LC CY7C190-25LC	L61	
	CY7C189-25DMB CY7C190-25DMB	D2	Military
	CY7C189-25LMB CY7C190-25LMB	L61	

Pin Configuration


NC
CS
A0
VCC
A1
3
2
1
20
19
WE 4
D0 5
(Ō0) O0 6
D1 7
NC 8
18 NC
17 A2
16 A3
15 D3
14 O3 (Ō3)
9
10
11
12
13
O1 (Ō1)
GND
O2 (Ō2)
D2
NC

0011-4

(7C189)
7C190

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C191
CY7C192

65,536 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **Transparent write (7C192)**
- **CMOS for optimum speed/ power**
- **High speed**
  - **25 ns t_{AA}**
- **Low active power**
  - **385 mW**
- **Low standby power**
  - **110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C191 and CY7C192 are high performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 85% when deselected.

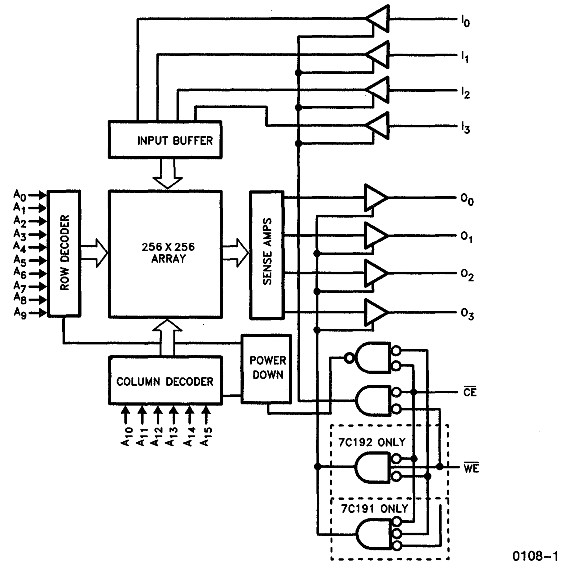
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_1 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while the write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high impedance state when write enable ($\overline{WE}$) is LOW (7C192 only), or chip enable ($\overline{CE}$) is HIGH.

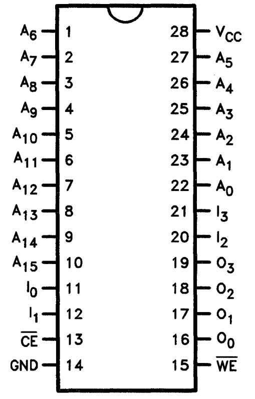
A die coat is used to insure alpha immunity.

Logic Block Diagram


I0
I1
I2
I3
INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
ROW DECODER
256 X 256 ARRAY
SENSE AMPS
O0
O1
O2
O3
POWER DOWN
COLUMN DECODER
A10
A11
A12
A13
A14
A15
CE
WE
7C192 ONLY
7C191 ONLY

0108-1

Pin Configuration


A6 1
A7 2
A8 3
A9 4
A10 5
A11 6
A12 7
A13 8
A14 9
A15 10
I0 11
I1 12
CE 13
GND 14
28 VCC
27 A5
26 A4
25 A3
24 A2
23 A1
22 A0
21 I3
20 I2
19 O3
18 O2
17 O1
16 O0
15 WE

0108-2

Selection Guide

		7C191-25 7C192-25	7C191-35 7C192-35	7C191-45 7C192-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20	20	20
	Military		20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883, Method 3015.2)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C191-25 7C192-25		7C191-35 7C192-35		7C191-45 7C192-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		70		50	mA
			Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military		20		20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

[1] Not more than one output should shorted at one time. Duration of the short circuit should not exceed 30 seconds.

[2] Tested on a sample basis.

AC Test Loads and Waveforms

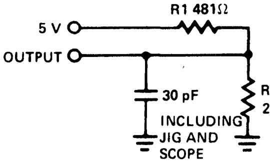


Figure 1a

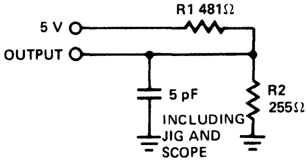
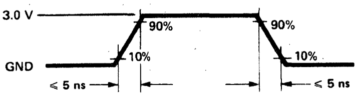


Figure 1b

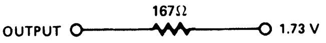
0108-3



0108-5

Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0108-4

Switching Characteristics Over Operating Range[3]

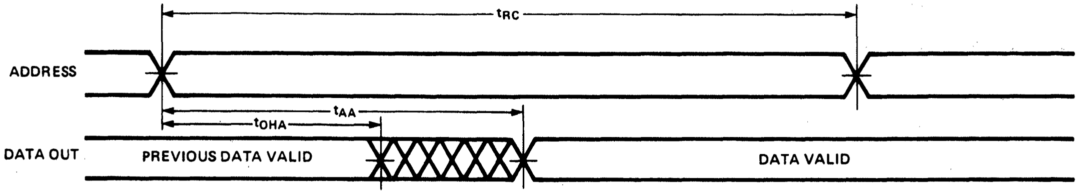
Parameters	Description	7C191-25 7C192-25		7C191-35 7C192-35		7C191-45 7C192-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to LOW Z[5]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4, 5]		15		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		25		25		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		20		ns
t_{SD}	Data Set-up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5] (7C192)	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5] (7C192)		10		15		20	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C191)		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		25		30		35	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. These parameters are specified and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is high for read cycle.
8. Device is continuously selected. $\overline{CE} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

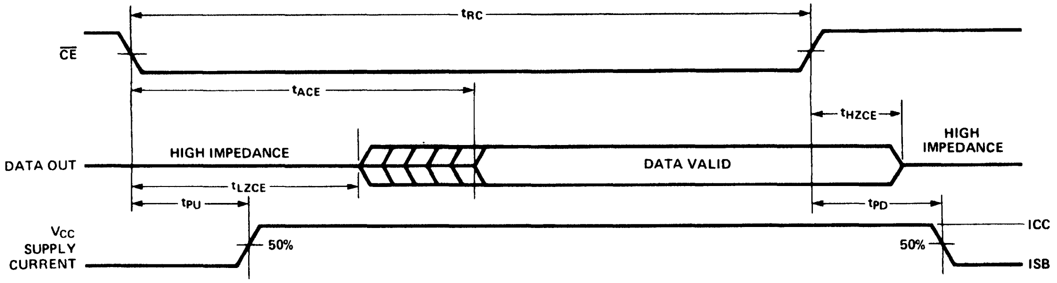
Read Cycle No. 1 (Notes 7, 8)



0108-6

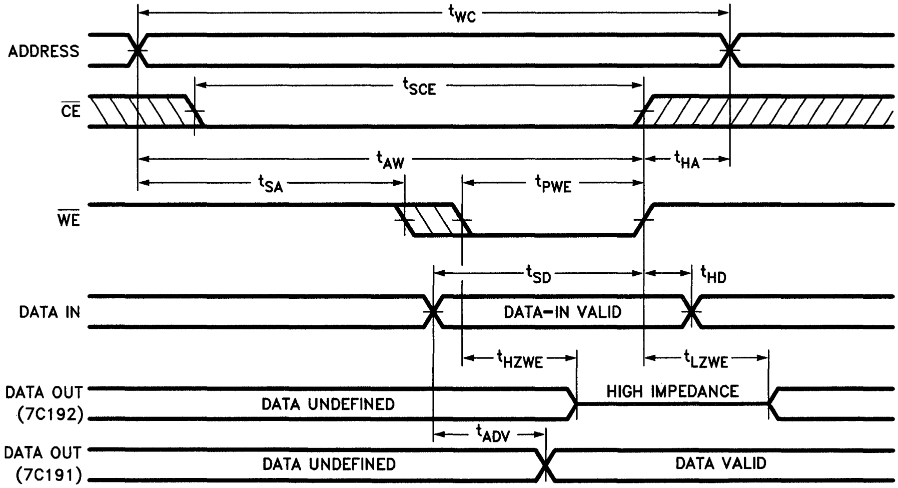
Switching Waveforms (Continued)

Read Cycle (Notes 7, 9)


tRC
CE
tACE
tHZCE
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
tLZCE
tPU
tPD
VCC SUPPLY CURRENT
50%
50%
ICC
ISB

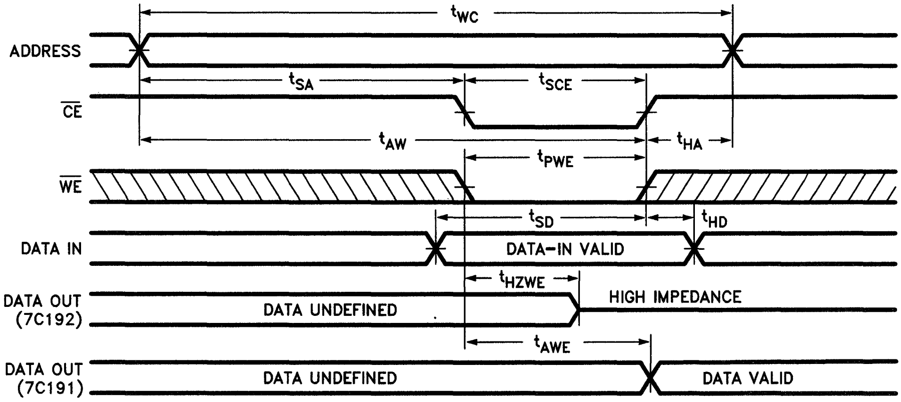
0108-7

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) (Note 6)


tWC
ADDRESS
tSCE
CE
tAW
tHA
tSA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
tLZWE
DATA OUT (7C192)
DATA UNDEFINED
HIGH IMPEDANCE
tADV
DATA OUT (7C191)
DATA UNDEFINED
DATA VALID

0108-8

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) (Note 6)


tWC
ADDRESS
tSA
tSCE
CE
tAW
tHA
tPWE
WE
tSD
tHD
DATA IN
DATA-IN VALID
tHZWE
DATA OUT (7C192)
DATA UNDEFINED
HIGH IMPEDANCE
tAWE
DATA OUT (7C191)
DATA UNDEFINED
DATA VALID

Note: If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state (7C192 only).

0108-9

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C191-25PC	P21	Commercial
	CY7C191-25DC	D22	
35	CY7C191-35PC	P21	Commercial
	CY7C191-35DC	D22	
	CY7C191-35LC	L54	
	CY7C191-35DMB	D22	Military
45	CY7C191-45PC	P21	Commercial
	CY7C191-45DC	D22	
	CY7C191-45LC	L54	
	CY7C191-45DMB	D22	Military
	CY7C191-45LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C192-25PC	P21	Commercial
	CY7C192-25DC	D22	
35	CY7C192-35PC	P21	Commercial
	CY7C192-35DC	D22	
	CY7C192-35LC	L54	
	CY7C192-35DMB	D22	Military
45	CY7C192-45PC	P21	Commercial
	CY7C192-45DC	D22	
	CY7C192-45LC	L54	
	CY7C192-45DMB	D22	Military
	CY7C192-45LMB	L54	

PRELIMINARY **CY7C194**
CY7C196

CYPRESS
SEMICONDUCTOR

65,536 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **Output Enable ($\overline{OE}$) feature (7C196)**
- **CMOS for optimum speed/ power**
- **High speed**
  - **— 25 ns t_{AA}**
- **Low active power**
  - **— 385 mW**
- **Low standby power**
  - **— 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

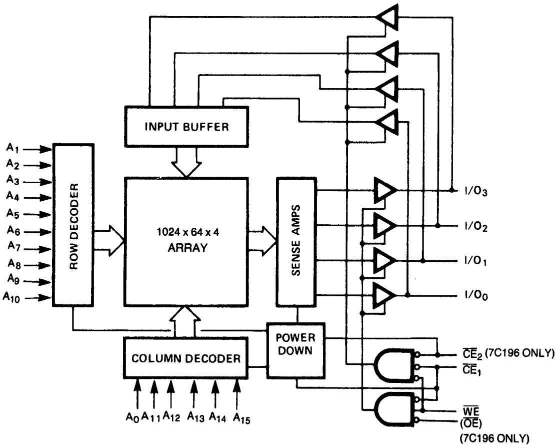
Functional Description

The CY7C194 and CY7C196 are high performance CMOS static RAMs organized as 65,536 x 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ($\overline{CE}_1$, on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

Writing to the device is accomplished when the chip enable(s) ($\overline{CE}$ on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable(s) ($\overline{CE}$ on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins. A die coat is used to insure alpha immunity.

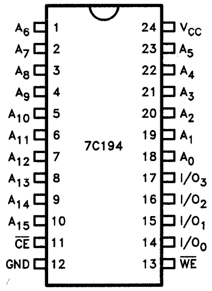
Logic Block Diagram



INPUT BUFFER
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
ROW DECODER
1024 x 64 x 4
ARRAY
SENSE AMPS
I/O3
I/O2
I/O1
I/O0
POWER DOWN
COLUMN DECODER
A0 A11 A12 A13 A14 A15
CE2 (7C196 ONLY)
CE1
WE
(OE)
(7C196 ONLY)

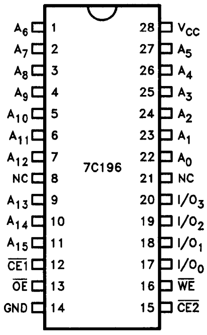
0109-1

Pin Configurations



A6 1
A7 2
A8 3
A9 4
A10 5
A11 6
A12 7
A13 8
A14 9
A15 10
CE 11
GND 12
7C194
24 VCC
23 A5
22 A4
21 A3
20 A2
19 A1
18 A0
17 I/O3
16 I/O2
15 I/O1
14 I/O0
13 WE

0109-2



A6 1
A7 2
A8 3
A9 4
A10 5
A11 6
A12 7
NC 8
A13 9
A14 10
A15 11
CE1 12
OE 13
GND 14
7C196
28 VCC
27 A5
26 A4
25 A3
24 A2
23 A1
22 A0
21 NC
20 I/O3
19 I/O2
18 I/O1
17 I/O0
16 WE
15 CE2

0109-3

Selection Guide

		7C194-25 7C196-25	7C194-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20	20	20
	Military		20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....20 mA

Static Discharge Voltage ....>2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current.........................>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C194-25 7C196-25		7C194-35 7C196-35		7C194-45 7C196-45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		70		50	mA
			Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military				20		20	
I_{SB_2}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} −0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

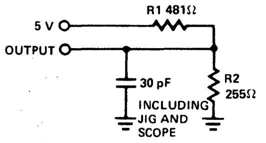


Figure 1a

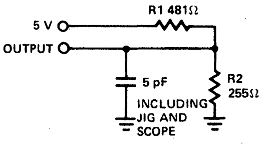


Figure 1b

0109-4

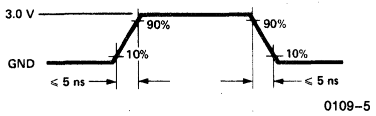
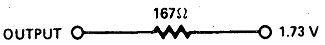


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0109-6

Switching Characteristics Over Operating Range[4]

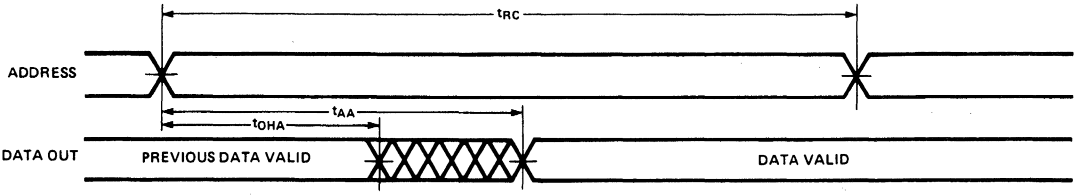
Parameters	Description		7C194-25 7C196-25 Min.	7C194-25 7C196-25 Max.	7C194-35 7C196-35 Min.	7C194-35 7C196-35 Max.	7C194-45 7C196-45 Min.	7C194-45 7C196-45 Max.	Units
READ CYCLE									
t_{RC}	Read Cycle Time		25		35		45		ns
t_{AA}	Address to Data Valid			25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		ns
t_{ACE_1, CE_2}	$\overline{CE}$ LOW to Data Valid			25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C196		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	7C196	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z	7C196		15		15		15	ns
t_{LZCE_1, CE_2}	$\overline{CE}$ LOW to LOW Z[6]		5		5		5		ns
t_{HZCE_1, CE_2}	$\overline{CE}$ HIGH to High Z[5, 6]			10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down			25		35		45	ns
WRITE CYCLE[7]									
t_{WC}	Write Cycle Time		20		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		20		30		35		ns
t_{AW}	Address Set-up to Write End		20		25		35		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		20		25		35		ns
t_{SD}	Data Set-up to Write End		13		15		20		ns
t_{HD}	Data Hold from Write End		0		0		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to LOW Z[6]		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to HIGH Z[5, 6]		0	7	0	10	0	15	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}/\overline{CE}_2 = V_{IL}$. (7C196: $\overline{OE} = V_{IL}$, $\overline{CE}_2 = V_{IL}$ also.)
10. Address valid prior to or coincident with $\overline{CE}$ and $\overline{CE}_2$ transition low.
11. 7C196 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms

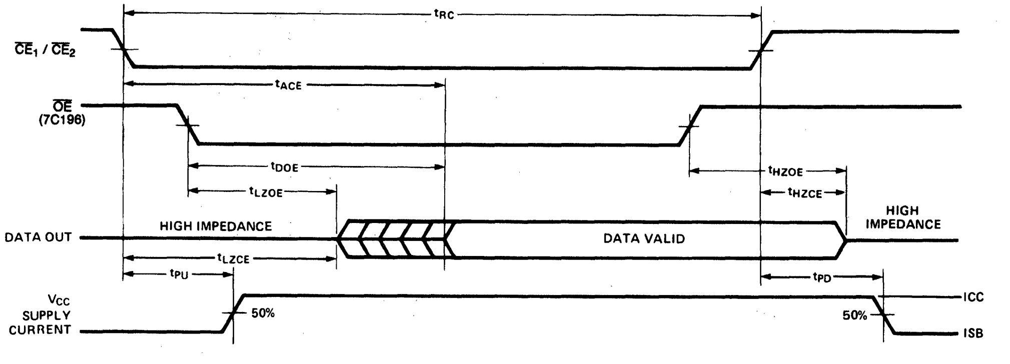
Read Cycle No. 1 (Notes 8, 9)



0109-7

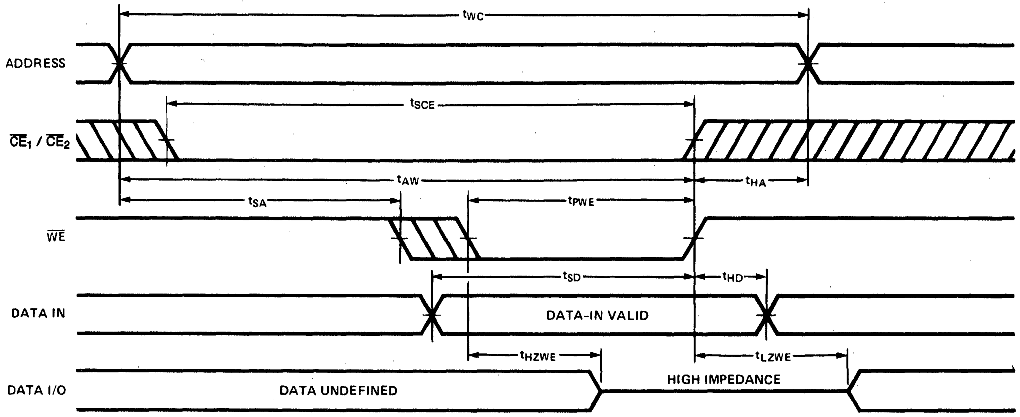
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)


t_{RC}
$\overline{CE}_1$ / $\overline{CE}_2$
t_{ACE}
$\overline{OE}$ (7C196)
t_{DOE}
t_{LZOE}
t_{HZOE}
t_{HZCE}
HIGH IMPEDANCE
HIGH IMPEDANCE
DATA OUT
DATA VALID
t_{LZCE}
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

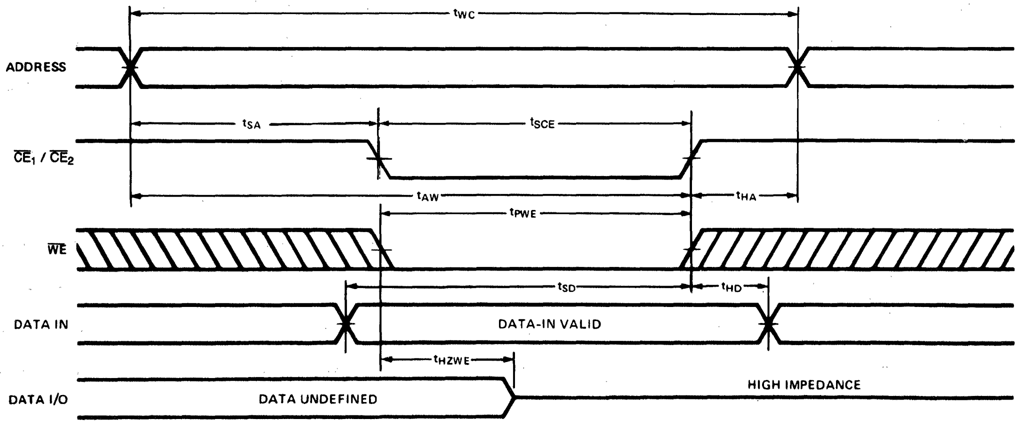
0109-8

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 7, 11)


t_{WC}
ADDRESS
t_{SCE}
$\overline{CE}_1$ / $\overline{CE}_2$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0109-9

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Notes 7, 11)


t_{WC}
ADDRESS
t_{SA}
t_{SCE}
$\overline{CE}_1$ / $\overline{CE}_2$
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

0109-10

7C194 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power Down
L	H	Data Out	Read
L	L	Data In	Write

7C196 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power Down
X	H	X	X		
L	L	H	L	Data Out	Read
L	L	L	X	Data In	Write
L	L	H	H	High Z	Deselect/Power Down

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C194-25PC	P13	Commercial
	CY7C194-25DC	D14	
35	CY7C194-35PC	P13	Commercial
	CY7C194-35DC	D14	
	CY7C194-35DMB	D14	Military
45	CY7C194-45PC	P13	Commercial
	CY7C194-45DC	D14	
	CY7C194-45DMB	D14	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C196-25PC	P21	Commercial
	CY7C196-25DC	D22	
35	CY7C196-35PC	P21	Commercial
	CY7C196-35DC	D22	
	CY7C196-35DMB	D22	Military
45	CY7C196-45PC	P21	Commercial
	CY7C196-45DC	D22	
	CY7C196-45DMB	D22	Military

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C197**

262,144 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power—385 mW**
- **Low standby power—110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C197 is a high performance CMOS static RAM organized as 262,144 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 71% when deselected.

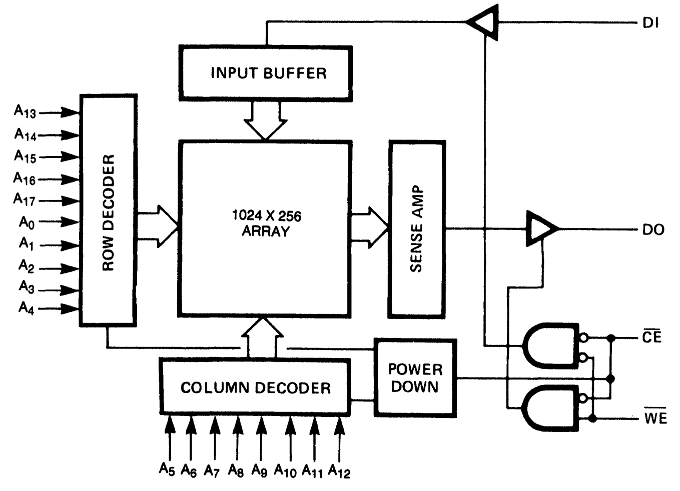
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

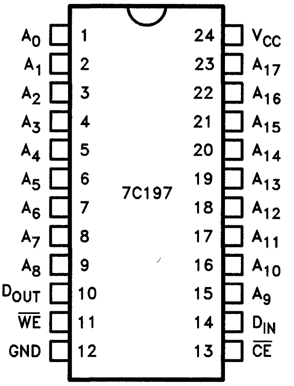
The 7C197 utilizes a Die Coat to ensure alpha immunity.

Logic Block Diagram


DI
INPUT BUFFER
A13
A14
A15
A16
A17
A0
A1
A2
A3
A4
ROW DECODER
1024 X 256 ARRAY
SENSE AMP
DO
CE
WE
COLUMN DECODER
POWER DOWN
A5 A6 A7 A8 A9 A10 A11 A12

0110-1

Pin Configuration


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
DOUT 10
WE 11
GND 12
7C197
24 VCC
23 A17
22 A16
21 A15
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 DIN
13 CE

0110-2

Selection Guide

		7C197-25	7C197-35	7C197-45
Maximum Access Time (ns)	Commercial	25	35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	70
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions			7C197-25		7C197-35		7C197-45		Units
					Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Military		0.4		0.4		0.4	V
			I_{OL} = 12.0 mA	Commercial							
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND				−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Commercial		70		70		50	mA
				Military				70		70	
I_{SB_1}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		Commercial		20		20		20	mA
				Military				20		20	
I_{SB_2}	Automatic $\overline{CE}$[2] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		Commercial		20		20		20	mA
				Military				20		20	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

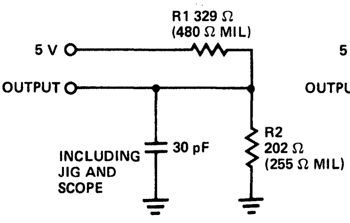


Figure 1a

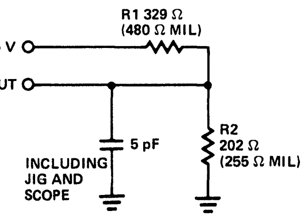
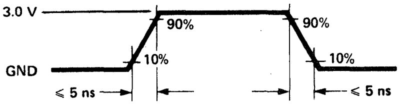


Figure 1b

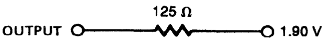
0110-3



0110-4

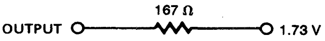
Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0110-5

Commercial



0110-6

Military

Switching Characteristics Over Operating Range[4]

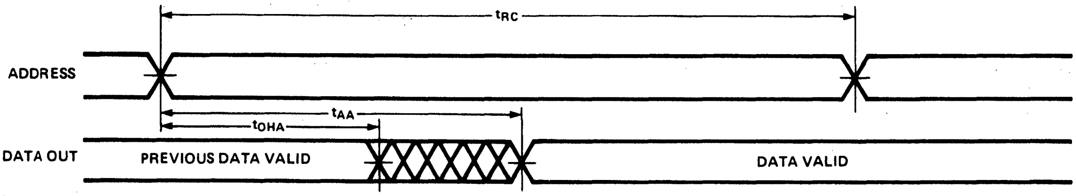
Parameters	Description	7C197-25		7C197-35		7C197-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High[5, 6]	0	15	0	20	0	20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	15	0	20	0	20	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b.* Transition is increased ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

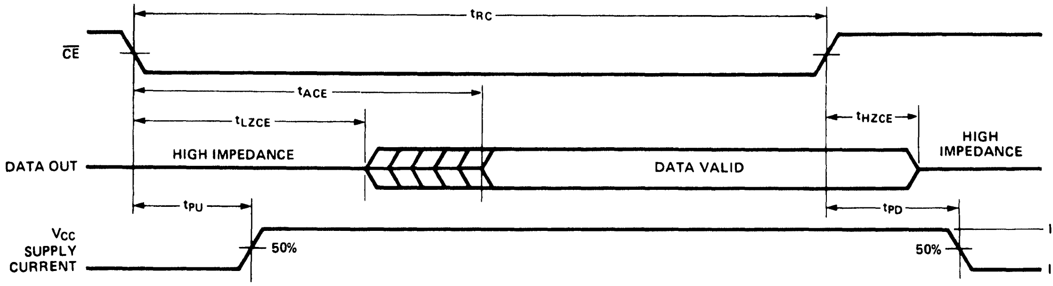
Read Cycle No. 1[8, 9]



0110-7

Switching Waveforms (Continued)

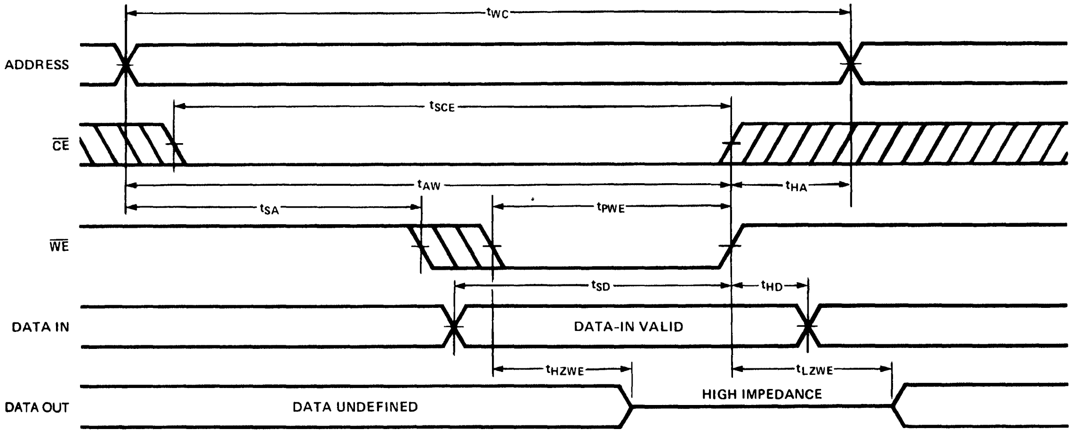
Read Cycle No. 2[9]


t_{RC}
$\overline{CE}$
t_{ACE}
t_{LZCE}
t_{HZCE}
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

0110-8

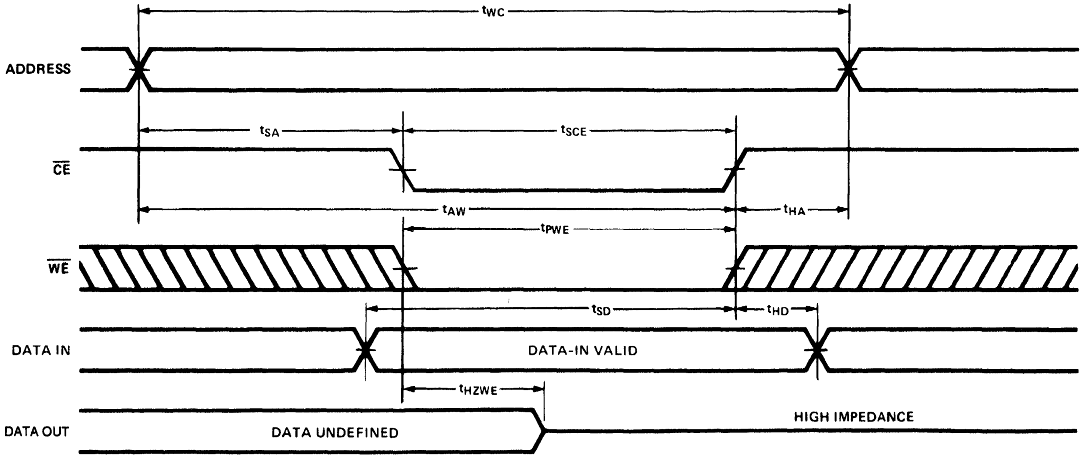
2

Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]


t_{WC}
ADDRESS
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
HIGH IMPEDANCE
DATA OUT
DATA UNDEFINED

0110-9

Write Cycle No. 2 ($\overline{CE}$ Controlled)[8]


t_{WC}
ADDRESS
t_{SA}
t_{SCE}
$\overline{CE}$
t_{AW}
t_{HA}
t_{PWE}
$\overline{WE}$
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
HIGH IMPEDANCE
DATA OUT
DATA UNDEFINED

0110-10

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect Power Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C197-25PC	P13	Commercial
	CY7C197-25DC	D14	
35	CY7C197-35PC	P13	Commercial
	CY7C197-35DC	D14	
	CY7C197-35DMB	D14	Military
45	CY7C197-45PC	P13	Commercial
	CY7C197-45DC	D14	
	CY7C197-45DMB	D14	Military

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C198
CY7C199

32,768 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—35 ns**
- **Low active power—550 mW**
- **Low standby power—110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

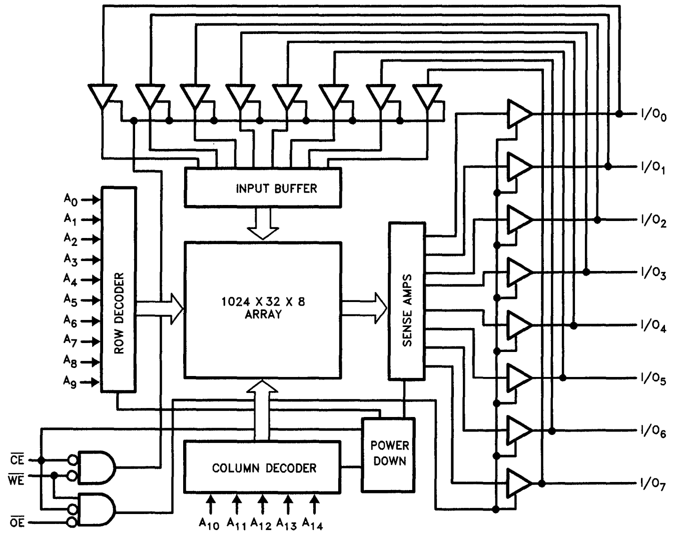
Functional Description

The CY7C198 and CY7C199 are high performance CMOS static RAMs organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by 80% when deselected. The CY7C199 is in the space saving 300 mil wide DIP package and leadless chip carrier. The CY7C198 is in the standard 600 mil wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O$_0$ through I/O$_7$) is written into the memory location addressed by the address present on the address pins (A$_0$ through A$_{14}$). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

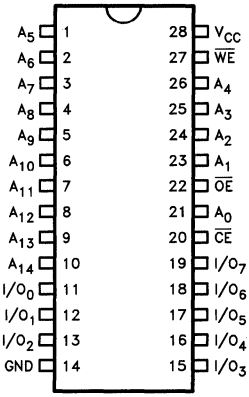
Logic Block Diagram



INPUT BUFFER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
ROW DECODER
1024 X 32 X 8 ARRAY
SENSE AMPS
POWER DOWN
COLUMN DECODER
A10 A11 A12 A13 A14
CE
WE
OE
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7

0111-1

Pin Configuration



A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
A14 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 A4
25 A3
24 A2
23 A1
22 OE
21 A0
20 CE
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3

0111-2

Selection Guide

		7C198-35 7C199-35	7C198-45 7C199-45	7C198-55 7C199-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	100	100	80
	Military		100	100
Maximum Standby Current (mA)	Commercial	20/20	20/20	20/20
	Military		20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14)................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(Per MIL-STD-883 Method 3015.2)

Latch-up Current........................ >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C198-35 7C199-35		7C198-45 7C199-45		7C198-55 7C199-55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	−10	10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		100		100		80	mA
			Military				100		100	
I_{ISB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Commercial		20		20		20	mA
			Military				20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Commercial		20		20		20	mA
			Military				20		20	

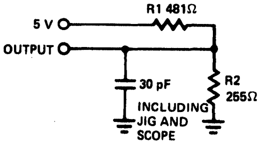
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

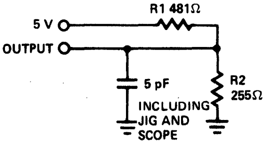
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms



0111-3

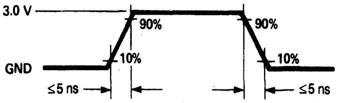
Figure 1a



0111-4

Figure 1b

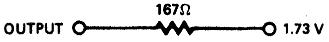
All Input Pulses



0111-5

Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0111-6

Switching Characteristics Over Operating Range[3]

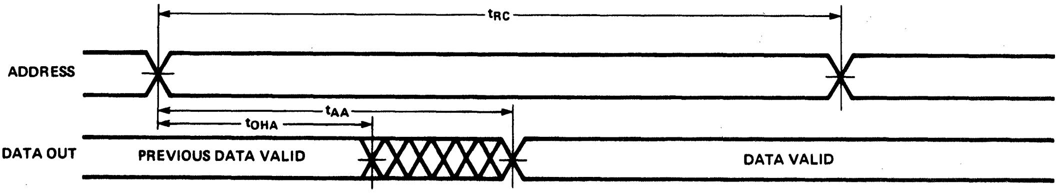
Parameters	Description	7C198-35 7C199-35		7C198-45 7C199-45		7C198-55 7C199-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		20		20		25	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[4]		20		25		30	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[5]	5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[4, 5]		15		20		20	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down		20		25		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		50		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	20		25		30		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[4]		15		20		25	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	3		3		3		ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{\text{WE}}$ is HIGH for read cycle.
8. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
10. Data I/O is HIGH impedance if $\overline{\text{OE}} = V_{IH}$.

Switching Waveforms

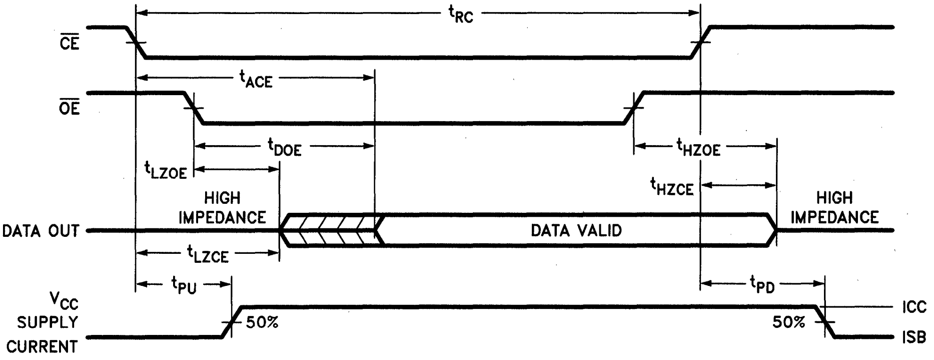
Read Cycle No. 1 (Notes 8, 9)



0111-7

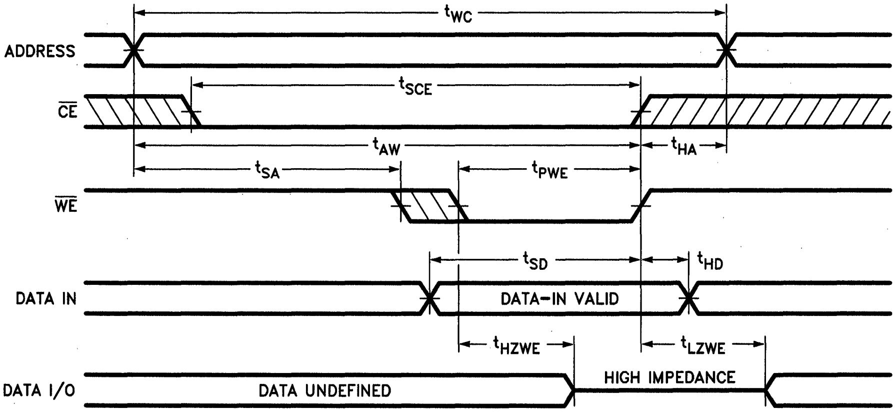
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 7, 9)


t_{RC}
CE
t_{ACE}
OE
t_{DOE}
t_{HZOE}
t_{LZOE}
t_{HZCE}
HIGH IMPEDANCE
DATA OUT
DATA VALID
HIGH IMPEDANCE
t_{LZCE}
t_{PU}
t_{PD}
V_{CC} SUPPLY CURRENT
50%
50%
ICC
ISB

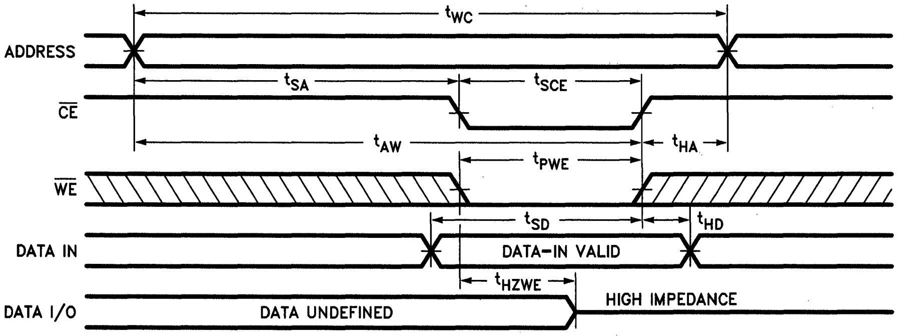
0111-8

Write Cycle No. 1 (WE Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SCE}
CE
t_{AW}
t_{HA}
t_{SA}
t_{PWE}
WE
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
t_{LZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0111-9

Write Cycle No. 2 (CE Controlled) (Notes 6, 10)


t_{WC}
ADDRESS
t_{SA}
t_{SCE}
CE
t_{AW}
t_{HA}
t_{PWE}
WE
t_{SD}
t_{HD}
DATA IN
DATA-IN VALID
t_{HZWE}
DATA I/O
DATA UNDEFINED
HIGH IMPEDANCE

0111-10

Note: If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect Power Down

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C198-35PC	P15	Commercial
	CY7C198-35DC	D16	Commercial
45	CY7C198-45PC	P15	Commercial
	CY7C198-45DC	D16	Commercial
	CY7C198-45DMB	D16	Military
55	CY7C198-55PC	P15	Commercial
	CY7C198-55DC	D16	Commercial
	CY7C198-55DMB	D16	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C199-35PC	P21	Commercial
	CY7C199-35DC	D22	Commercial
45	CY7C199-45PC	P21	Commercial
	CY7C199-45DC	D22	Commercial
	CY7C199-45DMB	D22	Military
55	CY7C199-55PC	P21	Commercial
	CY7C199-55DC	D22	Commercial
	CY7C199-55DMB	D22	Military

CY74S189, CY27LS03
CY27S03, CY27S07

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high speed CMOS RAMs**
- **Inverting outputs 27S03, 27LS03, 74S189**
- **Non-inverting outputs 27S07**
- **High speed**
  - **25 ns**
- **Low power**
  - **210 mW (27LS03)**
- **Power supply 5V ±10%**
- **Advanced high speed CMOS processing for optimum speed/ power product**
- **Capable of withstanding greater than 2001V static discharge**
- **Three-state outputs**
- **TTL compatible interface levels**

Functional Description

These devices are high performance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting and non-inverting outputs.

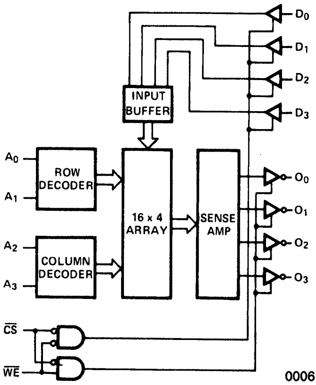
An active LOW write enable ($\overline{WE}$) signal controls the writing and reading of the memory. When the write enable ($\overline{WE}$) and chip select ($\overline{CS}$) are both LOW the information on the four data inputs (D_0-D_3) is written into the location addressed by the information on the address lines (A_0-A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0-O_3) when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is accomplished with an active LOW on the chip select line ($\overline{CS}$) and a HIGH on the write enable ($\overline{WE}$) line. The information stored is read out from the addressed location and presented at the outputs in inverted or non-inverted format.

During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

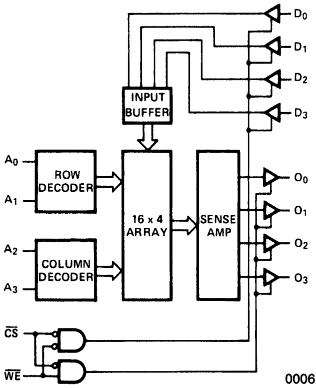
Logic Block Diagrams

27S03,
27LS03, 74S189


D0
D1
D2
D3
INPUT BUFFER
A0
A1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O0
O1
O2
O3
A2
A3
COLUMN DECODER
CS
WE

0006-1

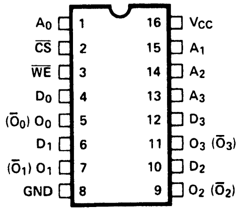
27S07


D0
D1
D2
D3
INPUT BUFFER
A0
A1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O0
O1
O2
O3
A2
A3
COLUMN DECODER
CS
WE

0006-2

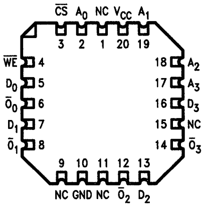
Pin Configurations

27S07
(27S03, 27LS03, 74S189)


A0 1
CS 2
WE 3
D0 4
(Ō0) O0 5
D1 6
(Ō1) O1 7
GND 8
16 Vcc
15 A1
14 A2
13 A3
12 D3
11 O3 (Ō3)
10 D2
9 O2 (Ō2)

0006-3

DIP
Top View


CS A0 NC VCC A1
3 2 1 20 19
WE 4
D0 5
Ō0 6
D1 7
Ō1 8
18 A2
17 A3
16 D3
15 NC
14 Ō3
9 10 11 12 13
NC GND NC Ō2 D2

0006-10

LCC
Top View

Selection Guide (For higher performance and lower power refer to CY7C189/90 data sheet.)

		27S03A 27S07A	27S03, 27S07 74S189	27LS03
Maximum Access Time (ns)	Commercial	25	35	
	Military	25	35	65
Maximum Operating Current (mA)	Commercial	90	90	
	Military	100	100	38

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 16 to 8) .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage..................... >2001 V
(per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		74S189, 27S03, 27S07		27LS03		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45			V
		V_{CC} = Min., I_{OL} = 8.0 mA					0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage[1]							
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90			mA
			Military		100		38	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. The CMOS process does not provide a clamp diode. However these devices are insensitive to −3V dc input levels and −5V undershoot pulses of less than 5 ns (measured at 50% points).
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
4. Tested on a sample basis.

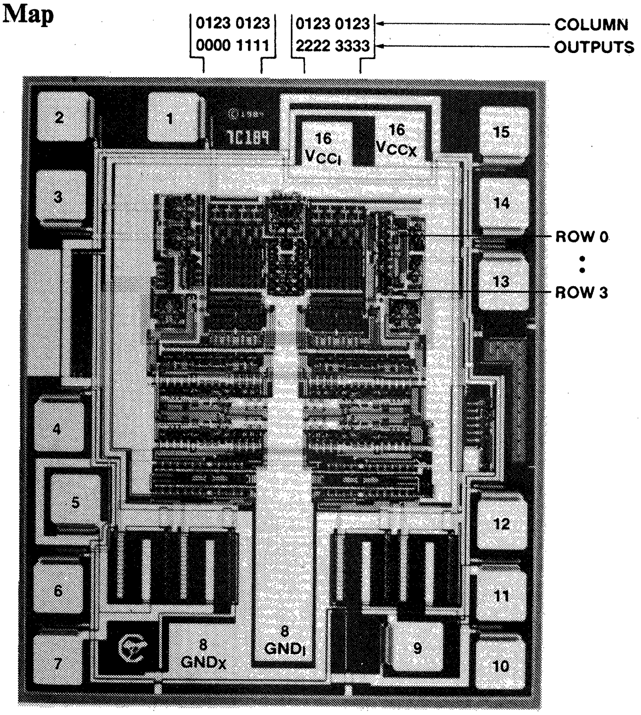
Switching Characteristics Over the Operating Range[5]

Parameters	Description	27S03A 27S07A Min.	27S03A 27S07A Max.	27S03 27S07 Min.	27S03 27S07 Max.	74S189 Min.	74S189 Max.	27LS03 Min.	27LS03 Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		35		65		ns
t_{AA}	Address to Data Valid[8]		25		35		35		65	ns
t_{ACS}	$\overline{CS}$ Low to Data Valid[8]		15		17		22		35	ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[7, 9, 10]		15		20		17		35	ns
WRITE CYCLE[3, 5, 6]										
t_{WC}	Write Cycle Time	25		35		35		65		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SCS}	$\overline{CS}$ Set-up to Write Start					0				ns
t_{HCS}	$\overline{CS}$ Hold from Write End					0				ns
t_{SD}	Data Set-up to Write End	20		25		20		55		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		20		55		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9, 10]		20		25		20		35	ns
t_{AWE}	$\overline{WE}$ HIGH to Output Valid[8]		20		35		30		35	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to intiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input.
8. t_{AA}, t_{ACS} and t_{AWE} are tested with $C_L = 30$ pF as in *Figure 1a.* Timing is referenced to 1.5V on the inputs and outputs.
9. t_{HZCS} and t_{HZWE} are tested with $C_L = 5$ pF as in *Figure 1b.*
10. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are specified and not 100% tested.

Bit Map



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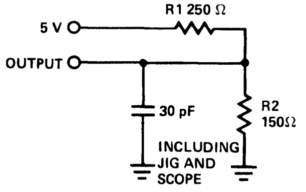
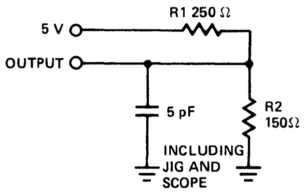
Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

AC Test Loads and Waveforms


R1 250 Ω
5 V
OUTPUT
30 pF
R2
150Ω
INCLUDING
JIG AND
SCOPE

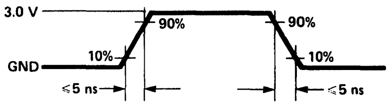

R1 250 Ω
5 V
OUTPUT
5 pF
R2
150Ω
INCLUDING
JIG AND
SCOPE

0006-4

Figure 1a

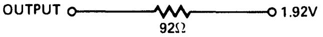
Figure 1b

ALL INPUT PULSES


3.0 V
GND
90%
90%
10%
10%
≤5 ns
≤5 ns

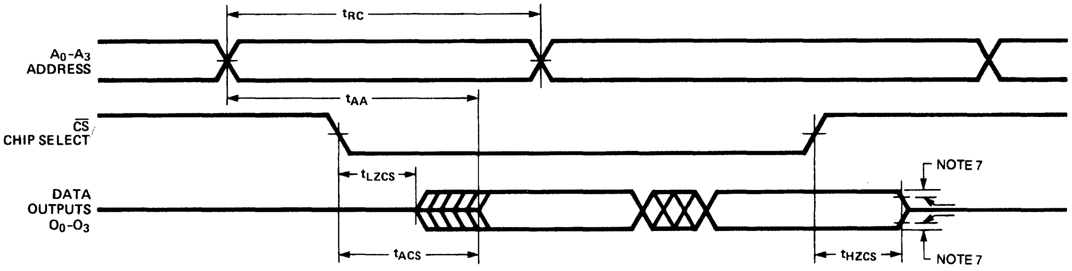
0006-6

Equivalent to: THÉVENIN EQUIVALENT


OUTPUT
92Ω
1.92V

0006-5

Read Mode


t_{RC}
A_0-A_3 ADDRESS
t_{AA}
$\overline{CS}$ CHIP SELECT
t_{LZCS}
DATA OUTPUTS O_0-O_3
NOTE 7
t_{ACS}
t_{HZCS}
NOTE 7

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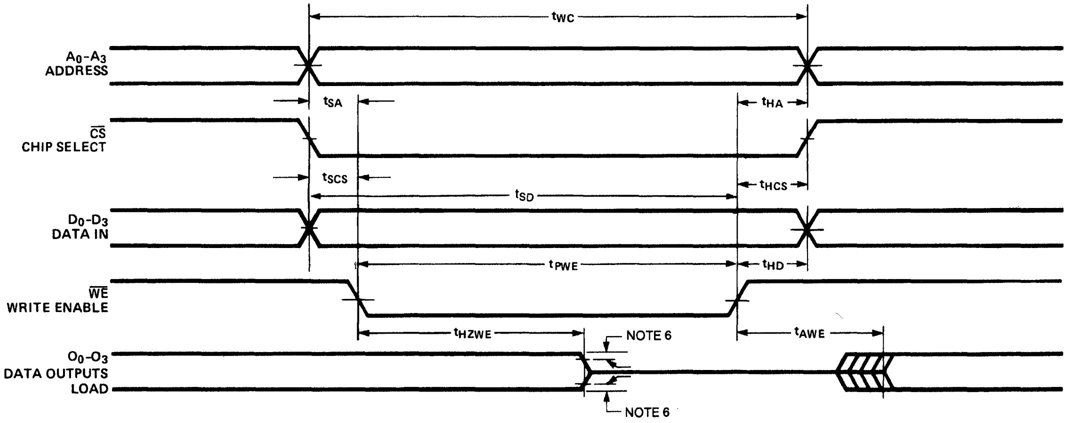
Write Mode


t_{WC}
A_0-A_3 ADDRESS
t_{SA}
t_{HA}
$\overline{CS}$ CHIP SELECT
t_{SCS}
t_{SD}
t_{HCS}
D_0-D_3 DATA IN
t_{PWE}
t_{HD}
$\overline{WE}$ WRITE ENABLE
t_{HZWE}
NOTE 6
t_{AWE}
O_0-O_3 DATA OUTPUTS LOAD
NOTE 6

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(All above measurements referenced to 1.5V)

Note: Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY27S03APC CY27S07APC	P1	Commercial
	CY27S03ADC CY27S07ADC	D2	
	CY27S03ALMB CY27S07ALMB	L61	Military
	CY27S03ADMB CY27S07ADMB	D2	
35	CY27S03PC CY27S07PC CY74S189PC	P1	Commercial
	CY27S03DC CY27S07DC CY74S189DC	D2	
	CY27S03LC CY27S07LC	L61	
	CY27S03LMB CY27S07LMB	L61	Military
	CY27S03DMB CY27S07DMB	D2	
65	CY27LS03LMB	L61	Military
	CY27LS03DMB	D2	

CY93422A/93L422A
CY93422/93L422

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control stores in high speed computer**
- **Processed with high speed CMOS for optimum speed/power**
- **Separate inputs and outputs**
- **Low power**
  - **Standard power:**
    660 mW (commercial)
    715 mW (military)
  - **Low power:**
    440 mW (commercial)
    495 mW (military)
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2000V static discharge**

Functional Description

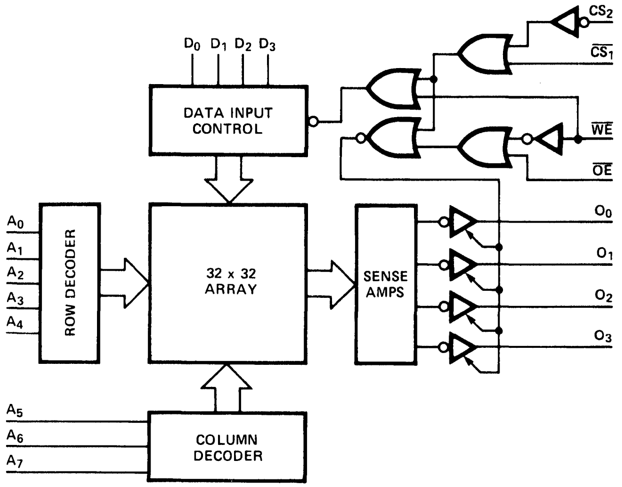
The CY93422 is a high performance CMOS static RAM organized as 256 x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



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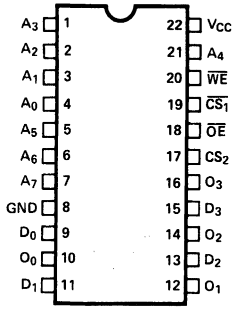
Pin Configuration



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Selection Guide (For higher performance and lower power refer to CY7C122 data sheet)

		93422A	93L422A	93422	93L422
Maximum Access Time (ns)	Commercial	35	45	45	60
	Military	45	55	60	75
Maximum Operating Current (mA)	Commercial	120	80	120	80
	Military	130	90	130	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) .... −0.5V to +7.0V

DC Voltage Applied to Outputs for High Output State .... −0.5V to V_{CC} Max

DC Input Voltage .... −0.5V to +5.5V

Output Current, into Outputs (Low) .... 20 mA

DC Input Current .... −30 mA to +5.0 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	V_{CC}	Ambient Temperature
Commercial	5V ±10%	0°C to +75°C
Military	5V ±10%	−55°C to +125°C

Function Table

Inputs					Outputs	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Select
X	H	X	X	X	*HIGH Z	Not Select
H	L	H	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*HIGH Z	Write “0”
H	L	L	X	H	*HIGH Z	Write “1”

H = High Voltage Level L = Low Voltage Level X = Don’t Care

*HIGH Z implies outputs are disabled or off. This condition is defined as a high impedance state for the CY93422.

DC Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions		93422 93422A Min.	93422 93422A Max.	93L422 93L422A Min.	93L422 93L422A Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −5.2 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 8.0 mA		0.45		0.45	V
V_{IH}	Input HIGH Level[1]	Guaranteed Input Logical HIGH Voltage for all Inputs		2.1		2.1		V
V_{IL}	Input LOW Level[1]	Guaranteed Input Logical LOW Voltage for all Inputs			0.8		0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40V			−300		−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5V			40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]			−90		−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.	T_A = 125°C		110		70	mA
			T_A = 75°C		110		70	
			T_A = 0°C		120		80	
			T_A = −55°C		130		90	
V_{CL}	Input Clamp Voltage			See Note 4		See Note 4		
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V			50		50	μA
		V_{OUT} = 0.5V, V_{CC} = Max.		−50		−50		
C_{IN}	Input Pin Capacitance	See Note 3			4		4	pF
C_{OUT}	Output Pin Capacitance	See Note 3			7		7	pF

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. Input and output capacitance measured on a sample basis at f = 1.0 MHz.
4. The CMOS process does not provide a clamp diode. However, the CY93422 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).

Commercial Switching Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +75°C (Unless Otherwise Noted)

Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[1] $t_{PHL(A)}$[1]	Delay from Address to Output (Address Access Time) (See *Figure 2*)		35		45		45		60	ns
t_{PZH} ($\overline{CS}_1$, CS_2) t_{PZL} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Active Output and Correct Data (See *Figure 2*)		25		30		30		35	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See *Figure 1*)		25		40		40		45	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data (See *Figure 2*)		25		30		30		35	ns
t_s (A)	Setup Time Address (Prior to Initiation of Write) (See *Figure 1*)	5		5		10		10		ns
t_h (A)	Hold Time Address (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s (DI)	Setup Time Data Input (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s ($\overline{CS}_1$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h ($\overline{CS}_1$, CS_2)	Hold Time Chip Select (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write (See *Figure 1*)	20		40		30		45		ns
t_{PHZ} ($\overline{CS}_1$, CS_2) t_{PLZ} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Inactive Output (HIGH Z) (See *Figure 2*)		30		40		30		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (HIGH Z) (See *Figure 1*)		30		40		35		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (HIGH Z) (See *Figure 2*)		30		40		30		45	ns

Notes:

1. t_{PLH} (A) and t_{PHL} (A) are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
2. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS}_1$, CS_2) and t_{PZH} ($\overline{OE}$) are measured with S_1 open, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS}_1$, CS_2) and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$), t_{PHZ} ($\overline{CS}_1$, CS_2) and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, $C_L \leq$ 5 pF and are measured between the 1.5V level on the input to the V_{OH} −500 mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}_1$, CS_2) and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and $C_L \leq$ 5 pF and are measured between the 1.5V level on the input and the V_{OL} +500 mV level on the output.

Military Switching Characteristics $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$ (Unless Otherwise Noted)

Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[1] $t_{PHL(A)}$[1]	Delay from Address to Output (Address Access Time) (See *Figure 2*)		45		55		60		75	ns
t_{PZH} ($\overline{CS}_1$, CS_2) t_{PZL} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Active Output and Correct Data (See *Figure 2*)		35		40		45		45	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See *Figure 1*)		40		45		50		50	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data (See *Figure 2*)		35		40		45		45	ns
t_s (A)	Setup Time Address (Prior to Initiation of Write) (See *Figure 1*)	5		10		10		10		ns
t_h (A)	Hold Time Address (After Termination of Write) (See *Figure 1*)	5		5		5		10		ns
t_s (DI)	Setup Time Data Input (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s ($\overline{CS}_1$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h ($\overline{CS}_1$, CS_2)	Hold Time Chip Select (After Termination of Write) (See *Figure 1*)	5		5		5		10		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write (See *Figure 1*)	35		40		40		45		ns
t_{PHZ} ($\overline{CS}_1$, CS_2) t_{PLZ} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Inactive Output (HIGH Z) (See *Figure 2*)		35		40		45		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (HIGH Z) (See *Figure 1*)		40		40		45		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (HIGH Z) (See *Figure 2*)		35		40		45		45	ns

Notes:

1. t_{PLH} (A) and t_{PHL} (A) are tested with S_1 closed and $C_L = 15$ pF with both input and output timing referenced to 1.5V.
2. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS}_1$, CS_2) and t_{PZH} ($\overline{OE}$) are measured with S_1 open, $C_L = 15$ pF and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS}_1$, CS_2) and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, $C_L = 15$ pF and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$), t_{PHZ} ($\overline{CS}_1$, CS_2) and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, $C_L \leq 5$ pF and are measured between the 1.5V level on the input to the $V_{OH} - 500$ mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}_1$, CS_2) and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5V level on the input and the $V_{OL} + 500$ mV level on the output.

Switching Waveforms

Write Mode (with $\overline{OE}$ = Low)

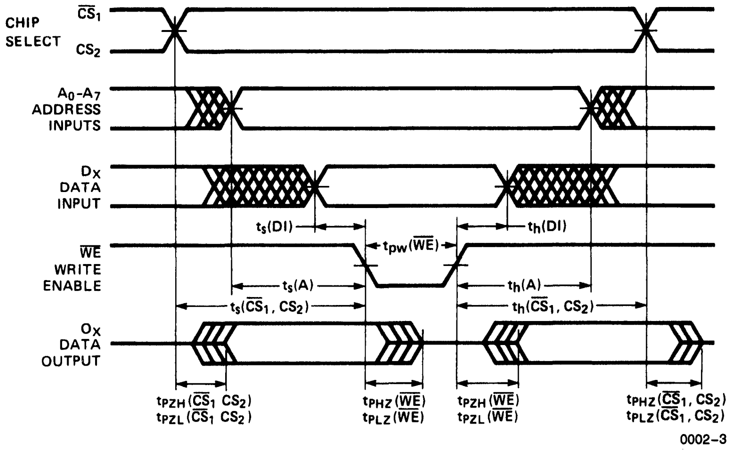
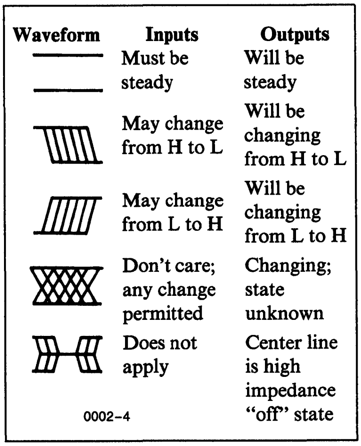

CHIP SELECT
$\overline{CS}_1$
CS_2
A_0-A_7 ADDRESS INPUTS
D_X DATA INPUT
$\overline{WE}$ WRITE ENABLE
O_X DATA OUTPUT
t_s(DI)
t_h(DI)
t_{pw}($\overline{WE}$)
t_s(A)
t_h(A)
t_s($\overline{CS}_1$, CS_2)
t_h($\overline{CS}_1$, CS_2)
t_{PZH}($\overline{CS}_1$ CS_2)
t_{PZL}($\overline{CS}_1$ CS_2)
t_{PHZ}($\overline{WE}$)
t_{PLZ}($\overline{WE}$)
t_{PZH}($\overline{WE}$)
t_{PZL}($\overline{WE}$)
t_{PHZ}($\overline{CS}_1$, CS_2)
t_{PLZ}($\overline{CS}_1$, CS_2)
0002-3

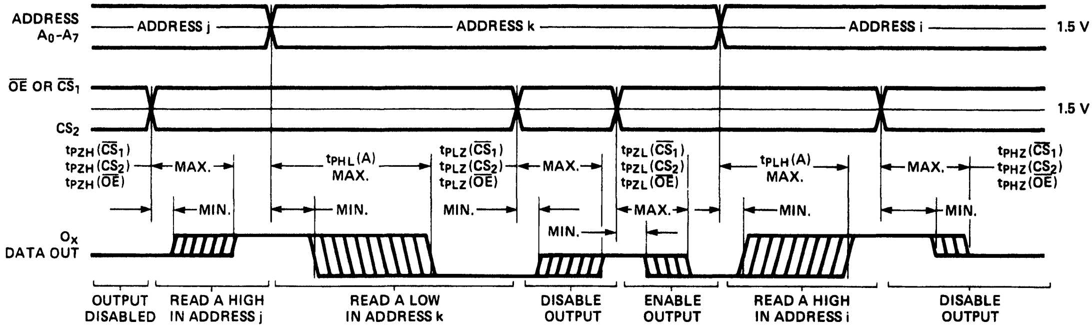
Figure 1

Key to Timing Diagram



Waveform	Inputs	Outputs
—	Must be steady	Will be steady
▥	May change from H to L	Will be changing from H to L
▨	May change from L to H	Will be changing from L to H
▩	Don't care; any change permitted	Changing; state unknown
⋈	Does not apply	Center line is high impedance "off" state

Read Mode


ADDRESS A_0-A_7
ADDRESS j
ADDRESS k
ADDRESS i
1.5 V
$\overline{OE}$ OR $\overline{CS}_1$
CS_2
1.5 V
t_{PZH}($\overline{CS}_1$)
t_{PZH}(CS_2)
t_{PZH}($\overline{OE}$)
MAX.
MIN.
t_{PHL}(A) MAX.
MIN.
t_{PLZ}($\overline{CS}_1$)
t_{PLZ}(CS_2)
t_{PLZ}($\overline{OE}$)
MAX.
MIN.
MIN.
t_{PZL}($\overline{CS}_1$)
t_{PZL}(CS_2)
t_{PZL}($\overline{OE}$)
MAX.
t_{PLH}(A) MAX.
MIN.
MAX.
MIN.
t_{PHZ}($\overline{CS}_1$)
t_{PHZ}(CS_2)
t_{PHZ}($\overline{OE}$)
O_X DATA OUT
OUTPUT DISABLED
READ A HIGH IN ADDRESS j
READ A LOW IN ADDRESS k
DISABLE OUTPUT
ENABLE OUTPUT
READ A HIGH IN ADDRESS i
DISABLE OUTPUT
0002-5

Switching delays from address input, output enable input and the chip select inputs to the data output. The CY93422 disabled output in the "OFF" condition is represented by a single center line.

Figure 2

AC Test Load and Waveform

AC Test Load

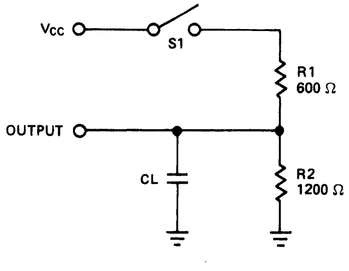

Vcc
S1
R1 600 Ω
OUTPUT
CL
R2 1200 Ω
0002-6

Figure 3

Input Pulses

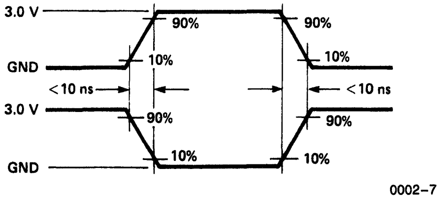

3.0 V
GND
90%
10%
90%
10%
<10 ns
<10 ns
3.0 V
GND
90%
10%
90%
10%
0002-7

Figure 4

See Notes 1 and 2 of Switching Characteristics

Ordering Information

Speed (ns)	Ordering Code		Package Type	Operating Range
	Std. Power	Low Power		
35	CY93422APC CY93422ADC		P7 D8	Commercial
45	CY93422PC CY93422DC	CY93L422APC CY93L422ADC	P7 D8	Commercial
45	CY93422ADMB		D8	Military
55		CY93L422ADMB	D8	Military
60	CY93422DMB		D8	Military
60		CY93L422PC CY93L422DC	P7 D8	Commercial
75		CY93L422DMB	D8	Military

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CY7C245	2048 x 8 Reprogrammable Registered PROM	3-24
CY7C251	16,384 x 8 Reprogrammable Power Switched PROM	3-35
CY7C253	16,384 x 8 Reprogrammable PROM	3-35
CY7C254	16,384 x 8 Reprogrammable PROM	3-35
CY7C261	8192 x 8 Reprogrammable Power Switched PROM	3-44
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Introduction to CMOS PROMs

1: Product Line Overview

The Cypress CMOS family of PROMs span 4K to 256K bit densities, three functional configurations, and are all byte-wide. The product line is available in both 0.3 and 0.6 inch wide dual-in-line plastic and CERDIP as well as LCC and PLCC packages. The programming technology is EPROM and therefore windowed packages are available in both dual-in-line and LCC configurations, providing erasable products. These byte-wide products are available in registered versions at the 512, 1K, 2K, and 8K by 8 densities, and in non-registered versions at the 1K, 2K, 8K, 16K and 32K by 8 densities. The registered devices operate in either synchronous or asynchronous output enable modes and may have an initialize feature to preload the pipeline register. The 8K by 8 registered devices feature a diagnostic shadow register which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at the level of their bipolar equivalents or beyond with reduced power levels of CMOS technology. They are capable of 2001 volts of ESD and operate with 10% power supply tolerances.

2: Technology Introduction

Cypress PROMs are executed in an "N" well 1.2 micron CMOS EPROM process. This process provides basic gate delays of 235 picoseconds for a fanout of one at a power consumption of 45 femto joules. This process provides the basis for the development of LSI products that outperform the fastest bipolar products currently available.

Although CMOS static RAMs have challenged bipolar RAMs for speed, CMOS EPROMs have always been a factor of three to ten times slower than bipolar fuse PROMs. There have been two major limitations on CMOS EPROM speed; 1) the single transistor EPROM cell is inherently slower than the bipolar fuse element, and 2) CMOS EPROM technologies have been optimized for cell programmability and density, almost always at the expense of speed. In the Cypress CMOS EPROM technology, both of the aformentioned limitations have been overcome to create CMOS PROMs with performance superior to PROMs implemented in bipolar technology.

In all Cypress PROMs, speed and programmability are optimized independently by separating the read and write transistor functions. Also, for the first time a substrate bias generator is employed in an EPROM technology to improve performance and raise latchup immunity to greater than 200 mA. The result is a CMOS EPROM technology that challenges bipolar fuse technology for both density and speed. In addition, at higher densities, performance and density surpasses the best that bipolar can provide. Limitations of devices implemented in the bipolar fuse technology such as PROGRAMMING YIELD, POWER DISSIPATION and HIGHER DENSITY PERFORMANCE are eliminated or greatly reduced using Cypress CMOS EPROM technology.

3: Design Approach

A. Four Transistor Differential Memory Cell

The 4K, 8K, and 16K PROM use an N-Well CMOS technology along with a new differential four transistor EPROM cell that is optimized for speed. The area of the four transistor cell is 0.43 square mils and the die size is 19,321 square mils for the 2K by 8 PROM (*Figure 1*). The floating gate cell is optimized for high read current and fast programmability. This is accomplished by separating the read and program transistors (*Figure 2*). The program transistor has a separate implant to maximize the generation and collection of hot electrons while the read transistor implant dose is chosen to provide a large read current. Both the n and p channel peripheral transistors have self-aligned, shallow, lightly doped drain (LDD) junctions. The LDD structure reduces overlap capacitance for speed improvement and minimizes hot electron injection for improved reliability. Although common for NMOS static and dynamic RAMs, an on-chip substrate bias generator is used for the first time in an EPROM technology. The results are improved speed, greater than 200 mA latch-up immunity and high parasitic field inversion voltages during programming.

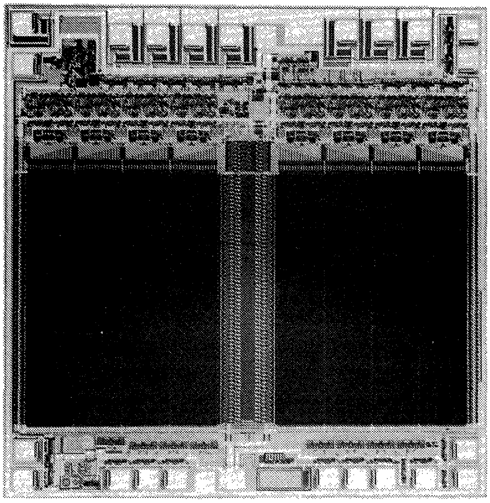
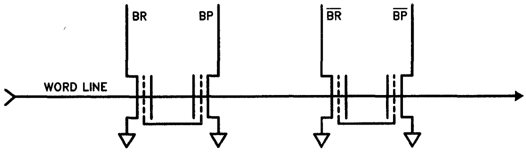

0034-1

Figure 1



0034-2

Figure 2. Non-volatile cell optimized for speed and programmability

Access times of less than 35 ns at 16K densities and 30 ns at 4K and 8K densities over the full operating range are achieved by using differential design techniques and by totally separating the read and program paths. This allows the read path to be optimized for speed. The X and Y decoding paths are predecoded to optimize the power-delay product. A differentail sensing scheme and the four transistor cell are used to sense bit-line swings as low as 100 mV at high speed. The sense amplifier (*Figure 3*) consists of three stages of equal gain. A gain of 4 per stage was found

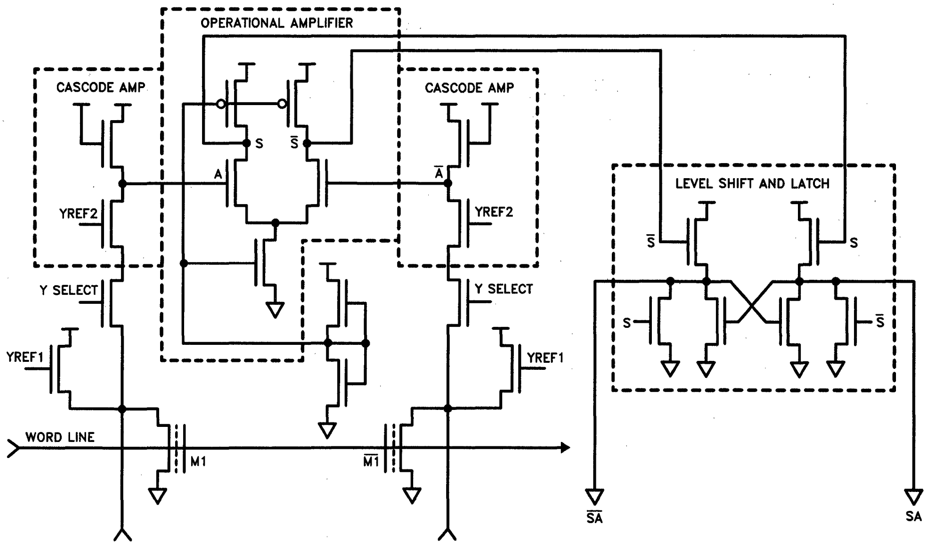


Figure 3. Differential sensing

to be optimum. The Cascode stage amplifies the bit line swings and feeds them into a differential amplifier. The output of the differential amplifier is further amplified and voltages shifted by a level shifter and latch. This signal is then fed into an output buffer having a TTL fan-out of ten.

B. Two Transistor Single Ended Memory Cell

At higher densities, the four transistor memory cell becomes too large and would create a die that is more expensive and difficult to package. For this reason, all 8K by 8 and larger PROMs from Cypress use a two transistor memory cell and single ended sensing. This is an excellent compromise between performance and high density, allowing the development of devices with performance of 35 ns and 45 ns access times at densities from 64K to 256K bits. This two transistor cell still uses the high speed read transistor and the optimized EPROM transistor for performance and reliable programming. The sense amplifier uses a reference voltage on one input and the read transistor on the other, instead of two read transistors. This single ended sensing is a more conventional technique and has the effect of causing an erased device to contain all "0"s.

4: Programming

A. Differential Memory Cells

Cypress PROMs are programmed a BYTE at a time by applying 12 to 14 volts on one pin and the desired logic levels to input pins. Both logic "ONE" and logic "ZERO" are programmed into the differential cell. A BIT is programmed by applying 12 to 14 volts on the control gate and 9 volts on the drain of the floating gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is enough to be determined as the correct logic state. Because an unprogrammed cell has neither a ONE nor a ZERO in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual BITs allowing the monitoring of the quality of programming during the manufacturing operation.

B. Single Ended Memory Cells

The programming mechanism of the EPROM transistor in a single ended memory cell is the same as its counterpart in a double ended memory cell. The difference is that only ones "1"s are programmed in a single ended cell. A "1" applied to the I/O pin during programming causes an erased EPROM transistor to be programmed while a "0" allows the EPROM transistor to remain unprogrammed.

5: Erasability

For the first time at PROM speeds, Cypress PROMs using CMOS EPROM technology offer reprogrammability when packaged in windowed CERDIP. This is available at densities of 16K and larger, both registered and non-registered.

Wavelengths of light less than 4000 Angstroms begin to erase Cypress PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30–35 minutes.

The PROM needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

6: Reliability

The CMOS EPROM approach to PROMs has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed and erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each CMOS PROM contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged thus assuring the user that not only will every cell program, but that the product performs to the specification.

CYPRESS
SEMICONDUCTOR

CY7C225

512 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered Common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP, or 28 pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

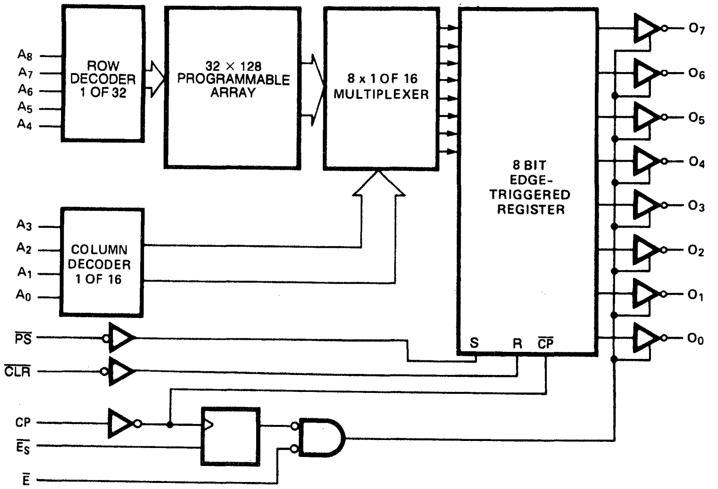
Product Characteristics

The CY7C225 is a high performance 512 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP and 28 pin Leadless Chip Carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C225 has asynchronous PRESET and CLEAR functions.

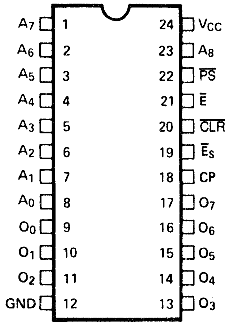
Logic Block Diagram



A8
A7
A6
A5
A4
ROW DECODER 1 OF 32
32 × 128 PROGRAMMABLE ARRAY
8 x 1 OF 16 MULTIPLEXER
8 BIT EDGE-TRIGGERED REGISTER
S
R
$\overline{\text{CP}}$
O7
O6
O5
O4
O3
O2
O1
O0
A3
A2
A1
A0
COLUMN DECODER 1 OF 16
$\overline{\text{PS}}$
$\overline{\text{CLR}}$
CP
$\overline{\text{E}}_S$
$\overline{\text{E}}$

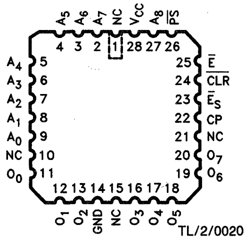
0020-1

Pin Configurations



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 $\overline{\text{PS}}$
21 $\overline{\text{E}}$
20 $\overline{\text{CLR}}$
19 $\overline{\text{E}}_S$
18 CP
17 O7
16 O6
15 O5
14 O4
13 O3

0020-2



A5 A6 A7 NC VCC A8 $\overline{\text{PS}}$
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 $\overline{\text{E}}$
24 $\overline{\text{CLR}}$
23 $\overline{\text{E}}_S$
22 CP
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

TL/2/0020-11

Selection Guide

		7C225-25	7C225-30	7C225-35	7C225-40
Maximum Set-up Time (ns)		25	30	35	40
Maximum Clock to Ouput (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90		90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 1				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF

Notes:

1. The CMOS process does not provide a clamp diode. However, the CY7C225 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Input and output capacitance measured on a sample basis.

Switching Characteristics Over Operating Range

Parameters	Description	7C225-25		7C225-30		7C225-35		7C225-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	10		10		10		10		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	0		5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ to Valid Output		20		20		20		20	ns
t_{RP}, t_{RC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Pulse Width	15		20		20		20		ns
t_{LZC}	Active Output from Clock HIGH[1]		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		20		25		30	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		20		25		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms[5, 6, 7]

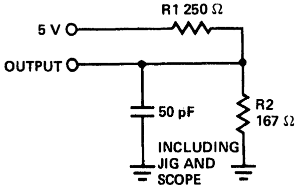


Figure 1a

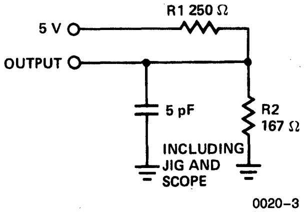


Figure 1b

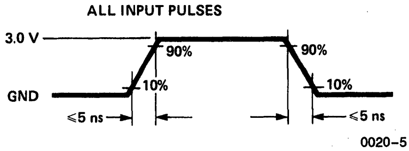
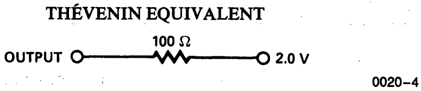


Figure 2

Equivalent to:



Functional Description

The CY7C225 is a CMOS electrically Programmable Read Only Memory organized as 512 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables, and $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address inputs (A_0–A_8) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

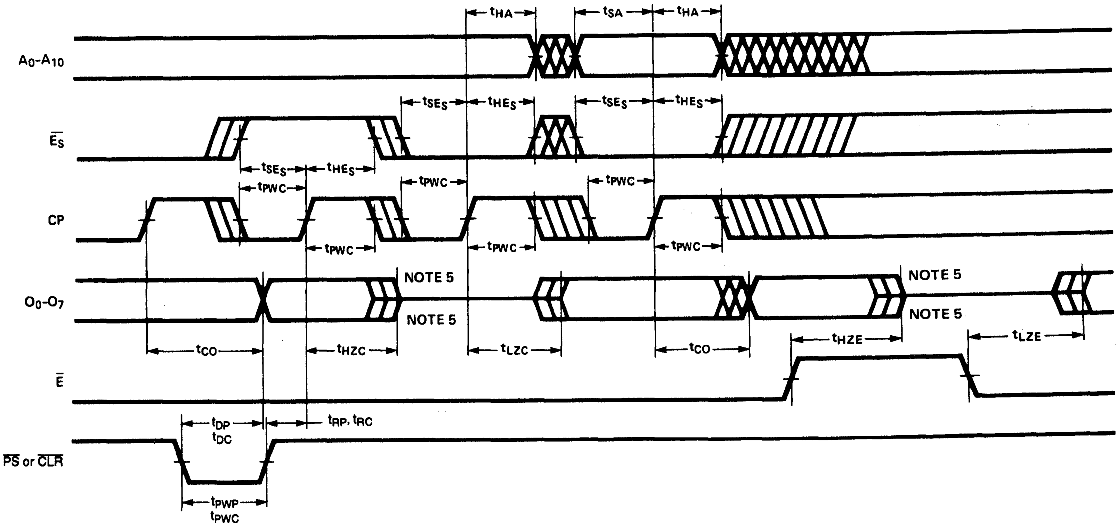
Regardless of the condition of Ē, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if Ē is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225 has buffered asynchronous $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences.

Applying a LOW to the $\overline{\text{PRESET}}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{\text{CLEAR}}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (Ē) LOW.

Switching Waveforms



0020-6

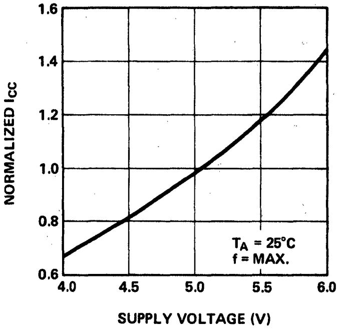
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

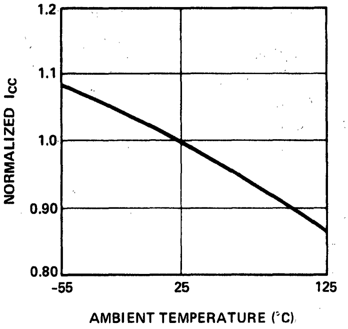
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

Typical DC and AC Characteristics

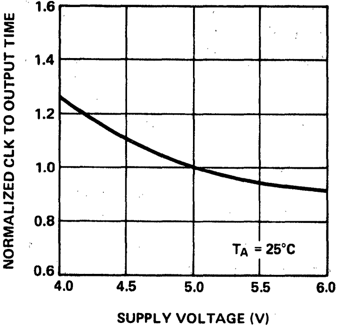
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



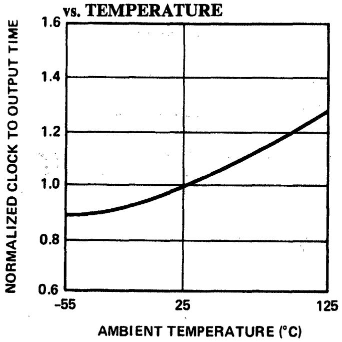
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



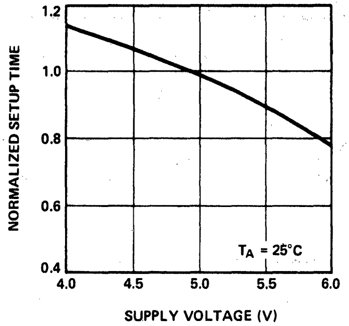
CLOCK TO OUTPUT TIME vs. V_{CC}



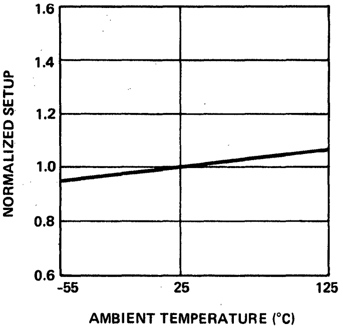
CLOCK TO OUTPUT TIME vs. TEMPERATURE



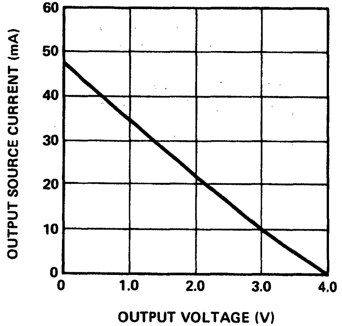
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



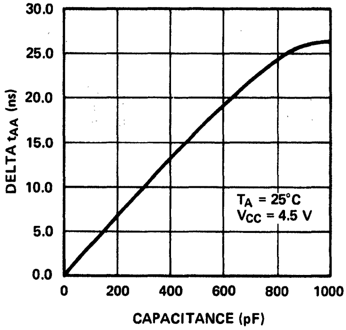
NORMALIZED SETUP TIME vs. TEMPERATURE



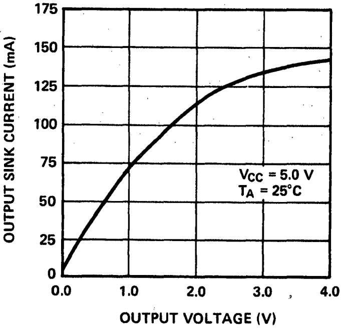
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0020-7

Device Programming

Overview:

There is a programmable function contained in the 7C225 CMOS 512 x 8 Registered PROM; the 512 x 8 array. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped.

The 512 x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	50		ns
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

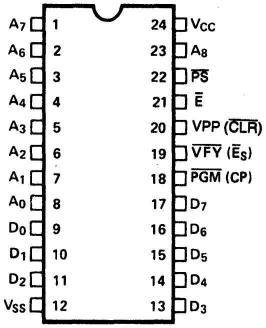
Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11,13–17)
	Read or Output Disable	CP	$\overline{E_S}$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	
	Pin	(18)	(19)	(20)	(21)	(22)	
Read[2,3]		X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out
Output Disable[5]		X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		X	X	V_{IH}	V_{IH}	V_{IH}	High Z
$\overline{\text{CLEAR}}$		X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
$\overline{\text{PRESET}}$		X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program[1,4]		V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	Data In
Program Verify[1,4]		V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	Data Out
Program Inhibit[1,4]		V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program[1,4]		V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	Data In
Blank Check Ones[1,4]		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	Ones
Blank Check Zeros[1,4]		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0020-8

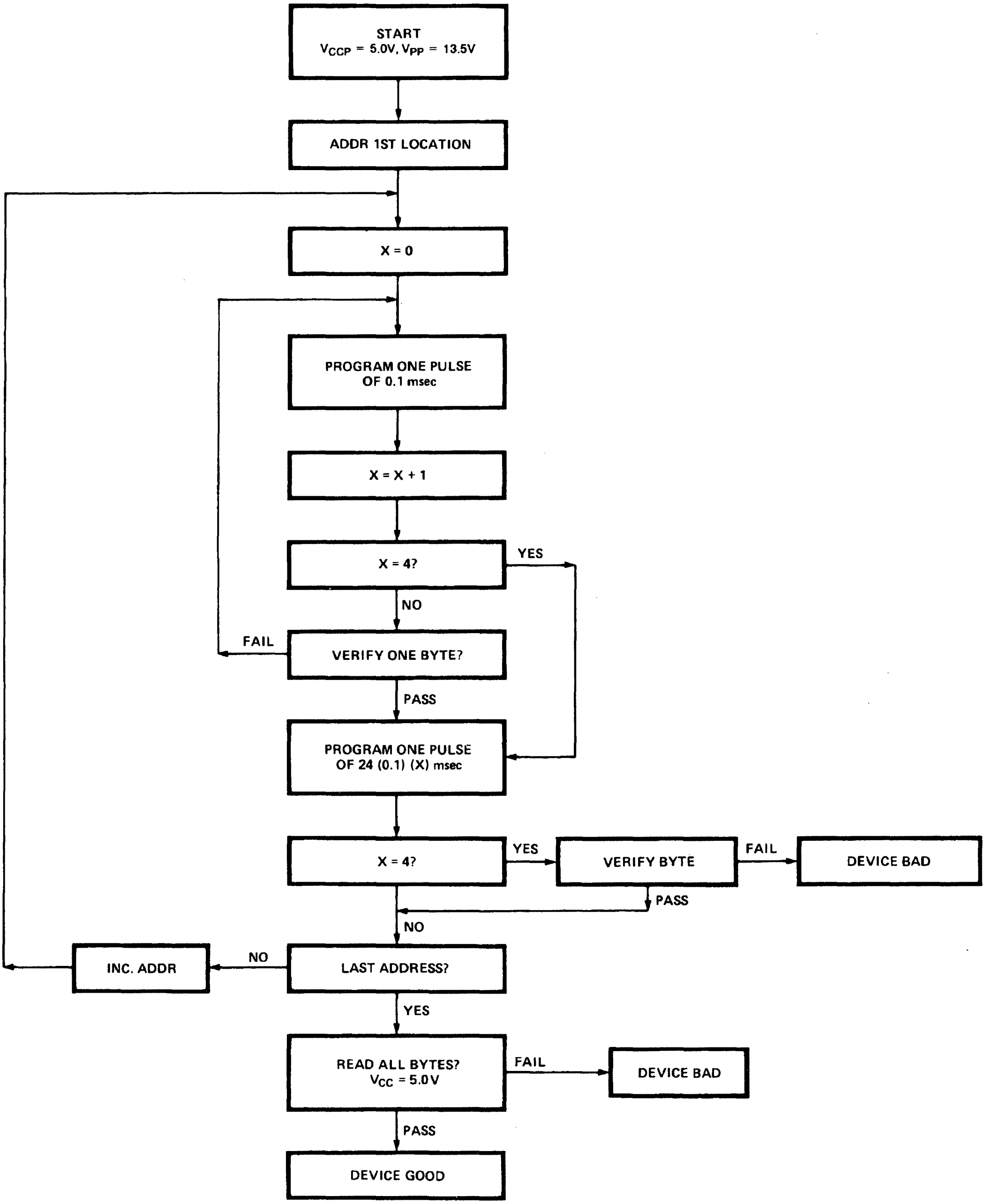
Figure 3. Programming Pinouts

The CY7C225 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.


START
V_{CCP} = 5.0V, V_{PP} = 13.5V
ADDR 1ST LOCATION
X = 0
PROGRAM ONE PULSE OF 0.1 msec
X = X + 1
X = 4?
YES
NO
FAIL
VERIFY ONE BYTE?
PASS
PROGRAM ONE PULSE OF 24 (0.1) (X) msec
X = 4?
YES
VERIFY BYTE
FAIL
DEVICE BAD
PASS
NO
INC. ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? V_{CC} = 5.0V
FAIL
DEVICE BAD
PASS
DEVICE GOOD

0020–9

Figure 4. Programming Flowchart

Programming Sequence 512 x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figure 5*. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 511. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

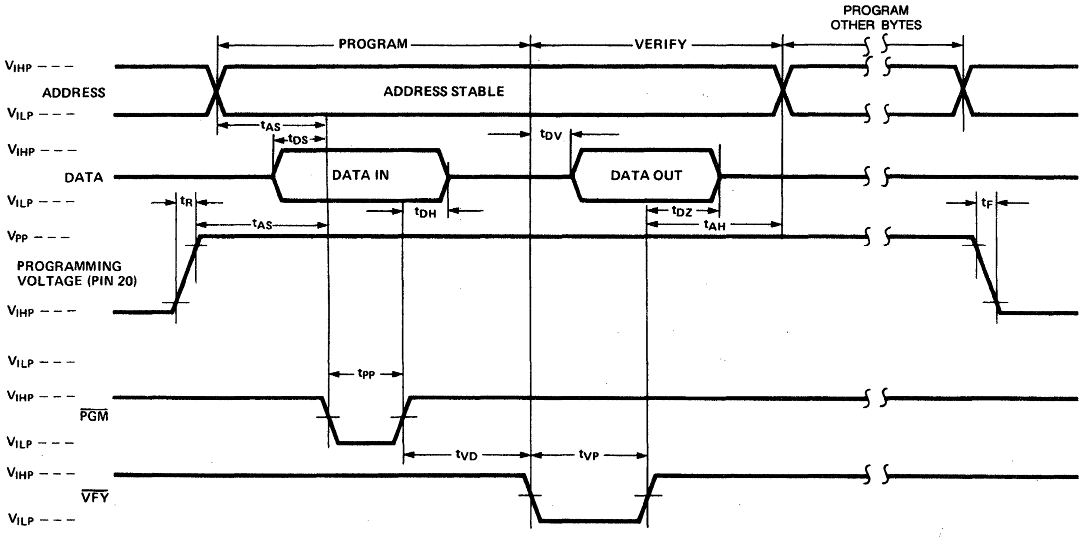

PROGRAM OTHER BYTES
PROGRAM
VERIFY
V_IHP
ADDRESS
ADDRESS STABLE
V_ILP
tAS
tDS
tDV
V_IHP
DATA
DATA IN
DATA OUT
V_ILP
tR
tDH
tDZ
tAS
tAH
tF
V_PP
PROGRAMMING VOLTAGE (PIN 20)
V_IHP
V_ILP
tPP
V_IHP
PGM
V_ILP
tVD
tVP
V_IHP
VFY
V_ILP
0020-10

Figure 5. PROM Programming Waveforms

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
25	12	CY7C225-25PC CY7C225-25DC CY7C225-25LC	P13 D14 L64	Commercial
30	15	CY7C225-30PC CY7C225-30DC CY7C225-30LC	P13 D14 L64	Commercial
		CY7C225-30DMB CY7C225-30LMB	D14 L64	Military
35	20	CY7C225-35DMB CY7C225-35LMB	D14 L64	Military
40	25	CY7C225-40PC CY7C225-40DC CY7C225-40LC	P13 D14 L64	Commercial
		CY7C225-40DMB CY7C225-40LMB	D14 L64	Military

CYPRESS SEMICONDUCTOR

CY7C235

1024 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 30 ns max set-up**
  - **— 15 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{\text{INIT}}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP or 28 pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

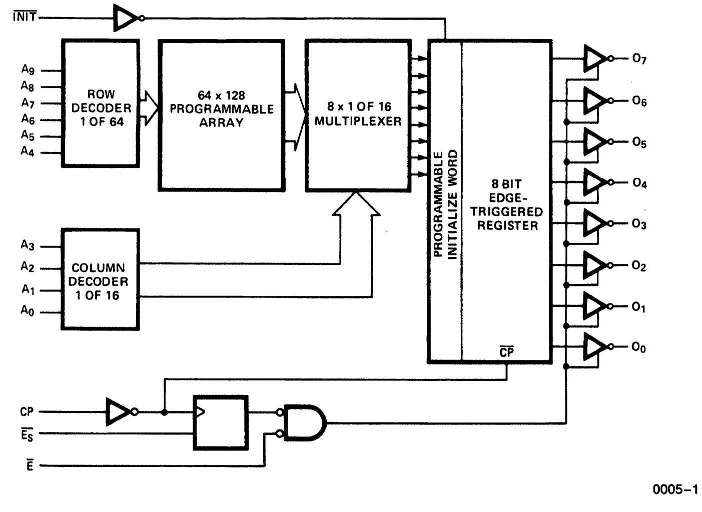
Product Characteristics

The CY7C235 is a high performance 1024 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP or 28-pin Leadless Chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C235 has an asynchronous initialize function ($\overline{\text{INIT}}$). This function acts as a 1025th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

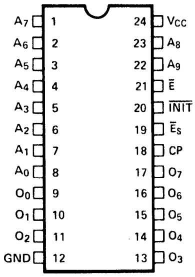
Logic Block Diagram



INIT
A9
A8
A7
A6
A5
A4
ROW DECODER 1 OF 64
64 x 128 PROGRAMMABLE ARRAY
8 x 1 OF 16 MULTIPLEXER
PROGRAMMABLE INITIALIZE WORD
8 BIT EDGE-TRIGGERED REGISTER
CP
O7
O6
O5
O4
O3
O2
O1
O0
A3
A2
A1
A0
COLUMN DECODER 1 OF 16
CP
ES
E

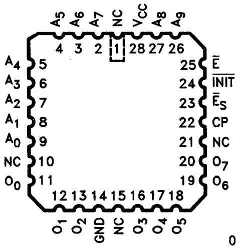
0005-1

Pin Configuration



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 E
20 INIT
19 ES
18 CP
17 O7
16 O6
15 O5
14 O4
13 O3

0005-2



A5 A6 A7 NC VCC A8 A9
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 E
24 INIT
23 ES
22 CP
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

0005-12

Selection Guide

		7C235-30	7C235-40
Maximum Set-up Time (ns)		30	40
Maximum Clock to Output (ns)		15	20
Maximum Operating Current (mA)	Commercial	90	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Volume .... >2001V
(Per MIL-STD-883 Method 3015.2)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 1				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. The CMOS process does not provide a clamp diode. However, the CY7C235 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Input and output capacitance measured on a sample basis.

Switching Characteristics Over Operating Range

Parameters	Description	7C235-30		7C235-40		Units
		Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		ns
t_{CO}	Clock HIGH to Valid Output		15		20	ns
t_{PWC}	Clock Pulse Width	15		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	10		15		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		ns
t_{DI}	Delay from $\overline{\text{INIT}}$ to Valid Output		25		35	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock HIGH	20		20		ns
t_{PWI}	$\overline{\text{INIT}}$ Pulse Width	20		25		ns
t_{LZC}	Active Output from Clock HIGH[1]		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		25	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		25	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b.*
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms [5, 6, 7]

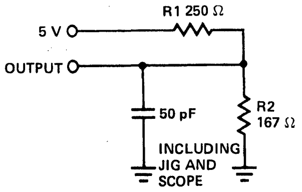


Figure 1a

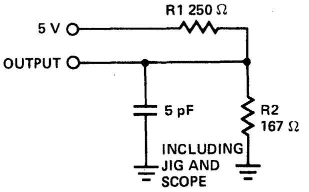


Figure 1b

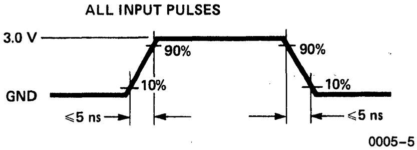
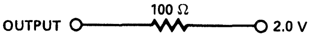


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



Functional Description

The CY7C235 is a CMOS electrically Programmable Read Only Memory organized as 1024 word x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C235 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{\text{INIT}}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0-O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address input (A_0-A_9) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0-O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

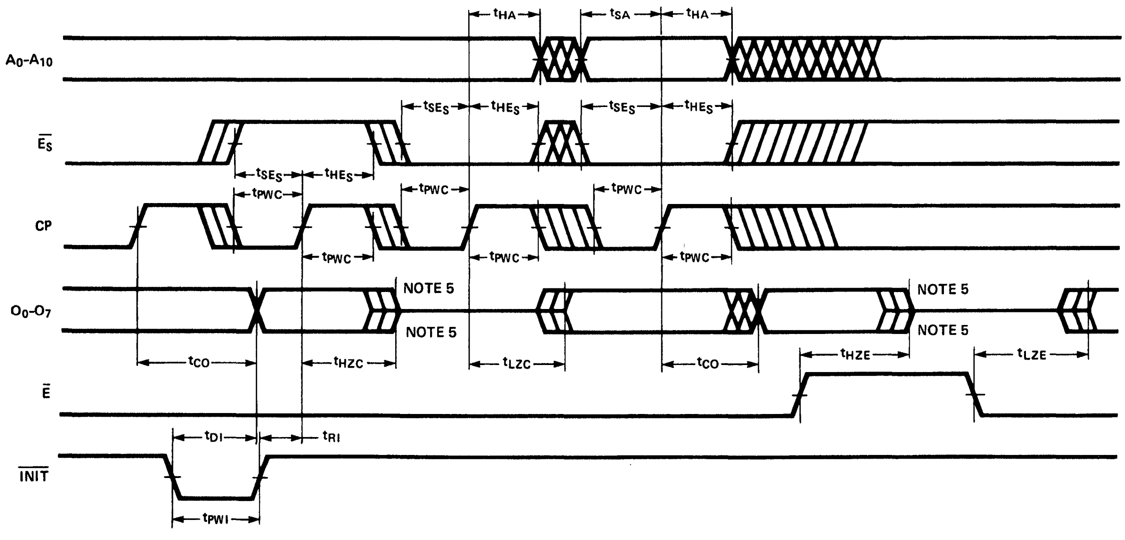
Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



0005-6

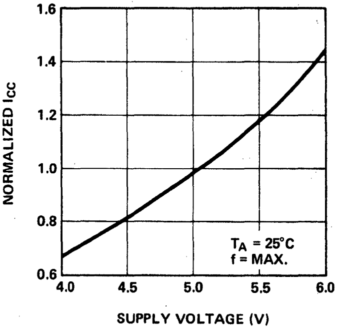
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

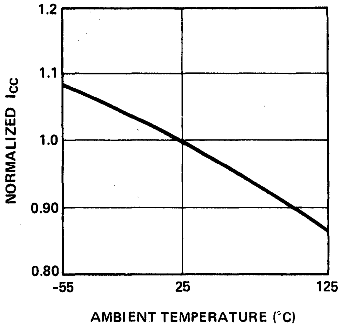
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

Typical DC and AC Characteristics

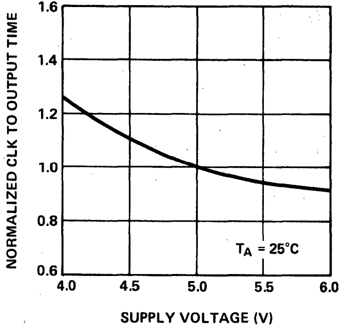
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



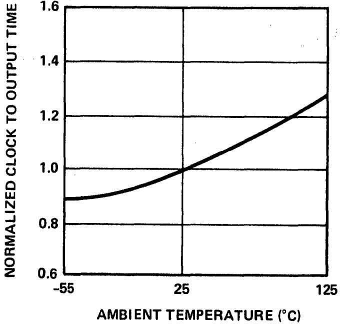
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



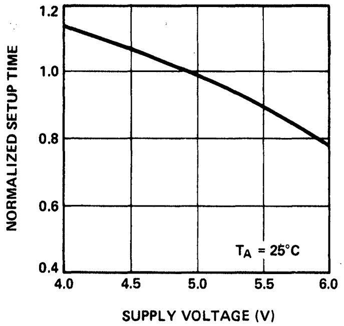
CLOCK TO OUTPUT TIME vs. V_{CC}



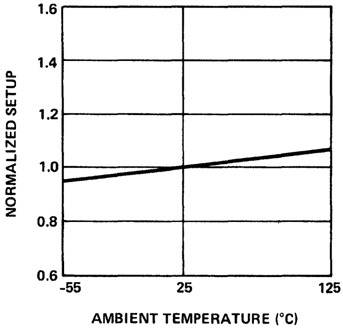
CLOCK TO OUTPUT TIME vs. TEMPERATURE



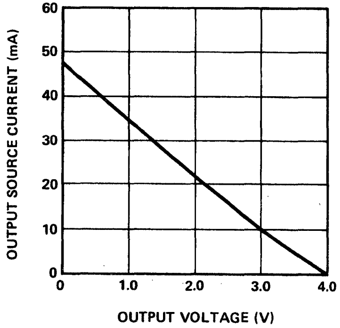
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



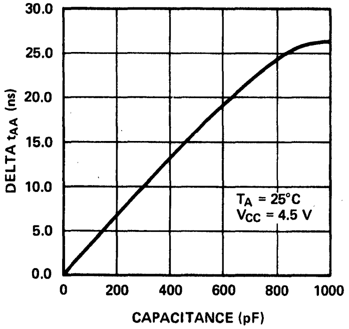
NORMALIZED SETUP TIME vs. TEMPERATURE



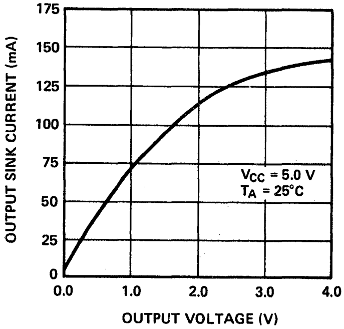
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0005–7

Device Programming

Overview:

There are two independent programmable functions contained in the 7C235 CMOS 1K x 8 Registered PROM; the 1K x 8 array, and the INITIAL BYTE. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally through the use of the initialize function. The 1K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

3

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

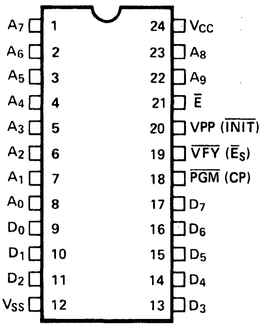
Mode Selection

Table 3

Mode		Pin Function						Outputs (9–11, 13–17)
	Read or Output Disable	**A_2**	**CP**	**$\overline{E_S}$**	**$\overline{INIT}$**	**$\overline{E}$**	**A_1**	
	Other	**A_2**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**$\overline{E}$**	**A_1**	
	Pin	**(6)**	**(18)**	**(19)**	**(20)**	**(21)**	**(7)**	
Read[2,3]		X	X	V_{IL}	V_{IH}	V_{IL}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	X	High Z
Output Disable		X	X	X	V_{IH}	V_{IH}	X	High Z
Initialize		X	X	X	V_{IL}	V_{IL}	X	1025th word
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	X	Data In
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	X	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0005-8

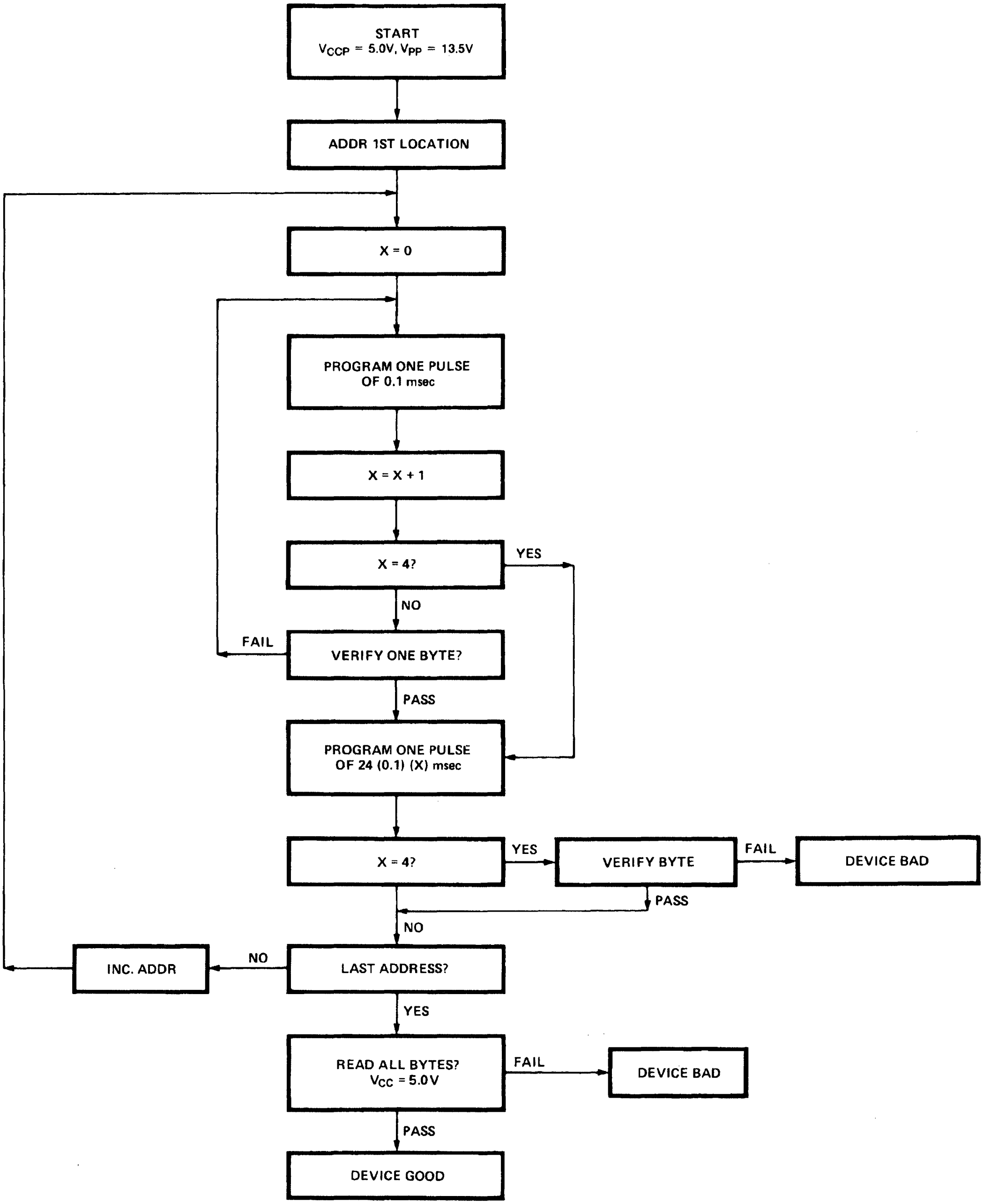
Figure 3. Programming Pinouts

The CY7C235 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.


START
V_{CCP} = 5.0V, V_{PP} = 13.5V
ADDR 1ST LOCATION
X = 0
PROGRAM ONE PULSE OF 0.1 msec
X = X + 1
X = 4?
YES
NO
FAIL
VERIFY ONE BYTE?
PASS
PROGRAM ONE PULSE OF 24 (0.1) (X) msec
X = 4?
YES
VERIFY BYTE
FAIL
DEVICE BAD
PASS
NO
INC. ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? V_{CC} = 5.0V
FAIL
DEVICE BAD
PASS
DEVICE GOOD

0005–9

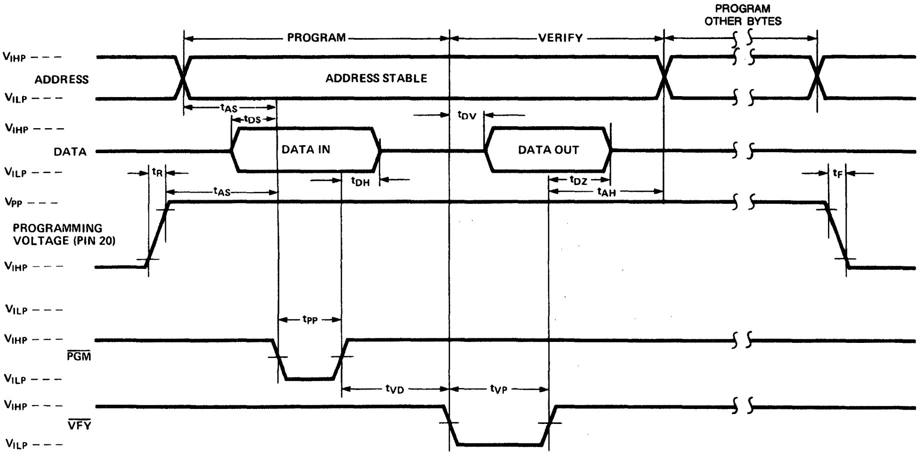
Figure 4. Programming Flowchart

Programming Sequence 1K x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 6* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 6* address program and verify one byte of data. Repeat this for each location to be programmed.

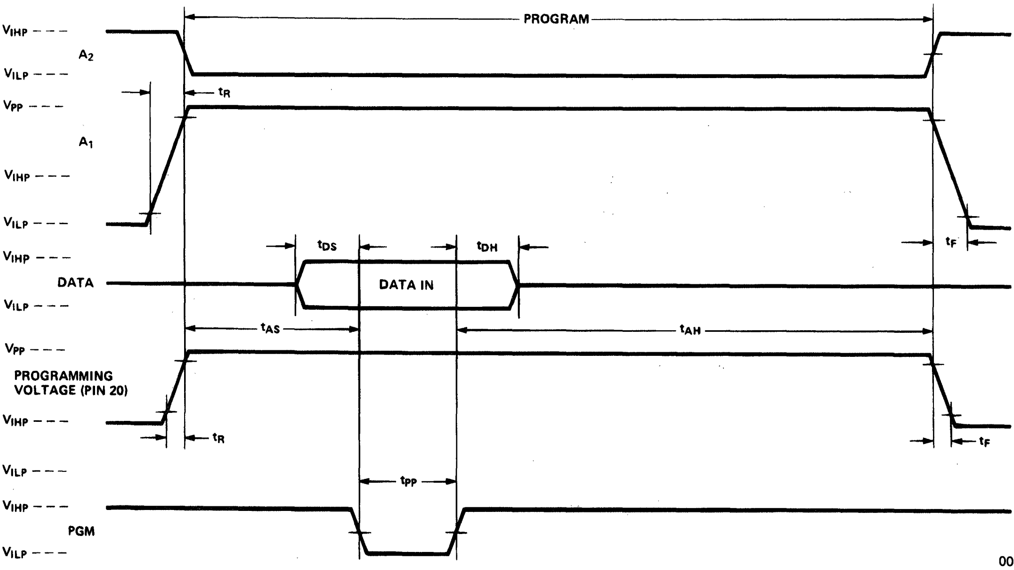
If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.


PROGRAM OTHER BYTES
PROGRAM
VERIFY
VIHP
ADDRESS
VILP
ADDRESS STABLE
tAS
tDS
tDV
VIHP
DATA
DATA IN
DATA OUT
VILP
tR
tDH
tF
tAS
tDZ
tAH
VPP
PROGRAMMING VOLTAGE (PIN 20)
VIHP
VILP
tPP
VIHP
PGM
VILP
tVD
tVP
VIHP
VFY
VILP

0005-10

Figure 5. PROM Programming Waveforms


PROGRAM
VIHP
A2
VILP
tR
VPP
A1
VIHP
VILP
tDS
tDH
tF
VIHP
DATA
DATA IN
VILP
tAS
tAH
VPP
PROGRAMMING VOLTAGE (PIN 20)
VIHP
tR
tF
VILP
tPP
VIHP
PGM
VILP

0005-11

Figure 6. Initial Byte Programming Waveforms

Programming the Initial Byte

The CY7C235 registered PROM has a 1025th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 1025th byte. This byte is programmed in a similar manner to the 1024 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
30	15	CY7C235-30PC CY7C235-30DC CY7C235-30LC	P13 D14 L64	Commercial
40	20	CY7C235-40PC CY7C235-40DC CY7C235-40LC	P13 D14 L64	
		CY7C235-40DMB CY7C235-40LMB	D14 L64	Military

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1's" and "0's" when addresses in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

CYPRESS SEMICONDUCTOR

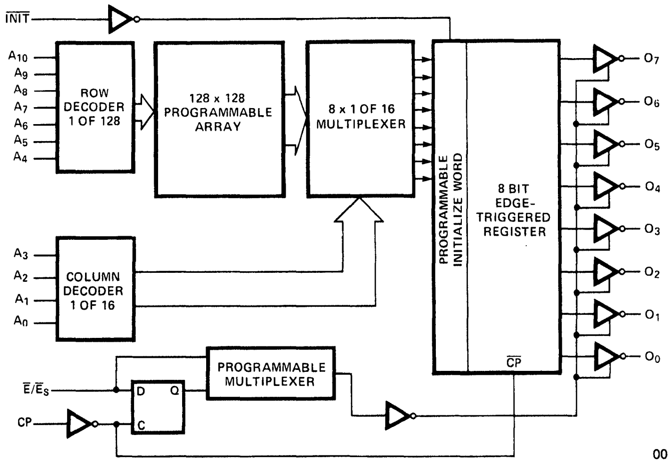
CY7C245

Reprogrammable 2048 x 8 Registered PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 330 mW (commercial) for −35 ns, −45 ns**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register (INIT)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

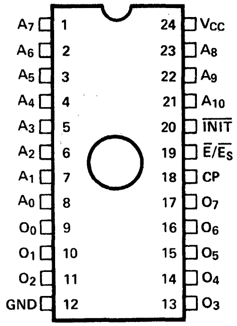
Logic Block Diagram



INIT
A10
A9
A8
A7
A6
A5
A4
ROW DECODER 1 OF 128
128 x 128 PROGRAMMABLE ARRAY
8 x 1 OF 16 MULTIPLEXER
PROGRAMMABLE INITIALIZE WORD
8 BIT EDGE-TRIGGERED REGISTER
CP
O7
O6
O5
O4
O3
O2
O1
O0
A3
A2
A1
A0
COLUMN DECODER 1 OF 16
PROGRAMMABLE MULTIPLEXER
E/ES
CP
D
Q
C

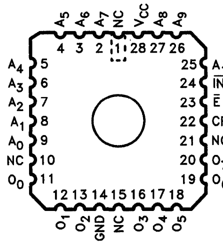
0016-1

Pin Configurations



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 INIT
19 E/ES
18 CP
17 O7
16 O6
15 O5
14 O4
13 O3

0016-2



A5 A6 A7 NC VCC A8 A9
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 A10
24 INIT
23 E
22 CP
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

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Selection Guide

			7C245-25	7C245-35	7C245-45
Maximum Setup Time (ns)			25	35	45
Maximum Clock to Output (ns)			12	15	25
Maximum Operating Current (mA)	STD	Commercial	90	90	90
		Military		120	120
	L	Commercial		60	60

Product Characteristics

The CY7C245 is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245 replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function ($\overline{\text{INIT}}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

UV Erasure .... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C245L-35, 45		7C245-25		7C245-35, 45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA $V_{IN} = V_{IH}$ or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5		Note 5						
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[3]		−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		60		90		90	mA
			Military						120	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. Input and output capacitance measured on a sample basis.
5. The CMOS process does not provide a clamp diode. However, the CY7C245 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).

Switching Characteristics Over Operating Range

Parameters	Description	7C245-25		7C245-35		7C245-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	12		15		15		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{\text{INIT}}$ to Valid Output		20		20		35	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock HIGH	15		20		20		ns
t_{PWI}	$\overline{\text{INIT}}$ Pulse Width	15		20		25		ns
t_{LZC}	Active Output from Clock HIGH[1]		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		15		20		30	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		15		20		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b.*
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms[5, 6, 7]

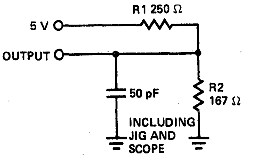


Figure 1a

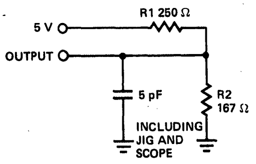


Figure 1b

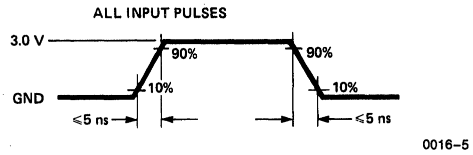
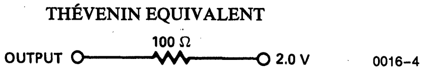


Figure 2

Equivalent to:



Functional Description

The CY7C245 is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{\text{INIT}}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a

Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

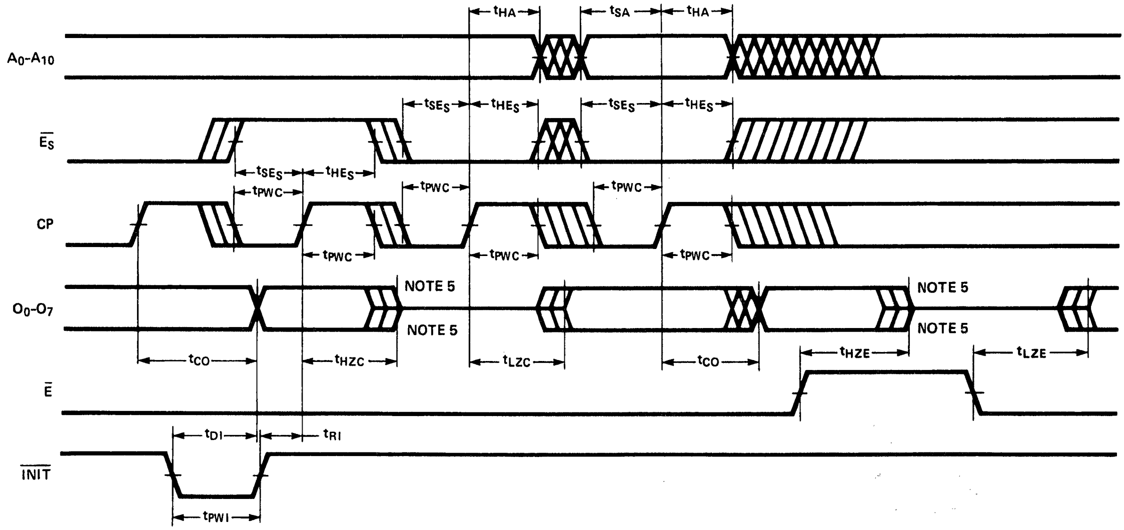
If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245 has an asynchronous initialize input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{\text{INIT}}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{\text{INIT}}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{\text{INIT}}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



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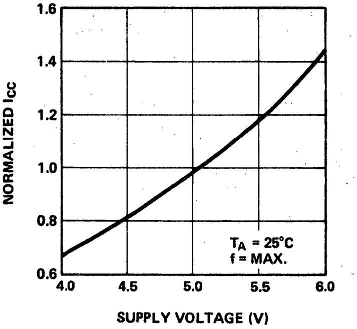
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

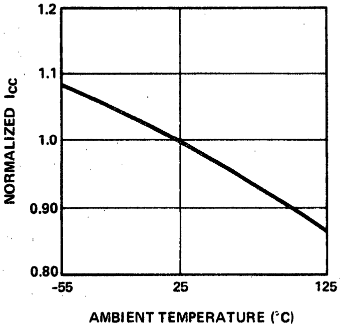
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

Typical DC and AC Characteristics

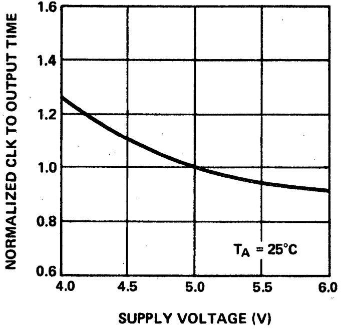
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



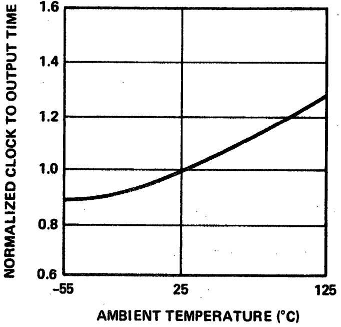
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



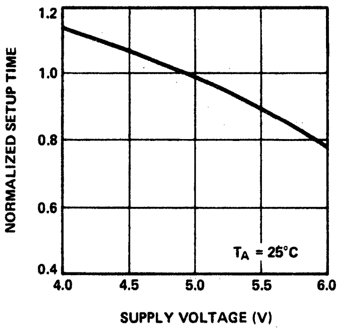
CLOCK TO OUTPUT TIME vs. V$_{CC}$



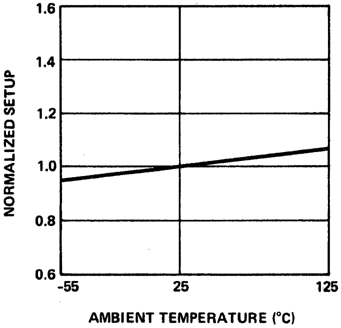
CLOCK TO OUTPUT TIME vs. TEMPERATURE



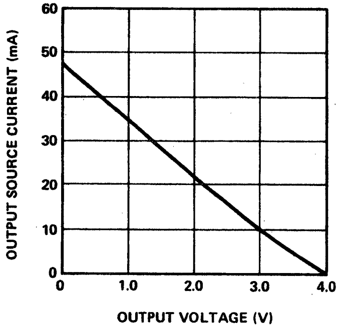
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



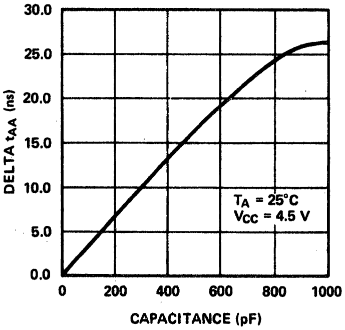
NORMALIZED SETUP TIME vs. TEMPERATURE



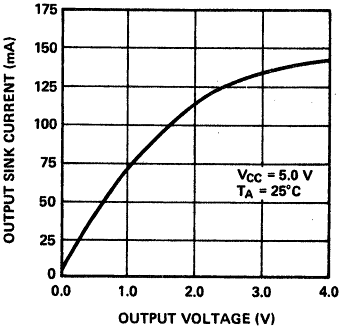
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0016-7

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30–35 minutes. The 7C245 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

OVERVIEW:

There are three independent programmable functions contained in the 7C245 CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The 2K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	Vpp Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

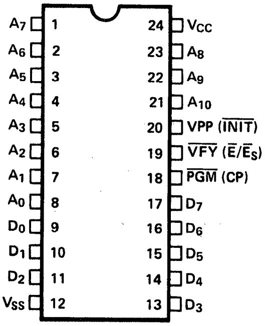
Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11, 13–17)
	Read or Output Disable	**A_2**	**CP**	**$\overline{E}/\overline{E}_S$**	**$\overline{INIT}$**	**A_1**	
	Other	**A_2**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**A_1**	
	Pin	**(6)**	**(18)**	**(19)**	**20**	**(7)**	
Read[2,3]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	High Z
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Synch Enable[4]		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	X	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0016–8

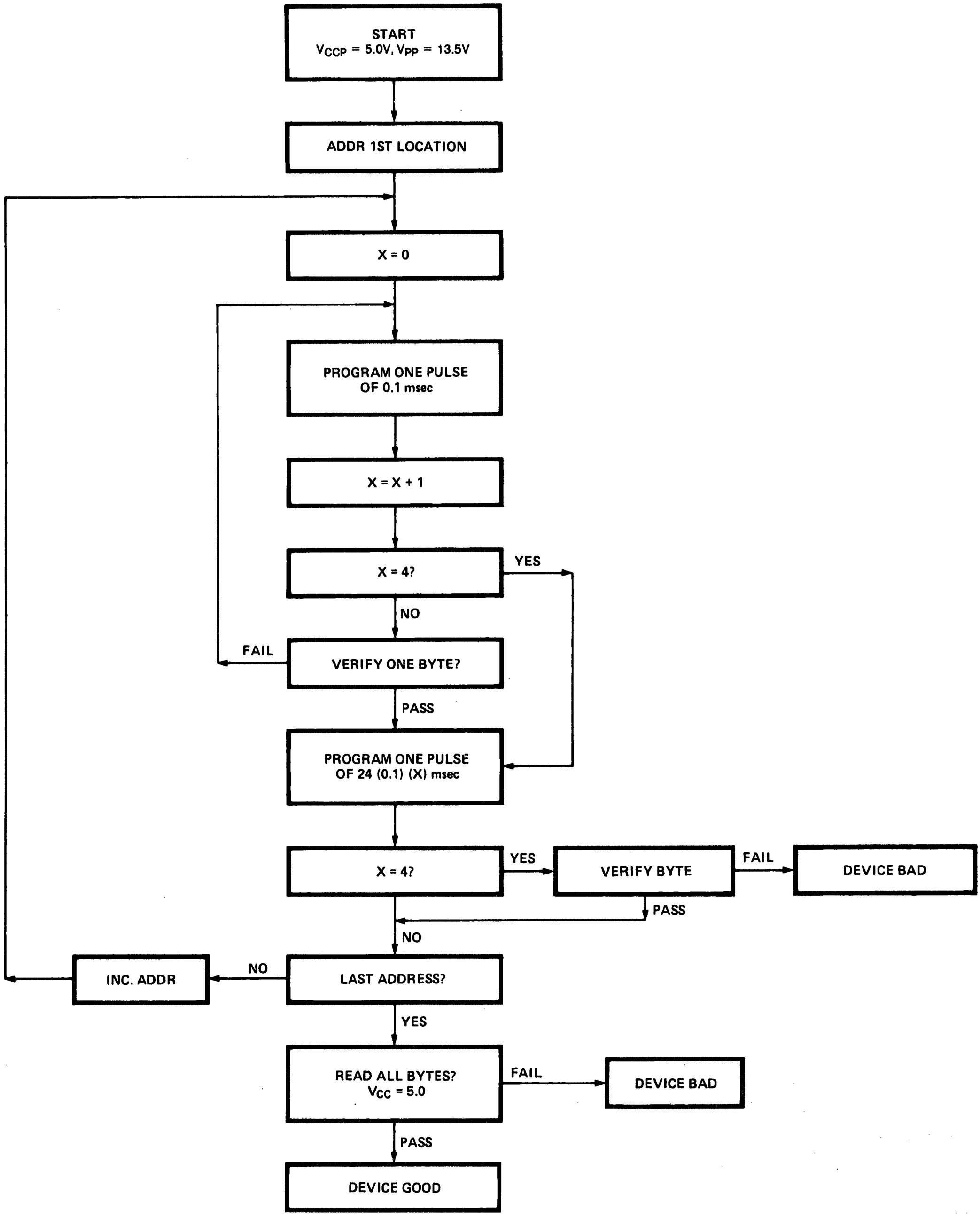
Figure 3. Programming Pinouts

The CY7C245 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.


START
V_{CCP} = 5.0V, V_{PP} = 13.5V
ADDR 1ST LOCATION
X = 0
PROGRAM ONE PULSE OF 0.1 msec
X = X + 1
X = 4?
YES
NO
FAIL
VERIFY ONE BYTE?
PASS
PROGRAM ONE PULSE OF 24 (0.1) (X) msec
X = 4?
YES
VERIFY BYTE
FAIL
DEVICE BAD
PASS
NO
INC. ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? V_{CC} = 5.0
FAIL
DEVICE BAD
PASS
DEVICE GOOD

0016–9

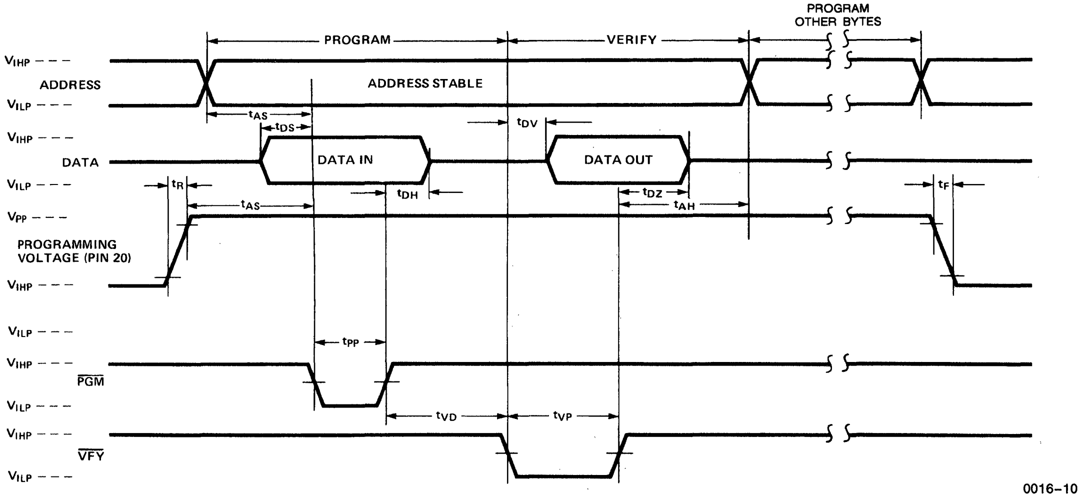
Figure 4. Programming Flowchart

Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

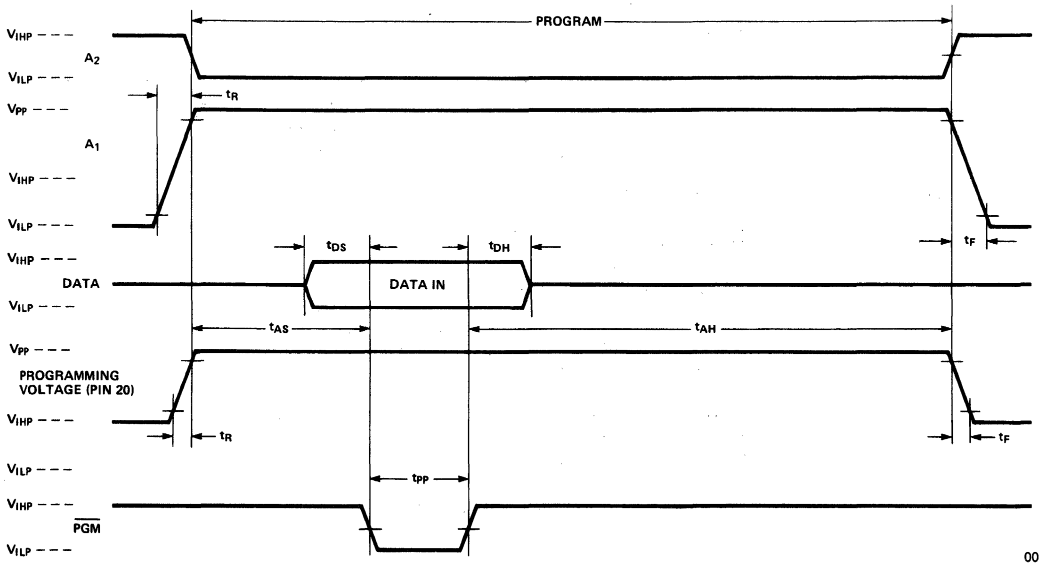
If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.


PROGRAM
VERIFY
PROGRAM OTHER BYTES
VIHP
ADDRESS
VILP
ADDRESS STABLE
tAS
tDS
tDV
DATA
DATA IN
DATA OUT
tR
tDH
tDZ
tAH
tF
VPP
PROGRAMMING VOLTAGE (PIN 20)
tPP
PGM
tVD
tVP
VFY

0016-10

Figure 5. PROM Programming Waveforms


PROGRAM
VIHP
A2
VILP
VPP
A1
tR
tDS
tDH
DATA
DATA IN
tF
tAS
tAH
PROGRAMMING VOLTAGE (PIN 20)
tPP
PGM

0016-11

Figure 6. Initial Byte Programming Waveforms

Programming the Initialization Byte

The CY7C245 registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Programming Synchronous Enable

The CY7C245 provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3, V_{PP} is applied to pin 7 (A_1) with pin 6 (A_2) at V_{IHP}. This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 ($\overline{PGM}$) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

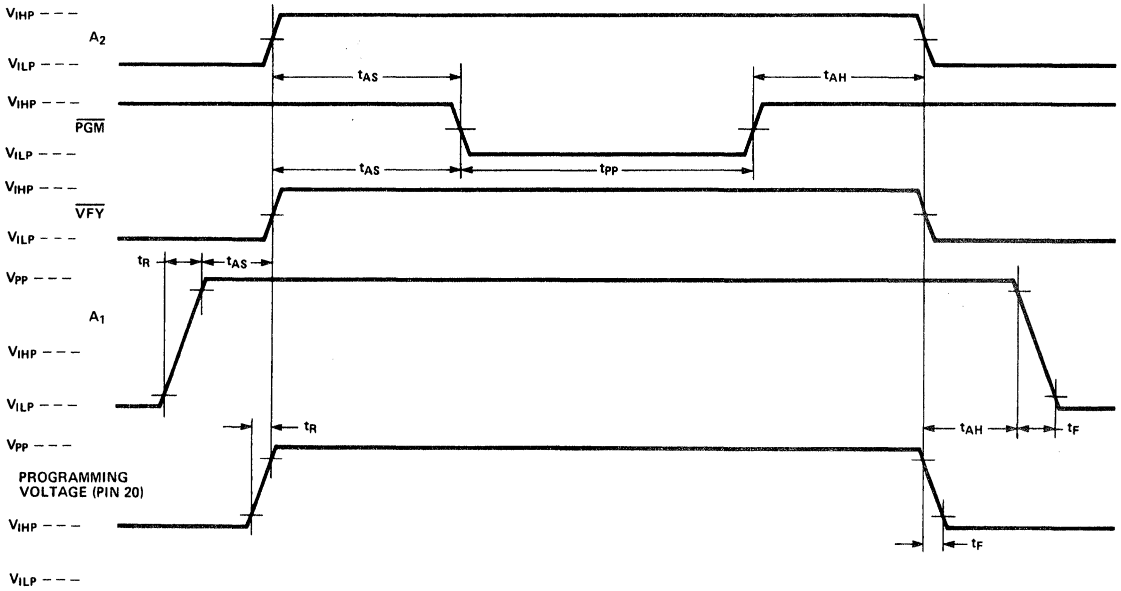


Figure 7. Program Synchronous Enable

Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at V_{IH}, cause clock pin 18 to transition from V_{IL} to V_{IH}. The output should be in a High Z state. Take pin 20, $\overline{ENABLE}$, to V_{IL}. The outputs should remain in a high Z state. Transition the clock from V_{IL} to V_{IH}, the outputs should now contain the data that is present. Again set pin 19 to V_{IH}. The output should remain driven. Clocking pin 18 once more from V_{IL} to V_{IH} should place the outputs again in a High Z state.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

Ordering Information

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
25	12	90	CY7C245-25PC	P13	Commercial
			CY7C245-25WC	W14	
35	15	60	CY7C245L-35PC	P13	Commercial
			CY7C245L-35WC	W14	
		90	CY7C245-35PC	P13	
			CY7C245-35SC	S13	
			CY7C245-35WC	W14	
			CY7C245-35LC	L64	
		120	CY7C245-35DMB	D14	Military
			CY7C245-35QMB	Q64	
			CY7C245-35WMB	W14	
			CY7C245-35LMB	L64	

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
45	25	60	CY7C245L-45PC	P13	Commercial
			CY7C245L-45WC	W14	
		90	CY7C245-45PC	P13	
			CY7C245-45SC	S13	
			CY7C245-45WC	W14	
			CY7C245-45LC	L64	
		120	CY7C245-45WMB	W14	Military
			CY7C245-45LMB	L64	
			CY7C245-45DMB	D14	
			CY7C245-45QMB	Q64	

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C251
CY7C253/CY7C254

16,384 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns (commercial)**
  - **— 55 ns (military)**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C251)**
  - **— Less than 165 mW when deselected**
  - **— Fast access: 50 ns**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

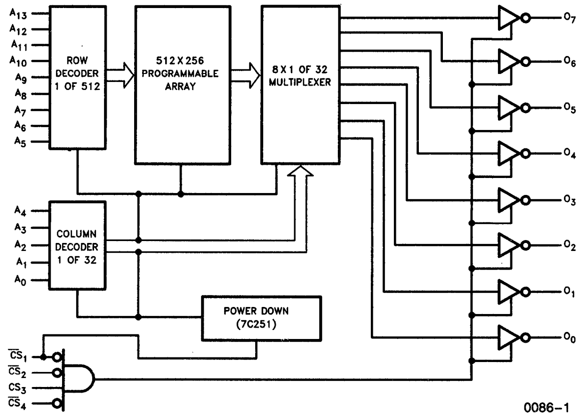
Product Characteristics

The CY7C251, CY7C253 and CY7C254 are high performance 16,384 word by 8 bit CMOS PROMs. When deselected, the 7C251 automatically powers down into a low power standby mode. It is packaged in the 300 mil wide package. The 7C253 and 7C254 are packaged in 300 mil and 600 mil wide packages respectively and do not power down when deselected. The 7C251 and 7C253 reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C251, CY7C253 and CY7C254 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

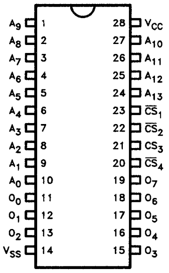
Reading is accomplished by placing all four chip selects in their active states. The contents of the memory location addressed by the address lines (A_0–A_{13}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

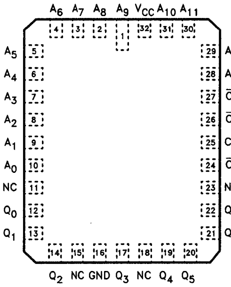

A13
A12
A11
A10
A9
A8
A7
A6
A5
ROW DECODER 1 OF 512
512 X 256 PROGRAMMABLE ARRAY
8 X 1 OF 32 MULTIPLEXER
A4
A3
A2
A1
A0
COLUMN DECODER 1 OF 32
POWER DOWN (7C251)
CS1
CS2
CS3
CS4
O7
O6
O5
O4
O3
O2
O1
O0

0086-1

Pin Configurations


A9 1
A8 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
VSS 14
28 VCC
27 A10
26 A11
25 A12
24 A13
23 CS1
22 CS2
21 CS3
20 CS4
19 O7
18 O6
17 O5
16 O4
15 O3

0086-2


A6 A7 A8 A9 VCC A10 A11
4 3 2 1 32 31 30
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
NC 11
Q0 12
Q1 13
29 A12
28 A13
27 CS1
26 CS2
25 CS3
24 CS4
23 NC
22 Q7
21 Q6
14 15 16 17 18 19 20
Q2 NC GND Q3 NC Q4 Q5

0086-11

Top View

Selection Guide

		7C251-45 7C253-45 7C254-45	7C251-55 7C253-55 7C254-55	7C251-65 7C253-65 7C254-65
Maximum Access Time (ns)		45	55	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military		120	120
Standby Current (mA) (7C251 only)	Commercial	30	30	30
	Military		35	35

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pin 22) 13.5V

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to + 125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C251-45 7C253-45 7C254-45		7C251-55,65 7C253-55,65 7C254-55,65		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[1]			2.0		2.0		V
V_{IL}	Input LOW Level[1]				0.8		0.8	V
I_{IX}	Input Current	V_{CC} = Max., V_{CC} = GND		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		
I_{OZ}	Output Leakage Current	$V_{OL} \leq V_{OUT} \leq V_{OH}$, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		100		100	mA
			Military				120	mA
I_{SB}	Standby Supply Current (7C251)	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				35	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C251, CY7C253 & CY7C254 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Measured on a sample basis.

Switching Characteristics Over the Operating Range[5]

Parameters	Description	7C251-45 7C253-45 7C254-45		7C251-55 7C253-55 7C254-55		7C251-65 7C253-65 7C254-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		65	ns
t_{HZCS_1}	Chip Select Inactive to High Z[6,7]		25		30		35	ns
t_{HZCS_2}	Chip Select Inactive to High Z (7C251, $\overline{\text{CS}}_1$ Only)[6]		50		55		65	ns
t_{ACS_1}	Chip Select Active to Output Valid[7]		25		30		35	ns
t_{ACS_2}	Chip Select Active to Output Valid (7C251, $\overline{\text{CS}}_1$ Only)		50		55		65	ns
t_{PU}	Chip Select Active to Power Up (7C251)	0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C251)		50		55		65	ns

AC Test Loads and Waveforms

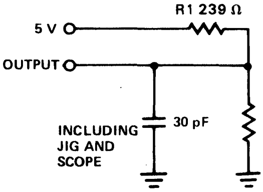

R1 239 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
30 pF
R2 186 Ω

Figure 1a

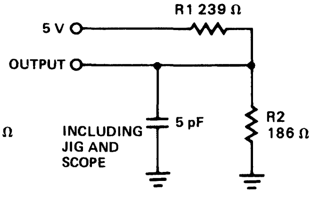

R1 239 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
5 pF
R2 186 Ω
0086-4

Figure 1b

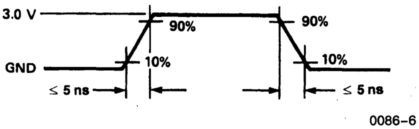
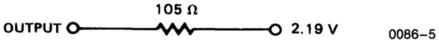
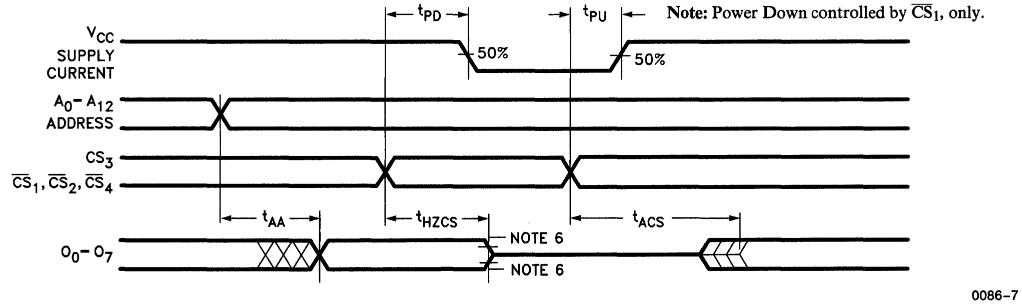

3.0 V
GND
90%
10%
90%
10%
≤ 5 ns
≤ 5 ns
0086-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT


105 Ω
OUTPUT
2.19 V
0086-5


tPD
tPU
Note: Power Down controlled by CS1, only.
VCC SUPPLY CURRENT
50%
50%
A0–A12 ADDRESS
CS3
CS1, CS2, CS4
tAA
tHZCS
tACS
NOTE 6
NOTE 6
O0–O7
0086-7

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
6. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.
7. t_{HZCS_1} and t_{ACS_1} refers to 7C253 and 7C254 (all chip selects); and 7C251 ($\overline{\text{CS}}_2$, CS_3 and $\overline{\text{CS}}_4$ only).

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C251 and 7C253 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C251 or 7C253 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. $7258\text{W} \times \text{sec/cm}^2$ is the recommended maximum dosage.

Device Programming

The CY7C251, CY7C253 & CY7C254 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 128K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 22 to V_{PP}. The addressed location is programmed and verified with the application of a $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ pulse applied to pins 23 and 21 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

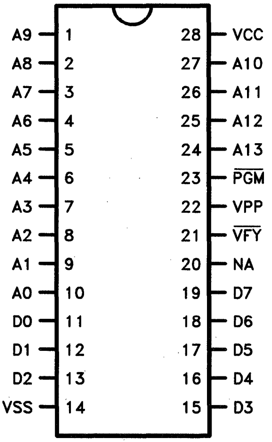
Programming And Blankcheck

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{\text{VFY}}$ toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s.

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin 22. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location, placing the data to be programmed into a location on the data pins, and clocking the $\overline{\text{PGM}}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{\text{VFY}}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{\text{VFY}}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{\text{PGM}}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more



0086–8

Figure 3. Programming Pinout (DIP Package)

verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at $V_{CCP} = 5.0V$.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 14 bit field, 4 chip select bits, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 22. Pin 23 becomes an active LOW program ($\overline{\text{PGM}}$) signal and pin 21 becomes an active LOW verify ($\overline{\text{VFY}}$) signal. Pins 21 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{\text{PGM}}$ is LOW, and $\overline{\text{VFY}}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{\text{PGM}}$ HIGH and $\overline{\text{VFY}}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in Figure 4, and some pertains only to entry and exit from the programming mode of operation.

T_P, T_{PD} and T_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ operations.

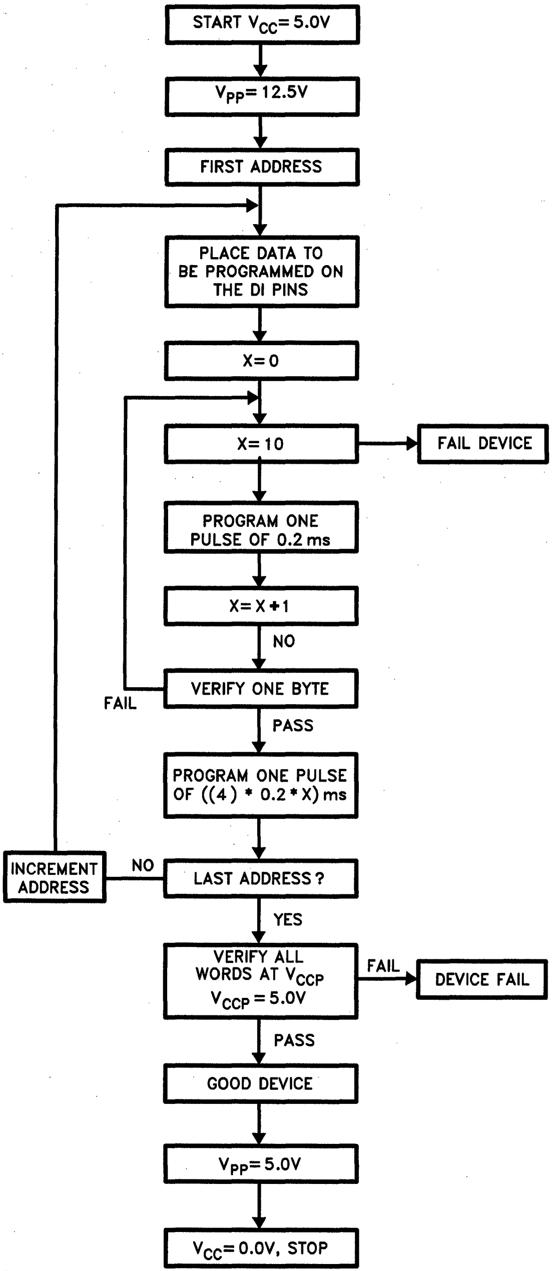
T_{DS}, T_{AS}, T_{AH} and T_{DH} refer to the required setup and hold times for the address and data for $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ operations. These parameters must be adhered to, in all operations, including V_{FY}. This precludes the option then of verifying the device by holding the V_{FY} signal LOW, and sequencing the addresses.

Table 1. Operating Modes

Mode		Pin Function				Outputs (11–13, 15–19)
	Read or Output Disable	$\overline{\text{CS}}_4$	CS_3	$\overline{\text{CS}}_2$	$\overline{\text{CS}}_1$	
	Other	N/A	$\overline{\text{VFY}}$	V_{PP}	$\overline{\text{PGM}}$	
	Pin Number	(20)	(21)	(22)	(23)	
Read		V_{IL}	V_{IH}	V_{IL}	V_{IL}	Data Out
Output Disable[1]		X	X	X	V_{IH}	High Z
Output Disable[1]		X	X	V_{IH}	X	High Z
Output Disable[1]		X	V_{IL}	X	X	High Z
Output Disable[1]		V_{IH}	X	X	X	High Z
Program		X	V_{IHP}	V_{PP}	V_{ILP}	Data In
Program Verify		X	V_{ILP}	V_{PP}	V_{IHP}	Data Out
Program Inhibit		X	V_{IHP}	V_{PP}	V_{IHP}	High Z
Blank Check		X	V_{ILP}	V_{PP}	V_{IHP}	Data Out

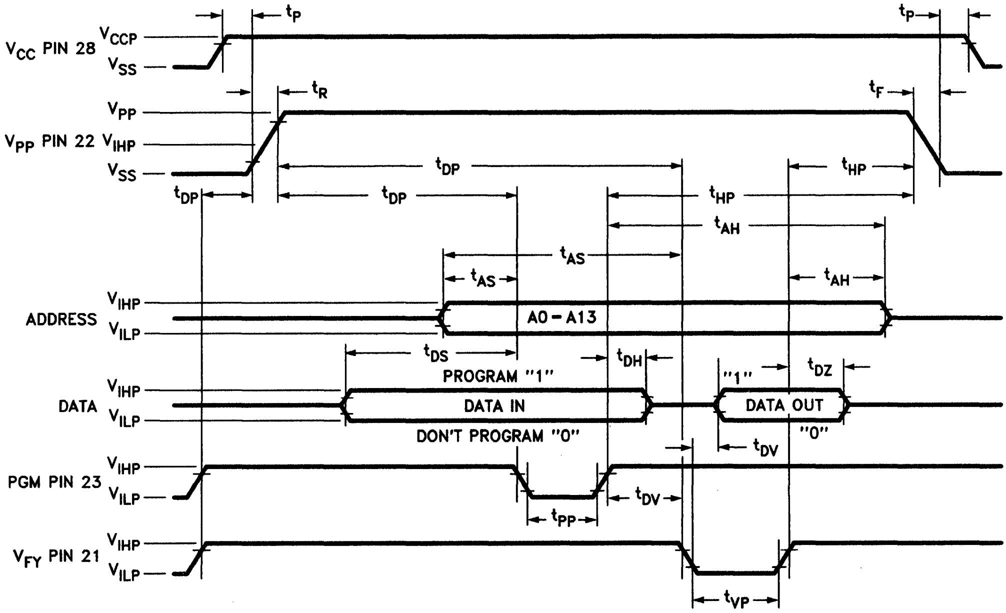
Note:

1. X = Don't care but not to exceed $V_{CC} + 5\%$.


START V_{CC}= 5.0V
V_{PP}= 12.5V
FIRST ADDRESS
PLACE DATA TO BE PROGRAMMED ON THE DI PINS
X= 0
X= 10
FAIL DEVICE
PROGRAM ONE PULSE OF 0.2 ms
X= X + 1
NO
VERIFY ONE BYTE
FAIL
PASS
PROGRAM ONE PULSE OF ((4) * 0.2 * X) ms
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
VERIFY ALL WORDS AT V_{CCP} V_{CCP} = 5.0V
FAIL
DEVICE FAIL
PASS
GOOD DEVICE
V_{PP}= 5.0V
V_{CC}= 0.0V, STOP

0086–9

Figure 4. Programming Flowchart


tP
tP
VCC PIN 28
VCCP
VSS
tR
tF
VPP
VPP PIN 22 VIHP
VSS
tDP
tHP
tDP
tDP
tHP
tAH
tAS
tAS
tAH
ADDRESS
VIHP
VILP
A0 - A13
tDS
tDH
"1"
tDZ
PROGRAM "1"
DATA
VIHP
VILP
DATA IN
DATA OUT
DON'T PROGRAM "0"
"0"
tDV
PGM PIN 23
VIHP
VILP
tDV
tPP
VFY PIN 21
VIHP
VILP
tVP

0086-10

Figure 5. Programming Waveforms

Note: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

Table 2. DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0	V_{CCP}	V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

Table 3. AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
t_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
t_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
t_{PP}	Program Pulse Width	0.2	10	ms
$t_{R, F}$	V_{PP} Rise and Fall Time	100		ns
t_{DV}	Delay to Verify	1.0		μs
t_{VD}	Verify to Data Out		1.0	μs
t_{VH}	Data Hold Time from Verify		1.0	μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DZ}	Verify to High Z		1.0	μs
t_{DP}	Delay to Function	1.0		μs
t_{HP}	Hold From Function	1.0		μs
t_P	Power Up/Down	20.0		ms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C251-45PC	P21	Commercial
	CY7C251-45WC	W22	
	CY7C253-45PC	P21	
	CY7C253-45WC	W22	
	CY7C254-45PC	P15	
	CY7C254-45DC	D16	
55	CY7C251-55PC	P21	
	CY7C251-55WC	W22	
	CY7C253-55PC	P21	
	CY7C253-55WC	W22	
	CY7C254-55PC	P15	
	CY7C254-55DC	D16	
	CY7C251-55WMB	W22	Military
	CY7C251-55DMB	D22	
	CY7C253-55WMB	W22	
	CY7C253-55DMB	D22	
	CY7C254-55DMB	D16	
65	CY7C251-65PC	P21	Commercial
	CY7C251-65WC	W22	
	CY7C253-65PC	P21	
	CY7C253-65WC	W22	
	CY7C254-65PC	P15	
	CY7C254-65DC	D16	
	CY7C251-65WMB	W22	Military
	CY7C251-65DMB	D22	
	CY7C251-65LMB	L55	
	CY7C251-65QMB	Q55	
	CY7C253-65WMB	W22	
	CY7C253-65DMB	D22	
	CY7C253-65LMB	L55	
	CY7C253-65QMB	Q55	
	CY7C254-65DMB	D16	

CYPRESS SEMICONDUCTOR

CY7C261
CY7C263/CY7C264

8192 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 40 ns (commercial)**
  - **— 45 ns (military)**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C261)**
  - **— Less than 185 mW when deselected**
  - **— Fast access: 25 ns**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

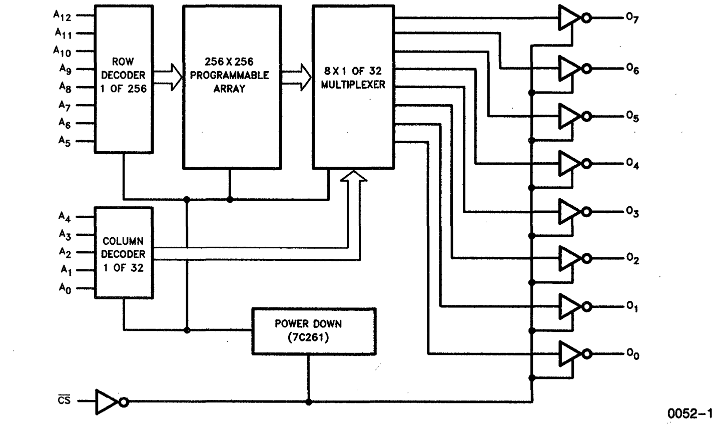
Product Characteristics

The CY7C261, CY7C263 and CY7C264 are high performance 8192 word by 8 bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low power standby mode. It is packaged in the 300 mil wide package. The 7C263 and 7C264 are packaged in 300 mil and 600 mil wide packages respectively and do not power down when deselected. The 7C261 and 7C263 reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263 and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address lines (A_0-A_{12}) will become available on the output lines (O_0-O_7).

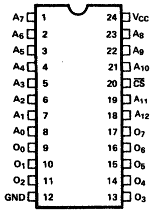
Logic Block Diagram



A12
A11
A10
A9
A8
A7
A6
A5
ROW DECODER 1 OF 256
256 X 256 PROGRAMMABLE ARRAY
8 X 1 OF 32 MULTIPLEXER
A4
A3
A2
A1
A0
COLUMN DECODER 1 OF 32
POWER DOWN (7C261)
CS
O7
O6
O5
O4
O3
O2
O1
O0

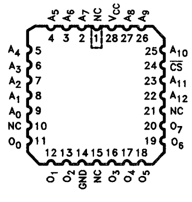
0052–1

Pin Configurations



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 CS
19 A11
18 A12
17 O7
16 O6
15 O5
14 O4
13 O3

0052–2



A5 A6 A7 NC VCC A8 A9
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 A10
24 CS
23 A11
22 A12
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

0052–3

Selection Guide

		7C261-40 7C263-40 7C264-40	7C261-45 7C263-45 7C264-45	7C261-55 7C263-55 7C264-55
Maximum Access Time (ns)		40	45	55
Maximum Operating Current (mA)	Commercial	100	100	100
	Military		120	120
Standby Current (mA) (7C261 only)	Commercial	30	30	30
	Military		30	30

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12)................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage
(Pin 19 DIP, Pin 23 LCC) 14.0V

Static Discharge Voltage ....>2001V
(per MIL-STD-883, Method 3015.2)

Latchup Current ....>200 mA

UV Exposure ....7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C261-40 7C263-40 7C264-40		7C261-45,55 7C263-45,55 7C264-45,55		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[1]			2.0		2.0		V
V_{IL}	Input LOW Level[1]				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		100		100	mA
			Military				120	mA
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				30	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C261, CY7C263 & CY7C264 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Measured on a sample basis.

Switching Characteristics Over the Operating Range[5]

Parameters	Description	7C261-40 7C263-40 7C264-40		7C261-45 7C263-45 7C264-45		7C261-55 7C263-55 7C264-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		40		45		55	ns
t_{HZCS_1}	Chip Select Inactive to High Z[6]		25		30		35	ns
t_{HZCS_2}	Chip Select Inactive to High Z (7C261)[6]		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid		25		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		45		45		55	ns
t_{PU}	Chip Select Active to Power Up (7C261)	0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C261)		40		45		55	ns

AC Test Loads and Waveforms

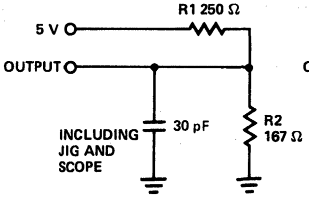

R1 250 Ω
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
30 pF
R2
167 Ω

Figure 1a

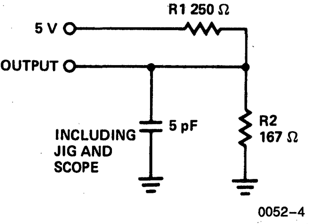

R1 250 Ω
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
5 pF
R2
167 Ω
0052-4

Figure 1b

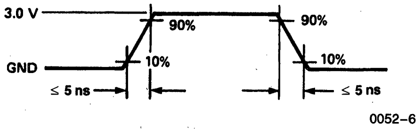
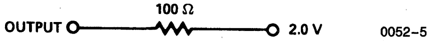
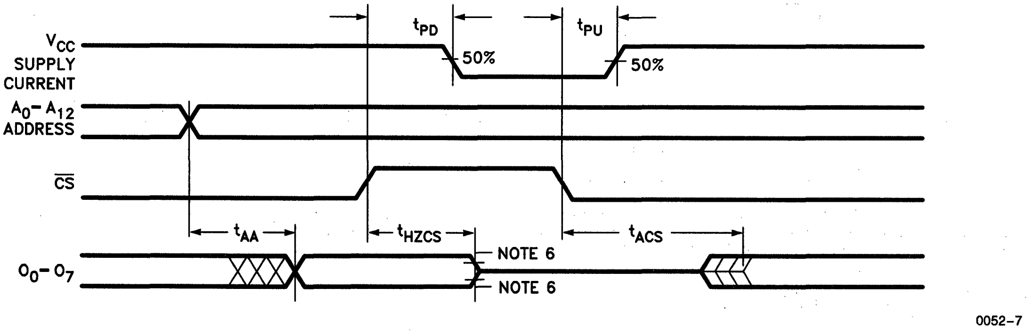

3.0 V
GND
90%
10%
90%
10%
≤ 5 ns
≤ 5 ns
0052-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT


100 Ω
OUTPUT
2.0 V
0052-5


tPD
tPU
VCC SUPPLY CURRENT
50%
50%
A0 - A12 ADDRESS
CS
tAA
tHZCS
tACS
NOTE 6
NOTE 6
O0 - O7
0052-7

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
6. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C261 and 7C263 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Device Programming

The CY7C261, CY7C263 & CY7C264 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 19 to V_{PP}. In this mode, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched and held in an onboard register, while the lower 8 address bits are presented on the same pins for selecting one of 256 memory bytes. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse applied to pins 22 and 23 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

Programming And Blankcheck

Addressing During Programming and Blankcheck

Addressing to these devices in all modes of operation other than normal read operation is accomplished by multiplexing the upper 5 address bits with the lower 8. The address designations for the lower 8 addressing bits is AX0 through AX7 and the upper 5 address bits are designated AY8 through AY12. This allows sufficient pins for an intelligent programming algorithm to be implemented without the need to switch high voltage signals during the blankcheck, programming, and verification operation.

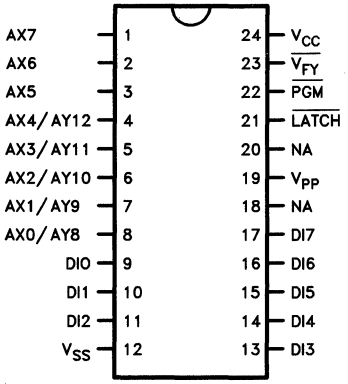
Addressing while in these modes is accomplished by placing the upper 5 bits of address on pins 8, 7, 6, 5, and 4 with the least significant bit on pin 8. These address bits are loaded into an onboard register by clocking pin 21, the latch signal, from V_{ILP} to V_{IHP} and back to V_{ILP}. The lower 8 address bits are then placed on pins 8 through 1, with the least significant bit on pin 8. The upper 5 bits remain in the onboard latch until a new value is loaded or power is removed from the device. All 256 bytes addressed by the lower 8 bits may be accessed by sequencing the lower 8 addresses without changing the upper 5 bits or relatching the value in the onboard register.

Blankcheck

Blankcheck is accomplished by performing a verify cycle, sequencing through all memory address locations, where all the data read will be "0"s.

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin 19. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{PGM}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{VFY}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{VFY}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{PGM}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the



0052-8

Figure 3. Programming Pinout (DIP Package)

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13 bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation. Note should be taken of the inner and outer addressing loops which allow 256 bytes to be programmed each time the onboard register containing the upper 5 address bits is loaded.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in the inner loops of Figure 5, some for the outer loop where the upper address is advanced, and some pertains only to entry and exit from the programming mode of operation.

In particular, the timing sequence associated with the Latch signal on pin 21 and addresses AY8 through AY12 pertain only to the outer loop where the upper 5 (N in the flow chart) address bits are incremented.

T_P, T_{PD} and T_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to LATCH, $\overline{PGM}$ and $\overline{VFY}$ operations.

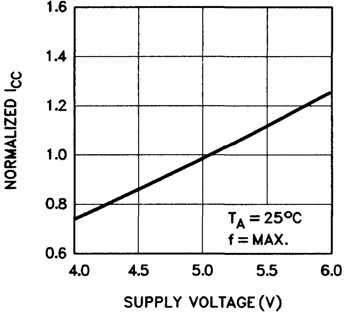
T_{DS}, T_{AS}, T_{AH} and T_{DH} refer to the required setup and hold times for the address and data for $\overline{PGM}$ and $\overline{VFY}$ operations. These parameters must be adhered to, in all operations, including V_{FY}. This precludes the option then of verifying the device by holding the V_{FY} signal LOW, and sequencing the addresses.

Table 1. Operating Modes

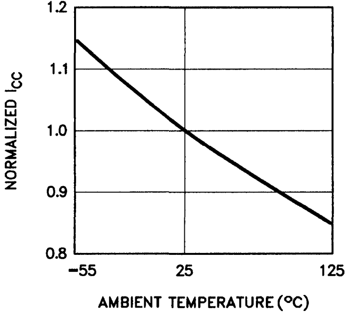
Mode	Pins 1 thru 3 A7–A5, AX7–AX5	Pins 4 thru 8 A4–A0, AX4–AX0 AY12–AY8	Pins 9 thru 11 D0 thru D2	Pins 13 thru 17 D3 thru D7	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22	Pin 23
Read	A7 thru A5	A4 thru A0	DO0 thru DO2	DO3 thru DO7	A12	A11	$\overline{CS}$	A10	A9	A8
Program	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Input	DI_3 thru DI_7 Input	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{ILP}	V_{IHP}
Program Inhibit	AX7 thru AX5	AX4 thru AX0 AY12–AY8	High Z	High Z	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{IHP}
Program Verify	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DO0 thru DO2 Output	DO3 thru DO7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}
Blank Check	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Output	DI_3 thru DI_7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}

Typical AC and DC Characteristics

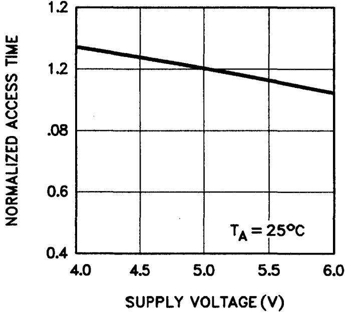
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



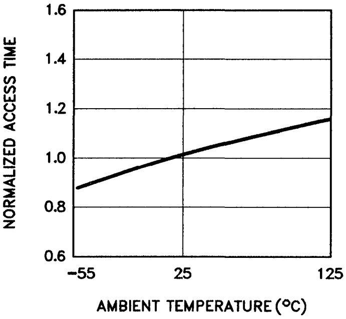
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



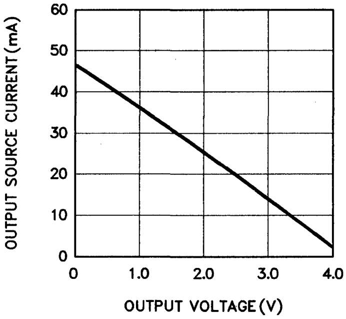
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



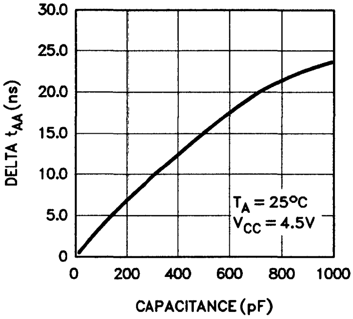
NORMALIZED ACCESS TIME vs. TEMPERATURE



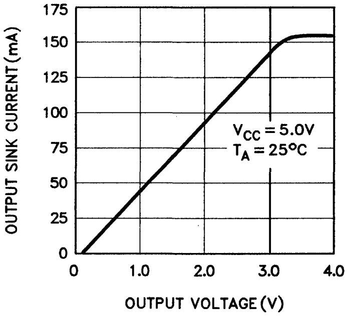
OUTPUT SOURCE CURRENT vs. VOLTAGE



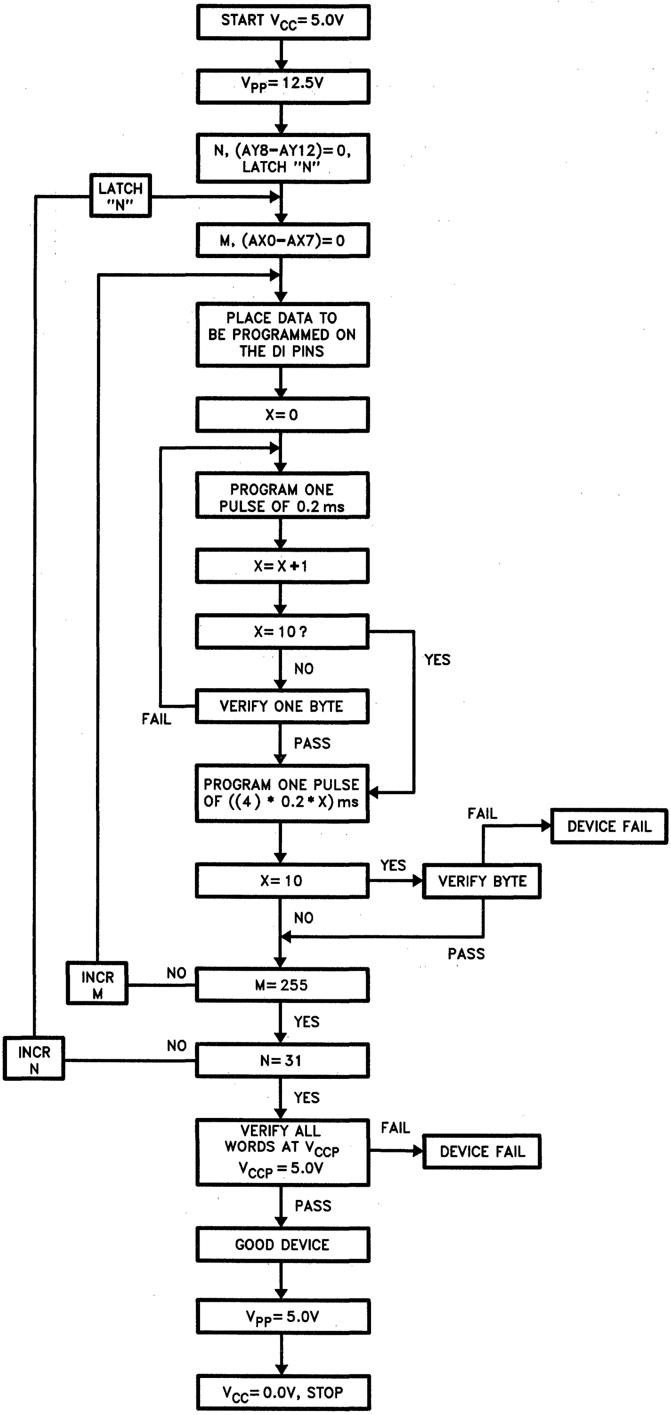
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

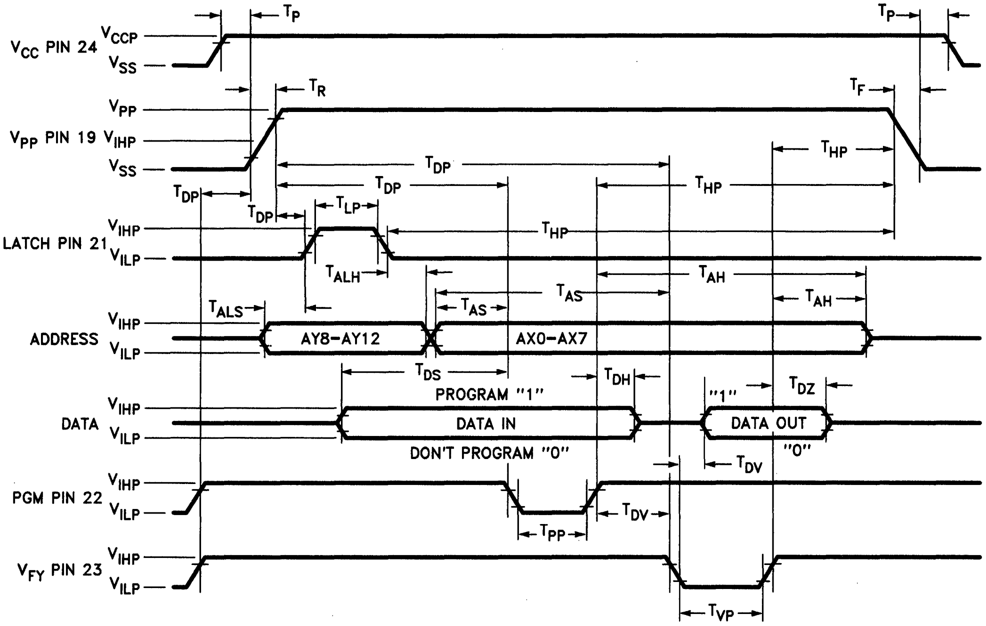


0052–11


START V_{CC}= 5.0V
V_{PP}= 12.5V
N, (AY8–AY12)= 0, LATCH "N"
LATCH "N"
M, (AX0–AX7)= 0
PLACE DATA TO BE PROGRAMMED ON THE DI PINS
X= 0
PROGRAM ONE PULSE OF 0.2 ms
X= X + 1
X= 10 ?
YES
NO
VERIFY ONE BYTE
FAIL
PASS
PROGRAM ONE PULSE OF ((4) * 0.2 * X) ms
FAIL
DEVICE FAIL
X= 10
YES
VERIFY BYTE
NO
PASS
INCR M
NO
M= 255
YES
INCR N
NO
N= 31
YES
VERIFY ALL WORDS AT V_{CCP} V_{CCP} = 5.0V
FAIL
DEVICE FAIL
PASS
GOOD DEVICE
V_{PP}= 5.0V
V_{CC}= 0.0V, STOP

0052–9

Figure 4. Programming Flowchart


VCC PIN 24
VCCP
VSS
TP
TP
VPP PIN 19
VPP
VIHP
VSS
TR
TF
TDP
TDP
TDP
TDP
THP
THP
THP
TLP
LATCH PIN 21
VIHP
VILP
TALH
TALS
TAS
TAS
TAH
TAH
ADDRESS
VIHP
VILP
AY8–AY12
AX0–AX7
TDS
TDH
TDZ
PROGRAM "1"
"1"
DATA
VIHP
VILP
DATA IN
DATA OUT
DON'T PROGRAM "0"
"0"
TDV
PGM PIN 22
VIHP
VILP
TPP
TDV
VFY PIN 23
VIHP
VILP
TVP

0052–10

Figure 5. Programming Waveforms

Note: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

Table 2. DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0	V_{CCP}	V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

Table 3. AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
T_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
T_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
T_{PP}	Program Pulse Width	0.2	10	ms
$T_{R,F}$	V_{PP} Rise and Fall Time	100		ns
T_{ALS}	Address Setup Time to Latch	1.0		μs
T_{ALH}	Address Hold Time from Latch	1.0		μs
T_{LP}	Latch Pulse Width	1.0		μs
T_{DV}	Delay to Verify	1.0		μs
T_{VD}	Verify to Data Out		1.0	μs
T_{VH}	Data Hold Time from Verify		1.0	μs
T_{VP}	Verify Pulse Width	2.0		μs
T_{DZ}	Verify to High Z		1.0	μs
T_{DP}	Delay to Function	1.0		μs
T_{HP}	Hold From Function	1.0		μs
T_P	Power Up/Down	20.0		ms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
40	CY7C261-40PC	P13	Commercial
	CY7C261-40WC	W14	
	CY7C263-40PC	P13	
	CY7C263-40WC	W14	
	CY7C264-40PC	P11	
	CY7C264-40DC	D12	
45	CY7C261-45PC	P13	
	CY7C261-45WC	W14	
	CY7C263-45PC	P13	
	CY7C263-45WC	W14	
	CY7C264-45PC	P11	
	CY7C264-45DC	D12	
	CY7C261-45WMB	W14	Military
	CY7C261-45DMB	D14	
	CY7C261-45LMB	L64	
	CY7C261-45QMB	Q64	
	CY7C263-45WMB	W14	
	CY7C263-45DMB	D14	
	CY7C263-45LMB	L64	
	CY7C264-45DMB	D12	
55	CY7C261-55PC	P13	Commercial
	CY7C261-55WC	W14	
	CY7C263-55PC	P13	
	CY7C263-55WC	W14	
	CY7C264-55PC	P11	
	CY7C264-55DC	D12	
	CY7C261-55WMB	W14	Military
	CY7C261-55DMB	D14	
	CY7C261-55LMB	L64	
	CY7C261-55QMB	Q64	
	CY7C263-55WMB	W14	
	CY7C263-55DMB	D14	
	CY7C263-55LMB	L64	
	CY7C264-55DMB	D12	

CYPRESS SEMICONDUCTOR

CY7C268
CY7C269

64K Registered Diagnostic PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 40 ns max set-up**
  - **— 20 ns clock to output**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **On-chip edge-triggered registers**
  - **— Ideal for pipelined microprogrammed systems**
- **On-chip diagnostic shift register**
  - **— For serial observability and controllability of the output register**
- **EPROM technology**
  - **— 100% programmable**
  - **— Reprogrammable (7C269W)**
- **5V ±10% V$_{CC}$, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **Slim, 300 mil 28 pin plastic or hermetic DIP (7C269)**

Functional Description

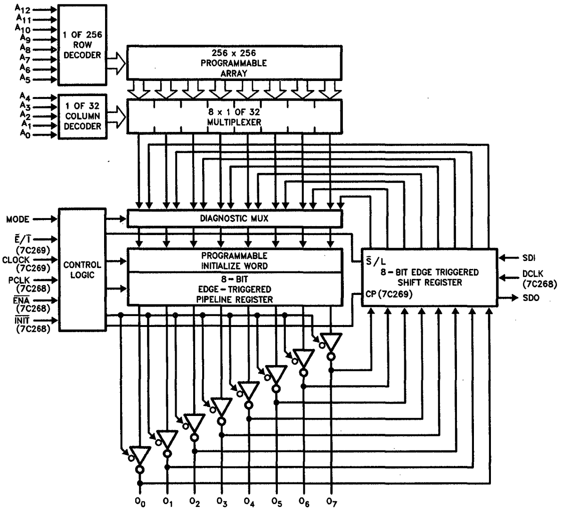
The CY7C268 and CY7C269 are 64K Registered Diagnostic PROMs. They are both organized 8192 words by 8 bits wide, and have both a Pipeline Output Register and an Onboard Diagnostic Shift Register. In addition, both devices feature a Programmable Initialize Byte which may be loaded into the Pipeline Register with the Initialize signal. The Programmable Initialize Byte is the 8193rd byte in the PROM and its value is programmed at time of use.

The 7C268 has 32 pins and features full diagnostic capabilities while the 7C269 provides limited diagnostics and is available in a space efficient 28 pin package. This allows the designer to optimize his design for either board area efficiency with the 7C269, or combine the 7C268 with other diagnostic products with the standard interface.

CY7C268: The 7C268 provides 13 address signals (A$_0$ through A$_{12}$), 8 data out signals (O$_0$ through O$_7$), $\overline{\text{ENA}}$ (enable), PCLK (pipeline clock) and $\overline{\text{INIT}}$ (initialize) for control. The full standard featured diagnostics of the 7C268 utilizes the SI and SO (shift in and shift out), MODE and DCLK signals. These signals allow serial data to be shifted into and out of the Diagnostic Shift Register at the same time the Pipeline Register is used for normal operation. The MODE signal is used to control the transfer of the information in the Diagnostic Register to the Pipeline Register or the data on the Output Bus into the Diagnostic Register. The data on the Output Bus may be provided from the Pipeline Register or an external source.

When the MODE signal is LOW, the PROM operates in a normal pipeline mode. The contents of the addressed memory location is loaded into the Pipeline Register on the rising edge of PCLK. The outputs are enabled with the $\overline{\text{ENA}}$ signal either synchronously or asynchronously, depending on how the device is configured when programmed. If programmed for asynchronous enable, $\overline{\text{ENA}}$ LOW enables

Logic Block Diagram

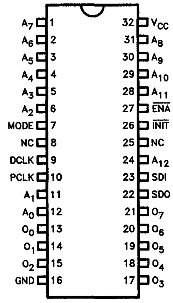


A12 A11 A10 A9 A8 A7 A6 A5
1 OF 256 ROW DECODER
256 x 256 PROGRAMMABLE ARRAY
A4 A3 A2 A1 A0
1 OF 32 COLUMN DECODER
8 x 1 OF 32 MULTIPLEXER
MODE
E/T (7C269)
CLOCK (7C269)
PCLK (7C268)
ENA (7C268)
INIT (7C268)
CONTROL LOGIC
DIAGNOSTIC MUX
PROGRAMMABLE INITIALIZE WORD
8-BIT EDGE-TRIGGERED PIPELINE REGISTER
S/L
8-BIT EDGE TRIGGERED SHIFT REGISTER
CP (7C269)
SDI
DCLK (7C268)
SDO
O0 O1 O2 O3 O4 O5 O6 O7

0112-1

Pin Configurations

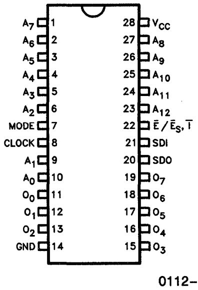
CY7C268



A7 1, A6 2, A5 3, A4 4, A3 5, A2 6, MODE 7, NC 8, DCLK 9, PCLK 10, A1 11, A0 12, O0 13, O1 14, O2 15, GND 16
32 VCC, 31 A8, 30 A9, 29 A10, 28 A11, 27 ENA, 26 INIT, 25 NC, 24 A12, 23 SDI, 22 SDO, 21 O7, 20 O6, 19 O5, 18 O4, 17 O3

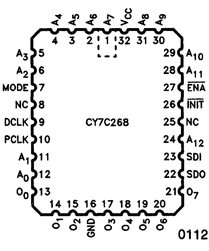
0112-2

CY7C269



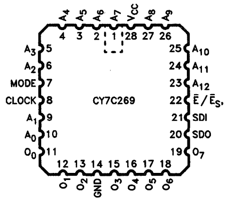
A7 1, A6 2, A5 3, A4 4, A3 5, A2 6, MODE 7, CLOCK 8, A1 9, A0 10, O0 11, O1 12, O2 13, GND 14
28 VCC, 27 A8, 26 A9, 25 A10, 24 A11, 23 A12, 22 E/ES, T, 21 SDI, 20 SDO, 19 O7, 18 O6, 17 O5, 16 O4, 15 O3

0112-3



A4 A5 A6 A7 VCC A8 A9
4 3 2 1 32 31 30
A3 5, A2 6, MODE 7, NC 8, DCLK 9, PCLK 10, A1 11, A0 12, O0 13
29 A10, 28 A11, 27 ENA, 26 INIT, 25 NC, 24 A12, 23 SDI, 22 SDO, 21 O7
CY7C268
14 15 16 17 18 19 20
O1 O2 GND O3 O4 O5 O6

0112-4



A4 A5 A6 A7 VCC A8 A9
4 3 2 1 28 27 26
A3 5, A2 6, MODE 7, CLOCK 8, A1 9, A0 10, O0 11
25 A10, 24 A11, 23 A12, 22 E/ES, T, 21 SDI, 20 SDO, 19 O7
CY7C269
12 13 14 15 16 17 18
O1 O2 GND O3 O4 O5 O6

0112-5

Selection Guide

		7C268/9-40	7C268/9-50	7C268/9-60
Maximum Set-up Time (ns)		40	50	60
Maximum Clock to Output (ns)		20	25	25
Maximum Operating Current (mA)	Commercial	100	80	80
	Military		120	100

Functional Description (Continued)

the outputs. If configured for synchronous enable, $\overline{\text{ENA}}$ LOW during the rising edge of PCLK will enable the outputs synchronously with PCLK. $\overline{\text{ENA}}$ HIGH during the rising edge of PCLK will synchronously disable the outputs. The asynchronous Initialize signal $\overline{\text{INIT}}$ transfers the Initialize Byte into the Pipeline Register on a HIGH to LOW transition. $\overline{\text{INIT}}$ LOW disables PCLK and needs to transition back to a HIGH in order to enable PCLK. DCLK shifts data into SI and out of SO on each rising edge.

When MODE is HIGH, the rising edge of the PCLK signal loads the Pipeline Register with the contents of the Diagnostic Register. Similarly, DCLK, in this mode, loads the Diagnostic Register with the information on the Data Output Pins. The information loaded will be either the contents of the Pipeline Register if the outputs are enabled, or data on the bus, if the outputs are disabled (in a high impedance state).

CY7C269: This product is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, the PROM has 13 Address Signals (A_0 through A_{12}), 8 Data Out Signals (O_0 through O_7), $\overline{\text{E}}/\overline{\text{I}}$, (Enable or Initialize) and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SI (shift in) and SO (shift out). Normal pipelined operation and Diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the Pipeline Register on each rising edge. The data will appear on the Outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the $\overline{\text{E}}/\overline{\text{I}}$ pin is used for a $\overline{\text{INIT}}$ (Asynchronous Initialize) function, the outputs are permanently enabled and the Initialize Word is loaded into the Pipeline Register on a High to LOW transition of the $\overline{\text{INIT}}$ signal. The $\overline{\text{INIT}}$ LOW disables CLOCK and must return high to re-enable CLOCK. If the $\overline{\text{E}}/\overline{\text{I}}$ pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation. This enable function then operates exactly the same as the 7C268.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The $\overline{\text{E}}/\overline{\text{I}}$ signal becomes a secondary mode signal designating whether to shift the Diagnostic Shift Register or to load either the Diagnostic Register or the Pipeline Register. If $\overline{\text{E}}/\overline{\text{I}}$ is HIGH, CLOCK performs the function of DCLK, shifting SI into the least significant location of the Diagnostic Register and all bits one location toward the most significant location on each rising edge. The contents of the most significant location in the Diagnostic Register are available on the SO pin.

If the $\overline{\text{E}}/\overline{\text{I}}$ signal is LOW, SI becomes a direction signal; transferring the contents of the Diagnostic Register into the Pipeline Register when SI is LOW. When SI is HIGH, the contents of the Output pins are transferred into the Diagnostic Register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the Outputs are enabled, the contents of the Pipeline Register are transferred into the Diagnostic Register. If the Outputs are disabled, an external source of data may be loaded into the Diagnostic Register. In this condition, the SO signal is internally driven to be the same as the SI signal thus propagating the "direction of transfer information" to the next device in the string.

Maximum Ratings

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 14.0V

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015.

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/c

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to 70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		Commercial		Military		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12 mA (I_{OL} = 8 mA for Military)			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND < VI < V_{CC}			10.0		10.0	μA
I_{OZ}	Output Leakage Current	GND < VI < V_{CC} Output Disabled			40.0		40.0	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90.0		90.0	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	7C268/9-40		100			mA
			7C268/9-50		80		120	
			7C268/9-60		80		100	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	V_{CC} = Max. $\overline{CE} \geq V_{IH}$			20		30	mA

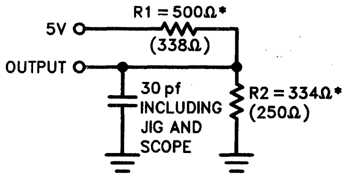
Switching Characteristics Over the Operating Range

Parameters	Description	7C268-40 7C269-40		7C268-50 7C269-50		7C268-60 7C269-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	40		50		60		ns
t_{HA}	Address Hold from Clock		0		0		0	ns
t_{CO}	Clock to Output Valid		20		25		25	ns
t_{PW}	Clock Pulse Width		15		20		20	ns
t_{ESS}	ES Set-Up to Clock (Sync Enable Only)	15		15		15		ns
t_{HES}	ES Hold from Clock		5		5		5	ns
t_{DI}	Init to Out Valid		25		35		35	ns
t_{RI}	Init Recovery to Clock	20		25		25		ns
t_{PWI}	Init Pulse Width	25		35		35		ns
t_{LZC}	Output Active from Clock (Sync. Mode)		20		25		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t_{LZE}	Output Active from $\overline{E}$ Low (Async. Mode)		20		25		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ High (Async. Mode)		20		25		25	ns

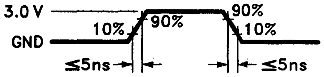
Diagnostic Mode Switching Characteristics Over the Operating Range

Parameters	Description	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{SSDI}	Set-Up SDI to Clock		30		35	ns
t_{HSDI}	SDI Hold from Clock	0		0		ns
t_{DSDO}	SDO Delay from Clock		30		40	ns
t_{DCL}	Minimum Clock Low	25		25		ns
t_{DCH}	Minimum Clock High	25		25		ns
t_{SM}	Set-Up to Mode Change	25		30		ns
t_{HM}	Hold from Mode Change (7C269)	0		0		ns
t_{MS}	Mode to SDO		25		30	ns
t_{SS}	SDI to SDO		40		45	ns
t_{SO}	Output Set-Up to DCLK	25		30		ns
t_{HO}	Output Hold from DCLK	10		15		ns

AC Test Loads and Waveforms


5V
R1 = 500Ω*
(338Ω)
OUTPUT
30 pf
INCLUDING
JIG AND
SCOPE
R2 = 334Ω*
(250Ω)

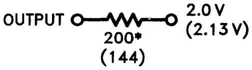
0112-6


3.0 V
GND
10%
90%
90%
10%
≤5ns
≤5ns

0112-7

*Military Values

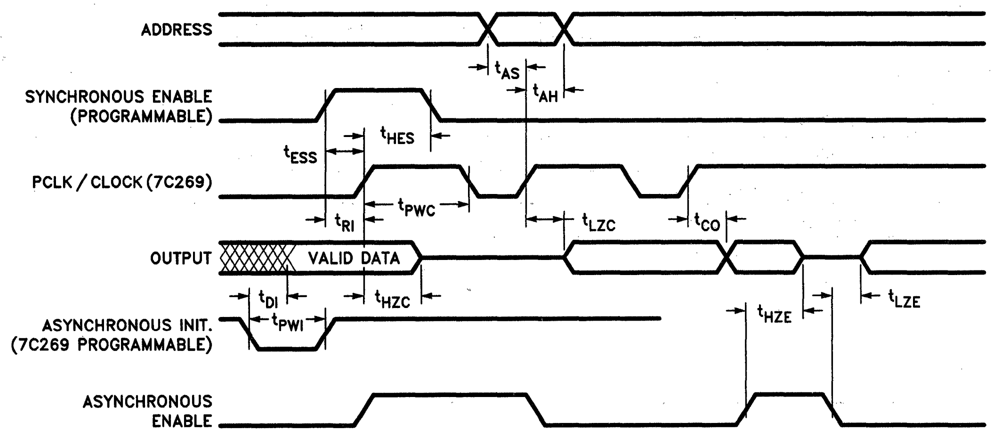
THÉVENIN EQUIVALENT


OUTPUT
200*
(144)
2.0 V
(2.13 V)

0112-8

Switching Waveforms 7C268, 7C269

Pipeline Operation (Mode = 0)


ADDRESS
SYNCHRONOUS ENABLE (PROGRAMMABLE)
PCLK / CLOCK (7C269)
OUTPUT
VALID DATA
ASYNCHRONOUS INIT. (7C269 PROGRAMMABLE)
ASYNCHRONOUS ENABLE
t_{AS}
t_{AH}
t_{HES}
t_{ESS}
t_{PWC}
t_{RI}
t_{LZC}
t_{CO}
t_{DI}
t_{HZC}
t_{PWI}
t_{HZE}
t_{LZE}

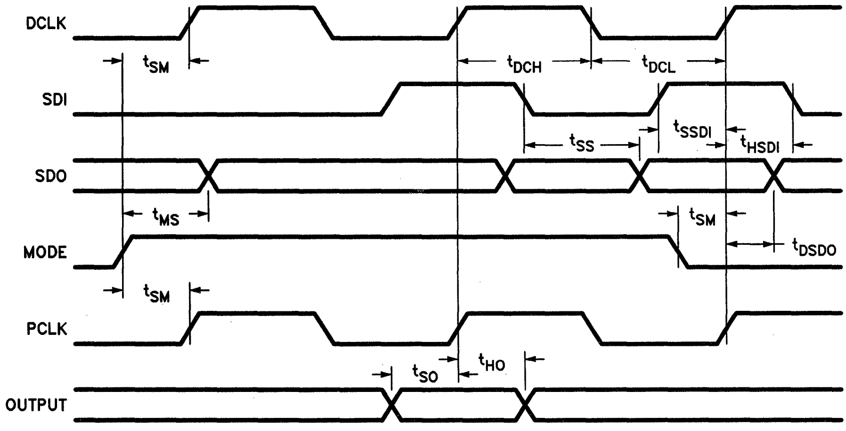
0112-9

Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

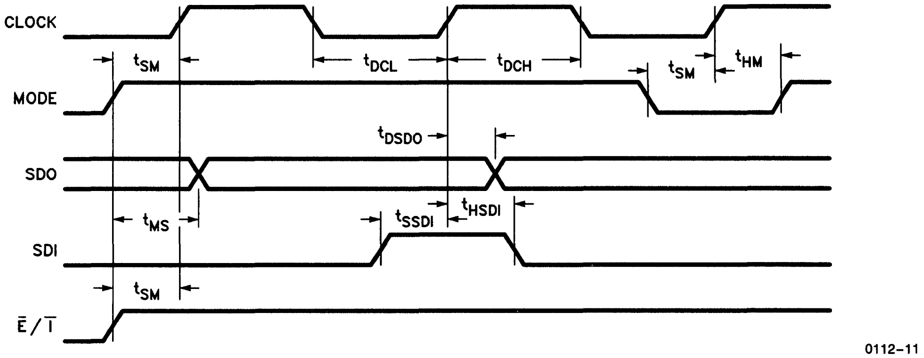
7C268 Diagnostic Waveforms


DCLK
SDI
SDO
MODE
PCLK
OUTPUT
t_{SM}
t_{DCH}
t_{DCL}
t_{SS}
t_{SSDI}
t_{HSDI}
t_{MS}
t_{SM}
t_{DSDO}
t_{SM}
t_{SO}
t_{HO}

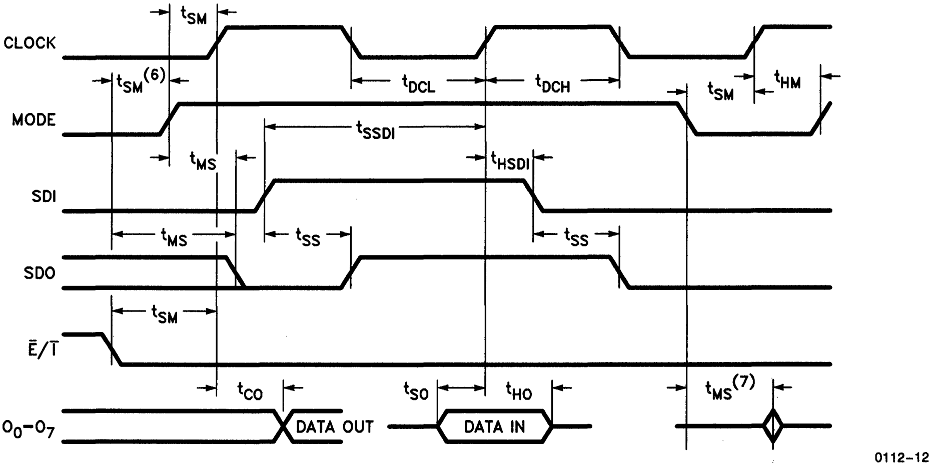
0112-10

Switching Waveforms (Continued)

7C269 Diagnostic Application (Shifting the Shadow Register)


CLOCK
MODE
SDO
SDI
Ē/T̄
tSM
tDCL
tDCH
tSM
tHM
tDSDO
tMS
tSSDI
tHSDI
tSM
0112-11

7C269 Diagnostic Application (Parallel Data Transfer)


tSM
CLOCK
tSM(6)
tDCL
tDCH
tSM
tHM
MODE
tSSDI
tMS
tHSDI
SDI
tMS
tSS
tSS
SDO
tSM
Ē/T̄
tCO
tSO
tHO
tMS(7)
O0–O7
DATA OUT
DATA IN
0112-12

Notes:

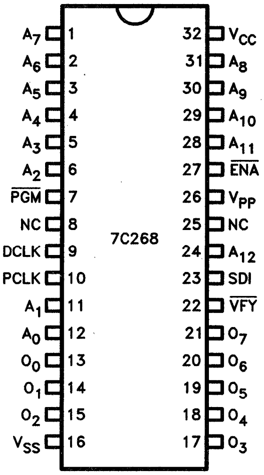
6. Asynchronous enable mode only.
7. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H → L) then the output impedance change delay is t_{MS}.

Device Programming

The CY7C268 and CY7C269 program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

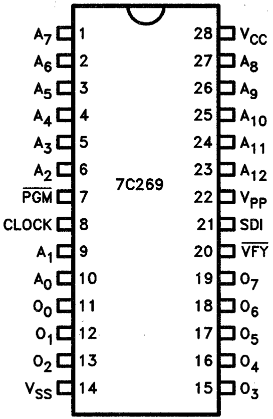
Programming Pinout

The Programming Pinout of both devices is shown in *Figures 3a* and *3b.* The programming mode is entered by putting 12.5V on the V_{PP} pin. The addressed location is programmed and verified with the application of a $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ pulse. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.



0112–13

Figure 3a. 7C268 Programming Pinout



0112–14

Figure 3b. 7C269 Programming Pinout

Programming and Blankcheck (Memory Bits)

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{\mathrm{VFY}}$ toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s. (Refer to mode table for pin states)

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing 12.5V on V_{PP}. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{\mathrm{PGM}}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{\mathrm{VFY}}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{\mathrm{VFY}}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{\mathrm{PGM}}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

After all locations are programmed, they should be verified at $V_{CCP} = 5.0V$.

Programming Algorithm for the Architecture

Both the 7C268 and 7C269 offer a limited selection of programmed architecture. Programming these features should be done with a single 10 ms wide pulse in place of the intelligent algorithm mainly because these features are verified operationally, not with the $\overline{\mathrm{VFY}}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C269 architecture V_{PP} is applied to pins 3, 9 and 22 while in programming the 7C268 architecture V_{PP} is applied to pins 3, 11, 26. Specific choice of a particular mode will depend on the states of the other pins during programming so it is important that the condition of the other pins be met as set forth in the mode table. The same considerations with respect to power up and power down apply during architecture programming as during intelligent programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{\mathrm{PGM}}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

To check whether a 7C269 has been programmed as output enable or initialize enable, pin 22 ($\overline{\mathrm{E}}/\overline{\mathrm{I}}$) should be pulled LOW followed by a LOW to HIGH transition on pin 8 (CLOCK). The data read at the outputs is stored and complement data is shifted into the shadow register. A shift from shadow to pipeline is performed and the CLOCK is again pulled from LOW to HIGH. At this point, if the new data read is data-complement, the device has been programmed as Output enable while if the new data read-true then the device is programmed as Initialize enable and the configuration of the Initialize byte can be read directly by pulling $\overline{\mathrm{E}}/\overline{\mathrm{I}}$ from HIGH to LOW.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM signals required for read mode are shown in the Mode Tables.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{\text{PGM}}$) signal and pin 23 becomes an active LOW verify ($\overline{\text{VFY}}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{\text{PGM}}$ is LOW, and $\overline{\text{VFY}}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{\text{PGM}}$ HIGH and $\overline{\text{VFY}}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in *Figure 4* is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams' AC and DC parameters accurately describe this complete operation. Note should be taken of the inner and outer addressing loops which allow 256 bytes to be programmed each time the onboard register containing the upper 5 address bits is loaded.

The timing diagram in *Figure 5* contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in the inner loops of *Figure 5,* some for the outer loop where the upper address is advanced, and some pertains only to entry and exit from the programming mode of operation.

In particular, the timing sequence associated with the Latch signal on pin 21 and addresses AY8 through AY12 pertain only to the outer loop where the upper 5 (N in the flow chart) address bits are incremented.

t_P, t_{PD} and t_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to LATCH, $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ operations.

t_{DS}, t_{AS}, t_{AH} and t_{DH} refer to the required setup and hold times for the address and data for $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ operations. These parameters must be adhered to, in all operations, including $\overline{\text{VFY}}$. This precludes the option then of verifying the device by holding the $\overline{\text{VFY}}$ signal LOW, and sequencing the addresses.

Mode Table 7C268

Mode Select	P2 A6	P3 A5	P30 A9	P6 A2	P7 MD $\overline{\text{PGM}}$	P9 DCLK	P10 PCLK	P11 A1	P12 A0	P22 SDO $\overline{\text{VFY}}$	P23 SDI	P24 A12	P26 $\overline{\text{INT}}$ V_{PP}	P27 $\overline{E/E_S}$	P28 A11
Normal Read[2]	A6	A5	A9	A2	L	X	L/H	A1	A0	SDO	X	A12	H	H/L	A11
Load SR to PR[2]	A6	A5	A9	A2	H	L	L/H	A1	A0	SDI	X	A12	H	X	A11
Load Output to SR	A6	A5	A9	A2	H	L/H	L	A1	A0	SDI	L	A12	H	H	A11
Shift Shadow[2]	A6	A5	A9	A2	L	L/H	L	A1	A0	SDO	DIN	A12	H	X	A11
Program (Memory)	A6	A5	A9	A2	L	L	L	A1	A0	H	L	A12	V_{PP}	H	A11
Program Verify	A6	A5	A9	A2	H	L	L	A1	A0	L	L	A12	V_{PP}	H	A11
Program Inhibit	A6	A5	A9	A2	H	L	L	A1	A0	H	L	A12	V_{PP}	H	A11
Async. Enable Read	A6	A5	A9	A2	L	L	X	A1	A0	SDO	L	A12	H	H/L	A11
Sync. Enable Read	A6	A5	A9	A2	L	L	L/H	A1	A0	SDO	L	A12	H	H/L	A11
Async. Init. Read	A6	A5	A9	A2	L	L	X	A1	A0	SDO	L	A12	L	L	A11
Program Sync. Enable[1]	H	V_{HH}	X	H	L	L	L	V_{HH}	L	H	L	H	V_{PP}	H	H
Program Initial Byte	H	V_{HH}	X	L	L	L	L	V_{HH}	H	H	L	X	V_{PP}	H	L

Notes:

1. Default is Async. Enable.
2. For the asynchronous enable operation, the data out is enabled by bringing $\overline{E}$ LOW. For the synchronous enable operation, data out is enabled on the first LOW to HIGH clock transition after $\overline{E}$ is brought LOW. When $\overline{E}$ goes from LOW to HIGH (enable to disable) the outputs will go to the high impedance state (after a propagation delay) immediately if the asynchronous enable was programmed. If the synchronous enable was selected, a LOW to HIGH clock transition is required.

Mode Table 7C269

Mode Select	P2 A6	P3 A5	P26 A9	P6 A2	P7 MD $\overline{\text{PGM}}$	P8 CLK	P9 A1	P10 A0	P21 SDI	P20 SDO $\overline{\text{VFY}}$	P24 A11	P22 $\overline{\text{E}}/\overline{\text{I}}$ V_{PP}	P23 A12
Normal Read	A6	A5	A9	A2	L	L/H	A1	A0	X	HI Z	A11	H/L	A12
Load SR to PR[3]	A6	A5	A9	A2	H	L/H	A1	A0	L	SDI	A11	L	A12
Load Output to SR[3]	A6	A5	A9	A2	H	L/H	A1	A0	H	SDI	A11	L	A12
Shift Shadow[3]	A6	A5	A9	A2	H	L/H	A1	A0	DIN	SDO	A11	H	A12
Program (Memory)	A6	A5	A9	A2	L	L	A1	A0	X	H	A11	V_{PP}	A12
Program Verify	A6	A5	A9	A2	H	L	A1	A0	X	L	A11	V_{PP}	A12
Program Inhibit	A6	A5	A9	A2	H	L	A1	A0	X	H	A11	V_{PP}	A12
Async. Enable Read	A6	A5	A9	A2	L	L	A1	A0	X	HI Z	A11	L	A12
Sync. Enable Read	A6	A5	A9	A2	L	L/H	A1	A0	X	HI Z	A11	L	A12
Async. Init. Read	A6	A5	A9	A2	L	L	A1	A0	X	HI Z	A11	L	A12
Program Sync. Enable[1]	H	V_{HH}	A9	H	L	L	V_{HH}	L	X	H	H	V_{PP}	H
Program Initialize[2]	H	V_{HH}	A9	L	L	L	V_{HH}	L	X	H	H	V_{PP}	L
Program Initial Byte	H	V_{HH}	A9	L	L	L	V_{HH}	H	X	H	L	V_{PP}	A12

Notes:

1. Default is Async. Enable.
2. Default is Enable.
3. If $\overline{\text{I}}$ selected, outputs always enabled. If $\overline{\text{E}}$ selected, during diagnostic operation the data outputs will remain in the state they were in when the mode was entered. When enabled, the data outputs will reflect the outputs of the pipeline register. Any changes in the data in the pipeline register will appear on the data output pins.

DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current	50		mA
V_{IHP}	Input High Voltage During Programming	3.0		V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

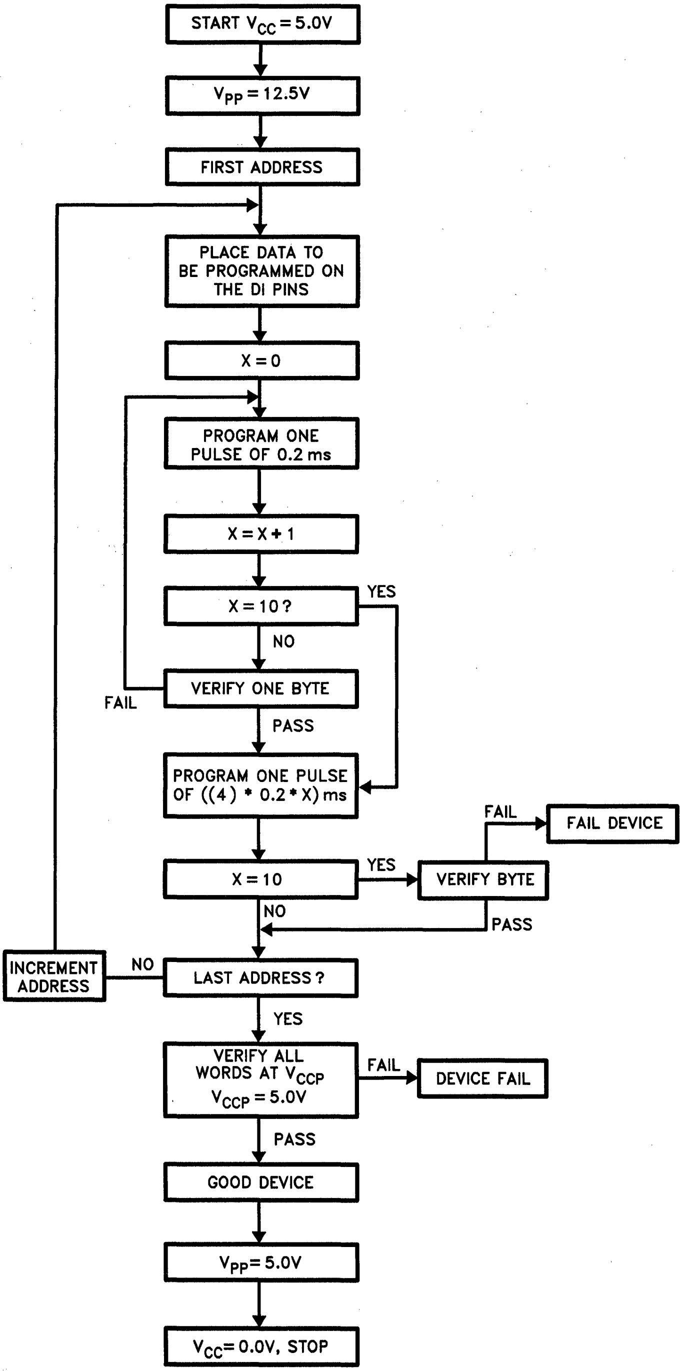
AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
t_{PP}	Program Pulse Width (Per Byte)		10.0	ms
t_{AS}	Address Set-up Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_{DS}	Data Set-up Time	1.0		μs
$t_{R,F}$	V_{PP} Rise and Fall Time	1.0		μs
t_{DV}	Delay to Verify	1.0		μs
t_{VD}	Verify to Data Out		1.0	μs
t_{VH}	Data Hold Time from Verify		1.0	μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DZ}	Verify to High Z		1.0	μs

Erasure Characteristics

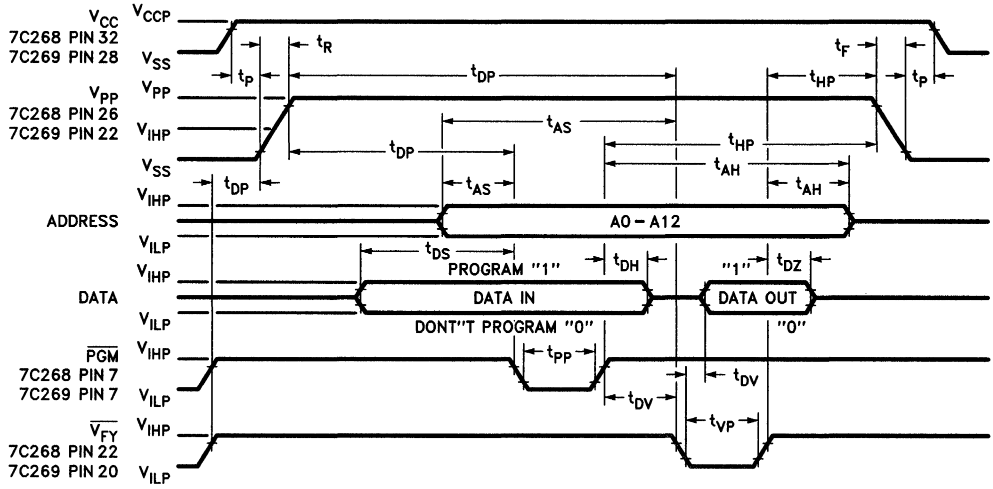
Wavelengths of light less than 4000 Angstroms begin to erase the 7C268 and 7C269 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C268 or 7C269 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.


START V_{CC} = 5.0V
V_{PP} = 12.5V
FIRST ADDRESS
PLACE DATA TO BE PROGRAMMED ON THE DI PINS
X = 0
PROGRAM ONE PULSE OF 0.2 ms
X = X + 1
X = 10 ?
YES
NO
VERIFY ONE BYTE
FAIL
PASS
PROGRAM ONE PULSE OF ((4) * 0.2 * X) ms
FAIL
FAIL DEVICE
X = 10
YES
VERIFY BYTE
NO
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS ?
YES
VERIFY ALL WORDS AT V_{CCP} V_{CCP} = 5.0V
FAIL
DEVICE FAIL
PASS
GOOD DEVICE
V_{PP}= 5.0V
V_{CC}= 0.0V, STOP

0112-15

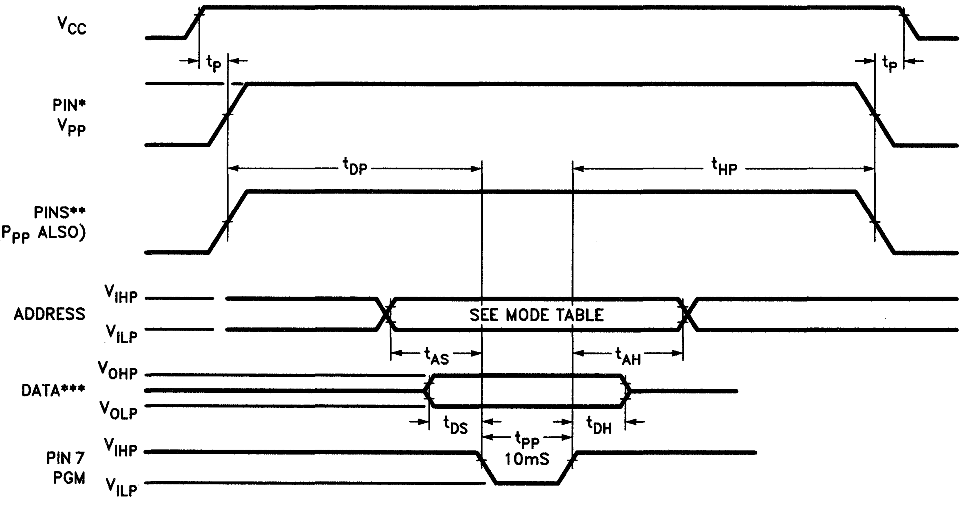
Figure 4. Programming Flowchart


VCC
7C268 PIN 32
7C269 PIN 28
VCCP
VSS
VPP
7C268 PIN 26
7C269 PIN 22
VPP
VIHP
VSS
ADDRESS
VIHP
VILP
DATA
VIHP
VILP
PGM
7C268 PIN 7
7C269 PIN 7
VIHP
VILP
VFY
7C268 PIN 22
7C269 PIN 20
VIHP
VILP
tR
tF
tP
tDP
tHP
tAS
tAH
tDS
tDH
tDZ
tPP
tDV
tVP
A0 - A12
PROGRAM "1"
DATA IN
DONT"T PROGRAM "0"
"1"
DATA OUT
"0"

0112-16

Figure 5. Programming Waveforms (Memory)

Note:
Power, VPP and VCC should not be cycled for each program verify cycle but remain static during programming.


VCC
PIN*
VPP
PINS**
(PPP ALSO)
ADDRESS
VIHP
VILP
DATA***
VOHP
VOLP
PIN 7
PGM
VIHP
VILP
tP
tDP
tHP
SEE MODE TABLE
tAS
tAH
tDS
tPP
10mS
tDH

0112-17

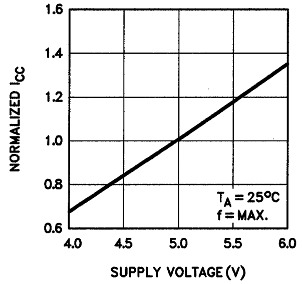
*7C268-pin 26
7C269-pin 22
**7C268-pins 3, 11
7C269-pins 3, 9

***Data required on I/O's only during initial byte programming

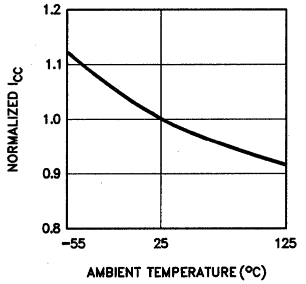
Figure 6. Programming Waveforms for the Architecture CY7C268 and CY7C269

Typical DC and AC Characteristics

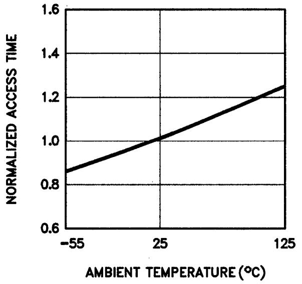
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



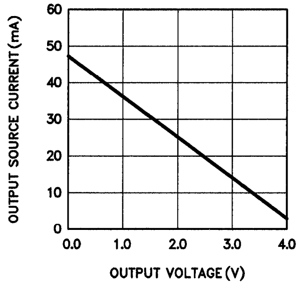
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



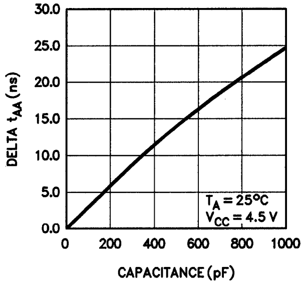
NORMALIZED ACCESS TIME vs. TEMPERATURE



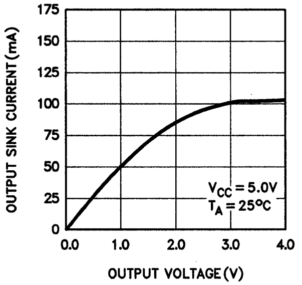
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0112–18

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
40	100	CY7C268-40DC	D20	Commercial
		CY7C268-40WC	W20	
		CY7C269-40PC	P21	
		CY7C269-40DC	D22	
		CY7C269-40WC	W22	
50	80	CY7C268-50DC	D20	
		CY7C268-50WC	W20	
		CY7C269-50PC	P21	
		CY7C269-50DC	D22	
		CY7C269-50WC	W22	
	120	CY7C268-50DMB	D20	Military
		CY7C268-50WMB	W20	
		CY7C268-50LMB	L55	
		CY7C268-50QMB	Q55	
		CY7C269-50DMB	D22	
		CY7C269-50WMB	W22	
		CY7C269-50LMB	L64	
		CY7C269-50QMB	Q64	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
60	80	CY7C268-60DC	D20	Commercial
		CY7C268-60WC	W20	
		CY7C269-60PC	P21	
		CY7C269-60DC	D22	
		CY7C269-60WC	W22	
	100	CY7C268-60DMB	D20	Military
		CY7C268-60WMB	W20	
		CY7C268-60LMB	L55	
		CY7C268-60QMB	Q55	
		CY7C269-60DMB	D22	
		CY7C269-60WMB	W22	
		CY7C269-60LMB	L64	
		CY7C269-60QMB	Q64	

PRELIMINARY **CY7C271**

32,768 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 55 ns (commercial)**
  - **— 65 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 715 mW (military)**
- **Super low standby power**
  - **— Less than 165 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding > 2001V static discharge**

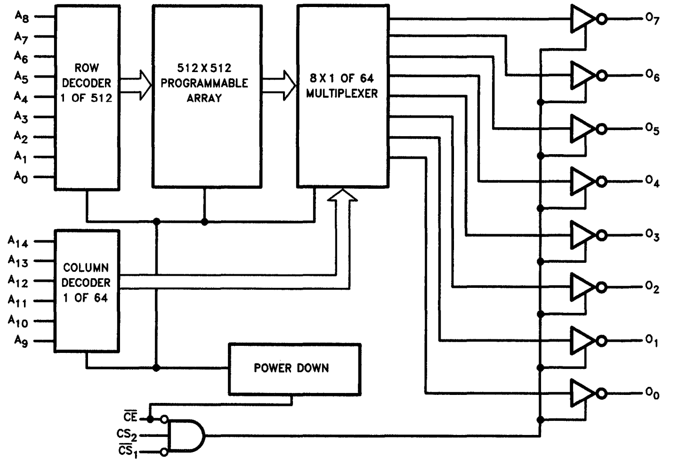
Product Characteristics

The CY7C271 is a high performance 32,768 word by 8 bit CMOS PROM. When deselected, the 7C271 automatically powers down into a low power standby mode. It is packaged in the 600 mil wide package. The 7C271 reprogrammable CERDIP package is equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 is a plug-in replacement for bipolar devices and offers the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

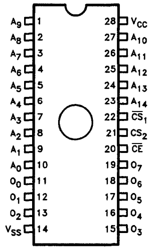
Reading is accomplished by placing active LOW signals on $\overline{CS}_1$, and $\overline{CE}$ and an active HIGH on CS_2. The contents of the memory location addressed by the address lines (A_0–A_{14}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

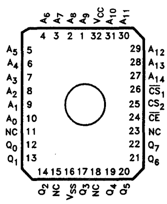

A8
A7
A6
A5
A4
A3
A2
A1
A0
ROW DECODER 1 OF 512
512 X 512 PROGRAMMABLE ARRAY
8 X 1 OF 64 MULTIPLEXER
O7
O6
O5
O4
O3
O2
O1
O0
A14
A13
A12
A11
A10
A9
COLUMN DECODER 1 OF 64
POWER DOWN
CE
CS2
CS1

0102-1

Pin Configurations


A9 1
A8 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
VSS 14
28 VCC
27 A10
26 A11
25 A12
24 A13
23 A14
22 CS1
21 CS2
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3

0102-2


A6 A7 A8 A9 VCC A10 A11
4 3 2 1 32 31 30
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
NC 11
O0 12
O1 13
29 A12
28 A13
27 A14
26 CS1
25 CS2
24 CE
23 NC
22 O7
21 O6
14 15 16 17 18 19 20
O2 NC VSS O3 NC O4 O5

0102-3

Selection Guide

		7C271-55	7C271-65	7C271-75
Maximum Access Time (ns)		55	65	75
Maximum Operating Current (mA)	Commercial	120	120	
	Military		130	130
Standby Current (mA)	Commercial	30	30	
	Military		35	35

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage
(Pin 21 DIP, Pin 24 LCC) 14.0V

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C271-55		7C271-65		7C271-75		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA*			0.5		0.5		0.5	V
V_{IH}	Input HIGH Level[1]			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level[1]				0.8		0.8		0.8	V
I_{IX}	Input Current	V_{CC} = Max., V_{CC} = GND		−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		Note 2		
I_{OZ}	Output Leakage Current	$V_{OL} \leq V_{OUT} \leq V_{OH}$, Output Disabled		−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		120		120			mA
			Military				130		130	mA
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ I_{OUT} = 0 mA	Commercial		30		30			mA
			Military				35		35	mA

*8.0 mA military

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C271 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Measured on a sample basis.

Switching Characteristics Over the Operating Range[5]

Parameters	Description	7C271-55		7C271-65		7C271-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		55		65		75	ns
t_{HZCS}	Chip Select Inactive to High Z[6] ($\overline{CS}_1$ and CS_2 Only)		30		35		45	ns
t_{ACS}	Chip Select Active to Output Valid ($\overline{CS}_1$ and CS_2 Only)		30		35		45	ns
t_{HZCE}	Chip Enable Inactive to High Z[6] ($\overline{CE}$ Only)		60		65		75	ns
t_{ACE}	Chip Enable Active to Output Valid ($\overline{CE}$ Only)		60		65		75	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		60		65		75	ns

AC Test Loads and Waveforms

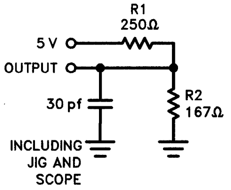
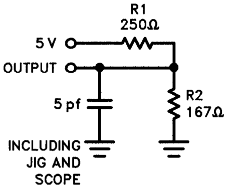
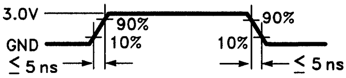

R1
250Ω
5 V
OUTPUT
30 pf
R2
167Ω
INCLUDING
JIG AND
SCOPE

Figure 1a


R1
250Ω
5 V
OUTPUT
5 pf
R2
167Ω
INCLUDING
JIG AND
SCOPE

0102-4

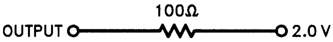
Figure 1b


3.0V
GND
90%
10%
10%
90%
≤ 5 ns
≤ 5 ns

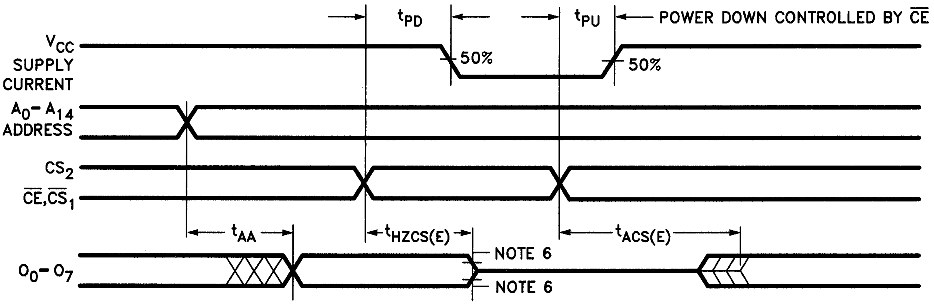
0102-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT


100Ω
OUTPUT
2.0 V

0102-5


tPD
tPU
POWER DOWN CONTROLLED BY CE
VCC SUPPLY CURRENT
50%
50%
A0- A14 ADDRESS
CS2
CE,CS1
tAA
tHZCS(E)
tACS(E)
NOTE 6
NOTE 6
O0- O7

0102-7

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
6. $t_{HZCS(E)}$ is tested with load shown in *Figure 1b.* Transition is measured at steady state High level − 500 mV or steady state Low level + 500 mV on the output from the 1.5 level on the input.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C271 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C271 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

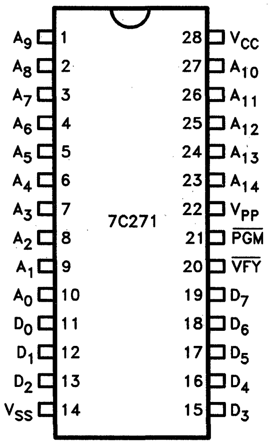
Table 2. DC Programming Parameters $T_A = 25°C$

Parameters	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0	V_{CCP}	V
V_{ILP}	Input Low Voltage During Programming		0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

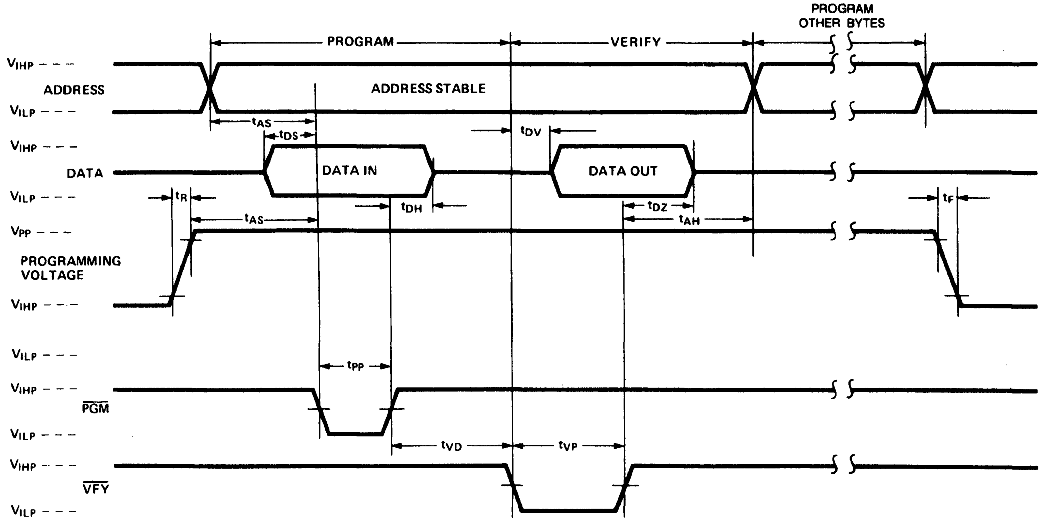
Table 3. AC Programming Parameters $T_A = 25°C$

Parameters	Description	Min.	Max.	Units
T_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
T_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
T_{PP}	Program Pulse Width	0.1	10	ms
$T_{R,F}$	V_{PP} Rise and Fall Time	100		μs
T_{DV}	Delay to Verify	1.0		μs
T_{VD}	Verify to Data Out		1.0	μs
T_{VH}	Data Hold Time from Verify		1.0	μs
T_{VP}	Verify Pulse Width	2.0		μs
T_{DZ}	Verify to High Z		1.0	μs
T_P	Power Up/Down	20.0		ms

7C271 Programming Pin-Out


7C271
A9 1
A8 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
VSS 14
28 VCC
27 A10
26 A11
25 A12
24 A13
23 A14
22 VPP
21 PGM
20 VFY
19 D7
18 D6
17 D5
16 D4
15 D3

0102–8


PROGRAM
VERIFY
PROGRAM OTHER BYTES
V_{IHP}
ADDRESS
V_{ILP}
ADDRESS STABLE
t_{AS}
t_{DS}
t_{DV}
V_{IHP}
DATA
V_{ILP}
DATA IN
DATA OUT
t_R
t_{DH}
t_{DZ}
t_{AS}
t_{AH}
t_F
V_{PP}
PROGRAMMING VOLTAGE
V_{IHP}
V_{ILP}
t_{PP}
V_{IHP}
$\overline{PGM}$
V_{ILP}
t_{VD}
t_{VP}
V_{IHP}
$\overline{VFY}$
V_{ILP}

0102-9

Figure 3. PROM Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
55	CY7C271-55PC	P15	Commercial
	CY7C271-55WC	W16	
65	CY7C271-65PC	P15	
	CY7C271-65WC	W16	
	CY7C271-65DMB	D16	Military
	CY7C271-65WMB	W16	
	CY7C271-65LMB	L55	
	CY7C271-65QMB	Q55	
75	CY7C271-75DMB	D16	Military
	CY7C271-75WMB	W16	
	CY7C271-75LMB	L55	
	CY7C271-75QMB	Q55	

CYPRESS
SEMICONDUCTOR

CY7C281
CY7C282

1024 x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 45 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 or standard 600 mil DIP or 28 pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding > 2000V static discharge**

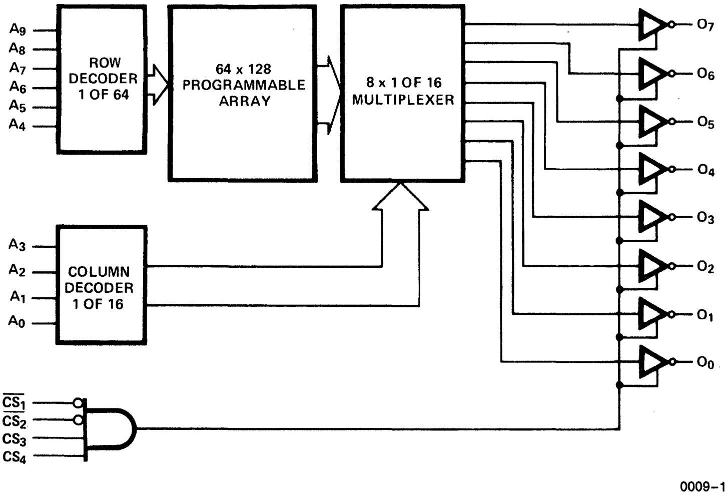
Product Characteristics

The CY7C281 and CY7C282 are high performance 1024 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The CY7C281 is also available in a 28 pin leadless chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C281 and CY7C282 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0–A_9) will become available on the output lines (O_0–O_7).

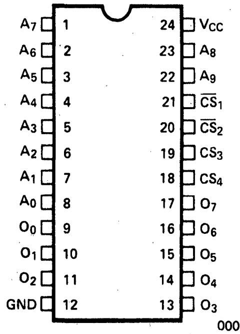
Logic Block Diagram



A9
A8
A7
A6
A5
A4
ROW DECODER 1 OF 64
64 x 128 PROGRAMMABLE ARRAY
8 x 1 OF 16 MULTIPLEXER
O7
O6
O5
O4
O3
O2
O1
O0
A3
A2
A1
A0
COLUMN DECODER 1 OF 16
CS1
CS2
CS3
CS4

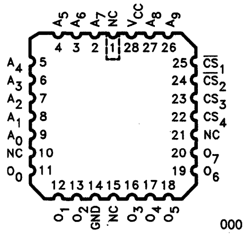
0009–1

Pin Configurations



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 CS1
20 CS2
19 CS3
18 CS4
17 O7
16 O6
15 O5
14 O4
13 O3

0009–2



A5 A6 A7 NC VCC A8 A9
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 CS1
24 CS2
23 CS3
22 CS4
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

0009–3

Selection Guide

		7C281-30 7C282-30	7C281-45 7C282-45
Maximum Access Time (ns)		30	45
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12). . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State. . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage . . . . >2001V (per MIL-STD-883, Method 3015.2)

Latch-up Current. . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C281-30 7C282-30		7C281-45 7C282-45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[2]			2.0		2.0		V
V_{IL}	Input LOW Level[2]				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	mA

Capacitance[1]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Measured on a sample base.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. The CMOS process does not provide a clamp diode. However, the CY7C281 & CY7C282 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Switching Characteristics Over the Operating Range[5]

Parameters	Description	CY7C281-30 CY7C282-30		CY7C281-45 CY7C282-45		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z[6]		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		20		25	ns

AC Test Loads and Waveforms

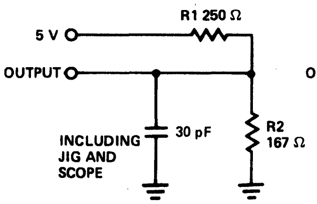
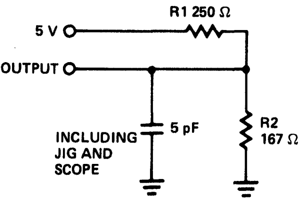

R1 250 Ω
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
30 pF
R2
167 Ω

Figure 1a


R1 250 Ω
5 V
OUTPUT
INCLUDING
JIG AND
SCOPE
5 pF
R2
167 Ω

0009-4

Figure 1b

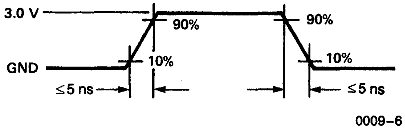
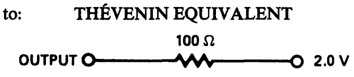
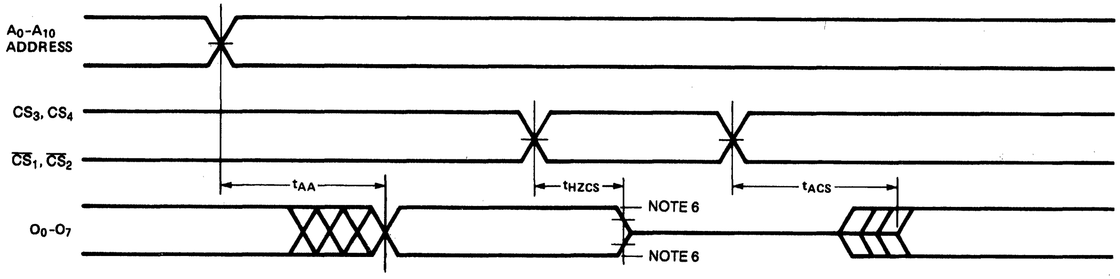

3.0 V
GND
90%
10%
90%
10%
≤5 ns
≤5 ns
0009-6

Figure 2. Input Pulses

Equivalent to:


THÉVENIN EQUIVALENT
100 Ω
OUTPUT
2.0 V

0009-5

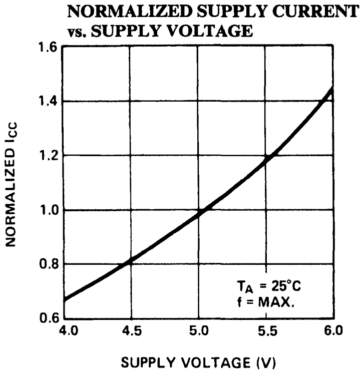

A0-A10
ADDRESS
CS3, CS4
CS1, CS2
O0-O7
tAA
tHZCS
tACS
NOTE 6
NOTE 6

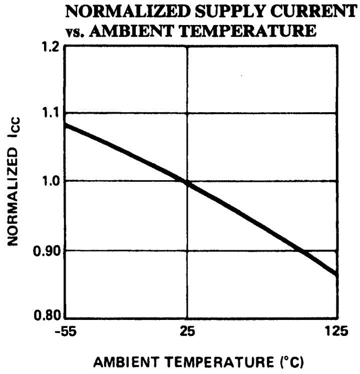
0009-7

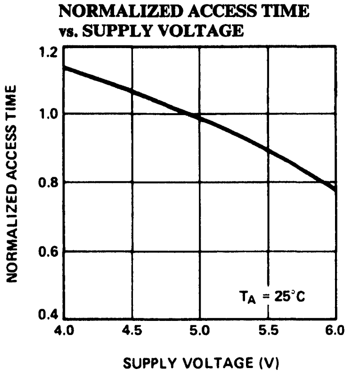
Notes:

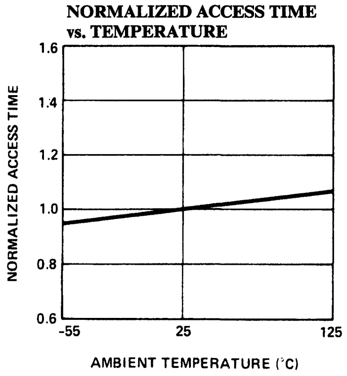
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
6. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level + 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

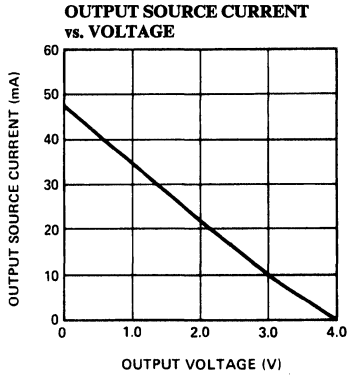
Typical DC and AC Characteristics

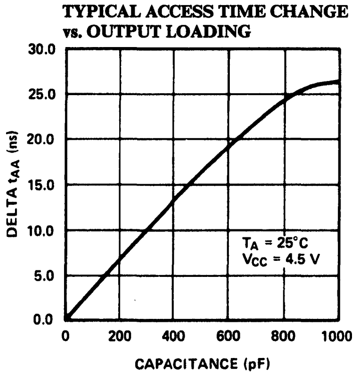


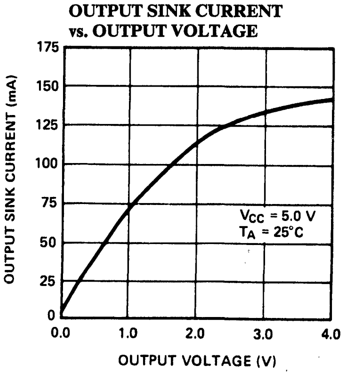




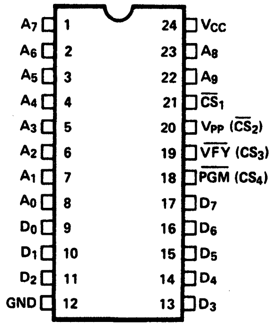








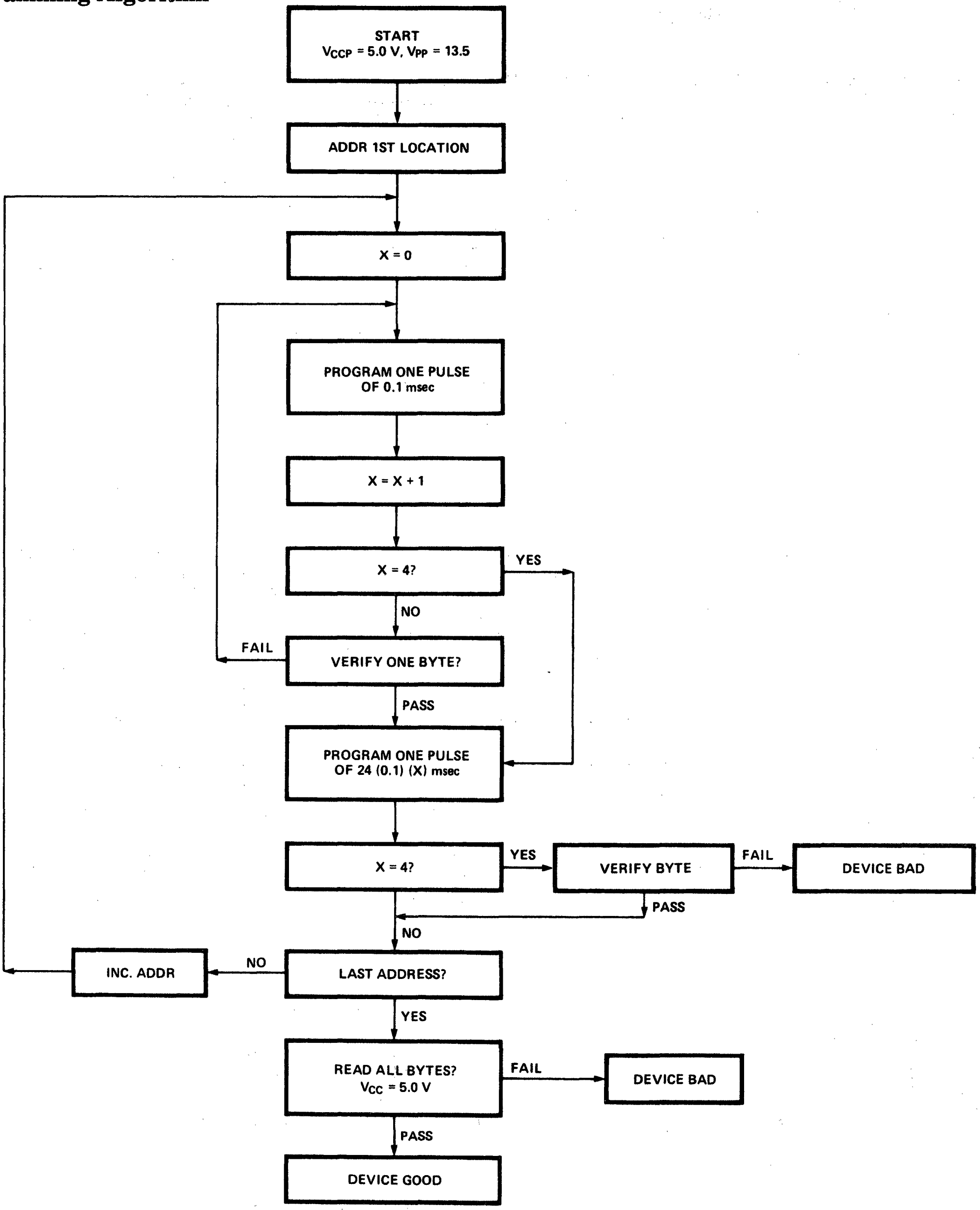
0009-8


A_7 1
A_6 2
A_5 3
A_4 4
A_3 5
A_2 6
A_1 7
A_0 8
D_0 9
D_1 10
D_2 11
GND 12
24 V_{CC}
23 A_8
22 A_9
21 $\overline{CS_1}$
20 V_{PP} ($\overline{CS_2}$)
19 $\overline{VFY}$ (CS_3)
18 $\overline{PGM}$ (CS_4)
17 D_7
16 D_6
15 D_5
14 D_4
13 D_3

0009-9

Figure 3. Programming Pinout

Programming Algorithm


START
VCCP = 5.0 V, VPP = 13.5
ADDR 1ST LOCATION
X = 0
PROGRAM ONE PULSE OF 0.1 msec
X = X + 1
X = 4?
YES
NO
FAIL
VERIFY ONE BYTE?
PASS
PROGRAM ONE PULSE OF 24 (0.1) (X) msec
X = 4?
YES
VERIFY BYTE
FAIL
DEVICE BAD
PASS
NO
INC. ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? VCC = 5.0 V
FAIL
DEVICE BAD
PASS
DEVICE GOOD

0009-10

The CY7C281 and CY7C282 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CC} = 5.0. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C281 and 7C282 1K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMS are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is neccessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function				Outputs (9–11, 13–17)
	Read or Output Disable	CS_4	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS}_1$	
	Pin Number	(18)	(19)	(20)	(21)	
Read		V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	X	High Z
Output Disable[4]		X	V_{IL}	X	X	High Z
Output Disable[4]		V_{IL}	X	X	X	High Z
Output Disable[4]		X	X	X	V_{IH}	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	Zeros

Notes:

4. X = Don't care but not to exceed V_{CC} +5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 1K x 8

Power the device for normal read mode operation with pin 18, 19, 20, and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Tables 3 and 4. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 × the sum of the previous programming pulses before advancing to the next address to repeat the process.

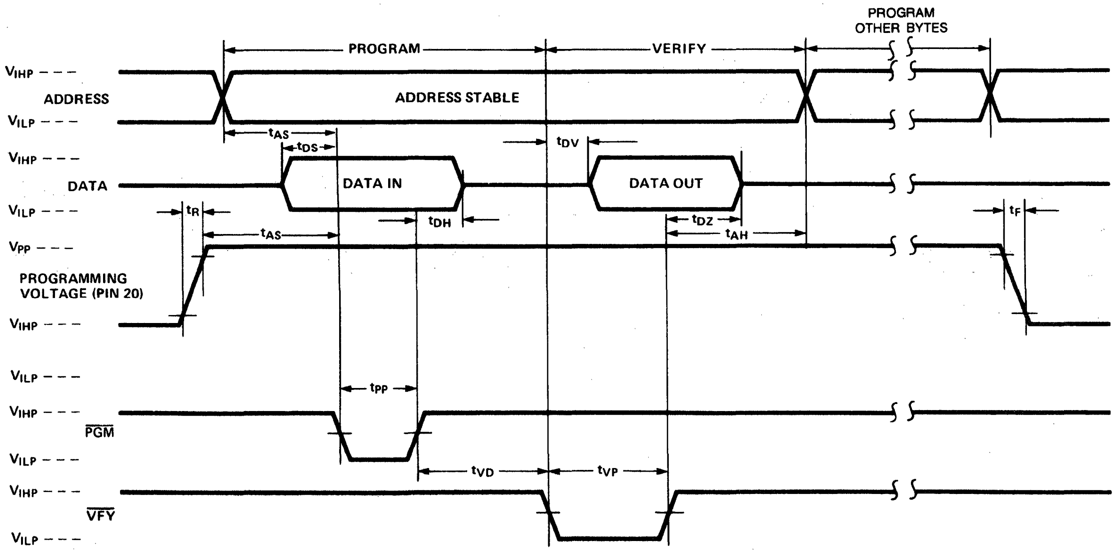

PROGRAM
VERIFY
PROGRAM OTHER BYTES
VIHP
ADDRESS
VILP
ADDRESS STABLE
tAS
tDS
tDV
VIHP
DATA
DATA IN
DATA OUT
VILP
tR
tDH
tDZ
tAH
tAS
tF
VPP
PROGRAMMING VOLTAGE (PIN 20)
VIHP
VILP
tPP
VIHP
PGM
VILP
tVD
tVP
VIHP
VFY
VILP
0009-11

Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30 ns	CY7C281-30PC	P13	Commercial
	CY7C282-30PC	P11	
	CY7C281-30DC	D14	
	CY7C281-30LC	L64	
	CY7C282-30DC	D12	
45 ns	CY7C281-45PC	P13	Commercial
	CY7C282-45PC	P11	
	CY7C281-45DC	D14	
	CY7C281-45LC	L64	
	CY7C282-45DC	D12	
	CY7C281-45DMB	D14	Military
	CY7C281-45LMB	L64	
	CY7C282-45DMB	D12	

CYPRESS
SEMICONDUCTOR

CY7C291
CY7C292

Reprogrammable 2048 x 8 PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 330 mW (commercial)**
  - **— 413 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

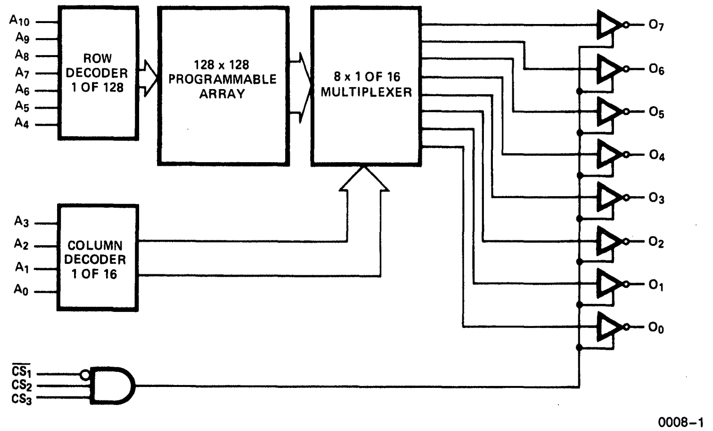
Product Characteristics

The CY7C291 and CY7C292 are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide plastic and hermetic DIP packages respectively. The 300 mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

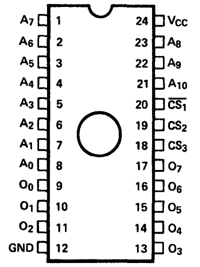
Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram


A10
A9
A8
A7
A6
A5
A4
ROW DECODER 1 OF 128
128 x 128 PROGRAMMABLE ARRAY
8 x 1 OF 16 MULTIPLEXER
O7
O6
O5
O4
O3
O2
O1
O0
A3
A2
A1
A0
COLUMN DECODER 1 OF 16
CS1
CS2
CS3

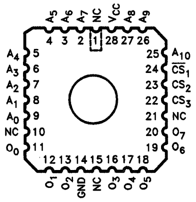
0008-1

Pin Configurations


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 CS1
19 CS2
18 CS3
17 O7
16 O6
15 O5
14 O4
13 O3

0008-2

Window available on 300 mil cerdip only


A5 A6 A7 NC VCC A8 A9
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
O0 11
25 A10
24 CS1
23 CS2
22 CS3
21 NC
20 O7
19 O6
12 13 14 15 16 17 18
O1 O2 GND NC O3 O4 O5

0008-3

Selection Guide

			7C291-35 7C292-35	7C291-50 7C292-50
Maximum Access Time (ns)			35	50
Maximum Operating Current (mA)	STD	Commercial	90	90
		Military	120*	120
	L	Commercial	60	60

*7C291 only

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

UV Exposure .... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to + 125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C291L-35, 50 7C292L-35, 50		7C291-35, 50 7C292-35, 50		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}[1]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[1]	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		60		90	mA
			Military*				120	mA

*-35: 7C291 only

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C291 & CY7C292 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Measured on a sample basis.

Switching Characteristics Over the Operating Range[5]

Parameters	Description	7C291-35 7C292-35		7C291-50 7C292-50		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		35		50	ns
t_{HZCS}	Chip Select Inactive to High Z[6]		25		25	ns
t_{ACS}	Chip Select Active to Output Valid		25		25	ns

AC Test Loads and Waveforms

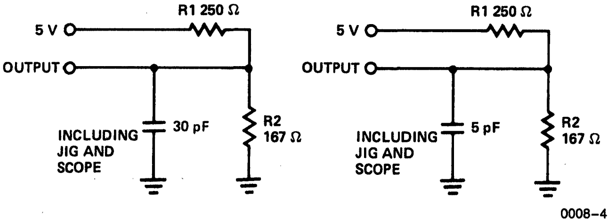

R1 250 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
30 pF
R2 167 Ω
R1 250 Ω
5 V
OUTPUT
INCLUDING JIG AND SCOPE
5 pF
R2 167 Ω
0008-4

Figure 1a

Figure 1b

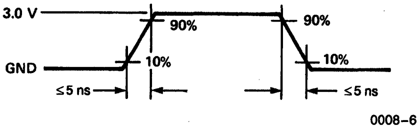
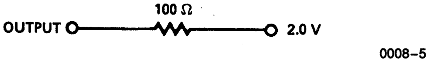
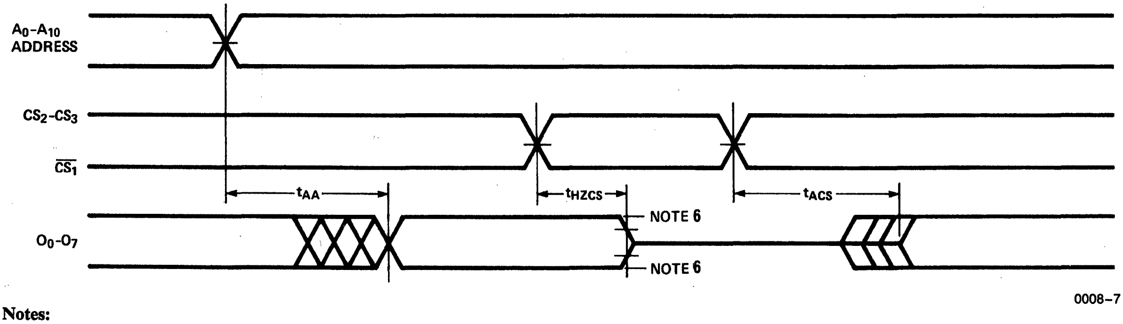

3.0 V
GND
90%
10%
90%
10%
≤5 ns
≤5 ns
0008-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT


100 Ω
OUTPUT
2.0 V
0008-5

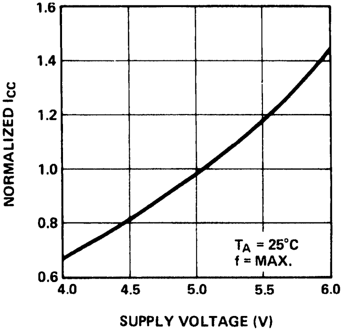

A_0-A_{10} ADDRESS
CS_2-CS_3
$\overline{CS_1}$
t_{AA}
t_{HZCS}
t_{ACS}
NOTE 6
NOTE 6
O_0-O_7
0008-7

Notes:

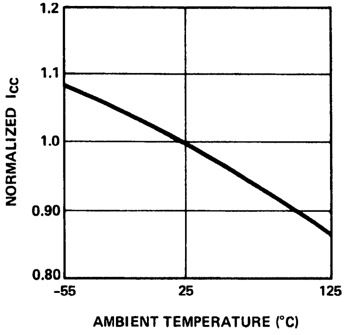
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figures 1a, 1b.*
6. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

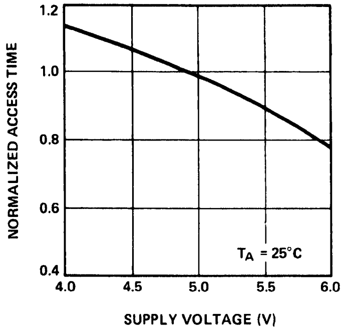
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



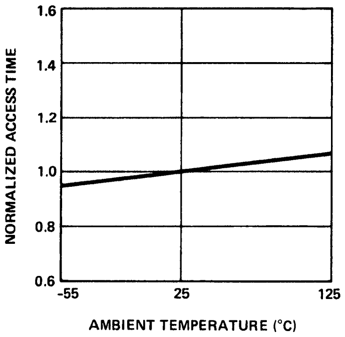
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



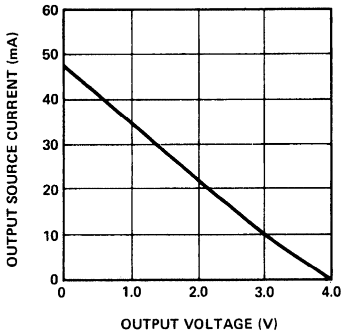
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



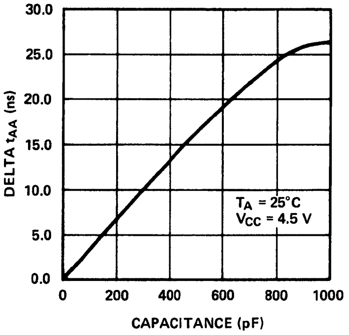
NORMALIZED ACCESS TIME vs. TEMPERATURE



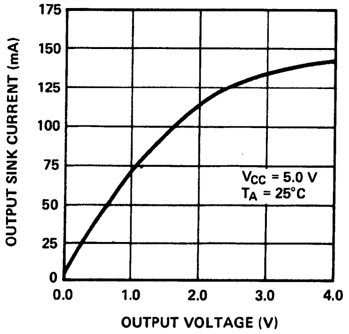
OUTPUT SOURCE CURRENT vs. VOLTAGE



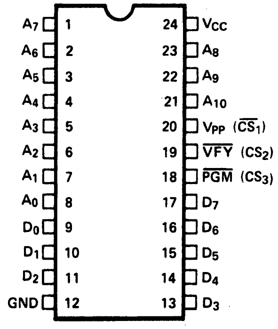
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



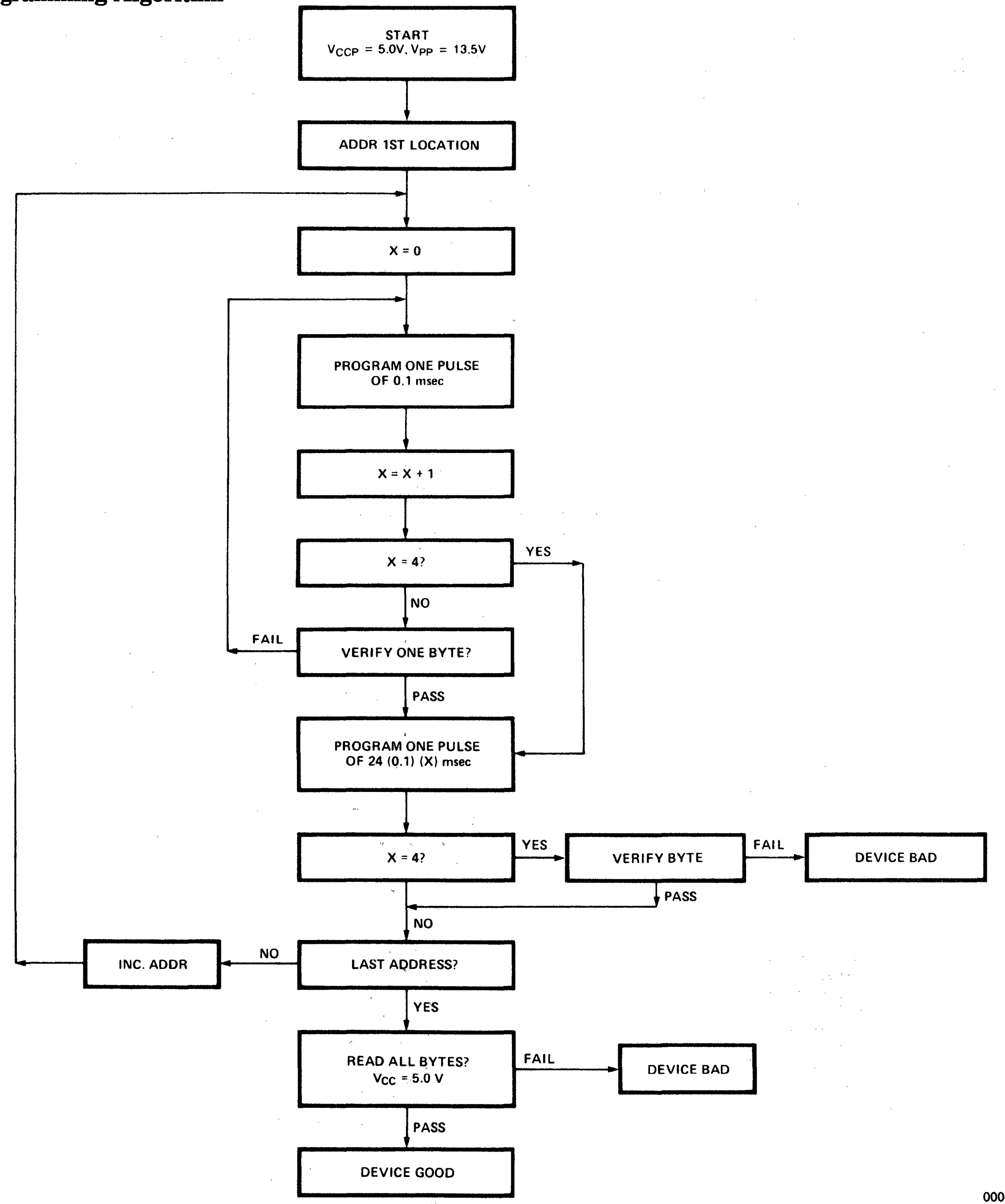
0008-8


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
D0 9
D1 10
D2 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 VPP (CS1)
19 VFY (CS2)
18 PGM (CS3)
17 D7
16 D6
15 D5
14 D4
13 D3

0008-9

Figure 3. Programming Pinout

Programming Algorithm


START
V_{CCP} = 5.0V, V_{PP} = 13.5V
ADDR 1ST LOCATION
X = 0
PROGRAM ONE PULSE OF 0.1 msec
X = X + 1
X = 4?
YES
NO
FAIL
VERIFY ONE BYTE?
PASS
PROGRAM ONE PULSE OF 24 (0.1) (X) msec
X = 4?
YES
VERIFY BYTE
FAIL
DEVICE BAD
PASS
NO
INC. ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? V_{CC} = 5.0 V
FAIL
DEVICE BAD
PASS
DEVICE GOOD

0008-10

The CY7C291 and CY7C292 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C291 and 7C292 2K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C291. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30-35 minutes.

The 7C291 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In each of these modes, the locations 0 thru 2047 should be addressed and read. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function			Outputs (9–11, 13–17)
	Read or Output Disable	CS_3	CS_2	$\overline{CS}_1$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	
	Pin Number	(18)	(19)	(20)	
Read		V_{IH}	V_{IH}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	High Z
Output Disable[4]		X	V_{IL}	X	High Z
Output Disable[4]		V_{IL}	X	X	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	Zeros

Notes:

[4] X = Don't care but not to exceed V_{CC} + 5%.

[5] During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

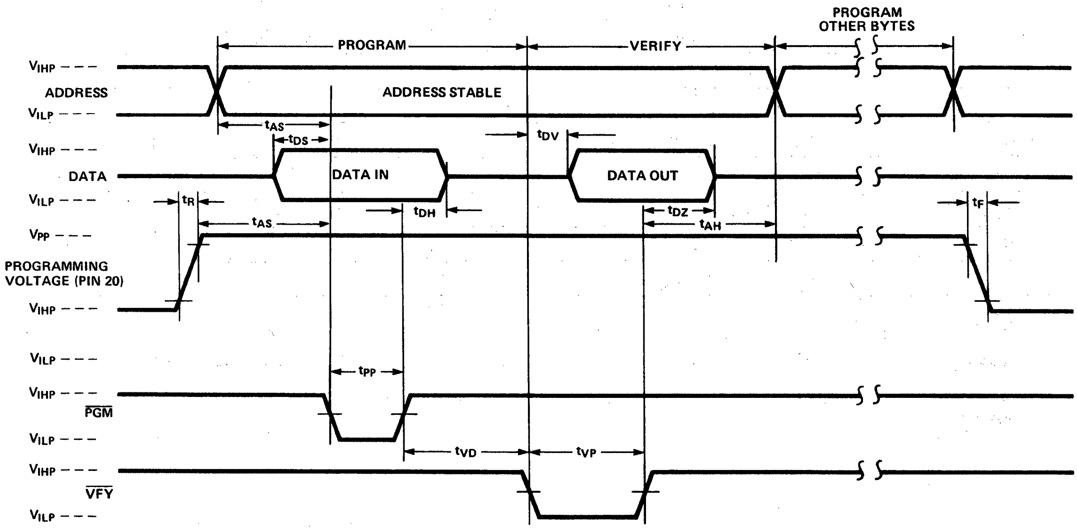

PROGRAM
VERIFY
PROGRAM OTHER BYTES
V_{IHP}
ADDRESS
V_{ILP}
ADDRESS STABLE
t_{AS}
t_{DS}
t_{DV}
V_{IHP}
DATA
V_{ILP}
DATA IN
DATA OUT
t_R
t_{DH}
t_{DZ}
t_{AS}
t_{AH}
t_F
V_{PP}
PROGRAMMING VOLTAGE (PIN 20)
V_{IHP}
V_{ILP}
t_{PP}
V_{IHP}
$\overline{PGM}$
V_{ILP}
t_{VD}
t_{VP}
V_{IHP}
$\overline{VFY}$
V_{ILP}
0008–11

Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	ICC (mA)	Ordering Code	Package Type	Operating Range
35	60	CY7C291L-35PC	P13	Commercial
		CY7C291L-35WC	W14	
	90	CY7C291-35PC	P13	
		CY7C291-35SC	S13	
		CY7C291-35WC	W14	
		CY7C291-35LC	L64	
	120	CY7C291-35WMB	W14	Military
50	60	CY7C291L-50PC	P13	Commercial
		CY7C291L-50WC	W14	
	90	CY7C291-50PC	P13	
		CY7C291-50SC	S13	
		CY7C291-50WC	W14	
		CY7C291-50LC	L64	
	120	CY7C291-50WMB	W14	Military
		CY7C291-50DMB	D14	
		CY7C291-50LMB	L64	
		CY7C291-50QMB	Q64	

Speed (ns)	ICC (mA)	Ordering Code	Package Type	Operating Range
35	60	CY7C292L-35PC	P11	Commercial
		CY7C292L-35DC	D12	
	90	CY7C292-35PC	P11	
		CY7C292-35DC	D12	
50	60	CY7C292L-50PC	P11	Commercial
		CY7C292L-50DC	D12	
	90	CY7C292-50PC	P11	
		CY7C292-50DC	D12	
	120	CY7C292-50DMB	D12	Military

PROM Programming Information

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970's and continue to provide the highest speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a Programming System. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance are easily identified. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the early 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point-of-view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of devices that program every time, and will perform as specified when programmed. In addition when these devices are supplied in a windowed package they can be programmed and erased indefinitely providing the designer a RE-PROGRAMMABLE PROM for development.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor, biasing it off.

Differential Memory Cells

In the 4K (CY7C225); 8K (CY7C235, CY7C281, CY7C282); and 16K (CY7C245, CY7C291, CY7C292) CMOS PROMs, Cypress employs a differential memory cell and sense amplifier technique. Higher density devices such as the 7C261, 7C263, 7C264 or 7C269 64K PROMs employ a single ended Cell and sense amplifier technique similar to the approach used in more conventional EPROMs.

In a conventional high density EPROM a single EPROM transistor is used to switch the input to one side of a differential sense amplifier. The other side of the sense amplifier is biased at an intermediate level with a dummy cell. An unprogrammed EPROM transistor will conduct and drive the sense amplifier to a logic "0". A programmed EPROM transistor will not conduct, and consequently drives the sense amplifier to a logic "1". A conventional EPROM cell therefore is delivered with a specific state "0" or "1" in it depending on the number of inversions after the sense amplifier and can always be programmed to the opposite state. Access time in this conventional approach is heavily dependent on the time the selected EPROM transistor takes to move the input of the sense amplifier from a quiescent condition to the threshold that the dummy cell is biasing the second input to the sense amplifier. This bias is several volts, and requires a significant delay before the sense amplifier begins to react.

Cypress PROMs employ a true differential cell approach, with EPROM cells attached to both inputs of the sense amplifier. As indicated above, the read transistor which is optimized for speed is actually the transistor attached to the sense amplifier. In the erased state, both EPROM transistors conduct when selected eccentrically biasing the input of the sense amplifier at the same level. If the inputs were at identical levels, the output of the sense amplifier would be in a mestastable condition or, neither a "1" nor "0". In actual practice the natural bias and high gain of the sense amplifier combine to cause the output to favor one or the other stable conditions. The difference between the two conditions is however only a few millivolts and the memory cell should be considered to contain neither a "1" nor a "0". As a result of this design approach, the memory cell must be programmed to either a "1" or a "0" depending on the desired condition and the conventional BLANK

CHECK mechanism is invalid. The benefit of the approach however is that only a small differential signal from the cell begins the sense amplifier switching and the access time of the memory is extremely fast.

Single Ended Memory Cells

Although a more conventional approach, single ended memory cells and sensing techniques offer a superior tradeoff between die size and performance than the differential cell for devices of 64K densities and above. The Single ended technique employed by Cypress uses a dummy cell for the reference voltage thus providing a reference that tracks the programmed cell in process related parameters, power supply and temperature induced variations. The Memory cell used is a second generation two transistor cell derived from earlier work at the 16K density level. It has an optimized READ transistor that is matched to the sense amplifier, and a second transistor optimized for programming. The floating gates of the two transistors that make up a memory cell are connected electrically so that the charge programmed onto one device controls the threshold of the second transistor.

Unlike the differential memory approach, the erased single ended device contains all "0"s and on the the ones are programmed. Therefore a "1" on the data pins during programming causes a "1" to be programmed into the addressed location.

Programming Algorithm

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data out pins during the programming operation and the data is read from these same pins for verification that the byte has been programmed.

Blank Check for Differential Cells

Since a differential cell contains neither a "1" nor a "0" before it is programmed, the conventional BLANK CHECK is not valid. For this reason, all Cypress CMOS PROMs contain a special BLANK CHECK mode of operation. Blank check is performed by separately examining the "0" and "1" sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes one comparing the "0" side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier and then repeating this operation for the "1"s side of the cell. The modes are called BLANK CHECK ONES, and BLANK CHECK ZEROS. These modes are entered by the application of a supervoltage to the device.

Blank Check for Single Ended Cells

Single ended cells BLANK CHECK in a conventional manner. An erased device contains all "0"s and a programmed call will contain a "1". Cypress PROMs that use the single ended approach provide a specific mode to perform the BLANK CHECK which also provides the verify function. This makes the need to switch high voltages unnecessary during the program verify operation. See specific data sheets for details.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ and a WRITE pin in the programming mode. These are active low signals and cause the data on the output pins to be written into the addressed memory location in the case of the WRITE signal or read out of the device in the case of the READ signal. When both the READ and WRITE signals are high, the outputs are disabled and in a high impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the WRITE signal. Verification of data is accomplished by reading the information on the output pins while the READ signal is active.

The timing for actual programming is supplied in the unique programming specification for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable INITIAL BYTE and Programmable SYNCHRONOUS/ASYNCHRONOUS ENABLE available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner, using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

Programming Support

Programming support for Cypress CMOS PROMs is available from a number of programmer manufacturers, some of which are listed below.

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA
98073-9746
(206) 881-6444

Data I/O 29B Unipak II

Cypress Part Number	Generic Part Number	Family Code and Pinout		Revision
CY7C225	27S25	F0	B6	V12
CY7C235	27S35	F0	B5	V09
CY7C245	27S45A	F0	B0	V09
CY7C261/3/4	27S49	EF	31	V11
CY7C281/2	27S281/181	EE	B4	V09
CY7C291/2	27S291/191	EE	AF	V09

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

Stag PPZ Zm2000

Cypress Part Number	Generic Part Number	Family Code and Pinout	Revision
CY7C225	27S25	Menu Driven	Rev 21
CY7C235	27S35		Rev 21
CY7C245	27S45A		Rev 24
CY7C281/2	27S281/181		Rev 21
CY7C291/2	27S291/191		Rev 21

Cypress Semiconductor, Inc.
3901 North First St.
San Jose, CA 95134
(408) 943-2600

Cypress CY3000 QuickPro Rev. PROM 2.10

Cypress Part Number	Generic Part Number	Family Code and Pinout
CY7C225	Menu Driven	Menu Driven
CY7C235		
CY7C245		
CY7C261/3/4		
CY7C268		
CY7C269		
CY7C281/2		
CY7C291/2		

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CY7C330	Synchronous State Machine	4-54
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CY7C332	Combinatorial Registered Reprogrammable PLD	4-58

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Introduction to CMOS PLDs

Cypress PLD Family Features

Cypress Semiconductor's PLD family offers the user the next generation in Programmable Logic Devices (PLD) that are based on our high performance 1.2μ CMOS process. These devices offer the user the power saving of a CMOS-based process, with delay times equivalent to those previously found only in bipolar devices. No fuses are used in Cypress' PLD family, rather all devices are based on an EPROM cell to facilitate programming. By using an EPROM cell instead of fuses, programming yields of 100% can be expected since all devices are functionally tested and erased prior to packaging. Therefore, no programming yield loss can be expected by the user.

The EPROM cell used by Cypress serves the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or Product Terms are connected via the EPROM cells to both the true and complement inputs. When the EPROM cell is programmed, the inputs from a gate or Product Term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or Product Terms. This is similar to "blowing" the fuses of a bipolar device which disconnects the input gate from the Product Term. Selective programming of each of these EPROM cells enables the specific logic function to be implemented by the user.

The programmability of Cypress' PLDs allows the user to customize every device in a number of ways to implement their unique logic requirements. Using PLDs in place of SSI or MSI components results in more effective utilization of boardspace, reduced cost and increased reliability. The flexibility afforded by these PLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The PLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output and product terms to the desired application.

PLD Notation

To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In *Figure 1*, an "x" represents an unprogrammed EPROM cell that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in *Figure 2* which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in *Figure 3*.

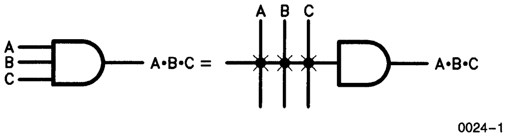


Figure 1

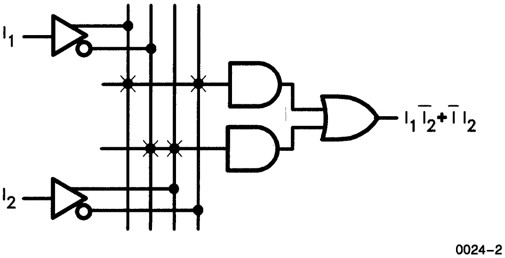


Figure 2

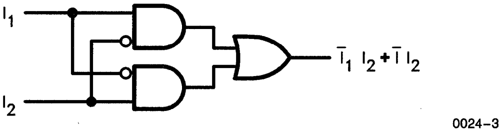


Figure 3

PLD Circuit Configurations

Cypress PLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows the designer to select a PLD that best fits the needs of their application. An example of some of the configurations that are available are listed below.

Programmable I/O

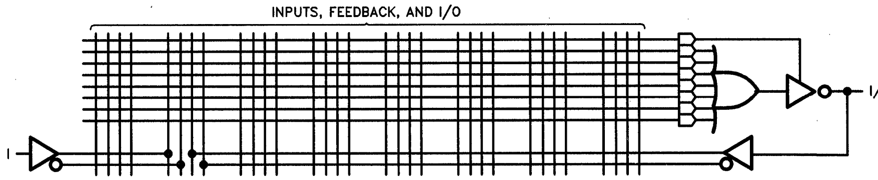
The programmable I/O offered in the Cypress PLD family allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, the I/O pin can be used as an input to the array when the three-state output is disabled.

Registered Outputs with Feedback

The registered output offered on a number of the Cypress PLDs allows this circuit to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift and branch.

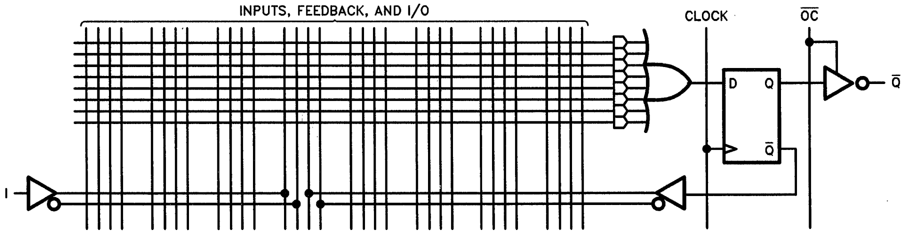
Programmable Macro Cell

The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.



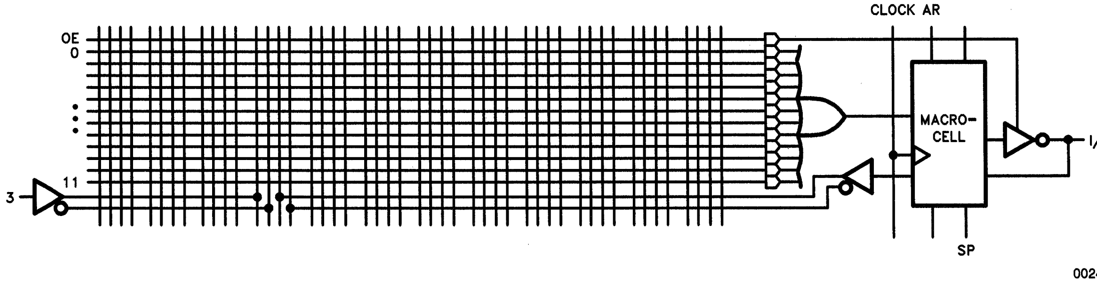
0024-4

Programmable I/O



0024-5

Registered Outputs with Feedback



0024-6

Programmable Macro Cell

CYPRESS
SEMICONDUCTOR

PAL® C 20 Series

Reprogrammable CMOS
PAL® C 16L8, 16R8, 16R6, 16R4

Features

- **CMOS EPROM technology for reprogrammability**
- **High performance at quarter power**
  - **— t_{PD} = 25 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 45 mA**
- **High performance at military temperature**
  - **— t_{PD} = 20 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 70 mA**
- **Commercial and military temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >2000V input protection from electrostatic discharge**
  - **— 100% AC/DC tested**
  - **— 10% power supply tolerances**
  - **— High noise immunity**
  - **— Security feature prevents pattern duplication**
  - **— 100% programming and functional testing**

Functional Description

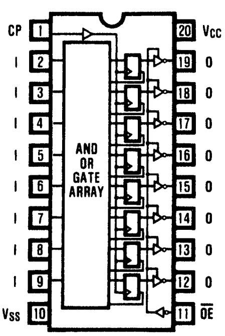
Cypress PAL C Series 20 devices are high speed electrically programmable and UV erasable logic devices produced in a proprietary "N" well CMOS EPROM process. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions serving unique requirements.

PALs are offered in 20-pin plastic, ceramic, and LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

Before programming, AND gates or PRODUCT TERMS are connected via EPROM cells to both TRUE and COMPLEMENT inputs. Programming an EPROM cell disconnects an INPUT TERM from a PRODUCT TERM. Selective programming

Logic Symbols and DIP, LCC and PLCC Pinouts

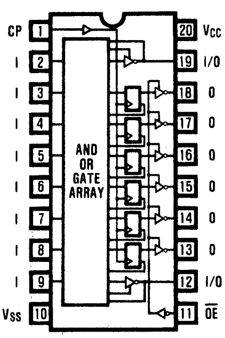
16R8



CP 1
I 2
I 3
I 4
I 5
I 6
I 7
I 8
I 9
Vss 10
20 Vcc
19 O
18 O
17 O
16 O
15 O
14 O
13 O
12 O
11 OE
AND OR GATE ARRAY

0038-1

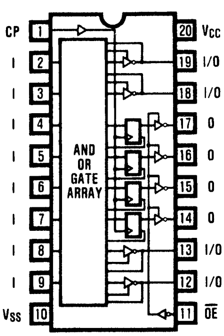
16R6



CP 1
I 2
I 3
I 4
I 5
I 6
I 7
I 8
I 9
Vss 10
20 Vcc
19 I/O
18 O
17 O
16 O
15 O
14 O
13 O
12 I/O
11 OE
AND OR GATE ARRAY

0038-2

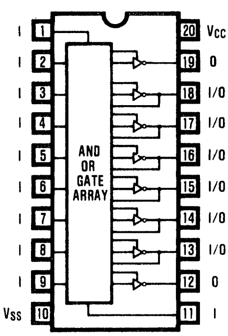
16R4



CP 1
I 2
I 3
I 4
I 5
I 6
I 7
I 8
I 9
Vss 10
20 Vcc
19 I/O
18 I/O
17 O
16 O
15 O
14 O
13 I/O
12 I/O
11 OE
AND OR GATE ARRAY

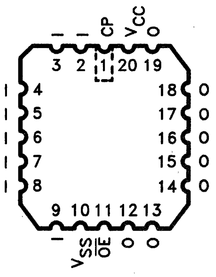
0038-3

16L8



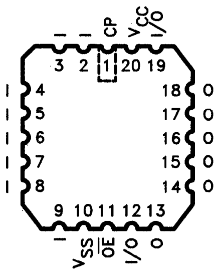
I 1
I 2
I 3
I 4
I 5
I 6
I 7
I 8
I 9
Vss 10
20 Vcc
19 O
18 I/O
17 I/O
16 I/O
15 I/O
14 I/O
13 I/O
12 O
11 I
AND OR GATE ARRAY

0038-4



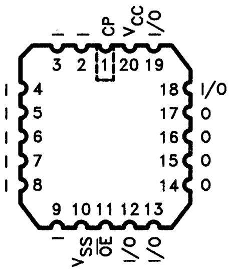
I I CP Vcc O
3 2 1 20 19
I 4
I 5
I 6
I 7
I 8
18 O
17 O
16 O
15 O
14 O
9 10 11 12 13
I Vss OE O O

0038-5



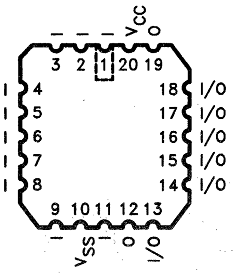
I I CP Vcc I/O
3 2 1 20 19
I 4
I 5
I 6
I 7
I 8
18 O
17 O
16 O
15 O
14 O
9 10 11 12 13
I Vss OE I/O O

0038-6



I I CP Vcc I/O
3 2 1 20 19
I 4
I 5
I 6
I 7
I 8
18 I/O
17 O
16 O
15 O
14 O
9 10 11 12 13
I Vss OE I/O I/O

0038-7



I I I Vcc O
3 2 1 20 19
I 4
I 5
I 6
I 7
I 8
18 I/O
17 I/O
16 I/O
15 I/O
14 I/O
9 10 11 12 13
I Vss I O I/O

0038-8

PAL® is a registered trademark of Monolithic Memories Inc.
CYPRESS SEMICONDUCTOR is a trademark of Cypress Semiconductor Corporation.

Functional Description (Continued)

of these cells allows a specific logic function to be implemented in a PAL C device. PAL C devices are supplied in four functional configurations, designated 16R8, 16R6, 16R4 and 16L8. These eight devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the four functional variations of the product family. All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the $\overline{Q}$ bar side of the register fed back into the main array.

All PAL C devices feature a SECURITY function which provides the user protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope. The PAL C device also contains a PHANTOM ARRAY used for functional and performance testing. The content of this array is always accessible, even when security is invoked.

Cypress PAL C products are produced in an advanced 1.2 micron "N" well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. The PHANTOM ARRAY and PHANTOM operating mode allow the device to be tested for functionality and performance after it has been packaged. Combining these inherent and designed-in features, an extremely high degree of functionality, programmability and assured AC performance are provided and testing becomes an easy task.

The REGISTER PRELOAD allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

The PHANTOM MODE of operation provides a completely separate operating mode where the functionality of the device along with its AC performance may be ascertained. The user need not be encumbered by programmed cells in the normal operating mode. This PHANTOM MODE of operation allows additional input lines to be programmed to operate the PAL C device, exercising the device functionally and allowing AC performance measurements to be made. The PHANTOM MODE of operation acknowledges only the INPUT TERMS shown shaded in the functional block diagrams. Likewise, the normal PHANTOM INPUT TERMS do not exist in the normal mode of operation. During the final stages of manufacturing, some cells in the PHANTOM ARRAY are programmed for final AC and functional testing. These cells remain programmed, and may be used at incoming inspection to verify both functional and AC performance.

Commercial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
				L	STD	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)	t_{PD} (ns)			t_S (ns)			t_{CO} (ns)		
					-20	-30	-40	-20	-30	-40	-20	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	30	40	—	—	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	—	—	20	25	35	15	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional										
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional										

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10)	−0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	−0.5V to +7.0V
DC Input Voltage	−3.0V to +7.0V
Output Current into Outputs (Low)	24 mA
DC Programming Voltage	14.0V
UV Exposure	7258 Wsec/cm^2
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2001V
Latchup Current	>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logic HIGH[2] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[2] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$[1]			−10	10	μA
V_{PP}	Programming Voltage	I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA[6]	"L"			45	mA
			STD			70	mA
			MIL			70	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{IN} \leq V_{CC}$			−100	100	μA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	7	

Switching Characteristics PAL C 20 Series Over Operating Range [4]

Parameters	Description	Commercial				Military						Units
		-25		-35		-20		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		15		25		15		20		25	ns
t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	20		30		20		25		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		0		0		0		ns
t_P	Clock Period	35		55		35		45		60		ns
t_W	Clock Width	15		20		12		20		25		ns
f_{MAX}	Maximum Frequency		28.5		18		28.5		22		16.5	MHz

Notes:

1. I_{IX} (Pin 1) = 25 μA Max., $V_{SS} \leq V_{IN} \leq 2.7V$. I_{IX} (Pin 1) = 1 mA Max., $2.7V \leq V_{IN} \leq V_{CC}$.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.
5. *Figure 1a* test load used for all parameters except t_{EA}, t_{ER} t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
6. $I_{CC(AC)}$ = (0.6 mA/MHz) × (Operating Frequency in MHz) + $I_{CC(DC)}$. $I_{CC(DC)}$ is measured with an unprogrammed device.

AC Test Loads and Waveforms

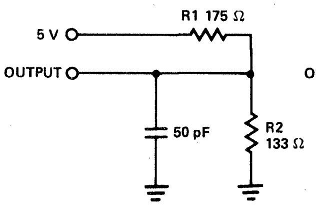

R1 175 Ω
5 V
OUTPUT
50 pF
R2
133 Ω

Figure 1a. Commercial

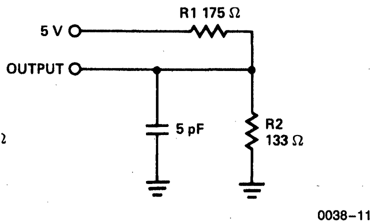
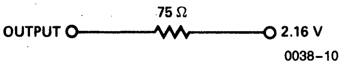

R1 175 Ω
5 V
OUTPUT
5 pF
R2
133 Ω
0038–11

Figure 1b. Commercial

Equivalent to:
THÉVENIN EQUIVALENT COMMERICAL


75 Ω
OUTPUT
2.16 V
0038–10

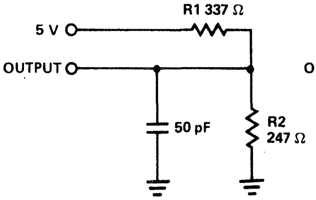

R1 337 Ω
5 V
OUTPUT
50 pF
R2
247 Ω

Figure 1c. Military

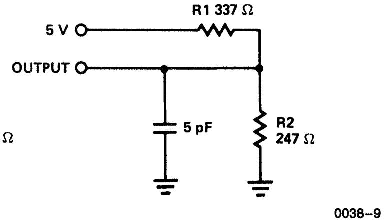
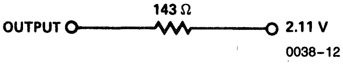

R1 337 Ω
5 V
OUTPUT
5 pF
R2
247 Ω
0038–9

Figure 1d. Military

Equivalent to:
THÉVENIN EQUIVALENT MILITARY


143 Ω
OUTPUT
2.11 V
0038–12

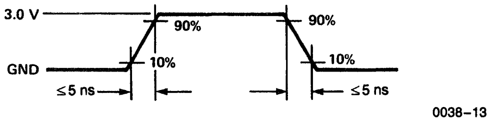

3.0 V
GND
90%
10%
90%
10%
≤5 ns
≤5 ns
0038–13

Figure 2

Switching Waveforms

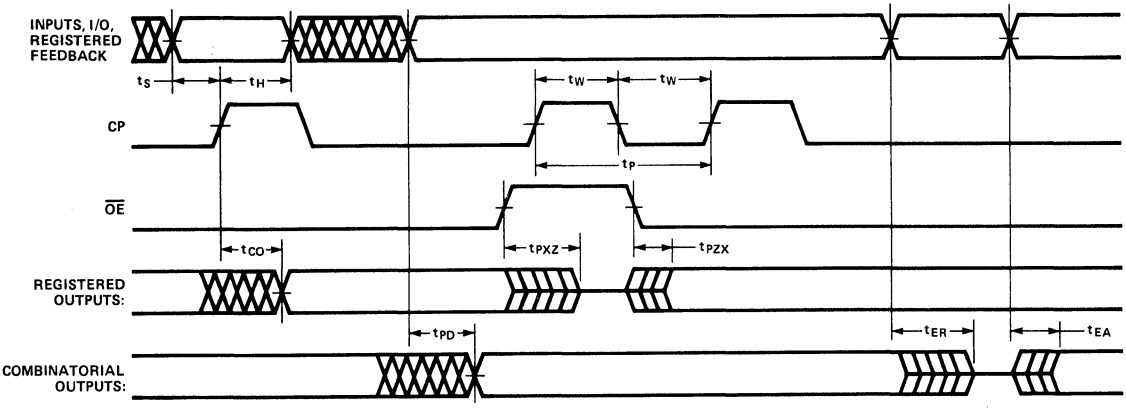


Figure 3

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PALs. For this reason, an opaque label should be placed over the window if the PAL is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 30–35 minutes. The window needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PAL is exposed to high intensity UV light for an extended period of time. 7258W sec/cm^2 is the recommended maximum dosage.

Programming

PAL C devices are programmed a BYTE at a time using a voltage to transfer electrons to a floating gate. The array programmed is addressed as memory of 256 bytes, using address Tables 4 and 5. These addresses are supplied to the device over Pins 2 through 9. The data to be programmed is supplied on data inputs D0 through D7 (Pins 19 through 12 inclusive). In the unprogrammed state, all inputs are connected to product terms. A "1" on a data line causes a cell to be programmed, disconnecting an INPUT TERM from a PRODUCT TERM. During verify, an unprogrammed cell causes a "1" to appear on the output, while a programmed cell will appear as a "0". Table 3 describes the operating modes of the device and the programming waveforms are described in *Figures* 6 through 9. The actual sequence required to program a cell is described in *Figure* 5 and applies for programming either standard or phantom portions of the array. The security bit should be programmed using a single 10 ms pulse, and verified per *Figure 9*.

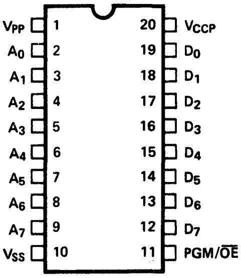


Figure 4. Programming Pin Configuration

DC Programming Parameters Ambient Temperature = 25°C

Table 1

Parameter	Description	Min.	Max.	Units	Notes
V_{PP}	Programming Voltage	13.0	14.0	V	
V_{CCP}	Supply Voltage During Programming	4.75	5.25	V	
V_{IHP}	Programming Input High Voltage	3.0		V	
V_{ILP}	Programming Input Low Voltage		0.4	V	
V_{OH}	Output High Voltage	2.4		V	1
V_{OL}	Output Low Voltage		0.4	V	1
I_{PP}	Programming Supply Current		50	mA	

AC Programming Parameters Ambient Temperature = 25°C

Table 2

Parameter	Description	Min.	Max.	Units	Notes
t_{PP}	Programming Pulse Width	100	10,000	µs	2
t_S	Setup Time	1.0		µs	
t_H	Hold Time	1.0		µs	
t_r, t_f	V_{PP} Rise and Fall Time	1.0		µs	2
t_{VD}	Delay to Verify	1.0		µs	
t_{VP}	Verify Pulse Width	2.0		µs	
t_{DV}	Verify to Data Valid	20.0		µs	
t_{DZ}	Verify to High Z		1.0	µs	

Table 3

Pin Name	V_{PP}	PGM/$\overline{OE}$	A1	A2	A3	A4	A5	D7–D0	
Pin Number	**(1)**	**(11)**	**(3)**	**(4)**	**(5)**	**(6)**	**(7)**	**(12–19)**	**Notes**
Operating Modes									
PAL	X	X	X	X	X	X	X	Programmed Function	3, 4
Program PAL	V_{PP}	V_{PP}	X	X	X	X	X	Data In	3, 5
Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	X	High Z	3, 5
Program Verify/Blank Check	V_{PP}	V_{ILP}	X	X	X	X	X	Data Out	3, 5, 11
Phantom PAL	X	X	X	X	X	V_{PP}	X	Programmed Function	3, 6
Program Phantom PAL	V_{PP}	V_{PP}	X	X	X	X	V_{PP}	Data In	3, 7
Phantom Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	V_{PP}	High Z	3, 7
Phantom Program Verify	V_{PP}	V_{ILP}	X	X	X	X	V_{PP}	Data Out	3, 7
Program Security Bit	V_{PP}	V_{PP}	V_{PP}	X	X	X	X	High Z	3, 8
Verify Security Bit	X	X	Note 9	V_{PP}	X	X	X	High Z	3
Register Preload	X	X	X	X	V_{PP}	X	X	Data In	3, 10

Notes:

1. During verify operation
2. Measured at 10% and 90% points
3. $V_{SS} < X < V_{CCP}$
4. All "X" inputs operational per normal PAL function.
5. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 4 and 5.
6. All "X" inputs operational per normal PAL function except that they operate on the function that occupies the phantom array.
7. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 4 and 5. Pin 7 is used to select the phantom mode of operation and must be taken to V_{PP} before selecting phantom program operation with V_{PP} on Pin 1.
8. See *Figure 8* for security programming sequence.
9. The state of Pin 3 indicates if the security function has been invoked or not. If Pin 3 = V_{OL} security is in effect, if Pin 3 = V_{OH}, the data is unsecured and may be directly accessed.
10. For testing purposes, the output latch on the 16R8, 16R6 and 16R4 may be preloaded with data from the appropriate associated output line.
11. It is necessary to toggle Pin 11 ($\overline{OE}$) HIGH during all address transitions while in the Program Verify or Blank Check mode.

The programmable array is addressed as a basic 256 by 8 memory structure with a duplication of the phantom array located at the same addresses as columns 0, 1, 2 and 3. The ability to address the phantom array as differentiated from the first 4 columns of the normal array is accomplished by taking Pin 7 to V_{PP} and entering the phantom mode of operation as shown in Tables 3 and 5. In either case, phantom or normal, product terms are addressed in groups of 8 per Table 4. Notice that this is accomplished by modulo 8 selecting every eighth product term starting with 0, 8, 16, 24, 32, 40, 48 and 56 corresponding to PROGRAMMED DATA INPUT on D0 through D7 respectively and incrementing each product term by one until all 64 PRODUCT TERMS are addressed. Each of the INPUT TERMS is addressed 8 times corresponding to the 8 groups of individual product terms addressed before being incremented.

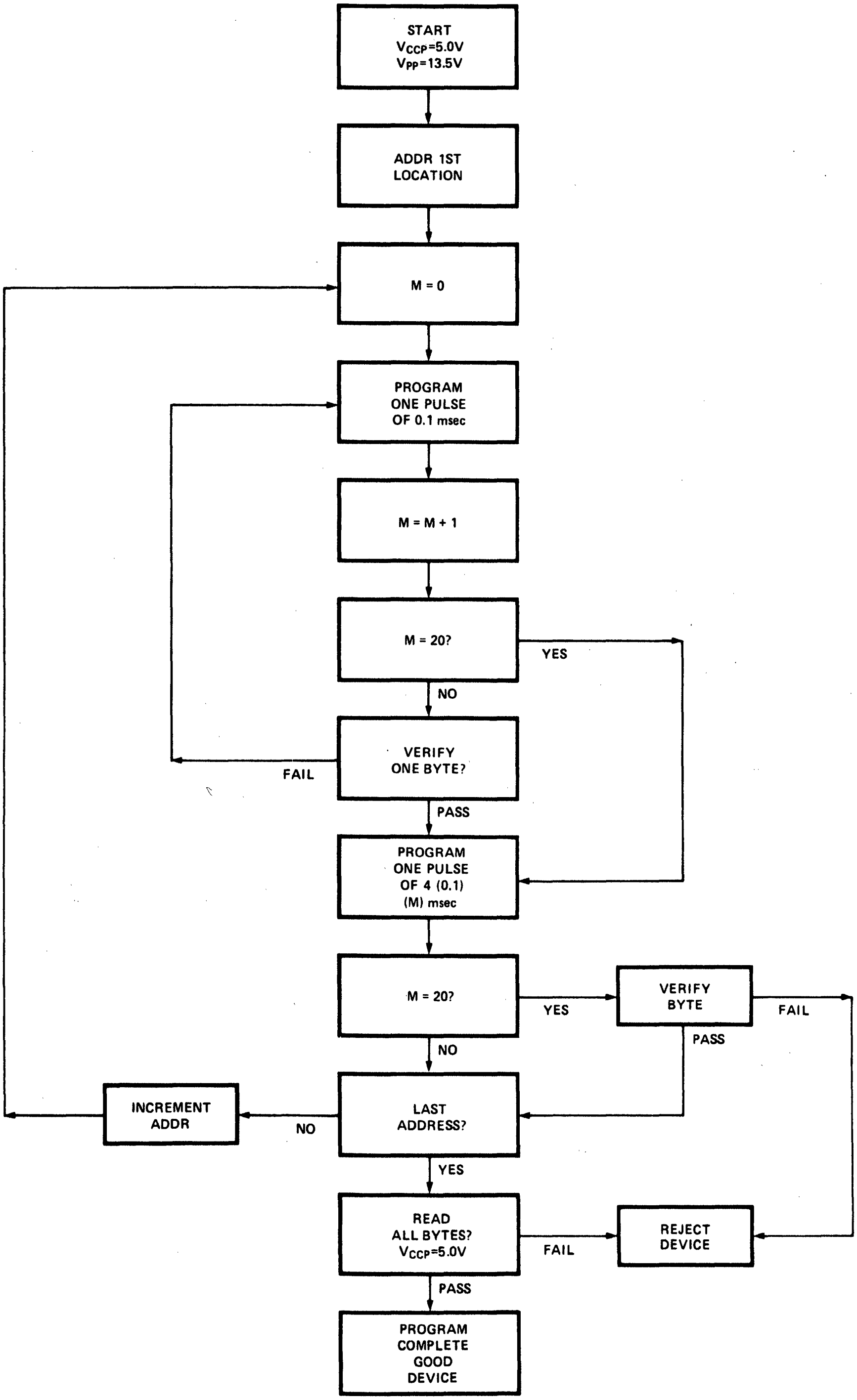
Table 4

Product Term Addresses										
Binary Addresses			Line Number							
Pin Numbers										
(4)	(3)	(2)								
V_{ILP}	V_{ILP}	V_{ILP}	0	8	16	24	32	40	48	56
V_{ILP}	V_{ILP}	V_{IHP}	1	9	17	25	33	41	49	57
V_{ILP}	V_{IHP}	V_{ILP}	2	10	18	26	34	42	50	58
V_{ILP}	V_{IHP}	V_{IHP}	3	11	19	27	35	43	51	59
V_{IHP}	V_{ILP}	V_{ILP}	4	12	20	28	36	44	52	60
V_{IHP}	V_{ILP}	V_{IHP}	5	13	21	29	37	45	53	61
V_{IHP}	V_{IHP}	V_{ILP}	6	14	22	30	38	46	54	62
V_{IHP}	V_{IHP}	V_{IHP}	7	15	23	31	39	47	55	63
			D0	D1	D2	D3	D4	D5	D6	D7
			Programmed Data Input							

Table 5

Input Term Addresses					
Input Term Numbers	Binary Addresses				
	Pin Numbers				
	(9)	(8)	(7)	(6)	(5)
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
2	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
3	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
5	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
6	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
8	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
9	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
11	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
12	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
15	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
16	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}

Input Term Addresses					
Input Term Numbers	Binary Addresses				
	Pin Numbers				
	(9)	(8)	(7)	(6)	(5)
18	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
20	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
22	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
24	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
25	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
26	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
28	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
29	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
30	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
P0	V_{ILP}	V_{ILP}	V_{PP}	X	X
P1	V_{ILP}	V_{IHP}	V_{PP}	X	X
P2	V_{IHP}	V_{ILP}	V_{PP}	X	X
P3	V_{IHP}	V_{IHP}	V_{PP}	X	X


START
V_{CCP}=5.0V
V_{PP}=13.5V
ADDR 1ST LOCATION
M = 0
PROGRAM ONE PULSE OF 0.1 msec
M = M + 1
M = 20?
YES
NO
VERIFY ONE BYTE?
FAIL
PASS
PROGRAM ONE PULSE OF 4 (0.1) (M) msec
M = 20?
YES
VERIFY BYTE
FAIL
PASS
NO
INCREMENT ADDR
NO
LAST ADDRESS?
YES
READ ALL BYTES? V_{CCP}=5.0V
FAIL
REJECT DEVICE
PASS
PROGRAM COMPLETE GOOD DEVICE

0038–16

Figure 5. Programming Flowchart

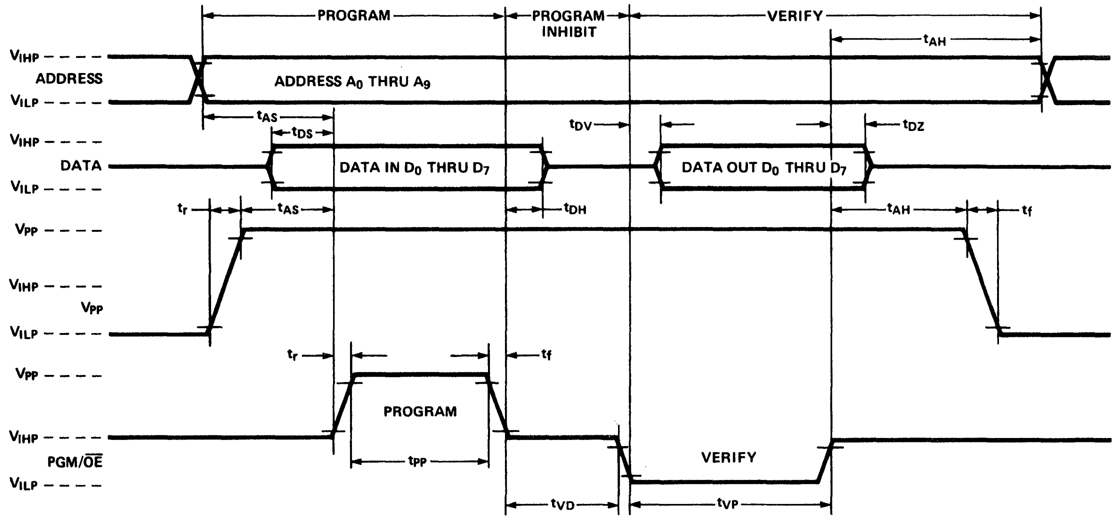

PROGRAM
PROGRAM INHIBIT
VERIFY
t_{AH}
V_{IHP}
ADDRESS
V_{ILP}
ADDRESS A_0 THRU A_9
t_{AS}
t_{DS}
t_{DV}
t_{DZ}
V_{IHP}
DATA
V_{ILP}
DATA IN D_0 THRU D_7
DATA OUT D_0 THRU D_7
t_r
t_{AS}
t_{DH}
t_{AH}
t_f
V_{PP}
V_{IHP}
V_{PP}
V_{ILP}
t_r
t_f
V_{PP}
PROGRAM
V_{IHP}
PGM/$\overline{OE}$
V_{ILP}
t_{PP}
VERIFY
t_{VD}
t_{VP}
0038-17

Figure 6. Programming Waveforms Normal Array

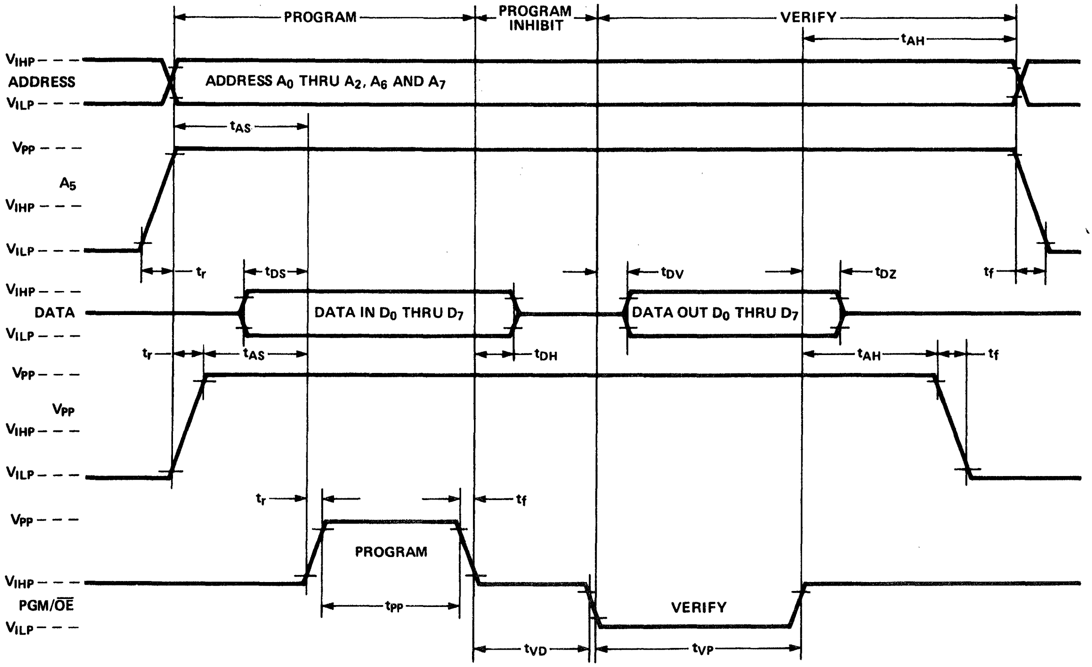
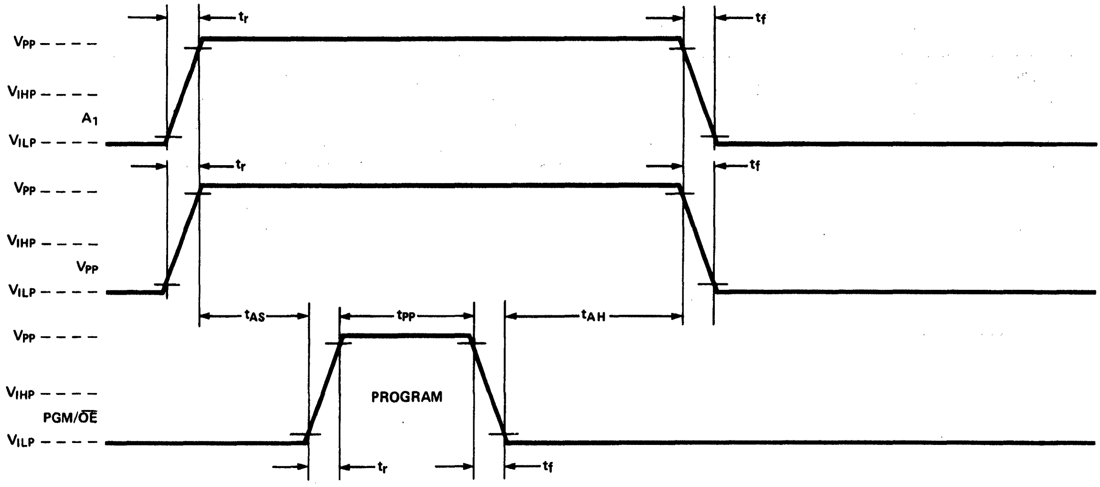
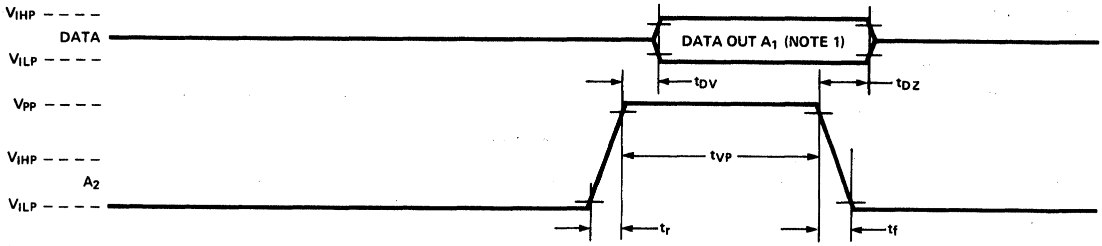

PROGRAM
PROGRAM INHIBIT
VERIFY
t_{AH}
V_{IHP}
ADDRESS
V_{ILP}
ADDRESS A_0 THRU A_2, A_6 AND A_7
t_{AS}
V_{PP}
A_5
V_{IHP}
V_{ILP}
t_r
t_{DS}
t_{DV}
t_{DZ}
t_f
V_{IHP}
DATA
V_{ILP}
DATA IN D_0 THRU D_7
DATA OUT D_0 THRU D_7
t_r
t_{AS}
t_{DH}
t_{AH}
t_f
V_{PP}
V_{PP}
V_{IHP}
V_{ILP}
t_r
t_f
V_{PP}
PROGRAM
V_{IHP}
PGM/$\overline{OE}$
V_{ILP}
t_{PP}
VERIFY
t_{VD}
t_{VP}
0038-18

Figure 7. Program Waveforms Phantom Array


VPP
VIHP
A1
VILP
tr
tf
VPP
VIHP
VPP
VILP
tr
tf
tAS
tPP
tAH
VPP
VIHP
PGM/OE
VILP
PROGRAM
tr
tf

0038-19

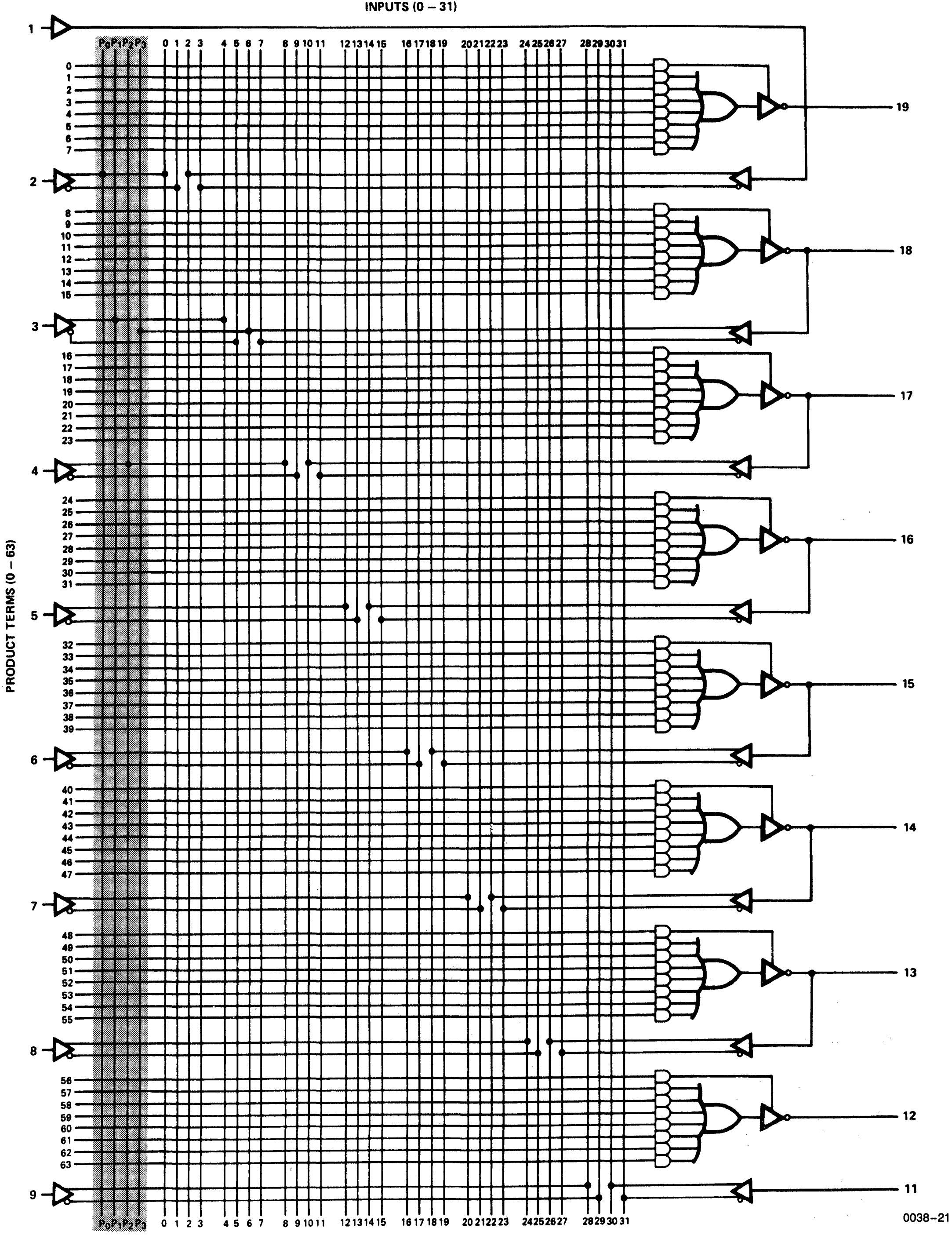
Figure 8. Activating Program Security


VIHP
DATA
VILP
DATA OUT A1 (NOTE 1)
tDV
tDZ
VPP
VIHP
A2
VILP
tVP
tr
tf

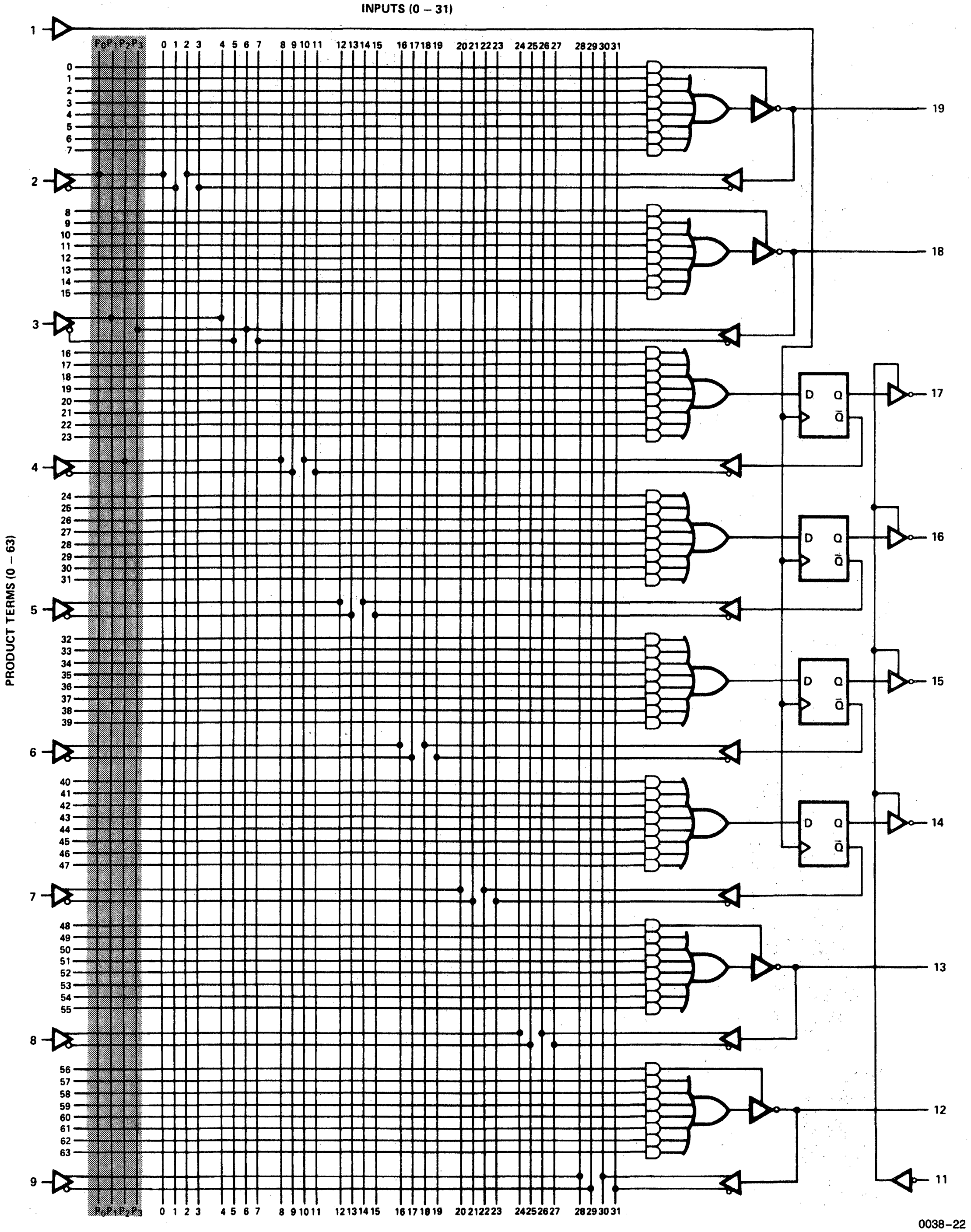
0038-20

Figure 9. Verify Program Security

Functional Logic Diagram PAL C 16L8


INPUTS (0 – 31)
PRODUCT TERMS (0 – 63)
P0 P1 P2 P3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
0038–21

Functional Logic Diagram PAL C 16R4


INPUTS (0 – 31)
P0 P1 P2 P3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
PRODUCT TERMS (0 – 63)
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
D Q
Q̄

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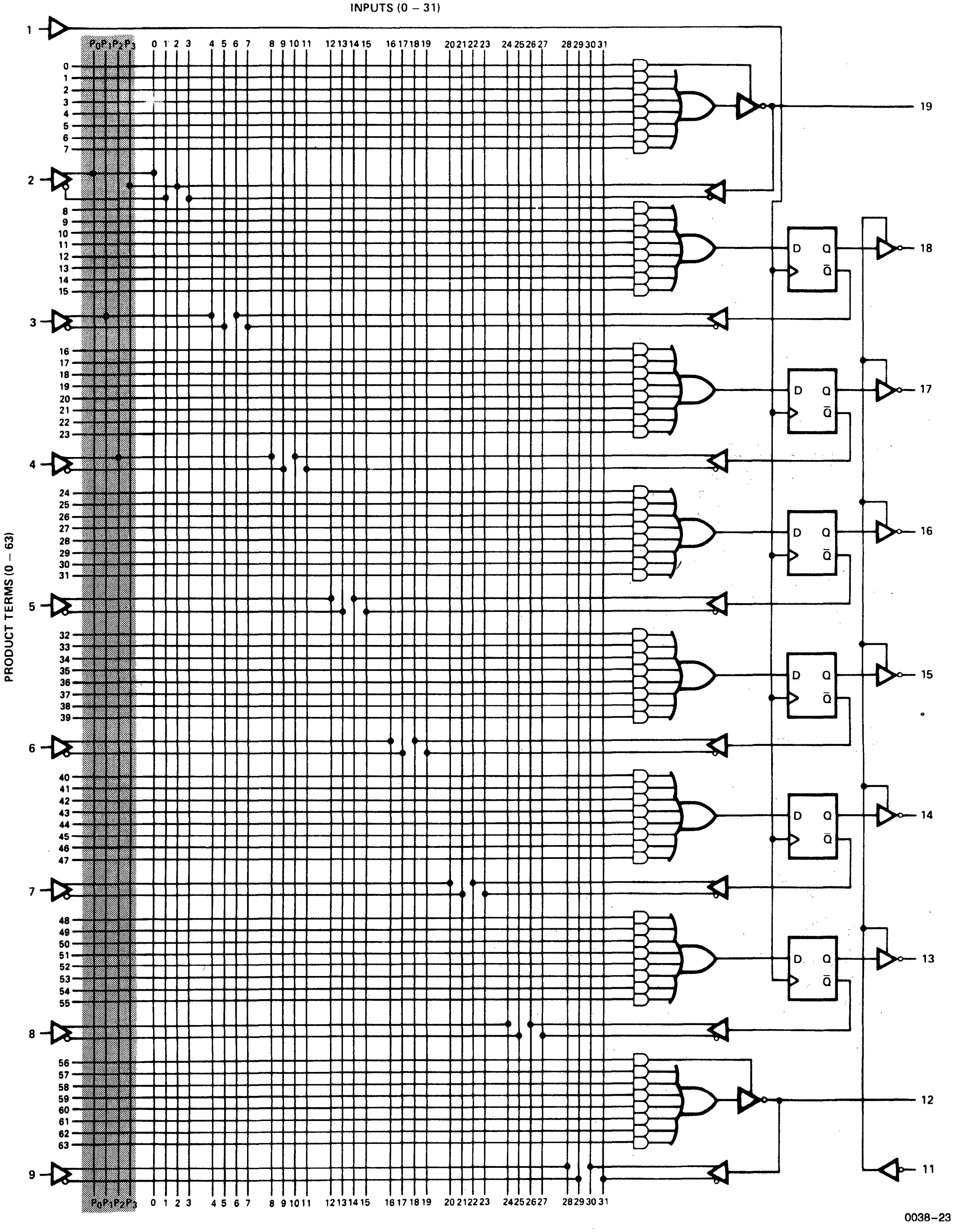
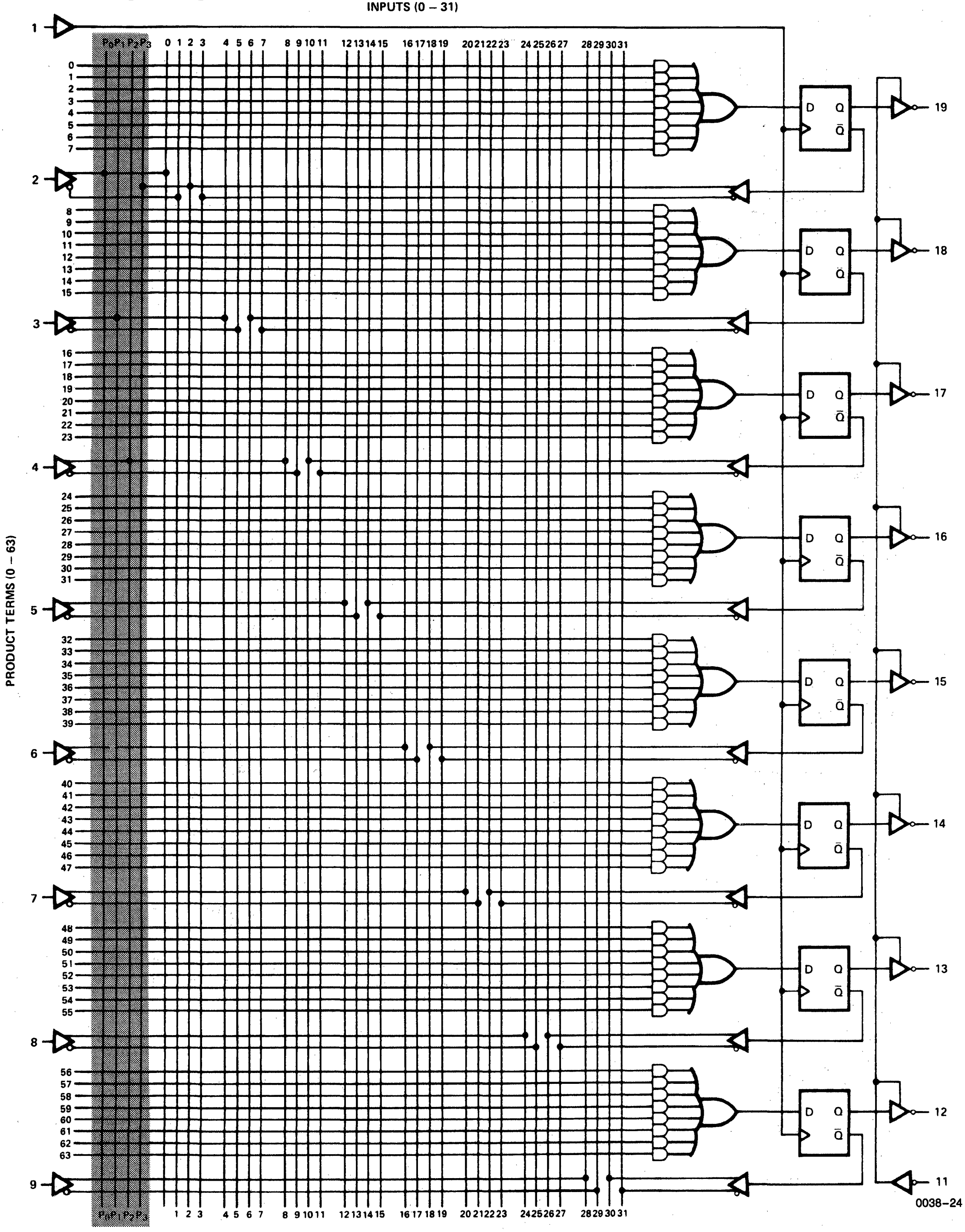
Functional Logic Diagram PAL C 16R6

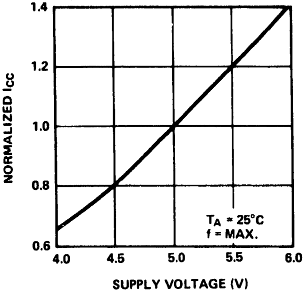

INPUTS (0 – 31)
PRODUCT TERMS (0 – 63)
P0 P1 P2 P3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
D
Q
Q̄
0038–23

Functional Logic Diagram PAL C 16R8

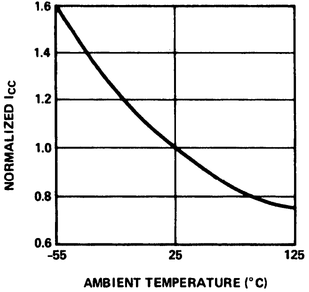

INPUTS (0 – 31)
PRODUCT TERMS (0 – 63)
P0 P1 P2 P3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
11
12
13
14
15
16
17
18
19
D
Q
Q̄
0038-24

Typical DC and AC Characteristics

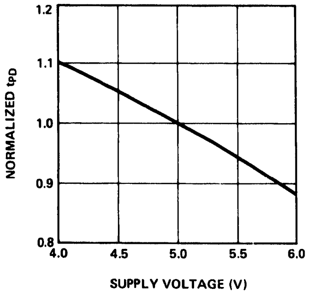
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



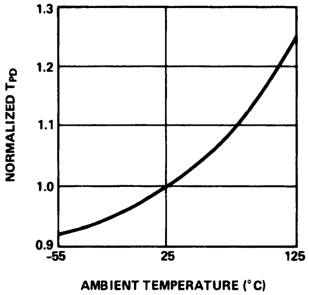
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



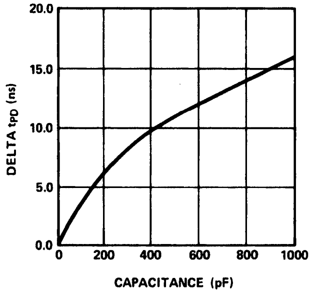
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



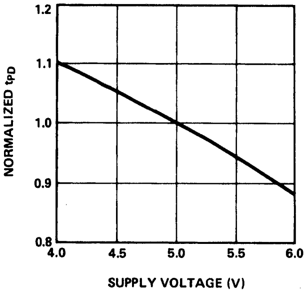
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



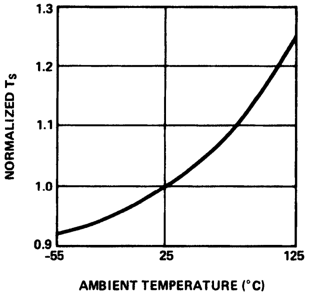
DELTA PROPAGATION TIME vs. OUTPUT LOADING



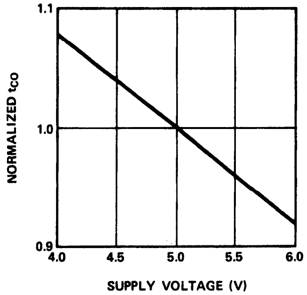
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



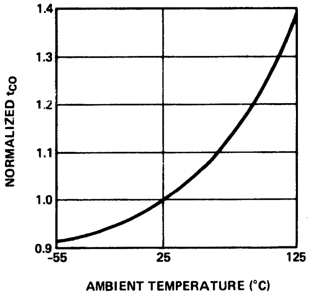
NORMALIZED SETUP TIME vs. TEMPERATURE



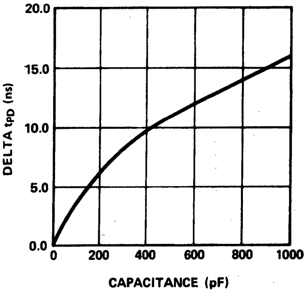
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



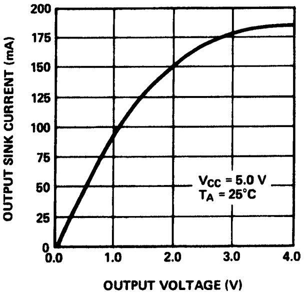
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



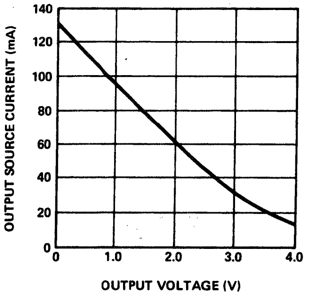
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
20	—	—	70	PAL C 16L8-20DMB	D6	Military
				PAL C 16L8-20LMB	L61	
				PAL C 16L8-20WMB	W6	
25	—	—	45	PAL C 16L8L-25PC	P5	Commercial
				PAL C 16L8L-25JC	J61	
				PAL C 16L8L-25LC	L61	
				PAL C 16L8L-25WC	W6	
			70	PAL C 16L8-25PC	P5	
				PAL C 16L8-25JC	J61	
				PAL C 16L8-25LC	L61	
				PAL C 16L8-25WC	W6	
30	—	—	70	PAL C 16L8-30DMB	D6	Military
				PAL C 16L8-30LMB	L61	
				PAL C 16L8-30WMB	W6	
35	—	—	45	PAL C 16L8L-35PC	P5	Commercial
				PAL C 16L8L-35JC	J61	
				PAL C 16L8L-35LC	L61	
				PAL C 16L8L-35WC	W6	
			70	PAL C 16L8-35PC	P5	
				PAL C 16L8-35JC	J61	
				PAL C 16L8-35LC	L61	
				PAL C 16L8-35WC	W6	
40	—	—	70	PAL C 16L8-40DMB	D6	Military
				PAL C 16L8-40LMB	L61	
				PAL C 16L8-40WMB	W6	
20	20	15	70	PAL C 16R4-20DMB	D6	Military
				PAL C 16R4-20LMB	L61	
				PAL C 16R4-20WMB	W6	
25	20	15	45	PAL C 16R4L-25PC	P5	Commercial
				PAL C 16R4L-25JC	J61	
				PAL C 16R4L-25LC	L61	
				PAL C 16R4L-25WC	W6	
			70	PAL C 16R4-25PC	P5	
				PAL C 16R4-25JC	J61	
				PAL C 16R4-25LC	L61	
				PAL C 16R4-25WC	W6	
30	25	20	70	PAL C 16R4-30DMB	D6	Military
				PAL C 16R4-30LMB	L61	
				PAL C 16R4-30WMB	W6	
35	30	25	45	PAL C 16R4L-35PC	P5	Commercial
				PAL C 16R4L-35JC	J61	
				PAL C 16R4L-35LC	L61	
				PAL C 16R4L-35WC	W6	
			70	PAL C 16R4-35PC	P5	
				PAL C 16R4-35JC	J61	
				PAL C 16R4-35LC	L61	
				PAL C 16R4-35WC	W6	
40	35	25	70	PAL C 16R4-40DMB	D6	Military
				PAL C 16R4-40LMB	L61	
				PAL C 16R4-40WMB	W6	

Ordering Information (Continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
20	20	15	70	PAL C 16R6-20DMB	D6	Military
				PAL C 16R6-20LMB	L61	
				PAL C 16R6-20WMB	W6	
25	20	15	45	PAL C 16R6L-25PC	P5	Commercial
				PAL C 16R6L-25JC	J61	
				PAL C 16R6L-25LC	L61	
				PAL C 16R6L-25WC	W6	
			70	PAL C 16R6-25PC	P5	
				PAL C 16R6-25JC	J61	
				PAL C 16R6-25LC	L61	
				PAL C 16R6-25WC	W6	
30	25	20	70	PAL C 16R6-30DMB	D6	Military
				PAL C 16R6-30LMB	L61	
				PAL C 16R6-30WMB	W6	
35	30	25	45	PAL C 16R6L-35PC	P5	Commercial
				PAL C 16R6L-35JC	J61	
				PAL C 16R6L-35LC	L61	
				PAL C 16R6L-35WC	W6	
			70	PAL C 16R6-35PC	P5	
				PAL C 16R6-35JC	J61	
				PAL C 16R6-35LC	L61	
				PAL C 16R6-35WC	W6	
40	35	25	70	PAL C 16R6-40DMB	D6	Military
				PAL C 16R6-40LMB	L61	
				PAL C 16R6-40WMB	W6	
—	20	15	70	PAL C 16R8-20DMB	D6	Military
				PAL C 16R8-20LMB	L61	
				PAL C 16R8-20WMB	W6	
—	20	15	45	PAL C 16R8L-25PC	P5	Commercial
				PAL C 16R8L-25JC	J61	
				PAL C 16R8L-25LC	L61	
				PAL C 16R8L-25WC	W6	
			70	PAL C 16R8-25PC	P5	
				PAL C 16R8-25JC	J61	
				PAL C 16R8-25LC	L61	
				PAL C 16R8-25WC	W6	
—	25	20	70	PAL C 16R8-30DMB	D6	Military
				PAL C 16R8-30LMB	L61	
				PAL C 16R8-30WMB	W6	
—	30	25	45	PAL C 16R8L-35PC	P5	Commercial
				PAL C 16R8L-35JC	J61	
				PAL C 16R8L-35LC	L61	
				PAL C 16R8L-35WC	W6	
			70	PAL C 16R8-35PC	P5	
				PAL C 16R8-35JC	J61	
				PAL C 16R8-35LC	L61	
				PAL C 16R8-35WC	W6	
—	35	25	70	PAL C 16R8-40DMB	D6	Military
				PAL C 16R8-40LMB	L61	
				PAL C 16R8-40WMB	W6	

CYPRESS SEMICONDUCTOR

PLD C 20G10

CMOS Generic 24 Pin Logic Device

Features

- Fast
  - Commercial: $t_{PD} = 25$ ns, $t_{CO} = 15$ ns, $t_S = 15$ ns
  - Military: $t_{PD} = 30$ ns, $t_{CO} = 20$ ns, $t_S = 20$ ns
- Low power
  - I_{CC} max.: 55 mA, Commercial
  - I_{CC} max.: 80 mA, Military
- Commercial and military temperature range
- User-programmable output cells
  - Selectable for registered or combinatorial operation
  - Output polarity control
  - Output enable source selectable from pin 13 or product term
- Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8
- Eight product terms and one OE product term per output
- CMOS EPROM technology for reprogrammability
- Highly reliable
  - Uses proven EPROM technology
  - Fully AC and DC tested
  - Security feature prevents logic pattern duplication
  - >2000V input protection for electrostatic discharge
  - ±10% power supply voltage and higher noise immunity

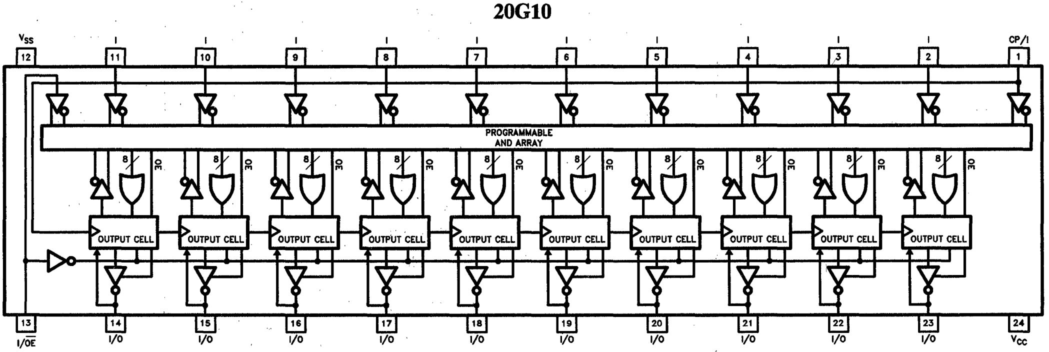
Functional Description

Cypress PLD devices are high speed electrically programmable Logic Devices. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

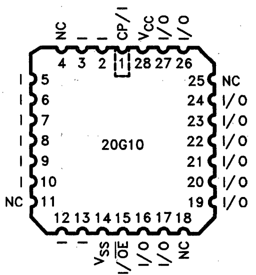
Cypress PLD C 20G10 uses an advanced 1.2 micron CMOS technology and a proven EPROM cell as the pro-

Logic Symbol


20G10
VSS 12
I 11
I 10
I 9
I 8
I 7
I 6
I 5
I 4
I 3
I 2
CP/I 1
PROGRAMMABLE AND ARRAY
8
OE
OUTPUT CELL
13 I/OE
14 I/O
15 I/O
16 I/O
17 I/O
18 I/O
19 I/O
20 I/O
21 I/O
22 I/O
23 I/O
24 VCC

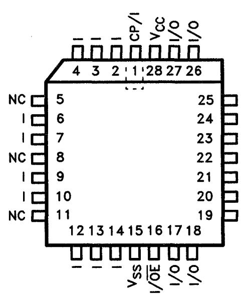
0053-15

LCC Pinout


NC I I CP/I VCC I/O I/O
4 3 2 1 28 27 26
I 5
I 6
I 7
I 8
I 9
I 10
NC 11
25 NC
24 I/O
23 I/O
22 I/O
21 I/O
20 I/O
19 I/O
20G10
12 13 14 15 16 17 18
I I VSS I/OE I/O I/O NC

0053-17

PLCC Pinout


I I I CP/I VCC I/O I/O
4 3 2 1 28 27 26
NC 5
I 6
I 7
NC 8
I 9
I 10
NC 11
25 I/O
24 I/O
23 I/O
22 I/O
21 I/O
20 I/O
19 NC
12 13 14 15 16 17 18
I I I VSS I/OE I/O I/O

0053-26

Selection Guide

Generic Part Number	t_{PD} ns		t_S ns		t_{CO} ns		I_{CC} mA	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
20G10-25	25	—	15	—	15	—	55	—
20G10-30	—	30	—	20	—	20	—	80
20G10-35	35	—	30	—	25	—	55	—
20G10-40	—	40	—	35	—	25	—	80

Functional Description (Continued)

grammable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

20G10 Functional Description

The PLD C 20G10 is a generic 24 pin device that can be programmed to logic functions which include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8. Thus, the PLD C 20G10 provides significant design, inventory and programming flexibility over dedicated 24 pin devices. It is executed in a 24 pin 300 mil molded DIP and a 300 mil windowed Cerdip. It provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The Programmable Output Cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with "REGISTERED" or "COMBINATORIAL" outputs, "ACTIVE HIGH" or "ACTIVE LOW" outputs, and "PRODUCT TERM" or "PIN 13" generated output enables. Three Architecture Bits determine the configurations as shown in Table 1 and in *Figures 2* through *9.* A total of eight different configurations are possible, with the two most common shown in *Figure 4* and *Figure 6.* The default or unprogrammed state is REGISTERED/ACTIVE LOW/PRODUCT TERM OE as shown in *Figure 2.* The entire Programmable Output Cell is shown in *Figure 1.*

The architecture bit 'C1' controls the REGISTERED/COMBINATORIAL option. In the "COMBINATORIAL" configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. In the "REGISTERED" configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the signal from Pin 1.

In both the Combinatorial and Registered configurations, the source of the "OUTPUT ENABLE" signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external $\overline{\text{OE}}$ pin (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for "OUTPUT POLARITY". The output can be either Active HIGH or Active LOW. This option is controlled by architecture bit 'CO'.

Along with this increase in functional density, the Cypress PLD C 20G10 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. The phantom array allows the 20G10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PLD C 20G10 at incoming inspection before committing the device to a specific function through programming.

Programmable Output Cell

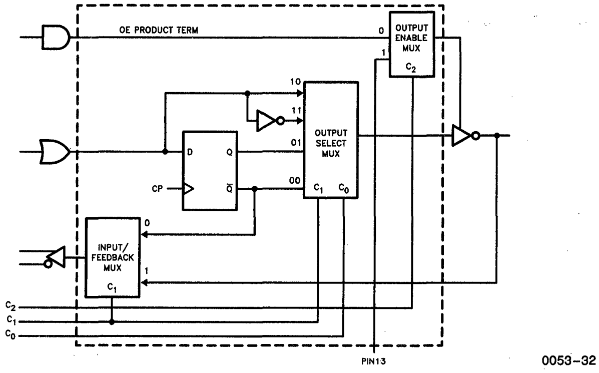


Figure 1

Configuration Table

Table 1

Figure	C_2	C_1	C_0	Configuration
2	0	0	0	Product Term OE/Registered/Active LOW
3	0	0	1	Product Term OE/Registered/Active HIGH
6	0	1	0	Product Term OE/Combinatorial/Active LOW
7	0	1	1	Product Term OE/Combinatorial/Active HIGH
4	1	0	0	Pin 13 OE/Registered/Active LOW
5	1	0	1	Pin 13 OE/Registered/Active HIGH
8	1	1	0	Pin 13 OE/Combinatorial/Active LOW
9	1	1	1	Pin 13 OE/Combinatorial/Active HIGH

Registered Output Configurations

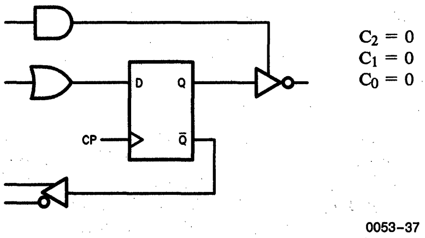

D
Q
CP
$\overline{Q}$
$C_2 = 0$
$C_1 = 0$
$C_0 = 0$
0053-37

Figure 2. Product Term OE/Active LOW

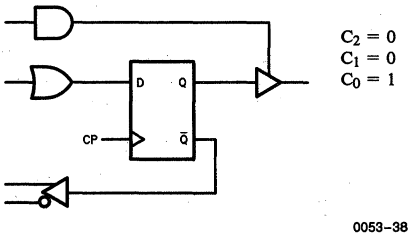

D
Q
CP
$\overline{Q}$
$C_2 = 0$
$C_1 = 0$
$C_0 = 1$
0053-38

Figure 3. Product Term OE/Active HIGH

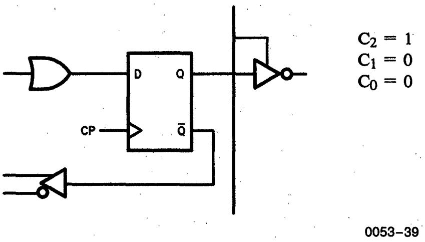

D
Q
CP
$\overline{Q}$
$C_2 = 1$
$C_1 = 0$
$C_0 = 0$
0053-39

Figure 4. Pin 13 OE/Active LOW

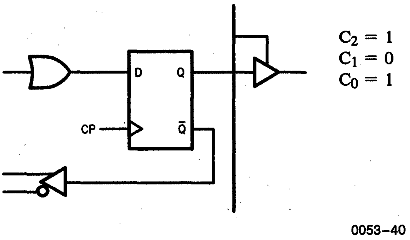

D
Q
CP
$\overline{Q}$
$C_2 = 1$
$C_1 = 0$
$C_0 = 1$
0053-40

Figure 5. Pin 13 OE/Active HIGH

Combinatorial Output Configurations

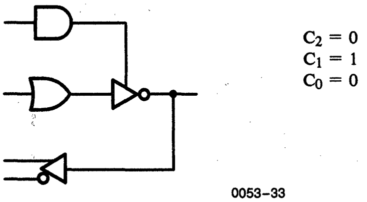

$C_2 = 0$
$C_1 = 1$
$C_0 = 0$
0053-33

Figure 6. Product Term OE/Active LOW

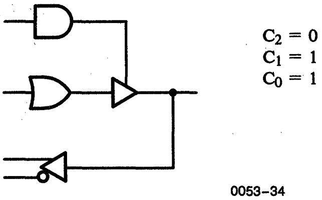

$C_2 = 0$
$C_1 = 1$
$C_0 = 1$
0053-34

Figure 7. Product Term OE/Active HIGH

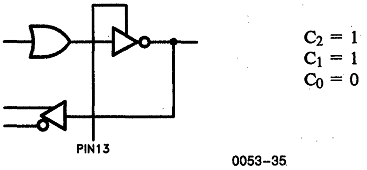

PIN13
$C_2 = 1$
$C_1 = 1$
$C_0 = 0$
0053-35

Figure 8. Pin 13 OE/Active LOW

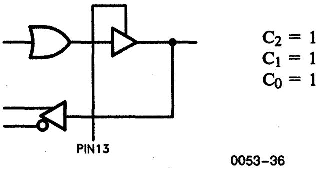

PIN13
$C_2 = 1$
$C_1 = 1$
$C_0 = 1$
0053-36

Figure 9. Pin 13 OE/Active HIGH

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

Output Current into Outputs (Low) . . . . 16 mA

DC Programming Voltage 14.0V

Static Discharge Voltage . . . . >2001V
(per MIL-STD-883 Method 3015.2)

Latchup Current . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Commercial		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[1] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[1] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			−10	10	μA
V_{PP}		Programming Voltage @ I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]				−90	mA
I_{CC}	Power Supply Current	$0 \leq V_{IN} \leq V_{CC}$ V_{CC} = Max., I_{OUT} = 0 mA	Commercial			55	mA
			Military			80	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−100	100	μA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C, f = 1$ MHz	4	pF
C_{OUT}	Output Capacitance	$V_{IN} = 0, V_{CC} = 5.0V$	7	

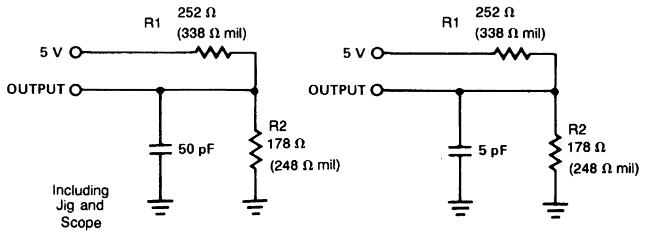
Switching Characteristics PLD C 20G10 Over Operating Range[4]

Parameters	Description	Commercial				Military				Units
		-25		-35		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		25		35		30			ns
t_{EA}	Input to Output Enable		25		35		30		40	ns
t_{ER}	Input to Output Disable		25		35		30		40	ns
t_{PZX}	Pin 13 to Output Enable		20		25		25		25	ns
t_{PXZ}	Pin 13 to Output Disable		20		25		25		25	ns
t_{CO}	Clock to Output		15		25		20		25	ns
t_S	Input or Feedback Setup Time	15		30		20		35		ns
t_H	Hold Time	0		0		0		0		ns
t_P	Clock Period	35		55		45		60		ns
t_W	Clock Width	15		20		20		25		ns
t_{MAX}	Maximum Frequency		33.3		18		25		16.5	MHz

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by tester ground degradation.
3. These parameters are not 100% tested, but are periodically sampled.
4. *Figure 10a* test load used for all parameters except t_{ER}, t_{PZX} and t_{PXZ}. *Figure 10b* test load used for t_{ER}, t_{PZX} and t_{PXZ}.

AC Test Loads and Waveforms (Commercial)


R1
252 Ω
(338 Ω mil)
5 V
OUTPUT
50 pF
R2
178 Ω
(248 Ω mil)
Including
Jig and
Scope
R1
252 Ω
(338 Ω mil)
5 V
OUTPUT
5 pF
R2
178 Ω
(248 Ω mil)

0053-6

Figure 10a

Figure 10b

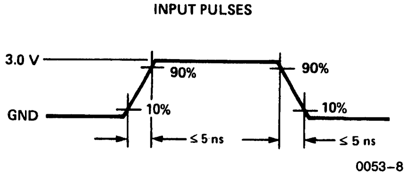
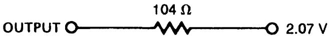

INPUT PULSES
3.0 V
GND
90%
10%
90%
10%
≤ 5 ns
≤ 5 ns
0053-8

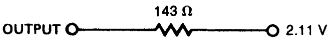
Figure 11

Equivalent to: THÉVENIN EQUIVALENT (Commercial)


104 Ω
OUTPUT
2.07 V

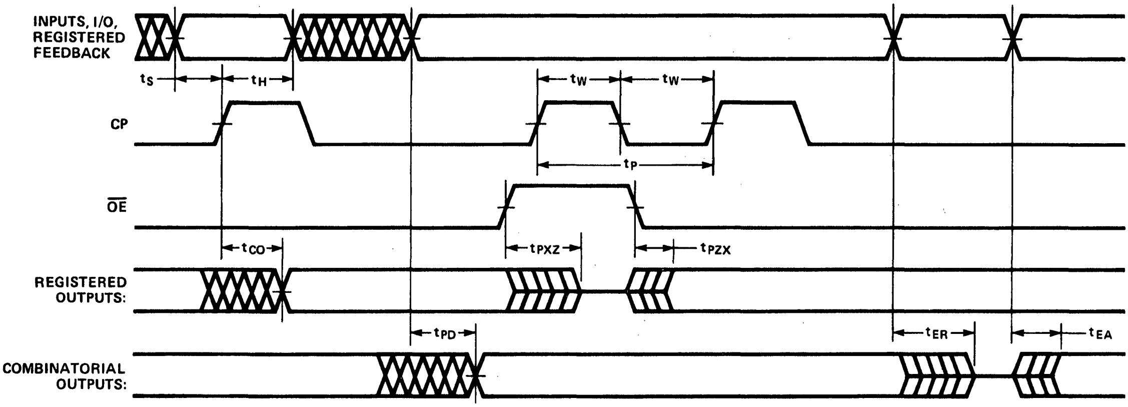
0053-7

Equivalent to: THÉVENIN EQUIVALENT (Military)


143 Ω
OUTPUT
2.11 V

0053-24

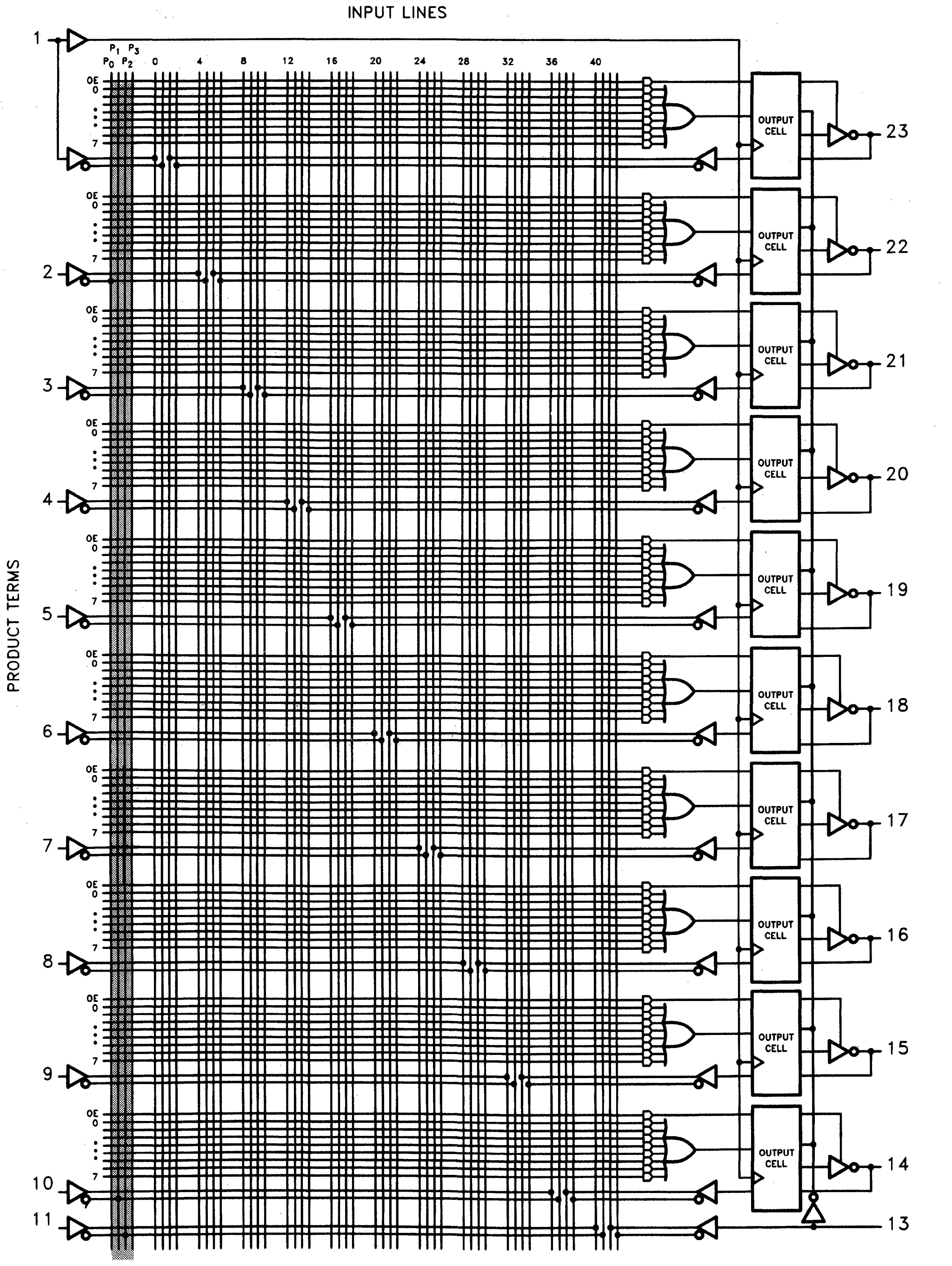
Switching Waveforms


INPUTS, I/O,
REGISTERED
FEEDBACK
t_S
t_H
t_W
t_W
CP
t_P
$\overline{OE}$
t_{CO}
t_{PXZ}
t_{PZX}
REGISTERED
OUTPUTS:
t_{PD}
t_{ER}
t_{EA}
COMBINATORIAL
OUTPUTS:

0053-9

Note:
For more information regarding PLD devices, refer to the Application Brief in the Appendix.

Functional Logic Diagram PLD C 20G10


INPUT LINES
P1 P3
P0 P2
0
4
8
12
16
20
24
28
32
36
40
OE
0
7
PRODUCT TERMS
OUTPUT CELL
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13

0053–23

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PLD C 20G10 in the windowed CERDIP package. For this reason, an opaque label should be placed over the window if the PAL device is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 1800 mW × min/cm^2. For an ultraviolet lamp with a 40 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The PLD C 20G10 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Device Programming

The PLD C 20G10 can be programmed on inexpensive conventional PROM/EPROM programmers with appropriate personality or socket adapters and the CY3000 QuickPro programmer. Once the PLD device is programmed, one additional location can be programmed to prohibit logic pattern verification. This security feature gives the user additional protection to safeguard his proprietary logic. This feature is highly reliable and due to EPROM technology it is impossible to visually read the programmed cell locations.

The PLD C 20G10 has multiple programmable functions. In addition to the normal array, a "PHANTOM" array, "TOP and BOTTOM TEST" and a "SECURITY" feature are programmable. The PLD C 20G10 security mechanism, when invoked, prevents access to the "NORMAL" and "TOP/BOTTOM TEST" array. The "PHANTOM" array feature is still accessible, allowing programming and verification of the pattern in the "PHANTOM" array. Functional operation of all other features is allowed regardless of the state of the "SECURITY BIT". In addition, the device contains 10 programmable output cells which are programmed to configure the device functionality for each specific application.

The logic array is divided into a "NORMAL" array and a "PHANTOM" array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress' testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The "PHANTOM" array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and programmable output cells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

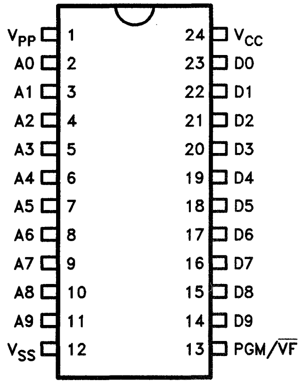
The "TOP TEST" and "BOTTOM TEST" feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the "TOP TEST" and "BOTTOM TEST" mode. Like the Phantom array above, this feature has no effect in the normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

The architecture bits C_0, C_1 and C_2 are used to configure each programmable output cell individually. C_0 selects output polarity, C_1 selects the combinatorial or registered mode of operation and C_2 selects the source of output enable. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the output cell into a combinatorial mode and disabling the ouput with the output enable product term.

Pinout

The PLD C 20G10 PROGRAMMING pinout is shown in *Figure 12*. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

Programming Pinout



0053-27

Figure 12

Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a "1" or "0" on the I/O pins. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 2 "Operating Modes" along with Tables 3 through 6 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the "PHANTOM" and "TEST" modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

20G10 JEDEC Map

The 20G10 JEDEC Map is organized as follows: the EPROM fuses for the product terms and input lines are located between 0000 and 3959 (decimal). The architecture bits are located between locations 3960 and 3989. Location 3960 is the Polarity Bit (CO), location 3961 is the Registered/Combinatorial Bit (C1), and location 3962 is the Output Enable Bit (C2) for output pin 23. Locations 3963, 3964, and 3965 are the architecture bit locations for output pin 22. This pattern repeats for output pins 21, 20, 19, 18, 17, 16, 15, and 14.

Operating Modes

Table 2 describes the operating and programming modes of the PLD C 20G10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in *Figures 14* & *15*. Tables 3 through 6 are used as indicated to provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10. These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The programmable output cells function as they are programmed for normal operation. If the programmable output cells have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage V_{PP} on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the V_{CC} is stable, and removed a minimum of 20 ms before V_{CC} is removed.

TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A "0" on the I/O pin preloads the register with a "0" and a "1" preloads the register with a "1". The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.

Operating Modes

Table 2

Operating Modes		Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 17	Pin 20	Pins 15, 16, 18, 19, 21 & 22	Pin 23
Feature	**Function**																	
Main Array Product	Program	V_{PP}	Table 3						Table 4				V_{PP}	Data In				
	Program Inhibit	V_{PP}											V_{IHP}	High Z				
	Program Verify[3]	V_{PP}											V_{ILP}	Data Out				
Output Enable Product Terms	Program	V_{PP}	Table 3						V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				
Top Test, Bottom Test Notes	Program	V_{PP}	Table 3						V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	Data In	Data In	Data In	V_{ILP}	Data In
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	High Z	High Z	High Z	High Z	High Z
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Data Out	Data Out	Data Out	Driven	Data Out
Architecture Bits	Program	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Table 5		V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{ILP}	Data Out				
Security Bit	Program	V_{PP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
	Verify	V_{ILP}	V_{ILP}	Data Out	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	Driven Outputs				
PAL Mode Operation	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O				
	Phantom	NA	I	NA	NA	NA	V_{PP}	I	NA	NA	I	I	NA	Output				
	Top Test	I	I	I	I	I	I	I	I	V_{PP}	I	I	I	NA				Out
	Bottom Test	I	I	I	I	I	I	I	I	I	V_{PP}	I	I	Out	NA			
	Reg Preload	Notes	NA	NA	NA	NA	NA	NA	V_{PP}	NA	NA	NA	V_{ILP}	Data In				
Phantom Array Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 6		V_{ILP}	V_{PP}	Table 4				V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{ILP}	Data Out				
Phantom Output Enable Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 6		V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{IL}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.
   Pin 14 = BOTTOM TEST
   Pin 17 = Synchronous Set
   Pin 20 = Asynchronous Reset
   Pin 23 = TOP TEST
2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
3. It is necessary to toggle $\overline{OE}$ (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

Input Term Addresses

Table 3 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 2. It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

Input Term Addresses

Table 3

Input Term	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
16	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
18	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
20	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
22	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
24	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
25	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
26	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
28	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
29	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
30	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
32	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
33	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
34	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
35	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
36	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
37	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
38	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
39	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
40	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
41	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
42	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
43	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}

Product Term Addresses

Table 4 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the 8 product terms associated with each input.

Product Term Addresses

Table 4

Product Term	Pin 8	Pin 9	Pin 10	Pin 11
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}

Architecture Bit Addressing

Table 5 provides the addressing for the architecture bits used to control the configuration of the individual Programmable Output Cells. In the unprogrammed state, the Programmable Output Cells are in a registered, active low or inverting configuration with output enable controlled from the product term. They are programmed with a "1" on the pin associated with the Programmable Output Cells and the appropriate address as shown in Table 5. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the Programmable Output Cells.

Architecture Bit Addressing

Table 5

Architecture Bit	Pin 9	Pin 10
Output Polarity C0	V_{ILP}	V_{ILP}
Register/ Combinatorial Output C1	V_{IHP}	V_{ILP}
Product Term/ Pin 13 Output Enable C2	V_{ILP}	V_{IHP}

Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively.

Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

Phantom Input Term Addresses

Table 6

Phantom Input Term	Pin 4	Pin 5
P0	V_{ILP}	V_{ILP}
P1	V_{IHP}	V_{ILP}
P2	V_{ILP}	V_{IHP}
P3	V_{IHP}	V_{IHP}

Programming Flow Chart

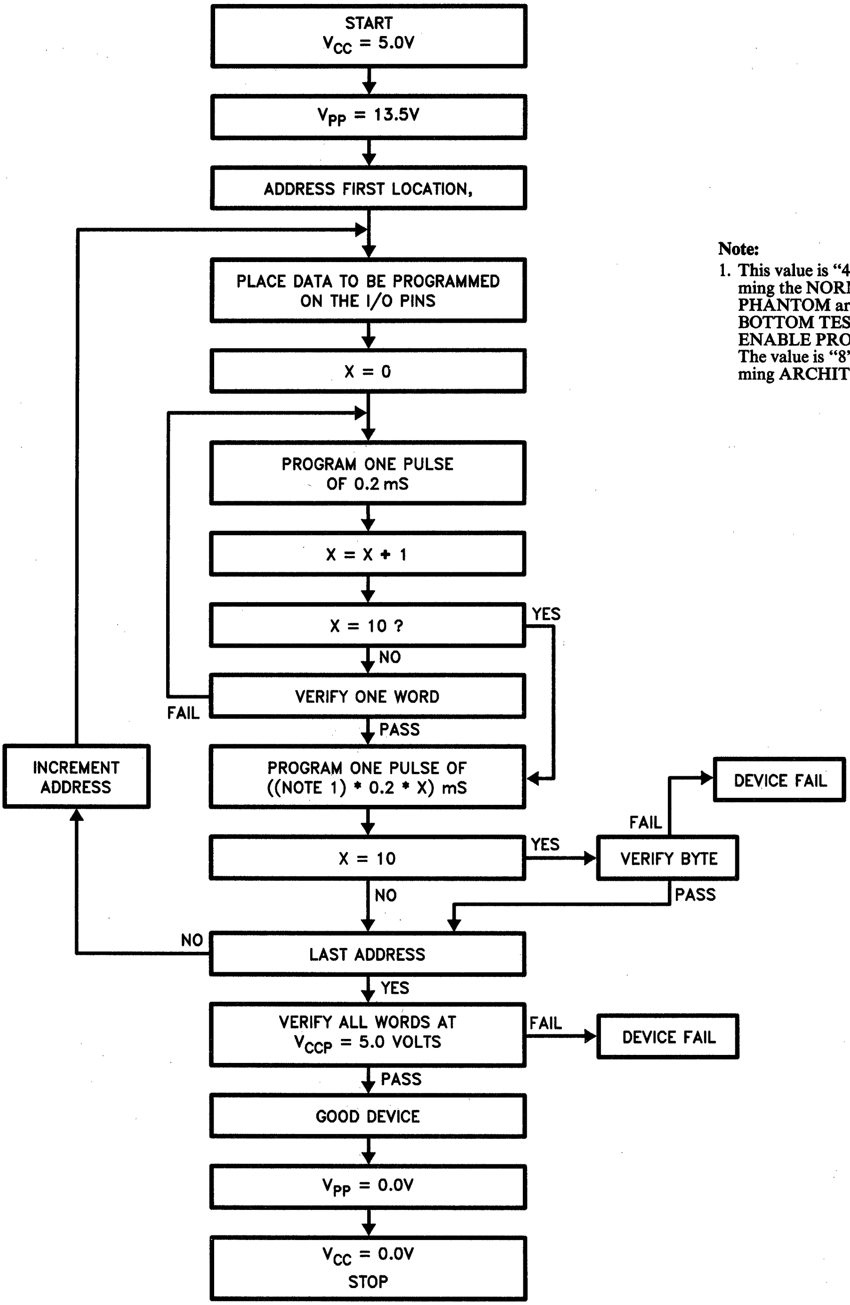
The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of V_{CC} prior to V_{PP}, and removal of V_{PP} prior to V_{CC}. See *Figure 14* and Table 8 for specific timing and AC requirements. Notice that all programming is accomplished without switching V_{PP} on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, *Figure 13* and timing diagram *Figure 14*. After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather *Figure 14* also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.

Programming Flowchart


START
V_{CC} = 5.0V
V_{PP} = 13.5V
ADDRESS FIRST LOCATION,
PLACE DATA TO BE PROGRAMMED ON THE I/O PINS
X = 0
PROGRAM ONE PULSE OF 0.2 mS
X = X + 1
X = 10 ?
YES
NO
VERIFY ONE WORD
FAIL
PASS
INCREMENT ADDRESS
PROGRAM ONE PULSE OF ((NOTE 1) * 0.2 * X) mS
DEVICE FAIL
FAIL
X = 10
YES
VERIFY BYTE
NO
PASS
NO
LAST ADDRESS
YES
VERIFY ALL WORDS AT V_{CCP} = 5.0 VOLTS
FAIL
DEVICE FAIL
PASS
GOOD DEVICE
V_{PP} = 0.0V
V_{CC} = 0.0V
STOP

Note:

1. This value is “4” for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is “8” when programming ARCHITECTURE BITS.

0053–28

Figure 13

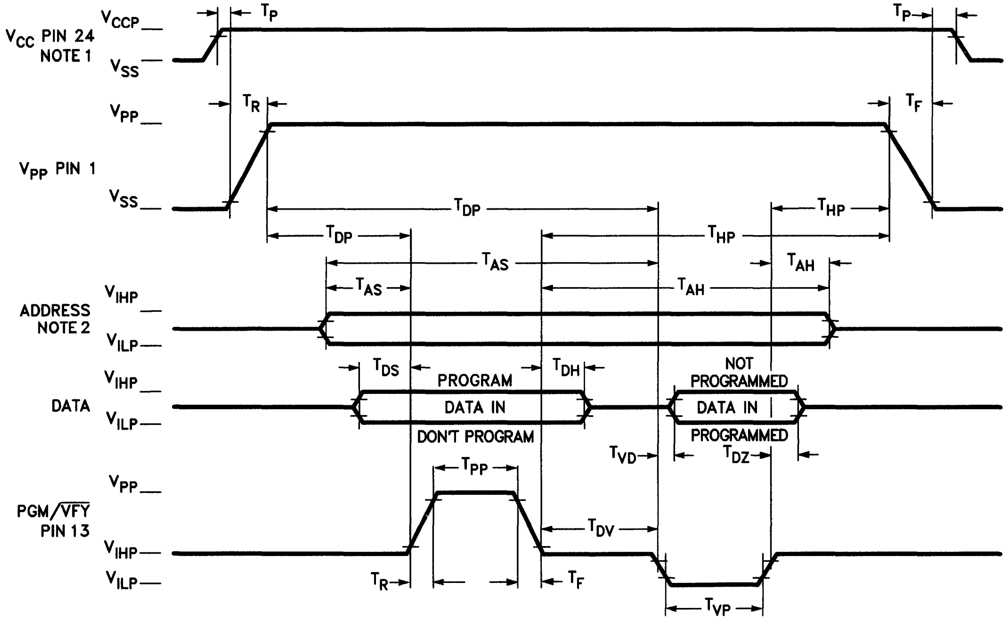
Timing Diagrams

Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 14.* ADDRESS refers to all applicable information in Tables 2 through 6 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and DATA OUT is verified on the same pins. A "1" (V_{IHP}) on an I/O pin causes the addressed location to be programmed. A "0" on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

Programming Waveforms


V_{CC} PIN 24 NOTE 1
V_{CCP}
V_{SS}
T_P
T_P
V_{PP} PIN 1
V_{PP}
V_{SS}
T_R
T_F
T_{DP}
T_{HP}
T_{DP}
T_{HP}
T_{AS}
T_{AH}
T_{AS}
T_{AH}
ADDRESS NOTE 2
V_{IHP}
V_{ILP}
DATA
V_{IHP}
V_{ILP}
T_{DS}
T_{DH}
PROGRAM
DATA IN
DON'T PROGRAM
NOT PROGRAMMED
DATA IN
PROGRAMMED
T_{VD}
T_{DZ}
T_{PP}
PGM/$\overline{VFY}$ PIN 13
V_{PP}
V_{IHP}
V_{ILP}
T_{DV}
T_R
T_F
T_{VP}

0053-29

Notes:

1. Power, V_{PP} & V_{CC} should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming $\overline{\text{OE}}$ Product Terms & Architecture bits, Pin 11 (A9) must go to V_{PP} and satisfy T_{AS} and T_{AN}.

Figure 14

Security Cell

The security cell is programmed independently per the timing diagram in *Figure 15,* and the information in Table 2. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the same pin. A "0" on pin 3 indicates that the security bit has been programmed, and a "1" indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after V_{PP} has been removed from pin 1.

Programming Waveforms Security Cell

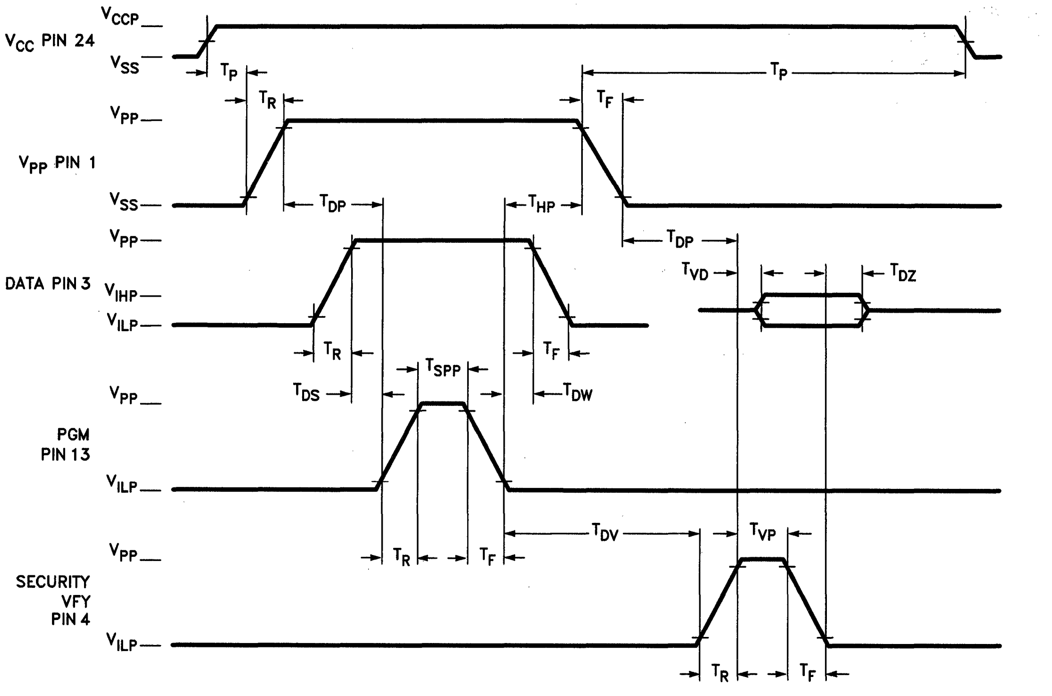

V_{CCP}
V_{CC} PIN 24
V_{SS}
T_P
T_P
T_R
T_F
V_{PP}
V_{PP} PIN 1
V_{SS}
T_{DP}
T_{HP}
T_{DP}
V_{PP}
DATA PIN 3
V_{IHP}
V_{ILP}
T_{VD}
T_{DZ}
T_R
T_F
T_{SPP}
T_{DS}
T_{DW}
V_{PP}
PGM PIN 13
V_{ILP}
T_{DV}
T_{VP}
V_{PP}
T_R
T_F
SECURITY VFY PIN 4
V_{ILP}
T_R
T_F
0053-30

Figure 15

DC Programming Parameters $T_A = 25°C$

Table 7

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	Volts
V_{CCP}	Supply Voltage During Programming	4.75	5.25	Volts
V_{IHP}	Input HIGH Voltage During Programming	3.0	V_{CCP}	Volts
V_{ILP}	Input LOW Voltage During Programming	−3.0	0.4	Volts
V_{OH}	Output HIGH Voltage	2.4		Volts
V_{OL}	Output LOW Voltage		0.4	Volts
I_{PP}	Programming Supply Current		40	mA

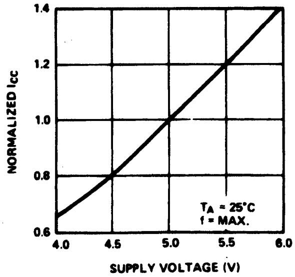
AC Programming Parameters

Table 8

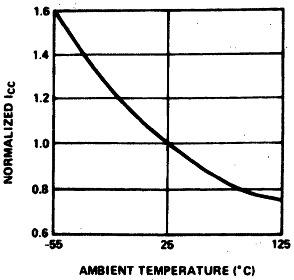
Parameter	Description	Min.	Max.	Units
T_P	Delay to Programming Voltage	20		ms
T_{DP}	Delay to Program	1		µs
T_{HP}	Hold from Program or Verify	1		µs
$T_{R,F}$	V_{PP} Rise & Fall Time	50		ns
T_{AS}	Address Setup Time	1		µs
T_{AH}	Address Hold Time	1		µs
T_{DS}	Data Setup Time	1		µs
T_{DH}	Data Hold Time	1		µs
T_{PP}	Programming Pulsewidth	0.2	10	ms
T_{SPP}	Programming Pulsewidth for Security	50		ms
T_{DV}	Delay from Program to Verify	2		µs
T_{VD}	Delay to Data Out		1	µs
T_{VP}	Verify Pulse Width	2		µs
T_{DZ}	Verify to High Z		1	µs

Typical DC and AC Characteristics

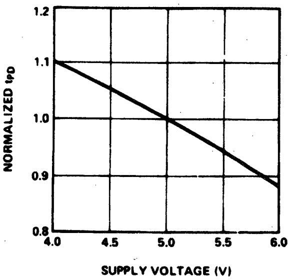
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



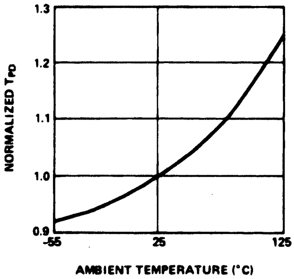
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



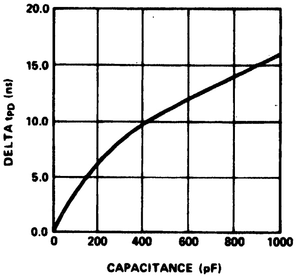
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



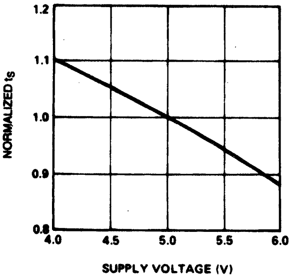
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



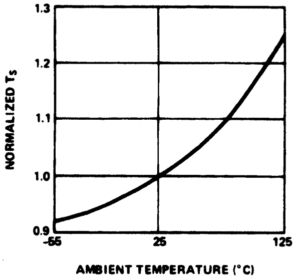
DELTA PROPAGATION TIME vs. OUTPUT LOADING



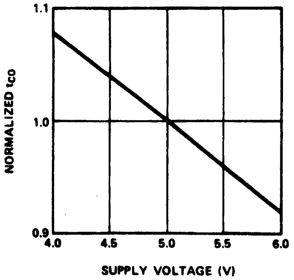
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



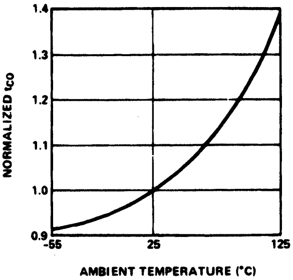
NORMALIZED SETUP TIME vs. TEMPERATURE



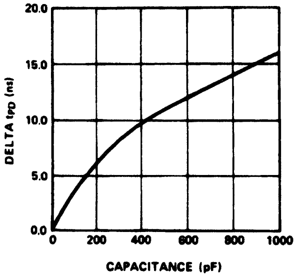
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



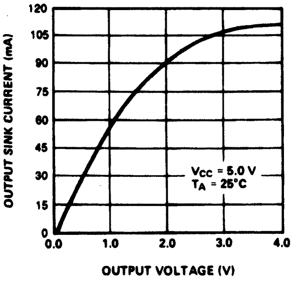
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



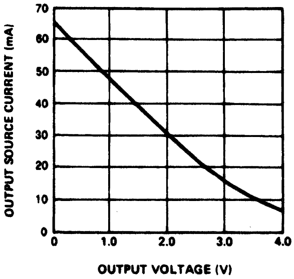
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



0053-31

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
25	15	15	55	PLD C 20G10-25PC	P13	Commercial
				PLD C 20G10-25WC	W14	
				PLD C 20G10-25JC	J64	
30	20	20	80	PLD C 20G10-30DMB	D14	Military
				PLD C 20G10-30WMB	W14	
				PLD C 20G10-30LMB	L64	
35	30	25	55	PLD C 20G10-35PC	P13	Commercial
				PLD C 20G10-35WC	W14	
				PLD C 20G10-35JC	J64	
40	35	25	80	PLD C 20G10-40DMB	D14	Military
				PLD C 20G10-40WMB	W14	
				PLD C 20G10-40LMB	L64	

CYPRESS SEMICONDUCTOR

PAL C 22V10

Reprogrammable CMOS PAL® Device

Features

- **Advanced second generation PAL architecture**
- **Low power**
  - **— 55 mA max "L"**
  - **— 90 mA max standard**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 × (8 thru 16) product terms**
- **User programmable macro cell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **25 ns commercial and military**
  - **— "25" commercial**
    15 ns t_{CO}
    15 ns t_S
    25 ns t_{PD}
    33.3 MHz
  - **— "25" military**
    20 ns t_{CO}
    20 ns t_S
    25 ns t_{PD}
    25 MHz
- **Up to 22 input terms and 10 outputs**
- **Enhanced test features**
  - **— Phantom array**
  - **— Top Test**
  - **— Bottom Test**
  - **— Preload**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >2000V input protection**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

Functional Description

The Cypress PAL C 22V10 is a CMOS second generation Programmable Logic Array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macro Cell".

The PAL C 22V10 is executed in a 24 pin 300 mil molded DIP, a 300 mil windowed Cerdip, and a 28 lead square leadless chip carrier and provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 22V10 is erased and then can be reprogrammed. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may

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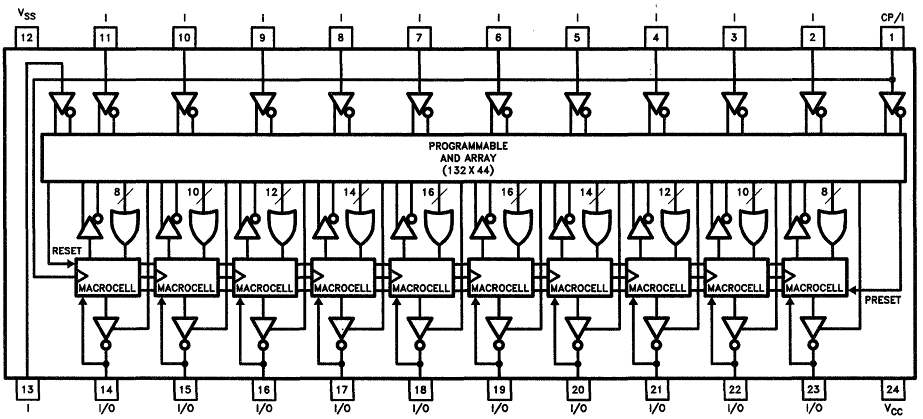
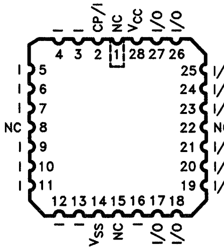
Logic Symbol and Pinout


V_{SS}
12
I
11
10
9
8
7
6
5
4
3
2
CP/I
1
PROGRAMMABLE AND ARRAY (132 X 44)
8
10
12
14
16
16
14
12
10
8
RESET
MACROCELL
PRESET
13
I
14
I/O
15
16
17
18
19
20
21
22
23
24
VCC

0023-1

LCC and PLCC Pinout


I
I
CP/I
NC
VCC
I/O
I/O
4 3 2 1 28 27 26
I 5
I 6
I 7
NC 8
I 9
I 10
I 11
25 I/O
24 I/O
23 I/O
22 NC
21 I/O
20 I/O
19 I/O
12 13 14 15 16 17 18
I
I
VSS
NC
I
I/O
I/O

0023-10

Functional Description (Continued)

also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.

The PAL C 22V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 22V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets on power-up.

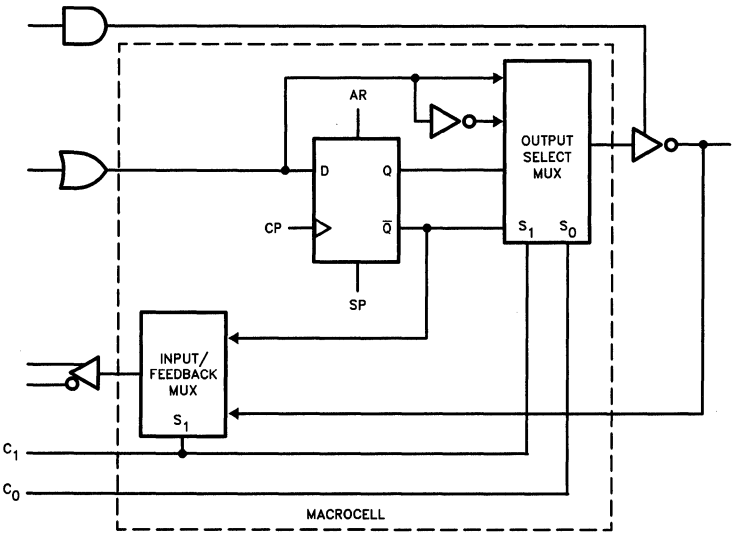
The PAL C 22V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled through the use of product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. These macro cells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 22V10 provides lower power operation thru the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. This phantom array (P_0–P_3) and the "TOP TEST" and "BOTTOM TEST" features allow the 22V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 22V10 at incoming inspection before committing the device to a specific function through programming. PRELOAD facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 1

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

Macrocell



0023-2

Selection Guide

Generic Part Number	I_{CC} mA			t_{PD} ns		t_S ns		t_{CO} ns	
	"L"	Com	Mil	Com	Mil	Com	Mil	Com	Mil
22V10-25	55	90	100	25	25	15	20	15	20
22V10-30		—	100	—	30	—	25	—	20
22V10-35	55	90	—	35	—	30	—	25	—
22V10-40		—	100	—	40	—	35	—	25

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 16 mA

UV Exposure .... 7258 Wsec/cm^2

DC Programming Voltage 14.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.2$ mA	COM'L	2.4		V
			$I_{OH} = -2$ mA	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16$ mA	COM'L		0.5	V
			$I_{OL} = 12$ mA	MIL			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		"L"		55	mA
				COM'L		90	mA
				MIL		100	mA

Capacitance[3]

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

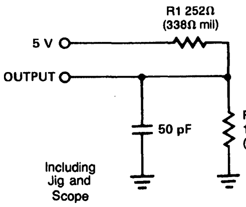
Notes:

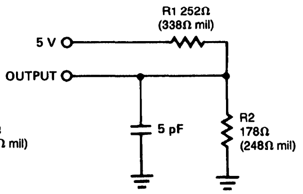
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation
3. These parameters are not 100% tested, but are periodically sampled.
4. *Figure 1a* test load used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.

Switching Characteristics PAL C 22V10[4]

Parameters	Description	Commercial				Military						Units
		−25		−35		−25		−30		−40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		25		35		25		30		40	ns
t_{EA}	Input to Output Enable		25		35		25		30		40	ns
t_{ER}	Input to Output Disable		25		35		25		30		40	ns
t_{CO}	Clock to Output		15		25		20		20		25	ns
t_S	Input or Feedback Setup Time	15		30		20		25		35		ns
t_H	Hold Time	0		0		0		0		0		ns
t_P	Clock Period ($t_s + t_{co}$)	30		55		40		45		60		ns
t_W	Clock Width	15		25		15		20		30		ns
f_{MAX}	Maximum Frequency		33.3		18		25		22		16.5	MHz
t_{AW}	Asynchronous Reset Width	25		35		25		30		40		ns
t_{AR}	Asynchronous Reset Recovery Time		25		35		25		30		40	ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		35		25		30		40	ns

AC Test Loads and Waveforms (Commercial)

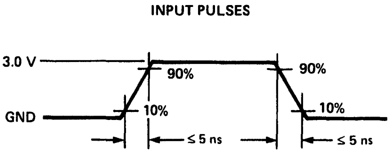

R1 252Ω
(338Ω mil)
5 V
OUTPUT
50 pF
R2
178Ω
(248Ω mil)
Including
Jig and
Scope


R1 252Ω
(338Ω mil)
5 V
OUTPUT
5 pF
R2
178Ω
(248Ω mil)

0023-11

Figure 1a

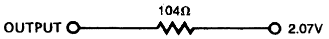
Figure 1b


INPUT PULSES
3.0 V
GND
90%
10%
90%
10%
≤ 5 ns
≤ 5 ns

0023-12

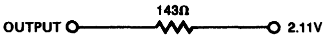
Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial)


104Ω
OUTPUT
2.07V

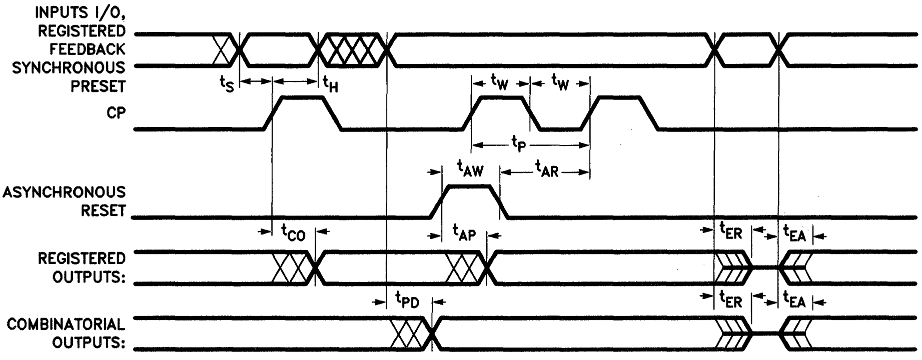
0023-13

Equivalent to: THÉVENIN EQUIVALENT (Military)


143Ω
OUTPUT
2.11V

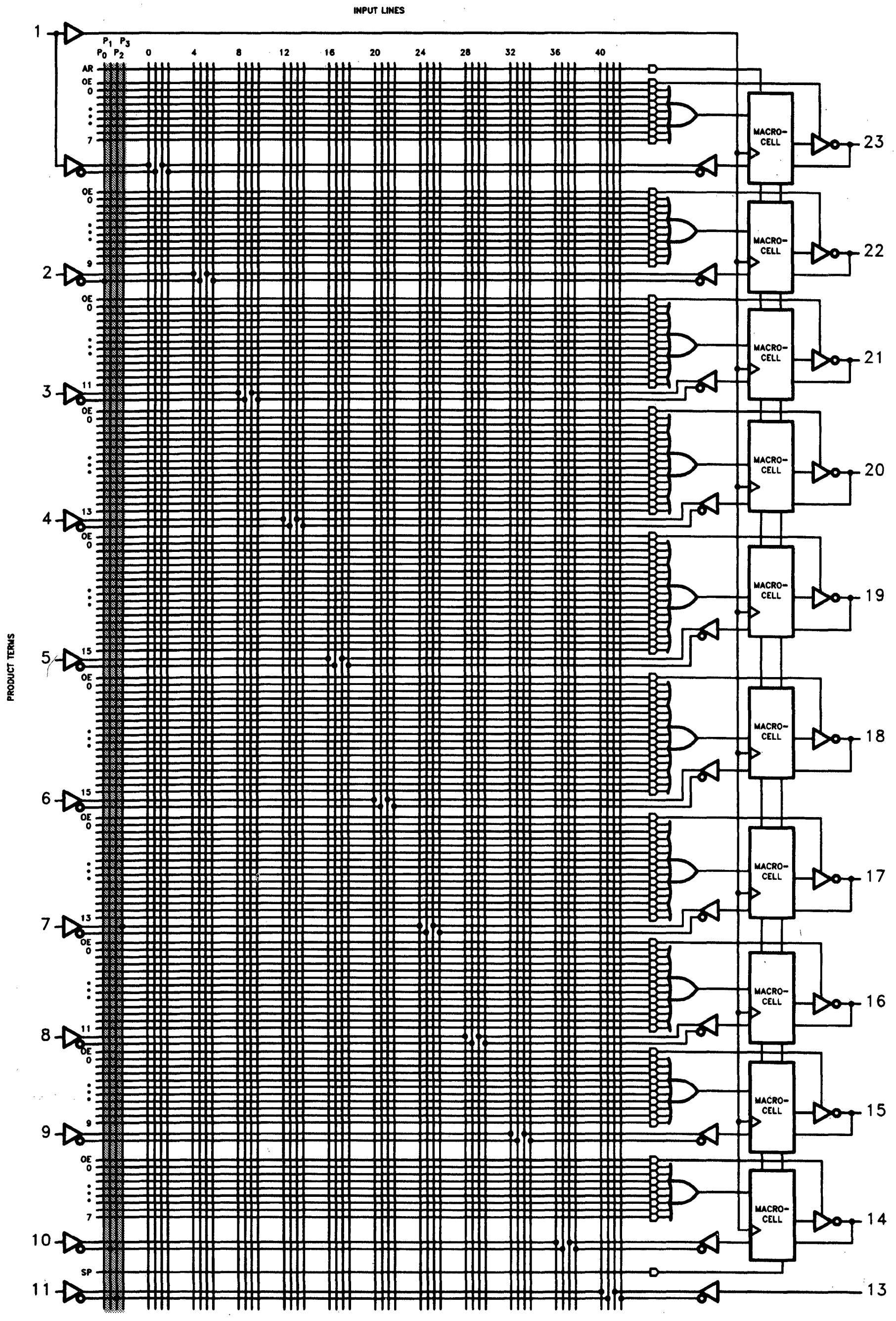
0023-14

Switching Waveforms


INPUTS I/O,
REGISTERED
FEEDBACK
SYNCHRONOUS
PRESET
t_S
t_H
t_W
t_W
CP
t_P
t_{AW}
t_{AR}
ASYNCHRONOUS
RESET
t_{CO}
t_{AP}
t_{ER}
t_{EA}
REGISTERED
OUTPUTS:
t_{PD}
t_{ER}
t_{EA}
COMBINATORIAL
OUTPUTS:

0023-3

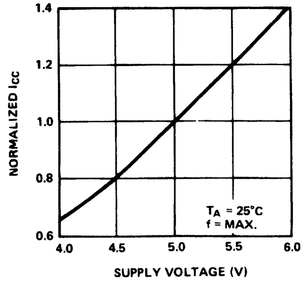
Functional Logic Diagram PAL C 22V10


INPUT LINES
PRODUCT TERMS
P1 P3
P0 P2
0
4
8
12
16
20
24
28
32
36
40
AR
OE
0
7
9
11
13
15
SP
MACRO-CELL
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13

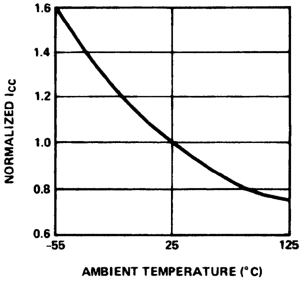
0023–4

Typical DC and AC Characteristics

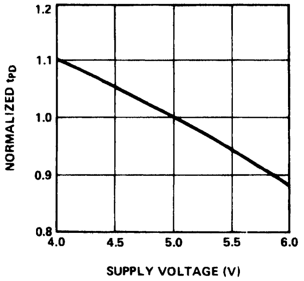
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



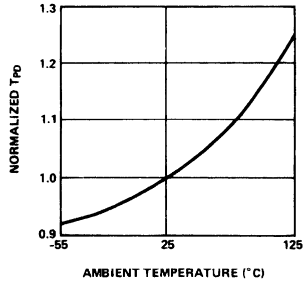
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



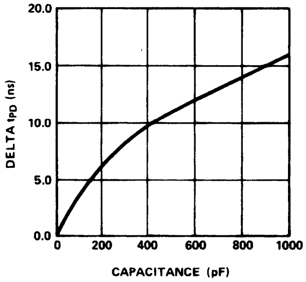
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



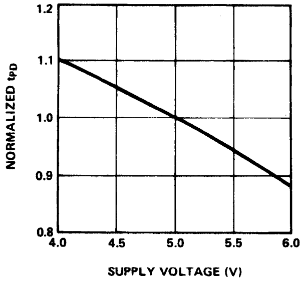
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



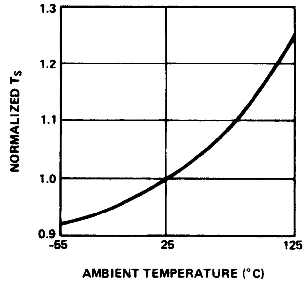
DELTA PROPAGATION TIME vs. OUTPUT LOADING



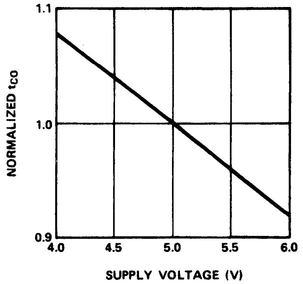
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



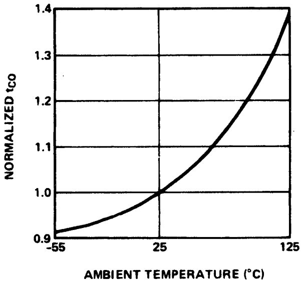
NORMALIZED SETUP TIME vs. TEMPERATURE



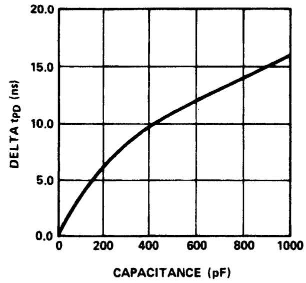
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



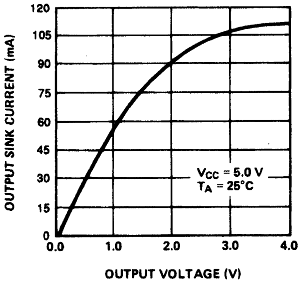
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



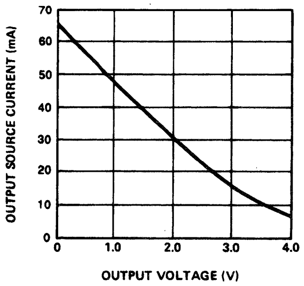
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



0023–15

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PAL C 22V10 in the windowed CERDIP package. For this reason, an opaque label should be placed over the window if the PAL device is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 1800 mW × min/cm^2. For an ultraviolet lamp with a 40 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 22V10 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Device Programming

The PAL C 22V10 has multiple programmable functions. In addition to the normal array, a "PHANTOM" array, "TOP and BOTTOM TEST" and a "SECURITY" feature are programmable. The PAL C 22V10 security mechanism, when invoked, prevents access to the "NORMAL" and "TOP/BOTTOM TEST" array. The "PHANTOM" array feature is still accessible, allowing programming and verification of the pattern in the "PHANTOM" array. Functional operation of all other features is allowed regardless of the state of the "SECURITY BIT". In addition, the device contains 10 MACROCELLS which are programmed to configure the device functionality for each specific application.

The logic array is divided into a "NORMAL" array and a "PHANTOM" array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress' testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The "PHANTOM" array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and macrocells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

The "TOP TEST" and "BOTTOM TEST" feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the "TOP TEST" and "BOTTOM TEST" mode. Like the Phantom array above, this feature has no effect in the normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

The Cypress PAL C 22V10 contains 10 identical MACROCELLS which may be individually configured. Each MACROCELL is associated with a single I/O pin and through the architecture bits, each associated pin may be permanently configured as an input, an output or be used as both input and output as a function of the logical function in the array. Each MACROCELL consists of a type "D" latch, an output multiplexer, a feedback multiplexer and a tristatable output driver that is controlled by a unique product term. The clock is common to all MACROCELLS, and comes from pin 1 of the device. Each register also has an asynchronous reset and a synchronous preset. These are each driven by product terms. These product terms are common to all MACROCELLS allowing all registers to either be asynchronously reset or synchronously preset by a logical function in the array. The device is automatically reset at power up. A preload feature allows the registers to be preloaded with any state for testing.

The architecture bits C0 and C1 are used to configure each MACROCELL individually. C0 selects the polarity of the

Macrocell

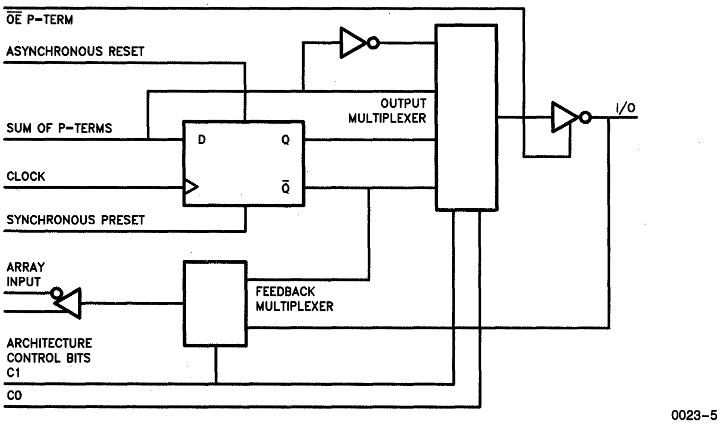


Figure 1

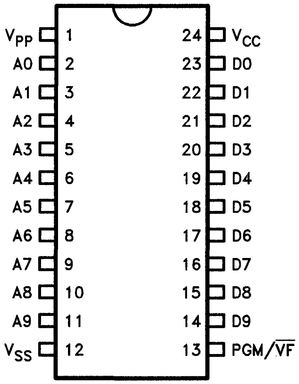
Device Programming (Continued)

output and C1 selects the combinatorial or registered mode of operation. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the MACROCELL into a combinatorial mode and disabling the ouput with the output enable product term.

Pinout

The PAL C 22V10 PROGRAMMING pinout is shown in *Figure 3*. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

Programming Pinout



0023-6

Figure 2

Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a "1" or "0" on the I/O pins. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 1 "Operating Modes" along with Tables 2 through 5 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the "PHANTOM" and "TEST" modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

Operating Modes

Table 1 describes the operating and programming modes of the PAL C 22V10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in *Figures 5 & 6*. Tables 2 through 5 are used as indicated to provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10. These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The MACROCELLS function as they are programmed for normal operation. If the MACROCELLS have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage V_{PP} on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the V_{CC} is stable, and removed a minimum of 20 ms before V_{CC} is removed.

TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A "0" on the I/O pin preloads the register with a "0" and a "1" preloads the register with a "1". The actual signal on the output pin will depend on the output polarity selected when the MACROCELL is programmed. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.

Operating Modes

Table 1

Operating Modes		Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 17	Pin 20	Pins 15, 16, 18, 19, 21 & 22	Pin 23
Feature	Function																	
Main Array Product	Program	V_{PP}	Table 2						Table 3				V_{PP}	Data In				
	Program Inhibit	V_{PP}											V_{IHP}	High Z				
	Program Verify[3]	V_{PP}											V_{ILP}	Data Out				
Output Enable Product Terms	Program	V_{PP}	Table 2						V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				
Sync Set, Async Reset, Top Test, Bottom Test Notes	Program	V_{PP}	Table 2						V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	Data In	Data In	Data In	V_{ILP}	Data In
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	High Z	High Z	High Z	High Z	High Z
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Data Out	Data Out	Data Out	Driven	Data Out
Architecture Bits	Program	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Table 4		V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{ILP}	Data Out				
Security Bit	Program	V_{PP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
	Verify	V_{ILP}	V_{ILP}	Data Out	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	Driven Outputs				
PAL Mode Operation	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O				
	Phantom	NA	I	NA	NA	NA	V_{PP}	I	NA	NA	I	I	NA	Output				
	Top Test	I	I	I	I	I	I	I	I	V_{PP}	I	I	I	NA				Out
	Bottom Test	I	I	I	I	I	I	I	I	I	V_{PP}	I	I	Out	NA			
	Reg Preload	Notes	NA	NA	NA	NA	NA	NA	V_{PP}	NA	NA	NA	V_{ILP}	Data In				
Phantom Array Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 5		V_{ILP}	V_{PP}	Table 3				V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{ILP}	Data Out				
Phantom Output Enable Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 5		V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{IL}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.
   Pin 14 = BOTTOM TEST
   Pin 17 = Synchronous Set
   Pin 20 = Asynchronous Reset
   Pin 23 = TOP TEST
2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
3. It is necessary to toggle $\overline{OE}$ (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

Input Term Addresses

Table 2 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 1. It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

Input Term Addresses

Table 2

Input Term	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
16	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
18	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
20	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
22	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
24	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
25	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
26	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
28	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
29	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
30	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
32	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
33	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
34	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
35	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
36	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
37	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
38	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
39	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
40	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
41	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
42	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
43	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}

Product Term Addresses

Table 3 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the up to 16 product terms associated with each input. Notice that the number of product terms varies from 8 to 16 and back to 8 from the top to the bottom output. In Table 3, product term "0" refers to the top product term associated with the MACROCELLS on pins 18 and 19, while address 15 refers to the bottom or last product term associated with the same pins. In the same manner, the 8 product terms associated with pins 14 and 23 are addressed as "0" through "7". The balance of the product terms associated with the remaining I/O pins are addressed as "0" through "10", "12" and "14".

Product Term Addresses

Table 3

Product Term	Pin 8	Pin 9	Pin 10	Pin 11
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}

Architecture Bit Addresssing

Table 4 provides the addressing for the architecture bits used to control the configuration of the individual MACROCELLS. In the unprogrammed state, the MACROCELLS are in a registered, active low or inverting configuration. They are programmed with a "1" on the pin associated with the MACROCELL and the appropriate address as shown in Table 4. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the MACROCELL.

Architecture Bit Addresssing

Table 4

Architecture Bit	Pin 9	Pin 10
Output Polarity C0	V_{ILP}	V_{ILP}
Register/ Non-Register Output C1	V_{IHP}	V_{ILP}

Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively. Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

Phantom Input Term Addresses

Table 5

Phantom Input Term	Pin 4	Pin 5
P0	V_{ILP}	V_{ILP}
P1	V_{IHP}	V_{ILP}
P2	V_{ILP}	V_{IHP}
P3	V_{IHP}	V_{IHP}

Programming Flow Chart

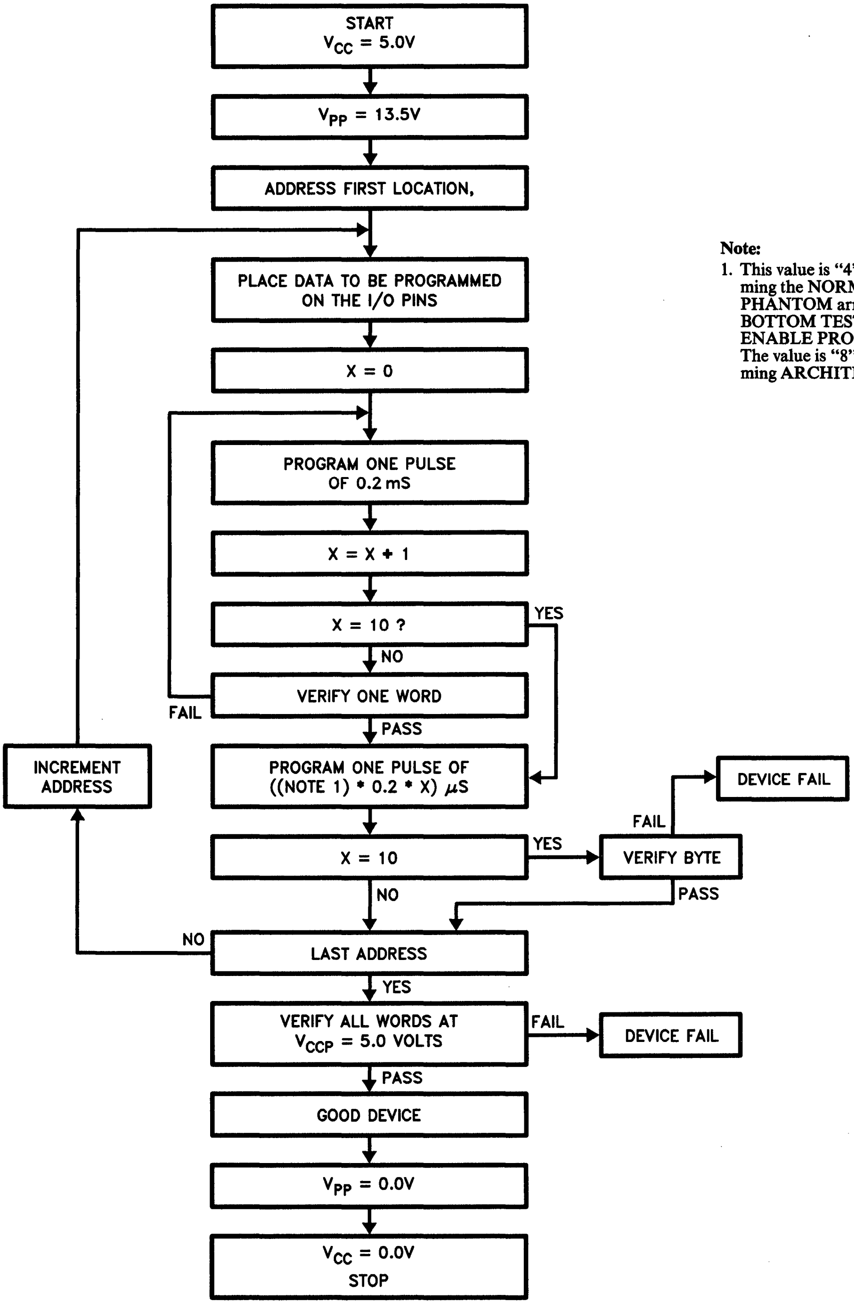
The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of V_{CC} prior to V_{PP}, and removal of V_{PP} prior to V_{CC}. See *Figure 5* and Table 7 for specific timing and AC requirements. Notice that all programming is accomplished without switching V_{PP} on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, *Figure 4* and timing diagram *Figure 5*. After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather *Figure 5* also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.

Programming Flowchart


START
V_{CC} = 5.0V
V_{PP} = 13.5V
ADDRESS FIRST LOCATION,
PLACE DATA TO BE PROGRAMMED ON THE I/O PINS
X = 0
PROGRAM ONE PULSE OF 0.2 mS
X = X + 1
X = 10 ?
YES
NO
VERIFY ONE WORD
FAIL
PASS
INCREMENT ADDRESS
PROGRAM ONE PULSE OF ((NOTE 1) * 0.2 * X) μS
DEVICE FAIL
FAIL
X = 10
YES
VERIFY BYTE
NO
PASS
NO
LAST ADDRESS
YES
VERIFY ALL WORDS AT V_{CCP} = 5.0 VOLTS
FAIL
DEVICE FAIL
PASS
GOOD DEVICE
V_{PP} = 0.0V
V_{CC} = 0.0V
STOP

Note:

1. This value is "4" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.

0023–7

Figure 3

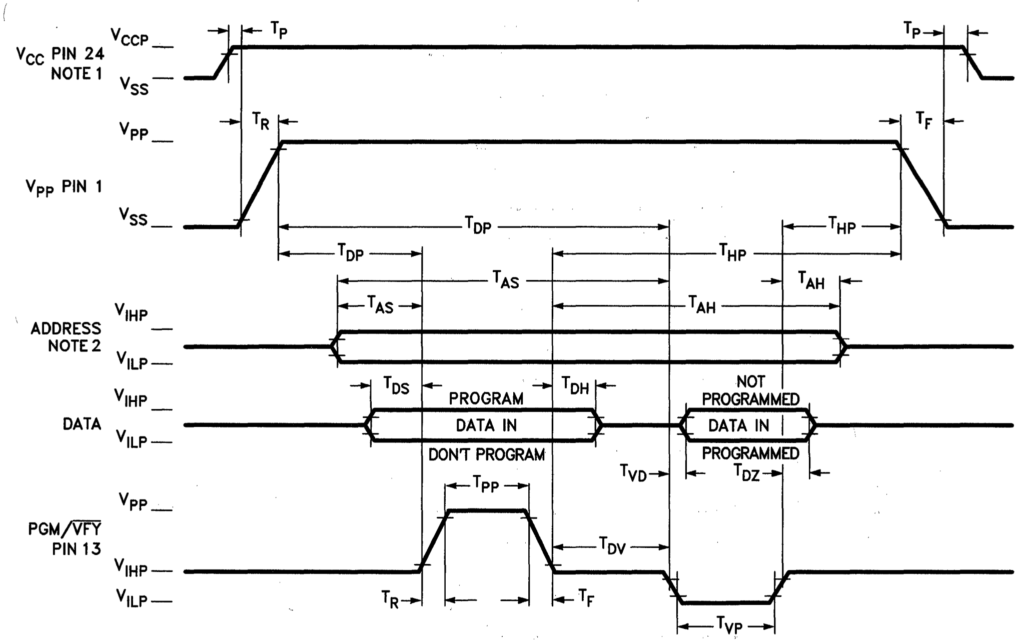
Timing Diagrams

Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 4.* ADDRESS refers to all applicable information in Tables 1 through 5 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and DATA OUT is verified on the same pins. A “1” (V_{IHP}) on an I/O pin causes the addressed location to be programmed. A “0” on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

Programming Waveforms



V_{CC} PIN 24
NOTE 1
V_{CCP}
V_{SS}
T_P
T_P
V_{PP} PIN 1
V_{PP}
V_{SS}
T_R
T_F
T_{DP}
T_{DP}
T_{HP}
T_{HP}
T_{AS}
T_{AS}
T_{AH}
T_{AH}
ADDRESS
NOTE 2
V_{IHP}
V_{ILP}
DATA
V_{IHP}
V_{ILP}
T_{DS}
PROGRAM
T_{DH}
DATA IN
DON'T PROGRAM
NOT PROGRAMMED
DATA IN
PROGRAMMED
T_{VD}
T_{DZ}
PGM/VFY
PIN 13
V_{PP}
V_{IHP}
V_{ILP}
T_{PP}
T_R
T_F
T_{DV}
T_{VP}

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Notes:

1. Power, V_{PP} & V_{CC} should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming $\overline{\text{OE}}$ Product Terms & Architecture bits, Pin 11 (A9) must go to V_{PP} and satisfy T_{AS} and T_{AN}.

Figure 4

Security Cell

The security cell is programmed independently per the timing diagram in *Figure 5*, and the information in Table 1. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the same pin. A "0" on pin 3 indicates that the security bit has been programmed, and a "1" indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after V_{PP} has been removed from pin 1.

Programming Waveforms Security Cell

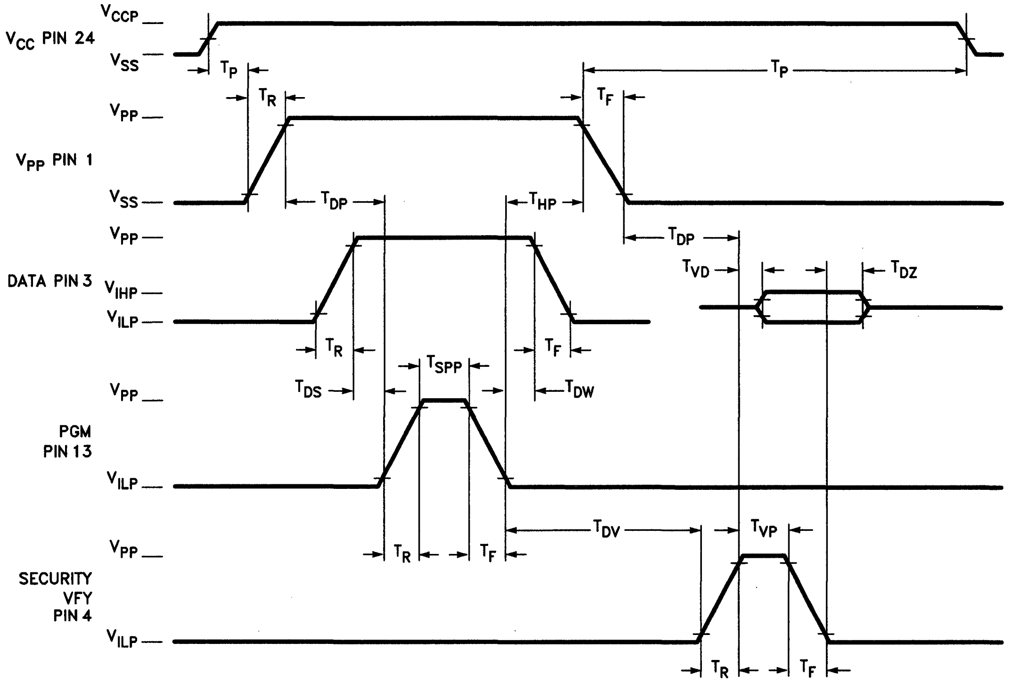

V_{CC} PIN 24
V_{CCP}
V_{SS}
T_P
T_P
T_R
T_F
V_{PP} PIN 1
V_{PP}
V_{SS}
T_{DP}
T_{HP}
T_{DP}
DATA PIN 3
V_{PP}
V_{IHP}
V_{ILP}
T_{VD}
T_{DZ}
T_R
T_F
T_{SPP}
T_{DS}
T_{DW}
PGM PIN 13
V_{PP}
V_{ILP}
T_{DV}
T_{VP}
T_R
T_F
SECURITY VFY PIN 4
V_{PP}
V_{ILP}
T_R
T_F
0023-9

Figure 5

DC Programming Parameters $T_A = 25°C$

Table 6

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	Volts
V_{CCP}	Supply Voltage During Programming	4.75	5.25	Volts
V_{IHP}	Input HIGH Voltage During Programming	3.0	V_{CCP}	Volts
V_{ILP}	Input LOW Voltage During Programming	−3.0	0.4	Volts
V_{OH}	Output HIGH Voltage	2.4		Volts
V_{OL}	Output LOW Voltage		0.4	Volts
I_{PP}	Programming Supply Current		40	mA

AC Programming Parameters

Table 7

Parameter	Description	Min.	Max.	Units
T_P	Delay to Programming Voltage	20		ms
T_{DP}	Delay to Program	1		μs
T_{HP}	Hold from Program or Verify	1		μs
$T_{R,F}$	V_{PP} Rise & Fall Time	50		ns
T_{AS}	Address Setup Time	1		μs
T_{AH}	Address Hold Time	1		μs
T_{DS}	Data Setup Time	1		μs
T_{DH}	Data Hold Time	1		μs
T_{PP}	Programming Pulsewidth	0.2	10	ms
T_{SPP}	Programming Pulsewidth for Security	50		ms
T_{DV}	Delay from Program to Verify	2		μs
T_{VD}	Delay to Data Out		1	μs
T_{VP}	Verify Pulse Width	2		μs
T_{DZ}	Verify to High Z		1	μs

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
55	25	15	15	PAL C 22V10L-25PC	P13	Commercial
				PAL C 22V10L-25WC	W14	
				PAL C 22V10L-25JC	J64	
90	25	15	15	PAL C 22V10-25PC	P13	Commercial
				PAL C 22V10-25WC	W14	
				PAL C 22V10-25JC	J64	
100	25	20	20	PAL C 22V10-25DMB	D14	Military
				PAL C 22V10-25WMB	W14	
				PAL C 22V10-25LMB	L64	
				PAL C 22V10-25QMB	Q64	
100	30	25	20	PAL C 22V10-30DMB	D14	Military
				PAL C 22V10-30WMB	W14	
				PAL C 22V10-30LMB	L64	
				PAL C 22V10-30QMB	Q64	
55	35	30	25	PAL C 22V10L-35PC	P13	Commercial
				PAL C 22V10L-35WC	W14	
				PAL C 22V10L-35JC	J64	
90	35	30	25	PAL C 22V10-35PC	P13	Commercial
				PAL C 22V10-35WC	W14	
				PAL C 22V10-35JC	J64	
100	40	35	25	PAL C 22V10-40DMB	D14	Military
				PAL C 22V10-40WMB	W14	
				PAL C 22V10-40LMB	L64	
				PAL C 22V10-40QMB	Q64	

CYPRESS
SEMICONDUCTOR

ADVANCED INFORMATION **CY7C330**

Synchronous State Machine

Features

- **6 dual macrocells having:**
  - **2 registered, three-state I/O pins**
  - **2 clock multiplexers for inputs**
  - **2 feedback multiplexers**
  - **2 OE multiplexers**
- **User configurable state flip-flops**
  - **JK, RS, T, or D**
- **11 dedicated, registered input pins**
  - **Each has a clock multiplexer**
- **3 separate clocks**
  - **2 input, 1 state**
- **12 state registers in the macrocells, can be hidden**
- **4 dedicated hidden registers**
- **256 product terms**
  - **32 per macrocell; variable distribution**
- **Common or product term OE for each I/O pin**
- **Common synchronous set and reset**
- **50 MHz operation**
  - **5 ns input setup and 15 ns clock to output**
  - **20 ns input register to state register**
- **Low power**
  - **30 mA quiescent I_{CC}**
  - **120 mA maximum I_{CC}**
- **28 pin 300 mil DIP, LCC**
- **Eraseable and reprogrammable**

Product Characteristics

The CY7C330 is a high-performance, eraseable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bi-directional I/O capability, input registers, and three separate clocks, enable the user to design high performance state machines that can communicate either with each other or with microprocessors over bi-directional parallel busses of user-definable widths.

The three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

The user-configurable state register flip-flops enable the designer to designate JK, RS, T, or D type devices, so that the number of product terms required to implement the logic are minimized.

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the six I/O macrocells and (4) the four hidden registers.

Logic Diagram

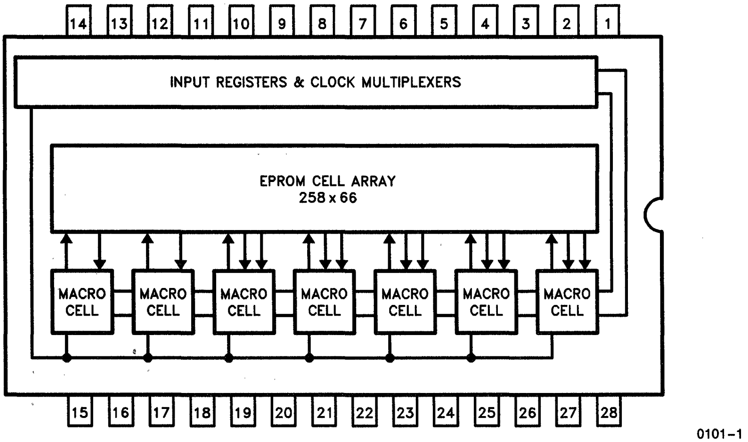


Figure 1

Selection Guide

		CY7C330-50	CY7C330-40	CY7C330-30	CY7C330-25
Maximum Operating Frequency (MHz)		50	40	30	25
Maximum Operating Current (mA)	Commercial	120		TBD	
	Military		150		TBD

Product Characteristics (Continued)

Input Registers and Clock Multiplexers

There are a total of eleven dedicated Input Registers. Each Input Register consists of a D flip-flop and a clock multiplexer. The clock multiplexer is user-programmable to select either C1 or C2 as the clock for the flip-flop. C2 and $\overline{\text{OE}}$ can alternatively be used as inputs to the array. The twenty-two outputs of the registers (i.e. the Q and $\overline{\text{Q}}$ outputs of the input registers) drive the array of EPROM cells. The details of the input registers and multiplexers are shown in *Figure 2.*

CY7C330 Macrocell

A logic diagram of the CY7C330 macrocell is shown in *Figure 3*. There are a total of six identical macrocells.

Each macrocell consists of:

Two output State Registers that are clocked by the state counter clock, CLK. The State Registers can be configured as D, JK, RS, or T flip-flops (default is a D flip-flop). Polarity can be controlled in the D flip-flop implementation. Data is sampled on the LOW to HIGH clock transition. All of the State Registers have a common, synchronous set, S, as well as a common, synchronous reset, R, which override the data at the D input. The S and R signals are PRODUCT TERMS that are generated in the EPROM cell array.

Two Macrocell Input Registers that may each be clocked by either the C1 or the C2 clock, as programmed by the user. The Macrocell Input Registers are initialized during power on such that all of the Q outputs are LOW and all of the $\overline{\text{Q}}$ outputs are HIGH.

Two (two input) Clock Multiplexers (C), which are user-programmable and select either the C1 or the C2 clock to the Macrocell Input Registers.

Two (two input) Output Enable Multiplexers ($\overline{\text{OE}}$), which are user-programmable and select either the $\overline{\text{OE}}$ signal from the pin or the $\overline{\text{OE}}$ product term from the array, on an individual basis, to enable the two output three-state drivers. Note that the $\overline{\text{OE}}$ signal to the array is clocked through an input register (*Figure 2*) using either the C1 or the C2 clock.

Two (two input) Feedback Multiplexers (FB), which are user-programmable and select either the output of the state register or the output of the macrocell input register to be fed back into the array. Note that if the output of the macrocell input register is selected by the FB multiplexer, the pin becomes bi-directional.

A single (two input) multiplexer (IN), which selects one or the other of the two macrocell input register outputs as an input to the array. This "sharing of inputs" serves two purposes. First, if one of the state registers is not needed as an output pin it can be fed back (via the FB multiplexer). This is called "hiding" the register. Second, the input multiplexer "saves the pin" because that output pin can be used as an input pin.

If the outputs of both state registers are fed back, only one of the I/O pins can be used as an input, but both may be used as outputs.

Two exclusive OR gates enable the user to configure the State Registers. The user can select the polarity of the output when the D flip-flop is configured (default) or, the user can change the D flip-flop to a JK, RS, or T flip-flop.

Hidden Registers

In addition to the six macrocells, which contain a total of twenty-four registers, there are four hidden registers whose outputs aren't brought out to the device output pins. The hidden registers are shown as two groups of two registers each in the logic diagram (*Figure 1*) and in *Figure 4.*

The four hidden registers are clocked by the same clock as the macrocell state registers. All of the hidden register flip-flops have a common, synchronous set, S, as well as a common, synchronous reset, R, which over-ride the data at the D input. The S and R signals are PRODUCT TERMS that are generated in the array and are the same signals used to preset and reset the state register flip-flops.

Macrocell Product Term Distribution

Each pair of macrocells has a total of thirty-two product terms. Two product terms of each macrocell are used for the output enables (OEs) for the two output pins. Two product terms are also used as one input to each of the two exclusive OR gates in the macrocell. The number of product terms available to the designer is then 32 − 4 = 28 for each macrocell. These product terms are divided between the two state register flip-flops as listed below.

Product Term Pairings

9	**19**
9	**19**
11	**17**
11	**17**
13	**15**
13	**15**

Hidden Register Product Term Distribution

Each pair of hidden registers also has a total of 32 product terms. Two product terms are used as one input to each of the exclusive OR gates. However, because the register outputs do not go to any output pins, output enable product terms are not required. Therefore, 30 product terms are available to the designer for each pair of hidden registers. The product term distribution for the four hidden registers is:

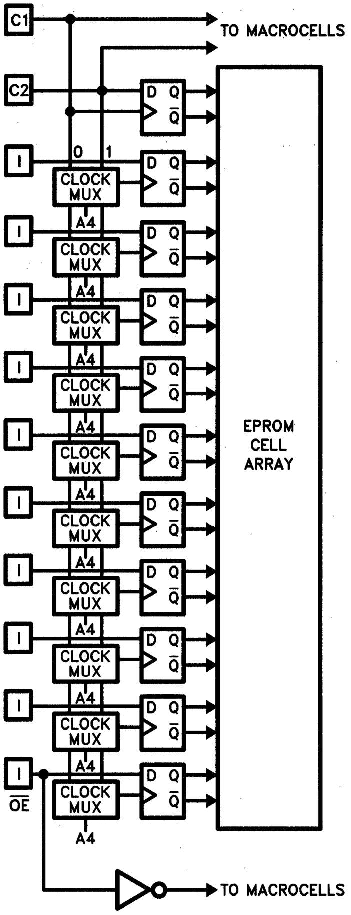
11	**19**
13	**17**

Architecture Bits

The architecture bits are used to program the multiplexers. The function of the architecture bits is outlined below.

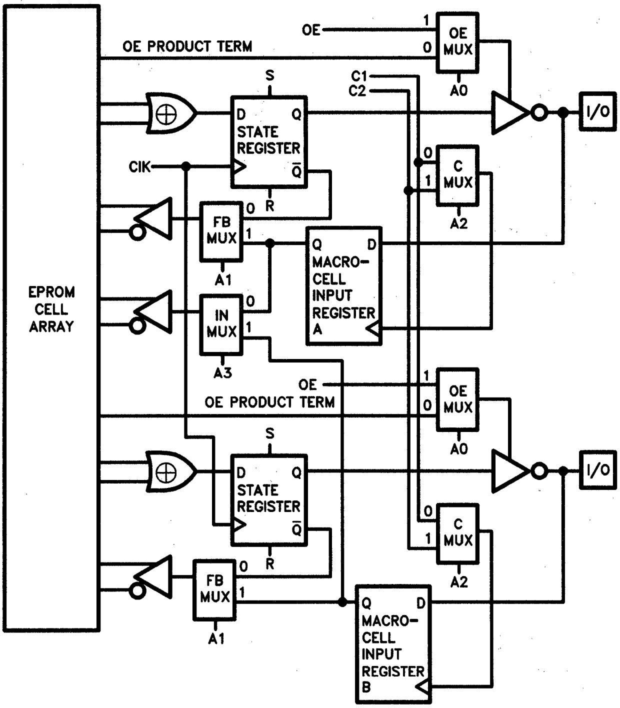
Architecture Bit	Value	Function
A0: OE Mux	0 1	$\overline{\text{OE}}$ Generated by Product Term $\overline{\text{OE}}$ from the Pin
A1: FB Mux	0 1	Feedback State Register's Output Feedback Input Register's Output
A2: C Mux	0 1	C1 to Macrocell Input Register C2 to Macrocell Input Register
A3: IN Mux	0 1	Selects Data from Input Register A Selects Data from Input Register B
A4: Clock Mux	0 1	Selects C1 to Input Register Selects C2 to Input Register

Product Characteristics (Continued)


C1
TO MACROCELLS
C2
I
0
1
CLOCK MUX
A4
D Q
Q̄
EPROM CELL ARRAY
OE
TO MACROCELLS

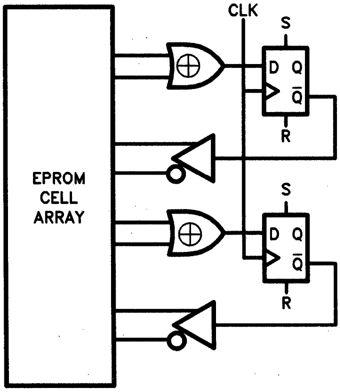
0101-2

Figure 2. Input Registers and Clock Multipliers


EPROM CELL ARRAY
OE PRODUCT TERM
OE
1
0
OE MUX
A0
S
D Q
STATE REGISTER
Q̄
R
C1
C2
CIK
I/O
C MUX
A2
FB MUX
A1
IN MUX
A3
Q D
MACRO-CELL INPUT REGISTER A
MACRO-CELL INPUT REGISTER B

0101-3

Figure 3. Macrocell


CLK
S
D Q
Q̄
R
EPROM CELL ARRAY

0101-4

Figure 4. Hidden Register Pair

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ADVANCED INFORMATION **CY7C331**

Asynchronous Registered EPLD

Features

- **6 dual MACROCELLS having:**
  - **2 registered three-state I/O pins**
  - **Independent asynchronous set/reset generated in the array**
  - **Combinatorial/Registered outputs**
  - **2 Feedback multiplexers**
  - **2 OE multiplexers**
  - **1 Input multiplexer**
  - **Parallel load for all registers**
- **12 user configurable flip-flops**
  - **JK, RS, T, or D**
- **13 dedicated input pins**
  - **1 can be used as $\overline{OE}$**
- **Common/Product term OE for each I/O pin**
- **Separate clock generation in the array**
- **192 product terms**
  - **32 per macrocell: variable distribution**
- **Security fuse**
- **25 MHz operation**
- **Low power**
  - **90 mA quiescent I_{CC}**
  - **180 mA maximum I_{CC}**
- **28 pin 300 mil DIP, LCC**
- **Eraseable and reprogrammable**

Product Characteristics

The architecture of the CY7C331, when combined with the user-configurable output macrocell, bi-directional I/O capability, separate asynchronous D flip-flop set and reset capability, and separate clock generation in the EPROM cell array provide the user with the most versatile EPLD available.

The CY7C331 consists of three major blocks; (1) the array input drivers (buffers) (2) the EPROM cell array, and the six dual Asynchronous Registered EPLD macrocells.

Input Buffers

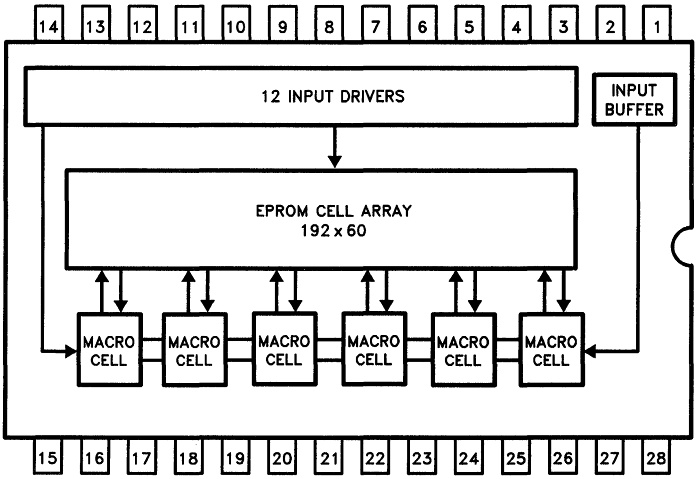
There are a total of thirteen dedicated input pins. The $\overline{PL}$ input is used exclusively for asynchronously loading the data applied to the I/O pins into the macrocell D flip-flops for testing or for initialization. The remaining twelve input pins drive the array. One pin may alternately be used as an output enable and be programmed, on an individual basis, to enable any or all of the output pins. A detailed logic diagram of the input drivers is not shown.

The CY7C331 Macrocell

There are a total of six identical macrocells in the CY7C331. Each macrocell controls two I/O pins. The State Registers can be configured by Macrocell Input Registers as D flip-flops. All flip-flops are clocked, and may be asynchronously set or reset by independent product terms that are generated in the array. When the asynchronous set and reset are both true the flip-flop becomes combinatorial. The outputs may be enabled either by a common enable or by separate array product terms. The I/O register pair may be loaded with the data on the I/O pin when the $\overline{PL}$ signal goes LOW. The same input and feedback multiplexers that are used in the CY7C330 are used in the CY7C331.

All registers are initialized at power-on such that their Q outputs are LOW and their $\overline{Q}$ outputs are HIGH.

Logic Symbol



0100-1

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION **CY7C332**

Combinatorial Registered EPLD

Features

- **6 dual macrocells having:**
  - **— 2 combinational, three-state I/O pins with feedback**
  - **— 2 OE multiplexers**
  - **— 2 macrocell input registers**
- **12 dedicated inputs**
  - **— Each may be programmed to be registered or combinatorial**
- **Programmable output polarity**
- **192 product terms**
  - **— 32 per macrocell; variable distribution**
- **Common or product term OE for each I/O pin**
- **Power-on initialization of all input registers**
- **Security fuse**
- **40 MHz operation**
- **Low power**
  - **— 90 mA quiescent I_{CC}**
  - **— 180 mA maximum I_{CC}**
- **28 pin 300 mil DIP, LCC**
- **Eraseable and reprogrammable**

Product Characteristics

The architecture of the CY7C332, combined with the user-configurable registered or un-registered inputs, bi-directional I/O capability, user-programmable output enable multiplexers, and the large number of variable product terms provide the user with one of the most powerful EPLD's available.

The CY7C332 consists of three major blocks; (1) the array input registers and drivers (input macrocell), (2) the EPROM cell array, and (3) the six dual I/O macrocells.

Input Macrocells

There are a total of thirteen dedicated input pins. Each input pin may be programmed to be registered or combinatorial. The CI input is used exclusively for synchronously loading the data into the input macrocell D flip-flops if the input is programmed to be registered. Twelve input pins drive the array with true and complement polarity signals. One pin may be alternately used as an output enable, and can be programmed, on an individual basis, to enable any or all of the output pins.

I/O Macrocell

There are a total of six identical dual macrocells. Each macrocell controls two I/O pins. The macrocells consist of:

Two (two-input) Output Enable Multiplexers (OE), which are user-programmable and select either the $\overline{\text{OE}}$ signal from the pin or the $\overline{\text{OE}}$ product term from the array, on an individual basis, to enable the two output three-state drivers. Note that the $\overline{\text{OE}}$ signal to the array can be clocked through an input macrocell using CI.

Each output is fed back into the array so that if the output is not required the pin may be used as an un-registered input.

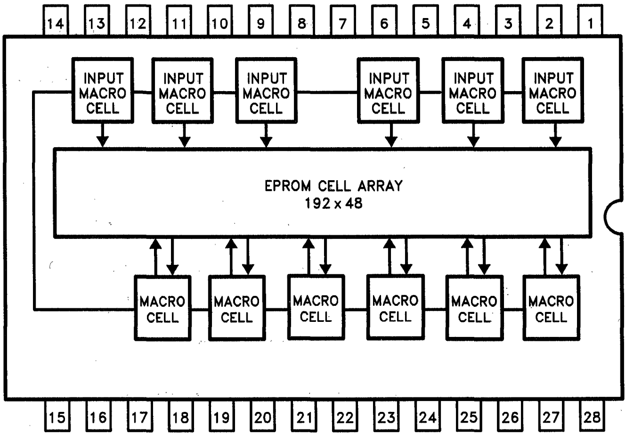
The polarity of the output signal may be selected by the user, on an individual basis, by programming the EPROM cell corresponding to the lower input of an exclusive OR gate.

Produce Term Distribution

Each pair of macrocells will have 32 product terms. The proposed distribution is (A/B/$\overline{\text{OE}}$); 20/10/2, 18/12/2, 15/15/2, 15/15/2, 12/18/2, 10/20/2.

The total number of products terms is 32 × 6 = 192.

Logic Symbol



0104-1

PLD Programming Information

Introduction

PLDs or Programmable Logic Devices provide an attractive alternative to logic implemented with discrete devices. Because the primary requirements for this logic has been to provide high performance and increased functional density, in the past all programmable logic functions have been implemented in a bipolar technology. Bipolar technology uses a fuse for the programming mechanism. The fuses are intact when the product is delivered to the user, and may be programmed once, then read and used indefinitely. The fuses are literally blown using a high current supplied by a programming system. Programming or blowing a fuse is a one time event, once blown the fuse is forever open. A fuse therefore may not be tested to see that it will blow or program properly before it is delivered to the user. This difficulty in testing fuses for programming results in less than 100% programming yield in the field, and this fallout falls into three categories.

A certain percentage of the product simply fails to program. These devices are easily identified, and may be returned for replacement. A small percentage of the product will program and verify correctly, but fail to function properly as a logic element. This can happen because, without programming each location, the connection between the programmed cell and the logic it is to control cannot be verified. Some programmers can test for this condition through the use of a set of test vectors for each unique code or part. Additional material will be lost, however, even if a structured set of test vectors is used due to the device functioning too slow. This failure is much more subtle and can only be found by 100% AC testing of the programmed device, or worse yet by troubleshooting an assembled board or system.

Cypress PLDs use an EPROM programming mechanism. This technology has been available since the early 1970's, however, as with most MOS technologies, the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM programming, offers a viable alternative to bipolar programmable logic from a performance point of view. In addition, CMOS EPROM technology offers two other overwhelming advantages. EPROM cells are programmed by injecting charge on an electrically isolated gate which causes the transistor to be permanently turned off. This mechanism may be reversed by irradiating the cell with ultraviolet light. This feature totally changes the testing philosophy and provides a new feature for the user. All programmable cells may now be tested by the manufacturer prior to delivery to the customer. This provides an easy methodology to certify programming, functionality, and performance. With built in test arrays, functionality and performance may be tested even if the device is packaged in a non-windowed package. Devices packaged in a windowed package may be programmed and erased indefinitely providing the designer a tool for the development of his logic without throwing away devices that are programmed incorrectly as the design proceeds.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

Programming Algorithm

Byte Addressing and Programming

All Cypress Programmable Logic Devices are addressed and programmed on BYTE or EXTENDED BYTE basis where an EXTENDED BYTE is a field that is as wide as the output path of the device. Each device or family of devices has a unique address map which is available in the product data sheet. Each BYTE or EXTENDED BYTE is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a "1" or HIGH is placed on the input pin and a "0" or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A "1" or HIGH during program verify operation indicates an unprogrammed cell, while a "0" or LOW indicates that the cell accessed has been programmed.

Blank Check

Before programming all Programmable Logic Devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a "1" or HIGH output indicates that the addressed cell is unprogrammed, while a "0" or LOW indicates a programmed cell.

Programming The Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ/WRITE pin in the programming mode. This signal causes a write operation when switched to a supervoltage, and a read operation when switched to a logic "0" or LOW. In the logic HIGH state "1" the device is in a program inhibit condition and the output pins are in a high impedance state. During a WRITE operation, the data on the output pins is written into the addressed array location. In a READ operation the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location Verification of data is accomplished by examining the information on the output pins during a READ operation.

The timing for actual programming is supplied in the unique programming specification for each device.

Phantom Operating Modes

All Cypress Programmable Logic Devices contain a PHANTOM ARRAY for the purposes of post assembly testing. This array is accessed, programmed and operated in a special PHANTOM mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the PHANTOM ARRAY is connected. In normal operation the PHANTOM ARRAY is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging, if desired by the user before programming and use. The PHANTOM modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific data sheets for details.

Special Features

Cypress Programmable Logic devices, depending on the device, have several special features. For example the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PAL C 22V10 and PLD C 20G10 the MACROCELLs are programmable through the use of the architecture bits. This allows the user to more effectively tailor the device architecture to his unique system requirements. These features are also programmed though the use of EPROM cells. Specific programming is detailed in the device data sheet.

Programming Support

Programming support for Cypress CMOS Programmable Logic Devices is available from a number of programmer manufacturers, some of which are listed as follows.

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA
98073-9746
(206) 881-6444

Data I/O 29B LOGICPAK VO4			Adapters:	
			PT	Generic
Cypress Part Number	Generic Part Number	Family Code and Pinout	303A-009 Revision	303A-011A/B Revision
PALC16R8	16R8[1]	28 24	V02	V01
PALC16R6	16R6[1]	28 24	V02	V01
PALC16R4	16R4[1]	28 24	V02	V01
PALC16L8	16L8[1]	28 17	V02	V01
PALC22V10	22V10[2]	28 28	V04	V01
PALC22V10	22V10[3]	28 83	V04	V01
PLDC20G10	20G10[2]	28 56	V04	V01
PLDC20G10	20G10[3]	28 69	V04	V01
PLDC20G10	20R4	28 65	V04	V01
PLDC20G10	20R6	28 66	V04	V01
PLDC20G10	20R8	28 27	V04	TBD
PLDC20G10	20L8	28 26	V04	V01
PLDC20G10	20L10	28 6	V04	V01
PLDC20G10	20L2	28 5	V04	V01
PLDC20G10	18L4	28 4	V04	V01
PLDC20G10	16L6	28 3	V04	V01
PLDC20G10	14L8	28 2	V04	V01
PLDC20G10	12L10	28 1	V04	V01

Notes:
1. Requires Design Adaptor 100.
2. Family/Pinout Code if Pin 1 is used as a clock.
3. Family/Pinout Code if Pin 1 is used as an input for fingerprinting only.

Data I/O Model 60A, 60H			
Cypress Part Number	Generic Part Number	Family Code and Pinout	Revision
PALC16R8	16R8	28 24	V05
PALC16R6	16R6	28 24	V05
PALC16R4	16R4	28 24	V05
PALC16L8	16L8	28 17	V05
PALC22V10	22V10	28 28	V05
PLDC20G10	20G10	28 56	V05

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118
STAG ZL32 Rev. 30A03

STAG PPZ Zm2200 Rev. 17 ZL32 Rev. 30A03		
Cypress Part Number	Generic Part Number	Family Code and Pinout
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Cypress Semiconductor Inc.
3901 North First Street
San Jose, CA 95134
(408) 943-2600

Cypress CY3000 QuickPro Rev. PLD 2.0

Cypress Part Number	Generic Part Number	Family Code and Pinout
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	
PLDC20G10	20G10	
PLDC20G10	20R4	
PLDC20G10	20R6	
PLDC20G10	20R8	
PLDC20G10	20L8	
PLDC20G10	20L10	
PLDC20G10	20L2	
PLDC20G10	18L4	
PLDC20G10	16L6	
PLDC20G10	14L8	
PLDC20G10	12L10	

Digelec Corporation
1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
(201) 493-2420

DIGELEC 803 FAM-52 Rev. A-6.0

Cypress Part Number	Generic Part Number	Family Code and Pinout	Adapter Rev. A-3
PALC16R8	16R8	Menu Driven	DA-53
PALC16R6	16R6		DA-53
PALC16R4	16R4		DA-53
PALC16L8	16L8		DA-53
PALC22V10	22V10		DA-53

Logical Devices Inc.
1321 N.W. 65th Place
Ft. Lauderdale, FL 33309
(305) 974-0975

Logical Devices ALLPRO Rev. V1.4

Cypress Part Number	Generic Part Number	Family Code and Pinout
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Kontron Electronics
1230 Charleston Road
Mountain View, CA
94039-7230
(415) 965-7020

Kontron EPP 80 UPM-P

Cypress Part Number	Generic Part Number	Family Code and Pinout
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Development Software	**Supported Devices:**
ABEL™	PALC16R8
Data I/O Corporation	PALC16R6
10525 Willows Rd. N.E.	PALC16R4
P.O. Box 97046	PALC16L8
Redmond, WA	PALC22V10
98073-9746	PLDC20G10
(206) 881-6444	
CUPL™	PALC16R8
Assisted Technology	PALC16R6
1290 Parkmoor Ave.	PALC16R4
San Jose, CA 95126	PALC16L8
(800) 523-5207	PALC22V10
(800) 628-8748 CA	
LOGIC	PALC16R8
ISDATA Gmbh	PALC16R6
Haid-und-Neu-Strasse 7	PALC16R4
D-7500 Karlsruhe 1 West Germany	PALC16L8
(0721) 69 30 92	PALC22V10

ABEL™ is a trademark of Data I/O Corporation.

CUPL™ is a trademark of Assisted Technology.

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PROMS 3

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LOGIC

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CYPRESS SEMICONDUCTOR

CY2901C

CMOS Four-Bit Slice

Features

- **Pin compatible and functional equivalent to AMD AM2901C**
- **Low power**
- **V_{CC} margin**
  - **5V ±10%**
  - **All parameters guaranteed over commercial and military operating temperature range**
- **Eight function ALU**
  Performs eight operations on two 4-bit operands
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Four status flags**
  Carry, overflow, negative, zero
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage

Functional Description

The CY2901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY2901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY2901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

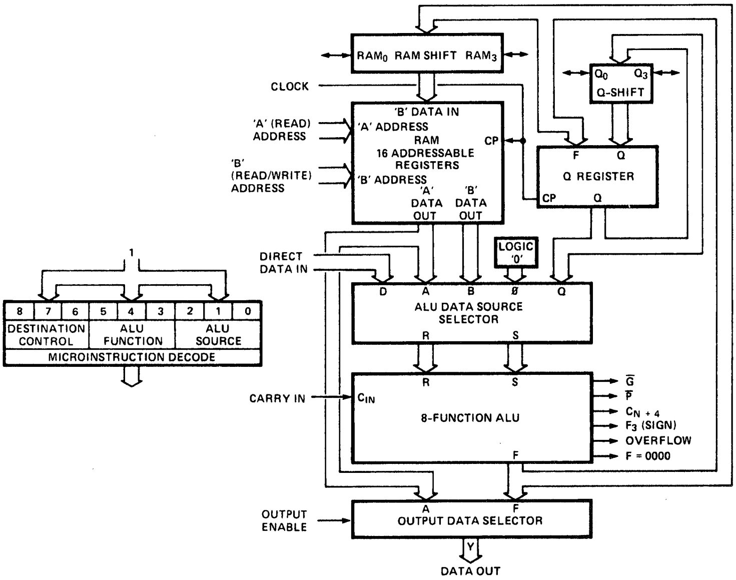
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from an instruction register.

The CY2901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full-look ahead carry or a ripple carry.

The CY2901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY2901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance at a low power dissipation.

Logic Block Diagram


RAM₀ RAM SHIFT RAM₃
CLOCK
'B' DATA IN
'A' (READ) ADDRESS
'A' ADDRESS
RAM
16 ADDRESSABLE REGISTERS
CP
'B' (READ/WRITE) ADDRESS
'B' ADDRESS
'A' 'B'
DATA DATA
OUT OUT
Q₀ Q₃
Q-SHIFT
F Q
Q REGISTER
CP Q
LOGIC '0'
DIRECT DATA IN
D A B 0 Q
ALU DATA SOURCE SELECTOR
R S
I
8 7 6 5 4 3 2 1 0
DESTINATION CONTROL
ALU FUNCTION
ALU SOURCE
MICROINSTRUCTION DECODE
CARRY IN
C_IN
8-FUNCTION ALU
R S
F
G
P
C_N + 4
F₃ (SIGN)
OVERFLOW
F = 0000
OUTPUT ENABLE
A F
OUTPUT DATA SELECTOR
Y
DATA OUT

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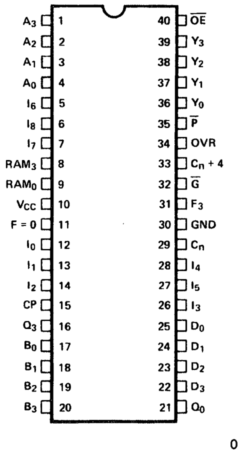
Pin Configuration

Top View


A₃ 1
A₂ 2
A₁ 3
A₀ 4
I₆ 5
I₈ 6
I₇ 7
RAM₃ 8
RAM₀ 9
V_CC 10
F = 0 11
I₀ 12
I₁ 13
I₂ 14
CP 15
Q₃ 16
B₀ 17
B₁ 18
B₂ 19
B₃ 20
40 OE
39 Y₃
38 Y₂
37 Y₁
36 Y₀
35 P
34 OVR
33 Cₙ + 4
32 G
31 F₃
30 GND
29 Cₙ
28 I₄
27 I₅
26 I₃
25 D₀
24 D₁
23 D₂
22 D₃
21 Q₀

0007-2

Selection Guide See last page for ordering information.

Read Modify-Write Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
31	140	Commercial	CY2901C
32	180	Military	CY2901C

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 10 to Pin 30)	−0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	−0.5V to +7.0V
DC Input Voltage	−3.0V to +7.0V
Output Current into Outputs (Low)	30 mA
Static Discharge Voltage (Per MIL-STD-883 Method 3015.2)	>2001V
Latchup Current (Outputs)	>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Pin Definitions

Signal Name	I/O	Description
A_0–A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0–B_3	I	These 4 address lines select one of the registers in the stack and output is contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0–I_8	I	These 9 instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$) and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
D_0–D_3	I	These are 4 data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
Y_0–Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the Y_0–Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock Input. The LOW level of the clock writes data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.
Q_3 RAM_3 (Cont.)	I/O	**Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM 3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}, \overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4 bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open collector output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 20 mA Commercial I_{OL} = 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = V_{CC}			10	μA
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = GND			−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{OH} = 2.4V		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	Commercial Military	20 16		mA mA
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = GND to V_{CC}		−40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V		−30	−85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial Military		140 180	mA mA

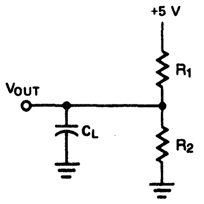
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f= 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

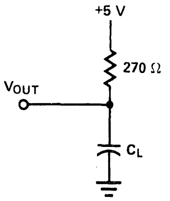
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested on a sample basis.

Output Loads used for AC Performance Characteristics



0007-3

All outputs except open drain



0007-4

Open drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.
3. Loads shown above are for commercial (20 mA) I_{OL} specifications only.

	Commercial	Military
R_1	203Ω	252Ω
R_2	148Ω	174Ω

CY2901C Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See previous page for loading circuit information.

This data applies to parts with the following numbers:
CY2901CPC CY2901CDC CY2901CLC

Cycle Time and Clock Characteristics

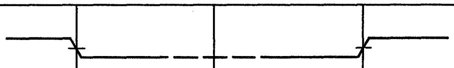
CY2901-	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	31 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	31 ns

For faster performance see CY7C901-23 specification.

Combinational Propagation Delays. $C_L = 50$ pF

To Output From Input	Y	F_3	$C_n + 4$	$\overline{G}, \overline{P}$	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A, B Address	40	40	40	37	40	40	40	—
D	30	30	30	30	38	30	30	—
C_n	22	22	20	—	25	22	25	—
I_{012}	35	35	35	37	37	35	35	—
I_{345}	35	35	35	35	38	35	35	—
I_{678}	25	—	—	—	—	—	26	26
A Bypass ALU (I = 2XX)	35	—	—	—	—	—	—	—
Clock ↑	35	35	35	35	35	35	35	28

Set-up and Hold Times Relative to Clock (CP) Input

Input	CP: 			
	Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	1 (Note 3)	30, 15 + t_{PWL} (Note 4)	1
B Destination Address	15	← Do Not Change	→	1
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0,3}, Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	23	23

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

CY2901C Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" of this data sheet for loading circuit information.

This data applies to parts with the following numbers:

CY2901CDMB

Cycle Time and Clock Characteristics

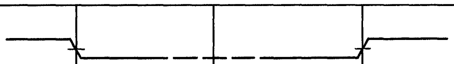
CY2901-	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	32 ns

For faster performance see CY7C901-27 specification.

Combinational Propagation Delays $C_L = 50$ pF

To Output / From Input	Y	F_3	$C_n + 4$	$\overline{G}, \overline{P}$	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A, B Address	48	48	48	44	48	48	48	—
D	37	37	37	34	40	37	37	—
C_n	25	25	21	—	28	25	28	—
I_{012}	40	40	40	44	44	40	40	—
I_{345}	40	40	40	40	40	40	40	—
I_{678}	29	—	—	—	—	—	29	29
A Bypass ALU (I = 2XX)	40	—	—	—	—	—	—	—
Clock ↑	40	40	40	40	40	40	40	33

Set-up and Hold Times Relative to Clock (CP) Input

	CP: 			
Input	Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	2 (Note 3)	30, 15 + t_{PWL} (Note 4)	2
B Destination Address	15	← Do Not Change	→	2
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0,3}, Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	25	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

Ordering Information

Read Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
31	CY2901CPC	P17	Commercial
31	CY2901CDC	D18	Commercial
32	CY2901CDMB	D18	Military

CYPRESS SEMICONDUCTOR

CY2909A
CY2911A

CMOS Micro Program Sequencers

Features

- **Fast**
  - **— CY2909A/11A has a 40 ns (min.) clock to output cycle time; commercial**
  - **— CY2909/11 has a 40 ns (min.) clock to output cycle time; military**
- **Low power**
  - **— I_{CC} (max.) = 70 mA commercial**
  - **— I_{CC} (max.) = 90 mA military**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Expandable**
  Infinitely expandable in 4-bit increments
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2909A/AM2911A**

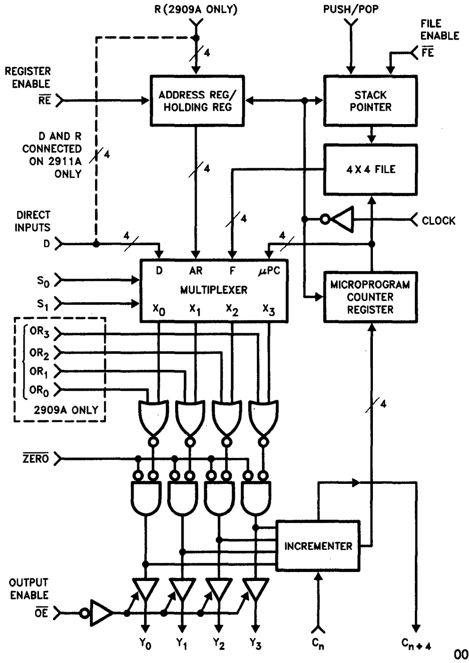
Description

The CY2909A and CY2911A are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY2909A can select an address from any of four sources. They are: 1) a set of four external direct inputs (D_i); 2) external data stored in an internal register (R_i); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be OR'ed with an external input for conditional skip or branch instructions. A $\overline{\text{ZERO}}$ input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable ($\overline{\text{OE}}$) input.

The CY2911A is an identical circuit to the CY2909A, except the four OR inputs are removed and the D and R inputs are tied together. The CY2911A is available in a 20-pin, 300-mil package. The CY2909 is available in a 28-pin, 600-mil package.

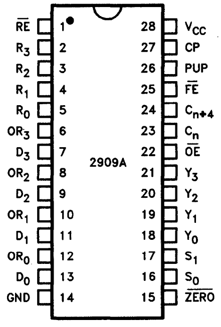
Logic Block Diagram



R (2909A ONLY)
PUSH/POP
FILE ENABLE
FE
REGISTER ENABLE
RE
ADDRESS REG/ HOLDING REG
STACK POINTER
D AND R CONNECTED ON 2911A ONLY
4X4 FILE
CLOCK
DIRECT INPUTS
D
4
D AR F μPC
MULTIPLEXER
X0 X1 X2 X3
S0
S1
MICROPROGRAM COUNTER REGISTER
OR3
OR2
OR1
OR0
2909A ONLY
ZERO
INCREMENTER
OUTPUT ENABLE
OE
Y0 Y1 Y2 Y3
Cn
Cn+4

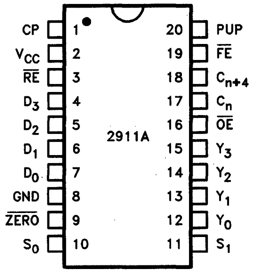
0066-1

Pin Configurations



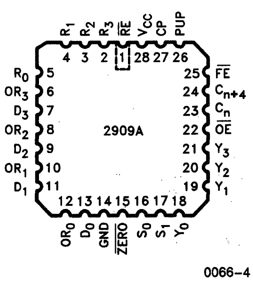
RE 1
R3 2
R2 3
R1 4
R0 5
OR3 6
D3 7
OR2 8
D2 9
OR1 10
D1 11
OR0 12
D0 13
GND 14
2909A
28 VCC
27 CP
26 PUP
25 FE
24 Cn+4
23 Cn
22 OE
21 Y3
20 Y2
19 Y1
18 Y0
17 S1
16 S0
15 ZERO

0066-2



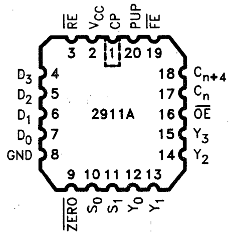
CP 1
VCC 2
RE 3
D3 4
D2 5
D1 6
D0 7
GND 8
ZERO 9
S0 10
2911A
20 PUP
19 FE
18 Cn+4
17 Cn
16 OE
15 Y3
14 Y2
13 Y1
12 Y0
11 S1

0066-3



R1 R2 R3 RE VCC CP PUP
4 3 2 1 28 27 26
R0 5
OR3 6
D3 7
OR2 8
D2 9
OR1 10
D1 11
2909A
25 FE
24 Cn+4
23 Cn
22 OE
21 Y3
20 Y2
19 Y1
12 13 14 15 16 17 18
OR0 D0 GND ZERO S0 S1 Y0

0066-4



RE VCC CP PUP FE
3 2 1 20 19
D3 4
D2 5
D1 6
D0 7
GND 8
2911A
18 Cn+4
17 Cn
16 OE
15 Y3
14 Y2
9 10 11 12 13
ZERO S0 S1 Y0 Y1

0066-5

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V
Output Current, into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.6 mA (Comm.)		2.4		V
		V_{CC} = Min., I_{OH} = −1.0 mA (Mil.)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−20	+20	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max.	V_{OUT} = GND	−30	−85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70	mA
			Military		90	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

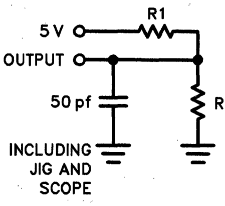
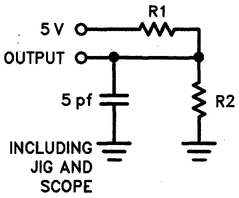
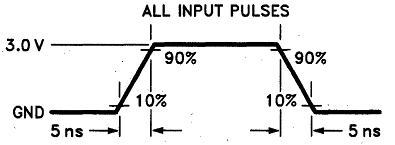


Figure 1a



0066-6

Figure 1b



0066-7

Figure 2

	Commercial	Military
R_1	254Ω	258Ω
R_2	187Ω	216Ω

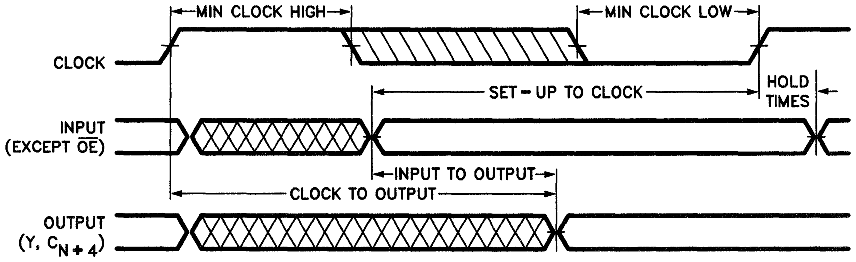
Switching Characteristics Over Operating Range

	2909A 2911A		2909A 2911A		Units
	Commercial		Military		
Minimum Clock Low Time	20		20		ns
Minimum Clock High Time	20		20		ns
MAXIMUM COMBINATIONAL PROPAGATION DELAYS					
From Input To:	Y	$C_N + 4$	Y	$C_N + 4$	ns
D_i	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_i CY2909A	17	22	20	25	ns
C_N	—	14	—	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ Low to Output	25	—	25	—	ns
$\overline{OE}$ High to High Z[3]	25	—	25	—	ns
Clock High, S_0, S_1 = LH	39	44	45	50	ns
Clock High, S_0, S_1 = LL	39	44	45	50	ns
Clock High, S_0, S_1 = HL	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)					
From Input	**Set-up**	**Hold**	**Set-up**	**Hold**	
$\overline{RE}$	19	4	19	5	ns
R_i [4]	10	4	12	5	ns
Push/Pop	25	4	27	5	ns
FE	25	4	27	5	ns
C_N	18	4	18	5	ns
D_i	25	0	25	0	ns
OR_i (CY2909A)	25	0	25	0	ns
S_0, S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

Notes:

3. Output Loading as in *Figure 1b.*
4. R_i and D_i are internally connected on the CY2911A. Use R_i set-up and hold times for D_i inputs.

Switching Waveforms


MIN CLOCK HIGH
MIN CLOCK LOW
CLOCK
SET-UP TO CLOCK
HOLD TIMES
INPUT (EXCEPT $\overline{OE}$)
INPUT TO OUTPUT
CLOCK TO OUTPUT
OUTPUT (Y, C_{N+4})

0066-8

Ordering Information

Ordering Code	Package Type	Operating Range
CY2909APC	P15	Commercial
CY2909ADC	D16	
CY2909ALC	L64	
CY2909ADMB	D16	Military
CY2909ALMB	L64	

Ordering Code	Package Type	Operating Range
CY2911APC	P5	Commercial
CY2911ADC	D6	
CY2911ALC	L61	
CY2911ADMB	D6	Military
CY2911ALMB	L61	

CYPRESS SEMICONDUCTOR

CY2910A

CMOS Microprogram Controller

Features

- **Fast**
  - **— CY2910AC has a 50 ns (min.) clock cycle; commercial**
  - **— CY2910AM has a 51 ns (min.) clock cycle; military**
- **Low power**
  - **— I_{CC} (max.) = 170 mA**
- **V_{CC} Margin 5V ±10% commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), branch address bus, 9-word stack, internal holding register**
- **Internal 9-word by 12-bit stack The internal stack can be used for subroutine return address or data storage**
- **12-bit Internal loop counter**
- **ESD protection Capable of withstanding over 2000 volts static discharge voltage**
- **Pin compatible and functional equivalent to Am2910A**

Functional Description

The CY2910A is a stand-alone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

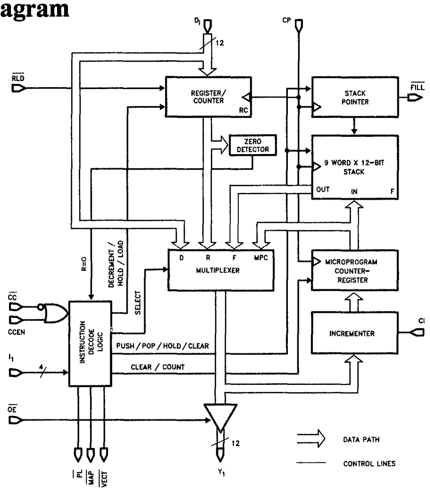
The CY2910A, as illustrated in the block diagram, consists of a 9-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY2910A is a pin compatible, functional equivalent, improved performance replacement for the Am2910A.

The CY2910A is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

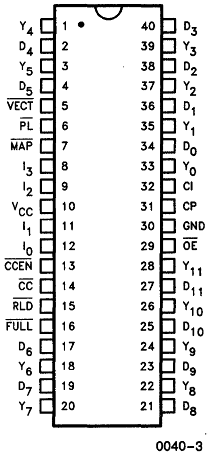
Logic Block Diagram



D_I
12
CP
RLD
REGISTER/ COUNTER
RC
STACK POINTER
FILL
ZERO DETECTOR
9 WORD X 12-BIT STACK
OUT
IN
F
R=0
DECREMENT / HOLD / LOAD
SELECT
D
R
F
MPC
MULTIPLEXER
MICROPROGRAM COUNTER-REGISTER
CC
CCEN
I_I
4
INSTRUCTION DECODE LOGIC
PUSH / POP / HOLD / CLEAR
CLEAR / COUNT
INCREMENTER
CI
OE
12
Y_I
PL
MAP
VECT
DATA PATH
CONTROL LINES

0040-2

Pin Configuration



Y4 1
D4 2
Y5 3
D5 4
VECT 5
PL 6
MAP 7
I3 8
I2 9
VCC 10
I1 11
I0 12
CCEN 13
CC 14
RLD 15
FULL 16
D6 17
Y6 18
D7 19
Y7 20
40 D3
39 Y3
38 D2
37 Y2
36 D1
35 Y1
34 D0
33 Y0
32 CI
31 CP
30 GND
29 OE
28 Y11
27 D11
26 Y10
25 D10
24 Y9
23 D9
22 Y8
21 D8

0040-3

Top View

Selection Guide

Clock Cycle (Min.) in ns	Stack Depth	Operating Range	Part Number
50	9 words	Commercial	CY2910AC
51	9 words	Military	CY2910AM

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current (Outputs).................. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{IH} = 2.4V	−1.6		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.5V	8		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND/V_{CC}	 −40	+40 	μA μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	V_{CC} = Max.		170	mA

Capacitance[2]

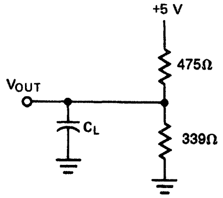
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
2. Tested on a sample basis.

Output Load for AC Performance Characteristics

All Outputs



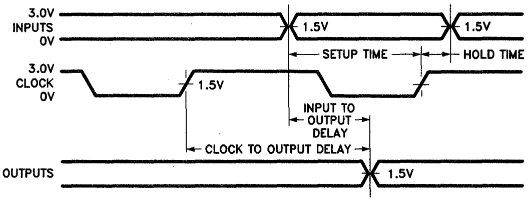
0040-4

Notes:

C_L = 50 pF includes scope probe, writing and stray capacitance.

C_L = 5 pF for output disable tests.

Switching Waveforms



0040-5

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY2910A over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements (Note 1)

	Commercial	Military
Minimum Clock LOW	20	25
Minimum Clock HIGH	20	25
Minimum Clock Period I = 14	50	51
Minimum Clock Period I = 8, 9, 15 (Note 2)	50	50

Combinational Propagation Delays. $C_L = 50$ pF

To Output	Commercial			Military		
From Input	Y	$\overline{PL}, \overline{VECT}, \overline{MAP}$	$\overline{FULL}$	Y	$\overline{PL}, \overline{VECT}, \overline{MAP}$	$\overline{FULL}$
D0–D11	20	—	—	25	—	—
I0–I3	35	30	—	40	35	—
$\overline{CC}$	30	—	—	36	—	—
$\overline{CCEN}$	30	—	—	36	—	—
CP I = 8, 9, 15 (Note 2)	40	—	31	—	—	35
CP All Other I	40	—	31	46	—	35
$\overline{OE}$ (Note 3)	25 27	—	—	25 30	—	—

Minimum Set-up and Hold Times Relative to clock LOW to HIGH Transition. $C_L = 50$ pF

	Commercial		Military	
Input	Set-up	Hold	Set-up	Hold
DI → RC	16	0	16	0
DI → MPC	30	0	30	0
I0–I3	35	0	38	0
$\overline{CC}$	24	0	35	0
$\overline{CCEN}$	24	0	35	0
CI	18	0	18	0
$\overline{RLD}$	19	0	20	0

Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.
2. These instructions are dependent upon the register/counter. Use the shorter delay times if the previous instruction either does not change the register/counter or could only decrement it. Use the longer delay if the instruction prior to the clock was 4 or 12 or if $\overline{RLD}$ was LOW.
3. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with $C_L = 5$ pF.

Table of Instructions

I_3–I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	RESULT					
				FAIL $\overline{CCEN}$ = L and $\overline{CC}$ = H		PASS $\overline{CCEN}$ = H or $\overline{CC}$ = L		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 1)	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	POP	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

Notes:

1. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load.

H = HIGH L = LOW X = Don't Care

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
50	CY2910ADC	D18	Commercial
	CY2910AJC	J67	
	CY2910ALC	L67	
	CY2910APC	P17	
51	CY2910ADMB	D18	Military
	CY2910ALMB	L67	

CYPRESS
SEMICONDUCTOR

CY3341

64 x 4 FIFO Serial Memory

Features

- **1.2/2 MHz data rate**
- **Fully TTL compatible**
- **Independent asynchronous inputs and outputs**
- **Direct replacement for PMOS 3341**
- **Expandable in word length and width**
- **CMOS for optimum speed/ power**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

The 3341 is a 64-word x 4-bit First-In First-Out (FIFO) Serial Memory. The inputs and outputs are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

Control signals are provided for both vertical and horizontal expansion.

The 3341 is manufactured using Cypress CMOS technology and is available in both ceramic and plastic packages.

Data Input

The four bits of data on the D_0 through D_3 inputs are entered into the first location when both Input Ready (IR) and Shift In (SI) are HIGH. This causes IR to go LOW but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus, data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

Data Output

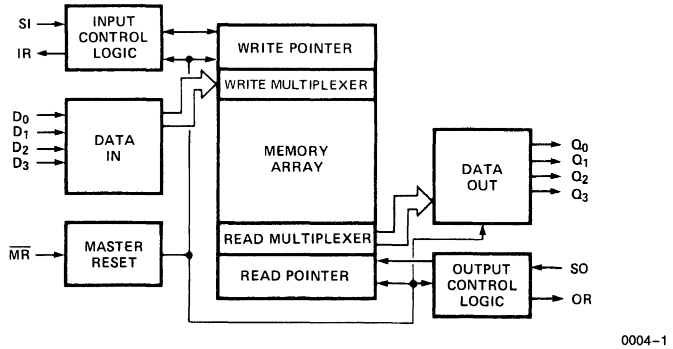
When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BT}) or completely empty (Output Ready stays LOW for at least t_{BT}).

Reset

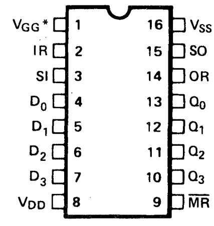
When Master Reset ($\overline{MR}$) goes LOW, the control logic is cleared, and the data outputs enter a LOW state. When $\overline{MR}$ returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW.

Logic Block Diagram



0004-1

Pin Configuration



0004-2

*Internally not connected

Selection Guide

		3341	3341-2
Maximum Operating Frequency		1.2 MHz	2.0 MHz
Maximum Operating Current (mA)	Commercial	45	45
	Military	60	60

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 16 to Pin 8)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Commercial	0°C to +70°C	5V ±10%	GND	NC
Military	−55°C to +125°C	5V ±10%	GND	NC

*Internally Not Connected.

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{SS} = Min., I_{OH} = −0.3 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{SS} = Min., I_{OL} = 1.6 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{SS}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{DD} \leq V_I \leq V_{SS}$		−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{SS} = Max., V_{OUT} = V_{DD}			−90	mA
I_{DD}	Power Supply Current	V_{SS} = Max., I_{OUT} = 0 mA	Commercial		45	mA
			Military		60	
I_{GG}	V_{GG} Current				0	mA

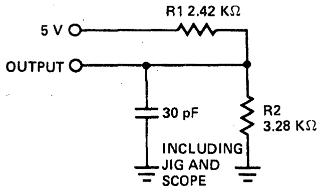
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{SS} = 5.0V	10	

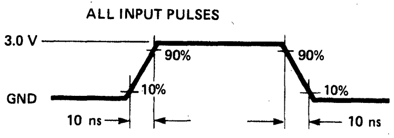
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms



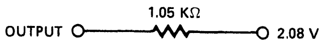
0004-3



0004-5

Equivalent to:

THÉVENIN EQUIVALENT



0004-4

Switching Characteristics Over the Operating Range[3]

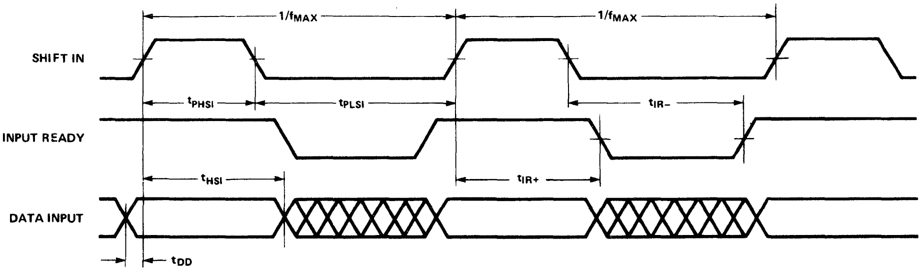
Parameters	Description	Test Conditions	3341		3341-2		Units
			Min.	Max.	Min.	Max.	
f_{MAX}	Operating Frequency	Note 4		1.2		2	MHz
t_{PHSI}	SI HIGH Time		80		80		ns
t_{PLSI}	SI LOW Time		80		80		ns
t_{DD}	Data Setup to SI		0		0		ns
t_{HSI}	Data Hold from SI		200		100		ns
t_{IR+}	Delay, SI HIGH to IR LOW		20	350	20	160	ns
t_{IR-}	Delay, SI LOW to IR HIGH		20	450	20	200	ns
t_{PHSO}	SO HIGH Time		80		80		ns
t_{PLSO}	SO LOW Time		80		80		ns
t_{OR+}	Delay, SO HIGH to OR LOW		20	370	20	160	ns
t_{OR-}	Delay, SO LOW to OR HIGH		20	450	20	200	ns
t_{DA}	Data Setup to OR HIGH		0		0		ns
t_{DH}	Data Hold from OR LOW		75		20		ns
t_{BT}	Bubble through Time			1000		500	ns
t_{MRW}	$\overline{MR}$ Pulse Width		400		200		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		30		30		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			400		200	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			400		200	ns

Notes:

3. Test conditions assume signal transitions of 10 ns or less. Timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. $1/f_{MAX} > t_{PHSI} + t_{IR-}$, $1/f_{MAX} > t_{PHSO} + t_{OR-}$.

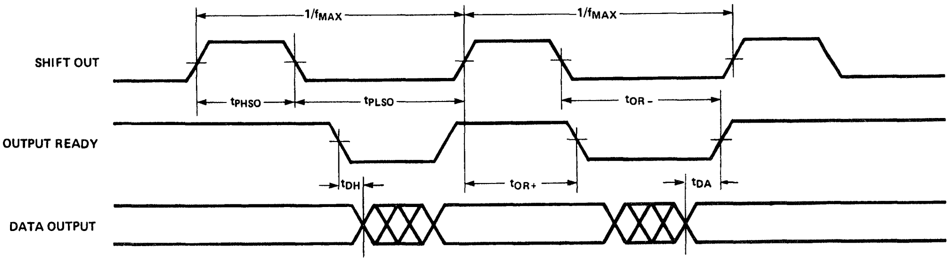
Switching Waveforms

Data In Timing Diagram


1/fMAX
1/fMAX
SHIFT IN
tPHSI
tPLSI
tIR−
INPUT READY
tHSI
tIR+
DATA INPUT
tDD

0004–6

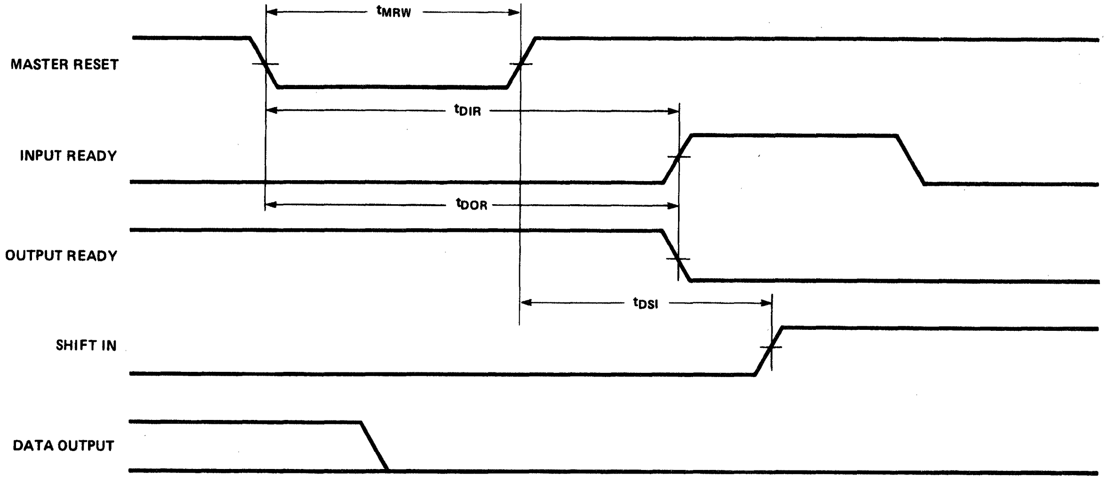
Data Out Timing Diagram


1/fMAX
1/fMAX
SHIFT OUT
tPHSO
tPLSO
tOR−
OUTPUT READY
tDH
tOR+
tDA
DATA OUTPUT

0004–7

Switching Waveforms (Continued)

Master Reset Timing Diagram


tMRW
MASTER RESET
tDIR
INPUT READY
tDOR
OUTPUT READY
tDSI
SHIFT IN
DATA OUTPUT

0004–8

Ordering Information

Ordering Code (1.2 MHz)	Package Type	Operating Range
CY3341PC CY3341DC	P1 D2	Commercial
CY3341DMB	D2	Military

Ordering Code (2 MHz)	Package Type	Operating Range
CY3341-2PC CY3341-2DC	P1 D2	Commercial
CY3341-2DMB	D2	Military

CY7C401/CY7C403
CY7C402/CY7C404

Cascadeable 64 x 4 FIFO and 64 x 5 FIFO

Features

- **64 x 4 (CY7C401 and CY7C403) 64 x 5 (CY7C402 and CY7C404) High speed first-in first-out memory (FIFO)**
- **Processed with high-speed CMOS for optimum speed/power**
- **25 MHz data rates available on CY7C403 and CY7C404**
- **50 ns bubble-through time— 25 MHz**
- **Expandable in word width and/or length**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Independent asynchronous inputs and outputs**
- **TTL compatible interface**
- **Output enable function available on CY7C403 and CY7C404**
- **Capable of withstanding greater than 2000V electrostatic discharge**
- **Pin compatible with MMI 67401A/67402A**

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five bit words. Both the CY7C403 and CY7C404 have an Output Enable (OE) function.

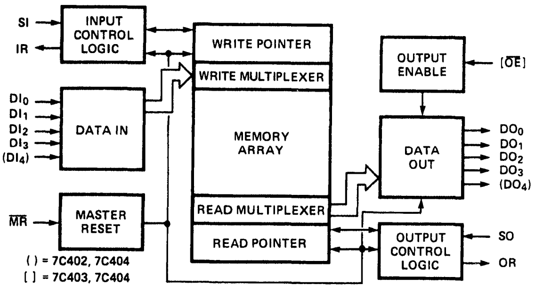
The devices accept 4/5 bit words at the data input (DI_0-DI_n) under the control of the Shift In (SI) input. The stored words stack up at the output (DO_0-DO_n) in the order they were entered. A read command on the Shift Out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The Input Ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The Output Ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

Parallel expansion for wider words is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device is connected to the Shift In (SI) pin of the receiving device.

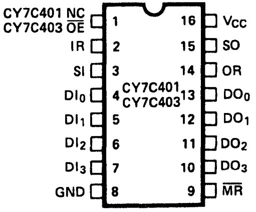
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25 MHz operation makes these FIFOs ideal for high speed communication and controller applications.

Logic Block Diagram

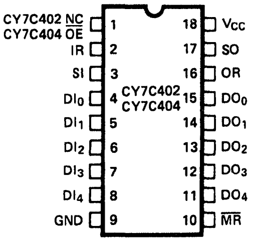

SI
IR
INPUT CONTROL LOGIC
WRITE POINTER
WRITE MULTIPLEXER
MEMORY ARRAY
READ MULTIPLEXER
READ POINTER
OUTPUT ENABLE
[OE]
DATA OUT
OUTPUT CONTROL LOGIC
DI0
DI1
DI2
DI3
(DI4)
DATA IN
MR
MASTER RESET
DO0
DO1
DO2
DO3
(DO4)
SO
OR
( ) = 7C402, 7C404
[ ] = 7C403, 7C404

0014–1

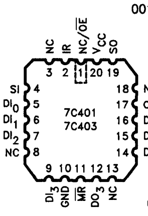
Pin Configurations


CY7C401 NC
CY7C403 OE
IR
SI
DI0
DI1
DI2
DI3
GND
CY7C401
CY7C403
Vcc
SO
OR
DO0
DO1
DO2
DO3
MR

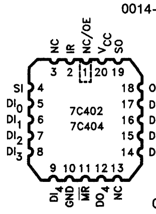
0014–2


CY7C402 NC
CY7C404 OE
IR
SI
DI0
DI1
DI2
DI3
DI4
GND
CY7C402
CY7C404
Vcc
SO
OR
DO0
DO1
DO2
DO3
DO4
MR

0014–3


NC
IR
NC/OE
VCC
SO
SI
DI0
DI1
DI2
NC
7C401
7C403
NC
OR
DO0
DO1
DO2
DI3
GND
MR
DO3
NC

0014–16


NC
IR
NC/OE
VCC
SO
SI
DI0
DI1
DI2
DI3
7C402
7C404
OR
DO0
DO1
DO2
DO3
DI4
GND
MR
DO4
NC

0014–17

Selection Guide

		7C401/2-5	7C40X-10	7C40X-15	7C403/4-25
Maximum Shift Rate (MHz)		5	10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75	75
	Military	—	90	90	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latch-up Current........................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions		7C40X-10, 15, 25 Min.	7C40X-10, 15, 25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
V_{CD}[1]	Input Diode Clamp Voltage[1]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		−50	+50	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

Capacitance

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Note:

For more information on FIFOs, please refer to the FIFO Application Brief in the Appendix of this book.

AC Test Load and Waveform

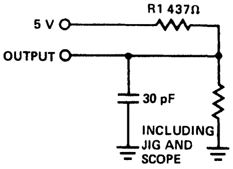


Figure 1a

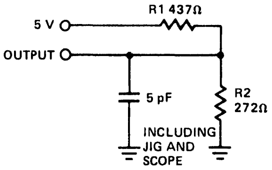
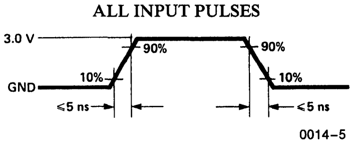
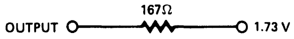


Figure 1b



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions	7C401-5 7C402-5		7C40X-10		7C40X-15		7C403-25 7C404-25 (9)		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 4		5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		20		20		20		11		ns
t_{PLSI}	SI LOW Time		45		30		25		24		ns
t_{SSI}	Data Setup to SI	Note 5	0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 5	60		40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			75		40		35		21/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			75		45		40		28/30	ns
t_{PHSO}	SO HIGH Time		20		20		20		11		ns
t_{PLSO}	SO LOW Time		45		25		25		24		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			75		40		35		19/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			80		55		40		34/37	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		ns
t_{BT}	Bubble through Time			200	10	95	10	65	10	50/60	ns
t_{SIR}	Data Setup to IR	Note 6	5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 6	30		30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		20		20		20		15		ns
t_{POR}	Output Ready Pulse HIGH		20		20		20		15		ns
t_{PMR}	MR Pulse Width		40		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		40		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			85		40		35		35	ns
t_{DIR}	MR LOW to IR HIGH			85		40		35		35	ns
t_{LZMR}	MR LOW to Output LOW	Note 7		50		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			—		35		30		20	ns
t_{HZOE}	Output HIGH-Z from OE HIGH	Note 8		—		30		25		15	ns

Notes:

3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a*.
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$
5. t_{SSI} and t_{HSI} apply when memory is not full.
6. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble through (t_{BT}) conditions exist.
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
8. HIGH-Z transitions are referenced to the steady-state $V_{OH} - 500$ mV and $V_{OL} + 500$ mV levels on the output. t_{HZOE} is tested with 5 pF load capacitance as in *Figure 1b*.
9. Commerical/Military

Operational Description

CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{\text{MR}}$) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs $DO_0 - DO_n$) will be in a LOW state.

SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 7C403-25/7C404-25 AT 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFO's requires attention to characteristics not easily specified in a Datasheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" SI frequency, followed by immediate shifting out of the data also at maximum "shift out" SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output Ready" OR signal during which the SO signal is not recoginized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25 MHz operation until after the window has passed.

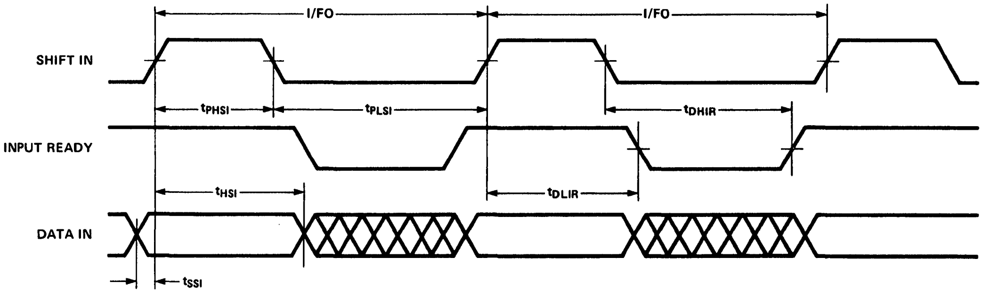
There are several implementation techniques to manage the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. This however requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR "output ready" signal. This however involves the requirement that this only occurs on the first occurance of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of "input ready" IR and SI conditions as well as SO.
4. Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken low again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the OR signal is most appropriate because DATA is guaranteed to be stable prior to and after the OR leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will provide a solution for correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

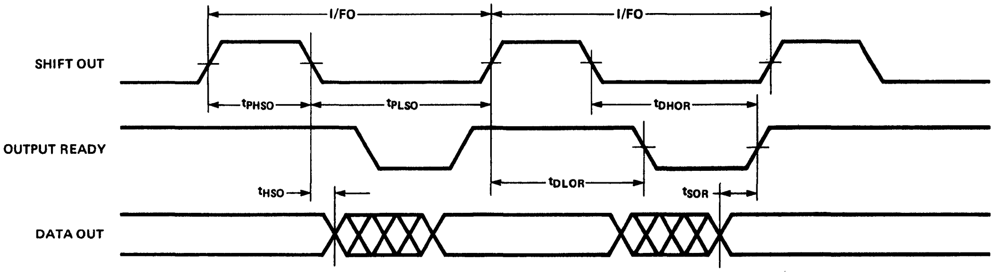
Switching Waveforms

Data In Timing Diagram


I/FO
I/FO
SHIFT IN
tPHSI
tPLSI
tDHIR
INPUT READY
tHSI
tDLIR
DATA IN
tSSI

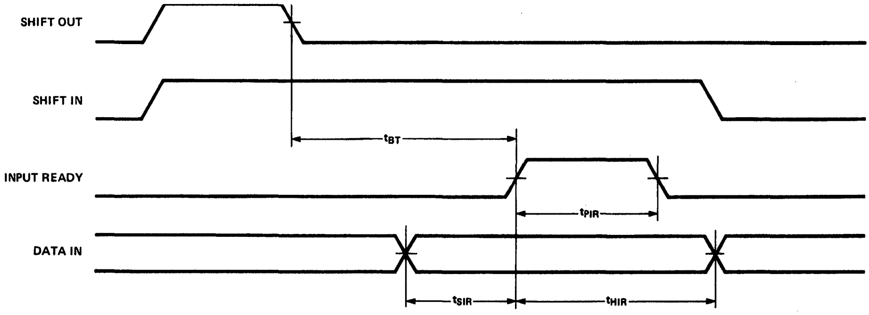
0014-7

Data Out Timing Diagram


I/FO
I/FO
SHIFT OUT
tPHSO
tPLSO
tDHOR
OUTPUT READY
tHSO
tDLOR
tSOR
DATA OUT

0014-8

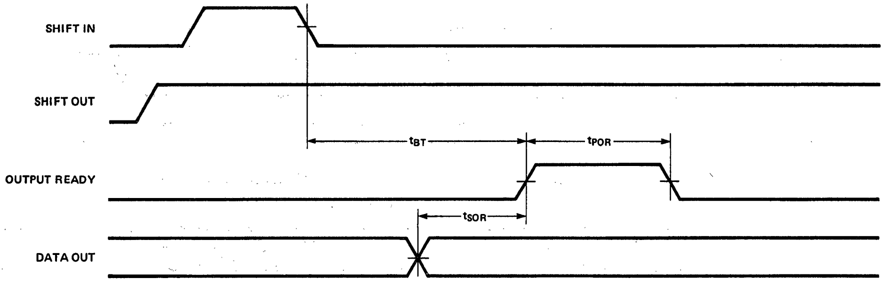
Bubble Through, Data Out To Data In Diagram


SHIFT OUT
SHIFT IN
tBT
INPUT READY
tPIR
DATA IN
tSIR
tHIR

0014-9

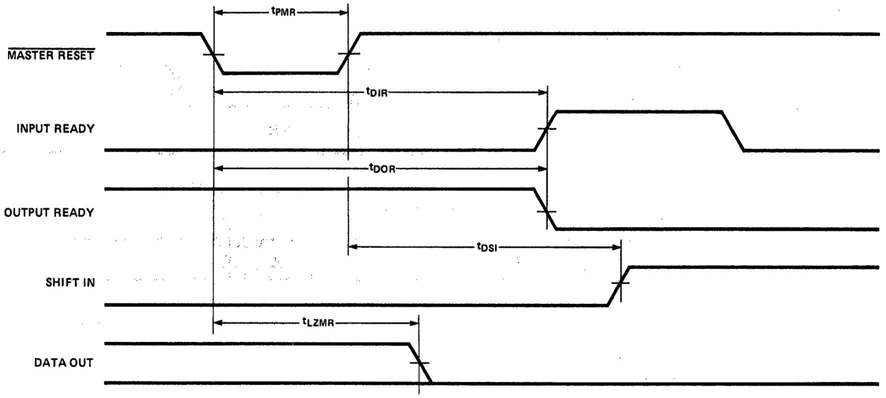
Switching Waveforms (Continued)

Bubble Through, Data In To Data Out Diagram


SHIFT IN
SHIFT OUT
tBT
tPOR
OUTPUT READY
tSOR
DATA OUT

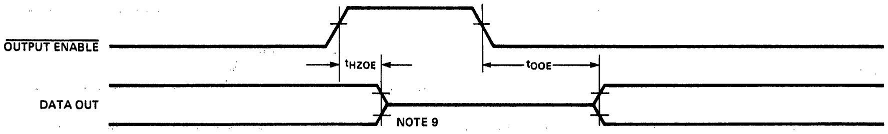
0014–10

Master Reset Timing Diagram


tPMR
MASTER RESET
tDIR
INPUT READY
tDOR
OUTPUT READY
tDSI
SHIFT IN
tLZMR
DATA OUT

0014–11

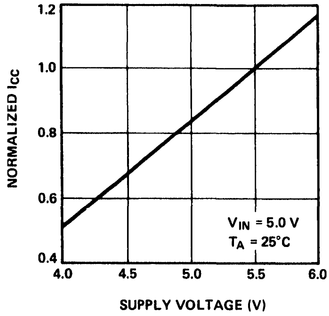
Output Enable Timing Diagram


OUTPUT ENABLE
tHZOE
tOOE
DATA OUT
NOTE 9

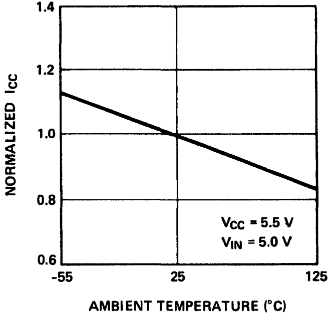
0014–12

Typical DC and AC Characteristics

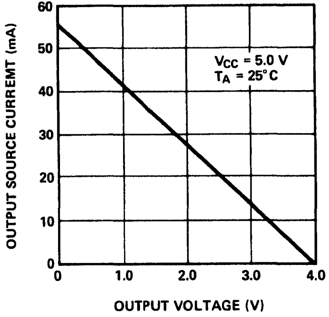
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



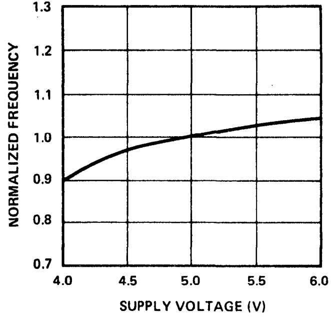
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



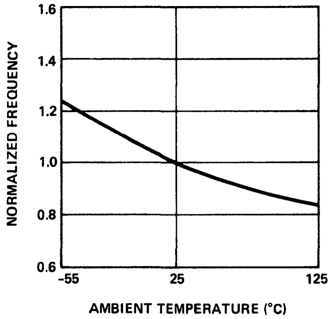
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



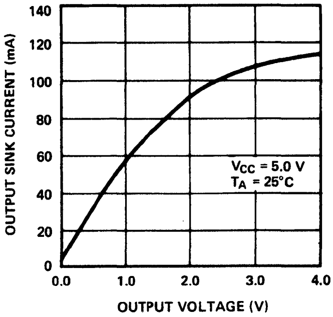
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



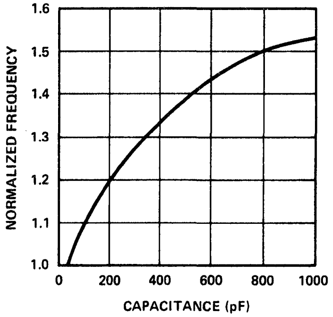
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



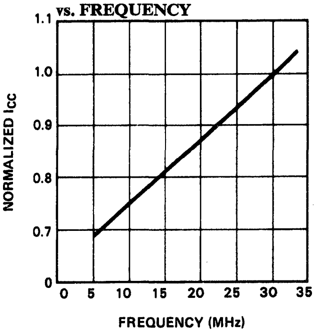
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY

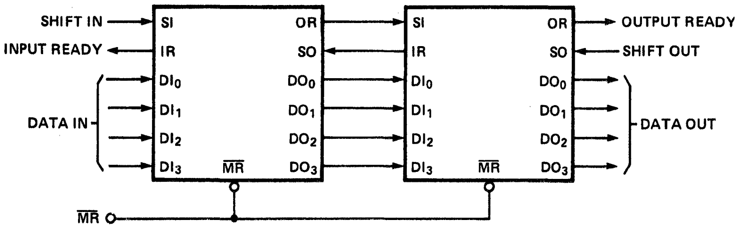


0014-13

5

FIFO Expansion

128 x 4 Application

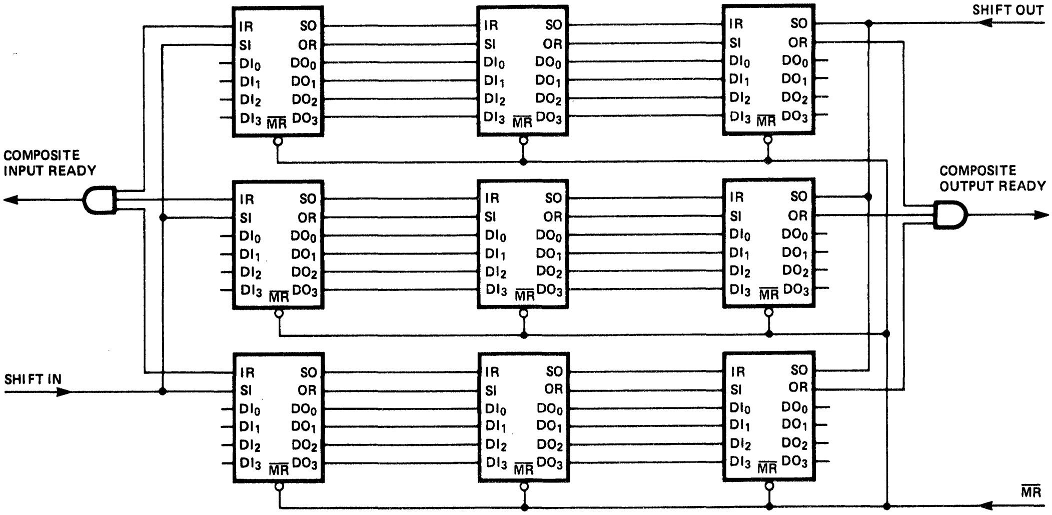

SHIFT IN
INPUT READY
DATA IN
SI
IR
DI0
DI1
DI2
DI3
$\overline{\text{MR}}$
OR
SO
DO0
DO1
DO2
DO3
SI
IR
DI0
DI1
DI2
DI3
$\overline{\text{MR}}$
OR
SO
DO0
DO1
DO2
DO3
OUTPUT READY
SHIFT OUT
DATA OUT
$\overline{\text{MR}}$

0014–14

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

---

192 x 12 Application


SHIFT OUT
COMPOSITE INPUT READY
COMPOSITE OUTPUT READY
SHIFT IN
IR
SI
DI0
DI1
DI2
DI3
$\overline{\text{MR}}$
SO
OR
DO0
DO1
DO2
DO3
$\overline{\text{MR}}$

0014–15

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with pin-compatible FIFO's from other manufacturers.

Ordering Information

Ordering Code (25 MHz)	Package Type	Operating Range
CY7C403-25PC	P1	Com.
CY7C404-25PC	P3	
CY7C403-25DC	D2	
CY7C404-25DC	D4	
CY7C403-25LC	L61	
CY7C404-25LC	L61	
CY7C403-25DMB	D2	Mil.
CY7C404-25DMB	D4	
CY7C403-25LMB	L61	
CY7C404-25LMB	L61	

Ordering Code (15 MHz)	Package Type	Operating Range
CY7C401-15PC	P1	Com.
CY7C402-15PC	P3	
CY7C403-15PC	P1	
CY7C404-15PC	P3	
CY7C401-15DC	D2	
CY7C402-15DC	D4	
CY7C403-15DC	D2	
CY7C404-15DC	D4	
CY7C401-15LC	L61	
CY7C402-15LC	L61	
CY7C403-15LC	L61	
CY7C404-15LC	L61	
CY7C401-15DMB	D2	Mil.
CY7C402-15DMB	D4	
CY7C403-15DMB	D2	
CY7C404-15DMB	D4	
CY7C401-15LMB	L61	
CY7C402-15LMB	L61	
CY7C403-15LMB	L61	
CY7C404-15LMB	L61	

Ordering Code (10 MHz)	Package Type	Operating Range
CY7C401-10PC	P1	Com.
CY7C402-10PC	P3	
CY7C403-10PC	P1	
CY7C404-10PC	P3	
CY7C401-10DC	D2	
CY7C402-10DC	D4	
CY7C403-10DC	D2	
CY7C404-10DC	D4	
CY7C401-10LC	L61	
CY7C402-10LC	L61	
CY7C403-10LC	L61	
CY7C404-10LC	L61	
CY7C401-10DMB	D2	Mil.
CY7C402-10DMB	D4	
CY7C403-10DMB	D2	
CY7C404-10DMB	D4	
CY7C401-10LMB	L61	
CY7C402-10LMB	L61	
CY7C403-10LMB	L61	
CY7C404-10LMB	L61	

Ordering Code (5 MHz)	Package Type	Operating Range
CY7C401-5PC	P1	Com.
CY7C402-5PC	P1	

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C408
CY7C409

Cascadeable 64 x 8 FIFO
Cascadeable 64 x 9 FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35 MHz shift-in and shift-out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual port RAM architecture**
- **Fast, 50 ns, bubblethrough**
- **Independent asynchronous inputs and outputs**
- **Output Enable (CY7C408)**
- **Expandable in word width and FIFO depth**
- **5V ±10% supply**
- **TTL compatible**
- **Capable of withstanding greater than 2000V electrostatic discharge voltage**
- **300 mil, 28-pin DIP**

Functional Description

The CY7C408 and CY7C409 are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry standard handshaking signals Almost Full/Almost Empty (AFE) and Half Full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty. Otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408 has an Output Enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI0–DI8) under the control of the Shift-In (SI) input when the Input-Ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO0–DO8 output pins under the control of the Shift-Out (SO) input when the Output-Ready (OR) control signal is HIGH. If the FIFO is full (IR LOW) pulses at the SI input are ignored: if the FIFO is empty (OR LOW) pulses at the SO input are ignored.

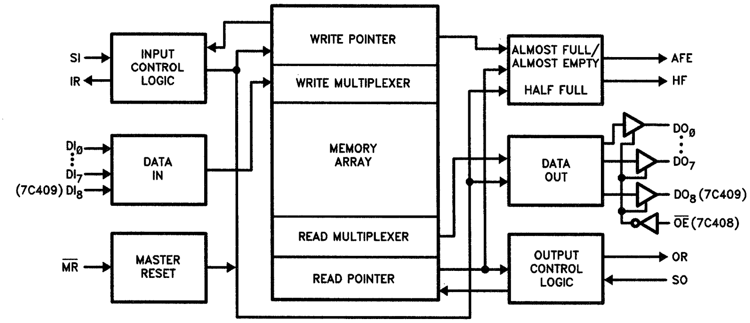
The IR and OR signals are also used to connect the FIFO's in parallel to make a wider word, or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together. The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or are ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO. In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration (called cascade) the IR and OR signals are used to pass data through full and empty FIFOs.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift-in and shift-out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual port RAM architecture, make them ideal for high speed communications and controllers.

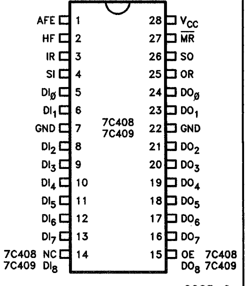
Logic Block Diagram



SI
IR
INPUT CONTROL LOGIC
DI0
DI7
(7C409) DI8
DATA IN
MR
MASTER RESET
WRITE POINTER
WRITE MULTIPLEXER
MEMORY ARRAY
READ MULTIPLEXER
READ POINTER
ALMOST FULL/ ALMOST EMPTY
HALF FULL
AFE
HF
DATA OUT
DO0
DO7
DO8 (7C409)
OE (7C408)
OUTPUT CONTROL LOGIC
OR
SO

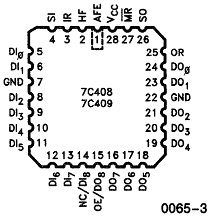
0065-1

Pin Configurations



AFE 1
HF 2
IR 3
SI 4
DI0 5
DI1 6
GND 7
DI2 8
DI3 9
DI4 10
DI5 11
DI6 12
DI7 13
7C408 NC 7C409 DI8 14
28 VCC
27 MR
26 SO
25 OR
24 DO0
23 DO1
22 GND
21 DO2
20 DO3
19 DO4
18 DO5
17 DO6
16 DO7
15 OE 7C408 DO8 7C409
7C408 7C409

0065-2



SI IR HF AFE VCC MR SO
4 3 2 1 28 27 26
DI0 5
DI1 6
GND 7
DI2 8
DI3 9
DI4 10
DI5 11
25 OR
24 DO0
23 DO1
22 GND
21 DO2
20 DO3
19 DO4
12 13 14 15 16 17 18
DI6 DI7 NC/DI8 OE/DO8 DO7 DO6 DO5
7C408 7C409

0065-3

Flag Definitions

HF	AFE	Words Stored
L	H	0–8
L	L	9–31
H	L	32–55
H	H	56–64

Selection Guide

		7C408-15 7C409-15	7C408-25 7C409-25	7C408-35 7C409-35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	120	120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latch-up Current.......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions		CY7C408 CY7C409 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	mA
I_{CC}[2]	Power Supply Current	f_{SO} = 35 MHz, f_{SI} = 35 MHz	Commercial		135	mA
			Military		160	mA

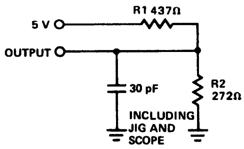
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

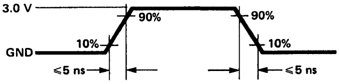
1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. $I_{CC} = I_{CC_Q} + 1\ \text{mA/MHz} \times (f_{SI} + f_{SO})/2$
3. Tested on a sample basis.

AC Test Load and Waveform



0065-4

Figure 1

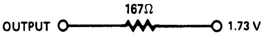


0065-5

Figure 2. All Input Pulses

Equivalent to:

THÉVENIN EQUIVALENT



0065-6

Switching Characteristics Over the Operating Range[4]

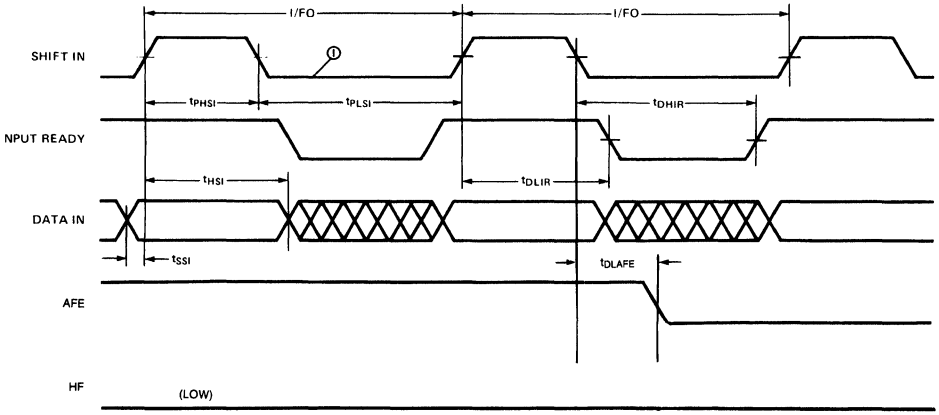
Parameters	Description	Test Conditions	CY7C409-15		CY7C409-25		CY7C409-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 5		15		25		35	MHz
t_{PHSI}	SI HIGH Time		23		11		9		ns
t_{PLSI}	SI LOW Time		25		24		17		ns
t_{SSI}	Data Setup to SI	Note 6	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 6	30		20		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time		23		11		9		ns
t_{PLSO}	SO LOW Time		25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Bubblethrough Time		10	65	10	60	10	50	ns
t_{SIR}	Data Setup to IR	Note 7	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 7	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH		23		15		10		ns
t_{POR}	Output Ready Pulse HIGH		23		15		10		ns
t_{DLZOE}	OE LOW to LOW Z (7C408)			35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408)			35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 8		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns

Notes:

4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1.*
5. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
6. t_{SSI} and t_{HSI} apply when memory is not full.
7. t_{SIR} and t_{HIR} apply when memory is full, SI is HIGH and minimum bubblethrough (t_{BT}) conditions exist.
8. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

Switching Waveforms

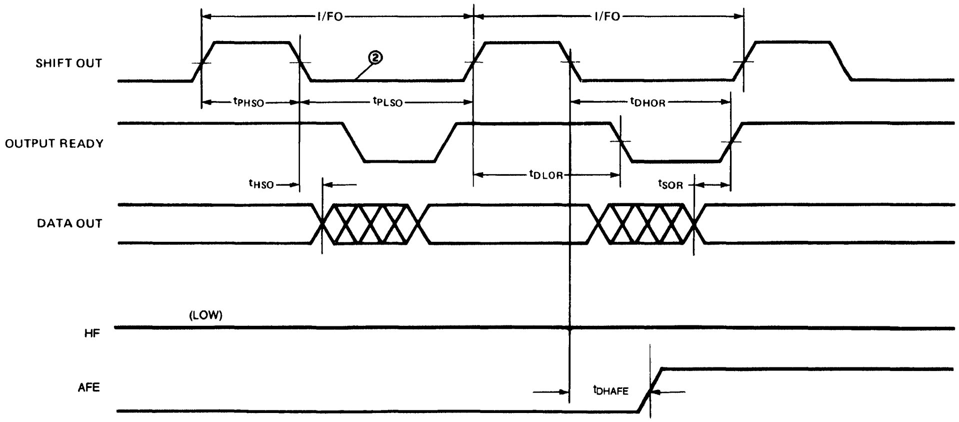
Data In Timing Diagram


I/FO
I/FO
SHIFT IN
①
tPHSI
tPLSI
tDHIR
NPUT READY
tHSI
tDLIR
DATA IN
tSSI
tDLAFE
AFE
HF
(LOW)

0065-7

① FIFO Contains 8 Words

Data Out Timing Diagram

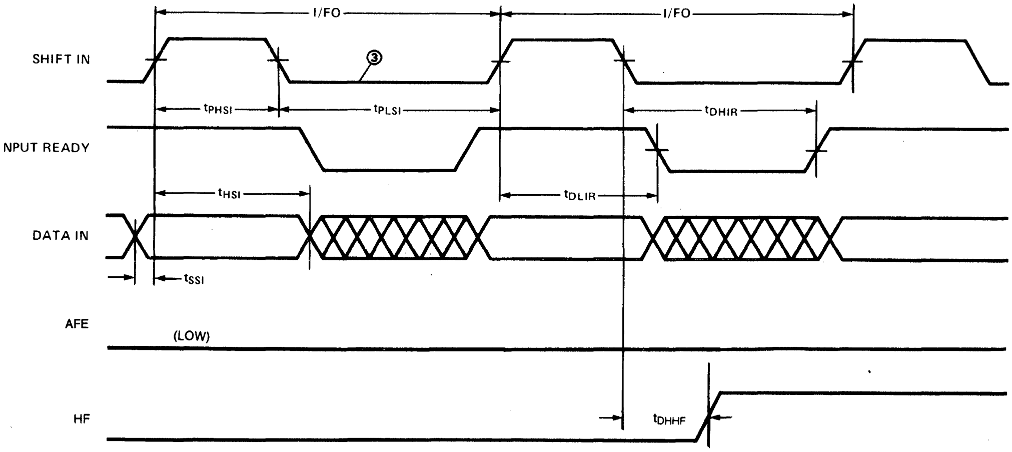

I/FO
I/FO
SHIFT OUT
②
tPHSO
tPLSO
tDHOR
OUTPUT READY
tHSO
tDLOR
tSOR
DATA OUT
(LOW)
HF
AFE
tDHAFE

0065-8

② FIFO Contains 9 Words

Switching Waveforms (Continued)

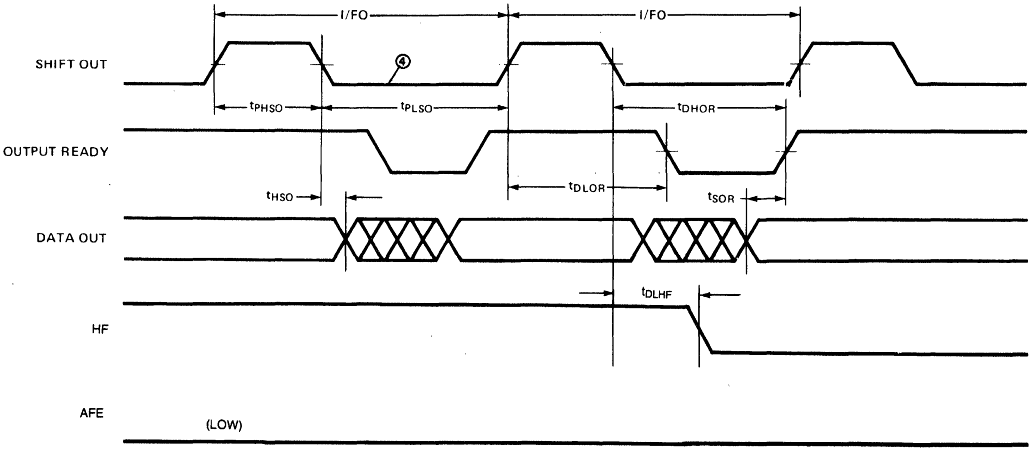
Data In Timing Diagram


I/FO
I/FO
SHIFT IN
③
tPHSI
tPLSI
tDHIR
NPUT READY
tHSI
tDLIR
DATA IN
tSSI
AFE
(LOW)
HF
tDHHF

0065-14

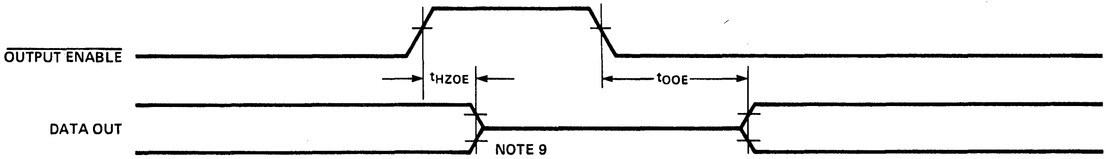
③ FIFO Contains 31 Words

Data Out Timing Diagram


I/FO
I/FO
SHIFT OUT
④
tPHSO
tPLSO
tDHOR
OUTPUT READY
tHSO
tDLOR
tSOR
DATA OUT
tDLHF
HF
AFE
(LOW)

0065-15

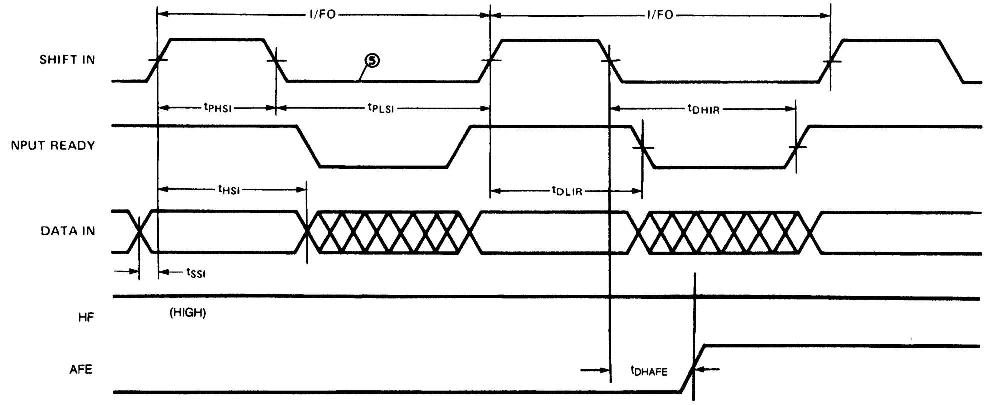
④ FIFO Contains 32 Words


OUTPUT ENABLE
tHZOE
tOOE
DATA OUT
NOTE 9

0065-20

Switching Waveforms (Continued)

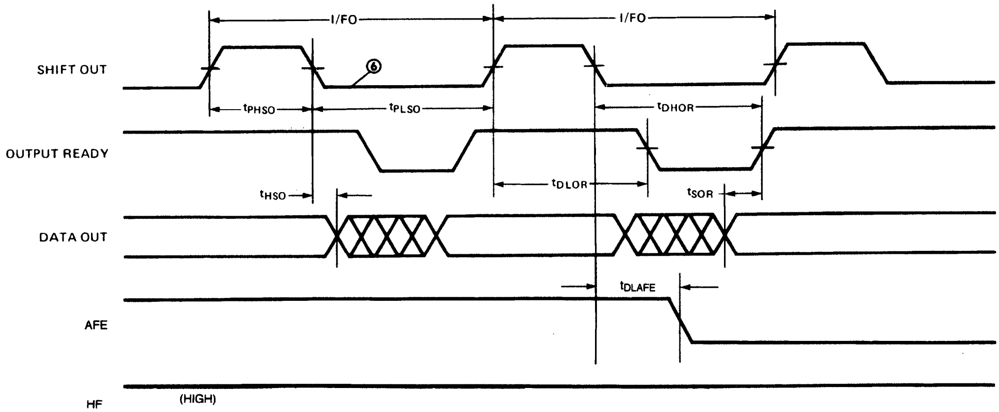
Data In Timing Diagram


I/FO
I/FO
SHIFT IN
⑤
t_{PHSI}
t_{PLSI}
t_{DHIR}
NPUT READY
t_{HSI}
t_{DLIR}
DATA IN
t_{SSI}
HF
(HIGH)
AFE
t_{DHAFE}

0065-16

⑤ FIFO Contains 55 Words

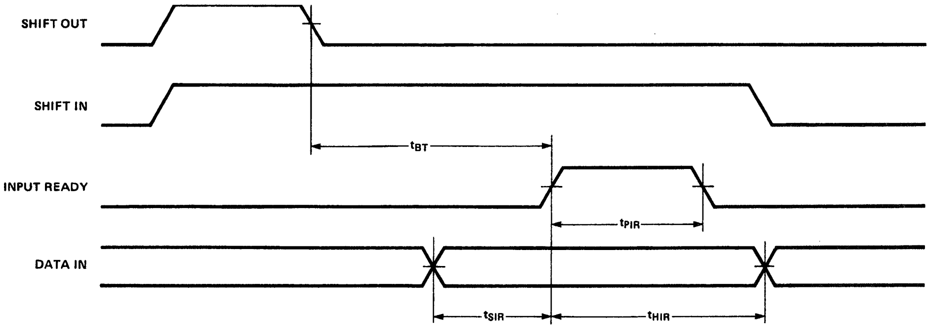
Data Out Timing Diagram


I/FO
I/FO
SHIFT OUT
⑥
t_{PHSO}
t_{PLSO}
t_{DHOR}
OUTPUT READY
t_{HSO}
t_{DLOR}
t_{SOR}
DATA OUT
t_{DLAFE}
AFE
HF
(HIGH)

0065-17

⑥ FIFO Contains 56 Words

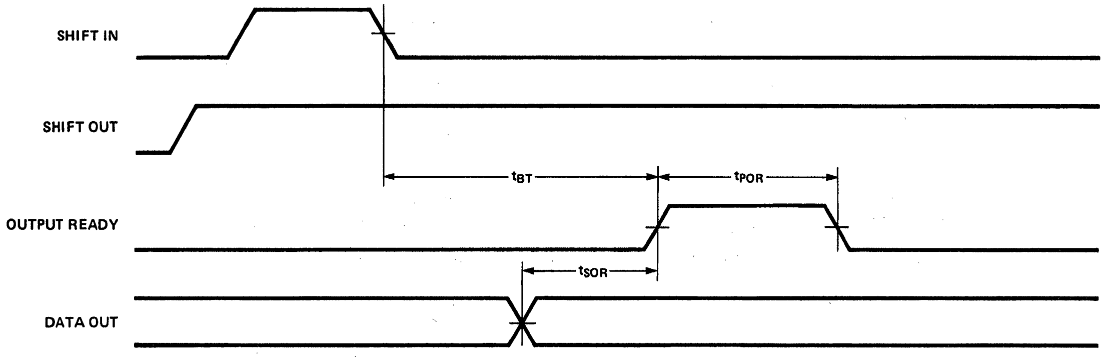
Bubblethrough, Data Out to Data In Diagram


SHIFT OUT
SHIFT IN
t_{BT}
INPUT READY
t_{PIR}
DATA IN
t_{SIR}
t_{HIR}

0065-9

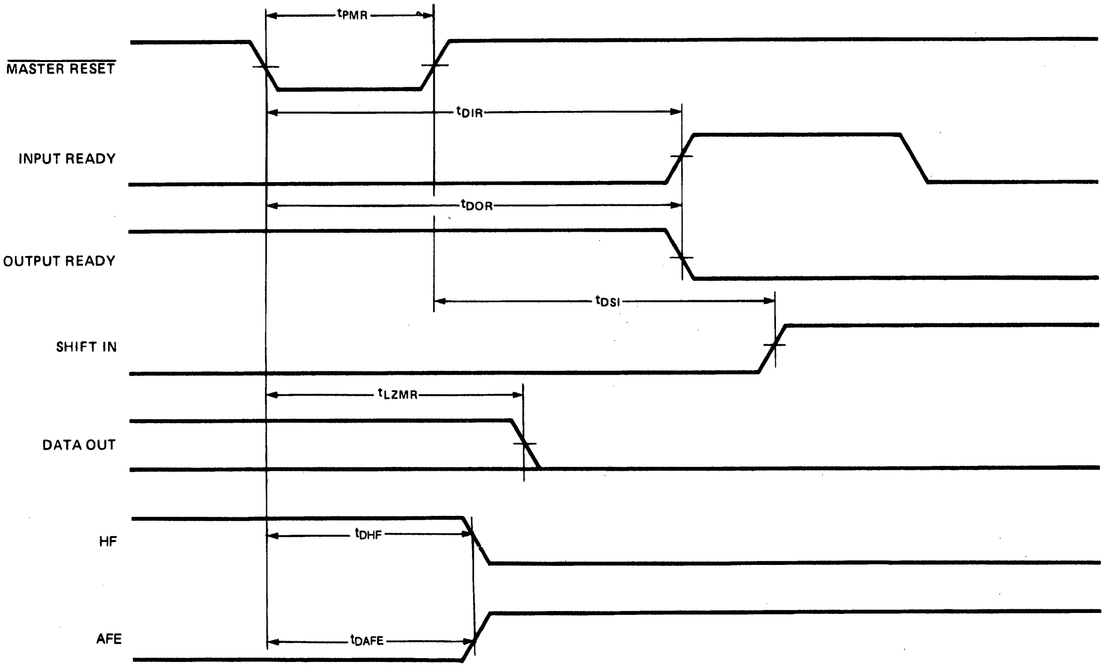
Switching Waveforms (Continued)

Fallthrough, (Bubblethrough) Data In to Data Out Diagram


SHIFT IN
SHIFT OUT
t_{BT}
t_{POR}
OUTPUT READY
t_{SOR}
DATA OUT

0065-10

Master Reset Timing Diagram


t_{PMR}
$\overline{\text{MASTER RESET}}$
t_{DIR}
INPUT READY
t_{DOR}
OUTPUT READY
t_{DSI}
SHIFT IN
t_{LZMR}
DATA OUT
HF
t_{DHF}
AFE
t_{DAFE}

0065-11

Architecture of the CY7C408 and CY7C409

The CY7C408 and CY7C409 FIFOs consist of an array of 64 words of 8- or 9-bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AFE) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Bubblethrough and Fallthrough

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fallthrough time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubblethrough time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fallthrough time when it is empty (or near empty) and by the bubblethrough time when it is full (or near full).

The conventional definitions of fallthrough and bubblethrough do not apply to the CY7C408 and CY7C409 FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power up the FIFO must be reset with a Master Reset ($\overline{\text{MR}}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO0–DO8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the Shift-In (SI) pin will load the data on the DI0–DI8 inputs into the FIFO. The IR output will then go LOW, indicating that the data has been sampled. The HIGH to LOW transition of the SI signal initiates the LOW to HIGH transition of the IR signal, as well as the AFE flag LOW to HIGH transition if the FIFO is almost full or almost empty.

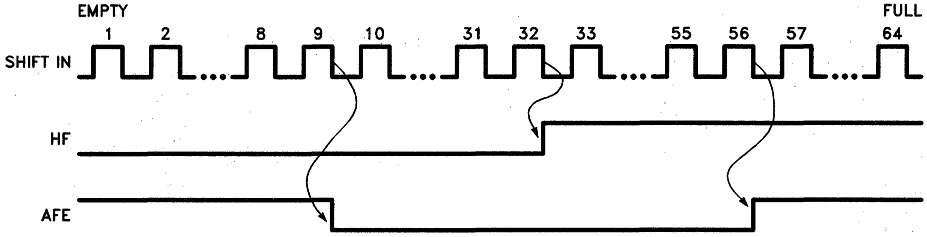
Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset all data outputs (DO0–DO8) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. Every data word except the first is shifted out in response to the falling edge of the SO pulse.

AFE and HF Flags

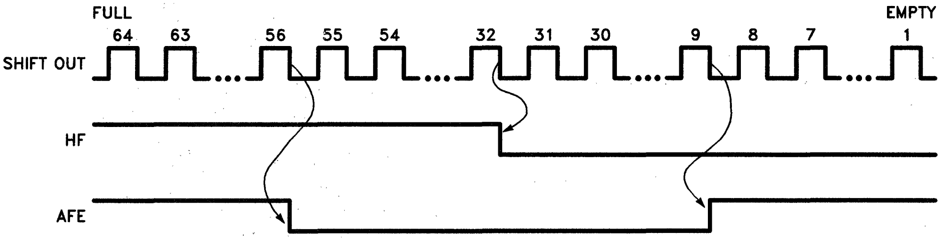
Two flags, Almost Full/Almost Empty (AFE) and Half Full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO.

Shifting Words In


EMPTY
FULL
1
2
8
9
10
31
32
33
55
56
57
64
SHIFT IN
HF
AFE

0065–18

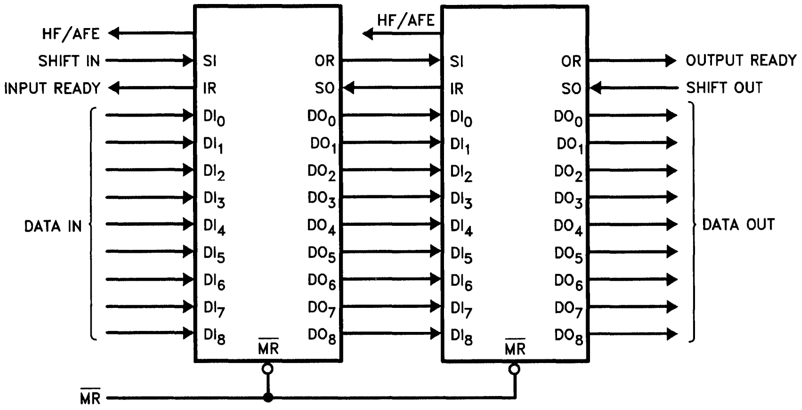
Shifting Words Out


FULL
EMPTY
64
63
56
55
54
32
31
30
9
8
7
1
SHIFT OUT
HF
AFE

0065–19

FIFO Expansion

128 x 9 Configuration



0065–12

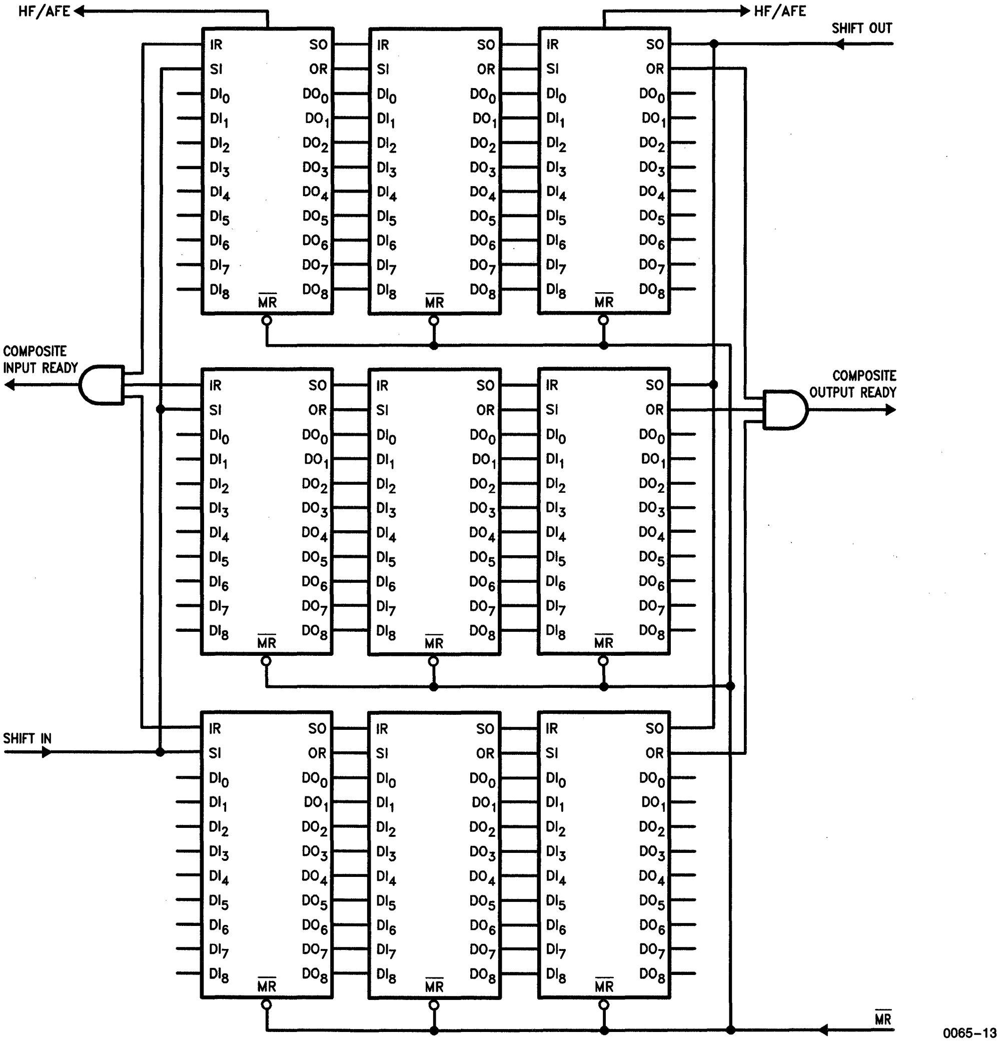
FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{DLOR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with FIFOs from other manufacturers.

FIFO Expansion (Continued)

192 x 27 Configuration



FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{DLOR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with FIFOs from other manufacturers.

Ordering Information

Frequency (MHz)	Ordering Code	Package Type	Operating Range
35	CY7C408-35PC CY7C408-35DC CY7C408-35LC	P21 D22 L64	Commercial
	CY7C408-35DMB CY7C408-35LMB	D22 L64	Military
25	CY7C408-25PC CY7C408-25DC CY7C408-25LC	P21 D22 L64	Commercial
	CY7C408-25DMB CY7C408-25LMB	D22 L64	Military
15	CY7C408-15PC CY7C408-15DC CY7C408-15LC	P21 D22 L64	Commercial
	CY7C408-15DMB CY7C408-15LMB	D22 L64	Military

Frequency (MHz)	Ordering Code	Package Type	Operating Range
35	CY7C409-35PC CY7C409-35DC CY7C409-35LC	P21 D22 L64	Commercial
	CY7C409-35DMB CY7C409-35LMB	D22 L64	Military
25	CY7C409-25PC CY7C409-25DC CY7C409-25LC	P21 D22 L64	Commercial
	CY7C409-25DMB CY7C409-25LMB	D22 L64	Military
15	CY7C409-15PC CY7C409-15DC CY7C409-15LC	P21 D22 L64	Commercial
	CY7C409-15DMB CY7C409-15LMB	D22 L64	Military

CYPRESS
SEMICONDUCTOR

PRELIMINARY

CY7C412
CY7C424/CY7C429

Cascadeable 512 x 9 FIFO
Cascadeable 1024 x 9 FIFO
Cascadeable 2048 x 9 FIFO

Features

- **512 x 9, 1024 x 9, 2048 x 9 FIFO buffer memory**
- **Dual port RAM cell**
- **Asynchronous read/write**
- **High speed 25 MHz read/write independent of depth/width**
- **Low operating power**
  I_{CC} (max.) = 100 mA commercial
  I_{CC} (max.) = 120 mA military
- **Lower standby power**
  I_{CC} (max.) = 8 mA commercial
  I_{CC} (max.) = 15 mA military
- **Automatic power down**
- **Half full flag in standalone**
- **Empty and full flags**
- **Automatic retransmit in standalone**
- **Expandable in width and depth**
- **Parallel Cascade minimizes bubblethrough**
- **5V ±10% supply**
- **TTL compatible**
- **Three-state outputs**
- **CY7C412 pin compatible and functional equivalent to MK4501**

Functional Description

The CY7C412, CY7C424, and CY7C429 are, respectively, 512, 1024, and 2048 words by 9-bit wide first-in first-out (FIFO) memories organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

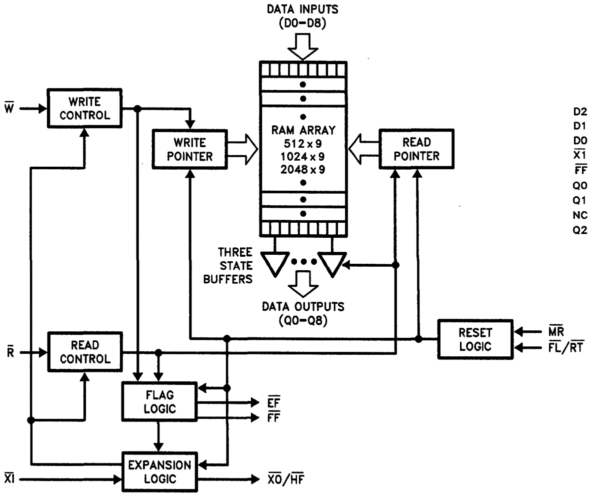
The read and write operations may be asynchronous; each can occur at a rate of 25 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW and Read ($\overline{R}$) is HIGH. Read occurs when Read ($\overline{R}$) goes LOW and Write ($\overline{W}$) is HIGH. The 9 data outputs go to the high impedance state when $\overline{R}$ is HIGH.

A Half-Full ($\overline{HF}$) output flag is provided that is valid in the standalone and parallel expansion configurations. In the depth expansion configuration this pin is used to tell the next FIFO that it will be receiving data.

In the standalone and parallel expansion configurations a LOW on the Retransmit ($\overline{RT}$) input causes the FIFO's to retransmit the data. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during retransmit.

The CY7C412, CY7C424, and CY7C429 are fabricated using an advanced 1.2 micron N-well CMOS technology. Input ESD protection is greater than 2000V and latchup is prevented by careful layout, guard rings and a substrate bias generator.

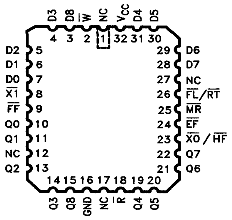
Logic Block Diagram


DATA INPUTS
(D0–D8)
$\overline{W}$
WRITE CONTROL
WRITE POINTER
RAM ARRAY
512x9
1024x9
2048x9
READ POINTER
THREE STATE BUFFERS
DATA OUTPUTS
(Q0–Q8)
RESET LOGIC
$\overline{MR}$
$\overline{FL}/\overline{RT}$
$\overline{R}$
READ CONTROL
FLAG LOGIC
$\overline{EF}$
$\overline{FF}$
EXPANSION LOGIC
$\overline{XI}$
$\overline{XO}/\overline{HF}$

0081-1

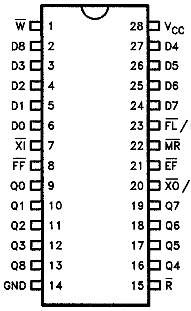
Pin Configurations

LCC
Top View


D3 4
D8 3
$\overline{W}$ 2
NC 1
V_{CC} 32
D4 31
D5 30
D2 5
D1 6
D0 7
$\overline{X1}$ 8
$\overline{FF}$ 9
Q0 10
Q1 11
NC 12
Q2 13
D6 29
D7 28
NC 27
$\overline{FL}/\overline{RT}$ 26
$\overline{MR}$ 25
$\overline{EF}$ 24
$\overline{XO}/\overline{HF}$ 23
Q7 22
Q6 21
Q3 14
Q8 15
GND 16
NC 17
$\overline{R}$ 18
Q4 19
Q5 20

0081-3

DIP
Top View


$\overline{W}$ 1
D8 2
D3 3
D2 4
D1 5
D0 6
$\overline{XI}$ 7
$\overline{FF}$ 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 V_{CC}
27 D4
26 D5
25 D6
24 D7
23 $\overline{FL}/\overline{RT}$
22 $\overline{MR}$
21 $\overline{EF}$
20 $\overline{XO}/\overline{HF}$
19 Q7
18 Q6
17 Q5
16 Q4
15 $\overline{R}$

0081-2

Selection Guide

		7C412-30 7C424-30 7C429-30	7C412-40 7C424-40 7C429-40	7C412-65 7C424-65 7C429-65
Address Access Time (ns)		30	40	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	120	120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State. . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) . . . . 20 mA

Static Discharge Voltage . . . . >2001V (per MIL-STD-883 Method 3015.2)

Latch-up Current . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		CY7C412 CY7C424 CY7C429		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltgage	V_{CC} = Min., I_{OH} = −2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = 25 MHz	Commercial		100	mA
			Military		120	mA
I_{SB}	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		8	mA
			Military		15	mA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90	mA

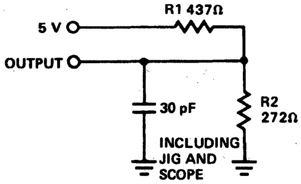
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

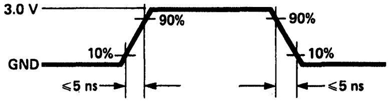
1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Load and Waveform



0081-4

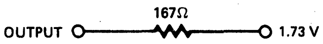
Figure 1



0081-5

Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0081-6

Switching Characteristics Over the Operating Range[1]

Parameter	Description	7C412-30 7C424-30 7C429-30		7C412-40 7C424-40 7C429-40		7C412-65 7C424-65 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_{AA}	Address to Data Valid		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}	Read LOW to Low Z	5		5		10		ns
t_{DVR}	Read HIGH to Data Valid	5		5		5		ns
t_{HZR}	Read HIGH to High Z		20		25		30	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{LZW}	Write LOW to Low Z	10		10		15		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		40		50		80	ns

Switching Characteristics Over the Operating Range[1] (Continued)

Parameter	Description	7C412-30 7C424-30 7C429-30		7C412-40 7C424-40 7C429-40		7C412-65 7C424-65 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{\text{EF}}$ HIGH		30		40		65	ns
t_{WAF}	Effective Write from from Read HIGH		30		35		60	ns
t_{PWF}	Effective Write Pulse Width after $\overline{\text{FF}}$ HIGH		30		40		65	ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		35		55	ns
t_{XOH}[2]	Expansion Out HIGH Delay from Clock		25		35		60	ns
t_{XCH}	Expansion Out HIGH Delay from Clock		35		35		60	ns
t_{PXF}	$\overline{\text{XI}}$ Pulse Width	30		40		60		ns
t_{XIR}	$\overline{\text{XI}}$ Recovery Time	10		10		15		ns
t_{XIS}	$\overline{\text{XI}}$ Set-Up to Write or Clock	15		15		25		ns

Notes:

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a.*
2. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

Architecture

The CY7C412/24/29 FIFOs consist of an array of 512/1024/2048 words of 9-bits each (implemented by a dual port RAM cell), a read pointer, a write pointer, control signals ($\overline{\text{W}}$, $\overline{\text{R}}$, $\overline{\text{XI}}$, $\overline{\text{XO}}$, $\overline{\text{FL}}$, $\overline{\text{RT}}$, $\overline{\text{MR}}$) and Full, Half Full, and Empty flags.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{\text{MR}}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{\text{EF}}$) being LOW, and both the Half-Full ($\overline{\text{HF}}$) and Full flag ($\overline{\text{FF}}$) resetting to HIGH. Read ($\overline{\text{R}}$) and Write ($\overline{\text{W}}$) must be HIGH t_{RPW} before and t_{RMR} after the rising edge of $\overline{\text{MR}}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full Flag ($\overline{\text{FF}}$). A falling edge of Write ($\overline{\text{W}}$) initiates a write cycle. Data appearing at the inputs (D0–D8) t_{DS} before and t_{DH} after the rising edge of $\overline{\text{W}}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{\text{EF}}$) LOW to HIGH transition occurs t_{WEF} after the first write into an empty FIFO. The Half-Full flag ($\overline{\text{HF}}$) will go LOW on the falling edge of the write operation following the occurrence of half full. $\overline{\text{HF}}$ will remain LOW while the difference between the values of the read and write pointers is less than one half of the total memory of this device. The LOW to HIGH transition of the $\overline{\text{HF}}$ flag occurs on the rising edge of Read ($\overline{\text{R}}$). $\overline{\text{HF}}$ is available in Single Device Mode only. The Full flag ($\overline{\text{FF}}$) goes low on the falling edge of $\overline{\text{W}}$ after the last available location in the FIFO is written, prohibiting overflow. $\overline{\text{FF}}$ goes HIGH t_{RFF} after the completion of a valid read.

Reading Data from the FIFO

The falling edge of Read ($\overline{\text{R}}$) initiates a read cycle if the Empty flag ($\overline{\text{EF}}$) is not LOW. Data outputs (Q0–Q8) are in a high impedance condition between read operations ($\overline{\text{R}}$ HIGH), when the FIFO is empty, or when the FIFO is in the Depth Expansion Mode but is not the active device.

Architecture (Continued)

The falling edge of the last read before empty triggers a HIGH to LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The Retransmit ($\overline{RT}$) input is active in the Single Device Mode only. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle.

Single Device/Width Expansion Modes

Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a $\overline{MR}$ cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

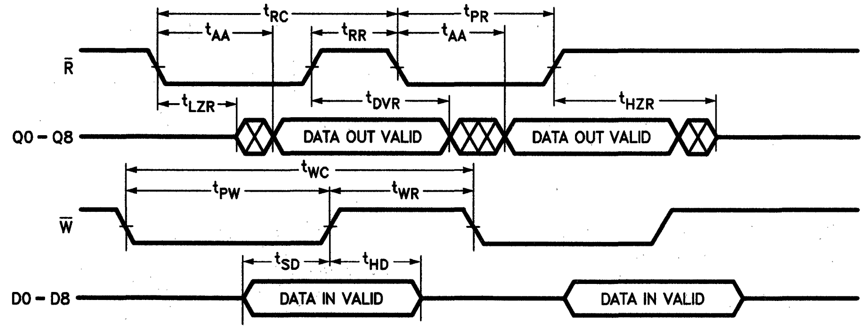
Depth Expansion Mode

Depth Expansion Mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the Depth Expansion Mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of a FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time, all other devices are disabled.

FIFOs can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in Depth Expansion Mode.

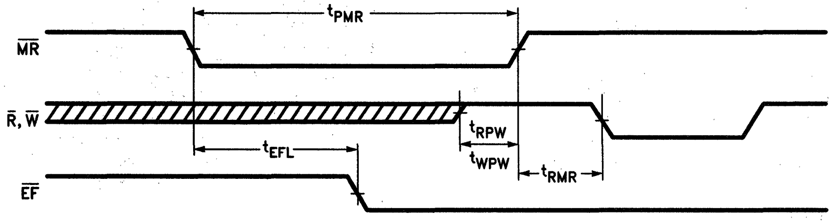
Switching Waveforms

Asynchronous Read and Write Timing Diagram



0081–7

Master Reset Timing Diagram



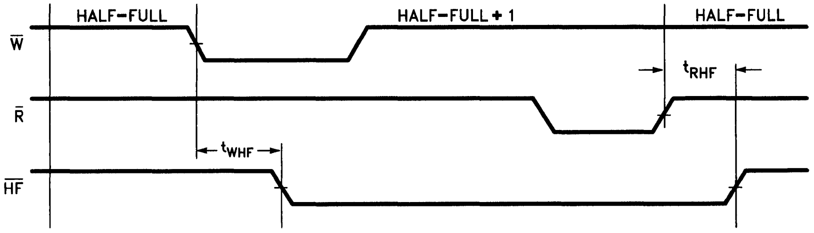
0081–8

Notes:

1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{MR}$.

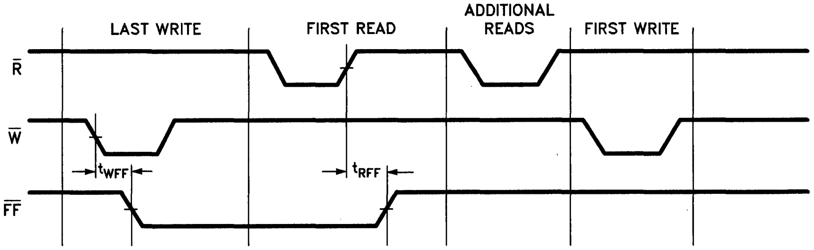
Switching Waveforms (Continued)

Half-Full Flag Timing Diagram


HALF-FULL
HALF-FULL + 1
HALF-FULL
$\overline{W}$
t_{RHF}
$\overline{R}$
t_{WHF}
$\overline{HF}$

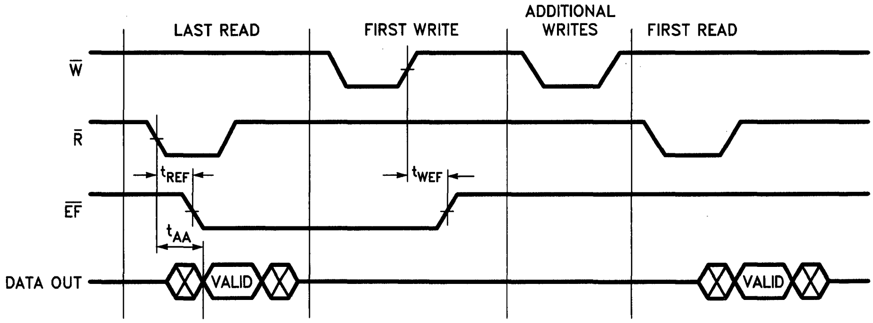
0081-9

Last WRITE to First READ Full Flag Timing Diagram


LAST WRITE
FIRST READ
ADDITIONAL READS
FIRST WRITE
$\overline{R}$
$\overline{W}$
t_{WFF}
t_{RFF}
$\overline{FF}$

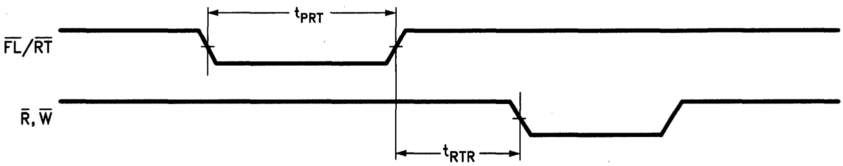
0081-10

Last READ to First WRITE Empty Flag Timing Diagram


LAST READ
FIRST WRITE
ADDITIONAL WRITES
FIRST READ
$\overline{W}$
$\overline{R}$
t_{REF}
t_{WEF}
$\overline{EF}$
t_{AA}
DATA OUT
VALID
VALID

0081-11

Retransmit Timing Diagram


t_{PRT}
$\overline{FL}/\overline{RT}$
$\overline{R}, \overline{W}$
t_{RTR}

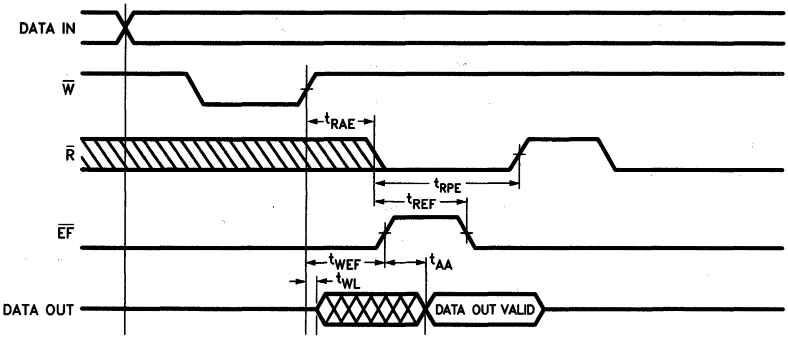
0081-12

Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

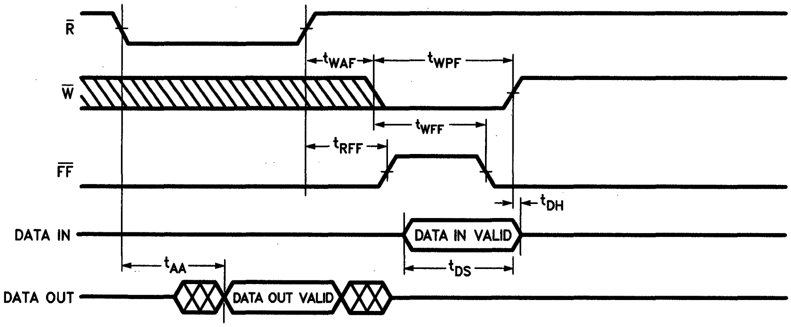
Switching Waveforms (Continued)

Empty Flag and Read Bubble-Through Mode Timing Diagram


DATA IN
$\overline{W}$
$\overline{R}$
t_{RAE}
t_{RPE}
t_{REF}
$\overline{EF}$
t_{WEF}
t_{AA}
t_{WL}
DATA OUT
DATA OUT VALID

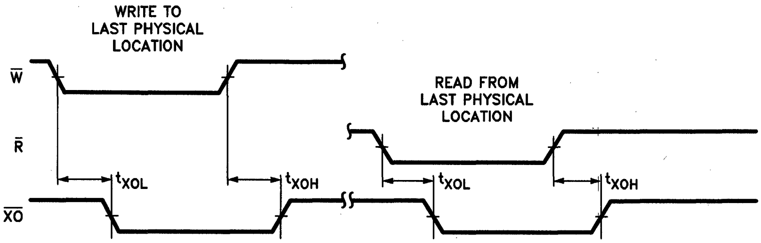
0081-13

Full Flag and Write Bubble-Through Mode Timing Diagram


$\overline{R}$
t_{WAF}
t_{WPF}
$\overline{W}$
t_{WFF}
t_{RFF}
$\overline{FF}$
t_{DH}
DATA IN
DATA IN VALID
t_{AA}
t_{DS}
DATA OUT
DATA OUT VALID

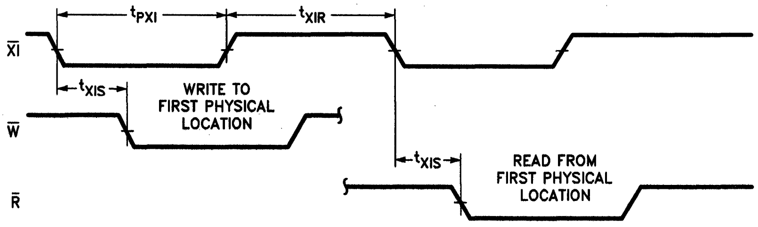
0081-14

Expansion-Out Timing Diagram


WRITE TO LAST PHYSICAL LOCATION
$\overline{W}$
READ FROM LAST PHYSICAL LOCATION
$\overline{R}$
t_{XOL}
t_{XOH}
t_{XOL}
t_{XOH}
$\overline{XO}$

0081-15

Expansion-In Timing Diagram


t_{PXI}
t_{XIR}
$\overline{XI}$
t_{XIS}
WRITE TO FIRST PHYSICAL LOCATION
$\overline{W}$
t_{XIS}
READ FROM FIRST PHYSICAL LOCATION
$\overline{R}$

0081-16

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C412-30 PC	P15	Commercial
	CY7C412-30 JC	J65	
	CY7C412-30 DC	D16	
	CY7C412-30 LC	L55	
	CY7C412-30 DMB	L16	Military
	CY7C412-30 LMB	L55	
40	CY7C412-40 PC	P15	Commercial
	CY7C412-40 JC	J65	
	CY7C412-40 DC	D16	
	CY7C412-40 LC	L55	
	CY7C412-40 DMB	D16	Military
	CY7C412-40 LMB	L55	
65	CY7C412-65 PC	P15	Commercial
	CY7C412-65 JC	J65	
	CY7C412-65 DC	D16	
	CY7C412-65 LC	L55	
	CY7C412-65 DMB	D16	Military
	CY7C412-65 LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C424-30 PC	P15	Commercial
	CY7C424-30 JC	J65	
	CY7C424-30 DC	D16	
	CY7C424-30 LC	L55	
	CY7C424-30 DMB	D16	Military
	CY7C424-30 LMB	L55	
40	CY7C424-40 PC	P15	Commercial
	CY7C424-40 JC	J65	
	CY7C424-40 DC	D16	
	CY7C424-40 LC	L55	
	CY7C424-40 DMB	D16	Military
	CY7C424-40 LMB	L55	
65	CY7C424-65 PC	P15	Commercial
	CY7C424-65 JC	J65	
	CY7C424-65 DC	D16	
	CY7C424-65 LC	L55	
	CY7C424-65 DMB	D16	Military
	CY7C424-65 LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C429-30 PC	P15	Commercial
	CY7C429-30 JC	J65	
	CY7C429-30 DC	D16	
	CY7C429-30 LC	L55	
	CY7C429-30 DMB	D16	Military
	CY7C429-30 LMB	L55	
40	CY7C429-40 PC	P15	Commercial
	CY7C429-40 JC	J65	
	CY7C429-40 DC	D16	
	CY7C429-40 LC	L55	
	CY7C429-40 DMB	D16	Military
	CY7C429-40 LMB	L55	
65	CY7C429-65 PC	P15	Commercial
	CY7C429-65 JC	J65	
	CY7C429-65 DC	D16	
	CY7C429-65 LC	L55	
	CY7C429-65 DMB	D16	Military
	CY7C429-65 LMB	L55	

CYPRESS
SEMICONDUCTOR

CY7C510

16 x 16 Multiplier Accumulator

Features

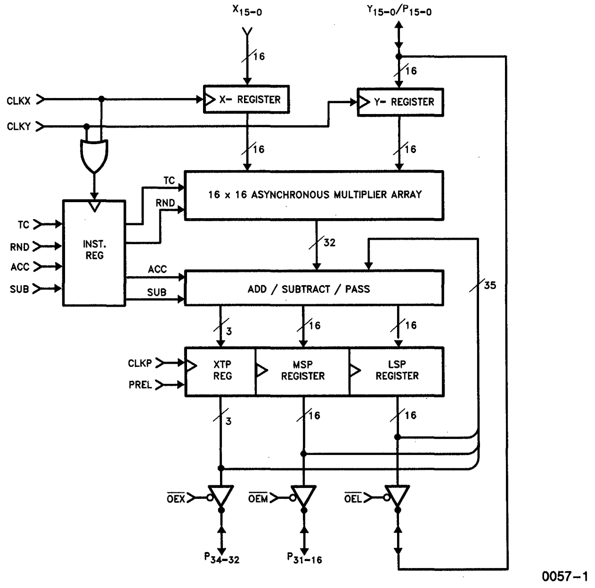
- **Fast**
  - **— CY7C510-45 has a 45 ns (max.) clock cycle (commercial)**
  - **— CY7C510-55 has a 55 ns (max.) clock cycle (military)**
- **Low Power**
  - **— I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} Margin**
  - **— 5V ± 10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **16 × 16 bit parallel multiplication with accumulation to 35-bit result**
- **Two's complement or unsigned magnitude operation**
- **ESD Protection**
  - **— Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functionally equivalent to Am29510 and TMC2110**

Functional Description

The CY7C510 is a high-speed 16 × 16 parallel multiplier accumulator which operates at 45 ns clocked multiply accumulate (MAC) time (22 MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instructions) and outputs are registered. These independently clocked registers are positive edge triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and MSP have dedicated ports for three-state output; the LSP is multiplexed with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

Logic Block Diagram



X15–0
Y15–0/P15–0
16
X– REGISTER
Y– REGISTER
CLKX
CLKY
16
16
16
TC
RND
16 x 16 ASYNCHRONOUS MULTIPLIER ARRAY
TC
RND
ACC
SUB
INST. REG
32
ACC
SUB
ADD / SUBTRACT / PASS
35
3
16
16
CLKP
PREL
XTP REG
MSP REGISTER
LSP REGISTER
3
16
16
OEX
OEM
OEL
P34–32
P31–16
0057–1

Selection Guide

		7C510-45	7C510-55	7C510-65	7C510-75
Maximum Multiply-Accumulate Time (ns)	Commercial	45	55	65	75
	Military		55	65	75

Maximum Ratings

(Above which the useful life may be impaired)

Ambient Temperature Under Bias .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

DC Voltage Applied to Outputs ..... −0.5V to V_{CC} Max.

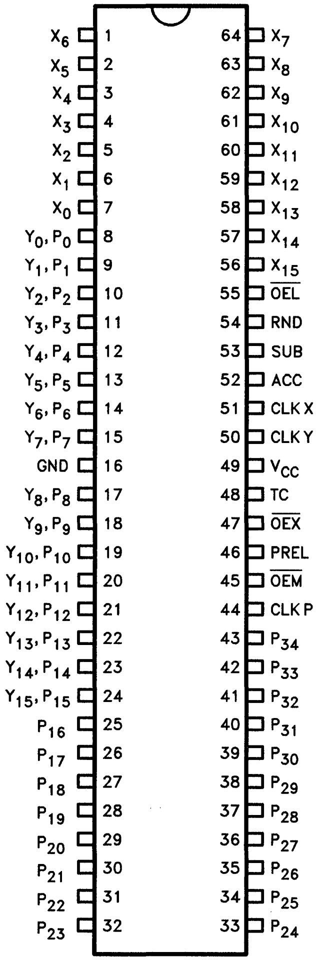
Output Current, into Outputs (low)............. 10 mA

Static Discharge Voltage (per Mil. Std. 883) ..... >2001V

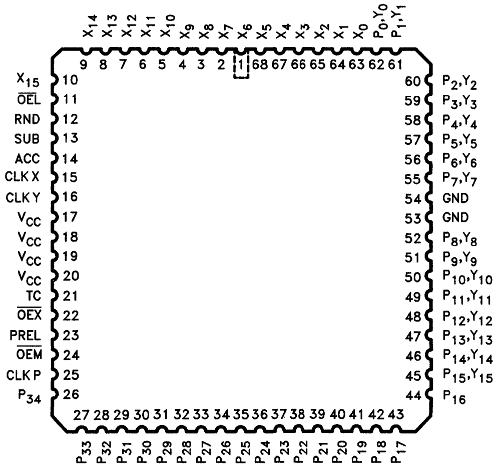
Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55° to +125°C	5V ±10%

Pin Configurations


X_6 1
X_5 2
X_4 3
X_3 4
X_2 5
X_1 6
X_0 7
Y_0, P_0 8
Y_1, P_1 9
Y_2, P_2 10
Y_3, P_3 11
Y_4, P_4 12
Y_5, P_5 13
Y_6, P_6 14
Y_7, P_7 15
GND 16
Y_8, P_8 17
Y_9, P_9 18
Y_{10}, P_{10} 19
Y_{11}, P_{11} 20
Y_{12}, P_{12} 21
Y_{13}, P_{13} 22
Y_{14}, P_{14} 23
Y_{15}, P_{15} 24
P_{16} 25
P_{17} 26
P_{18} 27
P_{19} 28
P_{20} 29
P_{21} 30
P_{22} 31
P_{23} 32
64 X_7
63 X_8
62 X_9
61 X_{10}
60 X_{11}
59 X_{12}
58 X_{13}
57 X_{14}
56 X_{15}
55 $\overline{OEL}$
54 RND
53 SUB
52 ACC
51 CLK X
50 CLK Y
49 V_{CC}
48 TC
47 $\overline{OEX}$
46 PREL
45 $\overline{OEM}$
44 CLK P
43 P_{34}
42 P_{33}
41 P_{32}
40 P_{31}
39 P_{30}
38 P_{29}
37 P_{28}
36 P_{27}
35 P_{26}
34 P_{25}
33 P_{24}

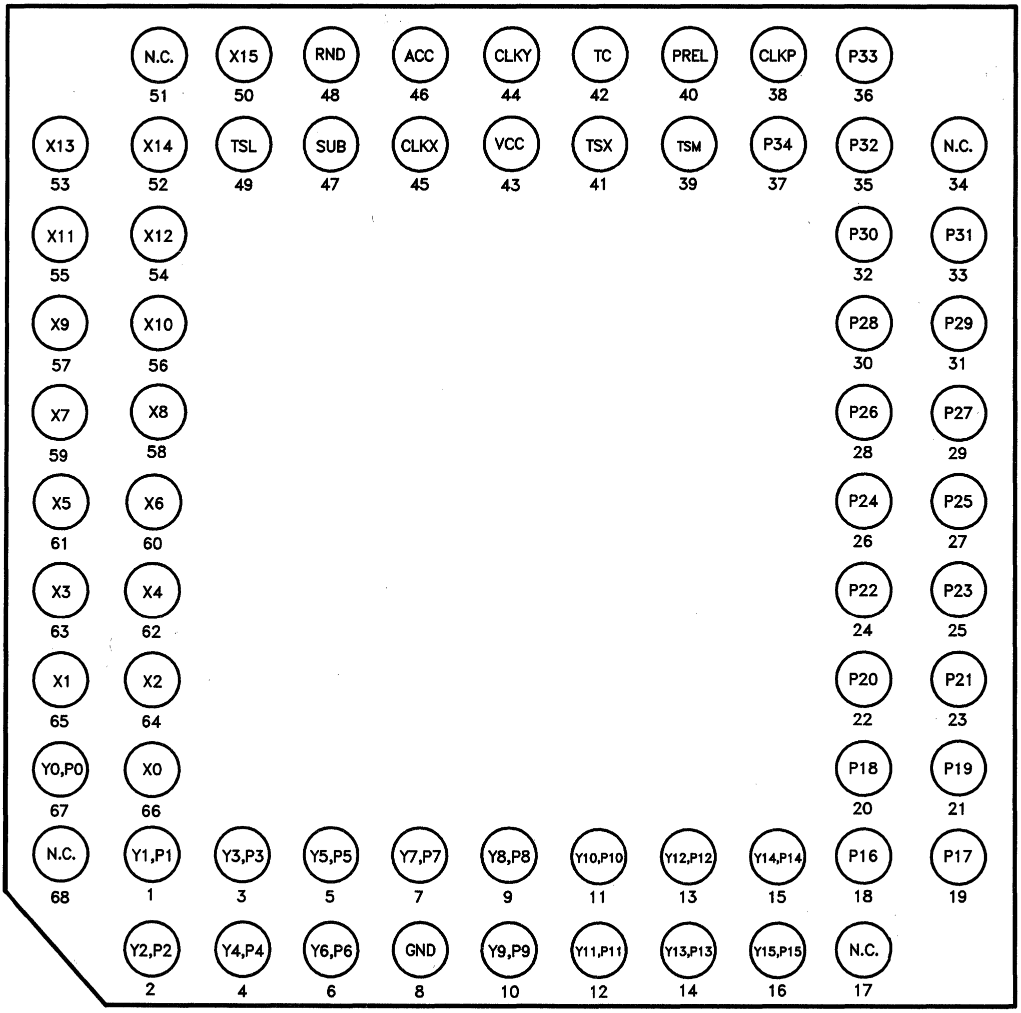
0057-2


X_{14} X_{13} X_{12} X_{11} X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0 P_0,Y_0 P_1,Y_1
9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
X_{15} 10
$\overline{OEL}$ 11
RND 12
SUB 13
ACC 14
CLK X 15
CLK Y 16
V_{CC} 17
V_{CC} 18
V_{CC} 19
V_{CC} 20
TC 21
$\overline{OEX}$ 22
PREL 23
$\overline{OEM}$ 24
CLK P 25
P_{34} 26
60 P_2,Y_2
59 P_3,Y_3
58 P_4,Y_4
57 P_5,Y_5
56 P_6,Y_6
55 P_7,Y_7
54 GND
53 GND
52 P_8,Y_8
51 P_9,Y_9
50 P_{10},Y_{10}
49 P_{11},Y_{11}
48 P_{12},Y_{12}
47 P_{13},Y_{13}
46 P_{14},Y_{14}
45 P_{15},Y_{15}
44 P_{16}
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
P_{33} P_{32} P_{31} P_{30} P_{29} P_{28} P_{27} P_{26} P_{25} P_{24} P_{23} P_{22} P_{21} P_{20} P_{19} P_{18} P_{17}

0057-3

Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array


N.C. 51
X15 50
RND 48
ACC 46
CLKY 44
TC 42
PREL 40
CLKP 38
P33 36
X13 53
X14 52
TSL 49
SUB 47
CLKX 45
VCC 43
TSX 41
TSM 39
P34 37
P32 35
N.C. 34
X11 55
X12 54
P30 32
P31 33
X9 57
X10 56
P28 30
P29 31
X7 59
X8 58
P26 28
P27 29
X5 61
X6 60
P24 26
P25 27
X3 63
X4 62
P22 24
P23 25
X1 65
X2 64
P20 22
P21 23
Y0,P0 67
X0 66
P18 20
P19 21
N.C. 68
Y1,P1 1
Y3,P3 3
Y5,P5 5
Y7,P7 7
Y8,P8 9
Y10,P10 11
Y12,P12 13
Y14,P14 15
P16 18
P17 19
Y2,P2 2
Y4,P4 4
Y6,P6 6
GND 8
Y9,P9 10
Y11,P11 12
Y13,P13 14
Y15,P15 16
N.C. 17

0057–13

Pin Definitions

Signal Name	I/O	Description
X_{15-0}	I	X-Input Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	Y-Input Data/LSP Output Data. When this port is used to input a Y value, the 16-bit number may be interpreted as two's complement or unsigned magnitude. This bidirectional port is multiplexed with the LSP output (P_{15-0}), and can also be used to preload the LSP register.
P_{34-32}	I/O	Extended Product (XTP) Output Data. This port is bidirectional. The extended product emerges through this port. The XTP register may also be preloaded through this port.
P_{31-16}	I/O	MSP Output Data. This port is bidirectional. The most significant product emerges through this port. The MSP register may also be preloaded through this port.
P_{15-0}	I/O	LSP Output Data. This port is bidirectional. The least significant product emerges through this port. The LSP register may also be preloaded through this port.
CLKX	I	X-Register Clock. X-Input Data are latched into the X-register at the rising edge of CLKX.
CLKY	I	Y-Register Clock. Y-Input Data are latched into the Y-register at the rising edge of CLKY.
CLKP	I	Product Register Clock. XTP, MSP, and LSP are latched into their respective registers at the rising edge of CLKP. If preload is selected, these registers are loaded with the preload data at the output pins via the bidirectional ports. If preload is not selected, these registers are loaded with the current accumulated product.
$\overline{\text{OEX}}$	I	Output Enable Extended. When LOW, the extended product bidirectional port is enabled for output. When HIGH, the outputs drivers are disabled (high impedance) and the XTP port may be used for preloading. See Preload Function Table.
$\overline{\text{OEM}}$	I	Output Enable Most. When LOW, the MSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.
$\overline{\text{OEL}}$	I	Output Enable Least. When LOW, the LSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.
PREL	I	Preload. When HIGH, the three bidirectional ports may be used to preload data into the accumulator register at the rising edge of CLKP. The three-state controls ($\overline{\text{OEX}}$, $\overline{\text{OEM}}$, $\overline{\text{OEL}}$) must be HIGH to preload data. When LOW, the accumulated product is loaded into the accumulator/output register at the rising edge of CLKP. The output drivers must be enabled ($\overline{\text{OEX}}$, $\overline{\text{OEM}}$, $\overline{\text{OEL}}$ must be LOW) for the accumulated product to be output. Ordinarily, PREL, $\overline{\text{OEX}}$, $\overline{\text{OEM}}$, and $\overline{\text{OEL}}$ are tied together. See accumulator function table.
TC	I	Two's Complement Control. When HIGH, the 7C510 is in two's complement mode, where the input and output data are interpreted as two's complement numbers. The device is in unsigned magnitude mode when TC is LOW. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
RND	I	Round Control. When HIGH, rounding is enabled and a "1" is added to the MSB of the LSB (P_{15}). When LOW, the product is unchanged. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
ACC	I	Accumulate Control. When HIGH, the accumulator/output register contents are added to or subtracted from the current product (XY) and this result is stored back into the accumulator/output register. When LOW, the product is loaded into the accumulator register, overwriting the current contents. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.
SUB	I	Subtract Control. When both ACC and SUB are HIGH, the accumulator register contents are subtracted from the current product XY and this result is written back into the accumulator register. When ACC is HIGH and SUB is LOW, the accumulator register contents and current product are summed, then written back to the accumulator register. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.

Functional Description

The CY7C510 is a high-speed 16 × 16-bit multiplier accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instructions) and outputs are registered. The 7C510 is divided into four sections: the input section, the 16 × 16 asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the X and Y operands, clocked by the rising edge of CLKX and CLKY, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLKX, CLKY.

The 16 × 16 asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on control TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P_{15}). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{\text{OEX}}$, $\overline{\text{OEM}}$, and $\overline{\text{OEL}}$. When PREL is HIGH, the output buffers are in high impedance state. When the controls $\overline{\text{OEX}}$, $\overline{\text{OEM}}$, and $\overline{\text{OEL}}$ are also high, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLKP. When PREL is LOW, the signals $\overline{\text{OEX}}$, $\overline{\text{OEM}}$, and $\overline{\text{OEL}}$ are enable controls for their respective three-state output ports.

Preload Function Table

PREL	$\overline{\text{OEX}}$	$\overline{\text{OEM}}$	$\overline{\text{OEL}}$	Output Register		
				XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = Output buffers at High impedance (disabled.)

Q = Output buffers at Low impedance. Contents of output register available through output ports.

PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKP.

Accumulator Function Table

PREL	ACC	SUB	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

CY7C510
Input Formats

Fractional Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Integer Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Unsigned Fractional Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

CY7C510
Output Formats

Two's Complement Fractional Output

XTP

34	33	32
-2^{4}	2^{3}	2^{2}
(Sign)		

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Two's Complement Integer Output

XTP

34	33	32
-2^{34}	2^{33}	2^{32}
(Sign)		

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

XTP

34	33	32
2^{2}	2^{1}	2^{0}

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

XTP

34	33	32
2^{34}	2^{33}	2^{32}

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −0.4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V	−0.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V	4.0		mA
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_{IN} = 7.0V		10	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V	−3	−30	mA
I_{OZL}	Output OFF (Hi-Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V		−25	μA
I_{OZH}	Output OFF (Hi-Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V	25		μA
I_{CC} (Q1)[2]	Supply Current (Quiescent)	V_{CC} = Max., V_{IN} = [GND to V_{IL}] or [V_{IH} to V_{CC}]		30	mA
I_{CC} (Q2)[2]	Supply Current (Quiescent)	V_{CC} = Max V_{CC} ≥ V_{IN} ≥ 3.85V 0.4V ≥ V_{IN} ≥ GND — Commercial		20	mA
		Military		25	
I_{CC} (Max.)[2]	Supply Current — Commercial	V_{CC} = Max., f_{CLK} = 10 MHz		100	mA
	Military			110	

Capacitance[3]

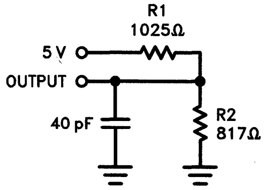
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. For I_{CC} measurements, the outputs are three-stated. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC} (A.C.), where I_{CC} (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC} (A.C.) = (8 mA/MHz) × Clock Frequency for Military temperature range.
3. Tested on a sample basis.

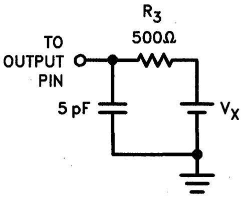
Output Loads Used for A.C. Performance Characteristics

Normal Load (Load 1)



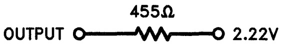
0057-4

Three-State Delay Load (Load 2)



0057-5

Equivalent to: THÉVENIN EQUIVALENT

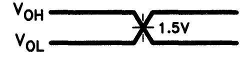
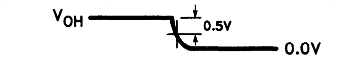
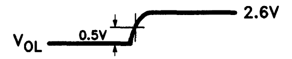
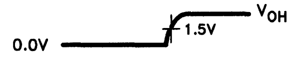
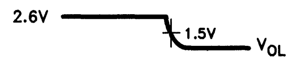


0057-6

Switching Characteristics Over Operating Range

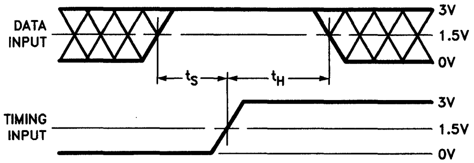
Parameters	Description		7C510-45		7C510-55		7C510-65		7C510-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply Accumulate Time			45		55		65		75	ns
t_S	Setup Time		20		20		25		25		ns
t_H	Hold Time		3		3		3		3		ns
t_{PW}	Clock Pulse Width		25		25		30		30		ns
t_{PDP}	Output Clock to P			30		30		35		35	ns
t_{PDY}	Output Clock to Y			30		30		35		35	ns
t_{PHZ}	$\overline{\text{OEX}}$, $\overline{\text{OEM}}$ to P; $\overline{\text{OEL}}$ to Y (Disable Time)	HIGH to Z		25		25		30		30	ns
t_{PLZ}		LOW to Z		25		25		30		30	ns
t_{PZH}	$\overline{\text{OEX}}$, $\overline{\text{OEM}}$ to P; $\overline{\text{OEL}}$ to Y (Enable Time)	Z to HIGH		30		30		35		35	ns
t_{PZL}		Z to LOW		30		30		35		35	ns
t_{HCL}	Relative Hold Time		0		0		0				ns

Test Waveforms

TEST	V_X	OUTPUT WAVEFORM – MEASUREMENT LEVEL
ALL t_{PD}'s	V_{CC}	
t_{PHZ}	0.0V	
t_{PLZ}	2.6V	
t_{PZH}	0.0V	
t_{PZL}	2.6V	

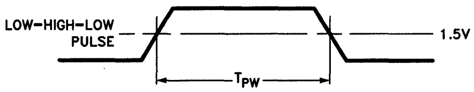
0057-7

Setup and Hold Time


DATA
INPUT
3V
1.5V
0V
tS
tH
TIMING
INPUT
3V
1.5V
0V

0057-8

Pulse Width

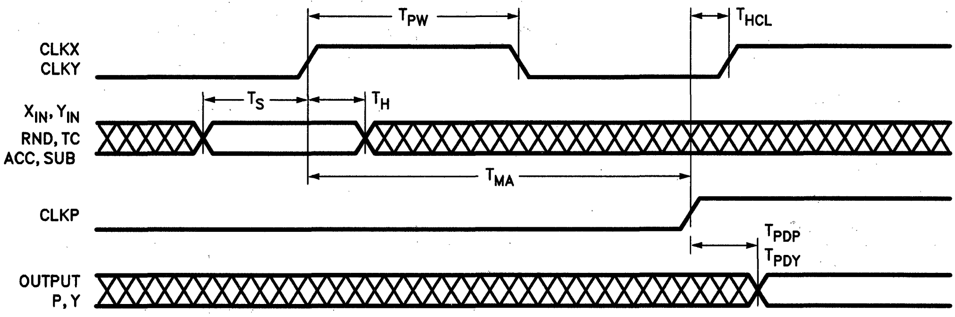

LOW-HIGH-LOW
PULSE
1.5V
TPW

0057-9

Notes:

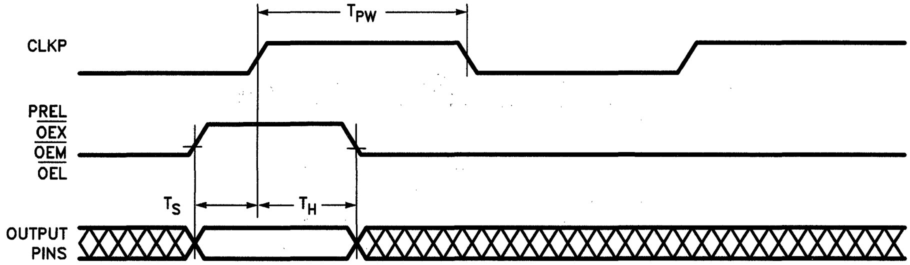
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

CY7C510 Timing Diagram


TPW
THCL
CLKX
CLKY
TS
TH
XIN, YIN
RND, TC
ACC, SUB
TMA
CLKP
TPDP
TPDY
OUTPUT
P, Y

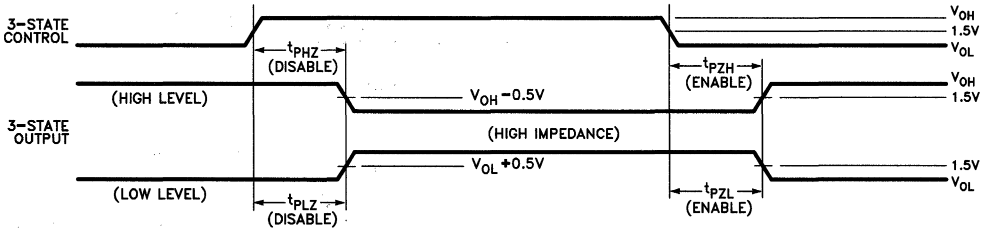
0057-10

Preload Timing Diagram


TPW
CLKP
PREL
OEX
OEM
OEL
TS
TH
OUTPUT
PINS

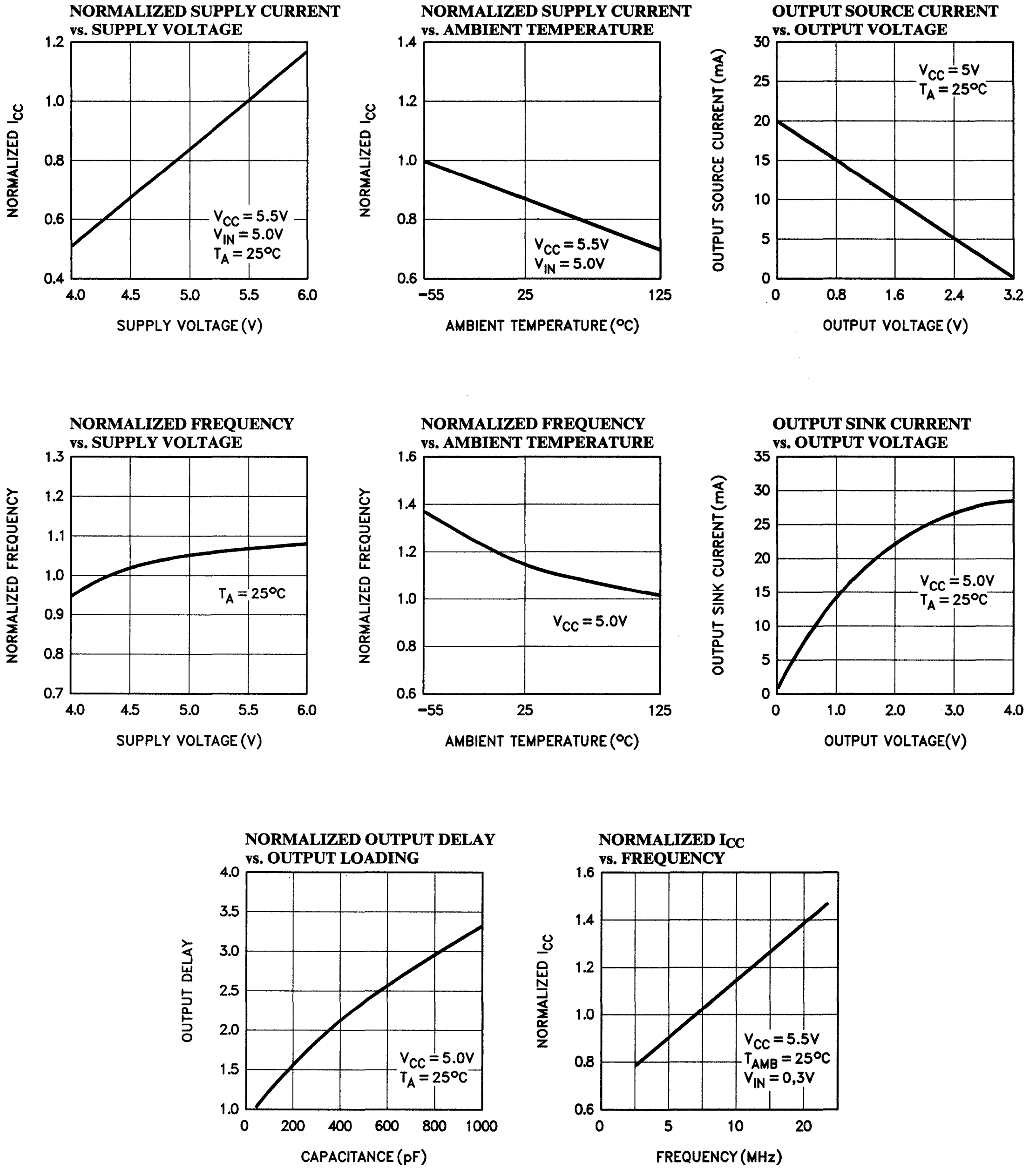
0057-11

Three-State Timing Diagram


3-STATE
CONTROL
tPHZ
(DISABLE)
tPZH
(ENABLE)
VOH
1.5V
VOL
(HIGH LEVEL)
VOH −0.5V
VOH
1.5V
3-STATE
OUTPUT
(HIGH IMPEDANCE)
VOL +0.5V
1.5V
VOL
(LOW LEVEL)
tPLZ
(DISABLE)
tPZL
(ENABLE)

0057-12

Typical AC and DC Characteristics



0057-14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C510-45 PC	P29	Commercial
	CY7C510-45 LC	L81	
	CY7C510-45 JC	J81	
	CY7C510-45 DC	D30	
	CY7C510-45 GC	G68	
55	CY7C510-55 PC	P29	Commercial
	CY7C510-55 LC	L81	
	CY7C510-55 JC	J81	
	CY7C510-55 DC	D30	
	CY7C510-55 GC	G68	
	CY7C510-55 LMB	L81	Military
	CY7C510-55 DMB	D30	
	CY7C510-55 GMB	G68	
65	CY7C510-65 PC	P29	Commercial
	CY7C510-65 LC	L81	
	CY7C510-65 JC	J81	
	CY7C510-65 DC	D30	
	CY7C510-65 GC	G68	
	CY7C510-65 LMB	L81	Military
	CY7C510-65 DMB	D30	
	CY7C510-65 GMB	G68	
75	CY7C510-75 PC	P29	Commercial
	CY7C510-75 LC	L81	
	CY7C510-75 JC	J81	
	CY7C510-75 DC	D30	
	CY7C510-75 GC	G68	
	CY7C510-75 LMB	L81	Military
	CY7C510-75 DMB	D30	
	CY7C510-75 GMB	G68	

CYPRESS SEMICONDUCTOR

CY7C516
CY7C517

16 x 16 Multipliers

Features

- **Fast**
  - **38 ns clock cycle (commercial)**
  - **42 ns clock cycle (military)**
- **Low Power**
  - **I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} Margin**
  - **5V ±10%**
  - **All parameters guaranteed over commercial and military operating temperature range**
- **16 x 16 bit parallel multiplication with full precision 32-bit product output**
- **Two's complement, unsigned magnitude, or mixed mode multiplication**
- **CY7C516 pin compatible and functionally equivalent to Am29516, MPY016K, MPY016H**
- **CY7C517 pin compatible and functionally equivalent to Am29517**

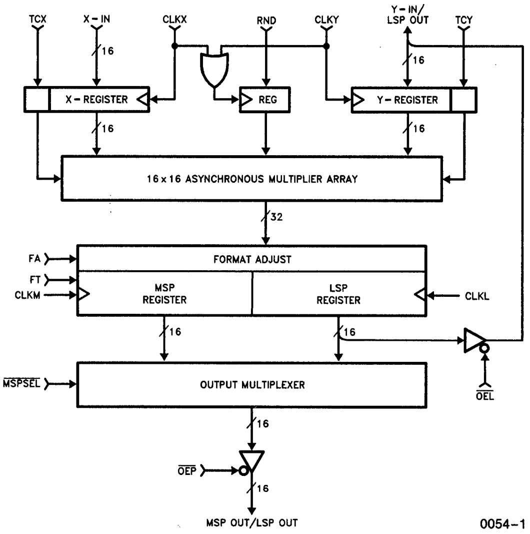
Functional Description

The CY7C516/517 are high-speed 16 x 16 parallel multipliers which operate at 38 ns clocked multiply times (26 MHz multiplication rate). The two input operands may be independently specified as either two's complement or unsigned magnitude numbers. Controls are provided for rounding and format adjustment of the full precision 32-bit product.

On the 7C516, individually clocked input and output registers are provided to maximize throughput and to simplify bus interfacing. On the 7C517, a single clock (CLK) is provided, along with three register enables. This facilitates the use of the 7C517 in microprogrammed systems. The input and output registers are positive edge triggered D-type flip-flops. The output register may be made transparent for asynchronous output.

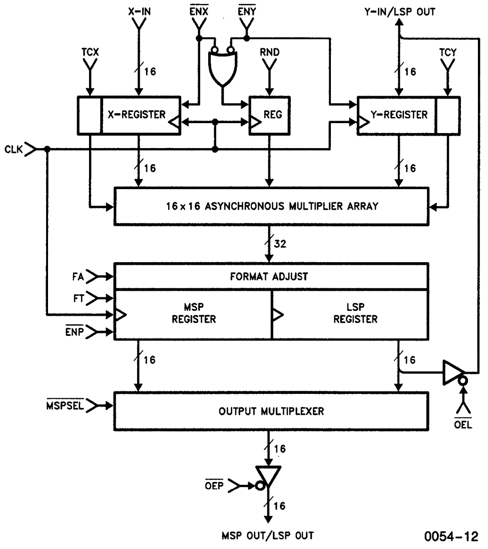
Logic Block Diagrams

CY7C516


TCX
X-IN
16
CLKX
RND
CLKY
Y-IN/LSP OUT
TCY
16
X-REGISTER
REG
Y-REGISTER
16
16
16 x 16 ASYNCHRONOUS MULTIPLIER ARRAY
32
FA
FT
CLKM
FORMAT ADJUST
MSP REGISTER
LSP REGISTER
CLKL
16
16
$\overline{\text{MSPSEL}}$
OUTPUT MULTIPLEXER
$\overline{\text{OEL}}$
16
$\overline{\text{OEP}}$
16
MSP OUT/LSP OUT

0054-1

CY7C517


X-IN
$\overline{\text{ENX}}$
$\overline{\text{ENY}}$
Y-IN/LSP OUT
TCX
16
RND
TCY
16
X-REGISTER
REG
Y-REGISTER
CLK
16
16
16 x 16 ASYNCHRONOUS MULTIPLIER ARRAY
32
FA
FT
FORMAT ADJUST
MSP REGISTER
LSP REGISTER
$\overline{\text{ENP}}$
16
16
$\overline{\text{MSPSEL}}$
OUTPUT MULTIPLEXER
$\overline{\text{OEL}}$
16
$\overline{\text{OEP}}$
16
MSP OUT/LSP OUT

0054-12

Selection Guide

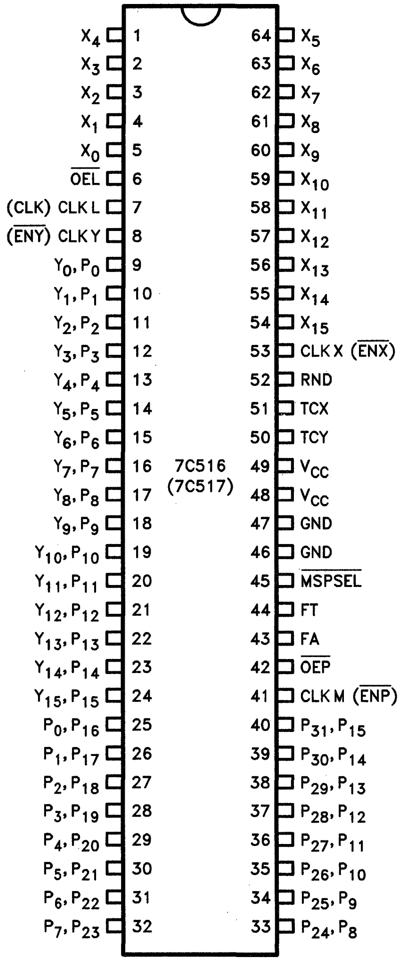
		7C516-38 7C517-38	7C516-42 7C517-42	7C516-45 7C517-45	7C516-55 7C517-55	7C516-75 7C517-75
Maximum Multiply Time (ns) Clocked/Unclocked	Commercial	38/58		45/65	55/75	75/100
	Military		42/65		55/75	75/100

Functional Description (Continued)

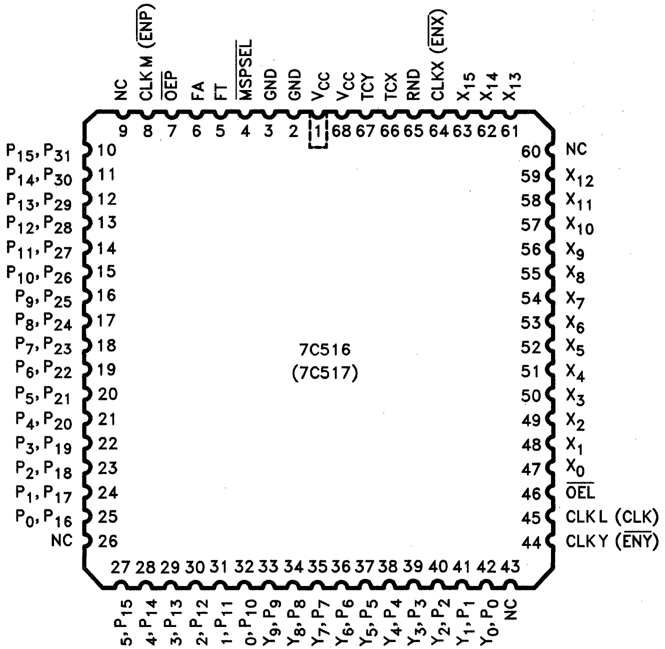
Two output modes may be selected by using the output multiplexer control, $\overline{\text{MSPSEL}}$. Holding $\overline{\text{MSPSEL}}$ LOW causes the most significant product (MSP) to be available at the dedicated output port. The LSP is simultaneously available at the bidirectional port shared with the Y-inputs.

The other mode of output involves toggling of the $\overline{\text{MSPSEL}}$ control, allowing both the MSP and LSP to be available for output through the dedicated 16-bit output port.

Pin Configurations


1 X_4
2 X_3
3 X_2
4 X_1
5 X_0
6 $\overline{\text{OEL}}$
7 (CLK) CLKL
8 ($\overline{\text{ENY}}$) CLKY
9 Y_0, P_0
10 Y_1, P_1
11 Y_2, P_2
12 Y_3, P_3
13 Y_4, P_4
14 Y_5, P_5
15 Y_6, P_6
16 Y_7, P_7
17 Y_8, P_8
18 Y_9, P_9
19 Y_{10}, P_{10}
20 Y_{11}, P_{11}
21 Y_{12}, P_{12}
22 Y_{13}, P_{13}
23 Y_{14}, P_{14}
24 Y_{15}, P_{15}
25 P_0, P_{16}
26 P_1, P_{17}
27 P_2, P_{18}
28 P_3, P_{19}
29 P_4, P_{20}
30 P_5, P_{21}
31 P_6, P_{22}
32 P_7, P_{23}
64 X_5
63 X_6
62 X_7
61 X_8
60 X_9
59 X_{10}
58 X_{11}
57 X_{12}
56 X_{13}
55 X_{14}
54 X_{15}
53 CLKX ($\overline{\text{ENX}}$)
52 RND
51 TCX
50 TCY
49 V_{CC}
48 V_{CC}
47 GND
46 GND
45 $\overline{\text{MSPSEL}}$
44 FT
43 FA
42 $\overline{\text{OEP}}$
41 CLKM ($\overline{\text{ENP}}$)
40 P_{31}, P_{15}
39 P_{30}, P_{14}
38 P_{29}, P_{13}
37 P_{28}, P_{12}
36 P_{27}, P_{11}
35 P_{26}, P_{10}
34 P_{25}, P_9
33 P_{24}, P_8
7C516
(7C517)

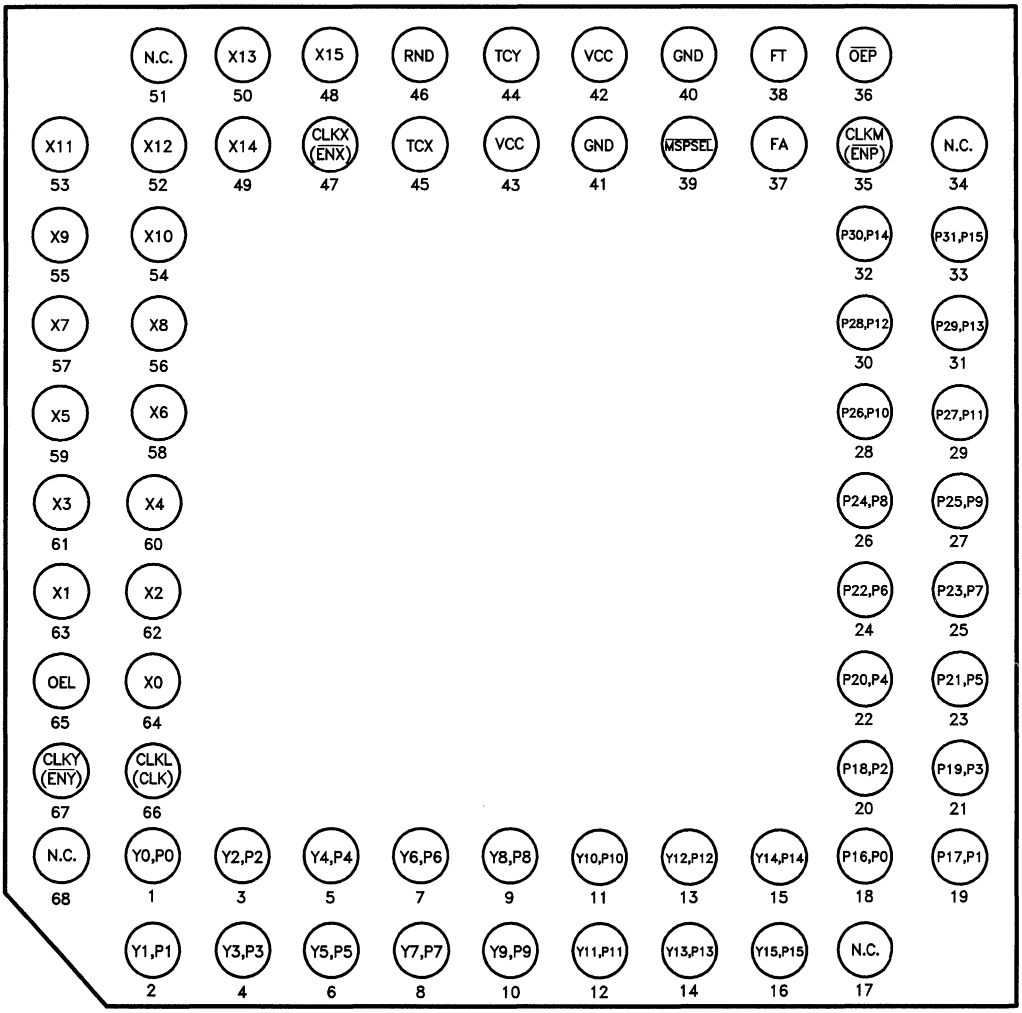
0054-2


9 NC
8 CLKM ($\overline{\text{ENP}}$)
7 $\overline{\text{OEP}}$
6 FA
5 FT
4 $\overline{\text{MSPSEL}}$
3 GND
2 GND
1 V_{CC}
68 V_{CC}
67 TCY
66 TCX
65 RND
64 CLKX ($\overline{\text{ENX}}$)
63 X_{15}
62 X_{14}
61 X_{13}
10 P_{15}, P_{31}
11 P_{14}, P_{30}
12 P_{13}, P_{29}
13 P_{12}, P_{28}
14 P_{11}, P_{27}
15 P_{10}, P_{26}
16 P_9, P_{25}
17 P_8, P_{24}
18 P_7, P_{23}
19 P_6, P_{22}
20 P_5, P_{21}
21 P_4, P_{20}
22 P_3, P_{19}
23 P_2, P_{18}
24 P_1, P_{17}
25 P_0, P_{16}
26 NC
27 Y_{15}, P_{15}
28 Y_{14}, P_{14}
29 Y_{13}, P_{13}
30 Y_{12}, P_{12}
31 Y_{11}, P_{11}
32 Y_{10}, P_{10}
33 Y_9, P_9
34 Y_8, P_8
35 Y_7, P_7
36 Y_6, P_6
37 Y_5, P_5
38 Y_4, P_4
39 Y_3, P_3
40 Y_2, P_2
41 Y_1, P_1
42 Y_0, P_0
43 NC
60 NC
59 X_{12}
58 X_{11}
57 X_{10}
56 X_9
55 X_8
54 X_7
53 X_6
52 X_5
51 X_4
50 X_3
49 X_2
48 X_1
47 X_0
46 $\overline{\text{OEL}}$
45 CLKL (CLK)
44 CLKY ($\overline{\text{ENY}}$)
7C516
(7C517)

0054-3

Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array


N.C. 51
X13 50
X15 48
RND 46
TCY 44
VCC 42
GND 40
FT 38
$\overline{OEP}$ 36
X11 53
X12 52
X14 49
CLKX ($\overline{ENX}$) 47
TCX 45
VCC 43
GND 41
$\overline{MSPSEL}$ 39
FA 37
CLKM ($\overline{ENP}$) 35
N.C. 34
X9 55
X10 54
P30,P14 32
P31,P15 33
X7 57
X8 56
P28,P12 30
P29,P13 31
X5 59
X6 58
P26,P10 28
P27,P11 29
X3 61
X4 60
P24,P8 26
P25,P9 27
X1 63
X2 62
P22,P6 24
P23,P7 25
OEL 65
X0 64
P20,P4 22
P21,P5 23
CLKY ($\overline{ENY}$) 67
CLKL (CLK) 66
P18,P2 20
P19,P3 21
N.C. 68
Y0,P0 1
Y2,P2 3
Y4,P4 5
Y6,P6 7
Y8,P8 9
Y10,P10 11
Y12,P12 13
Y14,P14 15
P16,P0 18
P17,P1 19
Y1,P1 2
Y3,P3 4
Y5,P5 6
Y7,P7 8
Y9,P9 10
Y11,P11 12
Y13,P13 14
Y15,P15 16
N.C. 17

0054–16

Maximum Ratings

(Above which the useful life may be impaired)

Ambient Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential .... −0.5V to +7.0V
DC Input Voltage .... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to V_{CC} Max.
Output Current, into Outputs (low)............. 10 mA
Static Discharge Voltage .... > 1000V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Pin Definitions

Signal Name	I/O	Description
X_{15-0}	I	**X-Input Data.** This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	**Y-Input/LSP Output Data.** This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y-input port may be multiplexed with the LSP output (P_{15-0}).
P_{31-16} (P_{15-0})	O	**Output Data.** This 16-bit port may carryeither the MSP (P_{31-16}) or the LSP (P_{15-0}).
FT	I	The MSP and LSP registers are made transparent (asynchronous operation) if FT is HIGH.
FA	I	**Format Adjust Control.** If FA is HIGH, a full 32-bit product is output. If FA is LOW, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be HIGH for two's complement integer, unsigned magnitude, and mixed mode multiplication.
$\overline{\text{MSPSEL}}$	I	**Output Multiplexer Control.** When $\overline{\text{MSPSEL}}$ is LOW, the MSP is available for output at the MSP output port, and the LSP is available at the Y-input/LSP output port. When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports (above) and the MSP is not available.
RND	I	**Round Control.** When RND is HIGH, a one is added to the MSB of the LSP. This position is dependent on the FA control; FA = HIGH means RND adds to the 2^{-15} bit (P_{15}), FA = LOW means RND adds to the 2^{-16} bit (P_{14}).
TCX	I	**Two's Complement Control X.** X-input data are interpreted as two's complement when TCX is HIGH. TCX LOW means the data are interpreted as unsigned magnitude.
TCY	I	**Two's Complement Control Y.** Y-Input data are interpeted as two's complement when TCY is HIGH. TCY LOW means the data are interpreted as unsigned magnitude.
$\overline{\text{OEP}}$	I	**P_{31-16}/P_{15-0} Output Port Three-State Control.** When $\overline{\text{OEP}}$ is LOW, the output port is enabled; when $\overline{\text{OEP}}$ is HIGH, the drivers are in a high impedance state.
$\overline{\text{OEL}}$	I	**Y-in/P_{15-0} Port Three State Control.** When $\overline{\text{OEL}}$ is LOW, the timeshared port is enabled for LSP output. When $\overline{\text{OEL}}$ is HIGH, the output drivers are in a high impedance state. This is required for Y-input.
CY7C516 Only		
CLKX	I	**X-Register Clock.** X-input data and TCX are latched in at the rising edge of CLKX.
CLKY	I	**Y-Register Clock.** Y-input data and TCY are latched in at the rising edge of CLKY.
CLKM	I	**MSP Register Clock.** The most significant product (MSP) is latched in at the MSP Register at the rising edge of CLKM.
CLKL	I	**LSP Register Clock.** The least significant product (LSP) is latched in at the LSP Register at the rising edge of CLKL.
CY7C517 Only		
CLK	I	**Clock.** All enabled registers latch in their data at the rising edge of CLK.
$\overline{\text{ENX}}$	I	**X-Register Enable.** When $\overline{\text{ENX}}$ is LOW, the X-Register is enabled. X-input data and TCX will be latched in at the rising edge of CLK when the register is enabled. When $\overline{\text{ENX}}$ is HIGH, the X-Register is in hold mode.
$\overline{\text{ENY}}$	I	**X-Register Enable.** $\overline{\text{ENY}}$ enables the Y-Register. (See $\overline{\text{ENX}}$.)
$\overline{\text{ENP}}$	I	**Product Register Enable.** $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP Sections are enabled by $\overline{\text{ENP}}$. (See $\overline{\text{ENX}}$.)

Input Formats (All Devices)

Fractional Two's Complement Input Format

TCX, TCY = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Integer Two's Complement Input Format

TCX, TCY = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Unsigned Fractional Input Format

TCX, TCY = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input Format

TCX, TCY = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Output Formats (All Devices)

Fractional Two's Complement (Shifted)* Format

FA = 0

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)															

Fractional Two's Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Integer Two's Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1.000 . . . (−1) with itself, yielding a product of 1.000 . . . or −1.

Electrical Characteristics Over Operating Range

Parameters	Description		Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min., $I_{OH} = -0.4$ mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min., $I_{OL} = 4.0$ mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{OH}	Output HIGH Current		V_{CC} = Min., $V_{OH} = 2.4V$	−0.4		mA
I_{OL}	Output LOW Current		V_{CC} = Min., $V_{OL} = 0.4V$	4.0		mA
I_{IX}	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.	−10	10	μA
I_{OS}[1]	Output Short Circuit Current		V_{CC} = Max., V_{OUT} = 0V	−3	−30	mA
I_{OZL}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE} = 2.0V$		−25	μA
I_{OZH}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE} = 2.0V$	25		μA
I_{CC} (Q_1)[2]	Supply Current (Quiescent)	Commercial (-38)	GND $\leq V_{IN} \leq V_{IL}$ or $V_{IH} \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		40	mA
		Military (-42)			45	
		All Others			30	
I_{CC} (Q_2)[2]	Supply Current (Quiescent)	Commercial	GND $\leq V_{IN} \leq 0.4V$ or $3.85V \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		20	mA
		Military			25	
I_{CC} (Max.)[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH		100	mA
		Military			110	

Capacitance[3]

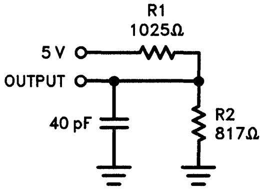
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC} (A.C.), where I_{CC} (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC} (A.C.) = (8 mA/MHz) × Clock Frequency for the Military temperature range.
3. Tested on a sample basis.

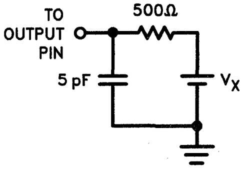
Output Loads Used for A.C. Performance Characteristics

Normal Load (Load 1)



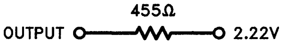
0054-4

Three-State Delay Load (Load 2)



0054-5

Equivalent to: THÉVENIN EQUIVALENT



0054-6

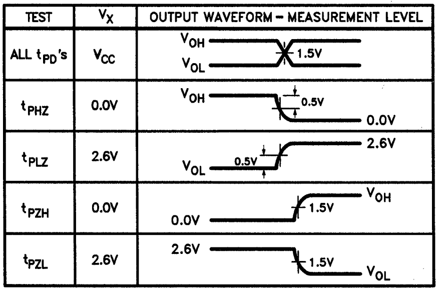
Switching Characteristics Over Operating Range

Parameters	Description		Test Conditions	7C516-38 7C517-38		7C516-42 7C517-42		7C516-45 7C517-45		7C516-55 7C517-55		7C516-75 7C517-75		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time		Load 1		58		65		65		75		100	ns
t_{MC}	Clocked Multiply Time				38		42		45		55		75	ns
t_S	X_i, Y_i, RND, TCX, TCY Set-up Time			7		8		20		20		25		ns
t_H	X_i, Y_i, RND, TCX, TCY Hold Time			3		3		3		3		3		ns
t_{SE}	$\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$ Set-up Time (7C517 Only)			10		15		20		20		25		ns
t_{HE}	$\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$ Hold Time (7C517 Only)			3		3		3		3		3		ns
t_{PWH}, t_{PWL}	Clock Pulse Width (HIGH and LOW)			10		10		20		25		30		ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out				18		21		25		25		30	ns
t_{PDP}	Output Clock to P				25		30		30		30		35	ns
t_{PDY}	Output Clock to Y				25		30		30		30		35	ns
t_{PHZ}	$\overline{\text{OEP}}$ Disable Time	HIGH to Z	Load 2		15		17		25		25		30	ns
t_{PLZ}		LOW to Z			15		17		25		25		30	ns
t_{PZH}	$\overline{\text{OEP}}$ Enable Time	Z to HIGH			23		25		30		30		35	ns
t_{PZL}		Z to LOW			23		25		30		30		35	ns
t_{PHZ}	$\overline{\text{OEL}}$ Disable Time	HIGH to Z			15		17		25		25		30	ns
t_{PLZ}		LOW to Z			15		17		25		25		30	ns
t_{PZH}	$\overline{\text{OEL}}$ Enable Time	Z to HIGH			23		25		30		30		35	ns
t_{PZL}		Z to LOW			23		25		30		30		35	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1]		Load 1	0		0		0		0		0		ns

Note:

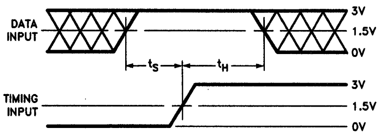
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

Test Waveforms (All Devices)


TEST
V_X
OUTPUT WAVEFORM – MEASUREMENT LEVEL
ALL t_{PD}'s
V_{CC}
V_{OH}
V_{OL}
1.5V
t_{PHZ}
0.0V
V_{OH}
0.5V
0.0V
t_{PLZ}
2.6V
2.6V
V_{OL}
0.5V
t_{PZH}
0.0V
V_{OH}
0.0V
1.5V
t_{PZL}
2.6V
2.6V
1.5V
V_{OL}

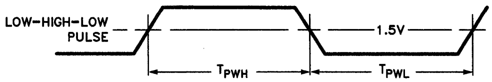
0054-7

Setup and Hold Time (All Devices)


DATA INPUT
3V
1.5V
0V
t_S
t_H
TIMING INPUT
3V
1.5V
0V

0054-8

Pulse Width (All Devices)

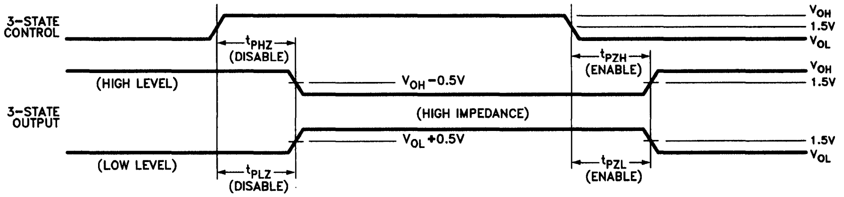

LOW-HIGH-LOW PULSE
1.5V
T_{PWH}
T_{PWL}

0054-9

Notes:

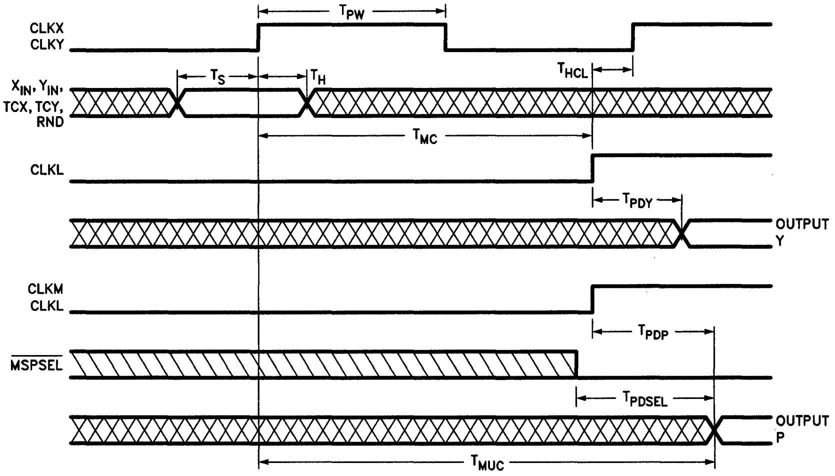
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Three-State Timing Diagram


3-STATE CONTROL
tPHZ
(DISABLE)
(HIGH LEVEL)
VOH -0.5V
3-STATE OUTPUT
(HIGH IMPEDANCE)
VOL +0.5V
(LOW LEVEL)
tPLZ
(DISABLE)
tPZH
(ENABLE)
tPZL
(ENABLE)
VOH
1.5V
VOL
VOH
1.5V
1.5V
VOL

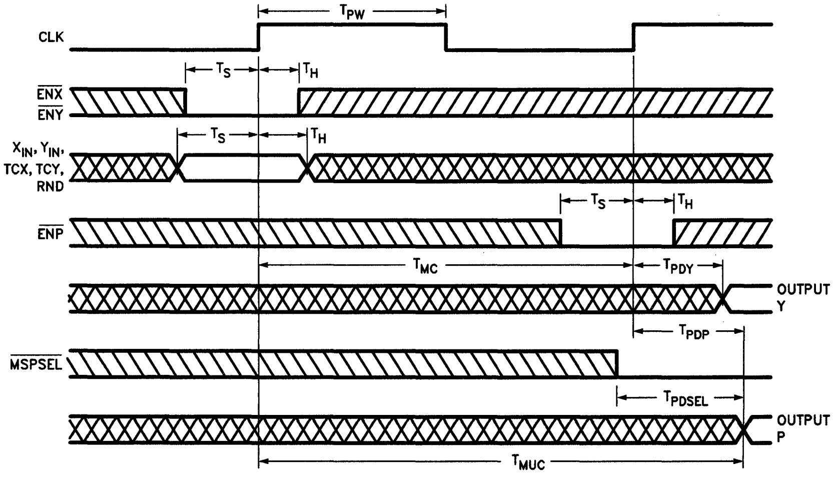
0054-10

Timing Diagram
7C516


TPW
CLKX
CLKY
TS
TH
THCL
XIN, YIN, TCX, TCY, RND
TMC
CLKL
TPDY
OUTPUT Y
CLKM
CLKL
TPDP
MSPSEL
TPDSEL
OUTPUT P
TMUC

0054-11

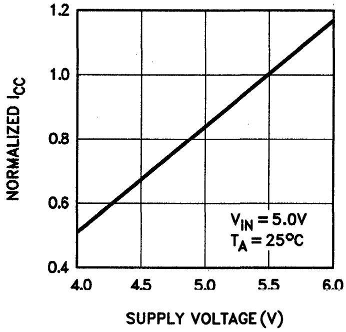
Timing Diagram
7C517


TPW
CLK
TS
TH
ENX
ENY
TS
TH
XIN, YIN, TCX, TCY, RND
TS
TH
ENP
TMC
TPDY
OUTPUT Y
TPDP
MSPSEL
TPDSEL
OUTPUT P
TMUC

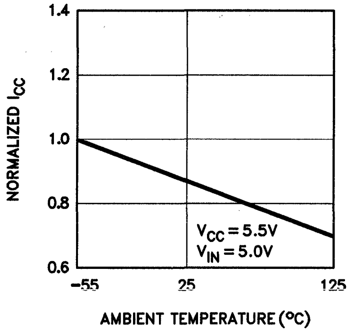
0054-15

Typical DC and AC Characteristics

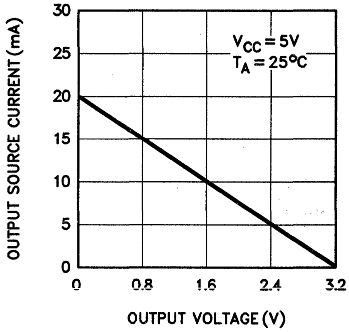
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



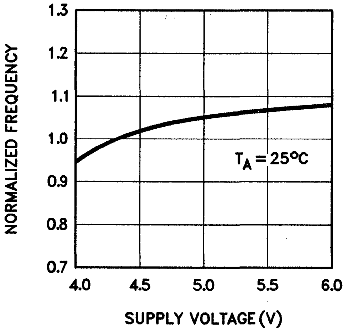
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



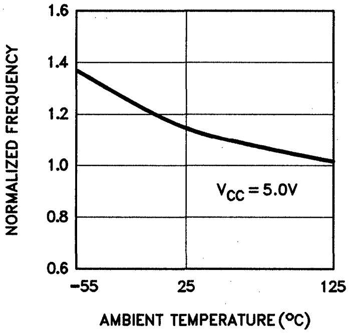
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



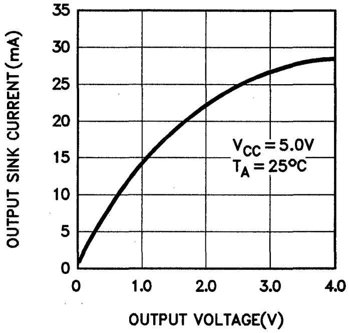
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



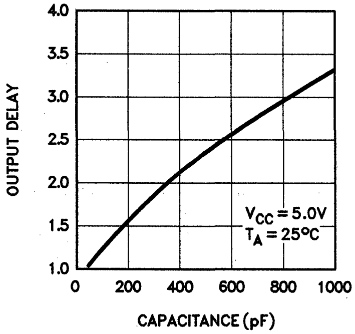
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



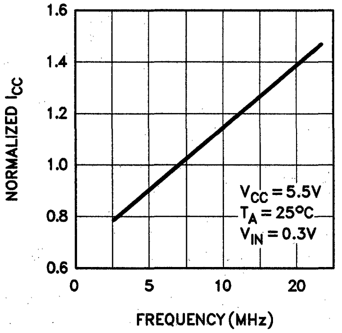
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED CURRENT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0054–17

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
38	CY7C516-38PC CY7C517-38PC	P29	Commercial
	CY7C516-38LC CY7C517-38LC	L81	
	CY7C516-38JC CY7C517-38JC	J81	
	CY7C516-38DC CY7C517-38DC	D30	
	CY7C516-38GC CY7C517-38GC	G68	
42	CY7C516-42LMB CY7C517-42LMB	L81	Military
	CY7C516-42DMB CY7C517-42DMB	D30	
	CY7C516-42GMB CY7C517-42GMB	G68	
45	CY7C516-45PC CY7C517-45PC	P29	Commercial
	CY7C516-45LC CY7C517-45LC	L81	
	CY7C516-45JC CY7C517-45JC	J81	
	CY7C516-45DC CY7C517-45DC	D30	
	CY7C516-45GC CY7C517-45GC	G68	

Speed (ns)	Ordering Code	Package Type	Operating Range
55	CY7C516-55PC CY7C517-55PC	P29	Commercial
	CY7C516-55LC CY7C517-55LC	L81	
	CY7C516-55JC CY7C517-55JC	J81	
	CY7C516-55DC CY7C517-55DC	D30	
	CY7C516-55GC CY7C517-55GC	G68	
	CY7C516-55LMB CY7C517-55LMB	L81	Military
	CY7C516-55DMB CY7C517-55DMB	D30	
	CY7C516-55GMB CY7C517-55GMB	G68	
75	CY7C516-75PC CY7C517-75PC	P29	Commercial
	CY7C516-75LC CY7C517-75LC	L81	
	CY7C516-75JC CY7C517-75JC	J81	
	CY7C516-75DC CY7C517-75DC	D30	
	CY7C516-75GC CY7C517-75GC	G68	
	CY7C516-75LMB CY7C517-75LMB	L81	Military
	CY7C516-75DMB CY7C517-75DMB	D30	
	CY7C516-75GMB CY7C517-75GMB	G68	

CYPRESS
SEMICONDUCTOR

CY7C901

CMOS Four-Bit Slice

Features

- **Fast**
  CY7C901-23 has a 23 ns Read Modify-Write Cycle; Commercial 25% Faster than "C" Spec 2901
  CY7C901-27 has a 27 ns Read Modify-Write Cycle; Military 15% Faster than "C" Spec 2901
- **Low Power**
  70 mA (commercial)
  90 mA (military)
- **V_{CC} 5V ±10%**
  Commercial and military
- **Eight Function ALU**
- **Infinitely expandable in 4-bit increments**
- **Four Status Flags:**
  Carry, overflow, negative, zero
- **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin Compatible and Functional Equivalent to Am2901B, C**

Functional Description

The CY7C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

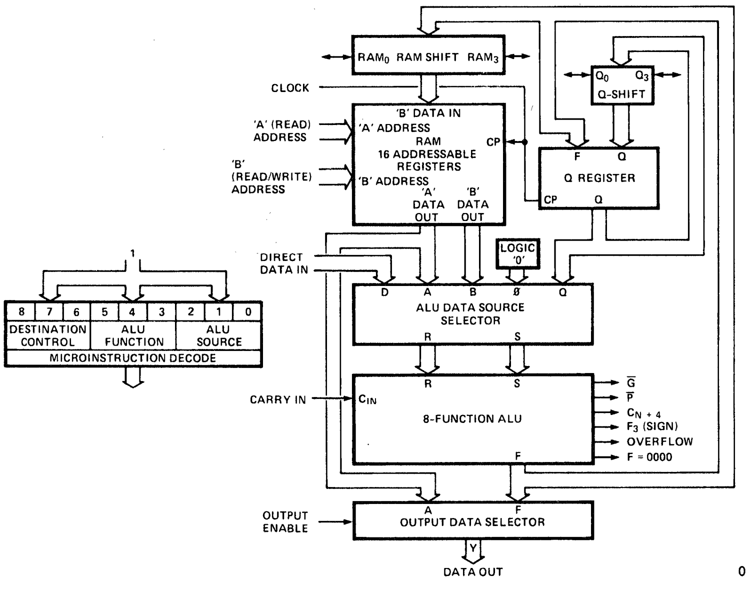
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from a microinstruction register.

The CY7C901 is expandable in 4-bit increments, has three-state data outputs as well as flag output, and can use either a full look ahead carry or a ripple carry.

The CY7C901 is a pin compatible, functional equivalent, improved performance replacement for the Am2901.

The CY7C901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance with low power dissipation.

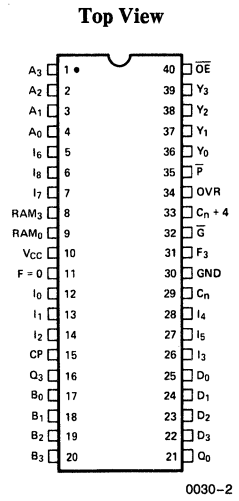
Logic Block Diagram


RAM0 RAM SHIFT RAM3
CLOCK
'B' DATA IN
'A' (READ) ADDRESS
'A' ADDRESS
RAM
16 ADDRESSABLE REGISTERS
CP
'B' (READ/WRITE) ADDRESS
'B' ADDRESS
'A' DATA OUT
'B' DATA OUT
Q0 Q3
Q-SHIFT
F Q
Q REGISTER
CP Q
LOGIC '0'
DIRECT DATA IN
D A B 0 Q
ALU DATA SOURCE SELECTOR
R S
1
8 7 6 5 4 3 2 1 0
DESTINATION CONTROL
ALU FUNCTION
ALU SOURCE
MICROINSTRUCTION DECODE
CARRY IN
CIN
8-FUNCTION ALU
F
G
P
CN + 4
F3 (SIGN)
OVERFLOW
F = 0000
OUTPUT ENABLE
A F
OUTPUT DATA SELECTOR
Y
DATA OUT

0030-1

Pin Configuration

Top View


A3 1
A2 2
A1 3
A0 4
I6 5
I8 6
I7 7
RAM3 8
RAM0 9
VCC 10
F = 0 11
I0 12
I1 13
I2 14
CP 15
Q3 16
B0 17
B1 18
B2 19
B3 20
40 OE
39 Y3
38 Y2
37 Y1
36 Y0
35 P
34 OVR
33 Cn + 4
32 G
31 F3
30 GND
29 Cn
28 I4
27 I5
26 I3
25 D0
24 D1
23 D2
22 D3
21 Q0

0030-2

Selection Guide

See last page for ordering information.

Read Modify-Write Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
23	80	Commercial	CY7C901-23
27	90	Military	CY7C901-27
31	70	Commercial	CY7C901-31
32	90	Military	CY7C901-32

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

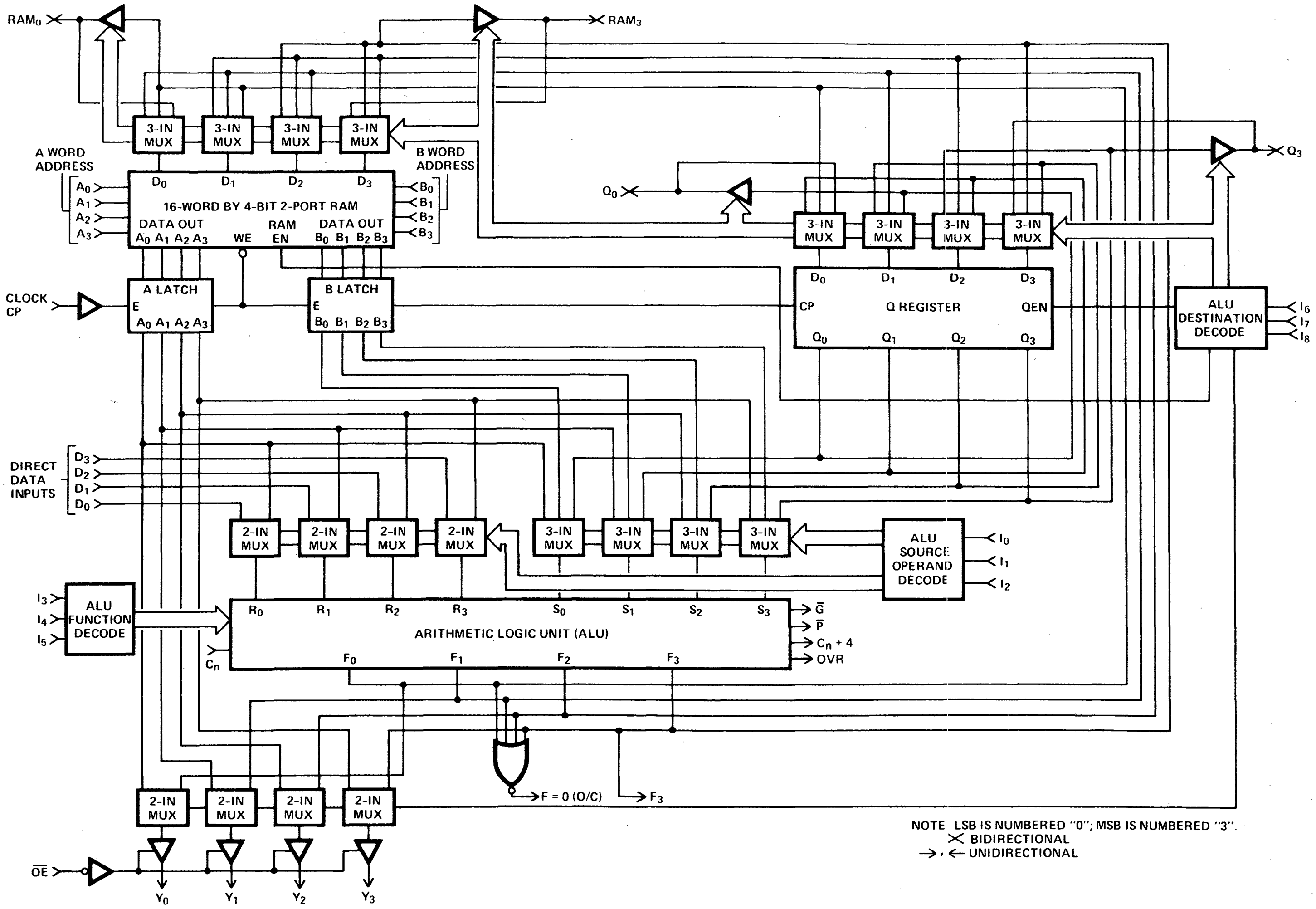
Latchup Current (Outputs).................. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
A_0–A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0–B_3	I	These 4 address lines select one of the registers in the stack and output is contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0–I_8	I	These 9 instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$) and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
D_0–D_3	I	These are 4 data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
Y_0–Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the Y_0–Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock Input. The LOW level of the clock write data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.
Q_3 RAM_3 (Cont.)	I/O	**Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM 3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}, \overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4-bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open drain output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.


RAM0
RAM3
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
A WORD ADDRESS
B WORD ADDRESS
A0
A1
A2
A3
16-WORD BY 4-BIT 2-PORT RAM
D0 D1 D2 D3
DATA OUT A0 A1 A2 A3
WE
RAM EN
DATA OUT B0 B1 B2 B3
B0
B1
B2
B3
Q0
Q3
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
CLOCK CP
A LATCH
E
A0 A1 A2 A3
B LATCH
E
B0 B1 B2 B3
Q REGISTER
D0 D1 D2 D3
CP
QEN
Q0 Q1 Q2 Q3
ALU DESTINATION DECODE
I6
I7
I8
DIRECT DATA INPUTS
D3
D2
D1
D0
2-IN MUX
2-IN MUX
2-IN MUX
2-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
ALU SOURCE OPERAND DECODE
I0
I1
I2
I3
I4
I5
ALU FUNCTION DECODE
R0 R1 R2 R3
S0 S1 S2 S3
ARITHMETIC LOGIC UNIT (ALU)
Cn
F0 F1 F2 F3
G̅
P̅
Cn + 4
OVR
F = 0 (O/C)
F3
2-IN MUX
2-IN MUX
2-IN MUX
2-IN MUX
OE̅
Y0
Y1
Y2
Y3
NOTE LSB IS NUMBERED "0"; MSB IS NUMBERED "3".
BIDIRECTIONAL
→, ← UNIDIRECTIONAL

0030-3

Figure 1. CY7C901 Block Diagram

Functional Tables

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Figure 3. ALU Function Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
A = Register Addressed by A inputs.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control

	I_{210} Octal	0	1	2	3	4	5	6	7
Octal I_{543}	ALU Source ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Figure 5. Source Operand and ALU Function Matrix

Description of Architecture

General Description

A block diagram of the CY7C901 is shown in *Figure 1.* The circuit is a 4-bit slice consisting of a register file (16 x 4 dual port RAM), the ALU, the Q register and the necessary control logic. It is expandable in 4-bit increments.

RAM

The RAM is addressed by two 4-bit address fields (A_0-A_3, B_0-B_3) that cause the data to appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

New data is written into the RAM location specified by the B address when the RAM write enable (RAM EN) is active and the clock input is LOW. Each of the four RAM inputs is driven by a 3-input multiplexer that allows the outputs of the ALU ($F_{0,\,1,\,2,\,3,}$) to be shifted one bit position to the left, the right, or not to be shifted. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins.

For a shift left (up) operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. For a shift right (down) operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled.

The data to be written into the RAM is applied to the D inputs of the CY7C901 and is passed (unchanged) through the ALU to the RAM location addressed by the B word address.

The outputs of the RAM A and B ports drive separate 4-bit latches that are enabled (follow the RAM data) when the clock is HIGH. The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU ($R_{0,\,1,\,2,\,3}$) and ($S_{0,\,1,\,2,\,3}$) and the ($Y_{0,\,1,\,2,\,3}$) chip outputs.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from four 2-input multiplexers whose inputs are from either the (RAM) A-port or the external data (D) inputs. The S inputs are driven from four 3-input multiplexers whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the $I_{0,\,1,\,2}$ inputs as shown in *Figure 2.* This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A, B, D, Q and "0" (unselected) inputs as 4-bits operands to the ALU. The logical and arithmetic operations performed by the ALU upon the data present at its R and S inputs are tabulated in *Figure 3.* The ALU has a carry-in (C_n) input, carry-propagate ($\overline{P}$) output, carry-generate ($\overline{G}$) output, carry-out ($C_n + 4$) and overflow (OVR) pins to enable the user to (1) speed up arithmetic operations by implementing carry look-ahead logic and (2) determine if an arithmetic overflow has occurred.

The ALU data outputs ($F_{0,\,1,\,2,\,3}$) are routed to the RAM, the Q register inputs and the Y outputs under control of the $I_{6,\,7,\,8}$ control signal inputs as shown in *Figure 4.* In addition, the MSB of the ALU is output as F3 so that the user can examine the sign bit without enabling the three-state outputs. The $F = 0$ output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open-drain output which may be wire OR'ed across multiple 7C901 processor slices.

Q Register

The Q register functions as an accumulator or temporary storage register. Physically it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from four 3-input multiplexers under control of the $I_{6,\,7,\,8}$ inputs. The Q_0 and Q_3 I/O pins function in a manner similar to the RAM_0 and RAM_3 pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is LOW and transferred from master to slave (output) when the clock changes from LOW to HIGH.

ALU Source Operand and ALU Functions

The ALU source operands and ALU function matrix is summarized in *Figure 5* and separated by logic operation or arithmetic operation in *Figures 6* and *7*, respectively. The $I_{0,\,1,\,2}$ lines select eight pairs of source operands and the $I_{3,\,4,\,5}$ lines select the operation to be performed. The carry-in (C_n) signal affects the arithmetic result and the internal flags; not the logical operations.

Conventional Addition and Pass-Increment/ Decrement

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	“ZERO”	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Figure 6. ALU Logic Mode Functions

Subtraction

Recall that in two’s complement integer coding −1 is equal to all ones and that in one’s complement integer coding zero is equal to all ones. To convert a positive integer to its two’s complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Figure 7* the symbol −Q represents the two’s complement of Q so that the one’s complement of Q is then −Q −1.

Octal I_{543}, I_{210}	$C_n = 0$ (Low)		$C_n = 1$ (High)	
	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q−1	PASS	Q
1 3		B−1		B
1 4		A−1		A
2 7		D−1		D
2 2	1’s Comp.	−Q−1	2’s Comp. (Negate)	−Q
2 3		−B−1		−B
2 4		−A−1		−A
1 7		−D−1		−D
1 0	Subtract (1’s Comp.)	Q−A−1	Subtract (2’s Comp.)	Q−A
1 1		B−A−1		B−A
1 5		A−D−1		A−D
1 6		Q−D−1		Q−D
2 0		A−Q−1		A−Q
2 1		A−B−1		A−B
2 5		D−A−1		D−A
2 6		D−Q−1		D−Q

Figure 7. ALU Arithmetic Mode Functions

Logic Functions for $\overline{G}$, $\overline{P}$, $C_n + 4$, and OVR

The four signals G, P, $C_n + 4$, and OVR are designed to indicate carry and overflow conditions when the CY7C901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to *Figure 2*.

Definitions (+ = OR)

$P_0 = R_0 + S_0$	$G_0 = R_0S_0$
$P_1 = R_1 + S_1$	$G_1 = R_1S_1$
$P_2 = R_2 + S_2$	$G_2 = R_2S_2$
$P_3 = R_3 + S_3$	$G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_N+4	OVR
0	$R+S$	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \veebar C_4$
1	$S-R$	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	$R-S$	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	$R \vee S$	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	$R \wedge S$	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R} \wedge S$	LOW	← Same as $R \wedge S$ equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	$R \veebar S$	← Same as $\overline{R \veebar S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \veebar S}$	$G_3+G_2+G_1+G_0$	$G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1P_0$	$\overline{G_3+P_3G_2+P_3P_2G_1}$ $\overline{+P_3P_2P_1P_0(G_0+\overline{C}_n)}$	See note

Notes:
$[P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \veebar [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$
+ = OR

Figure 8

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 20 mA Commercial I_{OL} = 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$ V_{CC} = Max.		−10	10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{OH} = 2.4V		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	Commercial	20		mA
			Military	16		
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = V_{SS} to V_{CC}		 −40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V			−85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial -31		70	mA
			Commercial -23		80	
			Military -27, -32		90	
I_{CC_1}	Supply Current	$V_{IH} \geq V_{CC}$ − 1.2V, 10 MHz $V_{IL} \leq$ 0.4V	Commercial		26.5	mA
			Military		31	

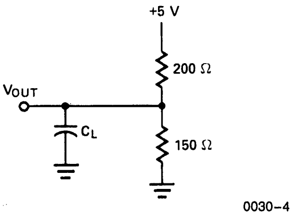
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f= 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

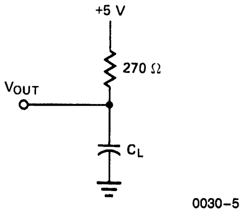
Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested on a sample basis.

Output Loads used for AC Performance Characteristics



All outputs except open drain



Open drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.
3. Loads shown above are for commercial (20 mA) I_{OL} spec only.

CY7C901-23 Commercial and CY7C901-27 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-23PC	CY7C901-23DC	CY7C901-23LC
CY7C901-23JC	CY7C901-27DMB	CY7C901-27LMB

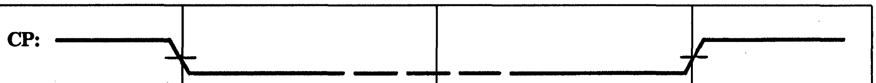
Cycle Time and Clock Characteristics

CY7C901	-23	-27
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	23 ns	27 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	43 MHz	37 MHz
Minimum Clock LOW Time	13 ns	15 ns
Minimum Clock HIGH Time	10 ns	12 ns
Minimum Clock Period	23 ns	27 ns

Combinational Propagation Delays. $C_L = 50$ pF

To Output From Input	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
CY7C901	23	27	23	27	23	27	23	27	23	27	23	27	23	27	23	27
A, B Address	30	33	30	33	30	33	28	33	30	33	30	33	30	33	—	—
Data	21	24	20	23	20	23	20	21	24	25	21	24	22	25	—	—
C_n	17	18	16	17	14	14	—	—	18	19	16	17	18	19	—	—
I_{012}	26	28	25	27	24	26	24	28	25	29	24	27	25	27	—	—
I_{345}	26	27	24	27	24	26	24	26	26	27	24	26	26	27	—	—
I_{678}	16	18	—	—	—	—	—	—	—	—	—	—	21	21	21	21
A Bypass ALU (I = 2XX)	24	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↑	24	27	23	26	23	26	23	25	24	27	24	26	24	27	19	20

Set-up and Hold Times Relative to Clock (CP) Input



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C901	23	27	23	27	23	27	23	27
A, B Source Address	10	12	0 (Note 3)		21, 10 + t_{PWL} (Note 4)		0	
B Destination Address	10	12	← Do Not Change →				0	
Data	—	—	—		16		0	
C_n	—	—	—		13		0	
I_{012}	—	—	—		19		0	
I_{345}	—	—	—		19		0	
I_{678}	7	9	← Do Not Change →				0	
$RAM_{0,3}, Q_{0,3}$	—	—	—		9		0	

Output Enable/Disable Times

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C901-23	$\overline{OE}$	Y	14	16
CY7C901-27	$\overline{OE}$	Y	16	18

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

CY7C901-31 Commercial and CY7C901-32 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-31PC CY7C901-31DC CY7C901-31LC CY7C901-31JC CY7C901-32DMB CY7C901-32LMB

Cycle Time and Clock Characteristics

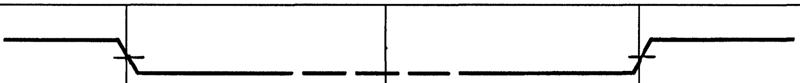
CY7C901-	-31	-32
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	31 ns	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz	31 MHz
Minimum Clock LOW Time	16 ns	17 ns
Minimum Clock HIGH Time	15 ns	15 ns
Minimum Clock Period	31 ns	32 ns

For faster performance see CY7C901-23 specification on page 9.

Combinational Propagation Delays. C_L = 50 pF

To Output	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
From Input	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**	**-31**	**-32**
A, B Address	40	48	40	48	40	48	37	44	40	48	40	48	40	48	—	—
D	30	37	30	37	30	37	30	34	38	40	30	37	30	37	—	—
C_n	22	25	22	25	20	21	—	—	25	28	22	25	25	28	—	—
I_{012}	35	40	35	40	35	40	37	44	37	44	35	40	35	40	—	—
I_{345}	35	40	35	40	35	40	35	40	38	40	35	40	35	40	—	—
I_{678}	25	29	—	—	—	—	—	—	—	—	—	—	26	29	26	29
A Bypass ALU (I = 2XX)	35	40	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↗	35	40	35	40	35	40	35	40	35	40	35	40	35	40	28	33

Set-up and Hold Times Relative to Clock (CP) Input

	CP: 			
Input	**Set-up Time Before H → L**	**Hold Time After H → L**	**Set-up Time Before L → H**	**Hold Time After L → H**
A, B Source Address	15	0 (Note 3)	30, 15 + t_{PWL} (Note 4)	0
B Destination Address	15	← Do Not Change	→	0
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0,3}, Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

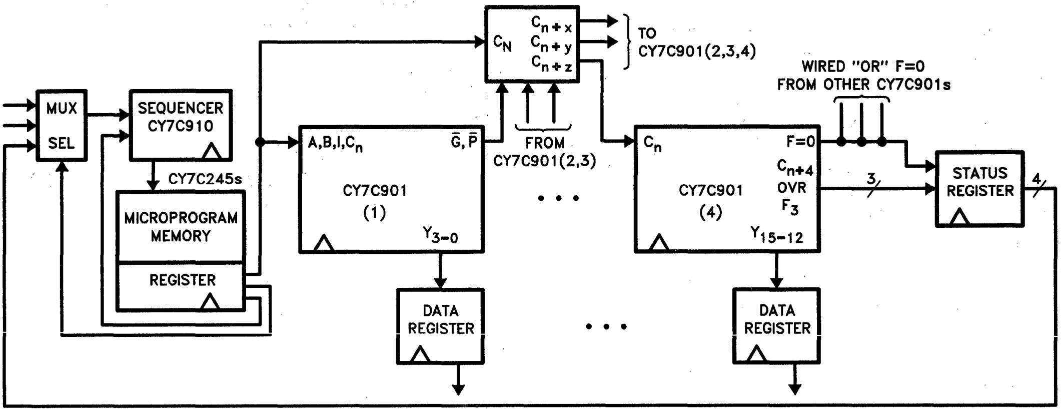
Device	Input	Output	Enable	Disable
CY7C901-31	$\overline{OE}$	Y	23	23
CY7C901-32	$\overline{OE}$	Y	25	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

Minimum Cycle Time Calculations for 16-Bit Systems

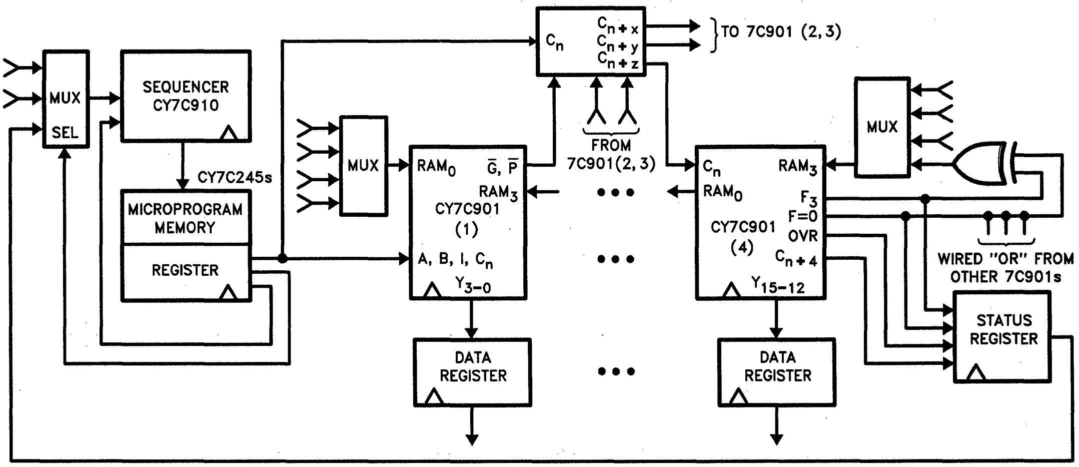
Speed used in calculations for parts other than CY7C901 are representative for MSI parts.


MUX
SEL
SEQUENCER
CY7C910
CY7C245s
MICROPROGRAM MEMORY
REGISTER
A,B,I,Cn
G, P
CY7C901
(1)
Y3-0
CN
Cn+x
Cn+y
Cn+z
TO CY7C901(2,3,4)
FROM CY7C901(2,3)
Cn
F=0
Cn+4
OVR
F3
CY7C901
(4)
Y15-12
WIRED "OR" F=0 FROM OTHER CY7C901s
3
STATUS REGISTER
4
DATA REGISTER
DATA REGISTER
0030-11

Pipelined System, Add without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G_0}$, $\overline{P_0}$ to $C_n + z$	9	CY7C910	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
Register	Setup	4			66 ns
		71 ns			

Minimum Clock Period = 71 ns

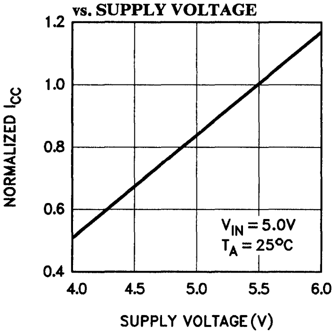

MUX
SEL
SEQUENCER
CY7C910
CY7C245s
MICROPROGRAM MEMORY
REGISTER
MUX
RAM0
G, P
RAM3
CY7C901
(1)
A, B, I, Cn
Y3-0
Cn
Cn+x
Cn+y
Cn+z
TO 7C901 (2, 3)
FROM 7C901(2, 3)
Cn
RAM3
RAM0
F3
F=0
CY7C901
(4)
OVR
Cn+4
Y15-12
MUX
WIRED "OR" FROM OTHER 7C901s
STATUS REGISTER
DATA REGISTER
DATA REGISTER
0030-12

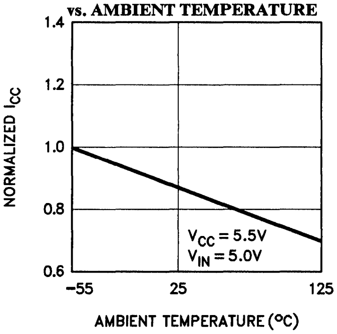
Pipelined System, Simultaneous Add and Shift Down (RIGHT)

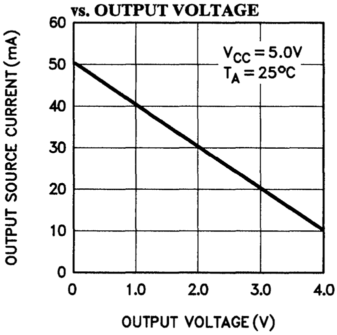
	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G_0}$, $\overline{P_0}$ to $C_n + z$	9	CY7C910	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
XOR and MUX	Prop. Delay, Select to Output	20			66 ns
CY7C901	RAM_3 Setup	9			
		96 ns			

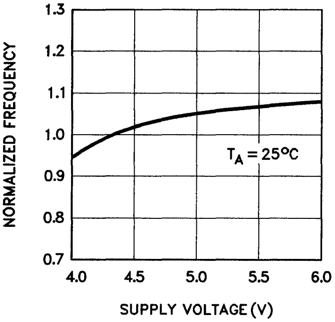
Minimum Clock Period = 96 ns

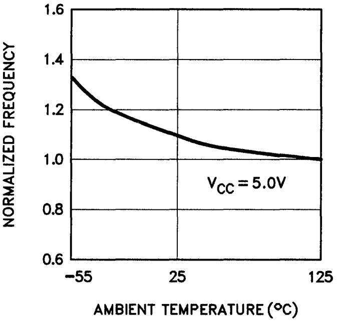
Typical DC and AC Characteristics

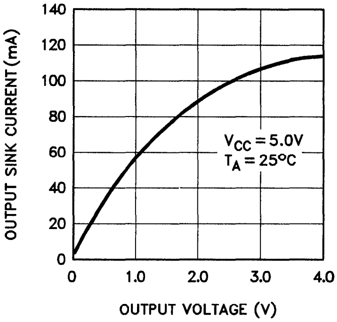

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

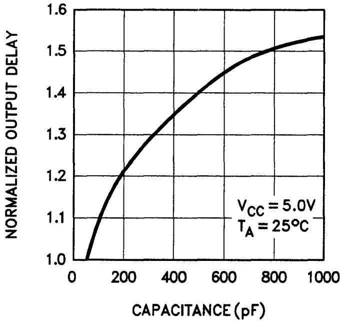

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

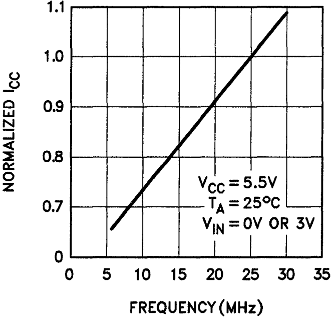

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE


NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE


NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING


NORMALIZED I_{CC} vs. FREQUENCY

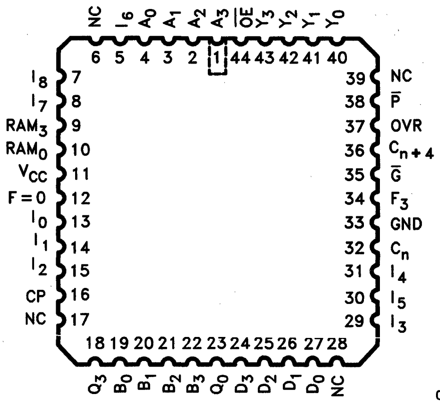
0030–10

Ordering Information

Read Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
23	CY7C901-23PC	P17	Commercial
	CY7C901-23DC	D18	Commercial
	CY7C901-23JC	J67	Commercial
	CY7C901-23LC	L67	Commercial
27	CY7C901-27DMB	D18	Military
	CY7C901-27LMB	L67	Military
31	CY7C901-31PC	P17	Commercial
	CY7C901-31DC	D18	Commercial
	CY7C901-31JC	J67	Commercial
	CY7C901-31LC	L67	Commercial
32	CY7C901-32DMB	D18	Military
	CY7C901-32LMB	L67	Military

Pin Configuration

Top View



NC
I6
A0
A1
A2
A3
OE
Y3
Y2
Y1
Y0
6 5 4 3 2 1 44 43 42 41 40
I8 7
I7 8
RAM3 9
RAM0 10
VCC 11
F=0 12
I0 13
I1 14
I2 15
CP 16
NC 17
39 NC
38 P
37 OVR
36 Cn+4
35 G
34 F3
33 GND
32 Cn
31 I4
30 I5
29 I3
18 19 20 21 22 23 24 25 26 27 28
Q3
B0
B1
B2
B3
Q0
D3
D2
D1
D0
NC

0030-9

CYPRESS
SEMICONDUCTOR

CY7C909
CY7C911

CMOS Micro Program Sequencers

Features

- **Fast**
  - **— CY7C909/11 has a 30 ns (min.) clock to output cycle time; commercial and military**
- **Low Power**
  - **— I_{CC} (max.) = 55 mA; commercial and military**
- **V_{CC} margin**
  - **— 5 V ± 10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functional equivalent to 2909A/2911A**

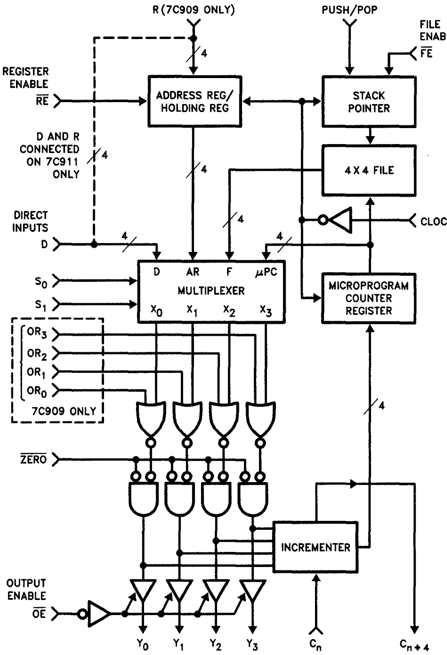
Description

The CY7C909 and CY7C911 are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY7C909 can select an address from any of four sources. They are: 1) a set of four external direct inputs (D_i); 2) external data stored in an internal register (R_i); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be OR'ed with an external input for conditional skip or branch instructions. A $\overline{\text{ZERO}}$ input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable ($\overline{\text{OE}}$) input.

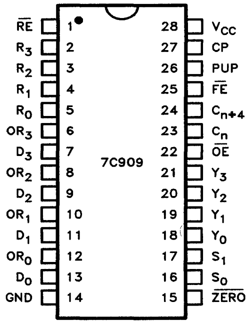
The CY7C911 is an identical circuit to the CY7C909, except the four OR inputs are removed and the D and R inputs are tied together. The CY7C911 is available in a 20-pin, 300-mil package.

Logic Block Diagram

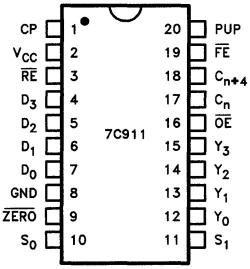

R (7C909 ONLY)
PUSH/POP
FILE ENABLE
$\overline{\text{FE}}$
REGISTER ENABLE
$\overline{\text{RE}}$
ADDRESS REG/ HOLDING REG
STACK POINTER
4X4 FILE
D AND R CONNECTED ON 7C911 ONLY
DIRECT INPUTS
D
CLOCK
4
S_0
S_1
D AR F μPC
MULTIPLEXER
X_0 X_1 X_2 X_3
MICROPROGRAM COUNTER REGISTER
OR_3
OR_2
OR_1
OR_0
7C909 ONLY
$\overline{\text{ZERO}}$
INCREMENTER
OUTPUT ENABLE
$\overline{\text{OE}}$
Y_0 Y_1 Y_2 Y_3
C_n
C_{n+4}

0042-1

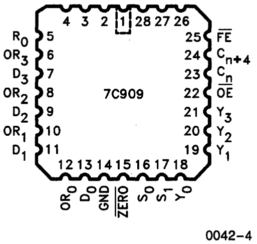
Pin Configurations


7C909
$\overline{\text{RE}}$ 1
R_3 2
R_2 3
R_1 4
R_0 5
OR_3 6
D_3 7
OR_2 8
D_2 9
OR_1 10
D_1 11
OR_0 12
D_0 13
GND 14
28 V_{CC}
27 CP
26 PUP
25 $\overline{\text{FE}}$
24 C_{n+4}
23 C_n
22 $\overline{\text{OE}}$
21 Y_3
20 Y_2
19 Y_1
18 Y_0
17 S_1
16 S_0
15 $\overline{\text{ZERO}}$

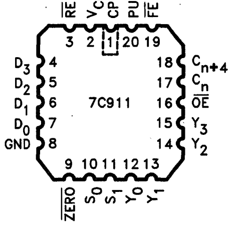
0042-2


7C911
CP 1
V_{CC} 2
$\overline{\text{RE}}$ 3
D_3 4
D_2 5
D_1 6
D_0 7
GND 8
$\overline{\text{ZERO}}$ 9
S_0 10
20 PUP
19 $\overline{\text{FE}}$
18 C_{n+4}
17 C_n
16 $\overline{\text{OE}}$
15 Y_3
14 Y_2
13 Y_1
12 Y_0
11 S_1

0042-3


7C909
R_1 R_2 R_3 $\overline{\text{RE}}$ V_{CC} CP PUP
4 3 2 1 28 27 26
R_0 5
OR_3 6
D_3 7
OR_2 8
D_2 9
OR_1 10
D_1 11
25 $\overline{\text{FE}}$
24 C_{n+4}
23 C_n
22 $\overline{\text{OE}}$
21 Y_3
20 Y_2
19 Y_1
12 13 14 15 16 17 18
OR_0 D_0 GND $\overline{\text{ZERO}}$ S_0 S_1 Y_0

0042-4


7C911
$\overline{\text{RE}}$ V_{CC} CP PUP $\overline{\text{FE}}$
3 2 1 20 19
D_3 4
D_2 5
D_1 6
D_0 7
GND 8
18 C_{n+4}
17 C_n
16 $\overline{\text{OE}}$
15 Y_3
14 Y_2
9 10 11 12 13
$\overline{\text{ZERO}}$ S_0 S_1 Y_0 Y_1

0042-5

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.6 mA (Comm.)		2.4		V
		V_{CC} = Min., I_{OH} = −1.0 mA (Mil.)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−20	+20	μA
I_{OS}	Output Short[1] Circuit Current	V_{CC} = Max.	V_{OUT} = GND	−30	−85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		55	mA
			Military		55	
I_{CC_1}	V_{CC} Operating Supply Current	V_{CC} = Max. V_{IH} ≥ 3.0V, V_{IL} ≤ 0.4V	Commercial		35	mA
			Military		35	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

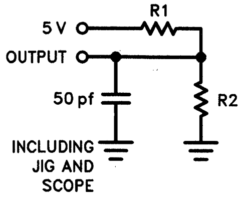


Figure 1a

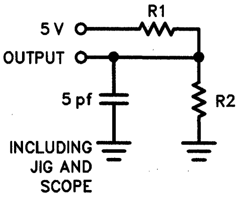
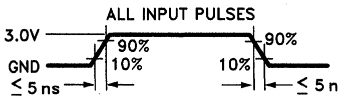


Figure 1b

0042-6



0042-7

Figure 2

	Commercial	Military
R_1	254Ω	258Ω
R_2	187Ω	216Ω

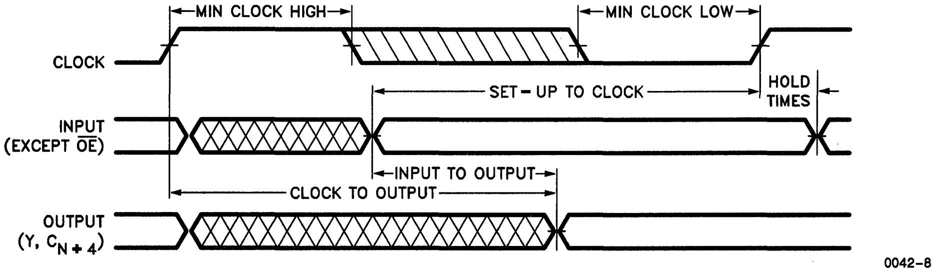
Switching Characteristics Over Operating Range

	7C909-30 7C911-30		7C909-30 7C911-30		7C909-40 7C911-40		7C909-40 7C911-40		Units
	Commercial		Military		Commercial		Military		
Minimum Clock Low Time	15		15		20		20		ns
Minimum Clock High Time	15		15		20		20		ns
MAXIMUM COMBINATIONAL PROPAGATION DELAYS									
From Input To:	Y	C_{N+4}	Y	C_{N+4}	Y	C_{N+4}	Y	C_{N+4}	ns
D_i	17	18	18	19	17	22	20	25	ns
S_0, S_1	18	18	20	20	29	34	29	34	ns
OR_i (7C909)	16	16	17	17	17	22	20	25	ns
C_N	—	13	—	15	—	14	—	16	ns
$\overline{\text{ZERO}}$	18	18	20	20	29	34	30	35	ns
$\overline{\text{OE}}$ Low to Output	16	—	18	—	25	—	25	—	ns
$\overline{\text{OE}}$ HIGH to HIGH Z[4]	16	—	18	—	25	—	25	—	ns
Clock HIGH, S_1, S_0 = LH	20	20	22	22	39	44	45	50	ns
Clock HIGH, S_1, S_0 = LL	20	20	22	22	39	44	45	50	ns
Clock HIGH, S_1, S_0 = HL	20	20	22	22	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)									
From Input	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	
$\overline{\text{RE}}$	11	0	12	0	19	0	19	0	ns
R_i [5]	10	0	11	0	10	0	12	0	ns
Push/Pop	12	0	13	0	25	0	27	0	ns
FE	12	0	13	0	25	0	27	0	ns
C_N	10	0	11	0	18	0	18	0	ns
D_i	14	0	16	0	25	0	25	0	ns
OR_i (7C909)	12	0	14	0	25	0	25	0	ns
S_0, S_1	14	0	16	0	25	0	29	0	ns
$\overline{\text{ZERO}}$	12	0	13	0	25	0	29	0	ns

Notes:

4. Output Loading as in *Figure 1b.*
5. R_i and D_i are internally connected on the CY7C911. Use R_i set-up and hold times when D_i inputs are used to load register.
6. System clock cycle time (Clock Low Time and Clock High Time) cannot be less than maximum propagation delay.

Switching Waveforms



Functional Description

The tables below define the control logic of the 7C909/911. Table 1 contains the Multiplexer Control Logic which selects the address source to appear on the outputs.

Table 1. Address Source Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS
0	L	L	Microprogram Counter (μPC)
1	L	H	Address/Holding Register (AR)
2	H	L	Push-Pop stack (STK)
3	H	H	Direct inputs (D_i)

Control of the Push/Pop Stack is contained in Table 2. $\overline{\text{FILE ENABLE}}$ ($\overline{\text{FE}}$) enables stack operations, while Push/Pop (PUP) controls the stack.

Table 2. Synchronous Stack Control

$\overline{\text{FE}}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Push current PC into stack increment stack pointer
L	L	pop stack, decrement stack pointer

Table 3 illustrates the Output Control Logic of the 7C909/911. The $\overline{\text{ZERO}}$ control forces the outputs to zero. The OR inputs are OR'ed with the output of the multiplexer.

Table 3. Output Control

OR_i	$\overline{\text{ZERO}}$	$\overline{\text{OE}}$	Y_i
X	X	H	High Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Table 4 defines the effect of S_0, S_1, $\overline{\text{FE}}$ and PUP control signals on the 7C909. It illustrates the Address Source on the outputs and the contents of the Internal Registers for every combination of these signals. The Internal Register contents are illustrated before and after the Clock LOW to HIGH edge.

Table 4

CYCLE	S_1, S_0, $\overline{\text{FE}}$, PUP	μ PC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N + 1	0 0 0 0 —	J J + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J —	Pop Stack	End Loop
N N + 1	0 0 0 1 —	J J + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J —	Push μPC	Set-up Loop
N N + 1	0 0 1 X —	J J + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J —	Continue	Continue
N N + 1	0 1 0 0 —	J K + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K —	Use AR for Address; Pop Stack	End Loop
N N + 1	0 1 0 1 —	J K + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K —	Jump to Address in AR; Push μPC	JSR AR
N N + 1	0 1 1 X —	J K + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K —	Jump to Address in AR	JMP AR
N N + 1	1 0 0 0 —	J Ra + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra —	Jump to Address in STK0; Pop Stack	RTS
N N + 1	1 0 0 1 —	J Ra + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra —	Jump to Address in STK0; Push μPC	
N N + 1	1 0 1 X —	J Ra + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra —	Jump to Address in STK0	Stack Ref (Loop)
N N + 1	1 1 0 0 —	J D + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D —	Jump to Address on D; Pop Stack	End Loop
N N + 1	1 1 0 1 —	J D + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D —	Jump to Address on D; Push μPC	JSR D
N N + 1	1 1 1 X —	J D + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D —	Jump to Address on D	JMP D

J = Contents of Microprogram Counter
K = Contents of Address Register
R_a, R_b, R_c, R_d = Contents in Stack

Functional Description (Continued)

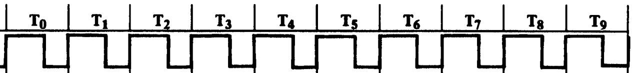
Two examples of Subroutine Execution appear below. *Figure 3* illustrates a single subroutine while *Figure 4* illustrates two nested subroutines.

The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the 7C909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to sub-routine at A". At the time T_2, this instruction is in the μWR, and the 7C909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. *Figure 4* is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_6	J+3	-
T_7	J+4	-
	-	-
	-	-
	-	-
	-	-
	-	-
T_3	A	I(A)
T_4	A+1	-
T_5	A+2	RTS
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	-	-	-	J+3	J+3	J+3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

0042-9

Figure 3. Subroutine Execution. C_n = HIGH

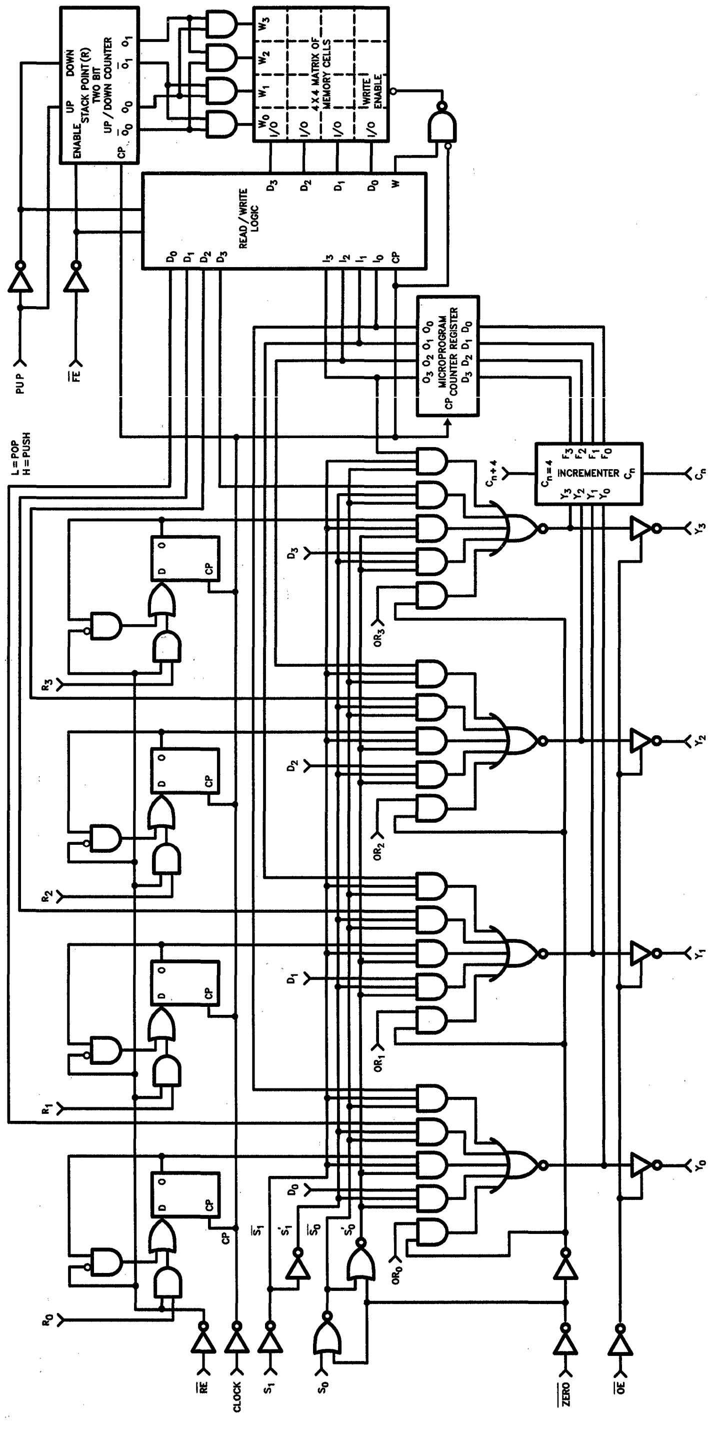
CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_9	J+3	-
	-	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A+1	-
T_5	A+2	JSR B
T_7	A+3	-
T_8	A+4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	-	-	-	J+3	J+3	J+3	A+3	J+3	J+3	-
	STK1	-	-	-	-	-	-	J+3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

0042-10

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH


PUP
FE
L = POP
H = PUSH
ENABLE
UP
DOWN
STACK POINT (R)
TWO BIT
UP / DOWN COUNTER
CP
$\overline{O}_0$
O_0
$\overline{O}_1$
O_1
W_0
W_1
W_2
W_3
I/O
4 X 4 MATRIX OF MEMORY CELLS
WRITE ENABLE
READ / WRITE LOGIC
D_0
D_1
D_2
D_3
I_3
I_2
I_1
I_0
CP
W
O_3 O_2 O_1 O_0
MICROPROGRAM COUNTER REGISTER
D_3 D_2 D_1 D_0
CP
C_{n+4}
$C_n = 4$
INCREMENTER
Y_3 Y_2 Y_1 Y_0
F_3 F_2 F_1 F_0
C_n
R_0
R_1
R_2
R_3
D
O
CP
$\overline{RE}$
CLOCK
S_1
S_0
$\overline{S_1}$
S_1'
$\overline{S_0}$
S_0'
D_0
D_1
D_2
D_3
OR_0
OR_1
OR_2
OR_3
$\overline{ZERO}$
$\overline{OE}$
Y_0
Y_1
Y_2
Y_3

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Note:
R_i and D_i connected together and OR_i Inputs removed on CY7C911

Figure 5. Microprogram Sequencer Block Diagram

Functional Description (Continued)

Architecture

The CY7C909 and CY7C911 are CMOS microprogram sequencers for use in high speed processor applications. They are cascadable in 4-bit increments. Two devices can address 256 words of microprogram, three can address up to 4K words, and so on. The architecture of the CY7C909/911 is illustrated in the logic diagram in *Figure 5*. The various blocks are described below.

Multiplexer

The Multiplexer is controlled by the S_0 and S_1 inputs to select the address source. It selects either the Direct Inputs (D_i), the Address Register (AR), the Microprogram Counter (μPC), or the stack (SP) as the source of the next microinstruction address.

Direct Inputs

The Direct Inputs (D_i) allow addresses from an external source to be output on the Y outputs. On the CY7C911, the direct inputs are also the inputs to the Address Register.

Address Register

The Address Register (AR) consists of four D-type, edge-triggered flip-flops which are controlled by the $\overline{\text{Register Enable}}$ ($\overline{\text{RE}}$) input. When $\overline{\text{Register Enable}}$ is LOW, new data is entered into the register on the LOW to HIGH clock transition.

Microprogram Counter

The Microprogram Counter (μPC) is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has a Carry-in (C_N) input and a Carry-out (C_{N+4}) output to facilitate cascading. The Carry-in input controls the microprogram counter. When Carry-in is HIGH the incrementer counts sequentially. The counter register is loaded with the current Y output plus one ($Y + 1 -> \mu$PC) on the next clock cycle. When Carry-in is LOW the incrementer does not count. The microprogram counter register is loaded with the same Y output ($Y -> \mu$PC) on the next clock cycle.

Stack

The Stack consists of a 4 x 4 memory array and a built-in Stack Pointer (SP) which always points to the last word written. The Stack is used to store return addresses when executing microsubroutines.

The Stack Pointer is an up/down counter controlled by $\overline{\text{File Enable}}$ ($\overline{\text{FE}}$) and Push/Pop (PUP) inputs. The $\overline{\text{File Enable}}$ input allows stack operations only when it is LOW. The Push/Pop input controls the stack pointer position.

The PUSH operation is initiated at the beginning of a microsubroutine. Push/Pop is set HIGH while $\overline{\text{File Enable}}$ is kept LOW. The stack pointer is incremented and the memory array is written with the microinstruction address following the subroutine jump that initiated the push.

The POP operation is initiated at the end of a microsubroutine to obtain the return address. Both Push/Pop and $\overline{\text{File Enable}}$ are set LOW. The return address is already available to the multiplexer. The stack pointer is decremented on the next LOW to HIGH clock transition, effectively removing old information from the top of the stack. The stack is configured so that data will roll-over if more than four POPs are performed, thus preventing data from being lost.

The contents of the memory position pointed to by the Stack Pointer is always available to the multiplexer. Stack reference operations can thus be performed without a push or a pop. Since the stack is four words deep, up to four microsubroutines can be nested.

The $\overline{\text{ZERO}}$ input resets the four Y outputs to a binary zero state. The OR inputs (7C909 only) are connected to the Y outputs such that any output can be set to a logical one.

The $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) input controls the Y outputs. A HIGH on $\overline{\text{Output Enable}}$ sets the outputs into a high impedance state.

Definition of Terms

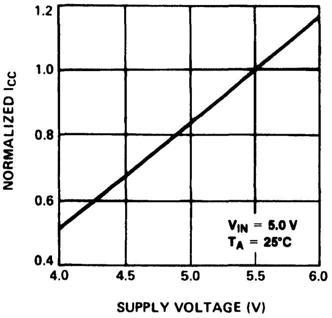
Name	Description
INPUTS	
S_1, S_0	Multiplexer Control Lines, for Access Source Selection
$\overline{\text{FE}}$	$\overline{\text{File Enable}}$, Enables Stack Operation, Active LOW
PUP	Push/Pop, Selects Stack Operation
$\overline{\text{RE}}$	$\overline{\text{Register Enable}}$, Enables Address Register Active LOW
$\overline{\text{ZERO}}$	Forces Output to Logical Zero
$\overline{\text{OE}}$	$\overline{\text{Output Enable}}$, Controls Three-State Outputs Active LOW
OR_i	Logic OR Input to each Address Output Line (7C909 only)
C_n	Carry-In, Controls Microprogram Counter
R_i	Inputs to the Internal Address Register
D_i	Direct Inputs to the Multiplexer
CP	Clock Input

Definition of Terms (Continued)

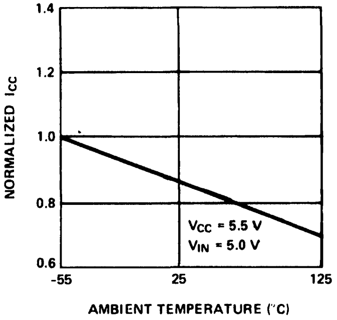
Name	Description
OUTPUTS	
Y_i	Address Outputs
C_{N+4}	Carry-Out from Incrementer
INTERNAL SIGNALS	
μPC	Contents of the Microprogram Counter
AR	Contents of the Address Register
STK0- STK3	Contents of the Push/Pop Stack
SP	Contents of the Stack Pointer
EXTERNAL SIGNALS	
A	Address to the Counter Memory
I(A)	Instruction in Control Memory at Address A
μWR	Contents of the Microword Register at the Output of the Control Memory
T_N	Time Period (Cycle) n

Typical DC and AC Characteristics

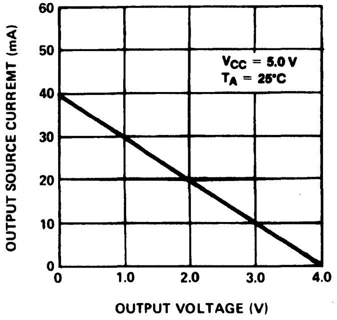
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



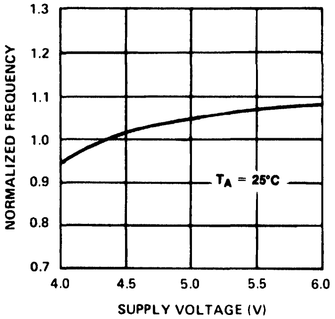
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



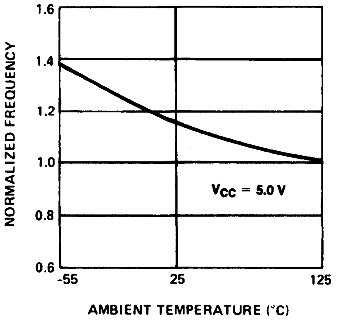
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



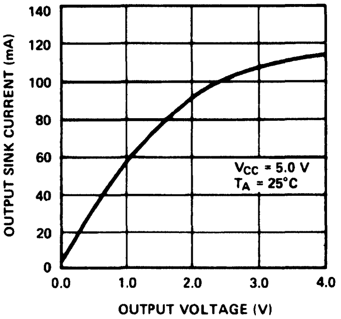
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



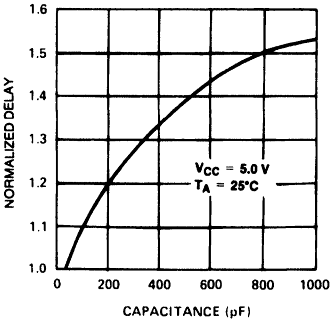
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



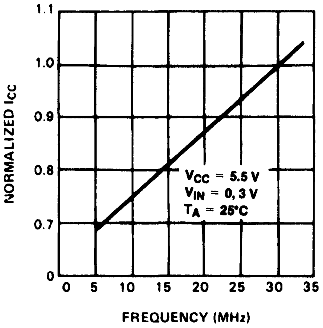
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0042-12

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C909-30PC	P15	Commercial
40	CY7C909-40PC	P15	Commercial
30	CY7C909-30JC	J64	Commercial
40	CY7C909-40JC	J64	Commercial
30	CY7C909-30DC	D16	Commercial
40	CY7C909-40DC	D16	Commercial
40	CY7C909-40LC	L64	Commercial
30	CY7C909-30DMB	D16	Military
40	CY7C909-40DMB	D16	Military
40	CY7C909-40LMB	L64	Military

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C911-30PC	P5	Commercial
40	CY7C911-40PC	P5	Commercial
30	CY7C911-30JC	J61	Commercial
40	CY7C911-40JC	J61	Commercial
30	CY7C911-30DC	D6	Commercial
40	CY7C911-40DC	D6	Commercial
40	CY7C911-40LC	L61	Commercial
30	CY7C911-30DMB	D6	Military
40	CY7C911-40DMB	D6	Military
40	CY7C911-40LMB	L61	Military

CYPRESS SEMICONDUCTOR

CY7C910

CMOS Microprogram Controller

Features

- **Fast**
  - **CY7C910-40 has a 40 ns (min.) clock cycle; commercial**
  - **CY7C910-46 has a 46 ns (min.) clock cycle; military**
- **Low power**
  - **I_{CC} (max.) = 70 mA**
- **V_{CC} margin 5V ±10% commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), stack, branch address bus, internal holding register**
- **12-bit internal loop counter**
- **Internal 17-word by 12-bit stack The internal stack can be used for subroutine return address or data storage**
- **ESD protection Capable of withstanding over 2000V static discharge voltage**
- **Pin compatible and functional equivalent to AM2910A**

Functional Description

The CY7C910 is a stand-alone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

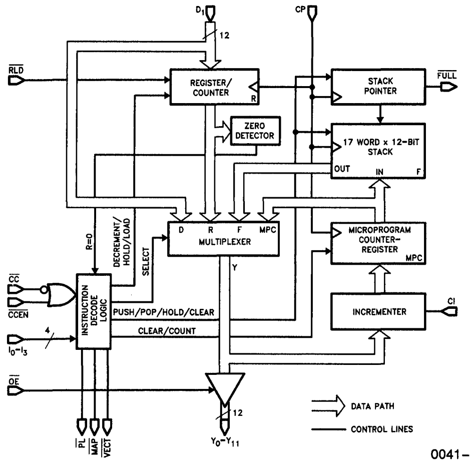
The CY7C910, as illustrated in the block diagram, consists of a 17-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY7C910 is a pin compatible, functional equivalent, improved performance replacement for the AM2910A.

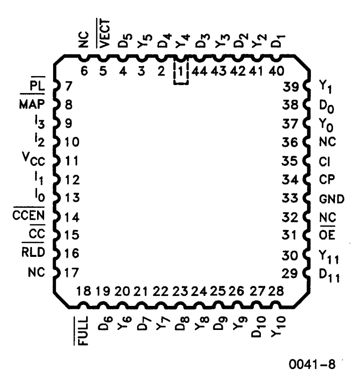
The CY7C910 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

Logic Block Diagram

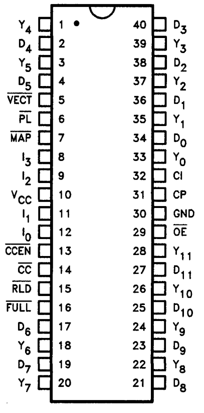

D$_I$
CP
12
$\overline{RLD}$
REGISTER/ COUNTER
R
STACK POINTER
$\overline{FULL}$
ZERO DETECTOR
17 WORD x 12-BIT STACK
OUT
IN
F
R=0
DECREMENT/ HOLD/LOAD
SELECT
D R F MPC MULTIPLEXER
MICROPROGRAM COUNTER-REGISTER
MPC
Y
$\overline{CC}$
$\overline{CCEN}$
INSTRUCTION DECODE LOGIC
PUSH/POP/HOLD/CLEAR
CLEAR/COUNT
INCREMENTER
CI
4
I$_0$-I$_3$
$\overline{OE}$
12
$\overline{PL}$
$\overline{MAP}$
$\overline{VECT}$
Y$_0$-Y$_{11}$
DATA PATH
CONTROL LINES

0041-1

Pin Configurations


NC
$\overline{VECT}$
D5 Y5 D4 Y4 D3 Y3 D2 Y2 D1
6 5 4 3 2 1 44 43 42 41 40
$\overline{PL}$ 7
$\overline{MAP}$ 8
I3 9
I2 10
VCC 11
I1 12
I0 13
$\overline{CCEN}$ 14
$\overline{CC}$ 15
$\overline{RLD}$ 16
NC 17
39 Y1
38 D0
37 Y0
36 NC
35 CI
34 CP
33 GND
32 NC
31 $\overline{OE}$
30 Y11
29 D11
18 19 20 21 22 23 24 25 26 27 28
$\overline{FULL}$ D6 Y6 D7 Y7 D8 Y8 D9 Y9 D10 Y10

0041-8


Y4 1 40 D3
D4 2 39 Y3
Y5 3 38 D2
D5 4 37 Y2
$\overline{VECT}$ 5 36 D1
$\overline{PL}$ 6 35 Y1
$\overline{MAP}$ 7 34 D0
I3 8 33 Y0
I2 9 32 CI
VCC 10 31 CP
I1 11 30 GND
I0 12 29 $\overline{OE}$
$\overline{CCEN}$ 13 28 Y11
$\overline{CC}$ 14 27 D11
$\overline{RLD}$ 15 26 Y10
$\overline{FULL}$ 16 25 D10
D6 17 24 Y9
Y6 18 23 D9
D7 19 22 Y8
Y7 20 21 D8

0041-2

Top View

Selection Guide

Clock Cycle (Min.) in ns	Stack Depth	Operating Range	Part Number
40	17 words	Commercial	CY7C910-40
46	17 words	Military	CY7C910-46
50	17 words	Commercial	CY7C910-50
51	17 words	Military	CY7C910-51
93	17 words	Commercial	CY7C910-93
99	17 words	Military	CY7C910-99

Pin Definitions

Signal Name	I/O	Description
D0–D11	I	Direct inputs to the RC (Register/Counter) and multiplexer. D0 is LSB and D11 is MSB.
$\overline{\text{RLD}}$	I	Register load. Control input to RC that, when LOW, loads data on the D0–D11 pins into RC on the LOW to HIGH clock (CP) transition.
I0–I3	I	Instruction inputs that select one of sixteen instructions to be performed by the CY7C910.
$\overline{\text{CC}}$	I	Control input that, when LOW, signifies that a test has passed.
$\overline{\text{CCEN}}$	I	Enable for $\overline{\text{CC}}$ input. When HIGH $\overline{\text{CC}}$ is ignored and a pass is forced. When LOW the state of $\overline{\text{CC}}$ is examined.
CP	I	Clock input. All internal states are changed on the LOW to HIGH clock transitions.

Signal Name	I/O	Description
CI	I	Carry input to the LSB of the incrementer for the MPC.
$\overline{\text{OE}}$	I	Control for Y0–Y11 outputs. LOW to enable; High to disable.
Y0–Y11	O	Address output to microprogram memory. Y0 is LSB and Y11 is MSB.
$\overline{\text{FULL}}$	O	When LOW indicates the stack is full.
$\overline{\text{PL}}$	O	When LOW selects the pipeline register as the direct input (D0–D11) source.
$\overline{\text{MAP}}$	O	When LOW selects the Mapping PROM (or PLA) as the direct input source.
$\overline{\text{VECT}}$	O	When LOW selects the Interrupt Vector as the direct input source.

Architecture of the CY7C910

Introduction

The CY7C910 is a high performance CMOS microprogram controller that produces a sequence of 12-bit addresses that control the execution of a microprogram. The addresses are selected from one of four sources, depending upon the (internal) instruction being executed (I0–I3), and other external inputs. The sources are (1) the (external) D0–D11 inputs, (2) the RC, (3) the stack and (4) the MPC. Twelve bit lines from each of these four sources are the inputs to a multiplexer, as shown in *Figure 1*, whose outputs are applied to the inputs of the Y0–Y11 three-state output drivers.

External Inputs: D0–D11

The external inputs are used as the source for destination addresses for the jump or branch type of instructions. These are shown as Ds in the two columns in the Table of Instructions. A second use of these inputs is to load the RC.

Register Counter: RC

The RC is implemented as 12 D-type, edge-triggered flip-flops that are synchronously clocked on the LOW to HIGH transition of the clock, CP. The data on the D inputs is synchronously loaded into the RC when the load control input, RLD, is LOW. The output of the RC is available to the multiplexer as its R input and is output on the Y outputs during certain instructions, as shown by R in the Table of Instructions.

The RC is operated as a 12-bit down counter and its contents decremented and tested if zero during instructions 8, 9 and 15. This enables micro-instructions to be repeated up to 4096 times. The RC is arranged such that if it is loaded with a number, N, the sequence will be executed exactly N + 1 times.

The Stack and Stack Pointer: SP

The 17-word by 12-bit stack is used to provide return addresses from micro-subroutines or from loops. Intergal to it is a SP, which points to (addresses) the last word written. This permits reference to the data on the top of the stack without having to perform a POP operation.

The SP operates as an up/down counter that is incremented when a PUSH operation (instructions 1, 4 or 5) is performed or decremented when a POP operation (instructions 8, 10, 11, 13 or 15) is performed. The PUSH operation writes the return address on the stack and the POP operation effectively removes it. The actual operation occurs on the LOW to HIGH clock transition following the instruction.

The stack is initialized by executing instruction zero (JUMP TO LOCATION 0 or RESET). Every time a "jump to subroutine" instruction (1, 5) or a loop instruction (4) is executed, the return address is PUSHed onto the stack; and every time a "return from subroutine (or loop)" instruction is executed, the return address is POPed off the stack.

When one subroutine calls another or a loop occurs within a loop (or a combination), which is called nesting, the Logical depth of the stack increases. The physical stack depth is 17 words. When this depth occurs, the $\overline{\text{FULL}}$ signal goes LOW on the next LOW to HIGH clock transition. Any further PUSH operations on a full stack will cause the data at that location to be over-written, but will not increment the SP. Similariły, performing a POP operation on a empty stack will not decrement the SP and may result in non-meaningful data being available at the Y outputs.

The Microprocessor Counter: MPC

The MPC consists of a 12-bit incrementer followed by a 12-bit register. The register usually holds the address of the instruction being fetched. When sequential instructions are fetched, the carry input (CI) to the incrementer is HIGH and one is added to the Y outputs of the multiplexer, which is loaded into the MPC on the next LOW to HIGH clock transition. When the CI input is LOW, the Y outputs of the multiplexer are loaded directly into the MPC, so that the same instruction is fetched and executed.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 10 to Pin 30).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V
(Per MIL-STD-883 Method 3015.2)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Commercial and Military Operating Range, V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description		Test Condition	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min. I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min. I_{OL} = 12 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IH}	Input HIGH Current		V_{CC} = Max. V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current		V_{CC} = Max. V_{IN} = V_{SS}		−10	μA
I_{OH}	Output HIGH Current		V_{CC} = Min. V_{IH} = 2.4V	−1.6		mA
I_{OL}	Output LOW Current		V_{CC} = Min. V_{OL} = 0.4V	12		mA
I_{OZ}	Output Leakage Current		V_{CC} = Max. V_{OUT} = V_{SS}/V_{CC}	−40	+40	μA μA
I_{SC}	Output Short Circuit Current		V_{CC} = Max. V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	Commercial	V_{CC} = Max.		70	mA
		Military			90	
I_{CC_1}	Supply Current	Commercial	$V_{IH} \geq 3.85V$, $V_{IL} \leq 0.4V$		35	mA
		Military			50	

Capacitance[2]

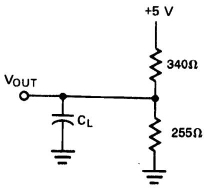
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
2. Tested on a sample basis.

Output Load used for AC Performance Characteristics

All Outputs

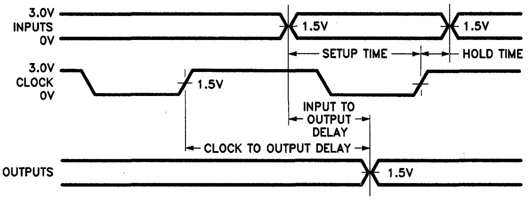


0041-4

Notes:

1. C_L = 50 pF includes scope probe, writing and stray capacitance.
2. C_L = 5 pF for output disable tests.

Switching Waveforms



0041-5

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY7C910 over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements (Note 1)

	Commercial			Military		
CY7C910-	40	50	93	46	51	99
Minimum Clock LOW	20	20	50	23	25	58
Minimum Clock HIGH	20	20	35	23	25	42
Minimum Clock Period I = 14	40	50	93	46	51	100
Minimum Clock Period I = 8, 9, 15	40	50	113	46	51	114

Combinatorial Propagation Delays. C_L = 50 pF

	Commercial									Military								
From Input	Y			$\overline{\text{PL}}$, $\overline{\text{VECT}}$, $\overline{\text{MAP}}$			$\overline{\text{FULL}}$			Y			$\overline{\text{PL}}$, $\overline{\text{VECT}}$, $\overline{\text{MAP}}$			$\overline{\text{FULL}}$		
CY7C910-	40	50	93	40	50	93	40	50	93	46	51	99	46	51	99	46	51	99
D0–D11	17	20	20	—	—	—	—	—	—	21	25	25	—	—	—	—	—	—
I0–I3	25	35	50	20	30	51	—	—	—	30	40	54	25	35	58	—	—	—
$\overline{\text{CC}}$	22	30	30	—	—	—	—	—	—	27	36	35	—	—	—	—	—	—
$\overline{\text{CCEN}}$	22	30	30	—	—	—	—	—	—	27	36	37	—	—	—	—	—	—
CP I = 8, 9, 15 (Note 2)	30	40	75	—	—	—	25	31	60	35	46	77	—	—	—	30	35	67
CP All Other I	30	40	55	—	—	—	25	31	60	35	46	61	—	—	—	30	35	67
$\overline{\text{OE}}$	21	25	35	—	—	—	—	—	—	22	25	40	—	—	—	—	—	—
(Note 2)	21	27	30	—	—	—	—	—	—	22	30	30	—	—	—	—	—	—

Minimum Set-Up and Hold Times Relative to clock LOW to HIGH Transition. C_L = 50 pF

	Commercial						Military					
Input	Set-Up			Hold			Set-Up			Hold		
CY7C910-	40	50	93	40	50	93	46	51	99	46	51	99
DI → RC	13	16	24	0	0	0	13	16	28	0	0	0
DI → MPC	20	30	58	0	0	0	20	30	62	0	0	0
I0–I3	25	35	75	0	0	0	27	38	81	0	0	0
$\overline{\text{CC}}$	20	24	63	0	0	0	25	35	65	0	0	0
$\overline{\text{CCEN}}$	20	24	63	0	0	0	25	35	63	0	0	0
CI	15	18	46	0	0	0	15	18	58	0	0	0
$\overline{\text{RLD}}$	15	19	36	0	0	0	15	20	42	0	0	0

Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.
2. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C_L = 5 pF.

Table of Instructions

I_3–I_0	Mnemonic	Name	Reg/ Cntr Con-tents	Result					
				Fail $\overline{CCEN}$ = L and $\overline{CC}$ = H		Pass $\overline{CCEN}$ = H or $\overline{CC}$ = L		Reg/ Cntr	Enable
				Y	Stack	Y	Stack		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 1)	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	POP	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

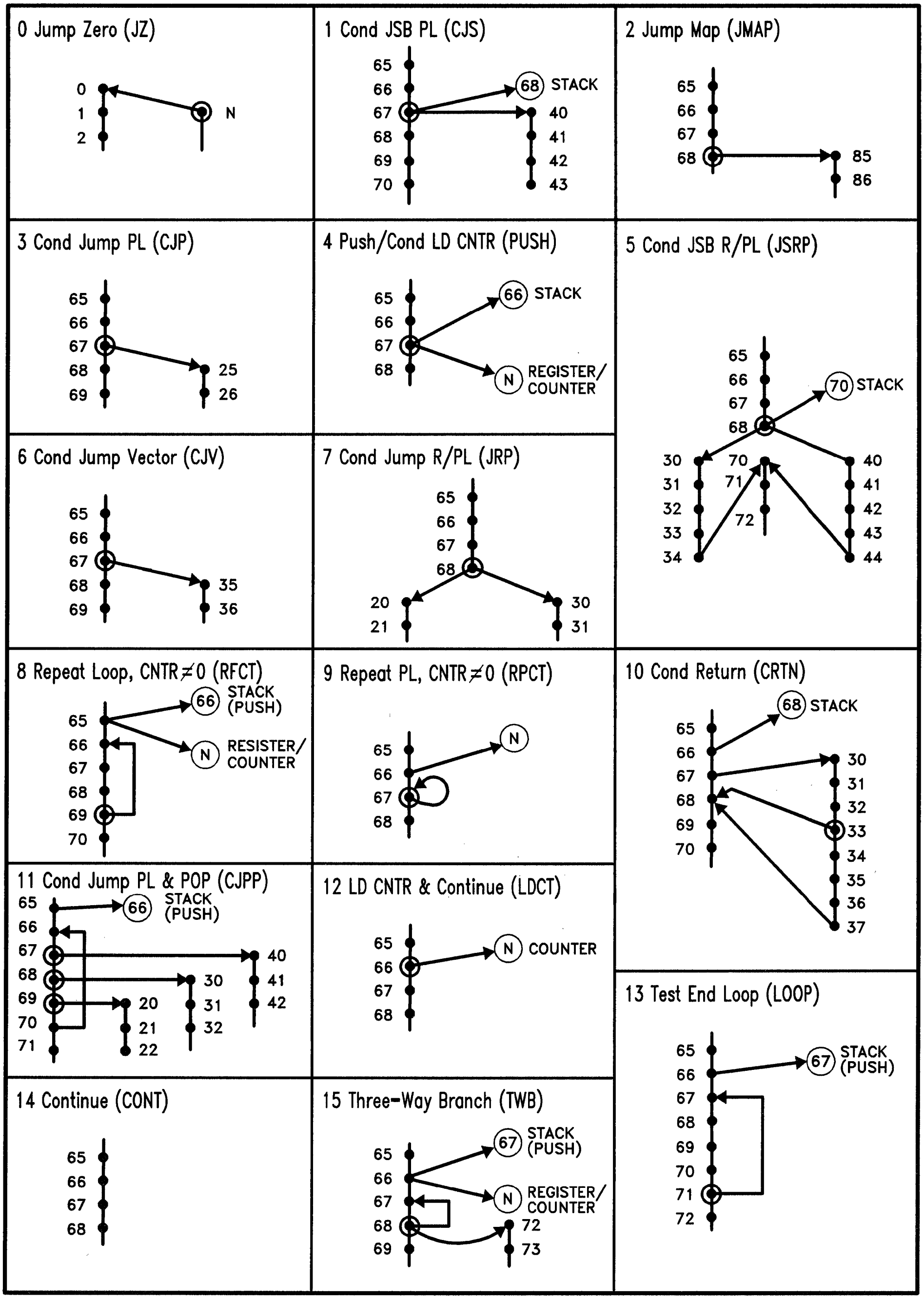
Notes:

1. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load.

H = HIGH L = LOW X = Don't Care

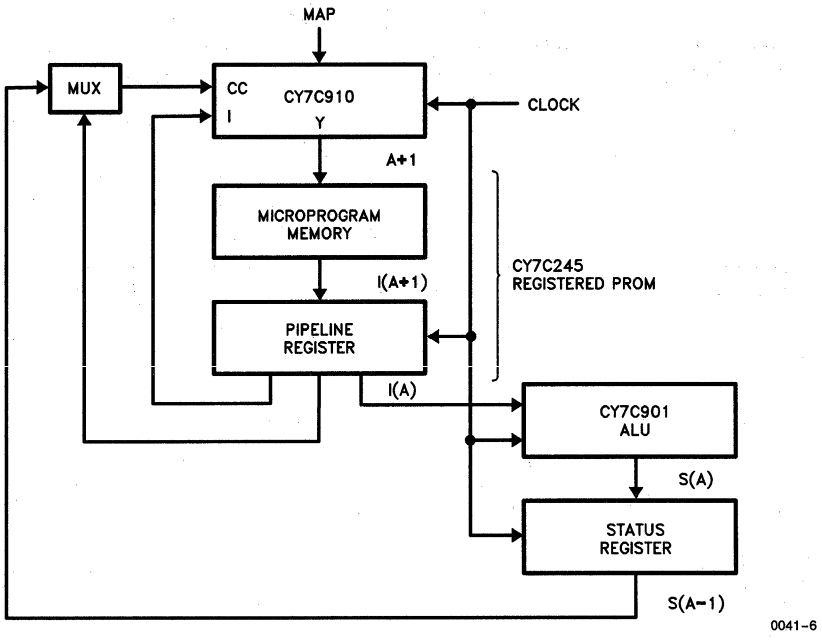
CY7C910 CMOS Microprogram Controller

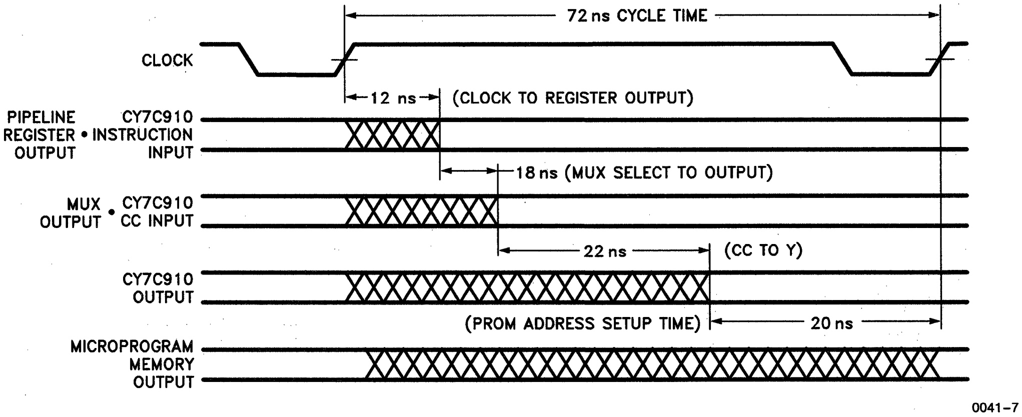
CY7C910 Flow Diagrams


0 Jump Zero (JZ)
0 1 2 N
1 Cond JSB PL (CJS)
65 66 67 68 69 70
68 STACK
40 41 42 43
2 Jump Map (JMAP)
65 66 67 68
85 86
3 Cond Jump PL (CJP)
65 66 67 68 69
25 26
4 Push/Cond LD CNTR (PUSH)
65 66 67 68
66 STACK
N REGISTER/ COUNTER
5 Cond JSB R/PL (JSRP)
65 66 67 68
70 STACK
30 31 32 33 34
70 71 72
40 41 42 43 44
6 Cond Jump Vector (CJV)
65 66 67 68 69
35 36
7 Cond Jump R/PL (JRP)
65 66 67 68
20 21
30 31
8 Repeat Loop, CNTR≠0 (RFCT)
66 STACK (PUSH)
N RESISTER/ COUNTER
65 66 67 68 69 70
9 Repeat PL, CNTR≠0 (RPCT)
65 66 67 68
N
10 Cond Return (CRTN)
68 STACK
65 66 67 68 69 70
30 31 32 33 34 35 36 37
11 Cond Jump PL & POP (CJPP)
65 66 67 68 69 70 71
66 STACK (PUSH)
40 41 42
30 31 32
20 21 22
12 LD CNTR & Continue (LDCT)
65 66 67 68
N COUNTER
13 Test End Loop (LOOP)
65 66 67 68 69 70 71 72
67 STACK (PUSH)
14 Continue (CONT)
65 66 67 68
15 Three-Way Branch (TWB)
67 STACK (PUSH)
N REGISTER/ COUNTER
65 66 67 68 69
72 73

0041-9

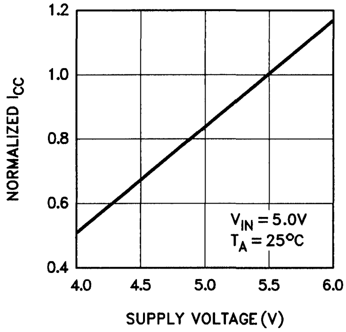
One Level Pipeline Based Architecture (Recommended)


MAP
MUX
CC
CY7C910
I
Y
CLOCK
A+1
MICROPROGRAM MEMORY
I(A+1)
CY7C245 REGISTERED PROM
PIPELINE REGISTER
I(A)
CY7C901 ALU
S(A)
STATUS REGISTER
S(A−1)
0041-6

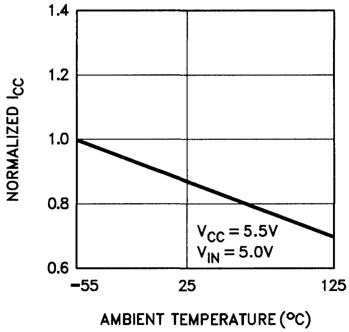

72 ns CYCLE TIME
CLOCK
12 ns
(CLOCK TO REGISTER OUTPUT)
PIPELINE REGISTER OUTPUT • CY7C910 INSTRUCTION INPUT
18 ns (MUX SELECT TO OUTPUT)
MUX OUTPUT • CY7C910 CC INPUT
22 ns
(CC TO Y)
CY7C910 OUTPUT
(PROM ADDRESS SETUP TIME)
20 ns
MICROPROGRAM MEMORY OUTPUT
0041-7

Typical DC and AC Characteristics

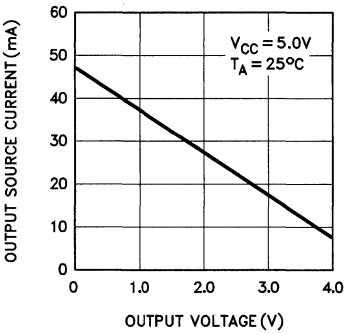
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



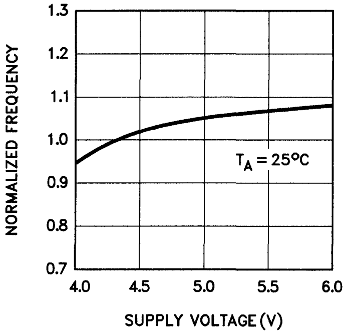
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



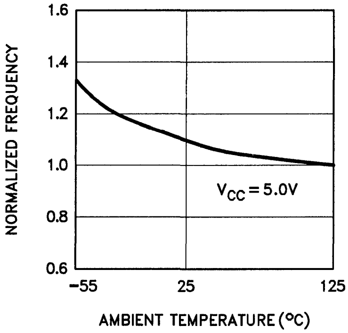
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



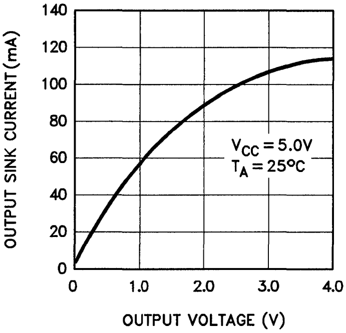
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



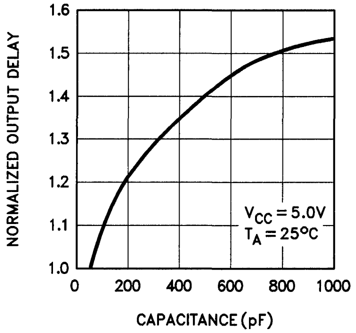
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



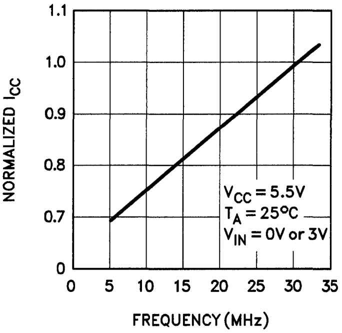
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0041–10

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
40	CY7C910-40PC	P17	Commercial
	CY7C910-40DC	D18	
	CY7C910-40JC	J67	
	CY7C910-40LC	L67	
46	CY7C910-46DMB	D18	Military
	CY7C910-46LMB	L67	
50	CY7C910-50PC	P17	Commercial
	CY7C910-50DC	D18	
	CY7C910-50JC	J67	
	CY7C910-50LC	L67	
51	CY7C910-51DMB	D18	Military
	CY7C910-51LMB	L67	
93	CY7C910-93PC	P17	Commercial
	CY7C910-93DC	D18	
	CY7C910-93JC	J67	
	CY7C910-93LC	L67	
99	CY7C910-99DMB	D18	Military
	CY7C910-99LMB	L67	

CYPRESS SEMICONDUCTOR

CY7C9101

CMOS Sixteen-Bit Slice

Features

- **Fast**
  - **— CY7C9101-30 has a 30 ns (max.) clock cycle (commercial)**
  - **— CY7C9101-35 has a 35 ns (max.) clock cycle (military)**
- **Low Power**
  - **— I_{CC} (max. at 10 MHz) = 60 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 85 mA (military)**
- **V_{CC} Margin**
  - **— 5V ±10%**
- **All parameters guaranteed over commercial and military operating temperature range**
- **Replaces four 2901's with carry look-ahead logic**
- **Eight Function ALU**
  - **— Performs three arithmetic and five logical operations on two 16-bit operands**
- **Expandable**
  - **— Infinitely expandable in 16-bit increments**
- **Four Status Flags**
  - **— Carry, overflow, negative, zero**
- **ESD Protection**
  - **— Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functionally equivalent to AM29C101**

Functional Description

The CY7C9101 is a high-speed, expandable, 16-bit wide ALU slice which can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C9101 is basic, yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C9101, as shown in the block diagram, consists of a 16-word by 16-bit dual-port RAM register file, a 16-bit ALU, and the necessary data manipulation and control logic.

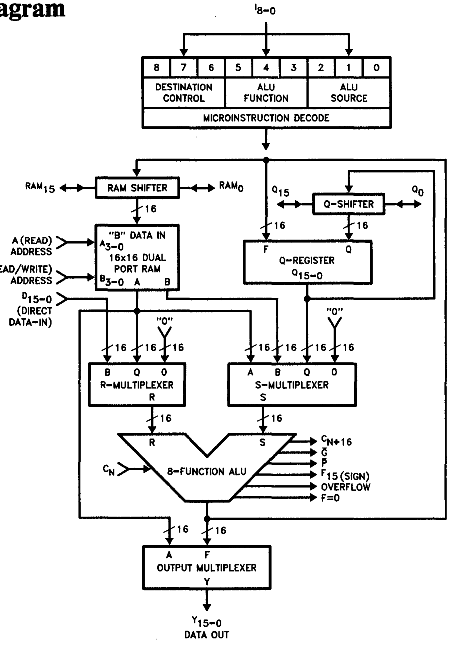
The function performed is determined by the nine-bit instruction word (I_8 to I_0) which is usually input via a microinstruction register.

The CY7C9101 is expandable in 16-bit increments, has three-state data outputs as well as flag outputs, and can implement either a full look-ahead carry or a ripple carry.

The CY7C9101 is a pin compatible, functional equivalent of the Am29C101 with improved performance. The 7C9101 replaces four 2901's and includes on-chip carry look-ahead logic.

Fabricated in an advanced 1.2 micron CMOS process, the 7C9101 eliminates latchup, has ESD protection greater than 2000V, and achieves superior performance with low power dissipation.

Logic Block Diagram



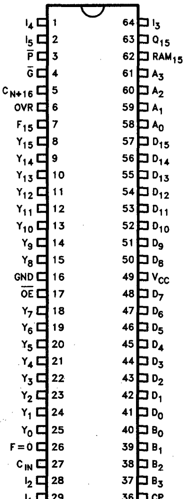
I8-0
8 7 6 5 4 3 2 1 0
DESTINATION CONTROL
ALU FUNCTION
ALU SOURCE
MICROINSTRUCTION DECODE
RAM15
RAM SHIFTER
RAM0
16
Q15
Q-SHIFTER
Q0
A (READ) ADDRESS
B (READ/WRITE) ADDRESS
"B" DATA IN
A3-0
16x16 DUAL PORT RAM
B3-0 A B
16
16
F Q
Q-REGISTER
Q15-0
D15-0 (DIRECT DATA-IN)
"0"
"0"
16 16 16
16 16 16 16
B Q 0
R-MULTIPLEXER
R
A B Q 0
S-MULTIPLEXER
S
16
16
R S
CN
8-FUNCTION ALU
CN+16
G
P
F15 (SIGN)
OVERFLOW
F=0
16 16
A F
OUTPUT MULTIPLEXER
Y
Y15-0 DATA OUT

0079-1

Figure 1

Pin Configuration

Top View



I4 1
I5 2
P 3
G 4
CN+16 5
OVR 6
F15 7
Y15 8
Y14 9
Y13 10
Y12 11
Y11 12
Y10 13
Y9 14
Y8 15
GND 16
OE 17
Y7 18
Y6 19
Y5 20
Y4 21
Y3 22
Y2 23
Y1 24
Y0 25
F=0 26
CIN 27
I2 28
I1 29
I0 30
I8 31
I7 32
64 I3
63 Q15
62 RAM15
61 A3
60 A2
59 A1
58 A0
57 D15
56 D14
55 D13
54 D12
53 D11
52 D10
51 D9
50 D8
49 VCC
48 D7
47 D6
46 D5
45 D4
44 D3
43 D2
42 D1
41 D0
40 B0
39 B1
38 B2
37 B3
36 CP
35 RAM0
34 Q0
33 I6

0079-2

Selection Guide

		7C9101-30 7C9101-35	7C9101-40 7C9101-45
Minimum Clock Cycle (ns)	Commercial	30	40
	Military	35	45
Maximum Operating Current at 10 MHz (mA)	Commercial	60	60
	Military	85	85

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current (Outputs).................. >200 mA

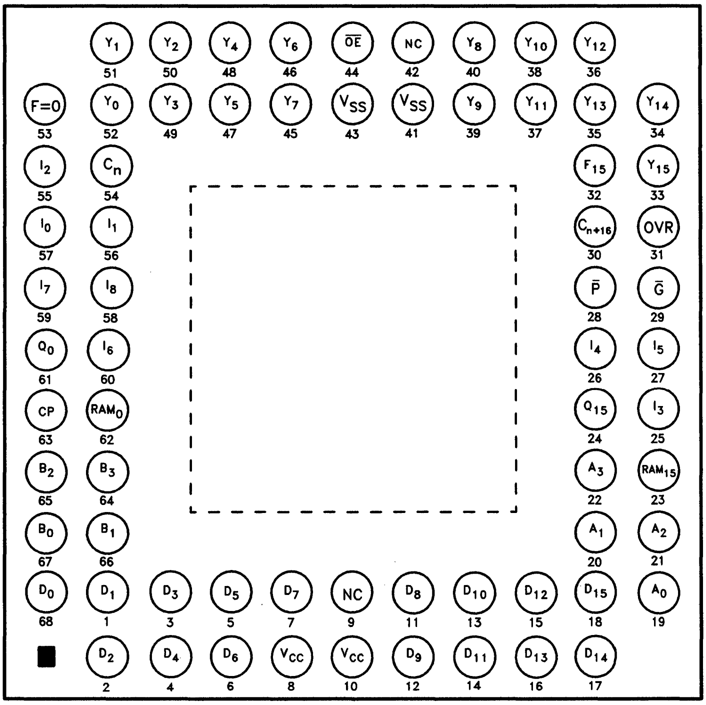
Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Pin Definitions

Signal Name	I/O	Description
A_{3-0}	I	**RAM Address A.** This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) A-port.
B_{3-0}	I	**RAM Address B.** This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) B-port. When data is written back to the register file, this is the destination address.
I_{8-0}	I	**Instruction Word.** This nine-bit word is decoded to determine the ALU data sources ($I_{0,1,2}$), the ALU operation ($I_{3,4,5}$), and the data to be written to the Q-register or register file ($I_{6,7,8}$).
D_{15-0}	I	**Direct Data Input.** This 16-bit data word may be selected by the $I_{0,1,2}$ lines as an input to the ALU.
Y_{15-0}	I	**Data Output.** These are three-state data output lines which, when enabled, output either the ALU result or the data in the A latch, as determined by the code on $I_{6,7,8}$.
$\overline{OE}$	I	**Output Enable.** This is an active LOW input which controls the Y_{15-0} outputs. A HIGH level on this signal places the output drivers at the high impedance state.
CP	I	**Clock.** The LOW level of CP is used to write data to the RAM register file. A HIGH level of CP writes data from the dual port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the LOW level of CP and transferred from master to slave during CP = HIGH.
Q_{15}, RAM_{15}	I/O	These two lines are bidirectional and are controlled by $I_{6,7,8}$. They are three-state output drivers connected to the TTL compatible CMOS inputs.
Q_{15}, RAM_{15} (Cont.)	I/O	**Output Mode:** When the destination code on lines $I_{6,7,8}$ indicates a left shift (UP) operation, the three-state outputs are enabled and the MSB of the Q register is output on the Q_{15} pin and likewise, the MSB of the ALU output (F_{15}) is output on the RAM 15 pin. **Input Mode:** When the destination code indicates a right shift (DOWN), the pins are the data inputs to the MSB of the Q register and the RAM, respectively.
Q_0, RAM_0	I/O	These two lines are bidirectional and function similarly to the Q_{15} and RAM_{15} lines. The Q_0 and RAM_0 lines are the LSB of the Q register and the RAM.
C_n	I	**Carry In.** The carry in to the internal ALU.
$C_n + 16$	O	**Carry Out.** The carry out from the internal ALU.
$\overline{G}$, $\overline{P}$	O	**Carry Generate, Carry Propagate.** Outputs from the ALU which may be used to perform a carry look-ahead operation over the 16-bits of the ALU.
OVR	O	**Overflow.** This signal is the logical exclusive-OR of the carry-in and carry-out of the MSB of the ALU. This indicates when the result of the ALU operation exceeded the capacity of the machine's two's complement number range. It is valid only for the sign bit.
F = 0	O	**Zero Detect.** Open drain output which goes HIGH when the data on outputs (F_{15-0}) are all LOW. It indicates that the result of an ALU operation is zero (positive logic assumed).
F_{15}	O	**Sign.** The MSB of the ALU output.

Top View

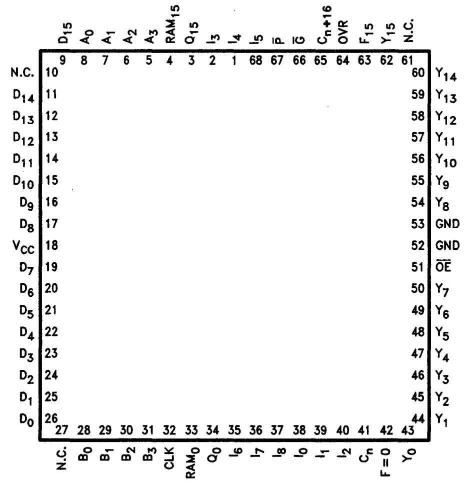

Y_1 51
Y_2 50
Y_4 48
Y_6 46
$\overline{OE}$ 44
NC 42
Y_8 40
Y_{10} 38
Y_{12} 36
F=0 53
Y_0 52
Y_3 49
Y_5 47
Y_7 45
V_{SS} 43
V_{SS} 41
Y_9 39
Y_{11} 37
Y_{13} 35
Y_{14} 34
I_2 55
C_n 54
F_{15} 32
Y_{15} 33
I_0 57
I_1 56
C_{n+16} 30
OVR 31
I_7 59
I_8 58
$\overline{P}$ 28
$\overline{G}$ 29
Q_0 61
I_6 60
I_4 26
I_5 27
CP 63
RAM_0 62
Q_{15} 24
I_3 25
B_2 65
B_3 64
A_3 22
RAM_{15} 23
B_0 67
B_1 66
A_1 20
A_2 21
D_0 68
D_1 1
D_3 3
D_5 5
D_7 7
NC 9
D_8 11
D_{10} 13
D_{12} 15
D_{15} 18
A_0 19
D_2 2
D_4 4
D_6 6
V_{CC} 8
V_{CC} 10
D_9 12
D_{11} 14
D_{13} 16
D_{14} 17

0079-11

CY7C9101 Pinout for 68PGA

NC = No Connect

Top View


D_{15} 9
A_0 8
A_1 7
A_2 6
A_3 5
RAM_{15} 4
Q_{15} 3
I_3 2
I_4 1
I_5 68
$\overline{P}$ 67
$\overline{G}$ 66
C_{n+16} 65
OVR 64
F_{15} 63
Y_{15} 62
N.C. 61
N.C. 10
D_{14} 11
D_{13} 12
D_{12} 13
D_{11} 14
D_{10} 15
D_9 16
D_8 17
V_{CC} 18
D_7 19
D_6 20
D_5 21
D_4 22
D_3 23
D_2 24
D_1 25
D_0 26
60 Y_{14}
59 Y_{13}
58 Y_{12}
57 Y_{11}
56 Y_{10}
55 Y_9
54 Y_8
53 GND
52 GND
51 $\overline{OE}$
50 Y_7
49 Y_6
48 Y_5
47 Y_4
46 Y_3
45 Y_2
44 Y_1
27 N.C.
28 B_0
29 B_1
30 B_2
31 B_3
32 CLK
33 RAM_0
34 Q_0
35 I_6
36 I_7
37 I_8
38 I_0
39 I_1
40 I_2
41 C_n
42 F=0
43 Y_0

0079-3

CY7C9101 Pinout for LCC/PLCC

NC = No Connect

Functional Tables

Table 1. ALU Source Operand Control

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Table 3. ALU Destination Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_{15}	X	Q_{15}

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
A = Register Addressed by A inputs.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Table 4. Source Operand and ALU Function Matrix

	I_{210} Octal	0	1	2	3	4	5	6	7
	ALU Source								
Octal I_{543}	ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	$C_n = L$ R plus S $C_n = H$	$A+Q$ $A+Q+1$	$A+B$ $A+B+1$	Q $Q+1$	B $B+1$	A $A+1$	$D+A$ $D+A+1$	$D+Q$ $D+Q+1$	D $D+1$
1	$C_n = L$ S minus R $C_n = H$	$Q-A-1$ $Q-A$	$B-A-1$ $B-A$	$Q-1$ Q	$B-1$ B	$A-1$ A	$A-D-1$ $A-D$	$Q-D-1$ $Q-D$	$-D-1$ $-D$
2	$C_n = L$ R minus S $C_n = H$	$A-Q-1$ $A-Q$	$A-B-1$ $A-B$	$-Q-1$ $-Q$	$-B-1$ $-B$	$-A-1$ $-A$	$D-A-1$ $D-A$	$D-Q-1$ $D-Q$	$D-1$ D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

$+$ = Plus; $-$ = Minus; $\vee$ = OR; $\wedge$ = AND; $\veebar$ = EX-OR

Description of Architecture

General Description

The 7C9101 block diagram is shown in Figure 1. Detailed block diagrams show the operation of specific sections as described below. The device is a 16-bit slice consisting of a register file (16-word by 16-bit dual port RAM), the ALU, the Q-register and the necessary control logic. It is expandable in 16-bit increments.

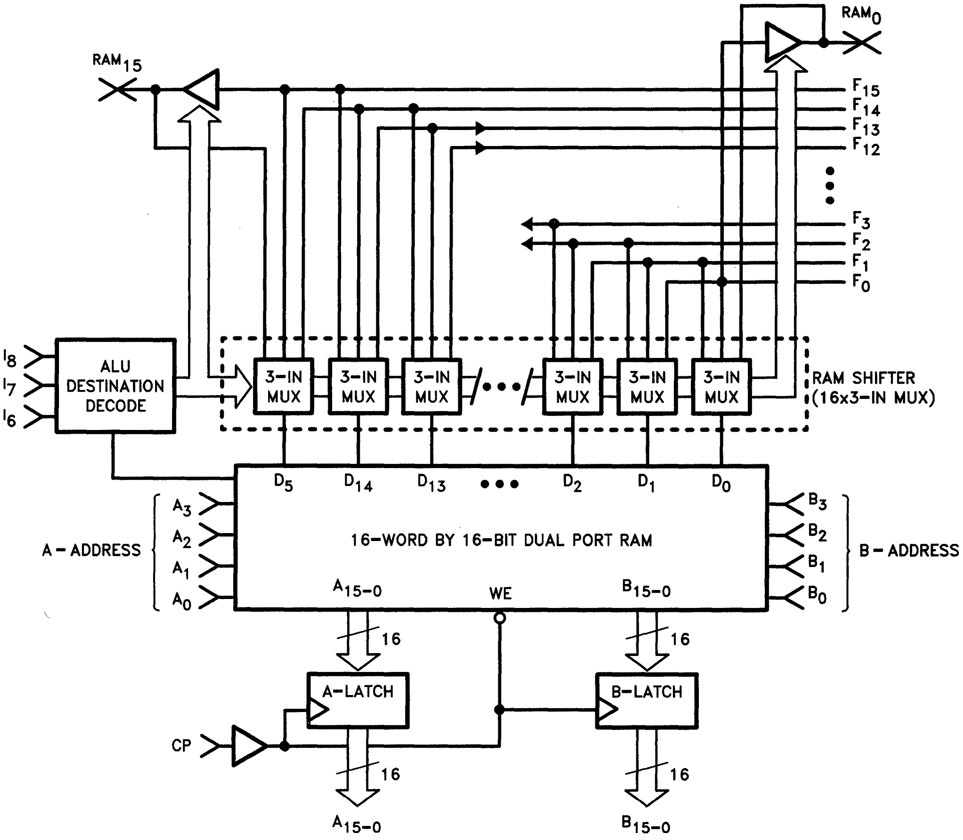
Register File

The dual port RAM is addressed by two 4-bit address fields (A_{3-0} and B_{3-0}) which cause the data to simultaneously appear at the A or B (internal) ports. Both the A and B addresses may be identical; in this case, the same data will appear at both the A and B ports.

Data to be written to RAM is applied to the D inputs of the 7C9101 and is passed (unchanged) through the ALU to the RAM location specified by the B-address word. New data is written into the RAM by specifying a B address while RAM write enable (RAM EN) is active and the clock input is LOW. RAM EN is an internal signal decoded from the signals $I_{6,\,7,\,8}$. As shown below, each of the 16 RAM inputs is driven by a three-input multiplexer that allows the ALU output (F_{15-0}) to be shifted one bit position to the left, right, or not shifted. The RAM_{15} and RAM_0 I/O pins are also inputs to the 16-bit, 3-input multiplexer.

During the left shift (upshift) operation, the RAM_{15} output buffer and RAM_0 input multiplexer are enabled. For the down shift (right) operation, the RAM_0 output buffer and the RAM_{15} input multiplexer are enabled.

The A and B outputs of the RAM drive separate 16-bit latches that are enabled (track the RAM data) when the clock is HIGH. The outputs of the A latch go to three multiplexers which feed the two ALU inputs (R_{15-0} and S_{15-0}) and the chip output (Y_{15-0}). The B latch outputs are directed to the multiplexer which feeds the S input to the ALU.



RAM15
RAM0
F15
F14
F13
F12
F3
F2
F1
F0
I8
I7
I6
ALU DESTINATION DECODE
3-IN MUX
RAM SHIFTER (16x3-IN MUX)
D5
D14
D13
D2
D1
D0
A-ADDRESS
A3
A2
A1
A0
16-WORD BY 16-BIT DUAL PORT RAM
A15-0
WE
B15-0
B3
B2
B1
B0
B-ADDRESS
16
A-LATCH
B-LATCH
CP
A15-0
B15-0

0079-4

Figure 2. Register File

Description of Architecture (Continued)

Q-Register

The Q-register is mainly intended for use as a separate working register for multiplication and division routines. It may also function as an accumulator or temporary storage register. Sixteen master-slave latches are used to implement the Q-register. As shown below, the Q-register inputs are driven by the outputs of the Q-shifter (sixteen 3-input multiplexers, under the control of $I_{6, 7, 8}$). The function of the Q-register input multiplexers is to allow the ALU output (F_{15-0}) to be either shifted left, right, or directly entered into the master latches. The Q_{15} and Q_0 pins (I/O) function similarly to the RAM_{15} and RAM_0 pins described earlier. Data is entered into the master latches when the clock is LOW and transferred to the slave (output) at the clock LOW to HIGH transition.

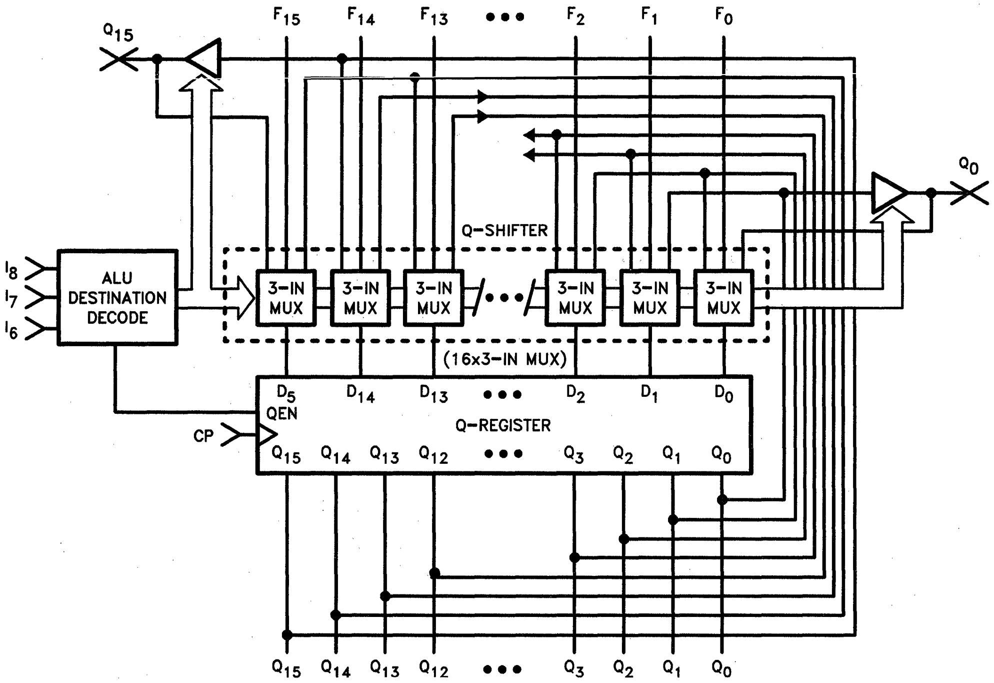

Q15
F15
F14
F13
•••
F2
F1
F0
Q0
Q-SHIFTER
I8
I7
I6
ALU DESTINATION DECODE
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
3-IN MUX
(16x3-IN MUX)
D5
D14
D13
•••
D2
D1
D0
QEN
CP
Q-REGISTER
Q15 Q14 Q13 Q12 ••• Q3 Q2 Q1 Q0
Q15 Q14 Q13 Q12 ••• Q3 Q2 Q1 Q0
0079-5

Figure 3. Q-Register

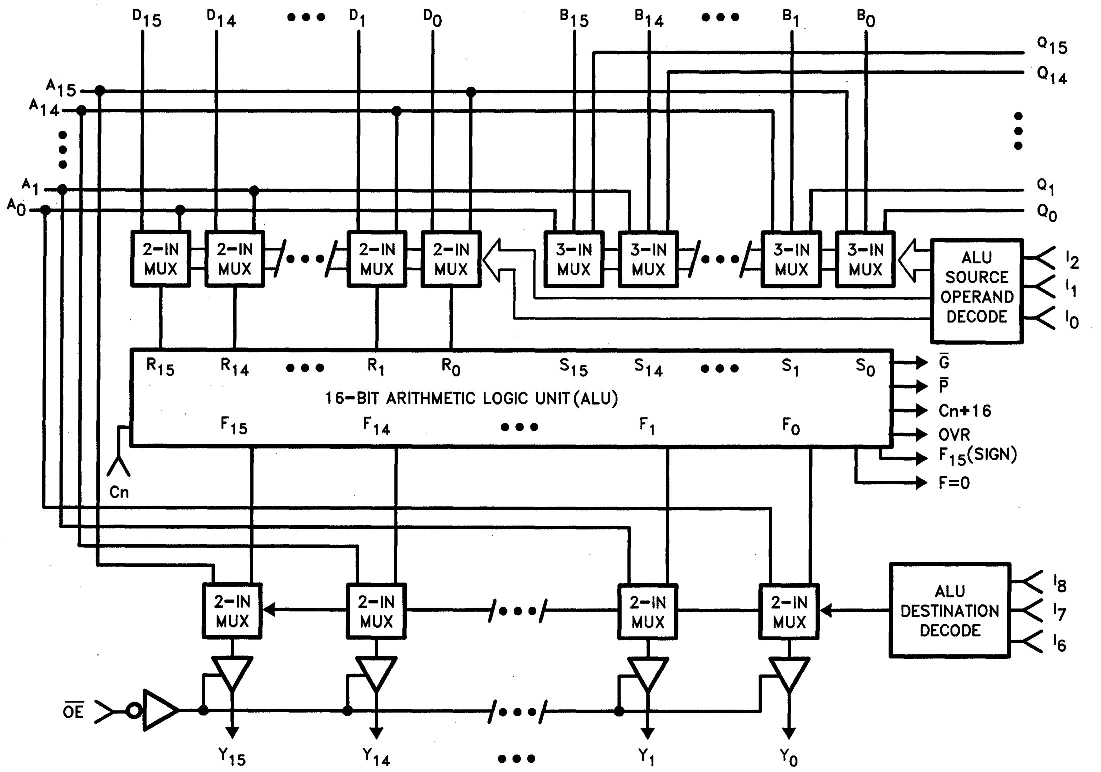
Description of Architecture (Continued)

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on the two 16-bit input operands, R and S. The R-input multiplexer selects between data from the RAM A-port and data at the external data input, D_{15-0}. The S-input multiplexer selects between data from the RAM A-port, the RAM B-port, and the Q-register. The R and S multiplexers are controlled by the $I_{0, 1, 2}$ inputs as shown in Table 1. The R and S input multiplexers each have an "inhibit capability," offering a state where no data is passed. This is equivalent to a source operand consisting of all zeroes. The R and S ALU source multiplexers are configured to allow eight pairs of combinations of A, B, D, Q, and "0" to be selected as ALU input operands.

The ALU functions, which are controlled by $I_{3, 4, 5}$, are shown in Table 2. Carry lookahead logic is resident on the 7C9101, using the ALU inputs carry in (C_n) and the ALU outputs carry propagate ($\overline{P}$), carry generate ($\overline{G}$), carry out (C_{n+16}), and overflow to implement carry lookahead arithmetic and determine if arithmetic overflow has occurred. Note that the carry in (C_n) signal affects the arithmetic result and internal flags; it has no effect on the logical operations.

Control signals $I_{6, 7, 8}$ route the ALU data output (F_{15-0}) to the RAM, the Q-register inputs, and the Y-outputs as shown in Table 3. The ALU result MSB (F_{15}) is output so the user may examine the sign bit without needing to enable the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open drain output which may be wire OR'ed across multiple 7C9101 processor slices.


D15
D14
D1
D0
B15
B14
B1
B0
Q15
Q14
Q1
Q0
A15
A14
A1
A0
2-IN MUX
3-IN MUX
ALU SOURCE OPERAND DECODE
I2
I1
I0
R15
R14
R1
R0
S15
S14
S1
S0
16-BIT ARITHMETIC LOGIC UNIT (ALU)
F15
F14
F1
F0
G
P
Cn+16
OVR
F15(SIGN)
F=0
Cn
ALU DESTINATION DECODE
I8
I7
I6
OE
Y15
Y14
Y1
Y0

0079-6

Figure 4. ALU

Description of Architecture (Continued)

Table 5. ALU Logic Mode Functions

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	“ZERO”	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{543}, I_{210}	$C_n = 0$ (Low)		$C_n = 1$ (High)	
	Group	Function	Group	Function
0 0	ADD	$A+Q$	ADD plus one	$A+Q+1$
0 1		$A+B$		$A+B+1$
0 5		$D+A$		$D+A+1$
0 6		$D+Q$		$D+Q+1$
0 2	PASS	Q	Increment	$Q+1$
0 3		B		$B+1$
0 4		A		$A+1$
0 7		D		$D+1$
1 2	Decrement	$Q-1$	PASS	Q
1 3		$B-1$		B
1 4		$A-1$		A
2 7		$D-1$		D
2 2	1’s Comp.	$-Q-1$	2’s Comp. (Negate)	$-Q$
2 3		$-B-1$		$-B$
2 4		$-A-1$		$-A$
1 7		$-D-1$		$-D$
1 0	Subtract (1’s Comp.)	$Q-A-1$	Subtract (2’s Comp.)	$Q-A$
1 1		$B-A-1$		$B-A$
1 5		$A-D-1$		$A-D$
1 6		$Q-D-1$		$Q-D$
2 0		$A-Q-1$		$A-Q$
2 1		$A-B-1$		$A-B$
2 5		$D-A-1$		$D-A$
2 6		$D-Q-1$		$D-Q$

Conventional Addition and Pass-Increment/ Decrement

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation. In logical operations, the carry-in (C_n) will not affect the ALU output.

Subtraction

Recall that in two’s complement integer coding -1 is equal to all ones and that in one’s complement integer coding zero is equal to all ones. To convert a positive integer to its two’s complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In Table 6 the symbol $-Q$ represents the two’s complement of Q so that the one’s complement of Q is then $-Q-1$.

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description		Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min. $I_{OH} = -3.4$ mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min. I_{OL} = 16 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$ V_{CC} = Max.	−10	10	μA
I_{OH}	Output HIGH Current		V_{CC} = Min. V_{OH} = 2.4V	−3.4		mA
I_{OL}	Output LOW Current		V_{CC} = Min. V_{OL} = 0.4V	16		mA
I_{OZ}	Output Leakage Current		V_{CC} = Max. $V_{OUT} = V_{SS}$ to V_{CC}	−40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]		V_{CC} = Max. V_{OUT} = 0V		−85	mA
$I_{CC}(Q_1)$[2]	Supply Current (Quiescent)	Commercial	$V_{SS} \leq V_{IN} \leq V_{IL}$ or		30	mA
		Military	$V_{IH} \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		35	
$I_{CC}(Q_2)$[2]	Supply Current (Quiescent)	Commercial	$V_{SS} \leq V_{IN} \leq 0.4V$ or		25	mA
		Military	$3.85V \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		30	
I_{CC}(Max.)[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz;		60	mA
		Military	$\overline{OE}$ = HIGH		85	

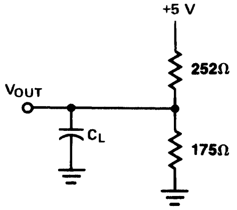
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

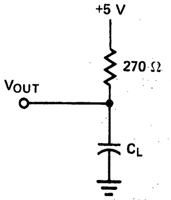
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given frequency, use $I_{CC}(Q_1) + I_{CC}$(A.C.) where $I_{CC}(Q_1)$ is shown above and I_{CC}(A.C.) = (3 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC}(A.C.) = (5 mA/MHz) × Clock Frequency for Military temperature range.
3. Tested on a sample basis.

Output Loads used for AC Performance Characteristics



0079-9

All Outputs except Open Drain



0079-10

Open Drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.

Table 7. Logic Functions for CARRY and OVERFLOW Conditions

I_{543}	Function	$\overline{P}$	$\overline{G}$	$C_n + 16$	OVR
0	R+S	$\overline{P_0 - P_{15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_{1-15}\,G_0}$	C_{16}	$C_{16} \veebar C_{15}$
1	S−R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R−S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$\overline{R} \wedge S$				
6	$R \veebar S$				
7	$\overline{R \veebar S}$				

Definitions: + = OR

$P_{0-15} = P_{15}\,P_{14}\,P_{13}\,P_{12}\,P_{11}\,P_{10}\,P_9\,P_8\,P_7\,P_6\,P_5\,P_4\,P_3\,P_2\,P_1\,P_0$
$P_0 = R_0 + S_0$
$P_1 = R_1 + S_2$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$, etc.

$G_{0-15} = G_{15}\,G_{14}\,G_{13}\,G_{12}\,G_{11}\,G_{10}\,G_9\,G_8\,G_7\,G_6\,G_5\,G_4\,G_3\,G_2\,G_1\,G_0$
$G_0 = R_0\,S_0$
$G_1 = R_1\,S_1$
$G_2 = R_2\,S_2$
$G_3 = R_3\,S_3$, etc.
$C_{16} = G_{15} + P_{15}\,G_{14} + P_{15}\,P_{14}\,G_{13} + \ldots + P_{0-15}\,C_n$
$C_{15} = G_{14} + P_{14}\,G_{13} + P_{14}\,P_{13}\,G_{12} + \ldots + P_{0-14}\,C_n$

CY7C9101-30 and CY7C9101-40 Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

Cycle Time and Clock Characteristics

CY7C9101-	30	40
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	30 ns	40 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	33 MHz	25 MHz
Minimum Clock LOW Time	20 ns	25 ns
Minimum Clock HIGH Time	10 ns	15 ns
Minimum Clock Period	30 ns	40 ns

This data applies to parts with the following numbers:

CY7C9101-30PC CY7C9101-30DC CY7C9101-30LC CY7C9101-30JC CY7C9101-30GC
CY7C9101-40PC CY7C9101-40DC CY7C9101-40LC CY7C9101-40JC CY7C9101-40GC

Combinational Propagation Delays. C_L = 50 pF

To Output / From Input	Y		F_{15}		$C_n + 16$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_{15}		Q_0 Q_{15}	
CY7C9101-	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**
A, B Address	37	47	36	47	35	44	32	41	35	46	32	42	32	40	—	—
D	29	34	28	34	25	32	25	30	29	36	21	26	27	33	—	—
C_n	22	27	22	27	20	25	—	—	22	26	22	26	24	30	—	—
$I_{0,1,2}$	32	40	32	40	30	38	28	36	34	42	26	32	27	35	—	—
$I_{3,4,5}$	34	43	33	42	33	42	27	35	34	40	32	42	29	38	—	—
$I_{6,7,8}$	19	22	—	—	—	—	—	—	—	—	—	—	22	26	22	26
A Bypass ALU (I = 2XX)	25	30	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↗	31	40	30	39	30	38	27	34	28	37	27	34	27	35	20	23

Set-Up and Hold Times Relative to Clock (CP) Input[1]

Input	CP: Set-Up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C9101-	30	40	30	40	30	40	30	40
A, B Source Address	10	15	3[3]	3[3]	30[4]	40[4]	0	0
B Destination Address	10	15	← Do Not Change[2] →				0	0
D	—	—	—	—	22	28	0	0
C_n	—	—	—	—	16	22	0	0
$I_{0, 1, 2}$	—	—	—	—	26	35	0	0
$I_{3, 4, 5}$	—	—	—	—	29	37	0	0
$I_{6, 7, 8}$	10	12	← Do Not Change[2] →				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	11	14	0	0

Output Enable/Disable Times

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101-30	$\overline{OE}$	Y	18	16
CY7C9101-40	$\overline{OE}$	Y	22	19

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

CY7C9101-35 and CY7C9101-45 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

This data applies to parts with the following numbers:

CY7C9101-35DMB CY7C9101-35LMB CY7C9101-35GMB
CY7C9101-45DMB CY7C9101-45LMB CY7C9101-45GMB

Cycle Time and Clock Characteristics

CY7C9101-	35	45
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	35 ns	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	28 MHz	22 MHz
Minimum Clock LOW Time	23 ns	28 ns
Minimum Clock HIGH Time	12 ns	17 ns
Minimum Clock Period	35 ns	45 ns

Combinational Propagation Delays $C_L = 50$ pF

To Output From Input	Y		F_{15}		C_{n+16}		$\overline{G}$, $\overline{P}$		F = 0		OVR		RAM_0 RAM_{15}		Q_0 Q_{15}	
CY7C9101-	35	45	35	45	35	45	35	45	35	45	35	45	35	45	35	45
A, B Address	41	52	40	51	38	48	37	45	40	48	36	46	36	43	—	—
D	31	37	31	36	29	36	28	32	33	40	23	32	30	35	—	—
C_n	25	30	24	29	23	27	—	—	24	29	23	27	26	31	—	—
$I_{0,1,2}$	36	44	35	43	33	41	31	38	38	46	29	38	30	38	—	—
$I_{3,4,5}$	38	48	37	47	37	46	31	38	38	45	36	45	33	41	—	—
$I_{6,7,8}$	21	24	—	—	—	—	—	—	—	—	—	—	24	28	24	28
A Bypass ALU (I = 2XX)	28	33	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock _/‾	35	44	34	43	34	42	30	37	34	40	28	38	30	37	21	25

Set-Up and Hold Times Relative to Clock (CP) Input[1]

Input	CP: Set-Up Time Before H → L		Hold Time After H → L		Set-Up Time Before L → H		Hold Time After L → H	
CY7C9101-	35	45	35	45	35	45	35	45
A, B Source Address	12	17	3[3]	3[3]	35[4]	45[4]	0	0
B Destination Address	12	17	← Do Not Change[2] →				1	1
D	—	—	—	—	25	30	0	0
C_n	—	—	—	—	19	24	0	0
$I_{0,1,2}$	—	—	—	—	30	37	0	0
$I_{3,4,5}$	—	—	—	—	33	40	0	0
$I_{6,7,8}$	12	16	← Do Not Change[2] →				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	13	15	1	1

Output Enable/Disable Times

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101-35	$\overline{OE}$	Y	20	17
CY7C9101-45	$\overline{OE}$	Y	23	20

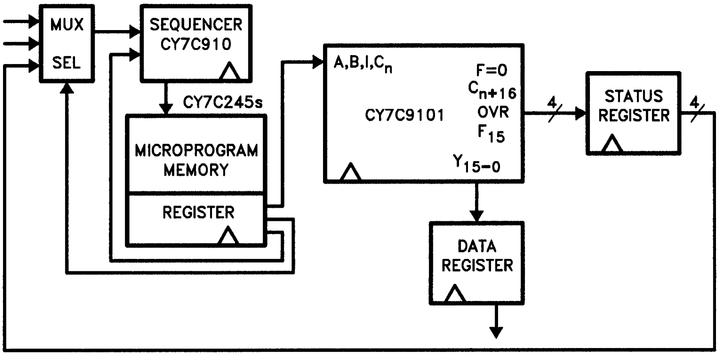
Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

Applications

Minimum Cycle Time Calculations for 16-Bit Systems

Speeds used in calculations for parts other than CY7C9101 and CY7C910 are representative for available MSI parts.

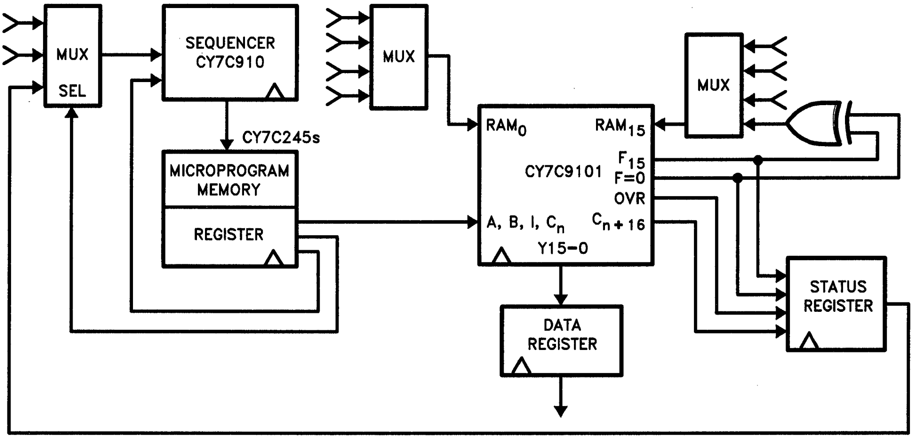

MUX
SEL
SEQUENCER
CY7C910
CY7C245s
MICROPROGRAM
MEMORY
REGISTER
A,B,I,C_n
CY7C9101
F=0
C_{n+16}
OVR
F_{15}
Y_{15-0}
4
STATUS
REGISTER
4
DATA
REGISTER

0079-15

Pipelined System, Add without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
Register	Setup	4	CY7C910	CC to Output	22
		53 ns	CY7C245	Access Time	20
					66 ns

Minimum Clock Period = 66 ns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SEQUENCER
CY7C910
CY7C245s
MICROPROGRAM
MEMORY
REGISTER
MUX
RAM_0
RAM_{15}
CY7C9101
F_{15}
F=0
OVR
A, B, I, C_n
C_{n+16}
Y15-0
MUX
STATUS
REGISTER
DATA
REGISTER

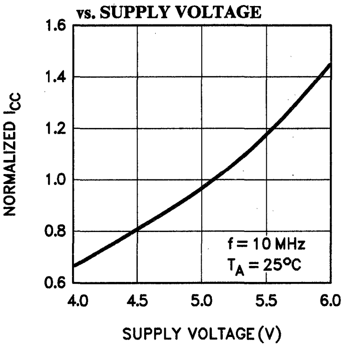
0079-13

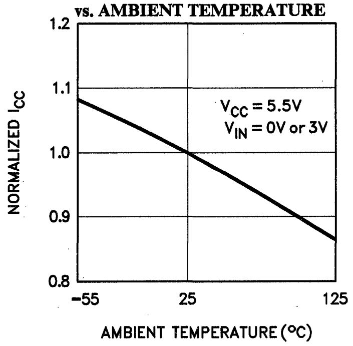
Pipelined System, Simultaneous Add and Shift Down (RIGHT)

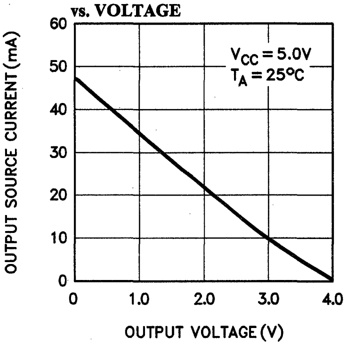
	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C9101	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
XOR and MUX	Prop. Delay, Select to Output	20	CY7C910	CC to Output	22
			CY7C245	Access Time	20
CY7C9101	RAM_{15} Setup	11			66 ns
		80 ns			

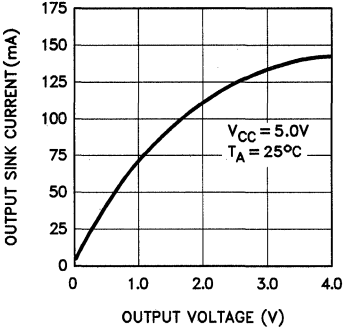
Minimum Clock Period = 80 ns

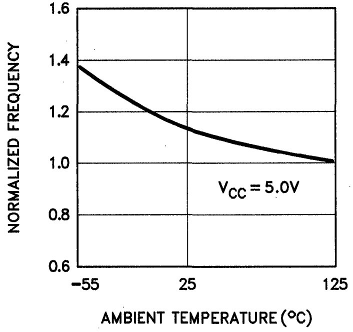
Typical DC and AC Characteristics

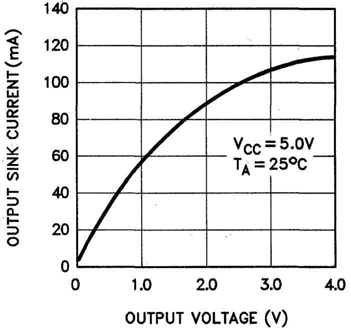

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

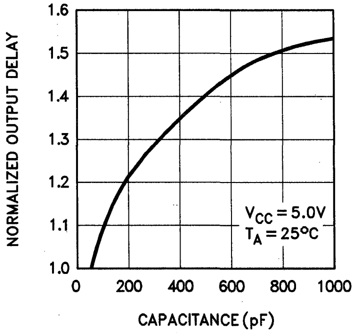

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

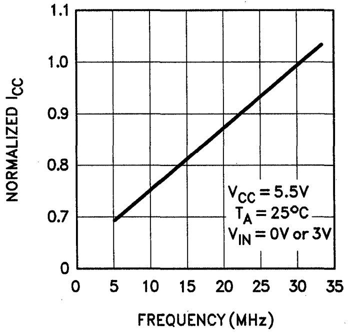

OUTPUT SOURCE CURRENT vs. VOLTAGE


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


TYPICAL OUTPUT DELAY CHANGE vs. OUTPUT LOADING


NORMALIZED I_{CC} vs. FREQUENCY

0079–14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C9101-30 PC	P29	Commercial
	CY7C9101-30 LC	L81	
	CY7C9101-30 JC	J81	
	CY7C9101-30 DC	D30	
	CY7C9101-30 GC	G68	
40	CY7C9101-40 PC	P29	
	CY7C9101-40 LC	L81	
	CY7C9101-40 JC	J81	
	CY7C9101-40 DC	D30	
	CY7C9101-40 GC	G68	
35	CY7C9101-35 LMB	L81	Military
	CY7C9101-35 DMB	D30	
	CY7C9101-35 GMB	G68	
45	CY7C9101-45 LMB	L81	
	CY7C9101-45 DMB	D30	
	CY7C9101-45 GMB	G68	

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BridgeMOS

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Device Number	Description	
CY8C150	BridgeMOS 1024 x 4 Static RAM Separate I/O	6-1
CY8C245	BridgeMOS 2048 x 8 Reprogrammable Registered PROM	6-1
CY8C291	BridgeMOS Reprogrammable 2048 x 8 PROM	6-1
CY8C901	BridgeMOS 4-Bit Slice	6-1
CY8C909	BridgeMOS Microprogram Sequencer	6-1
CY8C911	BridgeMOS Microprogram Sequencer	6-1

CYPRESS SEMICONDUCTOR

BridgeMOS

Features

- **May be driven by CMOS or TTL**
- **Drives fully loaded TTL**
  - **Inputs switch at 1.5V**
- **Can drive CMOS to full input levels**
  - **$V_{OL} = 0.2V$ @ $I_{OL} = 20\ \mu A$**
  - **$V_{OH} = 0.9\ V_{CC}$ @ $I_{OH} = -20\ \mu A$**
- **SRAM, PROM, LOGIC**
- **2.0V (V_{CC}) Data Retention on all devices**

Overview

The BridgeMOS™ product line from Cypress Semiconductor provides an electrical bridge between CMOS and TTL or TTL and CMOS devices. BridgeMOS devices may be driven by either TTL or CMOS devices and in turn can drive either fully loaded TTL or CMOS to full input levels. As a result, any combination of TTL and/or CMOS may be interfaced to Cypress BridgeMOS products.

All devices in the BridgeMOS product line are specified at a 2.0V (V_{CC}) standby mode of operation. This allows the device to be powered at 2.0 volts and maintain the integrity of the data in any volatile storage element.

The output drivers in the 7CXXX Cypress products are designed for TTL signals and pull up to 2.4 volts. For BridgeMOS, Cypress has designed an output driver which boosts the output voltage sufficiently to drive the inputs of a device to greater than 3.85 volts, thus guaranteeing that the input converter will draw minimum power. The output drivers source 20 microamps at their rated BridgeMOS levels. They will also source and drive normal TTL loads. Therefore, they are capable of driving other non-BridgeMOS loads and normal TTL loads at the same time.

Although the TTL to CMOS input converters power down as described above, they switch at TTL levels and all timing is referenced to 1.5 volts. The device will operate at normal TTL levels with no AC performance degradation.

CY8C150 Selection Guide

		8C150-15	8C150-25	8C150-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military		25	35
Maximum Operating Current (mA)	Commercial	100	100	100
	Military		125	125

CY8C245 Selection Guide

		8C245-35	8C245-45
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commercial	45	45
	Military	80	80

CY8C291 Selection Guide

		8C291-35	8C291-50
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commercial	45	45
	Military	80	80

CY8C901 Selection Guide

Read Modify-Write Cycle (min.) in ns	Operating I_{CC} (max.) in mA	Operating Range	Part Number
31	26.5	Commercial	8C901-31
32	31.0	Military	8C901-32

CY8C909/8C911 Selection Guide

	8C909-30 8C911-30	8C909-40 8C911-40
Minimum Clock to Output Cycle Time (ns)	30	40
Maximum Operating Current (mA)	15	15

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QuickPro

Device Number	Description	Page Number
CY3000	Combined PROM, PLD, and EPROM Programmer	7-1

CYPRESS
SEMICONDUCTOR

CY3000

QuickPro™

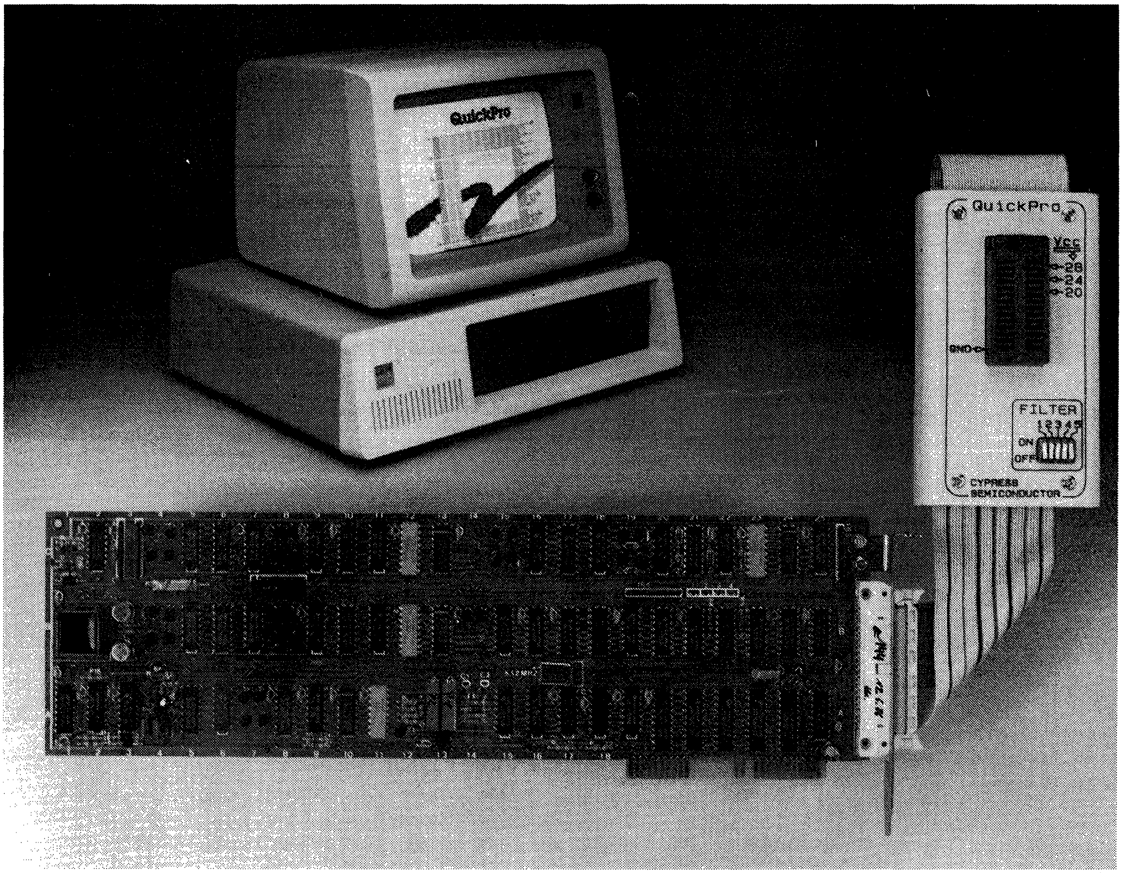
Features

- Combined PROM, PLD, and EPROM programmer
- Programs all Cypress CMOS PLDs and PROMs. (All future devices will also be supported)
- Reads bipolar PLDs and PROMs
- Easy to use, menu-driven software
- New device updates via floppy disk
- IBM-PC® plug-in card format, external ZIP-DIP socket
- Compatible with the IBM PC family of computers and plug compatibles
- Programs 24- and 28-pin NMOS and CMOS EPROMs
- One long slot and 256K bytes of memory required
- Designed for present and future NMOS and CMOS devices
- Optional LCC socket adapter

Description

QuickPro is a development tool for present and future CMOS PROM and PLD devices, and is used within the IBM PC and compatible environment. Older generation bipolar PLDs and PROMs required special programming voltages and current difficult to generate within the IBM PC.

QuickPro is designed for new generation of CMOS PLDs and PROMs which obsolete the older technology, and use a programming technique



0095–1

QuickPro is a trademark of Cypress Semiconductor Corporation.
IBM and IBM PC are registered trademarks of International Business Machines Corporation.
ABEL™ is a registered trademark of Data I/O Corporation.
CUPL™ is a registered trademark of Assisted Technology.
PALASM™ is a registered trademark of Monolithic Memories Inc.

Description (Continued)

which is more compatible with low cost programming methods.

QuickPro can also program standard NMOS and CMOS EPROMs and in packages up to 28 pins. And QuickPro is fast; intelligent programming is used to reduce programming time to a minimum.

QuickPro is future oriented. Each I/O pin is fully programmable, allowing the parameters and timing of each device to be handled via software. As new devices become available, they will be supported by QuickPro. Updates are managed by a simple exchange of floppy disks.

QuickPro includes a comprehensive set of commands to make programming PLDs and PROMs as easy as possible.

For PLDs, QuickPro uses the JEDEC standard data format, so present and future logic design tools such as ABEL™, CUPL™, and PALASM™ can be used. QuickPro avoids serial download problems from a PC to a stand-alone programmer. For PROMs, QuickPro reads PCDOS binary files for use with assemblers and compilers. And QuickPro is low cost, each workstation can have one, eliminating the inconvenience of sharing one expensive programmer. All actions are menu-driven, with complete explanations provided on-screen, in clear text. There is no need to look up manufacturer's codes in a table.

QuickPro Commands

- Program device
- Select device type
- Edit memory
- Display memory
- Read device
- Test PLD device
- Calculate checksum
- Read disk file
- Write disk file
- Verify device
- Blank check device
- Program security fuse
- Fill memory
- Convert PLD type

Technical Information

Size

IBM PC standard full length card. Uses port addresses 300–31F hex.

Power

+5V	1.0 amp
+12V	1.0 amp (peak) 0.4 amp average
−12V	0.05 amp

Socket Pod

This is the external socket for connection to the device to be programmed or read. It provides a 28-pin 300/600 mil socket for compatibility with a wide range of devices. Other adapters for leadless packages also available. Five filter switches are located on the pod for bypass capacitors according to manufacturers' published programming specifications.

Memory

256K bytes of total memory is sufficient to operate QuickPro.

Devices Supported

Cypress CMOS PROMs:
CY7C225, CY7C235, CY7C245, CY7C251, CY7C253, CY7C254, CY7C261, CY7C263, CY7C264, CY7C268, CY7C269, CY7C271, CY7C281, CY7C282, CY7C291, CY7C292

Cypress CMOS PLDs:
PAL16L8, PAL16R4, PAL16R6, PAL16R8, PAL22V10, PLD20G10

QuickPro can read 20 and 24 pin Bipolar PLDs, for conversion to Cypress PLDs.

EPROMs: (NMOS and CMOS)
2716, 2732, 2732A, 2764, 2764A, 27128, 27256

Ordering Information

CY3000	QuickPro System ($995.00) contains:
CY3001	QuickPro Board
CY3002	QuickPro Pod
CY3003	QuickPro System Disc Quick Pro Manual

QuickPro Package Adaptors Include:

CY3004 (CY3006) 28 Lead Square (P)LCC:
7C225, 7C235, 7C245, 7C261, 7C263, 7C264, 7C281, 7C282, 7C291, 7C292, PALC22V10

CY3005 (CY3007) 20 Lead Square (P)LCC:
16L8, 16R4, 16R6, 16R8

CY3008 (CY3009) 28 Lead Square (P)LCC:
7C251, 7C253, 7C254, 7C269, 7C271, 7C330, 7C331, 7C332

CY3010 (CY3011) 28 Lead Square (P)LCC:
PLDC20G10

CY3012 (CY3013) 32 Lead Rectangular (P)LCC:
7C268

CY3014 28 Pin SOIC:
7C225, 7C235, 7C245, 7C251, 7C253, 7C254, 7C261, 7C263, 7C264, 7C269, 7C271, 7C281, 7C282, 7C291, 7C292

CY3015 32 Pin SOIC:
7C268

CY3016 32 Pin DIP:
7C268

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Quality and Reliability

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Quality, Reliability and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability starts at the initial design inception. It is built into every product design from the very start.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883C and MIL-M-38510F as baseline documents to determine our Test Methods, Procedures and General Specifications for semiconductors.

Customers using our Commercial grade product receive the benefit of a military patterned process flow at no additional charge.

Product Testing Categories

Four different testing categories are offered by Cypress:

1) Commercial operating range product: 0°C to +70°C.
2) Military Grade product processed to MIL-STD-883C; Military operating range: −55°C to +125°C.
3) SMD (Standard Military Drawing) certified product; Military operating range: −55°C to +125°C, electrically tested per the applicable Military Drawing.
4) JAN qualified product; Military operating range: −55°C to +125°C, electrically tested per MIL-M-38510 slash sheet requirements.

Category 1 and 2 are available on all products offered by Cypress Semiconductor. Category 3 and 4 are offered on a more limited basis, dependent upon the specific part type in question.

Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in to MIL-STD-883, Method 1015.

Table 1 lists the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet the requirements of these programs.

Military Product Assurance Categories

Only one standard product assurance category exists for JAN, SMD and Military grade products. Cypress' military grade devices are processed per MIL-STD-883C using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

JAN, SMD and Military grade devices supplied by Cypress are processed for applications where maintainance is difficult or expensive and reliability is paramount. Tables 2 through 6 list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883C and MIL-M-38510.

Table 1. Cypress Commercial Product Screening Flows

Screen	MIL-STD-883 Method	Product Temperature Ranges			
		Commercial 0°C to +70°C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• High Temperature Storage	1008, Cond C	Not Performed	100%	Not Performed	100%
• Temperature Cycle	1010, Cond C	Not Performed	Not Performed	Not Performed	Not Performed
• Constant Acceleration	2001, Cond E, Y1 Orientation	Does Not Apply	Not Performed	Does Not Apply	Not Performed
• Hermeticity Check: Fine/Gross Leak	1014, Cond A & B; Fine Leak Cond C; Gross Leak	Does Not Apply	LTPD = 5; 77(1,2)	Does Not Apply	LTPD = 5; 77(1,2)
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	1015	Does Not Apply	Does Not Apply	100%[2]	100%[2]
• Post-Burn-In Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max)[1]	5% (max)[1]
Final Electrical	Per Device Specification				
• Functional, Switching, Dynamic (AC) and Static (DC) Tests	1) At 25°C and Power Supply Extremes	Not Performed	Not Performed	100%[1]	100%[1]
	2) At Hot Temperature and Power Supply Extremes	100%	100%	100%	100%
Cypress Quality Lot Acceptance					
• External Visual	2009	[3]	[3]	[3]	[3]
• Final Electrical Conformance	Cypress Method 17-00064	[3]	[3]	[3]	[3]
• Fine & Gross Leak Conformance	1014, Cond A & B; Fine Leak Cond C; Gross Leak	Does Not Apply	LTPD = 5; 77(1,2)	Does Not Apply	LTPD = 5; 77(1,2)

Notes:

1) Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
2) Burn-in is performed as a standard for 12 hours at 150°C.
3) Lot acceptance testing is performed on every lot to guarantee 200 PPM average outgoing quality.

Table 2. Cypress JAN/SMD/Military Product Screening Flows

Screen	Screening Per Method 5004 of MIL-STD-883C	Product Temperature Range: −55°C to +125°C	
		JAN	SMD/Military Product
Visual/Mechanical			
• Internal Visual	Method 2010, Cond B	100%	100%
• Stabilization Bake (No End Pt. Electricals)	Method 1008, 24 Hrs Cond C, Minimum	100%	100%
• Temperature Cycling	Method 1010, Cond C	100%	100%
• Constant Acceleration	Method 2001, Cond E (Min), Y1 Orientation Only	100%	100%
• Hermeticity			
—Fine Leak	Method 1014, Cond A & B	100%	100%
—Gross Leak	Method 1014, Cond C	100%	100%
Burn-in			
• Initial (Pre-Burn-in) Electrical Parameters	Per Applicable Device Specification	100%	100%
• Burn-in Test	Method 1015, 160 Hrs at 125°C Min or 80 hours at 150°C	100%	100%
• Interim (Post-Burn-in) Electrical Parameters, Percent Defective Allowable (PDA)	Per Applicable Device Specification Maximum PDA, for All Lots, 5%	100%	100%
Final Electrical Tests			
• Static Tests	Method 5005, Table 1, Subgroups 1, 2 and 3	100% Test to Slash Sheet	100% Test to Applicable Device Specification
• Dynamic and Switching Tests	Method 5005, Table 1, Subgroups 4, 5, 6, 9, 10 and 11	100% Test to Slash Sheet	100% Test to Applicable Device Specification
• Functional Tests	Method 5005, Table 1, Subgroups 7 and 8	100% Test to Slash Sheet	100% Test to Applicable Device Specification
Quality Conformance Tests			
• Group A	Method 5005, See Table 3–6 for Details	Sample	Sample
• Group B		Sample	Sample
• Group C		Sample	Sample
• Group D		Sample	Sample

Table 3. Group A Test Descriptions

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military products have a Group A sample test performed as outlined by the particular screen flow.

Subgroup	Description	LTPD	Sample Size/ Accept No.
1	Static Tests at 25°C	2	195/1
2	Static Tests at Maximum Rated Operating Temperature	3	129/1
3	Static Tests at Minimum Rated Operating Temperature	5	77/1
4	Dynamic Tests at 25°C	2	195/1
5	Dynamic Tests at Maximum Rated Operating Temperature	3	129/1
6	Dynamic Tests at Minimum Rated Operating Temperature	5	77/1
7	Functional Tests at 25°C	2	195/1
8	Functional Tests at Minimum and Maximum Temperatures	5	77/1
9	Switching Tests at 25°C	2	195/1
10	Switching Tests at Maximum Temperature	3	129/1
11	Switching Tests at Minimum Temperature	5	77/1

Table 4. Group B Quality Tests

Subgroup	Description	Quantity/Accept # or LTPD
1	Physical Dimensions, Method 2016	2/0
2	Resistance to Solvents, Method 2015	4/0
3	Solderability, Method 2003	10
4	Internal Visual/Mechanical, Method 2014	1/0
5	Bond Strength, Method 2011	15
6	Internal Water Vapor,[2] Method 1018	3/0 or 5/1
7	Seal: Fine & Gross Leak,[1] Method 1014	5
8	ESD Characteristics,[3] Method 3015	15/0

Notes:

1) Fine and Gross Leak is not performed because a 100% screen is employed.
2) Test is only performed if a package contains a dessicant.
3) Test is performed only at qualification and upon redesign.

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 5. Group C Quality Tests

Subgroup	Description	LTPD
1	Steady State Life Test, End Point Electricals, Method 1005	5
2	Temp Cycle, Constant Acceleration Seal: Fine & Gross Leaks, Visual Examination, End Point Electricals Methods 1010, 2001, 1014	15

Group C tests for JAN product are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-M-38510 from each three months production of devices, which is based upon the lot inspection identification (or date) codes.

Group C tests for SMD and Military products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-STD-883 from each twelve months production of devices, which is based upon the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per detailed device specification.

Table 6. Group D Quality Tests (Package Related)

Subgroup	Description	Quantity/Accept # or LTPD
1	Physical Dimensions, Method 2016	15
2	Lead Integrity, Seal: Fine & Gross Leak, Methods 2004 & 1014	15
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 1011, 1010, 1004 & 1014	15
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 & 1014	15
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15
6	Internal Water-Vapor Content; 500 ppm maximum @ 100°C. Method 1018	3/0 or 5/1
7	Adhesion of Lead Finish,[4] Method 2025	15
8	Lid Torque, Method 2024[5]	5/0

Notes:

4) Does not apply to leadless chip carriers.
5) Applies only to packages with glass seals.

Group D tests for JAN product are performed per MIL-M-38510 on each package type from each six months of production, based on the lot inspection identification (or date) codes.

Group D tests for SMD and Military product are performed per MIL-STD-883 on each package type from each twelve months of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per detailed device specification.

Product Screening Summary

Commercial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and Molded packages available
- Incoming Mechanical and Electrical performance guaranteed:
  - — 0.1% AQL Electrical Sample test performed on every lot prior to shipment
  - — 0.65% AQL External Visual Sample inspection
- Electrically tested to Cypress datasheet

Ordering Information

Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number

Ex: CY7C122-15PC

Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add "B" Suffix to Cypress standard part number when ordering to designate Burn-in option
- Parts marked the same as ordered part number

Ex: CY7C122-15PCB

Military Product

- Product processed per MIL-STD-883C, method 5004 product test flows
- Military grade devices electrically tested to Cypress datasheet specifications
- SMD (Standard Military Drawing) devices electrically tested to military drawing specifications

OR

- JAN devices electrically tested to slash sheet specifications
- All devices supplied in Hermetic packages
- Quality conformance assured: Method 5005, Groups A, B, C and D performed as part of the standard process flow
- Burn-in performed on all devices
  - — Cypress detailed circuit specification for non-JAN devices

OR

  - — Slash sheet requirements for JAN products
- AC, DC, Functionally and Dynamically tested at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

Ordering Information

JAN Product:

- Order per Military document
- Marked per Military document

Ex: JM38510/28901BVA

SMD Product:

- Order per Military document
- Marked per Military document

Ex: 5962-8684601EA

Military Grade Product:

- Order per Cypress standard Military part number
- Marked the same as ordered part number

Ex: CY7C122-25DMB

Product Quality Assurance Flow

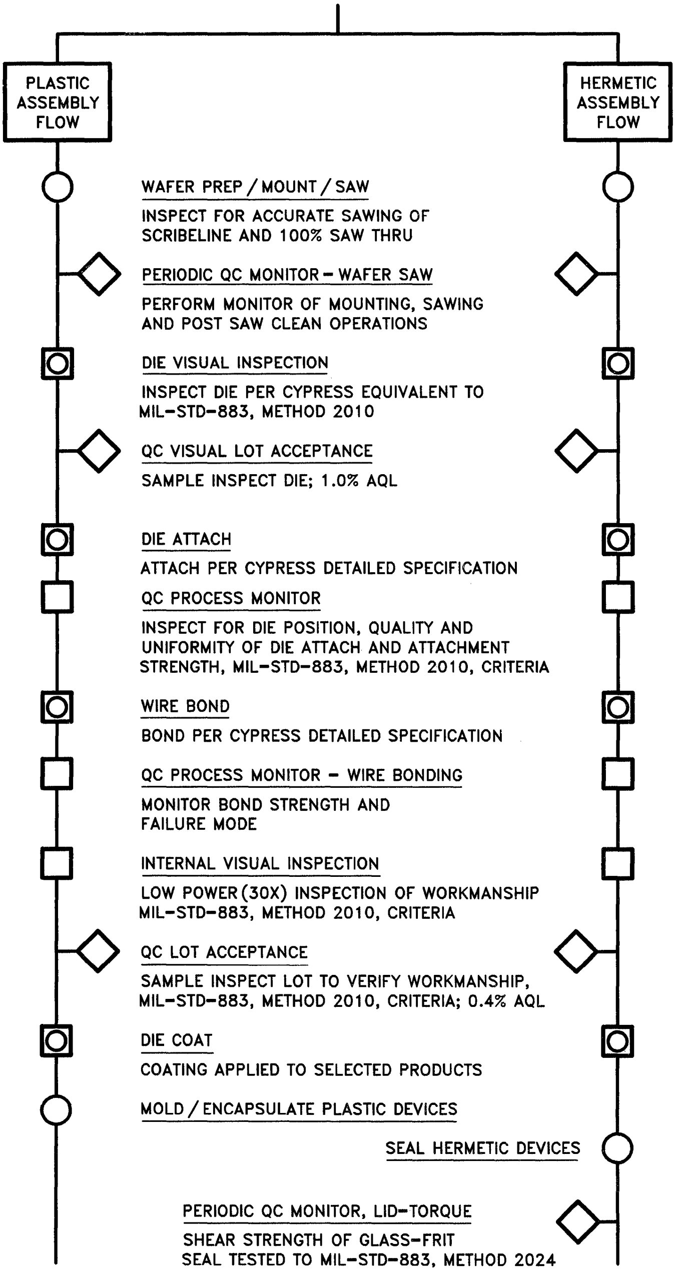
AREA	PROCESS	▼	PROCESS DETAILS
QC	INCOMING MATERIALS INSPECTION	☐	ALL INCOMING MATERIALS ARE INSPECTED TO DOCUMENTED PROCEDURES COVERING THE HANDLING, INSPECTION, STORAGE, AND RELEASE OF RAW MATERIALS USED IN THE MANUFACTURE OF CYPRESS PRODUCTS. MATERIALS INSPECTED ARE: WAFERS, MASKS, LEADFRAMES, CERAMIC PACKAGES AND/OR PIECE PARTS, MOLDING COMPOUNDS, GASES, CHEMICALS, ETC.
FAB	DIFFUSION / ION IMPLANTATION	⊡	SHEET RESISTANCE, IMPLANT DOSE, SPECIES AND CV CHARACTERISTICS ARE MEASURED FOR ALL CRITICAL IMPLANTS AND ON EVERY PRODUCT RUN. TEST WAFERS MAY BE USED TO COLLECT THIS DATA INSTEAD OF ACTUAL PRODUCTION WAFERS. IF THIS IS DONE, THEY ARE PROCESSED WITH THE STANDARD PRODUCT PRIOR TO COLLECTING SPECIFIC DATA. THIS ASSURES ACCURATE CORRELATION BETWEEN THE ACTUAL PRODUCT AND THE WAFERS USED TO MONITOR IMPLANTATION.
FAB	OXIDATION	⊡	SAMPLE WAFERS AND SAMPLE SITES ARE INSPECTED ON EACH RUN FROM VARIOUS POSITIONS OF THE FURNACE LOAD TO INSPECT FOR OXIDE THICKNESS. AUTOMATED EQUIPMENT IS USED TO MONITOR PIN HOLE COUNTS FOR VARIOUS OXIDATIONS IN THE PROCESS. IN ADDITION, AN APPEARANCE INSPECTION IS PERFORMED BY THE OPERATOR TO FURTHER MONITOR THE OXIDATION PROCESS.
FAB	PHOTOLITHOGRAPHY / ETCHING	⊡	APPEARANCE OF RESIST IS CHECKED BY THE OPERATOR AFTER THE SPIN OPERATION. ALSO, AFTER THE FILM IS DEVELOPED, BOTH DIMENSIONS AND APPEARANCE ARE CHECKED BY THE OPERATOR ON A SAMPLE OF WAFERS AND LOCATIONS UPON EACH WAFER. FINAL CD'S AND ALIGNMENT ARE ALSO SAMPLE INSPECTED ON SEVERAL WAFERS AND SITES ON EACH WAFER ON EVERY PRODUCT RUN.
FAB	METALIZATION	⊡	FILM THICKNESS IS MONITORED ON EVERY RUN. STEP COVERAGE CROSS-SECTIONS ARE PERFORMED ON A PERIODIC BASIS TO INSURE COVERAGE.
FAB	PASSIVATION	⊡	AN OUTGOING VISUAL INSPECTION IS PERFORMED ON 100% OF THE WAFERS IN A LOT TO INSPECT FOR SCRATCHES, PARTICLES, BUBBLES, ETC. FILM THICKNESS IS VERIFIED ON A SAMPLE OF WAFERS AND LOCATIONS WITHIN EACH GIVEN WAFER ON EACH RUN. PINHOLES ARE MONITORED ON A SAMPLE BASIS WEEKLY.
FAB	QC VISUAL OF WAFERS	◇	
FAB	E-TEST	☐	SAMPLE ELECTRICAL TEST IS PERFORMED FOR FINAL PROCESS ELECTRICAL CHARACTERISITICS ON EVERY RUN.
FAB	QC MONITOR OF E-TEST DATA	☐	WEEKLY REVIEW OF ALL DATA TRENDS; RUNNING AVERAGES, MINIMUMS, MAXIMUMS, ETC. ARE REVIEWED WITH PROCESS CONTROL MANAGER
TEST	WAFER PROBE / SORT	☐	VERIFY FUNCTIONALITY, ELECTRICAL CHARACTERISTICS, STRESS TEST DEVICES
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	◇	PASS / FAIL LOT BASED ON YIELD, CORRECT PROBE PLACEMENT

TO ASSEMBLY AND TEST

0032-1

(Continued)

Product Quality Assurance Flow (Continued)



WAFER PREP / MOUNT / SAW

INSPECT FOR ACCURATE SAWING OF SCRIBELINE AND 100% SAW THRU

PERIODIC QC MONITOR – WAFER SAW

PERFORM MONITOR OF MOUNTING, SAWING AND POST SAW CLEAN OPERATIONS

DIE VISUAL INSPECTION

INSPECT DIE PER CYPRESS EQUIVALENT TO MIL-STD-883, METHOD 2010

QC VISUAL LOT ACCEPTANCE

SAMPLE INSPECT DIE; 1.0% AQL

DIE ATTACH

ATTACH PER CYPRESS DETAILED SPECIFICATION

QC PROCESS MONITOR

INSPECT FOR DIE POSITION, QUALITY AND UNIFORMITY OF DIE ATTACH AND ATTACHMENT STRENGTH, MIL-STD-883, METHOD 2010, CRITERIA

WIRE BOND

BOND PER CYPRESS DETAILED SPECIFICATION

QC PROCESS MONITOR – WIRE BONDING

MONITOR BOND STRENGTH AND FAILURE MODE

INTERNAL VISUAL INSPECTION

LOW POWER (30X) INSPECTION OF WORKMANSHIP MIL-STD-883, METHOD 2010, CRITERIA

QC LOT ACCEPTANCE

SAMPLE INSPECT LOT TO VERIFY WORKMANSHIP, MIL-STD-883, METHOD 2010, CRITERIA; 0.4% AQL

DIE COAT

COATING APPLIED TO SELECTED PRODUCTS

MOLD / ENCAPSULATE PLASTIC DEVICES

SEAL HERMETIC DEVICES

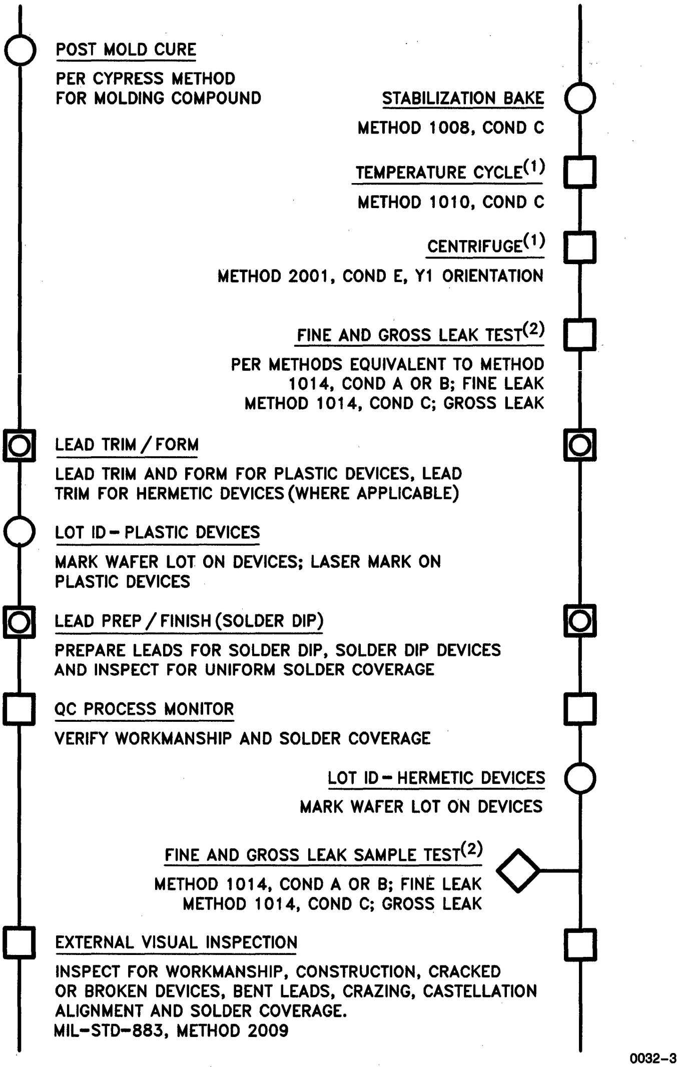
PERIODIC QC MONITOR, LID-TORQUE

SHEAR STRENGTH OF GLASS-FRIT SEAL TESTED TO MIL-STD-883, METHOD 2024

0032-2

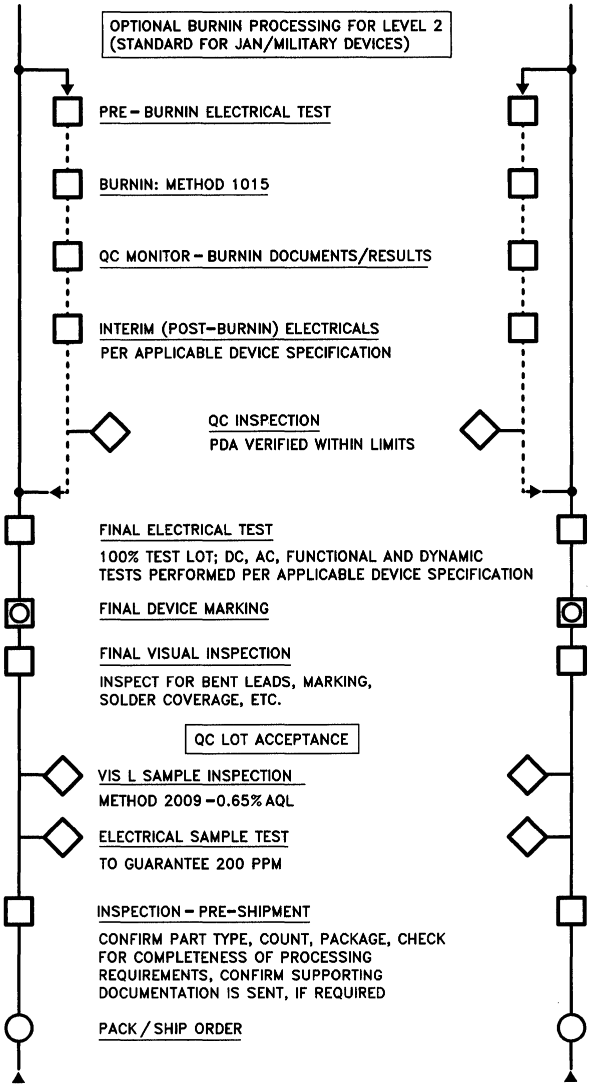
(Continued)

Product Quality Assurance Flow (Continued)


POST MOLD CURE
PER CYPRESS METHOD FOR MOLDING COMPOUND
STABILIZATION BAKE
METHOD 1008, COND C
TEMPERATURE CYCLE(1)
METHOD 1010, COND C
CENTRIFUGE(1)
METHOD 2001, COND E, Y1 ORIENTATION
FINE AND GROSS LEAK TEST(2)
PER METHODS EQUIVALENT TO METHOD 1014, COND A OR B; FINE LEAK METHOD 1014, COND C; GROSS LEAK
LEAD TRIM / FORM
LEAD TRIM AND FORM FOR PLASTIC DEVICES, LEAD TRIM FOR HERMETIC DEVICES (WHERE APPLICABLE)
LOT ID - PLASTIC DEVICES
MARK WAFER LOT ON DEVICES; LASER MARK ON PLASTIC DEVICES
LEAD PREP / FINISH (SOLDER DIP)
PREPARE LEADS FOR SOLDER DIP, SOLDER DIP DEVICES AND INSPECT FOR UNIFORM SOLDER COVERAGE
QC PROCESS MONITOR
VERIFY WORKMANSHIP AND SOLDER COVERAGE
LOT ID - HERMETIC DEVICES
MARK WAFER LOT ON DEVICES
FINE AND GROSS LEAK SAMPLE TEST(2)
METHOD 1014, COND A OR B; FINE LEAK METHOD 1014, COND C; GROSS LEAK
EXTERNAL VISUAL INSPECTION
INSPECT FOR WORKMANSHIP, CONSTRUCTION, CRACKED OR BROKEN DEVICES, BENT LEADS, CRAZING, CASTELLATION ALIGNMENT AND SOLDER COVERAGE. MIL-STD-883, METHOD 2009
0032-3

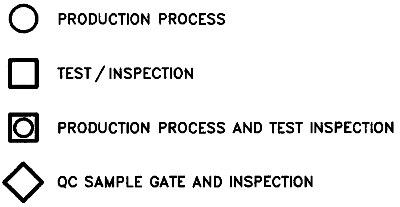
(Continued)

Product Quality Assurance Flow (Continued)


OPTIONAL BURNIN PROCESSING FOR LEVEL 2
(STANDARD FOR JAN/MILITARY DEVICES)
PRE-BURNIN ELECTRICAL TEST
BURNIN: METHOD 1015
QC MONITOR-BURNIN DOCUMENTS/RESULTS
INTERIM (POST-BURNIN) ELECTRICALS
PER APPLICABLE DEVICE SPECIFICATION
QC INSPECTION
PDA VERIFIED WITHIN LIMITS
FINAL ELECTRICAL TEST
100% TEST LOT; DC, AC, FUNCTIONAL AND DYNAMIC
TESTS PERFORMED PER APPLICABLE DEVICE SPECIFICATION
FINAL DEVICE MARKING
FINAL VISUAL INSPECTION
INSPECT FOR BENT LEADS, MARKING,
SOLDER COVERAGE, ETC.
QC LOT ACCEPTANCE
VIS L SAMPLE INSPECTION
METHOD 2009-0.65% AQL
ELECTRICAL SAMPLE TEST
TO GUARANTEE 200 PPM
INSPECTION-PRE-SHIPMENT
CONFIRM PART TYPE, COUNT, PACKAGE, CHECK
FOR COMPLETENESS OF PROCESSING
REQUIREMENTS, CONFIRM SUPPORTING
DOCUMENTATION IS SENT, IF REQUIRED
PACK/SHIP ORDER

0032-4

Key


PRODUCTION PROCESS
TEST/INSPECTION
PRODUCTION PROCESS AND TEST INSPECTION
QC SAMPLE GATE AND INSPECTION

0032-5

Notes:

1. Temp Cycle and Centrifuge performed per Applicable Product Screening Flow.
2. JAN/SMD/Military grade products are 100% Fine and Gross Leak tested and sample tested after wafer lot I.D. Commercial grade devices received sample test only. Sample size is per Commercial Product Screening Flow.

Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008 which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program is designed to monitor key products within each generic process family. This procedure requires that detailed failure analysis be performed on all test rejects and the corrective actions be taken as indicated by the analysis. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Reliability Monitor Program Sampling Plan

Test Description	Duration	Sample Size	Frequency[1]
Early Failure Rate (EFR) 150°C HTOL	12 Hours	125	Weekly
High Temp Steady State Life (HTSSL) 150°C HTOL with Deltas	1000 Hours	10	Monthly
Latent Failure Rate (LFR) 150°C HTOL	1000 Hours	125	Quarterly
High Temp Storage (HTS) 200°C HTS	1000 Hours	10	Monthly
Epoxy Packaged Data Retention 165°C Bake	168 Hours	55	Weekly
Hermetic Packaged Data Retention 250°C Bake	500 Hours	55	Monthly
Pressure Cooker (PCT) 121°C/100% R.H.	288 Hours	55	Weekly
Preconditioned Temperature Humidity Life (PCTH) 96 Hrs. PCT + Biased 85/85	1000 Hours	55	Every 6 Weeks
Extended Temperature Cycle (T/C) −65°C to +150°C	1000 Cycles	55	Quarterly

Note:

1) Maximum period between samples is listed. More frequent sampling may occur.

PRODUCT INFORMATION 1

STATIC RAMS 2

PROMS 3

PLDS 4

LOGIC 5

BRIDGEMOS 6

QUICKPRO 7

QUALITY AND RELIABILITY 8

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CYPRESS
SEMICONDUCTOR

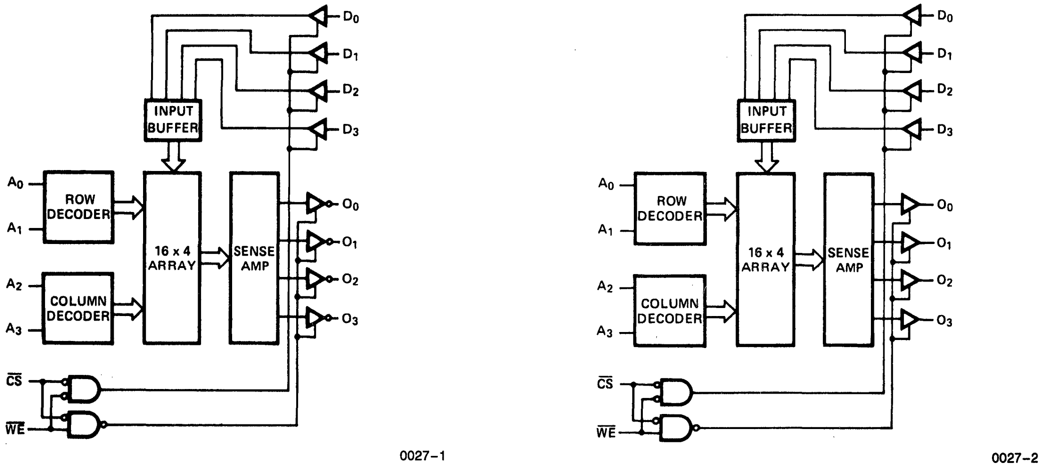
Application Briefs
RAM Input Output Characteristics

Introduction to Cypress RAMs

Cypress Semiconductor Corporation uses a speed optimized CMOS technology to manufacture high speed static RAMs which meet and exceed the performance of competitive bipolar devices while consuming significantly less power and providing superior reliability characteristics. While providing identical functionality, these devices exhibit slightly differing input and output characteristics which provide the designer opportunities to improve overall system performance. The balance of this application note describes the devices, their functionality and specifically their I/O characteristics.

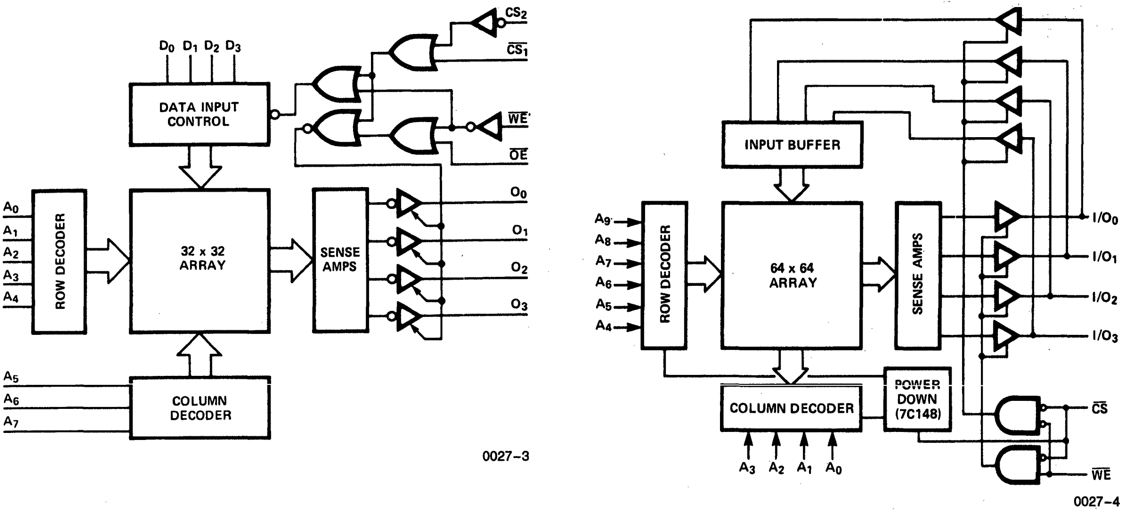
PRODUCT DESCRIPTION

The five parts in *Figure 1* constitute three basic devices of 64, 1024 and 4096 bits respectively. The 7C189 and 7C190 feature inverting and non-inverting outputs respectively in a 16 x 4 bit organization. Four address lines address the 16 words, which are written to and read from over separate input and output lines. Both of these 64 bit devices have separate active LOW select and write enable signals. The 256 x 4 7C122 is packaged in a 22 pin DIP, and features separate input and output lines, both active LOW and active HIGH select lines, eight address lines, an active LOW output enable, and an active LOW write enable. Both the


D_0
D_1
D_2
D_3
INPUT BUFFER
A_0
A_1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O_0
O_1
O_2
O_3
A_2
A_3
COLUMN DECODER
$\overline{CS}$
$\overline{WE}$
0027-1
D_0
D_1
D_2
D_3
INPUT BUFFER
A_0
A_1
ROW DECODER
16 x 4 ARRAY
SENSE AMP
O_0
O_1
O_2
O_3
A_2
A_3
COLUMN DECODER
$\overline{CS}$
$\overline{WE}$
0027-2

7C189 **7C190**

Figure 1. RAM Block Diagrams



7C122 **7C148/9**

Figure 1. RAM Block Diagrams (Continued)

7C148 and 7C149 are organized 1024 x 4 bits and feature common pins for the input and output of data. Both parts have 10 address lines, a single active LOW chip select and an active LOW write enable. The 7C148 features automatic power down whenever the device is not selected, while the 7C149 has a high speed, 15 ns, chip select for applications which do not require power control. This family of high speed static RAMs is available with access times of 15 to 45 ns with power in the 300 to 500 mW range. They are designed from a common core approach, and share the same memory cell, input structures and many other characteristics. The outputs are similar, with the exception of output drive, and the common I/O optimization for the 7C148 and 7C149. For more detailed information on these products, refer to the available data sheets.

GENERIC I/O CHARACTERISTICS

Input and output characteristics fall generally into two categories, when the area of operation falls within the normal limits of V_{CC} and V_{SS} plus or minus approximately 600 mV, and abnormal circumstances, when these limits are exceeded. Inputs under normal operating conditions are voltages that switch between logic "0" and logic "1". We will consider operation in a positive true environment and therefore a logic "1" is more positive than a logic "0". The I/O characteristics of the devices we are concerned with are what is considered to be TTL compatible. Therefore a logic "1" is 2.0V, while a logic "0" is 0.8V. The input of a device must be driven greater than 2.0V, not to exceed $V_{CC} + 0.6V$ to be considered a logic "1" and, to less than 0.8V, but not less than $V_{SS} - 0.6V$, to be considered a logic "0".

Output characteristics represent a signal that will drive the input of the next device in the system. Since the levels we are dealing with are TTL, we may assume that the V_{IL} and V_{IH} values of 0.8 and 2.0V referenced above are valid. In consideration of noise margin however, driving the input of the next stage to the required V_{IL} or V_{IH} is not sufficient. Noise margins of 200 to 400 mV are considered more than adequate, and therefore the V_{OH} we deal with is 2.4V while the V_{OL} is 0.4V, providing a noise margin of 400 mV. Since the driven node consists of both a resistive and a capacitive component, output characteristics are specified such that the output driver is capable of sinking I_{OL} at the specified V_{OL}, and capable of sourcing I_{OH} at V_{OH}. Since the values of I_{OL} and I_{OH} differ depending on the device, these values are shown in Table 1. Outputs have one other characteristic that we need to be concerned with, Output Short Circuit Current or I_{OS}. This is the maximum current that the output will source when driving a logic "1" into V_{SS}. We need to be concerned for two reasons. First, the output should be capable of supplying this current for some reasonable period of time without damage, and second, this is the current that charges the capacitive load when switching the output from a "0" to a "1" and will control the output rise time.

Since memories such as these are often tied together, we are also concerned about the output characteristics of the devices when they are deselected. All of the devices in this family feature three state outputs such that in addition to their active conditions when selected, when deselected, the outputs are in a high impedance condition which does not source or sink any current. In this condition, as long as the input is driven in its normal operating mode, it appears as an open, with less than 10 μA of leakage. Thus to any other device driving this node, it is non-existent.

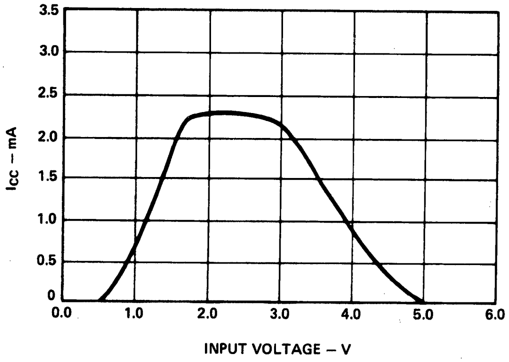
TECHNOLOGY DEPENDENCIES AND BENEFITS

Some of the products in this application note were originally produced in a BIPOLAR technology, some have since been re-engineered in NMOS technology and Cypress has now produced them in a speed optimized CMOS technology. There are both technology dependencies and benefits relative to the design of input and output structures that are associated with each technology. The designer who uses these products should be knowledgeable of these characteristics and how they can benefit or impede a design effort. One of the most obvious is that both NMOS and CMOS device inputs are high impedance, with less than 10 μA of input leakage. Bipolar devices, however, require that the driver of an input sink current when driving to V_{IL}, but appear as high impedance at V_{IH} levels. This is due to the fact that the input of a bipolar device is the emitter of a bipolar NPN type device with its base biased positive. The bias is what establishes the point at which the input changes from requiring current to be sourced to high impedance and is 1.5V. This switching level is the reason that AC measurements are done at the 1.5V level. Although NMOS and CMOS device inputs do not change from low to high impedance, great care is taken to balance their switching threshold at 1.5V. To a system designer this allows fanout to consider only capacitive loading with MOS devices while bipolar has both a capacitive and DC component. The other input characteristic which differs from bipolar to MOS is the clamp diode structure. This structure exists in both MOS and bipolar, however in MOS that uses BIAS GENERATOR techniques, all high speed MOS devices, the diode does not become forward biased until the input goes more negative than the substrate bias generator plus one diode drop. Since the bias generator is usually about −3V this has the effect of removing the clamping effect.

I/O Parameters

CMOS/NMOS/BIPOLAR INPUT CHARACTERISTICS

Although NMOS, CMOS and BIPOLAR technologies differ widely, the I/O characteristics tend to fall into two areas. The traditional characteristics are the TTL derivatives that have been covered above, and are documented in Table 1. With the exception of the differences in input impedance between MOS and BIPOLAR devices all three technologies are used to produce TTL compatible products. The second camp is the true CMOS interface where signals swing from V_{SS} to V_{CC}. These interface specifications define a "1" as greater than $V_{CC} - 1.5V$ and a "0" as less than $V_{SS} + 1.5V$. In addition, loads are primarily capacitive. Only devices produced in a CMOS technology are capable of behaving in this manner. CMOS devices can, however, handle both TTL and CMOS inputs. Devices such as the ones described in this application note have input characteristics depicted in *Figure 2.*



0027-5

Figure 2. Input Voltage vs. Current

Table 1. DC Parameters

Parameters	Description	Test Conditions	7C122		7C148/9		7C189/90		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	V_{CC} = Min., $I_{OH} = -5.2$ mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., $I_{OL} = 8.0$ mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.1	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IL}	Input Low Current	V_{CC} = Max., $V_{IN} = V_{SS}$		10		10		10	μA
I_{IH}	Input High Current	V_{CC} = Max., $V_{IN} = V_{CC}$		10		10		10	μA
I_{OFF}	Output Current (High Z)	$V_{OL} < V_{OUT} < V_{OH}$, T_A = Max.	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., 0°C < T_A < 70°C		−70		−90		−275	mA
		$V_{OUT} = V_{SS}$, −55°C < T_A < 125°C		−80		−90		−350	mA

When operated in the TTL range, they perform normally. Operated in full CMOS mode, an additional benefit of power savings is realized as the current consumed in the input converter decreases as the input voltage rises above 3.0V, or falls below 1.5V. Since the input signal is in the 1.5 to 3.0V range only when transitioning between logic states, the power savings in a large array with true CMOS inputs can be significant. With input signals on over half of the pins of a device, significant savings in a large system can be realized by using CMOS input voltage swings even in TTL systems.

Switching Characteristics

Although this application note does not directly deal with the AC characteristics of high speed RAMs, the input and output characteristics of these devices have a great deal to do with the actual AC specifications. Conventionally, all AC measurements associated with high speed devices are done at 1.5V and assume a maximum rise and fall time. This eliminates the variations associated with the various configurations that the device will be used in (as a figure of merit when testing the device) but, does not mean that the designer can ignore these influences when designing a system. Maximum rise and fall time is usually found in the notes included on every data sheet. For the products referred to in this application note, a 10 ns maximum rise and fall time is specified for all devices with access times equal to or greater than 25 ns and a 5 ns maximum rise and fall time for all devices with access times less than 25 ns. The AC load and its Thévenin equivalent in *Figure 3* represent the resistive and capacitive components of load which the devices are specified to drive. With either of these loads, the device will be required to source or sink its rated output current at its specified output voltage. The capacitance stresses the ability of the device output to source or sink sufficient current to slew the outputs at a high enough rate to meet the AC specifications. The high impedance load is a convenience to testing when trying to determine how rapidly the output enters a high impedance condition. Once the output enters a high impedance mode, the resistive divider will charge the capacitance until equilibrium is reached. Allowing for noise margin, testing for a 500 mV change is normal. By using a smaller capacitance than normal, the change will occur more quickly, allowing a more accurate determination of entry into the high impedance state.

SWITCHING THRESHOLD VARIATIONS

Switching threshold variations along with input rise and fall times can have an effect on the performance of any device. Input rise and fall times are under the control of the designer, and are primarily affected by capacitive loading, the driver and bus termination techniques. Switching threshold is affected by process variations, changes in V_{CC} and temperature. Compensation of these variables is the territory of the manufacturer, both at the design stage and the manufacturing of the device. Combined threshold shifts over full military temperature ranges and process variations average less than 100 mV. This translates directly to V_{IL} and V_{IH} variations which track well within the noise margins of normal system design particularly since the V_{OL} and V_{OH} changes track to the same 100 mV.

Input Protection Mechanisms

THE ELECTROSTATIC DISCHARGE PHENOMENON

Because of their extremely high input impedance and relatively low (approximately 30V) breakdown voltage, MOS devices have always suffered from destruction caused by ESD (Electro Static Discharge). This has caused two actions. First, major efforts to design input protection circuits without impeding performance has resulted in MOS devices that are now superior to bipolar devices. Second, care in handling semiconductors is now common practice. Interestingly enough, bipolar products that once did not suffer from ESD have now suddenly become sensitive to the phenomenon, primarily because new processing technology involving shallow junctions is in itself sensitive. MOS devices are in many cases now superior to bipolar products. A sampling of competitive BIPOLAR and NMOS 64 bit, 1K bit and 4K bit products reveals breakdown voltages as low as ±150V to greater than ±2001V magnitudes. The circuit in *Figure 4* is used to protect Cypress products against ESD. It consists of two thick oxide field transistors wrapped around an input resistor and a thin oxide device

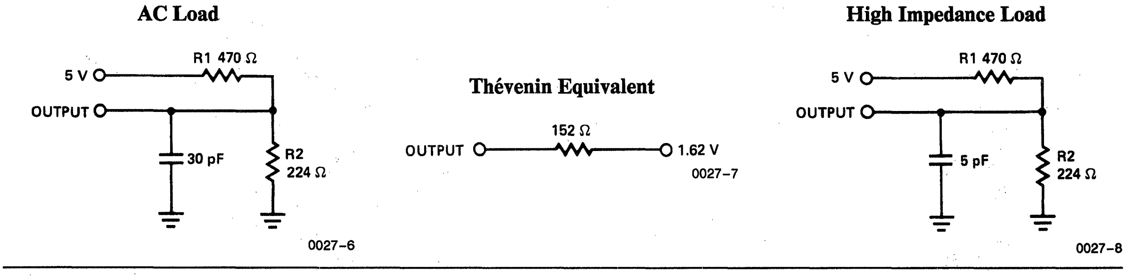
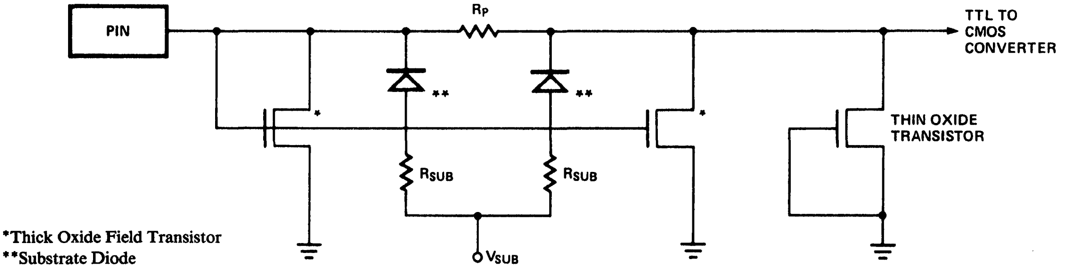


Figure 3. Test Loads


PIN
RP
TTL TO CMOS CONVERTER
**
**
*
*
THIN OXIDE TRANSISTOR
RSUB
RSUB
VSUB
0027-9

*Thick Oxide Field Transistor
**Substrate Diode

Figure 4. Input Protection Circuit

with a relatively low breakdown voltage of approximately 12V. Large input voltages cause the field transistors to turn on discharging the ESD current harmlessly to ground. The thin oxide transistor breaks down when the voltage across it exceeds the 12V level and it is protected from destruction by the current limiting of R_P. The combination of these two structures provides ESD protection greater than 2250V, the limit of the testing equipment available. In addition, repeated applications of this stress do not cause a degradation that could lead to eventual device failure as observed in functionally equivalent devices.

CMOS Latchup

The parasitic bipolar transistors shown in *Figure 5* result in a built-in silicon controlled rectifier illustrated in *Figure 6*. Under normal circumstances the substrate resistor R_{SUB} is connected to ground. Therefore, whenever the signal on the pin goes below ground by one diode drop, current flows from ground through R_{SUB} forward biasing the lower transistor in the effective SCR. If this current is sufficient to turn on the transistor, the upper PNP transistor is forward biased, the SCR turns on and normally destroys the device. Several solutions are obvious, decreasing the substrate resistance, or adding a substrate bias generator are two. The bias generator technique has several additional benefits, however, such as threshold voltage control which increases device performance and is employed in all Cypress products, along with guard rings which effectively isolate input and output structures from the core of the device and thus effectively decrease the substrate resistance by short circuiting the current paths. Latchup can potentially be induced at either the inputs or outputs. In true CMOS output structures as discussed above, the output driver has a PMOS pullup which creates additional vertical bipolar PNP transistors compounding the latchup problem. Additonal isolation using the guard ring technique can be used to solve this problem, at the expense of additional silicon

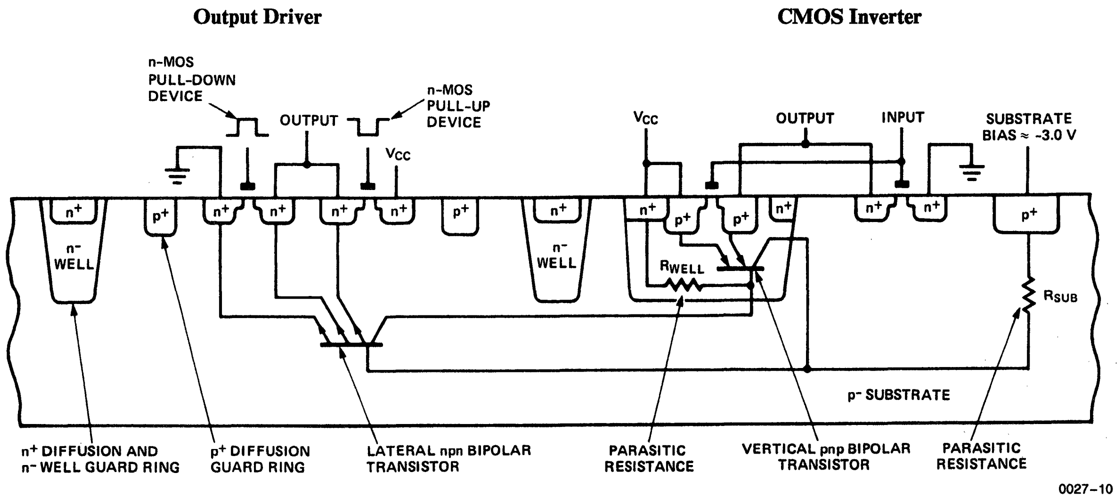

Output Driver
CMOS Inverter
n-MOS PULL-DOWN DEVICE
OUTPUT
n-MOS PULL-UP DEVICE
VCC
VCC
OUTPUT
INPUT
SUBSTRATE BIAS ≈ -3.0 V
n+
n- WELL
p+
n+
n+
n+
n+
p+
n+
n- WELL
n+
p+
p+
n+
n+
n+
p+
RWELL
RSUB
p- SUBSTRATE
n+ DIFFUSION AND n- WELL GUARD RING
p+ DIFFUSION GUARD RING
LATERAL npn BIPOLAR TRANSISTOR
PARASITIC RESISTANCE
VERTICAL pnp BIPOLAR TRANSISTOR
PARASITIC RESISTANCE
0027-10

Figure 5. CMOS Cross Section and Parasitic Circuits

Substrate Bias Generator

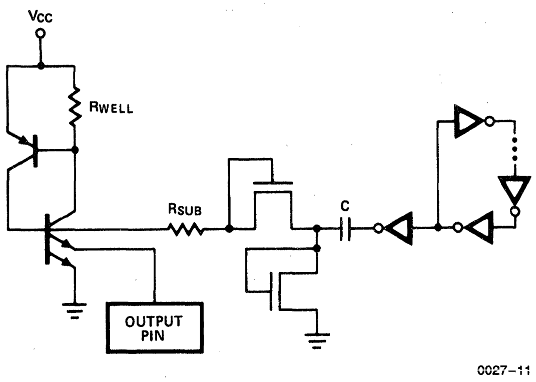


Figure 6. Parasitic SCR and Bias Generator

area. Since all of the devices of concern here require TTL outputs, the problem is totally eliminated through the use of an NMOS pullup.

LATCHUP CHARACTERISTICS

Inducing Latchup for Testing Purposes

Care needs to be exercised in testing for latchup since it is normally a destructive phenomena. The normal method is to power the device under test with a supply that can be current limited, such that when latchup is induced, insufficient current exists to destroy the device. Once this setup exists, driving the inputs or outputs with a current, and measuring the point at which the power supply collapses will allow non-destructive measurement of the latchup characteristics of the devices under question. In actual testing, with the device under power, individual inputs and outputs are driven positive and negative with a voltage and the current measured at which the device latches up. This provides the DC latchup data for each pin on the device as a function of trigger current.

Measurement of Latchup Susceptibility

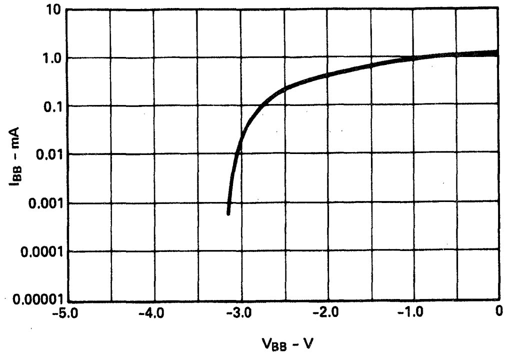
Actually measuring the latchup characteristics of devices should encompass ranges of reasonable positive and negative currents for trigger sources. Depending on the device, latchup can occur as low as a few mA to as high as several hundred mA of sink or source current. Devices which latch at trigger currents of less than 20 to 30 mA are in danger of encountering system conditions that will cause latchup failure.

Competitive Devices

Although there are few devices directly competitive with the Cypress devices covered in this application note, the latchup characteristics of the closest functionally similar devices were measured. The results show devices that latchup at as low as 10 mA all the way to devices that can sustain greater than 100 mA of trigger current without latchup. The Cypress devices covered in this document can sustain greater than 200 mA without incurring latchup, far more than is possible to encounter in any reasonable system environment.

Elimination of Latchup in Cypress RAMs

Since the latchup characteristic is one that inherently exists in any CMOS device, rather than change the laws of physics, we design to minimize its effects over the operating environment that the device must endure. These include temperature, power supply and signal levels as well as process variations. There are several techniques employed to eliminate the latchup phenomenon. Two of them involve moving the trigger threshold outside the operating range as to make it impossible to ever encounter it. These are either using low impedance, epitaxial, substrates and/or a substrate bias generator. The use of a low impedance substrate has the effect of increasing the undershoot voltage required to generate the required trigger current that causes latchup. A substrate bias generator has two effects which help to eliminate latchup. First, by biasing the substrate at a negative, −3.0V, voltage, the parasitic diodes can not be forward biased unless the undershoot exceeds the −3V by at least one diode drop. Second, if undershoot is this severe, the impedance of the bias generator itself is sufficient to deter sufficent trigger from being generated. The bias generator has one additional noticeable characteristic, it effectively removes the input clamp diode. This is due to the anode of the diode connecting to the substrate which is at −3.0V. Therefore, even though the diode exists as shown in *Figure 4*, DC signals of −3.0V do not forward bias the diode and exhibit the clamp condition. The benefits of this are apparent in higher noise tolerance as substrate currents due to input undershoot do not occur.



0027-12

Figure 7. Bias Generator Characteristics

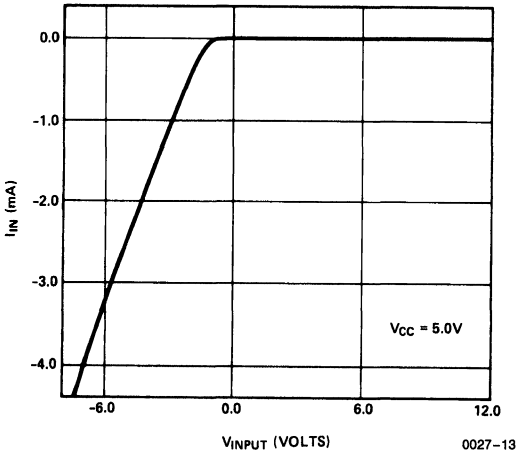
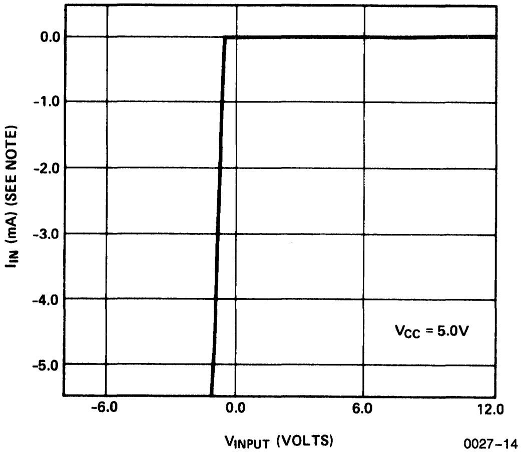


Figure 8. Input V/I Characteristics



Note: Output is in a High Impedance Condition.

Figure 9. Output V/I Characteristics

Figures 8 and *9* represent the voltage and current characteristics of the devices discussed in this application brief. *Figure 8* is characteristic of an input pin, and *Figure 9* an output pin in a high impedance state. In *Figure 8*, the input covers +12V to −6V, well outside the +7V to −3V specification. Referring to *Figure 4* to understand these characteristics, when the input voltage goes negative, the thin oxide transistor acts as a forward biased diode and the slope of the curve is set by the value of R_P. As the input voltage goes positive, only leakage current flows. The output characteristics in *Figure 9* show the same phenomenon, with the exception that, since this is not an input, no protection circuit exists, and therefore no R_P exists. An equivalent thin film device acts as a clamp diode which limits the output voltage to approximately −1V at −5 mA.

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74F189 Application Brief

Introduction

There are available in the market a number of high speed 64 bit static RAMs organized 16 by 4 bits. Because of the various different manufacturers specifications, there is no apparent true second source for these products as each operates with some unique characteristics. The composite specifications contained in this applications brief will allow the interchangeable use of the Cypress CY7C189 with the 74F189 and the Cypress CY7C190 with the 74F219 with optimization for either power or performance.

Specifications

Depending on system requirements, the SPEED OPTIMIZED specification will allow the designer to select performance at the expense of power, and use either Cypress's CY7C189-15 or the 74F189 interchangeably. If, however, the major criteria is power the designer can achieve a 55 mA max power specification using the Cypress CY7C189-25 interchangeably with the 74F189 by designing with the POWER OPTIMIZED specification.

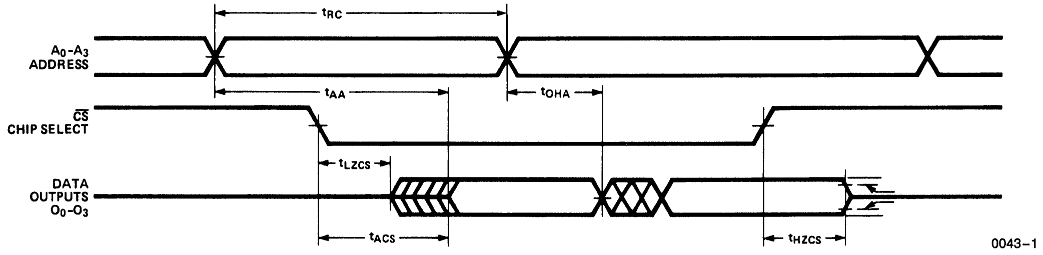
Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		Speed Optimized		Power Optimized		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.5		0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		−600	+20	−600	+20	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$		−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−150		−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		55	mA
			Military				70	mA

Switching Characteristics Over the Operating Range

Parameters	Description	Speed Optimized		Power Optimized		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	27		27		ns
t_{ACS}	Chip Select to Output Valid		14		15	ns
t_{HZCS}	Chip Select Inactive to High Z		12		15	ns
t_{LZCS}	Chip Select Active to Low Z		12		15	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{AA}	Address Access Time		27		27	ns
WRITE CYCLE						
t_{WC}	Write Cycle Time	15		20		ns
t_{HZWE}	Write Enable Active to High Z		14		20	ns
t_{LZWE}	Write Enable Inactive to Low Z		12		20	
t_{AWE}	Write Enable to Output Valid		29		29	ns
t_{PWE}	Write Enable Pulse Width	15		20		ns
t_{SD}	Data Setup to Write End	15		20		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{HCS}	Chip Select Hold from Write End	6		6		ns

Read Cycle



t_{RC}
A_0-A_3 ADDRESS
t_{AA}
t_{OHA}
$\overline{CS}$ CHIP SELECT
t_{LZCS}
DATA OUTPUTS O_0-O_3
t_{ACS}
t_{HZCS}

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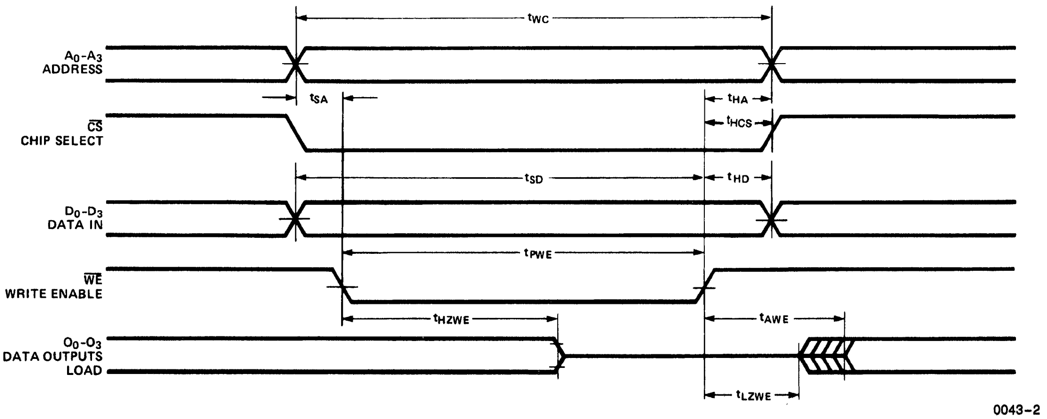
Write Cycle



t_{WC}
A_0-A_3 ADDRESS
t_{SA}
t_{HA}
$\overline{CS}$ CHIP SELECT
t_{HCS}
t_{SD}
t_{HD}
D_0-D_3 DATA IN
t_{PWE}
$\overline{WE}$ WRITE ENABLE
t_{HZWE}
t_{AWE}
O_0-O_3 DATA OUTPUTS LOAD
t_{LZWE}

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Programmable Logic Device Application Brief

Scope and Purpose

The purpose of this application brief is to provide the reader with a basic understanding of Cypress CMOS Programmable Logic Devices. This includes a description of their architecture and design, the technology used in their fabrication, how they are programmed and a discussion of their reliability.

This document will tell the reader how state-of-the-art CMOS technology and a unique architecture have been incorporated in a family of PLD integrated circuits that are functionally equivalent, pin compatible, and superior in performance to their bipolar counterparts.

The appendix discusses and illustrates the design techniques that Cypress uses on all products to eliminate latchup and improve ESD (Electro-Static-Discharge) protection.

Introduction

The PLD is a Programmable Logic Device. The basic (functional) logic structure of a PLD is programmable AND array whose outputs feed into a fixed OR array. The pertinent parameters are the number of inputs, the number of outputs, the width (number of factors) in the AND array and the width (number of terms) in the OR array. The Boolean equation implemented is the sum-of-products or minterm form.

The first PLDs were strictly combinatorial logic. They were followed by devices that added latches (D flip-flops) a clock input, and internal feedback. For the first time a programmable, sequential, state machine could be implemented in a single package. Three-state outputs, the "security fuse", flip-flop initialization, and in general terms "testability" are features that have been added for increased flexibility.

Applications

PLDs are used to replace SSI/MSI logic and "glue chips" primarily to increase packaging density. A single PLD is the functional equivalent of many SSI ICs (in the 200–500 equivalent gate range). When PLDs are used to replace standard logic gates, the resulting reduction in PC card area, although application dependent, has been found to vary between 4 to 1 and 10 to 1. i.e., One PLD will replace between four and ten 14 pin ICs. Secondary benefits to the user are reduced parts inventory, reduced power, higher reliability, faster design and turnaround time, product secrecy and equal (matched) propagation delays through the AND OR array.

Reliability

Reliability studies have shown that system reliability is inversely proportional to the number of interconnections between system elements. However, the failure rate for mature ICs is about 0.1% per thousand hours and has remained constant during the last twenty years in spite of the fact that circuit complexity (density) has increased by more than two orders of magnitude.

The conclusion is that higher levels of IC integration provide increased system reliability. Thus the user is increasing system reliability when Cypress CMOS PLDs replace glue chips.

Programming

PLDs must be programmed. This can be accomplished by either designing and building a programmer or purchasing one for $1,000 to $10,000.

Programming Bipolar PLDs

Bipolar PLDs use a fuse as the programmable element. In an unprogrammed device all of the connections are "made" during the manufacturing process and the unwanted connections are later "unmade" by blowing fuses during the programming process.

Bipolar products are programmed using 20 Volt pulses of durations from 50 microseconds to 10 milliseconds during which 100 to 300 milliamperes (mA) of current exist. In order to limit the heat generated during programming, the duty cycle for the programming pulses is limited to 20 to 30 percent. One fuse is blown at a time so that the heat generated will neither permanently damage the IC nor stress it to the point that it could fail later. Some programming algorithms take into account the physical locations of the fuses and avoid sequentially blowing fuses that are physically close to each other in order to prevent excessive localized heating of the chip. Because of the high currents required, bipolar products are not "gang" programmed, as are EPROMs.

Programming Cypress CMOS PLDs

Cypress PLDs are programmed by storing charge on the floating gate of an EPROM transistor. Charge storage is accomplished by hot carrier injection; a process that does not physically destroy material or heat the device. During programming, EPROM cells are stressed significantly less than fuses. In addition, every cell is programmed, tested and erased as part of the manufacturing process. This 100% testing guarantees a very high programming yield to the customer, which is impossible to guarantee with any fuse programmable device.

The storage mechanism is well understood. Products using it have been in volume production for more than ten years. Reliability studies have been performed by many independent organizations and all have concluded that the technology is reliable.

Cypress PLDs are programmed using high voltage pulses of durations from 100 microseconds to 10 ms, during which 50 milliamperes of programming current exist. Eight bits are programmed at the same time and, because of the lower currents required, gang programmers that can handle 10 to 20 devices in parallel are possible.

Before programming, AND gates or PRODUCT TERMS are connected via EPROM cells to both true and complement inputs. Programming an EPROM cell disconnects an input from a PRODUCT TERM. Selective programming of these cells enables a specific logic function to be implemented. PLDs are supplied in a number of functional configurations. These functional variations offer the user the choice of combinatorial as well as registered paths to implement logic functions.

CMOS Technology

Cypress PLDs are fabricated using an advanced "N-well" CMOS technology. The use of proven EPROM technology to achieve memory non-volatility, combined with novel circuit design and a unique architecture, provides the user with a superior product in terms of performance, reliability, testability and programmability.

PAL® is a registered trademark of Monolithic Memories, Inc.

Functional Description

General

The variations of PLD functions available are listed in Table 1. The 16L8, which is used as an example (*see Figure 2*), is purely combinatorial and consists of eight groups of 7-input AND gates, each of which can have up to 32 inputs. One of the AND gates of each group (of 8) is used to enable the (inverting) output driver, so that 7 AND gates (each of which may have 32 inputs) each feed one OR gate, whose output is inverted.

The 16R8 is similar to the 16L8, except that the outputs are latched using D flip-flops (with a common clock), the inputs to the 8 OR gates are the outputs of 8 AND gates; the three-state output drivers are enabled by a common enable input.

The reader should refer to the PLD data sheets for a more detailed description of the other members of the family. The 16R4, 16R6 and 16R8 have 4, 6, or 8 registered outputs with feedback.

The 22V10 offers a unique macro-cell flexibility to allow any combination of up to 10 combinatorial or registered outputs. In a similar manner the 20G10 uses macro-cells to allow the user to program the functionality of the 10 most popular PAL® 24 devices.

Register Preload

The preload function is used to load data into the internal register (of registered devices) for testing purposes. This significantly simplifies and shortens the testing procedure. Loading is accomplished by applying a supervoltage pulse of at least 100 microseconds duration to pin 5 as a write pulse while pin 11 is held at VIH and data is applied to pins 12 through 19.

Security Function

The security function prevents the contents of the regular array from being electrically verified. This enables the user to safeguard proprietary logic. The EPROM technology prevents the state of the cell from being visually ascertained. The security function is implemented by programming an EPROM cell that disconnects the lines that are used to verify the array. This cell has been designed to retain its charge longer than any of the other cells in the array.

Commercial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} mA		t_{PD} ns		t_S ns		t_{CO} ns	
				L	STD	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								
20G10	(10) 8-wide AND-OR-Invert with MACRO	Programmable or Dedicated	Programmable Bidirectional or Registered	—	55	25	35	15	30	15	25
22V10	(10) variable AND-OR-Invert with MACRO	Programmable	Programmable Bidirectional or Registered	55	90	25	35	15	30	15	25

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	V_{CC} mA	t_{PD} ns				t_S ns				t_{CO} ns			
					-20	-25	-30	-40	-20	-25	-30	-40	-20	-25	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	NA	30	40	—	NA	—	—	—	NA	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	NA	—	—	20	NA	25	35	15	NA	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	NA	30	40	20	NA	25	35	15	NA	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional													
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	NA	30	40	20	NA	25	35	15	NA	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional													
20G10	(10) 8-wide AND-OR-Invert with MACRO	Programmable	Programmable Bidirectional or Registered	80	NA	—	30	40	NA	—	25	35	NA	—	20	25
22V10	(10) variable AND-OR-Invert with MACRO	Programmable	Programmable Bidirectional or Registered	100	NA	25	30	40	NA	20	25	35	NA	20	20	25

Table 1. PLD Selection Guide

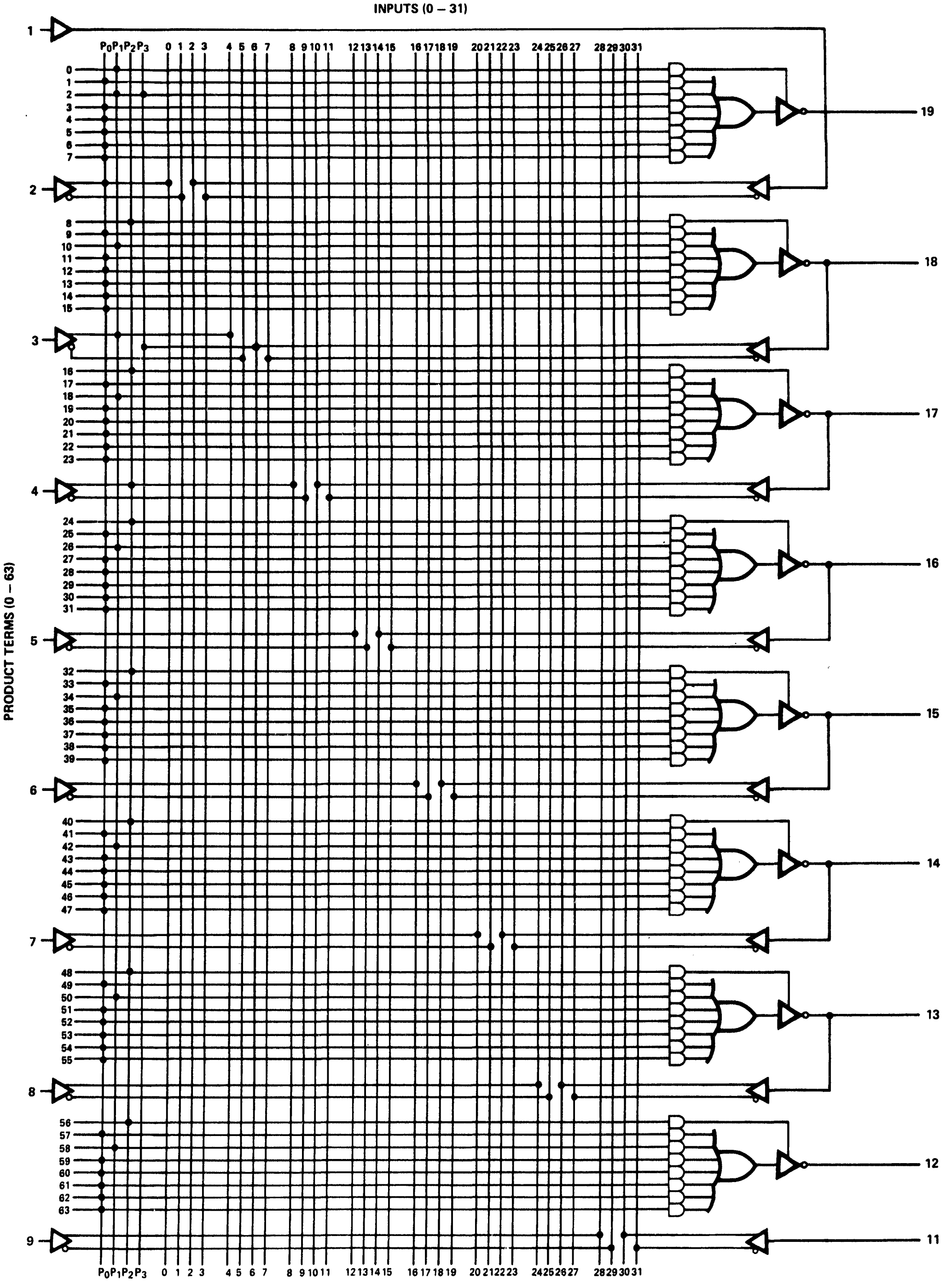

INPUTS (0 – 31)
PRODUCT TERMS (0 – 63)
P0P1P2P3 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
0049-2

Figure 2. Functional Logic Diagram PAL C 16L8A

There are 2048 EPROM cells in the PAL C 20 array that are used to specify up to 32 inputs for 8 groups of 7-input AND OR gates and 8 32-input AND output enable gates. In normal usage, a maximum of 16 inputs would be connected to any AND gate, because connecting both a true and a complement input of the same signal to the input of an AND gate will result in a constant LOW output.

Phantom Array

There are an additional 256 bits in a phantom array that are used to test the PAL C 20 device functionally and to verify dynamic (AC) operation without using the regular array after the device is packaged. The phantom array is programmed and verified as part of the final electrical test procedure during the manufacturing process. It may be used by the customer as part of an incoming inspection and could be used to verify programmability as well as functionality. Three input pins are used to verify operation of the phantom array. One (pin 2) has a worst case (longest physical length) propagation delay path through the regular array.

Programming the Arrays

The phantom array is programmed in the same manner as the regular array. Both are addressed as byte arrays for programming. The normal array has 256 bytes to program and the phantom array has 32 bytes. The customer may test the programmed phantom array functionally and dynamically as part of an incoming inspection.

Programming the EPROM Cell

A schematic of the two-transistor EPROM cell used in all PLDs is illustrated in *Figure 1.* Conventional EPROMS use one transistor per cell and its design is a compromise between being able to program (write) rapidly and read. Cypress uses a two-transistor cell that enables the PLDs to achieve superior performance by optimizing the read transistor, R, and program transistor, P, for their respective functions. The cell size is 20.4 microns by 6.7 microns. Note that the selection gates, the floating gates and the sources of both transistors are (respectively) connected together.

Operation

In the unprogrammed state, the threshold voltage of the R transistor is less than that of the P transistor.

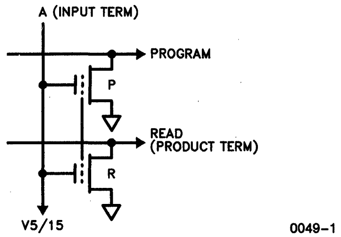


Figure 1. PLD EPROM Cell Schematic

To program the cell, the input line (A) is raised to 15 volts, which causes charge to be stored on the floating gate of the P transistor, which causes its threshold to increase by approximately 7 volts. Because the floating gates of both transistors are connected together, the threshold of the R transistor increases by the same amount.

To read from the cell, the input line (A) is raised to 5 volts. If the cell had been programmed, this voltage would not be sufficient to turn-on the read transistor. However, if the cell had not been programmed, the read transistor would turn-on. Under this condition the current through the read transistor is 150 microamperes; approximately an order of magnitude greater than that used in a conventional EPROM cell. The larger current is required in order to achieve the specified performance.

Operational Overview

The device operates in two basic modes; normal and PROGRAM. In the normal mode either the Regular array or the Phamtom array may be used, together with the data inputs, to determine the state of the outputs. In the PROGRAM mode either the Regular array or the Phantom array may be programmed using the 8 outputs (pins 12–19) as data inputs and pins 2 through 9 as address inputs.

Table 2 illustrates the various modes of operation for the PAL C 20 device. They are decoded by high-voltage-sensitive on-chip circuits. It is permitted to go from any mode to any other mode. Note that the normal data output pins (12–19) are used as data input pins for programming.

Programming

Tables 3 and 4 indicate how the regular and the phantom arrays in the PAL C 20 device are addressed. The 20G10 and 22V10 are similar. The regular array is addressed as a

256 word (8 × 32) by 8-bits per word memory. The phantom array is selected using the same addresses as columns 0, 1, 2 and 3, but with pin 7 at Vpp (per Tables 2 and 4).

In either case (normal or phantom array), the product terms are addressed in groups of 8 as shown in Table 3. There is a one-to-one correspondence between the data to be programmed and the D0–D7 inputs and the product terms, as modified modulo 8, by the address on pins 2, 3, 4 (Refer to *Figure 2*). In other words, a one on D0 corresponds to de-selecting the "product term input" at input line 0 and product term 0. A one on D1 corresponds to de-selecting the product term input at input line 0 and product term 8, etc. One method of programming the array would be to program and verify the bits corresponding to the first product term address and then increment a counter that generates the "OR" gate addresses (pins 2, 3, 4) and then program and verify the second row of Table 3, and continue this process 8 times until all 64 product terms associated with input line 0 have been programmed and verified. To select the second (1) input term, address pins 6, 7, 8 and 9 are held LOW (as before) and pin 5 = HIGH. The preceding sequence is then repeated 31 more times, incrementing pins 5 through 9 in a binary sequence, to program and verify the entire array. The other members of the family are programmed in an identical manner.

Table 2. PAL C 20 Series Operating Modes

Pin Name	V_{PP}	PGM/$\overline{OE}$	A1	A2	A3	A4	A5	D7–D0	Notes
Pin Number	(1)	(11)	(3)	(4)	(5)	(6)	(7)	(12–19)	
Operating Modes									
PAL	X	X	X	X	X	X	X	Programmed Function	3, 4
Program PAL	V_{PP}	V_{PP}	X	X	X	X	X	Data In	3, 5
Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	X	High Z	3, 5
Program Verify	V_{PP}	V_{ILP}	X	X	X	X	X	Data Out	3, 5
Phantom PAL	X	X	X	X	X	V_{PP}	X	Programmed Function	3, 6
Program Phantom PAL	V_{PP}	V_{PP}	X	X	X	X	V_{PP}	Data In	3, 7
Phantom Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	V_{PP}	High Z	3, 7
Phantom Program Verify	V_{PP}	V_{ILP}	X	X	X	X	V_{PP}	Data Out	3, 7
Program Security Bit	V_{PP}	V_{PP}	V_{PP}	X	X	X	X	High Z	3
Verify Security Bit	X	X	(Note 8)	V_{PP}	X	X	X	High Z	3
Register Preload	X	X	X	X	V_{PP}	X	X	Data In	3, 9

Notes:

1. V_{PP} = 13.5 ±0.5V, I_{PP} = 50 mA; V_{CCP} = 5 ±0.25V; V_{IHP} = 3V; V_{ILP} = 0.4V.
2. Measured at 10% and 90% points.
3. $V_{SS} < X < V_{CCP}$.
4. All "X" inputs operational per normal PAL function.
5. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address *Tables 3* and *4.*
6. All "X" inputs operational per normal PAL function except that they operate on the function that occupies the phantom array.
7. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address *Tables 3* and *4.* Pin 7 is used to select the phantom mode of operation and must be taken to V_{PP} before selecting phantom program operation with V_{PP} on Pin 1.
8. The state of Pin 3 indicates if the security function has been invoked or not. If Pin 3 = V_{OL} security is in effect, if Pin 3 = V_{OH}, the data is unsecured and may be directly accessed.
9. For testing purposes, the output latch on the 16R8, 16R6 and 16R4 may be preloaded with data from the appropriate associated output line.

Table 3. PAL C 20 Series Product Term Addresses

Product Term Addresses										
Binary Address			Line Number							
Pin Numbers										
(4)	(3)	(2)								
V_{ILP}	V_{ILP}	V_{ILP}	0	8	16	24	32	40	48	56
V_{ILP}	V_{ILP}	V_{IHP}	1	9	17	25	33	41	49	57
V_{ILP}	V_{IHP}	V_{ILP}	2	10	18	26	34	42	50	58
V_{ILP}	V_{IHP}	V_{IHP}	3	11	19	27	35	43	51	59
V_{IHP}	V_{ILP}	V_{ILP}	4	12	20	28	36	44	52	60
V_{IHP}	V_{ILP}	V_{IHP}	5	13	21	29	37	45	53	61
V_{IHP}	V_{IHP}	V_{ILP}	6	14	22	30	38	46	54	62
V_{IHP}	V_{IHP}	V_{IHP}	7	15	23	31	39	47	55	63
			D0	D1	D2	D3	D4	D5	D6	D7
			Programmed Data Input							

Table 4. PAL C 20 Series Input Term Addresses

Input Terms Numbers	Input Term Addresses				
	Binary Addresses				
	Pin Numbers				
	(9)	(8)	(7)	(6)	(5)
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
2	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
3	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
5	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
6	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
8	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
9	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
11	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
12	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
15	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
16	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
18	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
20	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
22	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
24	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
25	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
26	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
28	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
29	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
30	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
P0	V_{ILP}	V_{ILP}	V_{PP}	X	X
P1	V_{ILP}	V_{IHP}	V_{PP}	X	X
P2	V_{IHP}	V_{ILP}	V_{PP}	X	X
P3	V_{IHP}	V_{IHP}	V_{PP}	X	X

Implementation

A simplified block diagram of a 16L8 is presented in *Figure 3*. The method of programming and sensing is illustrated in *Figure 4*.

Programming Operation

Pins 5–9 are decoded (according to Table 4) in a one of 32 decoder, whose outputs correspond to the inputs labeled 0–31 of *Figure 2*. For programming, 15 volts is applied to the bottom of the input term line through a weak depletion mode device (*Figure 4*). The EN (enable) signal to all of the three-state drivers is LOW, which prevents the normal input signals from driving the input term lines during programming. The D0–D7 inputs (pins 19 through 12) drive the program transistors (0, 8, 16, 24 etc.) as selected by pins 2, 3, 4 and as listed in Table 3. To disconnect an input term line from a product term line, the P transistor is forward biased, which increases the threshold of the R transistor.

Verify Operation

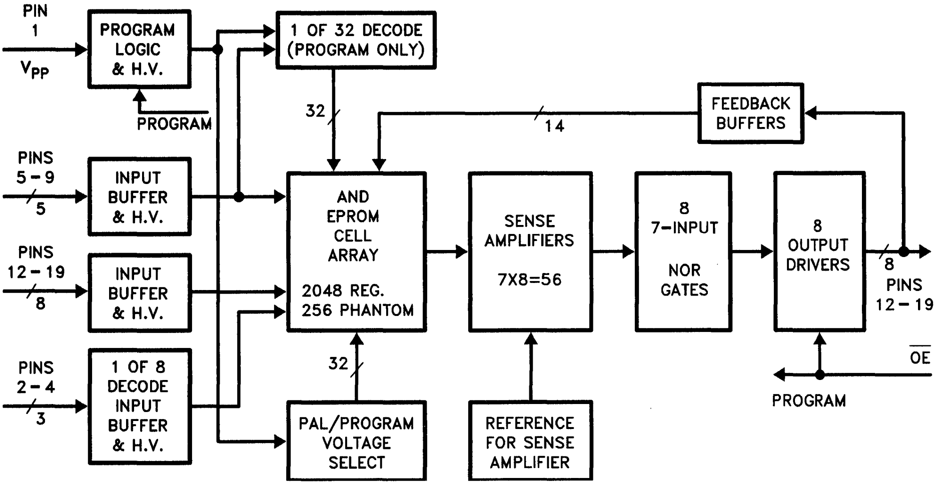
To verify the programmed cells, the device must go from the PROGRAM mode to the PROGRAM INHIBIT mode to the PROGRAM VERIFY mode. This is accomplished by reducing the voltage on pin 11 to VIHP (3V) and then to VILP (0.4V). Internal to the device (see *Figure 4*) the 1 of 32 decoder is disabled, the EN signal is LOW, and 31 of the 32 input term lines are at zero volts. The line being verified is at 5 volts. The input address lines (pins 2 through 9) do not need to change when going from program to verify.

The "ones" that were programmed cause the thresholds of the R transistors to increase, so they do not turn on during verify. Conversely, the unprogrammed transistors do turn on, so the complement (inverse) of the data programmed is read during verify.

Normal Operation

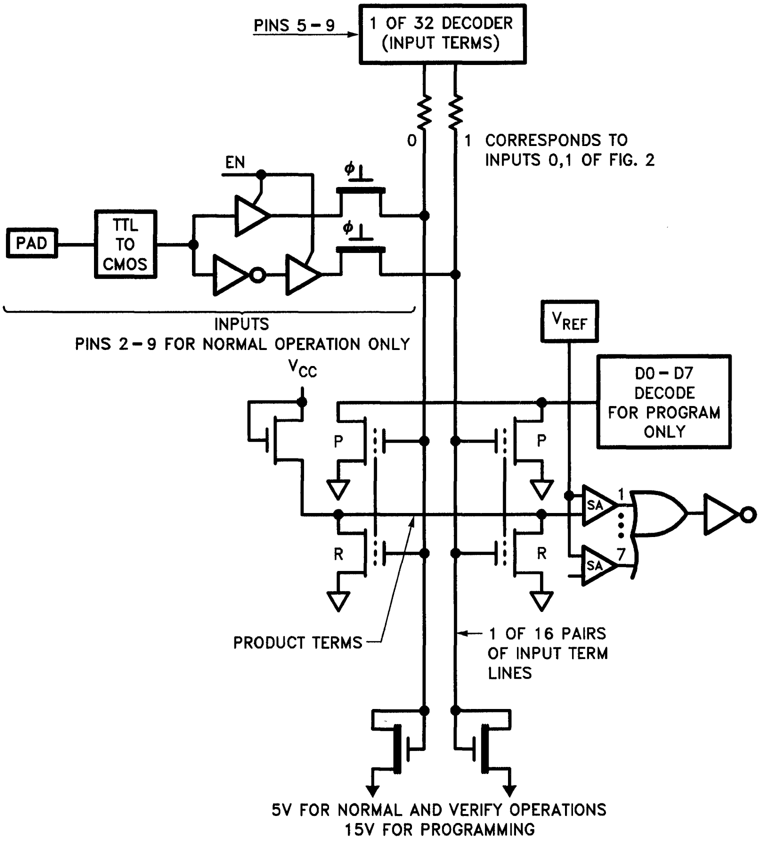
The PAL device will implement the programmed function when there are no supervoltages applied to any of the pins. During regular PAL operation the 1 of 32 decoder and the D0–D7 decoder are disabled, the EN signal is HIGH and all 32 input term lines are at 5 volts. Under these conditions, the data at the input pins is applied to all 64 of the product term lines. If any of the P transistors (16 per product term line) had not been programmed, they will turn on and pull the lower input to the corresponding sense amplifier (SA) to 2 volts or less. This voltage will be less than the reference (Vref) so that the output of the sense amplifier will be LOW.

The reference is an unprogrammed EPROM cell that tracks the same process, voltage and temperature variations that affect all of the cells in the array. It is approximately three volts at room temperature and nominal (5 volts) V_{CC}.


PIN
1
VPP
PROGRAM LOGIC & H.V.
PROGRAM
1 OF 32 DECODE (PROGRAM ONLY)
32
14
FEEDBACK BUFFERS
PINS
5-9
5
INPUT BUFFER & H.V.
PINS
12-19
8
INPUT BUFFER & H.V.
PINS
2-4
3
1 OF 8 DECODE INPUT BUFFER & H.V.
AND EPROM CELL ARRAY
2048 REG.
256 PHANTOM
SENSE AMPLIFIERS
7X8=56
8
7-INPUT
NOR GATES
8
OUTPUT DRIVERS
8
PINS
12-19
OE
PROGRAM
32
PAL/PROGRAM VOLTAGE SELECT
REFERENCE FOR SENSE AMPLIFIER

0049-3

Figure 3. 16L8 Device Simplified Block Diagram


PINS 5-9
1 OF 32 DECODER (INPUT TERMS)
0
1 CORRESPONDS TO INPUTS 0,1 OF FIG. 2
EN
ϕL
ϕL
PAD
TTL TO CMOS
INPUTS
PINS 2-9 FOR NORMAL OPERATION ONLY
VCC
VREF
D0-D7 DECODE FOR PROGRAM ONLY
P
P
SA
1
7
SA
R
R
PRODUCT TERMS
1 OF 16 PAIRS OF INPUT TERM LINES
5V FOR NORMAL AND VERIFY OPERATIONS
15V FOR PROGRAMMING

0049-4

Figure 4. Programming Method

Phantom Operation

The PAL C 20 device is in the PHANTOM mode of operation when a supervoltage ($V_{PP} = 13.5V$) is applied to pin 6. The phantom array is programmed as shown in *Figure 2.* The user may measure the worst case propagation delay from the pin 2 input to the outputs (pins 12 through 17). The truth table for the phantom array is shown in Table 5.

Table 5. Phantom Array Truth Table

	Inputs			**Outputs**							
Pin	**2**	**3**	**4**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**
	0	0	1	X	X	1	1	1	1	1	1
	1	0	1	X	X	0	0	0	0	0	0
	0	1	X	1	0	X	X	X	X	X	X
	0	1	X	0	1	X	X	X	X	X	X

Reliability

Reliability is designed into all Cypress products from the beginning by using design techniques to eliminate latchup, improve ESD and by paying careful attention to layout. In addition, all products are tested for all known types of CMOS failure mechanisms.

Failure mechanisms can be either classified as those generic to CMOS technology or those specific to EPROM devices.

Table 6 lists both categories of failures, their relevant activation energies, Ea in eV (electron volts), and the detection method used by Cypress. In both cases, the mechanisms are aggravated by HTOL (High Temperature Operating Life) tests and HTS (High Temperature Storage) tests.

Specific EPROM failure mechanisms include charge loss, charge gain and electron trapping. Charge loss is accelerated by thermal energy and field emission effects.

Thermal charge loss failures usually occur on random bits and are often related to latent manufacturing defects.

Field emission effects are generally detected as weakly programmed cells. The high voltages used to program a "selected bit" may disturb (as a result of a defect) an "unselected bit".

Charge gain is due to electrons accumulating on a floating gate as a result of bias or voltage on the gate. This results in a reduced read margin. This mechanism is generally negligible.

Charge gain and charge loss are monitored on every Cypress die in wafer form by programming, performing a HTS test and verifying that the programmed data is retained in the device.

Table 6. Generic CMOS Failure Mechanisms

Mechanism	Activation Energy (eV)	Detection Method
Surface Charge	0.5 to 1.0	HTOL, Fabrication Monitors
Contamination	1.0 to 1.4	HTOL, Fabrication Monitors
Electromigration	1.0	HTOL
Micro-cracks	—	Temperature Cycling
Silicon Defects	0.3	HTOL
Oxide Breakdown	0.3	High Voltage Stress, HTOL
Hot Electron Injection	—	LTOL (Low Temp. Operating Life)
Fabrication Defects	—	Burn In
Latchup	—	High Voltage Stress, Burn In, Characterization
ESD	—	Characterization
Charge Loss	0.8 to 1.4	HTS (High Temperature Storage)
Charge Gain (Oxide Hopping)	0.3 to 0.6	HTOL
Electron Trapping in Gate Oxide	—	Program/Erase Cycle

Notes:

Table 6 has been adapted from, "An Evaluation of 2708, 2716, 2532, and 2732 Types of U-V EPROMS, Including Reliability and Long Term Stability." Danish Research Center for Applied Electronics, Nov. 1980.

HTOL Testing

High Temperature Operating Life test (or burn-in) is used to detect most generic CMOS failure mechanisms. Units are placed in sockets under bias conditions with power applied and at elevated temperatures for a specific number of hours. This test is used to weed out the "weak sisters" that would fail during the first 100 to 500 hours of operation under normal operating temperatures. HTOL tests are also used to measure parameter shifts in order to predict (and screen for) failures that would occur much later.

HTS Testing

High Temperature Storage tests are used to thermally accelerate charge loss. These tests are performed at the wafer level and under unbiased conditions. Both pass/fail data as well as shifts in thresholds may be measured. For a more detailed discussion of charge loss screening the reader is referred to the article on EPROM reliability beginning on page 132 of the August 14, 1980, issue of Electronics magazine.

The generally accepted screening method for identifying charge loss is a 168 hour bake at 250°C. This correlates with more than 220,000 years of normal operation at 70°C using a failure activation energy of 1.4 eV.

Initial Qualification

The process in general and the EPROM cell design in particular was qualified using HTS (bake) at 250°C for 256 hours, in conjunction with an HTOL test at 125°C for 1000 hours.

Procedure

Four wafers were erased using ultraviolet light and the linear thresholds of the cell read transistors measured at twenty-five "sites" on each wafer.

The wafers were then programmed and the linear thresholds then measured and recorded.

The wafers were alternately baked at 250°C and the linear thresholds measured and recorded at 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64, 128, and 256 hours. The number of device hours is then 100 × 256 = 25,600.

Results

The average threshold reduction due to charge loss was 0.66 volts. The range was eight to ten percent of the average initial threshold of 7.7 volts. This reduced threshold is greater than four volts above the sense amplifier voltage reference. There were no failures.

If the charge loss failure activation energy is assumed to be 1.4 eV, the HTS time of 256 hours at 250°C translates to 438,356 years of operation at 70°C.

The time translations were computed using the industry standard Arrhenius equation, which converts the time to failure (operating lifetime) at one temperature and time to another temperature and time.

Summary

Sample size:	100
Device hours:	25,600 hours
HTS conditions:	256 hours at 250°C
Average initial threshold:	7.7 volts
Average threshold decrease:	0.66 volts
Standard deviation:	0.12
Lifetime (1.4 ev):	438,356 years at 70°C

Conclusion

An HTS experiment, performed according to industry standard conditions, and using representative Cypress product confirms that the data retention characteristics of the EPROM cell used in all Cypress PLDs and PROMs guarantees a minimum operating lifetime of 438,356 years for activation energies of 1.4 eV.

Production Screen

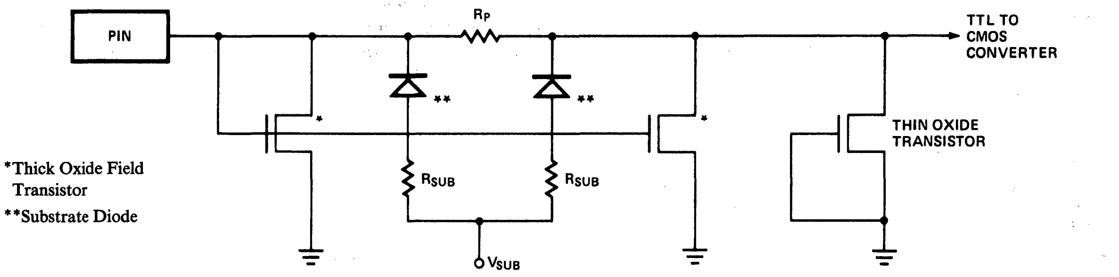
Units from the same population were assembled without being subjected to HTS and were subjected to an HTOL of 150 degrees C for 1000 hours. The units were tested at 12, 24, 48, 96, 168, 336, and 1008 hours and the measurements recorded. Variations in the thresholds of the EPROM cells were measured and correlated to the units tested in the HTS test in order to determine a maximum acceptable rate of charge loss in order to guarantee data retention over their normal operating lifetime.

Advantages Over Bipolar

Lower power results in several benefits to the user. They are:

- Lower capacity and, therefore, lower cost power supplies.
- Reduced cooling requirements.
- Increased long term reliability due to lower die junction temperatures.

Power dissipation may be further reduced by driving the inputs between 0.5 volts (or less) and 4 volts (or more). This reduces the power dissipation in the input TTL to CMOS buffers, which dissipate power when their inputs are between 0.8 volt and 3 volts. Each buffer draws approximately 0.8 mA of I_{CC} current at $V_{IN} = 2$ volts.



0049-5

Figure 5. Input Protection Circuit

Appendix

The Cypress double-layer polysilicon, single-layer metal, N-well, CMOS technology has been optimized for performance. Careful attention to design details and layout techniques has resulted in superior performance products with improved ESD input protection and improved latchup protection.

Input ESD Protection

The circuit shown in *Figure 5* is used at every input pin in all Cypress products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high (ESD) voltage from reaching the thin gate oxides of the internal transistors.

The circuit consists of two thick oxide (field) transistors wrapped around an input resistor (R_P) and a thin oxide (gate) transistor with a relatively low breakdown of 12 volts. Large input voltages cause the thick oxide transistors to turn on, discharging the ESD current to ground. The thin oxide transistor breaks down when the voltage across it (drain to source) exceeds 12 volts. It is protected from destruction by the current limiting action of R_P.

Experiments have confirmed that this input protection circuitry results in ESD protection in excess of 2001 volts.

Definition of Latchup

Latchup is a regenerative phenomenon that occurs when the voltage at an input pin or an output pin is either raised above the power supply voltage potential or lowered below the substrate voltage potential (which is usually ground).

Current rapidly increases until, in effect, a short circuit from V_{CC} to ground exists. If the (V_{CC}) current is not limited it will destroy the device; usually by melting a metal trace.

Causes of Latchup

The CMOS processing, which provides both N-channel and P-channel MOS transistors, also inherently provides parasitic bipolar transistors; both NPNs and PNPs. Latchup is caused when these parasitic transistors are inadvertently turned on.

As long as the voltages that are applied to the package pins of the CMOS IC remain within the limits of the power supply voltages (usually 0 volts to 5 volts), these parasitic bipolar transistors will remain dormant (i.e., off). However, when either negative voltages or positive voltages greater than the V_{CC} supply voltage are applied to input or output pins, these parasitic bipolar transistors may turn on and cause latchup.

Conditions For Latchup

A cross section of a typical CMOS inverter using a P-channel pullup transistor and an N-channel pulldown transistor is shown in *Figure 6*. Also shown is an N-channel output driver that is isolated from the CMOS inverter by a guard ring (channel stopper) that is necessary to prevent parasitic MOS transistors between devices. P+ guard rings surround N-channel devices and N+ guard rings surround P-channel devices. The parasitic SCR (PNPN) and bias generator are illustrated in *Figure 7.* The output driver schematic is not shown.

In order for latchup to occur two conditions must be satisfied; (1) the product of the betas of the NPN and PNP transistors must be greater than one, and (2) a trigger current must exist that turns on the SCR.

Since the SCR structure in bulk CMOS cannot be eliminated, preventing latchup is reduced to keeping the SCR from turning on. If either $R_{WELL} = 0$ or $R_{SUB} = 0$ the SCR cannot turn on because the base emitter junction of the PNP cannot be forward biased because they are tied together and the base emitter junction of the NPN cannot be forward biased because the base is connected to ground. Note, however, that the NPN could be turned on by a negative voltage on the output pin (if the right end of R_{SUB} is grounded).

Prevention of Latchup; Traditional Approaches

The traditional cures include increased horizontal spacing, diffused guard rings and metal straps to critical areas. These solutions are obviously opposite to the goal of greater density.

A brute-force approach that has been successful in reducing latchup has been to increase the conductivity of the N-well and the substrate. Changing the well

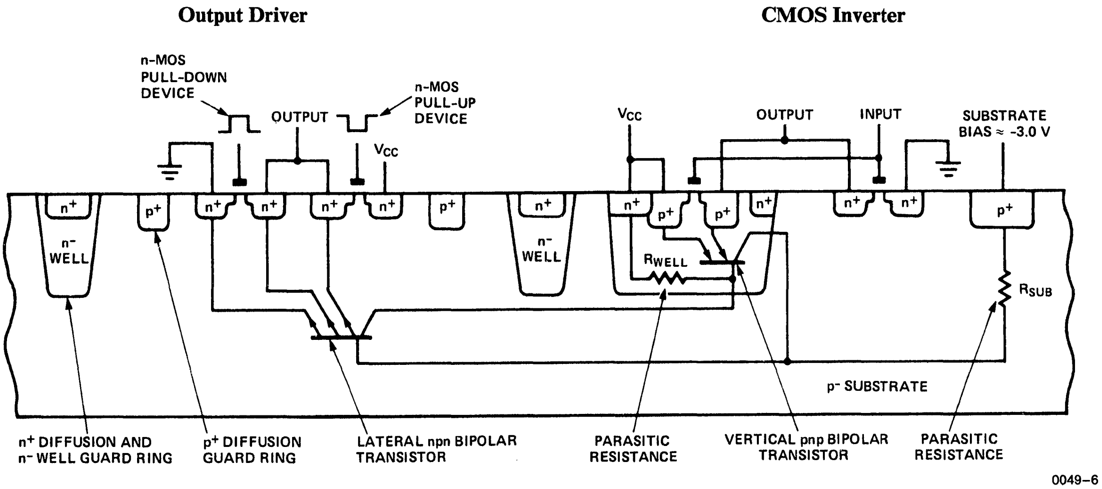
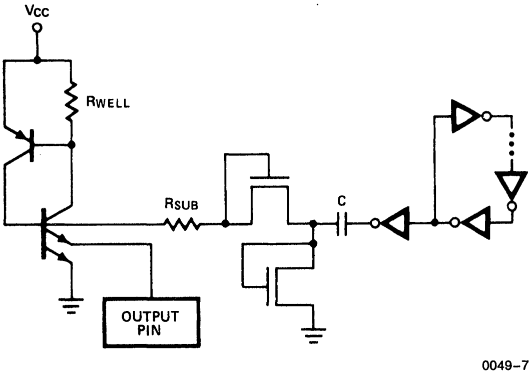

Output Driver
CMOS Inverter
n-MOS PULL-DOWN DEVICE
OUTPUT
n-MOS PULL-UP DEVICE
Vcc
n+
p+
n- WELL
Vcc
OUTPUT
INPUT
SUBSTRATE BIAS ≈ -3.0 V
RWELL
RSUB
p- SUBSTRATE
n+ DIFFUSION AND n- WELL GUARD RING
p+ DIFFUSION GUARD RING
LATERAL npn BIPOLAR TRANSISTOR
PARASITIC RESISTANCE
VERTICAL pnp BIPOLAR TRANSISTOR
PARASITIC RESISTANCE
0049-6

Figure 6. CMOS Cross Section and Parasitic Circuits

conductivity is unacceptable because it affects the characteristics of the P-channel MOS transistors. Using an epitaxial layer to reduce the substrate resistivity (R_{SUB}) is another possible solution.


Vcc
RWELL
RSUB
C
OUTPUT PIN
0049-7

Substrate Bias Generator →

Figure 7. Parasitic SCR and Bias Generator

The Cypress Solution to Latchup

Cypress uses several design techniques in addition to careful circuit layout and conservative design rules to eliminate latchup.

NMOS Output Pullup Transistors

Conventional CMOS technology uses a P-channel MOS as a pullup transistor on the output drivers. This has the advantage of being able to pull the output voltage HIGH level to within 100 millivolts of the positive voltage supply. However, this is of marginal value when TTL compatibility is required. In addition, the P-channel pullup is sensitive to overshoot and introduces another vertical PNP transistor that further compounds the latchup problem. Cypress uses N-channel pullup transistors that eliminate all of these problems and still maintain TTL compatibility.

Substrate Bias Generator

Cypress is the first company to use a substrate bias generator with CMOS technology. The bias generator keeps the substrate at approximately −3 volts DC, which serves several purposes.

Input Pins

The parasitic diodes shown in *Figure 5* cannot be forward biased unless the voltage at an input pin is at least one diode drop more negative than −3 volts. This translates into increased device tolerance to (negative voltage) undershoot at the input pins, caused by inductance in the leads. If the undershoot is this large, the output impedance of the bias generator itself is sufficient to prevent trigger current from being generated.

Output Pins

The same reasoning applies to negative voltages at the output pins as shown in *Figure 7*. In order to turn on the NPN transistor the voltage at the output pin must be at least one VBE more negative than −3 volts.

Guard Ring

To protect the "core" of the die from free floating holes and stray currents, a diffused collection guard ring that is strapped with metal and connected to the bias generator is used. This provides an effective wall against transient currents that could cause mis-reading of the EPROM cells.

CYPRESS
SEMICONDUCTOR

PAL® C 16R6 Design Example: GCR Encoder/Decoder

Introduction

Digital encoding and decoding of data is often used to increase the reliability of data transmission and storage. One area where digital techniques are employed is the transformation between data stored on one-quarter inch magnetic tape and serial digital data.

This document describes the procedure used to encode/decode serial digital data for recording/reading from one-quarter inch magnetic tape using a Cypress CMOS PAL C 16R6 to implement the logic.

History

The recording format and the Group Code Recording (GCR) code have been adopted and incorporated in a series of standards by a committee called the QIC (Quarter Inch Cartridge) Committee, composed of manufacturers and users of quarter inch tapes and cartridges. The purpose of the committee is to insure compatibility between manufacturers and reliability to end users.

Quarter inch tape cartridges are used extensively to backup or archive data from hard disks. Most drives are operated in a continuous or streaming mode (for reasons that will be discussed later) and data is recorded at 10,000 FRPS (Flux Reversals Per Inch) in a serpentine manner on seven to fourteen channels. The tape moves at 30 to 90 ips (inches per second) and the error rates achieved are one in 10^9 or 10^{10}. A cartridge holds 2000 to 3000 feet of tape 0.001 inch thick and stores 20 to 80 million bytes (mega-bytes) of data.

Typical System

A block diagram of a typical system is shown in *Figure 1.* The interface between the Host (or Host Adapter) is bi-

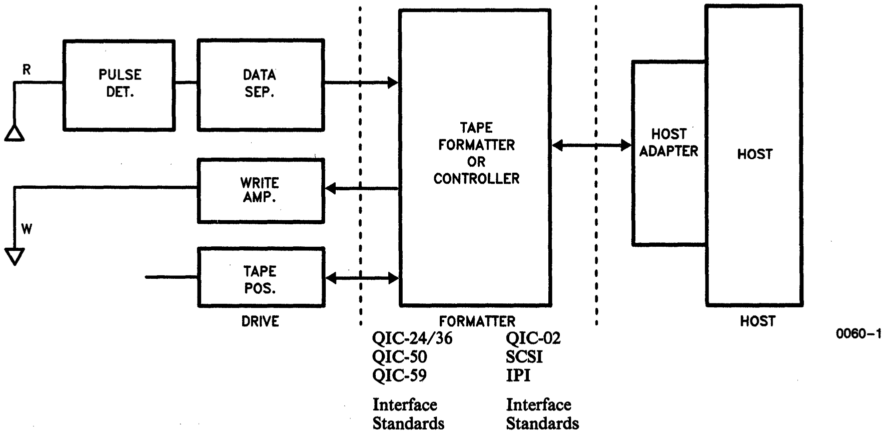


Figure 1. A Typical Tape Drive System

PAL® is a registered trademark of Monolithic Memories Inc.
ABEL™ is a trademark of Data I/O Corporation
PALASM™ is a trademark of Monolithic Memories Inc.
VAX™ is a trademark of Digital Equipment Corp.
WORDSTAR™ is a trademark of MicroPro International

Typical System (Continued)

directional, with a byte-wide data path and 10 to 20 control signals, depending upon the interface standard. Data rates are 300 KBs (thousand Bytes per second) to 1 MBs (Million Bytes per second).

The Formatter or Tape Controller performs serial/parallel conversion and encoding/decoding of the data as well as error checking and, in some cases, error correcting. Control is usually provided by a state machine that handles the handshaking between the host as well as control of the tape. Data is written in blocks of various lengths (depending upon the standard) and a "read after write" check is usually performed. Buffer storage of at least two blocks of data is usually provided using static RAMs (SRAMs), FIFOs, or some combination of the two.

The Drive electronics consist of digital signals that control and sense the tape motion and analog signals in the read and write paths. The interface between the Drive and the Formatter is digital and, once again, there are various standards.

Reading and Writing on Tape

To write on the tape a current of 100 mA or less is used to change the direction of magnetization. To read from the tape a coil of wire (the read head) is held against the tape and a voltage (10 mV or less) is induced by the change in direction of the magnetic flux on the tape.

Recording Codes

All codes used for recording on magnetic mediums are classified as Franaszek Run Length Limited (RLL) codes of the form:

(D, K)

where D = the minimum number of zeros between consecutive ones, and

K = the maximum number of zeros between consecutive ones.

D controls the highest frequency that can be recorded and K controls the lowest frequency.

Using the Franaszek notation, the GCR code is (1, 2). As illustrated in *Figure 2,* a flux reversal signifies a one and the absence of a flux reversal signifies a zero. This is true for all codes.

Peak Detection and Data Separation

Peaks are detected (versus zero crossings) because the circuits used are less sensitive to noise. The output of the peak detector goes to the most critical analog circuit in the drive; the data separator.

The function of the data separator is to provide ones and zeros that occur at a precise frequency. It does this by first synchronizing itself to a crystal controlled reference clock and then attempting to "lock" itself to the maximum data frequency on the tape by finding the phase difference between itself and the data output of the peak detector and driving a voltage controlled oscillator (VCO) such that they are equal. This is called a Phase Locked Loop (PLL). The frequency of the reference clock must be at least twice (2f) that of the highest frequency that is to be read (f).

The PLL is synchronized to the 2f reference frequency when it is not in use. A string of ones is recorded, which is called the preamble, before the block of data is recorded. When the command to read is given, the 2f reference frequency is removed from the data separator and the signal from the peak detector is applied to the data separator. The PLL then attempts to "lock" to the preamble. Just after the preamble, a code violation is recorded so that the Formatter can recognize where valid data begins. The procedure of locking onto the preamble is called "getting bit sync." The detection of the code violation is called "obtaining byte sync".

PLLs typically exhibit frequency and phase offsets during acquisition of the preamble. Phase errors also occur after lock, during the reading of the data field. Differences in tape speed during record and playback (as well as from unit to unit) result in frequency differences between the data read from the tape and the 2f reference.

Random phase errors caused by noise, intersymbol interference (bit crowding), timing errors and other transients may also get the PLL out of lock.

The data separator's PLL is susceptible to these errors because it must satisfy two conflicting conditions: (1) it must

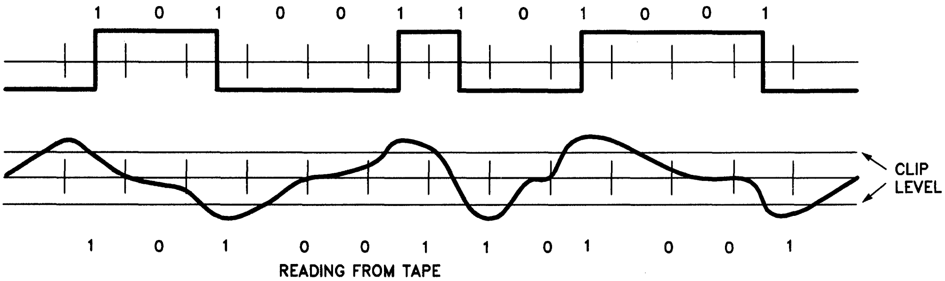


Figure 2

Reading and Writing on Tape (Continued)

lock quickly enough to detect the preamble, but (2) it must not overcorrect phase for a single misaligned bit.

Strings of zeros cause the phase of the PLL to shift and if the shift is larger than the "bit window", an error will occur. The QIC-24 standard calls for up to 37% bit shift tolerance, which means that the data separator must be able to recognize a "one" (flux transversal) that deviates ±18.5% from its expected time position without causing a data error. In order to achieve this performance a four-bit binary nibble is encoded into a five-bit "GCR code word" that is written onto the tape.

Reasons for the GCR Code

The 5-bit GCR code format is required to encode the data such that no more than two consecutive zeros occur in the serial data. This encoding relaxes the performance requirements of the PLL and the loop filter so that the desired system performance can be achieved.

Static Tolerances

Another reason for GCR encoding is to compensate for the speed variation of the tape due to:

- Mechanical Tolerances
    - Cartridge
    - Tape thickness (±3%)
- Tape Elasticity and Wear
- Motor Speed Variation
- Temperature and Humidity

The preceding static tolerances can result in a ±10% speed variation of the tape.

Dynamic Tolerances

In addition to the static tolerances, there are Instantaneous Speed Variations (ISV) due to discontinuous tape release at the unwind spool (10–20%), guide/back stick slip (5%) and shuffle ISV (vibration) due to start/stop (5–30%). The shuffle ISV can be avoided by operating the tape in a continuous (streaming) mode. If these dynamic tolerances are added together they can result in a ±15% speed variation.

Electronics Compensate

The electronics in the tape controller and the drive are designed to compensate for the tape speed variations due to the mechanical tolerances.

The compensation is performed by:

- Data Encoding and Error Detection and Correction
- Phase Locked Loop Design
- Bit Window Tolerance

Sequence of Operations

During a write operation the following sequence occurs:

1. Idle (Hold)
2. Convert 4-bit parallel input to 5-bit GCR code and load into 5-bit register.
3. Shift out 5-bits to write amplifier.

During a read operation the following sequence occurs:

1. Idle (same as during write)
2. Shift in 5-bits.
3. Detect sync mark

   Set/Clear invalid flag

   Convert 5-bit serial input to 4-bit binary value and load into register.

Note: that the read clock and the write clock are not the same.

Also, the logic must keep up with the tape data rate.

And finally, the read and write operations are mutually exclusive so that the storage elements (D flip-flops) can be time-shared and that read and write operations require 5 clocks.

A total of 5 states are required because the idle state is common to both read and write operations. Therefore, 3 control lines will be required. It is convenient to designate one control line as an enable line (active LOW) and the other two lines as Mode Control signals.

The control of these lines is not described here, nor is the required clock synchronization. The reason for not doing this is that at the next level of control, system considerations such as what action to take when errors occur must be implemented in hardware and these tend to be not only application dependent but also very subjective.

The diagrams of *Figure 3* show the flow of data under the control of the ENABLE signal and the M0 and M1 mode control signals.

The GCR Code

The GCR code is part of the QIC-24 Standard and is also the ANSI X3.54 standard (1976). The MSB (leftmost bit) is recorded first. Note that there are a maximum of two consecutive zeros in the five-bit code that is recorded on the tape.

	4-Bit Code				**5-Bit Code**				
Line Number (For Ref.)	**D 3**	**D 2**	**D 1**	**D 0**	**Y 3**	**Y 2**	**Y 1**	**Y 0**	**S o**
0	0	0	0	0	1	1	0	0	1
1	0	0	0	1	1	1	0	1	1
2	0	0	1	0	1	0	0	1	0
3	0	0	1	1	1	0	0	1	1
4	0	1	0	0	1	1	1	0	1
5	0	1	0	1	1	0	1	0	1
6	0	1	1	0	1	0	1	1	0
7	0	1	1	1	1	0	1	1	1
8	1	0	0	0	1	1	0	1	0
9	1	0	0	1	0	1	0	0	1
10	1	0	1	0	0	1	0	1	0
11	1	0	1	1	0	1	0	1	1
12	1	1	0	0	1	1	1	1	0
13	1	1	0	1	0	1	1	0	1
14	1	1	1	0	0	1	1	1	0
15	1	1	1	1	0	1	1	1	1
	A 3	A 2	A 1	A 0	B 0	B 1	B 2	B 3	B 4

Figure 4. GCR Code

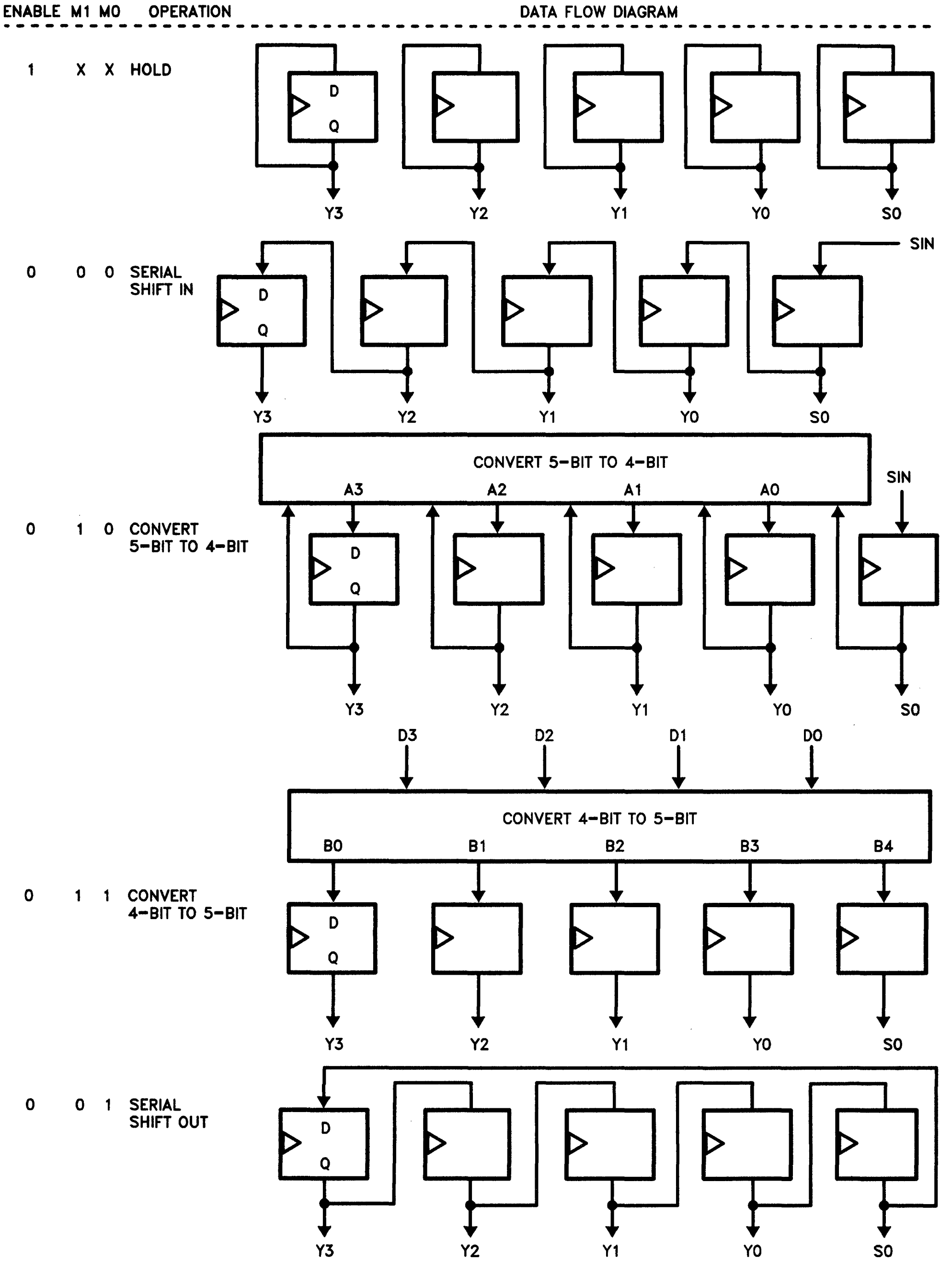

ENABLE M1 M0
OPERATION
DATA FLOW DIAGRAM
1 X X HOLD
D
Q
Y3
Y2
Y1
Y0
S0
0 0 0 SERIAL SHIFT IN
SIN
D
Q
Y3
Y2
Y1
Y0
S0
CONVERT 5-BIT TO 4-BIT
A3
A2
A1
A0
SIN
0 1 0 CONVERT 5-BIT TO 4-BIT
D
Q
Y3
Y2
Y1
Y0
S0
D3
D2
D1
D0
CONVERT 4-BIT TO 5-BIT
B0
B1
B2
B3
B4
0 1 1 CONVERT 4-BIT TO 5-BIT
D
Q
Y3
Y2
Y1
Y0
S0
0 0 1 SERIAL SHIFT OUT
D
Q
Y3
Y2
Y1
Y0
S0
0060-3

Figure 3. Data Flow Diagrams

Design Procedure

The design procedure will be to map the code conversions using Venn diagrams and write the logic equations as the "sum of products" or in minterm form. Six flip-flops are required, so the logic will be implemented using a PAL C 16R6. Because the PAL device has inverting output buffers, the zeros will be mapped. The D flip-flops require an "extra term" for them to hold their states when the ENABLE is HIGH.

For example, for a conventional D flip-flop the form of the logic equations would be:

D =	ENABLE 1 (Q)	; RECIRCULATE PRESENT STATE
+	ENABLE 2 (F2)	; FUNCTION 2
+	ENABLE 3 (F3)	; FUNCTION 3

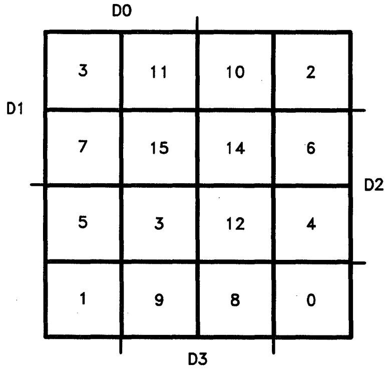
Where the ENABLE controls are mutually exclusive.

4-Bit to 5-Bit Conversion for Y3 Output

In *Figure 4* (at the bottom) the 5-bit code columns are labeled B0 through B4 to help the reader understand how the 4-bit code is mapped. In addition, the line numbers are labeled 0 through 15, which correspond to the values of the 4-bit binary code.

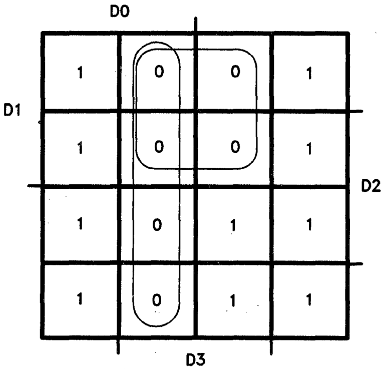
Figure 5a shows how the 4-bit binary code is mapped on the Venn diagram. For example, reference line number zero, which corresponds to binary value zero, is located in the lower right hand corner of *Figure 5a.*

The Venn diagram of *Figure 5b* shows the conversion for the $\overline{Y3}$ output. It is labeled the B0 input to the D flip-flop. Note that the parallel nibble (see *Figure 3*) is reversed (end for end) so that the MSB is written first when it is shifted out.



0060-4

Figure 5a. Binary Values



0060-5

Figure 5b. $\overline{Y3}$ Map

In *Figure 5b,* the ones and zeros in column B0 are mapped. For example, reference line zero has the value 1 in column B0 of *Figure 4.* Therefore, a one is placed in the square corresponding to binary value zero in *Figure 5b.* In a similar manner, ref. line 15 has a value of zero in column B0, so a zero is placed in the square corresponding to binary value fifteen.

Writing the Equation

If the output of the PAL C 16R6 were positive true logic, we would write the equation to include all of the ones on the Venn diagram. However, because the PAL device output is negative logic (active LOW) we will write the equation to include all of the zeros. Then, when the PAL device inverts the signals, the zeros will be changed to ones, so that the final outputs will be positive true logic.

By inspection:

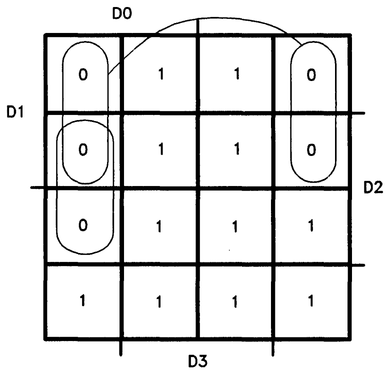
$\overline{B0}$ = D3 D0 + D3 D1 or,

$\overline{Y3}$ = D3 D0 + D3 D1

Design Procedure (Continued)

4-Bit to 5-Bit Conversions for $\overline{Y2}$, $\overline{Y1}$, $\overline{Y0}$, $\overline{So}$

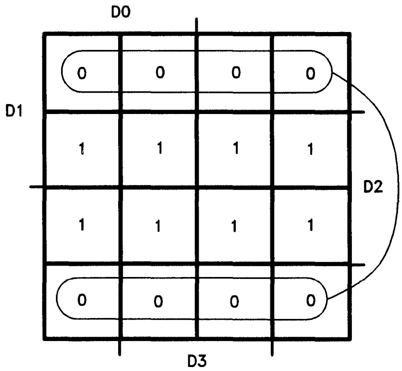
These are presented for the sake of completeness.



0060-6

$\overline{Y2} = \overline{B1} = \overline{D3}\,D1 + \overline{D3}\,D2\,D0$

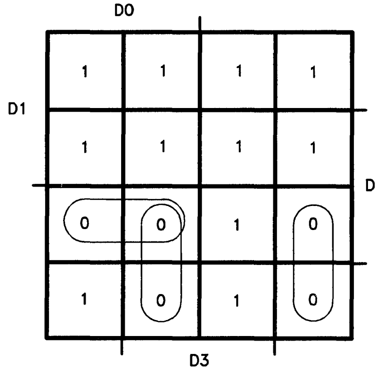
Figure 5c. $\overline{Y2}$ Map



0060-7

$\overline{Y1} = \overline{B2} = \overline{D2}$

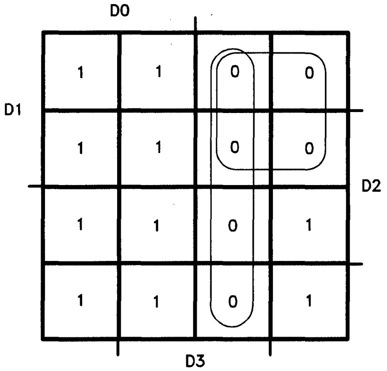
Figure 5d. $\overline{Y1}$ Map



0060-8

$\overline{Y0} = \overline{B3} = \overline{D3}\,\overline{D1}\,\overline{D0} + D3\,\overline{D1}\,D0 + D2\,\overline{D1}\,D0$

Figure 5e. $\overline{Y0}$ Map



0060-9

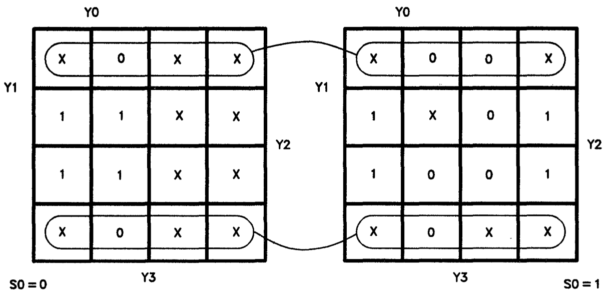
$\overline{So} = \overline{B4} = D1\,\overline{D0} + D3\,\overline{D0}$

Figure 5f. $\overline{So}$ Map

5-Bit to 4-Bit Conversion for $\overline{Y}$ Outputs

This conversion requires two 16 square Venn diagrams because there are $2^5 = 32$ possible binary values. However, note that in *Figure 4* not all 32 possible combinations are used in the 5-bit code columns. These unused combinations are "don't cares", which are represented by Xs in the Venn diagrams, which can be either ones or zeros, which further reduces or simplifies the logic equations.

The procedure is: plot the 1s and 0s
put Xs in the blank squares
write the equations for the zeros.


Y0
Y1
Y2
Y3
S0 = 0
Y0
Y1
Y2
Y3
S0 = 1

S0 = 0

X	0	X	X
1	1	X	X
1	1	X	X
X	0	X	X

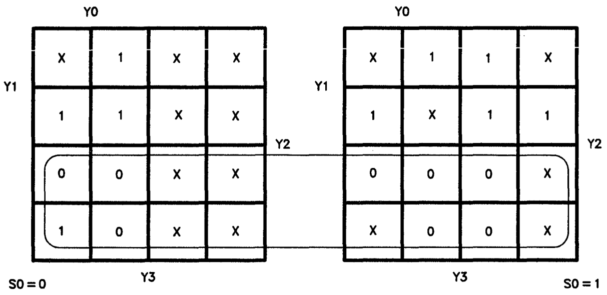
S0 = 1

X	0	0	X
1	X	0	1
1	0	0	1
X	0	X	X

0060–10

$\overline{Y3} = \overline{A3} = \overline{Y2} + Y3\,S_o$

Figure 6a


Y0
Y1
Y2
Y3
S0 = 0
Y0
Y1
Y2
Y3
S0 = 1

S0 = 0

X	1	X	X
1	1	X	X
0	0	X	X
1	0	X	X

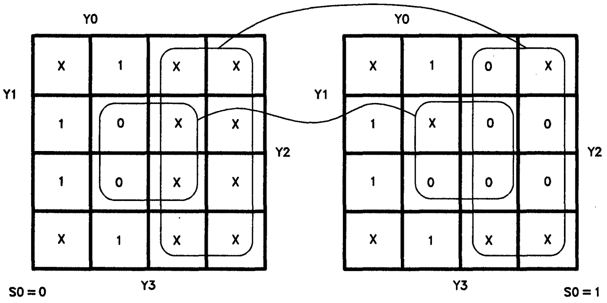
S0 = 1

X	1	1	X
1	X	1	1
0	0	0	X
X	0	0	X

0060–11

$\overline{Y2} = \overline{A2} = \overline{Y1}$

Figure 6b


Y0
Y1
Y2
Y3
S0 = 0
Y0
Y1
Y2
Y3
S0 = 1

S0 = 0

X	1	X	X
1	0	X	X
1	0	X	X
X	1	X	X

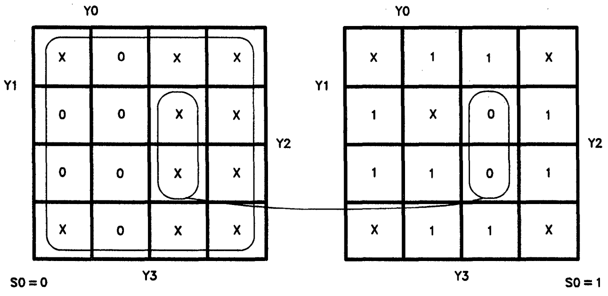
S0 = 1

X	1	0	X
1	X	0	0
1	0	0	0
X	1	X	X

0060–12

$\overline{Y1} = \overline{A1} = \overline{Y0} + Y3\,Y2$

Figure 6c


Y0
Y1
Y2
Y3
S0 = 0
Y0
Y1
Y2
Y3
S0 = 1

S0 = 0

X	0	X	X
0	0	X	X
0	0	X	X
X	0	X	X

S0 = 1

X	1	1	X
1	X	0	1
1	1	0	1
X	1	1	X

0060–13

$\overline{Y0} = \overline{A0} = Y3\,Y2\,\overline{Y0} + \overline{S_o}$

Figure 6d

Design Procedure (Continued)

Serial Shift In

During serial shift in (both mode control signals LOW) the data output of the data separator is applied to the input of the formatter. The signal is called SIN and is applied to the D input of the SOUT flip-flop. The output of the SOUT flip-flop is applied to the D input of the Y0 flip-flop and its output is applied to the input of the Y1 flip-flop, etc. After five read clocks the MSB of the 5-bit GCR coded data is in Y3 and the LSB is in SOUT.

Serial Shift Out

During a write operation, after the 4-bit data is converted to 5-bit data and reversed, it is shifted out using the write clock and written on tape. The shift direction is opposite to that in Serial Shift In. Note that it is right shifted "end around" (see *Figure 3*) so that after 5 write clocks the same data appears in the register.

Invalid Flag (INV Flip-Flop)

The Invalid flip-flop is set to a one when an invalid 5-bit code is read from the tape. This is used to tell the tape Formatter that the next data read is the beginning of the data block. This procedure is called getting "byte sync." INV is a negative true signal, so the logic equations are written for ones on the Venn diagram.

The 16 binary values that are NOT listed in *Figure 4* are plotted as ones in *Figure 7.* The procedure was to plot zeros in the squares where there were valid 5-bit codes, then fill the rest with ones and then write the equation for the ones.

The Invalid flip-flop is enabled by a signal called CIF (Control Invalid Flag) and reset when CIF is LOW.

Synchronization Mark Detection

Bit synchronization is achieved when the illegal 5-bit code of all ones is read from the tape. It is the logical AND of all five bits, or BS = Y3 • Y2 • Y1 • Y0 • SOUT.

Implementation Procedure

Once the conceptual design has been completed, it must be reduced to practice. There are two main steps in the process;

1. describe the logic using a high-level language, and
2. program the PAL device.

Several programs that run on the IBM PC (or equivalent) or the VAX™ computer are available from either semiconductor manufacturers or from third party software vendors. The first such program, called PALASM™ (PAL device Assembler) was developed by Monolithic Memories. It enables the designer to describe the logic in terms of Boolean equations, truth tables, or state diagrams using a language whose syntax is comparable to a microcomputer assembly language.

PALASM Equations

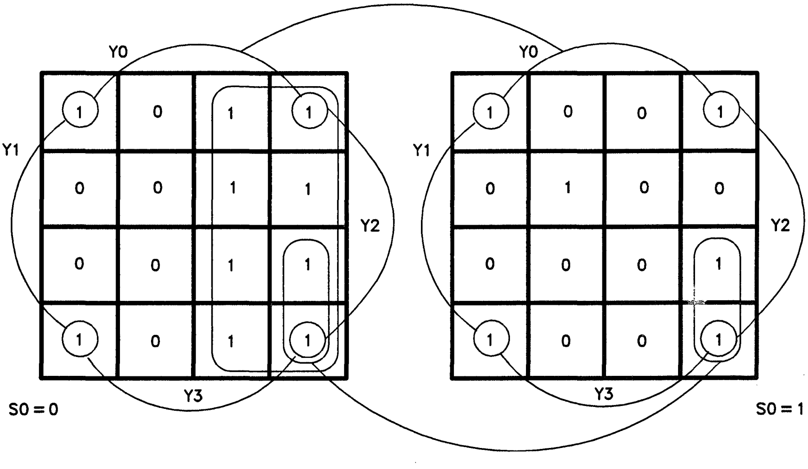
The equations were written in the PALASM syntax. The (ASCII) file created using WORDSTAR in the non-document (N) mode is shown in *Figure 8.*

Conversion to ABEL™

The PALASM file (GCREX.PAL) was then translated to ABEL syntax using the TOABEL program. The format of the command is:

TOABEL −IB:GCREX −OB:GCREXT

The TOABEL program converted the GCREX.PAL file to a file named GCREXT.ABL, whose listing is shown in *Figure 9.*



0060-14

$INV = \overline{Y0}\,\overline{SOUT} + \overline{Y3}\,\overline{Y2} + \overline{Y3}\,\overline{Y1}\,\overline{Y0} + Y3\,Y2\,Y1\,Y0\,SOUT$

Figure 7

ABEL Program Procedure

The ABEL program consists of an executive and several overlay programs that are executed by simply typing in;

```
ABEL B:GCREXT
```

followed by an enter (CR) from the keyboard of an IBM (or look-alike) PC. The ABEL program was developed by a programmer manufacturer, Data I/O Corporation. The source file may be simplified (logic reduction), a logic simulation may be performed, and test vectors may be generated.

ABEL Programs

The ABEL programs are:

Program Name	Function
PARSE	Read source file, check syntax, expand macros, act upon assembler directives.
TRANSFOR	Convert the description to an intermediate form.
REDUCE	Perform logic reduction.
FUSEMAP	Create the programmer load (JEDEC) file.
SIMULATE	Simulate the operation of a programmed device.
DOCUMENT	Create a design documentation file.

ABEL Outputs

The output files are:

GCREXT.LST	
GCREXT.OUT	
GCREXT.DOC	see *Figure 10*
GCREXT.SIM	(This design was not simulated.)
P16R6.JED	see *Figure 11*

The last file is in JEDEC (JC-42.1-81-62) format; suitable for loading into a PLD programmer. The listing is shown in *Figure 11*. The DOCUMENT program output is shown in *Figure 10*.

Programming the 16R6

The 16R6 was programmed using the Data I/O model 29B programmer operated in the remote mode to the PC. The design was then verified by checking out the device on the bench.

Summary

Space Saving Advantage

This design example illustrates the space saving advantage of Cypress CMOS PAL devices. The FUSEMAP program printed out that 40 of the 64 available product terms were used.

If the PALASM input equations of *Figure 8* are implemented in two-input gates, approximately thirty gates are required for each one of the six D flip-flop inputs, or a total of 6 × 30 = 180 two-input gates. The logic equations alone would then require 180 divided by 4 = 45 14 pin DIPs. The six flip-flops would require three 14 pin DIPs for a total of 48 DIPs. This example demonstrates the power of the Cypress PAL devices.

Power Saving Advantage

The maximum I_{CC} current, under worst case conditions, for the PAL C 16R6L-25PC is 45 mA.

If the typical I_{CC} per package is assumed to be 10 mA, the total I_{CC} for 50 TTL packages would be 500 mA.

The worst case I_{CC} for the TTL system could be as high as 20 mA per DIP, which would mean a total of one Ampere for the system.

The Cypress CMOS PAL device results in a system power reduction of between a factor of 10 or 15, depending upon whether typical or worst case numbers are compared.

PALASM Equations

```
PAL16R6               DESIGN EXAMPLE               FILENAME; GCREX.PAL
PAT001                                             BRUCE WENNIGER 9/17/85
4B-5B ENCODER/DECODER
CYPRESS SEMICONDUCTOR
 CK M1  M0   D3 D2 D1 D0 /EN  /CIF GND
/E  SIN /INV Y0 Y1 Y2 Y3 SOUT /BS  VCC
/SOUT:= EN*/SOUT                                   +         ; HOLD/RECIRCULATE
        /EN*/M1*/M0*/SIN                           +         ; SERIAL SHIFT IN
        /EN*/M1*M0*/Y0                             +         ; SERIAL SHIFT OUT
        /EN*/M1*/M0*/SIN                           +         ; CONV. SIN & LOAD
        /EN*/M1* M0* D1*/D0                        +         ; CONV. PAR. & LOAD
        /EN*/M1* M0* D3*/D0                                  ; DITTO
```

Figure 8

PALASM Equations (Continued)

```
/Y0    := EN*/Y0                             +      ; HOLD
          /EN*/M1*/M0*/SOUT                  +      ; SERIAL SHIFT IN
          /EN*/M1* M0*/Y1                    +      ; SERIAL SHIFT OUT
          /EN* M1*/M0*/SOUT                  +      ; CONV. SIN & LOAD
          /EN* M1*/M0* Y3* Y2*/Y0            +      ; DITTO
          /EN* M1* M0* D2*/D1*D0             +      ; CONV. PAR. & LOAD
          /EN* M1* M0* D3*/D1* D0            +      ; DITTO
          /EN* M1* M0*/D3*/D1*/D0                   ; DITTO

/Y1    := EN*/Y1                             +      ; HOLD
          /EN*/M1*/M0*/Y0                    +      ; SERIAL SHIFT IN
          /EN*/M1* M0*/Y2                    +      ; SERIAL SHIFT OUT
          /EN* M1*/M0*/Y0                    +      ; CONV. SIN & LOAD
          /EN* M1*/M0* Y3* Y2                +      ; DITTO
          /EN* M1* M0*/D2                           ; CONV. PAR. & LOAD

/Y2    := EN*/Y2                             +      ; HOLD
          /EN*/M1*/M0*/Y1                    +      ; SERIAL SHIFT IN
          /EN*/M1* M0*/Y3                    +      ; SERIAL SHIFT OUT
          /EN* M1*/M0*/Y1                    +      ; CONV. SIN & LOAD
          /EN* M1* M0*/D3* D1                +      ; CONV. PAR. & LOAD
          /EN* M1* M0*/D3* D2* D0                   ; DITTO

/Y3    := EN*/Y3                             +      ; HOLD
          /EN*/M1*/M0*/Y2                    +      ; SERIAL SHIFT IN
          /EN*/M1* M0*/SOUT                  +      ; SERIAL SHIFT OUT
          /EN* M1*/M0* Y3* SOUT              +      ; CONV. SIN & LOAD
          /EN* M1*/M0*/Y2                    +      ; DITTO
          /EN* M1* M0* D3* D0                +      ; CONV. PAR. & LOAD
          /EN* M1* M0* D3* D1                       ; DITTO

INV    :=/CIF* INV                           +      ; HOLD INV FLAG
                                                    ; (ACTIVE LOW)
          CIF* M1*/M0*/Y3*/Y2                +      ; SET IF INVALID
          CIF* M1*/M0*/Y3/Y1*/Y0             +      ; DITTO
          CIF* M1*/M0*/Y0*/SOUT              +      ; DITTO
          CIF* M1*/M0* Y3* Y2* Y1* Y0* SOUT  +      ; DITTO

BS     = Y3* Y2* Y1* Y0* SOUT                       ; BIT SYNC.
                                                    ; (ACTIVE LOW)
```

Figure 8 (Continued)

ABEL Listing

```
module --gcrext;                 flag '-r0;
title
'PAL16R6                         DESIGN EXAMPLE                  FILENAME: GCREX.PAL
PAT001                                         BRUCE WENNIGER 9/17/85
4B-5B ENCODER/DECODER
CYPRESS SEMICONDUCTOR
-Translated by TOABEL-';
P16R6 device 'P16R6';

"declarations
             TRUE,FALSE = 1,0;
             H,L = 1,0;
             X,Z,C = .X.,.Z.,.C.;
             GND,VCC
                     pin   10,20;
             CK,M1,M0,D3,D2,D1,D0,EN,CIF,E
                     pin   1,2,3,4,5,6,7,8,9,11;
             INV,Y0,Y1,Y2,Y3,SOUT
                     pin   13,14,15,16,17,18;
             SIN,BS
                     pin   12,19;
equations
             !SOUT   := !EN & !SOUT
                     # EN & !M1 & !M0 & !SIN
                     # EN & !M1 & M0 & !Y0
                     # EN & M1 & !M0 & !SIN
                     # EN & M1 & M0 & D1 & !D0
                     # EN & M1 & M0 & D3 & !D0 ;
             " HOLD/RECIRCULATE
             " SERIAL SHIFT IN
             " SERIAL SHIFT OUT
             " CONV. SIN & LOAD
             " CONV. PAR. & LOAD
             " DITTO
             !Y0     := !EN & !Y0
                     # EN & !M1 & !M0 & !SOUT
                     # EN & !M1 & M0 & !Y1
                     # EN & M1 & !M0 & !SOUT
                     # EN & M1 & !M0 & Y3 & Y2 & !Y0
                     # EN & M1 & M0 & D2 & !D1 & D0
                     # EN & M1 & M0 & D3 & !D1 & D0
                     # EN & M1 & M0 & !D3 & !D1 & !D0;
```

Figure 9

ABEL Listing (Continued)

```
" HOLD
" SERIAL SHIFT IN
" SERIAL SHIFT OUT
" CONV. SIN & LOAD
"DITTO
"CONV. PAR. & LOAD
"DITTO
"DITTO

!Y1          := !EN & !Y1
              # EN & !M1 & !MO & !YO
              # EN & !M1 & MO & !Y2
              # EN & M1 & !MO & !YO
              # EN & M1 & !MO & Y3 & Y2
              # EN & M1 & MO & !D2 ;

"HOLD
"SERIAL SHIFT IN
"SERIAL SHIFT OUT
"CONV. SIN & LOAD
"DITTO
"CONV. PAR. & LOAD

!Y2          := !EN & !Y2
              # EN & !M1 & !MO & !Y1
              # EN & !M1 & MO & !Y3
              # EN & M1 & !MO & !Y1
              # EN & M1 & MO & !D3 & D1
              # EN & M1 & MO & !D3 & D2 & DO

"HOLD
"SERIAL SHIFT IN
"SERIAL SHIFT OUT
"CONV. SIN & LOAD
"CONV. PAR. & LOAD
"DITTO

!Y3          := !EN & !Y3
              # EN & !M1 & !MO & !Y2
              # EN & !M1 & MO & !SOUT
              # EN & M1 & !MO & Y3 & SOUT
              # EN & M1 & !MO & !Y2
              # EN & M1 & MO & D3 & DO
              # EN & M1 & MO & D3 & D1 ;
```

Figure 9 (Continued)

ABEL Listing (Continued)

```
            "HOLD
            "SERIAL SHIFT IN
            "SERIAL SHIFT OUT
            "CONV. SIN & LOAD
            "DITTO
            "CONV. PAR. & LOAD
            "DITTO

            !INV        := CIF & !INV
                         # !CIF & M1 & !M0 & !Y3 & !Y2
                         # !CIF & M1 & !M0 & !Y3 & !Y1 & !Y0
                         # !CIF & M1 & !M0 & !Y0 & !SOUT
                         # !CIF & M1 & !M0 & Y3 & Y2 & Y1 & Y0 & SOUT ;
            " HOLD INV FLAG
            " SET IF INVALID
            " DITTO
            " DITTO
            " DITTO

            !BS         = Y3 & Y2 & Y1 & Y0 & SOUT;
            " BIT SYNC.
end --gcrext;
```

Figure 9 (Continued)

Document File

```
                                                                    Page 1
ABEL™ Version 1.10 - Document Generator                             17-Sept-85 8:30 AM
PAL16R6             DESIGN EXAMPLE                        FILENAME; GCREX.PAL
PAT001                               BRUCE WENNIGER 9/17/85
4B-5B ENCODER/DECODER
CYPRESS SEMICONDUCTOR
-Translated by TOABEL-
Equations for Module --gcrext
Device P16R6
        Reduced Equations:
            SOUT := !( !EN & !SOUT
                     # EN & !M0 & !M1 & !SIN
                     # EN & M0 & !M1 & !Y0
                     # EN & !M0 & M1 & !SIN
                     # !D0 & D1 & EN & M0 & M1
                     # !D0 & D3 & EN & M0 & M1) ;
            Y0 :=    !( !EN & !Y0
                     # EN & !M0 & !M1 & !SOUT
                     # EN & M0 & !M1 & !Y1
                     # EN & !M0 & M1 & !SOUT
                     # EN & !M0 & M1 & !Y0 & Y2 & Y3
                     # D0 & !D1 & D2 & EN & M0 & M1
                     # D0 & !D1 & D3 & EN & M0 & M1
                     # !D0 & !D1 & !D3 & EN & M0 & M1) ;
            Y1 :=    !( !EN & !Y1
                     # EN & !M0 & !M1 & !Y0
                     # EN & M0 & !M1 & !Y2
                     # EN & !M0 & M1 & !Y0
                     # EN & !M0 & M1 & Y2 & Y3
                     # !D2 & EN & M0 & M1) ;
            Y2 :=    !( !EN & !Y2
                     # EN & !M0 & !M1 & !Y1
                     # EN & M0 & !M1 & !Y3
                     # EN & !M0 & M1 & !Y1
                     # D1 & !D3 & EN & M0 & M1
                     # D0 & D2 & !D3 & EN & M0 & M1) ;
            Y3 :=    !( !EN & !Y3
                     # EN & !M0 & !M1 & !Y2
                     # EN & M0 & !M1 & !SOUT
                     # EN & !M0 & M1 & SOUT & Y3
                     # EN & !M0 & M1 & !Y2
                     # D0 & D3 & EN & M0 & M1
                     # D1 & D3 & EN & M0 & M1) ;
            INV =    !(CIF & !INV
```

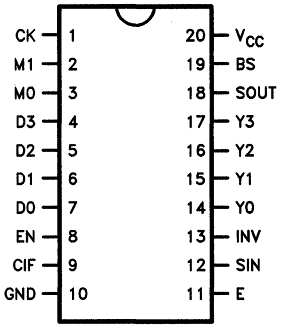
Figure 10

Document File (Continued)

```
                                                                    Page 1
ABEL™ VERSION 1.10 - Document Generator                             17 Sept-85 8:30 AM
PAL16R6                                 DESIGN EXAMPLE                  FILENAME: GCREX.PAL
PAT001                                                      BRUCE WENNIGER 9/17/85
4B-5B ENCODER/DECODER
CYPRESS SEMICONDUCTOR
-Translated by TOABEL-
Equations for Module --gcrext
Device P16R6
              # !CIF & !MO & M1 & !Y2 & !Y3
              # !CIF & !MO & M1 & !YO & !Y1 & !Y3
              # !CIF & !MO & M1 & !SOUT & !YO
              # !CIF & !MO & M1 & SOUT & YO & Y1 & Y2 & Y3);
       BS = !(SOUT & YO & Y1 & Y2 & Y3);
Chip diagram for Module --gcrext
Device P16R6
```

Figure 10 (Continued)

PAL C 16R6


CK 1
M1 2
MO 3
D3 4
D2 5
D1 6
DO 7
EN 8
CIF 9
GND 10
20 VCC
19 BS
18 SOUT
17 Y3
16 Y2
15 Y1
14 YO
13 INV
12 SIN
11 E
0060-15

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end of module --gcrext
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JEDEC File

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ABEL™ Version 1.10 JEDEC file for: P16R6
Created on: 17-Sept-85 8:30 AM
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PAT001                              BRUCE WENNIGER 9/17/85
4B-5B ENCODER/DECODER
CYPRESS SEMICONDUCTOR
-Translated by TOABEL-*
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Figure 11

JEDEC File (Continued)

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Figure 11 (Continued)

CYPRESS
SEMICONDUCTOR

Understanding FIFOs

Introduction

FIFO is an acronym for First-In-First-Out.

In digital electronics, a FIFO is a buffer memory that is organized such that the first data entered into the memory is also the first data removed from the memory.

History of FIFOs

Software FIFOs

Software FIFOs have been (and are being) used extensively in computer programs where tasks are placed in queues waiting for execution. In the programmers' language the program (process) that puts data into the memory is a "producer" and the program that takes data out is a "consumer". Obviously the producer and the consumer cannot access the memory simultaneously. It is the responsibility of the programmer to insure that contention does not occur. Data transfer via a shared memory is a standard programming technique but it is not feasible to have the processor in the data path for data rates greater than 5 Megabytes per second (MB/s). For higher data rates DMA, FIFO, or some combination of the two techniques are used to transfer information.

Hardware FIFOs

In the design of systems, once procedures are standardized and verified in software, the software can be replaced with hardware. The benefits of doing this are improved performance, reduced software, ease of design and usually reduced costs.

Register Array

The first hardware FIFOs were of the "register array" architecture and included the serializer/deserializer (SERDES) within the IC. As they evolved, and due to the ubiquitous microprocessor, the parallel input and parallel output configuration became the standard. For applications that required SERDES users added external shift registers.

The method of transferring data from one register to another is called a "bucket brigade". The transfer is controlled by a "valid data" bit (one per word) that designates which words have been written into but not yet read from and combinatorial control logic. The time for this logic to propagate a word of data from the input to the output of an initially empty FIFO is called "fallthrough time".

Dual Port Ram

The "second generation" of FIFOs are of the "dual port RAM" architecture. In order to achieve truly independent, asynchronous operation of inputs and outputs, the capability to read and write simultaneously must be designed into the basic memory cell.

The fallthrough time present in the register array organization is eliminated by the RAM architecture. However, the RAM must be (internally) addressed, which requires two pointers. One points to the location to be written into and the other points to the location to be read from. In addition, a bit is required for every FIFO word to designate which words have been written to but not yet read.

Applications

FIFOs are used as building blocks in applications where equipment that are operating at different data rates must communicate with each other, i.e., where data must be stored temporarily or buffered.

These include:

- Word processing systems
- Terminals
- Communications systems; including Local Area Networks
- EDP, CPU, and peripheral equipment; including disk controllers and streaming tape controllers

The Ideal FIFO

The characteristics of an ideal FIFO are:

INPUTS

- Infinitely variable input frequency (0 to infinity)
- Infinitely variable input handshaking signals

OUTPUTS

- Infinitely variable output frequency
- Infinitely variable output handshaking signals

The Ideal FIFO (Continued)

BOTH

- Inputs and outputs are completely independent and asynchronous to each other, except that over-run or under-run are not possible.

STATUS INDICATORS

- Full/empty
- One-half full, $1/4$ full, $1/4$ empty

LATENCY

- The latency should be zero. In other words, the data should be available at the FIFO outputs as soon as it is written. In the empty condition this would be the next cycle.

EXPANSION

- Expandable word length and depth without external logic and without performance degradation.

NO FALLTHROUGH OR BUBBLETHROUGH TIME

Analysis of Present Architectures

Register Array

The first Integrated Circuit FIFOs were an extension of the simplest FIFO of all; a serial shift register.

Input Stage

As illustrated in *Figure 1*, the input stage is a one word by m-bit parallel shift register that is under control of the input handshaking signals SI (Shift In) and IR (Input Ready).

Output Stage

The output stage is also a one word by m-bit parallel shift register that is under control of the output handshaking signals OR (Output Ready) and SO (Shift Out).

Register Array

The middle N-2 X m-bit registers are controlled by signals derived from the preceding control signals.

Valid Data

A flag bit is associated with each word of the FIFO in order to tell whether or not the data stored in that word is valid. The usual convention is to set the bit to a one when the data is written and to clear it when the data is read.

Fallthrough and Bubblethrough

The preceding statements regarding input and output stages are not precisely correct under two special conditions, which occur when the FIFO is empty and full:

EMPTY CONDITION - FALLTHROUGH

In the empty condition the data must enter the input stage and propagate to the output stage. This is called Fallthrough time and it limits the output data rate.

FULL CONDITION - BUBBLETHROUGH

When the FIFO is full and one word is read, all of the remaining words must move down one word (or the empty word must propagate to the input). This is called Bubblethrough time and it limits the input data rate.

As we shall see, Bubblethrough time and Fallthrough time are usually equal because the same logic is used.

Dual Port RAM Architecture

The dual port RAM architecture refers to the basic memory cell used in the RAM. By adding read and write transistors to the conventional two transistor RAM cell, the read and write functions can be made independent of each other. Obviously this increases the size of the RAM cell, but doing this is more than compensated for by simpler control logic and improved performance.

The RAM requires two address pointers; one to address the location where data is to be written and the other to address where data is to be read. Comparators are used to sense the empty and full conditions and control logic is required to prevent over-run and under-run.

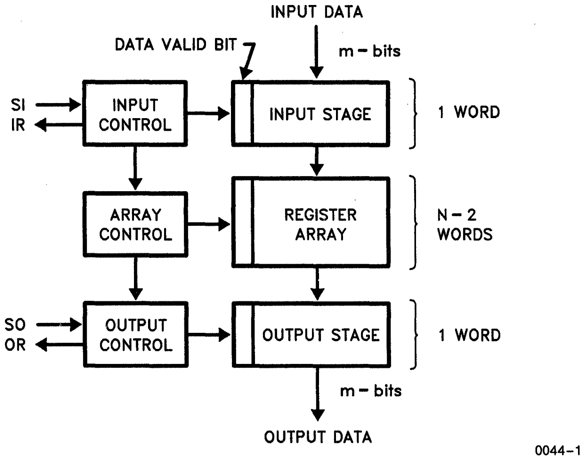


Figure 1. Register Array Architecture

Analysis of FIFOs

The procedure will be to first analyze the FIFO as a "black box" and then to compare the most important characteristics of a class of representative FIFOs with the characteristics of the CY7C401 FIFO.

The class of FIFOs chosen is the industry standard XXX401A and XXX402A that are available from several sources. The 401 is 64 x 4 and the 402 is 64 x 5 with the same performance. Both are of the register array architecture. Both are expandable in depth (number of words), which is called cascadeable, without additional logic as well as expandable in word width (number of bits per word) with additional logic. The operation will first be analyzed in the standalone configuration.

Functional Description

Data Input - Refer to *Figures 2, 3*

After power-on the Master Reset ($\overline{MR}$) input is pulsed LOW to initialize the FIFO. When the IR output goes high it signifies that the FIFO is able to accept data from the producer at the DI inputs. Data is entered into the input stage when the SI input is brought high (if IR is also high). SI going high causes IR to go low, acknowledging receipt of the data, which is now in the input stage.

When SI goes low (in response to IR going low) and if the FIFO is not full, IR will go back high, indicating that more room is available in the FIFO. At the same time SI goes low data is propagated to the next empty location, which may be the second location, but could be any location up to but not including the output stage.

Data Output - Refer to *Figures 4, 5*

Data is read from the DO outputs of the output stage under control of the SO and OR handshaking signals. The high state of OR indicates to the consumer that valid data is available at the outputs. When OR is high, data may be shifted out by bringing the SO line high (request), which causes the OR line to go low (acknowledge). Valid data is maintained on the outputs as long as SO is high. When SO goes low (in response to OR going low) and if the FIFO is not empty, OR will go back high, indicating that there is new valid data at the outputs. If the FIFO is empty OR will remain low and the data on the outputs will not change.

Empty/Full

If the FIFO is empty, OR will not go high within a fall-through time after SO goes low, so this condition may be sensed and used to indicate EMPTY.

Similarly, if the FIFO is full, IR will not go high within a bubblethrough time after SI goes low, so this condition may be sensed and used to indicate FULL.

Standalone Operation

Input Data Setup and Hold

The input data must be stable for an amount of time equal to the setup time (t_{IDS}) before the rising edge of SI and

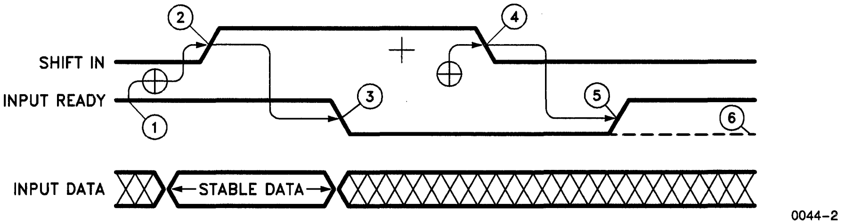


Figure 2. Method of Data Input

Notes:

Shift in pulses applied while Input Ready is LOW will be ignored.

⊕ External "producer" response time.

+ SI pulse could be of fixed positive duration and would then not depend upon response time of producer.

① Input Ready HIGH indicates space is available and a Shift in pulse may be applied.

② Input Data is loaded into the first word.

③ Input Ready goes LOW indicating the first word is full.

④ The Data from the first word is released to propagate to the second word.

⑤ The Data from the first word is transferred to the second word. The first word is now empty as indicated by Input Ready HIGH.

⑥ If the second word is already full then the data remains at the first word. Since the FIFO is now full, Input Ready remains low.

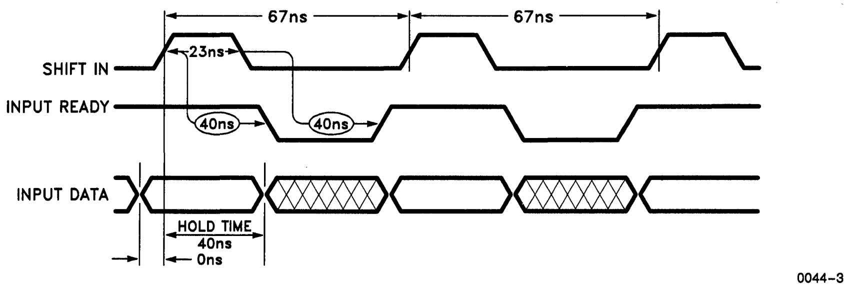
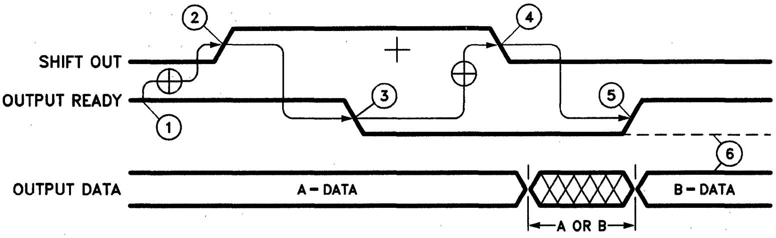


Figure 3. Input Timing for FIFO

Analysis of FIFOs (Continued)

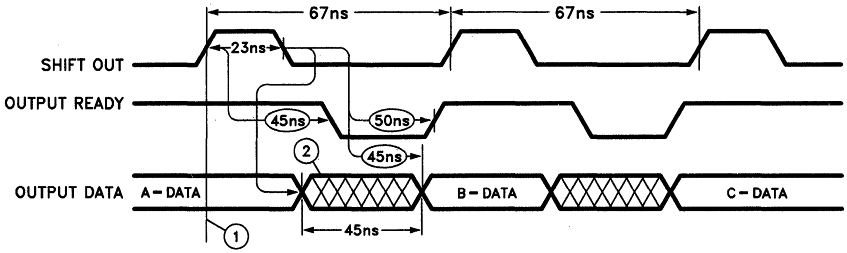


0044-4

Figure 4. The Method of Shifting Data Out of the FIFO

Notes:

- ⊕ External "consumer" response time.
- + SO pulse could be of fixed positive duration and would then not depend upon response time of consumer.
- ① Output Ready high indicates that data is available and a Shift Out pulse may be applied.
- ② Shift Out goes high causing the next step.
- ③ Output Ready goes LOW.
- ④ Contents of word 52 (B-DATA) is released to propagate to word 53.
- ⑤ Output Ready goes high indicating that new data (B) is now available at the FIFO outputs.
- ⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



0044-5

Figure 5. Output Timing for Register Array FIFO

Notes:

- ① The diagram assumes that, at this time, words 63, 62, 61 are loaded with A, B, C Data respectively.
- ② Data in the crosshatched region may be A or B Data.

remain stable for an amount of time equal to the hold time (t_{IDH}) after the rising edge of SI.

$t_{IDS} = 0$ ns

$t_{IDH} = 40$ ns

Input Timing

Figure 3 shows the timing relationships between the input data and the handshaking signals when operating at the maximum input data rate of 15 MHz. The Input Ready signal lags (follows) the rising edge of the Shift In signal by 40 ns (max.) for this two edge handshake.

Fallthrough Time

Figure 2 shows the method of entering data into the FIFO. The fallthrough time (*Figure 6*) is measured from the falling edge of the SI signal to the rising edge of the IR signal. For a 15 MHz Register Array FIFO, this time is specified as $t_{PT} = 1.6\ \mu s$ (microseconds).

Register Array Propagation Delay Time

The register array propagation delay time may be approximated by using the delay from the falling edge of the SO signal to the rising edge of the OR signal as being representative of the data propagation delay through the output stage and subtracting this from the fallthrough time.

$$\text{Reg. Prop. Delay} = \text{Fallthrough time} - \text{Output Prop. Delay Time}$$

The delay per stage is then calculated by dividing the register array propagation delay time by the number of stages the data propagates through.

$$\text{Reg. Prop. Delay} = 1.6\ \mu s - 50\ \text{ns} = 1.55\ \mu s$$

$$\text{Delay per stage} = \frac{1.55\ \mu s}{64 - 2} = 25\ \text{ns}$$

Analysis of FIFOs (Continued)

Output Timing

Figure 5 shows the timing relationships between the output data and handshaking signals when operating at the maximum output data rate of 15 MHz. The Output Ready signal lags the Shift Out signal by 45 ns (max.) for this two edge handshake. Data is shifted to the output stage on the falling edge of SO, but does not stabilize until 45 ns later. OR goes low in response to SO going high (45 ns later) and then goes back high 50 ns (max) after the high to low transition of SO.

The reader may assume that the (new) output data is valid 50 – 45 = 5 ns before the rising edge of the OR signal, but this is incorrect. The data sheet specifies these two numbers only as maximums and not also as minimums. Evaluation of these FIFOs has revealed that the data may change several nanoseconds AFTER the rising edge of the OR signal.

The consumer is responsible for delaying the rising edge of the SO signal in order to satisfy his data setup time requirements, which may further reduce the throughput.

Full Condition

The maximum propagation delay from SI going low until IR goes high is 40 ns (*Figure 3*). The bubblethrough time for the full condition is illustrated in *Figure 7*. This time, t_{PT}, is specified as 1.6 μs on the data sheet. The delay per stage is calculated by subtracting 40 ns from 1.6 μs and dividing by the number of stages (64 − 2).

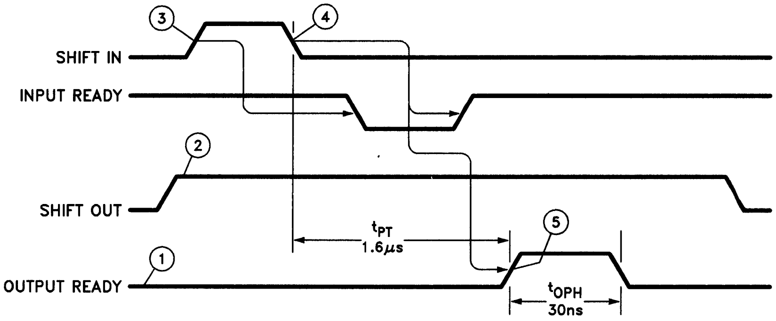
$$\text{Delay per stage} = \frac{\text{Bubblethrough time} - \text{Output Delay time}}{\text{Number of stages}}$$

$$= \frac{1.6\ \mu\text{s} - 0.04\ \mu\text{s}}{64 - 2}$$

$$= 25.16\ \text{ns}$$

Bubblethrough Time

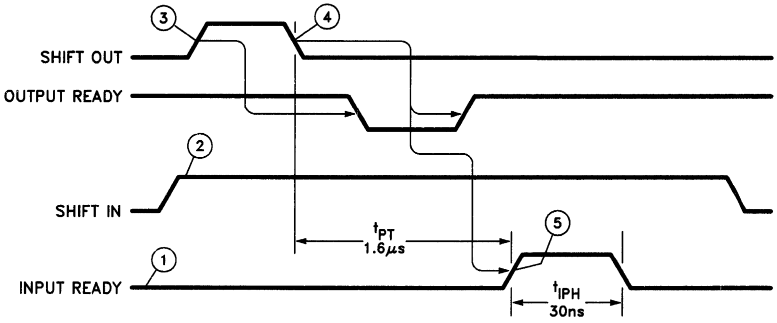
The bubblethrough timing is illustrated in *Figure 7*. It is seen to be equal to the fallthrough time.



0044-6

Figure 6. Fallthrough Timing

Notes:
① FIFO initially empty.
② Consumer requests data.
③ Producer enters data.
④ Data enters internal register array.
⑤ Data is available at output.



0044-7

Figure 7. Bubblethrough Timing

Notes:
① FIFO is initially full.
② Shift In held HIGH.
③ Consumer reads data.
④ Empty location begins to propagate to input.
⑤ Empty location reaches input.

Analysis of FIFOs (Continued)

Maximum Throughput Calculations

The maximum throughput of the FIFO is seen to be limited by the fallthrough time when it is empty and the bubblethrough time when it is full.

The "throughput period" corresponding to the "standalone period" (t_A) and the fallthrough time (t_F) is:

$$T_{max.} = t_A + t_F$$

Converting to frequency yields

$$\frac{1}{F_{max.}} = \frac{1}{F_A} + t_F$$

Rearranging and solving for F_{max} yields

$$F_{max} = \frac{1}{\frac{1}{F_A} + t_F} \qquad \text{EQ. 1}$$

The expressions for the throughput frequencies for the FIFO under the full and empty conditions are then;

EMPTY FIFO

$$F_{in} = F_{in\,(max.)}$$

$$F_{out} = \frac{1}{\frac{1}{F_A} + t_F}$$

FULL FIFO

$$F_{out} = F_{out\,(max.)}$$

$$F_{in} = \frac{1}{\frac{1}{F_A} + t_F}$$

The maximum throughput that can be handled by a "nearly empty" or a "nearly full" FIFO operating in the standalone mode is then:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + t_F}$$

$$F_{(max.)} = \frac{1}{\frac{1}{15\text{ MHz}} + 1.6\ \mu\text{s}} = \frac{1}{1.667\ \mu\text{s}}$$

$$F_{(max.)} = 599.88\text{ kHz}$$

Note that this is considerably less than the 15 MHz specified on the data sheet.

FULLNESS SENSITIVITY (STANDALONE)

The number of words written into the FIFO corresponding to the fallthrough time if the input data rate is at the maximum (15 MHz) is:

$$\frac{F_{in}}{F\text{ fallthrough}} = \frac{15\text{ MHz}}{\frac{1}{1.6\ \mu\text{s}}} = 24\text{ words.} \qquad \text{EQ. 2}$$

Since the bubblethrough time is the same as the fallthrough time (in this case) the same number of words can be output at the maximum data rate from a full FIFO.

What this means is that the FIFO can operate at its maximum data rate (15 MHz) only when it is between 24 words and 64 − 24 = 40 words full. In order to NOT be sensitive to its fullness, the FIFO must be operated at a maximum frequency less than or equal to the frequency corresponding to the fallthrough/bubblethrough time (625 KHz).

Cypress proposes defining a Fullness Sensitivity (FS) figure of merit for FIFOs that is a measurement of the capacity range (or fullness) over which the FIFO can be operated at its maximum input rate AND its maximum output rate. The FS is normalized; one (1) is ideal and 1 > FS > 0.

$$FS = \frac{N - F_{IA}\,t_F - F_{OA}\,t_B}{N} \qquad \text{EQ. 3}$$

Where: FS = Fullness Sensitivity
N = The number of words in the FIFO
F_{IA} = Standalone maximum input frequency
t_F = Fallthrough time
F_{OA} = Standalone maximum output frequency
t_B = Bubblethrough time

As an example we will calculate FS for a typical register array FIFO.

$$F_{IA} = F_{OA} = 15\text{ MHz}$$

$$t_F = t_B = 1.6\ \mu\text{s}$$

$$N = 64\text{ words}$$

$$FS = \frac{64 - 15\times10^6\times1.6\times10^{-9} - 15\times10^6\times1.6\times10^{-9}}{64}$$

$$FS = \frac{64 - 24 - 24}{64}$$

$$FS = 0.25$$

If the partial products would have had fractional parts we would have rounded them up to the next highest integers.

FIFO Expansion

The interconnection of two 64 word FIFOs to form a 128 x 4 FIFO is shown in *Figure 8*. Observe that the OR output of the first FIFO becomes the SI input of the second FIFO and that the IR of the second becomes the SO input to the first.

What this means is that the bubblethrough/fallthrough times serially add when the FIFOs are cascaded.

The maximum throughput that can be handled by two FIFOs cascaded together is:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + 2\,t_F}$$

$$F_{(max.)} = 306\text{ KHz}$$

Where, as before, F_A = 15 MHz, t_F = 1.6 μs.

Analysis of FIFOs (Continued)

In general, when N FIFOs are cascaded together, the maximum throughput of the combination is:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + N\,t_F} \qquad \text{EQ. 4}$$

The FS is also affected by the cascading of FIFOs. If N FIFOs are cascaded together the number of words that can be output or input is N times that of the standalone condition.

$$\frac{F_{in}}{F\ \text{fallthrough}} = \frac{F_A}{\frac{1}{N\,t_F}} \qquad \text{EQ. 5}$$

If this number is greater than the actual (physical) FIFO depth it means that the FIFO cannot be operated at its maximum frequency.

To make a wider word, as well as a deeper FIFO, connect the FIFOs as illustrated in *Figure 9*. Composite IR and OR signals must be generated using two external AND gates (e.g., 74LS08) to compensate for variations in the propagation delay of these signals from device to device. The maximum throughput for this configuration is 205 KHz (N = 3 in preceding formula).

Cascadability Considerations

In order to guarantee the ability of multiple FIFOs to reliably cascade with each other using the handshaking method previously described, certain conditions must be met. These are now considered.

SI or OR Signal Compatability

In the cascaded configuration, the OR signal of the Nth FIFO must be specified such that it can be detected when it is applied to the SI input of the N+1th FIFO. See *Figure 8*. This means that the minimum high time (positive pulse width) of the OR output signal of the input FIFO must be able to be recognized at the SI input of the output FIFO.

IR and SO Signal Compatability

In the cascaded configuration, the IR output of the N+1th FIFO must be specified such that it can be detected when it is applied to the SO input of the Nth FIFO.

Minimum Delay Between SI and IR

The minimum delay between SI going HIGH and IR going LOW is an unspecified parameter in the industry standard

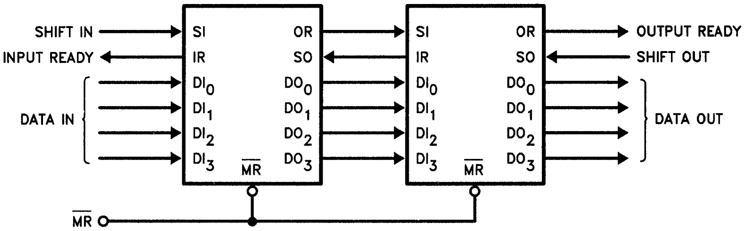

SHIFT IN
INPUT READY
DATA IN
SI
IR
DI0
DI1
DI2
DI3
MR
OR
SO
DO0
DO1
DO2
DO3
OUTPUT READY
SHIFT OUT
DATA OUT
MR
0044-8

Figure 8. 128 x 4 FIFO

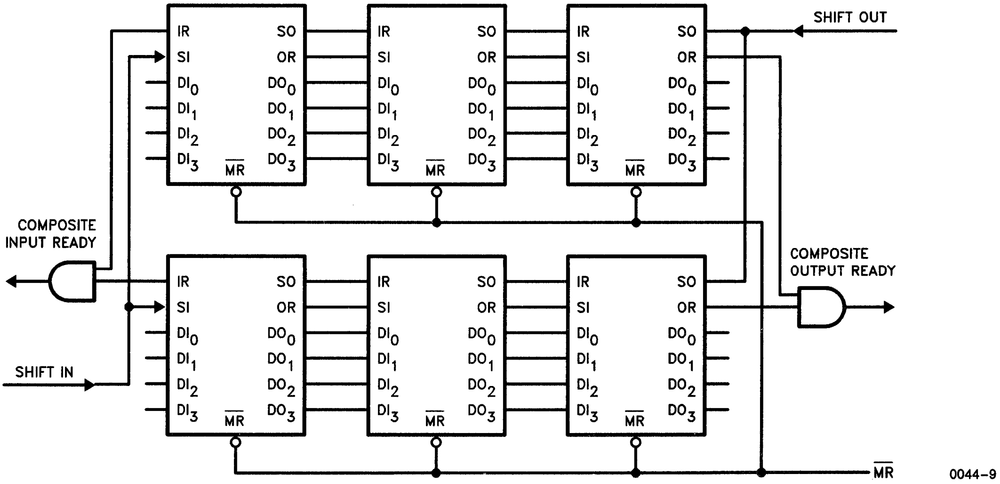

SHIFT OUT
IR
SI
DI0
DI1
DI2
DI3
MR
SO
OR
DO0
DO1
DO2
DO3
COMPOSITE INPUT READY
SHIFT IN
COMPOSITE OUTPUT READY
MR
0044-9

Figure 9. 192 x 8 FIFO

Analysis of FIFOs (Continued)

data sheets. The Cypress FIFO exhibits a 6 to 10 ns minimum delay. Care must be taken when mixing Cypress FIFOs and competitive FIFOs to insure that the parts will cascade with one another. In general, delaying the IR output of the Cypress FIFOs enables competitive parts to cascade with Cypress parts. The Cypress FIFO can always recognize the output of the competitive product.

Minimum Delay Between OR and SO

Another unspecified industry parameter is the delay between OR and SO. The minimum delay for Cypress FIFOs is 6 ns. A 500 pF capacitor added between the OR pin and ground and the IR pin and ground of all Cypress FIFOs will permit cascading with competitive FIFOs. These capacitors delay the signals the appropriate amount of time.

Cascading at the Operating Frequency

In order to operate at a given frequency, F_O, in the cascaded configuration the following relationship must be satisfied;

$$t_{SIH} + t_{IRH} < \frac{1}{F_O}$$

This condition is met by both the MMI and Cypress FIFOs.

Description of the CY7C401

A block diagram of the CY7C401 is shown in *Figure 10.* It is a direct, pin for pin, functional equivalent, improved performance, replacement for the register array FIFOs. The similarities and differences between the 401, 402, 403, and 404 are summarized in the table.

Product	Configuration	t_F	Package	Description
CY7C401	64 x 4	65 ns	16 pin DIP	Industry Standard
CY7C403	64 x 4	65 ns	16 pin DIP	Pin 1 is three-state output enable
CY7C402	64 x 5	65 ns	18 pin DIP	Industry Standard
CY7C404	64 x 5	65 ns	18 pin DIP	Pin 1 is three-state output enable

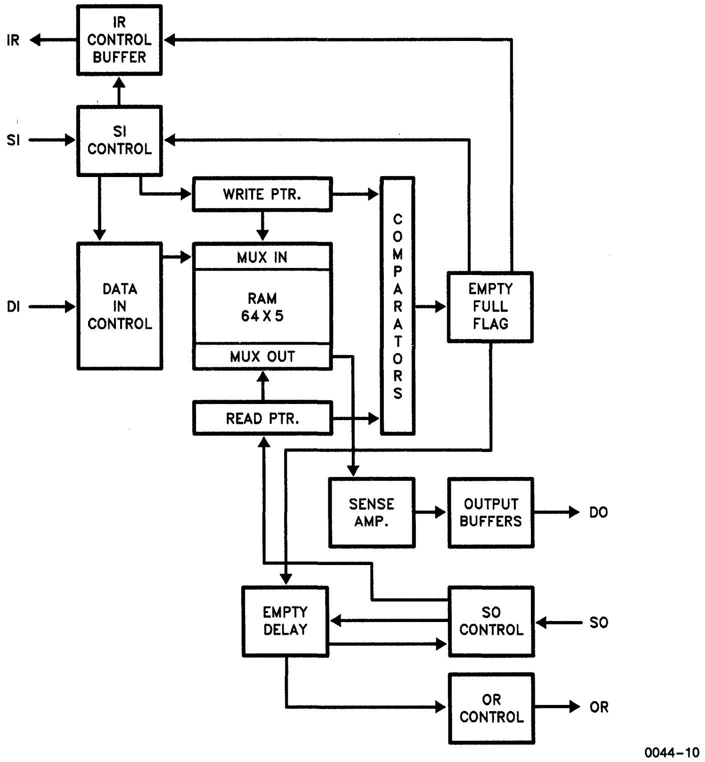

IR
IR CONTROL BUFFER
SI
SI CONTROL
WRITE PTR.
COMPARATORS
DI
DATA IN CONTROL
MUX IN
RAM 64 X 5
MUX OUT
EMPTY FULL FLAG
READ PTR.
SENSE AMP.
OUTPUT BUFFERS
DO
EMPTY DELAY
SO CONTROL
SO
OR CONTROL
OR
0044-10

Figure 10. CY7C401 Block Diagram

Description of the CY7C401 (Continued)

Architecture Refer to *Figure 10*

The architecture is that of a dual port RAM, which is accessed by two pointers; a read pointer and a write pointer. The input data and output data do not reside in input or output registers as in the register array architecture. Instead, the pointers address the memory locations of the input and output data. Comparators are used to control the IR and OR lines to prevent overflow and underflow. The key to this architecture is the dual port RAM cell, which is illustrated in *Figure 11*. It is only 1.2 square mils in area. Separating the read and write functions enables the memory cell to be read from and written to simultaneously and independently. This increases the basic cell size, but simplifies the overall architecture and improves the performance.

The bubblethrough time is greatly reduced (65 ns versus 1.6 μs) because it now represents the time required to update the pointers, not the time required for data to propagate through the memory array.

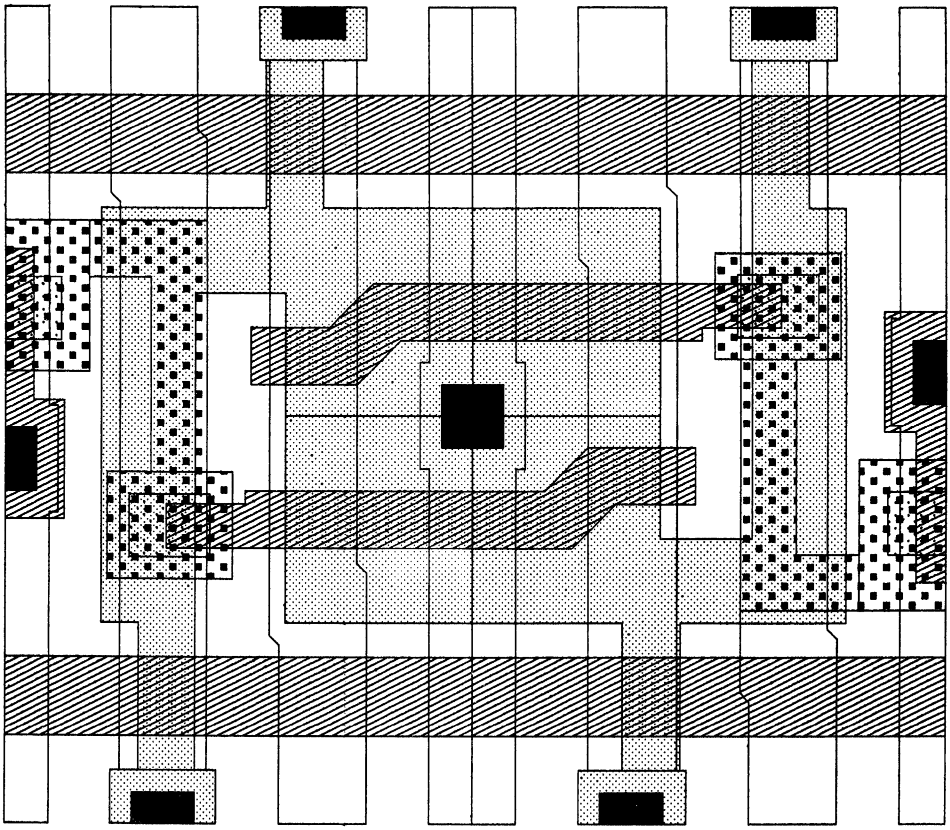
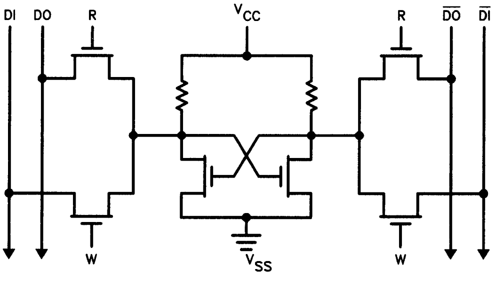

0044-11

Figure 11A. CY7C401 Ram Cell Layout



0044-12

Figure 11B. Cell Schematic

Description of The CY7C401 (Continued)

Functional Description

To the "outside world" the CY7C401 appears functionally equivalent to the register array FIFOs. All of the timing diagrams as well as the expansion diagrams of *Figures 8* and *9* apply.

Input data is sampled with the rising edge of the SI signal if the IR signal is high. The input (write) pointer is incremented on the falling edge of the SI signal.

Data is output with the falling edge of the SO signal if the OR signal is high. The output (read) pointer is incremented on the rising edge of the SO signal.

Output Timing

In the discussion on output timing it was pointed out that (for the register array FIFO) the way the timing of the data out with respect to OR, there is no guarantee that the data will be stable before the rising edge of OR. This time (t_{SOR}) is guaranteed to be a minimum of 5 ns on the CY7C401 data sheet.

Comparison of Register Array FIFOs and the CY7C401

Throughput

Using equation 4 the values in the following table were calculated and are plotted in *Figure 12.*

Fullness Sensitivity

Register Array FIFOs in the Standalone Mode

Equation 2 was used to calculate the number of words that could be input and output corresponding to the maximum frequency of 15 MHz. Subtracting these from the FIFO capacity (64) gives us the capacity range over which the FIFO can operate at its maximum rate. This was calculated to be between 24 and 40 words, or 32 ± 8 words. Equation 3 was used to calculate the FS and it was found to be 0.25.

Using equation 2 we have;

$$\frac{F_{in}}{F\ \text{fallthrough}} = \frac{F_A}{\frac{1}{t_F}}$$

$$= \frac{15\ \text{MHz}}{\frac{1}{67\ \text{ns}}} = 0.975\ \text{words}$$

The CY7C401 is seen to be much less sensitive to fullness than the register array FIFOs. Its capacity can range from 2 to 63 words, or 32 ± 31 words in the standalone mode.

The Fullness Sensitivities are plotted in *Figure 13.* They are also plotted in a slightly different form in *Figure 14.*

A little thought will convince the reader that Fullness Sensitivity is another way of quantifying the range of the difference between input and output data rates. The closer the FS is to 1 the greater the capacity of the FIFO to handle bursts of data.

Latency

The classic definition of latency is the difference, in elapsed time, between when a resource is requested and when it is granted. In disks, the worst case latency is the time required for one revolution of the disk. The average latency is then the time required for one-half a revolution. The assumptions are one head per track and no contention for the head.

Worst Case Latency - refer to *Figures 6* and *7*

The worst case latency for the consumer occurs when the FIFO is empty and for the producer when it is full. It is;

Where: $t_{in} + t_{out} + t_F$

t_{in} = period of the input frequency

t_{out} = period of the output frequency

t_F = Fallthrough time

Average Latency

If the FIFO is operated such that it is not sensitive to its fullness $t_F = 0$. In addition, if $t_{in} = t_{out}$ the average latency is one cycle. Otherwise, it is;

$$\frac{t_{in} + t_{out}}{2}$$

			Throughput		
	N	D	C67401A	CY7C401-5	CY7C401-25
F_A	—	—	15 MHz	15 MHz	25 MHz
t_F	—	—	1.6 μs	65 ns	65 ns
	1	64	600 KHz	7.57 MHz	9.52 MHz
	2	128	306 KHz	5.01 MHz	5.8 MHz
	4	256	155 KHz	3 MHz	3.3 MHz
	8	512	77.7 KHz	1.7 MHz	1.78 MHz
	16	1024	38.9 KHz	903 KHz	925.9 KHz
	32	2048	19.5 KHz	465.7 KHz	471 KHz

Comparison of Register Array FIFO's and the CY7C401 (Continued)

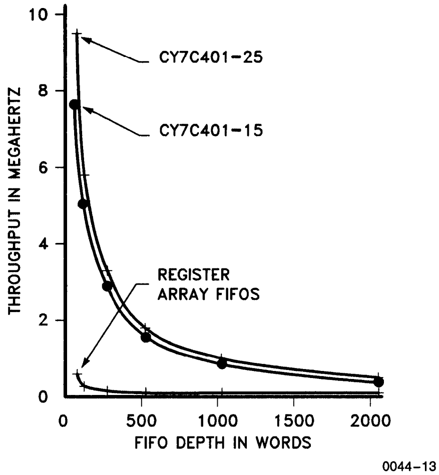


Figure 12. Maximum FIFO Throughput vs. Depth

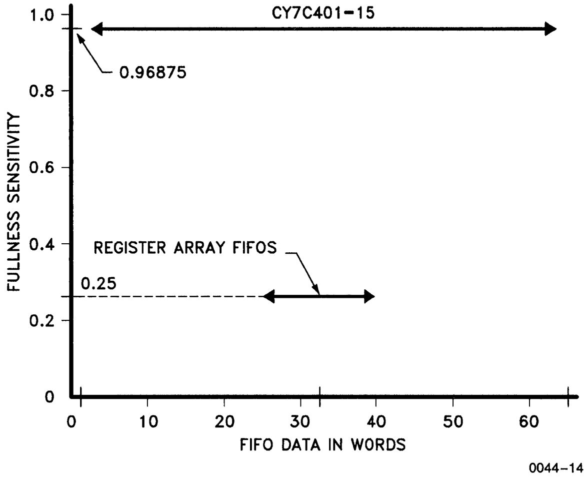


Figure 13. Fullness Sensitivity in the Standalone Mode

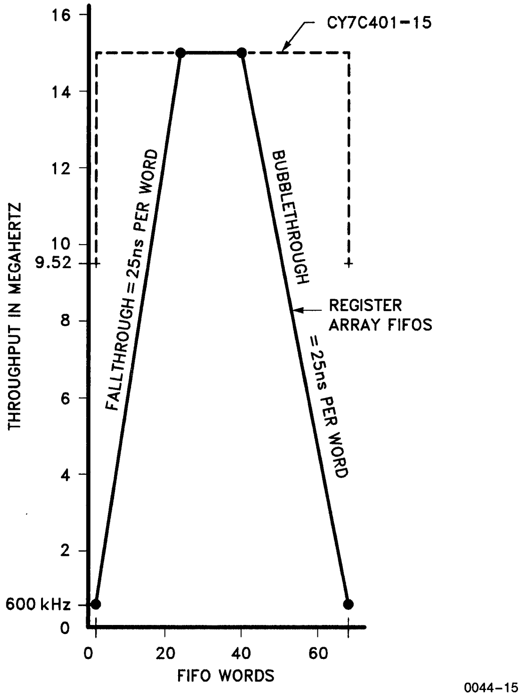


Figure 14. Standalone Throughput

Summary and Conclusions

In most systems where FIFOs are used they are neither full nor empty, except at the beginning or end of an operation. After analyzing the preceding two FIFOs the reader can understand why. Serious performance degradation occurs under these conditions, especially if the FIFO uses the register array architecture. To compensate for this, manufacturers have added one-half empty/full indicators (etc.), which has helped by alerting the system controller before the performance suffers.

A better solution to the performance problem is to use a FIFO that has the dual port RAM architecture, which has been shown to result in a superior performance FIFO.

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Interfacing to the FIFO Application Brief

Introduction

This application brief is intended to be a guide to the FIFO user and to make him aware of certain conditions that should be considered when interfacing to the FIFO. The two areas of concern are (1) voltage sensitivity on the SI and SO inputs and, (2) metastability when the SI or the SO signals are derived from independent clocks. These two issues are independent of each other.

High Gain Inputs

The minimum positive SI and SO pulse widths are specified on the FIFO data sheet as 11 ns (25 MHz SI/SO) and 20 ns (other speed grades). At room temperature and nominal (5V) V_{CC} the FIFO will operate reliably with SI/SO pulses as short as 5 ns. The reason these FIFOs respond to such short pulses is that the Cypress high performance CMOS process yields circuits that have very high gains and, consequently, require very little energy to change state.

Termination networks are recommended on the SI and SO lines (traces) on Printed Circuit Boards (PCBs) when the lines exceed seven inches in length (from source to load). The termination matches the load impedance to the characteristic impedance of the PCB trace, which is typically 50Ω or less for microstrip or stripline construction on G-10 glass epoxy material. For minimum voltage reflections a slightly overdamped termination is preferred. Cypress recommends a series capacitor of 10 pF and resistor of 47Ω be connected from the input pin (SI/SO) to ground as shown in *Figure 1*. This termination network acts as a low pass filter for short, high frequency pulses and dissipates no DC power. If more than one FIFO is connected in parallel to make a wider word only one termination network is required. It should be located at the input that is electrically the farthest away from the source.

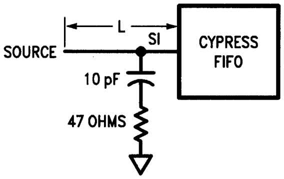
Synchronous And Asynchronous Operation

When the SI and SO signals are derived from a common frequency source (or clock) the FIFO is, by definition, operating in the synchronous mode. There is a precise, known relationship between the SI and SO signals.

Conversely, when the SI and SO signals are derived from two independent frequency sources, the FIFO is operating in an asynchronous mode.

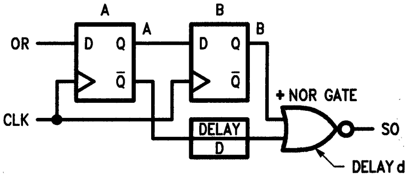
In the synchronous mode the designer can assure that the OR signal not occur within the setup and hold time window that normally "surrounds" the output system clock edge (or sampling signal). The same reasoning applies to the occurance of the IR signal with respect to the input system clock.

In the asynchronous mode, the designer cannot assure a known relationship between the OR signal and the output system clock either with respect to frequency or with respect to phase. It is the responsibility of the designer to insure that, even though the output system clock edge may occur at the same time that the OR signal occurs, the FIFO still receives a SO clock that is wide enough to be reliably recognized as such by the FIFO. The same reasoning applies to the SI signal that is generated in response to the IR signal under control of the input system clock.



0097-1

Figure 1. Recommended Termination Network



0097-2

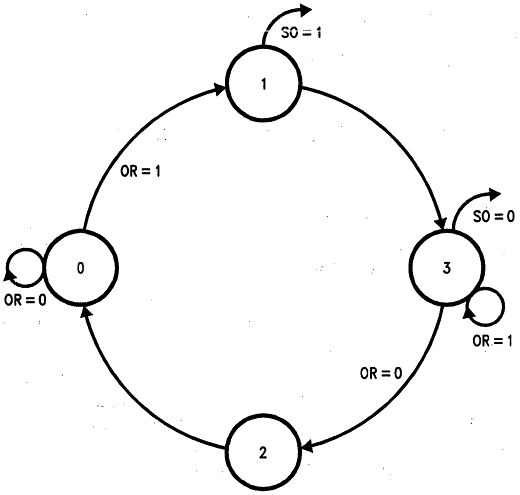
Figure 2. Pulse Synchronizer

Pulse Synchronizer

The circuit of *Figure 2* is recommended to generate the SO pulse as a function of OR under control of the output system clock. An identical circuit should be used to generate the SI pulse as a function of IR under control of the input system clock. If it is required to perform control functions on the OR or the IR signals, it should be done before they are clocked by the first D flip-flop.

State Diagram

The two stage shift register is analyzed as a state machine in *Figure 3*. Other, more complex state machines can be designed, but the idea is the same; reliably generate a single pulse of a known minimum width for every OR or IR LOW to HIGH transition.



0097-3

Figure 3. Pulse Synchronizer State Diagram

Transition Table

A	B	STATE	DESCRIPTION
0	0	0	IDLE AT STATE 0
1	0	1	GENERATE SO = 1
1	1	3	GENERATE SO = 0
0	1	2	TRANSITION STATE

0097-4

Design Considerations

The frequency of the clock to the pulse synchronizer should be at least twice that of the maximum rate data is shifted into or out of the FIFO.

For example, if it is required to shift data into the FIFO at a 10 MHz (SI) rate, the clock to the input pulse synchronizer should be 20 MHz. If it is required to shift data out of the FIFO at a 15 MHz (SO) rate the clock to the output pulse synchronizer should be 30 MHz.

Minimum SI/SO Pulse Width

The minimum pulse width of the SO signal of *Figure 2* under normal operating conditions will be one cycle of the output clock (CLK). However, when the OR or the IR signal changes within the "unallowed window" around the clock edge, defined by the flip-flop setup time and hold time, the flip-flop may go into a metastable state. i.e., its outputs may be between the logic ONE and the logic ZERO voltage levels. The amount of time the flip-flop will stay in the metastable region will be approximately 4 X, where X = clock to output propagation delay time.

The minimum pulse width of the SO signal is determined by the delay, d, through the NOR gate, plus any delay the designer may add (D, shown as a box) in the path from the /Q output of the A flip-flop to the input of the NOR gate. The NOR gate acts as a low pass filter and will not pass a pulse if its width is less than d. Adding an external delay, D, increases the minimum pulse width to d + D. The maximum frequency that the circuit can operate at, assuming equal gate turn-on and turn-off times, is then

$$f\,(\text{max.}) = \frac{1}{2\,(d + D)}.$$

The total delay should be chosen such that the minimum pulse width is sufficient to reliably be detected by the FIFO.

Implementation Of The Delay

If only the NOR gate provides the delay, the following table lists typical and maximum propagation delays under nominal V_{CC} and loading (20 pF) conditions.

Table 1. Propagation Delay in ns

Family	Typical	Maximum
LS	10	15
ALS	5	11
HCMOS	8	23
FACT	5	9.5

A 74LS02 NOR gate will result in a minimum pulse width of 10 ns, which will reliably operate a 25 MHz CY7C403 or a CY7C404 FIFO.

If it is required to operate a 10 MHz CY7C401/402, the Q output of the A flip-flop may be inverted through a 74LS04 and applied to the lower input of the NOR gate. The minimum pulse width is then 10 + 10 = 20 ns.

A delay line or a RC network could also be used to delay the signal to the lower input of the NOR gate.

The circuit of *Figure 2* can also be used to synchronize the SI and SO inputs of the CY7C3341.

The rising edge of the SO signal should be used to sample the FIFO data.

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Power Characteristics of Cypress Products

Introduction

SCOPE AND PURPOSE

This document presents and analyzes the power dissipation characteristics of Cypress products. The purpose of this document is to provide the user with the knowledge and the tools to manage power when using Cypress CMOS products.

DESIGN PHILOSOPHY

The design philosophy for all Cypress products is to achieve superior performance at reasonable power dissipation levels. The CMOS technology, the circuit design techniques, architecture and the topology have been carefully combined in order to optimize the speed/power ratio.

SOURCES OF POWER DISSIPATION

Power is dissipated within the integrated circuit as well as external to it. Both internal and external power have a quiescent (or DC) component and a frequency dependent component. The relative magnitudes of each depend upon the circuit design objectives. In circuits designed to minimize power dissipation at low to moderate performance, the internal frequency dependent component is significantly greater than the DC component. In the high performance circuits designed and manufactured by Cypress, the internal frequency dependent power component is much less than the DC component. The reason for this is that a large percentage of the internal power is dissipated in linear circuits such as sense amplifiers, bias generators and voltage/current references that are required for high performance.

External Power Dissipation

The input impedance of CMOS circuits is extremely high. As a result, the DC input current is essentially zero (10 μA or less). When CMOS circuits drive other CMOS circuits there is practically no DC output current. However, when CMOS circuits drive either bipolar circuits or DC loads, external DC power is dissipated. It is standard practice in the semiconductor industry to NOT include the current from a DC load in the device I_{CC} specification. Cypress supports this practice. It is also standard practice to NOT include the current required to charge and discharge capacitive loads in the data sheet I_{CC} specification. Cypress also supports this standard practice.

Frequency Dependent Power

CMOS integrated circuits inherently dissipate significantly less power than either bipolar or NMOS circuits. In the ideal digital CMOS circuit there is no direct current path between V_{CC} and V_{SS}; in circuits using other technologies such paths exist and DC power is dissipated while the device is in a static state.

The principal component of power dissipation in a power-optimized CMOS circuit is the transient power required to charge and discharge the capacitances associated with the inputs, outputs, and internal nodes. This component is commonly called CV^2f power and is directly proportional to the operating frequency, f. The corresponding current is given by the formula

$$I_{CC}(f) = CVf.$$

The primary sources of frequency dependent power are due to the capacitances associated with the internal nodes and the output pins. For "regular" logic structures, such as RAMs, PROMs and FIFOs the internal capacitances are "balanced" so that the same delay and, therefore, the same frequency dependent power is dissipated independent of the location that is addressed. This is not true for programmable devices such as PALs because the capacitive loading of the internal nodes is a function of the logic implemented by the device. In addition, PALs and other types of logic devices may contain sequential circuits so the input frequency and the output frequency may be different.

The capacitance of each input pin is typically 5 pF, so its contribution to the total power is usually insignificant.

PAL® is a registered trademark of Monolithic Memories.

Introduction (Continued)

Derivation of Applicable Equations

The charge, Q, stored on a capacitor, C, that is charged to a voltage, V, is given by the equation;

$$Q = CV. \qquad \text{EQ. 1}$$

Dividing both sides of equation 1 by the time required to charge and discharge the capacitor (one period or T) yields;

$$\frac{Q}{T} = \frac{CV}{T} \qquad \text{EQ. 2}$$

By definition, current (I) is the charge per unit time and

$$f = \frac{1}{T}.$$

Therefore,

$$I = CVf. \qquad \text{EQ. 3}$$

The power (P = VI) required to charge and discharge the capacitor is obtained by multiplying both sides of equation 3 by V.

$$P = VI = CV^2f \qquad \text{EQ. 4}$$

It is standard practice to make the assumption that the capacitor is charged to the supply voltage (V_{CC}) so that

$$P = V_{CC}I = C\,[V_{CC}]^2f \qquad \text{EQ. 5}$$

The total power consumption for a CMOS integrated circuit is dependent upon:

- the static (quiescent or DC) power consumption.
- the internal frequency of operation
- the internal equivalent (device) capacitance
- the number of inputs, their associated capacitance, and the frequency at which they are changing
- the number of outputs, their associated capacitance, and the frequency at which they are changing

In equation form:

$$P_D = [(C_{IN})(F_{IN}) + (C_{INT})(F_{INT}) + (C_{LOAD})(F_{LOAD})]\,[V_{CC}]^2 + I_{CC}\,(\text{quiescent})\,V_{CC}. \qquad \text{EQ. 6}$$

The first three terms are frequency dependent and the last is not. This equation can be used to describe the power dissipation of every IC in the system. The total system power dissipation is then the algebraic sum of the individual components.

The relative magnitudes of the various terms in the equation are device dependent. Note that equation 6 must be modified if all of the inputs, internal nodes or all of the outputs are not switching at the same frequency. In the general case, each of the terms is of the form $C1\ F1 + C2\ F2 + C3\ F3 + \ldots Cn\ Fn$. In practical reality the terms are estimated using an equivalent capacitance and frequency.

Transient Power: Input Buffers and Internal

In the N-well CMOS inverter, the P-channel pullup transistor and the N-channel pulldown transistor (which are in series with each other between V_{CC} and V_{SS}) are never on at the same time. This means that there is no direct current path between V_{CC} and ground, so that the quiescent power is very nearly zero. In the real world, when the input signal makes the transition through the linear region (i.e., between logic levels) both the N-channel and the P-channel transistors are partially turned ON. This creates a low impedance path between V_{CC} and V_{SS}, whose resistance is the sum of the N-channel and P-channel resistances. These gates are used internally in Cypress products.

DC or Static Power

In addition to the conventional gates there are sense amplifiers, input buffers and output buffers, bias generators and reference generators that all dissipate power. The RAMs and FIFOs also have memory cells that dissipate standby power whether the IC is selected or not. The PROM and PAL® products have EPROM memory cells that do not dissipate as much standby power as a RAM cell.

Power Down Options

Five of the Cypress static RAMs have power down options that enable the user to reduce the power dissipation of these devices by approximately an order of magnitude when they are not accessed. The technique used is to disable or turn-off the input buffers and the sense amplifiers.

Worst Case Device Power Specifications

All Cypress products are specified with I_{CC} under worst, worst, worst case conditions. This means that the V_{CC} voltage is at its maximum (5.5V), the operating temperature is at its minimum, which is 0°C for commercial product and −55°C for military product and all inputs are at $V_{IN} = 2V$.

I_{CC} TEMPERATURE DEPENDENCE

For all Cypress products operating under all conditions, the I_{CC} current increases as the temperature decreases. The I_{CC} temperature coefficient is −0.12% per °C. To calculate the percentage change in I_{CC} from one temperature to another, this temperature coefficient is multiplied by the temperature difference.

If, for example, it is required to calculate the expected reduction in I_{CC} if either a commercial or a military grade Cypress IC is operated at room temperature (25°C), the calculations are:

For commercial products

$[0 - 25] \times [-0.12\%] = 3\%$ less I_{CC} at room temperature than at 0°C.

For military products

$[-55 - (25)] \times [-0.12\%] = 9.6\%$ less I_{CC} at room temperature than at −55°C.

Procedure

The procedure will be to develop a general purpose power dissipation model that applies to all of the Cypress CMOS products and to then present tables so that users can estimate typical and worst case power dissipations for each product. The data will be presented in chart form as functions of product type and capacitance, that is: SRAM, PROM, PAL or Logic; including FIFOs.

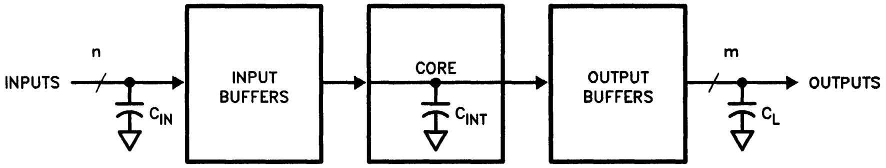

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Figure 1. Power Dissipation Model

Power Dissipation Model

A general purpose power dissipation model for all Cypress integrated circuits is shown in Figure 1.

The procedure will be to isolate the four components of power dissipation described by equation 6 by controlling the inputs to the IC. The quiescent (I_{CC}) current is measured with the inputs to the IC at 0.4V or less. Under this condition the input buffers and output buffers (unloaded DC wise) draw only leakage currents. All other direct currents are due to the substrate bias generator, sense amplifiers, other internal voltage or current references and NMOS memory circuits.

At $V_{IN} = 2.0V$ the input buffers draw maximum I_{CC} current. The total current is measured and the quiescent current subtracted to find the total input buffer I_{CC} current. The current per input buffer is then calculated by dividing the total input buffer current by the number of input buffers.

INPUT BUFFERS

Three different types of input buffers are used in Cypress products. For purposes of illustration they are referred to as types A, B and C. Table 1 lists which buffers are used on the various products.

Table 1. Types of Input Buffers

Buffer Type	I_{CC} (max. in mA)	Cypress Product
A	1.3	CY7C122
B	0.8	CY7C189/190 CY7C148/149 CY7C147 CY7C128/129 CY7C245 CY7C281/282 CY7C291/292 CY7C225 CY7C235 PAL16R8/16L8/16R6/16R4 CY7C401/402/403/404 CY3341
C	0.6	CY7C167/168/169, CY7C909/911/910/9101 CY7C510/516/517 CY7C261/263/264 CY7C268/269

The schematics and input characteristics for the three types of buffers are illustrated in Figure 2. A circle on the gate of a transistor means that it is a P-channel device.

As can be seen from the figure, the input buffers draw essentially zero I_{CC} current when V_{IN} is 0.4V or less or (except for type A) when V_{IN} is 4V or more. In other words, if the inputs are driven "rail to rail" the B and C input buffers will dissipate power only during the input signal transitions.

To reach these levels the input pins should be either driven by a CMOS driver or by a TTL driver whose output does not drive any other TTL inputs.

When the inputs are driven by the minimum TTL levels ($V_{IH} = 2V$, $V_{IL} = 0.8V$) each input buffer draws 20% more I_{CC} current than if it were driven rail to rail.

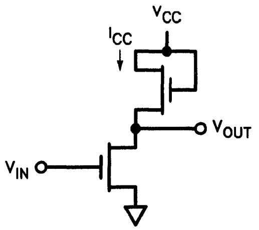

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Figure 2A

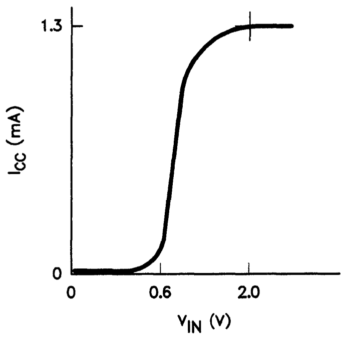

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Figure 2B
Type A

Power Dissipation Model (Continued)

DUTY CYCLE CONSIDERATIONS

The input characteristics of the type B (Figure 2D) and the type C (Figure 2F) buffers may be approximated by triangles symmetric about the $V_{IN} = 2V$ points, whose amplitudes are 0.8 mA and 0.6 mA, respectively. Therefore, between the $V_{IN} = 0.5V$ and $V_{IN} = 3.5V$ points the average current is one-half the peak current, or 0.4 mA and 0.3 mA, respectively. In most systems the input signal slew rates are one-half volt per nanosecond or greater so the input transitions occur quickly. Under these conditions the duty cycle of the input buffers must be considered.

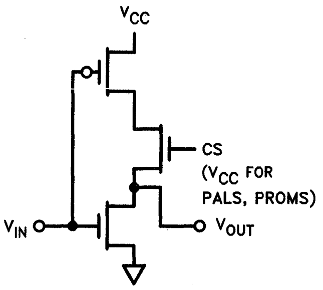

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Figure 2C

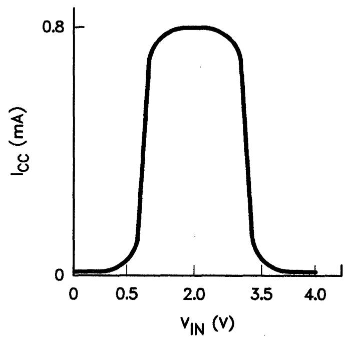

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Figure 2D
Type B

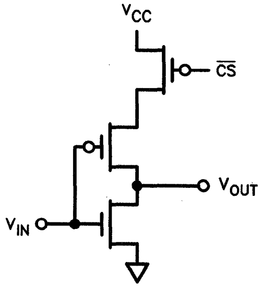

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Figure 2E

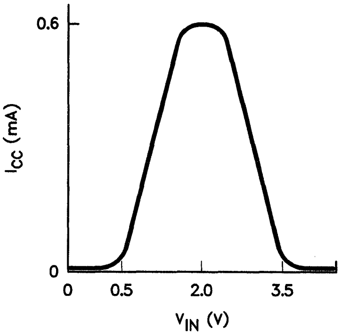

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Figure 2F
Type C

For example, if the CY7C167-35 RAM were used with input signals having a slew rate of one-half volt per nanosecond it would take

$$[3.5V - 0.5V] \times \frac{1}{0.5V/ns} = 6\text{ ns}$$

for the input signals to go through the 3V transition. During the transition each input buffer would be drawing 0.3 mA of current from the I_{CC} supply. However, this time is only 6 ns/35 ns = 0.17 or 17% of the access cycle. Therefore, the actual input buffer transient current is only 0.17×0.3 mA = 0.051 mA. It will be shown that this is insignificant in most power calculations.

INPUT BUFFER FREQUENCY DEPENDENT CURRENT

This is the current required to charge and discharge the capacitance associated with each input buffer. The capacitance is typically 5 pF and the voltage swing is typically 4V.

Using equation 3; $I = CVf$

$$I_{CC}(f) = 5 \times 10^{-12} \times 4 \times f.$$

$$I_{CC}(f) = 20 \times 10^{-12}f.$$

CORE AND OUTPUT BUFFERS

The memory core will have a standby power dissipation due to the substrate bias generator, reference generators, sense amplifiers, and polyload RAM cells or EPROM cells. This current is measured with $V_{IN} = 0V$, so that the input buffers draw no current. Under these conditions the output buffers will draw only leakage current and dissipate essentially no power.

The output buffers have N-channel pullup devices that cause the output voltage level to reach $V_{OH} = V_{CC} - 1V$.

The capacitance of the output buffers, including stray capacitance, is typically 10 pF.

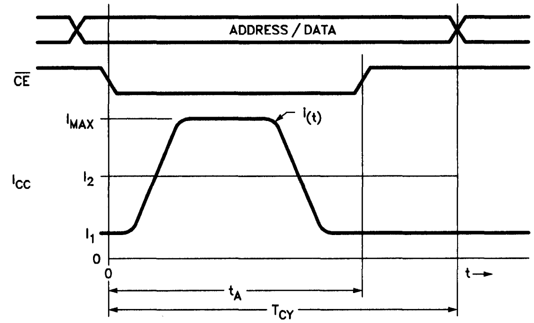
$$\text{IF } C_L = 10pF, V_{OH} \cong 4V.$$

Again, using equation 3, $I_{CC}(f) = 40 \times 10^{-12}f$ for the output buffers.

Current Measurement

INSTANTANEOUS CURRENT

Figure 3 illustrates the instantaneous current drawn by a Cypress RAM. The instantaneous power is calculated by multiplying this current times the constant supply voltage, V_{CC}. Most of the power is dissipated in the time corresponding to the access time. This is also true for PROMs and PALs.



I_1 = Quiescent I_{CC}
I_2 = Average I_{CC}
i(t) = Instantaneous I_{CC}

Figure 3. RAM I_{CC}

AVERAGE CURRENT

The current measurement unit in an automatic tester integrates the instantaneous current over the measurement cycle and arrives at an equivalent average current. In other words, the average current, I_2, during time TCY is equal to the area between the instantaneous current, i (t), and the X axis during TCY. Therefore, when the frequency is decreased, the "current pulse" is (figuratively) spread over a longer time, so the average current is proportionately less.

DC Load Current

Note that the preceding calculations have not accounted for any DC loads. The user must calculate these separately.

Product Characteristic Tables

The following tables are listed to enable the user to calculate the current requirements for Cypress products. C_{INT} is the equivalent device internal capacitance, I_{CC} (Q) is the quiescent or DC current and $I_{CC(MAX)}$ is the maximum I_{CC} current (as specified on the data sheet) for the commercial operating temperature range.

STATIC RAMs

Table 2

Part No.	No. Inputs	No. Outputs	C_{INT} (pF)	I_{CC} (Q) (mA)	$I_{CC(Max.)}$ (mA)
CY7C122	12	4	24	50	90
CY7C128/129	14	8	27	59	120
CY7C147	15	1	34	28	90
CY7C148/149	12	1	32	45	90
CY7C167	17	1	75	25	70
CY7C168/169	18	4	75	50	90
CY7C189/190	10	4	21	32	90

PROMs

Table 3

Part No.	No. Inputs	No. Outputs	C_{INT} (pF)	I_{CC} (Q) (mA)	$I_{CC(Max.)}$ (mA)
CY7C225	11	8	32	35	90
CY7C235	12	8	35	35	90
CY7C245	13	8	35	50	90
CY7C261/3/4	14	8	60	45	100
CY7C268/269	19/17	9	60	60	100
CY7C281/282	14	8	35	35	100
CY7C291/292	14	8	35	50	100

PALs

For the 16L8, 16R8, 16R6 and 16R4 the number of inputs and outputs is, within limits, user configurable.

Table 4

Part No.	C_{INT} (pF)	I_{CC} (Q) (mA)	$I_{CC(Max.)}$ (mA)
PALC16L8/R8/R6/R4	40	25	45
PLDC20G10	50	30	55
PALC22V10	50	40	80

LOGIC PRODUCTS

Table 5

Part No.	No. Inputs	No. Outputs	C_{INT} (pF)	I_{CC} (Q) (mA)	$I_{CC(Max.)}$ (mA)
CY7C401	6	6	53	30	75
CY7C402	8	7	53	30	75
CY7C403	7	6	53	30	75
CY7C404	8	7	53	30	75
CY7C510	—	—	60	30	100
CY7C516/517	—	—	60	30	100
CY3341	6	6	53	30	45
CY7C901	28/24	10/14	160	25	70
CY7C909	21	5	80	25	55
CY7C911	13	5	80	25	55
CY7C9101	—	—	70	30	85

The CY7C901 has four bi-directional I/O pins.

Static RAM Example

To illustrate how to use the preceding tables and perform the required calculations the following example is provided.

Estimate the typical I_{CC} current for the CY7C169-35 RAM at room temperature ($T_A = 25°C$) and $V_{CC} = 5V$. Assume the duty cycle is 100% at the specified access time. Calculate typical and worst case I_{CC} (all inputs and outputs changing) with output loading of 10 pF.

From the RAM product characteristic table;

# inputs = 18
# outputs = 4
C_{INT} = 75 pF
I_{CC} (Q) = 50 mA

Static RAM Example (Continued)

TRANSIENT INPUT BUFFER CURRENT

The input buffers on the CY7C169 are type C, so the average current is 0.3 mA. If the input signal level transitions are 4V and the transition times are 0.5 V/ns, the transition time is:

$$Tt = \frac{4V}{0.5\ V/ns} = 8\ ns.$$

The duty cycle is then;

$$8\ ns/35\ ns = 0.23.$$

Therefore, each input buffer draws

$$0.3\ mA \times 0.23 = 0.069\ mA.$$

If all inputs change, the total transient input buffer current is

$18 \times 0.069 = 1.24\ mA.$

CVf Input Buffer Current

$I = CVf \qquad C_{IN} = 5\ pF$
$I = 0.57\ mA \qquad V = 4V$
$f = 1/35\ ns$

Total $= 18 \times 0.57 = 10.28\ mA$

Internal CVf Current

$I = CVf \qquad C_{INT} = 75\ pF$
$I = 10.71\ mA \qquad V = 5V$
$f = 1/35\ ns$

Output CVf Current

$I = CVf \qquad C_{OUT} = 10\ pF$
$I = 1.15\ mA \qquad V = 4V$
$f = 1/35\ ns$

Total $= 4 \times 1.15 = 4.6\ mA$

The Quiescent Current is 50 mA

The Total Current At TCY = 35 ns is;

Input Transient	1.24 mA
Input CVf	10.28 mA
Internal CVf	10.71 mA
Output CVf	4.6 mA
Quiescent	50 mA
Total I_{CC}	78.83 mA (all inputs/outputs changing)

Note that the worst case transient current is 26.83 mA.

If one-half of the inputs and outputs change this is reduced to 13.4 mA, which gives a total current of 63.4 mA (typical I_{CC}).

If the duty cycle is 10% the transient current is reduced to 1.34 mA, which results in a total current of 51.34 mA.

Note also that the Input CVf current and the output CVf current would have the same values for a bipolar device.

WORST, WORST, WORST CASE I_{CC}

Next, let's estimate the I_{CC} for worst case V_{CC} and low temperature, in addition to all inputs and outputs changing and compare it with the I_{CC} specified on the data sheet.

The I_{CC} current will be greater at high V_{CC}, which is 5.5V or 1.1 × the nominal 5V V_{CC}. The increase in I_{CC} due to the lower temperature is 3%, so the total increase is 13%. These factors apply to the internal CVf current (10.71 mA), the output CVf current (4.6 mA), and the quiescent current (50 mA), (total 65.31 mA).

$$\text{Total } I_{CC} = \text{Input Transient } I_{CC} + \text{Input CVf } I_{CC} + [\text{Internal CVf} + \text{Output CVf} + I_{CC}(Q)] \times 1.13$$

$$I_{CC} = 1.24 + 10.28 + [65.31] \times 1.13 = 85.32\ mA.$$

This is approximately 95% of the 90 mA specified on the data sheet.

Note, however, that the data sheet I_{CC} maximum does NOT include the output CVf current.

Typical I_{CC} Versus Frequency Characteristic

The I_{CC} versus frequency curves for all Cypress products have the same basic shape, which is illustrated by the PAL 16R8 curve of Figure 4. The current remains essentially constant at the quiescent I_{CC} value until the frequency increases to the point where the capacitances begin to cause appreciable currents. This point depends upon the capacitances (input, internal, and output), the number of inputs and outputs, the rate at which they change, and the voltage levels that they are switched between. For Cypress products this point is in the 1–10 MHz range.

The PAL 16R8 devices that were tested to obtain the data for the curve were exercised such that all inputs and all outputs changed every cycle. Curve A shows the total I_{CC} current for a 50 pF load on each of the eight outputs. Curve B shows the total I_{CC} current when the outputs are disabled. The B curve results from the input and the internal capacitances. In most applications the actual operation of the device will be somewhere between the A and B curves.

The A and B curves may be extrapolated backwards until they intersect the quiescent current (point C in Figure 4).

Point C is approximately 5.6 MHz. This gives the user an easy to use approximate formula to calculate the I_{CC} current.

For frequencies less than 5.6 MHz

$$I_{CC} = I_{CC}(Q) = 25\ mA$$

For frequencies greater than 5.6 MHz

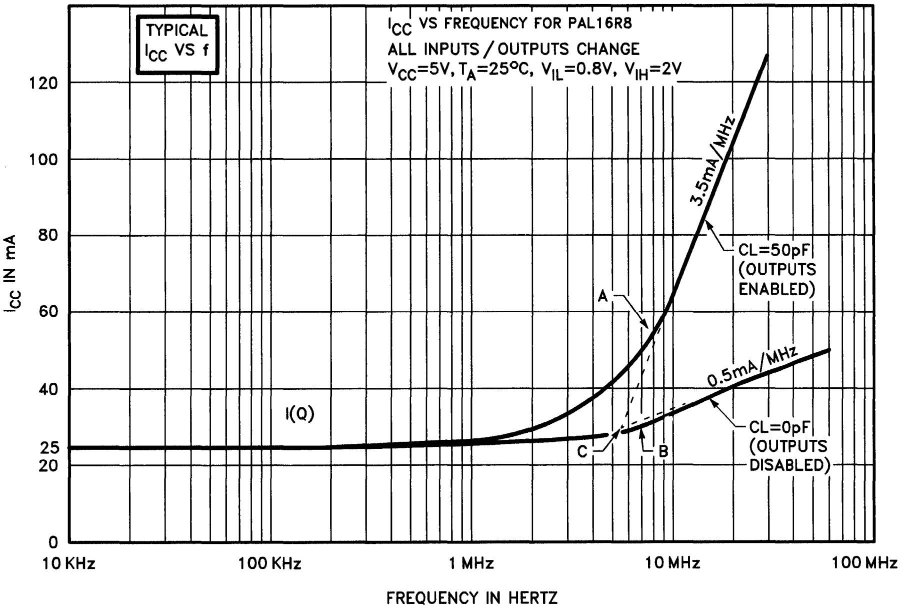
$$I_{CC} = I_{CC}(Q) + 3.5\ mA \text{ per MHz (all outputs changing)}$$

or,

$$I_{CC} = I_{CC}(Q) + 0.5\ mA \text{ per MHz (no outputs changing)}$$

TRANSIENT INPUT BUFFER CURRENT (Continued)

Frequency in Hertz



0059–9

Figure 4. Typical I_{CC} vs f

CYPRESS
SEMICONDUCTOR

Systems Design Considerations When Using Cypress CMOS Circuits

Introduction

This document is intended to be a guide for the systems designer. Its purpose is to make him aware of the things to consider either when designing new systems using Cypress high performance CMOS integrated circuits or when Cypress products replace either bipolar or NMOS circuits in existing systems. The two major areas of concern are transmission line effects due to impedance mismatching between the source and load, and device input sensitivity.

Design for Performance

In order to achieve maximum performance when using Cypress CMOS integrated circuits, the systems designer must pay attention to the placement of the components on the Printed Circuit Board (PCB), the routing of the metal traces that interconnect the components, the layout and decoupling of the power distribution system on the PCB and, perhaps most important of all, the impedance matching of (some of) the traces (which, under certain conditions, must be analyzed as transmission lines) between the source and the loads. The most critical traces are those of clocks, write strobes (on SRAMS), and chip enables.

Issues of Concern When Cypress ICs Replace Either Bipolar or NMOS ICs

Cypress CMOS ICs have been designed to replace both bipolar ICs and NMOS products, and to achieve equal or better performance at one-third (or less) the power of the components they replace.

When high performance Cypress CMOS circuits replace either bipolar or NMOS circuits in existing sockets, the user must be aware of certain conditions, which may be present in the existing system, that could cause the Cypress ICs to behave in a manner different than expected. These conditions fall into two general categories; (1) device input sensitivity and, (2) sensitivity to reflected voltages.

Input Sensitivity

High performance products, by definition, require less energy at their inputs in order to change state than low or medium performance products.

Unlike a bipolar transistor, which is a current sensing device, a MOS transistor is a voltage sensing device. In fact, a MOS circuit design parameter called K′ is analogous to the gm of a vacuum tube, and is inversely proportional to the gate oxide thickness.

The thin gate oxides, which are required to achieve the desired performance, result in highly sensitive inputs that require very little energy. High frequency signals that bipolar devices would not respond to may be detected by CMOS products.

MOS transistors also have extremely high (5 to 10 million ohm) input impedances, which make their gate inputs analogous to the input of a high gain amplifier (or an RF antenna). In contrast, bipolar ICs have input impedances of 1000Ω or less, so they require much more energy to change state than MOS ICs. In fact, a Cypress IC requires less than 10 picojoules of energy to change state.

Therefore, when Cypress CMOS ICs replace either bipolar or NMOS ICs in existing systems, they may respond to pulses of energy that are present in the system that are not detected by the bipolar or NMOS products.

Reflected Voltages

Cypress CMOS ICs have very high input impedances and, to achieve TTL compatibility and to drive capacitive loads, low output impedances. The impedance mismatch, due to low impedance outputs driving high impedance inputs may, under certain conditions, cause unwanted voltage reflections and ringing, which could result in less than optimum system operation.

When the impedance mismatch is very large, a nearly equal and opposite negative pulse is reflected back from the load to the source when the (electrical) length of the line (PCB trace) is greater than

$$\ell = \frac{T_R \text{ (ns)}}{2\,T_{pd} \text{ (ns/ft.)}}$$

where T_R is the rise time of the signal at the source and T_{PD} is the one-way propagation delay of the line per unit length.

The input clamping diodes that bipolar logic "IC families" (e.g., TTL, LS, ALS, FAST) all have are inherent in the fabrication process. The p-substrate is usually grounded and n wells are used for the NPN transistors and p type resistors. The wells are reverse biased by connecting them to the V_{CC} supply. As a result, a PN junction diode is formed between every input pin (cathode or n material)

Introduction (Continued)

and the substrate (anode or p-material). When a negative voltage occurs at an input pin, either due to lead inductance or to a voltage reflection, the diode is forward biased, turns on, and clamps the input pin to a Vf below ground (approximately $-0.8V$).

As circuit performance improved, the output rise and fall times of the bipolar circuits decreased to the point where voltage reflections began to occur (even for short traces) when there was an impedance mismatch between the line and the load. Most users, however, were unaware of these reflections because they were suppressed by the clamping action of the diodes.

Conventional CMOS processing results in PN junction diodes. However, they adversely affect the ESD (Electrostatic Discharge) protection circuitry at each input pin and cause an increased susceptibility to latchup. To eliminate this, a substrate bias generator is used.

Voltage reflections should be eliminated by using impedance matching techniques and crosstalk should be reduced by careful PCB layout.

Crosstalk

The rise and fall times of the waveforms generated by the output circuits are 2 to 4 ns between levels of 0.4V and 4V. The fast transition times and the large voltage swings could cause capacitive and inductive coupling (crosstalk) between signals if insufficient attention is paid to PCB layout. Crosstalk is reduced by avoiding running PCB traces parallel to each other. If this is not possible, ground traces should be run between signal traces. In synchronous systems, the worst time for the crosstalk to occur is during the clock edge with which the data is sampled. In most systems it is sufficient to isolate the clock and other data strobe lines so that they do not cause coupling to the data lines.

The Theory of Transmission Lines

A connection (trace) on a PCB should be considered as a transmission line if the wavelength of the applied frequency is short compared to the line length. If the wavelength of the applied frequency is long compared to the length of the line, conventional circuit analysis can be used.

In practice, transmission lines on PCBs are designed to be as nearly lossless as possible. As a result, the mathematics required for their analysis, compared to a lossy (resistive) line can be simplified.

Ideally, all signals between ICs travel over constant-impedance transmission lines that are terminated in their characteristic impedances at the load. In practice this ideal situation is seldom achieved for a variety of reasons.

Perhaps the most basic reason is that the characteristic impedances of all real transmission lines are not constants, but present different impedances depending upon the frequency of the applied signal. For "classical" transmission lines driven by a single frequency signal source the characteristic impedance is "more constant" than when the transmission line is driven by a square wave or a pulse.

A square wave is composed of an infinite set (Fourier series expansion) of discrete frequency components, i.e., fundamental plus odd harmonics of decreasing amplitudes. When the square wave is propagated down a transmission line the higher frequencies are attenuated more than the lower frequencies and, due to dispersion, all of the frequencies do not travel at the same speed.

Dispersion indicates the dependance of phase velocity upon the applied frequency. (Ref. 1, pg. 192). The result is that the square wave is distorted when all of the frequency components are added together at the load.

A secondary reason why practical transmission lines are not ideal is that they frequently (of necessity) have multiple loads. The loads may be distributed along the line at regular (or irregular) intervals or they may be lumped together (as close as practical) at the end of the line. The signal-line reflections and ringing caused by impedance mismatches, nonuniform transmission line impedances, inductive leads, and non-ideal resistors could compromise the dynamic system noise margins and cause inadvertent switching.

One of the system design objectives is to analyze the critical signal paths and design the interconnections such that adequate system noise margins are maintained. There will always be signal overshoot and undershoot. The objective is to accurately predict them and to keep them within acceptable limits.

The Ideal (Lossless) Transmission Line

An equivalent circuit for a transmission line is presented in *Figure 2.1.* It consists of subsections of series resistance (R) and inductance (L) and parallel capacitance (C) and shunt admittance (G) (or parallel resistance, R_P). For clarity and consistency these parameters will be defined per unit length. The value of the parameter (R, L, C, R_P) must be multiplied by the length of the subsection, ℓ, to find the total value. The line is assumed to be infinitely long.

If the line of *Figure 2.1* is assumed to lossless ($R = 0$, $R_P = \text{infinity}$) *Figure 2.1* is reduced to Figure 2.2.

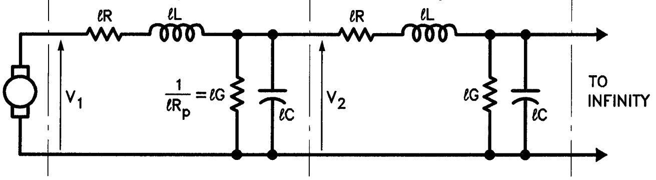


Figure 2.1. Transmission Line Model

The Theory of Transmission Lines (Continued)

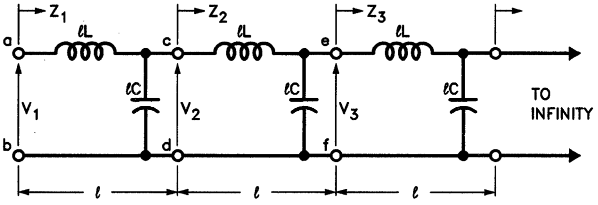


Figure 2.2. Ideal Transmission Line Model

Input or Characteristic Impedance

We shall now calculate the characteristic impedance (AC impedance or surge impedance) looking into terminals a-b of Figure 2.2.

Let the input impedance looking into terminals a-b be Z1, that looking into terminals c-d be Z2, that looking into terminals e-f be Z3, etc. The input impedance, Z1, looking into terminals a-b is the series impedance of the first inductor (ℓ L) in series with the parallel combination of Z2 and the impedance of the capacitor (ℓ C).

From AC theory:

$$XL = j\omega \ell L$$

Where XL is the inductive reactance.

$$XC = \frac{1}{j\omega \ell C}$$

Where XC is the capacitive reactance.

Then $$Z1 = XL + \frac{Z2\,XC}{Z2 + XC} \qquad (2\text{-}1)$$

If the line is "reasonably" long Z1 = Z2 = Z3. Substituting Z1 = Z2 into equation 2-1 yields;

$$Z1 = XL + \frac{Z1\,XC}{Z1 + XC}.$$

Or, $$Z1^2 - Z1\,XL - XC\,XL = 0 \qquad (2\text{-}2)$$

Substituting the expressions for XC and XL yields;

$$Z1^2 - j\omega \ell L = \frac{L}{C} \qquad (2\text{-}3)$$

Equation 2-3 contains a complex component that is frequency dependent. It can be eliminated by allowing ℓ to become very small and by recognizing that the ratio L/C is constant and independent of ℓ or ω.

$$Z1 = \sqrt{\frac{L}{C}} \qquad (2\text{-}4)$$

The AC input impedance of a purely reactive, uniform, lossless line is a resistance. This is true for AC or DC excitation.

Propagation Velocity and Propagation Delay

The propagation velocity (or phase velocity) of a sinusoid traveling on an ideal line (Ref. 1, pg. 33) is:

$$\alpha = \frac{1}{\sqrt{LC}}.$$

The propagation delay for a lossless line is the reciprocal of the propagation velocity.

$$T_{pd} = \sqrt{LC} \qquad (2\text{-}5)$$
$$= Z1\,C$$

where L and C are the intrinsic line inductance and capacitance per unit length.

If additional stubs or loads are added to the line the propagation delay will increase by the factor (Ref. 2, pg. 129).

$$\sqrt{1 + \frac{C_D}{C}}.$$

Where C_D = load capacitance.

Therefore, the propagation delay, T_{PD}', of a loaded line is:

$$T_{PD}' = T_{PD}\sqrt{1 + \frac{C_D}{C}}. \qquad (2\text{-}6)$$

The characteristic impedance of a capacitively loaded line is decreased by the same factor that the propagation delay is increased.

$$Z1' = \frac{Z1}{\sqrt{1 + \frac{C_D}{C}}} \qquad (2\text{-}7)$$

Reflection Coefficients

The third attribute of the ideal transmission line; reflection coefficients, are not actually a line characteristic. The line is treated as a circuit component (which it is) and reflection coefficients are defined that measure the impedance mismatches between the line and its source and the line and its load. The reason for defining the reflection coefficients will become apparent later when it will be shown that if the impedance mismatch is sufficiently large, either a negative voltage or a positive voltage may be reflected back from the load to the source, where it may either add to or subtract from the original signal. If the impedance of the source is mismatched to the line impedance it may also cause a voltage reflection, which in turn will be reflected back to the load. Therefore, two reflection coefficients will be defined.

For classical transmission lines driven by a single frequency source the impedance mismatches cause standing waves. When pulses are transmitted and the output impedance of the source changes depending upon whether a LOW to HIGH or a HIGH to LOW transition occurs, the analysis is further complicated. Classical transmission analysis,

The Theory of Transmission Lines (Continued)

where pulses are represented by complex variables with exponentials, could be used to calculate the voltages at the source and the load after several back and forth reflections. However, these complex equations tend to obscure what is physically happening.

Energy Considerations

Consider next, driving the ideal transmission line from a source capable of generating digital pulses and analyze the behavior of the line under various driving and loading conditions.

The circuit to be analyzed is illustrated in *Figure 2.3*. The ideal transmission line of length ℓ is being driven by a digital source of internal resistance R_S and loaded with a resistive load of RL. The characteristic impedance of the line appears as a pure resistance, $Z_O = \sqrt{L/C}$ to any excitation.

The ideal case is when $R_S = Z_O = RL$. The maximum energy transfer from source to load occurs under this condition, and there are no reflections. One half the energy is dissipated in the source resistance, R_S, and the other half is dissipated in the load resistance, RL, (the line is lossless).

If the load resistor is greater (larger) than the characteristic impedance of the line there will be extra energy available at the load, which will be reflected back to the source. This is called the underdamped condition, because the load underuses the energy available. If the load resistor is smaller than the line impedance the load will attempt to dissipate more energy than is available. Since this is not possible, a reflection will occur that is a signal to the source to send more energy. This is called the overdamped condition. Both of these cases will cause negative traveling waves, which would cause standing waves if the excitation were sinusoidal. The condition $Z_O = RL$ is called critically damped.

It should be intuitively obvious to the reader that the "safest" termination condition, from a systems design viewpoint, is the slightly overdamped condition. No energy is reflected back to the source.

Derivation of the Line Voltage for Step Function Excitation

The procedure is to apply a step function to the ideal line and to analyze the behavior of the line under various loading conditions. The following section will analyze pulses, reflections from various terminations, and the effects of rise times on the waveforms.

The step function response is important because any pulse can be represented by the superposition of a positive step function and a negative step function, delayed in time with respect to each other. By proper superposition the response of any line and load to any width pulse can be predicted. The principle of superposition applies to all linear systems.

According to theory, the risetime of the signal driven by the source is not affected by the characteristics of the line. This has been substantiated in practice by using a special coaxially constructed reed delay that delivered a pulse of 18 amperes into 50Ω with a risetime of 0.070 ns (70 ps). (Ref. 1, pg. 162).

The equation representing the voltage waveform going down the line (Figure 2.3) as a function of distance and time is:

$$VL(X, t) = VA(t)\,U(t - X\,tpd) \quad \text{for } t < T_O \qquad (2\text{-}8)$$

Where:

$$VA(t) = V_S(t)\left(\frac{Z_O}{Z_O + R_S}\right) \qquad (2\text{-}9)$$

VA = the voltage at point A

X = the voltage at a point X on the line

ℓ = the total line length

t_{pd} = the propagation delay of the line in ns/ft.

$T_O = \ell\, t_{pd}$, or the one-way line propagation delay

U(t) = a unit step function occurring at X = 0, and

$V_S(t)$ = the source voltage

When the incident voltage reaches the end of the line a reflected voltage, VL′, will occur if RL is not equal to Z_O. The reflection coefficient at the load, ρL, can be obtained by applying Ohm's Law.

The voltage at the load is VL + VL′, which must be equal to $(I_L + I_L')RL$. But $I_L = VL/Z_O$ and $I_L' = -VL'/Z_O$ (the minus sign is due to I_L being negative. i.e., it is opposite to the current due to VL.)

Therefore,

$$VB = VL + VL' = \left(\frac{VL}{Z_O} - \frac{VL'}{Z_O}\right) RL \qquad (2\text{-}10)$$

By definition:

$$\rho L = \frac{\text{reflected voltage}}{\text{incident voltage}} = \frac{VL'}{VL}.$$

Solving for VL′/VL in equation 2-10 and substituting in the equation for ρL yields:

$$\rho L = \frac{RL - Z_O}{RL + Z_O}. \qquad (2\text{-}11)$$

The reflection coefficient at the source is:

$$\rho S = \frac{R_S - Z_O}{RL + Z_O}. \qquad (2\text{-}12)$$

Re-arranging equation 2-10 yields:

$$VB = VL + VL' = \left(1 + \frac{VL'}{VL}\right) VL = (1 + \rho L)\,VL \qquad (2\text{-}13)$$

Equation 2-13 describes the voltage at the load (VB) as the sum of an incident voltage (VL) and a reflected voltage (ρL VL) at time $t = T_O$. When $RL = Z_O$ no voltage is reflected. When $RL < Z_O$ the reflection coefficient at the load is negative, so the reflected voltage subtracts from the incident voltage, giving the load voltage. When $RL > Z_O$ the reflection coefficient is positive, so the reflected voltage adds to the incident voltage, again giving the load voltage. Note that the reflected voltage at the load has been defined as positive when traveling toward the source. This means that the corresponding current must be negative, subtracting from the current driven by the source, which it does.

This "piecewise" analysis is cumbersome and can be tedious. However, it does provide an insight into what is physi-

The Theory of Transmission Lines (Continued)

cally happening and demonstrates that a complex problem can be solved by dividing it into a series of simpler problems. Also, the mathematics are simple if the exponentials, which provide phase information in the classical transmission line equations, are eliminated. One must provide the "bookkeeping" to combine the reflections at the proper time. This is quite straightforward, since a pulse travels with a constant velocity along an ideal or low loss line and the time delay between reflected pulses can be predicted.

The rules to keep in mind are that at any point and instant of time the voltage or the current is the algebraic sum of the waves traveling in the positive X and the negative X directions. For example, two voltage waves of the same polarity and equal amplitudes, traveling in opposite directions, at a given point and time will add together to yield a voltage of twice the amplitude of the individual wave. The same reasoning applies to points of termination and discontinuities on the line. The total voltage or current is the algebraic sum of all of the incident and reflected waves. Polarities must be observed. A positive voltage reflection results in a negative current reflection and vice versa.

Before considering reflections at the source, due to impedance mismatches between the source impedance and the line impedance, the behavior of the ideal line with various loads will be analyzed when it is driven by a step function.

Step Function Response of the Ideal Line for Various Loads

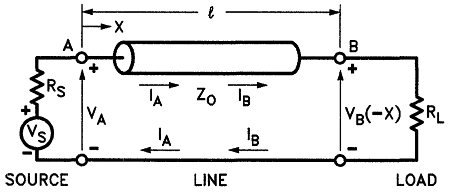
The voltage and current waveforms at point A (line input, Figure 2.3) and point B (the load) for various loads are presented in Table 1. They have been reproduced from Table 5.1, pages 158, 159 of Reference 1. Note that $R_S = Z_O$ and that VA at $t = 0$ is equal to $V_S/2$, which means that there is no impedance mismatch between the source and the line, so there will be no reflection from the source at $t = 2\ T_O$.

T_O is the one way propation of the line.

The time domain response of the reactive loads are obtained by applying a step function to the LaPlace transform of the load and then taking the inverse transform.

Note that the reflection coefficient at the load is not the total reflection coefficient (a complex number) but represents only the real part of the load. The reason for doing this is to eliminate the complex (jωt) terms because we are performing the bookkeeping involving the phase relationships, which are performed by them in classical transmission line analysis.

Also note that for the open circuit condition, Table 1 (b), Z_L = infinity, so that $\rho L = +1$. The voltage is reflected back from the load to the source (at amplitude $V_O = V_S/2$), so that at time $= 2\ T_O$ it adds to the original voltage, $V_O = V_S/2$ to give a value of $2\ V_O = V_S$. During the time the voltage wave is traveling down to and back from the load a current of $I_O = V_O/Z_O = V_S/2\ Z_O$ exists. This current charges up the distributed line capacitance to the value V_S, at which time it stops.



Direction of Travel
VA, IA → +X
VB, IB ← −X

0099-3

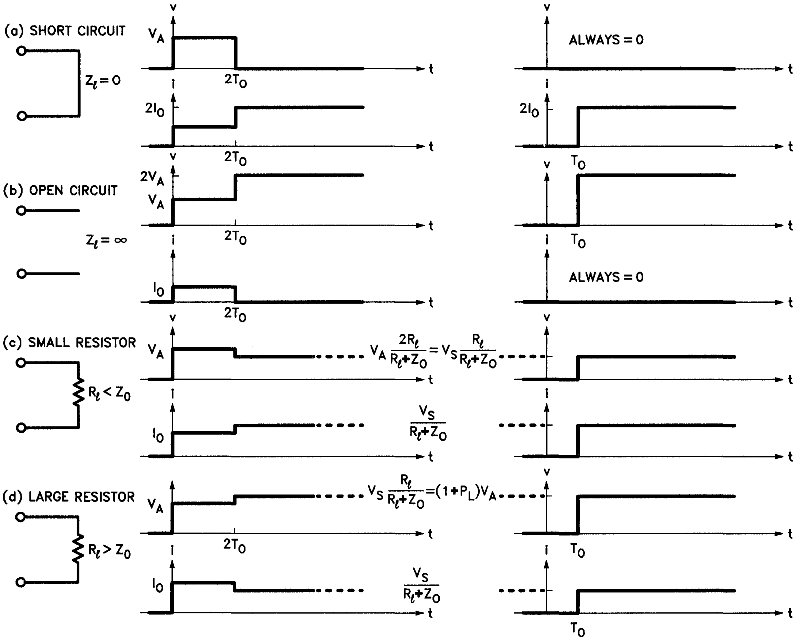
Figure 2.3. Ideal Transmission Line Loaded and Driven

The Theory of Transmission Lines (Continued)

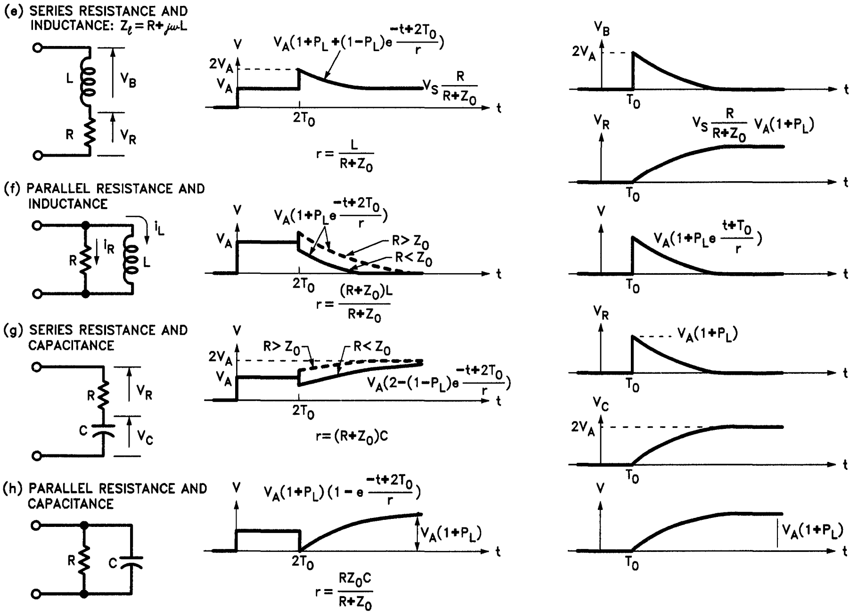
Table 1. Step Function Response of Figure 2.3 for Various Terminations

$V_A = V_S/2,\ I_O = V_O/Z_O,\ T_O = \ell\sqrt{LC},\ \rho L = (R_L - Z_O)/(R_L + Z_O)$

Termination — Input waveforms v_{in}, i_{in} — Output waveforms v_ℓ, i_ℓ


(a) SHORT CIRCUIT
Zℓ = 0
VA
2T0
2I0
ALWAYS = 0
T0
(b) OPEN CIRCUIT
Zℓ = ∞
2VA
VA
I0
ALWAYS = 0
(c) SMALL RESISTOR
Rℓ < Z0
VA 2Rℓ/(Rℓ+Z0) = VS Rℓ/(Rℓ+Z0)
VS/(Rℓ+Z0)
(d) LARGE RESISTOR
Rℓ > Z0
VS Rℓ/(Rℓ+Z0) = (1+PL)VA
VS/(Rℓ+Z0)
v
i
t

0099-10


(e) SERIES RESISTANCE AND INDUCTANCE: Zℓ = R+jωL
L
R
VB
VR
VA(1+PL+(1−PL)e^((−t+2T0)/r))
2VA
VA
VS R/(R+Z0)
2T0
r = L/(R+Z0)
VS R/(R+Z0) VA(1+PL)
(f) PARALLEL RESISTANCE AND INDUCTANCE
iL
iR
VA(1+PLe^((−t+2T0)/r))
R > Z0
R < Z0
r = (R+Z0)L/(R+Z0)
VA(1+PLe^((t+T0)/r))
(g) SERIES RESISTANCE AND CAPACITANCE
C
VC
R > Z0
R < Z0
VA(2−(1−PL)e^((−t+2T0)/r))
r = (R+Z0)C
VA(1+PL)
(h) PARALLEL RESISTANCE AND CAPACITANCE
VA(1+PL)(1 − e^((−t+2T0)/r))
VA(1+PL)
r = RZ0C/(R+Z0)
T0
v
t

0099-11

The Theory of Transmission Lines (Continued)

The waveforms at the source and load for (g) and (h) are of particular interest because (g) represents a series RC termination that dissipates no DC power and can be used to terminate a transmission line in its characteristic impedance at the input to a Cypress IC. The equivalent circuit of the input to a Cypress IC is represented by (h). The addition of (g) and (h) then models a Cypress IC driven by a transmission line terminated in its characteristic impedance when the values of R and C are properly chosen.

Reflections Due to Discontinuities

Table 2 illustrates three types of common discontinuities found on transmission lines. When a discontinuity occurs at a point on the line it causes a reflection and some energy is directed back to the source. The amount of energy reflected back is determined by the reflection coefficient at that point. Discontinuities are usually small (by design), so most of the energy is transmitted to the load.

Pulse Response of the Ideal Transmission Line

Consider next the behavior of the ideal transmission line when driven by a pulse whose width is short compared to the electrical length of the line. In other words, when the width of the pulse is less than the one-way propagation delay time, T_O, of the line.

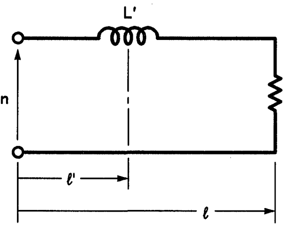
The voltage waveforms at point A (line input, Figure 2.3) and point B (the load) for various loads are presented in Table 3. They have been reproduced from Table 5.2, pages 160, 161 of Reference 1. Note that $R_S = Z_O$ and that VA at $t = 0$ is equal to $V_S/2$, which means that there is no impedance mismatch between the source and the line, so there will be no reflection from the source at $t = 2\ T_O$.

Table 2. Reflections from Discontinuities with an Applied Step Function

Discontinuity

Voltage Seen at Input End: $V_A = V_S/2$ also, $R_S = Z_O$

(a) Series Inductance



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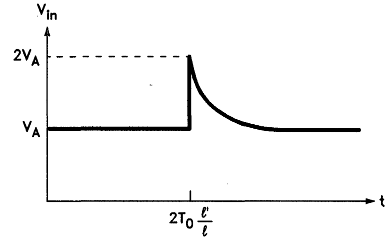

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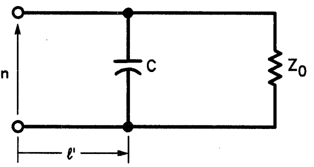
(b) Shunt Capacitance



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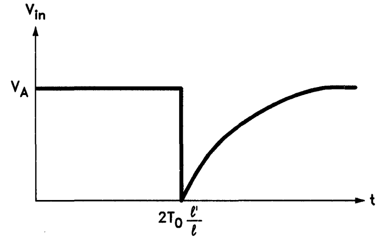

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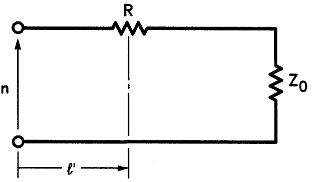
(c) Series Resistance



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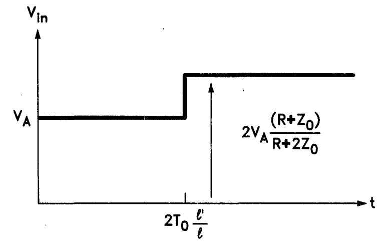

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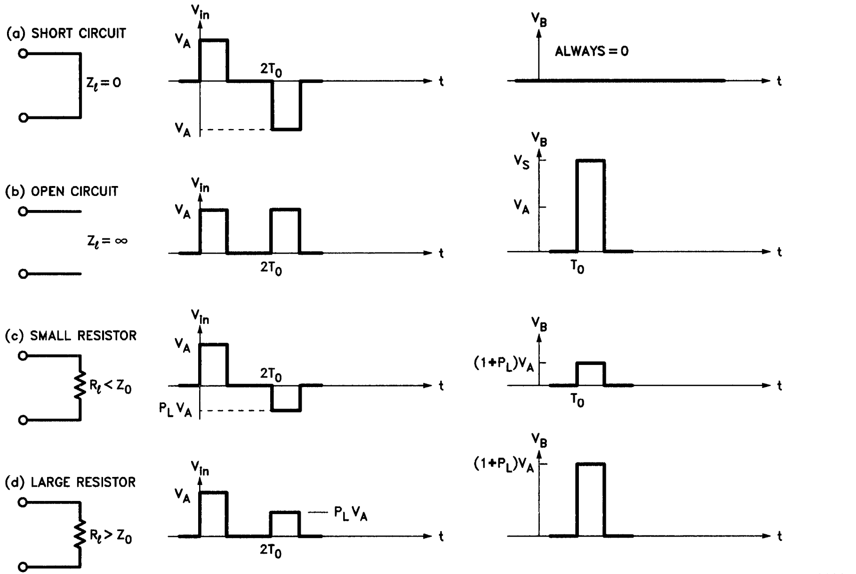
Pulse Response of the Ideal Transmission Line (Continued)

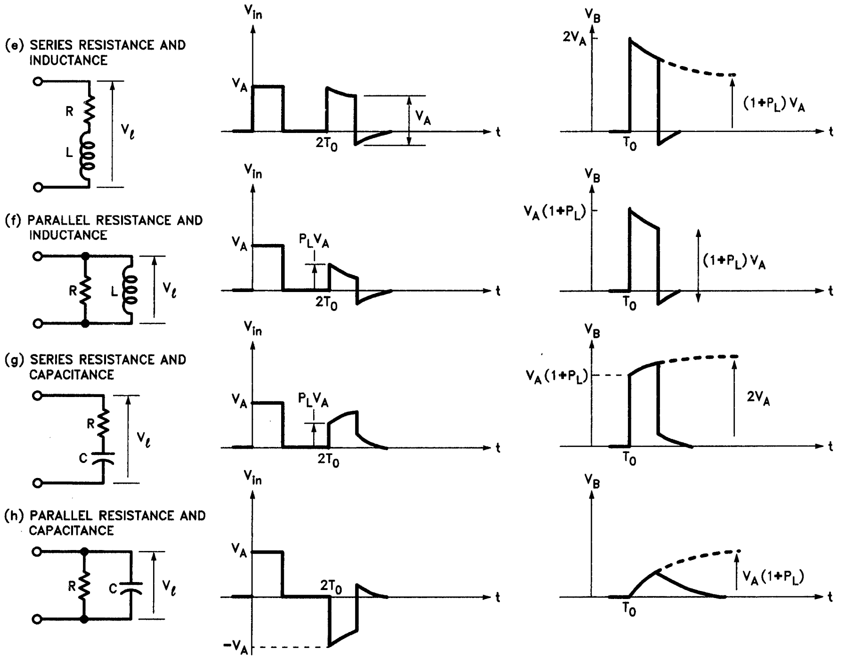
Table 3. Pulse Response of Figure 2-3 for Various Terminations

$V_A = V_S/2, \; T_O = \ell\sqrt{LC}, \; \rho_\nu = (R_L - Z_O)/(R_L + Z_O)$

Termination | Input waveform V_{in} | Output waveform v_B


(a) SHORT CIRCUIT
$Z_\ell = 0$
V_{in}
V_A
$2T_O$
V_A
t
V_B
ALWAYS = 0
t
(b) OPEN CIRCUIT
$Z_\ell = \infty$
V_{in}
V_A
$2T_O$
t
V_B
V_S
V_A
T_O
t
(c) SMALL RESISTOR
$R_\ell < Z_O$
V_{in}
V_A
$2T_O$
$P_L V_A$
t
V_B
$(1+P_L)V_A$
T_O
t
(d) LARGE RESISTOR
$R_\ell > Z_O$
V_{in}
V_A
$P_L V_A$
$2T_O$
t
V_B
$(1+P_L)V_A$
t

0099-18


(e) SERIES RESISTANCE AND INDUCTANCE
R
L
V_ℓ
V_{in}
V_A
$2T_O$
V_A
t
V_B
$2V_A$
$(1+P_L)V_A$
T_O
t
(f) PARALLEL RESISTANCE AND INDUCTANCE
R
L
V_ℓ
V_{in}
V_A
$P_L V_A$
$2T_O$
t
V_B
$V_A(1+P_L)$
$(1+P_L)V_A$
T_O
t
(g) SERIES RESISTANCE AND CAPACITANCE
R
C
V_ℓ
V_{in}
V_A
$P_L V_A$
$2T_O$
t
V_B
$V_A(1+P_L)$
$2V_A$
T_O
t
(h) PARALLEL RESISTANCE AND CAPACITANCE
R
C
V_ℓ
V_{in}
V_A
$2T_O$
$-V_A$
t
V_B
$V_A(1+P_L)$
T_O
t

0099-19

Finite Rise Time Effects

Now consider the effects of step functions with finite rise times driving the ideal transmission line.

If TR is sufficiently fast, the voltage at the load will change in discrete steps. The amplitude of the steps is determined by the impedance mismatch and the width of the steps is determined by the two-way propagation delay of the line.

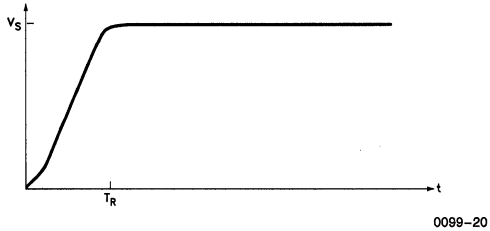
As the risetime becomes slower and the line shorter (smaller T_O), or both, the result converges to the familiar RC time constant, where C is the static capacitance. All devices should be treated as transmission lines for transient analysis when an ideal step function is applied. However, as the rise time becomes larger (slower) and the traces shorter (or both) the transmission line analysis reduces to conventional AC circuit analysis.

Reflections from Small Discontinuities

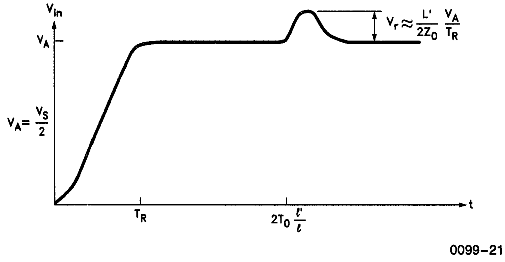
Table 4 shows a pulse with a linear rise time and rounded edges driving the transmission line of Table 2 (a), (b). The expressions for V_r are derived on pages 171 and 172 of Reference 1. The reflection caused by the small series inductance is useful for calculating the value of the inductor, L′, but little else.

Table 4. Reflections from Small Discontinuities with Finite Rise Time Pulse

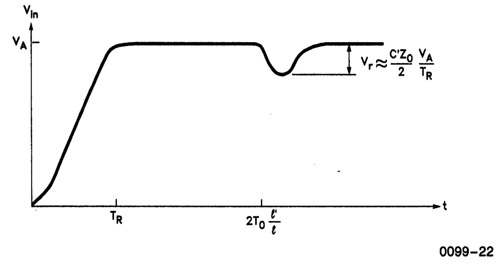
(a) Applied Pulse from Generator



(b) Reflection from Small Series Inductor L′



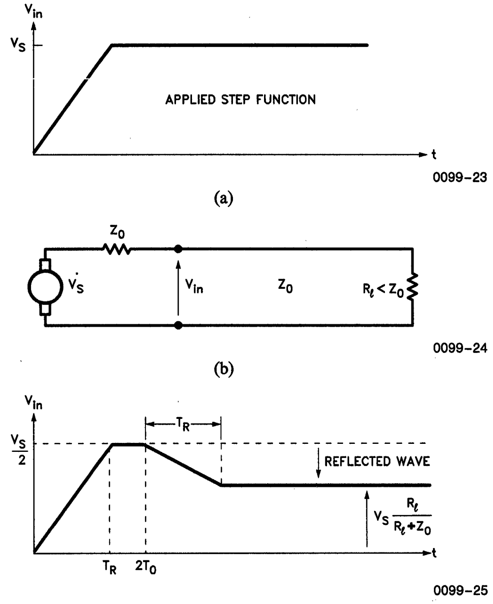
(c) Reflection from Small Shunt Capacitor C′



The reflection caused by the small shunt capacitor is more interesting because if it is sufficiently large it could cause a device connected to the transmission line to see a logic ZERO instead of a logic ONE.

The Effect of Rise Time on Waveforms

Next, consider the ideal line terminated in a resistance less than its characteristic impedance and driven by a step function with a linear rise time. The stimulus, the circuit, and the response are illustrated in *Figures 4.1 (a), (b)* and *(c)*, respectively. Once again, note that the source resistance is equal to the line characteristic impedance, so there are no reflections from the source.



(c)

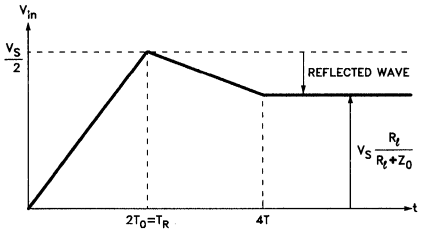
Figure 4.1. Effect of Rise Time on Step Response of Mismatched Line with $R_\ell < Z_O$

The resulting waveforms are similar to those of Table 1 (c) as modified as shown in Figure 4.1 (c). The final value of the waveform must be the same as before (Table 1 (c)).

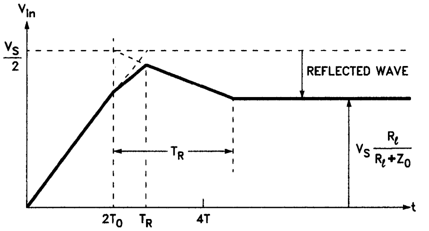
The resultant wave at the line input (V_{in}) is easily obtained by superposition of the applied wave and the reflected wave at the proper time. In *Figure 4.1* the rise time of the step function is less than the (two-way) propagation delay of the line so the input wave reaches its final value, $V_S/2$. At $t = 2\ T_O$ the reflected wave arrives back at the source and subtracts from the applied step function.

The cases where the step function rise time is equal to twice the propagation delay and greater than the propagation delay are illustrated in *Figure 4.2 (a)* and *(b)*, respectively.

Finite Rise Time Effects (Continued)



(a) $T_R = 2\,T_O$



(b) $T_R > 2\,T_O$

Figure 4.2. Effects of Rise Time on Step Response for $R_\ell < Z_O$: (a) $T_R = 2\,T_O$; (b) $T_R > 2\,T_O$

Multiple Reflections and Effective Time Constant

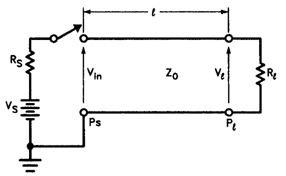
We will now consider the case of an ideal transmission line with multiple reflections causes by improper terminations at both ends of the line. The circuit and waveforms are illustrated in *Figure 4.3.* The reflection coefficients at the source and the load are both negative. i.e., the source resistance and the load resistance are both less than the line characteristic impedance. Refer to equations 2-11 and 2-12.

When the switch is initially closed, a step function of amplitude $V_O = V_{in} = \dfrac{V_S\,Z_O}{R_S + Z_O}$ appears on the line and travels toward the load. A one-way propagation delay time later, T_O, the wave is reflected back with an amplitude of $\rho L\ V_O$.

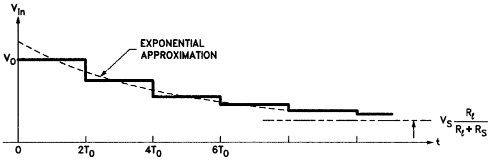
This first reflected wave then travels back to the source and at time $t = 2\ T_O$ it reaches the input end of the line. At this time the first reflection at the source occurs and a wave of amplitude $\rho S\ (\rho L\ V_O)$ is reflected back to the load. At time $t = 3\ T_O$ this wave is again reflected from the load back to the source with amplitude $\rho L\ \rho S\ (\rho L\ V_O) = \rho S\ \rho L^2\ V_O$. This back and forth reflection process continues until the amplitudes of the reflections become so small that they cannot be observed, at which time the circuit is said to be in a quiescent state.

Effective Time Constant

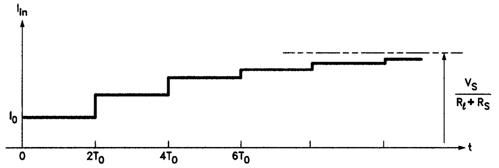
From an examination of *Figure 4.3* it is reasonable that if the voltage reflections occur in small increments that are of short durations the resultant waveform will approximate an exponential function, as indicated by the dashed line in *Figure 4.3 (b).* The smaller and narrower the steps become, the more closely the waveform will approach an exponential.



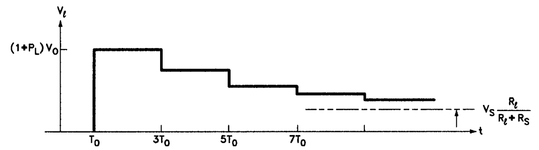
(a)



(b)



(c)



(d)

Figure 4.3. Step Function Applied to Line Mismatched on both ends; waveforms shown for negative values of ρ_S and ρ_ℓ.

The mathematical derivation is presented on pages 178 and 179 of Reference 1. The time constant is shown to be:

$$K = -\frac{2\,T_O}{1 - \rho S\ \rho L} \tag{4-1}$$

So that the resultant waveform can be approximated by;

$$V(t) = V_O\,\epsilon\left(\frac{t}{K}\right) \tag{4-2}$$

In order for equation 4-2 to be accurate ρL and ρs must be reasonably large (approaching ± 1) so that the incremental steps are small. The product $\rho S\ \rho L$ is a positive number, less than one, so the time constant is a negative number, which indicates that the exponential decreases with time. This is usually the case in transient circuits.

Both reflection coefficients must also have the same sign in order to yield a continually decreasing (or increasing) waveform. Opposite signs will give oscillatory behavior that cannot be represented by an exponential function.

Finite Rise Time Effects (Continued)

The Transition from Transmission Line to Circuit Analysis

When a transmission line is terminated in its characteristic impedance it behaves like a resistor and it usually does not matter if transmission line or circuit analysis is used; provided that the propagation delays are taken into account.

Consider the case of a short-circuited transmission line driven by a step function with a source impedance unequal to the characteristic line impedance. The general case is shown in Figure 4.3 (a). For RL = 0 the reflection coefficients are;

$$\rho S = \frac{Z_S - Z_O}{Z_S + Z_O} \quad \rho L = -1.$$

The approximate time constant is;

$$-k = \frac{2\,T_O}{1 - \rho S\,\rho L} = \frac{2\,T_O}{1 + \rho S} = \frac{T_O\,(Z_S + Z_O)}{Z_S}, \text{ or}$$

$$-k = T_O + \frac{T_O\,Z_O}{Z_S} \qquad (4\text{-}3)$$

Recall that $T_O = \ell\,\sqrt{LC}$ (one-way delay)

and $Z_O = \sqrt{\frac{L}{C}}$, where ℓ is the physical length of the line and L and C are the per-unit-length parameters.

Substitution of these into equation 4-3 yields

$$-k = T_O + \ell\,\frac{L}{Z_S}.$$

It is necessary to have Z_S smaller than Z_O.

Thus the reflection coefficients have the same sign in order to give exponential behavior. Opposite signs give oscillatory behavior.

If $Z_S \ll Z_O$, the exponential approximation becomes more accurate. If Z_S is very small compared to Z_O, then T_O is negligible compared to ℓ L/Z_O, so that equation 4-5 reduces to;

$$k = -\ell\,\frac{L}{Z_S}.$$

But ℓ L is the total loop inductance and Z_S is the total series impedance of the circuit. The time constant is then;

$$k = \frac{L'}{R_S}.$$

This is the same time constant that would have been obtained by a circuit analysis approach if the line were considered a series combination of L′ and R_S.

By open-circuiting the line and performing a similar analysis it can be shown that a RC time constant results.

Types of Transmission Lines

The types of transmission lines are:
Coaxial cable
Twisted pair
Wire over ground
Microstrip lines
Strip lines

Coaxial Cable

Coaxial cable offers many advantages for distributing high frequency signals. The well defined and uniform characteristic impedance permits easy matching. The ground shield on the cable reduces crosstalk and the low attenuation at high frequencies make it ideal for transmitting the fast rise and fall time signals generated by Cypress CMOS integrated circuits. However, because of its high cost, coaxial cable is usually restricted to applications where there are no other alternatives. These are usually clock distribution lines on PCBs or backplanes.

Characteristic Impedance

Coaxial cables have characteristic impedances of 50, 75, 93, or 150 ohms. Special cables can be made with other impedances, but these are the most common.

Propagation Delay

The propagation delay is very low. It may be computed using the formula;

$$T_{pd} = 1.017\,\sqrt{e_r}\ \text{ns/ft}. \qquad (5\text{-}1)$$

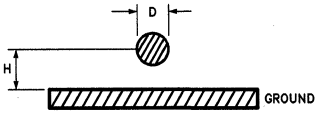
where e_r is the relative dielectric constant and depends upon the dielectric material used. For solid teflon and polyethylene it is 2.3. The propagation delay is 1.54 ns per foot. For maximum propagation velocity, coaxial cables with dielectric styrofoam or polystyrene beads in air may be used. Many of these cables have high characteristic impedances and are slowed considerably when capacitively loaded.

Twisted Pair

Twisted pairs can be made from standard wire (AWG 24-28) twisted about 30 turns per foot. Typical characteristic impedance is 110Ω. Because the propagation delay is directly proportional to the characteristic impedance (equation 2-5) the propagation delay will be approximately twice that of coaxial cable. Twisted pairs are used for backplane wiring and for breadboarding.

Wire Over Ground

Figure 5.1 shows a wire over ground. The wire over ground is used for breadboarding and for backplane wiring. The characteristic impedance is approximately 120Ω and may vary as much as ±40%, depending upon the distance from the groundplane, the proximity of other wires, and the configuration of the ground.



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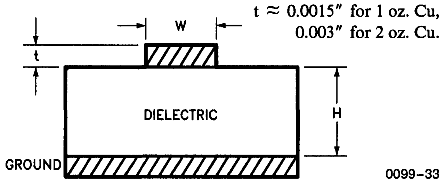
$$Z_O = \frac{60}{\sqrt{e_r}}\,\ln\left(\frac{4h}{d}\right),$$

Figure 5.1. Wire Over Ground

Types of Transmission Lines (Continued)

Microstrip Lines

A microstrip line *(Figure 5.2)* is a strip conductor (signal line) on a PCB separated from a ground plane by a dielectric. If the thickness and width of the line, and the distance from the ground plane are controlled, the characteristic impedance of the line can be predicted with a tolerance of ±5%.



$$Z_O = \frac{87}{\sqrt{e_r} + 1.41} \ln\left(\frac{5.98H}{0.8w + t}\right),$$

where:

e_r = relative dielectric constant of the board material (about 5 for G-10 fiber-glass epoxy boards),

w, h, t, = dimensions indicated.

Figure 5.2. Microstrip Line

The formula of *Figure 5.2* has proven to be very accurate for ratios of width to height between 0.1 and 3.0 and for dielectric constants between 1 and 15.

The inductance per foot for microstrip lines is;

$$L = Z_O^2 C_O \qquad (5\text{-}2)$$

where Z_O = characteristic impedance,

C_O = capacitance per foot.

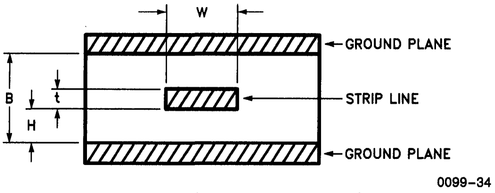
The propagation delay of a microstrip line is;

$$T_{pd} = 1.017 \sqrt{0.45\, e_r + 0.67} \text{ ns per foot} \qquad (5\text{-}3)$$

Note that the propagation delay is dependent only upon the dielectric constant and is not a function of the line width or spacing. For G-10 fiber-glass epoxy PCBs (dielectric constant of 5) the propagation delay is 1.74 ns per foot.

Strip Line

A strip line consists of a copper strip centered in a dielectric between two conducting planes *(Figure 5.3)*. If the thickness and width of the line, the dielectric constant, and the distance between ground planes are all controlled, the tolerance of the characteristic impedance will be within ±5%. The equation of *Figure 5.3* is accurate for W/(b-t) < 0.35 and t/b < 0.25.



$$Z_O = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\,\pi w \left(0.8 + \frac{t}{w}\right)}\right)$$

Figure 5.3. Stripline

The inductance per foot is given by the formula;

$$L_O = Z_O^2 C_O.$$

The propagation delay of the line is given by the formula;

$$T_{pd} = 1.017 \sqrt{e_r} \text{ ns per foot.} \qquad (5\text{-}4)$$

For G-10 fiber-glass epoxy boards the propagation delay is 2.27 ns per foot. The propagation delay is not a function of line width or spacing.

Power Distribution

Instantaneous Current

In order to realize the fast rise and fall times that Cypress CMOS integrated circuits are capable of achieving, the power distribution system must be capable of supplying the instantaneous current required when the device outputs switch from LOW to HIGH.

The energy is stored as charge on the local decoupling capacitors. It is standard practice to use one decoupling capacitor for each IC that drives a transmission line and to use one for every three devices that do not.

The value of the decoupling capacitor is determined by estimating the instantaneous current required when all the outputs of the IC switch from LOW to HIGH, assuming a reasonable "droop" of the voltage on the capacitor.

Calculations

The charge stored on the local decoupling capacitor of *Figure 6.1* is Q = C V. Differentiating yields;

$$i(t) = \frac{dQ}{dt} = C\frac{dV}{dt}. \qquad (6\text{-}1)$$

The characteristic impedance of a typical transmission line is 50Ω. Heavily (capacitively) loaded lines will have lower characteristic impedances (equation 2-7).

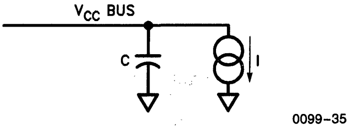


Figure 6.1. Local Decoupling Capacitor

Next, assume that the IC is an eight output PROM, such as the CY7C245 or the CY7C261. The outputs will reach V_{CC} -Vt = 5V-1V = 4V. Each output will then require 4V/50 = 8 mA. Since there are eight outputs a total of 64 mA will be required.

Solving equation 6-1 for C yields;

$$C = I\frac{dt}{dV}. \qquad (6\text{-}2)$$

The signal rise and fall times are 2 to 4 ns so we will use dt = 3 ns.

The last step is to assume a reasonable, tolerable droop in the capacitor voltage. Assume dV = 100 mV.

Therefore, substituting these values in equation 6-2 yields;

$$C = \frac{64 \times 10^{-3} \times 3 \times 10^{-9}}{100 \times 10^{-3}} = 0.192 \times 10^{-9} = 192\,\text{pF}.$$

It is standard practice to use 0.01 to 0.1 μF decoupling capacitors. A 0.01 μF capacitor is capable of supplying 330 mA under the preceding conditions.

Power Distribution (Continued)

Decoupling capacitors for high speed Cypress CMOS circuits should be of the high K ceramic type with a low ESR (Equivalent Series Resistance). Capacitors using 5 ZU dielectric are a good choice.

Low Frequency Filter Capacitors

A solid tantalum capacitor of 10 μF is recommended for each 50 to 100 ICs to reduce power supply ripple. This capacitor should be as close as possible to where the V_{CC} and ground enter the PCB or module.

When Should Transmission Lines Be Terminated?

Transmission lines should be terminated when they are long. From the preceding analysis it should be apparent that

$$\text{Long Line} > \frac{T_r}{2\,T_{pd}}.$$

Where T_{pd} is the propagation delay per unit length.

For Cypress products the rise time, T_r, is typically two nanoseconds.

The propagation delay per unit length has been shown to be as small as 1.7 ns per foot.

$$\text{Long Line} > \frac{2\text{ ns}}{2 \times 1.7\text{ ns/ft.}} = 0.59\text{ ft. or 7 inches.}$$

Not all lines exceeding 7 inches will need to be terminated. Terminations are usually only required on clock inputs, write and read strobe lines on SRAMs, and chip select or output enable lines on RAMs, PROMs, and PLDs. Address lines and data lines on RAMs and PROMs usually have time to settle.

In the case where multiple loads are connected to a transmission line, only one termination circuit is required. The termination network should be located at the load that is electrically the longest distance from the source. This is usually the load that is the longest physical distance from the source.

Types of Terminations

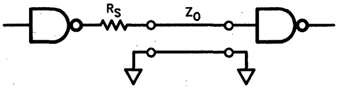
There are three basic types of terminations. They are called series damping, parallel, and pullup/pulldown. Each has their advantages and disadvantages.

Except for series damping, the termination network should be attached to the input (load) that is electrically furthest away from the source. Component leads should be as short as possible in order to prevent reflections due to lead inductance.

Series Damping

Series damping is accomplished by inserting a small resistor (typically 10Ω to 75Ω) in series with the transmission line, as close to the source as possible, as illustrated in *Figure 8.1.* Series damping is a special case of damping in which the series resistor value plus the circuit output impedance is equal to the transmission line impedance. The strategy is to prevent the wave that is reflected back from the load from reflecting back from the source by making the source reflection coefficient equal to zero.

The channel resistance (ON resistance) of the pulldown device for Cypress ICs is ten to twenty ohms (depending upon the current sinking requirements), so this value should be subtracted from the series damping resistor, R_S.



0099-36

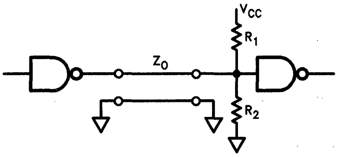
Figure 8.1. Series Damping

The disadvantage of the series damping technique is that during the two-way propagation delay time the voltage at the input to the line is half-way between the logic levels, due to the voltage divider action of R_S. This means that no inputs can be attached along the line, because they would respond incorrectly. However, any number of devices may be attached to the load end of the line because all of the reflections will be absorbed at the source.

Due to the low input current required by Cypress CMOS ICs, there will be essentially no DC power dissipation and the only AC power required will be to charge and discharge the parasitic capacitances.

Pullup/Pulldown

The pullup/pulldown resistor termination shown in *Figure 8.2* is included only for the sake of completeness. If both resistors are used there will be DC power dissipated all the time and if only a pulldown resistor is used DC power will be dissipated when the input is in the logic HIGH state. Due to these power dissipations, this termination is not recommended.



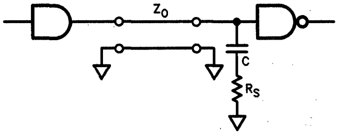
0099-37

Figure 8.2. Pullup/Pulldown

However, in special cases where inputs should be either pulled up (HIGH) for logic reasons or because of very slow rise and fall times, a pullup resistor to V_{CC} may be used in conjunction with the terminating network described below. DC power will be dissipated when the source is LOW.

Parallel AC Termination; *Figure 8.3*

This is the recommended general purpose termination. It does not have the disavantage of the half-voltage levels of series damping and it causes no DC power dissipation. Loads may be attached anywhere along the line and they will see a full voltage swing.



0099-38

Figure 8.3. Parallel AC

The disadvantages is that it requires two components, versus the series damping termination of one.

Types of Terminations (Continued)

The value of C should be as small as possible. Such that Xc is less than two ohms at the frequency

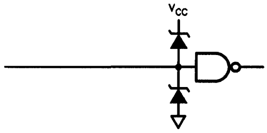
$$F = \frac{1}{2\,T_{PD}}.$$

R_S can then equal Z_O.

Schottky Diode Termination

In certain instances it may be expedient to use Schottky diodes to terminate lines. Where line impedances are not well defined, as in breadboards and backplanes, the use of diode terminations is convenient and may save time.

A typical diode termination is shown in *Figure 9.1.* The low forward voltage, V_f, of the diode (typically 0.3 to 0.45V) clamps the input signal to a V_f below ground (lower diode) and $V_{CC} + V_f$ (upper diode), thereby significantly reducing signal undershoot and overshoot. In some applications both diodes may not be required.



0099-39

Figure 9.1. Schottky Diode Termination

The advantages of diode terminations are:

- Impedance matched lines are not required.
- The diodes replace terminating resistors or RC terminations.
- The clamping actions of the diodes reduce overshoot and undershoot.
- Although diodes are more expensive than resistors, the total cost of layout may be less because a precise, controlled transmission line environment is not required.
- If ringing is discovered to be a problem during system checkout the diodes can be easily added.

As with resistor or RC terminations, the leads should be as short as possible in order to avoid ringing due to lead inductance.

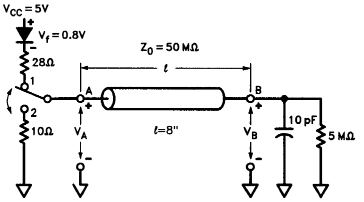
A few of the types of Schottky diodes commercially available are :

- 1N4148 (Switching)
- 1N5711
- MBD101 (Motorola)
- HP5042 (Hewlett Packard)

Example: Unterminated Line

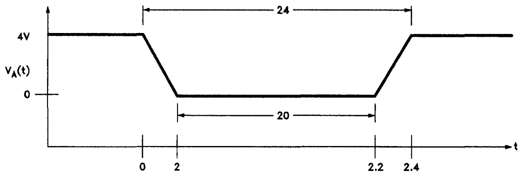
The following example is presented to illustrate the procedure for calculating the waveforms when a Cypress PLD is used to generate the write strobe for a Cypress SRAM. The PLD is a PAL®C 20 device and the SRAM is the CY7C189-25.

The equivalent circuit is illustrated in *Figure 10.1* and the (unmodified) driving waveform in *Figure 10.2.* The rise and fall times are two nanoseconds. The length of the microstrip trace on the PCB is eight inches and the characteristic line impedance is 50Ω. It is required to calculate the voltage waveforms at the source (point A) and the load (point B) as functions of time.



0099-40

Figure 10.1. Equivalent Circuit for Cypress PAL Driving RAM



0099-41

Figure 10.2. V_A (t), Unmodified

Equivalent Circuits for The PLD and SRAM

The equivalent ON channel resistance of the PLD pullup device, 28Ω, was calculated using the output source current versus voltage graph over the region of interest (0 to 2V) from the data sheet. The equivalent resistance of the pulldown device, 10Ω, was calculated in a similar manner, using the output sink current versus output voltage graph, also on the data sheet.

The equivalent input circuit for the SRAM was constructed by approximating the input and stray capacitance with a 10 pF capacitor and the resistance with a 5 million ohm resistor. The input leakage current for all Cypress products is specified as a maximum of ± 10 μA, which guarantees a minimum of 500,000Ω at $V_{in} = 5V$. Typical leakage current is one microampere.

Transmission Line Calculations

The next step is to calculate the propagation delay and loaded characteristic impedance of the line.

Propagation Delay

The unloaded propagation delay of the line is calculated using equation 5-3 with a dielectric constant of 5.

$$T_{pd} = 1.74 \text{ ns/ft.}$$

In order to calculate the loaded line propagation delay, the intrinsic capacitance must first be calculated using equation 2-5.

$$T_{pd} = Z_O\,C_O,$$

where Z_O is the intrinsic characteristic impedance and C_O is the intrinsic capacitance.

$$C_O = \frac{T_{pd}}{Z_O} = \frac{1.74 \text{ ns/ft.}}{50} = 34.8 \text{ pF/ft.}$$

Example: Unterminated Line (Continued)

The line is loaded with 10 pF, so equation 2-6 is used to compute the loaded propagation delay of the line.

$$T_{pd}' = T_{pd}\sqrt{1 + \frac{C_D}{C_O}}$$

$$T_{pd}' = 1.74\text{ ns/ft.}\sqrt{1 + \frac{10\ \rho F}{34.8\ \rho F/\text{ft.} \times \frac{8\text{ in.}}{12\text{ in./ft.}}}}$$

$$T_{pd}' = 2.08\text{ ns/ft.}$$

Note that the capacitance per unit length must be multiplied by the line length to arrive at an equivalent lumped capacitance.

Characteristic Impedance

The intrinsic line impedance is reduced by the same factor by which the propagation delay is increased (1.96). See equation 2-7.

$$Z_O' = \frac{50\Omega}{1.196} = 41.8\Omega.$$

Initial Conditions

At time t = 0 the circuit of *Figure 10.1* is in a quiescient state. The voltage at points A and B must be the same.

By inspection;

$$VA = VB = (V_{CC} - Vf)\left(\frac{RL}{RS + RL}\right)$$

$$= (5\text{-}1)\left(\frac{5 \times 10^6}{28 + 5 \times 10^6}\right) = 4V$$

The Falling Edge of the Write Strobe

At t = 0 the driving waveform changes from 4V to 0V (approximately) with a fall time of two nanoseconds. This is represented in *Figure 10.1* by the switch arm moving from position 1 to position 2. The wave propagates to the load at the rate of 2 ns per foot (approximately) and arrives there

$$T_O = 2\text{ ns/ft.} \times \frac{8\text{ in.}}{12\text{ in./ft.}} = 1.33\text{ ns}$$

later, as illustrated in *Figure 10.3 (b)*.

The reflection coefficient at the load is ρL = 1, so a nearly equal and opposite polarity waveform is propagated back to the source from the load, arriving at t = 2 T_O = 2.66 ns, as shown in *Figure 10.3 (a)*. (See Table 3 {h}). Note that the falltime is preserved. The reflection coefficient at the source is;

$$\rho s = \frac{RS - Z_O'}{RS + Z_O'} = \frac{10 - 41.8}{10 + 41.8} = -0.61$$

The magnitude of the reflected voltage at the source is then;

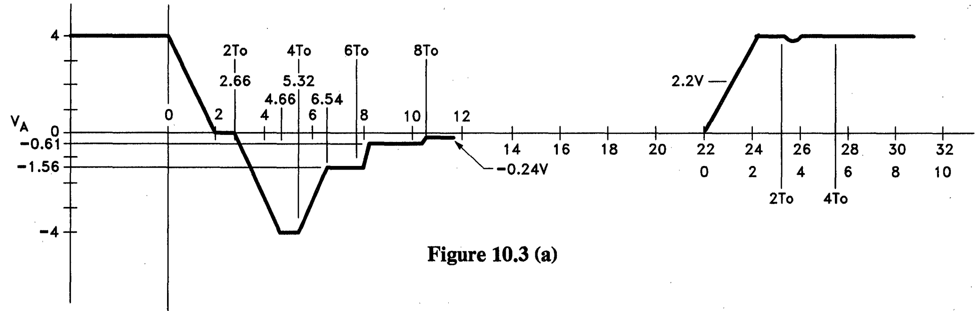
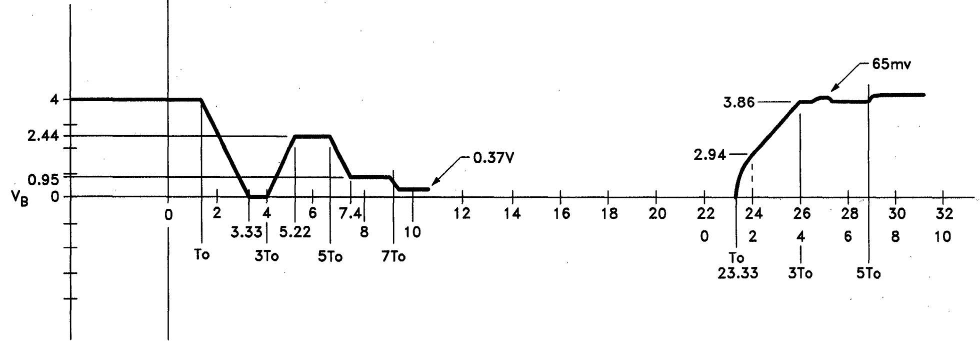


Figure 10.3 (a)



0099–42

Figure 10.3 (b)

Example: Unterminated Line (Continued)

$$VS1 = -4V \times (-0.61) = 2.44V.$$

This wave propagates from the source to the load and arrives at $t = 3\ T_O$, and adds to the (zero volts) signal. The risetime is preserved, so the time required for the signal to go from 0V to 2.44V is;

$$t_r = 2.44V \times 2\ ns/4V = 1.22\ ns.$$

The signal at the load thus reaches the 2.44V level at time $t = 3\ T_O + 1.22\ ns = 5.22\ ns$ and remains at that level until the next reflection occurs at $t = 5\ T_O$. The wave that arrived at the load at $3\ T_O$ is reflected back to the source and arrives at $t = 4\ T_O$ (5.32 ns). The 2.44V level adds to the −4V level, so that the resultant level is −1.56V. The risetime is preserved, so that this level is reached at $t = 4\ T_O + 1.22\ ns = 6.54\ ns$, and maintained until the next reflection occurs at $t = 6\ T_O$. The 2.44V wave that arrived at the source at $t = 4\ T_O$ is reflected back to the load and arrives at $t = 5\ T_O$. The portion that is reflected back is;

$$VS2 = 2.44 \times (-0.61) = -1.49V.$$

This subtracts from the 2.44V level to give 2.44 − 1.49 = 0.95V. The falltime is preserved, so the time required for the signal to go from 2.44V to 0.95V is;

$$t_f = 1.49V \times 2\ ns/4V = 0.75\ ns.$$

The 0.95V level is thus reached at time $t = 5\ T_O + 0.75\ ns = 7.4\ ns$.

At $t = 6\ T_O$ the 0.95V wave arrives back at the source, where it subtracts from the −1.56V level to give −0.61V. The risetime is $t_r = 0.95 \times 0.5\ ns/V = 0.45\ ns$.

The 0.95V wave that arrived at the source at $t = 6\ T_O$ is reflected back to the load and arrives at $t = 7\ T_O$. The portion that is reflected back is;

$$VS3 = 0.95 \times (-0.61) = -0.58V.$$

This subtracts from the 0.95V level to give 0.37V. The falltime is approximately 0.5 ns.

This process continues until the voltages at points A and B decay to approximately zero volts.

Observations

The positive reflection coefficient at the load and the negative reflection coefficient at the source result in an oscillatory behavior that eventually decays to acceptable levels. The voltage at point A reaches −0.61V after 6 T_O delays and the voltage at point B reaches 0.37V after 7 T_O delays.

The reflection at the load that causes the voltage to exceed the TTL minimum ONE level (2V) at $T = 3\ T_O$ could cause a problem if either the data to be written in the RAM changes up to 5 T_O delays after the falling edge of the write strobe or if the observed shortening of the write strobe by 5 T_O delays violates the minimum write strobe specification.

However, if this reflection occurred on a clock line to a logic device, registered PROM, or a PLD the reflection could be interpreted by the device as a second clock. The width of the pulse caused by the reflection in this case is $2\ T_O = 2.66\ ns$, which is probably too short to be detected. If the line were either slightly longer or more heavily capacitively loaded the pulse would be wider and could be detected as a second clock.

The Rising Edge of the Write Strobe

At t = 22 ns the rising edge of the write strobe begins, which is the equivalent of closing the switch in *Figure 10.1* in the 1 position. For this analysis it its convenient to start the time scale over at zero, as is shown in *Figures 10.3 a* and *b*.

If the forcing function were a step function, the equations of Table 1 (h) would apply. The time constant in the equation is:

$$T = \frac{R\ Z_O'\ Ce}{R + Z_O'}. \qquad (10\text{-}1)$$

Because $R \gg Z_O'$, $T = Z_O'\ Ce$, where $Z_O' = 41.8\Omega$ and $Ce = 33.2\ pF$.

This is the equivalent of saying that the five megohm device input resistance can be ignored for transient circuit analysis. Substitution of Z_O' and Ce into the preceding equation yields a time constant of T = 1.39 ns.

Writing the equation for the voltages for the circuit of Figure 10.1

$$VA(t) = i\,Z_O' + \frac{1}{Ce}\int_0^t i\,dt. \qquad (10\text{-}2)$$

Also, $VA(t) = Kt\,U(t) - K(t - T1)\,U(t - T1)$. (10-3)

Where Kt is the rising edge of the write strobe (K = 2V/ns) applied at t = 0 using a unit step function, U(t), and −K (t − T1) represents an equal but opposite waveform applied at t = T1 (after the risetime) using a unit step function, U(t − T1).

Equating the equations and taking the LaPlace transforms of both sides yields:

$$\frac{K}{s^2} - \frac{K\,\epsilon^{-T1S}}{s^2} = Z_O'\,I(s) + \frac{I(s)}{Ce\,s} = \left(Z_O' + \frac{1}{Ce\,s}\right) I(s). \qquad (10\text{-}4)$$

$$\text{However, } VB(t) = \frac{1}{Ce}\int_0^t i\,dt, \text{ or } VB(s) = \frac{I(s)}{Ce\,s}.$$

Therefore:

$$\frac{K}{s^2} - \frac{K\,\epsilon^{-T1S}}{s^2} = \left(Z_O' + \frac{1}{Ce\,S}\right) Ce\,s\,VB(s). \qquad (10\text{-}5)$$

Solving for VB(s) yields:

$$VB(s) = \frac{\frac{K}{s^2}\left(1 - \epsilon^{-T1S}\right)}{Ce\,s\left(Z_O' + \frac{1}{Ce\,s}\right)}. \qquad (10\text{-}6)$$

Which is equivalent to:

$$VB(s) = \frac{\frac{K}{Z_O'\,Ce}\left(1 - \epsilon^{-T1S}\right)}{s^2\left(S + \frac{1}{Z_O'\,Ce}\right)}. \qquad (10\text{-}7)$$

Example: Unterminated Line (Continued)

Taking the inverse LaPlace transform yields:

$$VB(t) = \left[K\,Z_O'\,Ce\left(\epsilon^{\frac{-t}{Z_O'\,Ce}} - 1\right) + Kt\right]U(t) - \qquad (10\text{-}8)$$

$$\left[K\,Z_O'\,Ce\left(\epsilon^{\frac{-(t-T1)}{Z_O'\,Ce}} - 1\right) + K(t - T1)\right]U(t - T1)$$

Equation 10-8 consists of two terms. The first term applies from time zero up to and including T1 and the second term applies after T1.

$$VB(t) = \frac{K\,Z_O'\,Ce}{T1}\left(\epsilon^{\frac{-t}{Z_O'\,Ce}} - 1\right) + \frac{K}{T1}(t)\; t \leq T1 \qquad (10\text{-}9)$$

$$VB(t) = \frac{K\,Z_O'\,Ce}{T1}\left(1 - \epsilon^{\frac{T1}{Z_O'\,Ce}}\right)\epsilon^{\frac{-t}{Z_O'\,Ce}} + K1\; t > T1 \qquad (10\text{-}10)$$

where K1 = final value = 4V

Substitution of the proper values into equation 10-9 yields at t = T1 = 2 ns.

VB (t = T1) =

$$\frac{2 \times 41.8 \times 33.2 \times 10^{-12}}{2 \times 10^{-9}}\left(\epsilon^{-1.439} - 1\right) + \frac{2V}{ns} \times 2\,ns$$

$$= -1.057 + 4 = 2.94V$$

If the forcing function would have been a step function the equation would be:

$$VB(t) = 4V\left(1 - \epsilon^{\frac{-t}{Z_O'\,Ce}}\right) \qquad (10\text{-}11)$$

at t = 2 ns, VB = 3V, which is greater than the 2.94V calculated using equation 10-9.

At t = (22 ns) + T_O the voltage waveform begins to build up at the load and continues to build until the first reflection from the source occurs at t = 3 T_O.

Equation 10-10 is used to calculate the voltage at the load at t = 2 T_O (because 1 T_O is used for propagation delay time).

VB (t = 2 T_O) =

$$\frac{-2V \times 41.8 \times 33.2 \times 10^{-12}}{2 \times 10^{-9}}\left(1 - \epsilon^{-1.439}\right)\left(\epsilon^{-2}\right) + 4$$

$$= -1.39\,(0.762)\,(0.135) + 4$$

$$= -0.143 + 4 = 3.86V$$

The voltage at the load will remain at this value until the first reflection from the source reaches the load at t = 3 T_O.

Meanwhile, at t = T_O, the wave at the load is reflected back to the source and arrives there at t = 2 T_O. It subtracts from the 4V level at the source as illustrated in Table 4 (c). The amplitude of the "droop" is given by:

$$V_r \cong \frac{C'\,Z_O'\,V_O}{2\;\;TR} \qquad (10\text{-}11)$$

for the case Vs = Z_O'.

If Vs ≠ Z_O' equation 10-11 must be modified. Instead of $\frac{V_O}{2}$ the voltage is $V_O\left(\frac{R_S}{R_S + Z_O'}\right)$, so that equation 10-11 becomes:

$$V_r \cong \frac{C'\,Z_O'\,V_O}{TR}\left(\frac{R_S}{R_S + Z_O'}\right). \qquad (10\text{-}12)$$

where: $C' = 10$ pF
$Z_O' = 41.8\Omega$
$R_S = 28\Omega$
$T_R = 2$ ns
$V_O = 4V$

Substitution of these values into equation 10-12 yields:

$$V_r = 0.33V.$$

4V − 0.33V = 3.67V, so there is no danger of the voltage dropping below the minimum HIGH level.

The reflection coefficient at the source is:

$$\rho s = \frac{R_S - Z_O'}{R_S + Z_O'} \text{ where: } \begin{array}{l} R_S = 28\Omega \\ Z_O' = 41.8\Omega \end{array}$$

$$\rho s = -0.198$$

The amount of voltage reflected from the source back to the load is then:

$$VS_1 = (-0.33) \times (-0.198) = +0.065V.$$

This same result could have been obtained by applying the ramp function of *Figure 10.2* to a large resistor and then to a capacitive load and adding the results using superposition.

Observations

The risetime of the waveform at the load is reduced by the 10 pF load capacitor. The reflection at the source caused by the load capacitor is insufficient to reduce the 4V level to less than the TTL one level (2V).

The reflection coefficient at the source is sufficiently small so that the energy reflected back to the load is insufficient to cause a problem.

Summary

The example has demonstrated that, under certain conditions, the voltage reflections caused by the impedance mismatch between a PCB trace and the input of a Cypress CMOS integrated circuit may cause a pulse whose energy is sufficient to be detected by another circuit.

It is the responsibility of the system designer to identify and to analyze these conditions and to then modify the design such that the reflections will not occur.

References

1. Matick, Richard E,: *Transmission Lines For Digital and Communications Networks,* McGraw Hill, 1969.
2. Blood, Jr, William R.,: *MECL System Design Handbook,* Motorola Inc., 1983.

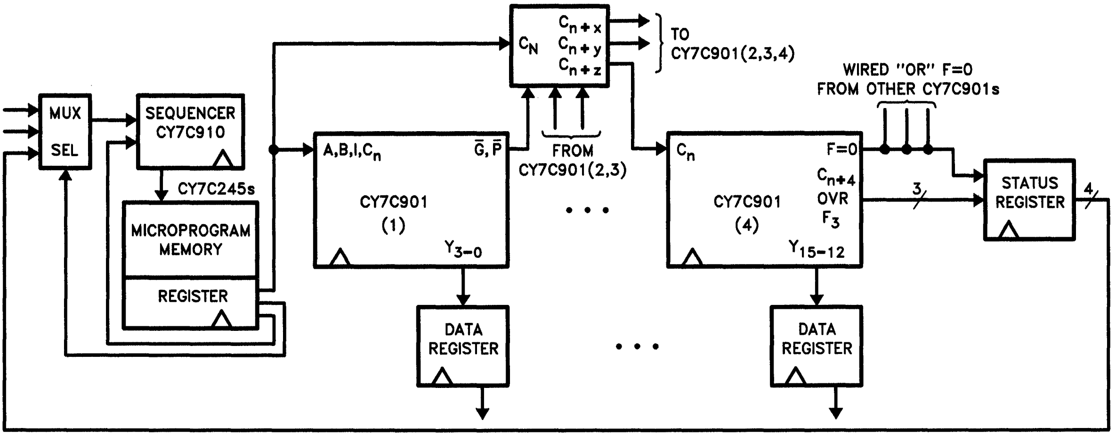
CYPRESS
SEMICONDUCTOR

Microcoded Systems Performance

The microcoded processor family of devices offered by Cypress Semiconductor are the fastest available. High performance systems designed for specific applications can be configured using this high performance chip set. The performance of these devices in 16- and 32-bit processors is detailed below.

Increasing functional integration is evident in the CY7C9101 16-bit slice, which is the equivalent to four CY7C901s (4-bit slice) and a 2902 carry lookahead generator. By placing these functions on a single chip, the interconnect delays between chips are reduced. Significant improvement in overall system throughput, reduced board space, and reduced power requirements are among the advantages of the CY7C9101 systems over CY7C901 based systems. Following is a critical path timing analysis of the data loop and control loop for generic 16- and 32-bit systems. A discussion of the speed and power advantages offered by CY7C9101 systems will also be presented.

Minimum Cycle Time Calculations for 16- and 32-Bit Systems


MUX
SEL
SEQUENCER
CY7C910
CY7C245s
MICROPROGRAM
MEMORY
REGISTER
C_N
C_{n+x}
C_{n+y}
C_{n+z}
TO
CY7C901(2,3,4)
A,B,I,C_n
$\overline{G}$,$\overline{P}$
CY7C901
(1)
Y_{3-0}
FROM
CY7C901(2,3)
• • •
WIRED "OR" F=0
FROM OTHER CY7C901s
C_n
F=0
C_{n+4}
OVR
F_3
CY7C901
(4)
Y_{15-12}
3
STATUS
REGISTER
4
DATA
REGISTER
• • •
DATA
REGISTER

0096-1

Figure 1. CY7C901 Based 16-Bit System (Pipelined System, Add without Simultaneous Shift)

	Data Loop	
CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $C_n + z$	9
CY7C901	C_n to Worst Case	18
Register	Setup	4
		71 ns

	Control Loop	
CY7C245	Clock to Output	12
MUX	Select to Output	12
CY7C910	CC to Output	22
CY7C245	Access Time	20
		66 ns

Minimum Clock Period = 71 ns

Minimum Cycle Time Calculations for 16- and 32-Bit Systems (Continued)

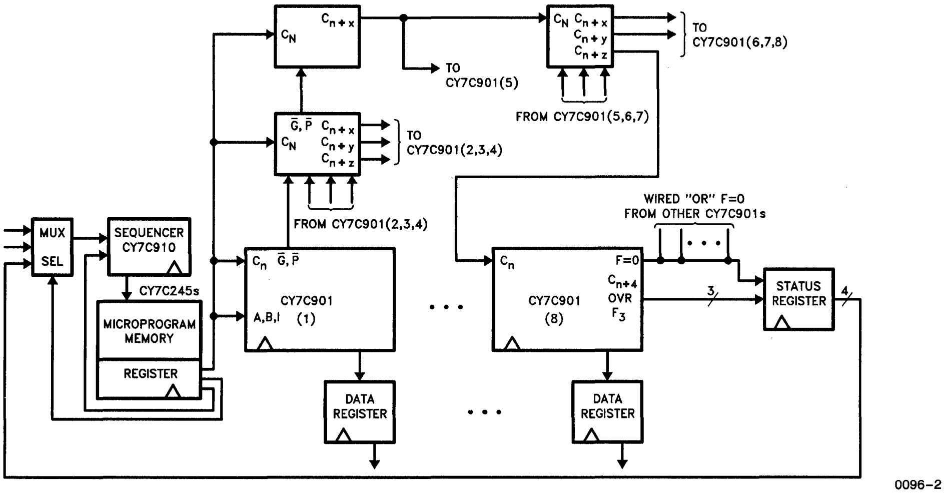

C_{n+x}
C_N
TO CY7C901(5)
C_N C_{n+x} C_{n+y} C_{n+z}
TO CY7C901(6,7,8)
FROM CY7C901(5,6,7)
$\overline{G}$, $\overline{P}$ C_{n+x} C_N C_{n+y} C_{n+z}
TO CY7C901(2,3,4)
FROM CY7C901(2,3,4)
WIRED "OR" F=0 FROM OTHER CY7C901s
MUX
SEL
SEQUENCER CY7C910
CY7C245s
MICROPROGRAM MEMORY
REGISTER
C_n $\overline{G}$, $\overline{P}$
CY7C901
A,B,I (1)
C_n
F=0
C_{n+4}
OVR
F_3
CY7C901 (8)
3
STATUS REGISTER
4
DATA REGISTER
DATA REGISTER
0096-2

Figure 2. CY7C901 Based 32-Bit System (Pipelined System, Add without Simultaneous Shift)

	Data Loop	
CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $\overline{G}$, $\overline{P}$	12
	$\overline{G}_0$, $\overline{P}_0$ to C_{n+x}	9
	C_n to $C_{n+x,y,z}$	14
CY7C901	C_n to Worst Case	18
Register	Setup	4
		97 ns

	Control Loop	
CY7C245	Clock to Output	12
MUX	Select to Output	12
CY7C910	CC to Output	22
CY7C245	Access Time	20
		66 ns

Minimum Clock Period = 97 ns

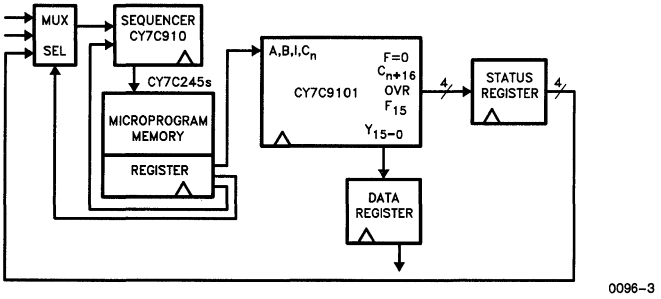

MUX
SEL
SEQUENCER CY7C910
CY7C245s
MICROPROGRAM MEMORY
REGISTER
A,B,I,C_n
CY7C9101
F=0
C_{n+16}
OVR
F_{15}
Y_{15-0}
4
STATUS REGISTER
4
DATA REGISTER
0096-3

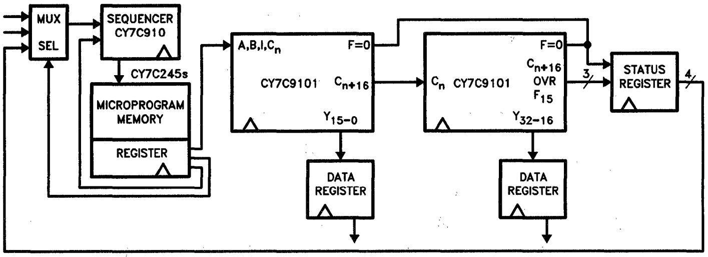
Figure 3. CY7C9101 Based 16-Bit System (Pipelined System, Add without Simultaneous Shift)

	Data Loop	
CY7C245	Clock to Output	12
CY7C9101	A, B to Y, C_{n+16}, OVR	37
Register	Setup	4
		53 ns

	Control Loop	
CY7C245	Clock to Output	12
MUX	Select to Output	12
CY7C910	CC to Output	22
CY7C245	Access Time	20
		66 ns

Minimum Clock Period = 66 ns

Minimum Cycle Time Calculations for 16- and 32-Bit Systems (Continued)



0096-4

Figure 4. CY7C9101 Based 32-Bit System (Pipelined System, Add without Simultaneous Shift)

	Data Loop	
CY7C245	Clock to Output	12
CY7C9101	A, B to $C_n + 16$	35
CY7C9101	C_n to Worst Case	24
Register	Setup	4
		75 ns

	Control Loop	
CY7C245	Clock to Output	12
MUX	Select to Output	12
CY7C910	CC to Output	22
CY7C245	Access Time	20
		66 ns

Minimum Clock Period = 75 ns

Power is an important consideration in microcoded systems. For an equivalent system, the CY7C901 offers substantial savings in power over the bipolar devices. Coupled with other low power Cypress CMOS devices, the power savings over bipolar is clearly evident. The functional integration of four CY7C901s with carry lookahead gives the CY7C9101 even greater advantages. The number of ALU elements is reduced by a factor of four, also, there is a reduction in the carry logic needed. A comparison between bipolar, CY7C901-based, and CY7C9101-based systems is given below in Table 1. Note that in this comparison, the devices common to all 16- and 32-bit system configurations are included in the I_{CC} computations.

Cypress CMOS devices offer the highest speed microcoded solutions while keeping power consumption to reasonable levels. The CY7C901-based systems win over bipolar's fastest devices in a speed comparison, while consuming roughly ⅓ the power. Upgrading to the CY7C9101 will result in even faster systems, at close to ⅓ the power of the CY7C901-based systems. This comparison is illustrated below, in Table 2.

Table 1

I_{CC} Calculations for 16-Bit Systems (All Figures in mA)

	Cypress CMOS		
	CY7C901 Based	**CY7C9101 Based**	**Bipolar**
Sequencer	100	100	340
Registered PROM	90	90	185
Carry Logic	110	—	110
ALU Elements			
4x Four-Bit Slice	320		1060
16-Bit Slice		75	
Total	620	265	1695

I_{CC} Calculations for 32-Bit Systems (All Figures in mA)

	Cypress CMOS		
	CY7C901 Based	CY7C9101 Based	Bipolar
Sequencer	100	100	340
Registered PROM	90	90	185
Carry Logic	330	110	330
ALU Elements			
8x Four-Bit Slice	640		2120
2x Sixteen-Bit Slice		150	
Total	1160	450	2975

Table 2. Speed/Power Comparison between Bipolar, CY7C901, CY7C9101

	Minimum Clock Cycle (ns)			**Maximum I_{CC} (mA)**		
	Bipolar	**CY7C901**	**CY7C9101**	**Bipolar**	**CY7C901**	**CY7C9101**
16-Bit Systems	85	71	66	1695	620	265
32-Bit Systems	111	97	75	2975	1160	450

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Packages

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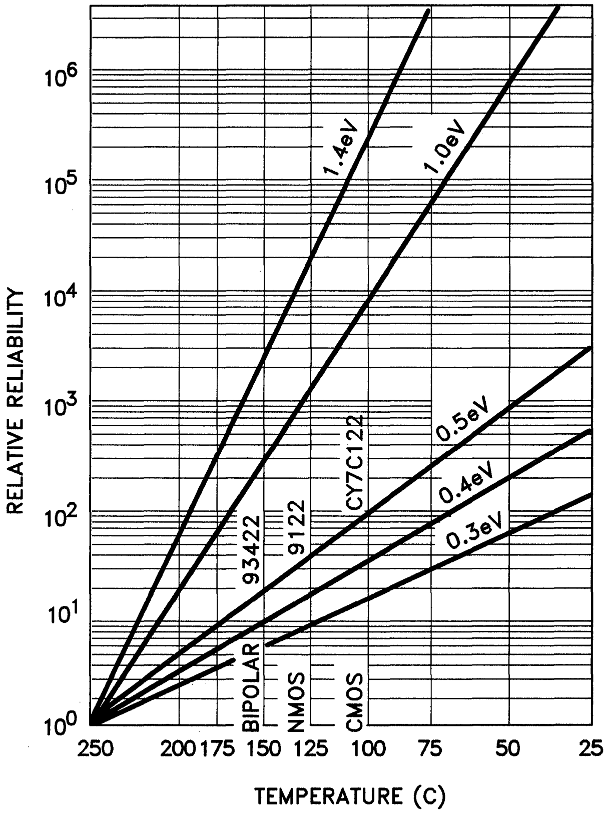
CYPRESS
SEMICONDUCTOR

Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device *(Figure 1).*

Typical activation energies for commonly observed failure mechanism in CMOS devices are shown in Table 2.



0064-1

Figure 1. Arrhenius plot, which assumes a failure rate proportional to EXP ($-E_A/kT$) where E_A is the activation energy for the particular failure mechanism

Table 2. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (EQ)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5–1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally-activated reliability failures, Cypress Semiconductor has optimized both their low power generating 1.2μ CMOS device fabrication process and their high heat dissipation packaging capabilities. Table 3 demonstrates this optimized thermal performance by comparing bipolar, NMOS and Cypress high speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 3. Thermal Performance of Fast 1K SRAMS in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I_{CC} (mA)	150	110	60
V_{CC}(V)	5.0	5.0	5.0
P_{MAX}(MW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Data Sheet P_{MAX}*	160	136	91

*$T_{ambient} = 70°C$

The Cypress 7C122 device, during its normal operation, experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0 eV activation energy failure mechanisms, this translates into an improvement in excess of two orders of magnitude (100X) over the bipolar 93422 device and more than one order of magnitude (30X) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as,

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation:

$$T_J = T_A + P\,[\theta_{JA}] = T_A + P\,[\theta_{JC} + \theta_{CA}]$$

where:

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation equals 70°C

T_J = Junction temperature of the IC chip

T_C = Temperature of the case (package)

P = Power at which the device operates

θ_{JC} = Junction to case thermal resistance

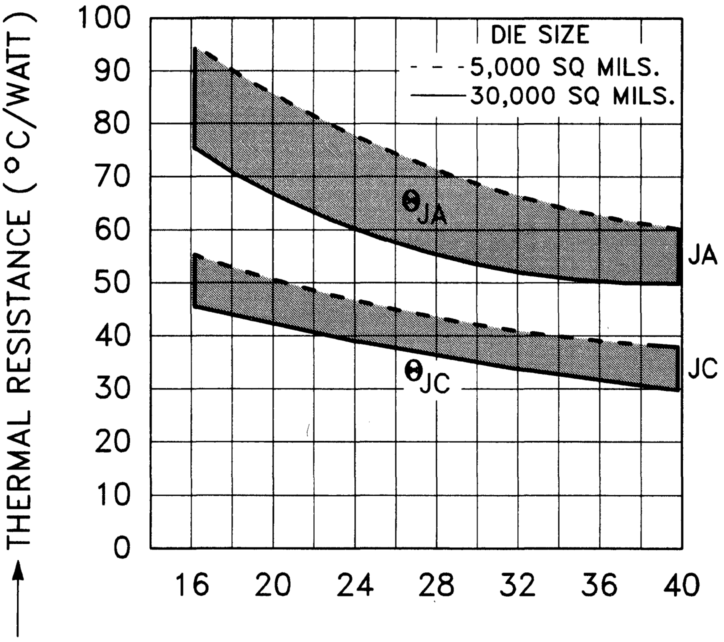
θ_{JA} = Junction to ambient thermal resistance

θ_{CA} = Case to ambient thermal resistance

The junction-to-ambient environment is a still-air environment where the device is inserted into a low-cost standard device socket and mounted on a standard .062″ G10 PC board. For junction-to-case measurements, the same assembly is immersed into a constant temperature liquid reservoir approaching infinite heat sinking for the heat dissipated from the package surface.

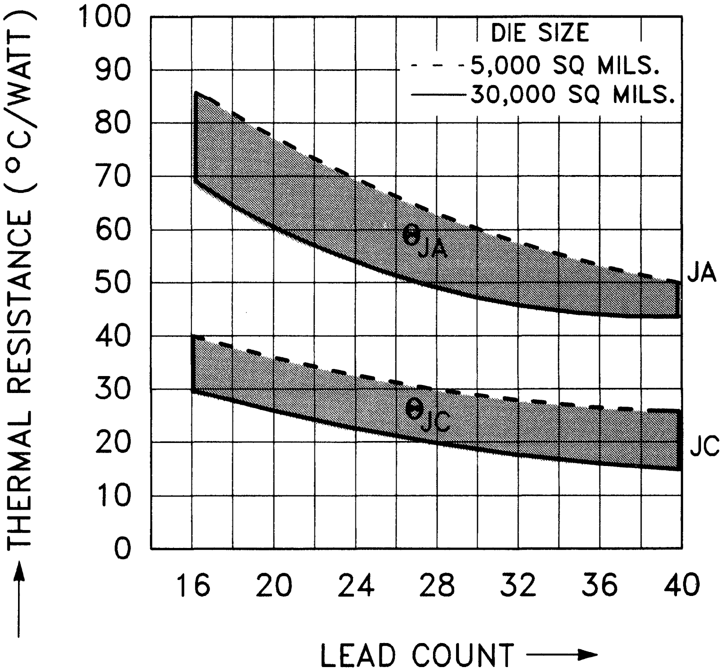
The thermal resistance values of Cypress standard packages are graphically illustrated in *Figures 4* through *7*. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary = 5000 Mils^2, lower boundary = 30,000 Mils^2) in their thermally optimized packaging environment.

All thermal characteristics are measured using the TSP (Temperature Sensitive Parameter) test method described in MIL STD 883C, Method 1012.1. A thermal silicon test chip, containing a 25Ω diffused resistor to heat the chip and a calibrated TSP diode to measure the junction temperature, is used for all characterizations.



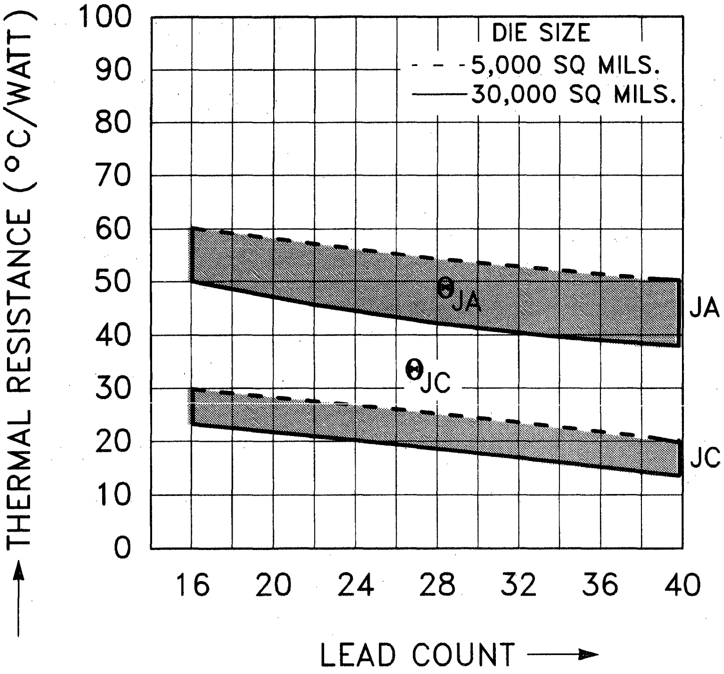
0064-2

Figure 4. Thermal Resistance of Cypress Plastic DIP Packages



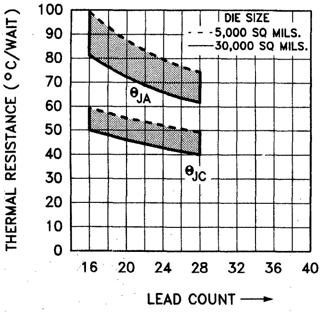
0064-3

Figure 5. Thermal Resistance of Cypress Cerdip Packages



0064-4

Figure 6. Thermal Resistance of Cypress Hermetic Chip Carriers (HLCC)



0064-5

Figure 7. Thermal Resistance of Cypress SOICs

Packaging Materials

CYPRESS PLASTIC PACKAGES INCORPORATE:

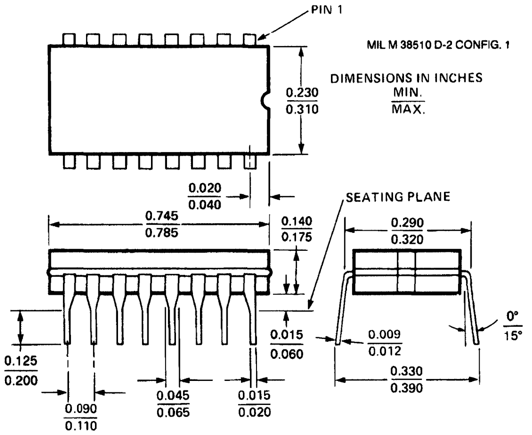
- High thermal conductivity copper lead frame.
- Molding compound with high thermal conductivity.
- Silver filled conductive epoxy as die attach material.
- Gold bond wires.

CYPRESS CERDIP PACKAGES INCORPORATE:

- High conductivity Alumina substrates.
- Silver filled glass as die attach material.
- Alloy 42 lead frame.
- Aluminum bond wires.

Package Diagrams

16 Lead (300 MIL) Cerdip D2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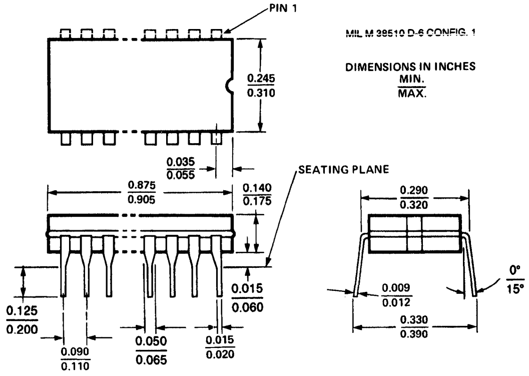
0.310
0.020
0.040
0.745
0.785
0.140
0.175
SEATING PLANE
0.290
0.320
0.125
0.200
0.015
0.060
0.009
0.012
0°
15°
0.330
0.390
0.045
0.065
0.015
0.020
0.090
0.110

MIL M 38510 D-2 CONFIG. 1

DIMENSIONS IN INCHES
MIN.
MAX.

18 Lead (300 MIL) Cerdip D4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0.035
0.055
0.875
0.905
0.140
0.175
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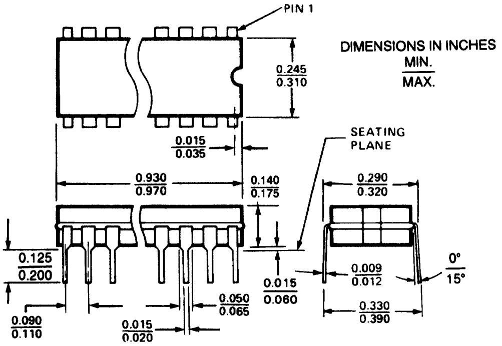
0.015
0.060
0.125
0.200
0.009
0.012
0°
15°
0.330
0.390
0.050
0.065
0.015
0.020
0.090
0.110

MIL M 38510 D-6 CONFIG. 1

DIMENSIONS IN INCHES
MIN.
MAX.

20 Lead (300 MIL) Cerdip D6

MIL M 38510 D-8 CONFIG. 1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0.970
0.140
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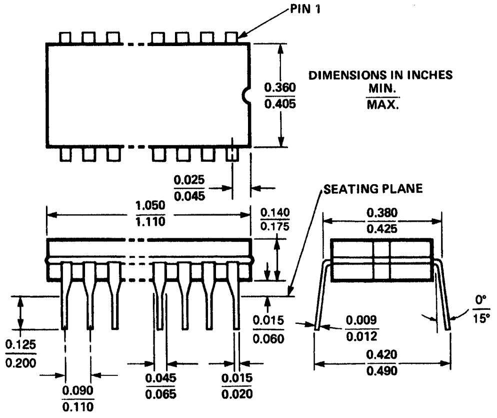
0.125
0.200
0.015
0.060
0.009
0.012
0°
15°
0.050
0.065
0.330
0.390
0.090
0.110
0.015
0.020

DIMENSIONS IN INCHES
MIN.
MAX.

22 Lead (400 MIL) Cerdip D8

MIL M 38510 D-7 CONFIG. 1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0.405
0.025
0.045
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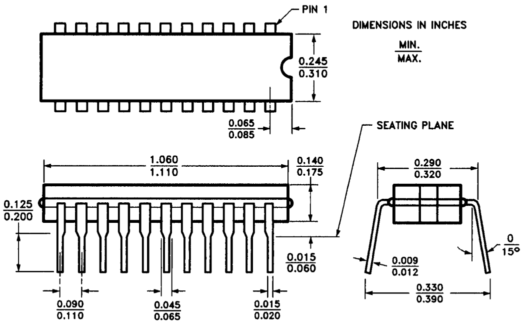
1.050
1.110
0.140
0.175
0.380
0.425
0°
15°
0.015
0.060
0.009
0.012
0.125
0.200
0.420
0.490
0.045
0.065
0.015
0.020
0.090
0.110

DIMENSIONS IN INCHES
MIN.
MAX.

22 Lead (300 MIL) Cerdip D10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MAX.
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0.310
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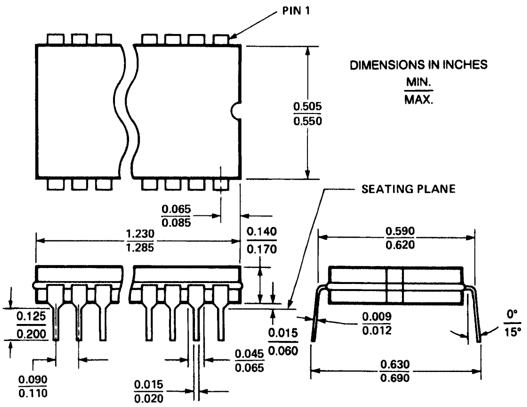
0.085
SEATING PLANE
1.060
1.110
0.140
0.175
0.290
0.320
0.125
0.200
0.015
0.060
0
15°
0.009
0.012
0.330
0.390
0.090
0.110
0.045
0.065
0.015
0.020

24 Lead (600 MIL) Cerdip D12

MIL M 38510 D-3 CONFIG. 1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0.170
0.590
0.620
0.125
0.200
0.015
0.060
0.009
0.012
0°
15°
0.045
0.065
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0.090
0.110
0.015
0.020

24 Lead (300 MIL) Cerdip D14

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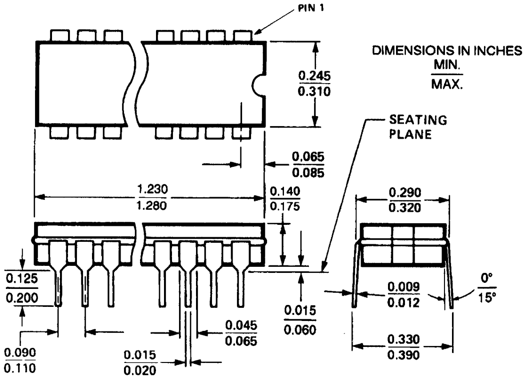
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0.175
0.290
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0.125
0.200
0.009
0.012
0°
15°
0.015
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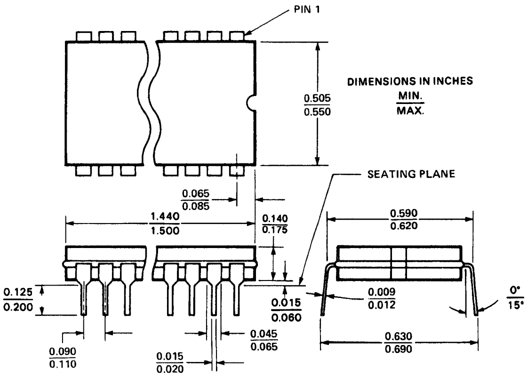
0.065
0.330
0.390
0.090
0.110
0.015
0.020

28 Lead (600 MIL) Cerdip D16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0.590
0.620
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0.200
0.015
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0.009
0.012
0°
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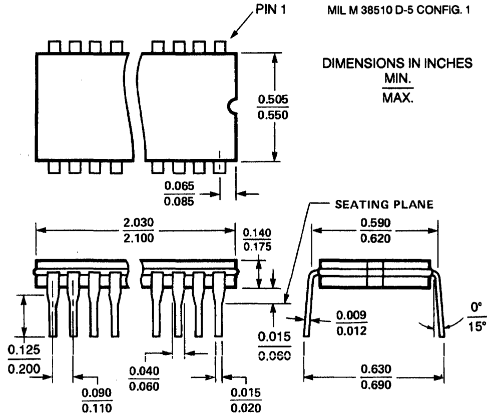
0.020

40 Lead (600 MIL) Cerdip D18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MAX.
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2.100
0.140
0.175
0.590
0.620
0.009
0.012
0°
15°
0.015
0.060
0.125
0.200
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0.060
0.630
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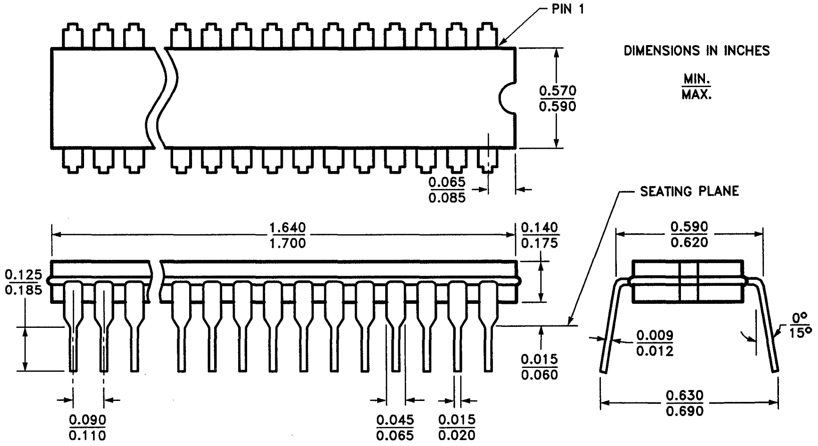
0.090
0.110
0.015
0.020

32 Lead (600 MIL) Cerdip D20 (Preliminary)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0.175
0.590
0.620
0.125
0.185
0°
15°
0.009
0.012
0.015
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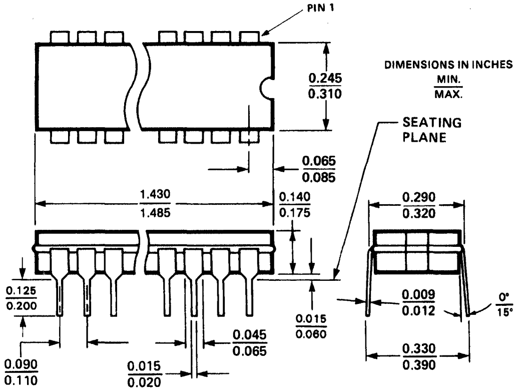
0.065
0.015
0.020

28 Lead (300 MIL) Cerdip D22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0.175
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0.125
0.200
0.009
0.012
0°
15°
0.015
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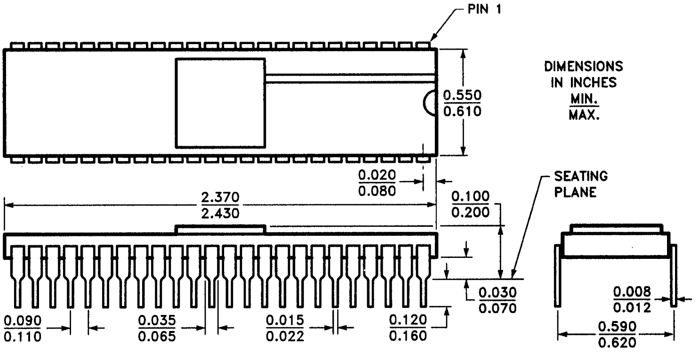
0.015
0.020

48 Lead (600 MIL) Sidebraze DIP D26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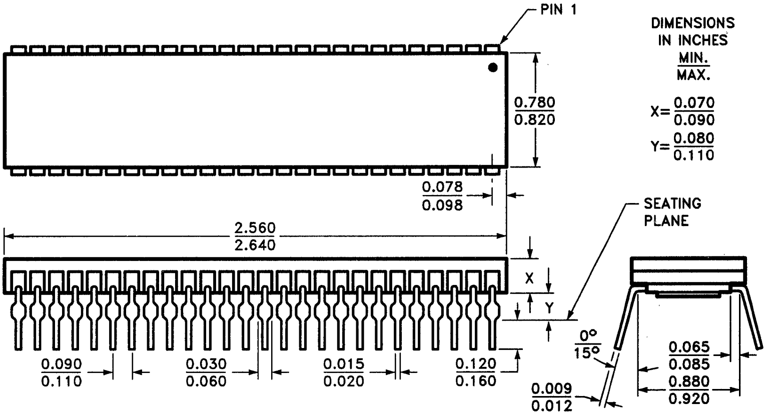
SEATING PLANE
0.030
0.070
0.008
0.012
0.590
0.620
0.090
0.110
0.035
0.065
0.015
0.022
0.120
0.160

52 Lead (900 MIL) Bottombraze DIP D28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MAX.
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Y= 0.080
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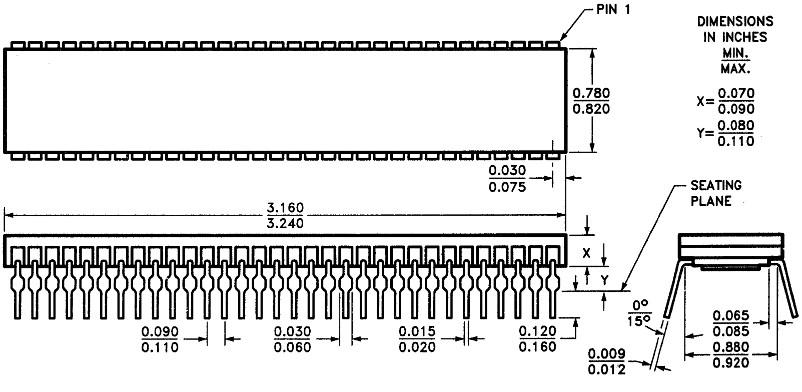
0.820
0.078
0.098
2.560
2.640
SEATING PLANE
X
Y
0°
15°
0.065
0.085
0.880
0.920
0.009
0.012
0.090
0.110
0.030
0.060
0.015
0.020
0.120
0.160

64 Lead (900 MIL) Bottombraze DIP D30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3.160
3.240
SEATING PLANE
X
Y
0°
15°
0.065
0.085
0.880
0.920
0.009
0.012
0.090
0.110
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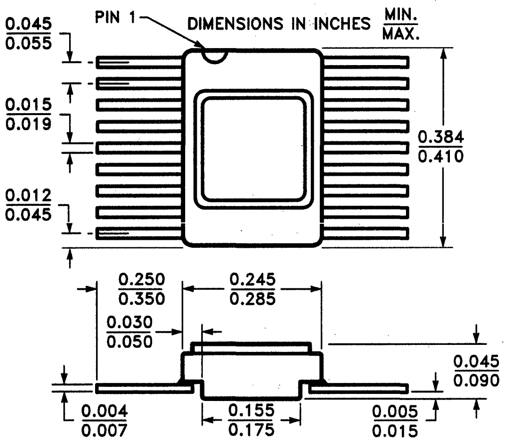
0.015
0.020
0.120
0.160

16 Lead Rectangular Flatpack F69

(MIL-M 38510F F-5 CONFIG 2)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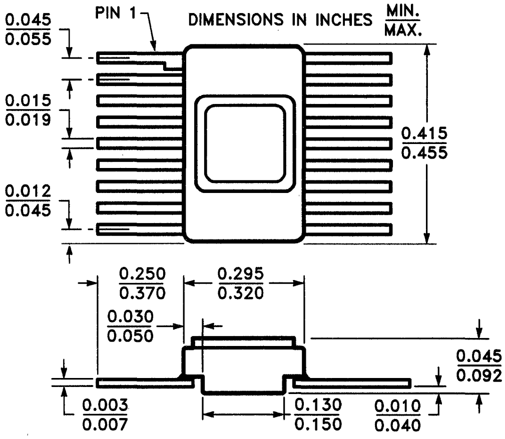
0.012/0.045
0.384/0.410
0.250/0.350
0.245/0.285
0.030/0.050
0.045/0.090
0.004/0.007
0.155/0.175
0.005/0.015

18 Lead Rectangular Flatpack F70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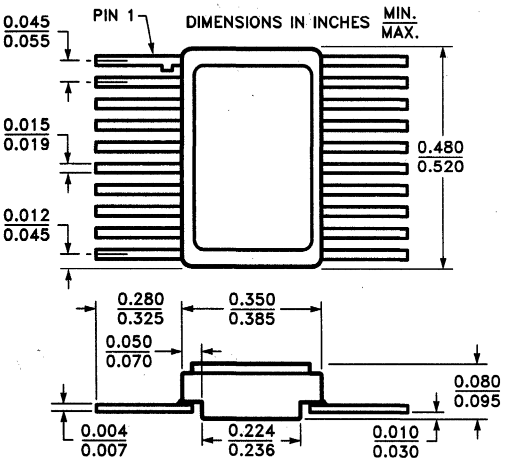
0.015/0.019
0.012/0.045
0.415/0.455
0.250/0.370
0.295/0.320
0.030/0.050
0.045/0.092
0.003/0.007
0.130/0.150
0.010/0.040

20 Lead Rectangular Flatpack F71

(MIL-M 38510 F-9 CONFIG 2)


PIN 1
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0.012/0.045
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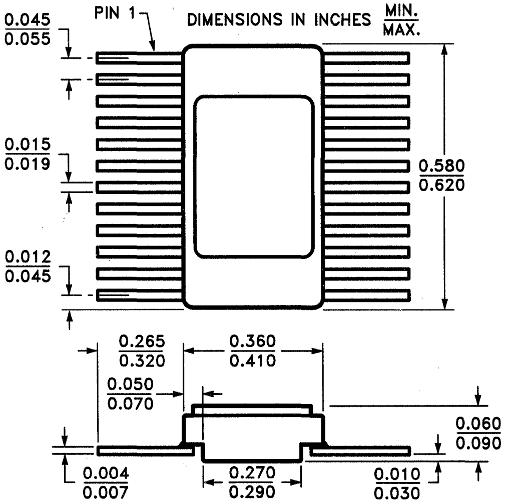
0.350/0.385
0.050/0.070
0.080/0.095
0.004/0.007
0.224/0.236
0.010/0.030

24 Lead Rectangular Flatpack F73

(MIL-M 38510 F-6 CONFIG 2)


PIN 1
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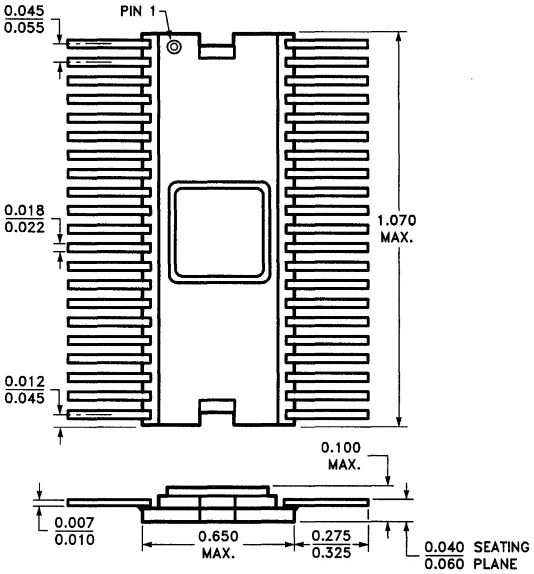
0.012/0.045
0.580/0.620
0.265/0.320
0.360/0.410
0.050/0.070
0.060/0.090
0.004/0.007
0.270/0.290
0.010/0.030

42 Lead Rectangular Flatpack F76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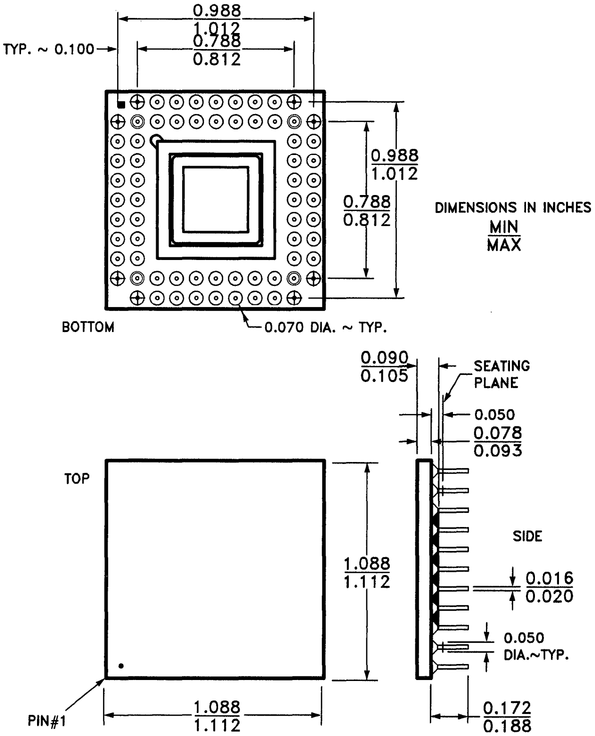
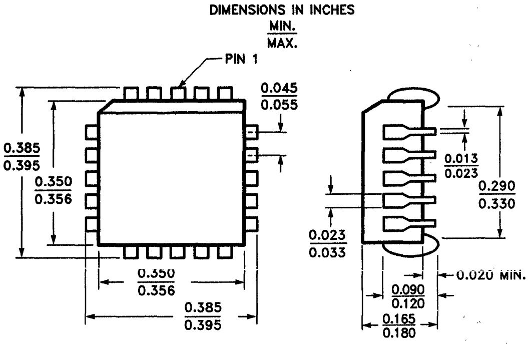
PIN 1
0.018
0.022
1.070
MAX.
0.012
0.045
0.100
MAX.
0.007
0.010
0.650
MAX.
0.275
0.325
0.040 SEATING
0.060 PLANE

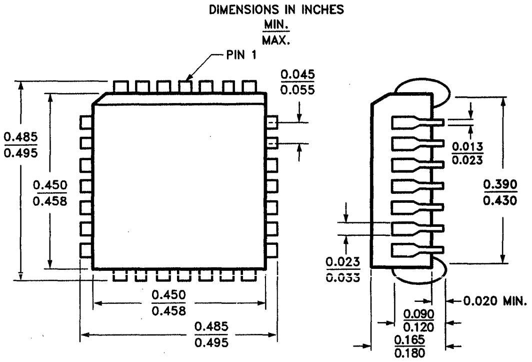
68 Pin Grid Array Package G68


0.988
1.012
0.788
0.812
TYP. ~ 0.100
0.988
1.012
0.788
0.812
DIMENSIONS IN INCHES
MIN
MAX
BOTTOM
0.070 DIA. ~ TYP.
0.090
0.105
SEATING
PLANE
0.050
0.078
0.093
TOP
SIDE
1.088
1.112
0.016
0.020
0.050
DIA.~TYP.
PIN#1
1.088
1.112
0.172
0.188

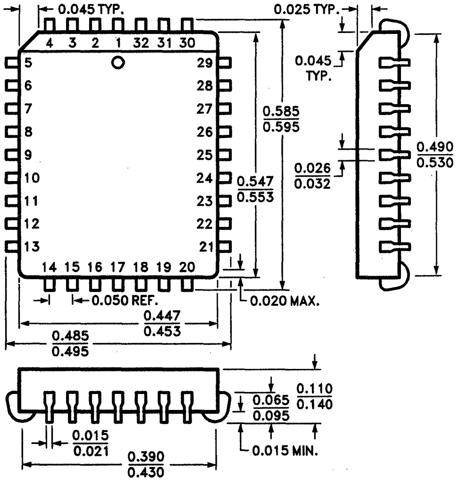
20 Lead Plastic Leadless Chip Carrier J61


DIMENSIONS IN INCHES
MIN.
MAX.
PIN 1
0.045
0.055
0.385
0.395
0.350
0.356
0.013
0.023
0.290
0.330
0.023
0.033
0.350
0.356
0.385
0.395
0.020 MIN.
0.090
0.120
0.165
0.180

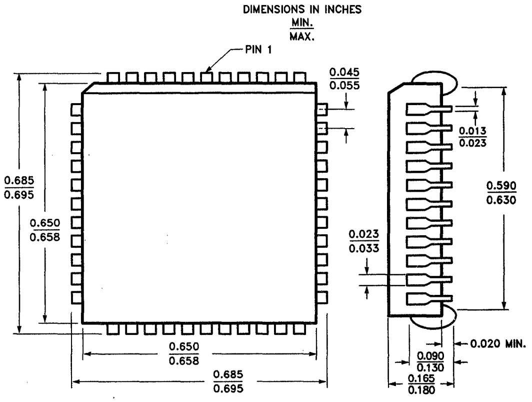
28 Lead Plastic Leadless Chip Carrier J64


DIMENSIONS IN INCHES
MIN.
MAX.
PIN 1
0.045
0.055
0.485
0.495
0.450
0.458
0.013
0.023
0.390
0.430
0.023
0.033
0.450
0.458
0.485
0.495
0.020 MIN.
0.090
0.120
0.165
0.180

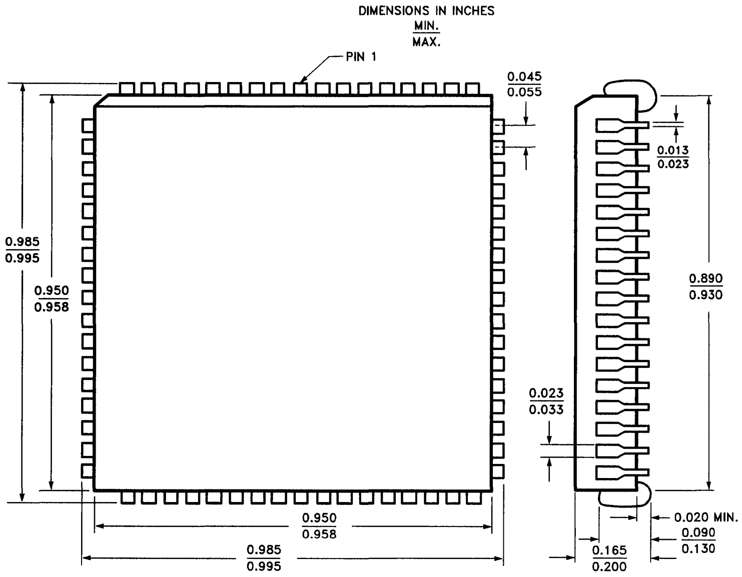
32 Lead Plastic Leadless Chip Carrier J65


0.045 TYP.
0.025 TYP.
4 3 2 1 32 31 30
5
6
7
8
9
10
11
12
13
29
28
27
26
25
24
23
22
21
14 15 16 17 18 19 20
0.045
TYP.
0.585
0.595
0.490
0.530
0.026
0.032
0.547
0.553
0.050 REF.
0.020 MAX.
0.447
0.453
0.485
0.495
0.110
0.140
0.065
0.095
0.015
0.021
0.390
0.430
0.015 MIN.

44 Lead Plastic Leadless Chip Carrier J67

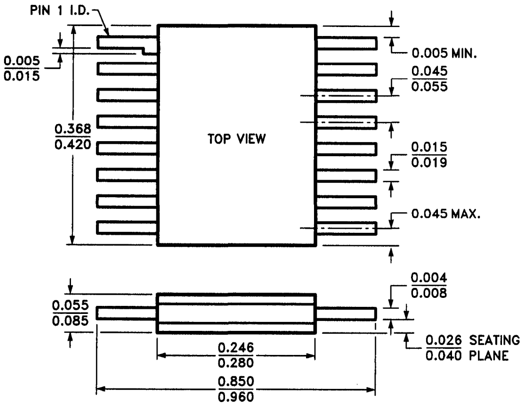

DIMENSIONS IN INCHES
MIN.
MAX.
PIN 1
0.045
0.055
0.685
0.695
0.650
0.658
0.013
0.023
0.590
0.630
0.023
0.033
0.650
0.658
0.685
0.695
0.020 MIN.
0.090
0.130
0.165
0.180

68 Lead Plastic Leadless Chip Carrier J81


DIMENSIONS IN INCHES
MIN.
MAX.
PIN 1
0.045
0.055
0.013
0.023
0.985
0.995
0.950
0.958
0.890
0.930
0.023
0.033
0.020 MIN.
0.090
0.130
0.165
0.200
0.950
0.958
0.985
0.995

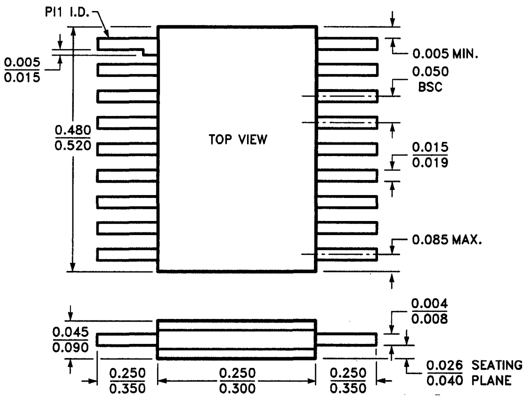
16 Lead Rectangular Cerpack K69

(MIL-M 38510 F-5 CONFIG 1)


PIN 1 I.D.
0.005
0.015
0.368
0.420
TOP VIEW
0.005 MIN.
0.045
0.055
0.015
0.019
0.045 MAX.
0.055
0.085
0.004
0.008
0.026 SEATING
0.040 PLANE
0.246
0.280
0.850
0.960

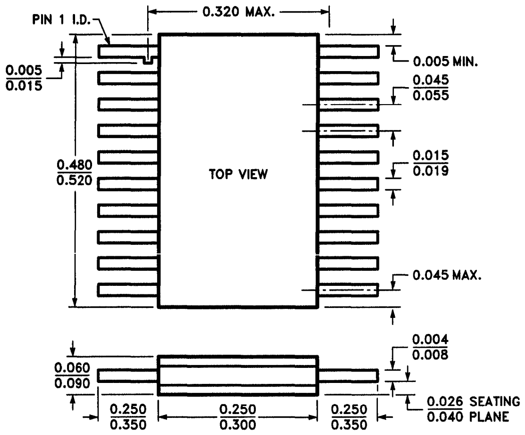
18 Lead Rectangular Cerpack K70

(MIL-M 38510F F-10)


PI1 I.D.
0.005
0.015
0.480
0.520
TOP VIEW
0.005 MIN.
0.050
BSC
0.015
0.019
0.085 MAX.
0.045
0.090
0.004
0.008
0.026 SEATING
0.040 PLANE
0.250
0.350
0.250
0.300
0.250
0.350

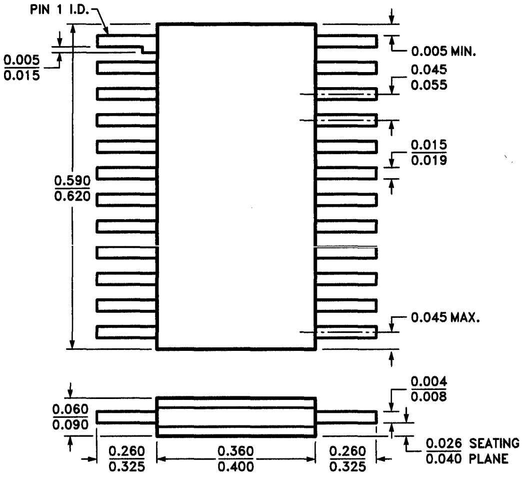
20 Lead Rectangular Cerpack K71

(MIL-M 38510F F-9 CONFIG 1)


PIN 1 I.D.
0.320 MAX.
0.005
0.015
0.005 MIN.
0.045
0.055
0.015
0.019
0.480
0.520
TOP VIEW
0.045 MAX.
0.004
0.008
0.060
0.090
0.250
0.350
0.250
0.300
0.250
0.350
0.026 SEATING
0.040 PLANE

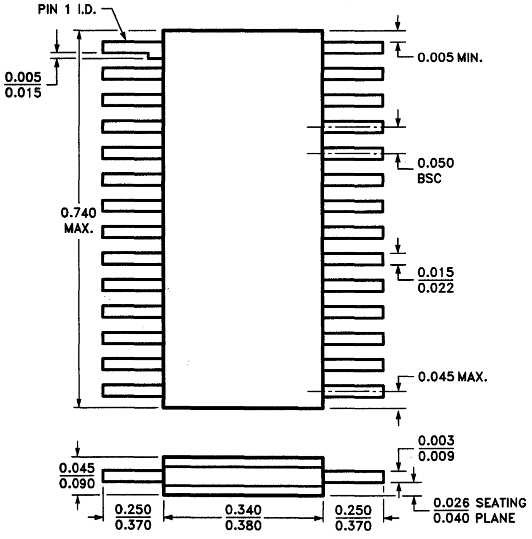
24 Lead Rectangular Cerpack K73

(MIL-M 38510F F-6 CONFIG 1)

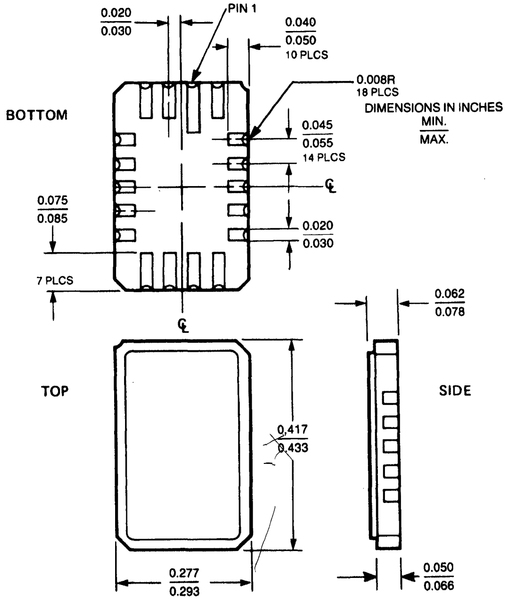

PIN 1 I.D.
0.005
0.015
0.005 MIN.
0.045
0.055
0.015
0.019
0.590
0.620
0.045 MAX.
0.004
0.008
0.060
0.090
0.260
0.325
0.360
0.400
0.260
0.325
0.026 SEATING
0.040 PLANE

28 Lead Rectangular Cerpack K74

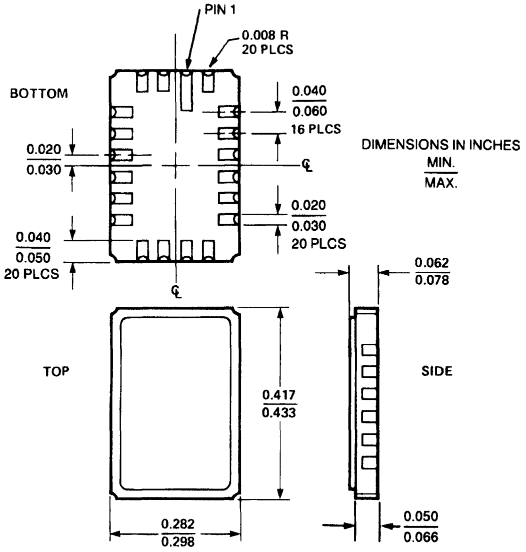
(MIL-M 38510F F-11)


PIN 1 I.D.
0.005
0.015
0.005 MIN.
0.050
BSC
0.740
MAX.
0.015
0.022
0.045 MAX.
0.003
0.009
0.045
0.090
0.250
0.370
0.340
0.380
0.250
0.370
0.026 SEATING
0.040 PLANE

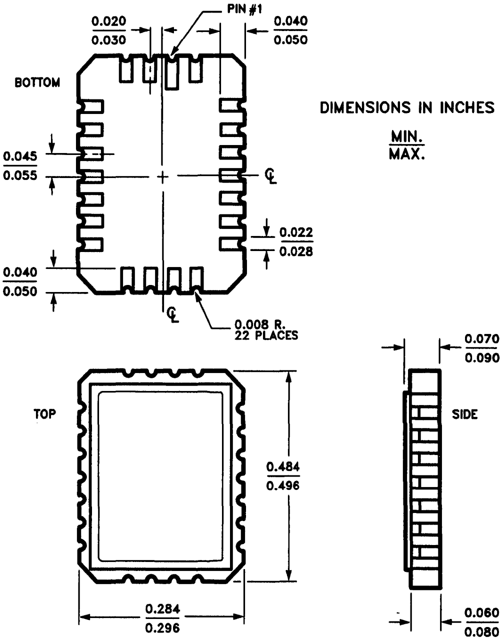
18 Pin Rectangular Leadless Chip Carrier L50


0.020
0.030
PIN 1
0.040
0.050
10 PLCS
0.008R
18 PLCS
DIMENSIONS IN INCHES
MIN.
MAX.
BOTTOM
0.045
0.055
14 PLCS
℄
0.075
0.085
0.020
0.030
7 PLCS
℄
0.062
0.078
TOP
SIDE
0.417
0.433
0.277
0.293
0.050
0.066

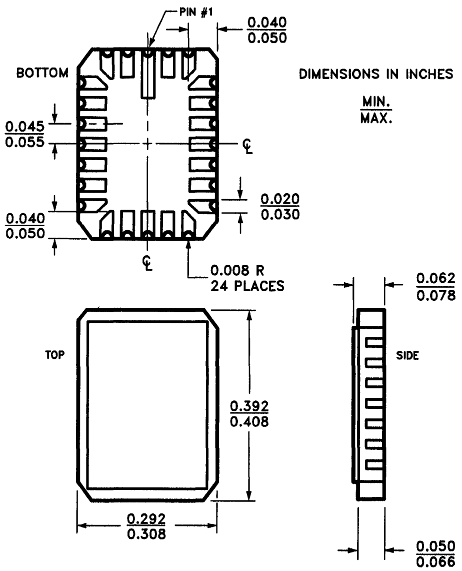
20 Pin Rectangular Leadless Chip Carrier L51


PIN 1
0.008 R
20 PLCS
BOTTOM
0.040
0.060
16 PLCS
0.020
0.030
℄
0.020
0.030
20 PLCS
0.040
0.050
20 PLCS
℄
DIMENSIONS IN INCHES
MIN.
MAX.
0.062
0.078
TOP
SIDE
0.417
0.433
0.282
0.298
0.050
0.066

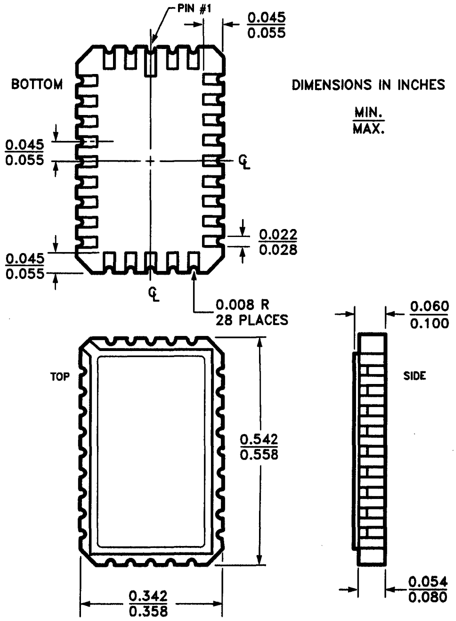
22 Pin Rectangular Leadless Chip Carrier L52


PIN #1
0.020
0.030
0.040
0.050
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.040
0.050
℄
0.008 R.
22 PLACES
0.070
0.090
TOP
SIDE
0.484
0.496
0.284
0.296
0.060
0.080

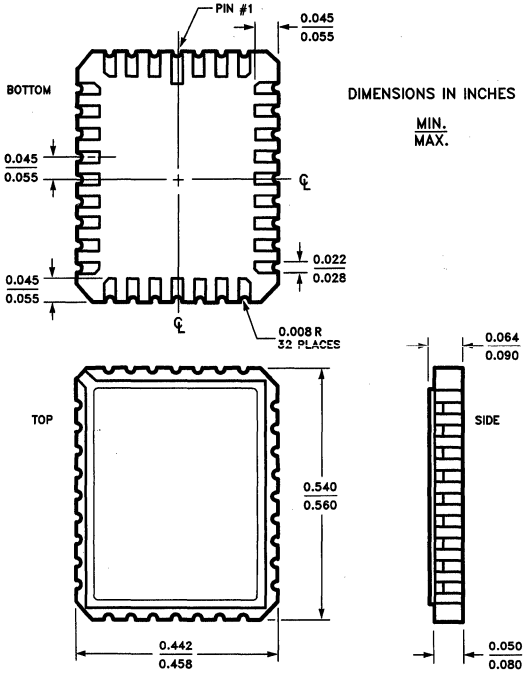
24 Pin Rectangular Leadless Chip Carrier L53


PIN #1
0.040
0.050
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.020
0.030
0.040
0.050
℄
0.008 R
24 PLACES
0.062
0.078
TOP
SIDE
0.392
0.408
0.292
0.308
0.050
0.066

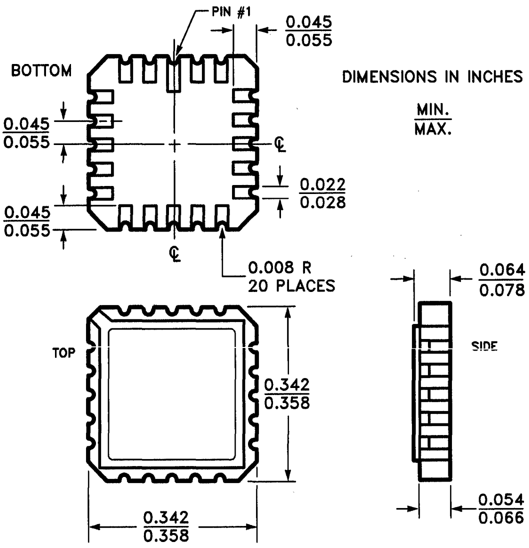
28 Pin Rectangular Leadless Chip Carrier L54


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
28 PLACES
0.060
0.100
TOP
SIDE
0.542
0.558
0.342
0.358
0.054
0.080

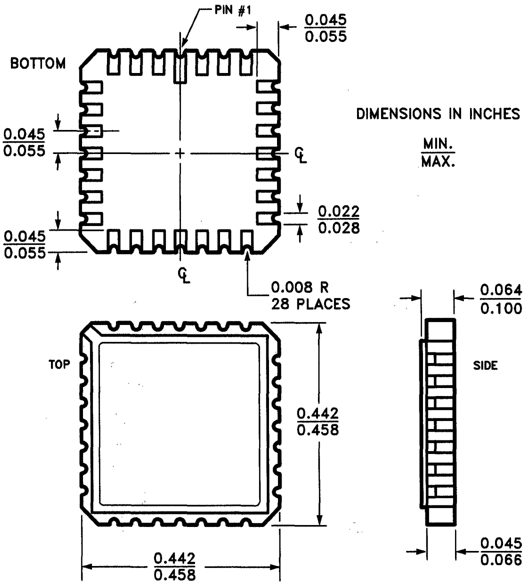
32 Pin Rectangular Leadless Chip Carrier L55


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
32 PLACES
0.064
0.090
TOP
SIDE
0.540
0.560
0.442
0.458
0.050
0.080

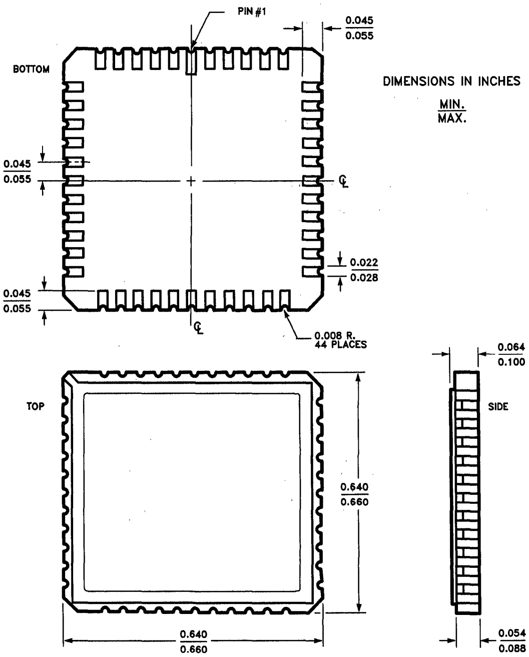
20 Pin Square Leadless Chip Carrier L61


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
20 PLACES
0.064
0.078
TOP
SIDE
0.342
0.358
0.054
0.066
0.342
0.358

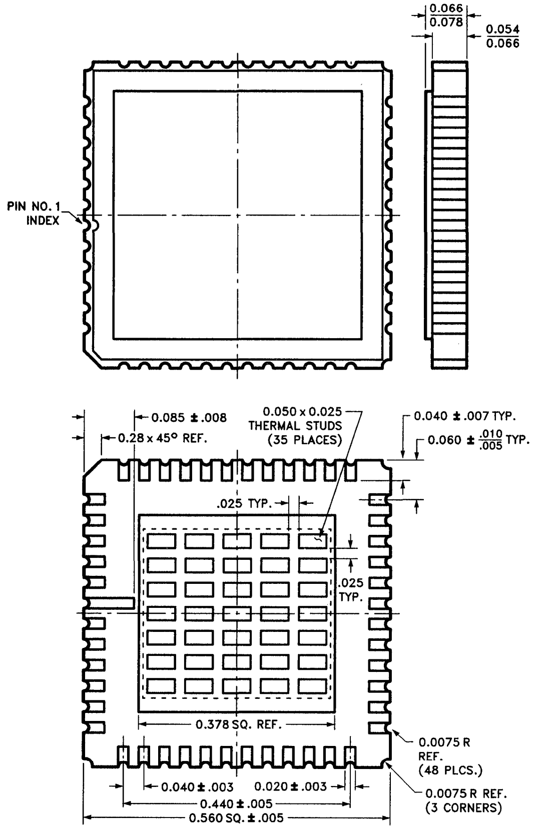
28 Pin Square Leadless Chip Carrier L64


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
28 PLACES
0.064
0.100
TOP
SIDE
0.442
0.458
0.045
0.066
0.442
0.458

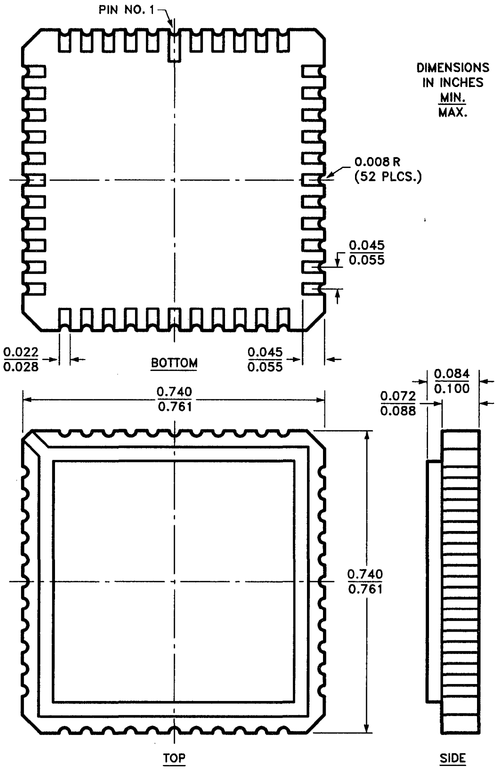
44 Pin Square Leadless Chip Carrier L67


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R.
44 PLACES
0.064
0.100
TOP
SIDE
0.640
0.660
0.640
0.660
0.054
0.088

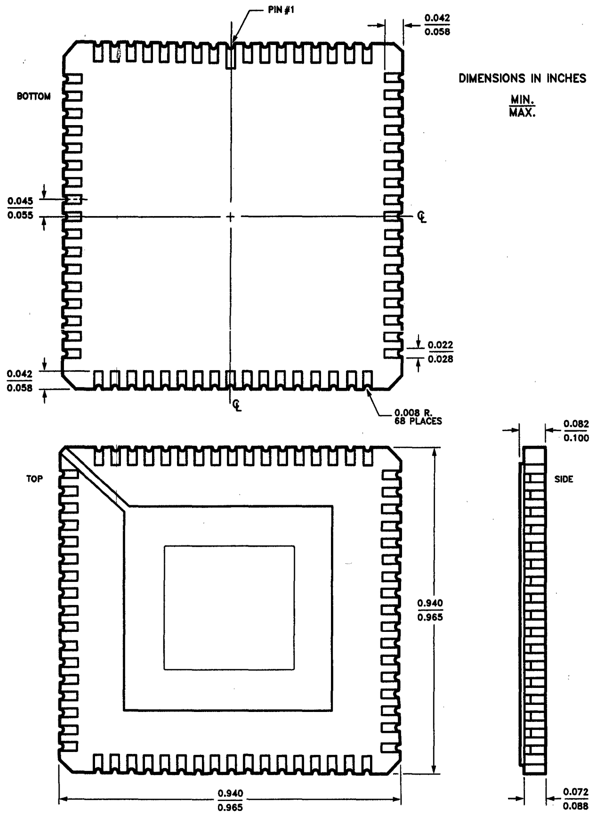
48 Pin Square Leadless Chip Carrier L68


0.066
0.078
0.054
0.066
PIN NO. 1
INDEX
0.085 ±.008
0.28 x 45° REF.
0.050 x 0.025
THERMAL STUDS
(35 PLACES)
0.040 ±.007 TYP.
0.060 ± .010/.005 TYP.
.025 TYP.
.025 TYP.
0.378 SQ. REF.
0.0075 R
REF.
(48 PLCS.)
0.040 ±.003
0.020 ±.003
0.440 ±.005
0.560 SQ. ±.005
0.0075 R REF.
(3 CORNERS)

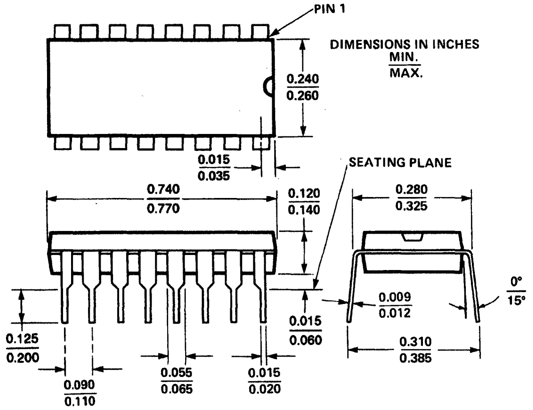
52 Pin Square Leadless Chip Carrier L69


PIN NO. 1
DIMENSIONS
IN INCHES
MIN.
MAX.
0.008 R
(52 PLCS.)
0.045
0.055
0.022
0.028
BOTTOM
0.045
0.055
0.740
0.761
0.072
0.088
0.084
0.100
0.740
0.761
TOP
SIDE

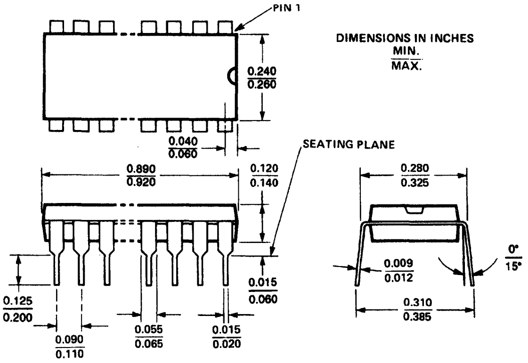
68 Pin Square Leadless Chip Carrier L81


PIN #1
0.042
0.058
DIMENSIONS IN INCHES
MIN.
MAX.
BOTTOM
0.045
0.055
℄
0.022
0.028
0.042
0.058
℄
0.008 R.
68 PLACES
0.082
0.100
SIDE
TOP
0.940
0.965
0.940
0.965
0.072
0.088

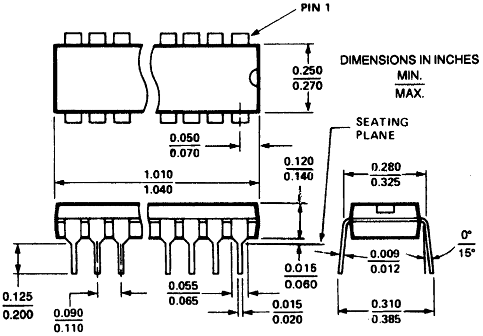
16 Lead (300 MIL) Molded DIP P1


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.240
0.260
0.015
0.035
SEATING PLANE
0.740
0.770
0.120
0.140
0.280
0.325
0°
15°
0.009
0.012
0.015
0.060
0.310
0.385
0.125
0.200
0.090
0.110
0.055
0.065
0.015
0.020

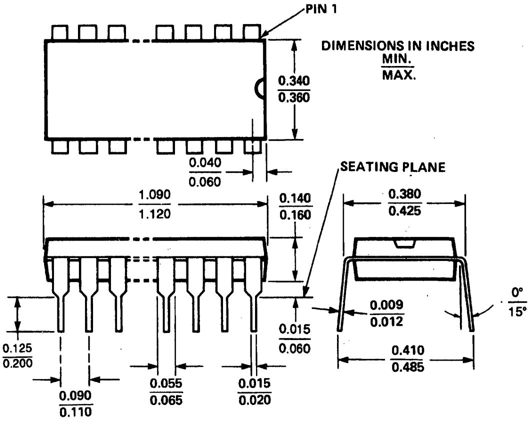
18 Lead (300 MIL) Molded DIP P3


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.240
0.260
0.040
0.060
SEATING PLANE
0.890
0.920
0.120
0.140
0.280
0.325
0°
15°
0.009
0.012
0.015
0.060
0.125
0.200
0.310
0.385
0.090
0.110
0.055
0.065
0.015
0.020

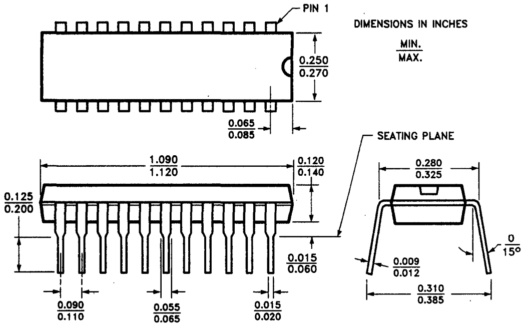
20 Lead (300 MIL) Molded DIP P5


PIN 1
0.250
0.270
DIMENSIONS IN INCHES
MIN.
MAX.
SEATING PLANE
0.050
0.070
1.010
1.040
0.120
0.140
0.280
0.325
0°
15°
0.009
0.012
0.015
0.060
0.125
0.200
0.090
0.110
0.055
0.065
0.015
0.020
0.310
0.385

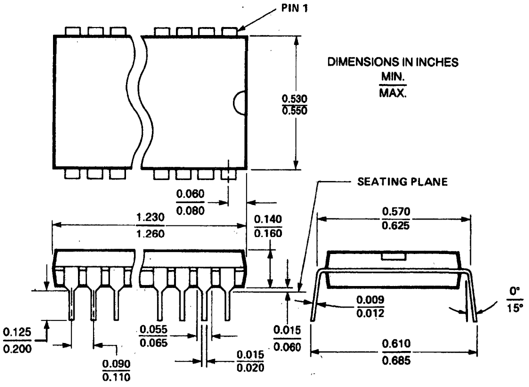
22 Lead (400 MIL) Molded DIP P7


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.340
0.360
SEATING PLANE
0.040
0.060
1.090
1.120
0.140
0.160
0.380
0.425
0°
15°
0.009
0.012
0.015
0.060
0.410
0.485
0.125
0.200
0.090
0.110
0.055
0.065
0.015
0.020

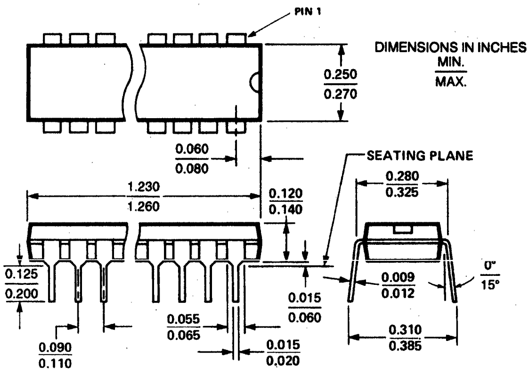
22 Lead (300 MIL) Molded DIP P9


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.250
0.270
0.065
0.085
SEATING PLANE
1.090
1.120
0.120
0.140
0.280
0.325
0.125
0.200
0
15°
0.015
0.060
0.009
0.012
0.310
0.385
0.090
0.110
0.055
0.065
0.015
0.020

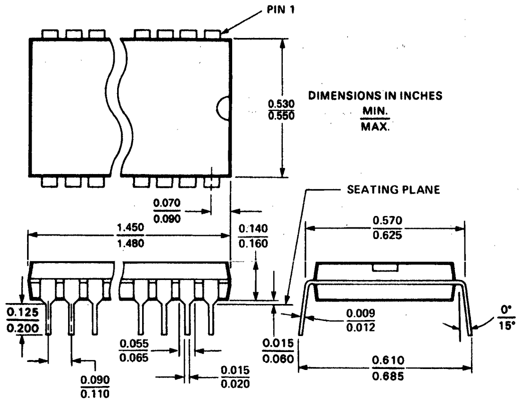
24 Lead (600 MIL) Molded DIP P11


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.530
0.550
SEATING PLANE
0.060
0.080
1.230
1.260
0.140
0.160
0.570
0.625
0°
15°
0.009
0.012
0.125
0.200
0.055
0.065
0.015
0.060
0.610
0.685
0.015
0.020
0.090
0.110

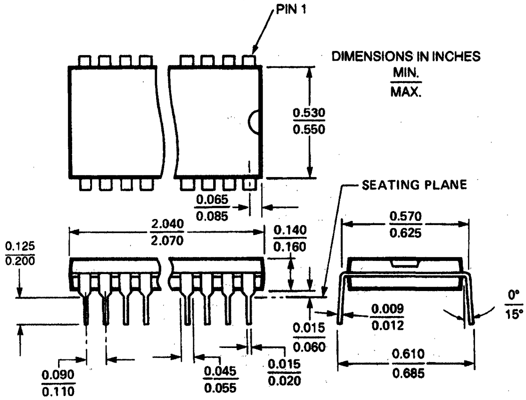
24 Lead (300 MIL) Molded DIP P13


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.250
0.270
0.060
0.080
SEATING PLANE
0.280
0.325
1.230
1.260
0.120
0.140
0.125
0.200
0.009
0.012
0°
15°
0.015
0.060
0.055
0.065
0.310
0.385
0.090
0.110
0.015
0.020

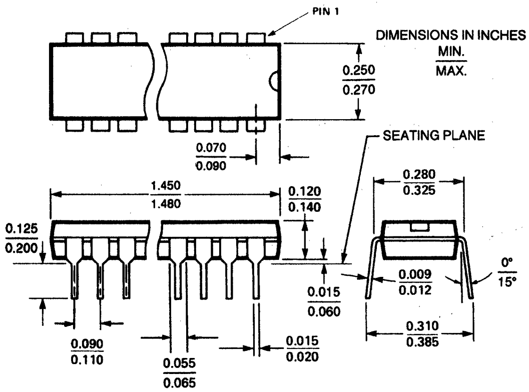
28 Lead (600 MIL) Molded DIP P15


PIN 1
0.530
0.550
DIMENSIONS IN INCHES
MIN.
MAX.
SEATING PLANE
0.070
0.090
1.450
1.480
0.140
0.160
0.570
0.625
0.125
0.200
0.009
0.012
0°
15°
0.055
0.065
0.015
0.060
0.610
0.685
0.015
0.020
0.090
0.110

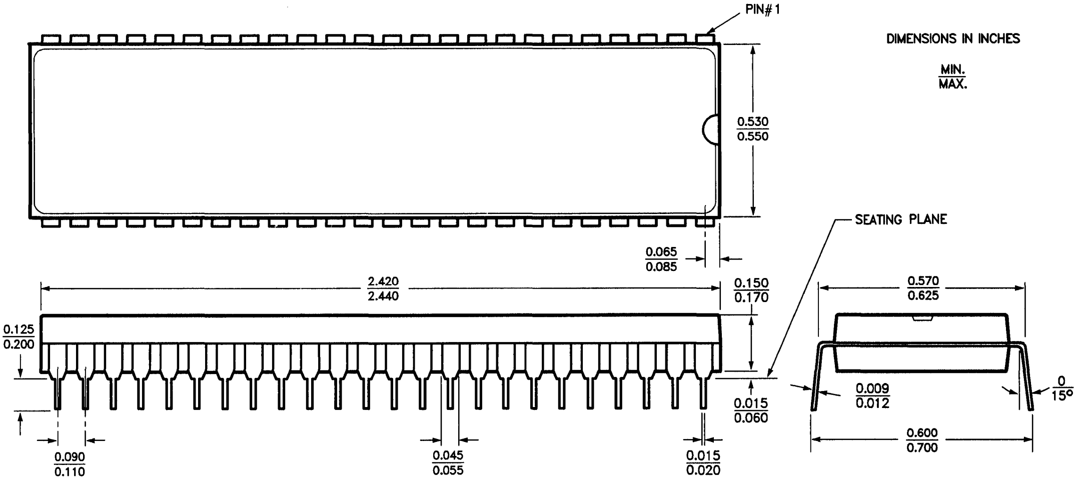
40 Lead (600 MIL) Molded DIP P17


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.530
0.550
SEATING PLANE
0.065
0.085
2.040
2.070
0.140
0.160
0.570
0.625
0.125
0.200
0°
15°
0.009
0.012
0.015
0.060
0.610
0.685
0.090
0.110
0.045
0.055
0.015
0.020

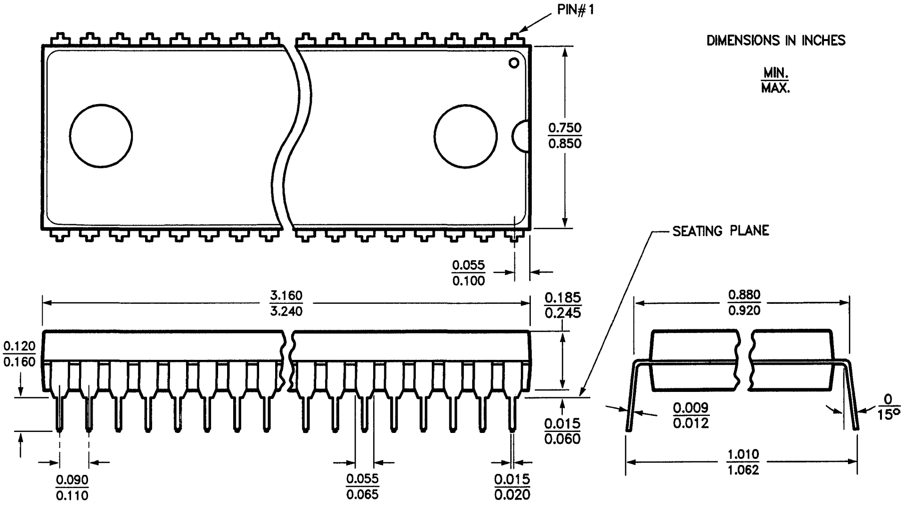
28 Lead (300 MIL) Molded DIP P21


PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.250
0.270
SEATING PLANE
0.070
0.090
0.280
0.325
1.450
1.480
0.120
0.140
0.125
0.200
0°
15°
0.009
0.012
0.015
0.060
0.310
0.385
0.090
0.110
0.015
0.020
0.055
0.065

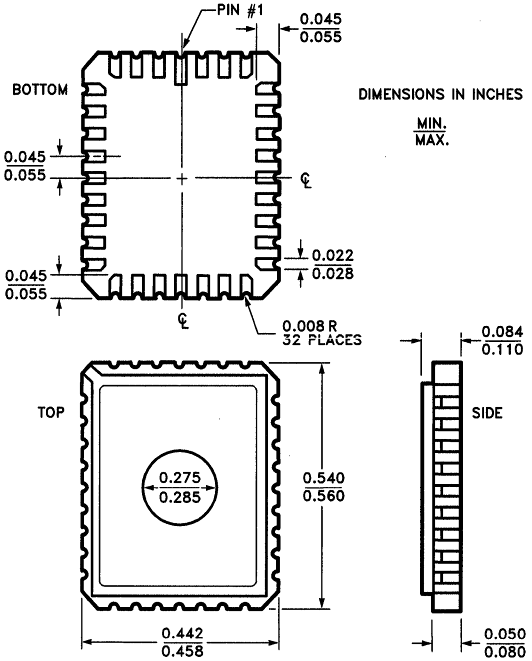
48 Lead (600 MIL) Molded DIP P25


PIN# 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.530
0.550
SEATING PLANE
0.065
0.085
2.420
2.440
0.150
0.170
0.570
0.625
0.125
0.200
0.009
0.012
0
15°
0.015
0.060
0.600
0.700
0.090
0.110
0.045
0.055
0.015
0.020

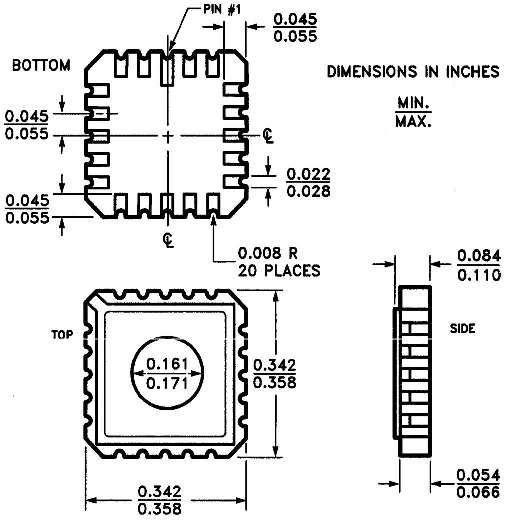
64 Lead (900 MIL) Molded DIP P29


PIN# 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.750
0.850
SEATING PLANE
0.055
0.100
3.160
3.240
0.185
0.245
0.880
0.920
0.120
0.160
0.009
0.012
0
15°
0.015
0.060
1.010
1.062
0.090
0.110
0.055
0.065
0.015
0.020

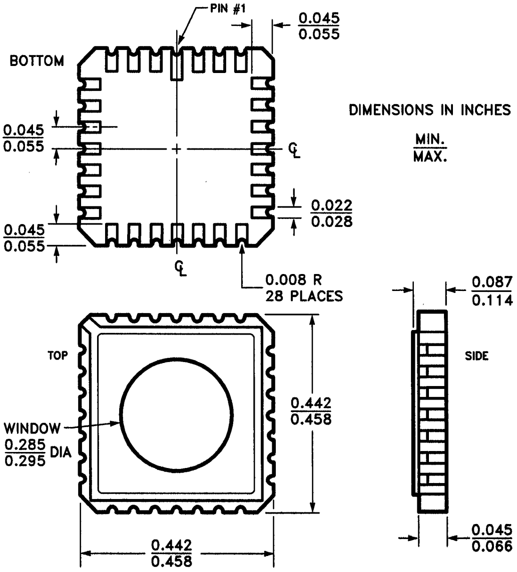
32 Pin Windowed Rectangular Leadless Chip Carrier Q55


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
32 PLACES
0.084
0.110
TOP
SIDE
0.275
0.285
0.540
0.560
0.442
0.458
0.050
0.080

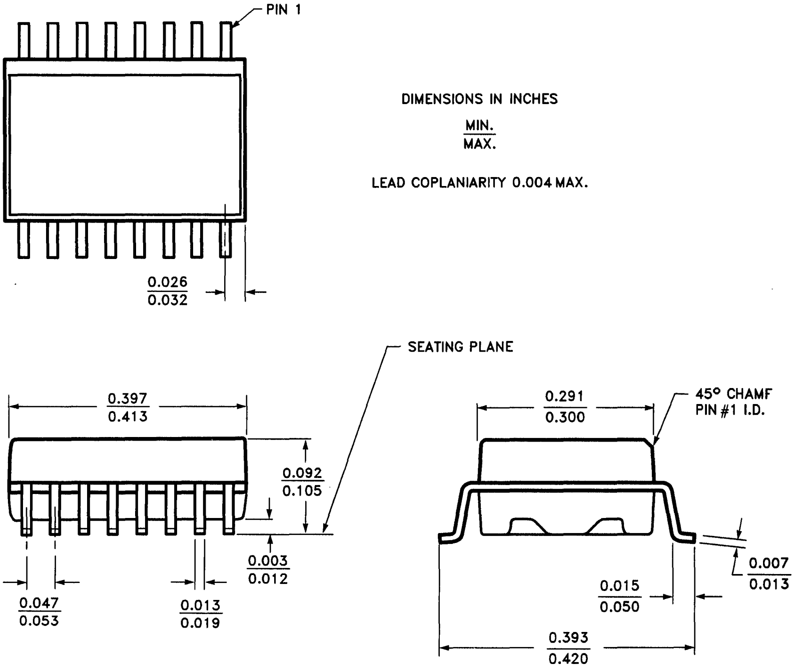
20 Pin Windowed Square Leadless Chip Carrier Q61


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
20 PLACES
0.084
0.110
TOP
0.161
0.171
0.342
0.358
SIDE
0.342
0.358
0.054
0.066

28 Pin Windowed Leadless Chip Carrier Q64


PIN #1
0.045
0.055
BOTTOM
DIMENSIONS IN INCHES
MIN.
MAX.
0.045
0.055
℄
0.022
0.028
0.045
0.055
℄
0.008 R
28 PLACES
0.087
0.114
TOP
SIDE
WINDOW
0.285
0.295
DIA
0.442
0.458
0.442
0.458
0.045
0.066

16 Lead Molded SOIC S1

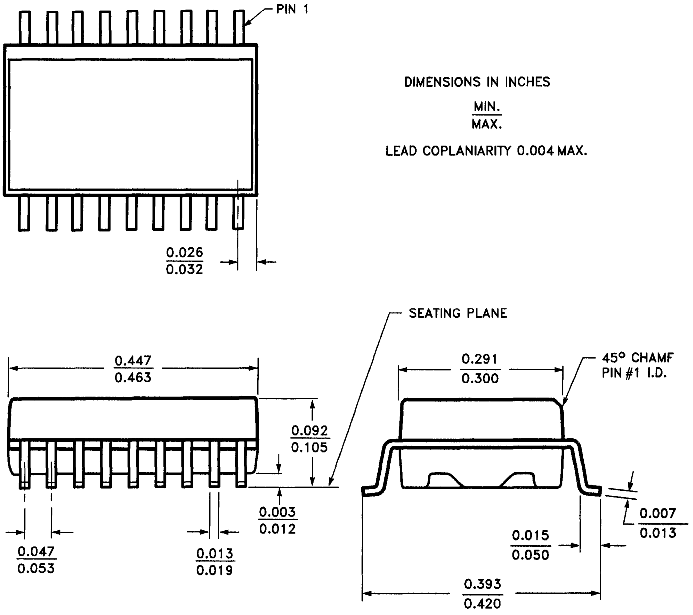

PIN 1
0.026
0.032
SEATING PLANE
0.397
0.413
0.092
0.105
0.003
0.012
0.047
0.053
0.013
0.019
0.291
0.300
45° CHAMF
PIN #1 I.D.
0.007
0.013
0.015
0.050
0.393
0.420

DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.

18 Lead Molded SOIC S3

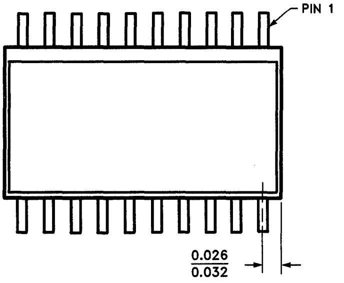

PIN 1
0.026
0.032
SEATING PLANE
0.447
0.463
0.092
0.105
0.003
0.012
0.047
0.053
0.013
0.019
0.291
0.300
45° CHAMF
PIN #1 I.D.
0.007
0.013
0.015
0.050
0.393
0.420

DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.

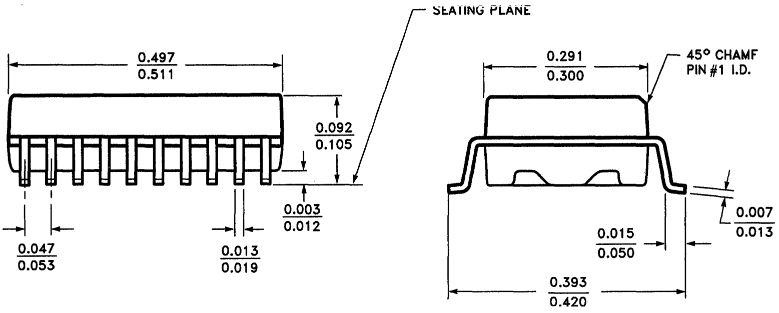
20 Lead Molded SOIC S5


PIN 1
0.026
0.032

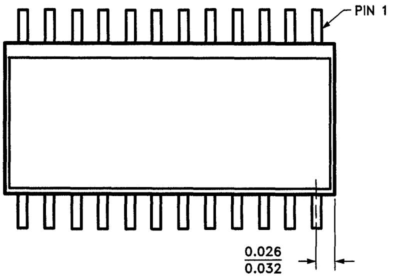
DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.


SEATING PLANE
0.497
0.511
0.092
0.105
0.003
0.012
0.047
0.053
0.013
0.019
0.291
0.300
45° CHAMF
PIN #1 I.D.
0.007
0.013
0.015
0.050
0.393
0.420

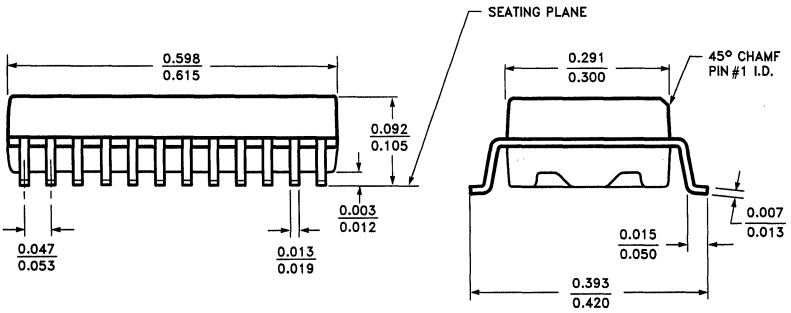
24 Lead Molded SOIC S13


PIN 1
0.026
0.032

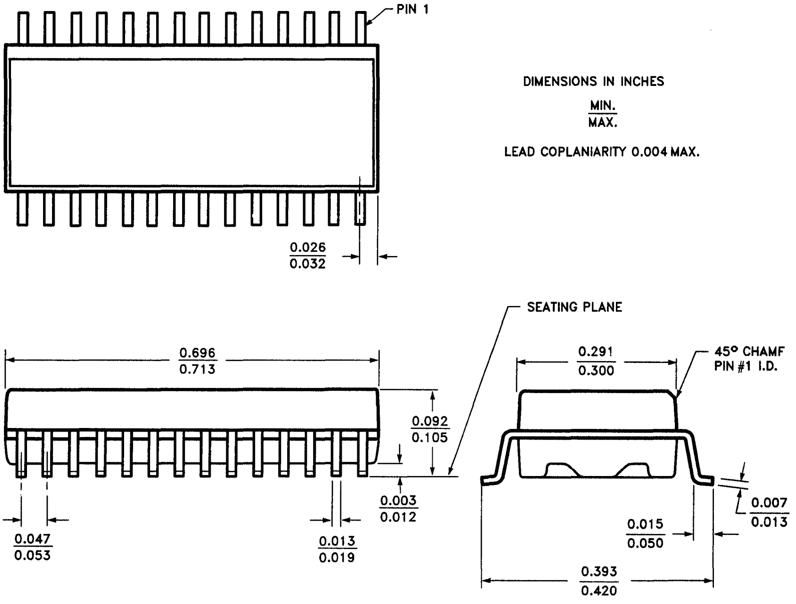
DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.


SEATING PLANE
0.598
0.615
0.092
0.105
0.003
0.012
0.047
0.053
0.013
0.019
0.291
0.300
45° CHAMF
PIN #1 I.D.
0.007
0.013
0.015
0.050
0.393
0.420

28 Lead Molded SOIC S21

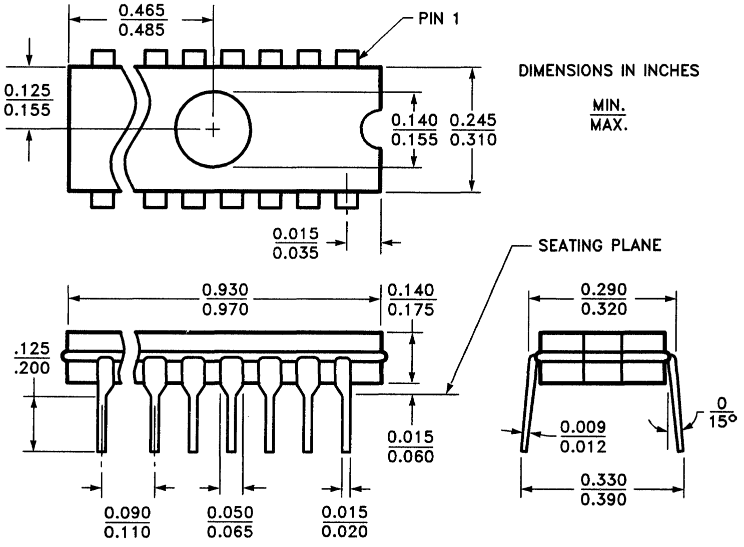

PIN 1
0.026
0.032
SEATING PLANE
0.696
0.713
0.092
0.105
0.003
0.012
0.047
0.053
0.013
0.019
0.291
0.300
45° CHAMF
PIN #1 I.D.
0.007
0.013
0.015
0.050
0.393
0.420

DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.

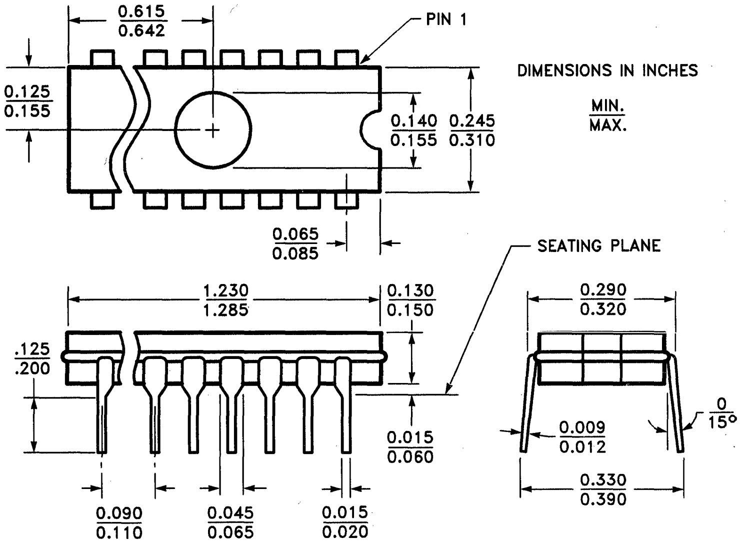
20 Lead Windowed Cerdip W6


0.465
0.485
PIN 1
0.125
0.155
0.140
0.155
0.245
0.310
0.015
0.035
SEATING PLANE
0.930
0.970
0.140
0.175
.125
.200
0.015
0.060
0.090
0.110
0.050
0.065
0.015
0.020
0.290
0.320
0.009
0.012
0
15°
0.330
0.390

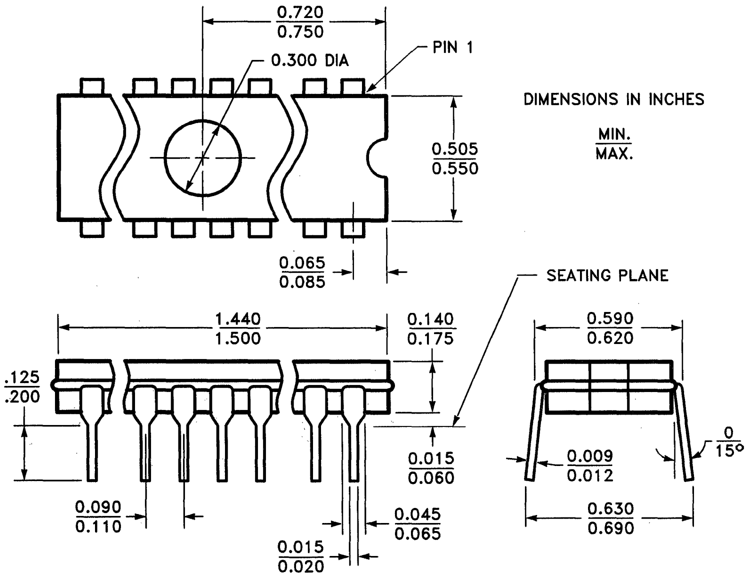
DIMENSIONS IN INCHES

MIN.
MAX.

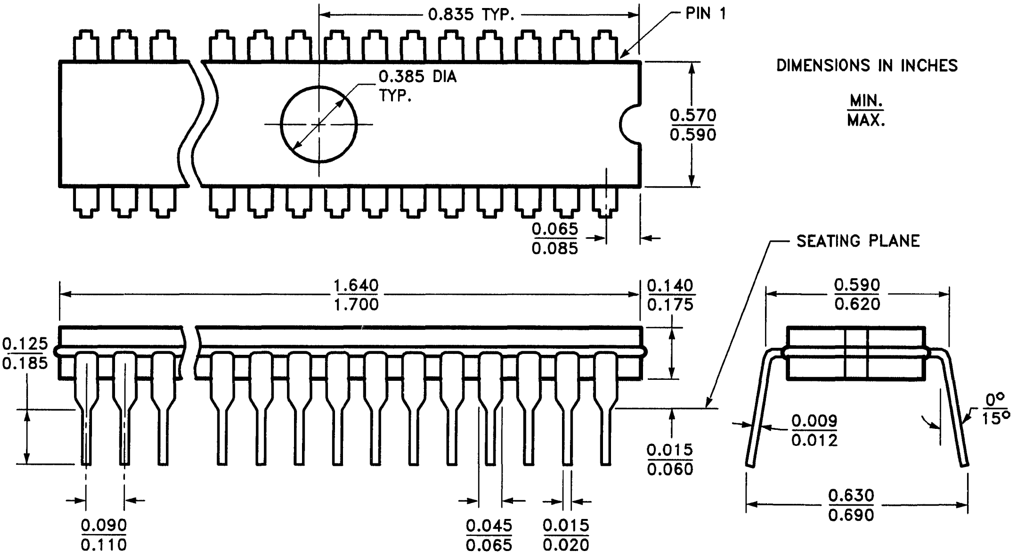
24 Lead Windowed Cerdip W14


0.615
0.642
PIN 1
DIMENSIONS IN INCHES
MIN.
MAX.
0.125
0.155
0.140
0.155
0.245
0.310
0.065
0.085
SEATING PLANE
1.230
1.285
0.130
0.150
0.290
0.320
.125
.200
0
15°
0.009
0.012
0.015
0.060
0.330
0.390
0.090
0.110
0.045
0.065
0.015
0.020

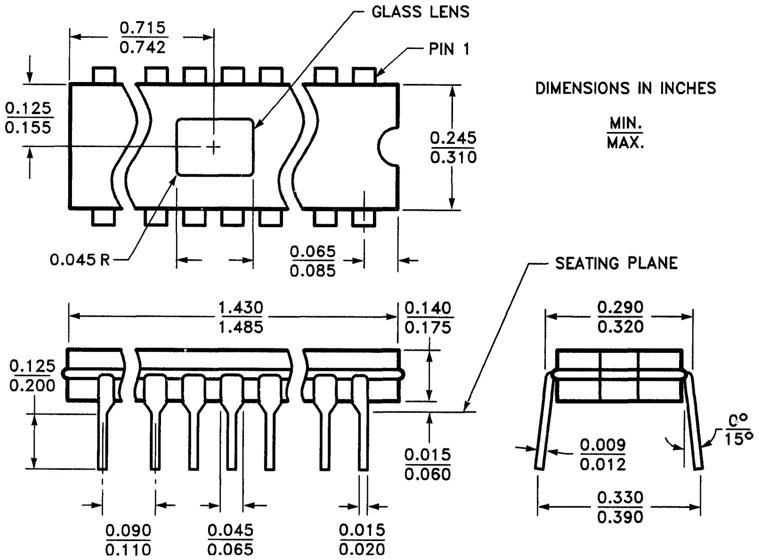
28 Lead (600 MIL) Windowed Cerdip W16


0.720
0.750
PIN 1
0.300 DIA
DIMENSIONS IN INCHES
MIN.
MAX.
0.505
0.550
0.065
0.085
SEATING PLANE
1.440
1.500
0.140
0.175
0.590
0.620
.125
.200
0
15°
0.015
0.060
0.009
0.012
0.090
0.110
0.045
0.065
0.630
0.690
0.015
0.020

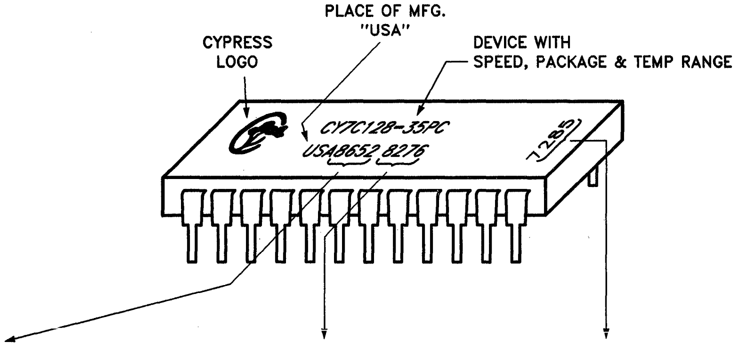
32 Lead (600 MIL) Windowed Cerdip W20 (Preliminary)


0.835 TYP.
PIN 1
0.385 DIA TYP.
DIMENSIONS IN INCHES
MIN.
MAX.
0.570
0.590
0.065
0.085
SEATING PLANE
1.640
1.700
0.140
0.175
0.590
0.620
0.125
0.185
0°
15°
0.009
0.012
0.015
0.060
0.630
0.690
0.090
0.110
0.045
0.065
0.015
0.020

28 Lead Windowed Cerdip W22


GLASS LENS
0.715
0.742
PIN 1
DIMENSIONS IN INCHES
0.125
0.155
MIN.
MAX.
0.245
0.310
0.045 R
0.065
0.085
SEATING PLANE
1.430
1.485
0.140
0.175
0.290
0.320
0.125
0.200
0°
15°
0.009
0.012
0.015
0.060
0.330
0.390
0.090
0.110
0.045
0.065
0.015
0.020

Typical Marking for DIP Packages (P and D Type)


PLACE OF MFG.
"USA"
CYPRESS
LOGO
DEVICE WITH
SPEED, PACKAGE & TEMP RANGE
CY7C128-35PC
USA8652 8276
7285

DATE CODE:

XXYY
XX = YEAR
YY = WORK WEEK
WEEK PARTS WERE MARKED (FOR PLASTIC)
WEEK PARTS WERE SEALED (FOR HERMETIC)

SHIP CODE:

IDENTIFIES SPECIFIC SHIPMENT LOTS TO CUSTOMERS.

ASSEMBLY CODE:

IDENTIFIES THE SPECIFIC ASSEMBLY LOT THE PRODUCT CAME FROM.

0047–1

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(219) 432-5553

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Wichita, KS 67203
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Richfield, OH 44286
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Westerville, OH 43081
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