

1977

A/D CONVERTERS

D/A CONVERTERS

ANALOG MULTIPLEXERS

SAMPLE-HOLD AMPLIFIERS

OPERATIONAL AMPLIFIERS

DC POWER SUPPLIES

DIGITAL PANEL METERS

DIGITAL PANEL PRINTERS

DIGITAL PANEL INSTRUMENTS

DATA LOGGERS

DATA ACQUISITION SYSTEMS

DIGITAL CASSETTE RECORDERS

MOST PRODUCTS IN THIS BROCHURE ARE COVERED BY GSA CONTRACT

Contents

PAGE

Nost Datel Syst Nost Date by are	45
	products.
	ems cont
tel SY	G5.
st Datred I	
Mos cov	PAG
	INTRODUCTION
	DATA CONVERSION DEVICES
	Principles of Data Acquisition and Conversion 6
	A/D Converters 19
	D/A Converters 65
	DATA CONVERSION ACCESSORY CIRCUITS 10
	Analog Multiplexers
	Sample-Hold Circuits
	Operational Amplifiers 120
	Active Filters 144
	V/F and F/V Converters 14
	MODULAR DATA ACQUISITION SYSTEMS 15:
	DC POWER SUPPLIES
	Modular DC Power Supplies
	High Power Open Frame Supplies 172 DC to DC Converters 176
	DC to DC Converters
	DIGITAL COUNTER/TOTALIZER
	DIGITAL TIMER/STOP CLOCK
	DIGITAL TIME CLOCK
	DIGITAL COMPARATORS 22
	DIGITAL VOLTAGE CALIBRATOR
	DIGITAL PANEL PRINTER
	DATA LOGGERS
	COMPUTER COMPATIBLE DATA ACQUISITION
	SYSTEMS 256
	DIGITAL CASSETTE RECORDERS AND SYSTEMS . 270
	OTHER AVAILABLE LITERATURE FROM DATEL . 28
	EXTENDED PERFORMANCE CIRCUITS AND
SVSTEMS INC	MODULES 284
SYSTEMS, INC. 1020G Turnpike Street, Building S	ACCESSORY PRODUCTS 280
Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000	ORDERING GUIDE 28
TWX: 710-348-0135 TELEX: 924461	SALES OFFICES Inside Back Cove



Printed in U.S.A. Copyright[®] 1976 Datel Systems, Inc. All rights reserved.

Introduction

Datel Systems Inc. was founded in February, 1970, and began production of a basic line of A/D converters, D/A converters, miniature power supply modules, and other circuit modules. Since then these basic lines have expanded considerably and many new product lines have been developed. Now in its seventh operating year, Datel Systems holds a leadership position in the areas of data converters, data acquisition systems, digital panel meters, digital panel printers, data logging systems, and power supplies. Although still a young company compared with others in these product areas, Datel has grown rapidly and achieved significant diversification of its product lines. This diversification is significant in assuring the future growth of the company.

A recently added hybrid microelectronics division is dedicated to the production of new lines of high performance hybrid data converters. Datel Systems' modern plant of 75,000 square feet is located on Route 138 in Canton, Massachusetts, just 15 miles southwest of Boston. It is easily accessible from Logan International Airport.

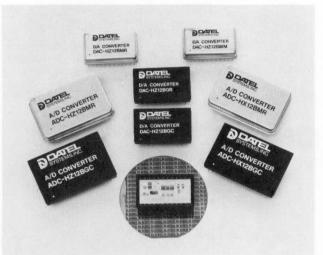
DATEL SYSTEMS' PRODUCTS

Datel Systems' product lines now include the following:

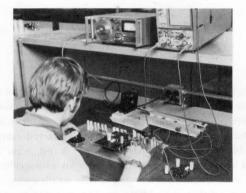
- A/D Converters
 - D/A Converters
- Sample Holds
- Analog Multiplexers
- Operational Amplifiers
- Instrumentation Amplifiers
- Active Filters
- Computer Analog Peripheral
 Systems
- Digital Panel Meters
- Digital Parlet Weters
- Data Acquisition Systems
- Data Logging Systems
- Power Supplies
- V/F Converters
- Digital Control Instruments
 Digital Panel Printers
- Digital Cassette Transports and Systems

Datel Systems' reputation in these product areas has been established by the tens of thousands of products presently in use throughout the world. These products are used in a wide variety of applications from military and government systems to industrial, scientific, medical, environmental, and oceanographic systems.

Product reliability is an important part of any company's reputation. Reliability at Datel Systems begins with conservative engineering design, use of quality pre-tested components, manufacturing methods with built-in checking procedures, and sufficient product electrical tests at the proper stages of the manufacturing cycle. These procedures in conjunction with a fully implemented Quality Assurance Program have resulted in an extremely low return rate for delivered products.



About this Product Handbook



NEW PRODUCTS

Over the past year Datel Systems has introduced a significant number of new products. Some of these products are:

- A line of high performance hybrid 12 bit A/D and D/A converters (DAC-HZ, ADC-HZ, and ADC-HX series)
- A new portable data logging instrument for field use (DL-2)
- Industry's fastest 12 bit A/D converter with a 2 μsec. conversion time (ADC-EH12B3)
- A new low cost 3-1/2 digit DPM selling for \$59.00 in quantities of 100 (DM-350)
- A new ultra low-power incremental digital cassette transport (ICT Series)
- A new line of digital control instruments for industrial timing and control applications (8000 Series)
- A new high resolution, isolated, ratiometric dual slope converter series (ADC-EP Series)
- A low-cost modular data acquisition system featuring 16 channels, 12 bit resolution and 50 kHz throughput rate.

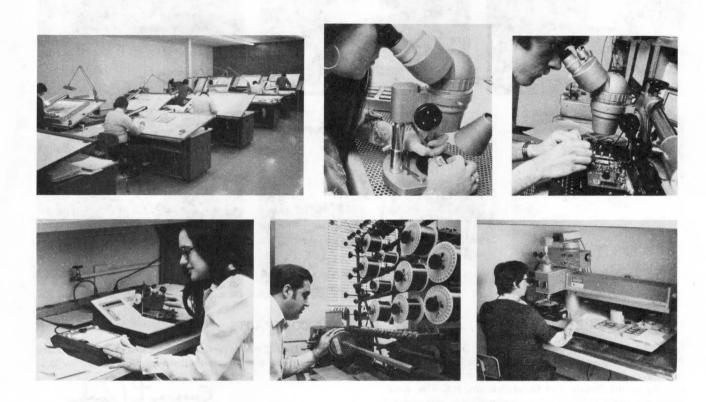
Watch for future new products from Datel Systems announced and advertised in the electronics trade journals. New products are also discussed in detail in the periodical, "Datel Digest".

ABOUT THIS PRODUCT HANDBOOK

This new edition of Datel's Engineering Product Handbook is written primarily for the systems and circuit design engineer who requires a substantial amount of technical information about products in order to select and apply the right product in his specific requirement. The goal of this product handbook, therefore, has been to present detailed technical data in an easily readable form in order to simplify the product evaluation and selection process.

This edition, however, is a departure in format from previous editions. We have here, for the first time, combined product data in tabular form with product data sheets. Not all Datel Systems' product data sheets are included here, but our most significant products are included. Other data sheets may be obtained by contacting the factory or Datel's nearest sales office.

The product evaluation and selection process in most cases can be shortened by referring first to the specification tables in order to compare performance and pricing, and then going to the appropriate data sheet section of the catalog. In all cases the data sheets of a particular product category immediately follow the specification tables.



Also included in this product handbook is a 13 page section entitled "Principles of Data Acquisition and Conversion" which is basic background material about the operation and application of the products described in this catalog. This material will serve as both a quick review of basics for those already experienced in the application of data converters and as tutorial material for those who are not familiar with data conversion systems.

ORGANIZATION OF THIS PRODUCT HANDBOOK

This product handbook is divided into the following major sections: Data Conversion Devices, Converter Accessory Circuits, Modular Data Acquisition Systems, Power Supplies, Digital Panel Instruments, Data Loggers, and Digital Cassette Recording Systems. Most of these sections include product specification tables in addition to product data sheets.

Also included in this catalog are sections on extended performance modules, accessory products (sockets, trimming potentiometers, etc.) and an ordering guide.

PRODUCT SUPPORT

All Datel Systems' products are backed up by a detailed technical data sheet. In many cases there is also an instruction manual available. The appropriate literature may be obtained by contacting the factory. In all cases the appropriate technical data is shipped with each product ordered. There is also a number of technical application notes available from the factory.

While the available literature gives all the information normally required to use any of our products, we also maintain an applications engineering department to answer any additional questions you may have regarding the application of these products.

Our qualified team of field sales engineers is available to service our customers throughout the United States, Canada, Western Europe, and the Far East. Datel Systems has direct sales offices in Santa Ana, California; Sunnyvale, California; and Gaithersburg, Maryland. There are Datel sales subsidiaries in London, England; Paris, France; Munich, West Germany; Tokyo, Japan; and Osaka, Japan.



QUALITY ASSURANCE

Datel Systems has a fully implemented Quality Assurance Program in conformance with MIL-STD-9858A. This program is under a full-time Quality Assurance Manager who reports directly to the President of Datel Systems, Inc. The quality assurance responsibility is superimposed over procurement, material control, manufacturing, and shipping activities. The Quality Assurance Manager is responsible for the following areas: quality assurance engineering, systems test, in-process inspection, purchased material inspection, and calibration. The quality assurance program encompasses receiving inspection of all components, in-process inspection of all assemblies, burn-in or shock testing where required, calibration of all instruments and maintenance of calibration records, component vendor records and vendor rating systems, and implementation and control of a material review board. The Q.A. Manager also submits monthly, to management, in-house quality performance reports on all departments.

GSA CONTRACTS

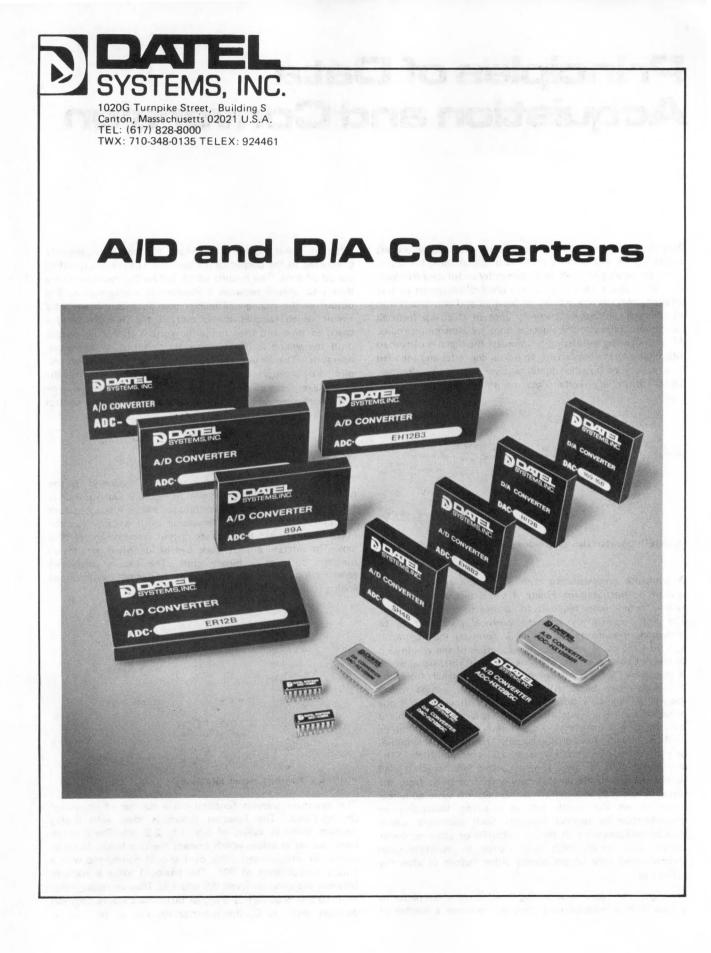
Most of Datel Systems products are covered under appropriate GSA contracts which permit a discount on purchases by U.S. Government.

ene L. Eugene L. Zuch

Product Marketing Manager



PRODUCTION MODULAR PRODUCTS



Principles of Data Acquistion and Conversion

Data acquisition and conversion systems are used to process analog signals and convert them into digital form for subsequent processing or analysis by computer or for data transmission. In general a transducer takes a physical parameter such as pressure, temperature, strain, or position and converts it into an electrical voltage or current. Once in electrical form all further processing of the signal is done by electronic circuits. After the analog processing is complete the signal is converted into digital form by an analog to digital converter and then fed to a variety of possible digital systems such as a computer, digital controller, digital data transmitter, or digital data logger.

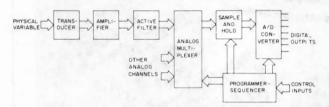


FIGURE 1. Complete Data Acquisition and Conversion System.

A complete representative data acquisition and conversion system is illustrated in Figure 1. This diagram shows the various components required for an interconnected system. The input to the system, the physical parameter to be measured, is converted to electrical form by the transducer and then fed to an amplifier. The function of the amplifier is to convert the signal to a high level (1 to 10 volt) signal which is necessary for further processing. The signal from the transducer may be a millivolt level signal, a high source impedance signal, a differential signal with common mode noise, or a current signal. In any of these cases the amplifier is used to convert the signal to a high level voltage which can be used to drive the next analog circuit. An operational amplifier or instrumentation amplifier is used to accomplish this. The amplifier is followed by a low pass active filter which is used to eliminate high frequency components or noise from the signal. There may also be a need to perform some nonlinear operation on the signal such as squaring, linearizing, or multiplication by another function. Such operations, which may be performed by an analog multiplier or other nonlinear circuit, also require high level signals to maintain good accuracy and may be performed either before or after the active filter.

The signal then goes to an *analog multiplexer* which performs a time division multiplexing operation between a number of

different signal inputs. Each input channel is sequentially connected to the output of the multiplexer for some specified period of time. The circuits which follow the multiplexer are thus time shared between a number of analog signals. The output of the analog multiplexer goes to a *sample and hold* circuit which samples the output of the multiplexer at a specified time and then holds the voltage level at its output until the *analog to digital converter* performs its conversion operation. The timing and control of this system is accomplished by a *programmer-sequencer* circuit which controls the multiplexer, sample and hold, and A/D converter. The programmer-sequencer in turn is controlled by digital control inputs from a data processor.

QUANTIZING THEORY

The operation of quantizing a signal is illustrated by the quantizer transfer function shown in Figure 2. Quantization is the process of converting a continuous analog input into a set of discrete output levels. The analog input is shown on the horizontal axis and the discrete output levels on the vertical axis. The discrete output levels can be identified by a set of numbers such as a binary code. The two processes of quantization and coding represent the basic operation of analog to digital conversion.

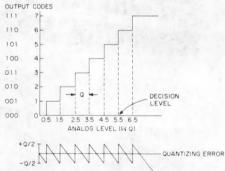


FIGURE 2. Transfer Function for Quantizer.

The quantizer transfer function has a number of important characteristics. The function shown is ideal with analog decision levels at values of 0.5, 1.5, 2.5, etc. The decision levels are set at values which bracket the true levels. In other words, an analog input value of 1 should correspond with a binary output level of 001. The analog 1 value is halfway between the decision levels 0.5 and 1.5. Thus an analog value of 1 \pm 0.5 is read out as a digital 001. The distance between decision levels is Q, the quantization size or bit size. A



quantizer with a binary output code has 2^n discrete output levels with 2^n-1 analog decision levels. The decision levels in an actual quantizer would not be precise but would have a finite uncertainty band around them. For an analog value within this uncertainty band the output could be at either of two discrete output levels. In addition, in an actual quantizer the decision levels would not necessarily be at precisely the correct analog values, but would miss these values due to nonlinearity, offset, and gain errors.

If the input to the quantizer is moved through its full range of values and subtracted from the discrete output levels an error signal will result. This error is called "quantizing error" and is an irreducible error due to the quantizing process and dependent on the number of quantization levels, or resolution, of the quantizer. When the quantizing error is plotted, as shown in the illustration, it has the form of a sawtooth waveform with a peak to peak value of Q. The output of the quantizer can be thought of as the input analog signal with quantization noise added to it. Thus the output, which is restricted to a finite number of discrete values, jumps from one value to the next as the input moves through its full range. The quantization error is zero only midway between the decision levels. The peak value of quantization noise is Q/2 and the RMS value can be computed from the triangular shape and found to be $Q/2\sqrt{3}$. Although the quantization noise can be reduced by increasing the resolution of the quantizer, there always remains a quantization uncertainty of at least $\pm Q/2$ for any quantizer.

An A/D converter performs the operations of quantizing and coding a signal in some finite amount of time. The time required to do this depends both on the resolution of the converter and the particular conversion method used. The speed of conversion required in a particular situation depends on the time variation of the signal to be converted and the amount of resolution required. The time required to make a measurement or conversion is generally called the "aperture time."

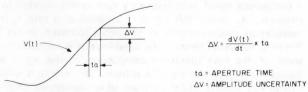


FIGURE 3. Aperture Time and Amplitude Uncertainty.

Aperture time can be considered to be a time uncertainty or amplitude uncertainty. As shown in Figure 3 the aperture

time and amplitude uncertainty are related by the time rate of change of the signal. For the particular case of a sinusoidal signal to be converted, the maximum rate of change occurs at the zero crossing of the waveform and the amplitude change is:

 $\Delta V = \frac{d}{dt} (Vsin\omega t)_{t=0} \times t_a = V\omega t_a$

giving

$$\frac{\Delta V}{V} = \omega t_a = 2\pi f t_a$$

From the result we can determine, for example, the aperture time (or conversion time) required to digitize a 1 kilohertz signal to 10 bits resolution. This is a resolution of 1 part in 2^{10} or 0.1%, and using the above equation:

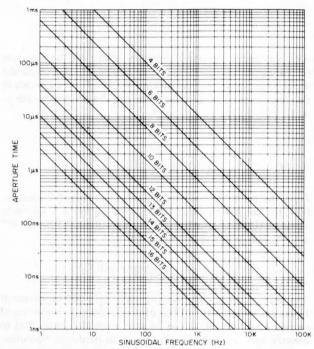
$$t_a = \frac{\Delta V}{V} \times \frac{1}{2\pi f} = \frac{.001}{6.28 \times 10^3} = 160 \times 10^{-9}$$

The result is a required aperture time of only 160 nanoseconds to remain within 1 bit (0.1%) of resolution due to the rate of change of the signal. It can be seen from this result that to convert even a slowly varying signal to moderate resolution levels requires an extremely fast and, therefore, expensive analog to digital converter. Fortunately there is a simple and inexpensive way around this problem by the use of the sample and hold circuit which can reduce the aperture time considerably by taking a rapid sample of the signal and then holding its value for the required conversion time. The aperture time required for sinusoids of other frequencies and different resolutions is summarized by the graph shown in Figure 4.

SAMPLING THEORY

The operation of sampling is illustrated in Figure 5 which shows an analog signal and a train of periodic sampling pulses. The pulses represent a fast acting switch which connects to the analog signal for a very short time and then opens for the remainder of the period. Sampling pulses thus have a very short ON time compared to the total period. The result of the sampling process is identical with multiplying the analog signal with a train of pulses of unity amplitude. The resultant modulated signal is shown in Figure 5 (c) where the amplitude of the analog signal is preserved in the modulation envelope of the pulses. If the switch-type sampler is replaced by a switch and a capacitor, then the analog signal is sampled and stored until the next sample pulse with the result shown in Figure 5 (d). This type of sampler is called a sample and hold.

PRINCIPLES OF DATA ACQUISITION AND CONVERSION





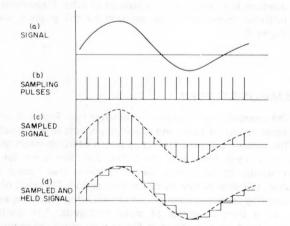
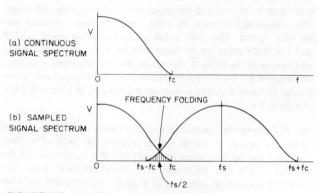


FIGURE 5. Signal Sampling Process.

The purpose of signal sampling is the efficient use of data processing equipment or data transmission facilities. A single data transmission link can be used to transmit many channels of information by simply sampling each channel periodically. Likewise, for the efficient use of data processing equipment to monitor and control a process, for example, it may only be necessary to sample the state of a process once every 5 minutes, perform a computation and correction, and then free the computer the remaining time for other tasks. Continuous monitoring of a single information channel by a computer would be very expensive indeed. In data conversion systems it is also more economical to use a single A/D converter, which may be the most expensive component in the system, for a number of information channels by using sampling.

An important and fundamental question to ask about sampleddata channels is "how often must I sample a given signal in order not to loose information from the signal?" It seems obvious that all useful Information can be extracted by sampling a slowly changing signal at a much faster rate than any change which occurs, and likewise that if a signal is significantly changing value between samples, information is being lost. The answer is contained in the well known Sampling Theorem which can be stated as follows: If a continuous bandwidth limited signal contains no frequency components higher than f_c then the original signal can be completely recovered without distortion if it is sampled at the rate of at least $2f_c$ samples per second.





The sampling theorem can be illustrated by the frequency spectra shown in Figure 6. Figure 6 (a) shows the spectrum of a continuous signal with frequency components limited to a frequency fc. When this signal is sampled at a rate fs the modulation process results in the signal spectrum shown in Figure 6 (b). Here, because the sampling rate is not sufficient. some of the high frequency components of the signal are folded back into the signal spectrum. This effect is called "frequency folding." In the process of recovering the original signal, the folded frequency components cause distortion and cannot be separated or distinguished from the original signal. It can be seen from the figure that by changing the sampling rate such that $f_s - f_c > f_c$, we obtain the result that $f_s > 2f_c$ which demonstrates the sampling theorem. Frequency folding is eliminated by either using a high enough sampling frequency or filtering the original signal to eliminate any frequency

Electronic Design's

1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

components above one half the sampling rate. It should be noted, however, that in practice there is always some frequency folding due to wideband noise and non-ideal filters and that one must attempt to reduce the effect to negligible proportions.

Another effect which is the result of frequency folding is known as an "alias." Figure 7 illustrates this by showing a periodic signal which is sampled at a rate less than twice per cycle. The sample amplitudes are shown connected by a dotted line which obviously has a period quite different from the original signal and is an alias. From this figure it can be readily seen that if the waveform is sampled at least twice per period as required by the sampling theorem, its original frequency is preserved.

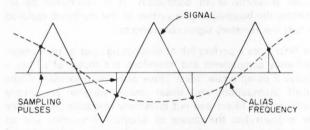


FIGURE 7. Alias Frequency Caused by Inadequate Sampling Rate.

The sample and hold device, which is so commonly used in data conversion systems and also analog multiplexed data systems, has some important characteristics which should be briefly discussed. An ideal sample and hold, or zero order hold as it is also known, takes a sample in zero time and then holds the value of the sample indefinitely with perfect accuracy. In practical units, a sample is taken in a time period which is short compared to the holding time. During the holding time there is some change in the output which is small compared to the system accuracy. The effect of this process on a continuous analog input signal can be determined by finding the transfer function of a sample and hold. By use of the impulse response of this device and using the Laplace transform the transfer function is found to be:

$$G(j\omega) = \frac{1 - e^{-j\omega T}}{j\omega} = \frac{2\pi}{\omega_s} \frac{\sin \pi \, \omega/\omega_s}{\pi \, \omega/\omega_s} e^{-j\pi} \left(\frac{\omega}{\omega_s}\right)$$

where T is the sampling period and ω_s is the sampling radian frequency. The magnitude and phase of this function are plotted in Figure 8 which shows that a sample and hold device acts like a low pass filter with a cutoff frequency of approximately $f_s/2$ and a phase delay of T/2, or one half the sampling period. Circuit characteristics of the sample and hold will be discussed in a following section.

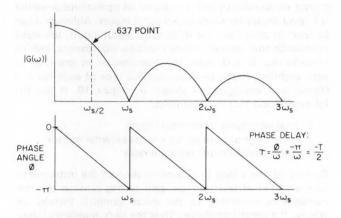
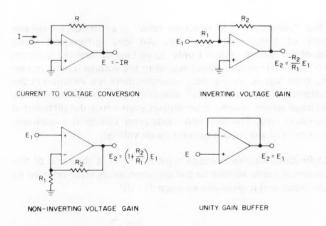


FIGURE 8. Sample and Hold Transfer Function.

AMPLIFIERS AND FILTERS

The first part of a data acquisition and conversion system is concerned with extracting the signal which is to be measured. The initial processing of the signal is done with an amplifier, filter, and possibly a nonlinear operator. The purpose of the amplifier is to perform one or more of the following functions: boost the amplitude of the signal, buffer the signal, convert a signal current into a voltage, or separate a differential signal from common mode noise. For most data conversion systems the desired voltage level out of the amplifier is 5 or 10 volts full scale. This is the level accepted by most analog multiplexers, sample and holds, and A/D converters to give the best accuracy.





Operational or instrumentation amplifiers are used to perform the above listed signal translations. Some of the operational amplifier configurations used are shown in Figure 9 with their

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

output relationships given. In general an operational amplifier is a good choice for single ended signal inputs. Although it can be used in some cases for differential signal inputs, the input impedance and common mode rejection adjustments limit its effectiveness. In such cases the instrumentation amplifier, or data amplifier, is the best choice. This type of amplifier is a closed loop configuration shown in Figure 10. It has the following important characteristics.

- 1. high impedance differential inputs
- 2. wide range of gains set by a single external resistor
- 3. high common mode rejection ratio

Because of the closed loop configuration of the instrumentation amplifier, it does not use gain setting resistors or other components connected to the input terminals thereby degrading the input impedance. Thus the high impedance inputs maintain the high common mode rejection characteristic even with moderate source impedances.

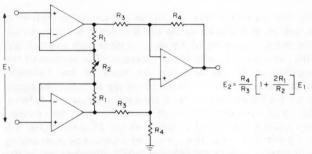


FIGURE 10. Instrumentation Amplifier Configuration.

The "common mode rejection ratio" is an important parameter of differential amplifiers. An ideal differential input amplifier would respond only to voltage differences between its input terminals without regard to the voltage level common to both inputs. In practice, however, there is a variation in the balance of the differential amplifier due to common mode voltage which results in an output even when the differential input is zero. The common mode error voltage is a nonlinear function of the input common mode voltage.

Definition: Common mode rejection ratio is the ratio of the common mode voltage to the common mode error referred to the input and is generally expressed in dB.

$$CMRR = 20 \log_{10} \left[\frac{V_{cm}}{e_{cm}} \right]$$

where V_{cm} is the common mode voltage and e_{cm} is the common mode error referred to the input. CMRR is a function

of both common mode voltage and frequency. At even moderate frequencies a high CMRR can be significantly degraded by small unbalances in source impedance and input capacitances.

Following the amplifier in our system, it may be necessary to use a low pass filter. Filtering is used in a data acquisition system for two reasons: to limit the bandwidth of the processed signal to less than half the sampling frequency in order to eliminate frequency folding, and to reduce either man-made or electrically generated noise in the system. Man-made noise usually has some identifiable characteristic such as periodicity and regular shape and can be eliminated by some specific technique such as a notch filter. Thermal, or Johnson noise, on the other hand is random noise with a noise power proportional to bandwidth. It is minimized by restricting the bandwidth of a system to the minimum required to pass the necessary signal components.

No filter does a perfect job of eliminating noise or undesirable frequency components and, therefore, the choice of a filter is always a compromise. Ideal filters with flat response, infinite cutoff attenuation, and linear phase response are simply mathematical filters and not physically realizable. In practice the engineer has the choice of a cutoff frequency, and an attenuation rate and phase response based on the number of poles and filter characteristic chosen. The effect of overshoot and non-uniform phase delay must also be considered.

Active filters are very popular due to a number of excellent features they have over older RLC type passive filters. They eliminate inductors and associated saturation and temperature stability problems. The response of an active filter can be accurately set by temperature stable capacitors and resistors. In addition, they overcome the problems of insertion loss and loading effects by their use of operational amplifiers.

SETTLING TIME

A parameter that occurs very often in data acquisition and conversion systems is "settling time." Settling time is defined as the time elapsed from the application of a full scale step input to an amplifier to when the output has entered and remained within a specified error band around its final value. Although this definition is stated in the terms of an amplifier response, settling time is also used in the specification of other components such as D/A converters, analog multiplexers, and sample holds. It has essentially the same meaning in these other cases although in some of them the input step is actually applied by turning on a switch and, therefore, a switching time is included in the settling time. In the case of sample and holds, the equivalent of settling time is the acquisition time and includes both the turn-on time of the sampling switch and the charging time of the holding capacitor to its final value.



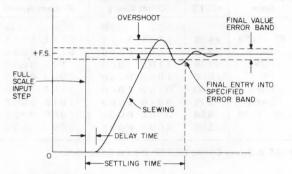


FIGURE 11. Amplifier Settling Time.

The settling time of a fast amplifier is illustrated in Figure 11. After the application of the input step, there is a small delay time after which the amplifier begins to slew or change its output at the maximum possible rate. During this time the amplifier is in a non-linear or saturated state. The output then overshoots its final value, recovers from saturation, and then settles into its specified error band after a small amount of ringing. The definition distinguishes that the amplifier must enter and remain in the error band rather than just enter it the first time.

Settling time, unfortunately, is not readily predictable from other amplifier parameters such as bandwidth, slew rate, or overload recovery time although it depends on all of these. It is also dependent on the amplifier open loop response characteristic, dielectric absorption by internal capacitors, output load capacitance, and input capacitance. An amplifier must be designed and optimized for settling time, and settling time is a parameter which must be evaluated by testing.

One of the important requirements of a fast settling amplifier in addition to wide bandwidth, fast slew rate, and fast overload recovery is that it have a true single pole open loop response characteristic. This means a smooth 6dB per octave frequency roll-off characteristic. Such an amplifier can never settle to its final value in less time than that derived from the number of time constants required to reach this accuracy. Figure 12 shows a plot of the output error as a function of the number of time constants. The settling time may actually be quite a bit larger due to slew rate limitation and other problems. An amplifier with a closed loop bandwidth of 1MHz has a time constant of 160 nanoseconds and to settle within .01% of final value requires at least 9 time constants or 1.44 microseconds.

If an amplifier does not have a single pole response and, therefore, an uneven gain roll-off characteristic, its output response may get to the vicinity of the error band quickly but then require a very long time to actually enter it. Likewise, it may overshoot the error band and take a long time to enter it a remain inside it. This is the case for amplifiers with pole-zero mismatches in their response characteristic. Modern fast settling amplifiers are generally specified to 0.1% or .01% settling for small closed loop gains and have settling times of less than 1 μ sec. In data acquisition systems these

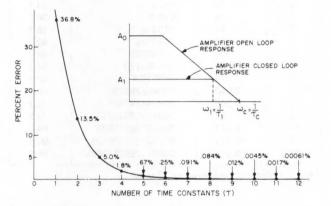


FIGURE 12. Error as a Function of the Number of Time Constants for a Single Pole Response.

amplifiers are useful in the design of sample and hold circuits, buffer amplifiers for analog multiplexers or A/D converters, and output amplifiers for fast D/A converters. In many cases fast settling amplifiers are required even though slowly changing signals are being processed. This is because of the high data switching rate through the analog multiplexer.

DIGITAL CODING

A/D and D/A converters relate analog and digital values by means of an appropriate digital code. The codes used are various binary related codes, the most common of which is natural binary. A binary number is represented as

$$N = a_n 2^n + a_{n-1} 2^{n-1} + \dots + a_2 2^2 + a_1 2^1 + a_0 2^0$$

where the coefficients a_n assume the values of "0" or "1". Table 1 shows the decimal equivalents of 2^n and 2^{-n} for values of n up to 16.

In an A/D or D/A converter the first bit is called the most significant bit or MSB and has a weight of $\frac{1}{2}$ of full scale of the converter; the second bit has a weight of $\frac{1}{4}$ FS and so on down to the last bit which is called the least significant bit or LSB and has a weight of $1/2^{n}$ FS. The resolution of the converter is determined by the number of bits, and the size of the LSB is FS/2ⁿ. It should be noted that the digital code used in general does not correspond to its decimal equivalent in analog voltage. The coding used is the set of coefficients of 2^{-n} representing a fractional part of full scale. The MSB is always positioned on the left and the LSB on the right of the digital code. The binary code 10110 thus represents $(1 \times 1/2) + (0 \times 1/4) + (1 \times 1/8) + (1 \times 1/16) + (0 \times 1/32)$ or 11/16 of full scale of the converter. The full scale analog value for a

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

n	2 ⁿ	2 ⁻ⁿ	dB
0	1	1 in the first starting the starting	0
1	2	.5	-6
2	4	.25	-12
3	8	.125	-18.1
4	16	.0625	-24.1
5	32	.03125	-30.1
6	64	.015625	-36.1
7	128	.0078125	-42.1
8	256	.00390625	-48.2
9	512	.001953125	-54.2
10	1 024	.0009765625	-60.2
11	2 048	.00048828125	-66.2
12	4 096	.000244140625	-72.2
13	8 192	.0001220703125	-78.3
14	16 384	.00006103515625	-84.3
15	32 768	.000030517578125	-90.3
16	65 536	.0000152587890625	-96.3

TABLE 1. Decimal Equivalents of 2ⁿ and 2⁻ⁿ

converter can be any convenient voltage, but voltages such as 0 to ± 5 , 0 to ± 10 , ± 2.5 , ± 5 , and ± 10 are most commonly used. A 12 bit converter, for example, has a resolution of 1 part in 4096. If the full scale analog voltage is 10 volts then the LSB size is 10V/4096 or 2.44 millivolts. The resolution of a converter can be conveniently related to dynamic range in dB since a factor of 2 corresponds to 6.02dB. Therefore, the number of bits \times 6.02 gives the dynamic range in dB. A 12 bit converter has a dynamic range of 72.2dB.

Scale	+10VFS	Straight	Binary	Complementary Bir		
+FS-1LSB	+9.96	MSB 1 1 1 1	LSB 1 1 1 1	MSB 0 0 0 0	LSB 0 0 0 0	
+3/4FS	+7.50	1100	0000	0011	1111	
+1/2FS	+5.00	1000	0000	0111	1111	
+1/4FS	+2.50	0100	0000	1011	1111	
+1/8FS	+1.25	0010	0000	1101	1111	
+1LSB	+0.04	0000	0001	1111	1110	
0	0.00	0000	0000	1111	1111	

TABLE 2. Binary Coding for 8 Bit Unipolar Converters.

Converters have both unipolar and bipolar analog values and use a number of different binary related codes. Table 2 shows binary coding for a unipolar 8 bit converter with a 10 volt full scale. Notice ' that all one's in the digital code does not correspond to full scale but $(1-2^{-n})FS$. In some converters it is convenient to use reverse sense binary coding, or complementary binary, where the most negative analog value corresponds to full scale digital value. This code is just the binary code with all 1's made 0's and vice versa. For bipolar analog values the most common codes are offset binary and 2's complement which are shown for an 8 bit converter in Table 3.

Scale	±5VFS	Offset Binary		2's Com	plement
Contract Providence		MSB	LSB	MSB	LSB
+FS-1LSB	+4.96	1111	1111	0111	1111
+3/4FS	+3.75	1110	0000	0110	0000
+1/2FS	+2.50	1100	0000	0100	0000
0	0.00	1000	0000	0000	0000
-1/2FS	-2.50	0100	0000	1100	0000
-3/4FS	-3.75	0010	0000	1010	0000
-FS + 1LSB	-4.96	0000	0001	1000	0001
-FS	-5.00	0000	0000	1000	0000

TABLE 3. Binary Coding for 8 Bit Bipolar Converters.

Offset binary is simply a shifted binary code where ½ FS binary corresponds to analog zero. 2's complement coding is the same as offset binary except that the MSB is complemented, resulting in a digital code of all 0's corresponding to, analog zero. Binary coded decimal or BCD coding is also commonly used in converters and is illustrated by the 8 bit coding shown in Table 4. In BCD, 4 binary digits are used to code each decimal digit. This code can also be used for bipolar analog values if a separate sign bit is used. Other codes such as gray code, sign-magnitude binary, and 1's complement are sometimes used but are not as common as the codes just described.

Scale	+10VFS	BCD		
int official and a		MSD LSD		
+FS-1LSD	+9.9	1001 1001		
+3/4FS	+7.5	0111 0101		
+1/2FS	+5.0	0101 0000		
+1/4FS	+2.5	0010 0101		
+1LSD	+0.1	0000 0001		
0	0.0	0000 0000		

TABLE 4. BCD Coding for 2 Digit Unipolar Converter.

D/A CONVERTERS

In addition to being used as a basis for a large fraction of all A/D converters that are manufactured, D/A converters have a large number of important uses in their own right. Among these uses are computer driven CRT displays, digitally controlled power supplies for automatic test equipment, digital generation of analog waveforms, and digital control of automatic process control systems.

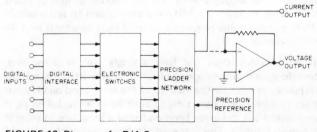


FIGURE 13. Diagram of a D/A Converter.



Although there exists a large array of techniques for accomplishing digital to analog conversion, the methods discussed here will be limited to the most commonly used parallel conversion methods. The basic configuration of a D/A converter, or DAC, is shown in Figure 13. A digital interfacing circuit converts the logic inputs to the control levels of a set of switches. These operate in conjunction with a precision resistor ladder network to give binary weighted currents or voltages; the ladder network is referenced to a stable precision voltage source. The output of the ladder network is the sum of all the binary weights in the form of a voltage or current. In the figure a current output ladder is shown. The two types of D/A converters are current output DAC's and voltage output DAC's. For current output types, the current output of the ladder is brought out as the output of the converter; for voltage output types the current goes to an operational amplifier current-to-voltage converter circuit. In most high speed applications a current output DAC is used since there is always some loss of speed due to current-to-voltage conversion.

A frequently used method of achieving a binary weighted set of currents is the circuit shown in Figure 14. A series of transistor current sources has its collector currents set by emitter resistors with values of R, 2R, 4R, 8R, etc. A stable reference voltage, compensated for the base to emitter voltage variation with temperature, is used to bias the bases of all of the transistors and thus set up constant emitter currents. The current source transistors are switched on or off by logic inputs connected through diodes to the emitters. Depending

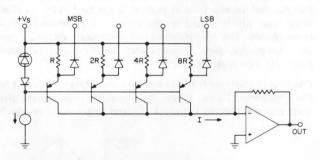


FIGURE 14. Weighted Current Source D/A Converter.

on the logic level at each diode input, the current will flow either through the diode or through the transistor. The weighted currents are summed at the collectors of all the transistors and become either the current output of the converter or the current input to an operational amplifier as shown in the diagram. Alternatively, to preserve the high speed of the current output, a resistor can be connected to this output to convert the current directly to a voltage. This is an excellent way of maintaining the speed of the converter but is restricted to relatively small full scale voltages of a volt or so, due to the limited positive voltage swing of the transistor collectors. The weighted current source method has the advantage of simplicity and high speed. Current output DAC's of this type can also be used in configurations where one or more units are used to sum their output currents together directly. The disadvantage of this method is the wide range of resistance values required for a high resolution converter and the resultant effect on both temperature tracking and speed. Nevertheless, high resolution converters with high speed can be made by using several groups, with 4 or 5 current sources each, and dividing down the current output of each group. This is illustrated in Figure 15 which shows 3 groups of current sources with resistive current dividers following groups 2 and 3. If each group has 4 binary current sources, then the dividers would have to reduce the current outputs of groups 2 and 3 to 1/16 of their original value.

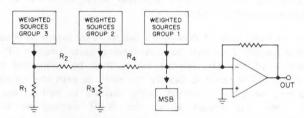


FIGURE 15. Groups of Identical Binary Weighted Current Sources to Achieve High Resolution.

Figure 15 also shows the method of achieving a bipolar output for a D/A converter. A current source with a current equal to the MSB weight is connected to the output of all the other weighted sources. This offsets the output of the converter by one half the full scale value, thus setting analog zero at one half digital full scale. This gives offset binary coding as discussed previously.

A second popular method for D/A conversion is the R-2R ladder technique. As shown in Figure 16 this consists of a network of series values of R and shunt values of 2R. The bottoms of the shunt resistors are switched between a voltage reference source and common. The operation of the ladder

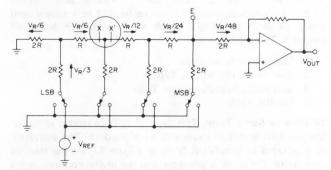


FIGURE 16. R-2R Network D/A Converter.

network is based on the binary division of a current as it flows down the ladder. This can be seen by examination of the

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

points X and X' in the network. The following conclusions are valid: from point X looking to the right a resistance R is seen and looking to the left a resistance of 2R is seen; from point X' looking to the right a resistance of 2R is seen and looking to the left a resistance of R is seen. These properties hold for any of the junctions along the ladder. If a 2R resistor is switched to the voltage reference source, the source sees a resistance of 2R plus 2R in paralle! with 2R, or 3R total, and a current of VREE/3R flows into the junction. At the junction this current divides equally, with half flowing to the left and half to the right. The right-hand current flows to the next junction where it is again divided in half, and so on to the right end of the ladder where it becomes part of the total output current. The total output current is the sum of all the currents from the shunt resistors which are weighted binarily with the LSB at the leftmost switch and MSB at the rightmost switch. The output of the ladder can be a current, as shown going into the operational amplifier input, or it can be a voltage appearing at terminal E.

An alternate way of driving the ladder is by means of equal value switched current sources feeding each junction. The bottom of the 2R resistors would then be connected to common. The result is exactly the same as with the voltage source, with each current being divided in half at each junction. The advantages of the R-2R method are the following:

- 1. All resistors are values of either R or 2R resulting in easy matching and temperature tracking.
- 2. Resistor values can be kept low to insure high speed.
- The output amplifier always sees a constant resistance value at its input terminal.

Compared to the weighted current source method the R-2R ladder requires two resistors per bit whereas the former requires one resistor per bit.

A/D CONVERTERS

In analog to digital conversion there is an even larger number of methods commonly used than in D/A conversion. This is so because A/D conversion, except in the very fastest requirements, lends itself to many serial methods and indirect methods. The discussion here will be limited to 4 widely used types of A/D converters which are available in low cost modules. These types are:

- 1. Counter or Servo Type
- 2. Dual Slope Integrating Type
- 3. Successive Approximation Type
- 4. Parallel Type

Counter or Servo Type: This type of A/D converter is one of the simplest and least expensive to implement. The converter is illustrated in simplified form in Figure 17. At the start of conversion the clock is gated on, and the digital counter begins to count clock pulses. As it counts it changes the output of the D/A converter which is compared to the analog input voltage.

When the DAC output is equal to the input, the comparator changes state and inhibits the clock pulses. At this time conversion is complete and the output digital number is contained in the output register of the counter.

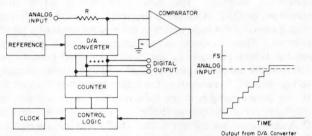


FIGURE 17. Counter or Servo Type A/D Converter.

This converter features simplicity, low cost, and good accuracy but has the disadvantage of slow speed. Conversion time is proportional to input voltage and is longest for a full scale input. In some applications the speed is improved if an up-down counter is used, and the converter counts either up or down from its previous value rather than resetting to zero. In this way the counting converter can follow slowly varying inputs. This converter is also called a servo type because of the feedback method of controlling the counter.

Dual Slope Integrating Type: Integrating A/D converters operate by the indirect method of converting a voltage to a time period which is then measured by a counter. There are several different types of converters using the integrating, or ramp principle including single ramp, dual ramp, and triple ramp which are all variations on the basic principle. The most popular and widely used at present is the dual ramp, or dual slope type, which is used in most digital voltmeters and digital panel meters. The advantages of this method are relatively low cost, simplicity, high accuracy and linearity, and excellent noise rejection characteristics.

Conversion starts with the unknown input voltage switched to the integrator input. When the output ramp crosses the comparator threshold the clock is gated to the counter which

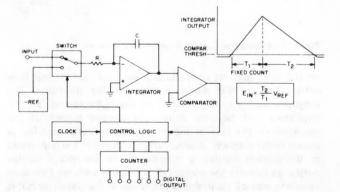


FIGURE 18. Dual Slope Type A/D Converter.

counts up to a predetermined number. At this time the input of the integrator is switched to the reference and the counter is reset to zero. The integrator then integrates the reference back down to the comparator threshold at which time the count is stopped. The input voltage is then the ratio of T_2 counts to T_1 counts times the reference voltage, and can be read directly from the counter register.

The dual slope method has a number of important features. Conversion accuracy is independent of the clock frequency and integrating capacitor value as long as they are stable within a conversion period, and depends only on the accuracy and stability of the reference. Resolution is basically only limited by the analog resolution of the converter. In addition, this converter gives excellent noise rejection because of the integration operation; in particular, normal mode noise rejection is infinite for T_1 equal to a multiple of the period of the interfering noise. The main drawback of this method is the relatively long conversion time.

Successive Approximation Type: This conversion method is the most widely used in general practice due to its combination of high resolution and high speed. The successive approximation converter operates with a fixed conversion time per bit, independent of the value of the analog input. The method is illustrated in Figure 19 and operates by comparing the input voltage with the D/A converter output, one bit at a time.

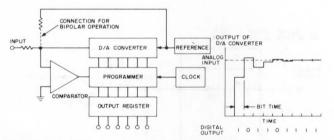


FIGURE 19. Successive Approximation Type A/D Converter.

At the start of the conversion cycle, the D/A converter's MSB output, which is 1/2 full scale, is compared with the input. If it is smaller than the input, the MSB is left on and the next bit is tried. If the MSB is larger than the input, it is turned off when the next bit is turned on. This process of comparison is continued down to the LSB after which the output register contains the complete output digital number. Both serial and parallel output data can be brought out of this converter and, in addition, the conversion can be synchronized to an external clock on some units. Speeds as high as 100 nanoseconds per bit can be achieved by this method. Successive approximation converters can also be quite accurate, but the accuracy depends on the stability of the reference, the switches, the ladder network, and the comparator. In the figure it is also shown how bipolar operation is accomplished using a precision resistor connected from the reference source to the compar-



ator input, thus subtracting a ½ full scale current from the input. Many converters have this resistor built in so that bipolar operation can be achieved by external pin connection.

Parallel Type: While the successive approximation converter is capable of speeds as high as 100 nsec. per bit, giving conversion rates of 1 MHz for 10 bits, significantly faster conversion must be achieved using the parallel technique. This method is sometimes referred to as the simultaneous, or flash technique, and is capable of 25MHz conversion rates for 4 bits. As shown in Figure 20, the method employs an input quantizer comprised of 2^{n-1} comparators biased 1 LSB apart by a reference voltage. For a given analog input voltage to the comparators, all comparators below the input level turn on while all comparators above it are off. The quantization process is accomplished in the switching time of a single comparator.

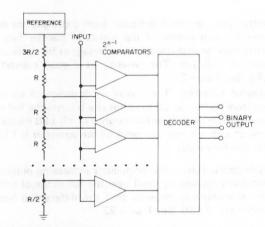


FIGURE 20. Parallel Type A/D Converter.

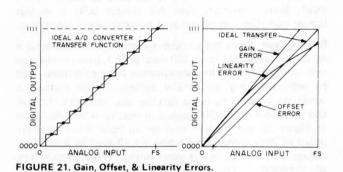
The comparator outputs, however, are not in the binary code and must, therefore, go through a decoder. The parallel method has the advantage of the fastest speed but is limited to a relatively few bits, usually about 4, due to the large number of comparators required. To convert a large number of bits it is necessary to employ a hybrid technique whereby a parallel conversion stage is followed by a fast D/A converter, the output of which is subtracted from the input voltage, the difference amplified and then converted using another parallel stage. This results in a speed compromise but higher resolution.

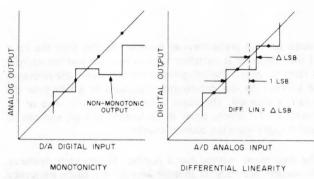
There are a number of important parameters used to characterize the accuracy of A/D and D/A converters. Since they have specific meanings as applied to converters, these parameters are defined here.

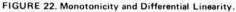
Resolution: The smallest analog change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution is the analog value of the LSB, which is $FS/2^n$ for an n bit binary converter and $FS/10^d$ for a d digit BCD converter. Resolution is often specified in percentage of full scale, as in a 10 bit converter which has a resolution of 0.1%.

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

In many cases the useful resolution of a converter may be less than its specified resolution.







ANALOG MULTIPLEXERS

Linearity: The maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity may be expressed as a percentage of full scale or as a fraction of LSB size. The linearity of a good converter is $\pm \frac{1}{2}$ LSB. See Figure 21.

Differential Linearity: The maximum deviation of an actual bit size from its theoretical value for any bit over the full range of the converter. A differential linearity of $\pm\frac{1}{2}$ LSB means that the size of each bit over the range of the converter is 1 LSB $\pm\frac{1}{2}$ LSB. See Figure 22.

Monotonicity: Having a continuously increasing output for a continuously increasing input over the full range of the converter. Monotonicity requires that the differential linearity be less than 1 LSB. See Figure 22.

Missing Code: In an A/D converter this occurs when the output code skips a digit. This happens when the differential linearity is greater than 1 LSB for some bit.

Quantizing Error: The basic uncertainty associated with digitizing an analog signal due to the finite resolution of an A/D converter. An ideal converter has a maximum quantizing error of $\frac{1}{2}$ LSB. See Figure 2.

Relative Accuracy: The input to output error as a fraction of full scale, with gain and offset errors adjusted to zero. Relative accuracy is a function of linearity.

Absolute Accuracy: The full scale analog error referenced to the NBS standard volt:

Offset Error: The error by which the transfer function fails to pass through the origin, referred tc the analog axis. This is adjustable to zero in available converters. See Figure 21.

Gain Error or Scale Factor Error: The difference in slope between the actual transfer function and the ideal function in percent. This error is also adjustable to zero in available converters. See Figure 21. Analog multiplexer circuits are used for time sharing of analog to digital converters between a number of different analog information channels. An analog multiplexer consists of a group of analog switches arranged with inputs connected to the individual analog channels and outputs connected in common, as shown in Figure 23. The switches can be addressed by a digital input code. MOSFET switches are generally used and may be connected directly to an output load if it is a high enough impedance, or to an output buffer amplifier which provides a very high impedance to the switches. Using a fast bipolar transistor follower amplifier as a buffer, an input impedance of 10⁹ ohms is achieved resulting in a negligible transfer error due to the switch resistance of typically 2K ohms.

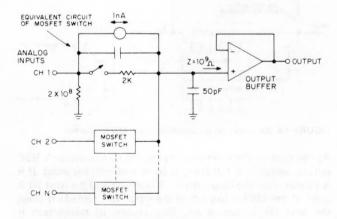


FIGURE 23. Analog Multiplexer Circuit.

Figure 23 shows the equivalent circuit of one of the MOSFET switches which is characterized by series and shunt resistance, shunt capacitance and a leakage current. Differential analog multiplexing can also be accomplished by using two MOSFET switches for each input channel.



There are several important parameters used to characterize analog multiplexers which are defined below.

Transfer Accuracy: The input to output error as a percentage of the input. Transfer accuracy depends on the source impedance, switch resistance, load impedance if the multiplexer is not buffered, and the signal frequency.

Settling Time: Same definition as discussed earlier. Here it includes the switching time of the switches.

Throughput Rate: The highest rate at which the multiplexer can switch from channel to channel at its specified accuracy. This rate is determined by the settling time.

Crosstalk: The amount of signal coupled to the output as a percentage of input signal applied to all OFF channels together. The inverse of the above is expressed as an attenuation in dB.

Input Leakage Current: The highest current that flows into or out of an OFF channel input terminal due to switch leakage.

SAMPLE AND HOLD CIRCUITS

Some of the properties of sample and hold circuits were discussed in the section on sampling theory. Here the circuit configurations and operating parameters will be discussed. Sample and hold circuits are used in conjunction with both A/D converters and D/A converters. With A/D converters they are used to shorten the aperture time for the converter by rapidly sampling the input signal and then holding its value until the conversion is completed. In the case of D/A converters they are used in display applications to remove "glitches" which appear at the output of all DAC's as they change from one analog level to another.

As described before, a sample and hold in its basic form consists of a switch and a capacitor. When the switch is closed the unit is in the sampling or tracking mode and will follow a changing input signal. When the switch is opened the unit is in the hold mode and retains a voltage on the capacitor for some period of time depending on capacitor and switch leakage.

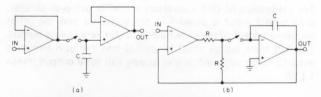


FIGURE 24. Sample and Hold Circuit Configurations.

Practical sample and hold circuits also use input and output buffer amplifiers and sophisticated switching techniques. The output buffer amplifier must be a low input current FET amplifier in order to have as small an effect as possible on the leakage of the capacitor. Likewise, the electronic switch used must be a low leakage type such as an FET switch. Figure 24 illustrates two sample and hold circuit configurations which are commonly used. Circuit (a) is used for fast sample and holds and is an open loop configuration using fast voltage follower amplifiers. For very fast circuits a diode bridge type sampling switch is used. Circuit (b) is a closed loop configuration with an operational integrator in the feedback path of the input buffer amplifier. This circuit results in extremely good accuracy and linearity.

Sample and holds are characterized by a number of important parameters, each with a specific meaning for these circuits. These are defined below.

Acquisition Time: The time from when the sample command is given to the point when the output enters and remains within a specified error band around the input value. At the end of the acquisition time the output is tracking the input. Note similarity to definition of settling time.

Aperture Time: The time elapsed between the hold command and the point at which the sampling switch is completely open. Aperture time is also referred to as turn-off time.

Aperture Uncertainty Time: The variation in aperture time for a sample and hold. The difference between maximum and minimum aperture time.

Decay Rate: The maximum change in output voltage with time in the hold mode.

Feedthrough: The amount of input signal appearing at the output when the unit is in the hold mode. Feedthrough varies with signal frequency and may be expressed as an attenuation in dB.

A/D AND D/A CONVERTER ADJUSTMENTS

A timing diagram for a typical successive approximation A/D converter is shown in Figure 25. The start of conversion is initiated by a start convert pulse of 30 nsec. minimum duration. The EOC (end of conversion) or status output then goes high indicating that conversion is in process. The MSB output of the D/A converter is turned on to be compared with the input voltage, registering a logic "1" at the Bit 1 parallel data output. If the MSB is smaller than the input voltage it stays on and the logic "1" remains on the Bit 1 output. If it is larger than the input, it turns off after the first clock pulse and the Bit 1 output goes to logic "0". After the first clock pulse the serial output for Bit 1 appears on the serial output pin. After the first clock pulse. Bit 2 is compared with the input remainder, after the second clock pulse Bit 3 is compared, and so on down to Bit 10 in this case. Thus each succeeding bit is compared to the remaining input during one clock interval, and the true output for that bit appears at the next clock interval. At the end of the 10th clock pulse, all parallel bit outputs are true and the serial LSB output appears. Also, the EOC output returns to logic "O" indicating that conversion is complete. The EOC or status output may be used to control the sample and hold preceding the A/D converter, since when



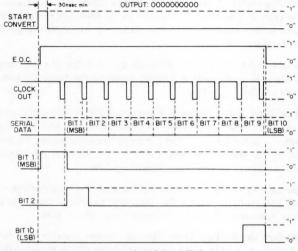


FIGURE 25. Timing Diagram for 10 Bit A/D Converter.

it is low the sample and hold is put in the tracking mode, and when it is high, during conversion, the sample and hold is put in the hold mode.

Most Datel A/D and D/A converters are capable of both unipolar and bipolar operation with several analog ranges selected by external pin connection. The commonly used ranges are 0 to $\pm 5V$, 0 to $\pm 10V$, $\pm 2.5V$, $\pm 5V$, and $\pm 10V$. The digital coding used is binary or BCD for unipolar operation and offset binary or two's complement for bipolar operation. All Datel A/D and D/A converters have provision for user adjustment of full scale and offset in order to obtain optimum accuracy in a given application. Figure 26 shows the circuit connection necessary to perform the calibration adjustments on an A/D converter. Calibration is accomplished as follows for a unipolar A/D converter:

 Connect a precision pulse generator to the "Start Convert" input terminal. The generator should be set to give a pulse width and amplitude as specified in the converter data sheet. The repetition rate should be set for the conversion time of the converter.

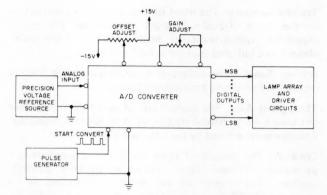


FIGURE 26. Connections for Calibration of A/D Converter.

- 2. Connect a precision voltage reference source to the analog input terminal.
- 3. Adjust the output of the voltage reference source to zero plus ½ LSB. This voltage is found by multiplying the converter full scale voltage range by one half the value of 2⁻ⁿ for an n bit converter. Adjust the zero offset trimming potentiometer until the LSB output flickers between logic "0" and logic "1".
- 4. Adjust the output from the voltage reference source to full scale minus 1½ LSB. Adjust the gain trimming potentiometer until the LSB output flickers between logic "0" and logic "1".

In the case of a bipolar A/D converter the calibration is identical except that the first part of step three is modified as follows:

3. Adjust the output from the voltage reference source to minus full scale plus ½ LSB.

The calibration of D/A converters is similar but even simpler. Zero digital input is applied to the converter and the offset trimming potentiometer is adjusted to give zero analog output. The full scale digital input is applied and the gain trimming potentiometer adjusted to give analog full scale output minus 1 LSB.

A/D Converter Rapid Selection Guide

The Rapid Selection Guide presented below is a capsule summary of all of Datel Systems' A/D converter lines. Because we manufacture the broadest line of A/D converters in the industry, this table is a useful guide for quickly locating the converters, by price range and performance, that are best suited for your particular application.

After locating the desired converter series, turn to the following pages which present more detailed specifications of the various models in tabular form.

Converter Type	Series	Resolution	Conversion Method	Conversion Time	Tempco	Price Range	See Page
1	ADC-Econo	6 Bits	Count Up	50 µsec.	100 ppm/°C	\$29.95	20
General	ADC-89A	8 Bits	Count Up	100-200 µsec.	50 ppm/°C	\$69.00	20
Purpose	ADC-D, K	8, 10, 12 Bits	Succ. Approx.	50 µsec.	30-50 ppm/°C	\$ 79 - \$139	20
- 10 terral	ADC-MA	10, 12 Bits	Succ. Approx.	20-40 µsec.	30 ppm/°C	\$ 95 - \$145	20
LIC-4	ADC-149	14 Bits	Succ. Approx.	50 μsec.	15 ppm/°C	\$239.00	22
	ADC-CM	8, 10, 12 Bits	Succ. Approx.	250-350 μsec.	30 ppm/°C	\$149 - \$169	22
	ADC-L, M	8, 10, 12 Bits	Succ. Approx.	4-20 µsec.	10 ppm/°C	\$135 - \$349	22
	ADC-E	8, 10, 12 Bits	Dual Slope	312 µsec 5 msec.	50 ppm/°C	\$ 79 - \$ 99	24
Type Low Cost A General A Purpose A A A Performance A A A Dual Slope A A A Jltra-Fast A A A Monolithic A A A A A A A A A A A A A A A A A A A A A A A A A	ADC-ER	8, 10, 12 Bits	Dual Slope	43.3-76.7 msec.	35 ppm/°C	\$ 79 - \$ 99	24
	ADC-EP	14 Bits	Dual Slope	230 msec.	13 ppm/°C	\$29.95 \$69.00 \$ \$ 79 - \$139 \$ 95 - \$145 \$239.00 \$149 - \$169 \$135 - \$349 \$ 79 - \$ 99 \$ 79 - \$ 99 \$ 79 - \$ 99 \$179.00 \$ 85 - \$209 \$275 - \$325 \$ 79.00 \$249.00 \$239 - \$349 \$695 - \$895	24
	ADC-EH	8, 10, 12 Bits	Succ. Approx.	2.0-8.0 µsec.	30-50 ppm/°C	\$ 85 - \$209	26
	ADC-N, P	8, 10, 12 Bits	Succ. Approx.	2.0-4.0 μsec.	20 ppm/°C	\$275 - \$325	26
	ADC-SH4B	4 Bits	Succ. Approx.	500 nsec.	200 ppm/°C	\$29.95 \$69.00 \$79 - \$139 \$95 - \$145 \$239.00 \$149 - \$169 \$135 - \$349 \$79 - \$99 \$79 - \$99 \$179.00 \$275 - \$325 \$79.00 \$2249.00 \$239 - \$349 \$695 - \$895 * * \$13.50 - \$36 \$85 - \$155 \$119 - \$195 *	26
	ADC-EH12B3	12 Bits	Succ. Approx.	2.0 µsec.	30 ppm/°C	\$249.00	28
TypeSeriesResolutionLow Cost General PurposeADC-Econo6 BitsADC-89A8 BitsADC-D, K8, 10, 12 BitsADC-MA10, 12 BitsHigh PerformanceADC-14914 BitsADC-L, M8, 10, 12 BitsADC-L, M8, 10, 12 BitsADC-L, M8, 10, 12 BitsADC-L, M8, 10, 12 BitsADC-E8, 10, 12 BitsADC-E8, 10, 12 BitsADC-E8, 10, 12 BitsADC-ER8, 10, 12 BitsADC-EP14 BitsADC-EP14 BitsADC-SH4B4 BitsADC-SH4B4 BitsADC-G, H4,6,8, 10 BitsADC-UH, VH4, 6, 8 BitsADC-TV8 Bits	Succ. Approx.	400 nsec1.0 µsec.	20-50 ppm/°C	\$239 - \$349	28		
Offra-Fast	ADC-UH, VH	4, 6, 8 Bits	Parallel (Flash)	40-200 nsec.	50 ppm/°C	\$695-\$895	28
	ADC-TV	8 Bits	Parallel (Flash)	60 nsec.	100 ppm/°C	\$29.95 \$69.00 C \$ 79 - \$139 \$ 95 - \$145 \$239.00 \$149 - \$169 \$135 - \$349 \$ 79 - \$ 99 \$ 79 - \$ 99 \$ 79 - \$ 99 \$ 79 - \$ 99 \$ 275 - \$325 \$ 79.00 \$2249.00 C \$239 - \$349 \$695 - \$895 * \$ 13.50 - \$36 \$ 85 - \$155 \$119 - \$195 *	28
Monolithic	ADC-EK	8, 10, 12 Bits	Volt. to Freq.	1.25-20 msec.	40 ppm/°C	\$ 13.50 - \$36	30
	ADC-HX	12 Bits	Succ. Approx.	20 µsec.	20 ppm/°C	\$ 85 - \$155	30
	ADC-HZ, HS	12 Bits	Succ. Approx.	8 µsec.	20 ppm/°C	\$119 - \$195	30
Hybrid	ADC-HC	12 Bits	Succ. Approx.	300 µsec.	20 ppm/°C	*	30
	ADC-HF	12 Bits	Succ. Approx.	2 µsec.	20 ppm/ ^b C	*	30
	ADC-HU	3 Bits	Parallel	20 nsec.	5 ppm/°C	*	30

*To be announced

Low Cost, General Purpose A/D Converters

	Model	Resolution	Accuracy (% FS)	Conversion Time	Output Coding (2)	Input Ranges
	ADC-Econo.	6 Bits	0.8%	50 µsec.	Bin	+5, +10, ±2.5, ±5∨
Lowest Cost	ADC-89A8B	8 Bits	0.2%	200 µsec.	Bin	0 to +10V, ±5V
Lowest Cost Low Cost Successive Approximation	ADC-89A8D	2 Digits	0.5%	100 µsec.	BCD	0 to +10V
Successive	ADC-D8B	8 Bits	0.2%		201.002	
	ADC-D10B	10 Bits	.05%	50 µsec.	Bin, 2C	0 to +10V, ±5V
	ADC-D12B	12 Bits	.01%		1 201	
Low Cost	ADC-K8B	8 Bits	0.2%			
Successive	ADC-K10B	10 Bits	.05%	50 µsec.	Bin, 2C	0 to +10V, ±5V
Approximation	ADC-K12B	12 Bits	.01%	198 12		
	ADC-MA10B2A	10 Bits	.05%	40 µsec.		
	ADC-MA10B2B	10 Bits	.05%	20 µsec.	Bin, 2C	0 to +5, +10V
ADC-12QZ	ADC-MA12B2A	12 Bits	.01%	40 µsec.	Din, 20	±2.5, ±5, ±10V
	ADC-MA12B2B	12 Bits	.01%	20 µsec.	1.1.1.2.20	

NOTES: 1. An optional high impedance buffer amplifier is available on special order to give 1000 megohms input impedance. Add \$20.00 to price.

2. Coding: Bin = Straight binary or offset binary

BCD = Binary coded decimal

2C = Two's complement

ADC-ECONOVERTER: This lowest cost model is a counting type converter with 6 bit resolution and 50 μ sec. conversion time for a full scale conversion.

ADC-89A SERIES: These low cost models are 8 bit binary or 2 digit BCD counting type converters with 200 and 100 μ sec. conversion times respectively.

ADC-D SERIES: This series uses successive approximation for 8, 10, and 12 bit resolutions with conversion time of 50 µsec.

ADC-K SERIES: These models are also low cost successive approximation types with 8, 10, and 12 bit resolutions and 30 ppm/℃ tempco.

ADC-MA SERIES: These versatile 10 and 12 bit models feature pin programmable operating features with conversion times of 40 and 20 μ sec. The ADC-MA12B2A is a pin and performance equivalent of the popular ADC-12QZ model.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible outputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 283 and 284 for information on Extended Performance versions.



Linearity	Input Impedance	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page		
1/2 LSB	4.2 K	100 ppm/°C	±15V, +5V	2 x 2 x 0.375	\$29.95			
1/2 LSB	5 K	50 ppm/°C	±15V, +5V	3 x 2 x 0.375	\$69.00	*		
1/2 L3B 5 K	oo ppin/ c	±13V, 13V	5 × 2 × 0.575	\$69.00				
1/2 LSB 10 K				\$ 79.00				
	50 ppm/℃	±15V, +5V	±15V, +5V	±15V, +5V	n/°C ±15V, +5V 4 x 2 x 0.4	4 x 2 x 0.4	\$105.00	*
			marker of the second	\$129.00				
					\$109.00			
1/2 LSB	10 K	30 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$129.00	*		
		10,02	11.25	A March March	\$139.00			
	1000 Dec 100 - 100	13.5 Inco		ana ana cu	\$95.00	all a second		
1/2 LSB 2.5, 5, 10 K	30 ppm/°C	±15V, +5V	$4 \times 2 \times 0.4$	\$125.00	51			
1/2 200	(1)	oo ppin/ o	-10V, 10V	T A Z A U.T	\$125.00			
					\$145.00			

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

*Contact nearest Datel sales office for data sheet.

High Performance A/D Converters

	Model	Resolution	Accuracy (% FS)	Conversion Time	Output Coding (2)	Input Ranges	
14 Bits	ADC-149-14B	14 Bits	.005%	50 µsec.	Bin, 2C	-10, -20, ±5, ±10V	
	ADC-CM8B	8 Bits	0.2%	250 µsec.			
Low Power CMOS	ADC-CM10B	10 Bits	.05%	300 µsec.	Bin	-5,-10,±5,±10V	
- (115 m	ADC-CM12B	12 Bits	.01%	350 µsec.			
Low Power CMOS High Performance Successive Approximation High Performance Successive	ADC-L8B	8 Bits	0.2%	12 µsec.			
	ADC-L10B	10 Bits	.05%	16 µsec.	Bin, 2C	+5, +10, ±5, ±10V	
	ADC-L12B	12 Bits	.01%	20 µsec.			
Approximation	ADC-L8D	2 Digits	0.5%	12 µsec.	— BCD	0 to +5, +10V	
and the second second	ADC-L12D	3 Digits	.05%	20 µsec.		0.00,0,0,000	
	ADC-M8B	8 Bits	0.2%	4.0 µsec.			
High	ADC-M10B	10 Bits	.05%	11.5 μsec;	Bin, 2C	+5, +10, ±5, ±10V	
CMOS High Performance Successive Approximation High Performance Successive	ADC-M12B	12 Bits •	.01%	13.0 µsec.			
Approximation	ADC-M8D	2 Digits	0.5%	4.0 µsec.	— BCD	0 to +5, +10V	
and the second states and	ADC-M12D	3 Digits	.05%	13.0 µsec.	000	010 +5, +100	

NOTES: 1. An optional high impedance buffer amplifier is available on special order to give 10 megohms input impedance. Add \$20.00 to price.

2. Coding: Bin = Straight binary on offset binary

- BCD = Binary coded decimal
 - 2C = Two's complement

ADC-149-14B: This low cost, high resolution converter uses the successive approximation method to achieve 14 bit resolution with a 15 ppm/°C tempco. Conversion time is 50 μ sec.

ADC-CM SERIES: These 8, 10, and 12 bit converters use CMOS circuitry to achieve a low power consumption of 140mW for portable and remote instrumentation applications. These units can operate from either a single +12 to +15V supply or from dual ± 12 to $\pm 15V$ supplies.

ADC-L SERIES: These high performance successive approximation converters feature 8, 10, and 12 bit conversions in less than 20 μ sec. and a low tempco of 10 ppm/°C. Specific input voltage ranges must be ordered by model number.

ADC-M SERIES: These models are also fast, high performance successive approximation converters with less than 13 μ sec. conversion time. Tempco is 10 ppm/°C and input voltage ranges must be ordered by model number.

ALL MODELS: have operating temperature range of 0° C to 70°C; have DTL/TTL or CMOS compatible outputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Linearity	Input Impedance	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
1 LSB	5, 10 K	15 ppm/°C	±15V, +5V	4 x 2 x 0.8	\$239.00	55
					\$149.00	
1/2 LSB	25, 50 100 K	30 ppm/°C	+12 to +15V	3 x 2 x 0.8	\$159.00	57
	STR. STR.			\$169.00		
	18.40	1.22 1.80		3 x 2 x 0.375	\$135.00	soul.
					\$155.00	
1/2 LSB	10 K (1)	10 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$175.00	*
					\$135.00	
	Constant Party		in the second second	in the act	\$175.00	
111	Sec. Con Mr.	and they are	and method	3 × 2 × 0.375	\$229.00	1.00
					\$295.00	
1/2 LSB	10 K (1)	10 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$349.00	*
					\$229.00	100
				\$349.00		

GOLD BOOK 76/77

Dual Slope Integrating A/D Converters

	Model	Resolution	Accuracy (% FS)	Conversion Time	Output Coding (2)	Input Ranges
	ADC-E8B	8 Bits	0.2%	312 µsec.		
Low Cost Fast	ADC-E10B	10 Bits	.05%	1.25 msec.	S.M. Bin	±1, ±5, ±10V
	ADC-E12B	12 Bits	.01%	5.0 msec.		
Integrating High	ADC-E8D	2 Digits	0.5%	500 µsec.	SM BCD	±2, ±5, ±10V
I FONGER !!	ADC-E12D 3 Digits .05% 5.0 msec.	-2, -3, -10 V				
•	ADC-EP14B	14 Bits	.01%	230 msec.	S.M. Bin	±2V (1)
Resolution	ADC-EP16D	4 Digits	.01%	230 msec.	S.M. BCD ± .0 msec. 30 msec. 30 msec. S.M. BCD ±	±2V (1)
	ADC-ER8B	8 Bits	0.2%	43.3 msec.		
ntegrating High Resolution	ADC-ER10B	10 Bits	.05%	43.3 msec.	S.M. Bin	±1V (1)
Ratiometric	ADC-ER12B	12 Bits	.01%	43.3 msec.		
	ADC-ER8D	2 Digits	0.5%	76.7 msec.	S.M. BCD	±2V (1)
	ADC-ER12D	3 Digits	.05%	76.7 msec.	J.W. BCD	÷∠v (1)

NOTES: 1. Has four wire ratiometric inputs

2. Coding: S.M. Bin = Sign-magnitude binary

S.M. BCD = Sign-magnitude BCD

ADC-E SERIES: These models feature 8, 10, and 12 bit resolution with both binary and BCD coding. Conversion time is from $312 \,\mu$ sec. to 5 msec. depending on the resolution. Coding is sign-magnitude binary or sign-magnitude BCD.

ADC-EP SERIES: These high resolution models feature 14 binary bits or 4 BCD digits with a conversion time of 230 msec. Temperature coefficient is 13ppm/°C. The analog front end of this converter is electrically floated from digital ground to give \pm 300V common mode input range with greater than 100 dB CMR. The input is 4 wire ratiometric with a flying capacitor reference input. An auto zeroing circuit stabilizes zero drift to less than 1µV/°C. A crystal controlled clock results in better than 60 dB normal mode rejection to input frequency noise.

ADC-ER SERIES: This series also features 4 wire ratiometric input along with operation from a single +5V supply. The analog input is differential with 70 dB of common mode rejection. The internal clock can be adjusted for synchronism with the power line frequency to give 40 dB of normal mode rejection to this noise. Resolution is 8, 10, and 12 bits with both binary and BCD models.

ALL MODELS: have operating temperature range of 0°C to 70°C: have DTL/TTL compatible outputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Linearity	Input Impedance	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
					\$ 79.00	
					\$ 89.00	
.01% 100 Meg, 10K	50 ppm/°C	±15V, 5V	4 x 2 x 0.4	\$ 99.00	*	
					\$ 79.00	01
		A STREET		and the second second	\$ 99.00	
.01% 100 Meg.	100 Meg.	eg. 13 ppm/°C ±15V, +5V 4 x 2 x 0.8	4 x 2 x 0.8	\$179.00	- 05	
.0170	TOO Weg.	15 ppm/ C	±15V, +5V	4 X 2 X 0.8	\$179.00	- 65
	4.8	28.02			\$ 79.00	11.00
					\$ 89.00	_
.05%	100 Meg.	35 ppm/°C	+5V	4 x 2 x 0.4	\$ 99.00	61
					\$ 79.00	_
					\$ 99.00	

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

*Contact nearest Datel sales office for data sheet.

Fast A/D Converters

	Model	Resolution	Accuracy	Conversion Time	Output Coding (1)	Input Ranges	
Fast	ADC-EH8B1	8 Bits	0.2%	4.0 μsec.	— Bin, 2C	0 to +10V, ±5V	
8 Bit	ADC-EH8B2	8 Bits	0.2%	0.2% 2.0 μsec.	bin, 20	010+100,±30	
Fast	ADC-EH10B1	10 Bits	.05%	4.0 µsec.	— Bin, 2C	0 to +10V, ±5V	
10 Bit	ADC-EH10B2	10 Bits	.05%	2.0 µsec.	Din, 20	010+100,±30	
	ADC-EH12B1	12 Bits	.01%	8.0 µsec.	— Bin, 2C	0 to +10V, ±5V	
	ADC-EH12B2	12 Bits	.01%	4.0 μsec.	Din, 20	0101100, ±30	
Fast	ADC-N10B	10 Bits	.05%	4.0 μsec.	— Bin	0 to -5, -10V	
10 & 12 Bit	ADC-N12B	12 Bits	.01%	4.0 μsec.	Din	±5, ±10V	
Fast	ADC-P8B	8 Bits	0.2%	2.0 µsec.	— Bin	0 to -5, -10V	
8 & 10 Bit	ADC-P10B	10 Bits	.05%	2.0 µsec.	Diff	±5, ±10V	
4 Bit w. S/H	ADC-SH4B	4 Bits	3.0%	500 nsec.	Bin	0 to +1V	

OTES: 1. Coding: Bin = Straight binary or offset binary

2C = Two's complement

ADC-EH8B SERIES: These 8 bit successive approximation converters feature 4 and 2 μ sec. conversion times at low cost. Temperature coefficient is 50ppm/°C.

ADC-EH10B SERIES: This series of 10 bit converters uses the successive approximation method with 4 and 2 μ sec. conversion times and 30ppm/°C tempco.

ADC-EH12B SERIES: These 12 bit models are also successive approximation types with 8 and 4 μ sec. conversion times. Tempco is 30ppm/°C.

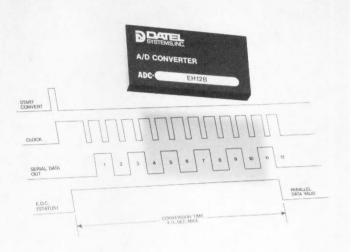
ADC-N SERIES: This series features 10 and 12 bit models both with 4 μ sec. conversion times and 20ppm/°C tempco. Successive approximation is used.

ADC-P SERIES: These 8 and 10 bit models are successive approximation converters both with 2 μ sec. conversion time and 20ppm/°C tempco.

ADC-SH4B: This model is a 4 bit A/D converter with a selfcontained sample-hold circuit. Time for both acquisition and conversion is 500 nsec. This device is designed for optical scanning and fast pulse code modulation applications.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible outputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Linearity	Input Impedance	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
1/2 LSB	4.45 K	50 ppm/°C	±15V, +5V	2 x 2 x 0.375	\$ 85.00	- 37
1/2 LOD	4.43 K	50 ppm/ C	±150, 150	2 × 2 × 0.375	\$129.00	37
1/2 LSB	2.3 K	30 ppm/°C·	±15V, +5V	3 x 2 x 0.375	\$149.00	- 39
1/2 LJD	2.5 K	50 ppm/ C	±150,150	5 X 2 X 0.375	\$189.00	39
1/2 LSB	1/2 LSB 2.3 K	30 ppm/°C	±15V, +5V	4 x 2 x 0.375	\$169.00	- 41
1/2 L3D	2.3 K	SO ppin/ C	±15V, +5V	4 X 2 X 0.375	\$209.00	41
1/2 LSB	500, 1K, 2K	1K 2K 20 ppm/90	+15)/ +5)/	4 x 2 x 0.8	\$275.00	
1/2 L3D	500, TK, 2K	20 ppm/°C	±15V, +5V	4 X Z X U.O	\$295.00	*
1/2 LSB	/2 LSB 500, 1K, 2K	20 ppm/°C	±15V, +5V –	4 x 2 x 0.4	\$305.00	×
1/2 LOD	500, TK, 2K	20 ppm/ C	±150,150 -	4 x 2 x 0.8	\$325.00	'n
2%	50 ohms	200 ppm/°C	±15V, +5V	2 x 2 x 0.375	\$ 79.00	*

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

* Contact nearest Datel sales office for data sheet.

Ultra-Fast A/D Converters

	Model	Resolution	Accuracy	Conversion Time	Output Coding	Input Ranges	
12 Bit, 2 µsec.	ADC-EH12B3	12 Bits	.01%	2.0 µsec.	Bin, 2C	0 to +10V, ±5V	
100 /D:+	ADC-G8B	8 Bits	0.2%	800 nsec.	Din 20	F 10 +F +10V	
100 nsec./Bit	ADC-G10B	10 Bits	.05%	1.0 µsec,	Bin, 2C	-5, -10, ±5, ±10V	
	ADC-H4B	4 Bits	3.0%	400 nsec.	110		
100 /0:4	ADC-H6B	6 Bits	0.8%	600 nsec.		0 to - 5, - 10V	
100 nsec./Bit	ADC-H8B	8 Bits	0.2%	800 nsec.	Bin, 2C	±5V, ±10V	
	ADC-H10B	10 Bits	.05%	1.0 µsec.			
A STATISTICS	ADC-VH4B	4 Bits	3.0%	100 nsec.		No.	
Parallel Type	ADC-VH6B	6 Bits	0.8%	200 nsec.	Bin	0 to -2.56 (1)	
	ADC-VH8B	8 Bits	0.4%	200 nsec.			
	ADC-UH4B	4 Bits	3.0%	40 nsec.			
Parallel Type	ADC-UH6B	6 Bits	0.8%	100 nsec.	Bin	0 to -2.56 (1)	
	ADC-UH8B	8 Bits	0.4%	100 nsec.			
8 Bit Video	ADC-TV8B	8 Bits	0.2%	50 nsec.	Bin	±0.25 to ±10V (2	

NOTES: 1. Bipolar versions are also available with ±1.28V input. Add \$50.00 to price.

2. Input can be configured for unipolar operation by user. Input impedance is 50 ohms for $\pm 0.25V$ input.

3. Coding: Bin= Straight binary or offset binary 2C = Two's complement **ADC-EH12B3:** This 12 bit converter with 2 μ sec. conversion time is the fastest 12 bit modular converter in the industry. Unipolar or bipolar operation is achieved by pin connection.

ADC-G SERIES: These converters feature conversions of 100 nsec. per bit for 8 and 10 bit conversions with a tempco of 50 ppm/ $^\circ$ C.

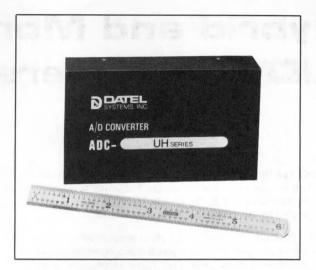
ADC-H SERIES: This series also features 100 nsec. per bit for 4 through 10 bit conversions. Tempco is 20 ppm/°C.

ADC-VH SERIES: These models use the parallel (or flash) conversion technique to realize a 4 bit conversion in 100 nsec. and 6 or 8 bit conversions in 200 nsec.

ADC-UH SERIES: This series is identical with the VH series except for faster conversion speed of 40 nsec. for 4 bits and 100 nsec. for 6 or 8 bits.

ADC-TV8B: This soon to be available model is a small circuit card made up of hybrid and monolithic components. It performs 8 bit conversions at better than 15 MHz rate.

ALL MODELS: Have operating temperature range of 0°C to 70°C; have DTL/TTL compatible outputs (ADC-TV8B has ECL compatible outputs); use DILS-1 or DILS-2 dual-in-line strips for sockets (ADC-TV8B uses a standard edge connector).



See pages 284 and 285 for information on Extended Performance versions.

Linearity	Input Impedance	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
1/2 LSB	1.15 K	30 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$249.00	43
1/2100	E00 1K 2K	50 mm ⁶ 0	+151/ -151/	4 x 2 x 0.4	\$239.00	
1/2 LSB	500, 1K, 2K	, 2K 50 ppm/°C ±15V, +5V	4 × 2 × 0.8	\$279.00	45	
		5. martin 8		4 × 2 × 0.4	\$279.00	
1/2 1 2 2	500 414 014	00 ⁰ 0	and the second second	4 × 2 × 0.4	\$299.00	**
1/2 LSB 500, 1K, 2K	20 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$319.00		
			4 × 2 × 0.8	\$349.00		
1/2 LSB	1.0	Contra Co	- 10 - ATP 8	RMS: IX A. TO	\$695.00	
1/2 LSB	100 ohms	50 ppm/°C	±15V, ±5V	5 x 3 x 1.15	\$745.00	**
1 LSB					\$795.00	-
1/2 LSB	1991 March 1997	9.0	40. M68	RIA STATE	\$795.00	
1/2 LSB	100 ohms	50 ppm/°C	±15V, ±5V	5 x 3 x 1.15	\$845.00	47
1 LSB	U. C. Starting Street	80	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1		\$895.00	- Aller
1/2 LSB	50 ohms (2)	60 ppm/°C	±15V, ±5V	7.5 x 4.25 x 0.875	*	**

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

*To be announced

**Contact nearest Datel sales office for data sheet and availability.

Hybrid and Monolithic A/D Converters

ADC-EK SERIES: This series of monolithic converters are integrating devices using the voltage to frequency conversion principle. Resolutions of 8, 10, and 12 binary bits and 3 BCD digits are offered. An external reference is required.

ADC-HX SERIES: This series of hybrid models offer 12 bit conversion in 20 μ sec. The units have pin-programmable input ranges and short cycling capability. Three temperature range versions are available.

ADC-HZ SERIES: These hybrid converters give 12 bit resolution in only 8 μ sec. conversion time. Pin-programmable input ranges and short cycle capability are featured. Short cycling results in 10 bit conversion in 6 μ sec. and 8 bit conversion in 4 μ sec. Three temperature range versions are available.

	Model	Resolution	Accuracy	Conversion Time	Output Coding	Input Ranges
New!	ADC-EK8B	8 Bits	0.2%	1.25 msec.	Bin	
Monolithic	ADC-EK10B	10 Bits	.05%	5 msec.	Bin	0 + 10 1514
	ADC-EK12B	12 Bits	.01%	20 msec.	Bin	0 to +10, ±5V
Series	ADC-EK12D	3 Digits	.05%	10 msec.	BCD	
- 00 - 44	ADC-HX12BGC					
New! Hybrid 12 Bit, 20 µsec.	ADC-HX12BMR	12 Bits	.01%	20 µsec.	C Bin, C 2C	0 to +5, +10V
12 Dit, 20 µsec.	ADC-HX12BMM					±2.5, ±5, ±10V
00.8612	ADC-HZ12BGC					1.50
New! Hybrid	ADC-HZ12BMR	- 12 Bits	.01%	8 µsec.	C Bin, C 2C	0 to +5, +10V
12 Bit, 8 μsec.	ADC-HZ12BMM			n i men in		±2.5, ±5, ±10V
Coming! Hybrid	ADC-HS12B (1)	12 Bits	.01%	8 µsec.	C Bin, C 2C	+5, +10, ±2.5, ±5, ±10V
Coming! 12 Bit	ADC-HC12B	12 Bits	.01%	300 µsec.	Bin, 2C	+5, +10, ±2.5, ±5, ±10V
Hybird CMOS	ADC-HC12D	3 Digits	.05%	300 µsec.	BCD	0 to +5, +10V
Coming! Hybrid	ADC-HF12B	12 Bits	.01%	2 µsec.	Bin, 2C	+5, +10, ±2.5, ±5, ±10V
Coming! Hybrid	ADC-HU3B	3 Bits	6%	20 nsec.	Bin	±2.5V

NOTES: 1. The ADC-HS12B has an internal sample hold circuit ahead of the A/D converter.

2. Coding: Bin = Straight binary or offset binary

- 2C = Two's complement
- BCD = Binary coded decimal

C Bin = Complementary binary or comp. offset Bin

C 2C = Complementary two's complement

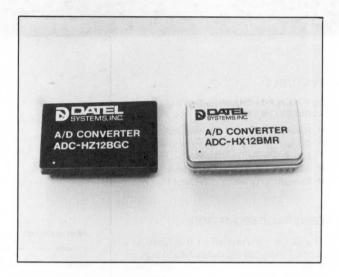
ADC-HS12B: This model combines a 12 bit 8 usec, converter and a sample-hold circuit into a single hybrid package. Coming soon.

ADC-HC SERIES: These models are 12 bit hybrid CMOS devices for low power applications. Coming soon.

ADC-HF12B: This ultra speed hybrid converter provides 12 bit conversion in just 2 µsec. Coming soon.

ADC-HU3B: This hybrid model is a 3 bit parallel (flash) type. A 3 bit conversion is performed in 20 nsec. Several units may be used together to make an ultra fast 8 bit A/D converter. Coming soon.

ALL MODELS: Have operating temperature range of 0°C to 70°C except for those models specified otherwise; have DTL/TTL compatible outputs except for ADC-HC which has CMOS compatible outputs; use DILS-1 or DILS-2 dual-in-line strips for sockets except for ADC-IC and ADC-EK.



Linearity	Temp. Range	Gain Tempco.	Power Requirement	Case Size (inches)	Price (1-9)	See Page
Levis.	10 th 10 th			and the second second	\$13.50	- **
1/2 LSB	0 to 70C	10 mm PC			\$26.00	
1/2 L3D	010700	40 ppm/ ^o C	±5V	24 Pin DIP	\$36.00	
					\$29.00	17 NO 15
	0 to 70C			10000	\$ 85.00	with the last
1/2 LSB	-25 to +85C	20 ppm/°C	±15V, +5V	32 Pin DIP	\$125.00	33
	- 55 to +100C				\$155.00	
	0 to 70C			Trate to	\$119.00	Le Le ser
1/2 LSB	-25 to +85C	20 ppm/°C	±15V, +5V	32 Pin DIP	\$169.00	33
	- 55 to +100C				\$195.00	
1/2 LSB	0 to 70C	20 ppm/°C	±15V, +5V	32 Pin DIP	*	**
1/2 LSB	SB	20 nnm /°C	+151/ +51/	22 8:- 010	*	1021.8
1/2 LSB	- 0 to 70C	20 ppm/°C	ppm/°C ±15V, +5V	32 Pin DIP	*	- **
1/2 LSB	0 to 70C	20 ppm/°C	±15V, +5V	32 Pin DIP	*	rich geben
0.2%	0 to 70C	5 ppm/°C	±5V	32 Pin DIP	*	- **
1.5		Lindi kan	*	To be announced	Addition of the second second	12.5.5

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

** Contact nearest Datel sales office for data sheet and availability.



DATA ACQUISITION SYSTEM PROGRAMMER SEQUENCER

MODEL SCL-1

FEATURES

LOW POWER 16 CHANNEL DATA ACQUISITION SYSTEM CONTROL LOGIC

- Random/Sequential Channel Selection
- Gated Inputs for Computer Bus or Party Line Operation
- 16 Channel Capacity-Expandable
- Compatibility with Other Datel Modules

GENERAL DESCRIPTION

The SCL-1 provides all of the necessary control logic that is needed to integrate Datel's multiplexer, sample and hold, and A/D converters into a working 16 channel data acquisition system, all at substantial cost savings over prepackaged systems and with the additional choice of speed and performance specs of the components.

The SCL-1 reduces the basic external control functions to a simple ready/ busy - strobe technique while providing both random or sequential channel selection modes. Other features include all the necessary controls for easy computer interfacing such as device select and strobe inputs for party line operations. All significant inputs are carried through the SCL-1 for system variations.

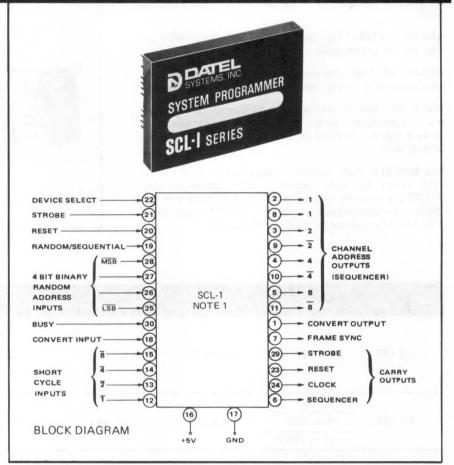
The SCL-1 also has provisions for short cycle (less than 16 channel operation) and provides a frame sync output at channel 1 for system expansion.

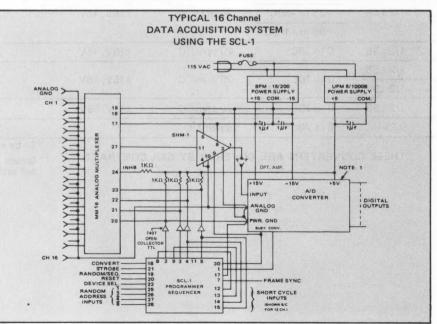
A single SCL-1 is capable of handling one Model MM-16 analog multiplexer for a 16 channel single ended system or an MMD-8 analog multiplexer for an 8 channel differential system. Channel capacity can be expanded, in the increments mentioned above, by simply adding MM-16's and SCL-1's. By employing the AM-201 instrumentation amplifier, a low level differential system can be configured for transducer monitoring and digital processing. With the exception of the SHM-2, all of Datel Systems' sample and hold circuits can be connected directly to the SCL-1. Datel's selection of A/D converters will allow for high conversion speeds with 8 bit to 14 bit resolution.

Price (1-9) \$69.00

NOTE:

For low power applications contact Datel for information on Model SCL-CM







LOW COST, 12 BIT HYBRID ANALOG TO DIGITAL CONVERTERS

ADC-HX, ADC-HZ SERIES

FEATURES

- 12 Bit Resolution
- ▶ 8 or 20µSec. Conversion
- Programmable Ranges
- Internal Buffer Amp.
- Short Cycle Capability
- Glass or Metal Package

GENERAL DESCRIPTION

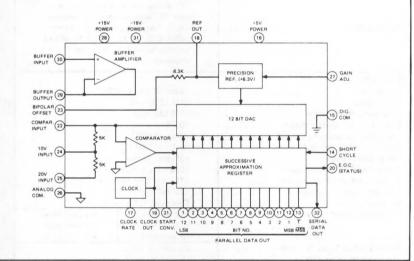
The ADC-HX12B and ADC-HZ12B are selfcontained, high performance, 12 bit A/D converters manufactured with thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12 bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, $\pm 2.5V$, $\pm 5V$, and $\pm 10V$. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

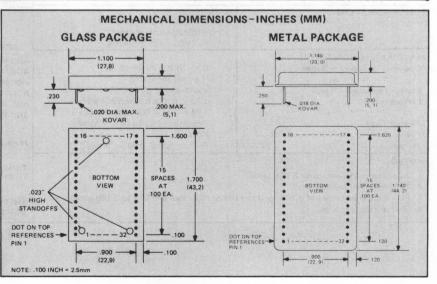
These converters utilize a fast 12 bit DAC consisting of tightly matched monolithic quad current switches, a stable nichrome thin-film resistor network, and a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12 bit successive approximation register, a clock, and a monolithic buffer amplifier. The thin-film resistor network is functionally trimmed by a laser to precisely set the 8-4-2-1 current weighting in the guad current switches. The close tracking of the thin-film resistor and guad current switches result in a differential nonlinearity tempco of only ±2ppm/°C. Gain tempco is ±20ppm/°C maximum.

Both models have identical operation except for conversion speed. They can be shortcycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3 μ sec., the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. Serial data is also brought out. The package is a 32 pin hermetically sealed glass or metal case. Six different models are offered covering the operating temperature ranges of 0 to 70°C, -25 to +85°C, and -55 to +100°C.



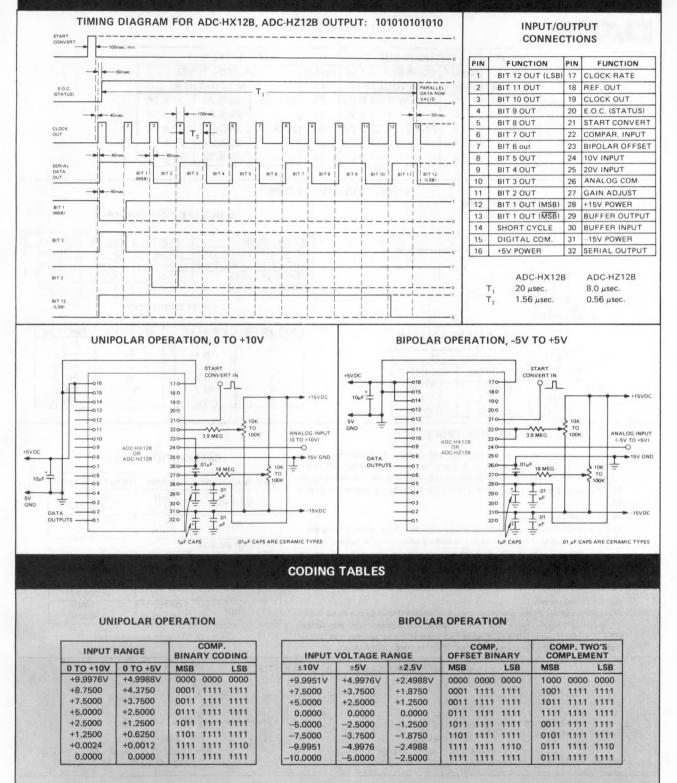
(ACTUAL SIZE)





ADC-HX12B ADC-HZ12B 1. It is recommended that the ±15V power inpu pins both be bypassed to ground with a .01µf ceramic capacitor in parallel with a 1µF electro lytic capacitor and the ±5V power input pins both	SPECIFICATIONS, Typical at 25°C, ±15V and +5V supp	olies unless otherv	vise noted)	TECHNICAL NOTES		
Autos por Ranges, unçolor 0 : 0 : 90, 0 : 10/0; FS Autos por Ranges, backer 1: 2, 92, 91, 10/2; FS Input Impediance with Buffer 1: 2, 92, 10/2; FS Input Impediance with Buffer 1: 0, 10/2; FS Stard Competition 1: 0, 10/2; FS Stard Competition 1: 0, 10/2; FS Stard Competition 1: 0, 20/2; FS Coding, Unpole 1: 0, 20/2; FS <th></th> <th></th> <th>A REAL PROPERTY AND A REAL</th> <th>1 It is recommended that the +151/ nower input</th>			A REAL PROPERTY AND A REAL	1 It is recommended that the +151/ nower input		
Analog maps. Impout 2.5 U - SV , 10V - SV 1.5 U - SV , SV +			L			
1put Impedance 2.5K (0 to +5V, 2.5V) 5K (0 to +10V, 10V) 5K (0 to +10V, 10V) 1put Impedance with Buffer 10K (10V) 1put Impedance with Buffer 125A (Vp, 2.5V) 1put Gouveries 2000 (10000 (1000 (1000 (1000 (1000 (1000 (1000 (1000 (1000 (1000 (1000 (1		the state of the state of the state of the				
bK (0 to -100/, :EV) input impedance with Buffer 100 Megams input imput imacurant of Buffer 120 A typ, 250A max. :15V 125 M max. partitive guita with input image imacurant interment 2 arXiv Start Convention 2 arXiv UTPUTS' 12 parallel lines of data held until next conversion Logic '0'' initiates conversion. Logic '0'' initiates conversion. Logic '0'' initiates conversion. Logic '0'' initiates conversion compaint. Coding, unipolar				lytic capacitor and the +5V power input pin b		
Input Impedance with Buffer 100 (± 1010) Input Bis Current of Buffer 1250A 170p, 250A max. Input Bis Current of Buffer 1250A 170p, 250A max. Start Conversion 2V mit, to 5 SW max, positive pulse with duration of 100mer. Input Bis Current of Buffer 100 (± 1000) Start Conversion 2V mit, to 5 SW max, positive pulse with duration of 100mer. Loading: 1 TTL lead Digital Gormmon (in 15) and Anales Commonded that the task Etwaw in the connection and 2159 positive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration in the connection and 2150 possitive pulses with duration possitive pulses with and duration in the connection and 2150 possitive pulses with and 20 possitive pulses with duration possitive pulses with and 20 possithand 20 possithand 20 possitive pulses with and 20 possithand 20	Input Impedance					
Input Bing Umpetance with Buffer 100 Meganns input Bing Umpetance with Buffer 120 An typ, 250M max. 15W Start Conversion 2V min. to 5.5V max, positive pulse with duration of 100msc. min. Rise and fail umes. 30msc. 20. Logic "1" relation converter Logic "1" relation converter conversion converter Logic "1" relation converter Logic "1" relation converter Logic "1" relation converter Logic "1" relation converter conversion tarts signal. Output signal Listing Tarts (1) the converter to not converter to conversion tarts signal Conversion (Statua) 2. External adjustment of converter to not conversion conversion to not conversion tarts signal. Conversion tarts signal conversion conversion conversion to not conversion tarts signal. Conversion tarts signal conversion (Statua) 2. External adjustment of conversion tarts to not conversion tarts signal conversion conversion to not conversion (Statua) 2. External adjustment of conversion to a trans to be conversion tarts signal conversion (Statua) 2. 2. External adjustment of the conversion conversion to not conversion tarts signal conversion (Statua) 2. 2. 2. 2. 2. 2. 2. 2.	and the second of the second sec	5K (0 to +10V, ±	5V)			
100 magazine 100 magazine 100 magazine 22 min. to 55 max. positive gula with dury tom of 100 mc. mi. Rise and fait times < 30 mc.		10K (±10V)				
Input Bick Current of Buffer 125A Typ, 250A max. Input Overviews 2V min: to 55V max, positive pulse with duration of 100mex. 2.0 jailed Common (jain 15) and Analysi Common (jain 15) and Jain (jain 16) and Jain 16) and Jain 10	Input Impedance with Buffer	100 Megohms				
19but Oraverblage -15V Start Conversion 2V min. to 5.5V max, positive pulse with duration of 100msc. min. Rise and fail times - 30msc. 2 Logic ''' rests converter Logic ''' rests converter Complementary York Complement NY 2UC ('''' - 0.42V Complementary York Status) 2. External adjustment of zero or offstan dag in an Provided for 'v' training posts should be conversion status signal. Output is fold ''' during rest and conversion and logic '''' when conversion complets. Train of postiwe policy bin 17 grounded. 2. External adjustment of zero or offstatus is fold to rest training posts should be located as pression complets. Train of postiwe policy bin 17 grounded. End of Conversion (Status) 12 bits (1 part in 4096) = 12 bits (1 part in 4006) = 12 bits (1 part in 4096) = 12 bits (1 part in 4000m) = 12 bits (1 part in 400m) = 12 bits (1 part in 4			A max			
Start Conversion 2V min. to 55W max, positive pulse with duration of 100mex, min. Rise and fail turnes < 30 mix.			A HIGAT			
duration of 100nsec, min, Rus and fail times - 30nsec. and therefore muscles as intercity a provided for two memorands that be the commended that			any positive pulse with			
UTPUTS' possible external science. UTPUTS' 12 parallel lines of data held until next Parallel Output Data 12 parallel lines of data held until next Coding, unipolar 12 parallel lines of data held until next Coding, unipolar 12 parallel lines of data held until next Coding, unipolar 12 parallel lines of data held until next Coding, unipolar Complementary Bray Coding, unipolar Complementary Mrest Binary Coding Complementary Mrest Binary Coding Complementary Mrest Binary Coding, UT 12 List Coding Complementary Mrest Binary Coding Complementary Mrest Binary Coding Complementary Mrest Binary Coding Complementary Mrest Binary Coding Complementary Brest Binary Coding Complementary Mrest Binary Coding Complementary Brest Binary Coding Complementary Brest Binary Coding Complementary Brest Binary <t< td=""><td>Start Conversion</td><td></td><td></td><td></td></t<>	Start Conversion					
UTHER Scatures Logic "0" instate conversion. Logic "0" instate conversion. Logic "0" instate conversion. Logic "0" instate conversion. Logic "0" instate conversion. Terrarelle Output Data 12 parallel lines of data held until next. VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "0" > 1-0.4V VOUT "10" > 1-2.4V Consplementary Brany Complementary Green Brany Complementary Orders Brany Complementary Green Status End of Conversion (Status) Complementary Green Status Signal. Output is logic "1" during reset and conversion and logic "0" when conversion camplete. ERFORMANCE Train of positive going 450 '100nse. Status 1.2 bits 11 part in 4069) 11/2 LSB max. 1.0 % of FSR ¹ 12/12 LSB max. 1.0 % of FSR ¹ 10 bits '1 These conversion complementary 2 sources of the conversion during the conversion d			ec. min. Alse and fait			
Logic "0" initiates conversion. bower ground should be run to pin 28 wherea UTPUTS' 12 parallel lines of data held until next arailel Output Data 12 parallel lines of data held until next coding, unipolar YOUT '('') 4 4-3.4 Coding, bipolar Complementary Offest Binary Complementary Offest Binary Complementary of Complement NC2 voiresion explores on the convertion and logic '0" where coversion complete. Intervention explores on the covertion and logic '0" where coversion explores on and logic '0" where explores on and logi						
Loading: 1 TTL load digital ground and +5V ground should be run to more state (Dutput Data 12 parallel lines of data held until next conversion command. 3: External adjuttment of zero or offset and gain an to conversion command. 20ding, unipolar Complementary Offset Sinary Complementary Offset Complement WUUT (*1') > +2.4V 3: External adjuttment of zero or offset and gain an types (such as bet 5xtem) TM enteres (The WUUT (*1') > +2.4V Coding, unipolar Complementary Offset Complement WUUT (*1') > +2.4V 5: External adjuttment of zero or offset and gain an types (such as bet 5xtem) TM enteres (The WUUT (*1') > +2.4V Coding, unipolar Complementary Offset Complement WUUT (*1') > +2.4V 5: External adjuttment of zero or offset and on a set to set the conversion (the complementary offset complementary work the necessary. End of Conversion (Status) "'' during rest and conversion completes train of positive going 5V 100brics pales, 600 kHz for ADCLH212B (pin 17 grounded). This is conversion (the set two cases the cloc train of positive going 5V 100brics pales do the set two cases the cloc train adjuttment of zero or offset and gain an train of positive going 5V 100brics pales do the set the adjuttment conversion to the set the adjut of the set two cases the cloc train adjuttment of zero or offset train of positive going 5V 100brics pales do the set the adjut of the set two cases the cloc train of positive going 5V 100brics pales do the set the adjut of the set two cases the cloc train of positive going 5V 100brics pales do the set the adjut of the set two cases the cloc train of positive gorthe set the adjut of the set two train of posititwe going 5V 10br						
UTPUTS1 pin 15. 12 parallel lines of data held until next conversion command. VOUT ("1") > 4.04V VOUT ("1") > 4.24V pin 15. 20ding, unipolar Complementary Binary Complementary Dirat Binary Complementary Dirat Binary Complementary Two's Complement The Successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding 100K ohrea and should be 100ppm/"C enter 100K ohrea and conversion complete. 100K ohrea and bould be 100ppm/"C enter 114 C to be attr 14 to the output bin the two convertion 14 to the output bin the two convertion 14 to the output bin of short cycled conversion sing the cher 14 to the output bin of short cycled conversion sing the transition 14 to the output bin of short cycled conversion sing the should be the 14 to the output bin of short cycled conversion sing the should be the 14 to the output bin sing the should be the 14 to the output bin sing the 14 to the output bin sing the 14 to th						
JTPUTS ¹ 12 parallel lines of data held until next conversion command. 3. External adjustment of zero or offset and gains and to put from the between 10K and Yourt for 11° > 2 + 2.4V Loding, unipolar Complementary Wies (A out to be between 10K and Yourt for 11°) > 2 + 2.4V Loding, unipolar Complementary Work Complementary Work Complementary Yorks Complementary Work Complementary Works Complementary Work		Loading: 1 TTL Ic	bad			
arailel Output Data 12 parallel lines of data held until next comversion command. YOUT ("0") < 4.0.4V YOUT ("0") > 4.0.4V YOUT ("1") = 4.0.4						
conversion command. netted as shown in the connection diagrams. The value scale is 0.2% of SR1 for zero or offse and 30.3% of SR1 for zero or offse and 20.3% of SR1 for zero or offse and						
Componential: Componential: Componential: Componenti: </td <td>arallel Output Data</td> <td>12 parallel lines of</td> <td>data held until next</td> <td></td>	arallel Output Data	12 parallel lines of	data held until next			
VOUT ("1") < 40.4V						
Vour ("1") > +2.4V Complementary Binary Complementary Offset Binary Complementary Vords V		VOUT ("0") ≤ +0	.4V			
cdaing, uipolar Complementary Binary Complementary Offset Binary Complementary Toffset Binary Complementary Offset Binary Complementary Toffset Binary Complementary Offset Binary Complementary Complement Information of Binary Complement Information Complementary Complementary Complementary Complementary Complement Information and Ingle Off whether Complementary Complementary Complementary Isolation of Binary Complementary Isolati Complementary I		VOUT ("1") ≥ +2	.4V			
coding, bipolar Complementary Offset Binary Complementary Two's Complement NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding and 32% for gain. The trimming pots should be located as close apossible to the converter and of Conversion (Status) Cinck Output Short conversion adjurtment binary Coding The conversion adjurtment binary Coding Cinck Output Train of positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "O" when conversion complete. Train of positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "O" when conversion adjurtment positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "O" when conversion adjurtment positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "O" when conversion adjurtment positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "O" when conversion adjurtment positive going +SV 100nsec. pulses. 600 kHz for ADC-HX12B max. 11/2 LSB max. 12.1% of FSR ³ to 1% of FSR ³ to 1% of FSR ³ to 10 max. 10 pum/"C of FSR max. ³ to 10 pm/"C of FSR max. ³ to 10 power. The case to ambient thermal resistance to for werter (sing an op am p connected for gain o theread with result. Net REQUIREMENT 20 pare. to 0.1% to werter. 0.0 pare. to 0.1% to 20 pare. Thermal for ablue thermal resistance to power. The case to ambient thermal resistance to 10000. The converters thermal resistance to power. The case to ambient thermal resistance to power. The case to ambient thermal resistance	oding, unipolar			justment range is ±0.2% of FSR for zero or offse		
Complementary Two's Complementary Complementary Two's Complementary			and the second se	and ±0.3% for gain. The trimming pots should b		
iarial Output Data NR2 successive decision pulses out, MSB first. Compl. Offset Binary Coding bit structures decision, external adjustmen may not be necessary. ind of Conversion (Status) Sint Conversion adjustmen may not be necessary. bit structures decision pulses out, MSB first. Compl. Offset Binary Coding ind of Conversion (Status) Train of positive going #5V 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "0" when conversion complete. Train of positive going #5V 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "0" when conversion complete. Train of positive going #5V 100nsec. pulses. 600 kHz for ADC-HX12B and logi: "0" when conversion adjust (pin 17) to +5V (10 bits) or +15V (10 bits). The clock the adjust (pin 17) to +5V (10 bits) or +15V (10 bits). The clock the adjust (pin 17) to +5V (10 bits) or +15V (10 bits). The clock rate should not be arbitrarity speeded up by commerting the clock rate ad given resolution, however, or missi codes will result. resolution 12 bits (1 part in 4096) e1/2 LSB max. ±0.1% of FSR ³ ±0.1% of FSR ³ ±0.0% of FSR ⁴ ±0.0% of FSR ⁴ ±0	seeing, pipoint and a second sec					
ind of Conversion (Status) first. Compl. Binary or Compl. Offset Binary Coding may not be necessary. conversion (Status) first. Compl. Binary or Compl. Offset Binary Coding Short cycled operation results in shorter conversion cables. Gol Net for ADC-HZ128 (pin 17 grounded). clock Output Train of positive going 45V 100nec. grounded). Train of positive going 45V 100nec. Train of positive going 45V 100nec. RFORMANCE Train of positive going 45V 100nec. grounded). The toe curve to for short-cycled conversion of 8 or 10 bits. In these toe cases the foc rate adjust (in 71) to +5V (10 bits) or +15V. RFORMANCE 12 bits (1 part in 4096) ti /2 LSB max. tifferential Nonlinearity ti /2 LSB max. ti /2 LSB max. tifferential Nonlinearity ti /2 LSB max. ti /2 LSB max. tifferential Nonlinearity ti /2 LSB max. ti /2 LSB max. tifferential Nonlinearity to 1% of FSR ³ to may and for bits of the tor rate adjust (in 71) to +5V (10 bits) or +15V. reader to complementary complementary componentary complementary complementary complementary componentary complementary complementa	Parial Quetaut Data					
Binary Coding Binary Coding Binary Coding Binary Coding Binary Coding Conversion status signal. Output is logic "I' during rest and conversion complete. Train of positive going +100 Mice. Dick Output Train of positive going +100 Mice. Dick Output Train of positive going +100 Mice. Dick Output Train of positive going +100 Mice. Publics. Conversion Complete. Train of positive going +100 Mice. publics. Train of positive going +100 Mice. Publics. The set work cases the clock rate should not be arbitrari file is conversion and togic *17 when conversion and togic *17 when conversion complete. RFORMANCE 12 bits (1 part in 4096) ti// L SB max. 11/2 LSB max. tion Time set adjust (pin 17) to +5V (10 bits) or +5V (10 bits) or +5V (10 bits). Note that output stime complementary complementary 25 complement is required, this can be provented is then calibrated to the stime calibrate or binary or 27 stomplement is required, this can be provented is then calibrated or the converter is then calibrated or the complementary 25 complement is required, this can be adjust (pin 17) to +5V (10 bits). Mifer Error, bipolar 10,01% of FSR max. ³ tioppm/ C of FSR max. ³ 10,02% / % Supply max. Over oper temp. range 00 to 70° c, -25 to +85° c, or -95° co +100° C on or 50° co 100° C						
End of Conversion (Status) Durk Young Conversion status signal. Output is logic "" during reset and conversion and logic "O" when conversion complete. Train of positive going ±5V 100nsec. pulses. 600 kHz for ADC-HX128 and 1.5MHz for ADC-HX128 (pin 17 grounded). CRFORMANCE Tzbits This to bit 9 output. Maximum conversion and 1.5MHz for ADC-HX128 (pin 17 grounded). Informativy 12/Dits (1 part in 4096) 12/Dits (1 part in 4096) 12/Dits (1 part in 4096) 12/Dits (1 part in 4096) 12/Dits (1 part in 4096) 12/Dits (1 part in 4096) 10/Dits (1 Dits) or +15V (1 Dits) or +15	Contract to the second s		ry or Compl. Offset			
conversion Status Conversion status Conversion status Conversion status Clock Output ''' d'uning rest and conversion complete. Train of positive going 45V 100nsec. pulses. 600 kHz for ADC-HX128 and 1.5MHz for ADC-HZ12B (pin 17 grounded). '''' d'uning rest and conversion and 15M For ADC-HX128 and 1.5MHz for ADC-HZ12B (pin 17 grounded). '''' d'uning rest and conversion and 15M For ADC-HX128 and 1.5MHz for ADC-HZ12B (pin 17 grounded). '''' d'uning rest and conversion and 15M For ADC-HX128 and 1.5MHz for ADC-HZ12B (pin 17 grounded). '''' d'uning rest and conversion and 15M For ADC-HX128 and 1.5MHz for add). 12 bits (1 part in 4096) 12 bits (1 part in 4096) 11/2 LSB max. 11/2 LSB max. 10.1% of FSR ³ Topport C of FSR max. ³ 20ppm /'C of FSR max. ³ 20ppm /'C of FSR nax. ³ 20ppm /'C of FSR nax. ³ 10 bits' 10 jusec. max. 10 jusec. max. 8.0 jusec. max. 10 jusec. max. 8.0 jusec. max. 10 jusec. max. 10 jusec. not 0% 12 bits' 10 jusec. not 0% 10 juse		Binary Coding				
"1" during reset and conversion and logic "0" when conversion complexe. pulses. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HX12B (pin 17 grounded). pin 14 to the output bit following the last bit desired. Cert X2B and 1.5MHz for ADC-HX12B (pin 17 grounded). IRFORMANCE 12 bits (1 part in 4096) as of 8 or 10 bits. In these two cases the cloce trace is able to the analysim conversion are is a bits. In the two cases the cloce or the submit of up to 400 certain the submit of the submit of up to the certain the submit of the submit of up to the certain the submit of the submit of up to the certain the submit of the submit of up to exceed the maximum conversion are is a law present of the submit of the submit of up to exceed the maximum conversion are is a law present of the submit of the submit of up to the certain the submit of the submit of up to exceed the maximum conversion are is a law present of the submit of up to the corver the submit of up to exceed the maximum conversion are is a law present of the submit of the corver the submit of up to exceed the maximum conversion are is a law present of the submit of up to the submit of up to the corver the submit of the corver the submit of up to the corver the submit of the co	End of Conversion (Status)	Conversion status	signal. Output is logic			
Clock Output Iogic "0" when conversion complete. Train of positive going 15V 100sec. pulsas. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HX12B and 1.5MHz for ADC-HZ12B (pin 17 grounded). 14 is connected to bit of output. Second times are given for short-cycled conversion prisms of so 10 bits. In these two cases the cloc rate adjust (pin 17) to 5V (10 bits) or 15V (10 press the clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The clock rate should not be arbitrarii press to 10 bits. The press te 10 bits. The press to 10 bits		"1" during reset a	nd conversion and			
Clock Output Train of positive going +5V 100nsec. pulses. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HX12B and 1.5MHz for ADC-HX12B (pin 17 grounded). 14 is connected to bit 9 output. Maximum con version for short-cycled conver- sions of 8 or 10 bits. In these two cases the cloc rate a jast speeded up to exceed the maximum conversion to 12 bits (1 part in 4096) ±1/2 LSB max. Sain Error, before adjustment 12 bits (1 part in 4096) ±1/2 LSB max. 5. Note that output coding is complementary coding of offset given resolution, however, or missin codes will result. Sain Error, before adjustment ±0.1% ±0.0% of FSR ³ ±0.1% of FSR ³ ±0.1% of FSR ³ ±0.1% of FSR ³ ±0.0% of FSR ³ ±0.0% of FSR ³ ±0.0% of FSR ³ ±0.0m/°C of FSR max. ³ ±10pm/°C of FSR max. ³ ±10pm/°C of FSR max. ³ ±10pm/°C of FSR ³ ±0.0µsec.max. 5. 0µsec.max. ±0.0µsec.max. ±0.0µsec.max. Su juster.max. B bits ⁴ 20 µsec.max. ±0.0µsec.max. ±0.						
Pulses. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HZ12B (pin 17 grounded). Version times are given for short-cycled conver- sion times are given for short-cycled conver- rate is also speeded up by connecting the cloc rate is also speeded up to exceed the maximum conversion rate at a given resolution. However, or missin speeded up to exceed the maximum conversion rate at a given resolution, however, or missin speeded up to exceed the maximum conversion rate at a given resolution, however, or missin speeded up to exceed the maximum conversion rate at a given resolution, however, or missin speeded up to exceed the maximum conversion rate at a given resolution, however, or missin speeded up to exceed the maximum conversion rate at a given resolution it is complementary speeded up to exceed the maximum conversion rate at a given resolution, however, or missin plementary offets binary or complementary 25 com mentary offets binary or complementary 25 com plements is required, this can b achieved by inverting the analog input to the conter to forwer. The case to ambient thermal resistance is abproximately 25° cpr wark. In Cost 1101 Tit 1111. Converter is the clock reserver dissipate approximately 2 wart of power. The case to ambient thermal resistance is abproximately 25° cpr wark. For ambien temperatures above 50° C, care should be taken not to creduation in the vicinity of the sover supply Rejection	Clock Output					
1.5MHz for ADC-H212B (pin 17 grounded). 15MHz for ADC-H212B (pin 17 grounded). abits 5 of 0 10 dis. In these two cases the column of the colu			0			
grounded). rate adjust [pin 17] to ±5V [10] bits] or ±15V [ERFORMANCE 12 bits (1 part in 4096) Resolution 12 bits (1 part in 4096) Stifferential Nonlinearity ±1/2 LSB max. 10 first, bioora adjustment ±0.1% Error, broora adjustment ±0.1% Error, broora adjustment ±0.1% Error, broora adjustment ±0.05% of FSR ³ ±0.05% of FSR ³ ±0.05% of FSR ³ ±0.07 C of Gain ±0.07m/° C of FSR ³ Diff. Nonlinearity Tempco ±20ppm/° C of FSR ³ Diff. Nonlinearity Tempco ±20ppm/° C of FSR ³ Diver oper. temp. range 0.0 upsec. max. Not bits ⁴ 10 justec. max. 10 justec. max. 8.0 justec. max. 10 justec. max. 8.0 justec. max. 10 justec. max. 10 justec. max. 10 to 70°C,25 to +85°C, or -55 t		the second se				
ERFORMANCE Resolution 12 bits (1 part in 4096) ±1/2 LSB max. Outlinearity ±1/2 LSB max. Sain Error, before adjustment ±0.1% Zero Error, unjolar, before adj. ±0.5% of FSR ³ Diffs ential Noninearity ±0.1% Error, before adjustment ±0.1% Store Error, unjolar, before adj. ±0.5% of FSR ³ Diffs te Iror, bipolar, before adj. ±0.1% of FSR ³ Store Thero, Coeff. of Gain ±20ppm/ ² C of FSR max. ³ ±20ppm/ ² C of FSR max. ³ ±10ppm/ ² C of FSR max. ³ ±10pim/ ² C of FSR max. ³ ±10ppm/ ² C of FSR max. ³ ±20ppm/ ² C of FSR max. ³ ±0.9 µsec. max. Bits ⁴ 10 µsec. max. Bits ⁴ 10 µsec. max. 10 µsec. max. 8.0 µsec. max. 10 µsec. max. 8.0 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec			HZ12B (pin 17			
ERFORMANCE 12 bits (1 part in 4096) Resolution 12 bits (1 part in 4096) Audinearity 11/2 LSB max. Shifter an proper bio sediustment 10.1% Store Fror, unipolar, before adj. ±0.5% of FSR ³ Bene, Coeff. of Gain ±0.0% of FSR max. ³ Termp, before adj. ±0.1% of FSR ³ Diffs endiustment ±0.0% of FSR ³ Diff. Nonlinearity Tempco ±0.0% of FSR ³ Diff. Nonlinearity Tempco ±0.0% of FSR ³ Diff. Nonlinearity Tempco ±0.0% of FSR ³ Suppm/°C of FSR ³ ±0.0000. The converter's then calibrated so tha Staff Secting Time, 10V step 0.0 usec. max. 10 bits ⁴ 10 usec. max. 10 usec. max. 8.0 usec. max. 10 usec. max. 4.0 usec. max. 10 usec. max. 0.0 usec. to 0.1% ower Supply Rejection 0.02% / % Supply max. OWER REQUIREMENT + 15VDC ±0.5V @ 55mA + 5VDC ±0.5V @ 55mA -17/4 X ±114 × 0.12 ko.20 inches (Glass) 1.74 X		grounded).				
Resolution 12 bits (1 part in 4096) Joninearity 11/2 LSB max. ain Error, before adjustment 10/1% zero Error, bipolar, before adj. ±0.5% of FSR ³ joninearity ±0.5% of FSR ³ continearity ±0.5% of FSR ³ continearity ±0.5% of FSR ³ joninearity ±0.5% of FSR ³ continearity ±0.1% of FSR ³ continearity ±0.1% of FSR ³ continearity ±0.1% of FSR ³ context ±0.0% of FSR ³ context ±0.0% of FSR max. ³ ±10 bits ⁴ ±0.0% context 10 bits ⁴ ±0.0% context 10 bits ⁴ ±0.0% sec. max. 10	DEC DU ANOE					
Nambulation 12 JC SB max. 12 JC LSB max. 11/2 LSB max. 2 Join Error, before adjustment 1.01% 2 an Error, before adjustment 1.01% 2 may. 1.0000 2 may. 1.00000 2 may. 1.00000 2 may. 1.00000 2 may. 1.000000000000000000000000000000000000		1011 11	10001			
Montinearity 11/2 LSB max. ain Error, before adjustment 11/2 LSB max. binstror, before adjustment 10.1% fere Error, unipolar, before adj. 10.1% fere Error, unipolar, before adj. 10.1% ferembore, Coeff, of Gran 20psm/°C of FSR max. ³ remp. Coeff, of Offset, bipolar 10ppm/°C of FSR max. ³ 20psm/°C of FSR max. ³ 10ppm/°C of FSR max. ³ 20psm/°C of FSR max. ³ 10ppm/°C of FSR max. ³ 20psm/°C of FSR max. ³ 10ppm/°C of FSR max. ³ 20psc cdes 0 to Missing Codes 10 bits ⁴ 15 µsec. max. 6.0 µsec. max. 10 µsec. max. 6.0 µsec. max. 10 µsec. max. 6.0 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 0.0 µsec. max. 10 µsec.max. 0.0 µsec.max. <		execution of the second second second	4096)	codes will result. 5. Note that output coding is complementary co		
11/2 LSB max. ±1/2 LSB max. 2ain Error, before adjustment ±0.1% 2aro Error, bipolar, before adjustment ±0.5% of FSR ³ 0.1% of FSR ³ ±0.1% of FSR ³ 10 may. Coeff. of Gain ±20ppm/°C of FSR max. ³ ±10 kmst. ±5ppm/°C of FSR max. ³ ±10 kmst. ±10 pm/°C of FSR ³ Over oper. temp. range 0 ver oper. temp. range 10 birst 10 psec. max. 8 bitst 10 psec. max. 10 birst 10 psec. max. 10 birst 10 psec. max. 10 psec. max. 8.0 µsec. max. 10 birst 10 µsec. max. 10 psec. max. 10 µsec. max. 10 psec. max. 10 µsec. max. 10 µsec. max.						
Zero Error, unipolar, before adj. ±.05% of FSR ³ Offset Error, bipolar, before adj. ±.05% of FSR ³ Offset Error, bipolar, before adj. ±.05% of FSR ³ Diffset, for Gain ±.00pm/°C of FSR max. ³ *10pm/°C of FSR ³ ±.00pm/°C of FSR ³ Ownersion Time ³ , 12 bits 20 sec. max. 10 bits ⁴ 10 bits ⁴ Suffer Settling Time, 10V step 3.0 µsec. max. 8 bits ⁴ 10 µsec. max. 10 µsec. max. 3.0 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. max. 3.0 µsec. max. 10 µsec. max. 10 µsec. max.	Differential Nonlinearity					
Diffset Error, bipolar, before adj. ±0.1% of FSR ³ Femp. Coeff. of Gain ±20ppm/°C or FSR max. ³ 10ppm/°C of FSR max. ³ ±2ppm/°C of FSR max. ³ ±20pm/°C of FSR max. ³ ±2ppm/°C of FSR max. ³ ±20pm/°C of FSR max. ³ ±2ppm/°C of FSR max. ³ bits ⁴ 10 bits ⁴ 50 µsec. max. Buffer Settling Time, 10V step 3.0 µsec. to .01% 6.0 µsec. max. ower supply Rejection .002% /% Supply max. ORDERING INFORMATION TEMP. + 5VDC ±0.5V @ 55m A -15VDC ±0.5V @ 55m A -15VDC ±0.5V @ 55m A -15VDC ±0.5V @ 55m A -100°C or askage Size 1.74 × 1.14 × 0.2 inches (Glass) <t< td=""><td>Gain Error, before adjustment</td><td></td><td></td><td></td></t<>	Gain Error, before adjustment					
Dist Prof., biplice adj	Zero Error, unipolar, before adj	±.05% of FSR ³				
remp. Coeff. of Gain ±20ppm/° C max. femp. Coeff. of Zero, unipolar ±20ppm/° C of FSR max. ³ isppm/° C of FSR max. ³ ±2ppm/° C of FSR max. ³ conversion Time*, 12 bits ±2ppm/° C of FSR max. ³ 10 bits ⁴ ±2ppm/° C of FSR max. ³ 20 visc. max. 8.0 µsec. max. 10 bits ⁴ 50 µsec. max. 10 bits ⁴ 50 µsec. max. 10 bits ⁴ 50 µsec. max. 10 µsec. max. 6.0 µsec. max. 10 µsec. max. 6.0 µsec. max. 10 µsec. max. 10 µsec. max. 10 µsec. 0.0 µsec. to .01% .002% / % Supply max. 000% O000 Dower Supply Rejection 0 to 70° C, -25 to +85° C, or -55° c to +100° C .15 VDC ±0.5V @ 55mA -15V C ±0.25 @ 100mA HYSICAL-ENVIRONMENTAL 0 to 70° C, -25 to +85° C, or -55° c to +100° C .170 x 1.10 x 0.2 µches (Glass) 1.74 x 1.	Offset Error, bipolar, before adj.	±0.1% of FSR ³				
femp. Coeff. of Zero, unipolar ±5ppm/°C of FSR max.³ femp. Coeff. of Offset, bipolar ±5ppm/°C of FSR max.³ femp. Coeff. of Offset, bipolar ±10ppm/°C of FSR max.³ t0 Missing Codes 20 µsec. max. 10 bits* 10 µsec. max. 10 µsec. max. 6.0 µsec. max. 10 µsec. max. 4.0 µsec. max. 10 µsec. max. 3.0 µsec. to .01% .002% / % Supply max. 0000 00000 DWER REQUIREMENT +15VDC ±0.5V @ 55mA +15VDC ±0.5V @ 45mA +5VDC ±0.25 @ 100mA VYSICAL-ENVIRONMENTAL 0 to 70° C, -25 to +85° C, or -55° c to +100° C 170 x 1.10 x 0.2 inches (Glass) 1.70 x 1.10 x 0.2 inches (Glass) 1.70 x 1.10 x 0.2 inches (Glass) 1.74 x 1.14 x 0.2 inches (Glass) 1.70 x 2.10 x 0.2 inches (glass), 0.53 oz. (metal) Acting Socket: DILS-2 (2/converter) at \$5.00 /pair Trimming Potentiometers: TP2K. TP5K, TP10h Took is for 0 to +10V or ±5V input and 20V for ±10V input.	the second s	±20ppm/°C max.				
Temp. Coeff. of Offset, bipolar ± 10ppm/°C of FSR max. ³ > Diff. Nonlinearity Tempco. ± 10ppm/°C of FSR max. ³ > 20 µsec. max. S.0 µsec. max. 10 bits ⁴ 20 µsec. max. 10 bits ⁴ 20 µsec. max. 10 bits ⁴ 20 µsec. max. 10 bits ⁴ 3.0 µsec. to. 01% 20 µsec. max. 4.0 µsec. max. 10 µsec. max. 4.0 µsec. max. 10 µsec. max. 4.0 µsec. max. 10 µsec. max. 10.0 µsec. max. 10 µ			max ³			
Diff. Nonlinearity Tempco						
Dr. Notlinearity remped: 1111 Do Missing Codes 0.0 yeoper, temp, range Conversion Time ² , 12 bits 20 µsec, max. 10 bits ⁴ 10 µsec, max. 10 µsec, max. 10 µsec, max.		STORE STORE STORE				
Work Sing Codes Over oper. temp. range 1111. Conversion Time ² , 12 bits 20 µsec. max. 8.0 µsec. max. 6.0 µsec. max. 10 bits ⁴ 15 µsec. max. 6.0 µsec. max. 6.0 µsec. max. 3uffer Settling Time, 10V step 3.0 µsec. to 0.1% 6.0 µsec. max. 10 µsec. max. 3.0 µsec. to 0.1% 0.002% / % Supply max. 0.002% / % Supply max. 0.002% / % Supply max. DWER REQUIREMENT + 15VDC ± 0.5V @ 55mA - 15VDC ± 0.5V @ 55mA - 15VDC ± 0.25 @ 100mA IVSICAL-ENVIRONMENTAL 0 to 70°C, -25 to +85°C, or -55°C to +100°C -55°C to +100°C -55°C to +100°C ackage Size 0.1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) ADC-HX12BMR -25 to +85C METAL \$125.00 ins 0.42 oz. (glass), 0.53 oz. (metal) Hermetically sealed glass or metal Kovar Mating Socket: DILS-2 (2/converter) at \$5.00 / pair OTES: All digital outputs can drive 2 TTL loads. . Mating Socket: DILS-2 (2/converter) at \$3.00 each Without buffer amplifier used. . FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. Timming Potentiometers: TP2K, TP5K, TP10A						
10 bits ⁴ 15 μsec. max. 6.0 μsec. max. 4.0 μsec. max. 30 μsec. max. 10 μsec. max. 4.0 μsec. max. 0 μsec. max. 30 μsec. max. 3.0 μsec. max. 4.0 μsec. max. 0 μsec. max. 30 μsec. max. 3.0 μsec. max. 4.0 μsec. max. 10 μsec. max. 30 μsec. max. 3.0 μsec. max. 4.0 μsec. max. 10 μsec. max. 30 μsec. max. 3.0 μsec. max. 4.0 μsec. max. 10 μsec. max. 30 μsec. max. 3.0 μsec. max. 4.0 μsec. max. 10 μsec. max. 30 μsec. max. 3.0 μsec. max. 10 μsec. max. 10 μsec. max. 30 μsec. max. 3.0 μsec. max. 10 μsec. max. 10 μsec. max. 30 μsec. max. 15 μsec. max. 15 μsec. max. 10 μsec. max. 30 μsec. max. 15 μsec. max. 15 μsec. max. 10 μsec. max. 30 μsec. to .01% wsupply max. 002% / % supply max. 002% / % supply max. 0WER REQUIREMENT + 15 VDC ± 0.5 V @ 55mA TEMP. NODEL RANGE CASE PRICE(1- VISICAL-ENVIRONMENTAL 0 to 70° C, -25 to +85° C, or -55° to +100° C ADC-HX12BGC 0 to 70° C GLASS \$19.00			range			
10 bits ⁴ 15 μsec. max. 6.0 μsec. max. of power. The case to ambient thermal resistance is approximately 25° C per watt. For ambient thermal resistance is approximately 25° C p	Conversion Time ² , 12 bits	20 µsec. max.	8.0 µsec. max.	6. These converters dissipate approximately 2 watt		
8 bits ⁴ 10 μsec. max. 4.0 μsec. max. Buffer Settling Time, 10V step 3.0 μsec. to .01% is approximately 25°C per watt. For ambien temperatures above 50°C, care should be taken to to restrict air circulation in the vicinity of the converter. DWER REQUIREMENT + 15VDC ±0.5V @ 55mA - 15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA -15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA -15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA -15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA -15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA - 15VDC ±0.5V @ 45mA -15VDC ±0.5V @ 45mA - 55°C to +100°C - 55°C to +100°C torage Temperature Range - 55°C to +100°C - 55°C to +100°C ackage Size - 1.70 × 1.10 × 0.2 inches (Glass) - 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal kovar - 0.42 oz. (glass), 0.53 oz. (metal) - 55°C to +100C METAL \$195.00 Veight - 0.42 oz. (glass), 0.53 oz. (metal) - 51LS-2 (2/converter) at \$5.00 /pair Nating Socket: DILS-2 (2/converter) at \$5.00 /pair Trimming Potentiometers: TP2K. TP5K, TP10A TP20K, TP50K or TP100K at \$3.00 each These converteres Are covereed U	10 bits ⁴	15 μsec. max.	6.0 µsec. max.	of power. The case to ambient thermal resistance		
Buffer Settling Time, 10V step 3.0 µsec. to .01% temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter. DWER REQUIREMENT +15VDC ±0.5V @ 55mA not to restrict air circulation in the vicinity of the converter. DWER REQUIREMENT +15VDC ±0.5V @ 55mA TEMP. HYSICAL-ENVIRONMENTAL 0 to 70°C, -25 to +85°C, or -55 to +100°C MODEL RANGE CASE PRICE(1) Apperating Temperature Range 0 to 70°C, -25 to +85°C, or -55°C to +100°C -55°C to +100°C ADC-HX12BMR -25 to +85C METAL \$15.00 ackage Size .1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal Kovar ADC-HZ12BMR -25 to +85C METAL \$169.00 OTES: . All digital outputs can drive 2 TTL loads.	8 bits ⁴	10 µsec. max.	4.0 µsec. max.	is approximately 25°C per watt. For ambien		
Dower Supply Rejection .002% / % Supply max. Dower Supply Rejection Dower Supply Rejection DWER REQUIREMENT + 15VDC ±0.5V @ 55mA -15VDC ±0.5V @ 45mA + 5VDC ±0.25 @ 100mA ORDERING INFORMATION IVSICAL-ENVIRONMENTAL operating Temperature Range 0 to 70°C, -25 to +85°C, or -55°C to +100°C MODEL RANGE CASE PRICE(1- ADC-HX12BGC 0 to 70°C, GLASS \$ 85.00 ADC-HX12BMR -25 to +85°C, oto -55°C to +100°C ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.70 × 1.10 × 0.2 inches (Metal) ADC-HZ12BGC 0 to 70°C GLASS \$ 119.00 ADC-HZ12BMR -25 to +85°C METAL \$ 155.00 ADC-HZ12BMR -55 to +100°C ADC-HZ12BMR -55 to +100°C ADC-HZ12BMR <td< td=""><td></td><td>3.0 µsec. to .01%</td><td></td><td></td></td<>		3.0 µsec. to .01%				
OWER REQUIREMENT + 15VDC ±0.5V @ 55mA ORDERING INFORMATION -15VDC ±0.5V @ 45mA -15VDC ±0.25 @ 100mA TEMP. YSICAL-ENVIRONMENTAL 0 to 70°C, -25 to +85°C, or -55 to +100°C ADC-HX12BGC 0 to 70°C, GLASS \$ 85.00 torage Temperature Range -55°C to +100°C -55°C to +100°C ADC-HX12BGC 0 to 70°C, GLASS \$ 119.00 ackage Size -1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) ADC-HZ12BGM -55 to +100°C ADC-HZ12BGM 55 to +100°C METAL \$ 169.00 ackage Type 0.42 oz. (glass), 0.53 oz. (metal) Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) Mating Socket: DILS-2 (2/converter) at \$5.00 /pair Trimming Potentiometers: TP2K, TP5K, TP10H TP2K, TP5K or TP100K at \$3.00 each These converters ARE coverter UNDE			max.			
+ 15VDC ±0.5V @ 55mA -15VDC ±0.5V @ 45mA + 5VDC ±0.25 @ 100mA YSICAL-ENVIRONMENTAL perating Temperature Range 0 to 70° C, -25 to +85° C, or -55° C to +100° C torage Temperature Range -55° C to +100° C ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.						
-15VDC ±0.5V @ 45mA TEMP. YSICAL-ENVIRONMENTAL 0 to 70° C, -25 to +85° C, or -55 to +100° C ADC-HX12BGC 0 to 70C GLASS \$ 85.00 torage Temperature Range -55°C to +100° C ADC-HX12BMR -25 to +85C METAL \$125.00 ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) ADC-HZ12BMR -25 to +85C METAL \$159.00 ackage Type 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) Mating Socket: DILS-2 (2/converter) at \$5.00 /pair OTES: All digital outputs can drive 2 TTL loads. Trimming Potentiometers: TP2K. TP5K, TP10P TP20K, TP50K or TP100K at \$3.00 each THESE CONVERTERS ARE COVERED UNDER		+15VDC+0.5V@	55mA	ORDERING INFORMATION		
+ 5VDC ± 0.25 @ 100mA MODEL RANGE CASE PRICE(1: VSICAL-ENVIRONMENTAL 0 to 70° C, -25 to +85° C, or -55 to +100° C ADC-HX12BGC 0 to 70° C GLASS \$ 85.00 torage Temperature Range -55°C to +100° C -55°C to +100° C ADC-HX12BMR -25 to +85C METAL \$125.00 ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.70 × 1.10 × 0.2 inches (Metal) ADC-HZ12BMR -25 to +85C METAL \$169.00 hermetically sealed glass or metal ins Kovar 0.42 oz. (glass), 0.53 oz. (metal) Mating Socket: DILS-2 (2/converter) at \$5.00 / pair Trimming Potentiometers: TP2K, TP5K, TP10H TP20K, TP50K or TP100K at \$3.00 each OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDER						
VYSICAL-ENVIRONMENTAL 0 to 70°C, -25 to +85°C, or -55 to +100°C ADC-HX12BGC 0 to 70°C GLASS \$ 85.00 torage Temperature Range -55°C to +100°C -55°C to +100°C ADC-HX12BMR -25 to +85C METAL \$155.00 ackage Size						
perating Temperature Range 0 to 70°C, -25 to +85°C, or -55 to +100°C ADC-HX12BMR -25 to +85C METAL \$125.00 torage Temperature Range -55°C to +100°C -55°C to +100°C ADC-HX12BMR -25 to +85C METAL \$125.00 ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) ADC-HZ12BMR -25 to +85C METAL \$169.00 ackage Type Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) Mating Socket: DILS-2 (2/converter) at \$5.00 /pair OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDER		+ 5VDC ±0.25@	TOUMA	MODEL RANGE CASE PRICE(1		
perating Temperature Range 0 to 70°C, -25 to +85°C, or -55 to +100°C ADC-HX12BMR -25 to +85C METAL \$125.00 ADC-HX12BMM -55 to +100C METAL \$155.00 ADC-HX12BMM -55 to +100C METAL \$155.00 ADC-HX12BMM -55 to +100C METAL \$156.00 ADC-HX12BMM -55 to +100C METAL \$169.00 ADC-HZ12BGC 0 to 70C GLASS \$119.00 ADC-HZ12BMM -55 to +100C METAL \$169.00 ADC-HZ12BMM -55 to +100C METAL \$169.00 ADC-HZ12BMM -55 to +100C METAL \$195.00 METAL \$195.00 METAL \$195.00 ADC-HZ12BMM -55 to +100C METAL \$100.00 ADC-HZ12BMM -55 to +1	YSICAL-ENVIRONMENTAL			ADC-HX12BGC 0 to 70C GLASS \$ 85.00		
or -55 to +100° C -55° C to +100° C 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.	perating Temperature Range	0 to 70°C, -25 to	o +85°C,			
torage Temperature Range -55°C to ±100°C ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) Hermetically sealed glass or metal Kovar 0.42 oz. (glass), 0.53 oz. (metal) DTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to ±10V or ±5V input and 20V for ±10V input.						
ackage Size 1.70 × 1.10 × 0.2 inches (Glass) 1.70 × 1.10 × 0.2 inches (Glass) 1.74 × 1.14 × 0.2 inches (Metal) ackage Type Hermetically sealed glass or metal ins Kovar leight 0.42 oz. (glass), 0.53 oz. (metal) OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.	torage Temperature Range		and the second second			
1.74 × 1.14 × 0.2 inches (Metal) ackage Type ins leight 0.42 oz. (glass), 0.53 oz. (metal) OTES: All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.	-		inches (Glass)			
ackage Type Hermetically sealed glass or metal Kovar Mating Socket: DLLS-2 (2/converter) at \$5.00 /pair OTES: All digital outputs can drive 2 TTL loads. Trimming Potentiometers: TP2K, TP5K, TP10k TP20K, TP50K or TP100K at \$3.00 each Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDER	ackaye 3128					
ins Kovar Mating Socket: DILS-2 (2/converter) at \$5.00 /pair OTES: All digital outputs can drive 2 TTL loads. Trimming Potentiometers: TP2K. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDE				ADC-HZ12BMM -55 to +100C METAL \$195.00		
Veight			ed glass or metal			
OTES: All digital outputs can drive 2 TTL loads. Trimming Potentiometers: TP2K, TP5K, TP10K TP20K, TP50K or TP100K at \$3.00 each Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDER						
OTES: Trimming Potentiometers: TP2K, TP5K, TP10H All digital outputs can drive 2 TTL loads. Trimming Potentiometers: TP2K, TP5K, TP10H Without buffer amplifier used. TP20K, TP50K or TP100K at \$3.00 each FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDER		0 12 07 (alace) 0	.53 oz. (metal)			
All digital outputs can drive 2 TTL loads. Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. Trimming Potentiometers: TP2K, TP5K, TP10K TP20K, TP50K or TP100K at \$3.00 each THESE CONVERTERS ARE COVERED UNDER	ins	0.42 02. (glass), 0.		ar \$5.00 / pair		
Without buffer amplifier used. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input. THESE CONVERTERS ARE COVERED UNDE	ins	0.42 02. (glass), 0.				
. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.	Veight	0.42 02. (glass), 0.				
I HESE CONVERTERS ARE COVERED UNDE	Veight	0.42 02. (grass), 0.				
	Veight					

TIMING AND CONNECTION DIAGRAMS

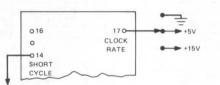


CONNECTIONS AND CALIBRATION

INPUT CONNECTIONS

INPUT	WI	THOUT B	UFFER	WITH BUFFER			
VOLT.	INPUT	CONNEC	T THESE	INPUT	CC	NNECT TH	ESE
RANGE	PIN	PINS TO	GETHER	PIN	PI	NS TOGET	HER
0 TO +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 TO +10V	24		23 & 26	30	-	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24		23 & 22	30	-	23 & 22	29 & 24
±10V	25	-	23 & 22	30	-	23 & 22	29 & 25

SHORT CYCLE OPERATION



TO SELECTED

DATEL

CLOCK RATE VS. VOLTAGE

PIN 17	CLOCK RATE			
VOLTAGE	ADC-HX12B	ADC-HZ12B		
0V	600 kHz	1.5MHz		
+5V	720 kHz	1.8MHz		
+15V	880 kHz	2.2MHz		

8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE	17 & 15	17 & 16	17 & 28
PINS TOGETHER	14 & 16	14 & 2	14 & 4

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

CALIBRATION PROCEDURE

 Connect converter as shown in the Standard Connection diagrams. Use the Input Connection Table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nsec. minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.

2. Zero and Offset Adjustments

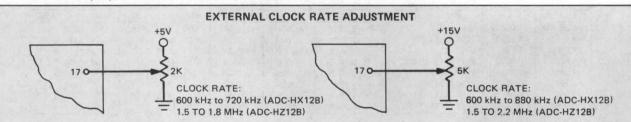
Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero $+\frac{1}{2}$ LSB) or the bipolar offset adjustment (-FS+ $\frac{1}{2}$ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.

3. Full Scale Adjustment

Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS-1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
O TO LEV	ZERO	+0.6 mV
0 TO +5V	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
010+100	GAIN	+9.9963V
BIPOLAR RANGE		
10.514	OFFSET	-2.4994V
±2.5V	GAIN	+2.4982V
151	OFFSET	-4.9988V
±5V	GAIN	+4.9963V
±10V	OFFSET	-9.9976V
TUV	GAIN	+9.9927V





FAST, 8 BIT ANALOG TO DIGITAL CONVERTER

MODEL ADC-EH8B

FEATURES

8 Bit Resolution

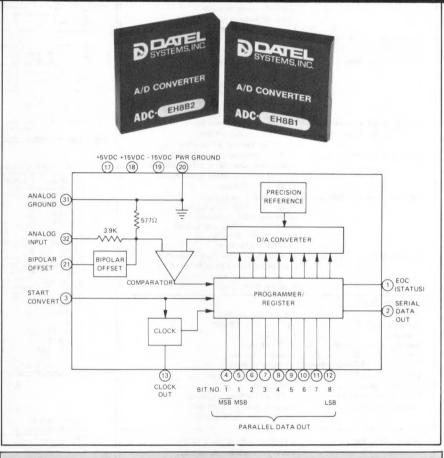
- ▶ 4.0 & 2.0 µsec. Conversion Time
- Unipolar or Bipolar Operation
- Parallel & Serial Outputs
- Low Cost

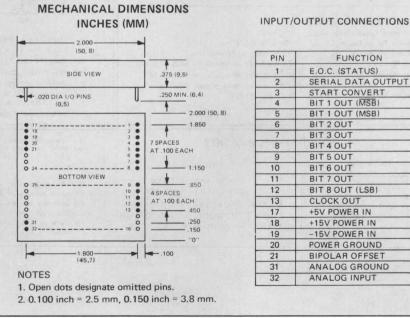
GENERAL DESCRIPTION

The model ADC-EH8B is a fast, 8 bit successive approximation type analog to digital converter in a compact 2 x 2 x .375 inch module. These converters are low cost devices with application in pulse code modulation systems and instrumentation and control systems requiring fast data conversion rates up to 400,000 per second. There are two models to choose from based on conversion speed: ADC-EH8B1 with a conversion time of 4.0 µsec. (250 kHz rate), and ADC-EH8B2 with a conversion time of 2.0 µsec. (416 kHz rate). The high speed in a small size is made possible by the use of an MSI integrated circuit which provides all the necessary successive approximation logic, along with other new integrated circuit components. The analog input range is either unipolar 0 to +10V or bipolar -5V to +5V, determined by external pin connection. For unipolar operation no external adjustments are necessary; for bipolar operation only a bipolar offset adjustment must be made externally. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight or offset binary coding. Other outputs are clock output for synchronization with serial data, and MSB output for two's complement coding.

Other specifications include full scale temperature coefficient of 50 ppm/°C max., long term stability of .05%/year, and linearity of $\pm 1/2$ LSB. Power requirement is ± 15 VDC and ± 5 VDC.

The ADC-EH8B1 & 2 are improved versions of Datel's former models ADC-EH1 & 2, and are identical in all specifications and pin positions except for a small change in input impedance and three added output pins for Clock Out, MSB Out, and Serial Data Out.





SPECIFICATIONS, ADC-EH8B

(Typical at 25°C, ±15V & +5	V Supplies, unless otherwise indicated)) nsec. min.			1
INPUTS Analog Input Range Input Impedance Input Overvoltage Start Conversion	0V to +10V FS or ±5V FS 4.45K ohms ±50 ohms ±20V (no damage) 2V min. to 5.5V max. positive pulse with du- ration of 100 nsec. min. Rise and fall times <50 nsec.		MRC: 170-		-	0 PARALLE 1 PARALLE DATA HOW VALID 4-30 rest. typ. 1 0 0
	Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load	SERIAL DATA OUT25 m typ.		T 3 BIT 4 BIT 5	BIT 6 BIT	7 81T 8 (LSB) 0
OUTPUTS		BIT 1	50C.			BIT 1
Parallel Output Data	8 parallel lines of data held until next conversion command. V out ("0") $\leq +0.4$ V	(MSB) typ. 81T 2				0N 0FF
	V out $("1") \ge +2.4V$ Each output capable of driving up to 4 TTL loads.	BIT 8				
Coding, Unipolar Operation Bipolar Operation	Straight Binary, positive true Offset Binary, positive true.	(LS8) !	T ₁ T ₂ ADC-EH881 670 80 ADC-EH882 400 45	T ₃ T ₄ 440 3880 neec 200 2000 neec	. typ.	0FF 0
Serial Output Data	NRZ successive decision pulse output gener- ated during conversion, with MSB first.	UNIPOLAR		T CODING		
	Straight binary or offset binary coding.	SCALE	INPUT VOLTAGE	STRAIGHT B	INARY	
End of Conversion (EOC)	Loading: 4 TTL loads Conversion Status Signal. V out (''0'') $\leq +0.4$ V indicates conversion time completed. V out (''1') $\geq +2.4$ V during reset	+FS-1 LSB +7/8 FS +3/4 FS +1/2 FS	+9.96V +8.75V +7.50V +5.00V	1111 11 1110 000 1100 000 1000 000	00	
	and conversion periods. Loading: 4 TTL loads.	+1/4 FS +1 LSB	+2.50∨ +0.04∨	0100 000	01	
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on	0 BIPOLAR (-	0.00V -5V TO +5V)	0000 000	00	
	during conversion time. Loading: 6 TTL loads	SCALE	INPUT VOLTAGE	OFFSET BIN		PLEMENT
PERFORMANCE Resolution Accuracy at 25° C Linearity Differential Nonlinearity Temp. Coeff. of Gain Temp. Coeff. of Zero, Unipolar Temp. Coeff. of Offset, Bipolar		+FS-1 LSB +3/4 FS +1/2 FS 0 -1/2 FS -3/4 FS -FS+1 LSB -FS	+4.96V +3.75V +2.50V 0.00V -2.50V -3.75V -4.96V -5.00V	1111 1111 1110 0000 1100 0000 0100 0000 0010 0000 0000 0001 0000 0000	0110 0100 0000 1100 1010 1000	1111 0000 0000 0000 0000 0000 0000 000
Long Term Stability Power Supply Rejection Conversion Time	± 35 ppm of FS/ ^o C max. ± .05%/year ± .02% of FS/% supply, max. 4.0 μsec. max., ADC-EH8B1 2.0 μsec. max., ADC-EH8B2	CONNECTION FOF		CALIBRAT	ION	
POWER REQUIREMENT	± 15VDC ±0.5V @ 25mA max. +5VDC ± 0.25V @ 125mA max.	ONLY	0 18 0 19 0 20	BOTTOM VIEW	TRIMMING POT	ENTIOMETER
PHYSICAL-ENVIRONMENTAL Operating Temp. Range Storage Temp. Range Relative Humidity Case Size Case Material Pins Weight		 UNIPOLA pot is no than 1/2 I BIPOLAF 100Ω tri voltage sc or +0.02 	AR – No adjustment t used. Full scale a SB. Pin 21 is left op R – Connect pin 18 mming potentiomet burce to pin 32 and 0V. Adjust the tri bde flickers equally b	ts are necessary nd zero are int pen. 3 (+15VDC) to ter as shown. set the input of mming potenti	is 100 PPM/*C (15 TURN, ORDI TP190 AT \$3,000 and 100 G ernally set o pin 21 Connect a voltage to iometer so	SERMET TYPE ER DATEL MODEL FA. 2 trimming t to better through a a precision + 1/2 LSB that the
ADC-EH8B	NG INFORMATION PRICES (1-9) ADC-EH8B1 \$ 85.00	added to the r -EX -EXX-HS	temperature range nodel number. Cons -25° C to +85° C -55° C to +85° C semiconductor co H881 & 2 replace	ult factory for operation operation with omponents.	pricing. hermetica	illy sealed
CONVERSION TIME 1 = 4.0 μSEC. 2 = 2.4 μSEC.	ADC-EH8B2 \$129.00 MATING SOCKETS: DILS-2 (2/MODULE) \$5.00/PAIR TP100 TRIMMING POT. \$3.00 EA.	improved mod the previous r clock output, 5K ohms to 4.	lels of these units r models is the 3 add and MSB output, a 45K ohms. If the ne n existing application	respectively. Th ditional output and a change in ewly used pins (ne only di pins for input im nos. 2, 4,	fference from serial output, pedance from and 13) cause

TIMING DIAGRAM FOR ADC-EH8B -----1

Output: 10101010



10 BIT, 2.0 AND 4.0µSEC. ANALOG TO DIGITAL CONVERTERS

MODEL ADC-EH10B

FEATURES

- ▶ 2.0 µsec. Conversion \$189.
- ▶ 4.0 µsec. Conversion \$149.
- ► 10 Bit Resolution
- ▶ Compact 3" x 2" x .375" Module
- ▶ ±30ppm/°C max. Tempco

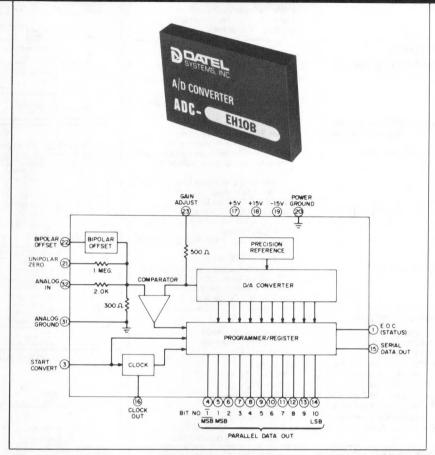
GENERAL DESCRIPTION

Model ADC-EH10B is a very fast 10 bit successive approximation type A/D converter in a compact low profile package. Low pricing makes this converter an ideal choice for many applications including fast scanning data acquisition systems, PCM systems, and fast pulse analysis. This converter is available in two versions based on conversion speed: ADC-EH10B1 with 4.0 μ sec. (250kHz rate) and ADC-EH10B2 with 2.0 μ sec. (500kHz rate).

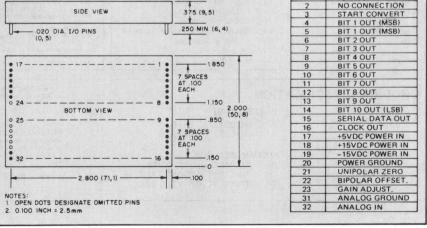
High speed and moderate power consumption (1.7 watts) in a compact size $(3'' \times 2'' \times .375'')$ are made possible by use of an MSI integrated circuit successive approximation programmer/register used with 10 fast switching current sources driving a low impedance R-2R ladder network. A fast precision comparator and precision voltage reference circuit are also used.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. The converter has a maximum full scale temperature coefficient of ±30ppm/°C and is monotonic over the full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronizing serial data, MSB output for two's complement coding, and end of conversion (status) signal. All outputs are DTL/ TTL compatible. Power requirement is ±15VDC and +5VDC. The ADC-EH10B is also available in extended temperature range versions.

The ADC-EH10B1 is an improved version of Datel's former ADC-EH10B converter. The ADC-EH10B1 is identical in all specifications and pin positions with the former model except for a change in input impedance and reduction in +5V supply current.

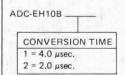


MECHANICAL DIMENSIONS INCHES (MM) PIN FUNCTION PIN FUNCTION PIN FUNCTION 2 NO CONNECTION



GOLD BOOK 76/77

				Contraction of the second	0
INPUTS	LAND IN THE REAL	EOC	80 need typ	and the second second	PARAL FI-1
Analog Input Range	OV to +10V FS or ±5V FS	E O C (STATUS)	+		PARALLEL DATA NOW VALID
nput Impedance		-		-	SO nsec
nput Overvoltage		CLOCK			יוֹחִ
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise				0 10 00 meec
	and fall times <500 nsec.	SERIAL	25 nsec typ		
	Logic "1" resets converter	DATA OUT	80 nsec BIT 1 typ (MSB) BIT 2 BIT	3 BIT 4 BIT 5 BIT 6 BIT 7	BIT 8 BIT 9 BIT 10 (LSB)
	Logic "O" initiates conversion				
	Loading: 1 TTL load	BIT 1 (MSB)	BO nsec typ		
DUTPUTS		BIT 2			
Parallel Output Data	10 parallel lines of data held until				0
	next conversion command.	817 3			1
	V out (''0'') ≤ +0.4V V out (''1'') ≥ +2.4V				
	Each output capable of driving up to	817 10 (L\$8)	τ, τ		
	4 TTL loads.		ADC-EHIOBI 115 36 ADC-EHIOB2 59 19	DO need typ } For Start Convert = 100	nsec 0
Coding, Unipolar operation			01170		
Bipolar operation				UT CODING	
Serial Output Data	Two's complement, positive true NRZ successive decision pulse output	UNIPOLAR	(0V TO +10V)		
	generated during conversion with	SCALE	INPUT VOLTAGE	STRAIGHT BINARY	
	MSB first.	+FS - 1 LSB	+9.9902V	1111 1111 11	
	Straight binary or offset binary,	+7/8 FS +3/4 FS	+8.7500∨ +7.5000∨	1110 0000 00	
	positive true coding. Loading: 4 TTL loads	+1/2 FS	+5.0000V	1000 0000 00	
End of Conversion (EOC)	Conversion Status Signal.	+1/4 FS + 1 LSB	+2.5000∨ +0.0098∨	0100 0000 00 000000 01	
	V out ("0") \leq +0.4V indicates con-	0	0.0000V	0000 0000 00	
	version completed.	BIPOLAR (-	5V TO +5V)		
	V out $(''1'') \ge +2.4V$ during reset and conversion.			OFFORT DUMARY	THOM COURT CHENT
	Loading: 4 TTL loads	SCALE +FS -1 LSB	+4.9902V	OFFSET BINARY	TWO'S COMPLEMENT
Clock Output	Internal clock pulse train of negative	+FS -1 LSB +3/4 FS	+4.9902V +3.7500V	1111 1111 11 1110 0000 00	0111 1111 11 0110 0000 00
	going pulses from +5V to 0V gated on	+1/2 FS	+2.5000V	1100 0000 00	0100 0000 00
	during conversion time. Loading: 6 TTL loads	0 -1/2 FS	0.0000∨ -2.5000∨	1000 0000 00 0100 0000 00	0000 0000 00
Second and a second		-3/4 FS	-3.7500V	0010 0000 00	1010 0000 00
PERFORMANCE		-FS + 1 LSB -FS	-4.9902∨ -5.0000∨	0000 0000 01	1000 0000 01 1000 0000 00
Resolution	10 Bits (1 part in 1024)				
Accuracy at 25°C		*Using MSB out	but for Bit 1		
Nonlinearity	Contraction of the second s		GAIN & OFF	SET ADJUSTMEN	TS
Differential Nonlinearity		and the second s	GAILGOIT	OET ABVOOTMEN	110
Differential Nonlinearity T.C Temp. Coeff. of Gain		+ 15 V		t+	15V
Temp. Coeff. of Zero, unipolar	± 30 ppm/°C max. $\pm 100 \mu$ V/°C max.	l t,		OFFSET	~
Temp. Coeff. of Offset, bipolar	± 20 ppm/°C max.		ADJ. OZI	ADJ.	150-000
Power Supply Rejection	.01% FS/% supply, max.			L	
Conversion Time	4.0 µsec. max., ADC-EH10B1	-15V T	023	GAIN	023
	2.0 µsec. max., ADC-EH10B2	GAIN L	-\$20A	ADJ L	\$20A
POWER REQUIREMENT	+15VDC ±0.5VDC @ 45mA max.	ANALOG ADJ.	0 31	ANALOG O	031
Linest in 1993au	-15VDC ±0.5VDC @ 20mA max.	IN IN	0 32	ANALOG O	032
	+5VDC ±0.25VDC @ 150mA max.		POPERATION	PIPOL A	POPERATION
PHYSICAL-ENVIRONMEN			ROPERATION		ROPERATION
Operating Temp. Range		specifications and		specifications and	ONVERT pulses to pin 3 (se d timing diagram).
Storage Temp. Range		ANALOG IN (pin	reference voltage source 32) and ANALOG GRO	UND ANALOG IN (pi	n reference voltage source to n 32) and ANALOG GROU
Relative Humidity		(pin 31). Adjust t	LSB (+4.9mV). Adjust t	refer- (pin 31). Adjust	the output of the voltage ref 2 LSB (-4.9951V). Adjust t
uase 3128	3 × 2 × .375 inches (76,2 × 30,8 × 9,5mm)	zero trimming por	entiometer so that the or	utput offset trimming p	ally between 0000 0000 00
Case Material	Black Diallyl Phthalate per MIL-M-14	and 0000 0000 01		and 0000 0000 0	1
Pins	.020" round, gold plated,	+FS - 1 1/2 LSB	of the voltage reference (+9.9854V). Adjust the 0	GAIN +FS - 1 1/2 LSE	t of the voltage reference to 3 (+4.9854V). Adjust the GA
Mariana and	.250" long min.		meter so that the output tween 1111 1111 10 and		iometer so that the output c between 1111 1111 10 and
Neight	3 oz. max. (85g.)	1111 1111 11.		1111 1111 11.	



PRICES (1-9) ADC-EH10B1 \$149.00 ADC-EH10B2 \$189.00

MATING SOCKETS: DILS-2 (2/MODULE) \$5.00/PAIR TRIMMING POTENTIOMETERS: TP20, TP200, TP20K \$3.00 EACH

THE ADC-EH10B CONVERTERS ARE COVERED BY GSA CONTRACT

 ⁻EX -25°C to +85°C operation -EXA-HS -55°C to +85°C operation with hermetically sealed semiconductor components NOTE: ADC-EH10B1 replaces former Datel model ADC-EH10B and is an improved version of the model. The only differences from the previous model is the change in input impedance from 10K ohms to 2.3K ohms, and the reduction in 5V supply current from 280mA to 150mA,



12 BIT, 4.0 AND 8.0µSEC. ANALOG TO DIGITAL CONVERTERS

MODEL ADC-EH12B1, ADC-EH12B2

FEATURES

- ▶ 4.0 µsec. Conversion \$209.
- ▶ 8.0 µsec. Conversion \$169.
- ▶ 12 Bit Resolution
- ► 30PPM/°C Tempco
- ▶ Low Profile 0.4" High

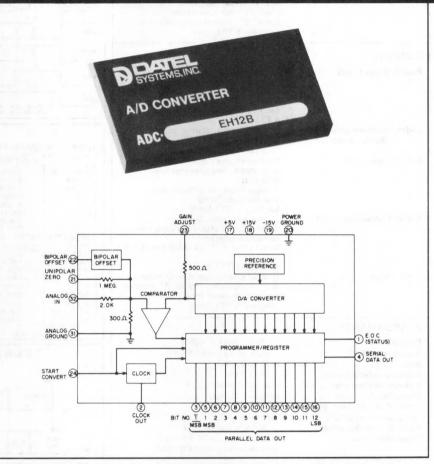
GENERAL DESCRIPTION

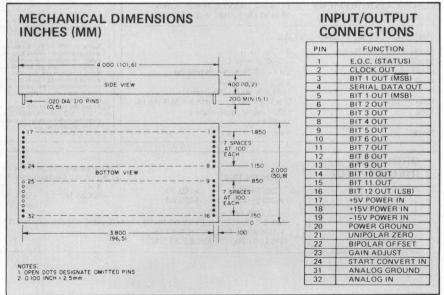
Model ADC-EH12B is a 4 microsecond, 12 bit successive approximation type A/D converter in a low profile 4 x 2 x 0.4 inch module. This high performance converter is priced at about half that of other competing models; in addition, it consumes only 2.0 watts of power, much less than competing devices. It is ideal for application in PCM systems, data acquisition systems, and other instrumentation and control systems requiring very fast data conversion rates up to 250,000 per second. The ADC-EH12B is also available in an even lower cost 8.0 usec. version.

The ADC-EH12B design utilizes an MSI integrated circuit successive approximation programmer/register, 12 fast switching current sources, a low impedance R-2R resistor network, a precision voltage reference circuit, and a fast precision comparator to achieve its very fast conversion rate.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. Full scale temperature coefficient is 30ppm/°C maximum and the converter is monotonic over its full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronization with serial data, MSB output for use in two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible.

Power requirement is $\pm 15VDC$ and $\pm 5VDC$. Extended temperature range versions are also available.





	L12P	TIMING D	AGRAM FOR	ADC-EH12B Out	put: 101010101010
SPECIFICATIONS, ADC-EF (Typical at 25°C, ±15V & +5V S	Supplies, unless otherwise indicated)		100 neec min.		1
			O need typ		•
INPUTS		EOC (STATUS)	o marc typ	T	I manuer
Analog Input Range	OV to +10V FS or ±5V FS				WALID
Input Impedance	2.3K ohms ±0.1% ±20V, no damage	CLOCK			
Start Conversion	2V min. to 5.5V max. positive pulse				
	with duration of 100 nsec. min. Rise	SERIAL			
	and fall times <500 nsec. Logic "1" resets converter	SERIAL DATA	BIT 1 BIT 2 BIT 3 B	HT 4 BIT 5 BIT 6 BIT 7 BIT 8	BIT 9 BIT 10 BIT 11 18/T 12 (LSB) 0
	Logic "0" initiates conversion	BIT 1 801			,
	Loading: 1 TTL load	BIT 1 (MSB)	P		
OUTPUTS		BIT 2		+++	++++
					0
Parallel Output Data	12 parallel lines of data held until next conversion command.	BIT 3			1
	V out (''0'') ≤ +0.4V	817 12 (LS8)			
	V out ("1") \geq +2.4V Each output capable of driving up to	i ADC	T1 T2 -EH1281 208 7600 mee, ty	p } For Start Convert = 100 neec	
	4 TTL loads.	ADC	- EH1282 105 3900 need, ty	p J	
Coding, Unipolar operation			OUT	PUT CODING	
Bipolar operation	Offset Binary, positive true Two's complement, positive true	UNIPOLAR	(0V TO +10V)		
Serial Output Data	NRZ successive decision pulse output	SCALE	INPUT VOLTAGE	STRAIGHT BINARY	
	generated during conversion with	+FS - 1 LSB	+9.9976V	1111 1111 1111	
	MSB first. Straight binary or offset binary,	+7/8 FS +3/4 FS	+8.7500∨ +7.5000∨	1110 0000 0000 1100 0000 0000	
	positive true coding.	+1/2 FS +1/4	+5.0000∨ +2.5000∨	1000 0000 0000 0100 0100 0000 0000	
End of Conversion (EOC)	Loading: 4 TTL loads Conversion Status Signal.	+1 LSB	+0.0024V	0000 0000 0001	
	V out ("0") $\leq +0.4V$ indicates con-	0	0.0000V	0000 0000 0000	
	version completed. V out (''1'') $\ge +2.4V$ during reset and		-5V TO +5V)		
	conversion.	SCALE +FS - 1 LSB	INPUT VOLTAGE +4.9976V	OFFSET BINARY	TWO'S COMPLEMENT* 0111 1111 1111
	Loading: 4 TTL loads	+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on	+1/2 FS	+2.5000∨ 0.0000∨	1100 0000 0000 1000 0000 0000	0100 0000 0000 0000 0000 0000 0000 0000 0000
	during conversion time.	-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
	Loading: 6 TTL loads	-3/4 FS -FS + 1 LSB	-3.7500∨ -4.9976∨	0010 0000 0000 0000 0000 0000 0000 0000 0000	1010 0000 0000 1000 0000 1000 0000 1000 0000 0001
PERFORMANCE		-FS	-5.0000V	0000 0000 0000	1000 0000 0000
Resolution	12 Bits (1 part in 4096)	*Using MSB out	put for Bit 1		
Accuracy at 25°C	±.012% of FS ±1/2 LSB.		GAIN & OFF	SET ADJUSTMEN	ITS
Nonlinearity		1.			
Differential Nonlinearity Differential Nonlinearity T.C		+ 15V			+15V
Temp. Coeff. of Gain	±30ppm/°C max.	11 1	ZERO	OFFSET	5
Temp. Coeff. of Zero, unipolar	$\pm 100 \mu \text{V/}^{\circ}\text{C}$ max.	201	ADJ. OZI	ADJ.	1500
Temp. Coeff. of Offset, bipolar Power Supply Rejection	±15ppm of F.S./°C max. .01% FS/% supply, max.	11 1			= 022
Conversion Time	8.0 µsec. max., ADC-EH12B1	-15V . GAIN	200	GAIN	200
	4.0 µsec. max., ADC-EH12B2	ANALOG ADJ.	031	ANALOG	031
POWER REQUIREMENT	15VDC 10 5VDC @ 40- 4	ANALOG	0 32	ANALOG	
FOWER REQUIREMENT	±15VDC ±0.5VDC @ 40mA max. +5VDC ±0.25VDC @ 150mA max.				
PHYSICAL-ENVIRONMENT		UNIPOL	AR OPERATION	BIPOLA	ROPERATION
		1. Apply START	CONVERT pulses to pin	24 (see 1. Apply START	CONVERT pulses to pin 24 (see
Operating Temp. Range		2. Apply a precision	nd timing diagram). on reference voltage sour	specifications an ce to 2. Apply a precision	d timing diagram). In reference voltage source to
Relative Humidity		ANALOG IN (p (pin 31), Adjust	in 32) and ANALOG GF the output of the voltage	ROUND ANALOG IN (p refer- (pin 31). Adjust	in 32) and ANALOG GROUND the output of the voltage refer
Case Size		ence to Zero +1 zero trimming p	/2 LSB (+1.2mV). Adjust the otentiometer so that the	t the ence to -FS+1 output offset trimming	2 LSB (-4.9988V). Adjust the potentiometer so that the outp
Case Material	(101,6 x 50,8 x 10,2mm) Black Diallyl Phthalate per MIL-M-14	code flickers eq and 0000 0000	ually between 0000 0000 0001.	0 0000 code flickers eq and 0000 0000	ually between 0000 0000 0000 0001.
	E STATE STATE STATE STATE STATE STATE	3. Adjust the outp	ut of the voltage references B (+9.9963V). Adjust th	ce to 3. Adjust the outp e GAIN +FS - 1 1/2 LS	ut of the voltage reference to B (+4.9854V). Adjust the GAIN
Pins	.020" round, gold plated,				tiometer so that the output cod
	.200" long min.	trimming poten flickers equally	tiometer so that the outp between 1111 1111 111	0 and flickers equally	between 1111 1111 1110 and
	.200" long min.	trimming poten	tiometer so that the outp between 1111 1111 111	0 and flickers equally 1111 1111 111	between 1111 1111 1110 and
Weight	.200" long min.	trimming poten flickers equally 1111 1111 111	tiometer so that the outp between 1111 1111 111 1.	0 and flickers equally 1111 1111 111	between 1111 1111 1110 and
	.200'' long min. 4 oz. max. (114 g.)	flickers equally 1111 1111 111	tiometer so that the outp between 1111 1111 111 1. mperature range o	0 and flickers equally 1111 1111 111 peration, the followin	between 1111 1111 1110 and I. g suffixes are
Weight	.200" long min. 4 oz. max. (114 g.) PRICES (1-9)	flickers equally 1111 1111 111	tiometer so that the outp between 1111 1111 111 mperature range o del number. Consi 25°C to +865	0 and flickers equally 1111 1111 111 peration, the followin ult factory for pricing ² C operation	between 1111 1111 1110 and
INFORMATION	.200'' long min. 4 oz. max. (114 g.)	For extended ter added to the mo	tiometer so that the outp between 1111 1111 111 1. mperature range of del number. Conso -25°C to +85° -55°C to +85°	0 and flickers equally 1111 1111 111 peration, the followin ult factory for pricing ² C operation with her	between 1111 1111 1110 and
Weight ORDERING INFORMATION	.200" long min. 4 oz. max. (114 g.) PRICES (1-9) ADC-EH12B1 \$169.00 ADC-EH12B2 \$209.00 MATING SOCKETS:	For extended ter added to the mo -EX -EXX-HS	tiometer so that the outp between 1111 1111 111 1. mperature range of del number, Consi -25°C to +85° -55°C to +85° semiconducto	0 and flickers equally 1111 1111 peration, the followin ult factory for pricing ^o C operation ^o C operation with her r components	g suffixes are metically sealed
Weight ORDERING INFORMATION ADC-EH12B	.200" long min. 4 oz. max. (114 g.) PRICES (1-9) ADC-EH12B1 \$169.00 ADC-EH12B2 \$209.00 MATING SOCKETS:	For extended ter added to the mo -EX -EXX-HS	tiometer so that the outp between 1111 1111 111 1. mperature range of del number, Consi -25°C to +85° -55°C to +85° semiconducto	0 and flickers equally 1111 1111 111 peration, the followin ult factory for pricing ² C operation with her	g suffixes are metically sealed



ULTRA FAST 12 BIT ANALOG TO DIGITAL CONVERTER

MODEL ADC-EH12B3

FEATURES

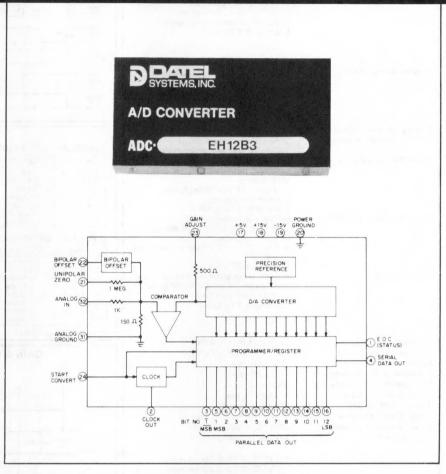
- ▶ 2.0 µsec. Conversion Time
- ▶ 12 Bit Resolution
- ▶ Low Power Consumption 2.25W
- ▶ Low Profile Case 0.4" High
- ▶ Economy Price \$249.00

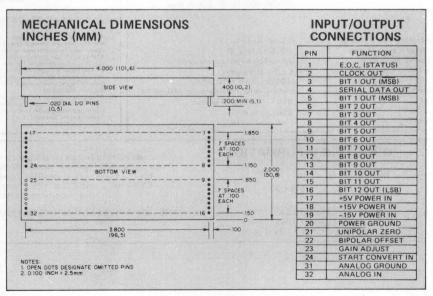
GENERAL DESCRIPTION

Model ADC-EH12B3 is a new, ultra fast, 12 bit successive approximation A/D converter with a 2.0 microsecond maximum conversion time. This converter utilizes 12 very fast switched current sources with a low impedance R-2R ladder network, a fast precision comparator, a precision zener reference source, and an MSI integrated circuit successive approximation register to achieve its state of the art performance. It is encapsulated in a low profile 2 x 4 x 0.4 inch module and consumes only 2.25 watts of power. The ADC-EH12B3 opens up a broad range of fast data conversion applications where conversion rates up to 500,000 per second are required.

Input voltage ranges are 0 to +10V unipolar or ±5V bipolar by external pin connection; input impedance is 1.15K ohms. The parallel output is in straight binary, offset binary, or two's complement coding. Serial output data is also brought out in the form of an NRZ format MSB first pulse train. Full scale temperature coefficient is ±30ppm/°C maximum and zero temperature coefficient is $\pm 100 \,\mu V/^{\circ}C$ maximum. Due to its low differential linearity temperature coefficient there are no missing codes over the 0°C to 70°C operating temperature range. Provision is made for precise alignment in a given application.

Other DTL/TTL compatible outputs include clock, MSB output (for two's complement coding), and end of conversion (status) output. Power supply requirement is ±15VDC and +5VDC.





SPECIFICATIONS, ADC-EH12B3

(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

					0
Analog Input Range	OV to +10V FS or ±5V FS	E O C ISTATUSI) nsec typ	1950 nsec	DATA NOW
nput Impedance	1.15K ohms ±0 1%		- 40 nsec. typ1	00 nsec	15 nsec. typ 1
nput Overvoltage	±20V, no damage 2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise	CLOCK OUT	1 21 31 4		10 11 12 40 nsec 0
	and fall times <500 nsec. Logic ''1'' resets converter	SERIAL DATA OUT	BIT 1 (MSB) BIT 2 BIT 3 BIT 3		BIT 9 BIT 10 BIT 11 1 15 12 1 (LSB) 0
	Logic ''0'' initiates conversion Loading: 1 TTL load	BIT 1 80 m			1
		BIT 2			
Parallel Output Data	12 parallel lines of data held until next conversion command. V out $("0") \le +0.4V$	BIT 3 BIT 12			
	V out $(''1'') \ge +2.4V$ Each output capable of driving up to 4 TTL loads.	(LSB)			<u>-</u> - <u>-</u>
Coding, Unipolar operation	Straight Binary, positive true		0117	PUT CODING	
Bipolar operation	Offset Binary, positive true Two's complement, positive true	UNIPOLAR	(0V TO +10V)	FUT CODING	
Serial Output Data	NRZ successive decision pulse output	SCALE	INPUT VOLTAGE	STRAIGHT BINARY	
	generated during conversion with MSB first.	+FS - 1 LSB +7/8 FS	+9.9976∨ +8.7500∨	1111 1111 1111 1111 1110 0000 0000	
	Straight binary or offset binary,	+3/4 FS	+7.5000V	1100 0000 0000	
	positive true coding.	+1/2 FS	+5.0000V	1000 0000 0000	
	Loading: 4 TTL loads	+1/4 +1 LSB	+2.5000∨ +0.0024∨	0100 0000 0000 0000 0000 0000 0000 0000 0000	
nd of Conversion (EOC)		0	0.0000V	0000 0000 0000	
	V out ("0") $\leq +0.4V$ indicates conversion completed.	BIPOLAR (-	-5V TO +5V)		
	V out ("1") +2.4V during reset and	SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
	conversion. Loading: 4 TTL loads	+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
Clock Output	Internal clock pulse train of negative	+3/4 FS +1/2 FS	+3.7500∨ +2.5000∨	1110 0000 0000 1100 0000 0000	0110 0000 0000 0100 0000 0000 0000
	going pulses from +5V to 0V gated on	0	0.0000V	1000 0000 0000	0000 0000 0000
	during conversion time.	-1/2 FS	-2,5000V	0100 0000 0000	1100 0000 0000
	Loading 6 TTL loads	-3/4 FS	-3 7500V	0010 0000 0000	1010 0000 0000 1000 0000 0001
		-FS + 1 LSB -FS	-4.9976∨ -5.0000∨	0000 0000 0001 0000 0000 0000	1000 0000 0000
		*Using MSB out	put for Bit 1		
Resolution	12 Bits (1 part in 4096)				
Accuracy at 25 C			GAIN & OFF	SET ADJUSTMEN	ITS
Nonlinearity					
Differential Nonlinearity Differential Nonlinearity T.C		+ 15 V			+15V
Temp. Coeff. of Gain	± 30ppm/°C max.	ll t	ZERO	OFFSET	5
Temp. Coeff. of Zero, unipolar	$\pm 100 \mu\text{V/}^{\circ}\text{C}$ max.	}	101	ADJ.	2000
Temp. Coeff. of Offset, bipolar		20K	AUG 021		- 150 - 15
Power Supply Rejection	+15ppm of F.S./ C max.				- 022
	±15ppm of F.S./ ^o C max. .01% FS/% supply, max.	-15/			
	 15ppm of F.S./ C max. .01% FS/% supply, max. 2.0 μsec. maximum 	-15V	023	GAIN	023
	.01% FS/% supply, max. 2.0 μsec. maximum	GAIN ADJ ANALOG		ANALOG	200 O23
	.01% FS/% supply, max.	GAIN	Laszon) ADJ	200
	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max.	GAIN ADJ ANALOG ANALOG IN	200		031
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max.	GAIN ANALOG ANALOG ANALOG UNIPOL	AR OPERATION	ANALOG GND ANALOG ANALOG BIPOLA BIPOLA 24 (see 1. Apply START)	AR OPERATION
Conversion Time	.01% FS/% supply, max. 2.0 µsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0 °C to 70° C	GAIN ANALOG GND ANALOG IN UNIPOL	AR OPERATION CONVERT pulses to pin d timing diagram).	ADJ ANALOG GND ANALOG ANALOG BIPOLA 24 (see 1. Apply START specifications at ce to 2. Apply a precision	AR OPERATION CONVERT pulses to pin 24 (s dt timing diagram).
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C	GAIN ANALOG GND ANALOG IN UNIPOL 1. Apply START specifications a 2. Apply a presis ANALOG IN (r	AR OPERATION CONVERT pulses to pin nd timing diagram). on reference voltage sourci in 321 and ANALOG GP	ADJ ANALOG GND ANALOG IN BIPOLA 24 (see 1. Apply START 1 specifications at ce to 2. Apply a precisio 30UND ANALOG IN (p	R OPERATION CONVERT pulses to pin 24 (s nd timing diagram). on reference voltage source to m 32) and ANALOG GROU
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C Up to 100% non-condensing	GAIN ANALOS GND ANALOS IN UNIPOL 1. Apply START specifications a 2. Apply a presis ANALOG IN (r (pin 31). Adjus ence to Zero 1	AR OPERATION CONVERT pulses to pin nd timing diagram). on reference voltage sourci in 321 and ANALOG GF t the output of the voltag 72 LSB (+1.2mV). Adjus	ADJ ANALOG GND ANALOG ANALOG IN BIPOLA 24 (see to 24 (see to 30UND BOUND ANALOG See to 30UND 24 Apply START 30UND 24 Apply START 30UND 26 Apply ADA 30UND 26 Apply START 30UND 26 Apply START 20	AR OPERATION CONVERT pulses to pin 24 (s and timing diagram). In reference voltage source to in 32) and AALOG GROUI the output of the voltage ref 2 LSB (-4 9988V). Adjust if
Departing Temp. Range	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C Up to 100% non-condensing 4 × 2 × 0.4 inches (101,6 × 50,8 × 10,2mm)	GAIN ANALOS GND ANALOS IN UNIPOL 1. Apply START specifications a Specifications ANALOS UNIPOL 1. Apply START specifications ANALOS IN Specifications ANALOS ANALOS AN	AR OPERATION CONVERT pulses to pin nd timing diagram). on reference voltage source in 321 and ANALOG GF t the output of the voltag 72 LSB (+1, 2mV). Adjus potentiometer so that the ually between 0000 000	ADJ ANALOG GND ANALOG ANALOG ANALOG ANALOG IN BIPOLA 24 (see 1. Apply START 1 specifications al specifications al S	AR OPERATION CONVERT pulses to pin 24 (in a timing diagram). on reference voltage source to in 32) and ANALOG GROUI ithe output of the voltage ref (2 LSB (-4 9988V). Adjust t potentiometer so that the ou ually between 0000 0000 000
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C Up to 100% non-condensing 4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm) Black Diallyl Phthalate per MIL-M-14	GAIN ANALOGO ANALOGO IN UNIPOL 1 Apply START specifications a 2 Apply a presis ANALOG IN ((pin 31). Adjus ence to Zero 11 zero trumming code flickers eg and 0000 0000	AR OPERATION CONVERT pulses to pin d timing diagram). In reference voltage sour in 321 and ANALOG GF t the output of the voltage joint of the voltage sources of the voltage voltage sources of the voltage sources of the voltage sources of the voltage voltage sources of the voltage sources of the voltage sources of the voltage voltage sources of the voltage sources of the voltage sources of the voltage voltage sources of the voltage sou	ADJ ANALOG GND ANALOG ANALOG ANALOG IN BIPOLA 24 [see 1. Apply START i specifications an ADJ ADJ ADJ ADJ ADJ ADJ ADJ ADJ	AR OPERATION CONVERT pulses to pin 24 (s dt timing diagram). on reference voltage source to in 32) and ANALOG GROUU the output of the voltage ref /2 LSB (-4.9988V). Adjust to potentiometer so that the potentiometer so that the 0001.
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max. -15VDC ±0.5V @ 20mA max. +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C Up to 100% non-condensing 4 × 2 × 0.4 inches (101.6 × 50.8 × 10.2mm) Black Diallyl Phthalate per MIL-M-14 .020″ round, gold plated,	GAIN ANALOG ANALOG ANALOG IN UNIPOL 1. Apply START specifications a 2. Apply a pressi ANALOG IN (r (pin 31). Adjus ence to Zero 11 zero trimming code flickers eg and 0000 0000 3. Adjust the outp +FS - 11/2 LS	AR OPERATION CONVERT pulses to pin d timing diagram). CONVERT pulses to pin d timing diagram). The output of the voltage source to the voltage to the voltage source to the voltage reference B (+9.99630). Adjust the source to the source to the voltage reference B (+9.996300). Adjust the source to the source to the voltage reference B (+9.996300). Adjust the source to the	ADJ ANALOG GND ANALOG ANAL	AR OPERATION CONVERT pulses to pin 24 (s d timing diagram). CONVERT pulses to pin 24 (s d timing diagram). In reference voltage source to in 32) and ANALOG GROUU the output of the voltage ref potentiometer so that the output potentiometer so that the output potentiometer so that the form output between 0000 0000 000 0001. ut of the voltage reference to 8 (+4.9854V). Adjust the GA
Conversion Time	.01% FS/% supply, max. 2.0 μsec. maximum +15VDC ±0.5V @ 80mA max, -15VDC ±0.5V @ 20mA max, +5VDC ±0.25V @ 150mA max. 0°C to 70°C -25°C to +85°C Up to 100% non-condensing 4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm) Black Diallyl Phthalate per MIL-M-14 .020″ long min.	GAIN ANALOG ADJ GND ANALOG IN UNIPOL 1. Apply START specifications a 2. Apply START specifications a 2. Apply START specifications a 2. Apply a precision ANALOG IN (f (pin 31) Adjus ence to Zero 1 zero trimming f code flickers eq and 0000 0003. Adjust the outp +FS - 1 1/2 LE trimming poten	AR OPERATION CONVERT pulses to pin d timing diagram). CONVERT pulses to pin d timing diagram). The output of the voltage source the output of the voltage voltage reference 18 (+9.9963V). Adjust to tiometer so that the output between 111 1111 111	ADJ ANALOG GND ANALOG ANALOG ANALOG ANALOG ANALOG ANALOG Compositions and Specifications and Specifications and Source and AnaLOG (IN) BIPOLA 24 (see 2 Apply START 1 Specifications and Source and Source and Source and S	AR OPERATION CONVERT pulses to pin 24 (s d timing diagram). CONVERT pulses to pin 24 (s d timing diagram). In reference voltage source to in 32) and ANALOG GROUM the output of the voltage ref /2 LSB (-4.9988V). Adjust the dual potentiometer so that the output co 8 (+4.9854V). Adjust the GA tiometer so that the output co between 1111 1111 1110 and

ORDERING INFORMATION

PRICES (1-9) ADC-EH12B3 \$249.00 MATING SOCKETS: DILS-2 (2/MODULE) \$5.00/PAIR

TRIMMING POTENTIOMETERS: TP20, TP200, TP20K \$3.00 EACH For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing. -EX -25°C to +85°C operation -EXX-HS -55°C to +85°C operation with hermetically sealed

semiconductor components

THE ADC-EH12B3 CONVERTER IS COVERED UNDER GSA CONTRACT.

TIMING DIAGRAM FOR ADC-EH12B3 Output 101010101010

- 100 nsec min

START CONVERT





1 µSEC TOTAL CONVERSION TIME

ADC-G SERIES

FEATURES

- ▶ 8 and 10 Binary Bit Versions
- 100 nsec/bit Conversion Time
- ▶ ±1/2 LSB Linearity
- Four Input Ranges To Choose From

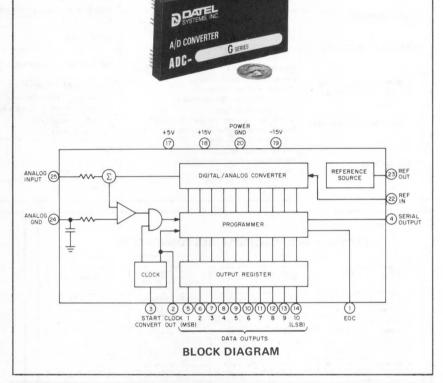
GENERAL DESCRIPTION

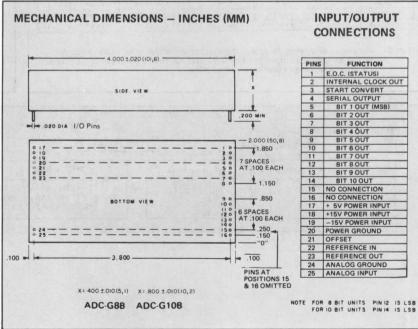
The ADC-G Series are 8 or 10 binary bit, analog to digital converters offering another price breakthrough by Datel Systems. The ADC-G Series provide the user with a combination of high speed, moderate high resolution, and compact size, all for a cost well below competing units. All this is made possible by the use of a proprietary modified successive approximation conversion technique, unique packaging methods and volume production.

Both models use the inherently accurate successive approximation conversion method to compare an unknown analog input signal against the output of a precision digital-to-analog converter in a high gain feedback loop. This method guarantees a full monotonic conversion and excellent linearity over the full scale input range.

The ADC-G Series is completely self contained, consisting of an operational temperature compensated voltage reference source, successive approximation logic circuitry, output storage register/ programmer, an ultra-high speed low noise voltage comparator and a precision digital-to-analog converter. All units provide adjustment free operation over a temperature range of 0° C to $+70^{\circ}$ C, requiring only D.C. power and a start convert command, which will interface with DTL or TTL logic levels.

Numerous other modules are available at little cost; these include a narrow aperture sample and hold, an eight channel multiplexer, ultra-miniature D.C. power supplies and system programmer. These modules are all compatible and can be easily integrated into a complete multi-channel data acquisition system.



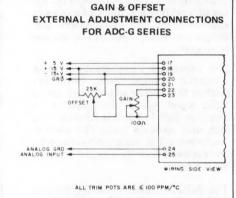


	ADC-G SERIES	and the second se	ADC-G SERIES	
INPUTS	1 1 1 1 2 3 2 3 1 1 1 2 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2	a series a series of the series	
INPUT VOLTAGE RANGE AND INPUT IMPEDANCE	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	SERIAL OUTPUT	NRZ successive decision pulse output generated during conversion, with MSB first V out (''0'') \leq +0.4V V out (''1'') \leq +2.4V	
INPUT OVERVOLTAGE	±15VDC		Loading up to 5 TTL loads	
INPUT IMPEDANCE	2K Ohms typical	PERFORMANCE		
SOURCE CURRENT	5 ma Max. 2V min. to 7V max. positive pulse	RESOLUTION	One part in 2 ⁿ (max. resolution 10 bits) n = number of binary bits	
	30 nanoseconds min. width	ACCURACY (@ 25°C)	Adj. to ±0.1% ±1/2 LSB - all models	
START CONVERSION (Trigger Command)	Loading, 3 TTL Loads 500 nSec	LINEARITY	±1/2 LSB	
(Trigger Command)	"1" Resets max. rise	LONG TERM STABILITY	±0.1%/6 month period	
	"0" Starts Conversion time.	TEMPERATURE COEFFICIENT	±50 ppm/°C	
DIGITAL OUTPUTS	GITAL OUTPUTS		100 nsec/bit for all models	
PARALLEL OUTPUT DATA	8 or 10 parallel lines of data, held until next conversion command V out ("0") $\leq +0.4V$	WORD RATE	1.25 MHz – 8 binary bits 1.0 MHz – 10 binary bits	
FARALLEL GOTFOT DATA	V out ("1") \ge +2.4V Each output capable of driving up to 6 TTL loads	INPUT POWER REQUIREMENTS	+ 5 VDC, ±0.25VDC @ 380 ma max. + 15 VDC, ±0.5 VDC @ 50 ma max. 15 VDC, ±0.5 VDC @ 30 ma max.	
OUTPUT DIGITAL CODING	Straight Binary (Unipolar Input) Offset Binary (Bipolar Input)	PHYSICAL ENVIRONMENTAL		
INVERTED OUTPUTS (2)	Two's Complement (Bipolar Input)	OPERATING TEMPERATURE RANGE	0° to + 70° C	
	Conversion Status Signal	STORAGE TEMPERATURE RANGE	-55° C to +85° C	
END OF CONVERSION OUTPUT	Conversion Complete – V out (''0'') $\leq +0.4V$	RELATIVE HUMIDITY	Up to 100% non-condensing	
	Reset & Conversion Period – V out ("1") ≥ +2.4V	CASE MATERIAL (1)	Black Diallyl Phthalate, per MIL-M-14	
	Loading up to 5 TTL loads Internal clock output	PINS	0.020" round gold plated 0.250" long min.	
CLOCK OUTPUT	Negative going pulse from +5V max. Pulse width 30 nsec	SIZE	2''W x 4''L x 0.4''H (8 bits) 2''W x 4''L x 0.8''H (10 bits)	
	Loading up to 6 TTL loads	WEIGHT	8 oz. max. Note (1): Converters are fully repairable	

and the second se				
CODING F	OR ADC-	-G10B	SERIES	CONVERTERS
00011101	011 1100	0.00	OFILEO	CONTRACTOR

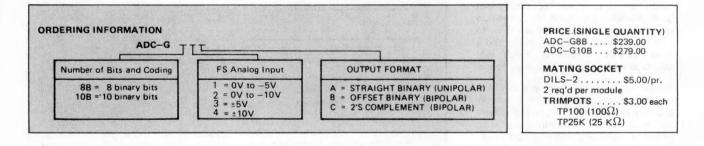
ANALOG INPUT RANGE 1 0 TO - 5V, FS	ANALOG INPUT RANGE 2 0 TO – 10V, FS	ANALOG INPUT RANGE 3 ±5V, FS	ANALOG INPUT RANGE 4 ±10V, FS	DIGITAL OUTPUTS NOTE (2) OFFSET BINARY FOR RANGES 3 AND 4 STRAIGHT BINARY FOR RANGES 1 AND 2	DIGITAL OUTPUTS NOTE (2) 2'S COMPLEMENT FOR RANGES 3 AND 4
ov	ov	+5 V	+10V	000000000000	100000000000
- 0.625V	-1.25V	+3.75V	+7.5V	001000000000	101000000000
-1.25 V	-2.5 V	+2.5V	+5.0V	010000000000	110000000000
- 1.875V	- 3.75V	+1.25V	+2.5V	011000000000	111000000000
-2.5V+1LSB	-5V+1 LSB	OV+I LSB	OV+I LSB	011111111111	
-2.5V	- 5 V	ov	ov	100000000000	0000000000000
-2.5V-1 LSB	- 5V - I LSB	OV-ILSB	OV-ILSB	100000000001	000000000000
- 3.125 V	-6.25V	-1.25V	-2.5V	101000000000	001000000000
- 3.75V	- 7.5 V	-2.5V	-5.0V	110000000000	010000000000
- 4.375V	-8.75V	-3.75V	-7.5V	111000000000	011000000000
-5V+1LSB	-10V+1 LSB	-5V+ILSB	- 10V+1 LSB		011111111111

Note 2: *Reverse coding sense:* Note that the most negative analog input corresponds to full scale digital output (11-1 binary). Normal coding sense can be obtained by using an external inverting input amplifier.



Connections shown here must be made to insure proper operation of converter.

Adjustment Ranges: Offset: ±0.5% of FS Gain: ±2% of FS





8 BINARY BITS-10 MILLION CONV'S/SEC ANALOG TO DIGITAL CONVERTER

ADC-UH SERIES

FEATURES

- Smallest Size . . . 3"W x 5"L x 1.150"H
- Fast Encoding Time..... to 40nsec
- Excellent Temperature
- ► Coefficient.....±0.005%/°C

GENERAL DESCRIPTION

The ADC-UH series are state-of-the-art ultra high speed analog to digital converters consisting of three models; six and eight binary bits operating at word repetition rates of up to 10 MHz and a four bit version capable of making a conversion every forty nanoseconds.

In addition to the cost and performance advantages of all three models, close attention to circuit detail has resulted in a highly reliable converter with relatively low power consumption.

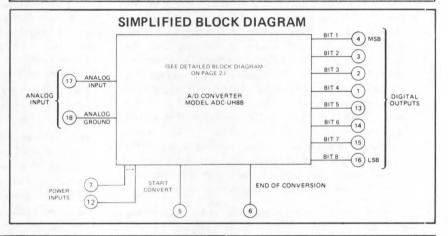
The entire converter is packaged in a black anodized aluminum module to provide electrostatic shielding. Overall physical size is 3'Wx5''Lx1.150''H, or one fifth the size of the nearest rival. Power drain has been reduced to eight watts, which is a fraction of competing units and a good measure of the ADC-UH series reliability.

Other features relating to the integrity of the circuit design, are its low temperature coefficient of $50ppm/^\circ C$ and long term stability of $\pm.25\%/year.$

Input power requirements are $\pm 15VDC$ and $\pm 5VDC.$

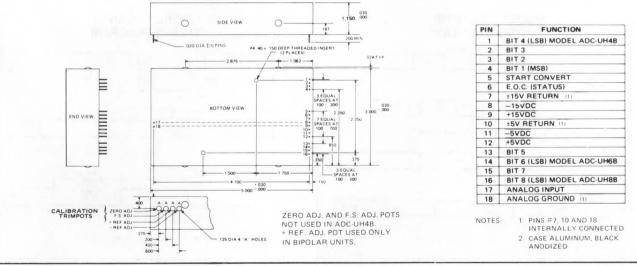
Output digital coding is straight binary for a unipolar input and inverted offset binary for the optional bipolar input.

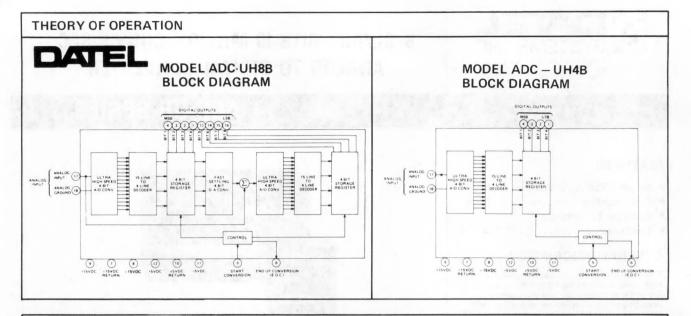




MECHANICAL DIMENSIONS (INCHES)







TECHNICAL DESCRIPTION

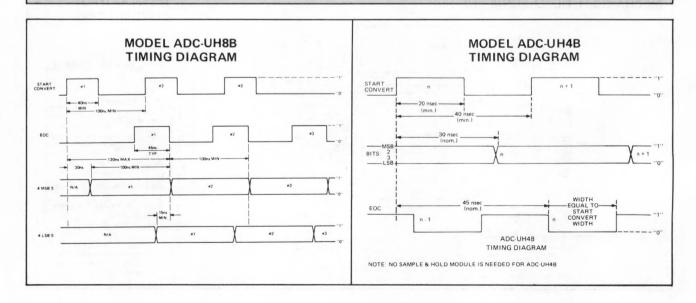
The model ADC-UH8B analog to digital converter employs a two step conversion technique as shown in the block diagram. The analog input signal is fed to a 15 line, 4 bit comparator array (4 bit A/D converter) where the four most significant bits are determined. This four bit word is then stored in an output register which also controls a 4 bit subtracting digital-to-analog converter where the analog value of the first four most significant bits is subtracted from the analog input. The voltage difference is then fed to a second 15 line, 4 bit comparator array (4 bit A/D converter) to determine the remaining four least significant bits. This 4 bit word is then stored in an output register with the four most significant bits to complete the conversion cycle.

As shown in the timing diagram the leading edge of the start convert pulse initiates a conversion cycle by activating the first stage A/D converter. One hundred and thirty nanoseconds later the End of Conversion pulse will go negative indicating the conversion is complete and the data is ready at the output. Although the throughput delay is 130 nanoseconds a new start convert input pulse can be issued at a minimum interval of 100 nanoseconds resulting in a maximum word rate of 10 MHz.

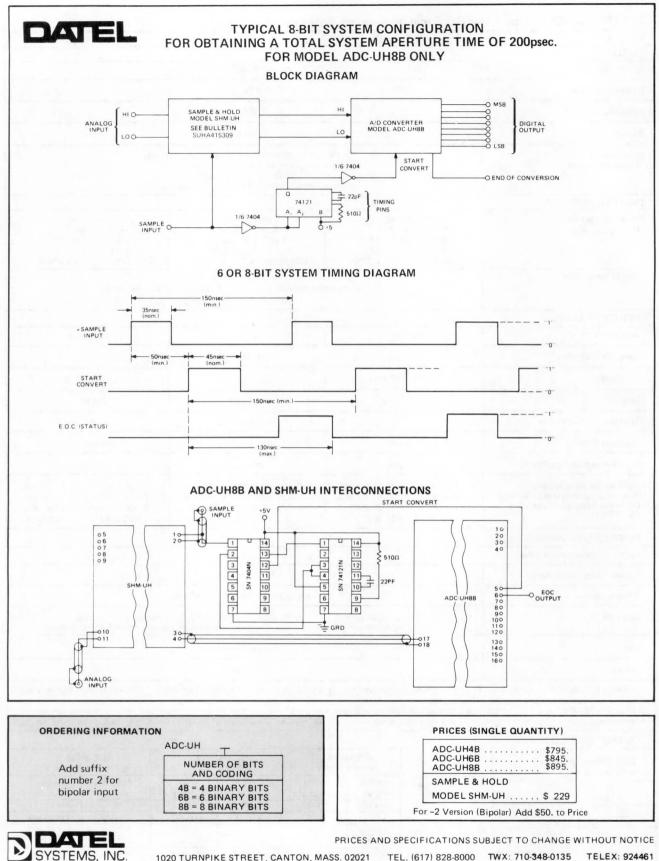
The 10 MHz word rate is made possible by the two stage conversion technique which allows a new conversion cycle to be started before the prior cycle is completed.

In transferring an output word, it should be noted that a minimum of 15 nanoseconds is allowed for transfer set-up while no time is allowed for holding the word after transfer. Transfer can be implemented by using a zero hold time register such as a SN 74H106.

The model ADC-UH4B block diagram shows that the 4-bit converter employs a single step conversion method and does not use the analog difference summing junction.



INPUTS: OV to -2560V FS (1) Analog laput Range OV to -2560V FS (1) Input Overotige ±5VDC Input Impedance 100 Ohms Source Current 25.6 mA Sert Conversion 2V min, to SV max, positive pulse, 40nsc min, width positive excursion infinises accentration (Friger Command) DIGITAL OUTPUTS: A parallel lines (4 Binary Bin) 6 parallel lines (6 Binary Bin) 8 parallel lines (9 Binary Bin) 8 p	MODEL		ADC-	UH4B	40 1 mm	ADC-UH6B	100	ADC-U	H8B	
Input Overvoltage = 5500C Input Impedance = 100 Ohms Source Current = 25.6 m A Start Conversion = 27.6 m A Start Conversion = 27	INPUTS:		Velocity Velocity	Section States	to cont	105				
Input Impedance 100 Dhms Source Current 25.6 mA Source Current 25.6 mA Source Current 27.0 min, to 5V max, positive puble, 40nsec min, width positive excursion initiates a convention LOADING: 1 TTL LOAD MAXIMUM REPETTION RATE – 10MHz (2) DIGITAL OUTPUTS: Parallel Output Date (4 Binary Bin) V out ("1") > 42.4V V out ("1") > 42.4V LOADING: 4 TTL LOADS 8 parallel lines (6 Binary Bin) V out ("1") > 42.4V V out ("1") > 42.4V LOADING: 14 TTL LOADS End of Conversion Positive Puble, Trailing edge (negative transition) indicates conversion complete LOADING: 12 TTL LOADS Vol ("1") > 42.4V V out ("1") > 42.4V V out ("1") > 42.4V PERFORMANCE: accurace 02 STC ±3% of FS ±0.0.8% of FS ±0.4% of FS Resolution 1LSB (160 mV) 1LSB (40 mV) 1LSB (10 mV) 1LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1/2LSB ±1/2LSB Temperature Coefficient ±500pm/f C Encoding Time 40 nsec 100 nsec (2) 100 mit (2) Word Repetition Rate (MAX.J) 25 MHz 10 MHz (2) 10 MHz (2) 10 MHz (2) 15VDC, 60.2VDC @ 90 mA -15VDC, 60.2VDC @ 90 mA	Analog Input R	ange	-		-	0V to -2.560V F	S (1)	The start was a set of the		
Source Current 25.6 mA Start Conversion (Trigger Command) 2V min, to 5V max, positive pulse, 40mac min, width positive exclusion marks the table (a Binary Bint) 2V min, to 5V max, positive pulse, 40mac min, width positive exclusion marks the table (a Binary Bint) DIGITAL OUTPUTS: Parallel lines (a Binary Bint) 6 parallel lines (a Binary Bint) 8 parallel lines (a Binty Bint) 8 parallel	Input Overvolta	nge				±5VDC				
Start Conversion (Trigger Command) 2V min, to SV max, positive pulse, 40nsec min, width positive scursion initiates a conversion LOADING: 1TTL LOAD MAXIMUM REPETITION RATE -10MH2 (2) DIGITAL OUTPUTS: Parallel Output Data (See coding chart) 4 parallel lines (4 Binary Bits) V out ("0" < 0.4V V out ("0" > 0.4V V out	Input Impedance	ce				100 Ohms	1			
ITrigger Command) Dositive excursion initiates a conversion LCADING: 1TL LOAD MAXIMUM REPETITION RATE -10MHz (2) DIGITAL OUTPUTS: 4 parallel lines (8 parallel lines (8 parallel lines) (9 parallel lines) (Source Current	- Aller		1.44		25.6 mA				
Parallel Output Data (See coding chart) 4 parallel lines (Binary Bit) V out ("") = 10.4V V out ("") = 7.4V LOADING: 4 TTL LOADS 8 parallel lines (Binary Bit) V out ("") = 7.4V LOADING: 4 TTL LOADS End of Conversion Positive Pales, Trailing edge (ngstive transition) indicates conversion complete LOADING: 12 TTL LOADS V out ("") = 7.4V LOADING: 4 TTL LOADS PERFORMANCE: Tailing edge (ngstive transition) indicates conversion complete LOADING: 12 TTL LOADS Positive Pales, trailing edge (ngstive transition) indicates conversion complete LOADING: 12 TTL LOADS PERFORMANCE: accuracy @ 25" C ±3% of FS ±0.4% of FS Long Term Stability ±0.25%/year #158B (10 mV) 1LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1LSB Temperature Coefficient ±500pm/"C 100 nsec (2) 100 nsec (2) Imput Power Requirements See Date System Ultraminiture PS/DC, 60 / VDC © 80 mA -15VDC, 60 / VDC © 9 mA -5VDC, 60 / VDC © 100 mA -5VDC, 50 / VDC © 100 mA +15VDC, 50 / VDC © 9 mA -5VDC, 50 / VDC © 100 mA +15VDC, 50 / VDC © 80 mA -5VDC, 50 / VDC © 100 mA -15VDC, 50 / VDC © 100 mA +15VDC, 50 / VDC © 100 mA -5VDC, 50 / VDC © 100 mA <t< td=""><td></td><td></td><td></td><td></td><td>sitive excursi LO</td><td>on initiates a con ADING: 1 TTL I</td><td>version LOAD</td><td></td><td></td></t<>					sitive excursi LO	on initiates a con ADING: 1 TTL I	version LOAD			
Ide Binary Bits) U Ide Binary Bits) U <	DIGITAL OU	TPUTS:			18					
Trailing edge (negative transition) indicates conversion complete LOADING: 12 TTL LOADIS PERFORMANCE: Accuracy @ 25° C ±3% of FS ±0.08% of FS ±0.4% of FS Long Term Stability ±0.25%/year ±0.08% of FS ±0.4% of FS Resolution 1LSB (160 mV) 1LSB (40 mV) 1LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1/2LSB ±1LSB Temperature Coefficient ±50ppm/°C 100 nsec (2) 100 nsec (2) 100 nsec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datel System Ultraminiature DCP Ower Supplies - Bulletin = 5VDC, 20 VDC @ 59 mA +5VDC, 20 VDC @ 9 mA +5VDC, 20 VDC @ 9 mA +5VDC, 20 VDC @ 9 mA +5VDC, 20 VDC @ 150 mA -5VDC, 20 VDC @ 10 mA 15VDC, 20 VDC @ 10 mA -5VDC, 20 VDC @ 1000 PHYSICAL-ENVIRONMENTAL: Operating Temperature Range 0.020° round goid plated 0.250° long minimum Case S° C Stres 0.020° round goid plated 0.250° long minimum Case S° C Strest Strest Strest Strest VIII Strest VIII Strest VIII Strest VIII Strest VIIII Strest VIIII S			(4 Binar V out (''0'' V out (''1''	ry Bits)) ≤ +0.4∨) ≥ +2.4∨		(6 Binary Bits) / out (''0'') \leq +0. / out (''1'') \geq +2.	4V .4V	(8 Binary V out (''0'') V out (''1'')	Bits) ≤ +0.4∨ ≥ +2.4V	
Accuracy @ 25° C ±3% of FS ±0.4% of FS ±0.4% of FS Long Term Stability ±0.25%/year Resolution 1LSB (160 mV) 1LSB (40 mV) 1LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1LSB Temperature Coefficient ±50ppm/°C ±100 nsec (2) 100 nsec (2) 100 nsec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datal Systems Ultraminiature DC Power Supplies: Bulletin PS/DC, ±0.2VDC @ 80 mA -15VDC, ±0.2VDC @ 90 mA -5VDC, ±0.1VDC @ 150 mA +15VDC, ±0.2VDC @ 80 mA -15VDC, ±0.2VDC @ 90 mA -5VDC, ±0.1VDC @ 170 mA +15VDC, ±0.2VDC @ 90 mA -5VDC, ±0.1VDC @ 170 mA +15VDC, ±0.2VDC @ 90 mA -5VDC, ±0.1VDC @ 170 mA +15VDC, ±0.2VDC @ 170 mA -5VDC, ±0.1VDC @ 170 mA	End of Conver	rsion		Trailir	· · · · · · · · · · · · · · · · · · ·	ive transition) in	dicates conve	rsion complete		
Long Term Stability ±0.25%/year Resolution 1LSB (160 mV) 1LSB (40 mV) 1LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1LSB Temperature Coefficient ±50ppm /° C ±100 nsec (2) 100 nsec (2) Bronding Time 40 nsec 100 nsec (2) 100 nsec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datel Systems Ultraminiature DC Power Supplies Bulletin PS-UDC, ±0.1VDC © 450 mA +5VDC, ±0.1VDC © 450 mA +5VDC, ±0.1VDC © 150 mA +15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC © 170 mA PHYSICAL-ENVIRONMENTAL: Operating Temperature Range 0° C to +70° C Storage Temperature Range 0° C to +70° C Storage Temperature Range 0.020° round gold plated 0.250° long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3° Wx5° Lx1.150° H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. 1) Models ADC-UH6B And ADC-UH6B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput	PERFORMA	NCE:								
Resolution 1 LSB (160 mV) 1 LSB (40 mV) 1 LSB (10 mV) Linearity ±1/2LSB ±1/2LSB ±1/2LSB ±1/2LSB Temperature Coefficient ±50ppm/°C ±50ppm/°C Encoding Time 40 nsec 100 nsec (2) 100 msec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) Input Power Requirements (See Date Systems Ultraminiature DC Power Supplies - Bulletin PSVDC, ±0.2VDC © 40 mA +5VDC, ±0.1VDC © 50 mA +15VDC, ±0.2VDC © 80 mA -5VDC, ±0.1VDC © 780 mA +5VDC, ±0.1VDC © 170 mA +15VDC, ±0.2VDC © 9 mA +5VDC, ±0.1VDC © 170 mA PHYSICAL-ENVIRONMENTAL: Operating Temperature Range 0° C to +70° C Storage Temperature Range 0.020° round gold plated 0.250° long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3° Wx5″ Lx1.150° H Weight 15 oz. NOTEs: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number.) Models ADC-UH6B and ADC-UH6B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th the most nega- tive analog input correspond store. ADC-UH6B ADC-UH6B have a throughput delay of 1	Accuracy @ 2	5°C	±3%	of FS		±0.8% of FS		±0.4%	of FS	
Linearity ±1/2LSB	Long Term Stability			±0.25%/year						
Temperature Coefficient ±50ppm/°C Encoding Time 40 nsec 100 nsec (2) 100 nsec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datel Systems Ultraminiature DC Power Supplies - Bulletin PSC-37.31) +15VDC, ±0.2VDC @ 80 mA +5VDC, ±0.1VDC @ 050 mA +5VDC, ±0.1VDC @ 050 mA +5VDC, ±0.1VDC @ 050 mA +5VDC, ±0.1VDC @ 150 mA +15VDC, ±0.2VDC @ 90 mA +5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 150 mA PHYSICAL-ENVIRONMENTAL: Operating Temperature Range 0° C to +70° C Storage Temperature Range 0° C to +70° C Storage Temperature Range 0° C to +70° C Storage Temperature Range 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic 0.250" long minimum Size 3''Wx5''Lx1.150''H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number. 2 to the model number. Nodels ADC-UH6B and ADC-UH6B mary at throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH6B and ADC-UH6B mary sense: Note that the m ost nega- tipout o	Resolution		1 LSB (1	160 mV)		1LSB (40 mV)		1 LSB (10 mV)		
Encoding Time 40 nsec 100 nsec (2) 100 nsec (2) Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datel Systems Ultraminiature PC Power Supplies - Bulletin PSC 3-73-1) +15VDC, ±0.2VDC @ 80 mA -15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 150 mA +15VDC, ±0.2VDC @ 9 mA -15VDC, ±0.1VDC @ 170 mA -15VDC, ±0.2VDC @ 9 mA -15VDC, ±0.1VDC @ 170 mA -15VDC, ±0.2VDC @ 9 mA -5VDC, ±0.1VDC @ 170 mA -5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 120 mA PHYSICAL-ENVIRONMENTAL: 0° C to +70° C -5VDC, ±0.1VDC @ 120 mA -5VDC, ±0.1VDC @ 120 mA -5VDC, ±0.1VDC @ 120 mA Operating Temperature Range 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3'Wx5''Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Models ADC-UH6B and ADC-UH6B make a throughput delay of 130 nsec. because of the two stage conversion technique employed.Although th throughput delay is 130 nsee both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more of OUTPUT DATA CODING ADC-UH6B ADC-UH6B Analog ADC-UH6B Straight Binary Analog	Linearity		± 1/:	2LSB		±1/2LSB		±1LSB		
Word Repetition Rate (MAX.) 25 MHz 10 MHz (2) 10 MHz (2) Input Power Requirements (See Datel Systems Ultraminiature DC Power Supplies - Bulletin PSC-3-73-1) +15VDC, ±0.2VDC @ 80 mA +15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 650 mA -5VDC, ±0.1VDC @ 780 mA +5VDC, ±0.1VDC @ 170 mA +15VDC, ±0.2VDC @ 90 +5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 170 mA PHYSICAL-ENVIRONMENTAL: 0° C to +70° C -5VDC, ±0.1VDC @ 170 mA -5VDC, ±0.1VDC @ 170 mA Operating Temperature Range 0° C to +70° C -5VDC, ±0.1VDC @ 170 mA -5VDC, ±0.1VDC @ 250 Relative Humidity Up to 100% NON-CONDENSING -5VDC, ±0.1VDC @ 170 mA -5VDC, ±0.1VDC @ 170 mA Size 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3'Wx5''Lx1.150"H 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data yof 130 nsec, because of the two stage conversion technique employed.Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH88 Straight Binary 1-1.270V Analog Di	Temperature C	Coefficient		±50ppm/°C						
Input Power Requirements (See Datel Systems Ultraminiature DC Power Supplies - Bulletin PSC-373-1) +15VDC, ±0.2VDC @ 80 mA -15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 150 mA -5VDC, ±0.1VDC @ 150 mA -5VDC, ±0.1VDC @ 170 mA +15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 170 mA PHYSICAL-ENVIRONMENTAL: 0°C to +70°C Operating Temperature Range 0°C to +70°C Storage Temperature Range 0°C to +85°C Relative Humidity Up to 100% NON-CONDENSING Case Pins 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3'Wx5''Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Models ADC-UH8B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH8B2 Offset Binary (1) (8-Bit Shown, 4 & 6-Bit available) Input Output ADC-UH48 Straight Binary ADC-UH88 Straight Binary ADC-UH88 Straight Binary Straight Binary Analog Input Output Digital Input Output Analog Input Output Digital Input Output	Encoding Time		40	nsec		100 nsec (2)		100 nsec (2)		
(See Datel Systems Ultraminiature DC Power Supplies - Bulletin -15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 650 mA -5VDC, ±0.1VDC @ 150 mA -15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 780 mA -5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 1300 -15VDC, ±0.2VDC @ 9 mA +5VDC, ±0.1VDC @ 1300 -5VDC, ±0.1VDC @ 1300 PHYSICAL-ENVIRONMENTAL: 0°C to +70°C Operating Temperature Range 0°C to +70°C Relative Humidity Up to 100% NON-CONDENSING Case Pins 0.020″ round gold plated 0.250″ long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3″Wx5″Lx1.150″H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See terming diagram for more d OUTPUT DATA CODING Reverse coding sense: Note that input Output ADC-UH48 Straight Binary ADC-UH48 Straight Binary ADC-UH48 Straight Binary Analog Digital input Output Analog Digital input Anal	Word Repetition Rate (MAX.)		25	MHz		10 MHz (2	2)	10 MH	Hz (2)	
Operating Temperature Range 0° C to +70° C Storage Temperature Range -55° C to +85° C Relative Humidity Up to 100% NON-CONDENSING Case Pins 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3"Wx5"Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number. Models ADC-UH4BB and ADC-UH4BB have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH4B2 Offset Binary (1) (8-Bit Shown. 4 & 6-Bit available) Input Reverse coding sense: Note that the most nega- tive analog input corresponds to -0.640V ADC-UH4B Digital Analog Analog Digital Analog Analog Digital Anal	(See Datel Systems Ultraminiature DC Power Supplies - Bulletin		-15VDC, ±0.2 +5VDC, ±0.1	VDC @ 9 m VDC @ 650 m	9 mA -15VDC, ±0.2VDC @ 9 mA 0 mA +5VDC, ±0.1VDC @ 780 mA					
Storage Temperature Range -55° C to +85° C Relative Humidity Up to 100% NON-CONDENSING Case Pins 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3"Wx5"Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number.)) Models ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec, because of the two stage conversion technique employed.Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH48B 2Offset Binary (1) (8-Bit Shown, 4 & 6-Bit available) Analog Reverse coding sense: Note that the em ost nega- ive analog input corresponds to full scale output ADC-UH4B Straight Binary ADC-UH6B Straight Binary Analog Digital Analog Analog Digital Input Output Input Output <td< td=""><td>PHYSICAL-</td><td>ENVIRONMENTA</td><td>L:</td><td>1.00</td><td></td><td>1.000</td><td>h</td><td></td><td></td></td<>	PHYSICAL-	ENVIRONMENTA	L:	1.00		1.000	h			
Relative Humidity Up to 100% NON-CONDENSING Case Pins 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3"Wx5"Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Nodels ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more di OUTPUT DATA CODING ADC-UH4B2 Offset Binary (1) (8-Bit Shown, 4 & 6-Bit available) Analog Digital Input Output ADC-UH4B Straight Binary ADC-UH6B Straight Binary ADC-UH8B Straight Binary ADC-UH8B Straight Binary Analog Digital Analog Digital Analog Digital Input Output Analog Digital Analog Digital Analog Digital Analog Digital Analog A	Operating Tem	perature Range			Hard	$0^{\circ} C to +70^{\circ}$	°C			
Case Pins 0.020" round gold plated 0.250" long minimum PC Board is covered with an aluminum electrostatic shield and encapsulated. All converters are fully repairable. Size 3"Wx5"Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Models ADC-UH8B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more d OUTPUT DATA CODING ADC-UH4B Straight Binary ADC-UH6B Straight Binary ADC-UH8B Straight Binary ADC-UH8B Straight Binary Analog Digital Digital Analog Digital Analog Di	Storage Tempe	erature Range	-55° C to +85° C							
0.250" long minimum shield and encapsulated. All converters are fully repairable. Size 3"Wx5"Lx1.150"H Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Models ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more de OUTPUT DATA CODING ADC-UH8B2 Offset Binary (1) (8-Bit Available) Reverse coding sense: Note that the m ost negative analog input Output ADC-UH4B ADC-UH6B ADC-UH8B Maiog Digital the m ost negative analog input Output Analog Digital Input Analog Digital Corresponds to full scale output Analog Digital Input Analog Digital Input Analog Digital Input Analog Digital Input Output Input	Relative Humi	dity	and the second		Up to	o 100% NON-CO	NDENSING			
Weight 15 oz. NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number. Models ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more de OUTPUT DATA CODING ADC-UH8B2 Offset Binary (1) (8-Bit Shown. 4 & 6-Bit available) Reverse coding sense: Note that the most negative analog input Output ADC-UH4B Straight Binary ADC-UH6B Straight Binary ADC-UH8B Straight Binary Analog Digital the most negative analog input Output Input Output Input Output Input Output -0.640V 11000000 -1.920V 1100 -1.920V 110000 -1.920V 110000	Case Pins									
NOTES: (1) A Bipolar input (±1.280V) is also available. Output data coding will be "reverse coding sense" (See below). When ordering a Bipolar add the number 2 to the model number.) Models ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more de OUTPUT DATA CODING ADC-UH8B2 Offset Binary (1) (8-Bit Shown. 4 & 6-Bit available) Reverse coding sense: Note that the m ost negative analog input ADC-UH4B ADC-UH6B ADC-UH8B Analog Digital Input Output Input Output </td <td>Size</td> <td></td> <td>A Children</td> <td colspan="7"></td>	Size		A Children							
add the number 2 to the model number. add the number 2 to the model number. Models ADC-UH6B and ADC-UH8B have a throughput delay of 130 nsec. because of the two stage conversion technique employed. Although th throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more description of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more description of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more description of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more description of the two stage conversion technique employed. Although the throughput delay is 130 nsec both models can start a new conversion every 100 nsec, for a word rate of 10 MHz. See timing diagram for more description of the two stage conversion technique employed. Although the two stages conversions to two stages	Weight		15 oz.							
ADC-UH8B2 Offset Binary (1) (8-Bit Shown, 4 & 6-Bit available) Reverse coding sense: Note that Input ADC-UH4B Straight Binary ADC-UH6B Straight Binary ADC-UH6B Straight Binary ADC-UH8B Straight Binary Analog Digital Reverse coding sense: Note that the most nega- tive analog input -0.640V Analog Digital Analog Digital -0.640V 11000000 full scale output 10000 -1.280V 1100 -1.920V 110000 -1.920V 1100000	2) Models ADC- throughput de	dd the number 2 to th UH6B and ADC-UH8 elay is 130 nsec both	ne model number. B have a throughput o	delay of 130 ns	ec. because o	f the two stage c	onversion tec	hnique employed.A	Although the	
(8-Bit Shown. 4 & 6-Bit available) Reverse coding sense: Note that Input Straight Binary Straight Binary Straight Binary Analog Digital sense: Note that the most negative analog input corresponds to full scale output Nalog Digital Analog Digital Nalog Digital Analog Digital Digital Analog Digital Digital Analog Digital Digital Analog Digital Digital <td colspan="2"></td> <td>1 30-10 m</td> <td colspan="2"></td> <td></td> <td></td> <td></td> <td></td>			1 30-10 m							
AnalogDigitalsense: Note that the most nega- tive analog inputAnalogDigitalAnalogDigitalAnalogDigitalInputOutputInputOutputInputOutputInputOutputInputOutput-1.270V1111111corresponds to full scale outputfull scale output1100-1.920V1110-2.550V11111-0.640V11000000full scale output1.280V1000-1.920V1100000-1.920V100000			Reverse coding Straight Bina						-	
Imput Output tive analog input corresponds to full scale output -2.400V 1111 -2.520V 111111 -2.550V 11111 -0.640V 11000000 full scale output -1.920V 1100 -1.920V 110000 -1.920V 110000 -1.920V 110000 -1.920V 110000	-	-	sense: Note that		-		-		Digital	
-1.270V 1111111 corresponds to full scale output 2.300V 1100 -1.920V 110000 -1.920V 110000 -0.640V 11000000 full scale output 1.320V 1100 -1.920V 110000 -1.920V 110000									11111111	
-0.640V 11000000 Tull scale output -1.280V 10000 -1.280V 100000 -1.280V 100000			corresponds to						11000000	
			full scale output (11 1, binary)	-1.280V	1000	-1.280V	100000	-1.280V	10000000	
0.000V 10000000 (11 1, 0101) 00001 00001 000001 000001			(i i i i i, binary)						00000001	
+1.270V 0000001									00000000	



Printed in U.S.A.

 1020 TURNPIKE STREET, CANTON, MASS. 02021
 TEL. (617) 828-8000
 TWX: 710-348-0135
 TELEX: 924461

 COPYRIGHT © 1973, DATEL SYSTEMS INC.
 Bulletin AUHCT 15312

Electronic Design's



GENERAL PURPOSE, ANALOG-TO-DIGITAL CONVERTERS

ADC-MA SERIES

FEATURES

- 10 & 12 Bit Resolution
- Selectable Input Ranges
- 20 & 40 µsec. Conversion Times
- Unipolar or Bipolar Operation
- Input Buffer Option
- Parallel & Serial Outputs
- ADC-MA12B1A & ADC-MA12B2A Are Equivalents to ADC-12QZ

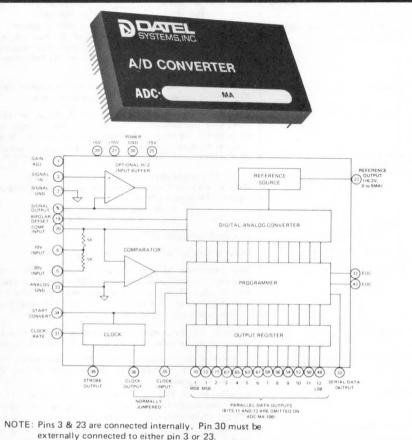
GENERAL DESCRIPTION

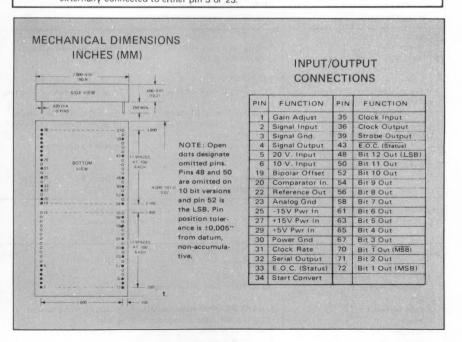
The ADC-MA series A/D converters consist of 10 and 12 bit resolution models with 20 or 40 microsecond conversion times. These units feature high performance and versatility at a low price.

The exceptional versatility of the ADC-MA series is seen in the following features. Single-ended input voltage ranges of 0 to +5V, 0 to +10V, ±5V, and ±10V are pin selectable by the user. In addition, an internal high input impedance buffer amplifier is available as an option. This amplifier gives an input impedance of 1000 megohms on all voltage ranges. Without the amplifier the input impedances are 2.5K, 5K, and 10K ohms on 5V, 10V, and 20V full scale ranges respectively. Digital output data is available in either parallel form or serial NRZ format with synchronizing strobe pulses. Serial data is straight binary for unipolar operation and offset binary for bipolar operation. Parallel data is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. The ADC-MA units can operate either internally or externally clocked. In addition, the internal clock rate can be decreased by use of an external capacitor.

The ADC-MA series uses the successive approximation technique to achieve excellent linearity, speed, and stability. Temperature coefficient is held to ± 30 ppm/°C for gain and ± 5 ppm/°C for offset in unipolar operation. Tight temperature tracking of the weighted current sources results in monotonic operation with no missing codes over the 0°C to 70°C temperature operating range.

These converters are encapsulated in a 4 \times 2 \times 0.4 inch module with DIP compatible .100" pin spacing. Input power requirements are ±15VDC and +5VDC and are available from Datel's line of modular power supplies. All digital inputs and outputs are DTL/TTL compatible.





	ADC-MA10B	ADC-MA12B				
	ADC-IMA TOB	ADC-WATZB				
INPUTS						
Analog Input Range		0 to +10V FS,				
	±5V FS, ±10V FS					
Input Overvoltage	±15V without d	lamage to unit				
Input Impedance						
0 to +5V FS Range	2.5K ohms	2.5K ohms				
±5V and 0 to +10V FS Range	5K ohms	5K ohms				
±10V FS Range	10K ohms	10K ohms				
With Optional Input Buffer	1000 Megohms	1000 Megohms				
Start of Conversion	+2V min. to +5.5V max. pos duration of 100 nsec. min. Rise Three TTL loads. Logic "1" r logic "0" initiates conversion.	e and fall times 500 nsec. max.				
Clock Input	Must be connected to Clock Output to use internal clou Clock Input can also be used with an external clock.					
Clock Rate	Rate is internally set to give m or 40 μ sec. per conversion. Th an external capacitor connec	is time may be increased with ted between pin 31 (Clock				
	Rate) and pin 36 (Clock Out). See conversion time formulas.					
OUTPUTS						
Parallel Output Data	10 Lines of data Data is held until next convers capable of driving 5 TTL loads. V out (Logic ' V out (Logic '	'0'') ≤ +0.4∨				
Unipolar Operation	Straight Binary, positive true.					
Bipolar Operation	Offset Binary or Two's Complement, positive true.					
Serial Output Data	NRZ (nonreturn to zero) successive decision pulse output					
	generated during conversion with MSB first. Serial data straight binary for unipolar operation and offset binary f bipolar operation. Output will drive 10 TTL loads. Two complement is not available with serial output.					
Strobe Output	Available for serial data synchronization. Serial output i usable on strobe pulse leading edges. Will drive 9 TTL loads					
EOC (End of Conversion)	Conversion status output. Logic "0" for conversion com- plete, Logic "1" during reset and conversion period. Will drive 10 TTL loads.					
<u>EOC</u>	Complement of End of Conversion output. Logic "1" to conversion complete and Logic "0" during reset and conver- sion period. Will drive 7 TTL loads.					
Clock Output	Internal clock pulse train outp time.					
Signal Output	Output of optional internal buf	fer amplifier.				
PERFORMANCE						
Resolution	10 Bits (one part in 1024) ±.05% FS ±½LSB	12 Bits (one part in 4096) ±.012%FS ±½LSB				
Linearity	±½LSB	±½LSB				
Temp. Coefficient of Gain	±30 ppm/°C max. of Reading	±30 ppm/°C max. of Reading				
Temp. Coefficient of Zero						
Unipolar	±5 ppm/°C max. of Range	±5 ppm/°C max. of Range				
Bipolar	±10 ppm/°C max. of Range	±10 ppm/°C max. of Range				
Conversion Time, max	20 or 40 µsec.	20 or 40 µsec.				
	(depending on model)	(depending on model)				
Power Supply Sensitivity						
(tracking ±15V supplies)						
Gain	±20 ppm/%	±20 ppm/%				
Zero	±10 ppm/%	±10 ppm/%				
POWER REQUIREMENT (with input buffer amplifier)	+15VDC ±0.5V @ 40mA, max. -15VDC ±0.5V @ 45mA, max. + 5VDC ±0.25V @ 200mA, max.					
PHYSICAL-ENVIRONMENTAL	-9					
Operating Temperature Range	0°C to 70°C					
Storage Temperature Range						
Relative Humidity						
		M 14 apovy apparented				
		g mm.				
-	-					
Mating Sockets (optional)	Dico-2, 4 required.					
	-55° C to +85° C Up to 100% non-condensing 4" x 2" x 0.4" Black Diallyl Phthalate per MIL .020" round, gold plated, .250" 8 oz. (227 grams) DILS-2, 4 required.					

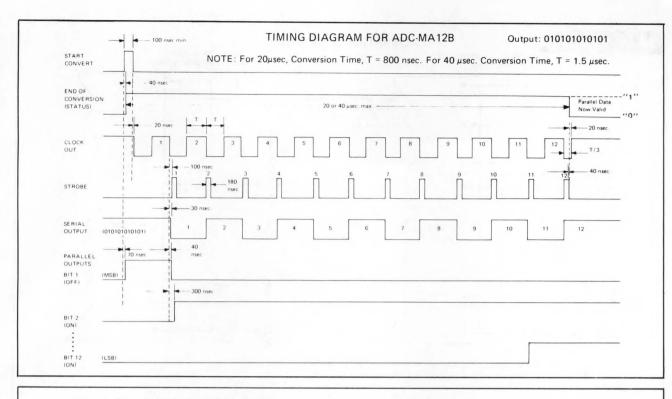
TECHNICAL NOTES

The ADC-MA series contains an internal clock which is set to the maximum conversion rate. This rate may be decreased by connecting an external capacitor between pins 31 and 36. The approximate capacitor value to achieve the desired conversion time is shown in the table at the bottom of the next page. The longer conversion time obtained in this manner does not improve accuracy but it does permit compatibility or synchronization with interfacing equipment for many applications. To use the internal clock a jumper must be connected between pins 35 and 36. For external clocking, which may be desirable in some applications, the jumper is removed and the external clock applied to pin 35. Use a symmetrical 0 to +5V square wave with a minimum 3.0 usec. period for the 40 usec. converters and a minimum 1.6 µsec. period for the 20 µsec. converters. The Start Convert pulse should have a minimum 100 nsec. width and should not be made too long since clocking begins on the falling edge of this pulse and, therefore, its width is part of the total conversion time.

Analog inputs are connected to pin 6 for 10V ranges and pin 5 for the 20V range when the input buffer amplifier is not used. The input impedances in these cases are 5K ohms and 10K ohms respectively. For the 0 to 5V range, pin 5 is connected to pin 20, thus paralleling the two internal 5K resistors to give a 2.5K ohm input impedance at pin 6.

The end of conversion or status pulse is available at pin 33 and its complement EOC is available at pin 43. Normally the EOC output is used to control the mode of the input sample and hold. Serial output data is available at pin 32 in straight binary code for unipolar operation or offset binary for bipolar operation. Nonreturn to zero (NRZ) format is used and the data is valid at the leading edge of the strobe pulse. Parallel data output is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Two's complement is obtained by using the complemented MSB output at pin 70.

DATE



OUTPUT DIGITAL CODING, ADC-MA SERIES

UNIPOLAR INPUT RANGE		STRAIGHT	BIPOLAR INPUT RANGE		OFFSET	TWO'S
0 TO +10V FS	0 TO +5V FS	BINARY MSB LSB	±10V FS	±5V FS	BINARY MSB LSB	COMPLEMENT MSB LSE
+9.9976	+4.9988	111111111111	+9.9951	+4.9976	111111111111	01111111111
+8.7500	+4.3750	111000000000	+7.5000	+3.7500	11100000000	01100000000
+7.5000	+3.7500	11000000000	+5.0000	+2.5000	11000000000	0100000000
+5.0000	+2.5000	10000000000	0.0000	0.0000	10000000000	000000000000
+2.5000	+1.2500	01000000000	- 5.0000	-2.5000	01000000000	11000000000
+1.2500	+0.6250	00100000000	-7.5000	-3.7500	00100000000	10100000000
+0.0024	+0.0012	00000000001	-9.9951	-4.9976	00000000001	10000000000
0.0000	0.0000	000000000000	- 10.0000	- 5.0000	000000000000	10000000000
C-MA10B (10 BI	TS)					and the
+9.9902	+4.9951	1111111111	+9.9805	+4.9902	111111111	0111111111
+8.7500	+4.3750	1110000000	+7.5000	+3.7500	1110000000	0110000000
+7.5000	+3.7500	1100000000	+5.0000	+2.5000	110000000	010000000
+5.0000	+2.5000	100000000	0.0000	0.0000	100000000	0000000000
+2.5000	+1.2500	010000000	- 5.0000	-2.5000	010000000	1100000000
+1.2500	+0.6250	0001000000	- 7.5000	-3.7500	001000000	1010000000
+0.0098	+0.0049	000000001	-9.9805	-4.9902	000000001	100000001
0.0000	0.0000	000000000	- 10.0000	-5.0000	000000000	1000000000

EXTERNAL PIN CONNECTIONS

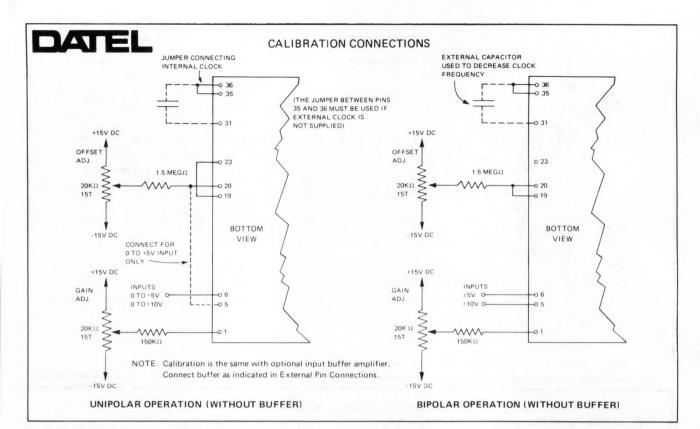
INPUT RANGE (FS)	BUFFER OPTION	TO PIN	JUMPER PIN 4 TO	JUMPER PIN 20 TO	JUMPER PIN 19 TO
0 TO +10V	WITHOUT	6			23
010+100	WITH	2	6	-	23
±5V	WITHOUT	6	_	-	20
IDV	WITH	2	6	-	20
±10V	WITHOUT	5		-	20
TION	WITH	2	5		20
0 TO +5V	WITHOUT	6		5	23
010 +50	WITH	2	6	5	23

CONVERSION TIME USING EXTERNAL CAPACITOR

The external capacitor is connected between pins 31 and 36. Conversion time in the table is in microseconds and capacitor value is in picofarads.

Conv. Time*	ADC-MA10B	ADC-MA12B
20 µsec.	C = 60(T-20µsec.)	C = 50 (T-20µsec.)
40 µsec.	C = 65(T-40µsec.)	C = 55(T-40µsec.)

GOLD BOOK 76/77

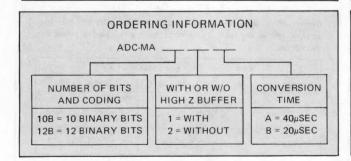


CALIBRATION PROCEDURE

Gain and offset adjustments are accomplished as shown in the above diagram using the Calibration Table. The trimming potentiometers used should be 15 turn 100ppm/°C temperature coefficient cermet type units and are available from Datel Systems at \$3.00 each. A pulse generator should be adjusted to give +5 volt pulses with 100 nsec. minimum duration and a spacing equal to or larger than the specified maximum conversion time (20 or 40 usec.). This generator should be connected to the "Start Convert" input. A precision voltage reference source should be connected to the selected analog input terminal.

Offset Adjustment: For unipolar operation set the output of the voltage reference source to zero plus 1/2 LSB. The value is shown in the Calibration Table. Adjust the offset trimming potentiometer until the LSB output flickers equally between logic "0" and logic "1". (Output between 000...001). For bipolar operation set the voltage reference source to minus full scale plus 1/2 LSB and make the same adjustment.

Gain Adjustment: Adjust the output of the voltage reference source to full scale minus 1 1/2 LSB. This value is also shown in the Calibration Table. Adjust gain trimming potentiometer until LSB output flickers equally between logic "0" and logic "1". (Output between 111...110 and 111...111).



CALIBRATION TABLE ADC-MA SERIES

	UT RANGE	ADJUST-	INPUT V	OLTAGE
INF	UT HANGE	MENT	10 BIT	12 BIT
	0 TO +5V	OFFSET	2.4 mV	0.61 mV
UNIPOLAR	010 +50	GAIN	+4.9927V	+4.9982V
UNIPO	0 TO +10V	OFFSET	4.9 mV	1.2 mV
	010 +100	GAIN	+9.9854V	+9.9963V
BIPOLAR	±5V	OFFSET	-4.9951V	-4.9988V
	130	GAIN	+4.9854V	+4.9963V
		OFFSET	-9.9902V	-9.9976V
	±10V	GAIN	+9.9707V	+9.9927

PRIC	CES (1-9)
------	-------	------

ADC-MA10B2A		\$ 95.00	
ADC-MA10B2B		\$125.00	

ADC-MA12B2A . . \$125.00 ADC-MA12B2B . . \$145.00

For optional internal high impedance buffer amplifier add \$20.00 to price.

Mating Socket: DILS-2, 4 required @ \$5.00 per pair Trimming Potentiometers: TP20K \$3.00 each (1-9)



HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERTER

MODEL ADC-149

FEATURES

- ▶ 14 Bit Resolution
- ▶ 50 µsec. Conversion Time
- ► Low Price-\$279
- Unipolar or Bipolar Inputs
- ▶ 15ppm/°C Gain Temp. Coeff.

GENERAL DESCRIPTION

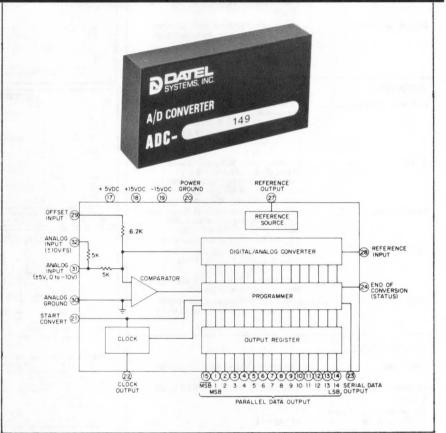
The ADC-149 is a 14 bit successive approximation type analog to digital converter for OEM use. It was specifically designed to give high resolution and accuracy at moderate cost for incorporation into precision instruments for process control systems and test and measurement systems.

This converter accepts either unipolar or bipolar input voltages of 0 to -10V, 0 to -20V, $\pm 5V$, or $\pm 10V$ full scale by external pin connection and performs a 14 bit conversion in 50 μ sec. Several output codes are available including straight binary for unipolar inputs and either offset binary or two's complement for bipolar inputs. Two's complement is obtained by using the MSB output pin. Reverse coding sense is used with the most negative analog input corresponding to full scale digital output. A serial data output is also provided and has a nonreturn-to-zero (NRZ) format. Logic outputs ate DTL/TTL compatible and will drive 6 standard TTL loads.

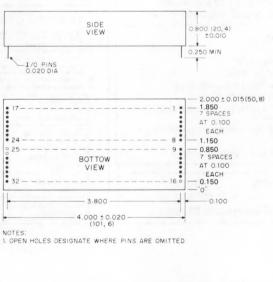
The ADC-149 can resolve 1 part in 16,384 giving an operating dynamic range of 84.3dB. On the 10 volt full scale range it can detect an input change of less than 1 millivolt. Accuracy is adjustable to $\pm.005\%$ of full scale $\pm\%$ LSB. The temperature coefficient is held to a low $\pm15ppm/^{\circ}C$ over the 0° to 70°C operating temperature range.

This converter is encapsulated in a compact $2\times 4\times 0.8$ inch module with DIP compatible pin spacing for PC board mounting. It can be stored from -55° C to $+85^{\circ}$ C. Power supplies required are standard ± 15 VDC and ± 5 VDC. (Available from Datel's line of modular power supplies.)

The high resolution and accuracy of the ADC-149 make it particularly valuable in applications such as moderate speed data reduction, and computer arithmetic processing of analog inputs. Digitizing inputs from sensors and transducers allows data transmission or storage with drastically reduced degradation of accuracy compared to analog methods. This is also vital for automatic process and alarm limit computer control, and digital linearization of logarithmic or special function analog inputs. The ADC-149 offers at least a \$100. price advantage over competitive converters in these applications.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
	BIT 10
11	BIT 11
	BIT 12
13	BIT 13
14	BIT 14 (LSB)
15	BIT 1 (MSB)
16	NOT USED
17	
18	
19	-15V POWER
20	POWER GROUND
21	START CONVERT
22	CLOCK OUTPUT
23	SERIAL OUTPUT
24	END OF CONVERT (STATUS)
25	NOT USED
26	NOT USED
27	REFERENCE OUTPUT
28	REFERENCE INPUT
29	OFFSET INPUT
30	ANALOG GROUND
31	ANALOG IN (0 to +10, ±5V)
32	ANALOG IN (±10V)

SPECIFICATIONS (Typical @ +25°C unless noted)

IN	PU	TS
----	----	----

INPUTS	
Analog Input Range (single-ended input referenced to ground)	. ±5V FS, ±10V FS 0 to -10V FS, 0 to -20V FS
Input Overvoltage	. ±15VDC without damage to unit.
Input Impedance	. 5K Ohms (\pm 5V and 0 to -10V FS range) 10K Ohms (\pm 10V and 0 to -20V FS range)
Start of Conversion	. +2.5V min. to +5.5V max. positive pulse with 150 nsec. min. duration. Loading: 1mA
	Logic "1" resets converter Logic "0" initiates conversion
OUTPUTS	Stand Stand
Parallel Output Data	. 14 parallel lines of data held until the next conversion command. Vout (Logic "0") $\leq +0.4V$ Vout (Logic "1") $\geq +2.4V$ Each output capable of driving up to 6 TTL loads.
Coding	. Straight Binary (Unipolar Input) Offset Binary (Bipolar Input) Two's Complement (Bipolar Input) Pin 15 provides MSB output for this coding. (Reverse coding sense used).
Serial Output	NRZ successive decision pulse output generated during conversion with MSB first. LO = "1", HI = "0"
	Straight binary or offset binary coding
End of Conversion	. Conversion Status Signal Vout (Logic "0") \leq +0.4V conver- sion complete Vout (Logic "1") \geq +2.4V during reset and conversion period.
Clock	. Internal clock output, positive going 3 microsecond pulse. Loading up to

PERFORMANCE

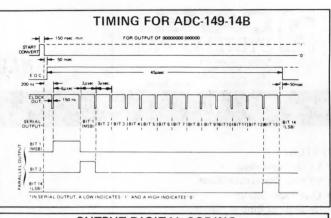
Resolution	One part in 16,384 (max. resolution 14 binary bits)
Accuracy (25°C)	Adjustable to ±.005% of FS ±1/2LSB.
Linearity	±½LSB
Temperature Coefficient of Full Scale	±15ppm/°C
Temperature Coefficient of Zero, Unipolar Bipolar	±10ppm/°C ±10ppm/°C
Conversion Time	50 µsec.
Throughput Rate	20kHz
Power Requirements	±15VDC ±0.5VDC @ 80mA max. +5VDC ±0.25 VDC @ 200mA max.

6 TTL loads.

PHYSICAL-ENVIRONMENTAL

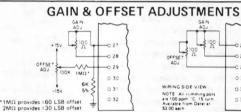
Operating Temperature Range	0° C to +70° C
Storage Temperature Range	-55°C to +85°C
Relative Humidity	Up to 100% non-condensing
Size	2''W×4''L×0.8" H
Pins	.020" round, gold plated, 0.250" long min.
Case Material	Black Diallyl Phthalate per MIL-M-14
Weight	8 oz.
Mating Sockets	DILS-2, 2 required @ \$5/pair.

ORDERING INFORMATION PRICE Model ADC-149-14B \$239. (1-9) Mating Socket DILS-2 (2 per module, \$5./pair)



OUTPUT DIGITAL CODING BIPOLAR UNIPOLAR Anelog

Analog Input Range		Offset Binary		2's Complement (MSB Output)		Input Range 0 to	Straight Binary	
5V FS	10V FS	MSB	LSB	MSB	LSB	10V FS	MSB	LSB
+ 5 0000	+10.0000	00000000	000000	10000000	000000	0 0000	000000000	00000
+ 2.5000	+ 5.0000	01000000	000000	11000000	000000	0 0006	000000000	00001
+0.0006	+ 0.0012	01111111	111111	11111111	111111	2 5000	010000000	00000
0 0000	0.0000	10000000	000000	00000000	000000	5 0000	100000000	00000
-2.5000	- 5.0000	11000000	000000	01000000	000000	-7 5000	110000000	00000
4.9994	85666 6 -	11111111	111111	01111111	111111	-9 9994	111111111	11111



UNIPOLAR

Adjustment Procedure – Unipolar Input A. Connect a precision pulse generator to the "Start Convert" input terminal. See specifications for pulse width and amplitude B. Connect a precision voltage reference source to the appropriate analog input terminals. See L/O Connections.

Zero Offset Control

Adjust the voltage output from the reference to minus % LSB. Rotate the zero offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one"

Full Scale Gain Control

Adjust the output from the reference source to full scale minus 1% LSB. Rotate the gain control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

100 -0 27 100 -0 28 -0 29 0.30 WIRING SIDE VIEW 03 NOTE All trimming pots are 100 ppm ⁻C 15 turn Available from Datel at \$3.00 each 0.32 BIPOLAR

Adjustment Procedure - Bipolar Input

upustment Procedure — Bipplar Input Connect a precision pulse generator to the "Start Convert" input terminals. See specifications for pulse width and amplitude Connect a precision voltage reference source to the appropriate analog input terminals. See I/O connections.

Zero Offset Control

Adjust the voltage output from the reference source to plus full scale minus % LSB Rotate the offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and loac "one".

Gain Control

Gain Control Adjust the output from the reference source to minus full scale minus 1% LSB Rotate the gain control until LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

TRIMMING OF 3 MOST SIGNIFICANT BITS (INTERNAL)

The three trimming potentiometers on the side of the module are for periodic adjustment of the three most significant bits. Normally no adjustment of these trims is necessary since they are calibrated at the factory at 25°C. Should readjustment the required for optimum accuracy sis ad ifferent temperature or to compensate periodically for long term drift, the following procedure should be carefully followed: 1. Adjust external offset and gain as above. 2. Readjust external gain trim and then bits 3, 2, and 1 in accordance with the table below. Adjust so that the output flickers equally between the two codes shown. 3. Readjust external zero offset and gain. 4. Repeat steps 2 and 3 as necessary.

Input Voltage	Langer and the	Output Code	Adjustment
Unipolar (0 to -10V)	Bipolar (±5V)	non na	incomes -
-0.625V -1/2 LSB	+4.375V - 1/2 LSB	0001001	Gain Trim
(-0.62531V)	(+4.37469V)	0001000	
-1.25V - 1/2 LSB	+3.75V -1/2 LSB	0010001	Trim #3
(-1.25031V)	(+3.74969V)	0010000	(Bit 3)
-2.5V -1/2 LSB	+2.50V -1/2 LSB	0100001	Trim #2
(-2.50031V)	(+2.49969V)	0100000	(Bit 2)
-5.0V -1/2 LSB	0V -1/2 LSB	10000 01	Trim #1
(-5.00031V)	(-0.00031V)		(Bit 1)



50 MILLIWATTS TOTAL POWER CONSUMPTION WILL OPERATE FROM 12 VOLT BATTERY ANALOG TO DIGITAL CONVERTER

ADC-CM SERIES

FEATURES

- AUTOMATIC SHUTDOWN BETWEEN CONVERSIONS
- CHOICE OF C/MOS OR TTL OUTPUTS
- UP TO 3000 CONVERSIONS PER SECOND
- ±0.025% ACCURACY
- ▶ FOUR INPUT RANGES

GENERAL DESCRIPTION

The most unique feature of the ADC-CM series analog-to-digital converters is their low power consumption, approximately two orders of magnitude lower than those attainable with conventional A/D converters. ADC-CM series are well adapted for applications in remote areas with limited power. Ideally suited for operation from battery power, they will find wide use in

battery power, they will find wide use in oceanography, pollution monitoring, meterology and seismology. They are also ideal for other scientific uses both in the laboratory and in the field.

Power consumption is a function of the conversion rate. For 100, 500 and 1000 conversions per second, the average power drain is approximately 5, 25, and 50 milliwatts, respectively.

Model ADC-CM converters have the capability of operating from either a single +12VDC to +15VDC power source (interrupt power mode) or from a ±12VDC to ±15VDC power supply (continuous power mode) at a maximum conversion rate of 3KHz.

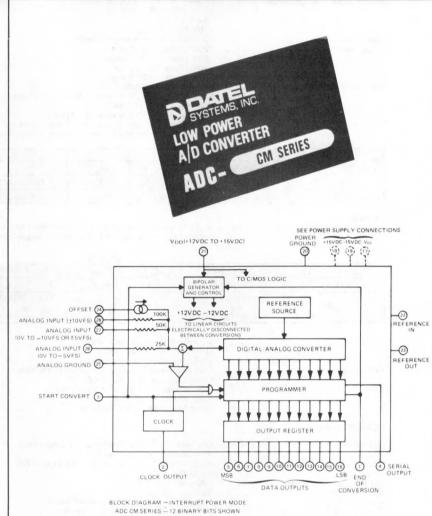
Another key feature of the ADC-CM series when operating in the interrupt power mode is its ability to normally reset in a standby state (power turned off to the analog section) and upon receipt of a convert command signal the converter will turn on, stabilize in 50 microseconds, make a complete conversion and automatically return to standby status.

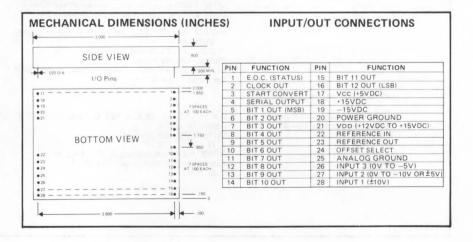
All input/output control signals and output data are C/MOS compatible plus a separate logic power supply connection (+VDC-Pin 17) is provided to allow the user the convenience of TTL compatibility when required.

The ADC-CM series converters utilize C/MOS logic throughput and employ the inherently accurate successive approximation conversion method to compare an unknown analog input signal against the output of a precision digital-to-analog converter in a high gain feedback loop. This method insures a full monotonic conversion and excellent linearity over the full scale input voltage range.

Full scale input can be unipolar (0 to -5V or 0 to -10V) or bipolar (±5V or ±10V) by simply making the appropriate pin connections.

The entire converter is contained in a 2"W x 3"L x 0.8"H plastic encapsulated module, yet fully repairable – a very significant consideration. Full scale accuracy is specified at $\pm 0.025\%$ with a temperature coefficient of ± 30 ppm/°C.







SPECIFICATIONS (Typical @ 25°C unless noted)

ELECTRICAL

Inputs:	
Analog Input Voltage Range	0V to - 5V FS - PIN 26
	0V to -10V FS - PIN 27
	±5V FS – PIN 27
	±10V FS – PIN 28
Input Overvoltage	±30VDC without damage to unit
Input Impedance	
	50K Ohms, -10V Range
	50K Ohms, ±5V Range
	100K Ohms, ±10V Range
Start of Conversion	Interrupt Power Mode
	Positive Pusle With Duration of 50 μ sec, ±10 μ sec.
	Continuous Power Mode
	Positive Pulse With Duration of 10 μ sec.
	Note: For either mode, the leading edge resets the converter and the trailing edge initiates a conversion. Pulse amplitude is determined by power supply used as shown below.

and the second second	PIN 17			
COMPATIBILITY	POWER SUPPLY	LOGIC "0"	LOGIC "1"	LOAD
TTL	+5VDC	≤ +0.4V	≥+2.4V	1 TTL Load. Terminate Pin 3 to Pin 17 with 4.7K
C/MOS	+12VDC to +15VDC	0V	VDD	Input Impedance 20K to Ground

Outputs: Parallel Output Data. .

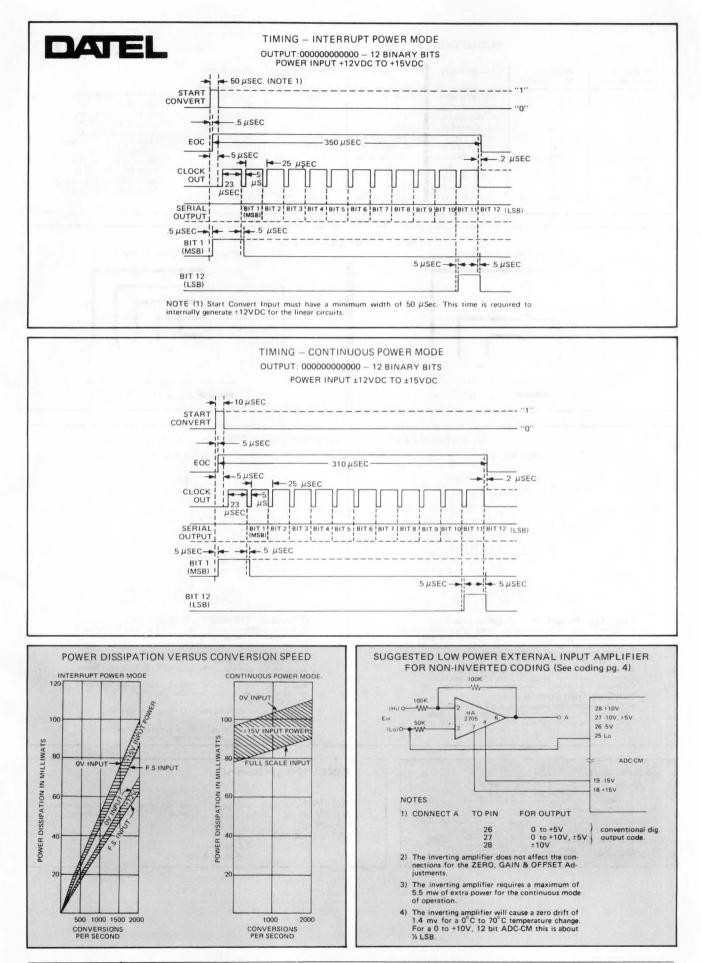
Up to 12 parallel lines of data held until next conversion command. Output logic levels determined by power supply used, as per Table 'A'.

			TABLE 'A'	the second second second second
COMPATIBILITY	POWER SUPPLY	LOGIC "0"	LOGIC "1"	FAN OUT
TTL	+5VDC	≤ +0.4V	≥+2.4V	2 TTL Loads
C/MQS	+12 VDC to +15VDC	0V	VDD	Output Impedance V out Low – 100 Ohms V out High – 1.5K

Coding	
	Offset Binary (Bipolar Input 2's Complement (Bipolar Input)
End of Conversion	Conversion status signal high during conversion.
	Output logic levels – See Table 'A'
Clock	Internal clock out. Positive pulse train.
	Pulse width: 20 µsec.
	Pulse Amplitude – See Table 'A'

PERFORMANCE:

Resolution	One part in 2 ⁿ (max. resolution 12 binary bits) (n = Number of Binary Bits)
Accuracy	±0.025% of FS ± ½ LSB (Externally adjustable)
Linearity	
Temperature Coefficient	
Encoding Time	
	10 μ sec for a full scale step at the input.
Throughput Time	
	350 µsec – interrupt power mode
Word Rate	
	Up to 2.8KHz – interrupt power mode (12-bit)
Input Power Requirements	Continuous power mode:
	+12VDC to +15VDC See power curves next page
	-12VDC to -15VDC
	+5VDC for TTL Compatibility
	Interrupt power mode:
	+12VDC to +15VDC - See power curves next page
	See Input Power Connections
PHYSICAL-ENVIRONMENTAL	
	0° C to +70° C (-25° C to +85° C – add Suffix "EX" to Part Number)
Storage Temperature Range	
Relative Humidity	
Size	
	0.020" round gold plated, 0.250" long min.
Case Material	
Weight	8 oz. Max.



GOLD BOOK 76/77

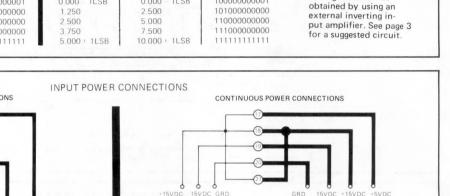
See inside back cover for DATEL sales offices

OUTPUT DIGITAL CODING *



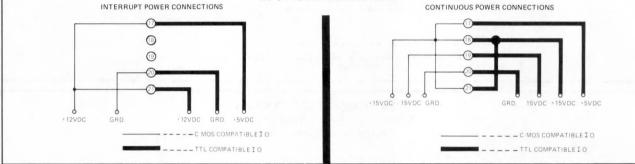
* Reverse coding sense: Note that the most negative analog input corresponds to full scale digital output (11 - 1 binary). Normal coding sense can be

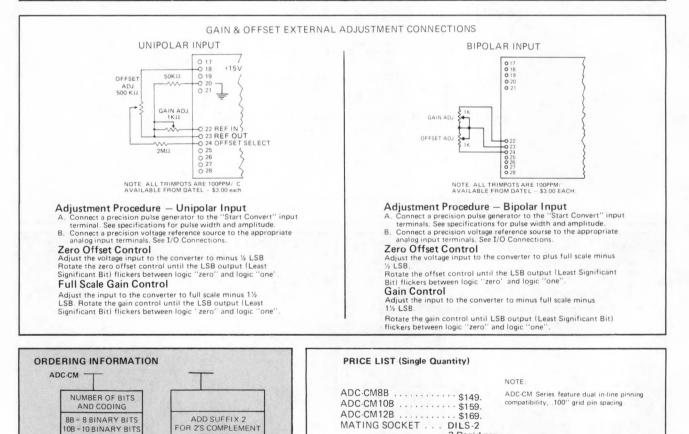
Analog Input OV to -5VFS	Analog Input 0V to -10VFS	Straight Binary	Analog Input ±5VFS	Analog Input ±10V	Offset Binary
0.000	0.000	000000000000	+5.000	+ 10.000	000000000000000000000000000000000000000
0.625	-1.250	001000000000	+3.750	+7.500	00100000000
1.250	-2.500	01000000000	12.500	+5.000	01000000000
1.875	-3.750	011000000000	1.250	+2.500	01100000000
2.500 + 1LSB	-5.000 + 1LSB	0111111111111	0.000 + 1LSE	0.000 + 1LSB	0111111111111
2 500	-5.000	10000000000	0.000	0.000	100000000000
2 500 - 1LSB	-5.000 - 1LSB	100000000001	0.000 1LSB	0.000 - 1LSB	10000000001
3.125	-6.250	101000000000	1.250	2.500	10100000000
3.750	-7.500	110000000000	2.500	5.000	11000000000
4.375	-8.750	111000000000	3.750	7.500	11100000000
5.000 + 1LSB	10.000 + 1LSB	1111111111111	5.000 + 1LSB	10.000 + 1LSB	11111111111111



2 Req'd per

module, \$5/pr





12B=12 BINARY BITS

OUTPUT CODING

Electronic Design's



RATIOMETRIC DUAL SLOPE ANALOG TO DIGITAL CONVERTERS

ADC-ER SERIES

FEATURES

- 4 Wire Ratiometric Operation
- ▶ Single +5V Power Requirement
- Differential Inputs
- 40 dB Normal Mode Noise Rejection
- ▶ 70 dB Common Mode Rejection
- ▶ Binary or BCD Coding

GENERAL DESCRIPTION

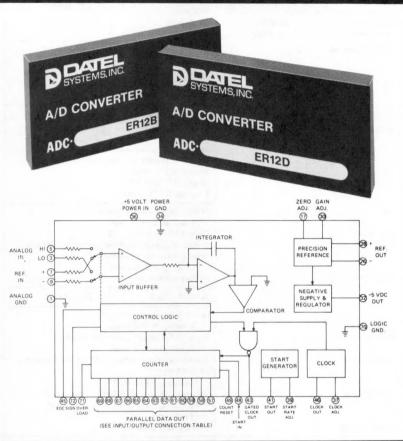
The ADC-ER series dual slope A/D converters feature ratiometric operation powered by a single \pm 5 volt logic supply. Fourwire differential inputs give high common mode rejection with the useful capability of operating with input signal and external reference at different common mode levels; the external reference voltage can be varied over \pm 50% of nominal reference value. In addition, the conversion time can be externally adjusted to a 50 or 60 Hz period to give 40 dB minimum normal mode rejection of AC power line noise.

This series is available in 5 different models with resolutions of 8, 10, or 12 binary bits and sign and 2-1/2 or 3-1/2 BCD digits and sign. Important applications for these converters include test and instrumentation systems and signal conversion at transducer locations. Other operating features include: a gated clock output with a counter reset pulse for transmitting data to an external counter; an internal start pulse generator with externally adjustable rate; and a -5VDC power output supplying up to 5mA for externally powering a transducer bridge or auxiliary amplifier.

This combination of features makes the ADC-ER an extremely versatile A/D converter for systems applications. It contains an internal precision reference of 1V for binary models and 2V for BCD models which is used for normal, non-ratiometric operation. In ratiometric operation the input switches between input signal and external reference during the conversion cycle. Full scale input signal is $\pm 1V$ for binary and $\pm 2V$ for BCD; the input common mode voltage range is $\pm 3V$.

The external reference voltage range is 0.5 to 1.5V for binary models and 1 to 3V for BCD models. Common mode rejection for both signal and reference inputs is 70 dB minimum. Optimum normal mode AC line noise rejection is achieved by external adjustment of the clock frequency to synchronize the signal integration time to either 50 Hz or 60 Hz line period. Sign-magnitude coding is used in all models.

Input power requirement is +5VDC at 250mA maximum and the module size is a low profile 4 x 2 x 0.4 inches.



MECHANICAL DIMENSIONS INPUT/OUTPUT CONNECTIONS INCHES (MM) DIGITAL OUTPUTS PIN FUNCTION PIN BINARY BIT BCDDIGIT 1 ANALOG GROUND 2.000 8B 10B 12B 8D 12D 3 ANALOG IN, LO 400 (10. A 57 X X X 58 X X 12 59 X X 11 SIDE VIE ANALOG IN, HI + REFERENCE IN X X T 020 DIA (0, 5 T REFERENCE IN X 4 60 X 10 10 X ZERO ADJUST 37 e 39 e 3.800 -REFERENCE OUT 61 X 9 9 1 10 26 +REFERENCE OUT 62 8 8 8 20 2 410 430 4 40 30 GAIN ADJ. 63 7 7 7 SPACES AT 100 EACH 45 **•** 46 **•** 80 -5VDC OUT 64 6 6 6 8 32 POWER GROUND 65 5 5 5 10 100 48. 34 4 20 200 +5V POWER IN 66 4 4 36 3 40 400 3 67 3 37 CLOCK ADJUST 540 2 100 2 2 80 800 START RATE ADJ. 68 39 -55 Q 57 018 T 41 START OUT 69 1 1 1 100 1000 43 GATED CLOCK OUT 45 E.O.C. (STATUS) 46 CLOCK OUT X INDICATES NO PIN START CONVERT 48 49 COUNTER RESET 12 70 LOGIC GROUND OVERLOAD 1 800 -- 100 72 SIGN Notes: 1. Open dots designate omitted pins 0.100 inch = 2.5mm 2 3. Pin position tolerance is ±0.005" from datum, non-accumulative 4. Analog Ground, Power Ground, and Logic Ground are all connected together internally.

SPECIFICATIONS, ADC-ER SERIES

	ADC-ER8B/10B/12B	ADC-ER8D/12D	
INPUTS	(BINARY)	(BCD)	
Analog Input Range	±1V	±2V	
Reference Input Range	+0.5 to +1.5V	+1 to +3V	
Input Overvoltage, no damage	±20V	•	
Input Impedance, both inputs	100 Meg. min.		
Input Bias Current, both inputs	45nA typ., 500 nA max.		
Common Mode Input Range	±3V min.		
Common Mode Rejection, DC-60Hz	70 dB min.		
Normal Mode Rejection, 50 or 60Hz	40 dB min.	-	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 μsec. min. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load		
OUTPUTS	and a second and a second	2.000	
Parallel Output Data	8/10/12 parallel lines	8/12 parallel lines and overrange	
	0		
	Output data held until ne Vout ("0") ≤ +0.4V	xt start convert puise.	
Contraction of the second second	Vout ("1") ≥ +2.4V		
and the second sec	Loading: 6 TTL loads		
Sign	Output HI for positive in		
	Loading: 10 TTL load		
Overload	Output HI for ± input > 1		
E.O.C. (Status)	Output HI during reset an		
	when conversion is compl Loading: 4 TTL loads		
Gated Clock	Output pulse train giving:		
	N+4096 pulses	N+2000 pulses	
	where N is converted cou		
	Loading: 8 TTL loads		
Counter Reset	Pulse HI for resetting ext Loading: 4 TTL loads		
Clock Output	Continuous clock pulses		
	of 100 kHz		
	Loading: 1 TTL load		
Start Output	Internally generated 100	nsec. start convert	
	pulse at 2/sec. Can be ext	ernally adjusted	
Persona Octobert	for faster rate. -5VDC ±5% @ 5mA max		
Power Output			
PERFORMANCE	050/ B		
Error, max	.05% Reading ±1 count 8/10/12 Bits	21/2/31/2 Digits	
Coding	Sign-Mag. Binary	Sign-Mag. BCD	
Temp. Coeff. of Gain, converter	±5ppm/°C max.	*	
Temp. Coeff. of Gain, reference	±30ppm/°C max.	*	
Temp. Coeff. of Zero	\pm 30 μ V/°C max.		
Internal Reference	1V ±0.1%	2V ±0.1%	
Power Supply Rejection	.01%/% max.	12.2	
Conversion Time, 60Hz period 50Hz period	76.6 msec. max. 90.0 msec. max.	43.3 msec. max. 50.0 msec. max.	
Warm Up Time	5 minutes	*	
POWER REQUIREMENT	+5.0VDC ±5% @ 250mA	max.	
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range	0°C to 70°C		
Storage Temperature Range	-55°C to +85°C		
	Up to 100% non-condens	ing	
Relative Humidity			
Relative Humidity	4 × 2 × 0.4 inches (101,6	6 × 50,8 × 10,2 mm)	
Case Size	4 × 2 × 0.4 inches (101,6	r MIL-M-14	

TECHNICAL NOTES

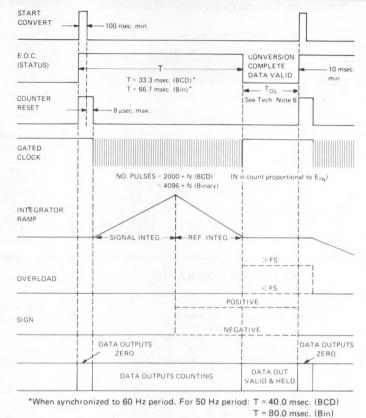
- 1. Both analog input signal and external reference look into identical differential inputs with an electronic switch switching between the two during the conversion cycle. A bias current of typically 45nA flows out of the input terminals and must be returned to ground. For single-ended operation Analog LO and either reference input should be connected to Analog Ground. Only one reference is required for either polarity of analog input.
- 2. Zero adjustment is required for either ratiometric or normal operation, but the gain adjustment is required only for normal operation (using internal reference) or applications where the internally trimmed accuracy of 0.1% is insufficient.
- 3. Optimum normal mode noise rejection for AC line frequencies is obtained by externally adjusting the clock frequency to give a signal integration time equal to the line frequency period of 50 or 60 Hz. This is most easily done by using a digital counter connected to the Clock Output (pin 46). If normal mode noise is negligible or of high frequency, the adjustment is not necessary. For short term measurements an adjustment to within 0.1% of line period can be achieved, resulting in 60 dB of rejection. For longer term measurements, both line frequency and clock frequency drift slightly and a more reasonable match to within 1% results in 40 dB rejection.
- 4. The start rate adjustment allows operating at an internally set rate of 2 conversions/sec. or at faster rates up to 23/sec.

	ADC-ER
	NO. OF BITS & CODING
	8B = 8 Binary Bits
	10B = 10 Binary Bits
	12B = 12 Binary Bits
	8D = 21/2 BCD Digits
	12D = 3½ BCD Digits
	PRICES (1-9)
	ADC-ER88\$79.00
	ADC-ER10B \$89.00
	ADC-ER12B \$99.00
	ADC-ER8D \$79.00
	ADC-ER12D \$99.00
	kets: DILS-2 (4/module) \$5.00/pair
Trimming I	Potentiometers:
	TP100K, TP10K at \$3.00 each
For extend	ded temperature range operation, the
following s	uffixes are added to the model number.
Consult fac	tory for pricing and delivery.
-EX	-25° to +85°C operation
-EXX-HS	-55°C to +85°C operation with her-
	metically sealed semiconductor com-
	ponents.
The ADC-E	R Series Converters are covered by GSA
Contract	

TECHNICAL NOTES (Cont'd)

(BCD) or 13/sec. (Binary) by external adjustment. To operate with the internal start convert, pin 41 must be connected to pin 48. The converter may also be started externally by means of a 100 nsec. min. start convert pulse applied directly to pin 48.

- 5. The -5V power output from the converter may be used to power a transducer bridge or an auxiliary input amplifier such as µA776, LM308, or 4250 in conjunction with the +5V input power. The 5mA maximum output should not be exceeded or it will affect the operation of the converter. This output is short circuit protected to ground but should not under any circumstance be connected to +5V or any other power supply output voltage since damage to the converter will result. The -5V output is regulated to give a constant 10V difference with respect to the +5V power input with a typical tempco of ±100ppm/°C.
- 6. Analog inputs exceeding the ±5V supply voltage, although they will not cause any damage up to ±20V, will cause the input switch to malfunction. This will cause the overload output to remain high and the sign output may be invalid. If inputs exceeding ±5V are to be encountered in an application, it is recommended that clamping diodes be used from the inputs to ±5V. Overload recovery time, T_{OL}, after a ±5V input overload is 30 msec. for all BCD models and 50 msec. for all binary models. See timing diagram.



CODING TABLES

	ווטנ		

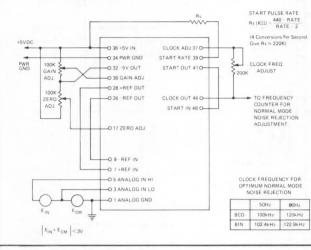
SCALE	21/	2 DIGIT	3	1/2 DIGIT
JUALE	INPUT (±)	OUTPUTCODE	INPUT (±)	OUTPUT CODE
FS-1 LSD	1.99V	1 1001 1001	1.999V	1 1001 1001 1001
3/4 FS	1.50V	1 0101 0000	1.500V	1 0101 0000 0000
1/2 FS	1.00V	1 0000 0000	1.000V	1 0000 0000 0000
1/2 FS-1 LSD	0.99V	0 1001 1001	0.999V	0 1001 1001 1001
1/4 FS	0.50V	0 0101 0000	0.500V	0 0101 0000 0000
1 LSD	0.01V	0 0000 0001	0.001V	0 0000 0000 0001
0	0.00V	0 0000 0000	0.000V	0 0000 0000 0000

BINARY CODING

COALE	81	BIT	1	OBIT	and a start of the start of the	12 BIT
SCALE	INPUT (±)	CODE	INPUT (±)	CODE	INPUT (±)	CODE
FS-1 LSB	.996V	1111 1111	.9990V	1111 1111 11	.99976V	1111 1111 1111
7/8 FS	.875V	1110 0000	.8750V	1110 0000 00	.87500V	1110 0000 0000
3/4 FS	.750V	1100 0000	.7500V	1100 0000 00	.75000V	1100 0000 0000
1/2 FS	.500V	1000 0000	.5000V	1000 0000 00	.50000V	1000 0000 0000
1/4 FS	.250V	0100 0000	.2500V	0100 0000 00	.25000V	0100 0000 0000
1/8 FS	.125V	0010 0000	.1250V	0010 0000 00	.12500V	0010 0000 0000
1 LSB	.004V	0000 0001	.0010V	0000 0000 01	.00024V	0000 0000 0001
0	.000V	0000 0000	.0000V	0000 0000 00	V00000.	0000 0000 0000

CALIBRATION & APPLICATION

STANDARD CONNECTIONS AND CALIBRATION



RATIOMETRIC OPERATION

CALIBRATION

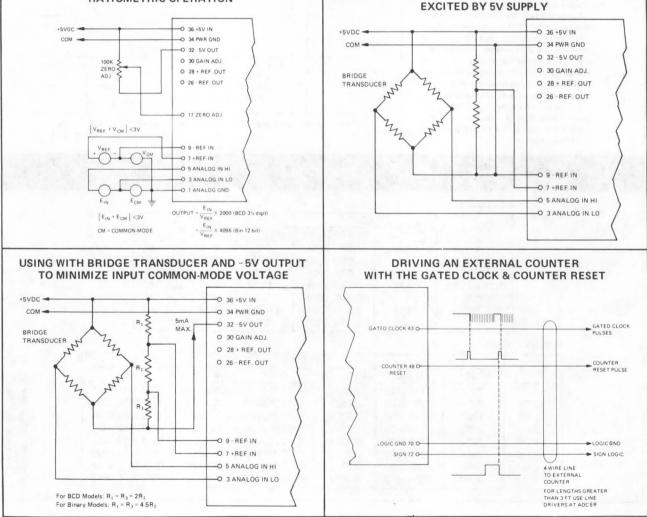
- Connect the converter as shown in the diagram. Allow a 5 minute warm-up before making final adjustments.
- Zero Adjustment. Short together Analog In HI (pin 5), Analog In LO (pin 3), and Analog Ground (pin 1). Adjust zero trimming potentiometer to obtain a flickering Sign (pin 72) and logic zero on all parallel data output lines.
- 3. Gain Adjustment. Apply a precision reference input voltage between Analog In HI (pin 5) and Analog In LO (pin 3) with the latter connected to Analog Ground (pin 1). Set the precision reference to a voltage near full scale (see coding tables) and adjust the gain trimming potentiometer to give the correct digital output code.

NOTE: The gain adjustment is internally trimmed to within $\pm 0.1\%$ accuracy. If this accuracy is sufficient, then pin 30 should be left open. The gain adjustment is not necessary for ratiometric operation.

ADJUSTMENT OF CLOCK FREQUENCY AND START RATE

- To obtain optimum normal mode noise rejection at either 50 or 60 Hz, the Clock Frequency Adjust potentiometer should be adjusted to give the appropriate clock frequency shown in the table. This is most easily done using a frequency counter connected to the Clock Out (pin 46). Although a 200K adjustment potentiometer gives a full range of adjustment, most accurate adjustment is achieved by a 10K trimming potentiometer in series with an appropriate fixed resistor value.
- 2. The internal start pulse generator operates at a nominal rate of 2 pulses/second with no connection to pin 39. To increase the conversion rate a resistor may be connected as shown from pin 39 to +5V as illustrated in the calibration diagram.

USING WITH BRIDGE TRANSDUCER





PRECISION RATIOMETRIC DUAL SLOPE ANALOG TO DIGITAL CONVERTERS

ADC-EP SERIES

FEATURES

- ▶ 4½ Digit BCD or 14 Bit Binary
- 4 Wire Ratiometric Operation
- Auto-Zero Drift Correction
- Quartz Crystal Controlled Clock
- ► Floated Input, ±300V Range
- ► 60dB AC Line Noise Rejection

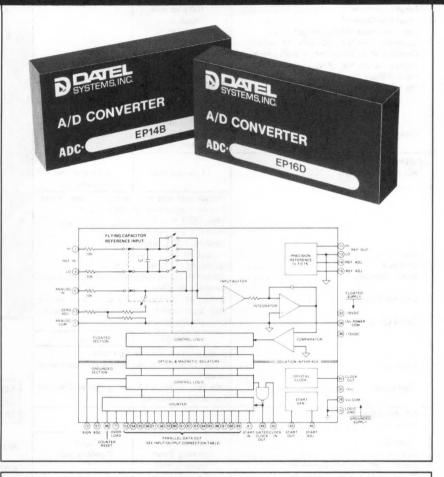
GENERAL DESCRIPTION

The ADC-EP series are high resolution, ratiometric A/D converters using the dual slope conversion principle. The analog input is electrically floated from digital ground by means of optical and magnetic coupling of digital signals, to permit a ±300V common mode input voltage range with greater than 100dB common mode rejection. A four-wire ratiometric input permits separate connection to input signal and reference; the reference input is a flying capacitor circuit which allows the reference to operate at a different common mode level from the input signal, with greater than 70dB common mode rejection. The external reference may vary ±50% from the nominal value of 1.0 volt for ratiometric measurements; a stable internal reference of 1.00V ±0.1% is also provided for fixed reference operation.

These converters are available in two basic models: a binary coded version with 14 bit resolution, and a BCD coded version with 41/2 digit resolution. Both models use signmagnitude coding. An internal quartz crystal controlled clock sets the signal integration time to a precise multiple of the AC line frequency to achieve greater than 60dB noise rejection of AC line noise. The converters can be ordered with clock frequency synchronized to either 50 or 60 Hz. An auto-zeroing circuit stabilizes the zero drift of the converters to less than $\pm 1\mu V/^{\circ}C$. The conversion time, which includes an 80 msec. period for auto-zeroing, is 230 msec. for a 60Hz synchronized model and 260 msec. for a 50Hz synchronized model. Conversion can be initiated by either an external start pulse or by an internally generated pulse. Accuracy of both converters is .01% of reading ±1 count.

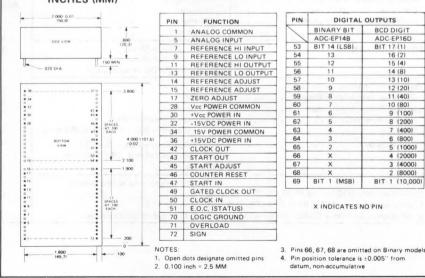
All digital outputs are from a CD4050 buffer, which will drive 1 TTL load or numerous CMOS loads. Other digital outputs include overrange on the BCD model, overload, sign, clock out, start out, and end of conversion (status). Two additional outputs, a gated clock and counter reset, permit serial transmission of output data to an external counter.

The unique features of these converters make them useful in a wide range of instrumentation and measurement applications. Power requirements are ± 15 VDC and +5V to +15VDC. Package size is $4 \times 2 \times 0.8$ inches and operating temperature range is 0° C to 70° C.



MECHANICAL DIMENSIONS INCHES (MM)

INPUT/OUTPUT CONNECTIONS



GOLD BOOK 76/77

SPECIFICATIONS, ADC-EP SERIES

	ADC-EP14B (Binary)	ADC-EP16D (BCD)	
INPUTS			
Analog Input Range	±2V		
Reference Input Range	0.5 to 2.0V		
Input Overvoltage, no damage ¹	±25V		
Input Impedance ¹	100 Meg. min.		
Input Bias Current ¹	100pA max. ±300V max.	*	
Common Mode Voltage Range	100dB min.	*	
Common Mode Range, ref. to analog com	±5V		
Common Mode Rej. of Reference, DC-60Hz.	70dB min.	· · · · · · · · · · · · · · · · · · ·	
Normal Mode Rej., 50 or 60 Hz	60dB min.	*	
Start Conversion	CMOS input, positive 0 t 1 µsec min. duration. 100 Logic "1" resets converte Logic "0" initiates conve CMOS input, positive 0 t approx. 50% duty cycle.	DK input impedance. r. rsion.	
OUTPUTS ³ Parallel Output Data	14 parallel lines	16 parallel lines and overrange	
	Output data held until n Positive true buffered CM Vout ("0") \leq +0.4V Vout ("1") \geq +2.5V	ext start convert pulse	
	Loading: 1 TTL load.		
Sign	Output HI for + inputs		
E.O.C. (Status)	Output HI for ± input > Output HI during conver		
	version is complete.		
Counter Reset	Output HI during and up to 1 clock period		
	after start pulse for resetting external counter.		
Gated Clock	Output pulse train of		
	N+8,192	N+10,000	
Clock	pulses where N is convert Continuous clock pulses clock.		
Start Output	Internally generated 1 µ for starting converter.	sec. pulses at 2/second	
PERFORMANCE			
Error, max	.01% Reading	1±1 count	
Resolution	14 Bits Sign-Mag. Binary	4½ Digits Sign-Mag. BCD	
Temp. Coeff. of Gain, Converter	±5ppm/°C max.	*	
Temp. Coeff. of Gain, Reference	±8 ppm/°C max.	*	
Temp. Coeff. of Zero	±1 μV/°C max. 1.00V ±0.1%	*	
Conversion Time, 60Hz period	230 msec.	*	
Conversion Time, 50Hz period	260 msec.	*	
Warm-Up Time	15 minutes	*	
POWER REQUIREMENT	+15VDC ±0.5V at 45 m -15VDC ±0.5V at 20 m +5VDC to +15VDC (Vc	A	
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range	0°C to 70°C		
Storage Temperature Range	-55°C to +85°C	sing	
Relative Humidity	Up to 100% non-conden $2 \times 4 \times 0.8$ inches (50,8	The second se	
	Black diallyl phthalate p		
Case Material			
Case Material	1.020" round aold plated		
Case Material	.020" round, gold plated 8 oz. max. (227 g)	, the long linit.	

3. All outputs are from a CD4050 buffer which can drive 1 TTL load or CMOS circuits.

TECHNICAL NOTES

- 1. In order to make use of the floated analog input capability of the ADC-EP series, the ±15VDC analog power supply must be floated with respect to the digital logic supply (Vcc). If floated analog input is not required, then analog and digital grounds may be connected together. The analog input is single-ended with 100 megohm input impedance. The input bias current between ANALOG IN and ANALOG COM-MON is 100 pA max. and this value doubles every 10°C.
- 2. The reference input is a flying capacitor circuit which permits the external reference to operate at a ±5V common mode voltage with respect to analog common with greater than 70dB CMR. The 1µF flying capacitor is charged from two 10K resistors which give a time constant of 20 msec. (not counting reference source impedance). This means that if the external reference changes value, 9 time constants or 180 msec. should be allowed before a correct conversion can be initiated. Or, more simply, after the reference changes to a new value approximately one full conversion period should be allowed before the next correct conversion. It should be noted that only one reference is required

trolled	ADC-EP	
second	NO. OF BITS & CODING	NOISE REJ. FREQ.
	14B = 14 Binary Bits	5 = 50Hz
	16D = 4½ BCD Digits	6 = 60Hz
CD	PRICES (1-9)	
	ADC-EP16D-5\$	179.00
(Logie		179.00
111	ADC-EP14B-5 \$	
	ADC-EP14B-6 \$	179.00
	Mating Sockets: DILS-2 (4/ Trimming Potentiometers: TP200, TP100K at \$	
	For extended temperature r following suffixes are added Consult factory for pricing a	to the model number.
mm)	-EX –25° to +85° C op -EXX-HS –55° C to +85° C o metically seaied s ponents.	
	The ADC-EP Series Convert Contract	ers are covered by GSA

ORDERING INFORMATION

TECHNICAL NOTES (cont'd)

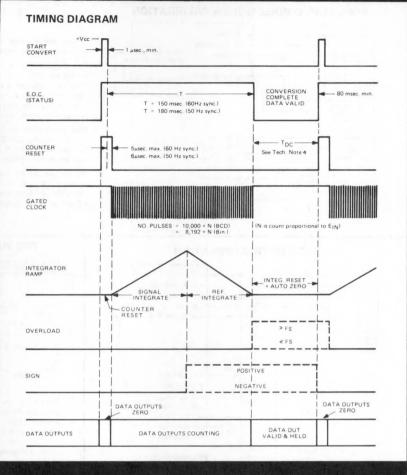
PERFORMANCE DATA

for either polarity of analog input. The polarity of the analog input is automatically sensed by the converter.

- 3. Both ADC-EP models are internally calibrated to within ±2 LSB's at zero and ±0.1% at full scale. If this accuracy is sufficient in an application, no external adjustments are required. The internal 1.0 volt reference may also be used as a reference for other A/D converters or other circuits provided that its output is buffered with a voltage follower op amp of sufficient stability. Temperature coefficient of this reference is only ±8 ppm/^oC and output impedance is 1.3K ohms.
- 4. For both models 80 milliseconds of the total conversion time is devoted to drift correction (auto-zeroing) before the next conversion cycle begins. A full scale input will be converted with parallel data ready in either 150 msec. (60Hz synchr.) or 180 msec. (50Hz synchr.) The E.O.C. (status) output changes state at this time, indicating that data is ready. The next conversion, however, should not be initiated until the 80 msec. auto-zero is completed. For inputs less than full scale, the output data is ready even sooner than 150 or 180 msec.
- 5. The converters can be operated with the internal start generator at 2 conversions/ second or they can be started with an external start pulse at 3.8 conversions/sec. (50 Hz models) or 4.3 conversions/sec. (60 Hz models). The internal start pulse generator can also be slowed to less than 2 pulses/sec. by means of an external capacitor as shown in the application diagram.
- The GATED CLOCK OUT and COUNT-ER RESET are convenient outputs for use with an external or remote counter in applications where serial data transmission is required.
- 7. An external clock may also be used with the ADC-EP converters by providing an input pulse train from OV to +Vcc at approximately 50% duty cycle. For proper operation, the external clock frequency should be within ±10% of the internal crystal clock frequencies which are given here:

	50 Hz Sync.	60 Hz Sync.
BCD	166.66kHz	200.00kHz
Bin	136.53kHz	163.84kHz

8. The excellent normal mode rejection of AC power line frequency noise of the converters is due to the accurate and stable synchronization of the signal integration part of the conversion cycle with the line frequency. This synchronization is held to within 0.1% by the quartz crystal controlled clock. The correct model should be specified for operation with the appropriate AC line frequency.



CODING TABLES

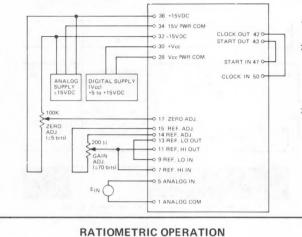
COALE		41/2 [DIGIT			
SCALE	INPUT (±)) OUTPUT CODE				E
FS-1LSB	1.9999V	1	1001	1001	1001	1001
3/4 FS	1.5000V	1	0101	0000	0000	0000
1/2 FS	1.0000V	1	0000	0000	0000	0000
1/2 FS-1LSB	0.9999V	0	1001	1001	1001	1001
1/4 FS	0.5000V	0	0101	0000	0000	0000
1 LSB	0.0001V	0	0000	0000	0000	0001
0	0.0000V	0	0000	0000	0000	0000

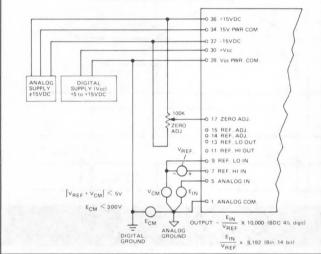
BINARY CODING

SCALE		14 BIT
SCALE	INPUT (±)	OUTPUT CODE
FS-1LSB	1.99988V	1111 1111 1111 11
7/8 FS	1.75000V	1110 0000 0000 00
3/4 FS	1.50000V	1100 0000 0000 00
1/2 FS	1.00000V	1000 0000 0000 00
1/4 FS	0.50000V	0100 0000 0000 00
1/8 FS	0.25000V	0010 0000 0000 00
1 LSB	0.00012V	0000 0000 0000 01
0	0.00000V	0000 0000 0000 00

CALIBRATION & APPLICATION

STANDARD CONNECTIONS & CALIBRATION





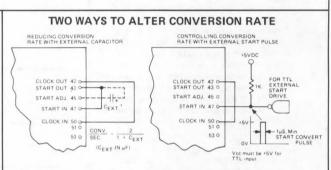
CALIBRATION INSTRUCTIONS

 Connect the converter as shown in the diagram. Allow a 15 minute warm-up time before making final adjustments.

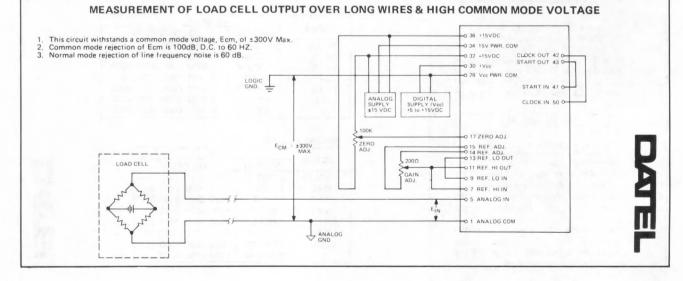
2. Zero Adjustments. Short together ANALOG IN (pin 5) and ANALOG COM (pin 1). Adjust the ZERO ADJ, potentiometer to obtain a flickering SIGN bit output (pin 72) along with logic zeros on all parallel data output lines. NOTE: The autozeroed initial offset is factory calibrated to within ±2 LSB's of zero (for either binary or BCD versions). If this is accurate enough for the required application, then no zeroing adjustment is required and pin 17 should be left open.

3. Gain Adjustment. Apply an external precision reference voltage between ANALOG IN (pin 5) and ANALOG COM (pin 1). Set the precision reference voltage to a voltage near full scale, say FS-1LSB (see coding tables), and adjust the GAIN ADJ. potentiometer to give the correct digital output code.

NOTE: The gain (set by internal reference) is factory calibrated to within $\pm 0.1\%$. If this is accurate enough for the required application, then no gain adjustment is required and the GAIN ADJ, potentiometer should be omitted. For ratiometric operation, a gain adjustment is not required.



The internal start pulse generator operates at a nominal rate of 2 pulses/second. This rate may be decreased, however, by means of an external capacitor between START OUT (pin 43) and START ADJ. (pin 45). A tantalum capacitor may be used to give a conversion time as shown in the formula. Since the conversion time of the ADC-EP is either 230 or 260 msec., depending on the model, a conversion rate as fast as 4.3 conversions per second may be achieved using an external start convert pulse as shown in the second diagram. If the pulse is from a TTL logic source, a 1K pull-up resistor must be used along with Vcc voltage of + 5VDC for the converter. The external start pulse may also be derived from CMOS logic in which case the same supply voltage must be used for the external logic and Vcc of the converter.



D/A Converters Rapid Selection Guide

The Rapid Selection Guide presented below is a capsule summary of all of Datel Systems' D/A converter series. Because we manufacture the broadest line of DAC's in the industry, this table is a useful guide for quickly locating the converters, by price range and performance, that are most suitable for your application.

After locating the desired converter series, turn to the following pages which present more detailed specifications of the various models in tabular form.

Converter Type	Series	Resolution	Output	Settling Time	Tempco	Price Range	See Page
Low Cost	DAC-9, 19, 29	8 Bits	Current, Voltage	300-500 nsec, 5-20μsec.	50-100 ppm/°C	\$14.95 - \$39	70
General Purpose	DAC-49	10 Bits	Current, Voltage	300 nsec, 5 μsec.	50 ppm/°C	\$49.00	70
	DAC-69	12 Bits	Current, Voltage	300 nsec, 20 μsec.	50 ppm/°C	\$59.00	70
High Per-	DAC-HB	8, 10, 12 Bits	Voltage	5 μsec.	30 ppm/°C	\$65 - \$89	72
formance	DAC-I	8, 10, 12 Bits	Current	150 nsec.	15 ppm/°C	\$69 - \$89	72
Moderate	DAC-R	8, 10, 12 Bits	Voltage	5 µsec.	30 ppm/°C	\$69 - \$79	72
Cost	DAC-V	8, 10, 12 Bits	Voltage	2 μsec.	20 ppm/°C	\$79 - \$119	72
	DAC-FI-GI, HI	8, 10, 12 Bits	Current	25-100 nsec.	15-30 ppm/°C	\$79 - \$129	74
High Speed	DAC-HV-100	6, 8, 10 Bits	Voltage	50-100 nsec.	60 ppm/°C	\$169 - \$189	74
Low Drift	DAC-169	16 Bits	Current, Voltage	750 nsec, 30 μsec.	10 ррт/°С	\$109.00	76
and High Resolution	DAC-HR	13, 14, 15, 16 Bits	Current	1 μsec.	1.5 ppm/°C	\$249 - \$299	76
	DAC-TR	8, 10, 12 Bits	Voltage	5 µsec.	7 ppm/°C	\$129 - \$179	76
	DAC-CM	8, 10, 12 Bits	Voltage	25 µsec.	30 ppm/°C	\$119 - \$139	78
Special	DAC-DG	12 Bits	Voltage	600 nsec.	35 ppm/°C	\$249.00	78
Purpose	DAC-MI, MV	8, 10, 12 Bits	Current, Voltage	150 nsec, 4 μsec.	30 ppm/°C	\$119 - \$159	78
	DAC-VR	8, 10, 12 Bits	Voltage	2 µsec.	20 ppm/°C	\$ 89 - \$129	78
	DAC-IG	8, 10 Bits	Current	250-300 nsec.	20 ppm/°C	\$ 8.95	80
Hybrid and	DAC-HZ, HK	12 Bits	Voltage	3 μsec.	10-20 ppm/°C	\$ 39 - \$139	80
Monolithic	DAC-HF	8, 10, 12 Bits	Current	50 nsec.	30 ppm/°C	*	80
	DAC-HA	12 Bits	Current	500 nsec.	3 ppm/°C	*	80
	DAC-HC	12 Bits	Voltage	10 µsec.	20 ppm/°C	*	80
	DAC-HU	4 Bits	Current	20 nsec.	40 ppm/°C	*	80

*To be announced.

Low Cost, General Purpose D/A Converters

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
	DAC-98BI (1)	8 Bits	0.2%			
Lowest Cost	DAC-98DI (1)	2 Digits	0.5%	- Current	rrent 500 nsec.	1/2 LSB
Current Output	DAC-98BIR	8 Bits	0.2%	Current		
	DAC-98DIR	2 Digits	0.5%	1.4.1		
8 Bit Voltage & Current Output	DAC-198B	8 Bits	0.2%	Voltage	20 µsec.	
	DAC-198D	2 Digits	0.5%	Voltage	20 µsec.	1/2 LSB
	DAC-198BI	8 Bits	0.2%	Current	300 nsec.	
	DAC-198DI	2 Digits	0.5%	Current	300 nsec.	
5 μsec.	DAC-298B	8 Bits	0.2%	- Voltage	5 µsec.	1/2 LSB
Settling Time	DAC-298D	2 Digits	0.5%	vortage	5μ sec.	1/2 LOD
	DAC-4910B	10 Bits	.05%	Voltage	5 µsec.	
10 Bit Voltage	DAC-4910BI	10 Bits	.05%	Current	300 nsec.	1/2 LSB
& Current Output	DAC4912D	3 Digits	.05%	Voltage	5 µsec.	.,2 200
	DAC-4912DI	3 Digits	.05%	Current	300 nsec.	
12 Bit Voltage	DAC-6912B	12 Bits	.01%	Voltage	20 µsec.	1/2 LSB
& Current Output	DAC-6912BI	12 Bits	.01%	Current	300 nsec.	1,2 200

NOTES: 1. These models derive their reference from the +15V supply.

2. Coding: Bin = Straight binary or offset binary

BCD = Binary coded decimal

2C = Two's complement

DAC-9 SERIES: These low cost modular DAC's feature an excellent choice of both current and voltage output models with 8 to 12 bit resolutions. All units have internal voltage references except for DAC-98BI and DAC-98DI which derive their reference voltage from the +15 volt supply. Output settling times vary from 300 to 500 nsec. for current outputs and from 5 μ sec. to 20 μ sec. for voltage outputs.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible inputs; use DIL-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.

Input Coding (2)	Output Ranges	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page	
Bin	0 to +2.6 mA				\$14.95	_	
BCD	0 to +1.6 mA	- 100 ppm/°C	+15V	2 x 1 x 0.375	\$14.95	- *	
Bin	0 to +2.6 mA		1130	2 X 1 X 0.075	\$16.95	_	
BCD	0 to +1.6 mA				\$16.95		
Bin, 2C	0 to +10V, ±5V				\$29.00		
BCD		50 ppm/°C	±15V	2 × 2 × 0.375	\$29.00	- *	
Bin		50 ppm/ C	±15V	2 X 2 X 0.575	\$29.00	_	
BCD	0 to +1.54 mA				\$29.00		
Bin, 2C	0 to +10V, ±5V	50 ppm/°C	±15V	2 × 2 × 0.375	\$39.00	- *	
BCD	0 to +10V	50 ppm/ C	±13V	2 X 2 X 0.375	\$39.00	1	
Bin, 2C	0 to +10V, ±5V			2 x 2 x 0.375	\$49.00		
Bin	0 to +2.5 mA	50 ppm/°C	±15V	2 x 2 x 0.375	\$49.00		
BCD	0 to +10V	50 ppm/ C	±13V	2 × 2 × 0.375	\$49.00	_	
BCD	0 to +1.54 mA			2 X 2 X 0.375	\$49.00		
Bin, 2C	0 to +10V, ±5V	50 ppm/°C	±15V	2 x 2 x 0.375	\$59.00	- *	
Bin	0 to +2.5 mA	30 ppm/ C	-1 5 v	2 X 2 X 0.375	\$59.00		

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

*Contact nearest Datel sales office for data sheet.



High Performance, Moderate Cost D/A Converters

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
	DAC-HB8B	8 Bits	0.2%			
Voltage Output,	DAC-HB10B	10 Bits	.05%	Voltage	5 μsec	1/2 LSB
5 μsec. Settling	DAC-HB12B	12 Bits	.01%	voltage	5 µsec	
00.05-	DAC-HB12D	3 Digits	.05%			
	DAC-18B	8 Bits	0.2%			
Current Output, 150 nsec.	DAC-I10B	10 Bits	.05%			1/2 LSB
Settling	DAC-I12B	12 Bits	.01%	Current	150 nsec.	
	DAC-18D	2 Digits	0.5%			
	DAC-I12D	3 Digits	.05%		Mar N- Fro	
	DAC-R8B	8 Bits	0.2%			
	DAC-R10B	10 Bits	.05%			
DAC-12QZ	DAC-R12B	12 Bits	.01%	Voltage	5 µsec.	1/2 LSB
Equivalent	DAC-R8D	2 Digits	0.5%			
do sant di co	DAC-R12D	3 Digits	.05%	0.3.5477.02	and mathem	1033323
	DAC-V8B	8 Bits	0.2%			
Fast, Voltage	DAC-V10B	10 Bits	.05%			
Output 2 μsec.	DAC-V12B	12 Bits	.01%	Voltage	2 µsec.	1/2 LSB
Settling	DAC-V8D	2 Digits	0.5%			
	DAC-V12D	3 Digits	.05%			

NOTE: 1. Coding: Bin = Straight binary or offset binary

BCD = Binary coded decimal

C Bin = Complementary binary

C BCD = Complementary BCD

DAC-HB SERIES: These models feature voltage outputs with settling time of 5 μ sec. Resolution is 8-12 bits with a 3 digit BCD model. Unipolar or bipolar operation is obtained by pin connection.

DAC-I SERIES: This series features low drift (15ppm/°C) current outputs with 150 nsec. settling time. Resolution is 8 through 12 bits with 2 BCD models.

DAC-R SERIES: This general purpose series features 8 through 12 bit performance with complementary input coding. Voltage output settling time is 5 μ sec. The DAC-R12B is a pin and performance equivalent of the popular DAC-12QZ converter.

DAC-V SERIES: These models are fast settling (2 μ sec.) voltage output devices with 8, 10, and 12 bit resolutions.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible inputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Input Coding (1)	Output Ranges	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
					\$ 65.00	
Bin	0 to +10V, ±5V	30 ppm/°C	±15V	2 x 1.5 x 0.375	\$ 79.00	
DIII	010 1100, -00	So bhuil C	±13V		\$ 89.00	
BCD	0 to +10V	10	1.28	DACC1988	\$ 89.00	1001
					\$ 69.00	00 Yu
Bin	0 to +2, ±1 mA				\$ 79.00	124
		15 ppm/°C	±15V	2 x 1 x 0.375	\$ 89.00	*
BCD	0 to +1.25 mA				\$ 69.00	i ar
BCD	0 t0 + 1.25 MA				\$ 89.00	1.142
	±2.5, ±5, ±10V		200 51	St. H.	\$ 69.00	
C Bin	0 to +5, +10V				\$ 75.00	1.68
		30 ppm/°C	±15V, +5V	2 × 2 × 0.375	\$ 79.00	99
C BCD	0 to +5, +10V				\$ 69.00	
CBCD	01049,4100	and without the	and a second second second	-100 AL 1 23700	\$ 79.00	
	±5, ±10V				\$ 79.00	
Bin	0 to +5, +10V				\$ 99.00	
		20 ppm/°C	±15V	2 x 2 x 0.375	\$119.00	*
BCD	0 to +5, +10V				\$ 79.00	
000	0 10 10, 100				\$119.00	

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

*Contact nearest Datel sales office for data sheet.

High Speed D/A Converters

DAC-FI, GI, HI SERIES: These fast current output models feature settling times from 100 nsec. down to 25 nsec. Resolution is from 8 bits to 12 bits with temperature coefficients from 30ppm/°C down to 15ppm/°C. This series is designed to drive a small value load resistor directly or the summing junction of a fast operational amplifier.

DAC-HV-100 SERIES: These ultra fast voltage output models have settling times from 100 nsec. to 50 nsec, with an output drive capability up to 100mA. These devices are ideal for fast applications where it is necessary to drive a 50 ohm cable directly.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible inputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
100 nsec.	DAC-FI8B	8 Bits	0.2%	- Current	100 nsec.	1/2 LSB
Current Out	DAC-FI10B	10 Bits	.05%	Current	TOO TISEC.	1/2 LOD
50 nsec. Current Out	DAC-GI8B	8 Bits	0.2%	- Current	50 nsec.	1/2 LSB
	DAC-GI10B	10 Bits	.05%	Guitent	50 11560.	1/2 230
	DAC-HI8B	8 Bits	0.2%		25 nsec.	
25 & 50 nsec. Current Out	DAC-HI10B	10 Bits	.05%	Current	25 nsec.	1/2 LSB
	DAC-HI12B	12 Bits	.01%		50 nsec.	
50 & 100 nsec.	DAC-HV6B-100	6 Bits	0.8%		50 nsec.	
Voltage Out	DAC-HV8B-100	8 Bits	0.2%	Voltage (1)	50 nsec.	1/2 LSB
	DAC-HV10B-100	10 Bits	.05%		100 nsec.	

NOTES: 1. Has 100 mA output current drive capability.

2. Coding: Bin = Straight binary or offset binary



Input Coding (2)	Output Ranges	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
Bin	±2.5, +5 mA	30 ppm/°C	±15V	2 x 2 x 0.375	\$ 79.00	- 91
2.0, 10 114		So ppin/ c	=13V	2 x 2 x 0.075	\$ 99.00	91
Bin ±2.5, +5 mA	±2.5, +5 mA 30 ppm/°C	±15V	2 x 2 x 0.375	\$ 89.00	- 91	
	±2.5, +5 mA	30 ppm/ C	±15V	2 X 2 X 0.375	\$109.00	51
32177		15ppm/°C	1.25	BRODI GAL	\$ 99.00	10
Bin	±2.5, +5 mA	15 ppm/°C	±15V	2 x 2 x 0.375	\$119.00	91
		20 ppm/°C	1.1.1	LL #STOTIAG	\$129.00	95
		1	Line Tra	RUTACOAG	\$169.00	
Bin	0 to +5V	60 ppm/°C	±15V	3 x 2 x 0.375	\$179.00	97
					\$189.00	

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

Low Drift and High Resolution D/A Converters

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
Low Cost	DAC-169-16B	16 Bits	.005%	Voltage (1)	30 µsec.	4 LSB
16 Bits	DAC-169-16D	4 Digits	.005%	vonage (1)	50 µsec.	1/2 LSB
Ultra Low Drift,	DAC-HR13B	13 Bits	.006%			1/2 LSB
	DAC-HR14B	14 Bits	.003%	— Current	1 μsec.	1/2 LSB
1.5 ppm/°C	DAC-HR15B	15 Bits	.0015%			1/2 LSB
program in	DAC-HR16B	16 Bits	.0015%		36. 36	1 LSB
	DAC-TR8B	8 Bits	0.2%			
1000	DAC-TR10B	10 Bits	.05%			
Low Drift, 7 ppm/°C	DAC-TR-12B	12 Bits	.01%	Voltage	5 µsec.	1/2 LSB
0.0-0-0-	DAC-TR-8D	2 Digits	0.5%			
	DAC-TR-12D	3 Digits	.05%			

NOTES: 1. Can also be connected for current output. Current output is 0 to + 2mA or $\pm 1 mA$ for binary version and 0 to + 1.25 mA for BCD version.

2. Coding: Bin = Straight binary or offset binary

- BCD = Binary coded decimal
 - C Bin = Complementary binary
 - C BCD = Complementary BCD

DAC-169 SERIES: These low cost, high resolution DAC's feature 16 bit or 4 BCD digit resolution with .005% linearity and 10ppm/°C temperature coefficient. By pin connection the output can be configured for either voltage or current output.

DAC-HR SERIES: This series features 13 through 16 bit resolutions with an ultra-low tempco of only 1.5ppm/°C. This is achieved by a low T.C. resistor network and an oven controlled zener reference. Linearity is .0015% and these models have current outputs.

DAC-TR SERIES: These models feature low tempco (7ppm/°C) voltage outputs with 5µsec. settling time. Input coding is complementary binary or complementary BCD.

ALL MODELS: have operating temperature range of 0°C to 70°C; have DTL/TTL compatible inputs; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Input Coding (2)	Output Ranges	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page	
Bin	+10V, -10V, ±5V	- 10 ppm/°C	±15V	2 x 2 x 0.375	\$109.00	- 10	
BCD	+10V, -10V	TO ppin/ C	±19V	2 x 2 x 0.375	\$109.00	10	
					\$249.00		
C Bin	C Bin 0 to +2mA, ±1mA	0 to +2mA +1mA	1.5 ppm/°C	±15V	$4 \times 2 \times 0.4$	\$263.00	- 103
O DIT	0 to 12mA, ± mA	1.5 ppm/ C	±15V	TAL A OTT	\$276.00	10.	
				Contraction of the	\$299.00		
	±2.5, ±5, ±10V	and the second second			\$129.00	-	
C Bin	0 to +5, +10V				\$159.00		
		- 7 ppm/°C	±15V, +5V	2 x 2 x 0.375	\$179.00	99	
C BCD	0 to +5, +10V				\$129.00		
0 000	0.010,1100				\$179.00		

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

Vol 3/77

Special Purpose D/A Converters

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
	DAC-CM8B	8 Bits	0.2%			
Low Power CMOS	DAC-CM10B	10 Bits	.05%	Voltage	25 µsec.	1/2 LSB
omoo	DAC-CM12B	12 Bits	.01%			
Deglitched	DAC-DG12B1	12 Bits	.01%	V/-1(4)	600	1/0100
DAC	DAC-DG12B2	12 Bits	.01%	Voltage (1)	600 nsec.	1/2 LSB
	DAC-MI8B	8 Bits	0.2%			
Multiplying	DAC-MI10B	10 Bits	.05%			
DAC, Two Quadrant	DAC-MI12B	12 Bits	.01%	Current	150 nsec.	1/2 LSB
Quadrant	DAC-MI8D	2 Digits	0.5%			
	DAC-MI12D	3 Digits	.05%			
	DAC-MV8B	8 Bits	0.2%			
Multiplying	DAC-MV10B	10 Bits	.05%			
DAC, Four Quadrant	DAC-MV12B	12 Bits	.01%	Voltage	4 μsec.	1/2 LSB
	DAC-MV8D	2 Digits	0.5%			
	DAC-MV12D	3 Digits	.05%			
	DAC-VR8B	8 Bits	0.2%			
Digital Input	DAC-VR10B	10 Bits	.05%			
Register	DAC-VR12B	12 Bits	.01%	Voltage	2 µsec.	1/2 LSB
	DAC-VR8D	2 Digits	0.5%			
	DAC-VR12D	3 Digits	.05%			

NOTES: 1. Glitch amplitude is ± 2 LSB's maximum.

2. Coding: Bin = Straight binary or offset binary

BCD= Binary coded decimal 2C = Two's complement

DAC-CM SERIES: These 8, 10, and 12 bit models are low power CMOS devices consuming only 40 milliwatts of power. They are ideal for portable and remote instrumentation systems.

DAC-DG SERIES: These devices are 12 bit self-contained deglitched DAC's in a compact $4 \times 2 \times 0.4$ inch module. Output settling is a fast 600 nsec. and glitch amplitude is less than 2 LSB's.

DAV-MI, MV SERIES: These 8, 10, and 12 bit DAC's feature 2 and 4 quadrant multiplying capability with voltage or current outputs and excellent bandwidth.

DAC-VR SERIES: These 8, 10, and 12 bit models have a fast (2 μ sec.) voltage output with a 20ppm/°C tempco. They feature a digital input storage register for maximum flexibility in transferring input data.

ALL MODELS: Have operating temperature range of 0° C to 70° C; have DTL/TTL compatible inputs, except for DAC-CM, which is CMOS; use DILS-1 or DILS-2 dual-in-line strips for sockets.

See pages 284 and 285 for information on Extended Performance versions.



Input Coding (2)	Output Ranges	Gain Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
					\$119.00	
Bin		30 ppm/°C	±15V	2 x 2 x 0.375	\$129.00	*
		1	A A A A A A A A A A A A A A A A A A A	- about sel	\$139.00	
Bin	-10V; ±5, ±10V	35 ppm/°C	±15V, +5V	4 x 2 x 0.4	\$249.00	×
2C	±5V, ±10V	oo ppiny o	=100,100	4 X 2 X 0.4	\$249.00	
					\$119.00	- 11
Bin	±1mA				\$129.00	_
-		30 ppm/°C	±15V	3 x 2 x 0.375	\$159.00	*
BCD	0 to -1.25 mA				\$119.00	_
BCD	0 to =1.25 MA			Satura Sasa	\$159.00	
					\$119.00	1.00
Bin	±5V, ±10V				\$129.00	0.00
		30 ppm/°C	±15V	3 × 2 × 0.375	\$159.00	*
BCD	0 to +5, +10V				\$119.00	_
				de contrato	\$159.00	
					\$ 89.00	100
Bin	±5V, ±10V 0 to +5, +10V				\$109.00	_
No inte	and the second second	20 ppm/°C	±15V, +5V	2 × 2 × 0.375	\$129.00	*
					\$ 89.00	100
BCD	0 to +5, +10V				\$129.00	

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

*Contact nearest Datel sales office for data sheet.

Hybrid and Monolithic D/A Converters

DAC-IC SERIES: These 8 and 10 bit DAC's are low cost current output models. They are monolithic devices in 16 pin DIP packages. The 10 bit models are coming soon.

DAC-HA SERIES: These models are new 12 bit multiplying CMOS DAC's with current output. Coming soon.

DAC-HC SERIES: These new models are high performance, low power CMOS units with internal reference and output amplifier Unipolar or bipolar operation is achieved by external pin connection. Coming soon.

DAC-HP SERIES: This series consists of a 16 bit binary and a 4 digit BCD model. The two models have voltage outputs and are housed in a metal case. Coming soon

DAC-HZ SERIES: These high performance 12 bit DAC's have pin-programmable outputs and a 20 ppm/°C tempco Models are available with either complementary binary or complementary BCD coding. A low drift version has a 10 ppm/°C max tempco. The different models in this series operate over 3 different temperature ranges and are in glass or metal cases.

	Model	Resolution	Accuracy (% FS)	Output	Settling Time	Linearity
8 Bit	DAC-IC8BC	8 Bits	0.2%	0	200	1/2
Monolithic	DAC-IC8BM	8 Bits	0.2%	Current	300 nsec.	1/2 LSB
Coming! 10 Bit	DAC-IC10BC	10 Bits	.05%	0	250	1/2
Monolithic	DAC-IC10BM	10 Bits	.05%	Current	250 nsec.	1/2 LSB
Coming! 12 Bit	DAC-HA12B	12 Bits	.01%	Constant	500	1/2
Hybrid CMOS	DAC-HA12D	3 Digits	.05%	Current	500 nsec.	1/2 LSB
Coming! 12 Bit	DAC-HC12B	12 Bits	.01%	Maltan	E	1/2 1 00
Hybrid CMOS	DAC-HC12D	3 Digits	.01%	Voltage	5 µsec.	1/2 LSB
Coming! 16 Bit Hybrid	DAC-HP16BM	16 Bits	.005%	N/ 11	10	4 LSB
	DAC-HP16DM	4 Digits	.005%	Voltage	10 µsec.	1/2 LSB
00/81 66	DAC-HZ12BGC	12 Bits	.01%		A. 1993	1.
	DAC-HZ12BGR	12 Bits	.01%			
High Performance	DAC-HZ12BMC	12 Bits	.0,1%	Malta	0	1/2 LSB
12 Bit Hybrids	DAC-HZ12BMR	12 Bits	.01%	Voltage	3 µsec.	
	DAC-HZ12BMR-1	12 Bits	.01%			
	DAC-HZ12BMM	12 Bits	.01%			
Coming! Hybrid	DAC-HK12B	12 Bits	.01%	Voltors	2	1/2 LSB
w. Input Register	DAC-HK12D	3 Digits	.05%	Voltage	3 μsec.	1/2 L3B
Coming! Fast,	DAC-HF8B	8 Bits	0.2%		Star-particists	
Current Output	DAC-HF10B	10 Bits	.05%	Current	50 nsec.	1/2 LSB
Hybrids	DAC-HF12B	12 Bits	.01%			
Coming! Ultra-Fast	DAC-HU4B	4 Bits	3.0%	Current	20 nsec.	1/4 LSB

NOTES: 1. All models in this series are also available with 3 digit BCD coding. Prices are same as binary. For correct model designation, change "B" to "D" in model number.

2. Coding: Bin = Straight binary or offset binary

BCD = Binary coded decimal

C Bin = Complementary binary or comp. offset Bin

C BCD = Complementary binary coded decimal

15 line = 8 bit input, no coding

DAC-HK SERIES: These models are identical in performance with the DAC-HZ series except that they have an input digital register. Coming soon

DAC-HF SERIES: This series of 8, 10, and 12 bit current output models feature a 10 mA full scale output current which settles in 50 nsec. for high speed applications. Coming soon.

DAC-HU4B: This model is a 4 bit, 15 line ECL input DAC for very fast applications The 15 mA full scale output current settles in 20 nsec. Coming soon.

ALL MODELS: Have operating temperature range of 0° C to 70° C except for those models specified otherwise; have DTL/TTL compatible inputs except for DAC-HU4B which is ECL compatible; use DILS-3 24 pin socket except for DAC-IC series, DAC-HA series and DAC-HU4B.







Input Coding	Output Ranges	Gain Tempco	Temp. Range	Power Requirement	Case	Price (1-9)	See Page
Bin	0 to -2 mA	20 ppm/° C	0 to 70C	(5)(15)(16 Pin DIP	\$8.95	83
BIN	0 to -2 mA	20 ppm/ C	-55 to +125C	+5V, -15V	16 PIN DIP	\$12.45	03
Bin	0 to -4 mA	20 ppm/°C	0 to 70C		16 Pin DIP	\$14.90	**
BIU	0 to -4 mA	20 ppm/ C	-55 to +125C	+5V, -15V	TO PIN DIP	*	**
Bin	±1 mA	3 ppm/°C	0 to 70C	+5V	18 Pin DIP	*	**
BCD	TIMA	3 ppm/ C	010700	+9 V		*	**
Bin	+5, +10, ±2.5, ±5, ±10V	20 ppm/°C	0 to 70C	±15V	24 Pin DIP	*	**
BCD	0 to +5, +10V	20 ppm/ C	010700	VCIT	24 FIII DIP	*	~ ~
C Bin	0 to +10, ±5V	20 ppm/°C	0 to 70C	±15V	24 Pin DIP	*	**
C BCD	0 to +10V	20 ppm/ C	010700	TIDV	(Metal)	*	**
No.	MUNICH	20 ppm/°C	0 to 70C	Kar Car	24 Pin DIP	\$39.00	
	The shares a start of	20 ppm/°C	-25 to +85C			\$55.00	87
C Bin (1)	±2.5, ±5, ±10V	20 ppm/°C	0 to 70C	+151/		\$49.00	
	0 to +5, +10V	20 ppm/°C	-25 to +85C	±15V 24 Pin DIP	24 Pin DIP	\$69.00	
		10 ppm/°C	-25 to +85C		(Metal)	\$139.00	
		20 ppm/°C	-55 to +125C			\$119.00	
Binary	0 to +10, ±5, ±10V	20 ppm/°C	0 to 70C	±15V, +5V	24 Pin DIP	*	
BCD	0 to +5, +10V	20 ppm/ C	010700	±13V, +5V	24111011	*	**
						*	
Bin	0 to +10 mA	20 ppm/°C	0 to 70C	±15V	24 Pin DIP	*	**
					(Metal)	*	
15 Line	0 to -15 mA	40 ppm/°C	0 to 70C	-4.4V	32 Pin DIP	*	* *

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

**Contact nearest Datel sales office for data sheet and availability.

From radar to computer ...

DATEL

A D CONVERTER

DATEL

SAMPLE AND HOLD

UH SERIES



The Datel ADC-UH series gives you a choice of three state-of-the-art ultra-high-speed analog to digital converters. Available are four, six and eight binary bits operating at word repetition rates of up to 25 MHz and a four bit version capable of making a conversion every forty nanoseconds.

They measure a mere 3"x5"x1.15" or about one fifth the size of their nearest rival. Power drain has been reduced to eight watts, temperature coefficient is 50ppm/ C and long term stability ±.25% / year.

Output digital coding is straight binary for a unipolar input and inverted offset binary for the optional bipolar input. All control inputs, outputs and data output lines are compatible with standard TTL logic levels. A companion to the ADC-UH series is our SHM-UH Sample/Hold amplifier unit, which features a tracking capability of 35 nanoseconds with an aperture time of less than 200 picoseconds. For complete details on both devices, call or write



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461



LOW COST, 8 BIT MONOLITHIC DIGITAL TO ANALOG CONVERTERS

MODELS DAC-IC8BC, DAC-IC8BM

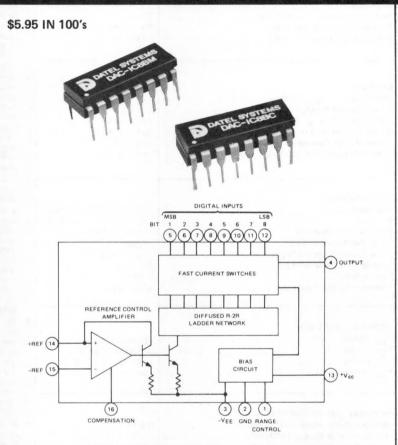
FEATURES

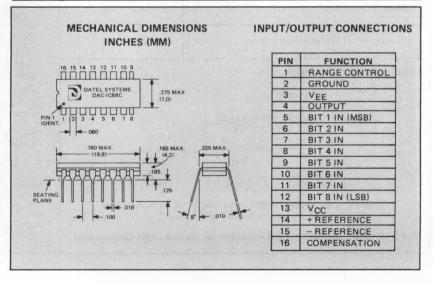
- ▶ Low Cost-\$5.95 in 100's
- ▶ 8 Bit Resolution
- ▶ Fast Settling-300 nsec.
- ▶ 1 or 2 Quadrant Multiplication
- ▶ ±1/2LSB Linearity
- ► DTL/TTL Compatible Inputs

The DAC-IC8BC and DAC-IC8BM are 8 bit monolithic DAC's with fast settling current outputs. The units are housed in a 16 pin ceramic DIP and require only an external reference and output amplifier for fast voltage output operation. A full scale output change settles in only 300 nanoseconds for current output operation and 600 nanoseconds for voltage output operation using a fast monolithic output amplifier (Datel Systems AM-452). Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation and is compatible with standard DTL/TTL logic. The DAC-IC8B converters consist of 8 fastswitching current sources, a diffused R-2R resistor ladder network, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of -20ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling, and low cost. Linearity is ±1/2LSB.

An external reference current of 2mA nominal programs the scale factor for the DAC; this is done by means of an external voltage reference source (such as a Zener diode) and a resistor. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar depending on whether an external offsetting current (derived from the reference) is used. Output voltage compliance of the DAC is -0.6V to +0.5V; this can be made as large as -5V to +0.5V by external pin connection for cases where direct voltage output from a load resistor is desired.

Power supply requirement is +5VDC and -5V to -15VDC. Model DAC-IC8BC has an operating temperature range of 0°C to 70°C while DAC-IC8BM operates over -55°C to +125°C. The two models are pin compatible with Motorola devices MC1408L-8 and MC1508L-8 respectively.





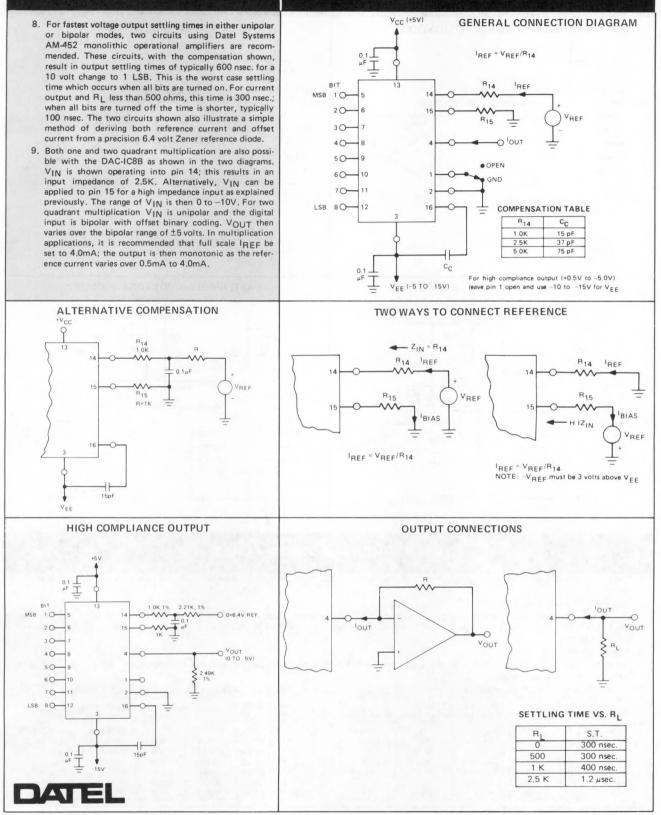
PECIFICATIONS, DAC-IC8BC & DAC-IC8B $_{CC}$ +5V, V _{EE} = -15V, and I _{REF} = 2mA unless othe	wise specified)
INPUTS Resolution Coding, unipolar output Coding, bipolar output Input Logic Level, bit ON ("1") Logic Level, bit OFF ("0") Logic Loading Nominal Reference Current (+ Ref.) Reference Current Range (+ Ref.) Reference Bias Current (- Ref.)	8 bits Straight Binary Offset Binary +2.0V to +5.5V @ 40µA 0V to +0.8V @ -0.8mA 1 TTL load 2.0mA 0 to 4.2mA -3µA max.
DUTPUTS Dutput Current, $I_{REF} = 2.0mA$ Dutput Current Range, $V_{EE} = -5V$ Dutput Current Range, $V_{EE} = -6$ to $-15V$ Dutput Current, all bits OFF Dutput Voltage Compliance, pin 1 gnded Dutput Voltage Comp., pin 1 open, $V_{EE} < -10V$	2.0mA ±0.1mA 0 to 2.1mA 0 to 4.2mA 4μA maximum -0.6 to +0.5V -5.0V to +0.5V
PERFORMANCE Relative Accuracy ¹	±½LSB (±0.19%) maximum ±½LSB (±0.19%) maximum ±½LSB (±0.19%) -20ppm/°C 2.7μA/V max. 300 nsec. 3.3MHz 4.0mA/μsec
POWER REQUIREMENT V _{CC} Voltage V _{CC} Current V _{EE} Voltage V _{EE} Current	+5VDC ±0.5V 22mA maximum -4.5V to -16.5VDC 13mA maximum
PHYSICAL-ENVIRONMENTAL Operating Temp. Range, DAC-IC8BC Deprating Temp. Range, DAC-IC8BM Storage Temp. Range, either model	0° C to 70° C -55° C to +125° C -65° C to +150° C 16 pin ceramic DIP
With zero and full scale adjustments made.	
RDERING INFORMATION	
$\begin{array}{c} \hline \textbf{OPER. TEMP. RANGE} \\ \textbf{C} &= 0^{\circ} \textbf{C} \ \textbf{TO} \ 70^{\circ} \textbf{C} \\ \textbf{M} &= -55^{\circ} \textbf{C} \ \textbf{TO} + 125^{\circ} \textbf{C} \\ \end{array}$	
PRICES (1.9) DAC-IC8BC \$8.95 DAC-IC8BM \$12.75	(100's) \$5.95 \$8.50
Trimming Potentiometers: TP500, TP1K, and TP20	DK are available from

TECHNICAL NOTES

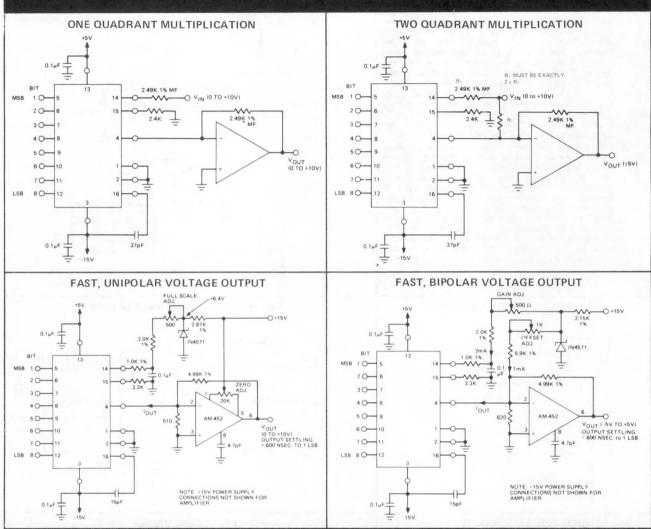
- 1. The General Connection Diagram shows the basic connections for the DAC-IC8B converter. The scale factor is set by a reference current injected into pin 14. Pins 14 and 15 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R₁₅ and pin 14 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R₁₄: IREF = VREF/R₁₄. R₁₄ should be a stable metal film resistor. R₁₅ is used only to compensate for the input bias current into pin 15 (1 μ A typical) and can be shorted out with negligible effect. R₁₅, if used, should be equal to R₁₄ and may be a carbon composition type. An IREF of 2.0mA is recommended for most applications.
- 2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference*. A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 14 is at the negative voltage and IREF still flows into pin 14. Again, R15 is used only to compensate for bias current and may be omitted. There is an important requirement for this connection: the negative reference voltage must always be 3 volts above VEE.
- 3. The reference amplifier must be externally compensated, and this is done by capacitor C_c , connected from pin 16 to pin 3 (V_{EE}). C_c may also be connected from pin 16 to ground, but connection to pin 3 improves the negative supply rejection. The value of C_c depends on R₁₄, and typical values are given in the compensation table. Compensation is particularly important when the DAC-IC8B is used as a multiplying D/A converter. Proper compensation assures that output peaking does not occur when the reference voltage steps to a new value. If pin 14 is driven from a high impedance current source such as a transistor collector, then much larger values of C_c must be used and the bandwidth of the reference amplifier is significantly reduced.
- 4. The Alternative Compensation Diagram shows another way of achieving the desired compensation. Here a 1.0K resistor is always used at pin 14, but it is in series with another R to the reference voltage. The junction of the two resistors is bypassed to ground by a 0.1 μ F capacitor. For high frequencies pin 14 always "sees" a 1K resistance, thus allowing a 15pF capacitor for C_C. R₁₅, if used, should be the sum of 1.0K and R. This compensation scheme is useful with voltage references such as 6.2 or 6.4 volt Zener diodes.
- . It is recommended that pin 13 (V_{CC}) and pin 3 (V_{EE}) always be bypassed to ground with at least $0.1\mu F$ capacitors located close to the pins.
- As shown in the General Connection Diagram, pin 1 may be either connected to around or left open. This connection determines the voltage compliance at pin 4 (IOUT). For pin 1 grounded, the output compliance is -0.6 to +0.5 volt. This is satisfactory when pin 4 is used to drive a current to voltage converter and pin 4 is held at virtual ground. It is also satisfactory for low values of RL connected to pin 4 to directly convert the output current to a voltage. The voltage compliance may be extended to -5.0 volts by leaving pin 1 open and using a VEE more negative than -10 volts. In this way a 2.5K load resistor may be used at pin 14 to give an output voltage range of 0 to -5 volts (with reference current of 2mA). As shown in the table of Settling Time vs RL, the output settling time is constant (300 nsec.) for ${\sf R}_{\sf L}$ values from O to 500 ohms; thereafter it increases to 1.2µsec for $R_1 = 2.5K$.
- 7. The accuracy of the DAC-IC8B is specified for a reference current of 2.0mA; the accuracy, however, is essentially constant for reference currents from 1.5mA to 2.5mA. Typically, this device is monotonic for all values of reference current above 0.5mA. Reference currents up to 4.2mA may be used. When using a 4mA reference current, VEE must be more negative than -6 volts.

TECHNICAL NOTES (Cont'd)

CONNECTION DIAGRAMS



APPLICATION DIAGRAMS



CALIBRATION AND CODING TABLES

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.

2. Zero and Offset Adjustments

For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.

3. Gain Adjustment

For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

UNIPOLAR OPERATION-STRAIGHT BINARY CODING

INPUT CODE	UNIPOLAR OUTPUT RANGES						
MSB LSB	0 TO +5V	0 TO +10V	0 TO 2MA	0 TO -4MA			
1111 1111	+4.980	+9.961V	-1.992MA	-3.984MA			
1110 0000	+4.375	+8.750	-1.750	-3.500			
1100 0000	+3.750	+7.500	-1.500	-3.000			
1000 0000	+2.500	+5.000	-1.000	-2.000			
0100 0000	+1.250	+2.500	-0.500	-1.000			
0000 0001	+0.020	+0.039	-0.008	-0.016			
0000 0000	0.000	0.000	0.000	0.000			

BIPOLAR OPERATION-OFFSET BINARY CODING

INPUT CO	DDE	BIPOLAR OUTPUT RANGES					
MSB	LSB	±5V	±10V	±1MA	±2MA		
1111 11	11	+4.961V	+9.922V	-0.992MA	-1.984MA		
1110 00	00	+3.750	+7.500	-0.750	-1.500		
1100 00	00	+2.500	+5.000	-0.500	-1.000		
1000 00	00	0.000	0.000	0.000	0.000		
0100 00	00	-2.500	-5.000	+0.500	+1.000		
0000 00	01	-4.961	-9.922	+0.992	+1.984		
0000 00	00	-5.000	-10.000	+1.000	+2.000		



LOW COST, 12 BIT HYBRID DIGITAL TO ANALOG CONVERTERS

DAC-HZ SERIES

FEATURES

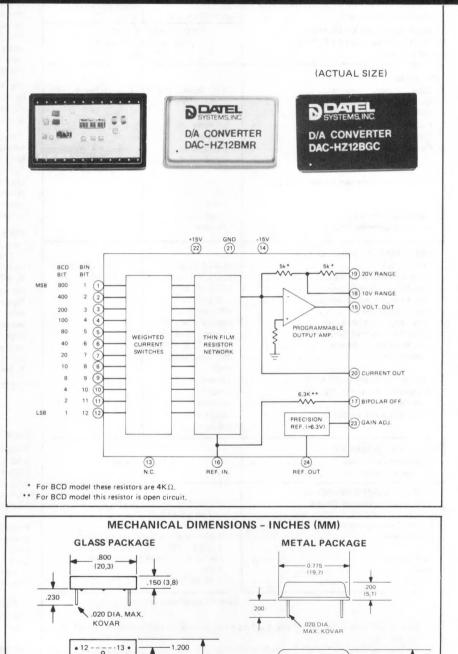
- 12 Bit Binary or 3 Digit BCD
- Pin-Programmable Outputs
- Internal Reference & Output Amp.
- Glass or Metal Package
- ▶ ±15VDC Supply Only
- ► Fast Settling Time
- ▶ 12 Different Models

GENERAL DESCRIPTION

The DAC-HZ series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. These converters are manufactured in volume in Datel Systems' modern in-house thin film hybrid facility. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V with only unipolar ranges available on the BCD models. Current output is also provided.

The internal design utilizes three quad current switches, two thin film resistor networks, a precision zener reference circuit, reference control circuit and output amplifier. The thin film resistor networks are functionally trimmed with a laser to precisely set the binary weights of the current switches. The excellent tracking of the thin film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2ppm/°C. Temperature coefficient of gain is ±20ppm/°C max. and tempco of zero is ±5ppm/°C of FS max. There are also two low drift models in the series with maximum gain tempco of ± 10 ppm/°C.

The DAC-HZ series consists of 12 different models covering the operating temperature ranges of 0°C to 70°C, -25°C to +85°C, and -55°C to +125°C. The models are available in miniature glass or metal hermetically sealed cases. Power requirement is ±15VDC at 35mA with no 5V logic supply required. Input coding is complementary binary or complementary BCD. Voltage output settling time is 3 µsec. to 1/2 LSB.



• 12

.

DOT ON TOP REFERENCES PIN 1 -- 13 •

BOTTOM

VIEW

(15 2)

- 1.1875

SPACES

100 FA

-.0875

3875

SPACES

AT

EACH

100

-.100

100

.

24 .

BOTTOM

VIEW

.600

(15,2)

1.300

(33.0)

023" HIGH

DOT ON

TOP REF.

ERENCES

PIN 1

STAND-OFFS

.

• 0

NOTE: .100 inch = 2.5 MM

1.275

SPECIFICATIONS, DAC-HZ SERIES (Typical at 25 $^{\circ}$ C and ±15V supplies unless otherwise noted)

	DAC-HZ12B (Binary)	DAC-HZ12D (BCD)
NPUTS Resolution Coding, unipolar output Coding, bipolar output	12 Binary bits Complementary Binary Comp. Offset Bin.	3 BCD digits Complementary BCD
Input Logic Level, bit ON ("0") Input Logic Level, bit OFF ("1") Logic Loading	0V to +0.8V +2.0V to +5.5 1 TTL	5V @ +40µA
OUTPUTS		
Output Current, unipolar Output Current, bipolar Output Current, bipolar Voltage Compliance, lout Output Impedance, lout, unipolar Output Impedance, lout, bipolar Output Voltage Ranges, unipolar	0 to -2mA, ±10% ±1mA, ±10% ±2.5V 5K ohms 2.8K ohms 0V to +5V 0V to +10V	0 to -1.25mA, ±10% * * 0 to +2.5V 0 to +5V
Output Voltage Ranges, bipolar	±2.5V ±5V ±10V	0 to +10V
Output Current, Vout	±5mA min. .05 ohm	*
PERFORMANCE, Voltage Output Nonlinearity Differential Nonlinearity Gain Error, before trimming Zero Error, before trimming Gain Tempco, max. ² Zero Tempco, unipolar, max. Offset Tempco, biopolar, max. ² Diff. Nonlinearity Tempco Monotonicity Settling Time, lout to 1/2 LSB Slew Rate Power Supply Rejection	$\pm 1/2$ LSB max, $\pm 1/2$ LSB max, $\pm 0.1\%$ of FSR ¹ $\pm .05\%$ of FSR ¹ $\pm 20ppm/^{\circ}C$ $\pm 5ppm/^{\circ}C$ of FSR ¹ $\pm 10ppm/^{\circ}C$ of FSR ¹ $\pm 2ppm/^{\circ}C$ of FSR ¹ $\pm 2ppm/^{\circ}C$ of FSR ¹ 0ver oper, temp, range 300nsec. $3 \mu sec$. $4 20V/\mu sec$. $\pm .002\%$ FSR/ % Supply ¹	±1/4 LSB max. ±1/4 LSB max. * * * * * * * * * * *
POWER REQUIREMENT Power Supply Voltage Quiescent Current	±15VD0 35	C ±0.5V mA
HYSICAL-ENVIRONMENTAL Operating Temperature Ranges	0°C to 70°C, -25°C	

 Operating Temperature Range
 0 C to 70 C, -25 C to 455 C, and -55°C to +125°C

 Storage Temperature Range
 -55°C to +125°C

 Package Size
 1.300 x 0.800 x 0.150 inches (Glass)

 1.275 x 0.775 x 0.200 inches (Metal)
 Hermetically sealed glass or metal

 Pins
 Kovar

 Weight
 0.15 oz. (Glass), 0.27 oz. (Metal)

*Specifications same as first column

1. FSR is full scale range and is 10V for 0 to +10V or -5V to +5V output; 20V for $\pm 10V$ output, etc.

2. For models DAC-HZ12BMR-1 and DAC-HZ12DMR-1 the temperature coefficients are: Gain, $\pm 10ppm/^{\circ}$ C max.; Bipolar Offset, $\pm 5ppm/^{\circ}$ C max.

3. Current output mode.

 For 2.5K or 5K feedback (2K or 4K, BCD). For 10K feedback (8K, BCD) the settling time is 4 µsec.

TECHNICAL NOTES

- 1. The DAC-HZ12 series converters are designed and factory calibrated to give \pm %LSB linearity (binary version) and \pm %LSB linearity (BCD version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be \pm 1/2 LSB (\pm 1/4 LSB, BCD) everywhere over the full output range without any additional adjustments to achieve a best straight line fit. The linearity specification is therefore a conservative one since the user does not have to make more complicated adjustments for a best straight line fit.
- 2. The external zero or offset adjustment for the converters has a range of $\pm 0.2\%$ of full scale and the external gain adjustment has a range of $\pm 0.3\%$ of full scale.
- 3. These converters must be operated with local supply by-pass capacitors from +15V to ground and -15V to ground. Tantalum type capacitors of 1μ F are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a .01 μ F ceramic capacitor should be used across each tantalum capacitor.

4. When operating in the current output mode the equivalent internal current source of 2mA (1.25mA, BCD) must drive both the internal source resistances and the external load resistor. A 300 nsec. output settling time is achieved for the voltage across a 100 ohm load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast settling amplifier such as Datel Systems AM-100 should be used in the inverting mode. Settling time of less than 1 µsec. can be achieved. See application diagram.

ORDERING INFORMATION

Model	Temp. Range	Case	Price (1-9)
DAC-HZ12BGC	0 to 70C	Glass	\$ 39.00
DAC-HZ12BMC	0 to 70C	Metal	\$ 49.00
DAC-HZ12BGR	-25 to +85C	Glass	\$ 55.00
DAC-HZ12BMR	-25 to +85C	Metal	\$ 69.00
DAC-HZ12BMR-1	-25 to +85C	Metal	\$139.00
DAC-HZ12BMM	-55 to +125C	Metal	\$119.00
DAC-HZ12DGC	0 to 70C	Glass	\$ 39.00
DAC-HZ12DMC	0 to 70C	Metal	\$ 49.00
DAC-HZ12DGR	-25 to +85C	Glass	\$ 55.00
DAC-HZ12DMR	-25 to +85C	Metal	\$ 69.00
DAC-HZ12DMR-1	-25 to +85C	Metal	\$139.00
DAC-HZ12DMM	-55 to +125C	Metal	\$119.00
*NOTE: Models DA are low drift mod max.			
Mating Socket: DI Trimming Potentic TP10K OR			5 ea.

THE DAC-HZ12 SERIES CONVERTERS ARE COV-ERED BY GSA CONTRACT.

INTERCONNECTIONS AND CALIBRATION

CALIBRATION PROCEDURE

- 1. Select the desired output range and connect the converter up as shown in the Output Range Selection table and the Standard Connection diagrams below.
- 2. To calibrate refer to the Coding Tables below. Note that complementary coding is used.
- 3. Zero and Offset Adjustments For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ, potentiometer for zero output voltage or current. For bipolar operation (binary model only) set all digital inputs to "1" and adjust the OFFSET ADJ, potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the Coding Table.
- 4. Gain Adjustment

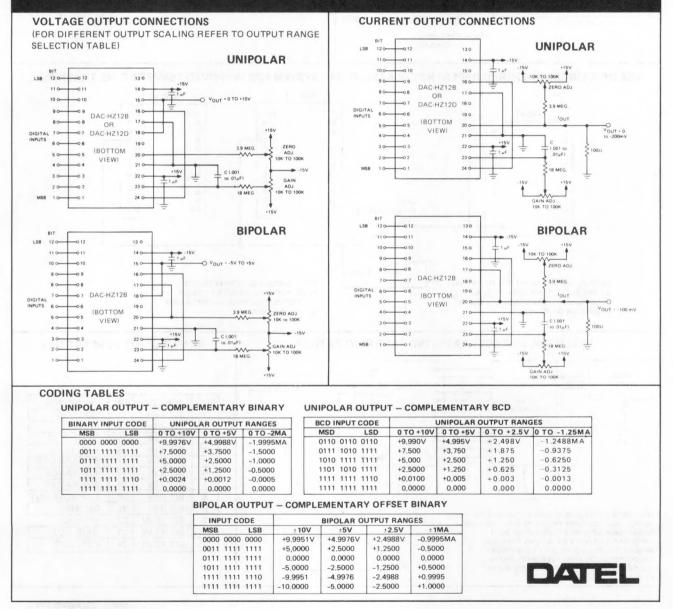
For the binary model set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ, potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table. For the BCD model (unipolar only) set each BCD digit to 0110 and adjust the GAIN ADJ, potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.

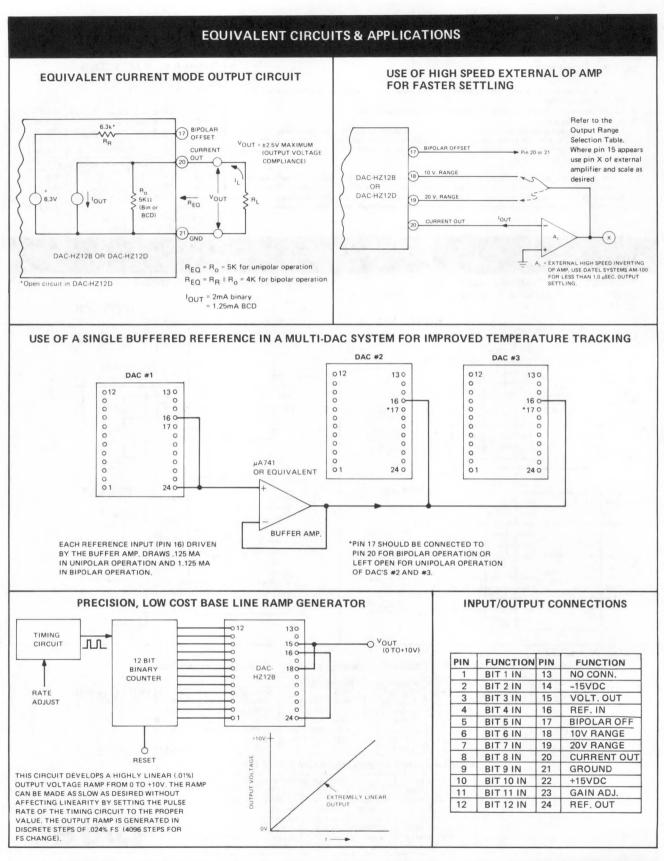
OUTPUT RANGE SELECTION

BIN. RANGE	CONNEC	T THESE	PINS TOO	GETHER
±10V	15 & 19	17 & 20		16 & 24
±5V	15 & 18	17 & 20		16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21		16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1mA		17 & 20		16 & 24
-2mA	-	17 & 21		16 & 24
BCD RANGE	CONNEG	CT THESE	PINS TO	GETHER
+10V	15 & 19			16 & 24
+5V	15 & 18			16 & 24
+2.5V	15 & 18		19 & 20	16 & 24
-1.25MA				16 & 24

VOLTAGE OUTPUT IS AT PIN 15 CURRENT OUTPUT IS AT PIN 20

STANDARD CONNECTIONS









FOR ULTRA-HIGH SPEED APPLICATIONS **25 NANOSEC. OUTPUT SETTLING TIME** DIGITAL TO ANALOG CONVERTERS

DAC-FI-GI-HI SERIES

FEATURES

- Fastest settling time available
- High Resolution
- Small Size
- Low Temperature coefficient
- Ultra linear
- Adjustment-Free operation

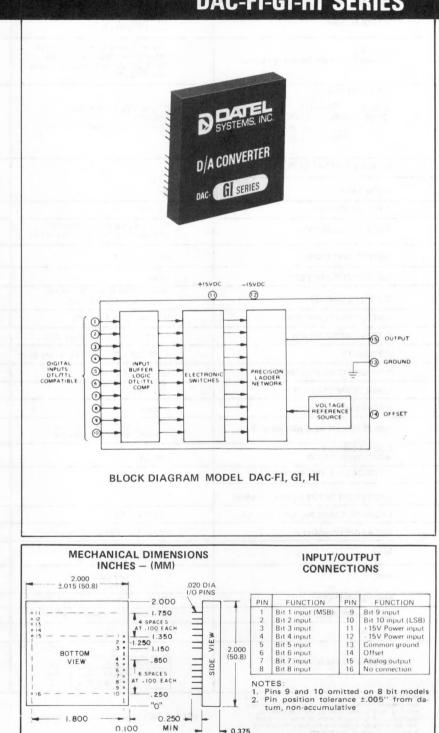
GENERAL DESCRIPTION

This series of D/A converters are miniature ultra high speed devices offering the user state-of-the-art output settling time. Twenty-five nanoseconds for DAC-HI, fifty nanoseconds for DAC-GI and one hundred nanoseconds for DAC-FI series. Standard versions are available with either eight bit or ten bit resolution. Accuracy specifications include ±1/2 LSB linearity, ±15ppm/°C temperature coefficient, and ±0.05% full scale accuracy.

Bipolar operation is achieved by externally connecting the built-in offsetting reference. Input coding can be straight binary for unipolar output or a choice of offset binary or two's complement for bipolar output.

Each D/A is completely self-contained requiring only ±15 volts D.C. power. Packaged in 2" x 2" x 0.375", low profile modules, they are readily soldered or plugged directly into P.C. cards or other mother board hardware. Included in each module is digital interface logic, a precision resistor ladder network, high speed electronic switches, and a temperature compensated precision voltage reference source.

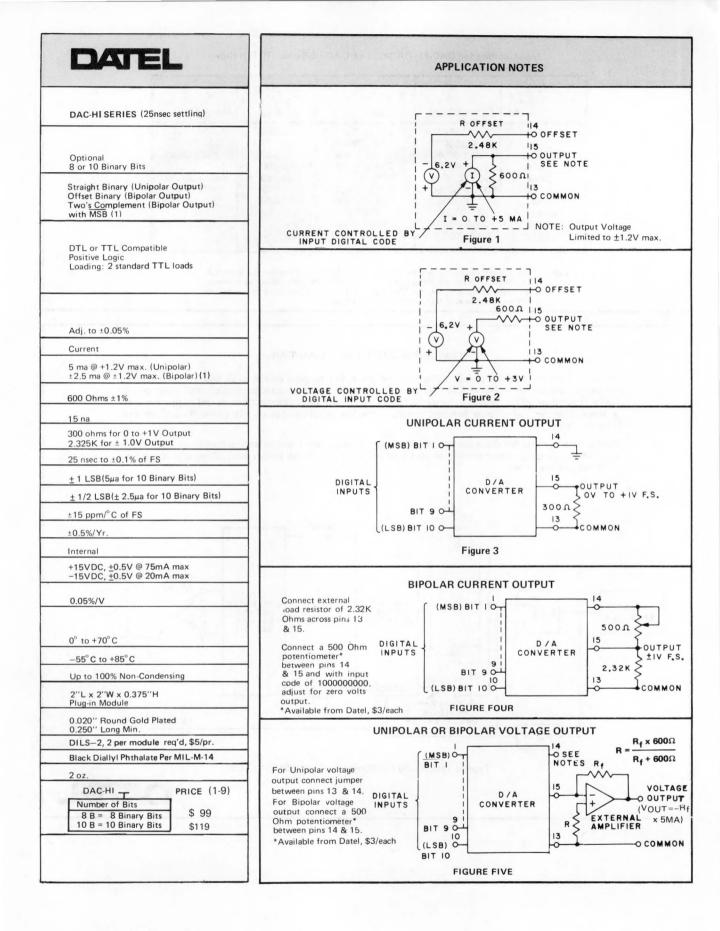
One of the many prime features is the output flexibility - 5 ma current output can be fed directly into an external resistor to develop a 1.2V maximum output or by external pin strapping a bipolar output of ±1.2V maximum can be generated across the output load resistor. The output current can also be fed into an operational amplifier for those who require sign inversion, scaling, etc. This amplifier can be selected to suit a particular application.

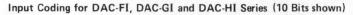


SPECIFICATIONS (TYPICAL @ 25°C UNLESS OTHERWISE NOTED)

DAC-FI - DAC-GI - DAC-HI

PARAMETERS	DAC-FI SERIES (100nsec settling)	DAC-GI SERIES (50nsec settling)	
DIGITAL INPUTS		Optional 8 or 10 Binary Bits	
RESOLUTION	Optional 8 or 10 Binary Bits		
CODING (Parallel Data in the following Formats)	Straight Binary (Unipolar Output) Offset Binary (Bipolar Output) Two' <u>s Co</u> mplement (Bipolar Output) with MSB (1)	Straight Binary (Unipolar Output) Offset Binary (Bipolar Output) Two's Complement (Bipolar Output) with MSB (1)	
DATA INPUTS INPUT VINPUT BIT CODE MIN. MAX. STATUS "0" OV +0.8V OFF "1" +2.0V +5.5V ON	DTL or TTL Compatible Positive Logic Loading: 2 standard TTL loads	DTL or TTL Compatible Positive Logic Loading: 2 standard TTL loads	
ANALOG OUTPUT (@ 25°C)	043		
ACCURACY	Adj. to ±0.05%	Adj. to ±0.05%	
TYPE OF OUTPUT	Current	Current	
FULL SCALE OUTPUT	5 ma @ +1.2V max. (Unipolar) ±2.5 ma @ ±1.2V max. (Bipolar)(1)	5 ma @ +1.2V max. (Unipolar) ±2.5 ma @ ±1.2V max. (Bipolar)(1)	
OUTPUT IMPEDANCE	600 Ohms ±1%	600 Ohms ±1%	
OUTPUT ZERO OFFSET	15 na	15 na	
OUTPUT LOADING	300 ohms for 0 to +1V Output 2.325K for ±1.0V Output	300 ohms for 0 to +1V Output 2.325K for ± 1.0V Output	
OUTPUT SETTLING TIME	OUTPUT SETTLING TIME 100 nsec to ±0.1% of FS 50 nsec to ±0.1%		
OUTPUT RESOLUTION ± 1 LSB(5µa for 10 Binary Bits) ±		± 1 LSB(5μa for 10 Binary Bits)	
LINEARITY	\pm 1/2 LSB(\pm 2.5µa for 10 Binary Bits)	\pm 1/2 LSB(\pm 2.5µa for 10 Binary Bit	
TEMPERATURE COEFFICIENT	±50 ppm/°C of FS	$\pm 30 \text{ ppm/}^{\circ} \text{C} \text{ of FS}$	
LONG TERM STABILITY	±0.5%/Yr.	±0.5%/Yr.	
REFERENCE SOURCE	Internal	Internal	
INPUT POWER REQUIREMENTS	+15VDC, <u>+</u> 0.5V @ 75mA max -15VDC, <u>+</u> 0.5V @ 20mA max	+15VDC, <u>+</u> 0.5V @ 75mA max -15VDC, <u>+</u> 0.5V @ 20mA max	
POWER SUPPLY REJECTION RATIO	0.05%/V	0.05%/V	
PHYSICAL - ENVIRONMENTAL	CATURA COMMENT		
OPERATING TEMPERATURE RANGE	0° to +70° C	0° to +70° C	
STORAGE TEMPERATURE RANGE	-55° C to +85° C	–55°C to +85°C	
RELATIVE HUMIDITY	Up to 100% Non-Condensing	Up to 100% Non-Condensing	
SIZE	2''L x 2''W x 0.375''H Plug-in Module	2''L x 2''W x 0.375''H Plug-in Module	
PINS	0.020" Round Gold Plated 0.250" Long Min.	0.020" Round Gold Plated 0.250" Long Min.	
MATING SOCKET	DILS-2, 2 per module req'd, \$5/pr.	DILS-2, 2 per module req'd, \$5/pr.	
CASE MATERIAL (2)	Black Diallyl Phthalate Per MIL-M-14	Black Diallyl Phthalate Per MIL-M-14	
WEIGHT	2 oz.	2 oz.	
ORDERING INFORMATION	DAC-FI PRICE (1-9) Number of Bits \$79. 8 B = 8 Binary Bits \$99. 10 B = 10 Binary Bits \$99.	DAC-GI _ PRICE (1-5 Number of Bits \$ 89. 8 B = 8 Binary Bits \$ 109.	





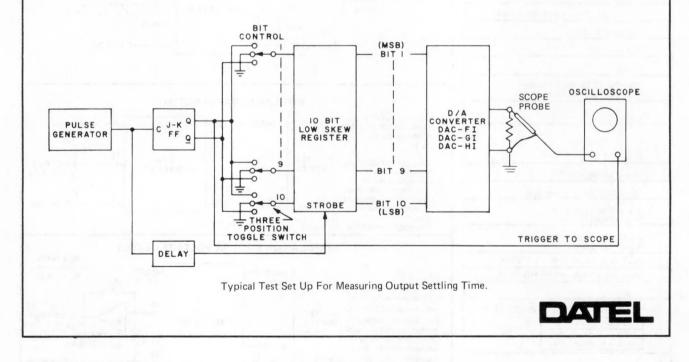
Analog Output Range (±2.5 ma FS)	Offset Binary	2's Complement (See Note)	Analog Output Range (0 to +5ma FS)	Straight Binary
+2.495	1111111111	011111111	+4.995	1111111111
+2.187	1111000000	0111000000	+4.375	1110000000
+1.875	1110000000	0110000000	+3.750	1100000000
+1.250	1100000000	010000000	+2.500	100000000
0.000	100000000	0000000000	+1.250	010000000
-1.250	010000000	1100000000	+0.625	0010000000
-1.875	001000000	1010000000	0.000	0000000000
-2.187	0001000000	1001000000		
-2.495	000000001	100000001	States and the	
-2.500	0000000000	100000000		

Note 1: The converter does not directly accept 2's complement coding without first externally complementing the 2's comp MSB by using an external inverter or FF \overline{Q} output. After this bit is complemented, the code appears as normal offset binary which the converter can process.

MEASURING OUTPUT SETTLING TIME

Because of the phenomenal output settling time of these devices, great care must be taken when measuring the output performance. Model 454 Tektronix Oscilloscope with low capacitance probe and probe ground lead is recommended for measuring output settling time. Input/Output connections should be made as close as possible to the "DAC" pins. Best results occur when the digital input source has a time skew of less than 5 nanoseconds.

Output settling time for these devices can be defined as that time between application of an input digital word and the analog output settling to $\pm 0.1\%$ of full scale, it includes switch delay, slewing time and final exponential decay time.





12 BINARY BIT RESOLUTION 25 NSEC OUTPUT SETTLING TIME DIGITAL TO ANALOG CONVERTER

MODEL DAC-HI 12B

FEATURES

- ULTRA FAST SETTLING
- HIGH RESOLUTION
- SMALL SIZE

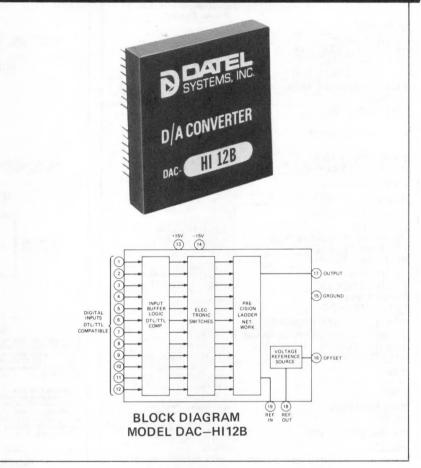
GENERAL DESCRIPTION

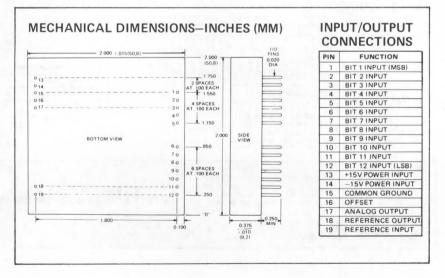
The DAC-HI12B is a 12 bit Digital to Analog converter featuring a state-ofthe-art output settling time of 25 nanoseconds combined with a \pm 1/2LSB linearity and a temperature coefficient of \pm 20ppm/°C.

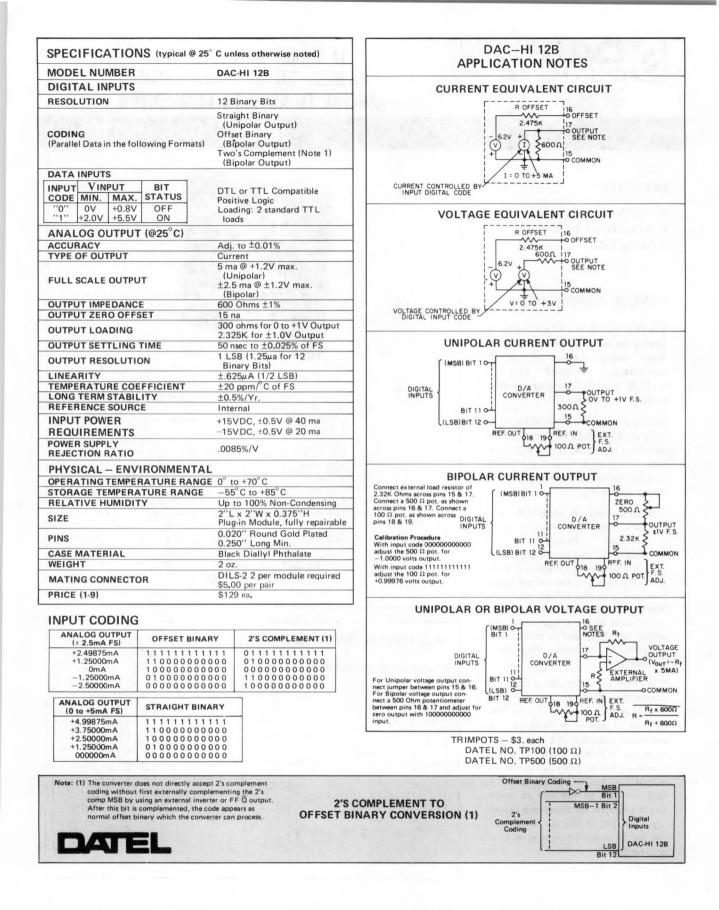
Bipolar operation is achieved by externally pin strapping a built-in offsetting reference. Input coding can be straight binary for unipolar output, or a choice of offset binary or two's complement for bipolar output.

The DAC-HI12B is completely selfcontained, requiring only ±15 volts DC power. Packaged in а 2"x2"x0.375", low profile module, it is readily soldered or plugged directly into P.C. cards or other mother board hardware. Included in each module is digital interface logic, a precision resistor ladder network, high speed electronic switches, and a temperature compensated precision voltage reference source.

One of the prime features is the unit's output flexibility with a 5 ma current output which can be fed directly into an external resistor to develop a 1.2V maximum output or, by external pin strapping, a bipolar output of \pm 1.2V maximum can be generated across the output load resistor. The output current can also be fed into an operational amplifier for those who require sign inversion, scaling etc. This amplifier can be selected to suit a particular application.









HIGH SPEED 50 Ω line driver digital to analog converters

DAC-HV-100 SERIES

FEATURES

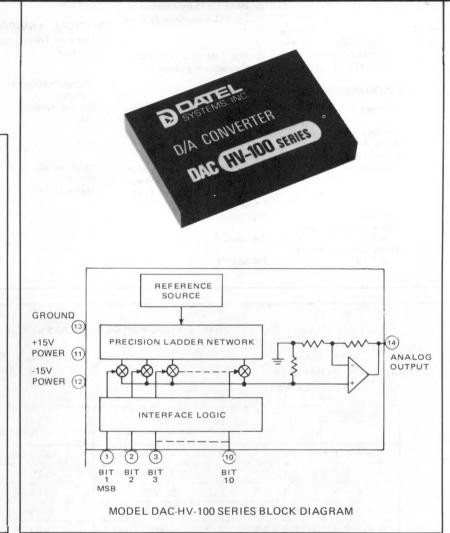
- Ultra High Speed
- ▶ High Output Current
- High Resolution
- Excellent Linearity
- Adjustment Free Operation

DESCRIPTION

The Model DAC-HV-100 Series Digital to Analog Converters are ultra high speed devices with a settling time of 50 nanoseconds. Standard versions are available with six, eight or ten binary bit input resolution. The output swings from 0 to +5 volts and is capable of driving a 50 ohm transmission line.

The superior transfer characteristic of the DAC-HV-100 Series include an accuracy of 0.1% of full scale, a linearity of $\pm 1/2$ LSB and a temperature coefficient of ± 100 PPM/°C. Long term stability of these converters is $\pm 0.5\%$ per year.

Each D/A is completely self contained requiring only ±15 VDC power. Packaged in a 2"Wx3"L x.375"H low profile module, they are readily soldered or plugged into PC boards which can then be mounted on 1/2 inch centers. The module includes digital interface logic and precision resistor ladder networks, high speed electronic switches, a temperature compensated precision voltage reference source and featuring an ultra high speed amplifier capable of settling to within 0.4% accuracy in 50 nanoseconds after a full scale output excursion.



MECHANICAL DIMENSIONS (INCHES) INPUT/OUTPUT CONNECTIONS 020 3.000 I/O PINS DIA. FUNCTION FUNCTION 2.000 PIN PIN - 1.750 - 1.650 - 1.550 • 11 • 12 • 13 1 BIT 1 (MSB) 9 BIT 9 2 BIT 2 BIT 10 -1.350 -1,250 -1.150 10 • 14 1.2.3. 3 BIT 3 11 +15V POWER INPUT 2.000 .850 456789 4 BIT 4 12 -15V POWER INPUT 6 SPACES .100 APART 5 BIT 5 13 GROUND .250 10 15 BIT 6 ANALOG OUTPUT 6 14 .250 MIN -0 7 BIT 7 15 NO CONNECTION 2.800 -.100 .375 8 BIT 8 BOTTOM VIEW SIDE VIEW

ELECTRICAL SPECIFICATIONS (typical @ 25°C, ±15 VDC unless otherwise specified)

DIGITIAL INTO TO.	DIGI	TAL	INPU	TS:
-------------------	------	-----	------	-----

Linearity

Temperature Coefficient

1

BIGITITE IIII OTOI		
Resolution	Optional 6, 8, or 10 Binary Bits Parallel data in Straight Binary input format	+15VDC, ±0. -15VDC, ±0.5
Data Inputs	Binary "0" \leq +0.8V (Switch off) Binary "1" \geq +2.0V (Switch on)	Power Supply Ratio
Voltage Input Code Output	DTL or TTL compatible, positive logic	PHYSICAL - E Operating Ten
0000000000 0V 1111111111 +5V -1 LSB	Loading; 2 standard TTL loads (See coding chart below)	Range
ANALOG OUTPUT (@25° C)		Storage Tempo Range
Accuracy	±.2% of FS(6&8 Bits); ±.1% of FS (10 Bits)	Relative Humi Size
Output Voltage Range Full Scale Output Output Load	0V to +5V +5V @ 100mA 50 Ohm (min)	Pins
Output Load		Case Material . Weight

250 max. nanoseconds to .1% of

FS (10 Bit)

±60 ppm/° C

±40 ppm/° C

±1/2 LSB

INPUT POWER REQUIREMENTS

+15VDC, -15VDC,			
Power Sup Ratio	 		0.1% per Volt

PHYSICAL - ENVIRONMENTAL

Operating Tem	pera	itur	е	
Range			·	0°C to +70°C (extended operating temperature ranges optionally available)
Storage Tempe	ratu	re		
Range				-55° C to +85° C
Relative Humic	fity			Up to 100% Non-Condensing
Size				2"W X 3"L X 0.375"H
				Plug-in Module
Pins				0.020" Round Gold Plated
				0.250" Long, min.
Case Material.				Black Diallyl Phthalate Per MIL-M-14
Weight				4 oz.
Mating Socket				Model DILS-2 2 Req'd per module,
				\$4 per pair

DATEL

INPUT CODING FOR DAC-HV-100 SERIES

STRAIGHT BINARY INPUT		ANALOG OUTPUT (+5V, FS)	
6 8 10	6 BIT DAC-HV6B-100	8 BIT DAC-HV8B-100	10 BIT DAC-HV 10B-100
111111 11 11	+4.9219V	+4.9805V	+4.9951V
110000 00 00	+3.7500V	+3.7500V	+3.7500V
100000 00 00	+2.5000V	+2.5000V	+2.5000V
010000 00 00	+1.2500V	+1.2500V	+1.2500V
000000 00 00	0.0000V	0.0000V	0.0000V

ORDERING INFORMATION

				6
MODEL	NUMBER OF BITS	PRICE (1-9)	OPTIONS*	
DAC-HV6B-100	6 BINARY BITS	\$169.	-EX (-25° C to +85° C)	
DAC-HV8B-100	8 BINARY BITS	\$179.	-EXX (-55°C to +85°C)	
DAC-HV10B-100	10 BINARY BITS	\$189.		
			 (Extended operating temperature ranges) 	



GENERAL PURPOSE, HIGH PERFORMANCE DIGITAL TO ANALOG CONVERTERS

DAC-R, DAC-TR SERIES

FEATURES

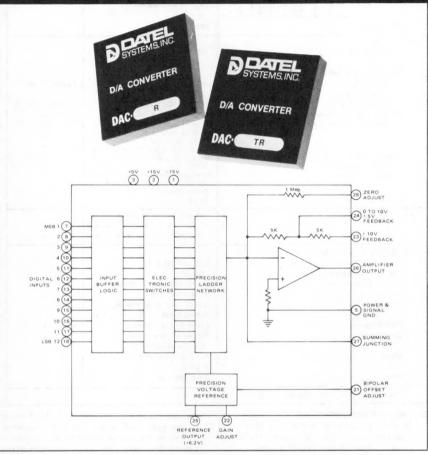
- ▶ 8, 10, 12 Bit Resolutions
- ▶ 5 µ sec Settling Time
- 5 Voltage Output Ranges
- ► Temp. Coeff. to 7ppm/°C
- 2 x 2 x .375 Inch Module

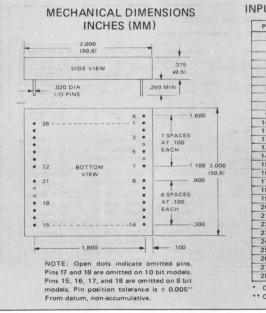
GENERAL DESCRIPTION

The DAC-R and DAC-TR series digital to analog converters feature high performance voltage outputs for 8, 10, and 12 bit resolutions. There are 5 different output voltage ranges which can be selected by external pin connection: 0 to +5V, 0 to +10V, -2.5V to +2.5V, -5V to +5V, and -10V to +10V. Internally these models contain input buffer logic and an electronic switch array, a precision resistor network, a precision stable zener voltage reference, and an output amplifier.

The output voltage settling time is 5 µsec. to specified accuracy, resulting in an update rate of 200kHz. The output can drive a load up to 5mA on the 0 to +10V and -10 to +10V ranges and up to 10mA on the other ranges. Input coding is complementary binary or complementary BCD for unipolar operation and complementary offset binary for bipolar operation. The logic inputs are DTL/ TTL compatible. External offset and gain adjustments are made using two 100K ohm trimming pots., resulting in an accuracy of .01% FS±1/2 LSB. The DAC-R models have a gain temperature coefficient of 30 ppm/°C while the DAC-TR models feature an exceptionally low coefficient of 7 ppm/°C.

These converters are encapsulated in compact 2 x 2 x .375 inch modules with DIP compatible .100" pin spacing. Pins are .020" diameter gold plated. Input power requirements are +5VDC and \pm 15 VDC and are available from Datel Systems' broad line of modular power supplies. Extended temperature range versions are also available by consulting the factory.

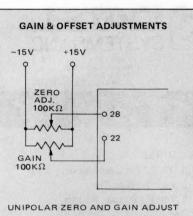




INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
к	KEY
1	-15 Volt Power Input
2	+ 15 Volt Power Input
3	+ 5 Volt Power Input
4	No Connection (pin is omitted)
5	Power and Signal Ground
6	No Connection (pin is omitted)
7	Bit 1 (MSB)
8	Bit 2
9	Bit 3
10	Bit 4
11	Bit 5
12	Bit 6
13	Bit 7
14	Bit 8
15	Bit 9*
16	Bit 10*
17	Bit 11* **
18	Bit 12* **
19	No Connection (pin is omitted)
20	No Connection (pin is omitted)
21	Bipolar Offset
22	Full Scale Gain Adjust
23	± 10V Feedback
24	0 to +10V, ±5V Feedback
25	Reference Output
26	Amplifier Output
27	Summing Junction
28	Zero Adjust

SPECIFICATIONS (Typical @ 25°C unless otherwise noted))	DAC-R	DAC-TR	
INPUTS Resolution Coding, Unipolar Output Coding, Bipolar Output					8, 10, 12 Bits Complementary Binary Complementary BCD Complementary Offset Binary	* * *	
Input Logic	Input Code "1" "0"	Voltag Min. +2V 0V	e Input Max. +5.5V +0.8V	Bit Status OF F ON	DTL/TTL Compatible One TTL Load/Bit	*	
Update Rate					200 kHz	*	
Update Rate					Adj. to .01% FS ±% LSB ±% LSB $30 \text{ ppm/}^{\circ} \text{C of FS}$ $10\mu \text{V/}^{\circ} \text{C}$ $100\mu \text{V/}^{\circ} \text{C}$ 0 to +10V @ 5mA max. 0 to +5V @ 10mA max. -5V to +5V @ 10mA max. -10V to +10V @ 5mA max. 2.5V to +2.5V @ 10mA max. $5 \mu \text{sec to } \pm.01\% \text{ of FS}$ $.02\Omega$ Precision temperature compensated, derived from Zener diode 20 ppm/%	* * 7 ppm/°C of F: * 20µV/°C * * * * *	
POWER REQUI	REMEN	ит			+5VDC ±.25V @ 30mA max, +15VDC ±.5V @ 35mA max, -15VDC ±.5V @ 45mA max.	* * *	
PHYSICAL-EN Operating Te Storage Tem, Relative Hun Size Pins Case Material Construction Mating Socke Weight	mperature nidity .	re Range Range	ge	· · · · · · · · · · · · · · · · · · ·	0° C to +70 $^{\circ}$ C -55 $^{\circ}$ C to +85 $^{\circ}$ C Up to 100% non-condensing 2" x 2" x .375" 0.020" dia, round, gold- plated brass, .250" long, min. Black Diallyl Phthalate Epoxy-encapsulated (fully repairable) DILS-2, 2 per module @ \$5/pr. 2 oz. (56,7g)		



-15V +15V OFFSET ZERO ADJ. 100KΩ 0 28 0 27 0 22 GAIN 100KΩ 0 21

OUTPUT VOLTAGE RANGE EXTERNAL PIN-STRAPPING

FULL SCALE OUTPUT RANGE	CONNECT PINS	THE FOLL	
-2.5V to +2.5V	21, 23 & 27	24 & 26	
-5V to +5V	21 & 27	24 & 26	See.
-10V to +10V	21 & 27	23 & 26	N.S. S.W.
0 to +5V	23 & 27	24 & 26	21 & 5
0 to +10V	24 & 26	21'& 5	

CALIBRATION PROCEDURE

1. Refer to the unipolar and bipolar adjustment diagrams and the coding tables. Note that

complementary binary coding is used. 2. OFFSET OR ZERO ADJUSTMENT: Set all digital inputs high (+2.0V to +5.5V). For unipolar output adjust the zero trimming potentiometer for zero output voltage. For bipolar operation adjust the offset trimming potentiometer to give -FS output voltage as shown

			G TABLES		
UNIPOLAF	OUTPUT - Complem	OUTPUT	GAIN ADJ.	OUTPUT VOL	TAGE RANGE
NO. BITS	DIGITAL INPUT	VOLTAGE	DIGITAL INPUT	0 TO +10V	0 TO +5V
8 Bin 10 Bin 12 Bin	1111 1111 1111 1111 11 1111 1111 111	0V 0V 0V	0000 0000 0000 0000 00 0000 0000 0000	+9.9609V +9.9902V +9.9976V	+4.9805V +4.9951V +4.9988V
8 BCD 12 BCD	1111 1111 1111 1111 1111	0V 0V	0110 0110 0110 0110 0110	+9.9000∨ +9.9900∨	+4.9500V +4.9950V

BIPOLAR OUTPUT - Complementary Offset Binary

NO. BITS	OUTPUT VOLTAGE RANGE	OFFSET ADJ. DIGITAL INPUT	OUTPUT VOLTAGE	GAIN ADJ. DIGITAL INPUT	OUTPUT VOLTAGE
8		1111 1111	-2.5000V	0000 0000	+2.4805V
10	±2.5V	1111 1111 11	-2.5000V	0000 0000 00	+2.4951V
12		1111 1111 1111	-2.5000V	0000 0000 0000	+2.4988V
8		1111 1111	-5.0000V	0000 0000	+4.9609V
10	±5V	1111 1111 11	-5.0000V	0000 0000 00	+4.9902V
12		1111 1111 1111	-5.0000 V	0000 0000 0000	+4.9976V
8		1111 1111	-10.0000V	0000 0000	+9.9219V
10	±10V	1111 1111 11	-10.0000V	0000 0000 00	+9.9805V
12		1111 1111 1111	-10,0000V	0000 0000 0000	+9.9951V

in the coding table.

3. GAIN ADJUSTMENT: Set all digital inputs low (0V to +0.8V) and adjust the gain trimming potentiometer to give +FS output voltage as shown in the coding table.

DAC-B	
DAC-TR	
NUMBER O	F BITS AND CODING
8B = 8 BIT CO	MPLEMENTARY BINARY
10B = 10 BIT CO	MPLEMENTARY BINARY
12B = 12 BIT CO	MPLEMENTARY BINARY
8D = 2 DIGIT	COMPLEMENTARY BCD
12D = 3 DIGIT	COMPLEMENTARY BCD
PRICES (1-9)	
DAC-R8B \$69.0	00 DAC-TR8B \$129.00
DAC-R10B \$75.0	00 DAC-TR10B \$159.00
DAC-R12B \$79.0	00 DAC-TR12B \$179.00
DAC-R8D \$69.0	00 DAC-TR8D \$129.00
DAC-R12D \$79.0	DO DAC-TR12D \$179.00
MATING SOCKE	T DILS-2 (2 per module
VIA TING SOURE	DILO-2 12 per modure



16 BINARY BIT D/A CONVERTER-\$109. SINGLE QUANTITY DIGITAL TO ANALOG CONVERTERS

DAC-169 SERIES

FEATURES

- High Resolution One Part In 65,535
- 4 Digit BCD Version
- 3 Selectable Voltage Outputs
- 2 Selectable Current Outputs

GENERAL DESCRIPTION

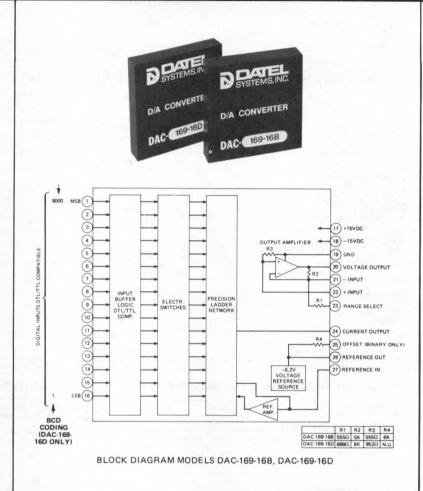
The DAC-169 series Digital-to-Analog Converters are low cost, moderate performance 16 binary bit or 4 digit BCD units contained in compact modular form, 2"Lx2"Wx0.375"H case, ideal for 0.5 inch card spacing.

Both models offer selectable current and voltage outputs. The user selects the desired output by externally jumping selector pins on the unit. There are five available output ranges for the 16 binary bit unit and three output ranges for the 4 digit BCD model.

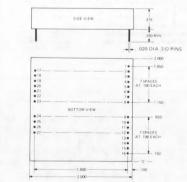
Input digital coding is straight binary or binary coded decimal for unipolar operation and offset binary for bipolar applications. DAC-169 series were specifically designed for incorporation in systems and equipment demanding a wide dynamic range. For example, with a full scale output of ten volts, DAC-169 can resolve down to 150 microvolts, a 96.3 db change.

Output settling time is specified at 750 nanoseconds and 30 microseconds for current and voltage outputs respectively. Output settling time is defined as that time between the application of an input digital word and the output settling to $\pm 0.005\%$ of full scale, and it includes switch delay, nonlinear slewing time and final exponential decay time.

Full scale output ranges for the binary version are 0 to +10V, 0 to -10V, or +5V @ \pm 5ma. The current output can be selected for 0 to +2ma or \pm 1ma. The BCD model can have a full scale voltage output of 0 to +10V or 0 to -10V @ 5ma. The current output can be pin strapped for 0 to +1.25ma full scale.



MECHANICAL DIMENSIONS (INCHES)



INPUT/OUTPUT CONNECTIONS

PIN	DAC-169-16B FUNCTION	DAC-169-16D FUNCTION	PIN	DAC-169-16B FUNCTION	DAC-169-16D FUNCTION
1	BIT 1 (MSB)	BIT 8000 (MSB)	15	BIT 15	BIT 2
2	BIT 2	BIT 4000	16	BIT 16 (LSB)	BIT 1 (LSB)
3	BIT 3	BIT 2000	17	+15 VDC POWER INPUT	+15 VDC POWER INPUT
4	BIT 4	BIT 1000	18	-15 VDC POWER INPUT	-15 VDC POWER INPUT
5	BIT 5	BIT 800	19	COMMON GROUND	COMMON GROUND
6	BIT 6	BIT 400	20	VOLTAGE OUTPUT	VOLTAGE OUTPUT
7	BIT 7	BIT 200	21	-INPUT	-INPUT
8	BIT 8	BIT 100	22	+INPUT	+INPUT
9	BIT 9	BIT 80	23	RANGE SELECT	RANGE SELECT
10	BIT 10	BIT 40	24	CURRENT OUTPUT	CURRENT OUTPUT
11	BIT 11	BIT 20	25	OFFSET (BINARY MODELS ONLY)	N/A
12	BIT 12	BIT 10	26	REFERENCE OUT	REFERENCE OUT
13	BIT 13	BIT 8	27	REFERENCE IN	REFERENCE IN
14	BIT 14	BIT 4			

PARAMETERS	MODEL DAC-169-16B	MODEL DAC-169-16D		
DIGITAL INPUTS	16 Binery Bits	4 Digit BCD		
CODING	Straight Binary (Unipolar Output)	BCD (8-4-2-1) (Unipolar Output)		
Parallel data in the following formats	Offset Binary (Bipolar Output)			
DATA INPUTS				
nput V Input Bit Code Min. Max. Status "0" 0V +0.8V OFF "1" +2.0V +5.5V ON	DTL or TTL competible positive TRUE logic LOADING: One Standard TTL Load	DTL or TTL compatible positive TRUE logic LOADING: One Standard TTL Load		
UPDATE RATE Voltage output limited by output amplifier settling time	5 MHz typical	5 MHz typical		
ANALOG OUTPUT (@25°C)				
ACCURACY	Adj. to 0.005% of F.S.	Adj. to 0.005% of F.S.		
INEARITY	±0.005% of F.S. (4)	±0.005% of F.S. (4)		
INEARITY TEMPERATURE COEFFICIENT	±0.0005%/°C	±0.0005%/°C		
EMPERATURE COEFFICIENT (GAIN)	±10ppm/°C (1), ±15ppm/°C (5)	±10ppm/°C(1), ±15ppm/°C (5)		
TEMPERATURE COEFFICIENT (OFFSET)	$\pm 50 \ \mu V/^{\circ}C \ typ \ (+10V), \pm 10 \ \mu V/^{\circ}C(-10V, \pm 5V)$	$\pm 50 \ \mu V/^{\circ}C \ typ \ (+10V), \pm 10 \ \mu V/^{\circ}C(-10V, \pm 5V)$		
TYPE OF OUTPUT	Current or Voltage	Current or Voltage		
OUTPUT Current output configuration	Externally selectable 0 to +2.0 mA or ±1 mA	0 to +1.25mA		
Voltage out configuration	Externally selectable 0 to +10V, 0 to -10V, or ±5V	Externally selectable 0 to +10V or 0 to -10V		
OUTPUT LOADING Current output configuration	555 Ohms for +1.0V output 1.57K Ohms for ±1.0V output	952 Ohms for +1.0V output		
Voltage output configuration	2K Ohms for 0 to +10V or 0 to -10V output 1K Ohms for ±5V output	2K Ohms for 0 to +10V or 0 to -10V output		
OUTPUT SETTLING TIME Current output configuration	750 nsec to ±0.005% of F.S.	750 nsec to ±0.005% of F.S.		
Voltage output configuration	30 usec to ±0.005% of F.S.	30 usec to ±0.005% of F.S.		
OUTPUT RESOLUTION				
Current output configuration	30 nA (1LSB)	200 nA (1LSD)		
Voltage output configuration	150 µV (1LSB)	1 mV (1LSD)		
LONG TERM STABILITY	±0.005%/yr.	±0.005%/yr.		
REFERENCE SOURCE	Internal: TC = ±0.0005%/°C (2)	Internal: TC = ±0.0005%/°C (2)		
INPUT POWER REQUIREMENTS	+15VDC ±.5VDC @ 25 mA (excluding output current) -15VDC ±.5VDC @ 25 mA	+15VDC ± 5VDC @ 25 mA -15VDC ± 5VDC @ 25 mA (excluding output current)		
PHYSICAL ENVIRONMENTAL OPERATING TEMPERATURE RANGE	0° C to +70° C	0° C to +70° C		
STORAGE TEMPERATURE RANGE	55°C to +85°C	-55°C to +85°C		
RELATIVE HUMIDITY	Up to 100% non-condensing	Up to 100% non-condensing		
SIZE	2"'Lx2"Wx0.375"H plug-in module	2"Lx2"Wx0.375"H plug-in module		
PINS	0.020" round gold plated 0.250" long minimum	0.020" round gold plated 0.250" long minimum		
CASE MATERIAL	Black Diallyl Phthalate (3)	Black Diallyl Phthalate (3)		
WEIGHT	2 02.	2 02.		
PRICE (1-9)	\$109.00 Each	\$109.00 Each		
MATING SOCKET	DILS-2 (2 per module) \$5.00 per pair	DILS-2 (2 per module) \$5.00 per pair		

INPUT DIGITAL CODING TABLE FOR DAC-169 SERIES

ADJUST	BINARY INPUT WOR (16 BINARY BITS)		ANALOG OUTPUTS						
MENT	MSB L	SB 0 to +2mA	±1mA	0 to +10V	0 to -10V	±5V			
GAIN	111111111111111111	+1.99997m	+.99997mA	+9.99985V	-9.99985V	-4.99985V			
N/A	100000000000000000000000000000000000000) 1mA	OA	+5V	-5V	ov			
OFFSET	000000000000000000000000000000000000000	OmA	-1mA	ov	ov	+5V			

ADJUST	4 DIGIT BCD (8-4-2-1) INPUT WORD	ANALOG OUTPUTS			
MENT	MSB LSB	0 to +1.25mA	0 to +10V	0 to -10V	
GAIN	1001 - 1001 - 1001 - 1001	+1.2499mA	+9.999V	-9.999V	
OFFSET	0000 - 0000 - 0000 - 0000	0mA	ov	ov	

OUTPUT RANGE SETTING TABLE

MODEL	OUTPUTS		EXTERNALLY	O AN	EXTERNAL	STMENT U	METER (3)	PINS
NUMBER	F.S. VALUE	AT	PINS	VALUE	HIGH END	WIPER	LOW END	USED
	0 to +2mA	24	19 to 25	N/A	-	-	-	20, 21, 22, 23
DAC- 169-16B	· 1mA	24	N/A	500Ω	to pin 24	to pin 25	to wiper	20, 21, 22, 23
(INPUTS)	0 to +10V	20	19 to 23 to 25. 22 to 24	100ΚΩ	10 pin 17	thru 1MΩ to pin 22	to pin 18	N/A
	0 to -10V	20	21 to 24, 19 to 25	100ΚΩ	10 pin 17	thru 1MS2 to pin 22	to pin 18	N/A
	+5V	20	21 to 24, to 25	100KΩ	to pin 17	thru 1MΩ to pin 22	to pin 18	N/A
DAC-	0 to +1.25mA	24	N/A	N/A		-	-	20, 21, 22 23, 25
(BCD	0 to +10V	20	19 to 23, 22 to 24	100ΚΩ	to pin 17	thru 1MΩ to pin 22	to pin 18	25
	0 to -10V	20	21 to 24	100ΚΩ	to pin 17	thru 1MΩ to pin 22	to pin 18	25

EXTERNAL GAIN POTENTIOMETER FOR ALL OUTPUT CONFIGURATIONS 500Ω (27)

(3) Use cermet type trimpots < 100ppm/° C Detel model TP500 trimpot - \$3.00 each.

CALIBRATION PROCEDURE

- (1) Make the appropriate connections as shown in the output range setting table.
- (2) OFFSET ADJUSTMENT
 Refer to the Input Digital Coding Table and connect the appropriate digital input.

 Adjust the offset potentiometer in order to bring the analog out-
 - Adjust the offset potentiometer in order to bring the analog ou put to the corresponding value as shown in table.
- (3) GAIN ADJUSTMENT Befer to the Input Digital (

(26)

Refer to the Input Digital Coding Table and connect the appropriate digital input.

Adjust the gain potentiometer in order to bring the analog output to the corresponding value as shown in table.



16 BINARY BIT RESOLUTION DIGITAL TO ANALOG CONVERTERS

DAC-HR SERIES

FEATURES

- Output Dynamic Range of 96db
- 1.5ppm/°C Temperature Coefficient
- ▶ ±0.0015% Accuracy
- ▶ 1 µsec Output Settling Time (.0015%FS)
- ▶ ±1/2 LSB Linearity
- ▶ 2"Wx4"Lx0.4"H

GENERAL DESCRIPTION

The DAC-HR series Digital-to-Analog converters are characterized by a resolution of up to one part in 65,535, with a linearity error of $\pm 0.0015\%$ and the lowest temperature coefficient of any commercially available D/A converter of 1.5ppm/° C.

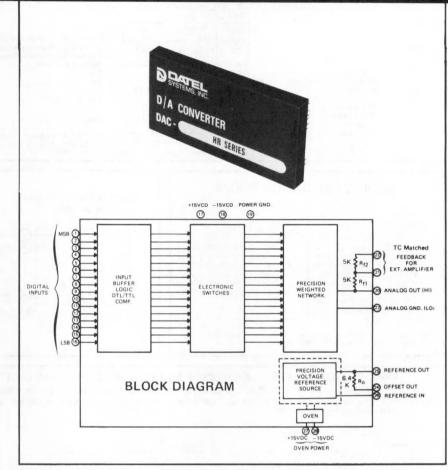
DAC-HR's excellence in both linearity and stability has been achieved by utilizing a precision thin film resistor ladder network which tracks to within 1ppm/°C; an oven controlled zener reference which exhibits a temperature coefficient of 0.25ppm/°C and is current controlled within a high gain servo loop; plus the use of four individual monolithic quad switches. These switches all being in close proximity on the same monolithic chip, have beta's which tend to track, both initially and with temperature. Also, the superior uniformity of these monolithic transistor switches leads to inherently high accuracy of matching thus requiring minor trimming.

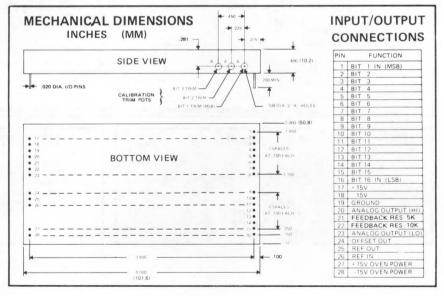
The DAC-HR series are completely self contained in a 2''Wx4''Lx0.4''H plastic encapsulated module, yet fully repairable – a very significant consideration.

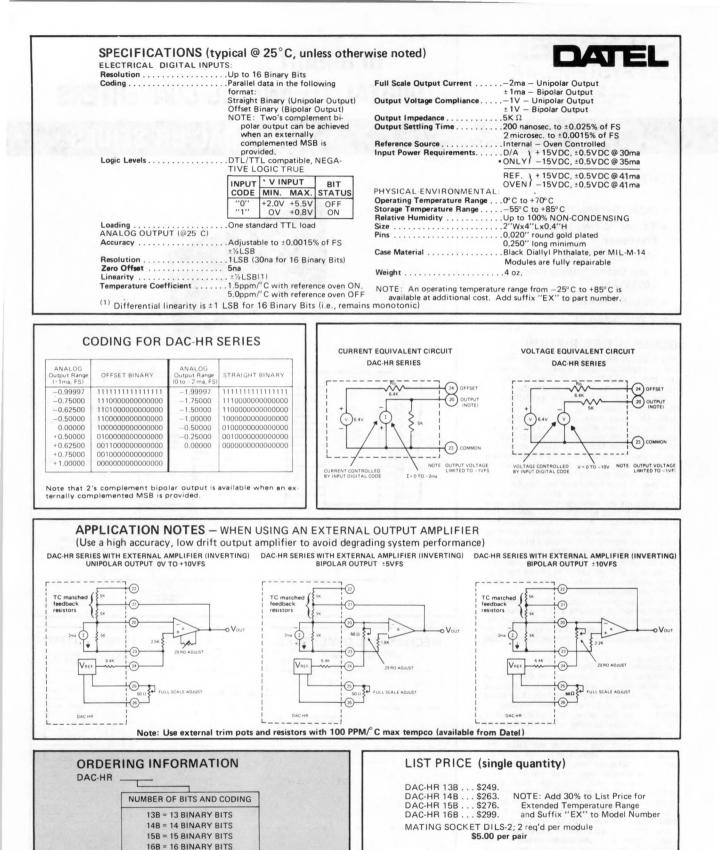
DAC-HR series were specifically designed for incorporation in systems and equipment demanding a wide dynamic range. For example, with a full scale output of one volt, DAC-HR can resolve down to 15 microvolts, a 96.3db change.

The output settling time is specified at 200 nanoseconds to 0.025% of full scale, and a maximum of 2 microseconds to 0.0015% of full scale. Output settling time is defined as that time between the application of an input digital word and the output settling to 0.0015% of full scale, it includes switch delay, nonlinear slewing time and final exponential decay time.

DAC-HR series may be used for either unipolar or bipolar applications. For unipolar operation full scale output is 0 to -2ma and \pm 1ma for bipolar output. Maximum voltage compliance is \pm 1V. Provisions have been provided for the user to connect an external operational amplifier for scaling, sign inversion, impedance transformation, etc. Feedback and offset resistors are included internally. These resistors have temperature coefficients matched to the ladder network. The values of the internal feedback and offset resistors are set to produce a unipolar (0V to +10V) or bipolar (\pm 5V or \pm 10V) output from an external amplifier. The amplifier should be selected to suit particular applications.





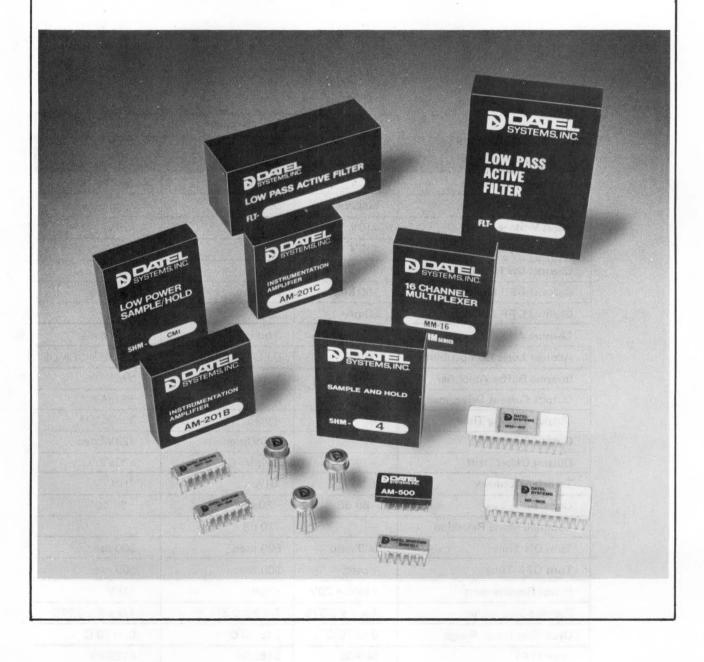


Electronic Design's



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

Data Conversion Accessory Circuits



Analog Multiplexers

	Modular MM-8	Modular MMD-8	Modular MM-16
Number of Channels	8	8	16
Type Input	Sing. End.	Differ.	Sing. End.
Input Voltage Range	±10V	±10V	±10V
Input Overvoltage, max.	±15V	±35V	±35V
Channel ON Resistance	300 ohms	2К	2К
Channel OFF Resistance	100 Meg.	200 Meg.	200 Meg.
Channel OFF Leakage	30 pA	30 pA	30 pA
Channel Addressing	3 bit code	3 bit code	4 bit code
Address Logic Compatibility	DTL/TTL	DTL/TTL/CMOS	DTL/TTL/CMOS
Internal Buffer Amplifier	No	Yes	Yes
Output Current Drive, max.	-	±10 mA	±5 mA
Output Settling Time	-	4 μsec. (1)	3 µsec. (1)
Output Slew Rate	-	100V/µsec.	120V/µsec.
Output Offset Drift	-	±60µV/°C	±30µV/°C
Transfer Accuracy	.01%	.01%	.01%
Crosstalk	- 80 dB	– 80 dB	- 80 dB
Common Mode Rejection	-	110 dB	-
Turn ON Time	300 nsec.	500 nsec.	500 nsec.
Turn OFF Time	1 μsec.	500 nsec.	500 nsec.
Power Requirement	+15V, -20V	±15V	±15V
Package Size, inches	1 x 2 x 0.375	2 x 2 x 0.375	1.5 x 2 x 0.375
Operating Temp. Range	0 to 70°C	0 to 70°C	0 to 70°C
Price (1-9)	\$69.00	\$169.00	\$129.00

Vol 3/106

NOTES: 1. For 20V step to .01% See inside back cover for DATEL sales offices

Electronic Design's

This complete line of analog multiplexers offers a choice of operating features and prices for data acquisition system applications. The four modular models offer 8 and 16 channel capability. The MMD-8 is an 8 channel model with differential inputs and output and an internal differential buffer amplifier. The MM-16 features single-ended 16 channel operation and also includes an internal buffer amplifier.

The four monolithic models use dielectrically isolated CMOS circuitry. The analog and digital inputs are protected from both the loss of power and from overvoltages that exceed the power supplies. The CMOS FET analog channel switches have fast settling time, low capacitance, low leakage current, and high OFF resistance. These monolithic devices offer 4, 8, and 16 channel single-ended operation and 8 channel differential operation at economical prices. Channel addressing is done by a 2, 3, or 4 bit binary code, depending on the particular model. There is also an inhibit input which enables or disables the multiplexer.



Modular	Monolithic	Monolithic	Monolithic	Monolithic
MM-16-1	MXD-409	MX-808	MXD-807	MX-1606
16	4	8	8	16
Sing. End.	Differ.	Sing. End.	Differ.	Sing. End.
±10V	±15V	±15V	±15V	±15V
±35V	±35V	±35V	±35V	±35V
2K	1.5K	1.5K	1.5K	1.5K
200 Meg.	200 Meg.	200 Meg.	200 Meg.	200 Meg.
30 pA	30 pA	30 pA	30 pA	30 pA
4 bit code	2 bit code	3 bit code	3 bit code	4 bit code
DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS
No	No	No	No	No
-		0	-	-
-			-	
- 100 a	-	- 9-1.18	-	-
-	-	A Electronica	-	-
.01%	.01%	.01%	.01%	.01%
– 80 dB	-86 dB	—86 dB	—86 dB	—86 dB
	120 dB	-	120 dB	- Allegative as
500 nsec.	500 nsec.	500 nsec.	500 nsec.	500 nsec.
500 nsec.	300 nsec.	300 nsec.	300 nsec.	300 nsec.
±15V	±15V	±15V	±15V	±15V
1.5 x 2 x 0.375	16 Pin DIP	16 Pin DIP	28 Pin DIP	28 Pin DIP
0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
\$119.00	\$14.00	\$14.00	\$34.00	\$34.00



4,8, AND 16 CHANNEL CMOS MULTIPLEXERS

MX SERIES

FEATURES

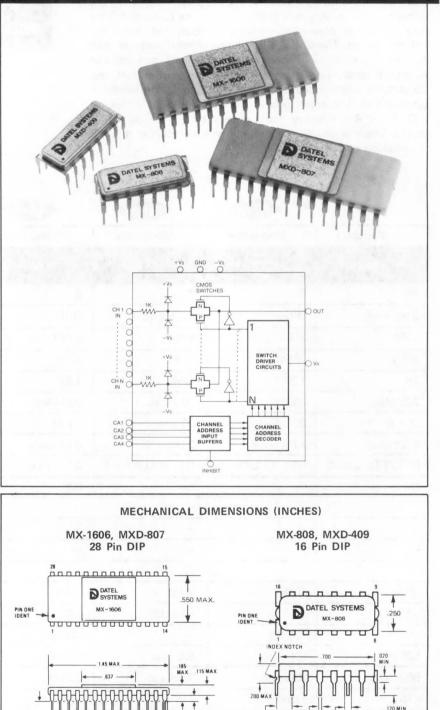
- Dielectrically Isolated CMOS
- Break-Before-Make Switching
- Single-Ended and Differential
- Overvoltage Protection
- DTL/TTL/CMOS Compatible
- 7.5 mW Standby Power

GENERAL DESCRIPTION

The MX series analog multiplexers are 4, 8, and 16 channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/ CMOS compatible and address the proper channel by means of a 2, 3, or 4 bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-beforemake switching to insure that no two channels are ever momentarily shorted together.

Transfer accuracies of .01% can be achieved at channel sampling rates up to 200 kHz and over ±10V signal ranges. These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. Channel ON resistance is typically 1.5K at 25°C and is less than 2K over the operating temperature range.

Power consumption is only 7.5 mW at standby and 15 mW at 100 kHz switching rate. Power supply range is \pm 5V to \pm 20V. The devices are packaged in 16 pin or 28 pin DIP's and operate over the 0°C to 70°C temperature range.



045

100 TYP

NON-CUMULATIVE

018

			and an area of the second s	
27 DV(259004-)3%4.4	MX-808	MX-1606	MXD-409	MXD-807
ANALOG INPUTS		BC JARRY		8-1.X.1
Number of Channels	8	16	4	8
Type Inputs	Single Ended	Single Ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Input Overvoltage, max.	± Vs +20V	± Vs +20V	± Vs +20V	± Vs +20V
Channel ON Resistance	1.5K	1.5K	1.5K	1.5K
Channel ON Resistance, max., 0 to 70°C	2.0K	2.0K	2.0K	2.0K
Channel OFF Input Leakage	30 pA	30 pA	30 pA	30 pA
Channel OFF Output Leakage	1.0 nA	1.0 nA	1.0 nA	1.0 nA
Channel ON Leakage	100 pA	100 pA	100 pA	100 pA
Channel OFF Input Capacitance	5 pF	5 pF	5 pF	5 pF
Channel OFF Output Capacitance	25 pF	50 pF	12 pF	25 pF
DIGITAL INPUTS ¹				
Logic "0" Threshold, max.	+0.8V	+0.8V	+0.8V	+0.8V
Logic "1" Threshold, min. (TTL) ²	+4.0V	+4.0V	+4.0V	+4.0V
Logic "1" Threshold, min. (CMOS) ³	+6.0V	+6.0V	-	
Input Current, max., high or low	5 μΑ	5 μΑ	5 μΑ	5 μΑ
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic "O"	Logic "0"	Logic "0"	Logic "0"
PERFORMANCE				
Transfer Error, max. ⁴	.01%	.01%	.01%	.01%
Crosstalk, 10 kHz	-86 dB	-86 dB	-86 dB	-86 dB
Common Mode Rejection	-	-	120 dB	120 dB
Settling Time, 20V step to 0.1%	2 µsec.	2 µsec.	2 µsec.	2 µsec.
Settling Time, 20V step to .01%	5 µsec.	5 µsec.	5 µsec.	5 µsec.
Turn ON Time	500 nsec.	500 nsec.	500 nsec.	500 nsec.
Turn OFF Time	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break Before Make Delay	80 nsec.	80 nsec.	80 nsec.	80 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
POWER REQUIREMENT			and the second second	
Rated Power Supply Voltage	±15 VDC	±15 VDC	±15 VDC	±15 VDC
Power Supply Voltage Range	±5 to ±20V	±5 to ±20V	±5 to ±20V	±5 to ±20V
Quiescent Current, max.	+5, – 2mA	+5, -2mA	+5, -2mA	+5, -2mA
Power Consumption, 10 kHz sampling	7.5 mW	7.5 mW	7.5 mW	7.5 mW
PHYSICAL-ENVIRONMENTAL				
Operating Temperature Range	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
Storage Temperature Range	– 65 to +150°C	– 65 to +150°C	– 65 to +150°C	-65 to +150°0
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP
Package Dissipation, max.	725 mW	1200 mW	725 mW	1200 mW
PRICE (1-9)	\$14.00	\$34.00	\$14.00	\$34.00

NOTES: 1. The digital inputs are the channel address inputs and the inhibit input.

2. To drive from DTL/TTL circuits 1K pull-up resistors to +5V are recommended.

With models MX-1606 and MXD-807 pin 13 should be left open. 3. For a +6.0V threshold with models MX-1606 and MXD-807 pin 13 is connected to +10V.

4. For output load >20 megohms.

THESE MULTIPLEXERS ARE COVERED BY GSA CONTRACT.

CONNECTION & APPLICATION

PIN CONNECTIONS

CA1 CA2 16 INHIB 15 CA4 -Vs 3 14 GND 4 1 IN 13 +Vs 2 IN -5 12 5 IN 3 IN 6 11 6 IN 4 IN 7 10 7 IN OUT 8 9 8 IN MXD-409 CA2 CAL 16 INHIR -GND 2 15 -Vs +Vs 3 14 1AIN-1B IN 4 13 2A IN -2B IN 5 12 3A IN 3B IN 6 11 4A IN 4B IN 10 A OUT BOUT q

NOTES:

CA = CHANNEL ADDRESS

Vs = SUPPLY VOLTAGE Vr = REFERENCE VOLTAGE NC = NO CONNECTIONS

MX-808

. 28 OUT +Vs -NC · 27 -Vs NC -26 8 IN 16 IN 25 7 IN 15 IN 24 6 IN 14 IN 23 5 IN 13 IN 22 4 IN 12 IN 21 3 IN 11 IN 20 - 2 IN 10 IN 10 19 1 IN 9 IN INHIBIT GND -CA1 Ve 13 16 CA2 CAR 14 15 CAA MXD-807 +Vc-28 AOUT BOUT-27 -Vs NC -26 8A IN 8B IN -25 7A IN 78 IN -24 6A IN 6B IN -23 - 5A IN 5B IN -22 4A IN 4B IN -21 - 3A IN 3BIN-20 2A IN 2B IN -10 19 1A IN 1BIN 18 INHIBIT GND-17 CA1 VR CA2 16 NC 14 15 CA4

MX-1606

TECHNICAL NOTES

- 1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2K ohms max. channel ON resistance, the load impedance should be at least 20 megohms to achieve .01% accuracy. In practice it is recommended that a load impedance of at least 100 megohms be used to minimize errors. This can be done by using a good high gain, high CMR operational amplifier as a buffer (such as Datel's AM-462). Source resistance should be kept as low as possible so that accuracy is not affected; less than 1K ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.
- 2. For differential operation two buffer amplifiers or a good quality instrumentation amplifier (such as Datel's AM-201) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used, and an amplifier with high CMR should be chosen.
- The maximum analog input overvoltage for these models is ± |Vs +20V|. Maximum logic input overvoltage is ± |Vs +4V|.
- 4. Channel expansion is accomplished by use of the inhibit input of the multiplexer. A logic "0" on this input disables the multiplexer. The expansion technique shown in the diagram to the right applies to all of the multiplexer models.
- 5. The reference terminal (VR) sets the noise immunity level of the input logic for models MX-1606 and MXD-807. In most cases this terminal is left open (TTL inputs). For higher level inputs (+6V min.) this terminal should be connected to +10V. When addressing from DTL/TTL logic it is recommended that 1K ohm pull-up resistors to the +5V supply be used.

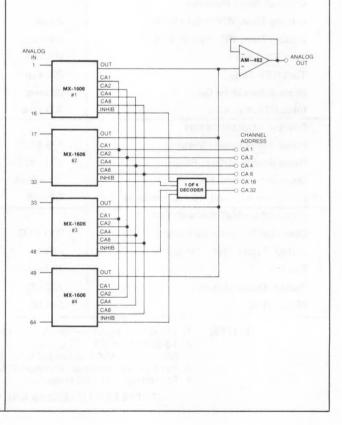
CHANNEL ADDRESSING

MX-1606

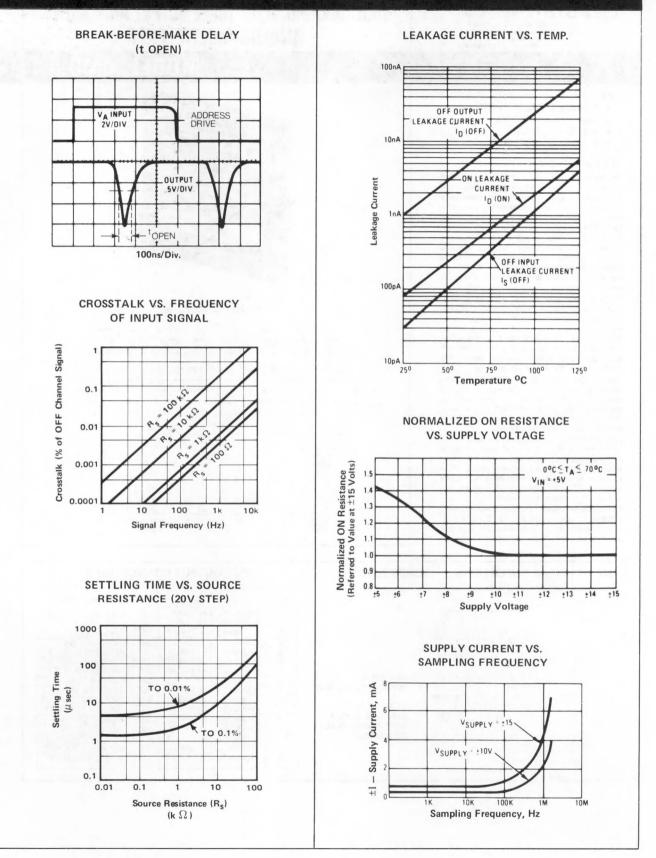
MX-808, MXD-807

8	4	2	1	INHIB.	ON CHANNEL	4	2	1	INHIB.	ON CHANNEL
Х	Х	х	Х	0	NONE	X	Х	х	0	NONE
0	0	0	0	1	1	0	0	0	1	1
0	0	0	1	1	2	0	0	1	1	2
0	0	1	0	1	3	0	1	0	1	3
0	0	1	1	1	4	0	1	1	1	4
0	1	0	0	1	5	1	0	0	1	5
0	1	0	1	1	6	1	0	1	1	6
0	1	1	0	1	7	1	1	0	1	7
0	1	1	1	1	8	1	1	1	1	8
1	0	0	0	1	9	100			MXD	-409
1	0	0	1	1	10	ſ	-	-	L	ON
1	0	1	0	1	11		2	1	INHIB.	CHANNEL
1	0	1	1	1	12		Х	Х	0	NONE
1	1	0	0	1	13		0	0	1	1
1	1	0	1	1	14		0	1	1	2
1	1	1	0	1	15		1	0	1	3
1	1	1	1	1	16		1	1	1	4

EXPANSION TO 64 CHANNELS



PERFORMANCE GRAPHS





8 CHANNEL DIFFERENTIAL—ANALOG TIME SHARING, WITH THREE OUTPUT AMPLIFIERS ANALOG MULTIPLEXER

MODEL MMD-8

FEATURES

- Differential Output Amplifier
- High Transfer Accuracy
- Fast Settling Time
- Break-Before-Make Switching

DESCRIPTION

The Datel Systems Model MMD-8 is a complete analog multiplexer with buffer amplifiers and a differential output amplifier for selectively switching one of eight differential input channels.

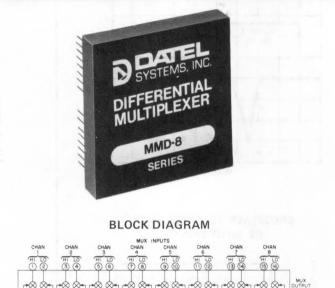
The MMD-8 exhibits excellent transfer characteristics with high speed break-before-make switching. A channel select inhibit (all channels off) is provided so that two MMD-8 multiplexers can be stacked to provide 16 differential input channel multiplexing with a four bit binary address.

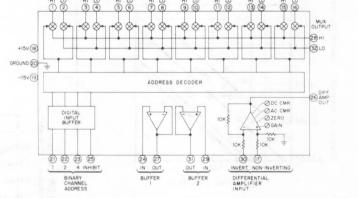
The 1.6 cubic inch module contains an electronic switch array with an associated decoder and digital input buffers, two analog buffer amplifiers and a differential output amplifier. The common differential pair from the switch is brought out through an I/O pin along with the inputs and outputs of the two buffer amplifiers and the differential amplifier.

The MMD-8 can accept differential analog inputs of up to ± 10 volts with a transfer accuracy of 0.01%. Without the amplifiers, the switching time is typically 500 nanoseconds. With the amplifier, the settling time is only 4 microseconds to 0.01% of full scale.

The differential output amplifiers will deliver ± 10 milliamps at ± 10 volts full scale. Linearity of this amplifier is 0.01% with an offset adjustable to less than 1 millivolt and an offset vs. temperature of 60 microvolts per degree centigrade. The amplifiers can be slewed at a rate of 100 volts per microsecond.

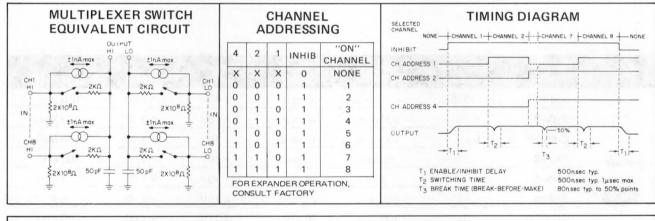
The entire 8-channel differential multiplexer is completely encapsulated in a $2^{\prime\prime}\times2^{\prime\prime}\times.375^{\prime\prime}$ module with dual in-line pinning (0.1 $^{\prime\prime}$ grid) and requires only ±15 volts at ±20 mA max for power.

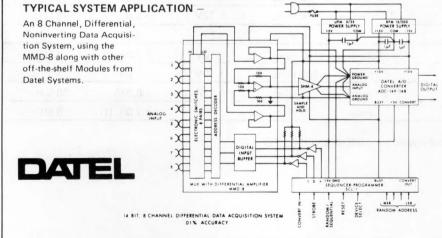




MECHANICAL DIMENSIONS - INCHES (MM) INPUT/OUTPUT CONNECTIONS DIFF AMP GAIN ADJ 0.00 PIN FUNCTION PIN FUNCTION AC CMR ADJ 0375+0010 0.020 DIA DIFF AMP ZERO ADJ 0.200 MIN (5, 1) CHANNEL 1 HI INPUT 17 DIFF, AMP, POS, IN 1 CHANNEL 1 LO INPUT 18 +15V POWER 2.000 ±.015 1.850 3 CHANNEL 2 HI INPUT 19 15V POWER 14----1. CHANNEL 2 LO INPUT PWR & SIG. GND 20 4 TRIM O ADJUSTMENTS CHANNEL 3 HI INPUT 21 ADDRESS INPUT 1 7 SPACES CHANNEL 3 LO INPUT CHANNEL 4 HI INPUT 6 22 ADDRESS INPUT 2 23 ADDRESS INPUT 4 - 1.150 AC CMR ADJ n 24 --- 8 • CHANNEL 4 LO INPUT CHANNEL 5 HI INPUT 24 BUEFER 1 INPUT 8 (SINGLE TURN POTS) BOTTOM VIEW 25 ADDRESS INHIBIT 9 o 25 -0.850 CHANNEL 5 LO INPUT DIFF. AMP. OUTPUT 10 26 15-TURN POTS: CHANNEL 6 HI INPUT BUFFER 1 OUTPUT 27 11 7 SPACES AT 0.100 DIFF AMP ZERO ADJ CHANNEL 6 LO INPUT CHANNEL 7 HI INPUT CHANNEL 7 LO INPUT 12 28 MUX. HI OUTPUT DIFF AMP GAIN ADJ 29 BUFFER 2 INPUT 13 0.150 DC CMR ADJ DIFF. AMP. NEG. IN 14 30 15 CHANNEL 8 HI INPUT 31 **BUFFER 2 OUTPUT** 0.100 (2, 5) 16 CHANNEL 8 LO INPUT 32 MUX. LO OUTPUT - 2.000 ±0.015 (50, 8) -PIN POSITION TOLERANCE:20.005 NON-ACCUMULATIVE

ANALOG INPUT		Enable/Inhibit Delay	300 ns Typ.	
No.# of Inputs	8 channel differential	Break Time (Break before		
Input Voltage Range	±10V	make)	80 ns Typ. to 50% points	
Input Overvoltage	±35V max.	Common mode Voltage	Ein Diff + CMV = ± 10 Vpk	
Input Impedance Without Buffer or Differential amplifier	2k Ohm switch Res. with 50 pf to Gnd. (High & Low inputs)	Common mode rejection ratio, At 0 to 100 Hz	Adjustable for both AC & DC to: 110dB with 1KΩ unbalance	
With Buffer Amplifier	100 meg Ohms (Channel on)	OUTPUT AMPLIFIER CHARAC	TERISTICS	
	200 meg Ohms (Channel off)	Output Voltage	±10V max.	
Leakage	.03 nA typ, from off channels into	Output Current	±10mA max.	
Loundago	source (±20V differential)	Output Loading	$1k\Omega$ in parallel with 1000 pf max.	
Channel Select	3 lines straight binary code (1	Gain	1.000 adjustable	
	through 8 channel select)	Linearity	0.01% of Full Scale	
Inhibit (All channels off)	Logical "O"	Offset (Vout-Vin)	Adjustable to <±1mV	
Input Logic Levels		Offset – vs – Temperature	±60µV/°C	
DTL/TTL/CMOS compatible	INPUT V INPUT	Slew rate	100 V/ µs	
(For TTL compatability use an	CODE MIN. MAX.	Settling Time (20 V step in)	4µs to 0.01% of Full Scale	
open collector device with	"0" 0V +0.8V	Input Power Requirements	±15V @ ±20 mA max.	
resistor pull up to $+5V$).	"1" +4V +15V	PHYSICAL ENVIRONMENTAL		
SWITCHING CHARACTERIST (Independent of Amplifier)	ics	Operating Temperature Storage Temperature	0° to + 70° C -55° C to +85° C	
Switching Time	500 ns typ., 1µSec max.	Relative humidity	Up to 100% non-condensing	
Sequence Rate	500kHz	Size	2" L × 2" W × .375" H	
Crosstalk	@ 10kHz 1 mv p-p @100kHz 4 mv p-p	Price (1–9)	\$169.00	
	@1MHz 40 mv p-p	Mating Socket	DILS-2, 2 reg'd per module, \$5/pr.	





DIFFERENTIAL AMPLIFIER CALIBRATION PROCEDURE

- Ground both the differential amplifier inverting and non-inverting inputs. Adjust the output to zero volts using the ZERO trim as seen on a DC-coupled scope.
- Connect both the inverting and non-inverting inputs to a 100 Hz, 20V pk-pk squarewave source referenced to ground. Adjust the DC CMR trim for minimum output on a DC scope.
- 3. Repeat step 2 but use a 1 kHz sinewave source and adjust the AC CMR for minimum output.
- 4. Ground the inverting input. Connect the noninverting input to a 20V pk-pk, 100 Hz sinewave source. Connect the differential inputs of a calibrated scope between the amplifier's non-inverting input and the amplifier output. Adjust the GAIN trim for minimum output on the scope. Note that the CMR trim is essentially independent of GAIN adjustments but the GAIN is affected by CMR adjustments.

Sample-Holds

	Model	Accuracy	Acquisition Time	Aperture Delay	Voltage Range	Gain	Band-Width
	SHM-1	.025%	5 μsec.	50 nsec.	± 10V	+ 1.00	650 k Hz
	SHM-2	0.1%	100 nsec.	10 nsec.	± 10V	+ 1.00	10 MHz
	SHM-2E	0.1%	100 nsec.	10 nsec.	± 10V	+ 1.00	10 MHz
Modular	SHM-3	.005%	50 µsec.	40 nsec.	± 10V	+ 1.00	100 kHz
	SHM-4	.005%	7 μsec.	40 nsec.	± 10V	+ 1.00	1 MHz
NEW	SHM-5	.01%	350 nsec.	20 nsec.	± 10V	-1.00	5 MHz
	SHM-CM	.01%	100 µsec.	20 nsec.	± 12V	+ 1.00	40 kHz
	SHM-CMI	.01%	150 µsec	20 nsec.	± 12V	-1.00	40 kHz
	SHM-UH	0.25%	50 nsec.	10 nsec.	± 5V	+ 0.95	45 MHz
Monolithic	SHM-IC-1	.01%	5 μsec.	50 nsec.	± 10V	± 1.00 (1)	2 MHz
NEW	SHM-LM-2	0.1%	5 μsec.	100 nsec.	± 10V	+ 1.00	1 MHz
Hybrid	SHM-HU	0.1%	25 nsec.	6 nsec.	± 2.5V	+ 0.975	20 MHz
COMING!	SHM-6	.01%	1 μsec.	20 nsec.	± 10V	± 1.00 (1)	5 MHz

NOTES: 1. Can also be configured for gains greater than ± 1 .

This line of sample-hold devices includes modular, hybrid, and monolithic models and is the most comprehensive line in the industry. The models listed here cover a broad range of applications from ultra-fast and high accuracy down to low cost, moderate performance units.

SHM-1: General purpose, high accuracy model with 5 $\mu \text{sec.}$ acquisition time.

SHM-2, SHM-2E: Very high speed units with open loop circuit to achieve acquisition times as fast as 100 nsec.

SHM-3: A low cost, .005% accuracy model with 50 $\mu {\rm sec.}$ acquisition time.

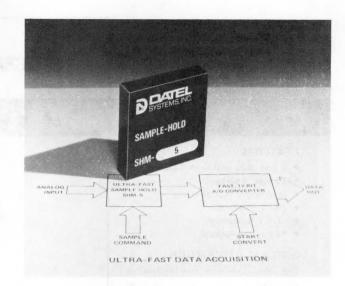
SHM-4: A low cost, .005% sample hold with a faster 7 $\mu \text{sec.}$ acquisition time.

SHM-5: A new ultra-fast sample hold designed for use with fast 10 and 12 bit A/D converters. Acquisition time is 350 nsec. to .01% and 200 nsec. to 0.1%. The SHM-5 also features high input impedance.

SHM-CM, SHM-CMI: These two CMOS models are designed for low power applications such as portable data acquisition systems. They offer inverting or noninverting performance and can operate from a single polarity power supply.

SHM-UH: This ultra-fast model features acquisition time of 50 nsec. and is ideal for use with ultra-fast 8 bit A/D converters such as ADC-UH8B.

SHM-IC-1: This monolithic sample-hold offers excellent performance characteristics for .01% accuracy at a low cost.



SHM-LM-2: This "coming soon" monolithic unit also gives excellent performance at even lower cost.

SHM-HU: This "coming soon" hybrid model is specifically designed for ultra-fast video data conversion applications.

SHM-6: This "coming soon" hybrid unit features .01% accuracy with 1 $\mu sec.$ acquisition time.

Hold-Mode Droop	Tempco	Power Requirement	Case Size (inches)	Price (1-9)	See Page
1 μV/μsec.	20 ppm/°C	+ 15V, - 20V	2 x 1 x 0.375	\$ 69.00	**
50 μV/μsec.	30 ppm/°C	± 15V	2 × 1 × 0.375	\$ 89.00	120
330 μV/μsec.	30 ppm/°C	± 15V	2 x 1 x 0.375	\$ 95.00	120
20 μ V/msec.	30 µ V/⁰C	± 15V	2 × 1.5 × 0.375	\$ 49.00	**
20 μ V/msec.	30 µV/⁰C	± 15́V	2 x 1.5 x 0.375	\$ 59.00	122
20 μV/μsec.	15 ppm/°C	± 15V	2 x 2 x 0.375	\$189.00	**
2 μV/μsec.	30 µV/⁰C	+ 10 to +15V	2 x 2 x 0.375	\$ 89.00	* *
2 μV/μsec.	60 µV/°C	+ 10 to +15V	2 x 1.5 x 0.375	\$ 89.00	**
50 μV/μsec.	50 μV/°C	± 15V, + 5V	2 x 1.5 x 0.375	\$229.00	124
50 μ V/msec.	20 µV/⁰C	± 15V	14 Pin DIP	\$ 19.00	116
200 µV/msec.	40 µV/°C	± 15V	8 Pin TO-99	\$ 7.95	**
20 μV/μsec.	50 μV/°C	± 15V, ± 5V	24 Pin DIP	*	* *
10 μV/μsec.	50 μV/℃	± 15V, + 5V	32 Pin DIP	*	* *

THESE SAMPLE-HOLDS ARE COVERED BY GSA CONTRACT

*To be announced.

** Contact nearest Datel sales office for data sheet.



INTEGRATED CIRCUIT SAMPLE AND HOLD

MODEL SHM-IC-1

FEATURES

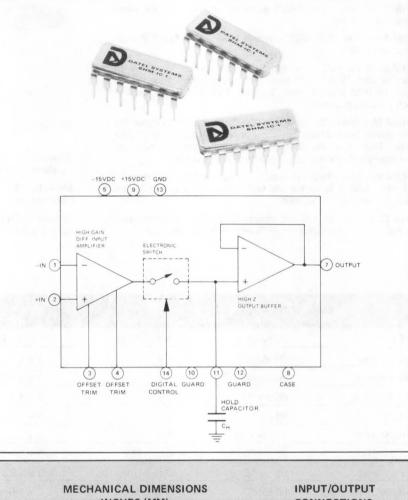
- ▶ 5 µsec. Acquisition to .01%
- ▶ 50 nsec. Aperture
- Inverting or Noninverting
- 2MHz Bandwidth
- ▶ .01% Feedthrough
- ▶ 14 Pin DIP Package

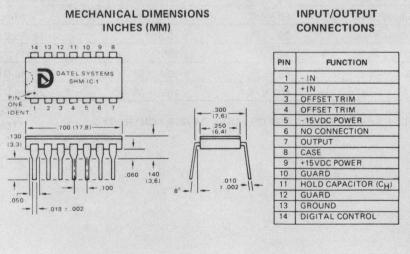
GENERAL DESCRIPTION

The SHM-IC-1 is a new monolithic integrated circuit sample and hold with excellent performance features. It is a self-contained device requiring only an external holding capacitor, the value of which can be chosen by the user to achieve his desired speed and accuracy requirement. The unit consists of a high gain differential input amplifier, a digitally controlled electronic switch, and a high input impedance buffer amplifier. The SHM-IC-1 operates in a closed loop configuration, either inverting or noninverting, with accuracy and speed determined by the input amplifier characteristics and the value of the holding capacitor. The electronic switch is controlled by a DTL/TTL compatible logic input.

The most common configuration for the SHM-IC-1 is a unity gain, noninverting sample and hold. In this configuration the device has a ±10V input and output range with 10⁸ ohms input impedance. Specifications are given for this unit with two different values of holding capacitor, $.001\mu$ F and $.01\mu$ F. The .001 μ F capacitor gives a 4 μ sec. acquisition time to 0.1% for a 10V change, a 2MHz tracking bandwidth and 50mV/sec. maximum hold mode droop. The $.01\mu$ F capacitor gives a 10 usec, acquisition time, 1MHz tracking bandwidth, and 5mV/sec. maximum droop. Characteristics for other values of holding capacitor can be determined from graphs which are shown. The SHM-IC-1 can also be configured as either an inverting or noninverting sample and hold with gain by the use of two external resistors.

This device is housed in a 14-pin hermetically sealed dual-in-line package. Operating temperature range is 0° C to $+75^{\circ}$ C.





SPECIFICATIONS, SHM-IC-1

(Typical at 25°C, ±15V Supplies, unless otherwise noted)

INPUT AMPLIFIER SPECIFICATIONS DC Gain, volts/volt	50K, 25K min. 50nA, 200nA max. 10nA, 50nA max. 3mV, 6mV max. 20 μ V/ $^{\circ}$ C ±10V min. 74dB min. ±30 μ V/ $^{\circ}$ max. 2MHz
GENERAL SPECIFICATIONS, SAMPLE & HOLD, G = +1 Input Voltage Range Input Impedance Output Voltage Range Output Voltage Range Output Voltage Range Output Urrent, S.C. protected Output Impedance Aperture Delay Aperture Uncertainty Gain Error, sampling mode Hold Mode Noise Digital Input, Sample Mode, DTL/TTL Hold Mode, DTL/TTL	± 10V min. 10 ⁸ ohms ± 10V min. ± 10mA min. 0.2 ohm 50 nsec. 5 nsec. .01% max. 350μV RMS 0 to +0.8V @-0.8mA +2.0 to +5.5V @ +20μA
$\begin{array}{l} SAMPLE \& HOLD, G = +1, C_H = .001 \mu F \\ Acquisition Time, 10V to 0.1\% \\ Acquisition Time, 10V to .01\% \\ Bandwidth, small signal, sampling \\ Bandwidth, small signal, sampling \\ Slew Rate \\ Hold Mode Voltage Droop \\ Hold Mode Feedthrough \\ Sample-to-Hold Offset Error, V_{1N = 0} \\ Sample-to-Hold Gain Error, V_{1N = \pm 10V} \\ Sample-to-Hold Nonlinearity Error \\ \end{array}$	4 μsec. 5 μsec. 2.0MHz 5V/μsec. 50mV/sec. max. .01% max. 20mV max. .05% max. of output .01% max. of output
SAMPLE & HOLD, G = +1, C _H = .01 μ F Acquisition Time, 10V to 0.1% Acquisition Time, 10V to .01% Bandwidth, small signal, sampling Slew Rate Hold Mode Voltage Droop Hold Mode Feedthrough Sample-to-Hold Offset Error, V _{IN} = 0 Sample-to-Hold Gain Error, V _{IN} = ±10V Sample-to-Hold Nonlinearity Error	10 μsec. 12 μsec. 1.0MHz 3V/μsec. 5mV/sec. max. .002% max. 2mV max. .005% max. .005% max. .001% max.
PHYSICAL-ENVIRONMENTAL Operating Temperature Range	0° C to +75° C –65° C to +150° C TO-116
PRICE (1-9)	\$19.00

TECHNICAL NOTES

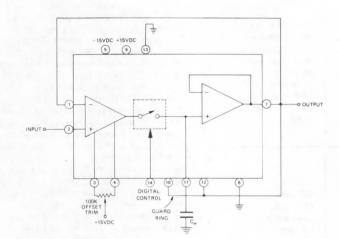
The most commonly used sample and hold configuration for the SHM-IC is the noninverting unity gain circuit. This gives a high input impedance of 10⁸ ohms, and the output voltage in the sample mode follows the input. Specifications are given for this configuration for two values of CH, .001µF and .01µF. The .001µF capacitor gives excellent speed (4 µsec. acquisition) with good hold mode voltage droop (only 50mV/sec. max). For even better speed, a 100 pF capacitor may be used to give an acquisition time of only 2 µsec. The hold mode droop, however, increases by an order of magnitude to 500mV/sec., and the sample-to-hold errors also increase. For excellent accuracy a .01 µF capacitor should be used, giving an acquisition time of 10 µsec., and a hold mode droop of only 5mV/sec. max. Even larger values of holding capacitor can be used with proportionate increases in accuracy but slower speed. The application graphs show the results for the different values.

For best results, C_H should be a good quality capacitor with very high insulation resistance and low dielectric absorption. For temperatures up to +85° C polystyrene type capacitors are recommended. It is also recommended for lowest hold mode droop that a guard ring be used around the C_H terminal (pin 11) in the circuit board layout as shown on the last page. This is done to present leakage to other conductors on the circuit board due to board leakage and contamination. If a large value polystyrene capacitor is used, such as 1 μ F, hold mode droop as low as 20 μ V/sec. (typical) can be achieved with an acquisition time of about 3 milliseconds.

Three error contributions are specified for sample-to-hold errors: offset error, gain error, and nonlinearity error. These sampling errors are caused by a small amount of charge being dumped to or from the holding capacitor by the sampling switch and are reduced by a larger value of CH. It is possible to compensate for these errors by changing the gain and offset elsewhere in the external circuitry for the noninverting unity gain case. For the inverting case, the gain can be accomplished by adjusting the external resistor values and an offset can be applied to pin 2 of the input amplifier. When this external compensation is used, the output will be in error during sampling, but will be accurate in the hold mode. Only the nonlinearity error will remain of the sample-to-hold errors. The offset adjustment of the input amplifiers should be used only to zero the device in the sample mode.

In the inverting gain of one operating mode, the feedback and input resistors should be carefully matched or trimmed to give the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration except that the sampling bandwidth is reduced by a factor of two. Likewise, for higher gain configurations the sampling bandwidth is proportionately reduced.

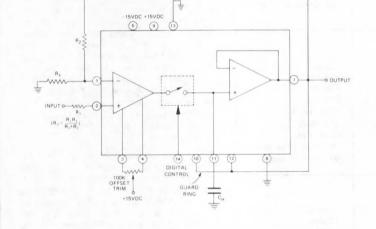
OPERATING MODES



SAMPLE & HOLD, UNITY GAIN, NONINVERTING

GAIN = +1

The 100K ohm offset trimming potentiometer should be a 100 ppm/ $^{\circ}$ C cermet 15 turn type. These are available from Datel Systems at \$3.00 each. To zero, ground input (pin 2) and digital control (pin 14) and adjust 100K offset trim for zero output (pin 7).



SAMPLE & HOLD, NONINVERTING WITH GAIN

 $GAIN = 1 + \frac{R_2}{R_1}$

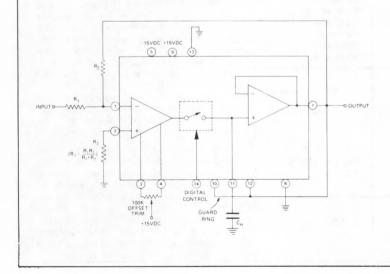
Bandwidth decreases proportionately with gain. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be 100 ppm/°C metal film type resistors.



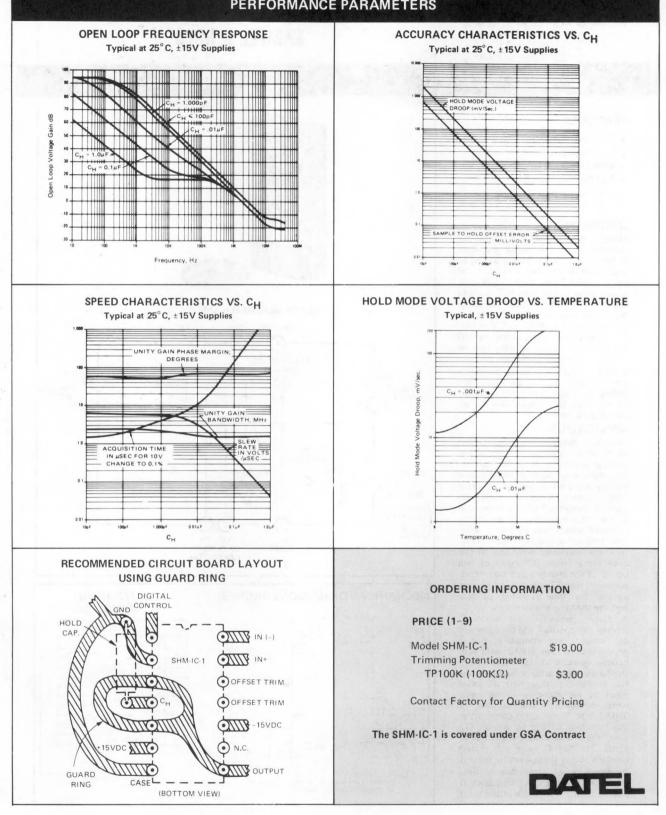
$$GAIN = -\frac{R_2}{R_1}$$

For a gain of -1 the bandwidth is one half of that given for the noninverting mode. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be matched 100 ppm/°C metal film type resistors for a gain of -1. For higher gains the ratio should be matched closely or trimmed with a small value carbon composition type resistor.





PERFORMANCE PARAMETERS





ULTRA FAST / ACCURATE ANALOG STORAGE SAMPLE & HOLD

MODEL SHM-2

FEATURES

- ► Ultra Fast Acquisition Time
- Short Aperture Time
- Wide Frequency Response
- Fast Output Settling
- ► Low Temperature Coefficient

DESCRIPTION

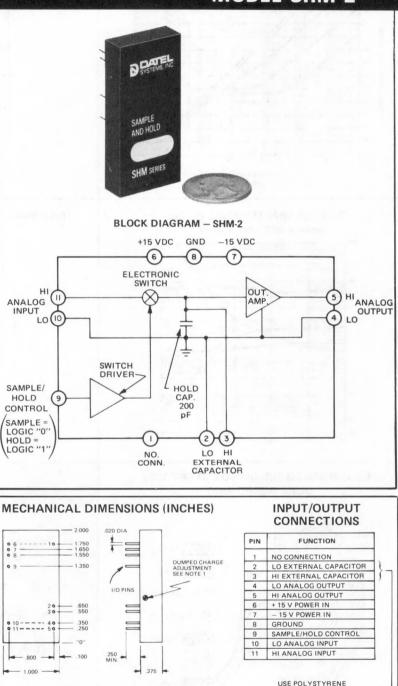
Model SHM-2 Sample and Hold is the ultimate in speed. Designed to operate in conjunction with Datel's analog to digital converters; Series H, P, N, M and L. SHM-2 can track a full scale analog input in less than 100 nsec's to within $\pm 0.1\%$ of full scale accuracy. Additional features include wide frequency response (D.C. to 500 KHz), an aperture uncertainty of less than 10 nsec's and an output settling time of one μ sec to within $\pm 0.1\%$.

SHM-2 is usually connected between a signal source to be quantized and analog to digital converter, providing an excellent throughput rate for an overall data system.

APPLICATION

When digitizing an analog signal which varies with time and having a frequency spectrum, it is difficult to determine what point of this signal is exactly represented by the resultant digital output. Since the maximum time "uncertainty" of the conversion is the total conversion time of the converter which may be called "aperture time or ambiguity time"; therefore, the maximum error due to this uncertainty is the difference of two points of the analog signal under measurement from To to time, T1 representing the time required to convert the changing analog signal.

A faster converter will obviously shorten the aperture and the error will be reduced proportionately, but a device such as the SHM-2 with very narrow aperture characteristics, controlled by command, is far more useful in trying to determine the exact point of the changing analog signal when converting. The purpose of SHM-2 is to "hold" upon command at the beginning of the conversion (To time) the analog voltage applied at its input. The "held" value will remain constant during the conversion process. Relationships of error due to time uncertainty versus input frequency is plotted on the reverse side of this sheet.



1. ADJUST FOR HOLD OFFSET AT VIN - 0 VOLTS

OR GROUNDED ANALOG INPUT

NOTE

TYPE CAPACITOR

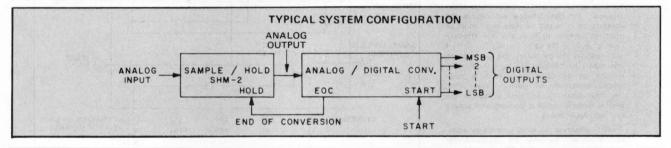
SPECIFICATIONS (Typical @ 25°C unless noted)

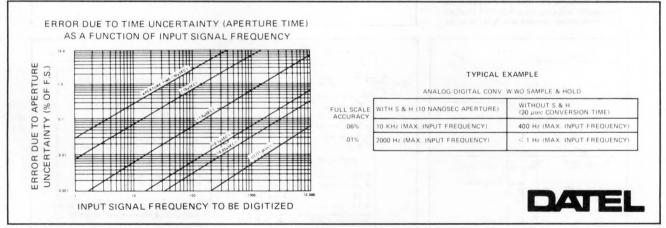
ELECTRICAL

Analog Input: Analog input voltage range .	Up to ±1	0 VFS				
		. ± 15V (max.) with a recovery time of 500 nsec				
Input source current	±2mA bia (Switchin	 ±12mA max drive during transitio ±2mA bias during steady state. (Switching circuit is a diode bridge driven by 2 current sources.) 				
Mode control input	DTL or T logic	TL com	pàtible,	positive		
	Status	Input Code	Vin Min,	put Max.		
	Sample Hold	"0" "1"	0V +2.0V	+0.8V +5.5V		
	Rise and maintain					
Analog Output						
Output voltage range	Up to ±10	VFS				
Output current	• • ±5 mA					
Dynamic Characteristics:						
Bandwidth	@ 3 db po	int				
Acquisition time	. 100 nsec of input s					
	. 10 nsec m	ax. (8 n	sec dela	y, 2 nse		
Aperture time	jitter)					
Aperture time Feedthrough @ any input frequency	jitter)					

Settling time	
Hold decay rate	
	00000
Performance:	
	+ 1.00 Max. to +0.999 Min
Accuracy (@ 25°C)	±0.1% of FS
Linearity	±0.1% of FS
Temperature coefficient	±30 ppm/°C of FS
Long term stability	±0.025%/6 months (gain & offset)
Input power requirements	+15±.5VDC @ 35 ma —15±.5VDC @ 35 ma
PHYSICAL-ENVIRONMENT	AL
Operating temperature range	0°C to +75°C
Storage temperature range	-55°C to +85°C
Relative humidity	
Size	2"L x 1"W x 0.375"H plug-in module
Pins	0.020" round gold plated 0.250" long minimum
Case material	Black diallyl phthalate, per MIL-M-14. Fully repairable
Weight	2 oz.
Mating Socket	DILS-2, 2 Req'd., Model SHM-2

Model SHM-2 sample and hold module is fully encapsulated and features dual in-line pinning compatibility (i.e., 0.100" grid pin spacing and 0.800" between rows of pins).







FOR SIMULTANEOUS SAMPLE AND HOLD APPLICATIONS SAMPLE AND HOLD

SHM-4

FEATURES

- ▶ Fast Acquisition Time
- Low Droop
- Adjustable Aperture Delay
- Low Gain Error
- High Input Impedance

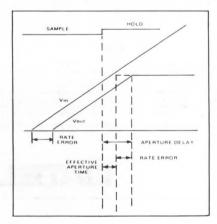
DESCRIPTION

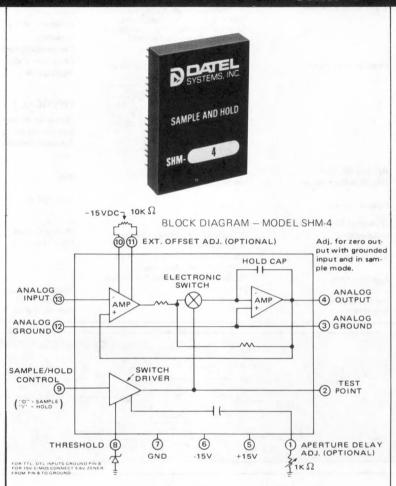
The SHM-4 is ideally suited to simultaneous sample and hold applications, where the gain and aperture delay between units must be matched, and where the output droop of the sampled signal is minimized for time shared A/D conversion.

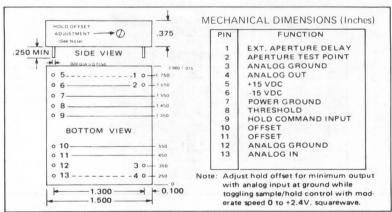
A double inversion circuit in the SHM-4 places the FET sampling switch near ground, which means that all variations of hold step and of aperture delay with input voltage are eliminated.

A unique closed loop design gives high accuracy and allows the rate ${\rm error}^1$ to be factory nulled. Rate error is the delay by which the output lags an input ramp and may be expressed in nsec or in mV/V/µsec. For conventional sample and hold applications rate error is not serious because it merely causes an advance in the effective time of hold and tends to cancel out part of the aperture delay. However, for simultaneous applications the aperture delay minus the rate error must be matched between units so that the effective time of hold is the same for all. The SHM-4 accomplishes this by nulling the rate error to less than 1 nanosecond and for critical applications, by providing an external 5 nanosecond adjustment of aperture delay. Also, the high accuracy and low droop of the SHM-4 make it useful in conventional sample and hold applications.

Careful attention to circuit detail in eliminating leakage currents has decreased the output droop to less than 20 microvolts per millisecond allowing several SHM-4 modules to be time shared between one A/D converter.







Electronic Design's

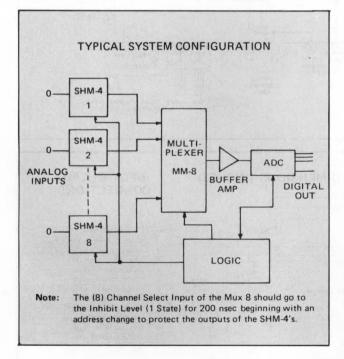
SPECIFICATIONS (typical @ 25° C unless otherwise noted)

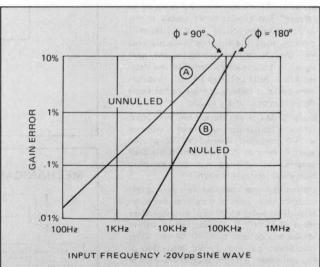
ELECTRICAL



Analog Input		Acquisition Time (1)	
Input Voltage Range	± 10V	Output	to \pm .005% 7 μ sec
Max. Safe Input	± 15V	Max. Current.	±5 mA
Impedance	10 ⁸ ohms in parallel with: 1) 400 nA current source and 2) 33K ohm in series with 20pF. Nominal Limits	Impedance	Output to GND indefinitely +15VDC @ 14 mA max
Sample	0V 0 to +.8V @ -1.5 mA		-15VDC @ 12 mA max
Hold (For 15V C/MOS threshold may be raise 5.6V zener from pin 8 to ground) Sample Offset V, (Vout -Vin) @ Vin = 0	4V +2 to +15V @ +0.1 mA ad to 6.5V with a	PHYSICAL - ENVIRONMENTA Operating Temperature Range Storage Temperature Range	0°C to +70°C
Offset V over temp. range (1)	$\pm 30 \mu \text{V/}^{\circ}\text{C}$	Relative Humidity	Up to 100% non-condensing
Offset V vs Supply Voltage	$\pm 100 \mu \text{V/V}$	Size	2"Lx 1.5"Wx0.375"H plug-in module
Gain Error (offset V vs Vin) Gain Error over temp. range	±.005% ±.001%/70°C	Pins	.020" round gold plated .250" Long Min.
Rate Error (offset V vs dVin/dt) (1) . Bandwidth, 3db, 20V .p-p (1)	200 KHz	Case Material	Black diallyl phthalate, per MIL-M-14
Bandwidth, 3db, 1V .p-p (1) Slew Rate (1)	1.0 MHz 5V/μsec	Weight	3 oz. DILS-2, 2 Reg'd per module,
Settling Time, 20V step, to \pm .05% (1) to \pm .005% (1)	6 μ sec 7 μ sec	land the second	\$5/pr
Noise, wideband	300 μ V rms	Price (1-9)	\$59.00
Hold Step (2)	Int. Adj. to 0	Model SHM-4 sample and hold modu tures dual in-line pinning compatibil	
Peak Transient	400 mV Ext. Adj. 40-45 nsec 1 nsec	NOTES:(1)Source resistance of 5K of (2)Adjust for hold offset at at ground.	
Droop	20 μ V/msec x2/10° C +.01%	ing a 1K ohm pot from p	sed by up to 5 nsec by connect- in 1 to ground and viewing the test point voltage crosses -5V.

Hold to Sample





Curve A represents the SHM-4 before rate error nulling where the rate error is 450 nsec. Curve B shows a nulled production SHM-4. The quadrature error due to the first order pole has been removed leaving only a residual gain error due to a second order pole.



200 PICOSECOND APERTURE TIME SAMPLE & HOLD

SHM-UH

FEATURES

- 100 MEG OHM Input Impedance
- 35 Nanosec Acquisition Time
- ▶ 500 V/µsec. Output Slew Rate
- 10 MHz Sample Rate
- ±30ma Output Current
- ▶ 2"Wx2"Lx.375"H

GENERAL DESCRIPTION

Model SHM-UH is characterized primarily by very high speed. Its tracking capability of 35 nanoseconds with an aperture uncertainty time of less than 200 picoseconds is the most unique feature of the device.

A 200 picosecond aperture time (uncertainty) enables tracking and holding of high bandwidth Video, Radar, or Television signals as well as wide band data for communication systems. The SHM-UH ingredients consist of a high impedance FET input buffer amplifier, a floating high speed electronic switch, holding capacitor, and a high power FET output amplifier.

Model SHM-UH was primarily designed to "freeze" fast moving video signals during A/D conversion or to store multiplexed outputs while the signal is being digitized and the multiplexer is seeking the next signal to be converted. In wideband datareduction, SHM-UH may be used to determine peaks or valleys, or measure fast single shot pulses of arbitrary width.

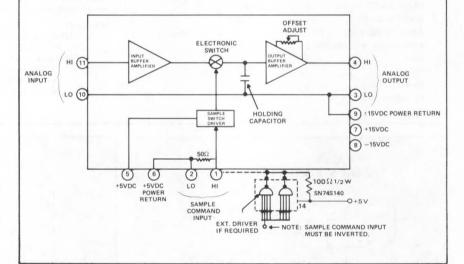
Model SHM-UH can track a full scale input $(\pm 5V)$ in 35 nanoseconds. Input impedance is 100 megohms shunted by 20 pf. An aperture time of 200 picoseconds has been obtained by utilizing a proprietary ultra high speed electronic switch.

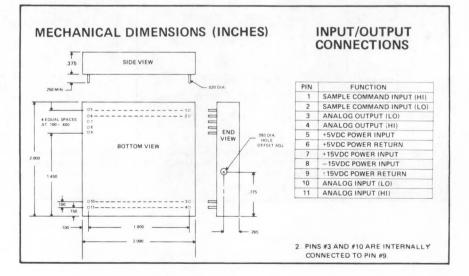
Output characteristics include a slewing rate of 500V/ μ sec, settling time (includes input acquisition time) of 50 nsec, output voltage range of \pm 5VFS @ \pm 30 ma and an output impedance of less than 10 Ohms. Other specifications include a Hold Decay Rate of 50 μ volts/ μ sec, a feedthrough attenuation of -60db @ 10 MHz (Sine Wave input) and -46db for a step input.

The Sample Command input is transformer coupled to the electronic switch and has an input impedance of 50 Ohms and requires a 35 nanosecond positive going pulse. The maximum sample rate is 10 MHz. Input power requirements are ±15VDC @ ±50 ma and +5VDC @ 100 ma.

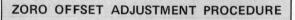


BLOCK DIAGRAM - MODEL SHM-UH

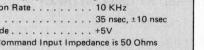


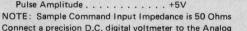


SPECIFICATIONS	DATEL	0000
Analog Input Range	Up to ±5VFS	
Input Impedance		ANALOG INPI
Sample Command	35 ± 10nsec OV to +5V, POSI- TIVE PULSE. (3nsec max. rise and fall time) NOTE: This input is transformer coupled to the electronic switch.	SAMPLE COMMAND INP
Sample Command Input		
Impedance	50 Ohms — Requires 100 ma of Source Current. NOTE: See Block Diagram for Buffer Input.	
PERFORMANCE:	Buffer Input.	
	11	
Output Voltage Range		ANALOG INPUT
Output Current		T SIGNAL
Output Impedance	and Personality Provident	
Gain	inverting	1 h
Linearity	±0.25% of F.S.	X
Input Acquisition Time/	35nsec for full scale input	
Output Settling Time to 0.2%		
(including input acquisition time) Aparture Delay		
Aperture Uncertainty		35 NSEC.
Output Slewing Rate	500V/µsec	1
Maximum Sample Rate	10 MHz	
Hold Decay Rate	50 μV/μsec	
Feedthrough	the second rear a second s	
	Input) -46db (Pulse Input)	0db
Output Zero T.C.		- 10db
Input Power Requirements		-20db
and a second	+5VDC, ±0.25VDC @ 100 ma	-30db
Operating Temperature Range	0°C to +70°C	-40db
Storage Temperature Range	-55°C to +85°C	-40db
Relative Humidity	Up to 100% NON-	-50db
	CONDENSING	-60db
Size	2"Lx2"Wx.375"H	
Case Material	Black Dyallyl Phthalate, per MIL-M-14	10HZ
Weight	3 oz.	

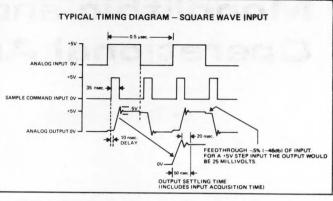


- 1) Connect the Analog Inputs together Pin 11 to Pin 10.
- 2) Connect a precision pulse generator via a coaxial cable to the "Sample Command Input" terminals. Pin 1 (High) and Pin 2 (Low).
 - Adjust its output to display the following: Pulse Repetition Rate 10 KHz Pulse Amplitude +5V
- 3) Connect a precision D.C. digital voltmeter to the Analog





- Output terminals. Pin 4 (High) and Pin 3 (Low).
- 4) Adjust the offset control until the analog output is CV.



APERTURE TIME ERROR Acquisition Time 200 PSEC

The acquisition time is the time necessary to charge the holding capacitor and start to track the input signal. To sample the input signal the Sample Command input must be a positive five volt signal with a duration of 35 ± 10 nsec.

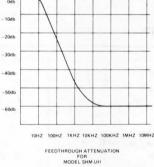
The total acquisition time for a five volt input step is 35 nanosec

Aperture Time

The aperture time is the uncertainty of the actual point in time the switch is opened. It is a measure of the repeatability of the switch characteristics. Aperture time for the SHM-UH is less than 200 psec. This time should not be confused with the fixed delays which can be compensated for. Typical delay between the hold command input and the actual switch open is approximately 10 meanser.

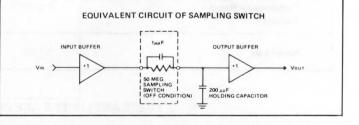
SINEWAVE INPUT

APERTURE TIME ACQUISITION TIME



Feedthrough Attenuation

After the switch has been opened and the signal is being held, a certain am ount of the signal still on the input will couple over to the output.



ORDERING INFORMATION

MODEL-SHM-UH PRICE (1-9) \$229.00 MATING SOCKET MODEL DILS-2 2 req'd/module, \$5/pr.

GOLD BOOK 76/77

Monolithic and Hybrid I.C. Operational Amplifiers

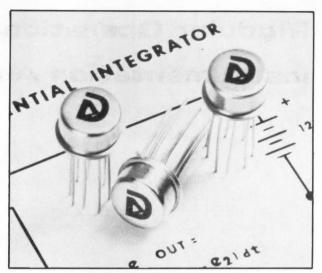
	MONOLITHIC	MONOLITHIC	MONOLITHIC	MONOLITHIC
SPECIFICATIONS (Typical at 25°C, ±15V supplies unless otherwise noted)	MOD.SLEW RATE AM-450-2	FAST SETTLING AM-452-2	LOW COST AM-460-2	WIDEBAND AM-462-1/2
DDD D D D D D D D D		1514	1501	- unol growth
DC Open Loop Gain	25K	15K	150K	150K
Gain Bandwidth Product	12 MHz	20 MHz	12 MHz	100 MHz
Slew Rate	30V/µsec.	120V/µsec.	7V/μsec.	35V/μsec.
Settling Time, 10V to 0.1%	330 nsec.	200 nsec.	1.5 μsec.	1.0 μsec.
Output, min.	±10V @ 10mA	±10V @ 10mA	±10V @ 10mA	±10V @ 10mA
Common Mode Range, min.	±10V	±10V	±11V	±11V
Common Mode Rejection	90 dB	90 dB	100 dB	100 dB
Input Impedance	50 Meg.	100 Meg.	300 Meg.	300 Meg.
Input Bias Current, max.	250nA	250nA	25nA	25nA
Input Offset Current, max.	50nA	50nA	25nA	25nA
Input Offset Voltage, max., adj. to 0	±8mV	±10mV	±5mV	±5mV
Input Offset Voltage Drift	20µV/°C	30µ∨/°C	10µV/°C	15μV/°C
Power Requirement	±15V @ 4mA	±15V @ 4mA	±15V @ 3mA	±15V @ 3mA
Temperature Range	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
Package	TO-99	TO-99	TO-99	TO-116/TO-99
Price (1-9)	\$7.50	\$10.50	\$6.50	\$9.00
Price (1-9)	\$7.50	\$10.50	\$6.50	\$9.00

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

Electronic Design's

This broad line of monolithic and hybrid operational amplifiers is designed for data acquisition and conversion applications where high speed and small size are required. The devices shown in this table are wide bandwidth, high slew rate, fast settling amplifiers. In addition to high speed, they also have excellent DC characteristics making them good choices for high accuracy applications.

Four basic models of bipolar input amplifiers are offered along with two FET input models. The AM-464-2 is a new high voltage, fast settling amplifier with \pm 35V output swing. The AM-500 is a new hybrid, ultra-fast amplifier for inverting-only applications. It features 1000V/µsec. slew rate, 100 MHz gain bandwidth product, and 200 nsec settling time to .01% for a 10V step input. The AM-490-2 series are monolithic, chopper stabilized operational amplifiers with open loop gain of 5 x 10⁸ and input offset drifts of 1.0, 0.3, and 0.1 µV/°C maximum.



AM-490 Series: Monolithic Chopper Amplifiers

		NEW	NEW		NEW	
MONOLITHIC	MONOLITHIC	MONOLITHIC	HYBRID		MONOLITHI	C
FAST SLEW FET AM-405-2	WIDEBAND FET AM-406-2	±35 V SWING AM-464-2	ULTRA FAST AM-500	СНОР	PER STABII AM-490-2	LIZED
1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1			1. Mar.	A	В	С
15Κ 20 MHz 120V/μsec. 400 nsec.	150K 100 MHz 35V/µsec. –	100Κ 4 MHz 5V/μsec. –	1×10 ⁶ 100 MHz 1000V/µsec. 100 nsec.(1)		5 x 10 ⁸ 3 MHz 2.5V/μsec.	
±10V @ 10mA ±10V 90 dB 10 ¹² ohms 20 pA 20 pA	±10V @ 10mA ±10V 90 dB 10 ¹² ohms 20 pA 20 pA	±35V @ 10mA ±35V 74 dB 200 Meg. 30nA 30nA	±10V @ 50mA 30 Meg. 4nA 0.5nA		±10V @ 7m/ ±10V 120 dB 100 Meg 150 pA 50 pA	4
±30mV 50 μV/°C	±15mV 50 μV/°C	±6mV 15 μV/°C	±3mV 5μV/°C	1.0 (2)	±20 μV 0.3 (2)	1.0 (2
±15V @ 6mA 0°C to 70°C TO-99	±15V @ 4mA 0°C to 70°C TO-99	±10V to ±40V @ 3.2mA 0°C to 70°C TO-99	±15V@22mA 0°C to 70°C 0.76 x 0.45 x 0.25''	±12V	to ± 20VDC (0°C to 70°C TO-99	
\$16:00	\$13.75	\$6.75	\$75.00	\$ 2 9.00	\$34.00	\$39.00
1.00	1	Contact Factory	Contact Factory	Se	ee page 140	2000

Notes:

(1.) Max. settling time for 10V to .01% is 200 nsec max. (2.) μ V/°C maximum.

Modular Operational Amplifiers and

Instrumentation Amplifiers

Fast Settling FET Operational Amplifiers

SPECIFICATIONS (Typical at 25°C, +15V supplies unless otherwise noted)	And the second second second	r sett AM-100	A DAMA	CAPACITIVE LOADS AM-101		FAST FOLLOWER AM-102		FAST SLEWING AM-103	
4.40	A	в	С	A	В	А	в	А	В
DC Open Loop Gain	300K		300 K		13	ок	130K		
Gain Bandwidth Product	1	3.5 MI	Hz	5.5	MHz	321	MHz		MHz
Slew Rate	4	5V/µse	ec.	45V/µsec.		140V/µsec.		400V/µsec.	
Settling Time, 10V to .01%	550 nsec. (1) 1.0 μsec. (1)		550 nsec. (2)		350 nsec. (1)				
Output, min.	±10V @ 20mA		±10V @ 20mA		±10V @ 20mA		±10V @ 20mA		
Common Mode Range, min.	±10V		±10V		±10V		±10V		
Common Mode Rejection		3,000	,	45,000 45,000			3,000		
Input Impedance	1	10 ¹² ohr	ms	10 ¹²	10 ¹² ohms 10 ¹² ohms		ohms	10 ¹²	ohms
Input Bias Current, pA max.	100	50	20	50	20		50		50
Input Offset Current, max.		10 pA		10 pA		10	pA	10) pA
Input Offset Voltage	1	Adj. to	0	Adj	. to 0	Adj.	to 0	Adj	. to 0
Input Off. Voltage Drift, μ V/ $^{\circ}$ C max.	50	25	10	40	20	40	20	40	20
Power Requirement	±15	5V @ 13	3mA	±15V @ 13mA		±15V @ 18mA		±15V @ 18mA	
Temperature Range	0°/	C to 70	0°C	0°C t	to 70°C	0°C to	o 70°C	0°C to 70°C	
Package	1.12 >	x 1.12)	x 0.4"	1.12 × 1.12 × 0.4"		1.12 x 1.12 x 0.4"		1.12 × 1.12 × 0.4"	
Socket	1100	MS-6		MS	S-6	MS	-6	MS	S-6
Price (1-9)	\$40	\$45	\$52	\$46	\$52	\$49	\$55	\$49	\$55

See page 134

Notes:

(1) Unity gain inverting

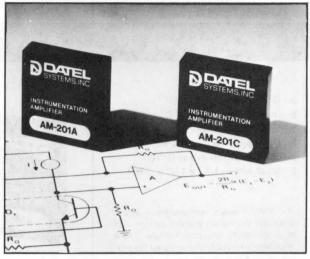
(2) Unity gain follower

DESCRIPTION

The AM-100 series of fast settling, FET input amplifiers, is designed for data conversion applications where optimum settling time is desired for up to 12 bit accuracy. While featuring exceptionally fast slew rates, wide bandwidths, and settling times faster than one microsecond, these amplifiers also have low drift and exceptionally low input bias currents. Output currents are rated at 20mA for good load driving capability.

Datel Systems' new AM-201 amplifiers are high performance instrumentation amplifiers designed for critical data acquisition applications where programmable gain at very low drifts is required. Input offset voltage drifts are 1.0, 0.5, and 0.25μ V/°C maximum for these models. In addition, these units have a bandwidth of 45 kHz at a gain of 1000.

......



AM-201 Series: High Performance, Instrumentation Amplifiers Feature Low Cost

NEW

	EW
	V FET 303
A	В
10 100V	0 ⁶ MHz //μsec. μsec.
±14 100	@ 20mA 40V ,000 ohms
30	pA pA mV
0°C to 1.8 x 2	20 50V @ 12mA o 70°C .4 x .61'' 5-11
\$90	\$120

Instrumentation Amplifiers

SPECIFICATIONS (Typical at 25°C, 15V supplies unless otherwise noted)	HIGH PERFORMANCE AM 201				
	A	В	C		
Gain Range		1 to 1000			
Gain Nonlinearity, max.	a hardware of	.01%	10 C 10 C		
Gain Equation Bandwidth, G=1000 Slew Rate	200K/R _G 45 kHz 1V/μsec.				
Output, min., S.C. protected Common Mode Range, min., ±15V Supply		±10V @ 5mA ±10V			
Common Mode Rejection, min. G=1000	100 dB	106 dB	114 dB		
Input Impedance, differential	1.0	10 ⁹ ohms			
Input Bias Current, max.	50nA	25nA	25nA		
Input Offset Current Input Offset Current Drift, nA/°C	2.5nA	1nA .02	1nA		
Input Offset Voltage	pole of a loss	Adj. to zero	and in parts		
Input Off. V. Drift, $\mu V/^{\circ}C$ max., G=1000	±1.0	±0.5	±0.25		
Output Offset Voltage Drift, G=1	the a	$\pm 100 \mu V/^{\circ} C$			
Power Requirement Quiescent Current Temperature Range Package Socket		2V to ±18VI 5mA 0°C to 70°C 5 x 1.5 x .37 MS-9			
Price (1-9)	\$69	\$79	\$89		

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

See page 130



HIGH PERFORMANCE INSTRUMENTATION AMPLIFIERS

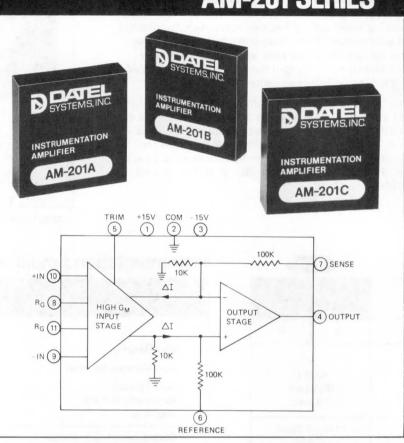
AM-201 SERIES

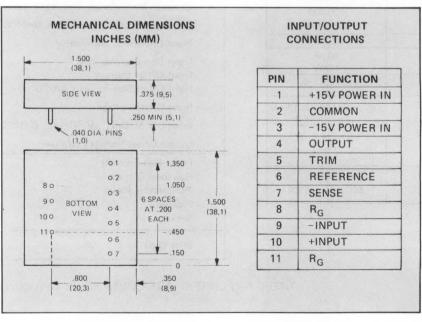
- Gain Range 1 to 1000
- ▶ Input Drift to .25 µV/°C
- CMRR to 114 dB
- ▶ Gain Nonlinearity .01% Max.
- 180kHz Bandwidth at G=100
- Small Size 1.5" x 1.5" x .375"

The AM-201 series instrumentation amplifiers offer the highest available performance in a compact, low cost module. These amplifiers are specifically designed for critical applications where the lowest input drifts and noise are required together with the highest possible common mode rejection; at the same time wide bandwidth and excellent settling time are achieved. This series rivals the performance of expensive rack-mounted instrumentation amplifiers and yet is packaged in a small $1.5 \times 1.5 \times ...375$ inch module.

The key to the performance of the AM-201 series is a unique very high transconductance (gm = 50 mhos) input stage which gives optimum results for high gains of 100 to 1000. The amplifiers are programmed by a single external resistor for gains of 1 to 1000 and give guaranteed total voltage offset drifts referred to the input of 1.0, 0.5, and 0.25µV/°C at a gain of 1000 for the three models AM-201A, AM-201B, and AM-201C respectively. At a gain of 1000 the common mode rejection ratio is 100, 106, and 114 dB minimum for the three models, with a source unbalance of 1 kilohm. The input stage gives very low bias currents and an input offset current drift of only 20pA/°C, allowing use of up to 50 kilohm balanced input source impedances. These performance characteristics are achieved without sacrificing good bandwidth: 3 dB bandwidth is 45 kHz at G=1000 and 180 kHz at G=100. Output settling time is 20 µsec. for a 10V step to .01%.

The gain equation for these models is: G=200K/R_G. Gain equation accuracy is ±0.5% with a gain nonlinearity of .01% maximum and gain temperature coefficient of 20ppm/°C maximum. Other input specifications include input voltage noise of 1 μ V peak to peak from 0.1 to 10 Hz and 1 μ V RMS from 10 Hz to 10 kHz. The input offset voltage is adjustable to zero by means of an external trimming potentiometer. These amplifiers also have sense and reference terminals for load sensing and externally offsetting the output voltage. Output capability is ±10V at 5mA, with output short circuit protection.





SPECIFICATIONS, AM-201 SERIES Typical at 25°C and ±15V supplies unless otherwise noted.

Δ В С INPUT CHARACTERISTICS Differential Input Voltage Range ±10V min. Common Mode Input Voltage Range ±10V min. Input Overvoltage, no damage ±V supply Input Impedance, Diff. or Com. Mode 10⁹ ohms Input Bias Current, nA max. 50 25 25 Input Offset Current, nA 25 1 1 Input Impedance, Ref. & Sense Inputs . . . 110K Input Offset Voltage Adi to zero OUTPUT CHARACTERISTICS +10V min. ±5mA min. Output Current, S.C. protected Output Impedance 0 1 ohm .01µF max. Capacitive Load ±10V min. Output Offset Range PERFORMANCE 1 to 1000 Gain Range 200K/RG Gain Equation Gain Equation Accuracy +0.5% .01% max. Gain Nonlinearity Gain Temperature Coefficient ±20ppm/°C max. CMR, ±10V, 1K unbal., DC-120 Hz 100 106 114 G=1000, dB min. G=100 dB min. 80 86 94 66 G=10 dB min. 60 74 G=1 dB min. 40 46 54 DRIFT AND NOISE Input Offset Voltage Drift¹, $\mu V/^{\circ}C$ max. at G=1000 ±0.5 ±1.0 ±0.25 Output Offset Voltage Drift, G=1 ±100µV/°C Input Bias Current Drift 100pA/°C 20pA/°C Input Offset Current Drift Power Supply Rej., μ V/V at G=1000 10 5 Input Voltage Noise, 0.1 to 10 Hz 1µV P-P Input Voltage Noise, 10 Hz to 10 kHz ... 1µV RMS Input Current Noise, 10 Hz to 10 kHz . . . 20pA RMS DYNAMIC RESPONSE Small Sig. Bandwidth, -3 dB, G=1000 . . . 45 kHz G=100 180 kHz G=10 300 kHz Slew Rate 1 V/usec. Full Power Response, 20V P-P 15 kHz Settling Time, 10V to .01% at G=1000 . . . 20 usec Overload Recovery 10 µsec. POWER REQUIREMENT ±15VDC ±0.5V Voltage, rated performance Voltage Range, operating² ±12V to ±18VDC Current, quiescent 5 mA PHYSICAL-ENVIRONMENTAL Operating Temperature Range 0°C to 70°C Storage Temperature Range -55°C to +85°C Relative Humidity Up to 100% non-condensing Case Size 1.5 x 1.5 x .375 inches (38.1 x 38.1 x 9.5 mm) Case Material Black Diallyl Phthalate per MIL-M-14 Pins040 round, gold plated, .250" long min. Weight 2.5 oz. max. (71 q.) \$89.00 **PRICE** (1-9) \$79.00 \$69.00 1. With input offset voltage initially zeroed. 2. Signal input and output range is ±7V to ±13V.

TECHNICAL NOTES

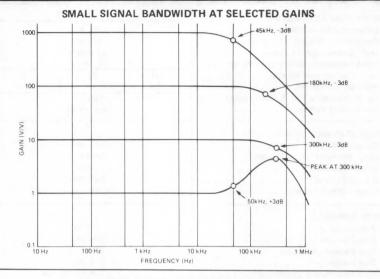
- 1. The guaranteed input offset voltage drift specification requires that the input offset voltage be zeroed. This is done by means of an external 50K trimming potentiometer connected from the TRIM pin to +15V. For minimum effect upon input offset drift, a low tempco trimming pot is recommended such as Vishay type 1203 (20ppm/°C). If the operating temperature range is relatively constant, then a 100ppm/°C cermet type trimming pot may be used (Datel Systems TP50K at \$3.00 each). A 100ppm/°C drift in the trimming pot causes a $0.3\mu V/°C$ input offset voltage drift in the amplifier.
- 2. For optimum gain stability a low tempco gain setting resistor is recommended. The temperature coefficient of this resistor adds directly to the 20ppm/°C maximum gain tempco of the amplifier. For negligible effect on tempco Vishay type S102 (±1ppm/°C) is recommended. For less critical applications a 5 or 10ppm/°C metal film resistor is recommended. The resistor should be located as close as possible to the ${\sf R}_{G}$ terminals of the amplifier, and shunt capacitance across the resistor should be kept to a minimum in order to prevent noise pick-up or instability at low gains. For gain-switched applications it is recommended that reed relays located close to the amplifier be used rather than running leads from a panel switch to the RG terminals.
- 3. The differential input terminals require a bias current path to ground and therefore cannot be used with floating inputs. Due to the very low input offset current drift of $20pA/^{6}C$, balanced source resistances up to 50K ohms can be used with these amplifiers. For example, 50K ohms x $20pA/^{6}C$ gives an equivalent input offset voltage drift of $1\mu V/^{6}C$.
- 4. The guaranteed input offset voltage drifts of 1.0, 0.5, or 0.25 μ V/^oC include both input and output drifts referred to the input at a gain of 1000. Drifts at other gains are approximately (referred to input): Δ Eos (μ V/^oC) = (Δ Eos)₁₀₀₀ + $\frac{100}{G}$

TECHNICAL NOTES (Cont'd)

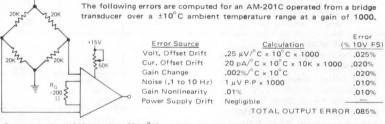
PERFORMANCE DATA

where $[\triangle \text{ Eos}]_{1000}$ is the drift spec. at G=1000 and G is the programmed gain.

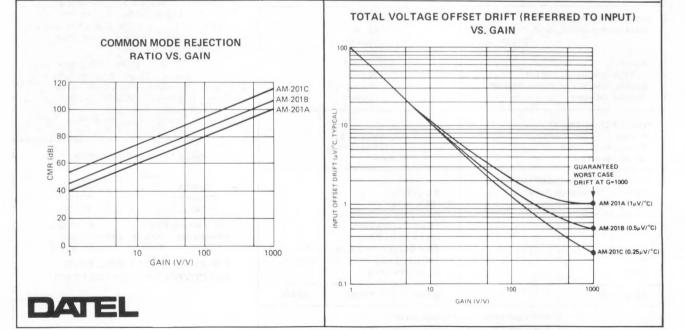
- 5. The sense terminal is normally connected to the output terminals, and the reference terminal is normally connected to ground. For remote loads or for load current sensing, the sense terminal is run separately to the load or to the current sensing resistor. The reference terminal may be connected to a voltage source in the range ±10V in order to directly offset the output of the amplifier by the same amount. Both sense and reference terminals should be connected only to low impedance sources (less than 10 ohms), as any impedance seen by these terminals will degrade the power supply rejection of the amplifier in proportion to the source impedance. A unity gain buffer amplifier can be used to isolate the reference terminal from high impedance sources. See application diagram.
- 6. The AM-201 series amplifiers have a distinct advantage over many other instrumentation amplifiers in gain-switched applications. Because the gain formula is 200K/R_G the switched gain varies precisely inversely with R_G. If R_G is halved, for example, the gain is exactly doubled. Therefore, unlike instrumentation amplifiers with a constant term of 1 in the gain formula, the selection of gain setting resistors is greatly simplified. In switched gain applications the AM-201 amplifiers should be zeroed at the highest gain. The input offset voltage then will not change with gain.



ANALYSIS OF SIGNIFICANT ERROR SOURCES USING BRIDGE TRANSDUCER

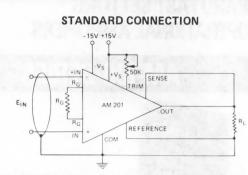


Power supply drift (assuming $.02\%/^{\circ}$ C) contributes a negligible amount to the error and therefore the computation is omitted. The total output errors for a 10° C temperature change are less than 0.1%.

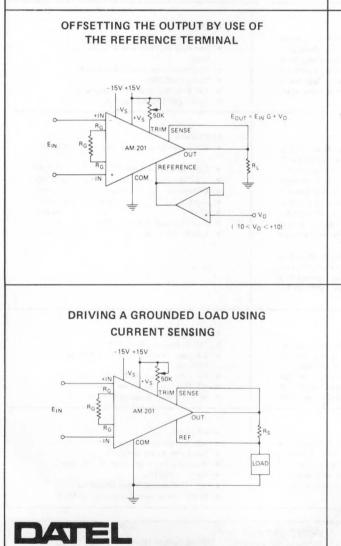


Electronic Design's

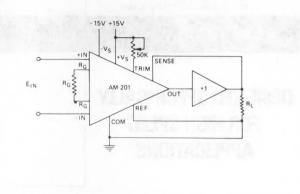
APPLICATION DIAGRAMS



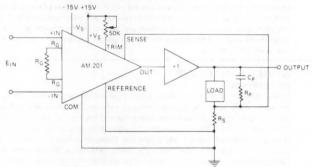
INPUT OFFSET TRIMMING: Short input terminals together and connect to ground or to common mode voltage at which input will be used. Adjust 50K trimming pot for zero output voltage. For critical applications R_G should be a Vishay type S102 and the trimming pot should be a Vishay type 1203. See technical notes.



USING AN OUTPUT CURRENT BOOSTER

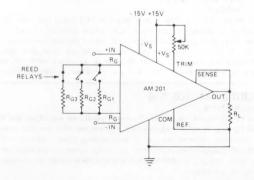


CONNECTION FOR DRIVING LOAD WITH CURRENT BOOSTER USING LOAD CURRENT SENSING



NOTE: The output voltage using the gain equation will appear across R_S . The load impedance and output of the current booster must be compatible with this. Highly inductive loads may cause ringing or oscillation. In this case add R_P and C_P as shown.

GAIN SWITCHING WITH THE AM-201



Gain is inversely proportional to ${\sf R}_G$. Thus if ${\sf R}_G$ is halved the gain is exactly doubled. Input offset voltage does not change with ${\sf R}_G$.



WIDE BAND FAST SETTLING FET INPUT OPERATIONAL AMPLIFIERS

AM-100-SERIES

DESIGNED SPECIFICALLY FOR HIGH SPEED APPLICATIONS



MODEL AM-100 A/B/C

Designed specifically to drive C.R.T. displays, the DATEL Models AM-100 A/B/C permit settling (to 0.01%) of a 0.5 V step within 0.15 μ sec. Clean, crisp alpha/numeric characters, together with sharp, linear vectors are the result on the screen face when these amplifiers with their fast settling, true 6dB/octave response and minimum overshoot and undershoot characteristics are used. These devices are also excellent choices for use in high speed applications such as D/A output drivers, integrators, comparators, buffers and many other analog sampling circuits.

MODEL AM-101 A/B DESCRIPTION:

Models AM-101 A/B are FET-input differential operational amplifiers designed specifically for applications requiring a combination of high accuracy, high gain and fast settling with the ability to drive substantial capacitive loads. They have a gain bandwidth product of 5 MHz and will settle to 0.01% within 1.5 μ sec., min. in a unity gain inverting mode while driving a capacitive load of 300 picofarads. These amplifiers will settle to 0.01% within 1 μ sec., min., in the same mode driving a 1000 picofarad load and are stable driving a load of 2000 picofarads, minimum. Typically they are stable up to 5,000 picofarads. In addition, low drift, low noise and excellent overload recovery characteristics together with a reasonable price make these amplifiers a must to consider wherever analog voltage sampling is required.

Model AM-101 A/B has a CMRR of 40,000 typical and 20,000 minimum and should be considered wherever a non-inverting amplifier is necessary such as in buffer or multiplexer applications. Since settling time to 0.01% is approximately the same in the non-inverting mode, excellent gain and linearity characteristics are achieved with the high CMRR of the AM-101 Series.

MODEL AM-102 A/B DESCRIPTION:

The Model AM-102 A/B is a differential FET input fast settling operational amplifier designed primarily for use in circuits where polarity reversal is not desired. All the ingredients of a good, fast and accurate FET Follower can be found in the AM-102 A/B. High CMRR, very high common mode resistance, high gain, wide bandwidth and fast settling along with high input impedance, excellent drift and noise characteristics all combine to make the AM-102 A/B one of the best all around Follower Amplifiers available.

MODEL AM-103 A/B

DESCRIPTION:

The fastest yet of the DATEL Systems operational amplifiers, the AM-103 A/B features a 250 Volt per microsecond slew rate, a guaranteed 400 nanosecond settling time (to 0.01%), an overload recovery time of 1 microsecond, max. together with a minimum gain of 100,000. Designed especially for use in high speed comparators, integrator, A/D and D/A converter circuits, the AM-103 A/B is an excellent choice for consideration whenever analog sampling is necessary.

FEATURES:

- ▶ 60 Volts/µsec. Slew Rate
- Settles to 0.01% Within 0.15 µsec. (Small Step)
- Recovery From Overload in 0.5 μsec.
- ► Gain of 500,000
- 10¹² Ω Differential Input Resistance
- True 6 dB/Octave Response

FEATURES:

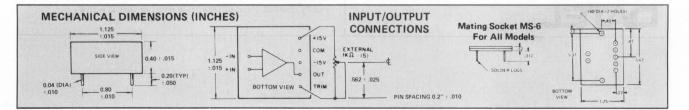
•	Will drive high capacitive load 2000 pF, min.
	Gain Bandwidth Product 7 MHz
٠	D.C. Gain at Rated Load 500,000
٠	Differential Input Resistance $10^{12} \Omega$ min.
	Output ± 10 V @ ± 20 mA, min.
►	CMRR
٠	Fast Overload Recovery Time 1 µsec.
٠	Low Profile Case 0.4"

FEATURES:

- ▶ 140 Volts/µsec. Slew Rate
- 0.4 μsec, Settling Time to 0.01% as Follower
- ▶ 0.5 µsec. Overload Recovery Time
- 400,000 Gain at Rated Load
- ▶ 45 MHz Gain Bandwidth Product

FEATURES:

- ▶ 400 Volts/µsec. Slew Rate
- ▶ Settles to 0.01% Within 0.3 µsec.
- Recovery From Overload in 0.5 µsec.
- ▶ Gain of 400,000
- ▶ 10¹² Differential Input Resistance
- Stable Unity Gain Frequency 37 MHz



THESE AMPLIFIERS ARE COVERED UNDER GSA CONTRACT

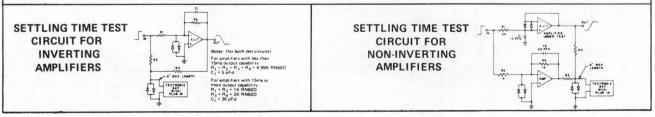
DATEL	MODEL AM-100			MODEL AM-101				MODEL AM-102		MODEL AM-103		
	A	в	С	A	В	1	A	В		A	в	
SPECIFICATIONS Typical @ 25°C, ±15 VDC, rated load unless otherwise specified.	HIGH SPEED DIFFERENTIAL FET 400 NANOSEC. SETTLING TIME			HIGH SPEED DIFFERENTIAL FET WILL DRIVE 2000pF CAP. LOAD		HIGH SPEED FET FOLLOWER 45 MH2 GAIN BANDWIDTH		ER	SUPER FAST DIFFERENTIAL FE 400 V/#SEC SLEW RATE			
PARAMETER Input Differential Voltage, max., no damage	±15V ±10V m			±15V ±10V			±15V ±10V			±15V ±10V		
Common Mode Voltage Range		in.										
Common Mode Rejection Ratio	10,000			40,00			40,00			10,00	0	
Common Mode Resistance	10 ⁴ 2 Ω	min.		1012	Ω min.		1012	Ω min.		1012	Ω min.	
Differential Input Resistance	10 ¹² Ω	min.		1012	Ω min.		1012	Ω min.		1012	Ωmin.	1.1
Output Voltage	±10Vm	in		±10V	min		±10V	min.		±10V	min	
Current, Continuous	±20mA				A min.			A min.			A min.	
Current, Transient	±30mA			±30m			±30m			±30m		
Capacitive Load	300 pF				oF min.		300 p			300 p		
Gain and Frequency Response				1			1					
D.C. Gain at Rated Load	500.000			500.0	00		400.0	000		400.0	00	
Gain Bandwidth Product	18 MHz			7 MH			400,0 45 M			400,0 45 MI		
Stable Unity Gain Frequency	18 MHz			7 MH			37 M			37 MI		
Full Power Response	900 KH				(Hz (1)			z (2)		6 MH		
Transient Response Slew Rate	60V/µs.				us. (1)			/µs. (2)			/µs. (1)	
Settling Time to 0.01%	0.4 µs. (1 µs.			0.4 #			0.3 #		
Settling Time to 0.01%	0.15 Hs.			1.5 4								
Overload Recovery Time	0.5 µs.	(0)		1 µs.			0.5 µ	s.		0.5 µs		
Rise Time to 90% (Small Signal)	50 ns. (1)		100 n	s. (1)		20 ns			20 ns.		
Offset and Noise Offset Voltage (Initial) @ 25 [°] C	(5) Adj. to	0	0.09-44	Adj. t		1.1.1	Adj.			(t Adj. t	0 0	đ
Vs. Temp. Range -25°C to +85°C, µV/°C	50 max	25 ma:	x 10 max	40 max	<. 20 ma:	×	40 max	. 20 max.			x. 20 ma>	۲.
Vs. Power Supply	±10µV/9	%		±10µ\	11%		±10µ	V/%		±104		
Vs. Time	±50µV/0	day		±50µ	V/day		±50µ	V/day		±504		
Input Offset Current	±10pAr	nax.		±10p/	A max.		±10p	A max.		±10p/	A max.	
Bias Current @ 25°C, pA	100 max.	50 ma	x. 20 max	50 ma	x. 20 ma	x		50 max.			50 max.	
Vs. Temperature Range												
-25°C to +85°C Input Noise (Voltage)	25nV V		10°C		VHz	10°C		VHz	10°C		VHz	10°0
Power Requirements					V			V			V	
Operating Voltage Range	±15V			±15V			±15V	,		±15V		
Quiescent Current	±13mA	max.		±15V ±13mA max.			±18mA max.			±18mA max.		
Temperature Range	1				-		1			1000		
	-25 to +	95°C		25 **	+95%		25 **	+85%		.25 +0	+85%	
Operating Storage	-25 to +				-25 to +85°C -55 to +125°C		-25 to +85°C -55 to +125°C			-25 to +85°C		
CASE SIZE	1.12"L 0.4"H	x 1.12'	′W ×		L x 1.12		1.12"L x 1.12"W x 0.4"H		w x	1.12"	L × 1.12'	'W ×
Mating Socket	MS-6 \$	_		-	\$3.50 e	9		\$3.50 ea.		0.4"H MS-6 \$3.50 ea.		
Price 1 - 9		\$45	\$52	\$46	\$52	a. T	\$49	\$55		\$49	\$55	· ·
the second s	s Follower.					t step (ain inverti	ing with 1			loa

SETTLING TIME

Settling time is one of the most important requirements an amplifier should meet for high speed applications. It is defined as the time that is required, after a full scale input step is applied, for the output voltage to reach a predetermined percentage of its final value. Settling time contributes a dynamic error. It characterizes the transient behavior of the amplifier, encompassing slew rate and other important effects. For high speed data system applications, the output signal should be within a specified error band before it is ready to be further processed. In all applications involving abrupt changes in gradient, the settling characteristics of an amplifier determine how long the output signal deviates from the true value and should be a prime consideration for its selection.

Settling time is a complex function of the open loop response and slewing rate under operating conditions. For optimum settling characteristics, the DATEL amplifiers have true 6 dB/octave stabilization determined by a single component instead of the usual multielement response shaping which introduces irregularities in the response curve.

Test circuits for measuring a settling time in both the inverting and non-inverting modes are shown. The test circuits are self explanatory but it is wise to keep the leads short, stray capacitance to a minimum and use a signal source that is a good clean squarewave with minimum aberrations. The oscilloscope and plug-in recommended in the test circuit will, in general, give good results on amplifiers with settling times of 1 microsecond or less. Many oscilloscopes of other types will introduce errors far in excess of the amplifier errors due to the overload condition to which they are subjected by this method of measurement.





HIGH SPEED MONOLITHIC OPERATIONAL AMPLIFIERS

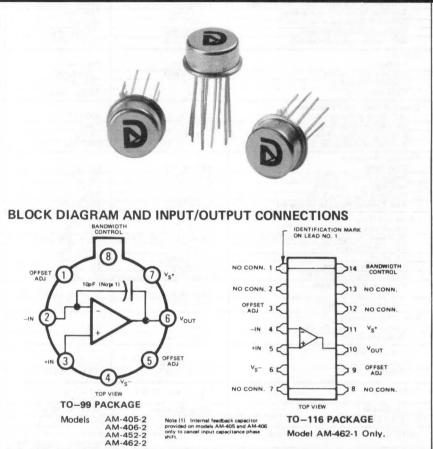
AM-400 SERIES

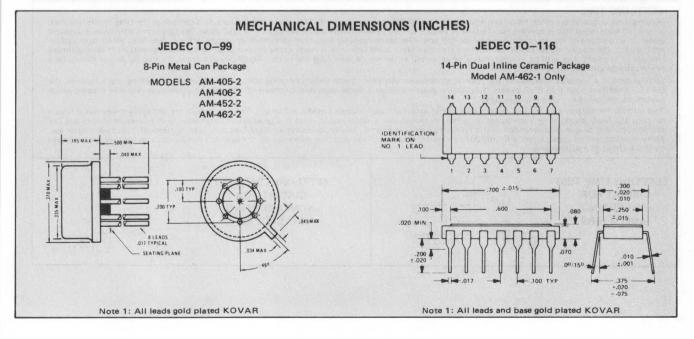
FEATURES

- ▶ 120 V/µSec Slew Rate
- 2 MHz Full Power Bandwidth
- 200n Sec Settling to 0.1% of FS
- ▶ 10¹² Ω Input Impedance
- ▶ FET or Bipolar Differential Input

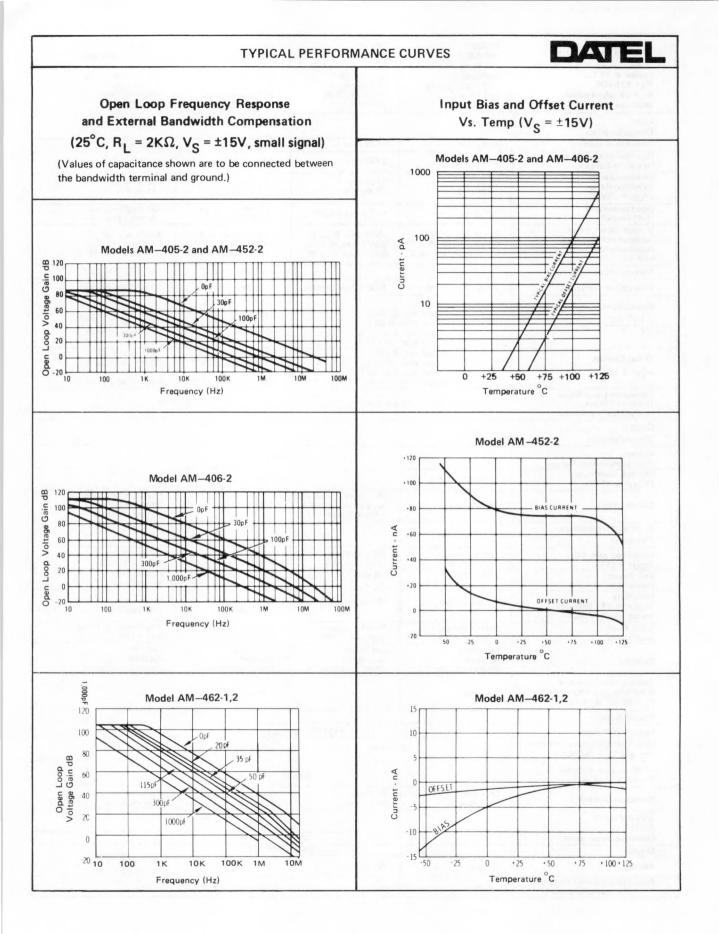
GENERAL DESCRIPTION

Datel's AM-400 Series operational amplifiers are designed specifically for fast acquisition of wide bandwidth signals. They feature high input imped-(10^{1 2} Ohms, AM-405 and ance AM-406) and high full power bandwidth (2MHz, AM-405), Models AM-405 and AM-406 feature FET differential inputs and the remaining models employ bipolar differential inputs. Settling time less than 200 nsec (within 0.1% of FS, AM-452) and slew rates up to 120V/µsec (AM-452) are available and all models may be operated in non-inverting as well as inverting configurations. Because of their superior high speed, high input impedance characteristics, these devices are ideal for applications such as fast acquisition sample and hold amplifiers, D/A and A/D converter amplifiers.

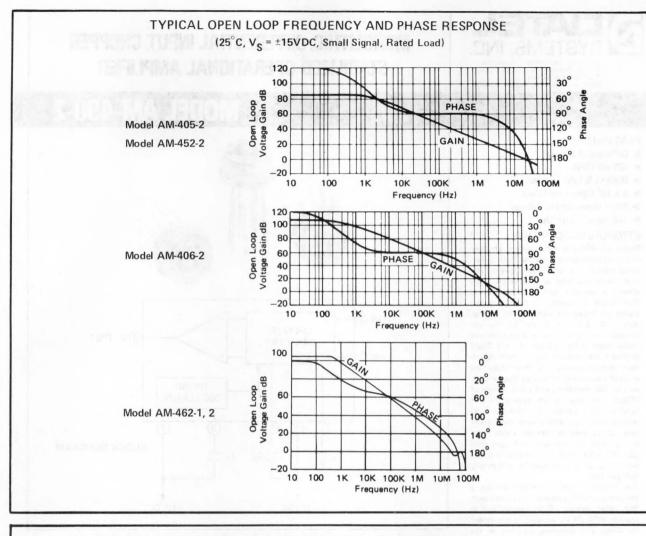


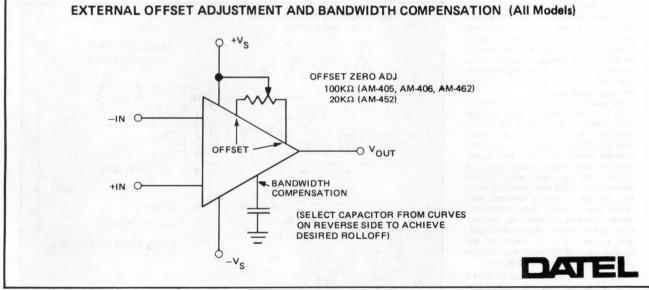


SPECIFICATIONS	MODEL AM-405-2	MODEL AM-406-2	MODEL AM-452-2	MODEL AM-462-1, AM-462-2	
Typical @ 25°C VS = ±15VDC RL = 2K Ohms unless otherwise noted	15VDC FET input, 2MHz K Ohms unless Full Power		Differential Bipolar input 200 nsec settling Slew 120 V/µsec	Differential olar Bipolar input 150 K DC Gain 100 MHz f _t	
Input Characteristics		tion	subsidth Gompanta	and Esthering Sa	
Differential Voltage	±15V max.	±12V max.	±15V max.	±12V max.	
Common Mode Voltage Operating Range	±10V min.	±10V min.	±10V min.	±11V min.	
Common Mode Rejection Ratio (V _{CM} = ±5VDC)	90 db typ. 70 db min.	90 db typ. 70 db min.	90 db typ. 74 db min.	100 db typ. 74 db min.	
Input Impedance (Differential)	10 ¹² Ohms 5pF	10 ¹² Ohms 5pF	100 MegOhms typ. 40 MegOhms min.	300 MegOhms typ. 40 MegOhms min.	
Voltage Offset Initial (without external trim. Adjustable to zero with trim)	30mV typ. @ 25° C 60mV max. @ 25° C 65mV max, 0 to 75° C	15mV typ. @ 25°C 60mV max. @ 25°C 65mV max, 0 to 75°C	5mV typ. @ 25°C 10mV max. @ 25°C 14mV max, 0 to 75°C	3mV typ. @ 25°C 5mV max. @ 25°C 7mV max, 0 to 75°C	
Voltage Offset vs. Temp	-	-	$30\mu V/^{\circ}C$, 0 to $75^{\circ}C$	15µV/°C, 0 to 75°C	
Zero Adjust (optional)	100K Ohms trimpot	100K Ohms trimpot	20K Ohms trimpot	100K Ohms trimpot	
Bias Current = <u>1⁺ + 1⁻</u> 2		. @ 25° C 0 to 75° C , 0 to 75° C	125nA typ. @ 25°C 250nA max. @ 25°C 500nA max, 0 to 75°C —	5nA typ. @ 25°C 25nA max. @ 25°C 40nA max, 0 to 75°C	
Offset Current = + - -		. @ 25°C 0 to 75°C	20nA typ. @ 25°C 50nA max. @ 25°C	5nA typ. @ 25°C 25nA max. @ 25°C	
Equivalent Input Noise (10Hz to 10KHz, zero source impedance)	500pA max 10	, 0 to 75°C μV rms	100nA max, 0 to 75°C 40nA max, 0 to 75°C 2 μ V rms		
Output Characteristics Voltage (Full Temperature Range)	labçid.	±10	V min.		
Current, Continuous (VOUT = ±10V)	- finder	±10n	nA min.		
Current, Peak	50mA max.	Short circuit protected (output to common) current limited	50mA max.	Short circuit protected (output to common) current limited	
Gain and Frequency Response			al and the		
Open loop gain, DC VOUT = ±10V	15K V/V typ. 7.5K V/V min.	150K V/V typ. 80K V/V min.	15K V/V typ. 7.5K V/V min.	150K V/V typ. 80K V/V min.	
Full Power Bandwidth	2MHz typ.	600KHz typ.	1.6MHz typ. 1.2MHz min.	600KHz typ. 320KHz min.	
Slew Rate (VOUT = ±10 Volt step transition, CL = 50pF)	120V/µsec typ.	35V/µsec typ. ─	120V/μsec typ. 80V/μsec min.	35V/μsec typ. 20V/μsec min.	
Unity Gain, small signal	20MHz (closed loop gain > 10	100MHz (closed loop gain > 10)	20MHz (closed loop gain > 10)	100MHz (closed loop gain ≠ 100, CL ≠ 50pF)	
Stability	Ext. comp. required at closed loop gain <3	Ext. comp. required at closed loop gain <5	Ext. comp. required at closed loop gain < 3	Ext. comp. required at closed loop gain <5	
Settling time to within 0.1% ($V_{OUT} = \pm 10V$ step, $C_L = 50 \text{ pF}, A_v = +3$)	400 nsec	-	200 nsec	and the second second	
Power Supply					
Operating Voltage		±15VDC, rate	d specifications	St. St. Alan	
Max. Voltage Difference between V_S^+ and V_S^- Terminals	35	5V max	40V max	45V max	
Absolute Max. Internal Power Dissipation		300ml		14 1 - A 18	
Quiescent Current	6mA typ. 8mA max.	4mA typ. 6mA max.	4mA typ. 6mA max.	3mA typ. 4mA max.	
Temperature Range					
Operating, rated specs. Storage			o 75°C o +150°C		
	ТО-99	то-99	ТО-99	AM-462-1 TO-116 AM-462-2 TO-99	
Package Price (1-9) Contact factory	10-99	10.00		Alvi-402-2 10-99	



Electronic Design's







MONOLITHIC, DIFFERENTIAL INPUT, CHOPPER STABILIZED OPERATIONAL AMPLIFIER

MODEL AM-490-2

FEATURES

- Differential Inputs
- ▶ 120 dB CMR
- **b** Drift to $0.1\mu V/^{\circ}C$ max.
- ▶ 5 x 10⁸ Open Loop Gain
- ▶ 20µV Input Offset Voltage
- ▶ 200 msec. Warm-Up

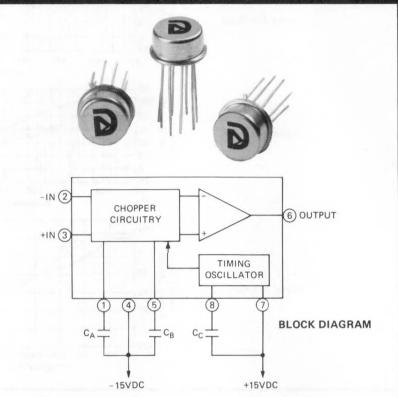
GENERAL DESCRIPTION

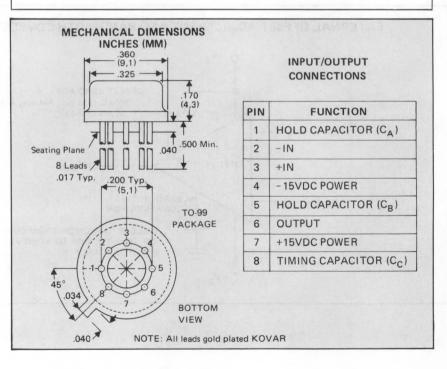
Model AM-490-2 is a monolithic, chopper stabilized operational amplifier with differential inputs; it is specifically designed for applications requiring ultra-stable DC characteristics together with good bandwidth. This device is available in three different grades of maximum input offset voltage drift: 1.0, 0.3, and 0.1µV/°C. The extremely low input offset voltage drift and initial input offset voltage of only 20µV eliminate the requirement for zero adjustment in most applications. Other important input characteristics include an input impedance of 100 megohms, input bias current of 150pA, and input offset current drift of 1pA/°C. This permits the AM-490-2 to operate accurately with source impedances over 100 kilohms. A common mode rejection of 120 dB minimum and open loop gain of 5 x 108 result in extremely low output errors. Long term stability is typically 5µV per year.

The circuit of the AM-490-2 utilizes a complex monolithic chip 93 x 123 mils with 256 active devices. Both bipolar and N channel MOS FET's are used to implement the linear and switching portions of the circuitry. The chopper circuitry utilizes two DC coupled sample-hold circuits driven by a multivibrator circuit. The DC coupling, contrasted with AC coupling commonly used in chopper amplifiers, results in fast overload recovery. Three external capacitors are required for the sample-hold circuits and the multivibrator which generates a 750 Hz chopping square wave.

Other specifications of the AM-490-2 include ±10V input common mode range and ±10V output at 7mA which is short circuit protected. The operating power supply range is ±12V to ±20VDC with a constant quiescent current drain of 3.5mA typical over this range. Power supply rejection is 120 dB. The low power drain and fast warm-up time of 200 msec. make this device ideal for use in battery operated, interrupted service circuits. Other applications include inverting, noninverting, and balanced gain amplifier configurations in addition to very accurate integrators and sample-holds. The AM-490-2 is packaged in a hermetically sealed, 8 pin TO-99 case.

CAUTION: The AM-490-2 has MOS FET input devices and should be handled carefully to prevent static charge pick-up which might damage the devices. The amplifiers should be kept in the shipping carriers until ready for installation.





SPECIFICATIONS, AM-490-2

(Typical at 25°C, ±15V supplies and $C_A = C_B = 0.1 \mu F$, $C_C = .0015 \mu F$ unless etherwise noted).

TECHNICAL NOTES

INPUT CHARACTERISTICS	A	В	С		
Common Mode Voltage Range	±10	V min.			
Maximum Diff. Input Voltage, no damage	±Vs				
Input Impedance, diff. or com. mode	100	megohms			
Input Capacitance	10pl	-			
Input Bias Current	150	A			
Input Offset Current	50p/	4			
Input Offset Voltage	±20µ∨				
OUTPUT CHARACTERISTICS					
Output Voltage	±10	V min.			
Output Current, S.C. protected		A min.			
Output Resistance		ohms			
Stable Capacitive Load	1000	JbF			
PERFORMANCE	a second second second		- 1.4		
DC Open Loop Gain, 2K load	5 x 1	10 ⁸			
Common Mode Rejection, DC, ±5V		dB min.			
Warm-Up Time		msec.			
DRIFT AND NOISE					
Input Offset Voltage Drift, $\mu V/^{\circ}C$ max	1.0	0.3	0.1		
Input Offset Current Drift	±1p/	A/°C			
Input Voltage Noise, .01 to 10 Hz	13µV	V P-P			
Input Voltage Noise, 10 Hz to 10 kHz		V RMS			
Input Current Noise, .01 to 10 Hz		RMS			
Input Current Noise, 10 Hz to 10 kHz	1	ARMS			
Chopper Voltage Noise, RTI, 100K unbal		ιV P-P dB min.			
Power Supply Rejection		dB min. //year			
	± 5μ	v / year			
DYNAMIC CHARACTERISTICS					
Gain Bandwidth Product	3 MH	Ηz			
Rise Time, small signal, 10%-90% ¹		nsec.			
Slew Rate	2.5V	/µsec.			
Full Power Frequency	40 k	Hz			
Overload Recovery Time	200	msec.			
POWER REQUIREMENT	15				
Voltage, rated performance		VDC, ±0.5V			
Voltage, operating		V to ±20VDC ² nA typ., 5mA m	22		
Current, quiescent	3.50	iA typ., SinA ii	idx.		
PHYSICAL-ENVIRONMENTAL					
Operating Temperature Range	0° C	to 70°C			
Storage Temperature Range	-65°	°C to +150°C			
Package, hermetically sealed	TO-9	99			
PRICE (1-9)	\$29	\$34	\$39		
	929	034	933		
 Connected as voltage follower. Input common mode range and output range are 	+7V to +15V				
e and output range and output range are	_/ V to 110V.				
ORDERING INFO	RMATION				
PRICES (1	-9)				
AM-490-2A 1.0μV/°C	2 max \$20	0.00			
AM-490-2B 0.3μV/°C		1.00			
AM-490-2C 0.1µV/°C		0.00			
AM-490-CK1 CAPACITO		.50			
Consists of 3 miniature metallized polycarbo		A 5	°C.		
	.203"D x .438				
	.156''D × .438'				
THESE AMPLIFIERS ARE CON	VERED BY GS.	A CONTRACT.			

1. Three external capacitors are required for operation of the AM-490-2. One of these, C_c (.0015 μ F) is used to set the timing oscillator to give a chopper frequency of 750 Hz; the other two, $\rm C_A$ and $\rm C_B$ (both 0.1µF), are used as holding capacitors for the direct coupled internal sample-holds. All three of these capacitors should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene. teflon or polycarbonate types are recommended. As a convenience, the capacitors are available as a kit of three miniature metallized polycarbonate types; the AM-490-CK1 capacitor kit is priced at \$4 50

- 2. In most requirements the AM-490-2 eliminates the need for a zeroing adjustment. Typical input offset voltage is only ±20µV while the maximum is only ±80µV over the operating temperature range. In cases where zeroing is still necessary, however, there are two methods shown in the application diagrams. In the inverting mode where the negative summing junction is at virtual ground, the zeroing can be accomplished by injecting an offset current into the summing junction by means of a high value resistor connected to a potentiometer. (See "Precision Integrator" diagram). In all other cases, zeroing is accomplished by means of a voltage divider connection to the positive input terminal. (See "Differential Amplifier Connection").
- 3. The superior input offset voltage drift (1.0, 0.3 or 0.1µ//°C max.) and input offset current drift (1pA/°C) of this amplifier permit it, when properly applied, to resolve microvolt and picoampere level signals. To successfully amplify these very low level signals, it is necessary to use great care in circuit layout and assembly with particular attention given to proper grounding and shielding. Other potential error sources include leakage, thermal environment, and thermocouple effects.
- 4. The highest practical input impedance which can be used with the AM-490-2 is determined by the point where input offset current drift and input offset voltage drift produce equal errors. Thus:

 $R_{MAX} = \frac{\Delta Eos/\Delta T}{\Delta Ios/\Delta T}$

Where R_{MAX} is the maximum practicable input resistance seen by either input terminal of the amplifier. This comes out to 1 megohm for the A version, 300 kilohms for the B version, and 100 kilohms for the C version.

5. The amplifier input terminals are differential and symmetrical; for best results the

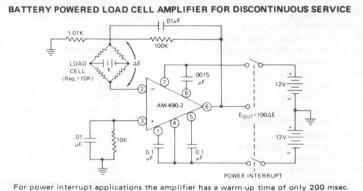


TECHNICAL NOTES (Cont'd.)

OPERATION AND APPLICATIONS

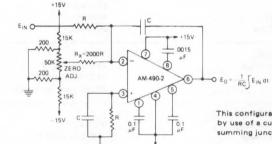
impedance to ground seen by each input terminal should be equal. Matched impedance (resistance and capacitance) as shown in the application diagrams result in minimum output offset drift due to bias currents and also minimum output chopper noise. Chopper noise appears as a common mode input current signal, and under balanced conditions of both resistance and capacitance this noise can be minimized to less than random noise at the output.

- 6. The AM-490-2 is dynamically stable with 100% feedback (unity gain follower) and 1000pF capacitive load. In very high closed loop gain configurations (>70 dB), it may become desirable to put a capacitor in parallel with the feedback resistor for better stability. This should be done to yield a gain-bandwidth product of 2MHz (RC=80 µsec.) to insure absolute stability. In general, the closed loop bandwidth should be limited to that necessary to pass the required signal frequency components only: this results in minimum output noise. Minimum bandwidth should also be used to eliminate small modulation effects of input signal frequencies near the chopper frequency (750 Hz).
- 7. Other features of these amplifiers include an exceptionally high open loop gain of 5 x 10⁸. For an output voltage swing of ±10V, this reduces the input error due to gain to only ± 20 nanovolts. Common mode rejection is very high (120 dB minimum) at DC, but falls off rapidly with frequency as shown in the graph under Performance Parameters. CMR is typically greater than 100 dB at 10 Hz. For best common mode rejection, therefore, the signal frequency should be limited to about 10 Hz. The noise performance of the amplifier can be readily computed from the two noise graphs shown under Performance Parameters.
- 8. The AM-490-2 amplifiers draw a quiescent current of only 3.5mA typical and 5mA maximum: the current is virtually constant over the operating power supply range of ±12V to ±20V. Bandwidth and slew rate change only slightly over this range as shown in the graph "Normalized AC Parameters vs. Power Supply". For the ±12V to ±20V supply range input common mode voltage range and output voltage range become ±7V to ±15V. The wide supply range together with the fast warm-up time of only 200 msec. make the AM-490-2 an excellent amplifier for precision, low power, interrupted supply operation in portable and remote instrumentation systems.



INPUT OFFSET CURRENT AND CHOPPER NOISE CONSIDERATIONS 4+15V 1B2 0 1B1 C 0015 E20-00 (8) AM-490-2 $\frac{R_2}{R_1}(E_1 - E_2)$ 6 O EOUT = (5) + (101-102) Ra E. OMAN (4 Errors due to bias current and 1st Ist chopper spike current are Is = chopper spike minimized by making both amplifier inputs look back into le = bias current equal impedances to ground. 15\

PRECISION INTEGRATOR

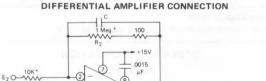


62

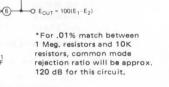
AM-490-2

15V

This configuration shows zeroing by use of a current into the summing junction.



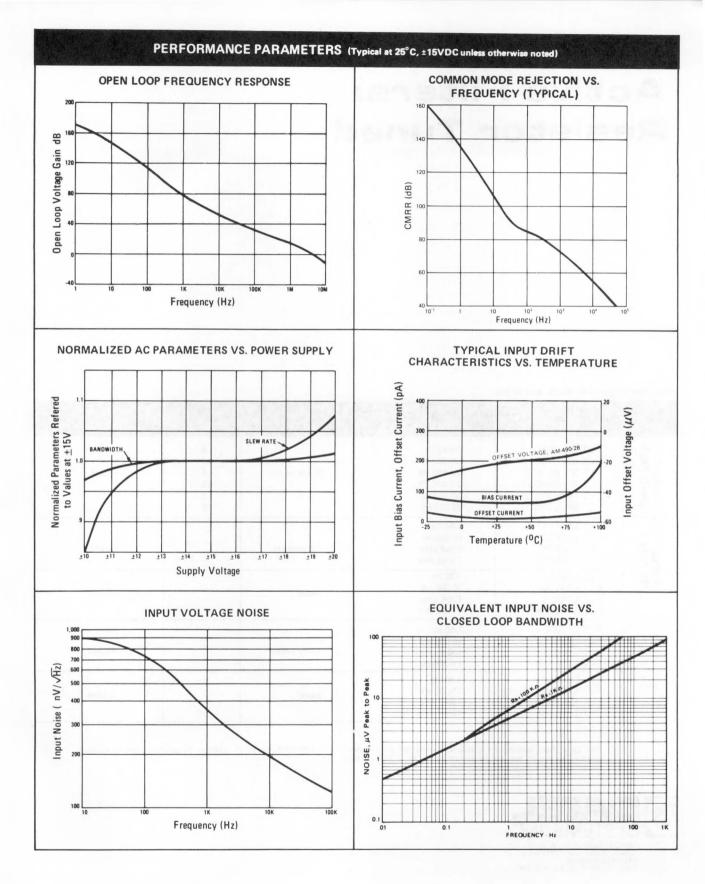
5



Capacitors C are used only to reduce bandwidth and hence output noise.

F. O

100



Active Filters: Resistor Tuned

GSA Special Item Nos. 66-31a and 66-31b

	MODEL	FREQUENCY (1)	ТҮРЕ	٥	GAIN ACCURACY (2)		
4 POLE BAND PASS	FLT-BP4B50Q5 FLT-BP4B50Q10 FLT-BP4B500Q5 FLT-BP4B500Q10 FLT-BP4B20KQ5 FLT-BP4B20KQ10	.05-50 Hz .05-50 Hz 0.5-500 Hz 0.5-500 Hz 20-500 Hz 20-20 kHz 20-20 kHz	Butterworth	5 10 5 10 5 10	±0.3dB		
POLE N PASS	FLT-LP4B50 FLT-LP4B500 FLT-LP4B5K FLT-LP4B50K	1-50 Hz 10-500 Hz 100-5 kHz 1 k-50 kHz	Butterworth	-	±.02dB		
4 PC	FLT-LP4L50 FLT-LP4L500 FLT-LP4L5K FLT-LP4L50K	1-50 Hz 10-500 Hz 100-5 kHz 1 k-50 kHz	Bessel		±.02dB		
POLE W PASS	FLT-LP6B50 FLT-LP5B500 FLT-LP6B5K FLT-LP6B50K	1-50 Hz 10-500 Hz 100-5 kHz 1 k-50 kHz	Butterworth		±.02dB		
6 PO	FLT-LP6L50 FLT-LP6L500 FLT-LP6L5K FLT-LP6L50K	1-50 Hz 10-500 Hz 100-5 kHz 1k-50 kHz	-50 Hz				

NOTES:

(1) For Low Pass models the frequency range can be extended another decade on the low frequency side with an increase by a factor of 10 of voltage offset and drift.

(2) For a gain of +1, using no external gain setting resistors.



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

GENERAL SPECIFICATIONS FOR ALL FILTERS:

Accuracy of Center or Cutoff

Frequency	±3% (using 1% tuning resistors)
Input Voltage Range	
Offset Voltage (adj. to zero)	±2mV
Output Voltage Range	±10V
Output Current	
(S.C. prot. to ground)	±2mA
Output Impedance	
Temperature Range, Operating	0°C to 70°C
Socket	MS-12 (\$5.00 each)

TUNING RESISTOR FORMULA:

$$R = 2 \left[\frac{f_0 (max.)}{f_0} - 1 \right]$$

- R is in kilohms
- $\mathbf{f}_{\mathbf{0}}$ is center frequency for Band Pass models or cutoff frequency for Low Pass models.
- $\boldsymbol{f}_0 \ \text{(max.)}$ is the maximum specified frequency for the model chosen.

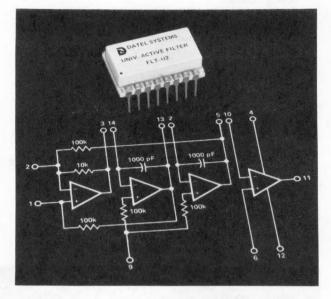


INPUT IMPEDANCE	FREQUENCY DRIFT	OFFSET DRIFT	POWER REQUIREMENT	CASE SIZE	PRICE (1-9)	
				2.0"×3.0"×0.99"	\$109.00 \$109.00	
100K ohms	±.03%/°C	±20µV/°C	±15VDC @ 16mA	2.0″×3.0″×.605″	\$ 99.00 \$ 99.00 \$109.00 \$109.00	
100K ohms	±.05%/°C	±50µV/°C	±15VDC @ 22mA	1.37''X 2.87''X 0.99''	\$ 79.00 \$ 79.00 \$ 79.00 \$ 79.00 \$ 79.00	
100K ohms	±.05%/°C	±50µ√/°C	±15VDC @ 22mA	1.37''X 2.87''X 0.99''	\$ 79.00 \$ 79.00 \$ 79.00 \$ 79.00 \$ 79.00	
10° ohms	±.05%/°C	±75µV/°C	±15VDC @ 28mA	2.0"×3.0"×0.99" 1.37"×2.87"×0.99" 1.37"×2.87"×0.99" 1.37"×2.87"×0.99"	\$109.00 \$109.00 \$109.00 \$109.00	
10° ohms	±.05%/°C	±75µV/°С	±15VDC @ 28mA	2.0"×3.0"×0.99" 1.37"×2.87"×0.99" 1.37"×2.87"×0.99" 1.37"×2.87"×0.99" 1.37"×2.87'×0.99"	\$109.00 \$109.00 \$109.00 \$109.00	

THESE FILTERS ARE COVERED BY GSA CONTRACT



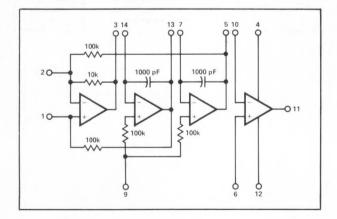
Universal Active Filter



DESCRIPTION

Datel Systems' model FLT-U2 is a universal-type active filter manufactured with hybrid technology. It uses the state variable active filter principle implemented with three committed op amps, resistors and capacitors, and a fourth uncommitted op amp which can be used to provide summing, buffering, gain, or an additional pole. The filter provides 2 pole lowpass, highpass, and bandpass functions simultaneously in addition to use in phase correction and notch circuits. The filter is tuned by 4 external resistors which set the gain, center frequency and Q of the circuit.

The Q range is up to 1000 and resonant frequency range is up to 200 kHz. Resonant frequency accuracy is typically $\pm 5\%$ and frequency stability is 100ppm/°C. The units are packaged in a 16 pin double spaced ceramic DIP.



SPECIFICATIONS (Typical at 25°C, ±15V supplies)

Frequency Range	.001 to 200 kHz
Q Range	0.1 to 1000
f _o Accuracy	±5%
f _o Tempco	100ppm/°C
Voltage Gain	0.1 to 1000
Output Voltage Range	±10V
Output Voltage	±10 mA
Amplifier Gain Bandwidth Prod	3 MHz
Input Offset Voltage	±6 mV max.
Amp. Voltage Gain	300,000
Input Offset Current	200 nA max.
Input Bias Current	500 nA max.
Output Slew Rate	1 V/μsec.
Power Supply, rated	±15 VDC
Power Supply Range	±5 to ±18 VDC
Quiescent Current	9 mA
Operating Temperature Range	0°C to 70°C
Package	16 pin double DIP
Price (1-9)	\$16.00



UNIVERSAL VOLTAGE TO FREQUENCY AND FREQUENCY TO VOLTAGE CONVERTER

VFV SERIES

FEATURES

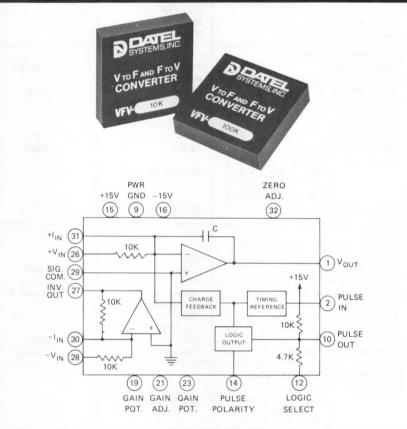
- ▶ Linearity to .005%
- V or I Input
- V/F or F/V Conversion
- 10kHz or 100kHz FS
- DTL/TTL or CMOS Output

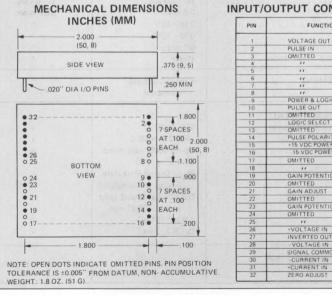
GENERAL DESCRIPTION

The VFV series voltage to frequency converters, with universal operating characteristics, offers significant advantages over other available units. These converters can be operated as either voltage to frequency or frequency to voltage converters by external pin connection. In addition, voltage inputs of 0 to +10V or 0 to -10V and current inputs of 0 to +1mA or 0 to - 1mA can be chosen by pin connection. As an F/V converter either 0 to +10V or 0 to -10V outputs can be chosen by pin connection. Output pulses can be selected to be positive or negative going, with DTL/TTL, CMOS, or high level logic interfacing. The output is short circuit proof to common or either supply voltage. The result of these universal pin connectable operating characteristics is wide flexibility in applications.

There are two basic models in this series, the VFV-10K and VFV-100K, with 10kHz and 100kHz full scale output frequencies respectively. Both models have a linear minimum overrange capability of 10%. The linearity holds down to zero input, resulting in an extremely wide dynamic range of operation. The output pulses are constant width pulses of 70 µsec. for the VFV-10K and 7 µsec. for the VFV-100K. Both models are internally trimmed to 1% accuracy with external offset and gain adjustments for precise calibration in a specific application. When used as an F/V converter, an external capacitor can be used to reduce output ripple to a specified level.

The modules are epoxy encapsulated in a compact 2 x 2 x .375 inch case with DIP compatible 0.100 inch pin spacing.





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	
1	VOLTAGE OUT	
2	PULSE IN	1.1
3	OMITTED	
4	11	
5	an and an arrest desperation of the second states and	
6	11	
7		
8	"	
9	POWER & LOGIC GND	
10	PULSE OUT	
11	OMITTED	
12	LOGIC SELECT	
13	OMITTED	
14	PULSE POLARITY	
15	+15 VDC POWER	
16	15 VDC POWER	
17	OMITTED	
18	11	
19	GAIN POTENTIOMETER	323
20	OMITTED	
21	GAIN ADJUST	
22	OMITTED	
23	GAIN POTENTIOMETER	
24	OMITTED	
25	"	
26	+VOLTAGE IN	
27	INVERTED OUT	
28	- VOLTAGE IN	10.11
29	SIGNAL COMMON	
30	-CURRENT IN	11
31	+CURRENT IN	-
32	ZERO ADJUST	

SPECIFICATIONS

Typical at 25°C, ±15V Supplies unless otherwise noted	VFV-10K	VFV-100K		
//F CONVERTER INPUT				
Input Voltage Range	0 to +10V			
	0 to -10V			
Input Current Range	0 to +1mA			
	0 to -1mA	*		
Input Overrange, min	10% 10K ohms	•		
//F CONVERTER OUTPUT	a thing was the			
Frequency Range	0 to 10kHz	0 to 100kHz		
Frequency Overrange, min	10%	*		
Pulse Width	70 μsec 200 nsec.	7 µsec		
Pulse Polarity.	Pos. or Neg.	*		
Settling Time to .01%	1 pulse of new freq.	*		
Overload Recovery.	1 pulse of new freq.			
Capacitive Loading, max	1000pF	100pF		
Output Logic Output				
Code Min. Max. 1 +2.4V +15V 0 0V +0.4V	DTL/TTL or CMOS	*		
Output Loading, S.C. protected	12 TTL loads			
CCURACY		Read and		
Full Scale Error, pretrimmed, max. (adj.	±1%			
to zero)	± 1% ±.005%	±.05%		
Offset Voltage, max. (adj. to zero)	±10mV	*		
Temp. Coefficient of Gain max	±20ppm/°C	±100ppm/°C		
Gain vs. time	±100ppm/day	*		
Temp. Coefficient of Zero, max	±30µV/°C	*		
Zero Drift vs. Time	±10µV/day	*		
Power Supply Sensitivity, max	.002%/%	.02%/%		
Warm Up Time to Rated Accuracy	1 minute	5 minutes		
V CONVERTER SPECIFICATIONS				
Input Pulses Input Code Min. Max.	Negative Going	*		
1 0V +0.8V 0 +2.0V +15V	<1TTL Load	*		
Input Impedance, min	30K ohms	4K ohms		
Input Pulse Width	10 - 60 µsec.	1 – 6 μsec.		
Filter Time Constant	0.5 msec.	.025 msec.		
Output Voltage	0 to +10V			
Outra to langed and a	0 to -10V			
Output Impedance	0.1 ohm ±5mA	*		
OWER REQUIREMENT	±15VDC@25mA quiescent			
HYSICAL-ENVIRONMENTAL				
Operating Temperature Range	0° C to 70° C			
Storage Temperature Range	-55°C to +85°C	*		
Case Size	Up to 100% non. cond. 2" x 2" x .375"	*		
Case Material	Black Diallyl Phthalate,			
	Epoxy Encapsulated			
Pins	0.020" dia. round, gold plated, .250" min.	•		
Weight	1.8 oz. (51 g.) DILS-2, 2 ea.	•		
Specifications same as VFV-10K				

TECHNICAL NOTES

V/F CONVERTER OPERATION

The V/F converter can be thought of as an A/D converter with serial output pulses which must be counted. The first applications diagram shows the V/F converter used as A/D converter by connecting the output to a digital counter and register. The digital counter is shown with a one second counting time base and an output register to store the output data while the V/F converter is making a conversion. The VFV-10K has a resolution of 1 part in 10,000 using a 1 second time base. This is equivalent to better than 13 bits binary resolution (1 part in 8,192). The nonlinearity of this model is 50 ppm maximum which is equivalent (50 ppm = 1/2 LSB) to a better than 13 bit binary converter. With a gain temperature stability of 20 ppm/°C worst case, the VFV-10K is equivalent to a very high quality A/D converter in its performance.

The VFV-100K has a resolution of 1 part in 100,000 using a 1 second time base. This is equivalent to better than 16 bits binary resolution (1 part in 65,536). The VFV-100K can be used to give equivalent resolution to the VFV-10K with only one tenth the time base, or 0.1 second for a resolution of 1 part in 10,000. An important characteristic of both the VFV-10K and VFV-100K is that their linearity does not fall off near zero as with some other converters. They are both linear right to zero. and this results in a wide dynamic operating range. In practice the lower limit of operation is about 1 millivolt input due to adjustment accuracy, long term stability, temperature drift, etc. This results in a dynamic range of 10,000 to 1 of 80dB for both models.

As a V/F converter positive inputs are achieved using inputs directly into the integrator (pins 26 or 31). For negative inputs the internal inverting amplifier is connected ahead of the integrator and the input is applied to pin 28 or 30. Using both the inverting amplifier inputs and the integrator inputs it is possible to algebraically add and subtract inputs for V/F converter operation.

The output logic level can be set from 0 to +15V by use of an external resistor connected to pin 10 while pin 12 is left open. The output voltage is determined by the resistor ratio with the internal 10K ohm resistor as shown in the Output Logic Connections diagram.

F/V CONVERTER OPERATION

For operation as an F/V converter negative going input pulses must be used. The pulses must go from a HI logic level of +2.0V to +15V to a LO logic level of 0 to +0.8V. The pulse widths must be between 10 and 60 usec for the VFV-10K and 1 and 6 usec for the VFV-10K. If these pulse widths are not available, then input conditioning circuits must be used as shown in the diagrams of Input Conditioning for F/V Converter.

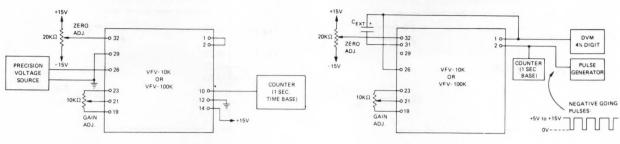
Output ripple of the F/V converter can be made arbitrarily low by using an external filtering capacitor. This also slows down the output response time. As an F/V converter, a positive output is taken directly from the integrator output (pin1). For a negative output voltage the internal inverting amplifier is used after the integrator and the output is taken at pin 27.

CALIBRATION PROCEDURE



AS V/F CONVERTER

AS F/V CONVERTER



Trimming potentiometers are 100ppm/°C, 15 turn type, available from Datel Systems at \$3.00 each.

V/F CONVERTER

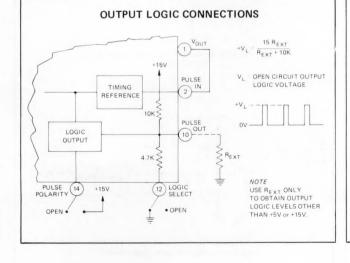
- 1. Connect the unit as a V/F converter as shown above with zero and gain trimming potentiometers.
- Connect a precision dial-up voltage source to +Vin (pin 26) and a digital counter and display set to a 1 second time base to PULSE OUT (pin 10) as shown.
- Set the precision voltage source to +.010 volt and adjust the zero trimming potentiometer to give an output count of 10 for the VFV-10K or 100 for the VFV-100K.
- Set the precision voltage source to +10.000 volts and adjust the gain trimming potentiometer to give an output count of 10,000 for the VFV-10K or 100,000 for the VFV-100K.

The above procedure applies for a positive input voltage V/F converter. For a negative input voltage, connect pin 27 to pin 26 and use pin 28 as the input.

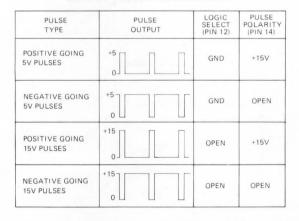
F/V CONVERTER

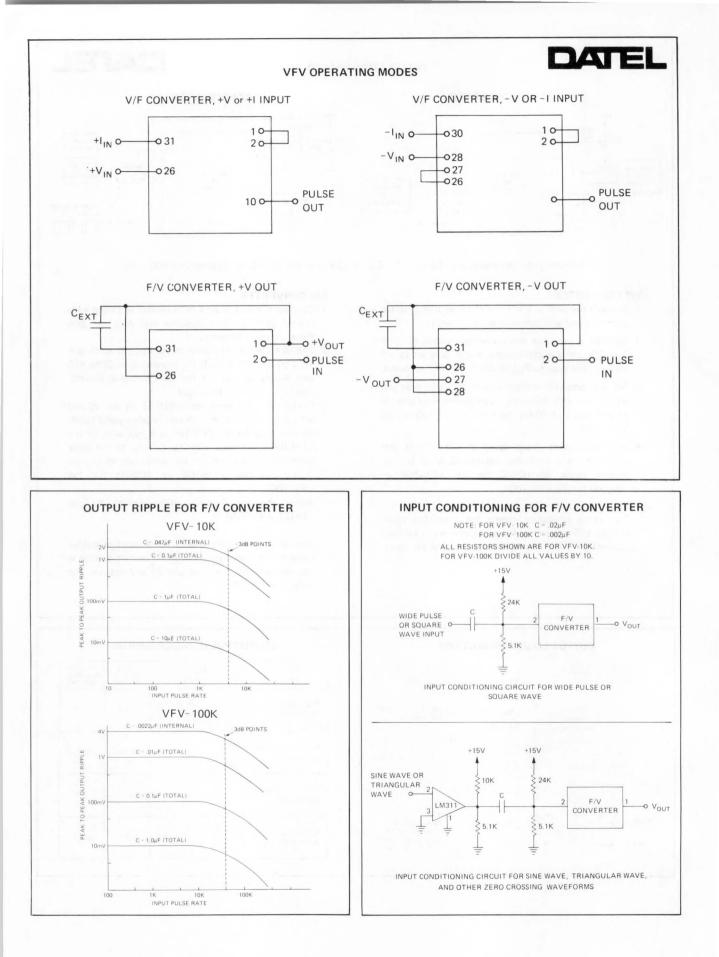
- Connect the unit as an F/V converter as shown with desired external filter capacitor and zero and gain trimming potentiometers.
- Connect a 4-1/2 digit DVM to the Vout terminal (pin 1). Connect the PULSE IN terminal (pin 2) to +15 volt supply, and adjust the zero trimming potentiometer for 0.000 volts output.
- 3. Connect a pulse generator to PULSE IN (pin 2) and set the generator to give +5 volt negative going pulses 50 μ sec wide for the VFV-10K or 5 μ sec wide for the VFV-100K. Connect a digital counter to the pulse generator output and set the pulse rate to exactly 10kHz for the VFV-10K or 100kHz for the VFV-100K.
- Adjust the gain trimming potentiometer to give +10.000 volts output.

The above procedure applies for a positive output voltage F/V converter. If negative output voltage is desired, connect pin 1 to pin 28 and measure the output at pin 27.

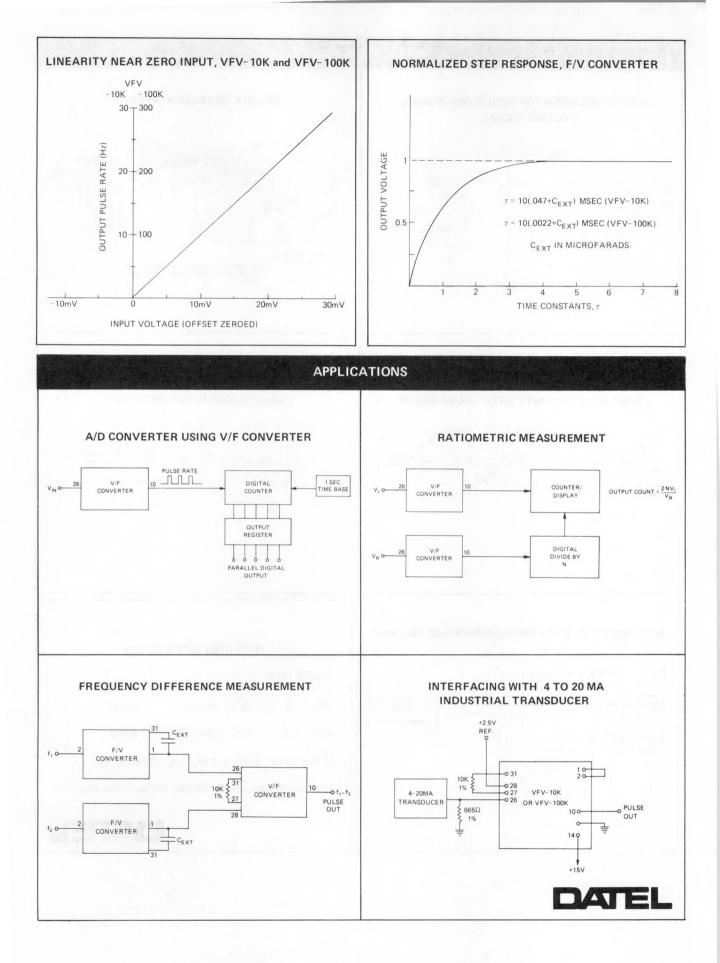


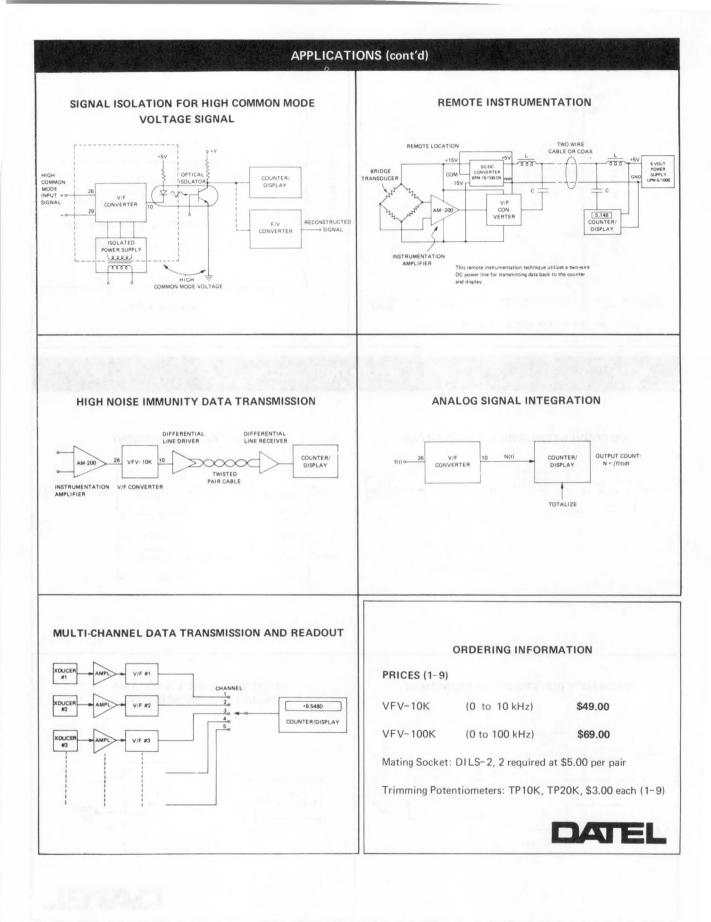
OUTPUT PULSE PROGRAMMING





Electronic Design's



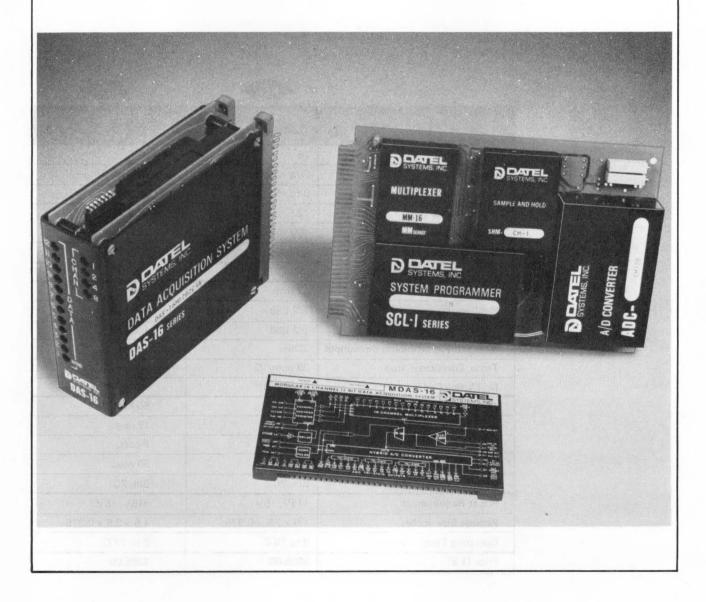


Electronic Design's



Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

Modular Data Acquisition Systems



Modular Data Acquisition Systems

	NEW	NEW
	MDAS-16	MDAS-8D
	Low Cost	Low Cost
No. Channels	16	8
Input Type	Single Ended	Differential
Input Voltage Ranges, Unipolar	0 to +5, +10V	0 to +5, +10V
Input Voltage Ranges, Bipolar	±2.5, ±5, ±10V	±2.5, ±5, ±10V
Input Impedance	100 Meg.	100 Meg.
Channel Addressing	4 Bit Code	3 Bit Code
Address Logic Compatibility	DTL/TTL	DTL/TTL
Resolution	12 Bits	12 Bits
Nonlinearity, max.	1/2 LSB	1/2 LSB
Differential Nonlinearity, max.	1/2 LSB	1/2 LSB
Max. Error at maximum throughput	.025%	.025%
Temp. Coefficient, max.	30 ppm/°C	30 ppm/°C
No Missing Codes	0 to 70°C	0 to 70°C
Throughput Rate, max.	50 kHz	50 kHz
Acquisition Time	12 µsec.	12 µsec.
Conversion Time	8 μsec.	8 µsec.
Aperture Time	50 nsec.	50 nsec.
Output Coding	Bin, 2C	Bin, 2C
Power Requirement	±15V, +5V	±15V, +5V
Package Size, inches	4.6 x 2.5 x 0.375	4.6 x 2.5 x 0.375
Operating Temp. Range	0 to 70°C	0 to 70°C
Price (1-9)	\$295.00	\$295.00

Vol 3/154

Electronic Design's

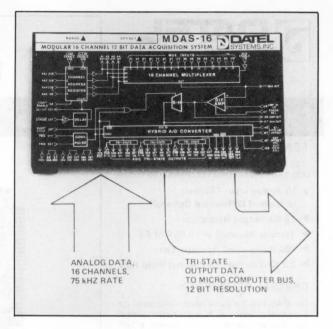
DESCRIPTION

This comprehensive line of modular data acquisition systems gives the user a range of choices from a miniature low cost 8 or 16 channel system, a 16 channel high speed system, to an 8 or 16 channel low power CMOS system.

MDAS-16, MDAS-8D: These new models are only $4.6 \times 2.5 \times 0.375$ inches in size and cost \$295. Features are 5 programmed input ranges, 16 single-ended or 8 differential channels, 12 bit resolution, and 50 kHz throughput rate. These models represent the best price-performance combination available.

DAS-250: This model, soon to be available, offers 16 channel capability at 250 kHz throughput rate. Resolution is 12 bits and the unit offers 0 to \pm 10V or \pm 5V single-ended input ranges. Package size is 5.0 x 4.5 x 1.5 inches.

DAS-16-LP12B, DAS-8D-LP12B: These two CMOS systems are low power units specifically for battery operated portable and remote data acquisition requirements. Both units operate from a single +12V to +15V power supply. The package is a 6.5 x 4.5 inch circuit card.



COMING SOON

DAS-250	DAS-16-LP12B	DAS-8D-LP12B		
High Speed	Low Power CMOS	Low Power CMOS		
16	16	8		
Single Ended	Single Ended	Differential		
0 to +10V	0 to +5, +10V	0 to +5, +10V		
±5V	±5, ±10V	±5, ±10V		
100 Meg.	1000 Meg.	1000 Meg.		
4 Bit Code	4 Bit Code	3 Bit Code		
DTL/TTL	CMOS	CMOS		
12 Bits	12 Bits	12 Bits		
1/2 LSB	1/2 LSB	1/2 LSB		
1/2 LSB	1/2 LSB	1/2 LSB		
.025%	.05%	.05%		
40 ppm/°C	150 ppm/°C	150 ppm/°C		
0 to 70°C	0 to 70°C	0 to 70°C		
250 kHz	2.2 kHz	2.2 kHz		
2 μsec.	150 μsec.	150 μsec.		
2 µsec.	310 µsec.	310 µsec.		
20 nsec.	100 nsec.	100 nsec.		
Bin, 2C	Bin, 2C	Bin, 2C		
±15V, +5V	+12 to +15V	+12 to +15V		
5.0 × 4.5 × 1.5	6.5 × 4.5 × 1.0	6.5 x 4.5 x 1.0		
0 to 70°C	0 to 70°C	0 to 70°C		
\$595.00	\$495.00	\$545.00		



LOW POWER 16 CHANNEL DATA ACQUISITION SYSTEM

MODEL DAS-16-LP

FEATURES

LESS THAN 120 MICROWATTS STANDBY POWER LESS THAN 200 MILLIWATTS OPERATING POWER

- 16 Analog Input Channels (8 Channel Differential Optional)
- ▶ 12 Bit Output Resolution
- ► Transfer Accuracy of ±0.05% of FS
- ▶ 100 Nanosecond Aperture Time
- ▶ 2.2 KHz System Throughput Word Rate

GENERAL DESCRIPTION

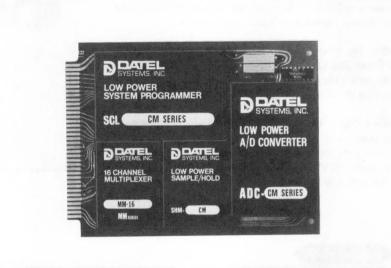
The DAS-16-LP is a low power 16-channel (or 8 channel differential) data acquisition system complete with an analog multiplexer, a high performance sample and hold amplifier, a high accuracy 12 bit analog-to-digital converter, plus all the necessary control logic for both random and sequential channel selection – all mounted on a 4½ by 6½ inch PC board.

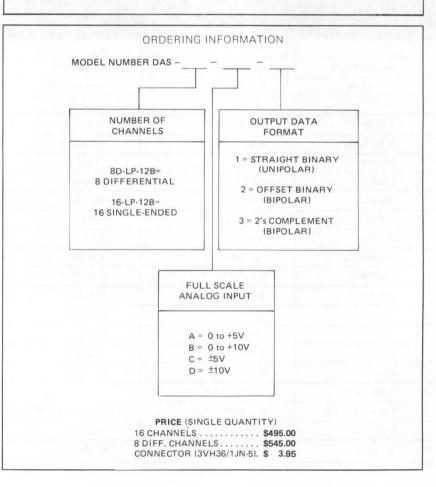
The remarkable feature of the DAS-16-LP however is its low power consumption of less than 200 milliwatts while operating, and only 120 microwatts in stand-by. A unique power supply operating from +12 to +15 volts generates bipolar power to the analog section only when a conversion is in process, thus providing power savings during standby. In addition, the system can be operated continuously from a bipolar power source.

Since the DAS-16-LP can be powered from a 12 volt battery for long periods of time, it easily lends itself to remote applications. As such, the DAS-16-LP is an ideal acquisition system for gathering oceanographic, meteorological, seismological, pollution or general environmental data. The system's computer compatible interface also makes it ideal for laboratory or industrial control use.

The 16 single-ended input channels (or 8 channel differential) can accept either 0 to +5 volt or ±5 volt full scale signals with 12 volt power and when 15 volt power is provided, either 0 to +10 volt or ±10 volt full scale signals can be accepted in addition. System transfer accuracy is 0.05% of full scale, ±1/2 LSB, with a linearity of ±1/2 LSB and a temperature coefficient of 150 ppm/°C. Dynamically, the input data acquisition time is 150 microseconds and the aperture time of the sample and hold amplifier is less than 100 nanoseconds. Data conversion is completed in less than 460 microseconds therefore the system throughput rate is 2.2 KHz.

The control logic included with the DAS-16-LP provides for input command storage using the device select and strobe inputs to enable the other input commands. As such, the input commands are only required to be true during the strobe period thus allowing for party line or computer bus operation. Besides providing random access to the input channels, an internal counter allows sequential addressing and a frame sync output indicates when the counter is at channel one. Short cycle inputs and outputs are also provided so the counter can be preset to jump back to channel one from any channel.







MINIATURE MODULAR DATA ACQUISTION SYSTEM

MODELS MDAS-16, MDAS-8D

FEATURES

- 16 Channels Single Ended or 8 Channels Differential
- 12 Bits Resolution
- 50 kHz Throughput Rate
- Tri-State Outputs
- Low Cost -
- Miniature Size

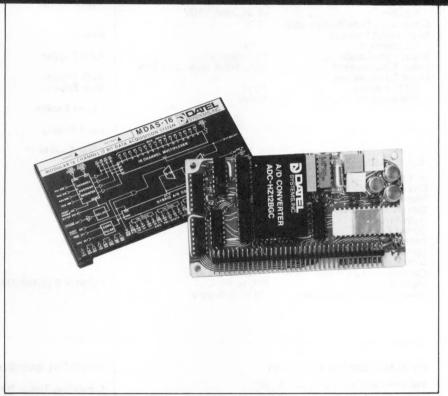
DESCRIPTION

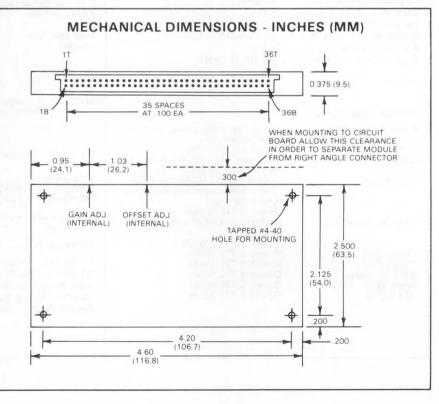
The MDAS-16 and MDAS-8D data acquisition modules are complete, selfcontained systems featuring 16 channel single ended or 8 channel differential operation respectively. Resolution is 12 bits and throughput rate is 50 kHz. Output data is buffered tri-state for interfacing to mini or micro-computer data buses. Output data can be transferred in three 4 bit bytes. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

The 4.6 x 2.5 x 0.375 inch size of these modules is $\frac{1}{2}$ inch narrower than other competitive models. The small size and low cost are made possible by extensive use of hybrid and monolithic circuits to reduce parts count and increase reliability. Both models use Datel Systems' new ADC-HZ12BGC 12 bit hybrid A/D converter along with a monolithic sample-hold and analog multiplexer.

The MDAS-16 and MDAS-8D feature a high degree of user flexibility with pinprogrammable input ranges of 0 to +5V, 0 to +10V, $\pm 2.5V$, $\pm 5V$, and $\pm 10V$. The systems may be operated in either random or sequential channel addressing modes. For applications where lower than 12 bit resolution can be used, the A/D converter can be short-cycled to achieve a faster conversion rate. Output data is also available in serial form with a gated clock output.

The modules are housed in a shielded steel case. Input-output connections are made by means of a 72-pin connector. The number of channels may be expanded by 32 for the MDAS-16 or by 16 for the MDAS-8D by use of the multiplexer expander modules MDXP-32, and MDXP-32-1.





GOLD BOOK 76/77

See inside back cover for DATEL sales offices

SPECIFICATIONS, MDAS-16 & MDAS-8D (Typical at $25^{\circ}C$, $\pm 15V$ and $\pm 5V$ supplies unless otherwise indicated)

ANALOG INPUTS

16 Single Ended (MDAS-16) Number of Channels **Input Voltage Ranges** unipolar bipolar Common Mode Range, min. ±10V Max. Input Voltage, no damage ±15V Input Impedance Input Bias Current Input Capacitance OFF channel 10 pF ON channel 100pF

8 Differential (MDAS-8D) 0 to +5V 0 to +10V ±2.5V, ±5V, ±10V 100 megohms 3nA, 10nA max. 0 to 70°C

DIGITAL INPUTS

Enable	Three separate inputs which enable tri-state outputs in 4 bit bytes.
Mux Address In	1 TTL load 3 bit (MDAS-8D) or 4 bit (MDAS-16) binary address
Strobe	1 LS TTL load 1 LS TTL load with 10K pull-up
A/D Trigger	resistor 1 LS TTL load with 10K pull-up resistor
A/D Trigger Mux Enable	1 LS TTL Load 1 TTL load with 10K pull-up
Count Enable	resistor 1 LS TTL load with 10K pull-up resistor
Load Enable	1 LS TTL load with 10K pull-up
Clear Enable	resistor 1 LS TTL load with 10K pull-up
MSB In	resistor 1 TTL load 1 TTL load with 10K pull-up resistor

ACCURACY

Resolution Error, max. 50 kHz sampling ±.025% of FSR Nonlinearity, max. Diff. Nonlinearity, max. Gain Error Offset Error Temp. Coeff. of Gain, max. ±30ppm/°C Temp. Coeff. of Offset, max. ±7ppm/°C of FS Diff. Linearity Tempco, max. Common Mode Rejec., min. Monotonicity Power Supply Rejection

12 Bits ±1/2 LSB ±1/2 LSB Adj. to zero Adj. to zero ±3ppm/°C of FS 70 dB at 1 kHz 0°C to 70°C .01%/% Supply

POWER REQUIREMENT

+15VDC ±0.5V@65mA -15VDC ±0.5V@60 mA +5VDC ±0.25V @ 200mA

PHYSICAL ENVIRONMENTAL

Operatin														
Storage	lemp	e	ra	a	tι	re	Э	ł	۲.	а	n	Q	16	Э
Package														
Package Weight	Туре		5	÷										

0°C to 70°C -25°C to +85°C 4.6 x 2.5 x 0.375 inches (116,8 x 63,5 x 9,5 mm) Steel, shielded on 5 sides 6 oz. (170 g)

NOTES: 1. All outputs are Vout ("O") ${}^{>}+0.4V$, Vout ("1") ${}^{>}+2.4V$ 2. All inputs are Vin ("O") ${}^{>}+0.8V$, Vin ("1") ${}^{>}+2.0V$

ORDERING INFORMATION

Price (1-9)	
MDAS-16	\$295.00
MDAS-8D	\$295.00

Included with each module is a mating right-angle 72 pin connector.

Trimming Potentiometers: TP 20K \$3.00 each.

Multiplexer expander modules are also available. The MDXP-32 adds 32 single ended or 16 differential channels with control logic. Price is \$199.00. The MDXP-32-1 is identical but without control logic. Price is \$179.00. Consult factory for delivery.

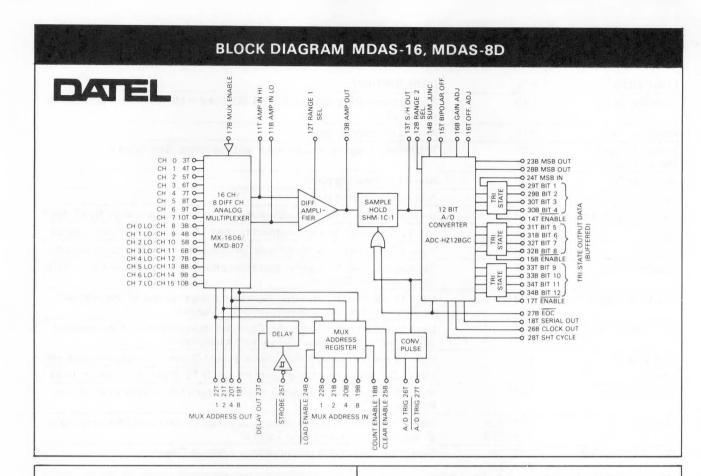


DYNAMIC CHARACTERISTICS

Throughput Rate, max	50 kHz
Acquisition Time	12 µsec.
Conversion Time	8 µsec.
Aperture Time, max	50 nsec.
Sample-Hold Droop, max	50 µV/msec.
Feedthrough, max	.01%
Channel Crosstalk (Mux.)	-80 dB at 1 kHz

DIGITAL OUTPUTS

DIGITAL OUTFOID	
Parallel Data Out	12 parallel lines of buffered tri- state output data. Drives 12 TTL loads.
Coding	Straight binary, offset binary, and two's complement
Serial Out	Output data in MSB first, NRZ format. Straight binary and offset binary coding. Drives 5 TTL loads
Mux Address Out	Buffered output of address register Drives 20 TTL loads
Delay Out	Drives 5 TTL loads
Clock Out	Drives 5 TTL loads
EOC (Status)	Drives 4 TTL loads
MSB Out	Drives 5 TTL loads
MSB Out	Drives 5 TTL loads



PIN CONNECTIONS for MDAS-16

	Тор	Bottom	
+15VDC	1T	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. O In	3T	3B	Ch. 8 In
Ch. 1 In	4T	4B	Ch. 9 In
Ch. 2 In	5T	58	Ch. 10 In
Ch. 3 In	6T	6B	Ch. 11 In
Ch. 4 In	71	7B	Ch. 12 In
Ch. 5 In	8T	8B	Ch. 13 In
Ch. 6 In	9T	9B	Ch. 14 In
Ch. 7 In	10T	10B	Ch. 15 In
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum. Junc. (Bipolar Off.)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out] Mux	19T	19B	8 In Mux
4 Out Address	20T	20B	4 In Address
2 Out Lines	21T	21B	2 In Lines
1 Out	22T	22B	1 In]
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC
	*Tri-St	ate Outpu	ts

PIN CONNECTIONS for MDAS-8D

	Тор	Bottom	
+15VDC	11	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. O Hi In	3T	3B	Ch. O Lo In
Ch. 1 Hi In	4T	4B	Ch. 1 Lo In
Ch. 2 Hi In	5T	5B	Ch. 2 Lo In
Ch. 3 Hi In	6T	6B	Ch. 3 Lo In
Ch. 4 Hi In	71	7B	Ch. 4 Lo In
Ch. 5 Hi In	8T	8B	Ch. 5 Lo In
Ch. 6 Hi In	9T	9B	Ch. 6 Lo In
Ch. 7 Hi In			Ch. 7 Lo In
	10T	10B	
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum.Junc.(Bipolar Off!)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12 Out)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out Mux	19T	19B	8 In] Mux
4 Out Address	20T	20B	4 In Address
2 Out Lines	21T	21B	2 In Lines
1 Out	22T	22B	1In Junes
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC
	*Tri-St	ate Outpu	ts

TABLE I DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION	
Amplifier In Lo	11B	Analog monitoring point for MDAS-8D. For the MDAS-16 this pin must be grounded.	
Amplifier In Hi	11T	Analog monitoring point.	
Range 2 Select Range 1 Select	12B 12T	These pins program analog input voltage range. See Table II	
Amplifier Out	13B	Analog monitoring point.	
Sample Hold Out	13T	Analog monitoring point.	
Summing Junction	14B	Used to program analog input voltage range and bipolar offset. See Table I	
Enable	14T	Input LO enables tri-state outputs for bits 1-4. Input HI inhibits outputs.	
Enable	15B	Input LO enables tri-state outputs for bits 5-8. Input HI inhibits outputs.	
Bipolar Offset	15T	Connects to 14B for bipolar operation and to analog ground for unipolar operation. See Table II	
Ext. Gain Adjust	16B	Used to adjust out gain error. Operates independently of the internal adjustment. See External Adjustments diagram.	
Ext. Offset Adjust	16T	Used to adjust out offset error. Operates independently of the internal adjustment. See External Adjustments diagram.	
Mux Enable	17B	Input HI enables analog multiplexer. Input LO inhibits analog multiplexer.	
Enable	17T	Input LO enables tri-state outputs for bits 9-12. Input HI inhibits outputs.	
Count Enable	18B	Input HI enables Mux Address Register. Input LO inhibits Mux address Register.	
Mux Address In	19B, 20B, 21B, 22B	Digital inputs for channel address selection in random addressing mode. Straight binary coding. See Table III	
Mux Address Out	19T, 20T, 21T, 22T	Straight binary coded output of Mux Address Register.	
MSB Out	23B	Bit 1 TTL output of A/D converter. Connect to pin 24T for straight binary or offset binary output coding.	
Delay Output	23T	An output delay pulse set for 12µsec. to allow for multiplexer and an plifier settling time and sample hold acquisition time. This pin is no mally connected to A/D Trigger (pin 27T) to initiate A/D conversion	
Load Enable	24B	Input HI for sequential addressing. Input LO for random addressing.	
MSB In	24T	Bit 1 input to tri-state output buffers. Connect to either pin 23B (MSB Out) or pin 28B (MSB Out).	
Clear Enable	25B	Input LO and a negative transition on pin 25T resets Mux address counter to zero.	
Strobe	25T	Negative input transition initiates channel scanning sequence in sequentia mode or a conversion in the random mode. A Schmidt trigger input adds hysteresis for good noise rejection.	
Clock Output	26B	A/D converter clock pulses for synchronization of serial data. Negative going pulses of approximately 100 nsec. duration.	
A/D Trigger	26T	A positive logic transition on this input initiates A/D conversion.	
EOC (status)	27B	End of conversion (status) output. Output HI during conversion and LO when conversion is complete.	
A/D Trigger	27T	A negative logic transition on this input initiates A/D conversion. This pi is normally connected to pin 23T (Delay Output).	
MSB Out	28B	Complemented bit 1 TTL output of A/D converter. Connect to pin 24T for two's complement output coding.	
Short Cycle	287	For 12 bit resolution connect this pin to ground. To short cycle A/D converter for lower resolution, connect this pin to output bit n + 1 for a resolution of n bits. Short cycling of the A/D converter can only be done with the Enable inputs (pins 14T, 15B and 17T) LO.	

CONNECTION DIAGRAMS AND TABLES

TABLE II INPUT RANGE SELECTION

	CONNECT THESE PINS TOGETHER						
INPUT RANGE	RANGE 1 PIN 12T	RANGE 2 PIN 12B	BIPOLAR OFF. PIN 15T				
0 TO +5V	13B	13T	2B OR 2T				
0 TO +10V	2B OR 2T	13T	2B OR 2T				
±2.5V	13B	13T	14B				
± 5V	2B OR 2T	13T	14B				
±10V	2B OR 2T	OPEN	14B				

TABLE IV THROUGHPUT RATES VS. NO. BITS FOR SHORT-CYCLED A/D CONVERTER

NO. BITS	THROUGHPUT RATE
12	50 kHz
10	53 kHz
8	57 kHz
4	67 kHz



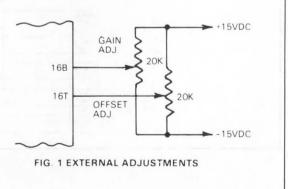
TABLE III MUX CHANNEL ADDRESSING

one Trace 12 U. o	Ш		>	DRESS- PIN	MUX AD	
	NNEL		22B	21B	20B	19B
non in other and the second	CHAN	MUX ENAB.	1	2	4	8
and the second second	NONE	0	X	X	X	X
Links a fur outface	0	1	0	0	0	0
iden i te son that	1	1	1	0	0	0
and the period of the second	2	1	0	1	0	0
An and the state of the	3	1	1	1	0	0
an briting arrestor	4	1	0	0	101 100	0
and the other ad the	5	1	1	0	1	0
MDAS-8D	6	1	0	1	1	0
(3 BIT ADDRES	7	1	1	1	1	0
	8	1	0	0	0	1
	9	1	1	0	0	1
1540M .96	10	1	0	1	0	1
	11	1	1	1	0	1
and a second	12	1	0	0	1	1
	13	1	1	0	1	1
MDAS-16	14	1	0	1	1	1
(4 BIT ADDRES	15	1	1	1	1	1

TABLE V

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
	BIPOLAR R	ANGE
±2.5V	OFFSET GAIN	-2.4994V +2.4982V
±5V	OFFSET GAIN	-4.9988V +4.9963V
±10V	OFFSET GAIN	-9.9976V +9.9927V



SET-UP AND CALIBRATION INSTRUCTIONS

- Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table II. If the MDAS-16 is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
- 2. Determine resolution to be used. For full 12 bits, ground pin 28T. For lower resolution requirements, connect pin 28T to bit output n + 1 for n bit resolution. For example: for 8 bit resolution connect pin 28T to pin 33T (Bit 9 Out). To operate the A/D converter in this short cycled mode, the Enable inputs (pins 14T, 15B, and 17T) must be connected to ground thereby enabling the tri-state outputs. For 12 bit resolution the tri-state outputs can be either enabled or disabled.
- Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar) connect pin 28B (MSB Out) to pin 24T.
- Select desired multiplexer mode. Connect pin 23T (Delay Out) to pin 27T (A/D Trigger).

A.Free Running Sequential Addressing

Connect pin 27B (EOC) to pin 25T (Strobe). Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Sequencing is initiated by a positive logic transition applied to pin 26T (A/D Trigger). Pin 26T must remain HI during free running sequential addressing. Sequencing is stopped by a LO applied to pin 26T.

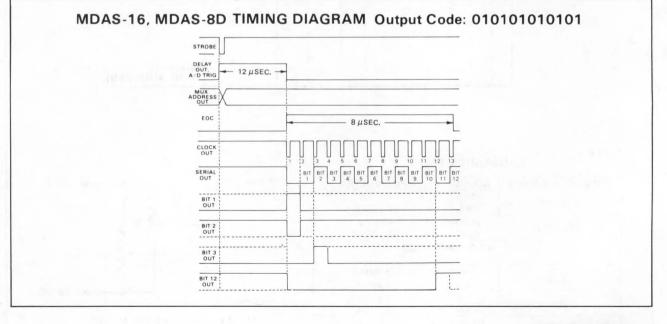
B.Triggered Sequential Addressing

Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Apply a falling edge trigger to pin 25T (Strobe). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.

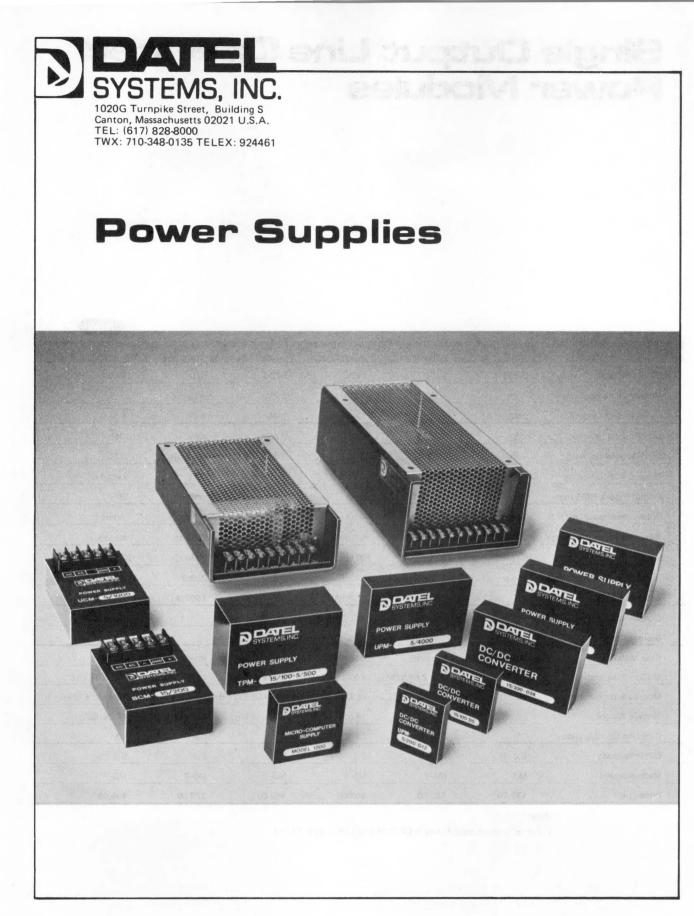
C.Random Addressing

Ground pin 24B (Load Enable). Leave pin 25B (Clear Enable) open. Each negative transition applied to pin 25T (Strobe) will cause the data at pins 19B, 20B, 21B and 22B (Mux Address In) to be loaded into the Address Register. Address inputs must be stable for at least 300 nsec, after negative transition of Strobe.

- 5. Calibration Procedure
 - A. Offset and gain adjustments may be made either internally or externally. Self-contained trimming potentiometers are provided for the internal adjustments. For external adjustment, 20K trimming potentiometers must be used with pins 16B and 16T. Connect as shown in Figure 1.
 - B. Connect power supplies to the module and a precision voltage source to pin 3T (Chan O In). If the MDAS-8D is used, connect pin 3B (Chan O LO) to analog ground. Ground pin 25B (Clear Enable) and momentarily short pin 25T (Strobe) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50kHz positive going pulses applied to pin 26T (A/D Trigger).
 - C. Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + $\frac{1}{2}$ LSB) or the bipolar offset adjustment (-FS + $\frac{1}{2}$ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
 - D. Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS 1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.







GOLD BOOK 76/77

Single Output Line Operated Power Modules

						NEW
SPECIFICATIONS, 25°C	UPM-5/250	UPM-5/500	UPM-5/1000	UPM-5/1000B	UPM-5/2000	UPM-5/4000
Output Voltage	5VDC	5VDC	5VDC	5VDC	5VDC	5VDC
Output Voltage Accuracy	±1%	±1%	±1%	±2%	±1%	±1%
Rated Output Current	250mA	500mA	1.0A	1.0A	2.0A	4.0A
Line Regulation, max.	.05%	.05%	.05%	0.25%	.05%	.05%
Load Regulation, max.	0.1%	0.1%	0.1%	0.25%	0.1%	0.1%
Temp. Coefficient, max.	.02%/°C	.02%/°C	.02%/°C	.02%/°C	.02%/°C	.02%/°C
Output Ripple, RMS max.	1mV	1mV	1mV	mV	1mV	2mV
Output Impedance, max.	.05Ω	.05Ω	.01Ω	.01Ω	.005Ω	.005Ω
Trans. Recovery Time, max.	50 µsec.	50 µsec.	50 µsec.	50 µsec.	50 µsec.	50 µsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range		1 1 3 1 1 4 1 4 1 4 1 4 1 4 1 4 1 4 1 4	-25°C to +71°C	C (No Derating)		
Storage Temp. Range	1		-25°C to +85°C	0		Carlo and
Case Material	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5X2.5X.875	3.5X2.5X.875	3.5X2.5X1.25	3.5X2.5X1.25	3.5X2.5X1.56	3.5X2.5X1.56
Module Size, millimeters	88,9X63,5X22,2	88,9X63,5X22,2	88,9X63,5X31,8	88,9X63,5X31,8	88,9X63,5X39,6	88,9X63,5X39,6
Module Weight	14 oz.(397g)	14 oz.(397g)	18 oz.(510g)	18 oz. (510g)	24 oz.(680g)	24 oz.(680g)
Case/Pin Configuration	C1	C1	C2	C2	C3	C3
Other Versions	E,J(1)	E,J (1)	E,J	E,J	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7	MS-7	MS-7	MS-7
Price (1-9)	\$39.00	\$49.00	\$69.00	\$49.00	\$79.00	\$99.00

Note:

1. For "E" version module size is C2 (3.5X2.5X1.25 inches, 18 oz.)



UPM-6/150A	UPM-9/100A	UPM-12/100A	UPM-15/100A
6VDC	9VDC	12VDC	15VDC
±1%	±1%	±1%	±1%
150mA	100mA	100mA	100mA
.05%	.05%	.02%	.02%
0.1%	0.1%	.05%	.05%
.02%/°C	.02%/°C	.02%/°C	.02%/°C
1mV	2mV	2mV	2mV
.05Ω	0.1Ω	0.1Ω	0.1Ω
50 µsec.	50 µsec.	50 µsec.	50 µsec.
100 Meg.	100 Meg.	100 Meg.	100 Meg.
250pF	250pF	250pF	250pF
1500VAC	1500VAC	1500VAC	1500VAC
	-25°C to +71°C	(No Derating)	
	-25°C to +85°C		
Phenolic	Phenolic	Phenolic	Phenolic
3.5X2.5X.875	3.5X2.5X.875	3.5X2.5X.875	3.5X2.5X.875
88,9X63,5X 22,2	88,9X63,5X 22,2	88,9X63,5X22,2	88,9X63,5X22,2
14 oz. (397g)	14 oz. (397g)	14 oz.(397g)	14 oz.(397g)
C1	C1	C1	C1
E,J (1)	E,J (1)	E,J (1)	E,J (1)
MS-7	MS-7	MS-7	MS-7
\$39.00	\$39.00	\$49.00	\$49.00

DESCRIPTION

This line of single output, voltage regulated DC power supplies features six 5 volt output models with output currents from 250mA to 4 amperes. In addition, there are 4 other models with 6V to 15V outputs. All outputs have current limiting short circuit protection. Temperature coefficients are .02%/°C and output ripple voltage is 1 to 2 millivolts RMS.

Model UPM-5/4000 is a special high current, high efficiency supply in a compact C3 case size. Full load efficiency of 65% is achieved by a high performance switching regulator.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: 115VAC $\pm 10\%$ @ 60 Hz

E version: 220VAC ±10% @ 50-60 Hz J version: 100VAC ±10% @ 50-60 Hz

There is no extra charge for E and J versions. When ordering, add E or J suffix after model number. Note that in some instances the module size is larger for the E version. MS-7 sockets are 3.50 each.

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Dual Output, Line Operated Power Modules

SPECIFICATIONS, 25°C	BPM-5/250	BPM-5/500	BPM-12/60	BPM-12/100	BPM-12/200	BPM-12/300
Output Voltage	±5VDC	±5VDC	±12VDC	±12VDC	±12VDC	±12VDC
Output Voltage Accuracy	±1%	±1%	±1%	±1%	±1%	±1%
Rated Output Current	±250mA	±500mA	±60mA	±100mA	±200mA	±300mA
Line Regulation, max.	.05%	.05%	.02%	.02%	.02%	.02%
Load Regulation, max.	0.1%	0.1%	.05%	.05%	.05%	.05%
Temp. Coefficient, max.	.02%/°C	.02%/°C	.02%/°C	.02%/°C	.02%/°C	.02%/°C
Output Ripple, RMS max.	1mV	1mV	2mV	2mV	2mV	2mV
Output Impedance, max.	.05Ω	.03Ω	0.2Ω	0.1Ω	.05Ω	.05Ω
Trans. Recovery Time, max.	50 µsec.					
Isolation Resistance, min.	100 Meg.					
Isolation Capacitance, max.	250pF	250pF	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range			-25°C to +71°C	(No Derating)		
Storage Temp. Range	140.05.8.2		-25°C to +85°C			
Case Material	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5X2.5X.875	3.5X2.5X1.25	3.5X2.5X.875	3.5X2.5X.875	3.5X2.5X1.25	3.5X2.5X1.56
Module Size, millimeters	88,9X63,5X22,2	88,9X63,5X31,8	88,9X63,5X22,2	88,9X63,5X22,2	88,9X63,5X31,8	88,9X63,5X39,6
Module Weight	14 oz.(397g)	18 oz.(510g)	14 oz.(397g)	14 oz. (397g)	18 oz.(510g)	24 oz.(680g)
Case/Pin Configuration	C1	C2	C1	C1	C2	C3
Other Versions	E,J (1)	E,J (2)	E,J (1)	E,J (1)	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7	MS-7	MS-7	MS-7
Price (1-9)	\$69.00	\$79.00	\$39.00	\$49.00	\$59.00	\$79.00

Notes:

(1) For "E" version module size is C2 (3.5X2.5X1.25 inches, 18 oz.)

(2) For "E" version module size is C3 (3.5X2.5X1.56 inches, 24 oz.)



	BPM-15/60	3PM-15/100 B	PM-15/200	BPM-15/300
	±15VDC	±15VDC	±15VDC	±15VDC
	±1%	±1%	±1%	±1%
	±60mA	±100mA	±200mA	±300mA
	.02%	.02%	.02%	.02%
	.05%	.05%	.05%	.05%
	.02%/°C	.02%/°C	.02%/°C	.02%/°C
	2mV	2mV	2mV	2mV
	0.2Ω	0.1Ω	.05Ω	.03Ω
	50 µsec.	50 µsec.	50 µsec.	50 µsec.
_	100 Meg.	100 Meg.	100 Meg.	100 Meg.
	250pF	250pF	250pF	250pF
	1500VAC	1500VAC	1500VAC	1500VAC
		-25°C to +71°	C (No Derating)	
		-25°C to +85°	С	
	Phenolic	Phenolic	Phenolic	Phenolic
	3.5X2.5X.875	3.5X2.5X.875	3.5X2.5X1.25	3.5X2.5X1.56
	88,9X63,5X,22,	2 88,9X63,5X,22,2	88,9X63,5X31	,8 8,9X63,5X39,6
	14 oz. (397g)	14 oz. (397g)	18 oz.(510g)	24 oz.(680g)
	C1	C1	C2	C3
	E,J (1)	E,J (1)	E,J	E,J
	MS-7	MS-7	MS-7	MS-7
	\$39.00	\$49.00	\$59.00	\$79.00

DESCRIPTION

This broad line of dual output, voltage regulated DC power supplies features 10 different models with a wide choice of output voltages and currents. Output voltages are ± 5 , ± 12 , and ± 15 VDC with $\pm 1\%$ accuracy. Rated output currents range from ± 60 to ± 500 mA with output short circuit protection.

Temperature coefficient is .02% per degree Centigrade and output ripple voltage is 1 to 2 millivolts RMS. These rugged, encapsulated modules are useful for powering a wide variety of devices including linear IC's, op amps, data converters, and other analog circuits.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: $115VAC \pm 10\%$ @ 60Hz.

E version: 220VAC $\pm 10\%$ @ 50-60Hz. J version: 100VAC $\pm 10\%$ @ 50-60Hz.

There is no extra charge for E and J versions. When ordering, add E or J suffix after model number. Note that in some instances the module size is larger for the E version. MS-7 sockets are 3.50 each.

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Triple Output Modules

These power modules are specially designed for operation with data conversion and other circuits where both a dual analog supply and a 5V logic supply are required. Using a triple output supply to power these circuits can be more economical than using two separate equivalent supplies.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: $115VAC \pm 10\%$ @ 60 Hz E version: 220VAC $\pm 10\%$ @ 50-60 Hz J version: 100VAC $\pm 10\%$ @ 50-60 Hz

Mating MS-13 sockets are \$3.50 each



Delogation of the second sectors and	NEW	NEW		
SPECIFICATIONS, 25°C	TPM-12/100-5/500	TPM-15/100-5/500		
Output Voltages	±12VDC/5VDC	±15VDC/5VDC		
Output Voltage Accuracy	±1%	±1%		
Rated Output Current	±100mA/500mA	±100mA/500mA		
Line Regulation, max.	.02% / .05%	.02% / .05%		
Load Regulation, max.	.05% / 0.1%	.05% / 0.1%		
Temperature Coefficient, max.	.02%/°C	.02%/°C		
Output Ripple, RMS max.	2mV/1mV	2mV/1mV		
Output Impedance, max.	0.1/.05 ohm	0.1/.05 ohm		
Transient Recovery Time, max.	50µsec.	50µsec.		
Isolation Resistance, min.	100 Meg.	100 Meg.		
Isolation Capacitance, max.	250pF	250pF		
Breakdown Voltage, min.	1500VAC	1500VAC		
Operating Temp. Range	-25°C to +71°C (No Derating)			
Storage Temp. Range	-25°C to +85°C	Albert, Street,		
Case Material	Phenolic	Phenolic		
Module Size, inches	3.5X2.5X1.56	3.5X2.5X1.56		
Module Size, millimeters	88,9X63,5X39,6	88,9X63,5X39,6		
Module Weight	24 oz. (681g)	24 oz. (681g)		
Case/Pin Configuration	E3	E3		
Other Versions	E,J	EJ		
Mating Socket	MS-13	MS-13		
Price (1-9)	\$67.00	\$67.00		

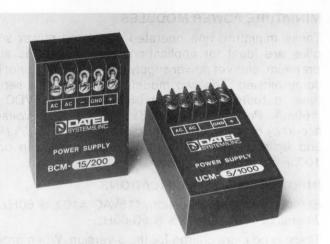
THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Chassis Mounting Modules

This line of popular power supplies has input-output connections made to a terminal strip on top of the modules. These supplies are useful in applications where it is impractical or undesirable to use printed circuit cards or sockets. For simple mounting to a metal chassis, screw inserts are provided on the bottom of the modules.

INPUT VOLTAGE SPECIFICATIONS

Standard Input Specification: $115VAC \pm 10\%$ @ 60 Hz E version: $220VAC \pm 10\%$ @ 50-60 Hz J version: $100VAC \pm 10\%$ @ 50-60 Hz



	NEW	NEW	NEW	NEW	NEW
SPECIFICATIONS. 25°C	SINGL	Ε Ουτρυτ		DUAL OUTPU	T. Start
	UCM-5/1000	UCM-5/2000	BCM-15/100	BCM-15/200	BCM-15/300
Output Voltage	5VDC	5VDC	±15VDC	±15VDC	±15VDC
Output Voltage Accuracy	±1%	±1%	±1%	±1%	±1%
Rated Output Current	1.0A	2.0A	100mA	200mA	300mA
Line Regulation, max.	.05%	.05%	.02%	.02%	.02%
Load Regulation, max.	0.1%	0.1%	.05%	.05%	.05%
Temperature Coefficient, max.	.02%/°C	.02%/°C	.02%/°C	.02%/°C	.02%/°C
Output Ripple, RMS max.	1mV	1mV	2mV	2mV	2mV
Output Impedance, max.	.01Ω	.005Ω	0.1Ω	.05Ω	.05Ω
Transient Recovery Time, max.	50µsec.	50µsec.	50µsec.	50µsec.	50µsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range	el e al l'A	-25°C to	+71°C (No Der	ating)	and a seal
Storage Temp. Range	all of the	-25°C to	0 +85°C	1	
Case Material	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5X2.5X1.25	3.5X2.5X1.56	3.5X2.5X.875	3.5X2.5X1.25	3.5X2.5X1.56
Module Size, millimeters	88,9X63,5X31,8	88,9X63,5X39,6	88,9X63,5X22,	2 88,9X63,5X31	8 88,9X63,5X3
Module Weight	18 oz.(510g)	24 oz.(680g)	14 oz.(397g)	18 oz.(510g)	24 oz.(680g)
Case/Pin Configuration	D2	D3	D1	D2	D3
Other Versions	E,J	E,J	E,J (1)	E,J	E,J
Price (1-9)	\$69.00	\$79.00	\$54.00	\$64.00	\$79.00

Note:

1. For "E" version module size is D2 (3.5X2.5X1.25 inches, 18 oz.)

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

GOLD BOOK 76/77

See inside back cover for DATEL sales offices

Miniature Power Modules

MINIATURE POWER MODULES

These miniature line operated, regulated power supplies are ideal for applications where space is at a premium, and yet power supply performance cannot be compromised. The two models offered in this series have outputs of 5VDC at 350mA and \pm 15VDC at \pm 60mA. Performance specifications include voltage accuracy of \pm 1%, temperature coefficient of .005%/°C, and isolation resistance of 100 megohms with only 100pF capacitive coupling.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: $115VAC \pm 10\% @ 60Hz$. J version: $100VAC \pm 10\% @ 50-60Hz$.

There is no extra charge for the J version. When ordering add J suffix after the model number.



SPECIFICATIONS. 25°C	UPM-5/350	BPM-15/60A	
Output Voltage	5VDC	±15VDC	
Output Voltage Accuracy	±1%	±1%	
Rated Output Current	350mA	±60mA	
Line Regulation, max.	.05%	.05%	
Load Regulation, max.	0.2%	.05%	
Temperature Coefficient, max.	.005%/°C	.005%/°C	
Output Ripple, RMS max.	2mV	1mV	
Output Impedance, max.	.005 ohm	0.15 ohm	
Transient Recovery Time, max.	50µsec.	50µsec.	
Isolation Resistance, min.	100 Meg.	100 Meg.	
Isolation Capacitance, max.	100pF	100pF	
Breakdown Voltage, min.	300VAC	300VAC	
Operating Temp. Range	-25°C to +71°C	(No Derating)	
Storage Temp. Range	-55°C to +85°C		
Case Material	Diallyl Phthalate	Diallyl Phthalate	
Module Size, inches	2x2x.432	-2x2x.432	
Module Size, millimeters	50,8×50,8×11,0	50,8x50,8x11,0	
Module Weight	2.5 oz. (71g.)	2.5 oz. (71g.)	
Case/Pin Configuration	G1	G1	
Other Versions	J	J	
Mating Socket	DILS-1, DILS-2	DILS-1, DILS-2	
Price	\$69.00	\$69.00	

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Vol 3/170

HighVoltageModules

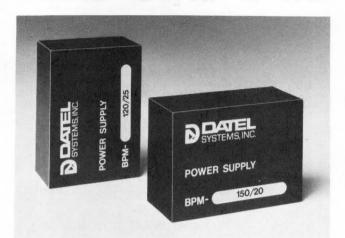
This series of dual high voltage supplies is specially designed for use with high voltage operational amplifiers such as Datel Systems AM-300 series. The 3 supplies in this series offer output voltages of ± 120 , ± 150 , and ± 180 volts with excellent regulation, stability, and low output ripple.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: 115VAC ±10% @60 Hz

E version: 220VAC $\pm 10\%$ @ 50-60 Hz J version: 100VAC $\pm 10\%$ @ 50-60 Hz

Mating MS-7 sockets are \$3.50 each



	NEW	NEW	NEW
SPECIFICATIONS. 25°C	BPM-120/25	BPM-150/20	BPM-180/16
Output Voltage	±120VDC	±150VDC	±180VDC
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current	25mA	20mA	16mA
Line Regulation, max.	.05%	.05%	.05%
Load Regulation, max.	0.1%	0.1%	0.1%
Temperature Coefficient, max.	.02%/°C	.02%/°C	.02%/°C
Output Ripple, RMS max.	10mV	10mV	10mV
Output Impedance, max.	5 ohms	5 ohms	5 ohms
Transient Recovery Time, max.	50µsec.	50µsec.	50µsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC
Operating Temp. Range	-2	5°C to +71°C (No Derat	ing)
Storage Temp. Range	-25	5°C to +85°C	i en en en en fi
Case Material	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5x2.5x1.56	3.5x2.5x1.56	3.5x2.5x1.56
Module Size, millimeters	88,9x63,5x39,6	88,9x63,5x39,6	88,9x63,5x39,6
Module Weight	24 oz. (681g.)	24 oz. (681g.)	24 oz. (681g.)
Case/Pin Configuration	C3	C3	C3
Other Versions	E,J	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7
Price (1-9)	\$79.00	\$79.00	\$79.00

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

GOLD BOOK 76/77

See inside back cover for DATEL sales offices

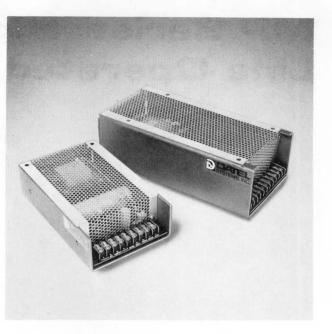
MP Series: High Power, Line Operated Supplies

MP SERIES: SUPPLIES FROM DATEL SYSTEMS ARE BETTER IN 12 WAYS

- **1.** No output derating over 0°C to 65°C operation. Twice as much power available at 65°C compared with open frame type supplies.
- **2.** No derating for 50 Hz operation. Open frame type supplies have 10% derating for 50 Hz operation.
- **3.** Overvoltalge protection on 5 volt outputs is standard. This is optional on most open frame type supplies.
- Barrier strip connector for input and output connections. Open frame type supplies require soldering connections directly to transformer and circuit board.
- **5.** Aluminum cover protects power supply circuitry. Open frame type supplies have no cover.
- High efficiency (40-50%) series regulated design. Open frame type supplies have efficiencies as low as 25%.
- **7.** Rugged, four-sided anodized aluminum chassis has 3 different mounting positions.
- 8. Output current limiting protects supplies from short circuit or overload conditions.
- **9.** Remote sensing with open lead protection is a standard feature.
- **10.** No turn-on or turn-off overshoot for protection of your circuits.
- **11.** Dual output supplies are tracking for best performance of your circuits.
- 12. Low prices start at \$38.00 for 5V at 3 amps.

CHECK THESE RELIABILITY FEATURES:

- ✓ Hermetically sealed series pass transistor with case temperature rise limited to 50°C.
- Computer grade 85°C aluminum electrolytic capacitors with conservative rating.
- ✓ Custom designed integral heat sink with conservative thermal design for cool operation.
- Layer wound, polyester impregnated transformer with integral Faraday shield.
- Single sided circuit board with wide conductor runs for best reliability.
- All heat generating components directly connected to heat sink.
- Low loss transformer and circuit technique to minimize internal power dissipation.
- \bigstar 4 hour burn-in at full load and 65°C before shipment.



GENERAL SPECIFICATIONS COMMON

TO ALL MODELS

Input Voltage	115/230VAC ±10%
Line Frequency.	50-60 Hz
Output Voltage Adjustment	±5%
Output Ripple	1mV RMS, max. 3mV P-P typ.
Transient Response	50 µsec. max.
Output Protection	Current Limiting or Foldback Limiting
Overvoltage Protection, 5V output	uts6.2V ±5%
Voltage Stability, after warmup	±0.25%, 24 hours
Dual Output Tracking	05%, 0.1% over temp. range
Operating Temperature Range.	0°C to 71°C
Storage Temperature Range	25°C to +85°C

DESCRIPTION

The MP Series high power, line operated supplies are new entries in the field of low cost, open frame type supplies. Although priced competitively with the open frame units, The MP Series offers significant advantage in performance and design features. The 16 models in this series offer popular single, dual, and triple outputs for use with data conversion devices, operational amplifiers, and other analog and digital circuits. Output power capability ranges from 15 Watts to 105 Watts and prices are from \$38 to \$149.

The unique feature of the MP Series over open frame type supplies is its conservative thermal design which results in full rated output over 0°C to 65°C ambient temperature and only 15% derating at 71°C. This results in approximately twice the output power at 65°C compared with open frame supplies. The careful attention to thermal design is evidenced by use of conservatively rated components including 85°C computer grade aluminum electrolytic capacitors, integral heat sink and chassis design, and a high efficiency linear regulator design. The power transformer is a low loss type with no derating for 50 Hz operation. It is layer wound with polyester impregnation, and incorporates a Faraday shield which is connected to chassis ground. Power supply efficiency is 50% for $\pm 12V$ and $\pm 15V$ outputs and 40% for 5V outputs.

Other significant features include output current limiting protection, .05% tracking of dual outputs, barrier strip terminal connector, ventilating protective cover, remote sensing with open lead protection, and $\pm 5\%$ output voltage adjustment by means of externally accessible trimming potentiometers. In addition, all 5V outputs have built-in overvoltage protection as a standard feature.

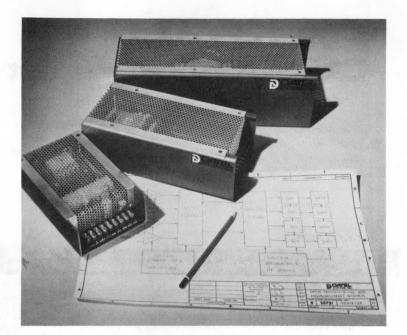
MP Series: High Power, Line Operated Supplies

MODEL	OUTPUT VOLTAGE & CURRENT (0 to 65°C)	OUTPUT I AT 71°C'	LINE REG. (MAX.) ²	LOAD REG. (MAX.) ³	TEMPCO (TYPICAL)	RIPPLE (RMS MAX.) ⁴
SINGLE OUTPUT						Acharos -
MPS-5/3	5V @ 3.0A	2.5A	0.1%	0.1%	.01%/°C	1mV
MPS-5/6	5V @ 6.0A	5.0A	0.1%	0.1%	.01%°C	1mV
MPS-5/12	5V @ 12.0A	10.0A	0.1%	0.1%	.01%°C	1mV
MPS-5/18	5V @ 18.0A	15.0A	0.1%	0.1%	.01%/°C	1mV
DUAL OUTPUT		Tanina -			1	nsie d Brspon
MPD-12/1	±12V @ 1.0A	0.85A	.05%	.05%	.01%/°C	1mV
MPD-15/1	±15V @ 1.0A	0.85A	.05%	.05%	.01%/°C	1mV
MPD-12/1.5	±12V @ 1.5A	1.25A	.05%	.05%	.01%/°C	1mV
MPD-15/1.5	±15* @1.5A	1.25A	.05%	.05%	.01%/°C	1mV
MPD-12/3	±12V @ 3.0A	2.5A	.05%	.05%	.01%/°C	1mV
MPD-15/3	±15V @ 3.0A	2.5A	.05%	.05%	.01%/°C	1mV
TRIPLE OUTPUT						
MPT-12/1-5/3	±12V @ 1A /5V @ 3A	0.85/2.5A	.05/0.1%	.05/0.1%	.01%/°C	1mV
MPT-15/1-5/3	±15V @ 1A /5V @ 3A	0.85/2.5A	.05/0.1%	.05/0.1%	.01%/°C	1mV
MPT-12/1.5-5/6	±12V @ 1.5A /5V @ 6A	1.25/5.0A	.05/0.1%	.05/0.1%	.01%/°C	1mV
MPT-15/1.5-5/6	±15V @ 1.5A /5V @ 6A	1.25/5.0A	.05/0.1%	.05/0.1%	.01%/°C	1mV
MPT-12/1.5-5/12	±12V @ 1.5A /5V @ 12A	1.25/10.0A	.05/0.1%	.05/0.1%	.01%/°C	1mV
MPT-15/1.5-5/12	±15V @ 1.5V/5V @ 12A	1.25/10.0A	.05/0.1%	.05/0.1%	.01%/°C	1mV

2. For $\pm 10\%$ line change.

Typically 3mV peak to peak.

Vol 3/174



EFFICIENCY (NOM. LINE)			OVER-VOLT. PROTECTION	CASE SIZE (HXWXL, INCHES/CM)	WEIGHT (LBS./KG)	PRICE (1-9)	
40%		YES	YES	2.0X4.6X7.6 / 50,8X116,8X193,0	3.6/1,6	\$ 38.00	
40%	-	YES	YES	4.9X5.3X10.3 / 12,4X13,5X26,2	6.5/2,9	\$ 56.00	
40%	_	YES	YES	4.9X5.3X11.9 / 12,4X13,5X30,2	10.4/4,7	\$ 88.00	
40%	-	YES	YES	4.9X5.3X11.9 / 12,4X13,5X30,2	14.0/6,3	\$ 99.00	
50%	.05%	YES NO		2.5X4.9X10.0 / 6,4X12,4X25,4	5.0/2,3	\$ 54.00	
50%	.05%	YES	NO	2.5X4.9X10.0 / 6,4X12,4X25,4	5.0/2,3	\$ 54.00	
50%	.05%	YES	NO	3.7X5.3X10.3 / 9,4X13,5X26,2	6.5/2,9	\$ 65.00	
50%	.05%	YES	NO	3.7X5.3X10.3 / 9,4X13,5X26,2	6.5/2,9	\$ 65.00	
50%	.05%	YES	NO	4.9X5.3X10.3 / 12,4X13,5X26,2	10.5/4,8	\$ 95.00	
50%	.05%	YES	NO	4.9X5.3X10.3 / 12,4X13,5X26,2	10.5/4,8	\$ 95.00	
45%	.05%	5V ONLY	5V ONLY	3.4X4.9X11.0 / 8,6X12,4X27,9	11.0/5,0	\$ 85.00	
45%	.05%	5V ONLY	5V ONLY	3.4X4.9X11.0 / 8,6X12,4X27,9	11.0/5,0	\$ 85.00	
45%	.05%	5V ONLY	5V ONLY	4.9X5.3X14.0 / 12,4X13,5X35,6	14.0/6,3	\$116.00	
45%	.05%	5V ONLY	5V ONLY	4.9X5.3X14.0 / 12,4X13,5X35,6	14.0/6,3	\$116.00	
45%	.05%	5V ONLY	5V ONLY	4.9X5.3X15.6 / 12,4X13,5X39,6	17.0/7,7	\$149.00	
45%	.05%	5V ONLY	5V ONLY	4.9X5.3X15.6 / 12,4X13,5X39.6	17.0/7,7	\$149.00	

1and 3 Watt DC-DC Converters

1 WATT SERIES

and the second se	OUTPUT OLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD	FULL LOAD	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/200-D1	2 + 5	V 200m	A 12VD0	c ±10%	40mA	170mA	50%	.05%
UPM-5/200-D2	8 + 5	V 200m	A 28VD0	c ±10%	10mA	75mA	50%	.05%
UPM-12/80-D5	+12	V 80m/	A 5VDC	±10%	85mA	360mA	53%	.05%
UPM-12/80-D2	8 +12	2V 80m/	4 28VD0	c ±10%	15mA	62mA	55%	.05%
UPM-24/40-D5	+24	V 40m/	A 5VDC	±10%	95mA	350mA	55%	.05%
UPM-24/40-D1	2 +24	V 40m/	A 12VD0	±10%	40mA	145mA	55%	.05%
UPM-28/25-D5	+28	3V 25m/	A 5VDC	±10%	95mA	250mA	55%	.05%
UPM-28/25-D1	2 +28	3V 25m/	A 12VD0	c ±10%	40mA	105mA	55%	.05%
BPM-12/25-D5	±12	2V 25m	A 5VDC	±10%	95mA	210mA	58%	.05%
BPM-12/25-D1	2 ±12	2V 25m	A 12VD0	c ±10%	40mA	85mA	60%	.05%
BPM-12/25-D2	8 ±12	25m/	A 28VD0	c ±10%	15mA	36mA	60%	.05%
BPM-15/25-D5	±15	V 25m/	A 5VDC	±10%	95mA	260mA	58%	.05%
BPM-15/25-D1	2 ±15	V 25m	A 12VD0	±10%	40mA	105mA	60%	.05%
BPM-15/25-D2	8 ±15	5V 25m	A 28VD0	c ±10%	15mA	45mA	60%	.05%
BPM-18/25-D5	±18	3V 25m/	A 5VDC	c ±10%	95mA	310mA	58%	.05%
BPM-18/25-D1	2 ±18	3V 25m/	A 12VD0	c ±10%	40mA	125mA	60%	.05%
BPM-18/25-D2	8 ±18	3V 25m/	A 28VD0	c ±10%	15mA	55mA	60%	.05%

3 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT- AGE TOLER.	NO LOAD	FULL LOAD	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/500-D5	+5V	500mA	5VDC	±10%	240mA	1100mA	45%	.05%
UPM-5/500-D12	+5V	500mA	12VDC	±10%	90mA	430mA	48%	.05%
UPM-5/500-D28	+5V	500mA	28VDC	±10%	32mA	180mA	50%	.05%
UPM-12/250-D5	+12V	250mA	5VDC	±10%	240mA	1100mA	55%	.05%
UPM-12/250-D28	+12V	250mA	28VDC	±10%	30mA	195mA	55%	.05%
UPM-24/125-D5	+24V	125mA	5VDC	±10%	240mA	1100mA	55%	.05%
UPM-24/125-D12	+24V	125mA	12VDC	±10%	75mA	450mA	55%	.05%
UPM-28/100-D5	+28V	100mA	5VDC	±10%	200mA	1000mA	55%	.05%
UPM-28/100-D12	+28V	100mA	12VDC	±10%	75mA	420mA	55%	.05%
BPM-12/100-D5	±12V	100mA	5VDC	±10%	190mA	900mA	53%	.05%
BPM-12/100-D12	±12V	100mA	12VDC	±10%	75mA	410mA	50%	.05%
BPM-12/100-D28	±12V	100mA	28VDC	±10%	30mA	156mA	55%	.05%
BPM-15/100-D5	±15V	100mA	5VDC	±10%	240mA	1100mA	53%	.05%
BPM-15/100-D12	±15V	100mA	12VDC	±10%	85mA	470mA	53%	.05%
BPM-15/100-D28	±15V	100mA	28VDC	±10%	30mA	195mA	55%	.05%
BPM-18/100-D5	±18V	100mA	5VDC	±10%	200mA	1360mA	53%	.05%
BPM-18/100-D12	±18V	100mA	12VDC	±10%	75mA	545mA	55%	.05%
BPM-18/100-D28	±18V	100mA	28VDC	±10%	30mA	235mA	55%	.05%

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461



LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.07Ω	F	\$42.00
0.1%	.02%/°C	.07Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$42.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00
.05%	.02%/°C	0.2Ω	F	\$49.00

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.07Ω	G1	\$64.00
0.1%	.02%/°C	.07Ω	G1	\$64.00
0.1%	.02%/°C	.07Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$64.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00
.05%	.02%/°C	0.2Ω	G1	\$69.00

DESCRIPTION

This broad line of DC-DC converters features 17 one watt models and 18 three watt models with single and dual output voltages. Input voltages are 5. 12, and 28V with single outputs of 5. 12, 24, and 28V, and dual outputs of ± 12 , ± 15 , and $\pm 18V$. Output voltage accuracies are $\pm 1\%$ with .02%/°C temperature coefficient. Other features include low output ripple. 100 megohm isolation, grounded internal copper shield, and output current limiting.

GENERAL SPECIFICATIONS - ALL MODELS

Output Voltage Accuracy Output Noise and Ripple, max. Back Ripple Current, max. Capacitive Coupling, max. Breakdown Voltage, min. Transient Recovery Time, max. Operating Temp. Range Storage Temp. Range Internal Shield Case Material

 \pm 1% 20mV P-P (2mV RMS) 1% of lin 250 pF 300VDC 50 μ sec. -25°C to +71°C -55°C to +85°C Copper, connected to common Diallyl Phthalate

 MODULE SIZES

 F Case:
 1.5X2.0X0.375 inches 38,1X50,8X9,5 mm

 Weight:
 1.5 oz. (43g.)

 G1 Case:
 2.0X2.0X0.432 inches 50,8X50,8X11,0 mm

 Weight:
 2.5 oz. (71g.)

Both 1 and 3 watt series use 2 DILS-1 or DILS-2 terminal strips (at \$5.00/pair) for sockets.

5 and 10 Watt DC-DC Converters

5 WATT SERIES

MODEL	OUTP VOLTA		UT INPUT NT VOLTAGE	INPUT VOLT- AGE TOLER.	NO LOAD	FULL LOAD ENT INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/1000-D12	+5V	1000mA	12VDC	±10%	88mA	776mA	54%	.05%
UPM-5/1000-D28	+5V	1000mA	28VDC	±10%	45mA	300mA	60%	.05%
UPM-12/420-D5	+12V	420mA	5VDC	±10%	300mA	1800mA	56%	.05%
UPM-12/420-D28	+12V	420mA	28VDC	±10%	40mA	270mA	67%	.05%
UPM-24/210-D5	+24V	210mA	5VDC	±10%	300mA	1800mA	56%	.05%
UPM-24/210-D12	+24V	210mA	12VDC	±10%	80mA	760mA	55%	.05%
UPM-28/180-D5	+28V	180mA	5VDC	±10%	300mA	1800mA	56%	.05%
UPM-28/180-D12	+28V	180mA	12VDC	±10%	80mA	760mA	55%	.05%
BPM-12/210-D5	±12V	210mA	5VDC	±10%	330mA	1800mA	56%	.05%
BPM-12/210-D12	±12V	210mA	12VDC	±10%	110mA	660mA	64%	.05%
BPM-12/210-D28	±12V	210mA	28VDC	±10%	43mA	278mA	65%	.05%
BPM-15/165-D5	±15V	165mA	5VDC	±10%	370mA	1750mA	56%	.05%
BPM-15/165-D12	±15V	165mA	12VDC	±10%	110mA	660mA	63%	.05%
BPM-15/165-D28	±15V	165mA	28VDC	±10%	43mA	278mA	64%	.05%
BPM-18/140-D5	±18V	140mA	5VDC	±10%	370mA	1750mA	58%	.05%
BPM-18/140-D12	±18V	140mA	12VDC	±10%	110mA	660mA	64%	.05%
BPM-18/140-D28	±18V	140mA	28VDC	±10%	43mA	278mA	65%	.05%

10 WATT SERIES

MODEL	OUT VOLT	PUT OUTP		INPUT VOLT- AGE TOLER.	NO LOAD	FULL LOAD	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/2000-D12	+5V	2000mA	12VDC	±10%	105mA	1700mA	49%	.05%
UPM-5/2000-D28	+5V	2000mA	28VDC	±10%	38mA	550mA	65%	.05%
UPM-12/840-D5	+12V	840mA	5VDC	±10%	400mA	3680mA	55%	.05%
UPM-12/840-D28	+12V	840mA	28VDC	±10%	38mA	550mA	65%	.05%
UPM-24/420-D5	+24V	420mA	5VDC	±10%	400mA	3400mA	59%	.05%
UPM-24/420-D12	+24V	420mA	12VDC	±10%	118mA	1230mA	68%	.05%
UPM-28/360-D5	+28V	360mA	5VDC	±10%	400mA	3400mA	59%	.05%
UPM-28/360-D12	+28V	360mA	12VDC	±10%	118mA	1230mA	68%	.05%
BPM-12/420-D5	±12V	420mA	5VDC	±10%	600mA	3600mA	56%	.05%
BPM-12/420-D12	±12V	420mA	12VDC	±10%	150mA	1410mA	60%	.05%
BPM-12/420-D28	±12V	420mA	28VDC	±10%	56mA	613mA	59%	.05%
BPM-15/330-D5	±15V	330mA	5VDC	±10%	600mA	3600mA	55%	.05%
BPM-15/330-D12	±15V	330mA	12VDC	±10%	150mA	1410mA	59%	.05%
BPM-15/330-D28	±15V	330mA	28VDC	±10%	56mA	613mA	58%	.05%
BPM-18/280-D5	±18V	280mA	5VDC	±10%	600mA	3600mA	56%	.05%
BPM-18/280-D12	±18V	280mA	12VDC	±10%	150mA	1410mA	60%	.05%
BPM-18/280-D28	±18V	280mA	28VDC	±10%	56mA	613mA	59%	.05%

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

	DEATEL SYSTEMS,INC
DETEL	DC/DC CONVERTER
DC/DC CONVERTER	BPM- 15/330-D28
UPM- 5/1000-D12	UZB CON

DESCRIPTION

This comprehensive line of higher power DC-DC converters features 34 different models with both single and dual outputs. Input voltages are 5, 12, and 28V with single output voltages of 5, 12, 24, and 28 volts, and dual outputs of ± 12 , ± 15 , and ± 18 volts. Output voltage accuracies are ±1% with .02%/°C temperature coefficients. Other features include low output ripple, 100 megohm isolation, grounded internal copper shield, and output current limiting protection.

GENERAL SPECIFICATIONS - ALL MODELS

dentenae of conformotion	ALL MODELO
Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20mV P-P (2mV RMS)
Back Ripple Current, max.	1% of lin
Capacitive Coupling, max.	250 pF
Breakdown Voltage, min.	300VDC
Transient Recovery Time, max.	50µsec.
Operating Temp. Range	-25°C to +71°C
Storage Temp. Range	-55°C to +85°C
Internal Shield	Copper, connected to common
Case Material	Diallyl Phthalate (G2)
	Phenolic (CB)
MODULE SIZES	
G2 Size:	2.0X2.0X.750 inches
	50,8X50,8X19,1mm
Weight	4.5 oz. (128g.)

4.5 oz. (128g.) 3.5X2.5X.875 inches 88,9X63,5X22,2 mm

14 oz. (397g.)

The 5 watt series use 2 DILS-1 or DILS-2 terminal strips (at \$5.00/pair) for sockets. The 10 watt series use the MS-7 socket at \$3.50 each.



CB Size:

Weight

1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

1	G LINE	100	-
100	NI	EIA	
	IN	EVV	1

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.005Ω	G2	\$69.00
0.1%	.02%/°C	.005Ω	G2	\$69.00
.05%	.02%/°C	.015Ω	G2	\$69.00
.05%	.02%/°C	.15Ω	G2	\$69.00
.05%	.02%/°C	.03Ω	G2	\$69.00
.05%	.02%/°C	.03Ω	G2	\$69.00
.05%	.02%/°C	.035Ω	G2	\$69.00
.05%	.02%/°C	.035Ω	G2	\$69.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00
.05%	.02%/°C	.03Ω	G2	\$75.00

NEW

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.005Ω	СВ	\$89.00
0.1%	.02%/°C	.005Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$89.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00
.05%	.02%/°C	.02Ω	СВ	\$94.00

4.5 Watt DC-DC Converters

These miniature, aluminum cased DC-DC converters are ideal for applications where mounting space is tight, yet highly regulated ±15VDC is required at up to 150mA output current. Specifications include voltage accuracy of $\pm 1\%$, line regulation of .05% max., load regulation of .05% max., and tempco of .005%/°C. For convenient heat sinking, two 2-56 studs are provided on the bottom of the case. All models have output current limiting protection.

OTHER SPECIFICATIONS

Isolation Resistance, min. 100 Meg. Isolation Capacitance, max. 100 pF Breakdown Voltage, min. 300VDC Operating Temp. Range -25° to +71°C Storage Temp. Range -55°C to +85°C

MS-6 sockets are \$3.50 each.



NEW

SPECIFICATIONS, 25°C BPM-15/150-D5 BPM-15/150-D24 BPM-15/150-D28 ±15VDC ±15VDC ±15VDC **Output Voltage Output Voltage Accuracy** ±1% ±1% $\pm 1\%$ Rated Output Current¹ ±150mA ±150mA ±150mA 24VDC Input Voltage 5VDC 28VDC **Input Voltage Tolerance** ±.25V ±3.5V $\pm 4V$ Maximum Input Current 1.75A 0.35A 0.3A Efficiency, full load 54% 54% 51% Line Regulation, max. 05% .05% .05% Load Regulation, max. 05% .05% .05% .005%/°C .005%/°C .005%/°C Temperature Coefficient, max. Output Ripple RMS max. 1mV 1mV 1mV Output Impedance, max. 05Ω .05Ω .05Ω Transient Recovery Time, max. 50µsec. 50µsec 50µsec. **Case Material** Aluminum Aluminum Aluminum 2.0X2.0X0.4 2.0X2.0X0.4 2.0X2.0X0.4 Module Size, inches Module Size, millimeters 50,8X50,8X10,2 50,8X50,8X10,2 50.8X50.8X10.2 **Module Weight** 3.0 oz.(85g) 3.0 oz.(85g) 3.0 oz.(85g) **Case/Pin Configuration** B В В MS-6 MS-6 **Mating Socket** MS-6 \$79.00 \$79.00 \$79.00 Price (1-9) NOTE:

THESE POWER SUPPLIES ARE **COVERED BY GSA CONTRACT**

1. Above 35°C (95°F) mounting surface temperature, derate 1.3mA/°C.

Model 1200: µC Supply

Model 1200 microcomputer supply is a DC-DC converter designed to operate from a 5 volt logic supply to power a CPU and 4K of memory. The output voltages of +12, -5, and -9V in conjunction with the 5V input will power an 8080 CPU and four 2107A RAM's or four 1702A ROM'S. This supply operates with a full load efficiency of 58% and has output current limiting protection.

Operating temperature range is -25° C to $+71^{\circ}$ C and storage temperature range is -55° C to $+85^{\circ}$ C.

Mating sockets, 2 DILS-1 or DILS-2 terminal strips, are \$5.00 per pair.



SPECIFICATIONS, 25°C **MODEL 1200** Outputs +12VDC @ 160mA -9VDC @ 300mA -5VDC @ 2mA **Output Voltage Accuracy** ±1% (+12V & -9V), ±5% (-5V) 5VDC ±0.25V Input Voltage Input Current, no load 0.3 Amp. Input Current, full load 1.6 Amp. Efficiency, full load 58% Line Regulation, max., all outputs .05% Load Regulation, max., +12V out 05% Load Regulation, max., -9V out 0.1% Load Regulation, max., -5V out 1.0% Temperature Coefficient, max. 02%/°C Output Ripple, RMS max. 1mV Transient Recovery Time, max. 25µsec. **Case Material Diallyl Phthalate** Module Size, inches 2.0X2.0X0.75 Module Size, millimeters 50,8X50,8X19,1 **Module Weight** 4.5 oz.(128g) Case/Pin Configuration K DILS-1, DILS-2 **Mating Socket** Price (1-9) \$89.00

THIS POWER SUPPLY IS COVERED BY GSA CONTRACT

DATEL		NEL METER SHORT	
DATEL MODEL ►	DM-350 3-1/2 Digits .43" H Displays AC or +5 VDC Portable Display Only	DM-3000 3 digit, 0 to +1V Input DPM/Counter .43"H Displays +5V Power, \$99	DM-2100 3-1/2 digits ±200mV, ±2V Differential Input, +5V Power, \$129
P. P. P. 2000	PHYSICAL Case Size Case Material Front Panel Cutout & f Temperature Ranges Operating	57,2 mm) Black Polycarbonate plastic. In Chemical resistant.	mpact and « 77,8 mm)
ANALOG INPUT Configuration Range, Full Scale CMR CMV Bias Current Impedance	Specifications (typical at +25° C unless Single Ended, Unipolar or Bipolar 0 to +1.999V or ±1.999V 70 db @ DC (AC Models Only) ±300 VDC (AC Models Only) 45nA typ, 500 nA Max. 100 Megohms, Min.	noted) Single-ended unipolar 0 to +999mV, (+9.99, +99.9V opt) NA (unipolar) NA (unipolar) 100nA typ, 250nA max 100 Megohms, min (1V),,1mΩ(10,100V)	Differential Bipolar ±199.9mV or ±1.999V 70dB, DC to 60Hz (See ordering ±2V to logic gnd. guide) 20nA 100 Megohms, min
PERFORMANCE Accuracy Temp Drift Sample Rate LED Digit Height BCD Outputs Power Supply	Adj. to ±0.05% of F.S. ±1 Digit ±100ppm FS/ ⁹ C typ. 2 Samples Per Sec, Adj. 0.43" (11 mm) NONE AC Line or +5 VDC, 300 mA Max.	Adj. to ±0,1% of Reading ±1 digit ±100ppm FS/° C max 0 to 250 Samples per Sec 0.43'' (11 mm) Full parallel Std. +5VDC, 800 mA max	Adj. to ±0.05% of Reading ±1 digit ±50ppm FS/° C max 0 to 200 Samples per Sec 0.30" (7,6 mm) Full parallel Std. +5VDC, 650mA max
NOTES	Low Cost for Display Only Applications	DM-3000 has count and reset inputs and optional crystal clock so that it can be configured as a 10Mz counter, frequency meter, tachometer or 4- wire slave display.	DM-2100 has true differential bipolar inputs and choice of $\pm 200 \text{mV}$ or $\pm 2 \text{V}$ input ranges.
ORDERING GUIDE Datel's products are available both direct and through GSA. If you are connected with a military or federal agency or receive federal funds, you may be entitled to purchase Datel's Digital Panel Meters and other prod- ucts through the General Services Administration. Datel's DPM's are approved under FSC Group 66-17, Part II, GSA Contract No. GS-00S- 27959. Contact Datel for assistance.	DM-350 POWER SUPPLY D=5VDC A=115 or 230 VAC (User-selected on rear connector) INPUT POLARITY 1= Unipolar 0 to +1.999V 2= Bipolar -1.999V to +1.999V	DM-3000 500 KHz Clock R=Ceramic Resonator X=Quartz Crystal Input Range and Resistance 1=0 to +999m V 100MΩ impedance 2=0 to +99.9V 100KΩ impedance 3=0 to +99.9V 100KΩ impedance	DM-2100 Input Range A=±199.9mV B=±1.999V Another version of the DM-2100 (model DM-1100) has special options available (optoisolation, low input bias, input filter, etc.) Contact Datel for details.
PRICES (1-9 quantity) (contact Datel for quantity discounts and Interna- tional prices and GSA orders)	DM-350D1 (5V, unipolar) \$69 DM-350D2 (5V, bipolar) \$75 DM-350A1 (AC, unipolar) \$79 DM-350A2 (AC, bipolar) \$89	DM-3000RI \$99 for 10V or 100V inputs add \$10 for crystal clock add \$10	DM2100A\$129 DM2100B\$129
DPM CONNECTORS (not included with DPM). Dual 18-pin, PC-type	2335-1 (Solder Tab)\$4.95 2335-2 (Wire Wrap)\$4.95	2335-1 (solder tab) \$4.95 2335-2 (wire wrap) \$4.95	2335-1 (solder tab) \$4.95 2335-2 (wire wrap) \$4.95
Suggested +5VDC POWER SUPPLY (not included with DPM) See Pg. 4	Not Required On AC Powered Versions	UPM-5/1000B Power Supply \$49.00 MS-7 Power Supply Socket \$3.50	UPM-5/1000B Power Supply \$49.00 MS-7 Power Supply Socket \$3.50
FOR FURTHER INFORMATION	SEE PAGE 184	SEE PAGE 186	SEE PAGE 191

DIGITAL PANEL METER SHORT FORM GUIDE SPECIFICATIONS • COVERED BY GSA CONTRACT

DM-2000AR

DM-2115



DM-4300

DM-2115	DM-2000AR	DM-4000	DM-4300
3-1/2 digits .43"H Displays	3-1/2 digit Autoranging ±200mV,	4-1/2 digit, ±2V Input Autozeroed	4-3/4 digit, ±4V Input Autozeroed
AC or +5V portable Differential, \$159	2V, 20V Input Ranges, \$169	Optoisolated Ratiometric, \$219	Optoisolated Ratiometric \$235
All panel meters have the following controls a Internal Start Clock Internal TTL s samples per sec External Start Adjust External adjust (not included D Internal Start Gate Provides extern start clock, or f BCD Data Outputs Full parallel t valid when the all models exce	tart clock trigger pulse, initially set at two ond	Overflow Overflow output indic EOC EOC End of Conversion is complete and BCD of Automatically indicat ong appropriate rear I automatically lights ti Input/Output Connector Displays Output States of All digits are red LE	(Status or Busy) indicates when conversion butput data is valid. es polarity of input (except unipolar DM-3000).
Differential Bipolar	Single-ended Bipolar floating (opt)	Differential Bipolar floating	Differential Bipolar floating
0 to ±1.999 Volts	0 to ±199.9mV, ±1.999V, ±19.99V	0 to ±1.9999 Volts	0 to ±3.9999 Volts
70dB, DC to 60Hz	70 dB, DC to 60Hz (optional)	120dB, DC to 60Hz	120dB, DC to 60Hz
±3V to logic gnd.	±100V to logic gnd (optional)	±300V to logic gnd	±300V to logic gnd
3nA typ, 2nA max	2nA	100pA max	100pA max
100 Megohms, min	1 Megohm to summing junction	100 Megohms, min	100 Megohms, min
Adj. to ±0.05% of Reading ±1 digit	Adj. to ±0.1% of Full Scale ±1 digit	Adj. to ±0.01% of Reading ±1 digit	Adj. to ±0.01% of Reading ±1 digit
±50ppm FS/°C max	±100ppm FS/° C max	±15ppm/° C of Reading max	±15ppm/°C of Reading, max
0 to 40 Samples per Sec	0 to 30 samples per Sec	0 to 5 samples per Sec	0 to 3.3 samples per Sec
0.43'' (11 mm)	0.30'' (7,6 mm)	0.43" (11 mm)	0.30'' (7,6 mm)
Full parallel optional	Full parallel Std.	Full parallel optional	Full parallel optional
AC line or +5VDC, 400mA max	+5VDC, 800m A max	+5VDC, 600mA max	+5VDC, 600mA max
DM-2115 may be operated AC or portable with +5VDC, 400mA max power. With blanked display, current drops to 120mA, ideal for "press to read" instruments.	DM-2000AR is a 3-decade autorang- ing DPM which automatically switches ranges and decimal point over ±0.2V, ±2V, and ±20V Full Scale.	DM-4000 features optoisolated in- puts, crystal oscillator counter for 60dB NMR AC line noise rejection and autozeroing to eliminate residual offset errors. DM-4000 includes a 3- wire ratiometric input.	DM-4300 features optoisolated in- puts, crystal oscillator counter for 60dB NMR AC line noise rejection and autozeroing to eliminate residual offset errors. DM-4300 includes a 3- wire ratiometric input.
DM-2115 Power Supply A=115VAC E=230VAC J=100VAC D=+5VDC (AC, 47 to 440Hz) Full Parallel BCD Output 1=without 2=with	DM-2000AR Add suffix -2 for optoisolated differential input (DM-2000AR less optoisolation has a single-ended input to logic ground)	DM-4000 Parallel TT L BCD Output A=without B=with Synch. to AC line frequency of 5=50Hz 6=60Hz	DM-4300 Parallel TTL BCD Output A=without B=with Synch. to AC line frequency of 5=50Hz 6=60Hz
DM-2115 +5V, no BCD \$129 DM-2115 +5V, with BCD \$145 DM-2115 AC, no BCD \$159 DM-2115 AC, with BCD \$175	DM-2000AR no optoisolation \$169 DM-2000AR-2 with optoisolation \$218	DM-4000A without BCD \$219 DM-4000B with BCD \$239	DM-4300A without BCD \$235 DM-4300B with BCD \$255
2335-3 (solder tab) \$4.95	2335-1 (solder tab) \$4.95	2335-1 (solder tab) \$4.95	2335-1 (solder tab) \$4.95
2335-4 (wire wrap) \$4.95	2335-2 (wire wrap) \$4.95	2335-2 (wire wrap) \$4.95	2335-2 (wire wrap) \$4.95
Not required DM-2115 includes In-	UPM-5/1000B Power Supply \$49.00	UPM-5/1000B Power Supply \$49.00	UPM-5/1000B Power Supply \$49.00
ternal AC Power Supply	MS-7 Power Supply Socket \$3.50	MS-7 Power Supply Socket \$3.50	MS-7 Power Supply Socket \$3.50
SEE PAGE 197	SEE PAGE 193	SEE PAGE 201	SEE PAGE 201



3¹/₂ DIGIT MINIATURE LOW COST DIGITAL PANEL METER

Covered by GSA Contract No. GS-OOS-27959

MODEL DM-350

FEATURES

- ▶ Large 0.43" (11 mm) LED Display
- Very Low Cost, \$69.
- Choice of Unipolar or Bipolar 1.999V Ranges
- Choice of AC or 5VDC Power Supply
- Very Low Power Consumption for Portable Instruments, 5VDC @ 300 mA max.

DESCRIPTION

Datel's model DM-350 Digital Panel Meter features very low cost but high performance in a miniature case for display-only applications. The instrument uses advanced CMOS LSI circuits for a very low overall parts count, high reliability and low internal heat rise. The large red high-efficiency LED displays measure 0.43 inches (11 mm) high for easy, noparallax viewing from comfortable working distances.

The DM-350 employs a high impedance (100 Megohms min.) single-ended input with a choice of 0 to ± 1.999 Volt or ± 1.999 Volt to ± 1.999 Volt input ranges.

The optional AC powered models are transformer-isolated, allowing operation in differential circuits not exceeding ± 300 Volts to the AC line. AC power voltages are user-selected by jumpers on the rear connector for 115 or 230 VAC, 47 to 440 Hz input. The +5VDC models require only 300 mA max. current, making them ideal for battery-operated instruments.

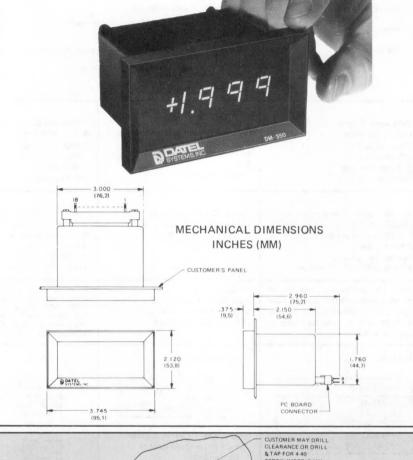
Additional application features include an automatic polarity sign for bipolar models and user-selected decimal points on the rear connector for scaling inputs. The sampling rate of 2 per second may be varied by using external resistors, and the display may be held using a rear connector input. Overscale inputs are automatically indicated with horizontal bars on the display.

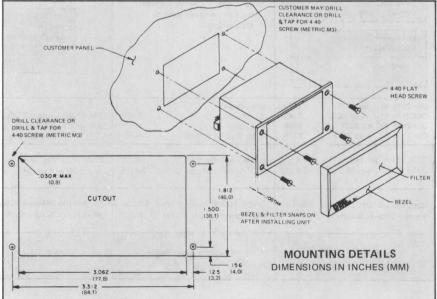
The DM-350 is housed in an impact-resistant, solvent-proof polycarbonate plastic case with four screwholes for front-panel mounting. The operating temperature range is 0 to $+50^{\circ}$ C.

Rear Connector Wiring



Pins A and B (Bottom and Top) are wired in parallel





SPECIFICATIONS (Typical @ +25°C unless noted)



Display Type Display Size Overscale Polarity Lamp Test Sampling Rate Underscale ANALOG INPUT	 3-½ digits with sign and 3 decimal points (+1.9.9.9) Red, Light Emitting Diode (LED) 0.43 inches (11 mm) high Inputs greater than 1.999V indicated by steady horizontal bars and a "one" Plus and minus sign automatically displayed on bipolar models. No sign on unipolar models. All display segments may be tested (using 888) by grounding pin 9. 2 samples per second, may be varied using ext. resistors Reads all zero's Single-ended referenced to ground and com- 	LAMP TEST Hold Display Sample Rate Adjust Decimal Points ADJUSTMENTS	the last displayed reading. 10 Kilohm load to ground. (Pin 11) Sampling rate is 2 samples per second with no connection on pin 11. Connect a 680 Kohms resistor to $\pm 5V$ for 4 samples/second. Connect a 1 μ F, 10V capacitor to ground for 1 sample/second. (Plus lead of cap to pin 11). (Pins 5, 6, and 7) Ground each pin to illuminate corresponding decimal points. Sink 20mA.
Full Scale	mon or single-ended transformer isolated (AC models) 0 to +1.999 Volts (unipolar) or -1.999 Volts to +1.999 Volts (bipolar)	Zero, Full Scale, Balance POWER SUPPLY +5VDC	Screwdriver trim pots for calibration adjust- able by removing front panel bezel and filter. (Pin 13) +5VDC power ±.25VDC @ 300 mA max. Noise and spikes must be less than
Displayed Accuracy	45nA, typical, 500nA, maximum Within 2mV of correct reading after cali- bration at steady operating temperature. (±0.05% of F.S. ±1 count) Within 10mV between 0 and +50° C	AC	50mV. Approximately 50mA may be used from pin 13 for external circuitry on AC models. Avoid errors by using a regulated sup- ply. (Pins 15 thru 18) 115 to 230 VAC, ±10%, 47
Operating Temp Range Storage Temp		PHYSICAL	to 440 Hz 5W max. required at these pins. Externally pin-strapped by the user as shown below.
Range Input Overvoltage Input Impedance Common Mode Voltage	±50V continuous maximum for no damage 100 Megohms minimum ±300VDC to AC pwr gnd (AC models only) 70dB @ DC (AC models only)	Case Size Case Material Weight Mounting	3''W X 1.75''H X 2.25''D Black polycarbonate plastic Approx. 10 oz. (280 g) AC Models Approx. 5 oz. (140 g) DC Models Panel mounted through a 1.812'' X 3.062'' cutout with 4-40 flathead screws. Dual 18-pin, PC edgeboard type 0.1'' centers, Datel #2335-1. (Viking 3VH18/IJN-5)
CALIBRATION PROC AC POWER CONNECTIONS	LOCATION OF TRIM POTS LOCATION OF TRIM POTS REMOVE FHONT PANEL BEZEL ROD FLITH BY PRIVING UP FROM BOTTOM I I I I I I I I I I I I I I I I I I I	 The instrument will have first applied, but a full BIPOLAR Models Connect pins 1 and 3 (i) Adjust the BALANCE p numerical content of the Apply +0.0005 Volts fr potentiometer until the control below the 000 instrument is calibrated recommend that the +0 volts. This will produce displays at zero. UNIPOLAR Models Apply any negative inp display 000. Apply +0.0 between 000 and 001. Apply 1-190 Volts and automatically read with Volts input. 	m a precision reference source to pin 1 and adjust the ZERO display filekers between 4000 and 4001. Rotating the ZERO reading will produce readings of 999, 998, etc. If the infrequently or operated over a wide temperature range, we 00 to 4001 change be calibrated with an input of +0.00075 a slightly "wide" zero but will preclude false 999, 998 but between −0.1 and −2V, and adjust the ZERO pot to 0005V, and adjust the BALANCE por so the display flickers d adjust the GAIN pot to display +1.900. Bipolar models will in <1 count of −1.900 if the polarity is reversed to −1.900 GGESTED EVERY 90 DAYS OR MORE OFTEN FOR
observe some simple preca cal meters in important wa 1. Input Characteristics present a negligible loa	panel meters, you'll find them easy to use if you utions. Digital Panel Meters differ from mechani- nys. These include: — DPM's have very high input impedance and d to most circuits. Because of input bias current (for amplifies in recent decimation)	that input filters giv devices and measure I external circuits to m make sure the input	or use an external multi-pole active filter. Note e delayed response time. DPM's are sampling DC or slowly-varying signals and require special easure AC or complex waveforms. If in doubt, is truly noiseless, slow DC by checking with a cope connected right at the DPM's input termi-

- . Input Characteristics DPM is have very high input impedance and present a negligible load to most circuits. Because of input bias current error, an external buffer amplifier is recommended for input source resistance of 10K Ω or greater. Always connect the signal source between ANALOG HI and ANALOG COMMON. Do not use the POWER COMMON as an analog return in order to prevent a ground loop.
- 2. AC and noise on the input terminals and power supply can cause variations in the display and possible loss of readings around zero. If this occurs, try to reduce input source noise and hum. An input filter consisting of 10K Ω from ANALOG HI to the source and 10 μF from ANALOG HI to ANALOG COMMON can be tried. Increase the capaci-

Covered by GSA Contract No. GS-00S-27959 ORDERING DM-350 -Prices (Single Quantity) DM-350D1 (5V, unipolar) DM-350D2 (5V, bipolar) DM-350A1 (AC, unipolar) DM-350A2 (AC, bipolar) \$69 GUIDE INPUT RANGE POWER SUPPLY \$75 Model Number 1 = Unipolar 0 to +1.999V \$79 D = +5VDCA = 115 or 230 VAC \$89 2 = Bipolar -1.999V to +1.999V (User-selected on Connector: Datel #2335-1, Solder Tab \$4.95 rear connector) (Viking 3VH18/1JN-5)

nals

Always use a regulated power supply for 5V-powered DPM's. A filtered

7805 or LM309K 3-terminal regulator can be used or Datel's

UPM-5/1000B supply. Current varies rapidly as digits turn off and on so

The DM-350 includes a hold display input to freeze the last reading.

Instrument manufacturers typically connect this input to a front panel pushbutton to allow an operator long enough to copy down a momen-

tarily-stabilized reading. Contact Datel if you need assistance.

that unregulated supplies cannot be used.



MULTIFUNCTION DIGITAL PANEL METER AND COUNTER DISPLAY

MODEL DM-3000

Covered by GSA Contract No. GS-00S-27959

USE AS: 3 digit DPM

- 4-wire slaved display
- 0.1% tachometer, period or frequency meter using optional crystal clock
- DC to 10 MHz general purpose counter with 0 to 999 selectable full count

FEATURES

- ▶ 3 red, 0.43" high LED displays
- Dimmable display using external variable duty cycle blanking input
- -5V, 5mA short-circuit proof output for external bipolar or differential op amps
- Built in 2 sample/second variable start clock
- Externally triggerable up to 250 conversions/second
- Selectable leading zero suppression

GENERAL DESCRIPTION

The model DM-3000 combines a low-cost unipolar digital panel meter, a DC to 10 MHz 3 digit general-purpose counter or slaved BCD digital display using only 4 lines in a single instrument. By using simple external circuits the DM-3000 3 digit DPM may be converted to a frequency meter, event counter, absolute value bipolar or differential input digital panel meter or 3-digit period measuring instrument.

The DM-3000 has a built-in short circuit proof -5V, 5 mA power supply to operate external input amplifiers or other circuitry, yet the DM-3000 is a complete 3-digit digital panel meter which includes its own internal start clock. Other operating modes include count termination at any arbitrary full scale displayed count. Many suggested circuits are shown in this brochure. A 0.02% crystal clock option may be ordered for precision period and frequency measurement.



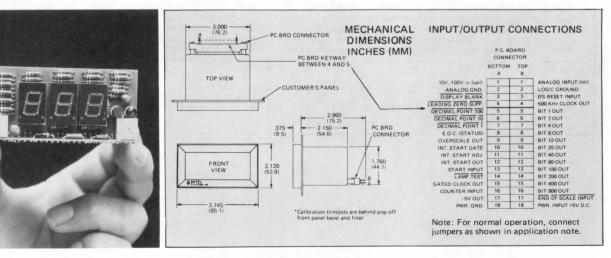
The DM-3000 accepts analog inputs from 0 to +0.999 volts, (10V and 100V ranges optional). uses a single slope conversion and displays the input on three seven-segment LED digits to an accuracy of 0.1% of reading, ±1 digit. The instrument uses conventional +5VDC TTL logic power (such as Datel's model UPM-5/1000B power supply) and consumes 800 mA (320 mA with blanked display).

The single-ended input has greater than 100 megohms input impedance and typically 100 nanoamps, bias current. The temperature coefficient is ±100 ppm/°C max. over an operating temperature range of 0 to +50°C. Storage temperature is from -20°C to +85°C. The DM-3000 can accept from 0 to 250 conversions per second from an external start pulse. A built-in start clock operates at 2 conversions/second and may be speeded up using an external resistor.

The red 7-segment LED displays are 0.43" high and each left-of-digit decimal point may be illuminated using contacts on the rear connector. Counter overflow is indicated by a blanked display and a high output on the rear connector contact

Included in the DTL/TTL compatible logic outputs are full parallel 1-2-4-8 BCD outputs for each digit, an end of conversion (busy) output and overflow. Digital inputs include the external start clock, internal start output, and gate (for hold-to-read) and a segment test input. Leading zero suppression of the 2 most significant digits can be selected as well as display blanking. Clock output and gated clock out are available with counter zero reset, and the end of scale inputs. The large number of control inputs and outputs are provided for extended system use and for custom programming.

The DM-3000 is packaged in a rugged Lexan case with overall dimensions of 3.745" W x 2.960" D x 2.120" H. The case mounts with 4 screws through a 1.812" H x 3.062" W front panel cutout identical to other Datel digital panel meters. A large degree of electrical and pin-out commonality is shared with other Datel DPM's for simple interchangeability.



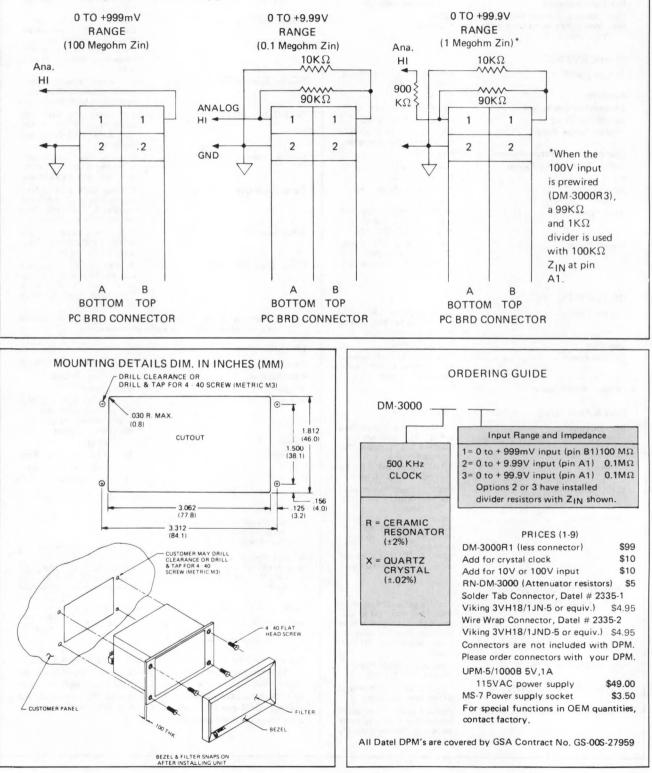
SPECIFICATIONS (Typical at 25°C unless otherwise stated)



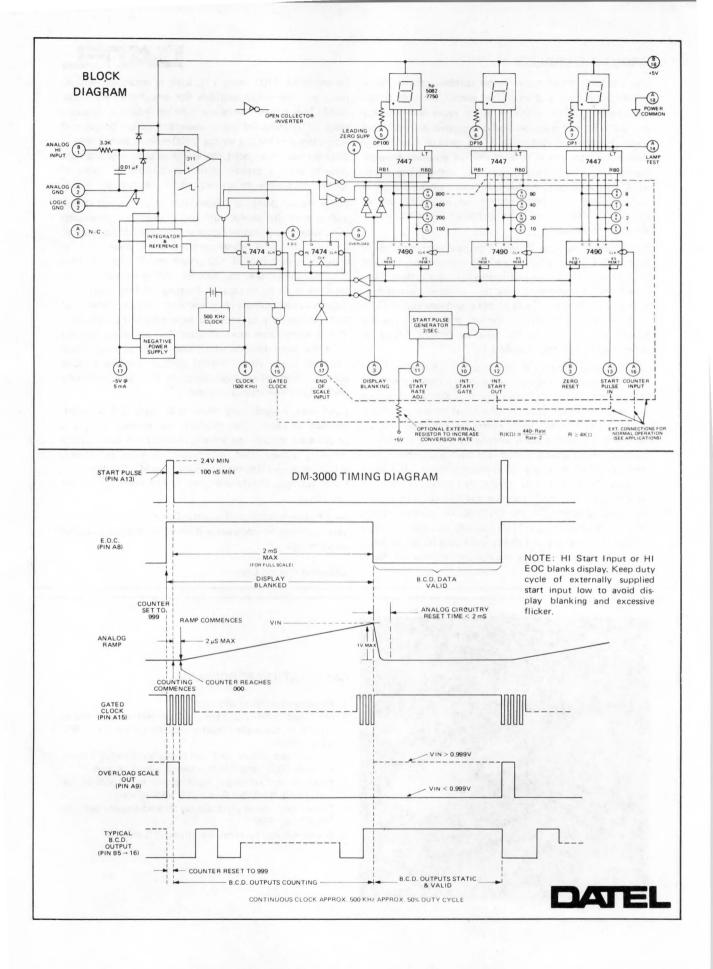
INPUTS	white do all with white	INPUT/OUTPUT CONTROL -Continued	
Input Voltage Range (Full Scale)		Lamp Test Input (A14)	Low input lights all seg- ments, 3 TTL loads,
Input Impedance	100 Megohms min. See pg.3. 100nA typ., 250nA max.	Leading Zero Suppression (A4)	
Input Configuration	±35V	Display Blanking (A3)	1 TTL load.
(5 sec. max.) PERFORMANCE	418 478		May be used for intensity modulation of display and conserving power. 1 TTL
Accuracy @ 25° C		Decimal Point Inputs (A5, 6, 7)	load.
Resolution	±1mV	AL-	nates corresponding dec- imal point. Sink 20 mA.
Conversion Speed	0-250 conversions/sec. 2/sec. adjustable upwards by	Clock Output (B4)	500 kHz ± 10 kHz 50% duty cycle. 2 TTL loads. 500 kHz ±0.02% crystal
Operating Temperature Range	external resistor. See note. 0 to +50° C	Counter Input (A16)	optional
Storage Temperature Range Warm Up Time	Essentially zero		Counting occurs on nega- tive transition. 2 TTL loads.
Adjustments	typ range) +5VDC ±5% @ 800 mA	Gated Clock Out (A15)	counts where N is displayed number. 5 TTL loads. Used
Output Power		Zeros Reset (B3)	to zero. 100 nS min. dura-
	Short circuit proof. For operation of external am- plifiers etc.	End of Scale Input (B17)	and blanks display on neg-
DISPLAY OUTPUT	5e	earns the second	ative input transition. 1 TTL load. Used to short cycle counter.
Display Type	Seven segment LED, Red 0.43" high full digits (0 to 9) and decimal points.	Note: unused inputs should be ground to avoid false readings in noisy	ed or tied to +5V as required
Overscale		PHYSICAL	
Decimal Points	Selectable at rear connec- tor. Decimal points are dis- played left of each digit.	Case Size	
Negative Analog Input		Weight	6 oz. approx.
DATA OUTPUTS - All DTL/TT			cut out. Secured with four 4-40 flathead screws. See
BCD Outputs	8-4-2-1 BCD positive true. Loading 5 TTL loads, To-	Price	mounting diagram. (1-9) \$99.00
Overscale	tem-pole. > 1000 counts indicated by high output, 5 TTL loads.	Connector	Dual 18-pin PC Brd. Edge Connector Type, 0.1" Cen- ters (not included with
End of Conversion		OPTIONS	DPM)
Logic Levels	Inputs +2V ≤ ''1'' (HI) ≤ +5.0V 0V ≤ ''0'' (LO) ≤ +0.8V	 Quartz crystal timebase 500 kHz . ±.02%. Operating temp. range drift undetectable on display. 	
	00 ≤ ''0'' (HI) ≤ +5.0V 0V ≤ ''0'' (LO) ≤ +0.4V	2. 0.1% Precision resistor atten- uator kit (RN-DM-3000) 900K, 90K, 10K for 10V and 100V	NOTE: BCD outputs are in- valid while EOC is HI.
INPUT/OUTPUT CONTROL		ranges.	valid willie EOC is Hi.
External Start Input (A13)	Positive pulse 100 nS min. transition from low to high resets register and blanks readout. Negative edge ini- tiates conversion. 10 TTL	Note: Internal start clock can be spi resistor from A11 to +5V. The resistor (Rate is in conversions/second) R≥4KΩ	value is: $R(K\Omega) \simeq \frac{440-Rate}{Rate-2}$
Internal Start Gate (A10)	loads. Low input holds last con- version. 3 TTL loads.	A recommended power supply is Dat equivalent highly regulated type. Avoid	
Internal Start Adjust (A11)	Resistor to +5V increases trigger rate. See note.	power input. Use external filtering or icant power supply spikes (> 10mV)	
Internal Start Out (A12)		readings. DPM current varies rapidly o digits displayed and sample rate.	up to 800mA depending on

INPUT RANGE SELECTION

To facilitate use of the DM-3000 for +9.99V and +99.9V ranges, a separate kit of matched, low drift input attenuator 0.1% resistors is available (part number RN-DM-3000). These resistors mount directly on the PC board connector and provide 0.1 and 1 Megohm input impedance on the +9.99V and +99.9V ranges. They are ratio matched and will track within ± 25 ppm/°C over the 0 to $\pm 50^{\circ}$ C operating range of the DM-3000. They are customer connected as shown below. Input attenuators may be ordered prewired. See ranges 2 and 3 in ordering guide below.



ATEL



Vol 3/189

ABOUT RELIABILITY

The DM3000 digital panel meter features proven mechanical construction and sound, yet simple, electrical design for a long trouble free service life of repeatable accuracy and performance. Recalibration is suggested every 90 days under variable conditions but the period after initial adjustment can safely be extended in constant environments, e.g., laboratories, offices, etc. without any significant change in performance. In cases where the panel meter is used as a digital counter for frequency, period, events, etc., front panel adjustments do not affect operation and can be ignored.

The DM3000 consists of only 2 printed circuit boards of high grade G10 epoxy-glass laminate (not phenolic) as used in military, aerospace and computer applications. The boards are permanently joined by a soldered interconnect to assure reliability. A gold plated edgeboard connector is used for all input/output connections and can be positively located and secured to the case by integral bosses. A polarizing key prevents mislocation.

The electronic circuitry is composed of high quality digital and linear integrated circuits and a small number of discrete components. Datel's extensive vendor quality assurance and incoming inspection program allows full control of reliability at the component level. Computer automated inspection, selection and grading techniques and a continuously updated vendor quality history file have established a very efficient, reliable supply of components for all Datel's products. Reliability at the component level is extended to reliability at the circuit level by the low parts count and functional simplicity of the DM3000. In addition, this is achieved in a small rugged black Lexan® case that requires a modest 3 inches of panel depth and leaves no doubt about the mechanical integrity of attachment or electrical insulation.



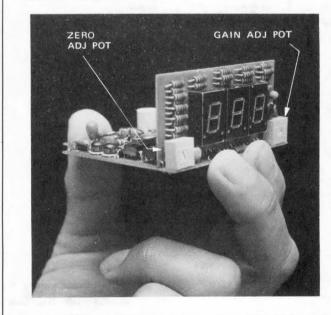
Conventional 7400 series TTL logic is employed, and all parts are commonly available for straightforward repair should it ever prove necessary. Datel maintains a complete stock of replacement parts, assembled circuit boards and repair facilities for fast service. 7400 series logic has been in common use throughout the world in computer and data systems with a proven record of billions of hours of operational experience in every conceivable circuit.

The electrical design is conservative of component ratings and is especially careful with regard to thermal characteristics which is a principal factor affecting reliable operation. Each Datel panel meter receives a 72 hour burn in comprising in excess of 100 power on/off cycles. Experience has shown that the thermal cycling inherent in this type of burn-in is best at locating "infant mortality" failures as components are stressed not only electrically but also mechanically by repeated expansion and contraction. This is many times more effective than a continuous burn in of the same duration which would only apply constant electrical stress. Also, thermal cycling provides a much closer accelerated correspondence to the most frequently encountered operational conditions.

Datel uses rugged solid state 0.43 inch L.E.D. seven segment displays. The displays are located behind a proprietary scratch and solvent resistant red filter with a diffusing surface that minimizes annoying reflections. L.E.D. displays offer exceptionally long life, freedom from lethal voltages, interference, and highly stressed interface circuitry.

As a further assurance of quality, Datel provides a full one year warranty on materials and workmanship for its digital panel meters.

®General Electric Corp.



CALIBRATION PROCEDURE

- 1. Remove front bezel and filter.
- Set input to DM-3000 from voltage reference source to +0.05% of full scale (+500 microvolts for the 0 to +.999 VFS model).
- 3. Rotate zero adjust pot until display flickers equally between "000" and "001". (±8mV typ adj. range)
- Reset voltage reference input source to 99.85% of full scale (+998.5 mV for 0 to +.999 VFS model).
- 5. Rotate gain adjust until display flickers equally between "998" and "999".
- 6. Recommended recalibration interval: 3 months.



3-1/2 DIGIT LOW COST DIGITAL PANEL METER

DM-2100 SERIES

Covered by GSA Contract No. GS-00S-27959

- ± 199.9mV or ± 1.999V Full Scale Inputs . True Floating Bipolar Differential Input
- Automatic Polarity and Overflow Display
- Up to 200 Readings per Second Using Exter-
- nal Trigge Includes 2 Samples/Second Internal Trigger Clock
- **Operates From Single +5VDC Supply** Solid State LED Display, Full parallel BCD
- outputs Adjustable Zero Control Compensating For
- External Offset Voltages Priced under \$100 in OEM quantities

DESCRIPTION

Featuring accurate, stable readings with 31/2 digit resolution, the DM-2100 digital panel meter has wide acceptance because of its proven record of performance and reliability.

The DM-2100 combines the ease and accuracy of digital readout with high input impedance and noise rejection to provide an inexpensive digital panel meter (digital voltmeter) that will enhance the operation, performance and appearance of any instrumentation system.

The DM-2100 is ideal for new equipment design or may be utilized in updating existing instruments or systems that require a stable, accurate digital readout for voltage. Simple to install, the DM-2100 is supplied complete and ready to operate requiring only a connection of an input signal and power cable. Applications include measuring of any parameter for which a suitable output voltage is available. These include absorption, acceleration, current, displacement, distortion, emission, flow, frequency, Ph, pressure, strain, torque, and many others.

The DM-2100 provides a differential input with a 100 MegOhms input impedance and a common mode rejection of 70 db at 60 Hz. The input range is ±1.999 volts or ±199.9 millivolts. The display is $3\frac{1}{2}$ digits including automatic polarity and overflow indication. In addition the output is presented to the I/O connector as BCD/TTL information.

High quality computer grade components, superior workmanship and wide-safety margin designs combine to make the DM-2100 a must in your designs.

CALIBRATION PROCEDURE

(Using Trimpots Shown At Right) The following adjustment procedure is recom-

mended after allowing for a five minute warm-up. **Balance** Control

1) Short the analog input terminals to analog common. (See I/O chart for proper pin connection)

2) Rotate the balance control until the display is flickering between (+) zero and (-) zero.

Zero Control

1) Connect a precision voltage reference source to the analog input terminals.

2) Adjust the voltage output from the reference source to .3LSD (30 μ V Model A, 300µV Model B). Rotate the zero control until the LSD (Least significant digit) flickers between zero and one.

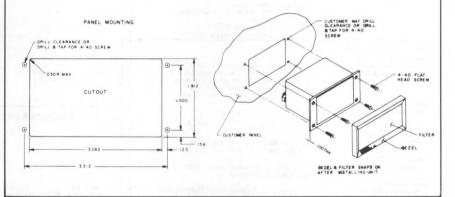
Full Scale Control

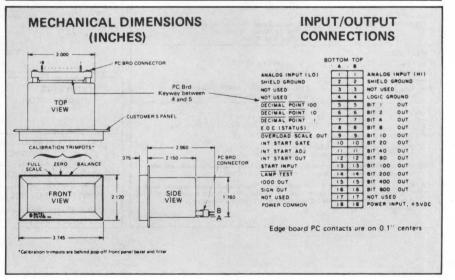
1) Adjust the output from the reference source to 1.990 volts. Rotate the full scale control of the panel meter until the meter displays 1.990 volts. Recalibration is suggested every 90 days or more often for variable conditions.

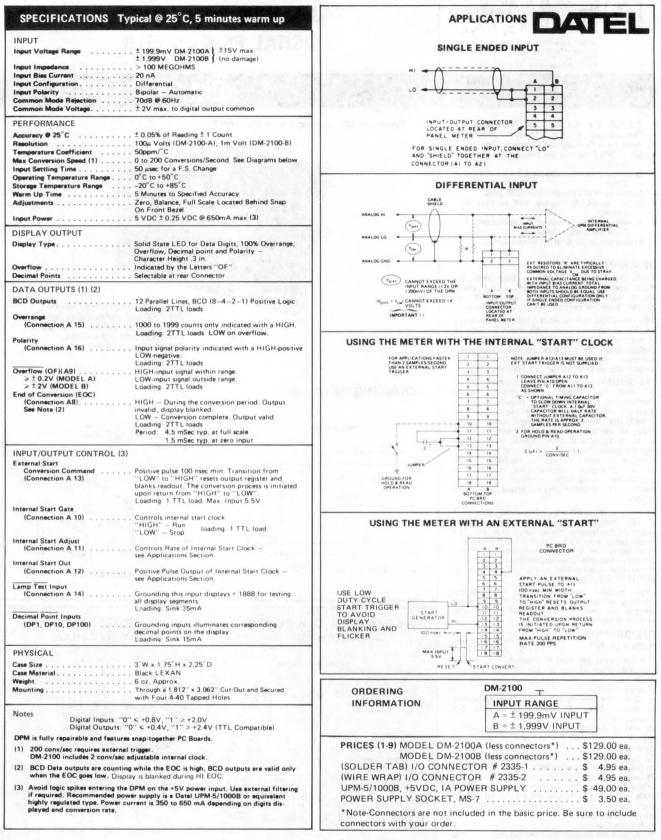


Note: The DM-2100 replaces the DM-2000 and is identical except for external timing capacitor wiring and conversion rate and displays. DM-2000 is available by contacting factory.

MOUNTING DETAILS









WORLD'S FIRST AUTOMATIC RANGING DIGITAL PANEL METER

MODEL DM-2000AR

DESCRIPTION

The Datel DM-2000AR is the first digital panel meter to feature automatic ranging over three full scale input ranges. It measures readings from 20 volts down to 100 microvolts without external scaling and increases the dynamic range of the instrument to 103 db over conventional DPM's. The unique autoranging circuitry operates by first sampling an input on the most sensitive range (±199.9mV). If an overange condition is indicated, the circuitry is automatically switched to the next higher range and recycled, and again to the highest range if the second is exceeded. The worst case conversion time is 33 milliseconds (30 conversions per second) if the highest range is selected and somewhat faster on the lower ranges.

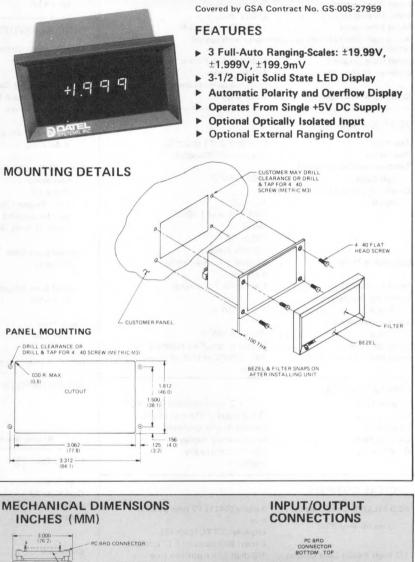
The automatic ranging feature, with three full scale input voltage ranges of ± 19.99 volts, ± 1.999 volts and $\pm 199.9mV$ offers the user a number of advantages. The cost savings over the parts, installation and test of a front panel range switch alone would justify the use of DM-2000AR. Another advantage is the savings in operator time and the associated errors incurred with the use of a range switch. Also, the versatility of a 20 volt to 100 microvolt dynamic range cannot be discounted in bench testing situations.

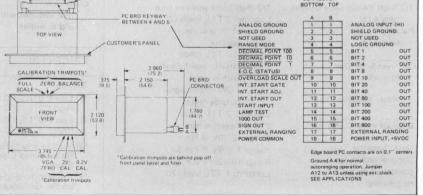
The DM-2000AR has a single ended input with an input impedance of 1 Megohm and over-voltage protection to ± 100 volts. Accuracy is $\pm .1\%$ of full scale, ± 1 count with a maximum conversion time of 33 milliseconds. The temperature coefficient of the DM-2000AR is ± 100 PPM/°C.

The display of the DM-2000AR is a 3-1/2 digit, seven-segment LED display with automatic polarity indication and automatic overflow indication. A digital input allows for the testing of all readout segments by displaying "+1888". All segments are viewed through a red filter which sharpens contrast and eliminates internal reflections.

All displayed information is available at the I/O connector in BCD form. Digital inputs and outputs also allow for start-stop control and external clocking. Also, the automatic ranging can be overriden for external (manual) control. In addition, an optical isolation option is available which decouples the analog input section from the digital logic so that ground disturbances caused by the fast-switching digital circuits will not affect the analog input.

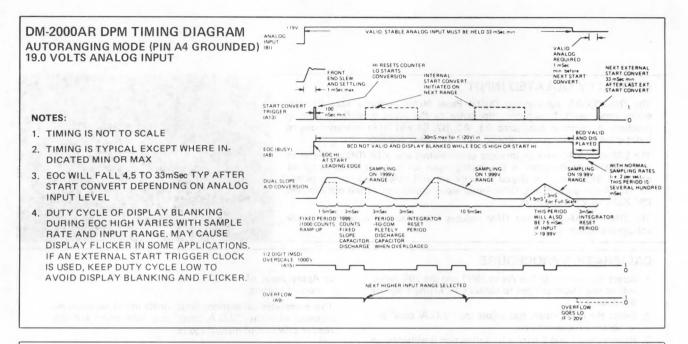
The DM-2000AR is packaged in a rugged 3"W x 1.3/4"H x 2-1/4"D LEXAN case with a total weight of less than 6 oz. Construction is entirely modular with snap-apart PC boards. The unit can easily be panel mounted with access to calibration controls obtained by snapping off the front bezel. The entire unit can be removed from its mounting panel and disassembled with just a screw driver in less than one minute.





	SPECIFICATIONS (T	ypical @ 25°C, 15 minutes warm-up)		
	ANALOG INPUT (single ended) Full Scale Input Ranges (automatic ranging)	Note: Display reads in volts on high ranges, millivolts on ±19.99V low range. ±1,999V ±199.9mV	End of Conversion (pin A8, Busy) Internal Start Output	1 line, HIGH - during the conversion period (display blanked) LOW - conversion complete Loading: 2 TTL loads (2) 1 line, positive true pulse
	Input Bias Current	±100V max.	(pin A12)	Loading: 1 TTL load (2)
	Input Impedance		DIGITAL INPUTS (Dynamic	inputs should have TTL rise times)
	isolation option):	bie only with optical	Ranging Mode Control	1 line, "1" = external ranging,
	Input Configuration	Single ended Bipolar Floating		"0" = automatic ranging
1	Common Mode Voltage	±100V _{CM} max.		Loading: 3 TTL loads (1)
	Common Mode Rejection	to digital output common 70dB @ 60 Hz		2 lines - Loading: 1 TTL load (1) Range Pin A17 Pin B17
_		700B @ 60 H2	Shown with pin	Range Pin A17 Pin B17 19.99V "0" "1"
	PERFORMANCE			1.999V "1" "0"
	and the second se		A17 & B17 are disabled	199.9mV "0" "0"
	Accuracy		if A4 is LO.	"11" Range code lights 2 D.P.
	Temperature Coefficient of		External Start Convert	Don't use.
	Full Scale	±100 PPM/°C		1 line-min pulse width-100 nsec
1	Zero Drift (referred to the		(Pin A13)	"O" to "1" (」) resets output
	input)	30µV/°C (199.9mV and 1.999V		register and blanks display, "1"
		(199.9m V and 1.999 V range)		to "0" (]) initiates conversion
		150µV/°C		process. Loading: 1 TTL load (1)
		(19.99V range)		1 line, gates internal clock
1	Conversion Time	33 msec max (see timing	(Pin A10)	"1" = run, "0" = stop
	Input Settling Time	diagram) 1 m sec for F.S. change	a be as the main of	Loading: 1 TTL load (1)
	Operating Temperature	This sector 1.3. change	· · · · · · · · · · · · · · · · · · ·	Controls rate of Internal Start Clock
	Range	0°C to +50°C		(see application section)
	Storage Temperature	22°2		1 line, negative true, displays
	Range			+1888 to test all display segments
	Input Power (See Note 4)	+5 ±.25VDC at 800mA (max), <50mV		Loading: sink 35mA. ples/second and is externally adjustat
		spikes	NOTE. Internal start clock is 2 sam	pres/second and is externally adjustat
	DISPLAY OUTPUT		ADJUSTMENTS	Zero, balance, full scale, VGA zero, 2V cal and 0.2V cal
	Display Type	red LED seven segment 0.3" high		trimpots accessible behind
	Data	3-1/2 digits (1999 max count)		snap-on front bezel
	Polarity	±automatically displayed automatically displayed	Recalibration Interval	(Normal conditions) 90 days
	Overflow	"OF" automatically		
_		displayed	PHYSICAL (3)	
	DIGITAL OUTPUTS		Case Size	3''W x 1.75''H x 2.25''D Black polycarbonate plastic
	BCD (3LSD's) Data Outputs	3 digits (8421) 12 lines positive	Weight	
		true	Mounting	Panel mounted through a 1.812" x
	(pins B5 thru B16)	Loading: 2 TTL loads (2)		3.062" cutout with four 4-40
	1/2 Digit (MCD) Data Output	Except 800 output: 1 TTL load	Connector	screws. Dual 18-pin, PC Edgeboard Type,
	1/2 Digit (MSD) Data Output . (pin A15)	1/2 digit-1 line-positive true Loading: 2 TTL loads (2)	(not included with DPM,	0.1" centers (Viking #3VH18/IJN-5
	Polarity	1 line, "1" = positive,	add to order)	or equal) with key between
	(pin A16)	"O" = negative	and the second second	pins 4 and 5
1	Overload Scale Out	Loading: 2 TTL loads 1 line, HIGH - input signal	PRICE (1-9)	\$169.
	(pin A9)	within range	NOTES	(no optoisolation, less connectors)
		LOW - input signal	NOTES:	Presented
	Note: Negative True	outside range	(1) Low ("0") ≤ + 0.8∨ High ("1") ≥ + 2.0∨	Recommended power supply is a Datel UPM-5/1000B or equiv
	Decimal Point Outputs	Loading: 2 TTL loads 3 lines, negative true	(2) Low ("0") $\leq + 0.4V$	alent highly regulated type.
		Range 19.99V @ Pin 6	High ("1") ≥ + 2.4∨	Power current is 400 to 800m max depending on digits dis-
	Note: Negative True,	Range 1.999V @ Pin 5	(3) Module is fully repairable and features snap together PC	played and sample rate
	Decimal points are	Range 199.9mV @ Pin 7	Boards	(5) 1 Megohm input resistor is in series with input summing junc
		Loading: 1 TTL load (2)	(A) Associations in the second in DD	
	controlled by auto- ranging logic.		(4) Avoid logic spikes entering DP on the +5V power input. Use	M tion. Accuracy specification windegrade with significant extern

Electronic Design's



COMPLETE MODULAR CONSTRUCTION

Total modular construction is another plus for the DM-2000 AR.

Servicing is simple and straightforward.

The unit can be removed through the front panel without opening the users' instrument. Once the snap-on front bezel and four mounting screws are removed, the meter slides out of its Lexan case. The procedure is uncomplicated and takes less than one minute. Once removed, modular service is possible due to the five plug-in interconnected PC boards – no wiring or soldering is required.

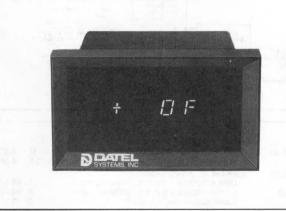
Troubleshooting is accomplished through board substitution and servicing can be completed within five minutes.

A full complement of replacement boards are readily available from Datel's Service Department.



ALPHA NUMERIC INDICATION OF OVERFLOW

When the voltage input exceeds full scale by a minimum of one least significant digit, the characters "OF" are displayed. All data digits are blanked. An example of this would be when full scale is +19.99V, then +20.00V would be the smallest possible overload.



BUILT IN DISPLAY TEST FOR PERIODIC TESTING

Testing for faulty display segments can be achieved in a matter of moments guarding against erroneous readings. Grounding pin 14 at the rear connector will display +1888 to test all possible segment combinations.



OPTICALLY ISOLATED INPUT

The DM-2000AR autoranging Digital Panel Meter normally uses a singleended input with 1 megohm impedance to the input amplifier summing junction. A common bus, (pins A1, A2, B2, B4 and A18) reference analog input ground, digital output ground and +5V power common.

The DM-2000AR-2 version includes optoisolators and a DC/DC converter to give transformer isolation of the analog input up to ±100 Volts to power common. However, the digital outputs are still referenced to the power common/logic ground bus. Differential input impedance of the optoisolated DM-2000AR-2 is 1 megohm.

The DM-2000AR-2 isolated DPM reduces false readings in common mode voltage applications.

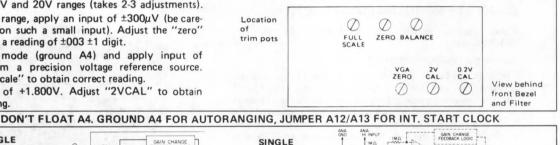
CALIBRATION PROCEDURE

- 1. Select manual mode (tie A4 to +5V) and the 20V range. Adjust the "balance" pot to obtain a flickering ± sign on the display.
- 2. Select the 0.2V range, and adjust the "V.G.A. zero" pot to obtain a flickering sign.
- 3. Repeat steps 1 and 2 until a flickering sign is obtained on both the 0.2V and 20V ranges (takes 2-3 adjustments).
- 4. On the 0.2V range, apply an input of ±300µV (be careful of noise on such a small input). Adjust the "zero" pot to obtain a reading of ±003 ±1 digit.
- 5. Select auto mode (ground A4) and apply input of +18.00V from a precision voltage reference source. Adjust "full scale" to obtain correct reading.
- 6. Apply input of +1.800V. Adjust "2VCAL" to obtain correct reading.

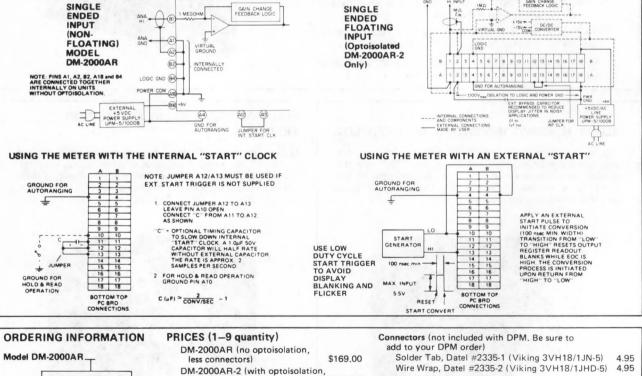


7. Apply input of +.1800V. Adjust "0.2VCAL" to obtain correct reading.

This completes calibration. Small drifts in the zero can be adjusted with the "V.G.A. zero" pot only which will not require selection of manual mode.



Suggested AC power supply: UPM-5/1000 B 5V, 1A, 115VAC input UPM-5/1000 BE 5V, 1A, 230VAC input Power supply Socket, MS-7



\$218.00

See inside back cover for DATEL sales offices

less connectors)

Covered by GSA Contract No. GS-00S-27959

\$ 49.00

\$ 54.00 \$ 3.50



MINIATURE 31/2 DIGIT AC-POWERED **DIGITAL PANEL METER**

MODEL DM-2115

Covered by GSA Contract No. GS-00S-27959

FEATURES

- Choice of AC line or +5VDC power
- Compact: Only 1.75" H. x 2.25" D. x 3" W.
- Large, Bright, 0.43" High Red LED Displays .
- Automatic Polarity and Overflow Display
- 5V/400mA Optional Power Input Ideal for . Portable Use
- **Differential Input**
- Optional Parallel BCD/TTL Output

GENERAL DESCRIPTION

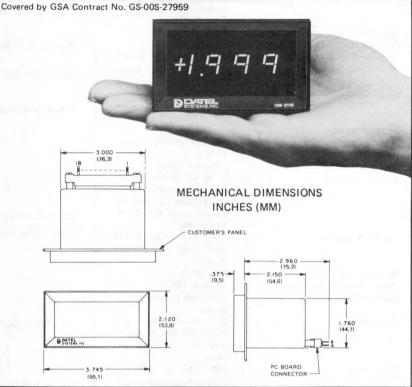
Datel Systems' DM-2115 is the world's smallest AC line operated Digital Panel Meter. Packaged in a compact 1.75" H. x 2.25" D x 3" W. Polycarbonate plastic case and using large 0.43" high seven-segment LED digits, Model DM-2115 provides an easy-to-read 31/2 digit display of ±1.999 volt full scale inputs complete with automatic polarity and overflow indication. Both the size and the power consumption of the DM-2115 have been significantly reduced through extensive use of MSI CMOS logic. Power input options include AC inputs of 100VAC, 115VAC or 230VAC at 47 to 440 Hz, or from +5VDC at 400mA, max. All AC supplies use a high quality C-core, strip-wound line transformer that consumes a low 3.5 watts of input power. For portable applications using the +5VDC input option, current drain can be further reduced to 120mA by blanking the display and using a press-to-read switch, or the display can be separately duty cycled.

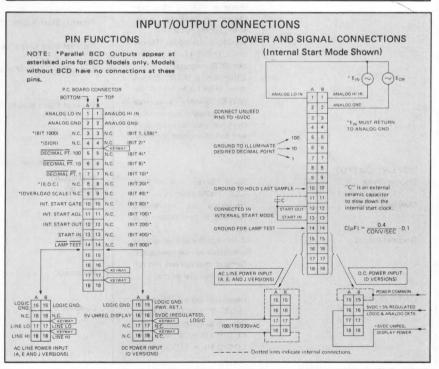
Model DM-2115 provides true differential input characteristics with an input impedance of 100 Megohms, min., and common mode rejection of 70 dB from DC to 60 Hz. The instrument accepts a single-ended or differential input voltage range of ±1.999V and generates a display that is accurate to within ±0.05% of reading ±1 count. The temperature coefficient is 50ppm/°C, max. over the operating temperature range of 0 to +50°C. Optional models are available with full parallel, BCD TTL data outputs and auxiliary signals at the PC board I/O connector.

An internal start clock commands 4 conversions per second but an external capacitor will reduce this sampling rate. Or this internal clock can be inhibited to hold and display the last sample. An external start trigger pulse may be used to sample from 0 to 40 conversions per second.

Convenience features include display test and decimal point illumination by grounding pins. In AC versions, the high isolation line transformer and the separation of analog and digital grounds provide additional protection against ground loops.

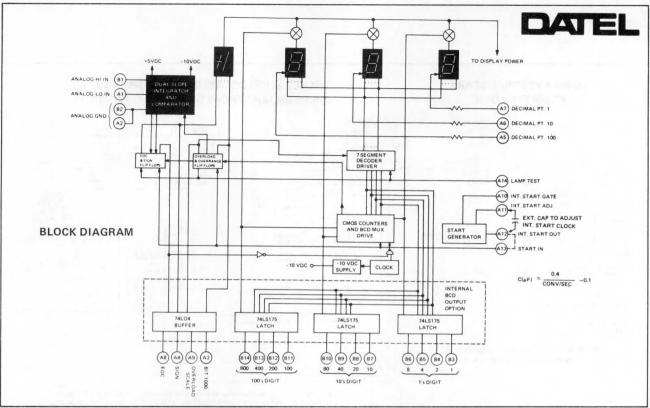
Applications for the DM-2115 include measurement and display of any variable that can be converted to a voltage. These include pH, pressure, distortion, torque, liquid level, temperature, displacement and many others.

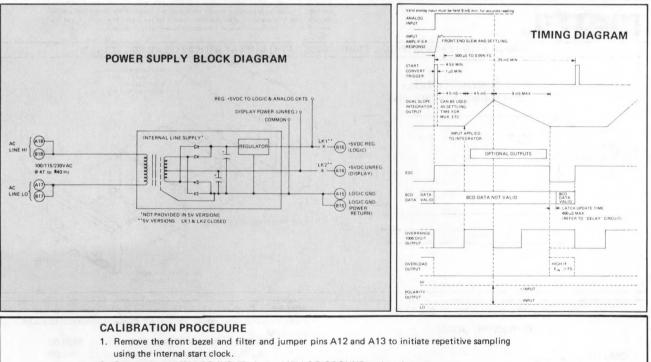




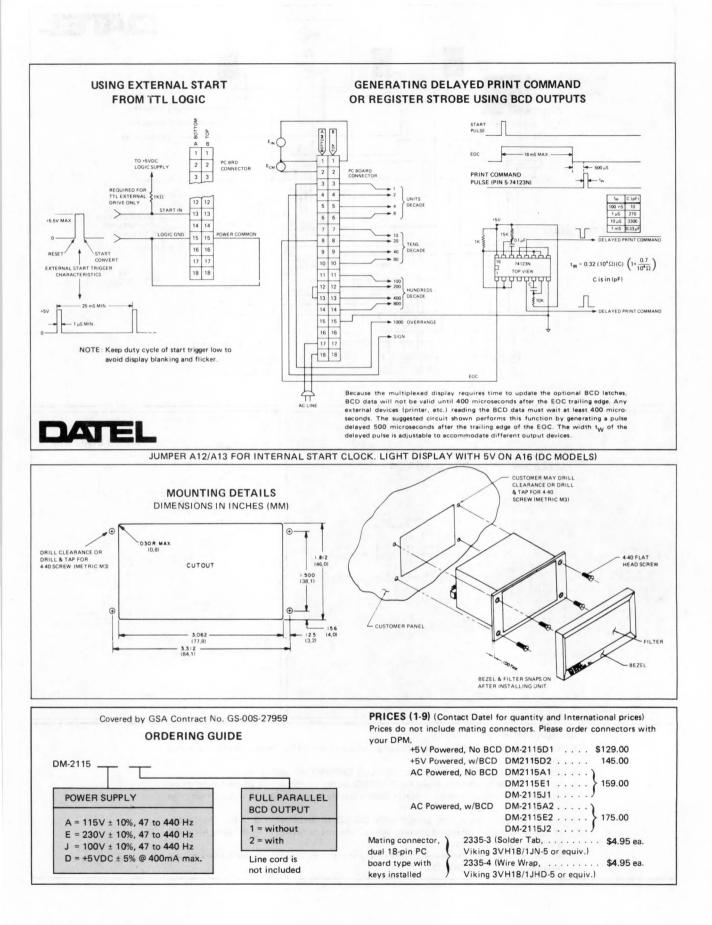
SPECIFICATIONS (Typical @ +25°C unless noted)

INPUTS		BCD Outputs	12 latched parallel lines
Input Voltage Range	±1.999 Volts DC		8-4-2-1 positive true binary
Input Impedance	100 Megohms, min.	CONTRACTOR OF A LAND AND AND AND A LAND AND AND AND AND AND AND AND AND AND	coded decimal. Loading 2
Type of Input	True Differential		TTL loads. BCD not valid
Input Bias Current	Analog HI Input 3nA Typ,		until 400 µsec after EOC
	7nA Max.		trailing edge. See timing.
	Analog LO Input 45nA	Overrange (Pin A3)	Counts between 1000 and
	Typ, 500nA Max.		1999 only, indicated by
Input Polarity	Bipolar-Automatic	(Arrest)	logic high (2TTL loads)
Common Mode Rejection	70 dB, DC-60 Hz	Overload Scale (Pin A9)	> 1999 counts indicated by
Common Mode Range	(EIN + ECM) Must be with-		logic high (2 TTL loads)
	in ±3.0V to logic or Analog	Polarity (Pin A4)	Logic high for positive in
	Ground, ±300V to AC line		puts, logic low for negative
Input Overvoltage	±50V Max. continuous		inputs (2 TTL loads)
	±200V Max. 5 sec. duration	End of Conversion (Busy) (Pin A8)	High on leading edge of
			start pulse and during con
PERFORMANCE	±0.05% of reading ± 1 count		version. BCD outputs are
Accuracy @ 25°C	1mV		counting while EOC is HI
Temperature Coefficient	±50ppm/°C Max.		and, therefore, are not valid
Conversion Speed	0 to 40 conversions/sec.		BCD outputs are valid 400 µSec after EOC goes LO
Conversion Speed	max. (ext. trigger required	- of the second second	indicating conversion com
	at max. rate) 4 samples/sec.	the second se	plete (2 TTL loads).
	normal from Int. Clock.	INPUT/OUTPUT CONTROL	piete (2 TTE loads).
	(adjustable)		A Contract of the second second
Input Settling Time	500 µs to 0.05% for full	External Start Input (Pin A13)	Positive pulse, 0 to +5V
	scale step. See timing	al and the second se	min., 1 μ s min. duration
	diagram.		CMOS input. For TTL
Operating Temperature Range	0 to +50° C		compatibility, connect start input through 1KΩ to +5V
Storage Temperature Range	-20°C to +85°C		TTL supply. Max. input
Warm Up Time	5 minutes to specified ac-		+5.5V.
	curacy.		
Adjustments	Diff. Amp. Balance and	ALL INPUT CONTROLS ARE TTL/E	TL COMPATIBLE EXCEPT
	Full Scale located behind	EXT. START (A13)	(SEE PG. 4)
	snap on front Bezel and	LOGIC LO = 0V < "0"	′ ≤ +0.8V
	filter.	LOGIC HI = +2.0V ≤ '	'1'′ ≤ +5.0V
Power Supply	100, 115 or 230VAC,	A	
	±10%, 47 to 440 Hz @ 3.5 Watts or +5VDC ±5%, reg-	Internal Start Gate (Pin A10)	HIGH - RUN Loading,
	ulated at 400mA max.		LOW - HOLD) TTL load.
	total, spikes ≤ 10 mV.	Internal Start Adjust (Pin A11)	
	LOGIC and Analog: 150mA	Internal Start Out (Dis A12)	Start Pulse. See pg. 1. +5V positive pulse 1 mS
	drain (+5V) (120mA with-	Internal Start Out (Pin A12)	duration.4 samples/sec.(adj
	out BCD outputs)	Lamp Test Input (Pin A14)	Grounding this input dis-
	DISPLAY: (+1888), 250mA		plays +1888 for testing all
	drain (+5V) max (pin A16)	State of the second second second	segments (4 TTL loads)
	NOTE: Display is on sep-	Decimal Point Inputs (Pins A5, 6, 7)	Grounding these inputs il-
	arate power connection,		luminates corresponding
	does not require regulation		decimal points on the dis-
	and can withstand 5V ± 1V		play. Sink 40mA, 80 µsec,
	ripple.		33% duty cycle
DISPLAY OUTPUT		Display Power (pin A16)	. 250 mA max. at +5VDC
Display Type	Solid State 0.43" Red	PHYSICAL	
Copiay type	LED. 100% overrange.	Case Size	3" W x 1.75" H x 2.25" D
Overload Scale	Indicated by alternating	and the second	(76,2 mm x 44,4 mm x
	flashing of center bars and	Contraction of the second	57,2 mm)
	zeroes.	Case Material	Black polycarbonate plastic
Decimal Points	3 left-hand decimal points	Weight	Line Power Units - 10 oz.
	selectable at rear connector.	and the set of the second	(284g)
	Ground appropriate pin for		5V Units - 5 oz. (141g)
	desired decimal point.	Mounting	1.812" x 3.062" cut ou
		A STATE OF A STATE OF A STATE OF A	attached by four 4-40 flat
DATA OUTPUTS	(Available with BCD option	Connector	head countersunk screws.
	only) TTL/DTL compat-	Connector	DUAL 18-pin PC edge- board type on 0.1" centers
	ible, all outputs buffered.		(Viking 3VH18/1JN-5 or
	LOGIC LO = "0" ≤ +0.4V	State of the second	
	LOGIC HI = "1" ≥ +2.4V		1JHD-5 equiv. w/keys).





- 2. Connect both ANALOG INPUT pins to ANALOG GROUND and apply power.
- After 5 minutes of warmup, adjust the BALANCE potentiometer so that all display digits read zero while the display polarity indicator flickers equally between plus and minus. Offset range is approximately ±15 mV.
- 4. On the DM-2115 under test, jumper ANALOG LO IN and ANALOG GND. Then, apply +1.9905VDC from a calibrated precision voltage reference to ANALOG HI IN, using ANALOG GND as signal input return.
- Adjust the GAIN potentiometer of the unit under test so that the display flickers equally between +1.990 and +1.991VDC.



Electronic Design's



MINIATURE 41/2 AND 43/4 DIGIT DIGITAL PANEL METERS

MODELS DM-4000 AND DM-4300

Covered by GSA Contract No. GS-00S-27959

GENERAL DESCRIPTION

The Datel Models DM-4000 and DM-4300 are, respectively, the world's smallest $4\frac{1}{2}$ and $4\frac{3}{4}$ digit LED digital panel meters, and include input offset autozeroing.

Both models feature large, easy to read red LED displays that are 0.43'' high in the DM-4000 and 0.3'' high in the DM-4300. Input power for either model is +5VDC at 600mA, max.

These DPM's employ a differential, optically isolated floating input that withstands ±300 volts common mode to digital ground with 120 dB common mode rejection from DC to 60 Hz. This provides high noise immunity in industrial applications.

The counter circuits are driven by a stable crystal controlled oscillator which may be specified to synchronize with either 50 or 60 Hz, the common AC power line frequencies. Dual slope integration synchronized to 50 or 60 Hz provides 60 dB of normal mode rejection to power hum on the signal input.

An internal ±6.4 VDC reference and the reference input may be externally connected for 3-wire, TC-tracking ratiometric measurements. This configuration reduces temperature drift errors by normalizing to a single positive reference voltage.

Model DM-4000 measures and displays a full scale input of ± 1.9999 V. The full scale input/ display range of Model DM-4300 is ± 3.9999 V. Both models have an input impedance in excess of 100 megohms, input bias current of 100 pA max. — which doubles each 10° C.

Accuracy of Models DM-4000/4300 is $\pm 0.01\%$ of reading ± 1 digit, with a temperature coefficient of 15 ppm/°C max. over the 0 to $\pm 50^{\circ}$ C operating range. When operating from the internal clock both models update their display at a 2 sample per second rate, but when driven by an external start pulse the DM-4000 sampling rate can be varied from 0 to 5 per second and the DM-4300 from 0 to 3.3 per second. Calibration adjustments after a 15 minute warmup are easily accessible behind the front panel filter.

The red LED seven segment digits provide automatic display of overrange, overload, polarity and decimal point: Overload is indicated by alternate flashing of the center bars of the sign and 4 LSD displays. The decimal points are illuminated by grounding the appropriate connector pin.

- Miniature Case With 5 Large, Red LED Displays
- Autozeroing, Optoisolated Floating Input
- Operates From +5VDC Logic Power
- High Noise Immunity using 120 dB CMR, ±300 V_{CM} Bipolar Floating Input
- AC Hum Rejection (60 dB NMR) using Line-synchronized Quartz Crystal Counter
- ► 3-Wire Ratiometric Input Reduces Drift Errors from Bridge Inputs

DTL/TTL compatible overrange, polarity, overload and EOC outputs are available at the rear case, 18-pin dual PC board connector in both models. Sixteen lines of BCD data are optionally available at the rear connector in full parallel, 8-4-2-1 positive true format.

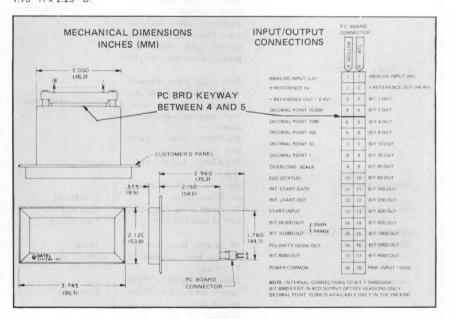
These DPM's are housed in a high-impact polycarbonate case that measures only $3'' W \times 1.75'' H \times 2.25'' D$.

High immunity to common mode and normal mode voltages combined with the ratiometric feature especially recommend these DPM's for use with many bridge transducers. Applications include temperature measurement, motion, stress and many other physical phenomena.

+39999

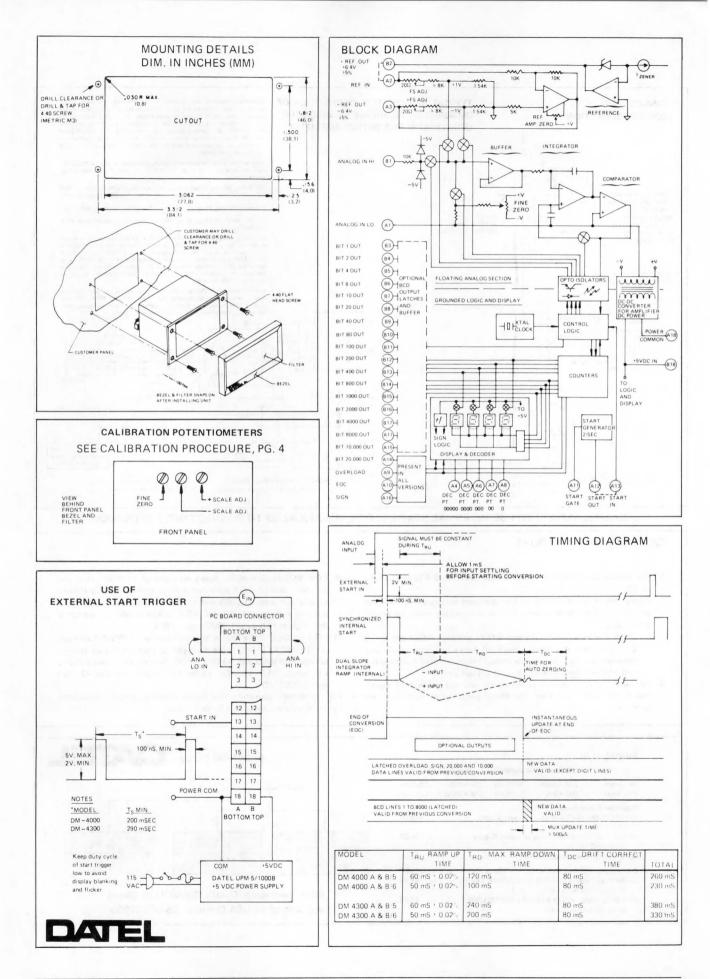
99

DATEL

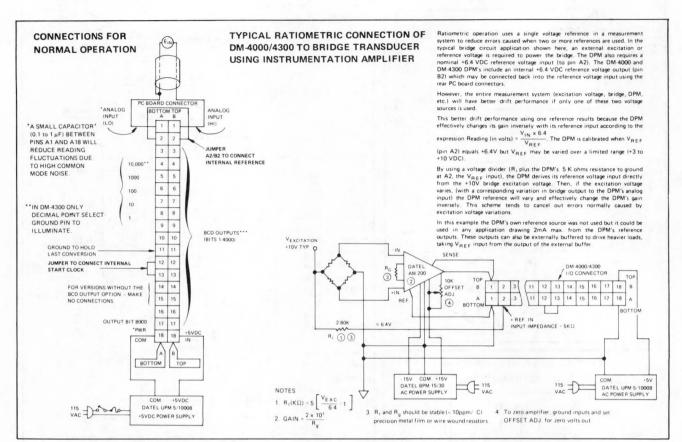


SPECIFICATIONS (Typical @ +25°C unless noted)

INPUT CHARACTERISICS			DM-4300: 10000 to 39999
Input Voltage Range (Full Scale)	DM-4000: +1.9999 Volts		counts indicated by a pos-
input voltage nange (i un ocale)	DM-4300: ±3.9999 Volts		itive true 2-1 BCD code on
Input Impedance		and the second sec	pins A14 and A15 along
Input Bias Current		and the later of the second second second	with a LOW on overflow
input bits current i i i i i i i i i i i i i	(doubles/10°C)	and the second	(pin A9)
Input Configuration	the second second second	Polarity	Input signal polarity pos-
input comiguration of the test of the	tical isolation to digital		itive indicated with a HIGH.
	ground employed for dif-		Negative polarity indicated
	ferential characteristics.		with a LOW.
Input Polarity	Automatic bipolar with	Overload Scale	DM-4000: Greater than
	polarity display indication.		19999 counts indicated by
Common Mode Rejection			a HIGH (positive true) on
	up to 1K ohm source un-		overflow (pin A9). Less
	balance.		than 19999 counts indi-
Common Mode Voltage Range	NTL TO T 02.7.9 8		cated by a LOW.
	ground.		DM-4300: Greater than
Input Overvoltage	5	ACT - UNCOMENT OF THE ACT OF	39999 indicated by HIGH
	tween inputs without dam-	And second se	on overflow (pin A9). Less
	age. ±100V to 5 seconds		than 39999 counts indi-
	without damage.	C protection in the second second	cated by a LOW.
PERFORMANCE	interest samager	End of Conversion (EOC)	HIGH - during conversion,
	+ 01% of reading + 1 digit		BCD outputs counting and
Resolution			invalid.
			LOW - conversion com-
Temperature Coefficient of Reading Conversion Speed (Adjustable using	rsppm/ c max.		plete. BCD outputs valid
	DM 4000: 0 to E conver	1 HIG Optimized States	500 µsec after EOC.
ext. trigger)	sions/sec.	The set in the set of	(See timing diagram)
	DM-4300: 0 to 3-1/3 con-	INPUT/OUTPUT CONTROL	
	versions/sec.	External Start Conversion Command	Positive pulse 100 nsec.
Land Catalian Time		and the second s	min. width. 2.0V min. 5V
Input Settling Time	the second se		max. height. Conversion
	Hz line. 60 mS integration	and a strength of the strength	initiated upon return from
Operating Temperature Range	for 50 Hz line optional.	The specific party of the second s	"HIGH" to "LOW".
Storage Temperature Range		Internal Clock Start Gate	Controls internal start clock
Warm Up Time			"HIGH" - Run
warm op nime		the spectrum of the second sec	"LOW" - Stop
Adiustante	curacy. Full scale (Gain) trim	and the second se	Loading - 1 TTL load.
Adjustments	located behind front bezel.	Internal Start Output	Positive pulse output of
			internal start clock. 2
	Separate ± adjustment and	the subset of the second second second	pulses/second.
Input Power	ratio zero trim. Autozero ing. +5 ± .25 VDC @ 600mA	Decimal Point Inputs	
Input Power			illuminates corresponding
	max. (with input logic		decimal points on the dis-
	spikes 10mV max.). Sug- gested power supply is a		play.
	Datel UPM-5/1000B or	Ratiometric Output	Derived from internal ref-
	equivalent highly regulated		erence for TC-tracking.
	type. Power current varies		Provides ±6.4V @ 2mA
	rapidly with digits dis-		max. for 3-wire ratiometric
	played, conversion rate, etc.		measurement. Ratiometric
DISPLAY OUTPUT		a series of the	inputs can be normalized
Display Type	Red, LED seven segment		to a single positive refer-
	digits with automatic dis-		ence voltage.
	play of overrange, over-	Ratiometric Input	Calibrated for +6.4 V±5%
	load, polarity and decimal		input (avail. from ratio-
	point:		metric output, above). May
	DM-4000: Digits 0.43"		be varied from +3V to +10
	high		VDC for TC-tracking
	DM-4300: Digits 0.30"		bridge applications. Read-
	high	and the second second second	VIN × 6.4
Overload Scale	Sign and 4 LSD's display		$ing (volts) = \frac{11}{V_{REF IN}}$
	center bars blink.	PHYSICAL	
Decimal Points	Selectable at rear connector.	Case Size	3''W x 1.75"'H x 2.25"D
	Left of each full digit.	Case Material	Black high-impact poly-
OPTIONAL DATA OUTPUTS		and the second second second	carbonate plastic.
BCD Outputs	16 parallel lines (8-4-2-1)	Weight	8-10 oz.
	positive true. Loading: 2	Mounting	Through a 1.812" x 3.062"
	TTL loads.	and the second	cutout secured with four
Overrange	DM-4000: 10000 to 19999	A share the second second	4-40 screws.
	counts indicated by HIGH	Connector	Dual 18-pin PC edgeboard
	counts indicated by HIGH on pin A15 with LOW on	Connector	Dual 18-pin PC edgeboard type, 0.1" centers (not in-



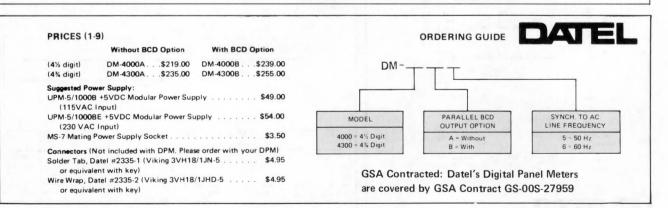
GOLD BOOK 76/77



JUMPER A12/A13 TO USE INTERNAL START CLOCK, JUMPER A2/B2 TO CONNECT INT. REFERENCE

CALIBRATION PROCEDURE

- 1. For normal operation (see figure) jumper pin A12 to A13 and pin A2 to B2.
- 2. Apply power to the DPM and a precision calibrated DC voltage source and allow both at least fifteen minutes for warm up before proceeding
 - a) Short the input leads (A1 and B1) to ground. Adjust the FINE ZERO so that the display reads all zero's and the sign flickers between plus and minus. Disconnect the input leads from ground and connect them to the precision voltage source.
- 3. For both models, zeroing is automatic and the calibration adjustments are accessible after the front panel bezel and filter are 4. For ratiometric operation (see figure showing typical connection) removed.
- a) FOR MODEL DM-4000: Apply an input of +1.99905 volts and set the + SCALE ADJ, potentiometer so that the display flickers equally between +1.9990 and +1.9991 VDC. Reverse the input polarity and set the -SCALE ADJ. potentiometer for a display that flickers between -1.9990 and -1.9991.
- b) FOR MODEL DM-4300: Apply an input of +3.99905 Volts and set the +SCALE ADJ. potentiometer so that the display flickers between +3.9990 and +3.9991 VDC. Reverse the input polarity and Set-SCALE ADJ, for display that flickers between -3.9990 and -3.9991 VDC.
 - the previous steps must first be performed.





6-DIGIT, PANEL-MOUNT COUNTER/ TOTALIZER WITH TIMEBASE

MODEL DPC-8100

FEATURES

- Count capacity 999,999 pulses (6 decades) displayed on .6" high digits, AC line or +5 VDC powered
- Accepts several input types:
- 1. Switch inputs, Form A, B & C
- 2. Comparator, 25 mV to 2 V, 300 V rms isolation 3. Logic to 10 MHz or optoisolated logic
- Logic to 10 MHz, or optoisolated logic to 500 kHz
 Full parallel BCD data outputs
- Full parallel BCD data outputs
 Optional stored BCD outputs can be gated or multiplexed onto a data bus.
- Optional crystal timebase to measure frequency, countrate or tachometer inputs.

DESCRIPTION

The DPC-8100 Digital Panel Counter records and displays up to 6 digits of input counts or events (999,999 capacity) on bright .6" (15 mm) high LED readouts. The panel mounting instrument accepts a very wide variety of inputs so that one basic instrument will serve many applications.

The all-electronic counting circuitry can record up to 10 million counts per second. Applications include industrial event counting and totalizing and process control batch counting.

Inputs may be derived from Form A, B or C switch closures with anti-bounce filtering provided. Low level signals down to ± 25 mV with $\pm 300V$ isolation may be accepted at rates up to 1 MHz using the optional low level comparator. Optoisolated inputs are also available with count rates up to 500 kHz and isolation to $\pm 300V$ RMS. Control inputs such as start, stop and reset as well as the count input may be optoisolated. Finally, direct TTL logic inputs will accept up to 10 MHz count rate.

The DPC-8100 Counter features digital logic outputs of the displayed count for data transmission to a computer or digital processor. These outputs are in full parallel standard binary coded decimal form (BCD) with TTL/ DTL compatible logic levels. An optional second PC board with a fully latched and gated BCD register will store the digital outputs.

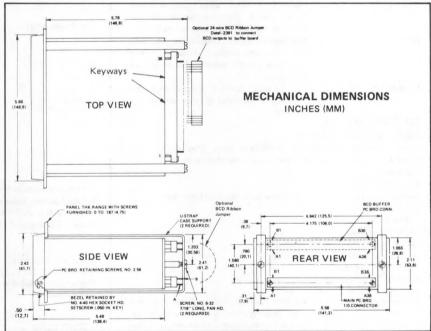
These stored outputs may be transmitted at any time on external command to a remote processor using a data bus. Gating is compatible to open collector TTL/DTL logic and outputs can be multiplexed in groups of 4 lines up to 24 lines (6 digits).

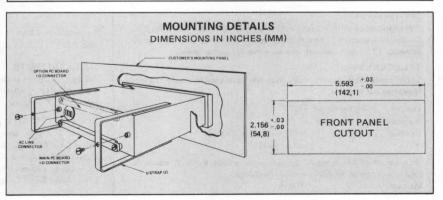
The optional second PC board can also contain a high accuracy timebase to allow precise gating of external count inputs. The crystal-controlled timebase converts the DPC-8100 into a countrate, frequency or period meter or a tachometer. When used with the BCD buffer, very short samples (down to 10 µs) of count rates may be taken then displayed for convenient viewing. (See Display Modes).

Front panel controls on the DPC-8100 manually control start, stop, and reset functions while logic inputs duplicate these functions. Many other input/output functions and displays are provided to adapt to a range of applications. The DPC-8100 Counter is powered by a choice of 100, 115 or 230 VAC, 47 to 440 Hz or from +5VDC at 1.5 Amps max.

A black anodized extruded aluminum case houses the DPC-8100 for high electrical noise rejection in industrial environments. Additional power line filtering is offered by a bifilarwound choke and regulated power supply.







GOLD BOOK 76/77

SPECIFICATIONS (typical @ +25°C unless noted)

GENERAL	A TOTAL CONTRACTOR AND	OPTOISOLATOR FOR TTL INPUT - Externally wired to TTL in	n-
	Six (6) self-illuminated digits, red LED	put. Pins A33 (+) and A34 (-), see applications.	
	0.6" (15mm) high, 7-segment format. Count capacity: 999,999 counts. Re-	Isolation	
	placable LED's on individual sockets.	DIGITAL INPUTS	
Power Fail	Front panel red LED lamp illuminates	ALL DIGITAL INPUTS ARE COMPATIBLE WITH DTL/TTI	L
	to warn if power has been interrupted,	LOGIC SOURCES:	
	indicating possible incorrect count dis-	LO = "ZERO" <+0.8V	
	played. Extinguished by RESET.	HI = "ONE" >+2.0V	
Gate On	Front panel red LED lamp illuminates while instrument is accepting counts.	RUN/STOP (pin A15) – 1 line, 1 TTL load, plus 4.7 K Ω pullup to +5V. STOP input (pin A18) must be grounded when using RUN	
Overrange (Overscale)	Front panel red LED lamp illuminates	STOP input. Leave RUN/STOP floating or HI if not used.	4/
	if count has exceeded 999,999. Display	Level sensitive (rise time not critical) using Schmitt logic	
	continues counting after 999,999 counts.	HI – Counting is stopped	
Display Latched		LO – Counts are accepted	
	when a count is being stored in the	Positive-going threshold . +1.7V	
	optional display latches. Display test not	Negative-going threshold +0.9V	
	available with optional display latch. Regulated 5V must be used.	START (pin A17) 1 line, 1 TTL load plus 4.7 K Ω pullup to	to
Temperature Ranges	0	+5V. Counts accepted after falling edge o	
Tomporataro Trangoo TT	Storage: -25°C to +85°C	LO pulse, 50 nsec min. width, until STO	P
FRONT PANEL CON		is pulsed. RESET must be HI to enabl	
Start	Pushbutton opens count gate to accept	start of counting. START LO pulse will b	
	input pulses. Hold start button in two	stored if RESET is LO but will not be en abled until RESET goes HI. (Note	
	seconds or longer to test display with all	START and STOP form an RS latch ci	
0	8's. Does not disrupt counting.	cuit. The last input to be LO determine	
Stop	Pushbutton closes count gate to block input pulses. Accumulated counts re-	the latch state.	-
	main on display until Reset occurs.	$\overline{\text{STOP}}$ (pin A18) 1 line, 1 TTL load plus 4.7 K Ω pullup t	to
Reset		+5V. Counting is stopped on falling edg	ge
	but does not inhibit additional counts	of LO pulse, 50 nsec min. width. Coun	
	(can be externally wired to inhibit further	pulse in progress is recorded if STO	
	counting).	occurs. Gnd. if using RUN/STOP contro	
Display Test	See START control. Display test not	Counts are held after STOP until cleare	90
	available if optional display latches are	By RESET. RESET (pin A16)	
CONTROL INPUTS	ordered.	1 line, 1 TTL load, LO pulse 50 nsec mir	n.
LOW LEVEL COMPARA	TOP	clears counter to 000,000 but does no	ot
	me not critical) to inputs from ± 25 mV min.	inhibit additional counts unless STOP ha	
	ext. threshold adj. (see applications).	occurred. Schmitt level-sensitive input	
Hysteresis		Negative going threshold to +0.9V. Pos	51-
Max count rate		tive-going threshold +1.7V. Optoisolated inputs for START, STOP, and RESET are also provided	
Isolation	300V rms from input to logic gnd.	see applications. Pulse resolution, 1 microsecond. Max. pulse rate, 50	
Input Impedance		KHz. Isolation 300 V rms	-
(differential)	1 MS2	Display Blank (pin A11) 1 line, 3 TTL load. Ground to illuminat	te
Input Impedance (to Lo Level Com.)	500 KQ	display. Float to blank display, or connec	ct
Input Bias Current		to TTL logic.	
Capacitive Coupling (In-		Display Follow/Hold (pin A12)	**
puts and floating power		(for optional latchable +5V. LO latches display on current count	
leads to logic gnd.)		display only) BCD outputs not latched, Display test no	
Excitation current	Up to 1 mA out available from +10V and	available with latch display option. +5V	
	-5V floating power outputs to excite ex-	regulated must be used on V LED's.	
	ternal threshold potentiometer, or bridge circuit.	Decimal Points 6 lines, ground to illuminate correspond	
SWITCH INPUT	un sum	ing left of digit decimal point (see pi	in
	./ext anti-bounce filtering for Form A, B or	Out). 16 mA sink req'd for logic drive.	
C switch inputs. 50 cc	ounts/sec, max., adj. using ext. filtr. com-	(pin A22) 1 line, 1 TTL load. LO blanks leadin	-
ponents. TTL input (belo	w) may be wired for higher speed.	zeroes.	.9
TTL COUNT INPUT		DATA OUTPUTS	
Logic compatible inputs	, using Schmitt level-sensitive NAND gates	All digital outputs are compatible with DTL/TTL logic levels.	
(rise time not critical).		LO = "ZERO" <+0.4V Positive	
Positive - going threshold	d +1.7V	HI = "ONE" >+2.4V True Logic	
Negative-going threshold		BCD COUNT DIGITS (pins B13 thru B36) Full parallel binary code	be
	1 TTL load plus 4.7 K Ω	decimal (1-2-4-8), consecutively spaced in ascending order. 24 lines	
	pullup to +5V	totem-pole TTL logic levels out, positive true. 7 TTL loads.	
May be wired for latch	ing operation to accept Form C contacts.	Overrange Out (pin A23) - 1 line, 10 TTL loads	
Count is recorded on A3		HI - Count exceeds 999,999	
Max count rate		LO – When RESET occurs, or if count is less than 1,000,000.	

SPECIFICATIONS (cont.)

CONTROL OUTPUTS

Reset Out (pin A35)	. 1 line, 10 TTL loads. Logic output of $\overrightarrow{\text{RE-SET}}$ function, can be tied to STOP input
	to clear and inhibit counts. Totem-pole
	format.
Gate Out (pin B8)	. 1 line, 10 TTL loads
	LO - counts are accepted. Count pulse
	in progress holds GATE LO until count is
	recorded, if STOP is pulsed.
	HI – counting is stopped
Power Fail (pin B9)	. 1 line, 10 TTL loads
	LO - power has been interrupted, counts
	may be invalid. LO at power turn-on.
	HI – when RESET occurs.
ADDITIONAL CONN	ECTIONS
VIED 1 (pin A36) 3MSD'	s Each input connects +5V power to 3 dis-
V (nin 87) 21 50'	Inlaw digita 200 mA may @ +EVDO aach

VLED 2 (pin B7) 3LSD's play digits. 300 mA max. @ +5VDC each connection. Internally connected on AC versions. (Don't connect.)

+5VDC Power (pins A1 &

B1 internally connected) These pins are for +5VDC logic power input on +5V powered units, 1 Amp max. On AC-powered models, an output of +5VDC @ 200 mA max is available from these pins. A1 & B1 are not internally connected to the displays except on AC models. (Use

VLED 1 & 2 for displays)

Power and Logic Ground

(pins A2 & B2 internally

connected +5V power return for display and logic.

POWER SUPPLY

Choice of 100, 115 or 230 VAC $\pm 10\%,$ 10 watts typ, 47 to 63 Hz. OR -

+5 $\pm 0.25 VDC$ @ 1.6A max (displays & logic), logic noise 50 mV max. BCD Buffer/Timebase +5VDC @ 175 mA, regulated (spikes <50 mV)

CONNECTORS

Dual 36-pin PC edgeboard type, 0.1" centers, solder tabs, Datel 2597-14 (Viking 3VH 36/1JN-5 or equivalent) AC power connected by triple ¼" tab assembly, recessed male, center tab grounded to case. PC board connectors included with each unit, plus a U.S. 3-prong type 9115 line cord.

MOUNTING

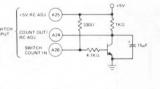
Panel-mounting through a cutout measuring 2.16"H X 5.59"W (54,8 X 142,1 mm) and secured by 2 U-Straps. See mounting diagram.

MECHANICAL DIMENSIONS

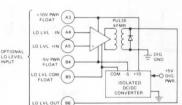
Case	5.56"W X 2.11"H X 5.78"D (141,2 X
	53,6 X 146,8 mm)
Bezel	5.86"W X 2.25"H X 0.50" THK (148,7 X
	57,0 X 12,7 mm) (See Diagrams) Bezel,
	filter and PC Brds are removable from
	front while unit remains secured in panel.
Weight	2.25 LB (1,0 Kg)

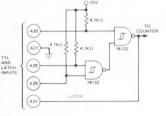
INPUT/OUTPUT CONNECTIONS DPC-8100 DIGITAL PANEL COUNTER (REAR PC BRD)

+5V POWER PWR & DIG. GND ISOL. RESET +
ISOL. RESET +
-5V PWR. FLOAT.
LO LVL. COM. FLOAT
LO LEVEL OUT
+5V TO VLED 2
GATE OUT
POWER FAIL OUT
DEC. PT0
DEC. PT00
DEC. PT000
BCD OUT 1
BCD OUT 2
BCD OUT 4
BCD OUT 8
BCD OUT 10
BCD OUT 20
BCD OUT 40
BCD OUT 80
BCD OUT 100
BCD OUT 200
BCD OUT 400
BCD OUT 800
BCD OUT 1K
BCD OUT 2K
BCD OUT 4K
BCD OUT 8K
BCD OUT 10K
BCD OUT 20K
BCD OUT 40K
BCD OUT 80K
BCD OUT 100K
BCD OUT 200K
BCD OUT 400K
BCD OUT 800K

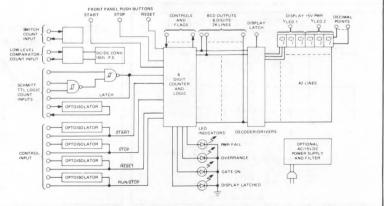


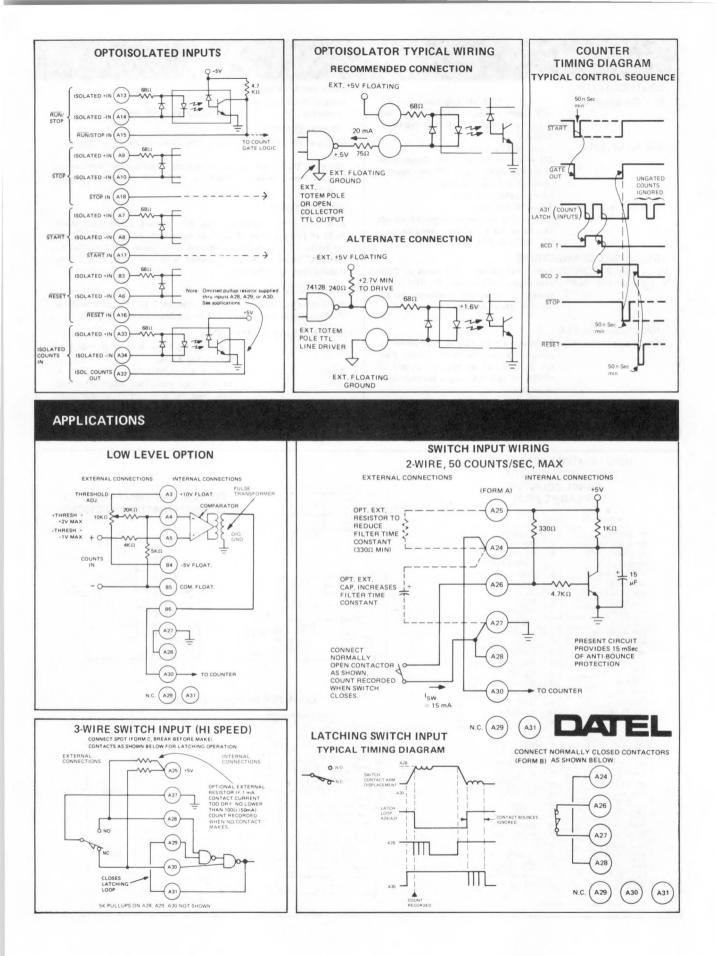
EQUIVALENT INPUT CIRCUITS (SEE APPLICATIONS SECTION)





COUNTER BLOCK DIAGRAM



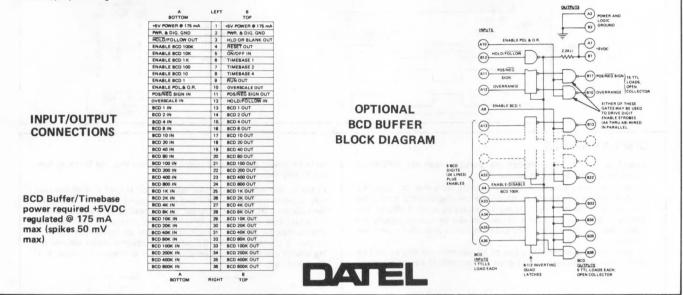


Electronic Design's

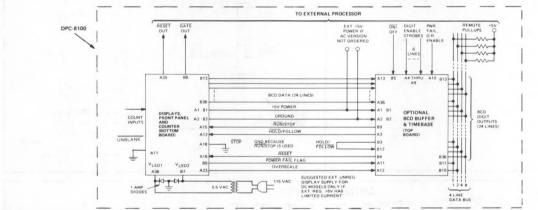
OPTIONAL BCD OUTPUT BUFFER/PROGRAMMABLE TIME BASE

A second PC board mounted in the upper card slot is available with the DPC-8100 Counter. This second board can contain a latchable, gatable BCD output buffer and/or a high-accuracy crystal-controlled timebase generator. The timebase produces count gates which are pin-selectable from 10 μ S to 10 seconds in decade steps. Overall accuracy of the timebase is ±50 ppm ±50 nanoseconds (0 to +50°C).

The BCD Buffer and Timebase allow for storing and transmitting count outputs, for frequency, period or tachometer counting modes and for several display viewing modes.



TYPICAL DATA TRANSMISSION APPLICATION



This block diagram shows the optional BCD Buffer and Timebase connected to the DPC-8100 Counter to create a complete data bussing system. This system utilizes a 4-bit, open-collector TTL data bus which is compatible with most microprocessors and minicomputers. By grouping appropriate DIGIT ENABLE STROBE lines, 8-Bit, 16-Bit or full parallel data transmission can be used for higher speeds.

This application shows all 6 BCD digits multiplexed onto 4 lines using bit-parallel, digit-serial format. The power fail and overscale flags are also multiplexed as a 2-bit 7th word after the (6) 4-bit BCD words. Six enable lines successively multiplex the open collector BCD digits and a seventh enable (A10) multiplexes the power fail and over range flags.

TIMEBASE OPTION

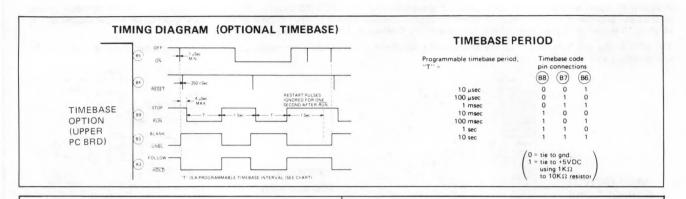
The timebase option produces a \overline{RUN} pulse of precise duration controlled by a crystal oscillator. The overall timing accuracy is \pm 50 ppm \pm 50 nSec over 0 to \pm 50°C. This \overline{RUN} pulse may be initiated asynchronously at any time by the \overline{ON}/OFF control (B5). The RUN pulse is normally connected to the RUN/STOP control (A15) of the counter to gate in external counts during accurately measured intervals. This mode of operation allows the counter to be used as a frequency meter, tachometer or digital integrator.

After each fixed length $\overline{\text{RUN}}$ pulse, a one second viewing pause is generated during which external counts are locked out and the display shows the last group of accumulated counts.

The fixed length $\overline{\text{RUN}}$ timebase pulse can be started at any time or the $\overline{\text{ON}}/\text{OFF}$ control may be held LO continuously to give a repeating series of $\overline{\text{RUN}}$ pulses followed by one second viewing intervals.

The length of the RUN timebase pulse is programmable using a 3 bit code wired to rear connector pins B6, B7, and B8. Timebase periods may be selected from 10 microseconds to 10 seconds (see chart).

A 250 nanosecond RESET pulse is issued just before the RUN pulse to clear the counter to zero. Complementary BLANK and FOLLOW/ HOLD outputs are also issued for display and BCD buffer control (see Display Modes description).



DISPLAY MODES

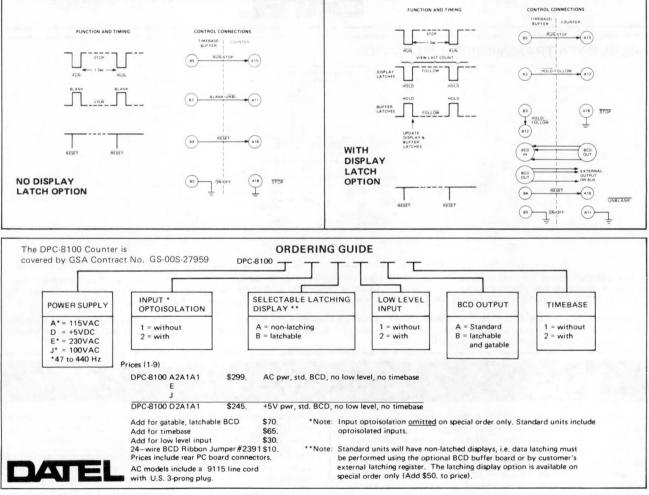
Several display viewing modes are possible with the DPC-8100 counter and timebase/buffer option.

In the first mode when the display latching feature is not used, the blanking line is connected to illuminate the display only during the one second viewing period. During the counting interval (RUN), the display is blanked to avoid confusion caused by counts rapidly accumulating on the display. The Gate On light shows that counts are accumulating.

In long timebase applications (up to 10 seconds) the display will be illuminated one second out of every 11 seconds. If counts are accu-

mulated slowly and the user wants to observe this, the blanking line can be left disconnected.

In the second mode, the display latch option is used so that the display is never blanked. At the end of the count interval, the display (and optional BCD buffer latches) are updated (unlatched) to follow the count now stored in the DPC-8100 output register. After the one second viewing period, this count is stored in the latches and the counter is cleared by a RESET pulse. The counter begins accumulating counts again while the previous count is displayed. The display is never blanked.





6-DIGIT, PANEL-MOUNT TIMER/STOPCLOCK

MODEL DSC-8200

FEATURES

- ► 6-Digit timing ranges available from 999999 µSec to 999:59.9 Hrs./Min
- Bright 0.6" high (15 mm) LED displays
- High accuracy event or interval timer or period meter with full parallel BCD outputs
- Use with 8400-series comparators to form preset timers for process control
- Accepts switch contact or logic control
- Optional stored BCD outputs can be gated or multiplexed onto a data bus

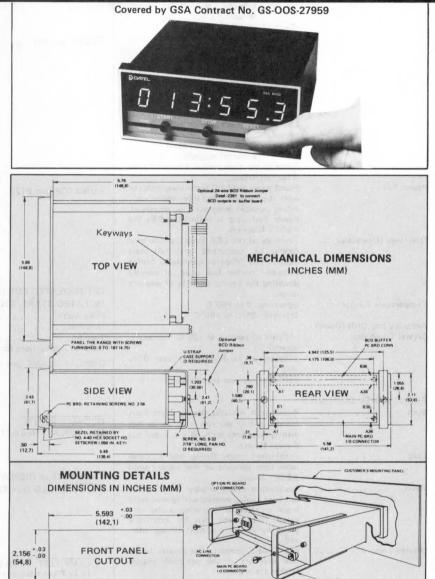
DESCRIPTION

The model DSC-8200 Digital Stop Clock is a general purpose count-up timer using allelectronic timing and display. A host of expandable systems features allow the user to progress from a simple hand-operated Stop Clock to a complete minicomputer data-buscompatible period measuring instrument. Yet, the DSC-8200 retains the small size and appearance of other panel-mounting instruments in Datel's 8000 series.

All DSC-8200 models have time displays consisting of six Light Emitting Diode (LED) 7-segment digits 0.6 inches (15 mm) high. A leading zero suppression control allows right-justified display of time periods less than six full digits. Five basic display formats using one or two colons or no colons, provide an extremely wide choice of full scale time ranges covering hours, minutes, seconds, milliseconds or microseconds, (See chart, Page five) An accurate, stable quartz crystal timebase is standard on all units providing ± 10 ppm maximum drift over the 0 to $\pm 50^{\circ}$ C operating temperature range. The user may select the optional 50 or 60Hz AC line timebase which provides very high long term accuracy periodically corrected by power utilities. The AC line timebase may be used with the +5VDC-powered versions of the DSC-8200 as well as 100, 115 or 230 VAC line-powered versions. Front panel pushbuttons control the start, stop and reset functions of the DSC-8200 but for high speed, high accuracy event tim-ing or automatic control, these functions are duplicated by rear connector logic inputs. These logic inputs accept digital commands from TTL/DTL compatible logic devices or from Form A or B Switch contacts. The switch contact inputs may be used for remote single or multiple station accumulated time functions as well as position or cam-operated limit switches.

Special care was taken in the DSC-8200 design to eliminate timing errors due to electrical or logic noise. The instrument is fully enclosed in a rugged shielded aluminum housing. The regulated AC power supply uses a bifilar-wound choke to filter line noise and all control inputs employ Schmitt level-sensitive logic (not edge-sensitive). Optional input optoisolation provides further immunity to digital noise or for use with floating AC inputs.

Full parallel, binary-coded-decimal (BCD) 1-2-4-8 outputs of the displayed time period



are provided on the rear I/O connector. These logic outputs have TTL/DTL levels and may be externally connected to an optional BCD Buffer board which fits in the top PC board slot. The BCD Buffer option will store one full output of the accumulated time and will transmit this data on external command in full parallel or in groups of 4 bits at a time.

The BCD Buffer provides storage and gating to asynchronous open-collector TTL data busses used on most main frame processors, minicomputers and microprocessors. A processing system can automatically poll the DSC-8200 to transmit its data as part of the instruction program of a complete control system.

Many other systems features are incorporated in the DSC-8200. These include power failure and overscale indicators and outputs. Optional display latches let the user view one time period while the next timing interval is counting. This feature is useful for short, high-speed measurements such as period meters requiring longer display viewing times.

SPECIFICATIONS (Typical @ +25°C unless noted)

如何的"你是是 ^{我们} 你们,我们们们们就			
GENERAL Displays	Six (6) self-illuminated digits, red LED 0.6″ (15 mm) high, 7-segment format.		(Note: START and STOP form an RS latch circuit. The last input to be LO determines the latch state.)
Eull Saala Tima Dangas	Replaceable displays are mounted on in- dividual sockets. (Type 1) 999:59.9 (center colon)	STOP (pin A6)	1 line, 1 TTL load plus $4.7 K\Omega$ pullup to +5V. Timing stops on falling edge of LO
Full Scale Time Ranges	minutes (Type 2) 99:59:59 (2 colons)		pulse, 50 nsec minimum width. Ground STOP if using the RUN/STOP INPUT. Time is held after STOP until cleared to
	hours: minutes: seconds (Type 3) 99:59.99 (left colon)	RESET (pin A5)	zero by RESET. 1 line, .75 TTL loads plus 4.7KΩ pullup to +5V. Schmitt level-sensitive input.
	minutes: seconds or hours: min (Type 4) 999999 (no colons includ- ing programmable left-of-digit		Negative-going threshold +0.9V. Positive-going threshold +1.7V.
	decimal point) Least significant digit is 1, 10 or 100 μ S, 1, 10 or 100mS, 1 Sec, or 0.1 minute.		LO: Falling edge of RESET LO pulse jams time at all zero's but does not affect the START-STOP latch. A
	LSD's are user-selected on rear I/O con- nector. (Type 5) 9999:59 (right colon)		START LO pulse may be stored but will be inhibited until RESET goes HI. Minimum RESET LO
	minutes: seconds Refer to the time format charts on page 5 for full details.		pulse width is 50 nsec. HI: START or STOP functions may be stored and enabled.
Power Fail	Front panel red LED lamp illuminates to warn if power has been interrupted, indi- cating possible incorrect time displayed. Power Fail lamp is extinguished by the	RUN/STOP (pin B12)	1 line, 1 TTL load plus 4.7KΩ pullup to +5V. Gnd. pin A6 when using RUN/ STOP, Float RUN/STOP if not used. HI: Timing is stopped.
Overrange (Overscale)	RESET function. Front panel red LED lamp illuminates if timing has continued past full scale range. The display continues timing	1.1.	LO: Timing in progress. (Schmitt level-sensitive input) Positive-going threshold +1.7V. Negative-going threshold +0.9V.
	through another full scale, effectively doubling the timing capacity of any one range.	OPTOISOLATED CONTROL	. INPUTS
Temperature Ranges	Operating: 0 to +50° C Storage: -25° C to +85° C	Pulse width	
Accuracy and Drift (Quartz Crystal Timebase)	$\pm 10 ppm$ of reading @ +25 $^{\circ} C$ (Initial Accuracy)	Isolation	300 Volts, RMS 15 mA sink ing details
	±10ppm of reading (Drift over 0 to +50°C) ±10ppm (one year crystal aging)	DISPLAY BLANK (pin A36)	1 line, I _{IL} = 5 mA (sink), I _{IH} = 0 @ +2.5V _{IN} , = 6.25 mA @ 5V _{IN} HI (float or cutoff open collector TTL)
FRONT PANEL CONTROL	S	and the second	= Blank Display
Start	Pushbutton initiates timing. Hold Start button in two seconds or longer to test display segments with all 8's. Does not	DECIMAL POINTS (pins A25, A27 thru A31)	LO or GND = illuminate display 6 lines, ground LO to illuminate cor-
Stop	disrupt timing. Pushbutton stops timing and accumu- lated time remains on the display until		responding left-of-digit decimal point (see I/O connections). 16 mA sink (10 TTL loads) for logic drive.
Reset	RESET occurs. Pushbutton clears display to all zero's,	LAMP TEST or DISPLAY FOLLOW/HOLD (pin B3)	1 line
	but next timing interval will immediately begin unless STOP function is also acti- vated (instrument can be externally wired to inhibit the next timing inter- val).		This input will test the display with all 8's if the latchable display option is not included. With the display latch option, this input stores a displayed time until updated, but the lamp test is not avail-
Display Test	See START control. The display test is not available if the optional display latches are ordered.	1. LAMP TEST, sink 9.6 m/ HI or Float = lamp test dis	able. A (6 TTL loads) sabled.
DIGITAL INPUTS All digital inputs are compati	ble with DTL/TTL logic sources:	LO or GND = lamp test en 2. DISPLAY FOLLOW/HOL HI or Float - display will la	D; sink 2.4 mA (1.5 TTL loads)
"ZERO" 0V ≤ LO ≤ +0.8V "ONE" +2.0V ≤ HI ≤ +5.0V		LO or GND = display will FOLLOW pulse width m	follow time inputs. ust be 100 nS minimum if input time is
All control inputs are level s dynamic inputs must use TTI START (pin B11) •••••	1 line, 1 TTL load plus 4.7K Ω pullup to +5V. Timing begins on falling edge of	BASE IN falling edge). T	nsec minimum after the COUNT TIME- The FOLLOW update latch pulse must be ne falling edge of COUNT TIMEBASE IN am.
	LO pulse, 50nsec minimum width. RE- SET must be HI to enable start of tim- ing. START LO pulse will be stored if	TIMEBASE INPUTS AC SINE WAVE SYNC	
	RESET is LO but will not be enabled until RESET goes HI.	(Pin B8)	1 line, ${\simeq}500\Omega$ to GND, to provide an AC timebase reference when used with

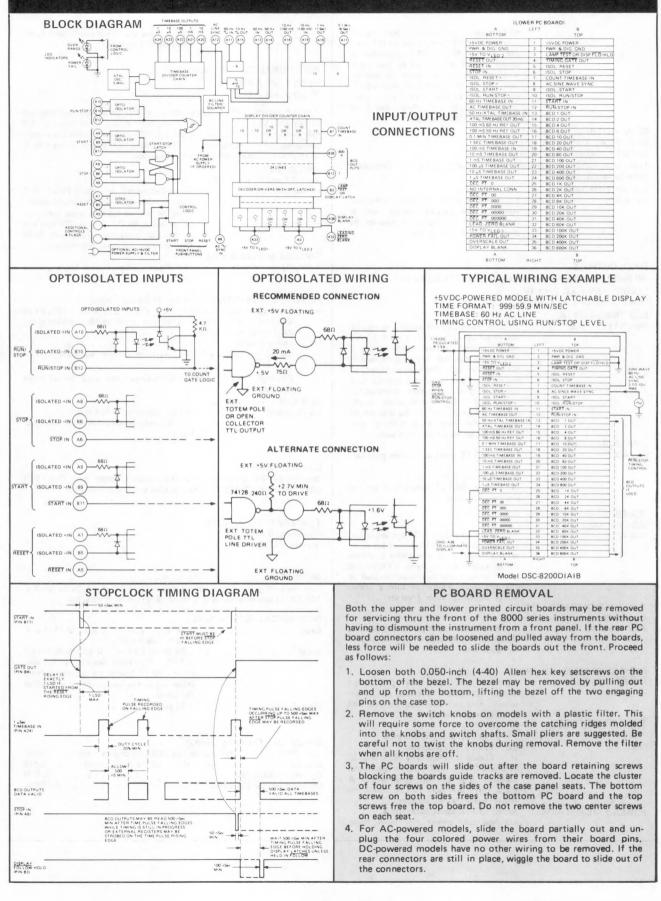
DATEL

SPECIFICATIONS (Cont'd)

ca ut po wi tic ca us	5V powered units with a least signifi- int digit of 100 mS, 1 sec or 0.1 min- te. 3V to 10V RMS, referenced to ower ground at 50 or 60 Hz. Internally ired on AC models, make no connec-	rupted, time may be invalid. Clear to HI when RESET occurs. ADDITIONAL CONNECTIONS
po wi tic ca us	ower ground at 50 or 60 Hz. Internally ired on AC models, make no connec-	ADDITIONAL CONNECTIONS
tic ca us		
us	on. Do not use pin B8 for least signifi-	V _{LED 1} (pin A33) V _{LED 2} (pin A3)
	ant digits less than 100 mS or when sing the crystal timebase. See note	
	nder "AC TIMEBASE OUT."	$V_{LED 1}$ supplies +5V display power to the three left digit display LED's and $V_{LED 2}$ is for the three right digits. Each input is 300
60 Hz TIMEBASE IN (pin A11) 50 Hz/XTAL TIMEBASE IN (pin 100 mS TIMEBASE IN (pin A19	in A13)	mA maximum +5VDC. Do not use on AC-powered models (internally connected). For DC models, the +5VDC may be full wave DC rectified, or +5VDC regulated 300mA each connection.
	jumpered for AC or crystal timebases.	+5VDC POWER
Refer to format charts.		(pins A1 and B1 internally
COUNT TIMEBASE IN		connected) On DC-powered models, +5VDC @ 1
ing tag	line, 1 TTL load. This line is the clock put to the display counter and is pped from the timebase counter as own in the format charts.	Amp regulated (50 mV maximum spikes) must be connected on these pins. On AC-powered models, up to 200 mA out at +5VDC regulated is available from
		these pins for optional external use.
		GROUND (pins A2 and B2
DATA OUTPUTS	a with DTI /TTI logic lough	internally connected) +5V Power, Display and Logic ground return.
All digital outputs are compatible "ZERO" = $0V \le LO \le +0.4V$.	e with DTE/TTE logic levels:	returli.
"ONE" = +2.4V ≤ HI ≤ +5.0V.		POWER REQUIREMENTS (See Ordering Guide)
BCD TIMING DATA		AC – powered models: Choice of 100, 115 or 230 VAC, ±10%, 47 to 440 Hz, 10 watts typical. Line freq. must be 50 or 60 Hz if the
	4 lines, consecutively spaced in ascend-	AC line timebase is used.
	g order. Full parallel 1-2-4-8 binary oded decimal (BCD). Positive true, 7	DC – power models:
	TL loads per line, totem pole format	Logic: +5 ±0.25 VDC @ 1 Amp maximum regulated, 50 mV
	rives HI or LO). Digits immediately to	max, spikes, Display: +5VDC @ 600 mA maximum regulated or full wave
	ne right of a colon only count up to 5 bits 1, 2, & 4) but vacant terminals for	rectified DC.
	e unused BCD "8" bits occur on the	BCD Buffer (optional up-
wi	nout sequence. Interfacing equipment ill usually require grounding cor- sponding unused input terminals.	per PC Board) +5VDC regulated @ 175 mA. (See separate specifications for the BCD Buffer)
OVERSCALE OUT		
	line, 10 TTL loads out, totem-pole for- at.	CONNECTORS
	I = Time exceeds full scale.	Dual 36-pin PC edgeboard type 0.1" centers, solder tabs, Datel P/N
	D = when $\overrightarrow{\text{RESET}}$ occurs or if time is ss than full scale.	2597-14 (Viking 3VH36/1JN-5) included with instrument.
TIMEBASE OUTPUTS		
AC TIMEBASE OUT (pin A12) 1	line, provides TTL-compatible,	TEMPERATURE RANGES Operating: 0 to +50° C
sq	quared-up 50 or 60 Hz pulses for input to the timebase counter chain as shown	Storage: -25° C to +85° C
	the format charts. Note: START and	
	TOP circuits are not synchronized to he AC lines. Therefore timing uncer-	MOUNTING
	ainty will be $\pm 1/50$ or $1/60$ sec.	Panel-mounting through a cutout measuring 2.16"H \times 5.59"W (54,8 \times 142,1 mm) and secured by 2 U-straps. See mounting diagram.
(pins A15 thru A18 and	line each totam rale Connect of	MECHANICAL DIMENSIONS
sh	line each, totem-pole. Connect as hown in the format charts for desired ull scale time.	Case
		Bezel
DIGITAL CONTROL OUTPUTS		filter, and PC boards are removable from
01	line, 10 TTL loads, totem-pole. Logic utput of RESET function, can be ex- ernally tied to STOP input to clear and	front while the unit remains secured in the panel.
	hibit further timing.	Weight 2.25 pounds (1,0Kg)
TIMING GATE OUT		
	line, 10 TTL loads, totem-pole. O = Timing is in progress.	PRICE (See Ordering Guide)
	U = Timing is in progress. II = Timing is halted. The rising edge of	DSC-8200 +5V power, std. BCD, no display latch \$269
T	IMING GATE OUT inhibits the crystal	DSC-8200 AC power, std. BCD, no display latch \$299 Optional BCD Buffer
	scillator gate counter chain input. A major carry will take 500 nS maximum	Optional latchable displays Add \$50
	o propagate thru all decades.	
POWER FAIL (pin A34) . 1	line, 10 TTL loads, totem-pole. O indicates power has been inter-	

Т

DSC-8200 BLOCK DIAGRAM



APPLICATIONS

TIME FORMATS

Rear Connector Timebase Wiring

Center colon (999:59.9 min/sec or hrs/min display) Models DSC-8200 _1_

Display Full Count and Timebase	Timebase Jumpers	Dec. Pt.	LSD Jumper
999:59.9 min/sec crystal timebase	A13-A14	Gnd. A25	B7-A16
999:59.9 min/sec 50 Hz timebase	A12-A13	Gnd A25	B7-A16
999:59.9 min/sec 60 Hz timebase	A11-A12	Gnd A25	B7-A15
999:59.9 hrs/min crystal timebase	A13-A14 A16-A19	Gnd A25	B7-A17
999:59.9 hrs/min 50 Hz timebase	A12-A13 A16-A19	Gnd A25	B7-A17
999:59.9 hrs/min 60 Hz timebase	A11-A12 A15-A19	Gnd A25	B7-A17

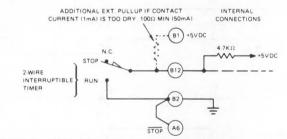
Two colon (99:59:59 hrs/min/sec display) Models DSC-8200 _2__

Display Full Count and Timebase	Timebase Jumpers	LSD Jumper
99:59:59 hrs/min/sec crystal timebase	A13-A14 A16-A19	B7-A18
99:59:59 hrs/min/sec 50 Hz timebase	A12-A13 A16-A19	B7-A18
99:59:59 hrs/min/sec 60 Hz timebase	A11-A12 A15-A19	87-A18

Left colon (99:59:59 hrs/min/sec display) Models DSC-8200 _3_ _

Displays Full Count and Timebase	Timebase Jumpers	Dec. Pt.	LSD Jumper
99.59.99 min/sec crystal timebase (can't use 50 or 60 Hz timebases)	NONE	Gnd A27	B7-A20
99:59.99 hrs/min (Xtal, no 50/60)	A20-A19	Gnd A27	B7-A17

LIMIT SWITCH OR CAM-CONTACTOR WIRING



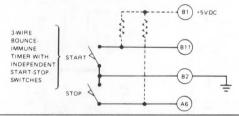
Models DSC-8200 4 Timebase Jumpers LSD Jumper Display Full Count 50 Hz 60 Hz Dec. Pt. Xtal 999999 sec Gnd B7-A24 None can't can't use use 431 9 99999 sec B7-A23 None can't can't Gnd A30 use use 99 9999 sec None can't can't Gnd B7.422 A29 Sec use use 999.999 sec None Gnd A28 B7-A21 can't can't use use 9999.99 sec None Gnd B7-A20 can't can't A27 use use 99999.9 sec A13-A14 A12-A13 A11-A12 B7-A19 Gnd A25 A13-A14 A12-A13 A11-A12 999999 sec RH Dec. 87-A18 A16-A19 A16-A19 A15-A19 Pt. not Available 99999.9 min A13-A14 A12-A13 A11-A12 Gnd B7-A17 A16-A19 A16-A19 A15-A19 A25 Min 9999 99 min B7-A17 A20-A19 can't can't Gnd use use A27 999.999 mS Gnd A28 B7-A24 None can't can't use use 9999.99 mS B7-A23 None Gnd can't can't A27 use use mS B7-A22 99999.9 mS None can't can't Gnd A25 use use 999999 mS None can't can't RH Dec B7-A21 use Pt. not use Available 999999 µS None can't can't RH Dec. B7-A24 μS use use Pt. not Available

Right colon (9999:59 min/sec display) Models DSC-8200 _5__

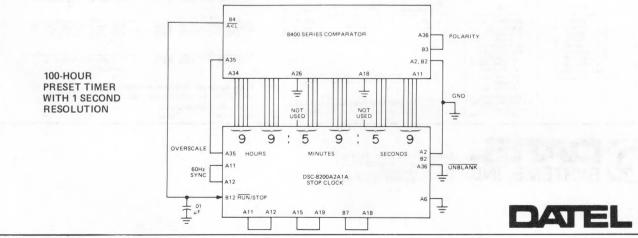
No-Colon Decimal (999999 display)

Display Full Count and Timebase	Timebase Jumpers LSD Jumper	
9999:59 min/sec crystal timebase	A13-A14 A16-A19	B7-A18
9999:59 min/sec 50 Hz timebase	A12-A13 A16-A19	B7-A18
9999:59 min/sec 60 Hz timebase	A11-A12 A15-A19	B7-A18

The suggested circuits shown here illustrate typical applications. Datel cannot warrant the performance of these circuits or their possible patent status by other manufacturers.



This diagram shows a 100 hour capacity count-up timer using a Datel model DSC-8200 stopclock and Datel 8400 Series Comparator. Front panel controls start and stop the DSC-8200. Logic controls can be wired to stop timing and hold at the preset time or clear to zero and stop or to clear and start timing. Note that bits BCD 800 (A18) and BCD 80K (A26) are grounded LO since the count in those decades doesn't exceed 5.



GOLD BOOK 76/77

OPTIONAL BCD OUTPUT BUFFER/STORAGE REGISTER

An optional BCD Buffer/Storage Register is available with the DSC-8200 Stopclock. This Buffer printed circuit board mounts in the upper card guides inside the DSC-8200 housing. The BCD Buffer/Storage Register allows for storing accumulated timing intervals and for transmitting this data to an external instrument such as Datel's 8400-series comparators or a computer data bus.

comparators or a computer data bus. Full parallel timing data is user-wired externally from the top pins of the bottom connector to the underside pins of the top connector. A Datel 24-wire ribbon jumper (Model 2391, \$10, singles) offers a convenient connection method between the two rear connectors. On external command through the hold/follow latch input (pin B12) the buffer will store one full parallel data word (26 lines total) with less than one microsecond acquisition time. A second group of external commands (the digit strobes, pins A4 through A10) enable the open collector output gates. These gate strobes are organized in 4-bit BCD groups so that output gating can be multiplexed in 4-bit multiples onto 4, 8 or 16-wire TTL data busses or 26-wire full parallel. The uncommitted open collectors accept up to 5 TTL loads for wide compatibility to mainframe processors, minicomputer or microprocessor data busses. Gating on or off is less than one microsecond using standard TTL loading and short leads. Cable reactance will lengthen this gating time. Logic levels are compatible to 7400-series TTL logic gates. The open collector format allows multiplexing the DSC-8200 outputs along with other instruments sharing the same bus.

OPTIONAL BCD BUFFER INPUT/OUTPUT CONNECTIONS (TOP PC BRD)

POWER REQUIRED FOR BCD BUFFER: +5V ±0.25VDC @ 175mA, LOGIC NOISE 50mV MAX.

PERIOD METER APPLICATION

The DSC-8200 is easily connected to operate as a period meter. This particular circuit uses a few external components and a floating analog comparator, part number 2543, available from Datel. The comparator is the same circuit used on Datel's model DPC-8100 Counter and includes a DC/DC converter for 300V RMS isolated operation. An external potentiometer is adjusted to set the triggering threshold (– 1V to + 2V threshold range).

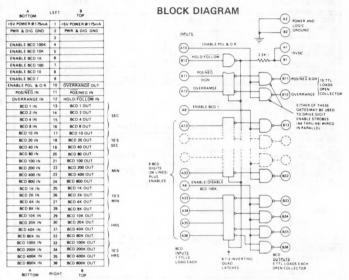
After the 555 viewing gate timer resets the previous timing and both control flip flops, the next positive-going threshold crossing starts the timing.

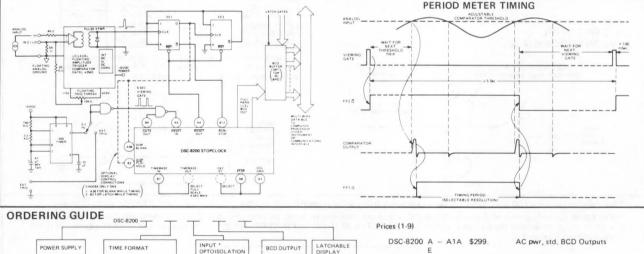
Timing stops on the next following threshold crossing. The control flip flops lock out restart triggers and the timed period is displayed for the remainder of the five second viewing pause.

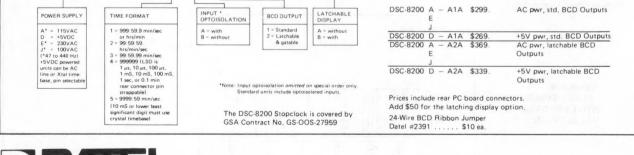
The DSC-8200 is by no means limited to this type of period timing. By selecting timebases, periods from microseconds to hours may be measured. The display may be blanked or latched and a different external circuit may be designed for full synchronous period timing triggered by the analog waveform. Complex waveforms may be measured for pulse widths or time between pulses.

PERIOD METER

Asynchronously triggered with 5 Second Viewing Pause









1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

Vol 3/216



6-DIGIT, PANEL MOUNT DIGITAL TIME CLOCK

MODEL DTC-8300

FEATURES

- Bright, long-life 0.6 inch high (15 mm) LED displays
- Full parallel TTL/DTL compatible BCD data outputs – optionally latched and gated.
- Choice of power supply: AC line or +5VDC.
- Both AC line frequency or crystal controlled time base are built in.
- Choice of 12, 24 or 100 hour displays.

DESCRIPTION

The Model DTC-8300 displays the time of day in hours, minutes and seconds in 12 or 24 hour formats on .6'' (15 mm) high LED digits. The panel mounting instrument features digital logic outputs of the displayed time for use in data logging systems and time-controlled automatic process systems.

The 12 and 24 hour time formats have two colon and one colon display modes respectively. The 12-hour format carries on 12:59:59 to 1:00:00 and the 24-hour version carries from 2359:59 to 0000:00. These modes are customer wired on the rear PC board connector. However, the left colon may be blanked or illuminated on any model. A 100 hour carry may also be connector-wired.

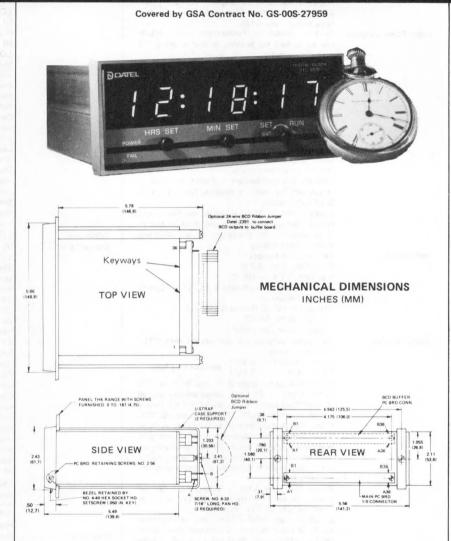
Power required for the DTC-8300 is 100, 115 or 230 VAC at 50 or 60 Hz or +5 volts DC at 1.5 Amps max.

The timebase for the clock is available from an internal quartz crystal oscillator supplied on all units or from a choice of 50 or 60 Hz AC line frequencies.

The line frequency timing reference may also be used on +5VDC powered units for long term accuracy periodically corrected by power utilities. AC line powered versions contain their own internal +5VDC regulated supply and 100mA at +5VDC may be tapped for external use.

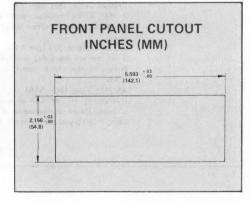
The DTC-8300 is housed in a black anodized aluminum case measuring 5.562''wide x 2.125'' high x 5.467'' deep (141 x 54 x 139 mm). The clock is mounted through a front-panel cut out and secured by two U-straps. The grounded case acts as shielding for the clock circuitry and additional power line filtering is provided by a bifilar-wound choke and bypass capacitors.

All displayed digits have a corresponding set of digital logic outputs available at the rear connector. These outputs are in full-parallel standard binary coded decimal form (BCD) with TTL/DTL compatible logic levels. Standard BCD versions have a HOLD input which stabilizes the output for one second minimum (2 sec. max. synchronously) for readout by an external device. This "HOLD" function stores one clock pulse during the 2 second read interval and reinserts this pulse so as not to disrupt timing accuracy.



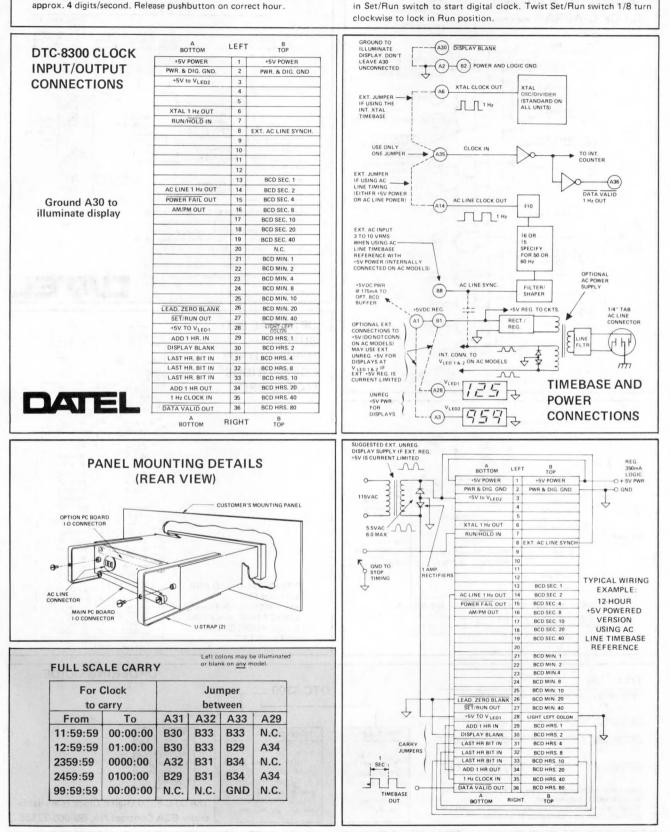
An AM/PM logic output for 12-hour versions may be used for data logging applica, tions. A "power fail" front panel LED lamp and corresponding logic output is set whenever power is momentarily interrupted, indicating to an external device that the time may be invalid. Resetting the clock using the front panel controls will extinguish the "power fail" lamp and flag.

An optional second PC board provides fully latched and gated BCD capability so that a clock word may be stored and transmitted at any time on external command. Gating is open collector TTL/DTL-compatible and gatable by individual digit These digits may be multiplexed onto 4 or 8 line data busses as well as transmitted in full parallel.



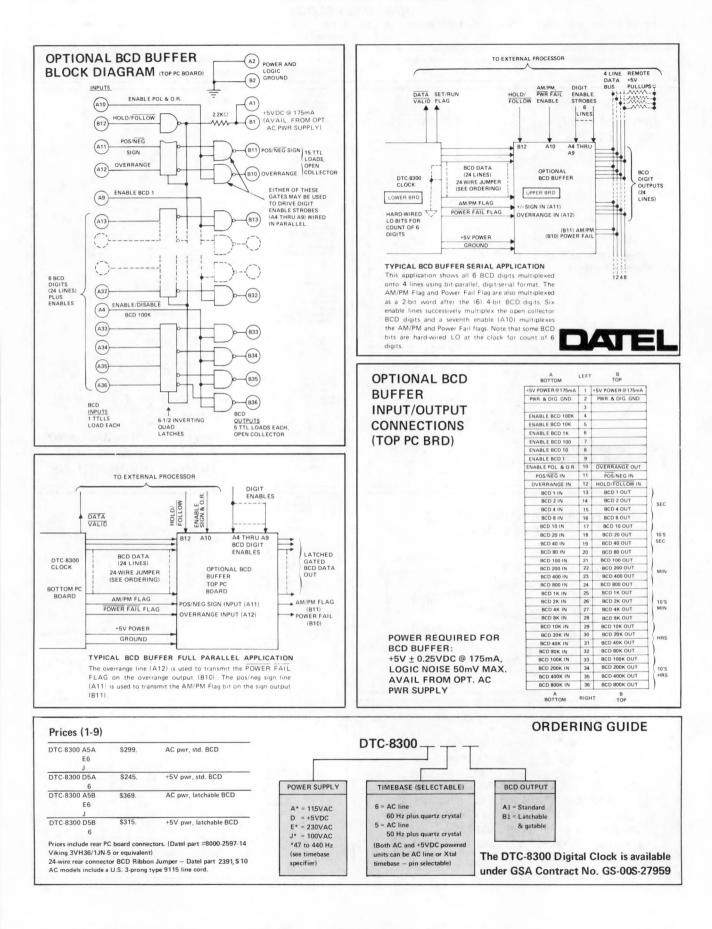
SPECIFICATIONS (Typical @ +25°C unless noted)

GENERAL			Set/Run Output (pin A27) - 1 line, switch
Displays	Six (6) self-illuminated digits, red LED 0.6"		contact to ground with 4.7K ohm pullup to
	(15 mm) high, 7-segment format.		+5V.
	Full scale readouts (with LED colons):	Same Same	GND - Clock is being set, BCD outputs are
	12:59:59 (HOURS:MINUTES:SECONDS) 2359:59 (HOURS MINUTES:SECONDS)		invalid. HI — Clock is running if Run/Hold (A7) is HI.
Power Fail	Front panel red LED lamp illuminates to warn	Digital Inputs	All digital inputs are compatible with DTL/
	if power has been interrupted, indicating pos-		TTL logic levels.
	sible incorrect time displayed. Corresponding		$LO = "ZERO" \leq +0.8V$ positive true logic
	logic output (pin A15).		HI = "ONE" ≥ +2.0V { positive true logic
Front Panel Controls	Set/Run Switch - (Pushbutton switch which		Run/Hold (pin A7) – 1 line, 1.6 TTL loads
	can be locked by pushing in and rotating 1/8		HI – Clock is running.
	turn clockwise). "Run" Mode (pushbutton in) – Clock is run-		LO – BCD outputs stabilized. May be held 1 sec. max. asynchronous to Data
	ning. Hours and minutes set pushbuttons (see		Valid output without disrupting timing. (Saves
	below) are disabled.		one pulse which is reinserted when HOLD is
	"Set" Mode (pushbutton released out) - Clock		released) Hold longer than 2 seconds disrupts
	is stopped. Hours and minutes set pushbuttons		timing. (See timing.) 1.6 TTL loads.
	are enabled. Seconds display will be stopped at		Clock In (pin A35) – 1 line, accepts 1 Hz
	the current:00 to :59 count.		pulses from Crystal Clock (A6) or AC Line Clock (A14) 1 TTL load
	Hours Set Pushbutton – Push in to set hours if Set/Run Switch is in "set". Push in will cycle		Clock (A14). 1 TTL load. Leading Zero Blank (pin A26) – 1 line, LO
	hours display at approx. 4 digits per second.		blanks the leading zero. 1 TTL load.
	Release on desired hours.		Display Blank (pin A30) – 1 line, HI blanks
	Minutes Set Pushbutton - Functions same as		display. 3 TTL loads. Works from jumper, open
	Hours Set for minutes display. [See "How to		collector, totem pole TTL, or DTL. Must sink
	Set Clock" section]		5mA pullup. Colons remain illuminated while
	Display Test – Hold in both the hours and		display is blanked. Must ground for normal
	minutes set pushbuttons at any time to test all	A 1 11	operation.
	digit segments by displaying all 8's. Will not disrupt clock timing.	Additional	LIGHT LEFT COLON (B28) Gnd. to light
Performance	Temperature Ranges	Connections	V _{LED} 1 (pin A28) Each input connects +5V V _{LED} 2 (pin A3) power to 3 display digits.
	Operating: 0 to +50° C		550mA max. @ +5VDC each connection. In-
	Storage: -25° C to +85° C		ternally connected to +5V power on AC
	Accuracy and Temperature Drift - (Quartz	1. A.	models.
	Crystal Timebase)		+5VDC POWER (pins A1 & B1 in parallel) -
	± 10 ppm @ $\pm 25^{\circ}$ C (Initial Accuracy)		These pins are for +5VDC logic power input
	±10ppm (0 to +50°C) +10ppm (one year aging)		on +5V-powered units, 400mA max. On AC-
Digital Outputs	±10ppm (one year aging) All digital outputs are compatible with DTL/		powered models, output of +5VDC power @
engitar ou tputs	TTL logic levels		275mA max, is available from these pins. Not
	$10 = "7 EBO" \le +0.4 V$)		internally connected to displays on DC models. (Use V _{LED} 1 & 2 for displays.)
	HI = "ONE" $\geq +2.4V$ positive true logic		Power and Logic Ground (pins A2 & B2 in
	BCD Clock Data (pins B13 thru B36, see I/O		parallel) +5V power return for display and logic.
	connections) - 24 lines, consecutively spaced	1 m m m m m m m m m m m m m m m m m m m	Carry Controls (pins A29, A31-A34) - For
	in ascending order. Full parallel 1-2-4-8 binary		selecting 12, 24 or 100 hour full scale carries
	coded decimal (BCD). Positive true, 6 TTL loads, totem pole format (drives high or low)		(see chart).
	Note: Tens of seconds and tens of minutes only		Ext. AC Line Synch. (pin B8) - 1 line, to
	reach 5 count, but vacant terminal location for	a sugar	provide an AC timebase reference when used with +5V powered units. 3V RMS to 10V RMS
	"8" bit occurs in sequence. Interfacing equip-		input, referenced to power supply ground, 50
	ment may require strapping corresponding ter-		or 60 Hz.
	minal to ground. Power Fail (pin A15) – 1 line LO indicates	Power Supply	Choice of 100, 115, or 230VAC, \pm 10% 10 W
	Power Fail (pin A15) – 1 line, LO indicates power has been interrupted. Cleared to HI by		typ., 47-63 Hz (unless using AC line for timing
	"Set" switch. 10 TTL loads out.		reference). Fuse .15A (100, 115 VAC), .10A
	Data Valid (pin A36) – 1 line, provides squared-		(230VAC) OR +5 ± 0.25VDC @ 1.5A max.,
	up 1 Hz logic output for external clock slave,	Connectors	logic noise 50mV max.
	read functions, etc. BCD valid on falling edge	Connectors	Dual 36 pin PC edgeboard type, 0.1" centers, solder tabs, Datel 2597-14 (Viking 3VH36/
	and while LO. Connected downstream from		1JN-5 or equivalent), (AC power connected by
	AC line or crystal oscillator input (see wiring diagram) 10 TTL loads		triple 1/4" tab, recessed male, center tab case
	diagram). 10 TTL loads. Crystal Clock Out (pin A6) – 1 line, provides		ground) PC Board connectors are included with
	1 Hz, 31.25 millisec. wide crystal oscillator		unit.
	clock pulses to the clock input, pin A35. 1 TTL	Mounting	Panel mounting through a cutout measuring
	load.		2.156" H x 5.593" W (54,8 x 142,1mm) and
	AC Line Clock Out (pin A14) - 1 line, provides	Contraction of the second	secured by 2 U-straps. See mounting diagram.
	1 Hz, square wave AC line-synchronized clock	Mechanical	
	pulses to the clock input, pin A35. 10 TTL	Dimensions	Case 5.56" H x 2.11" H x 5.78" D (141,2 x
	loads.	 Section of the section 	53,6 x 146,8 mm) behind front panel to rear of
	AM/PM Flag (pin A16) – 1 line, alternately transitions HI or LO at carry to 12:00:00	and the second second	U-strap. Bezel 5.86'' W x 2.25'' H x 0.50'' Thk (148,7 x
	o'clock. Reset to desired level by cycling clock	of the second of the	Bezel 5.86" W x 2.25" H x 0.50" Thk (148,7 x 57,0 x 12,7 mm) (See Diagrams) Removable
	using front panel set controls. 10 TTL loads.	Although the second	from front while unit remains secured in panel.
		Market Conference	
		Weight	2.25 pounds (1,0 Kg)
		1 A. A. M. M. M. M.	



HOW TO SET CLOCK

- 1. Release Set/Run pushbutton to "Set". Seconds display will stop at the 3. Push minutes set pushbutton and release on next correct minute current :00 to :59 indication.
- 2. Push hours set pushbutton in and the hours display will advance at 4. Wait until seconds display matches external reference clock then push approx. 4 digits/second. Release pushbutton on correct hour.
- indication



Electronic Design's



PRESET LIMIT DIGITAL COMPARATORS

MODELS DDC-8400 AND DLC-8400

FEATURES

- Front panel lights and logic outputs indicate under, over, between or equal to preset limits selected on thumbwheel switches.
- Two Models: DDC-8400: Two independent

single-channel single-limit com-

DLC-8400: A single-channel, two-limit, 3-zone comparator

- Optional relay outputs control external lamps, motors, pumps, valves, solenoids, etc.
- Compatible with Datel's counters and stopclocks to create mixing/ batching controllers, preset timers, limit alarms, etc.
- Limit tests may be stored and multiplexed onto a data bus.
- Full parallel BCD inputs make rapid limit tests in less than 1 microsecond.

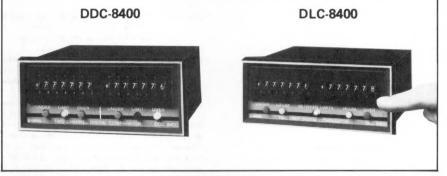
GENERAL DESCRIPTION

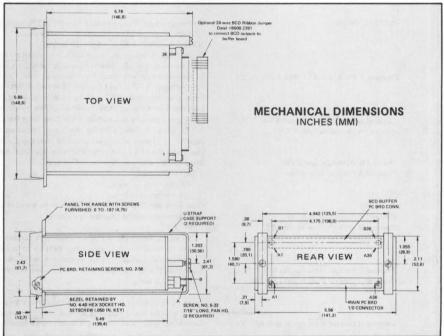
Models DDC-8400 and DLC-8400 are full parallel, high speed digital comparators housed in small aluminum panel-mounting cases. Digital inputs are connected at the rear of the instrument and are compared to bipolar decimal numbers selected on the front panel 6-digit thumbwheel switches. Front panel lights indicate various limit modes and rear connector logic outputs are available to operate other digital instruments or optional relays.

These instruments differ from lower cost count-up comparators (predetermining counters) which require a gated serial input and take longer to determine a comparison. The 8400 comparators have 6 digit resolution with polarity for both the inputs and the preset limits. Separate over scale inputs force an out of limit indication, in the appropriate direction depending on polarity. These comparators are fully algebraic in operation. Comparisons are fully algebraic in operation. Comparisons are fully bipolar so that true 4 quadrant operation is provided. Logic data inputs are full parallel 1-2-4-8 binary coded decimal (BCD) and are compatible to DTL/ITL logic sources. Inputs may be derived from digital panel meters, counters, clocks, timers, test equipment and digital processors.

Applications include: Precision count-up timers, digital setpoint controllers, batching/mixing/sorting controllers requiring a predetermining counter, level or flowrate monitors and alarms. The instruments are ideal for automatic test equipment applications performing component and system check-outs. New test parameters for pass-fail inspection may be quickly dialed in on the front panel limit selectors.

A full set of seven latchable, gatable logic outputs of comparator tests is available on the rear connector. These outputs indicate





the results of any comparison and may be stored and transmitted via open collector data bus to a remote processor upon external command. This bussing arrangement is compatible to most minicomputers and microprocessors. Using this bus, the 8400-series comparators will interface with a remote digital processor, providing limit indications when polled by the processor, yet retaining full manual control of the set-points at the site of measurement.

The digital outputs from the 8400 series comparators may also be rear-wired to an optional internal PC board containing relays. These relays will operate isolated circuits or power actuators, motors, alarm lamps or horns, pumps, valves or solenoids from the AC line. These relays are a choice of either Form C mechanical types with 2 Amp ratings or zeroswitching optoisolated solid state relays. Both types of relays may also be used in pilot service for larger electrical equipment.

The 8400 series comparators are housed in a

black anodized extruded aluminum grounded case for high electrical noise rejection in industrial environments. Power required is a choice of 100, 115, or 230 VAC, 47 to 440 Hz or +5VDC at 400 mA max. Additional power line filtering on AC models is provided by a bifilarwound choke and filtered, regulated power supply.

Two Models

Model DDC-8400 consists of 2 separate singlelimit, single-channel comparators in one case. Each comparator has 3 lights to indicate UNDER/AT LIMIT/OVER limit status of the input compared to the thumbwheel set-point limits selected. There are two sets of 3 lights per channel for 6 lights total. Model DLC-8400 accepts a single input channel and compares it to upper and lower set-point limits selected on two front panel thumbwheel switches. This is a 3-zone comparator with 5 lights indicating whether the input is UNDER/BETWEEN/OVER the LO and HI limits or equal to the LO or HI limits.

SPECIFICATIONS (Typical from 0 to +50°C)

GENERAL	
Function	Digital comparators accepting full parallel binary coded decimal (BCD) logic inputs and comparing them to 6-digit decimal values selected by thumbwheel switches. Comparisons are fully bipolar (4
	quadrant true algebraic with out of limit overscale input).
	DDC-8400: Two independent single-channel, single-limit comparators. DLC-8400: A single-channel, two-limit, 3-zone comparator with assigned LO and HI limits.
Displays	Front panel indicator lights display the status of limit comparisons. The lamps are long-life type 683 incandescent .05 mean spherical candlepower and are replaceable by removing the front panel
	colored lenses. DDC-8400: Each of 2 comparator channels A and B indicates:
	UNDER (Below limit, red lamp)
	AT LIMIT (Equal to limit, green lamp)
	OVER (Above limit, red lamp)
	DLC-8400: The single-channel comparator indicates:
	UNDER LIMIT (Below both limits, red lamp)
	LO LIMIT (Equal to lower limit, yellow lamp)
	BETWEEN LIMITS (Green lamp) HI LIMIT (Equal to upper limit, yellow lamp)
	OVER LIMIT (Above both limits, red lamp)
	Standard lamp lens colors are listed above. Colored lenses may be interchanged on special order
	using red, green, amber, blue, white or yellow lenses. Contact Datel for assistance.
Front Panel Controls	Two set of thumbwheel switches, each with six digits and polarity, are used to manually select limit setpoints. On the 3-zone model (DLC-8400) the lower limit is assigned to the left thumb-
	wheel selector and the upper limit is assigned to the right thumbwheel. Decimal points are not
	included, therefore, significant digits must be coincident with BCD input wiring. (See applications.)
	included, meretore, significant digits must be concluent with bob input wring, toes approxitons.
DIGITAL INPUTS	All digital inputs are compatible with DTL/TTL logic levels:
	"ZERO" = 0V. \leq LO \leq +0.8V) positive true
	"ONE" = +2.0V. ≤ HI ≤ +5.0V logic
	Unused inputs should be grounded LO or wired <u>HI</u> through an internal pullup resistor available on rear connector pin B3. Hold/Follow Latch and Gate Enable Inputs must use TTL rise and fall times.
Channel A Data (pin A11 thru A34)	24 lines, consecutively spaced in ascending order. Full parallel 1-2-4-8 binary coded decimal (BCD). Positive true, 1 TTL load per line. Channel A Data is compared to the left thumbwheel selector limit. Channels A and B must be externally wired in parallel for model DLC-8400 by inserting
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	each input wire through both upper and lower solder tabs.
Channel B Data (pins B11 thru B34) Channel A Overscale (pin A35)	
Channel B Overscale (pin B35)	
Channel A Polarity (pin A36)	
	HI = positive polarity LO = negative polarity
	Channel A and Channel B Polarities must be wired in parallel for model DLC-8400.
Channel B Polarity (pin B36)	Same specifications as Channel A Polarity.
Channel A Hold/Follow In (pin A5)	1 line, 1 TTL load.
	HI stores the results of the last Channel A comparison. Outputs will be stabilized. LO causes Channel A comparison outputs to be updated within 500 nSec of input channel data
	change; outputs will follow comparison decisions. Momentary LO: acts as update clock.
Channel B Hold/Follow In (pin B6)	
Channel A Output Gate Input (pin A6)	 line, 1 TTL load. HI disables Channel A comparison output after the storage circuits. (Output collectors arecut off
	and other devices sharing the same bus lines may pull these lines down.)
	LO enables the comparison outputs after the storage circuits.
Channel B Output Gate Input (pin A8)	
DIGITAL OUTPUTS	All digital outputs are compatible with DTL/TTL logic Max. I _{sink} = 16 mA "ZERO" = 0V. < LO < +0.4V.
	"ONE" = Open coll. output Potential +5.5V
	Note that the comparison outputs are valid when LO (negative true). Logic outputs are open collector.
Channel A A <l (pin="" b4)<="" output="" td=""><td>1 line, 10 TTL loads HI means that the Channel A input is equal to or greater than the left (lower) thumbwheel limit. LO means that the Channel A input is less than the left (lower) thumbwheel limit.</td></l>	1 line, 10 TTL loads HI means that the Channel A input is equal to or greater than the left (lower) thumbwheel limit. LO means that the Channel A input is less than the left (lower) thumbwheel limit.
Channel B B <u (pin="" a7)<="" output="" td=""><td></td></u>	
n a troop back of the back of the	HI means that the Channel B input is equal to or greater than the right (upper) thumbwheel limit.
	LO means that the Channel B input is less than the right (upper) thumbwheel limit.
Channel A A = L Output (pin B5)	1 line, 10 TTL loads
	HI means that the Channel A input is not equal to the left (lower) thumbwheel limit.
States and the second second second second	LO means that the channel A input is equal to the left (lower) thumbwheel limit.
Channel B B=U Output (pin A4)	1 line, 10 TTL loads
	HI means that the Channel B input is not equal to the right (upper) thumbwheel limit.
	LO means that the Channel B input is equal to the right (upper) thumbwheel limit.
Channel A A>L Output (pin B7)	
	HI means that the Channel A input is equal to or lower than the left (lower) thumbwheel limit. LO means that the Channel A input is greater than the left (lower) thumbwheel limit.

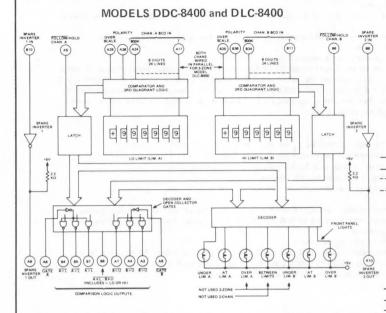
SPECIFICATIONS (Cont'd)

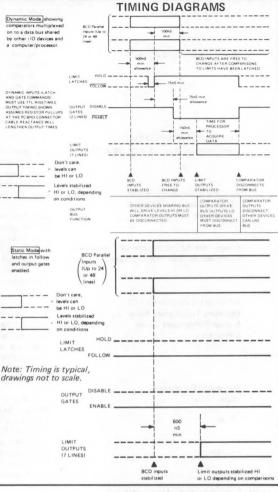
Channel B B>U Output (pin A3)		
	HI means that the Channel B input is equal limit.	to or lower than the right (upper) thumbwheel
	LO means that the Channel B input is higher the	an the right (upper) thumbwheel limit.
(B>U) • (A <l) (pin="" b8)<="" output="" th=""><th>1 line, 10 TTL loads</th><th></th></l)>	1 line, 10 TTL loads	
	This line is provided on both models DDC- and DLC LO on this line for the 3-zone model DLC-8400 i	
and the second	wired in parallel) is between the upper and lowe	
	channels A and B on model DDC-8400 are wired in	the second s
	Note that the "between limits" light on the DLC- limit although pin B8 will be low.	-8400 is dark if the single input is equal to either
the second s	innit artiougi pin bo will be low.	
ADDITIONAL CONNECTIONS	and a second	
Spare Inverters (pins A9, A10, B9, B10)	Two spare TTL logic inverters are available for optional customer use. (A9, Inv. 1 Ou B9, Inv. 2 In;	
	Outputs are open collector with 2.2 Kilohm pull up	
	8 TTL loads out, 1 TTL load in, each inverter.	
Aux. Pullup Resistor (pin B3) +5VDC Power (pins A1 and B1	Spare 2.2 Kilohm resistor connected to +5V for op	otional customer use.
internally connected)	On DC-powered models, +5VDC @ 400mA max.re	egulated input should be connected to these pins.
	On AC-powered models, up to 200mA out at +!	
Ground (pin A2 and B2 internally connected)	optional external use. +5V Power and Logic ground return.	
Power Supply: (See Ordering Guide)	AC powered models: Choice of 100, 115 or 230 V/	AC, ±10%, 47 to 440Hz, 10 watts typical.
	DC powered models: +5 ±0.25 volts DC at 400mA	
	(See separate specifications for optional upper PC r	relay boards)
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0° to +50° C	
Storage Temperature Range	-25° C to $+85^{\circ}$ C C Controls, data, DC power, and relays (lower and u	oper PC boards): Connected by a dual 36-pin PC
Cometors	edgeboard connector for each board, 0.1" centers,	, solder tab terminals, Datel Connector #2597-14
the second se	(Viking 3VH36/1JN-5), included with unit.	
Course and Co	AC Power is connected by a triple '4" tab assembl U.S. 3-prong line cord (P/N 9115) is included with	
Mechanical Dimensions		
Case	5.56 [°] W × 2.11 [°] H × 5.78 [°] D (141,2 × 53,6 × 146,8 mm)	
Bezel	5.86"W × 2.25"H × 0.50" THK	
	(148,7 × 57,0 × 12,7 mm)	
Mounting	Bezel, filter and PC boards are removable from from Panel-mounting through a cutout measuring 2.16"	
	2 U-straps.	
Weight	2.25 pounds (1,0 Kg)	
INPUT/OUTPUT CONNECTIONS		
LOWER PC BOARD (COMPARATORS,		MOUNTING DETAILS
THUMBWHEELS, LATCHES,		MOUNTING DETAILS
GATES AND LIGHTS)		CUSTOMER'S MOUNTING PANEL
80TTOM TOP +5V POWER IN 1 +5V POWER IN	OPTION	IPC BOARD
PWR. & DIG. GND. 2 PWR. & DIG. GND. CH. B B > U OUTPUT 3 AUX. PULL UP	10 CON	NNECTOR
CH. B B - U OUTPUT 4 CH. A A < L OUTPUT	5 593 *03	
CH. A OUTPUT GATE IN 6 CH. B HOLD/FOLLOW IN	(142,1) W (142,1)	
CH. B OUTPUT GATE IN 8 (B > U) + (A < L) OUTPUT		
SPARE INVERTER 1 OUT 9 SPARE INVERTER 2 IN 2.156 SPARE INVERTER 2 OUT 10 SPARE INVERTER 1 IN (54.8)	ACLINE	
CH. A IN 1 11 CH. B IN 1 CH. A IN 2 12 CH. B IN 2	Inches (mm)	N PC BOARD
CH. A IN 4 13 CH. B IN 4 CH. A IN 8 14 CH. B IN 8	1000	USTRAP (2)
CH. A IN 10 15 CH. B IN 10 CH. A IN 20 16 CH. B IN 20		
CH. A IN 40 17 CH. B IN 40 CH. A IN 80 18 CH. B IN 80		
CH. A IN 100 19 CH. B IN 100 CH. A IN 200 20 CH. B IN 200	LIMIT INDICA	ATIONS
CH. A IN 400 21 CH. B IN 400 CH. A IN 800 22 CH. B IN 800		DDC-8400 TWO CHANNEL, TWO LIMIT COMPARATOR
	8400 SINGLE-CHANNEL, 2-LIMIT, 3-ZONE COMPARATOR	LIMITA LIMITB CHANNELA CHANNELB
CH, A IN 4K 26 CH, B IN 8K FRONT	UNDER LO LIM LIMITS HI LIM OVER	UNDER LIMIT OVER UNDER LIMIT OVER
CH. A IN 10K 27 CH. B IN 10K LIGHTS		
CH. A IN 20K 28 CH. B IN 20K CH. A IN 40K 29 CH. B IN 40K	Input is greater	RED GREEN RED RED GREEN RED
CH, A IN 100K 31 CH, B IN 100K when lamp	Input is Input is than the LO Input is Input is Indica less than equal to the thumbwheel limit equal to greater than Indica both I LO and is less than the HI both whe	en less than I equal to greater than less than equal to greater than
CH. A IN 200K 32 CH. B IN 200K is lit. If CH. A IN 400K 33 CH. B IN 400K In 400K	numbwheel thumbwheel the thumbwheel thumbwheel lamps limits limit thumbwheel limit. limits limits. lit.	
CH. A IN 800K 34 CH. B IN 800K CH. A IN OVERSCALE 35 CH. B IN OVERSCALE	ONLY ONE LAMP CAN BE LIT IF RIGHT THUMBWHEEL LIMIT IS GREATER	ONLY ONE LAMP ONLY ONE LAMP
CH. A IN POLARITY 36 CH. A IN POLARITY A B	IF RIGHT THUMBWHEEL LIMIT IS GREATER THAN THE LEFT THUMBWHEEL LIMIT	CAN BE LIT. CAN BE LIT.
BOTTOM BIGHT TOP		

GOLD BOOK 76/77

A B BOTTOM RIGHT TOP

BLOCK DIAGRAM





The 8400 series Comparators include built-in latches and gates for the limit outputs. The latches and gates can be hard-wired so they continuously transmit all outputs as shown in the static mode drawing. Or the latches and gates can be externally controlled in the dynamic mode by an A/D converter, DPM, computer, microprocessor or logic circuits to transmit outputs on command on a common data bus shared by other devices. In the static mode, valid outputs can be expected within 600 nanoseconds after the BCD inputs stablize. In the dynamic mode, valid limit outputs are available within 725 nS, if the timing shown in the chart is observed. Any delay in the latch or gate commands will produce a corresponding limit output delay. Also, commands must use the sequence and timing shown to avoid multiplexing invalid data onto the bus.

1. Dual Limit Models

RULES

Left switch is for setting lower limit.

2. Input Bits Not Used

Should be wired to ground, and corresponding digits on setpoint switches set to zero.

3. Polarity Inputs

Negative sign enters as low level, positive as high. If unused, tie to +5V (pins A1, B1) through 1000 ohms resistor and leave setpoint polarity switches on (+). This gives normal first quadrant operation. For third quadrant operation, tie unused polarity sign to ground and leave setpoints on (-).

- 4. Over Scale Inputs Positive overscale input generates "OVER LIMITS" indication regardless of incoming data bits; negative overscale input generates "UNDER
- LIMITS" regardless of data bits. If not used, overscale input terminals should be grounded.
- 5. Positive numbers are handled as greater than negative numbers.
- 6. A negative number with large magnitude is smaller (lower) than a negative number with small magnitude.
- 7. Latch update terminals may be permanently grounded (enabled) so lamps will continually track the comparator decisions. Output logic lines are still under control of output gate terminals, for strobing.
- 8. For latched input sampling operation, actuate latch update terminals at desired time for usual TTL clock duration. Lamp and logic outputs will hold until next update clock. Output logic is still subject to output gate control (low level permissive).
- 9. When input is from a digital clock, two data bit inputs have to be grounded (i.e. the "8" bit line in the tens of seconds digit and tens of minutes digit). These lines are not controlled by digital clock outputs.

OPTIONAL RELAY BOARDS

The 8400 series comparators have a spare PC card slot available in the upper portion of the instrument for optional relay boards to control external devices using various limit outputs from the lower board. Because limit outputs from the lower board are externally wired to the upper (relay) board, a wide variety of control functions can be made. External devices such as pumps, motors, valves, solenoids, lamps, horns, etc. may be turned on or off either above, below, between, or outside of limits. Control and alarm limit functions may also be cascaded using the relay as logic gates. Thus, a pump could be turned on only if a valve was open and a tank level was below setpoint. Cascaded interlocking alarms can be created whereby a local lamp alarm is activated first then a loud horn if the alarm condition isn't corrected after a time delay.

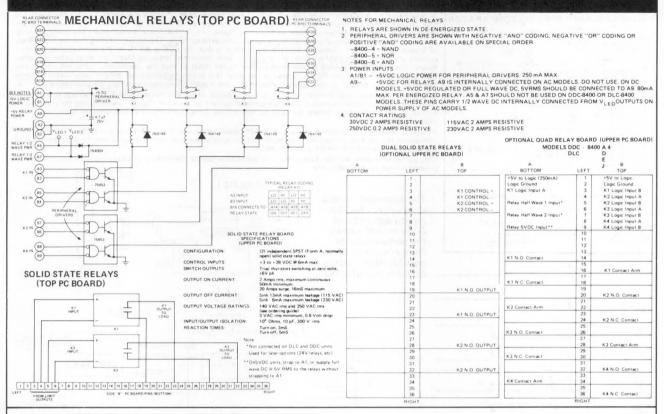
The relay boards directly control DC or AC line-powered devices and provide high isolation to external circuits. Larger electrical equipment may be controlled by using the 8400 relays in pilot service to secondary external relays.

Two types of relay boards are offered:

The first type includes (4) electromechanical relays with Form C SPDT contacts. The second type of relay board contains (2) solid-state relays. These solid-state relays are triac thyristor output devices simulating SPST normally-open relays. The solid-state relays use photocoupled optoisolation for very high resistance between input and output. Zero-voltage switching minimizes RFI and switches heavy loads (20 Amp surge for one line cycle). There are no contacts to pit, weld together, or burn out after many switching operations because all-semiconductor construction is used. The solid-state relays are ideal for lamp load surges and inductive loads (motors, solenoids, actuators, etc.)

Vol 3/224

OPTIONAL RELAY BOARDS (Cont'd)



APPLICATIONS

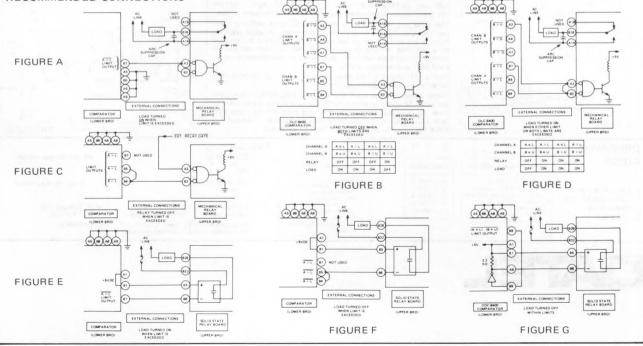
Because of the variety of relay configurations and output logic on the 8400 series comparators, a very broad range of applications can be implemented. Figures A through G shown here describe connections between the lower PC board limit outputs and the upper PC board relays. Figures A through D discuss the mechanical relays and E, F and G are concerned with the solid state relays.

The negative true, open collector limit outputs can be wire-OR'ed externally (shown in several applications). The input NAND configuration of the mechanical relays allows external gating of individual relays. The applications are by no means limited to those shown here.

The output gate and latch controls, A5, B6, A6, and A8 are shown grounded LOW. If the gate lines are externally disabled, the relays will simultaneously be de-energized.

Figure H shows a 5-zone sorting system using two comparators in cascade. A bipolar BCD input is bussed to both comparators and five output lines indicate which zone the input falls into. The configuration could be used to sort items by weight, size, electrical, mechanical or any measurable physical property. The logic outputs would be connected to relays and solenoids which would route the sorted items into bins or slots. The selection limits are dialed in on the comparator front panel thumbwheels, allowing a variation for different items. At least one and only one of the five limit output lines is valid at any one time so that there is no ambiguity or dead zones. Additional comparators can be cascaded to add two more zones per added comparator.

RECOMMENDED CONNECTIONS

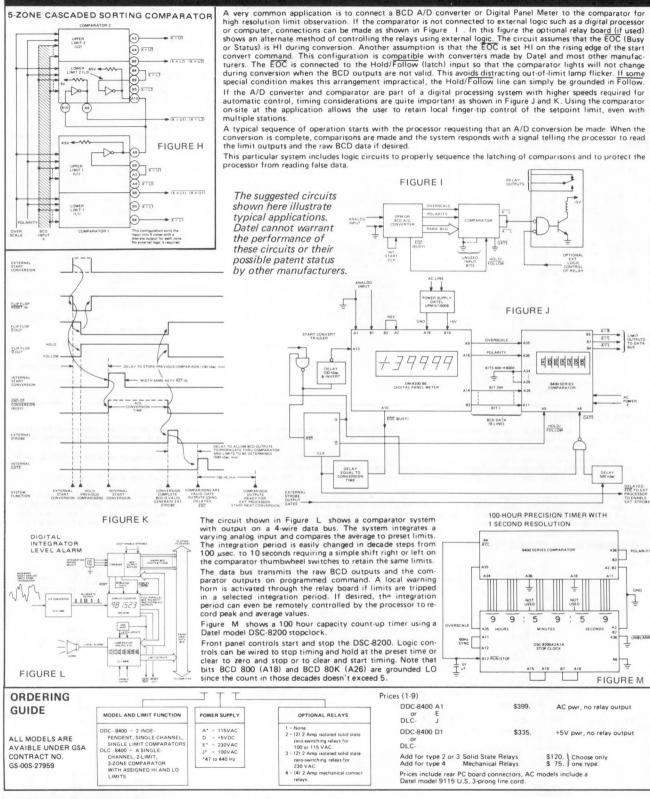


GOLD BOOK 76/77

See inside back cover for DATEL sales offices

Vol 3/225

APPLICATIONS (Cont'd)





Electronic Design's



0.005% MINIATURE DIGITAL **VOLTAGE CALIBRATOR**

MODEL DVC-8500

FEATURES

- ▶ ±19.999 Volts Isolated
- **Bipolar Output @ 25mA**
- 1mV Settability With ±1.5mV Continuous Vernier, 100µV Graduations
- Accuracy ±1mV of Setting With Low ±20µV/°C Drift
- Miniature Aluminum Case Includes Bench-Top Stand or Can Be Panel-Mounted
- Low Cost \$295.00 (1-9)

GENERAL DESCRIPTION

VOLTA OF OUTDUT

A digital voltage calibrator small enough for bench-top use or panelmounting is available from Datel Systems and fulfills many laboratory and portable applications. Datel's model DVC-8500 Calibrator offers full 4½ digit resolution (1mV steps) with a +19.999 Volt bipolar output. Up to 25mA output current may be drawn at the +1mV rated accuracy. This short-circuit proof output may be continuously varied within +1.5mV for precise vernier control. The $\pm 20\mu V/^oC$ drift specification applies over the 0°C to +50°C operating temperature range.

The DVC-8500 uses easy-to-operate digital lever switches to set the output voltage. Front panel banana jacks simplify the connection to cali-bration circuits while rear panel sense feedback inputs insure output accuracy.

*±10%, 47 to 440Hz

An overload LED lamp is lit when output loading exceeds 25mA. The rear connector accommodates either standard dual 36-pin gold-plated PC board connectors or solder or crimp lugs using 4-40 hardware. The +10V reference is derived from an oven-stabilized zener diode and is brought out at the rear connector for voltage-tracking of external circuits.

The DVC-8500 is powered by a choice of 100, 115, or 230 VAC +10%, 47 to 440 Hz at 5 watts typical. The black-anodized extruded aluminum housing provides excellent shielding to electrical noise and a regulated power supply provides excellent stability and performance.

SPECIFICATIONS: (Typical between +20°C to +30°C at steady ambient temperature after 5 minute warm-up)

VOLTAGE OUTPUT			
	to +19.999 Volts DC or 0 to -19.999 olts DC, lever switch selected.		selected output. Graduated in $100\mu V$ divisions.
Output Current Range 0	to ± 25 mA (source or sink) to rated ltage output accuracy.	INPUT/OUTPUT CON	
Output Overload Gr illu Ou	reater than ± 25mA (source or sink) will uminate front panel LED overload lamp. utput is current limited (continuous	Front Panel	Voltage output and output common avail- able from two (2) gold plated brass deep banana jacks.
	ort-circuit proof) to \pm 70mA (source or nk) at any voltage up to \pm 20VDC.	POWER SUPPLY	
Output Impedance: Le		Power Required	Choice of 100, 115. or 230 VAC, ±10% 47 to 440 Hz, 10 watts. 3-prong U.S.
PERFORMANCE			captive line cord installed. Ground wire
(ed	ithin ± 1 mV of setting when calibrated. quivalent to $\pm 0.005\%$ of Full Scale)		connected to case, but transformer isolated ±300VDC from output common.
	ue to all effects except temperature ift.	MECHANICAL DIMENS	SIONS
Resolution ±1	mV increments and ± 1.5 mV Vernier the 100=V graduations.	Case	5.56"W x 2.11"H x 5.78"D (141,2 x 53, 6 x 146, 8mm)
Temperature Drift Wi Operating Temperature	ithin ±20µV/ºC		5.86"W x 2.25"H x 0.50"THK (148,7 x 57.0 x 12,7 mm)
Range		Weight	2.25 pounds (1,0 Kg)
Output Noise 25 Reference Source 6.4		MOUNTING	Choice of bench-top mounting or panel
	x lever-operated, detented switches otary potentiometer, range ±1.5mV of		mounting through a cutout measuring 2.16"H x 5.59W (54,8 x 142,1 mm) and secured by 2 U-Straps. See ordering guide for optional panel-mount kit.
MODEL NO. DVC-8500			States and a second
AC POWER	SUPPLY	PRICE (1-9)	
A=115VAC E= 230VAC			rear PC-board connector, and hardware.
J= 100VAC	A CONTRACTOR OF		le supplied for bench-top use are screwed

Rubber feet and tilt-stand bale supplied for bench-top use are screwed to case bottom and must be removed before panel mounting).



DPP-7 DIGITAL PANEL PRINTER



FEATURES

- 3 Lines/Second OEM-Reliable Thermal Printer
- Includes All Electronics for BCD Inputs with Input Storage Register
- 6 Numeric Columns and Sign
- Selectable Leading Zero Blanking
- Positive or Negative True TTL/DTL Inputs
- +5VDC Power (2.3 lbs.) or AC (4.2 lbs.)
- \$475.00 Single Quantity
- Last Line Visible Immediately After Printing

DESCRIPTION

Imagine a low cost 7-column panelmounting printer just slightly larger than most digital panel meters. Imagine this lightweight, high-reliability digital panel printer installed in your instrument or system front panel. And imagine an inkless, non-impact thermal printing method with only two moving parts which will

This is Datel's miniature 3 line per second DPP-7 thermal panel printer. A no-nonsense, simple to apply, OEM-designed digital output device that weighs in at only 2.3 pounds (1,1Kg). OEM features are designed in to the DPP-7 such as selectable leading zero blanking, selectable positive or negative true coding inputs and choice of +5VDC or AC line power. Full parallel TTL input BCD electronics are included

Other OEM design features include a selection of printout formats, manual print and advance front panel switch, and a low-paper switch output. A unique mounting technique uses an aluminum housing which attaches directly through a front panel cutout. This housing permanently holds the electronics, although the mechancial assembly can be completely removed for paper replacement using a single front panel thumbscrew. As the mechanical assembly is removed, it disconnects from the internal electronics PC board connectors, so that no lethal power voltages are exposed during paper reloading. However, the external PC board connectors at the rear of the case remain connected to the internal electronics.

The housing supports the weight of the mechanical assembly and is mounted on a front panel through a 4.50" x 2.72" cutout and secured by four screws. Three DPP-7 panel printers can conveniently be mounted across a 19" x 3-1/2" high rack mount panel.

OEM pricing makes the DPP-7 ideal for instrument products. Comparable impact parallel printers with BCD decoding and drive electronics usually list for more than the DPP-7.

Standard 1-34" wide thermographic papers are used in handy 150 foot rolls giving about 9,000 lines per roll with 5 lines per inch. The 7-segment digits are .155" high with left-of-digit decimal points selectable at each digit. Seven column printing formats include sign and six digits or 2-channel (ident) digits, sign and 4 data digits. Other 7 column decimal formats are also available.

The DPP-7 Digital Panel Printer extends back 6.2" from the front surface of the mounting panel (8.62" for the AC powered versions), including space allowance for the two 30-conductor PC board connectors or AC fuses.

Three universal AC line voltages (100, 115, and 230 VAC) will power the DPP-7 Printer as well as +5VDC at 20 watts average (8 Amps peak).

The DPP-7 is ruggedly built, using a simple, but sophisticated mechanical design which is optimized for heavy duty OEM applications. A proprietary printhead character coating allows the head to be conservatively rated at 3 million lines.

HIGHLIGHTS

2.3 Lb. Panel-Mounting Featherweight

At 2.3 pounds (1,1Kg) the DPP-7 DC version is one of the lightest panel-mounted recording instruments available. It is directly compatible with the size, shape and interfacing of Digital Panel Meters.

OEM Reliable - only Two Moving Parts

Instead of the usual assembly of ratchets and gears, the DPP-7 Digital Panel Printer needs only two long-life moving parts - a linear solenoid and rotary clutch. Two 1/8" excursions of this solenoid connected to the one-direction rotary clutch cause one line advance. There are no banging hammers or twirling printwheels to fail and to cost extra in assembly. All electronics use low power Schottky TTL logic, assuring minimal heat rise and long, service-free life. Components have been generously derated and were selected particularly for their OEM reliability. A full one-year warranty provides further assurance of product excellence. An absolute minimum of maintenance is needed. Printhead cleaning required in other thermal printers can safely be ignored because of the wiping action of the paper.

Complete with Binary Coded Decimal Inputs and Storage Register

Datel's Miniature DPP-7 Printer is complete with BCD electronics. Many competitive printers don't include full parallel BCD or if they do, it is an expensive additional chasses with bulky cabling and unique power requirements. Datel's little DPP-7 printer is ready to use and all BCD I/O logic (with selectable positive or negative true TTL coding) is built in. A strobed input storage register allows multiplexing with other I/O devices sharing the same data bus lines.

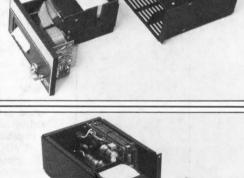
+5VDC or AC Line Powered

Take your pick of power voltages. Use either +5 Volts DC or 100, 115, or 230 Volts AC, 47 to 440 Hz. The +5VDC printer offers the smallest package, only 6.2 inches (158 mm) deep and only 2.3 pounds (1,1Kg). The +5V version requires a regulated power supply capable of 8 Amps peak during print cycles while the AC version can accept a variety of universal worldwide power voltages and is slightly longer than the DC version

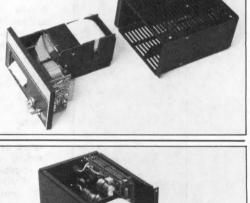
Thermal Printhead

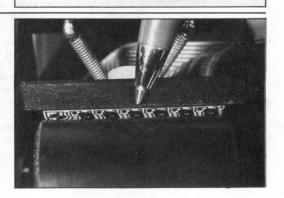
Printing couldn't be simpler. Heat-sensitive thermographic paper is positioned under six decimal digits in 7-segment format. Each digit consists of conductive thick film resistor matrix segments deposited on a ceramic substrate. Segment-parallel, digit-serial power pulses are applied to each digit for 25 milliseconds. I²R heating then darkens the paper in contact with the heated segments, leaving crisp, black printed digits. A proprietary, thermally conductive surface on the thickfilm elements has high wear resistance allowing a conservative 3 million line printhead life. Characters are formed along the bottom edge of the printhead so they may be viewed immediately after printing.











General

Number of columns: 7

7-column formats available:

- a) Leading \pm sign and 6 decimal digits
- b) 2 leading ident or channel digits, ±sign and 4 data digits
- **Decimal digit format:**

7-segment 0 to 9 digits .155" (4 mm) high with 10° slant and selectable left decimal point.

Printing method:

Thick film thermal print head, black characters on white paper (using 3M Type 161 paper)

Printer paper:

1.75" wide x 150 feet long, (44,5 mm x 45 m), 3M-type 161 thermal paper roll with the thermal surface facing away from the center of the roll.

Paper advance:

Via linear solenoid and one-direction rotary clutch. Paper tears off cleanly by lifting against the paper slot top edge.

Performance

Max, printing rate: 3 lines per second Print and paper advance cycle: 330 milliseconds

Line spacing: 0.2 inch (5 mm)

Line density: 5 lines per inch

Line capacity per paper roll: approx. 9,000 lines Minimum print head life: 3 million lines

Average print pulse on-time: 25 mSec. (height varied by temperature feedback)

Inputs

DTL/TTL compatible, selectable positive or negative true, level sensitive. TTLLS low power Schottky logic used on all inputs.

Logic Levels:

Positive true:	$+2.0V \le "1" \le +5.0V$ $0V \le "0" \le +0.5V$	Note TTLLS
Negative true	0V ≤ ''1'' ≤ +0.5V +2.0V ≤ ''0'' ≤ +5.0V	logic levels

Note: Pullup resistors to +5V may be optionally removed on all inputs and outputs.

Data: (24 lines)

Full parallel BCD (1-2-4-8), selectable positive or negative true, 1 TTLLS load plus 10 K ohm pullup to +5V. May be used with Form A (normally open) or Form B (normally closed) switch closure inputs. Level sensitive (rise-time non-critical). Data is stored (see timing, pg. 8)

Change Data Polarity: (Pin C1-B11)

Selects input polarity of data, decimal points and ± sign simultaneously.

LOW = positive true coding

HIGH = negative true coding

6 TTLLS loads, plus 1 K ohm pullup to +5V, level sensitive

Print and Advance Command: (Pin C1-B14)

Level sensitive for Form A or Form B contact closure,

selectable positive or negative true.

1 TTLLS load plus 10K ohm pullup to +5V.

Pulse Width: 1 miscrosecond to 200 mSec (data must be valid 1 µsec. after leading edge and 500 nSec. before the print command).

Maximum print command rate: 3 per second.

Paper advance automatically occurs after digit printing. Holding print command TRUE longer than the busy output is true (200 to 330 mSec, typ) causes continuous 3 lines/sec. printing.

Change Print Polarity: (Pin C1-B7)

HIGH = negative true coding

LOW = positive true coding

- 1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive
- Leading Zero Suppress: (Pin C1-B4) blanks all leading zero's to the left of decimal point except a zero just left of the decimal point
- HIGH = Leading O's blanked
- LOW = full print (no suppression)
- 2 Low Power TTL loads, plus 10K ohm pullup to +5V, level sensitive.

Minus Sign: (Pin C1-B1)

Selectable positive or negative true using data level select input.

1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive.

Plus Sign: (Pin C1-A5)

(Selectable positive or negative true using change data polarity input). (Minus sign must also be printed since it is used as the horizontal portion of the plus sign).

1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive

Note: Printing "plus" sign only results in vertical portion of plus sign. See above. Usable as 100% overrange digit.

Blanked Character:

Created by loading 1-1-1-1 in a given column. Can be hard-wired.

Decimal Points: (6 lines)

- 1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive
- (Selectable positive or negative true using change data polarity inputs).

No-Print Paper Advance: (Pin C1-A3)

- Ground this line 70±5 mSec to advance one line. Hold to ground for continuous advance at 6.7 lines per second.
- 1 TTLLS load plus 10K ohm pullup to +5V.

No Print Paper Advance:

May also be created by loading the illegal BCD character 1-1-1-1 in all decimal locations, and disabling all decimal points and ± signs, then initiating a print/ advance command.

Test: (Pin C2-B6)

- $LOW = \pm .8 .8 .8 .8 .8 .8$ printout when print/advance command is given.
- 1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive.

Change Busy Polarity: (Pin C1-A2)

- HIGH = positive true busy out
- LOW = negative true busy out
- 1 TTLLS load, plus 10K ohm pullup to +5V, level sensitive.

SPECIFICATIONS (continued)

Outputs

DTL/TTL compatible

Positive true:	0V ≤ "0" ≤ +0.4V +2.4V ≤ "1" ≤ +5.0V
Negative true:	+2.4V ≤ "0" ≤ +5.0V 0V ≤ "1" ≤ +0.4V

Busy: (Pin C2-B12) (Open collector TTL 7438 with 1K ohm pullup to +5V)

Remains TRUE during print and advance cycle (approximately 200 to 330 milliseconds). Data inputs may be changed 500 nSec. after transition to TRUE. Next print command can be enabled when busy goes FALSE. Selectable positive or negative true. 10 TTL loads.

Out of Paper: (Pin C2-B4) see dwg. pg. 10

Switch opening via mechanical pawl when approx. 6' (2m) of paper are left on roll. Paper roll visually indicates "low paper" within 10 to 15 feet (3 to 4.5m) of end of roll using red stripe on roll. Switch is in series with PC board contacts which disconnect if printer mechanism is not completely seated in case. Open switch contacts or print mechanism removed will disable both local and remote print command. Pin C2-B4 has an internal 1K ohm pullup to +5V normally grounded by switch before paper is low.

Front Panel

LED red power-on lamp

Paper Quantity Indicator:

Mechanical pointer which rides on paper roll, indicating relative amount of paper left.

Paper Roll Replacement:

By sliding out front panel printer assembly. PC board interlock automatically disconnects all power to printer assembly and power supply with electronics remain with housing case. Removal by a single Dzus-type front panel thumbscrew.

Print/Remote/Advance

Front panel 3 position toggle switch, stable in center position (REMOTE), must be held in top (ADVANCE) or bottom (PRINT) positions.

ADVANCE:

When switch is held up, the printer continuously advances paper without printing at a 6.7 line per second rate. Paper may be manually advanced simply by pulling paper out of front opening at any time.

REMOTE:

Center position enables all external inputs.

PRINT:

When switch is pushed down, printer prints one line and stops. After print and advance, external input is accepted even if the switch is held down.

Temperature Ranges

Operating: 0 to $+40^{\circ}$ C (to $+50^{\circ}$ C at derated speed) **Storage:** -25° C to $+85^{\circ}$ C (Paper darkens above $+60^{\circ}$ C) Active printhead temperature sensor is employed to maintain proper print head temperature at all ambient temperatures and during warmup.

Power Supply

+5 Volt Version:

4 Amps average current (20 watts dissipation) at 3 lines/sec. max. printing rate. (10 Watts, typ in standby)

Segment-parallel, character-serial printing requires +5V @ 8 Amps peak, duty cycle is 10 to 90% during print and advance period.*

Separate PC board connection available to supply "clean" ($\pm 2\%$ @ .3 Amp) 5 volts to logic section. Logic spikes must be held to 50mV max. pk-pk.

Unregulated +5V ($\pm 10\%$) connected through 1/4'' spade terminal connector, 16 gauge wire or larger not to exceed ten feet (3 meters).

Fuse:

7 Amp SLO-BLO, 1/4" x 1-1/4"

*8 Amp current pulses on and off during print and advance cycle from 10 to 90% duty cycle (depends on character printed, leading zeros, etc.). 8 Amp, 5 to 20 msec. pulses occur several times per second in standby.

Power consumption varies with print rate, leading zeroes, digits printed, signs and decimal points.

Power Supply

AC Version: 105-125 VAC, 47-440 Hz @ 40 watts max (10 watts, typ standby)

Optional:

205-240 VAC, 47-440 Hz @ 40 watts max (10 watts, typ standby)

Optional:

90-110 VAC, 47-440Hz @ 40 watts max (10 watts, typ standby)

AC Fuse: 1/4" x 1-1/4" Buss MDL or equivalent 1/2 A, SLO-BLO, 115VAC, 1/4A, SLO-BLO, 230 VAC.

Note: Case is isolated from 5V ground and AC line. A separate spade terminal is included to ground case. +5V, 200mA max, logic power out available with AC

+5V, 200mA max. logic power out available with AC version.

Connectors

Data and Controls: (and optional logic +5V)

(2)30-conductor (15 per side).

Double-sided PC board connectors. 0.1" centers, Viking #3VH15/1JN-5 or equivalent

, 2 included with printer).

+5V Power

(2) 1/4" spade terminal connectors, included.

AC Power

(1)Double 1/4" spade terminal connector. Mates to a 9115 AC line cord (included).

Weight (with housing and full paper roll)		
5 Volt Version:	2.3 lbs.	(1,1Kg)
AC Version:	4.2 lbs.	(1,9Kg)

Dimensions (Uses #4 hardware) Front panel mounting cutout: 4.50" WIDE x 2.72" HIGH (115 mm x 69 mm)

Front panel Bezel dimensions: 5.25" WIDE x 2.82" HIGH (134 mm x 72 mm)

Depth behind front surface of mounting panel including clearance for rear PC connectors and fuses:

5V Version: 6.2" (158 mm) AC Version: 8.7" (221 mm)



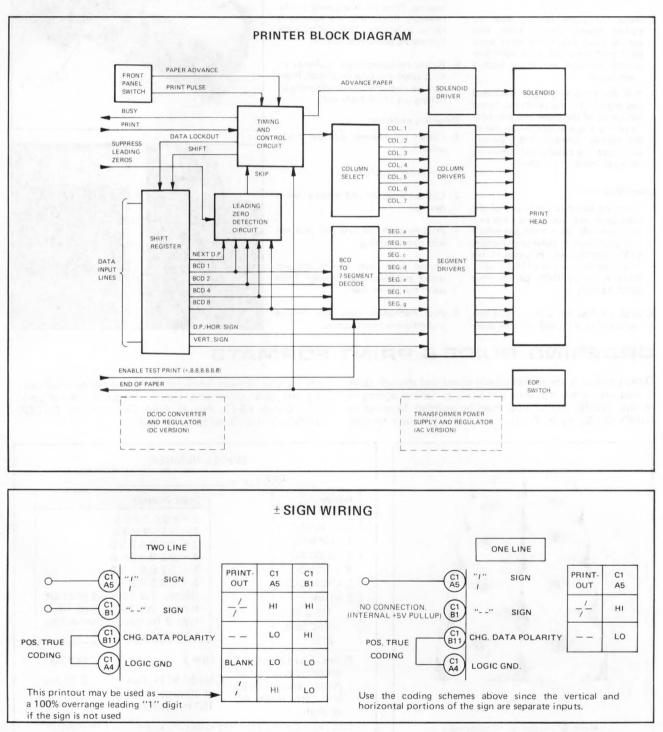
APPLICATIONS



An ideal use for the DPP-7 is to record analog values from a BCD output A/D converter or Digital Panel Meter. A simple external clock circuit or an A/D converter with an adjustable conversion rate can be used to form a printing data logger. With the addition of Datel's digital time-of-day clock and data acquisition module, a complete multi-channel logging system can be made. See page 11.

Most scientific and analytical instruments with digital interfacing capability will have full parallel BCD outputs which can be directly connected to the DPP-7. Use the DPP-7 with Datel's autoranging DM-2000AR Digital Panel Meter to create an analog sampling system with $3-\frac{1}{2}$ digit resolution over 3 decades from 200mV to 20V full scale. See page 11.

Using the DPP-7 printer with a DPM will allow faster sampling than taking readings by hand or by visual sampling of the DPM readout. Longer-term variations and drifts are more easily viewed when the printer and DPM work handin-hand.



PAPER LOADING

- 1. Shut off all power to the printer if the printer uses a separate power switch.
- 2. Slide out the printer mechanism by first loosening the front panel thumbscrew counterclockwise until it stops. Pull the thumbscrew firmly straight out and the front panel/printer assembly will slide out all the way. Some force may be needed to release the internal PC connection.
- 3. Raise the paper loading door by pulling forward until it stops. This automatically lifts the thermal printhead from the paper drive roller (see photo). Remove any paper from a 8. Rotate the thumbscrew clockwise unprevious roll.
- 4. Pull the remaining paper backward out from under the printhead. Grasp both ends of the paper roll axle with fingertips and pull straight up out of the printer assembly. The axle will slide past the circular axle retaining spring as shown in the photo.

Inserting new roll

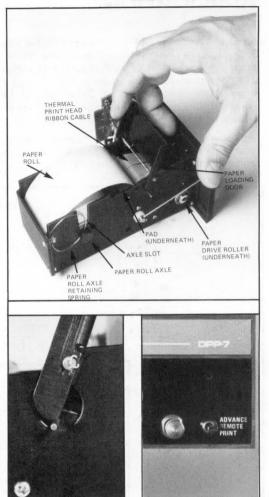
- 5. Slide the paper roll axle out of the used paper roll and reinsert the axle in a new roll. Do not discard axle!!! The paper roll is Datel part number 9101 supplied only in boxes of ten rolls. Order box number 9114 (\$19.95). Spare axles are Datel part number 9062, \$5 each.
- 6. Slide the new roll and the axle past the retaining spring and insert the paper

over the pad and under the printhead ribbon cable (see photo) until paper appears at front panel slot. Be sure the paper is threaded from the rear and passes over the roll. Paper should be cut straight across for easy insertion. Only the outside paper surface is treated for printing.

- 7. Pull paper through front panel slot, close the paper loading door and slide the printer mechanism back into the housing. Press the front panel printer assembly firmly into the housing as far as it will go. This will seat the internal PC board connection.
- til it stops and turn on power. Paper may be manually advanced simply by pulling out of the front slot.

Reloading summary:

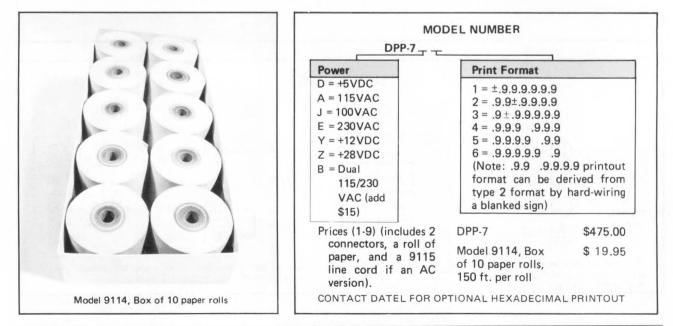
- 1. Loosen thumbscrew, pull out mechanism.
- 2. Lift paper loading door.
- 3. Lift out used roll and reinsert axle in new roll.
- 4. Press new roll and axle into axle slot past circular spring.
- 5. Thread paper over top of roll and under printhead out through front panel slot. Close door.
- 6. Push mechanism back into housing and retighten thumbscrew.



ORDERING GUIDE & PRINT FORMATS

Datel's products are available both direct and through GSA. If you are connected with a military or federal agency or receive federal funds, you may be entitled to purchase Datel's Digital Panel Printers and other products through

the General Services Administration to expedite requisitioning and order processing. Datel's printer is covered under FSC Group 66-17, Part II, GSA Contract No. GS-OOS-27959. Contact Datel for assistance.



See inside back cover for DATEL sales offices



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

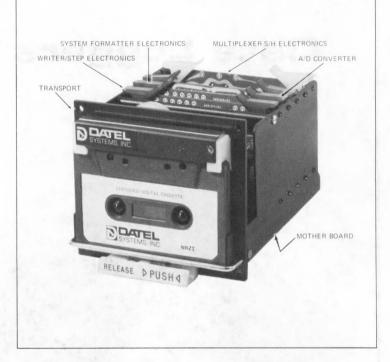
Data Loggers





LOW POWER CASSETTE DATA ACQUISITION AND LOGGING SYSTEM

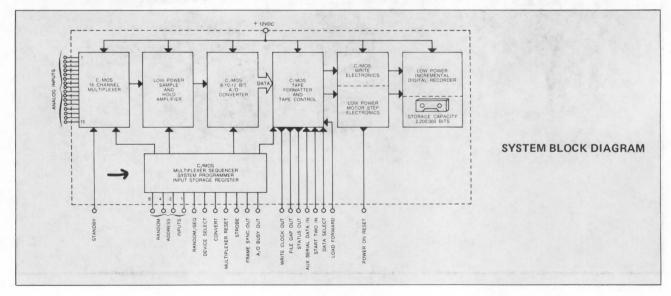
MODEL LPS-16 DATALOGGER



FEATURES

- Sixteen Channel Analog Input
- Digital Input for Timing Information
- ▶ 12 Bit A/D Resolution
- 12VDC Battery Operated
- 900 Milliwatts Maximum Power Consumption
- C/MOS Logic Throughout
- ► True Incremental Recording
- Certified Phillips Cassette
- ▶ 2.2 Million Bit Capacity
- ► Total Weight 2 Lbs.
- Cassette Reader for Computer Entry

SYSTEM I/O CONTROLS PROVIDE TOTAL SYSTEM FLEXIBILITY



INTRODUCTION



Datel Systems announces a new approach to the Data Logging system, a complete *Data Logging system in a Module*, occupying only 134 cubic inches weighing less than 2 lbs. and operating from a single 12VDC source requiring only 900 milliwatts when recording and microwatts during standby.

Through the use of C/MOS electronics and a unique incremental digital cassette recorder, Datel Systems has significantly reduced the size, power drain and cost over competitive systems.

In incremental recording, the cassette tape moves only when information is presented. This conserves power in portable operation, and no tape is wasted because data is uniformly recorded in precise tape increments. Further, the length of time a cassette can be left unattended can be accurately predicted from the data rate, the number of bits, and the tape length.

Applications include oceanography, pollution monitoring, meteorology, seismology, or other remote data logging requirements. It is also ideal for other scientific and technical data acquisition uses both in the laboratory and in the field.

A cassette reader is available which allows the user to transcribe the digital data on the cassette to computer compatible media. These readers may be interfaced to produce IBM 1/2" tape or to teletype, data terminals, acoustic coupler, or directly into a digital computer.

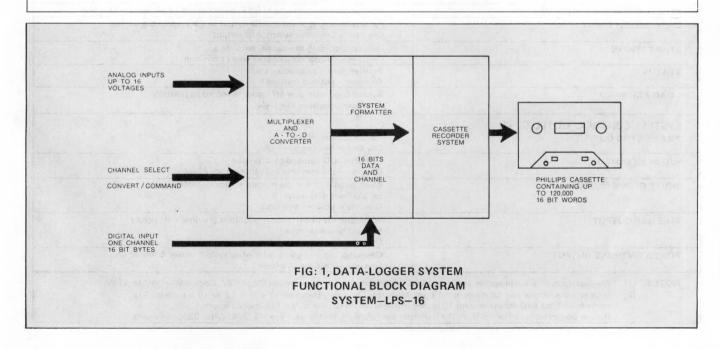
GENERAL DESCRIPTION

The LPS-16 Data Logging System is a complete package for recording multi-channel analog data and single channel digital data. It features low power consumption and compactness making it especially suitable for remote data logging applications in unattended areas over long time periods. It will accommodate up to 16 channels of analog input and any number of 16 bit bytes of digital data in serial form. The analog data inputs can be sequentially or randomly multiplexed, converted into digital form, formatted and stored on a standard Phillips cassette. Approximately 120,000 samples of data along with identifying channel number can be stored on one cassette.

A functional Block Diagram of the system is shown below. The inputs required are up to 16 analog voltages, one digital input channel, control logic signals and power. The system can be conveniently divided into two subsystems; analog multiplexing and digitizing is one, and the digital recording is the other.

System LPS-16 utilizes C/MOS type logic throughout, thus negligable stand-by power is consumed. Only during the actual A/D conversion and storage on tape is any appreciable current consumed. Therefore, system LPS-16 may be operated for long periods on battery with low average power.

Cassette tapes prepared in the system may be read with the Datel Systems LPR-16 Reader system which provides a 16 bit parallel output of the data on tape at a rate of about 90 sixteen bit words per second. Each word consists of a 12 bit A/D value plus 4 bit channel address. This LPR-16 reader recognizes and stops on record gaps for convenient computer interface.



LPS-16 SYSTEM SPECIFICATIONS

ANALOG INPUTS	
IUMBER OF ANALOG INPUTS	16
NPUT CHANNEL CONFIGURATION	Single ended
	0V to -5VFS or ±5VFS, 0 to +5VFS 100 MegOhms "ON" or "OFF"
HANNEL INPUT IMPEDANCE	NOTE: When the 12V DC system power is turned off each channel has an input impedance of 10K Ohms
HANNEL INPUT OVERLOAD	±10V (max.)
HANNEL MODE OF OPERATION	Random or Sequential
HANNEL INPUT ACQUISITION TIME	100 µsec – includes input settling time
	50 nsec
SYSTEM ACCURACY	±0.025% of FS ±1/2LSB
SYSTEM LINEARITY	±1/2LSB
/D RESOLUTION	8, 12 Binary Bits
SYSTEM TEMPERATURE COEFFICIENT	±0.004%/ ⁰ C
YSTEM THROUGHPUT RATE	200 msec per 16 bit word (12 bit A/D plus 4 bit channel address)
NPUT CHANNEL SCAN RATE	Up to 5 per second
A/D DIGITAL OUTPUT CODING	Straight Binary – Unipolar Input Offset Binary or 2's complement – Bipolar Input
ASSETTE TAPE STORAGE METHOD	Two channel NRZI: Track #1 – Data, Track #2 – Data (complement)
ASSETTE TAPE FORMAT (2)	16 bit words (12 A/D bits plus 4 bits for channel address)
ASSETTE TAPE RECORD GAP	Two bit gap separates each 16 bit word
ASSETTE TAPE END-OF-FILE GAP (3)	Twelve bit file gap every 64th word, or per order. See guide.
SYSTEM CONTROL INPUTS (1) RANDOM ADDRESS INPUTS	Selects analog channel Four lines 8-4-2-1-negative true logic
RANDOM/SEQUENTIAL INPUT	Selects multiplexer mode One line – logic zero selects random mode
DEVICE SELECT INPUT	Controls all input command lines One line – negative true logic
CONVERT INPUT	Initiates A/D conversion One line – negative true logic
NULTIPLEXER RESET	Resets multiplexer to channel one One line — negative true logic
TROBE INPUT	Strobes all input lines and internally stores them One line – negative true logic
AUXILIARY SERIAL DATA IN	Permits cassette recording of EXT. serial data in 16 bit bytes – One line
	Permits recording of either A/D output or EXT. serial digital data One line – Logic one selects A/D output
TART TWO IN	Initiates recording of external serial data One line — Triggers on negative going transition
TATUS	Positive during a recording cycle One line – positive true logic
OAD FORWARD	Advances cassette tape off leader to recording position One line – negation true logic
YSTEM CONTROL OUTPUTS (1) RAME SYNC OUTPUT	Identifies channel one One line — positive true logic
A/D BUSY OUTPUT	Identifies A/D conversion in process One line – positive true logic (during conv.)
VRITE CLOCK OUTPUT	When gated with file gap output, it provides shift signals for auxiliary data input One line – positive true logic
ILE GAP OUTPUT	When gated with write clock output, it provides shift signals for auxiliary data input One line — positive true logic
OWER ON RESET OUTPUT	Generates negative going pulse when system power is turned on One line — negative true logic
	tandard C/MOS logic levels, Logic zero $-$ 0V to +3V, Logic one $-$ +9V to +12V he formatter card allowing selection of either 12 or 16 bit words. For

LPS-16 SYSTEM SPECIFICATIONS (continued)

	heconder	R CHARACTERIS	51165	
STORAGE MEDIA		Standard Phillips certified data cassette 300 foot length		
STORAGE METHOD		2 channel NRZI		
NUMBER OF TRACKS		TWO: Data on trac Data comple	k one ement on track two	Bach this come
TAPE FORMAT		16 bit words (12 A/D data bits a	nd 4 channel address bit	ts)
RECORD GAP		Two step record ga	p for every 16 bit word	
FILE GAP		Twelve bit file gap e	every 64th word, or per	order. See guide.
TAPE STORAGE CAPACITY		120,000 sixteen bit	words including gaps an	nd load forward
WRITE SPEED		90 steps per second		
		5 sixteen bit words	the same state of the	
DATA INPUT/OUTPUT			Ilel 16-bit thru the A/D	Converter connector
PLAY-BACK SPEED		See Datel's LPR-16 Reader Single 1.5 ⁰ angle stepper coupled to take-up		
MOTOR		reel by slip clutch n		p
MOTOR STEP ANGLE		1.5 ⁰		
ANGULAR ACCURACY		±8 min. of arc non-	accumulative	
TAPE MOTION CONTROL		Single capstan pinch		
			anically during write tin	ne
TAPE TENSION		0.4 oz. inches		terre a second a second second second
ERROR RATE		1 bit in 10 ⁷		
TYPE OF CASSETTE LOADING		Front		
RECORDING HEAD		Dual channel single High quality digital		
OPERATING MODE		Write only	., po	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
PHYSICAL ENVIRONMENTAL SP		tinto only	the second s	
OPERATING TEMPERATURE RANGE		10μa during standb NOTE: Includes tap -10°C to +60°C	be transport plus all elec	tronics
STORAGE TEMPERATURE RANGE		-35°C to +70°C		
RELATIVE HUMIDITY		10% to 95% w/o co	ndensation	
SHOCK & VIBRATION		1.0G @ 0-50 cps, al	I 3 axes	
PHYSICAL SIZE W/ELECTRONICS (includes electronics)		4" high x 4 1/2" wide x 7 1/2" deep (6 1/2" deep behind panel)		
ELECTRONICS		Contained on four PC mother board	plug-in PC cards mounte	ed on a removeable
WEIGHT		2 lbs. includes recorder and electronics		
I/O MATING CONNECTORS		Cinch-part #251-22-30-160 – (I/O Command Signals) Elco-part #00-8218-24-722-005-(16 channel analog inputs, located on top rear of mux/S&H card)		
 An extremely important properly certified tape 	rol signals, and 12 VDC p factor in the reliability assette should be used. It factors in the reliability	embled and ready to op power source plus insert of the LPS-16 data log The mechanical tolera	erate. It is only necessar ing a cassette to begin r ging system is the casse nces of the cassette ca	ry to connect the ecording. tte itself. Only a rtridge and tape
RDERING INFORMATION			FOR EXA	
² S-16- <u> </u>			LPS-1	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
	UTPUT FORMAT	FILE LENGTH		12 Binary Offset
8B = 8 BINARY BITS A = S 0B = 10 BINARY BITS		00 = NONE 01 = 1 WORD		Bits Binary
	FFSET BINARY,	02 = 2 WORDS		±5V Conventional 32 Wo
		04 = 4 WORDS		MODEL PRICE (1-9)
C = 2		08 = 8 WORDS 16 = 16 WORDS	Connectors are	LPS - 16 - 8B \$1195.
THE OCALE ANALOG INDUT		32 = 32 WORDS	included with	LPS - 16 -10B \$1245.
			anab unit	
= 0V to -5V		64 = 64 WORDS FX = FXTERNALLY	each unit.	LPS - 16 - 12B \$1295.
$EULL$ SCALE ANALOG INPUT $= 0V$ to $-5V$ $2 = \pm 5V$, inverted analog $3 = 0$ to $+ 5V$ $= \pm 5V$, conventional		EX = 64 WORDS EX = EXTERNALLY CONTROLLED FILE LENGTH	TAPE CASSETTE	MODEL 12123-1 \$ 9.95 SSETTE MODEL TC-1R \$35.00

GSA Contracted: Datel's products are available both direct and through the General Services Administration (GSA). If you are connected with a military or federal agency or receive federal funds, you may be entitled to purchase Datel's data loggers and other products through GSA to expedite requisitioning and order processing. Datel's data loggers are covered under FSC Group 66-56, Part II, Section K, Contract GS-00S-29002



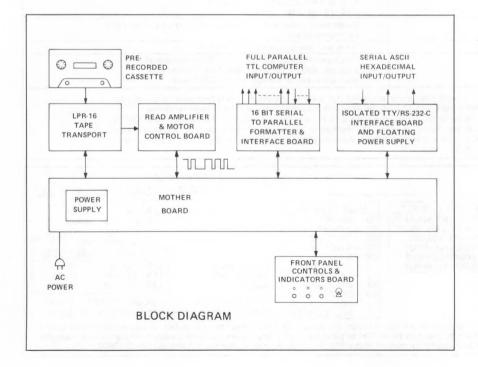
CASSETTE TAPE READER/INTERFACE FOR MODEL LPS-16 DATALOGGER

LPR-16 CASSETTE READER

FEATURES

- Digital Tape Cassette Reader for the 16-channel battery-powered LPS-16 Data Logger
- Full parallel interface to minicomputer or mainframe processor
- Teletypewriter/RS-232-C serial I/O interface
- Selectable I/O loading and logic coding for complete data buss compatibility
- Complete "handshaking" computer controls and flags for "on-line" external control
- Tape-to-Tape Interface for ½" 7/9 track tape transports
- Open collector parallel interface can be multiplexed with other I/O devices sharing common data bus





GENERAL DESCRIPTION

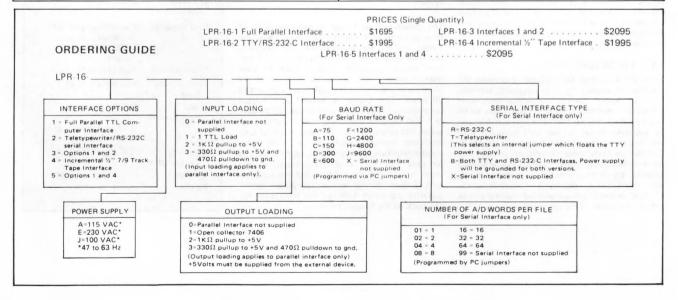
The LPS-16 Data Logger tape cassettes, containing up to 16 channels of analog data can be fed directly into a minicomputer or mainframe processor using the LPR-16 Cassette Reader. The LPR-16 will also simultaneously connect directly to a teletypewriter or RS-232C I/O device. The LPR-16 has two side-by-side interface card slots with identical pinout so that two interfaces can be simultaneously connected.

A special feature of the LPR-16 is selectable positive or negative true coding of the TTL outputs and a variety of input/output loading for full compatibility with an external minicomputer data bus.



LPR-16 CASSETTE TAPE READER SPECIFICATIONS (Typical @+25°C unless otherwise noted) For Full Parallel TTL Computer Interface.

GENERAL		LOGIC INPUT CHARACTERISTICS (Computer Interface)		Computer Interface)	
Function		Logic Levels TTL Compatible		mpatible	
Media	. Standard Phillips-type certified digital	2011/07/25/6		"0" = (L	O) = 0 to +0.8 volts
	tape cassette				(1) = +2.0V to +5.0 volts
Number of Tracks	. Two	Input Loadi	na		one TTL load, or 1 TTL
Tape Motion	One direction, capstan stepper motor	input Loudi			h 1K Ω pullup to +5V, or
	drive	 These encoders. 			
Tape Speed					ad with 330 pullup to +5V
Reading Format		and 470 Ω pull down to ground.			2 pull down to ground.
Reading Density		LOGIC INPUTS (Computer Interface)			
		Start Input 1 line, positive true			
Bit Rate		Start Input 1 line, negative true		egative true	
Bit Capacity	2.2 million bits per cassette (including	OUTPUT	EVEL		1
	all gaps)			OUTPUT	The output Level
Word Length	. 8, 12 or 16 bits		LINPUTS	CODING	Control Inputs control
Record, Word or		1	2		the coding of most
Intercharacter Gap		1	1	POS. TRUE	outputs as shown in
File gap		1	0	NEG. TRUE	the chart – see the
	Any (Standard is 64 words per file)	0	1	Jammed LO	listing of outputs.
Power Required	100, 115 or 230 VAC, 47 to 63 Hz,	0	0	ONE'S*	*With both Output
	60 Watts max.		0	ONE 5	Level Control Inputs at
LOGIC OUTPUT CHARACT	ERISTICS (Computer Interface)	zero, most o	utputs who	se coding is cont	trolled by these inputs
Logic Levels	TTL compatible	will have cu	toff open co	ollectors. In this	state, external open
2,301 (54)	''0'' = (LO) = 0 to +0.4 Volts	collector devices sharing the same data buss lines as the LPR-16			
	"1" = (HI) = +2.4V to +5.0 Volts	may be mult	iplexed ont	o these lines.	
Output Loading		CONTROLS AND INDICATORS			
Output Loading	7406 TTL Hex driver or with 1K Ω	Power On/C			
	pullup to +5V	Switch)			ower on and off. Illuminates
	or with 33012 pullup to +5V and 47012			entre tra	wer is on.
-	pulldown to ground	EOT/BOT (LED indicat		tes when on clear leader
Output Coding	Selectable positive or negative true	Load Forwa	rd (Pushbut	beginning	g of tape or at clear end of tape.
	coding using Level Control Inputs.	and the second sec			d to cause tape to load
LOGIC OUTPUTS (Compute	Interface)	ownedd,			from clear leader to oxide
(All outputs are selectable as	positive or negative true unless	1			of tape. (EOT/BOT lamp
otherwise noted.)		And the second			nguish over oxide).
Data Format	16 lines: Normally 12 A/D lines and 4	Domind (Du	hhutten au		d to cause tape to rewind to
Duturomut	address lines. However a 16 bit digital	Newind (Fus	induction sw		
	word can also be used.				ning of tape clear leader.
Word Sync Output					es when the tape is in motion.
	1 line, normally flags every 64 words.				es while tape is rewinding.
sectors and a part standard to the standard to		Run/Standb	y (Toggle Sv		"RUN", tape will contin-
Rewind Status Output				1	ad. When in "STANDBY"
Busy Status Output					read one file each time the
Load Forward Status					switch is depressed.
Output	1 line	Start (Pushb	utton Swite		standby mode, this switch will
Cassette-in-Place Status					e file to be read each time it is
Output				depressed	ł.
Head Down Status Output		Size		19"W x 5	5.25"H x 19"D (16.25"
EOT/BOT Status Output	1 line			chassis wi	idth)
Shift Clock Output	1 line, positive pulse	Connector T	уре	Dual 25/	pin PC Brd type, 0.1" Cen-
Tape Clock Output	1 line, positive pulse	and the second second		the second se	cing 3VH25/1JN-5 (1 in-
Serial Data Output	1 line, positive true, NRZI coding	a second second second		cluded wi	ith unit)
		COLUMN TO MAKE			



DATEL

Data Logger 2: A New Instrument for Field Data Logging



Scientists and industrial researchers have long required a battery-powered, portable multichannel analog recording system for long term unattended data logging of slowly varying signals. The power and long-term requirements have been particularly difficult to achieve in a portable commercial instrument. Many applications in meteorology, pollution monitoring, oceanography, biomedicine, geophysics and natural resource exploration require an instrument which can literally be left in the field to run on its own batteries, recording slowly changing data unattended for up to a year.

SYSTEM DESCRIPTION

Datel System's new Data Logger 2 provides the missing link needed for a remote analog recorder with an output system compatible with most computer systems. Using this system, up to 64 analog inputs derived from physical variables can be displayed or printed out on a computer with the date and time of each measurement. Up to 120,000 separate measurements or samples can be recorded using a single digital magnetic tape cassette. By using a suitable computer program, each input can be displayed — identifying the physical quantity being measured — and properly offset and scaled to the correct engineering units.

In this way the Data Logger 2 system and computer will print out the day, hours, minutes and seconds, and then the actual measurement (i.e. temperature in degrees F, wind speed in miles per hour, etc.). Connected to a set of sensors, the sealed Data Logger 2 makes an ideal weather station, geophysical monitor, or oceanographic buoy data acquisition and recording system.

The complete Data Logger 2 system consists of three separate instruments: the Data Logger, the Tester, and the Reader/Interface. The Logger is the data acquisition and write-only digital cassette recording system. It runs from its own internal battery and makes scans of up to 64 channels at preselected intervals from 1 second to 30 hours. The Logger is housed in a rugged weatherproof metal case and weighs 20 pounds (9,1 Kg). Analog inputs are connected through sealed I/O connectors on the case. A typical data recording system consists of one Tester, one Reader/Interface, and several Loggers deployed for data collection at different locations. The tester is taken to the field to test and calibrate each Logger during set-up; completed digital cassettes are taken back to the laboratory for playback on the Reader/Interface.

DATA LOGGER 2 TESTER

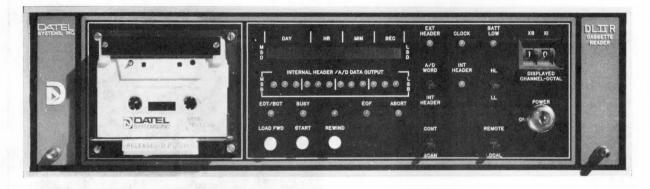
The Tester is used to calibrate the Logger and to test all its functions before it is committed to long-term unattended recording. The tester checks all controls of the Logger, the battery status (voltage and current), Logger power drain, and tape heads. Simulated data generated on the Tester can be recorded on the Logger. The Tester will also display actual data or the simulated data on the Tester's LED readouts. In addition the Tester performs a complete self-check of all its own switches, displays, and batteries. The Tester is housed in a portable weatherproof case identical to that of the Logger.

READER/INTERFACE AND INTERFACE OPTIONS

The Reader/Interface for the Data Logger 2 system is a complete computer front end for playing back the digital cassettes recorded on the Logger. The Reader can be operated from front panel controls or can be remotely controlled

KEY SPECS: DATA LOGGER 2

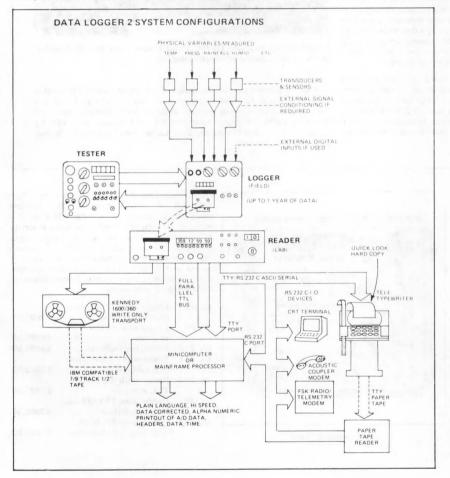
No. Observation	11
No. Channels	Up to 64
Analog Inputs, HI Level	0 to +5V or -5V to +5V (Single Ended)
Analog Inputs, LO Level	0 to +10mV or -5mV to +5mV
	(Differential)
Input Impedance	100 Megohms
Common Mode Voltage Range	±5V
Common Mode Rejection	110dB
Resolution	12 Bits, Hi Level
	8 Bits, Lo Level
Accuracy, HI Level	.04%FS ± 1/2 LSB
Temperature Coefficient	±12 ppm/°C
Data Capacity	120,000 samples/300' Cassette (2000 64 Channel Scans)
Scan Intervals	1 Second to 30 hours
Throughput Rate	5 samples/second
Power	12VDC (5 Lithium
Requirement	D-Cells)
	(100mA Recording, 1mA standby)
Operating Temperature Range	-20° C to +70° C
Weight	20 lbs. (9,1Kg)



Data Logger 2 Reader

on-line by a minicomputer, mainframe processor or other I/O device. Front panel displays allow the operator to manually step through a recording to find a sample on a particular date and time. Front panel binary and decimal LED's will display this date and time in addition to the raw binary data for that sample on a selected channel. By suitable computer programming an automatic search for a particular sample can be conducted.

The Reader is available with one of three interface types. A full parallel interface provides buffered TTL binary data at rates up to 100 samples per second with the cassette tape moving



continuously. This interface provides the highest output rate and may be used to load a computer memory in interrupt mode or block transfer (direct memory access).

7.

The second interface is full serial (2 wire) to connect to teletypewriters and RS-232-C I/O devices such as CRT terminals and high speed printers in ASCII format. The teletypewriter (TTY) output provides a simple way to connect to a computer which has a TTY port. The teletypewriter can be used off-line to prepare paper tapes of the raw data and to get a "quick look" at the data. Feeding the paper tape back to the computer on-line will then produce a plain language print out with suitable programming. The RS-232-C outputs may also operate an acoustic coupler modem for telephone transmission or frequency-shift keying of a radio link. The TTY/RS-232-C serial interfaces are programmable from 75 to 9600 baud rates to accommodate different output devices and transmission lines.

The third Reader interface connects to a Kennedy 1600 incremental 1/2" magnetic tape transport. Tapes prepared using this transport may be played back at high speed on any 7/9-track mainframe processor tape deck. This tape-to-tape interface provides simplified no-wiring data entry to a computer and user retention of the data on a high speed tape medium.

Various user configurations of the Data Logger 2 system are shown in the "Data Logger 2 System Configurations" diagram.

LOGGER OPERATION

The Logger and Reader both employ Datel Systems' low power stepper-motor incremental cassette tape transport. This transport features very fast power turn-on permitting the transport to be normally off except during actual recording. Extensive use of fast turn-on circuits using MOS devices allows the Logger to operate for a year or longer (depending on sample rate) using only 5 D cell Lithium batteries mounted inside the front cover. While recording, the tape transport and data acquisition electronics are powered up for only 11 seconds maximum to record all 64 channels. The system then turns off except for a

The Data Logger 2 Story

The conception and development of Data Logger 2 goes back a little over a year, and culminates on September 18, 1975 when Robert L. Hill, developer of the unit, received an IR-100 award from Industrial Research Magazine at its awards banquet. The awards are given annually for the 100 most significant new products developed during the past year. Products are selected by a distinguished panel of judges on the basis of importance, uniqueness, and usefulness, from a technical standpoint.

The Data Logger 2 design was conceived out of customer interest in another Datel Systems product, the LPS-16, an OEM type low power digital cassette recorder with built-in data acquisition system (see product description on page 10). Mr. Hill found that many customers were interested in a complete packaged instrument for field use and indeed were using the LPS-16 to build such units themselves. The field model needed to have features such as these: high and low level analog inputs: low temperature operation; low power consumption to permit extended unmanned field operation; provision for external digital inputs in addition to analog inputs; provision for recording operator identifying information on the cassette; and internal data/time clock to record when data was taken. The companies who expressed interest in such a system, which was not available from any other manufacturer were in such diverse fields as oil exploration, mining, oceanography, meteorology, and ecology. A further important requirement was a ruggedized all-weather type enclosure for field environment.

Robert Hill designed the Data Logger 2 based on these customer requirements, using the low power incremental cassette recorder of the LPS-16 along with low power CMOS circuitry. A key part of this design is the crystal-controlled CMOS clock which runs at 2.1MHz continuously while the Logger is in the standby mode; total current drain is typically 500 μ A in standby. While running and recording the current drain is typically 75 mA.



Robert L. Hill receiving IR-100 award plaque from Tim Burkholder, publisher of Industrial Research magazine.

Another important part of the design effort was the search for suitable internal batteries for field operation. Lithium batteries in D cell size were finally chosen based on their superior characteristics: operation down to 65° F, 10 ampere-hour capacity, and 10 year shelf life. By using just 5 of these D cells the Data Logger 2 can operate for a year, unattended in the field.

initiates the next scan at the time determined by the manually selected scan rate. During each scan the data and time are automatically recorded on the cassette tape. A battery monitor will record if the battery voltage falls too low.

The Logger is rated for a year or more of operation at moderate sample rates over an operating temperature range of -20° C to $+70^{\circ}$ C. External inputs may be used to record 36 bit parallel digital data on command or to make an analog scan on external command.

Both high and low level analog inputs are accepted with unipolar, bipolar, or two's complement coding on the 12 bit A/D converter. The high level ranges are -5V to +5V or 0 to +5V; low level ranges are 0 to +10mV or -5mV to +5mV with 8 bit accuracy. The low level inputs are differential with 100 meghom input impedance, \pm 5V common mode range, and 110dB common mode rejection out to 100 Hz. Basic high level accuracy is \pm .04% of full scale \pm 1/2 LSB with a temperature coefficient of \pm 12ppm/°C.



Data Logger 2 Tester

During recording the Logger draws a maximum 100 mA of current from its 12V Lithium batteries; between scans only the crystal clock is running, drawing just 1 mA maximum. A variety of power options may be used with Data Logger 2 including external AC, or +12VDC. In addition the internal battery holders may be rewired to accept rechargeable D cell nickel cadmium batteries or other types of D cells. Sample prices for Data Logger 2 systems are:

DL-2A	Logger with 32 high level channels	\$3995.00
DL-2E	Logger with 64 low level	00000.00
	channels	\$4995.00
DL-2T2	Tester, less calibrator	\$3495.00
DL-2T1	Tester with 12 bit + sign	
	D/A calibrator	\$3995.00
DL-2R1	Reader with full parallel	
	TTL interface	\$3495.00
DL-2R2	Reader with TTY/RS-232-	
	C serial interface	\$3895.00
DL-2R4	Reader with 7/9-track,	
	1/2" Mag. tape interface	\$3895.00



DATA LOGGER 2 64-CHANNEL, BATTERY-POWERED, WEATHERPROOF CASSETTE DATA LOGGER

MODEL DL-2

FEATURES

- 64 channel cassette digital tape data acquisition system in a sealed weatherproof, high reliability ruggedized metal case
- One year lithium battery supply
- ► -20°C to +70°C operating temperature range
- +10mV, ±5mV or ±5V, 0 to +5V Volt input ranges, 100 megohm impedance, 100dB CMR differential configuration
- 6mW standby power CMOS design, 1 watt power while scanning, +12VDC power
- 1 second to 30 hour selectable scan rates
- ▶ \$3995. single quantity



GENERAL DESCRIPTION

For remote environmental recording or long term unattended field measurement of any variable, the battery powered Data Logger 2 will record up to 64 channels of analog data on a Philips-type digital tape cassette. The Data Logger 2 is housed in a sealed, weatherproof ruggedized metal case and will operate for more than a year on its internal lithium battery supply in temperatures from -20°C to +70°C. Military type sealed connectors are used for all analog inputs and CMOS circuitry is employed for a low standby drain of 6 milliwatts.

Philips-type digital cassettes with 300 feet of tape are used to record analog data in selectable scan lengths from 1 second to 30 hours. The number of channels to be scanned is preset on front panel thumbwheel switches for efficient use of the tape. The incremental single direction NRZI recording method combined with low power electronics results in a running current of 100mA max. In addition, a header word may be recorded on the tape for later computer indentification of that particular tape. A longer 36-bit external header may be entered using the input connectors. In each scan of the selected number of input channels, a 40-bit clock word is recorded before each scan. This 40-bit clock word contains a 36-bit one-year digital clock derived from a CMOS crystal oscillator and having one second resolution. The last 4-bits of the clock word are used to flag a low battery voltage. The system will continue running with a low battery voltage but the user is advised that readings may be unreliable.

A normal scan consists of the clock word, a 12-bit file gap and a string of 14-bit data words up to 64 channels.

The 14-bit data words consist of an analog voltage represented by 12 binary bits and 2 additional high level/low level bits to describe whether full scale is ± 5 millivolts or 5 volts. A 2-bit character gap begins each word.

The Data Logger 2 can accept up to 64 high level or 64 low level channels or a mix of 32 high level and 32 low level channels. Full external control of the Data Logger 2 is also provided using the input connectors. This includes such flexibility as varied scan rate

for selected inputs by using a second external clock and control circuit.

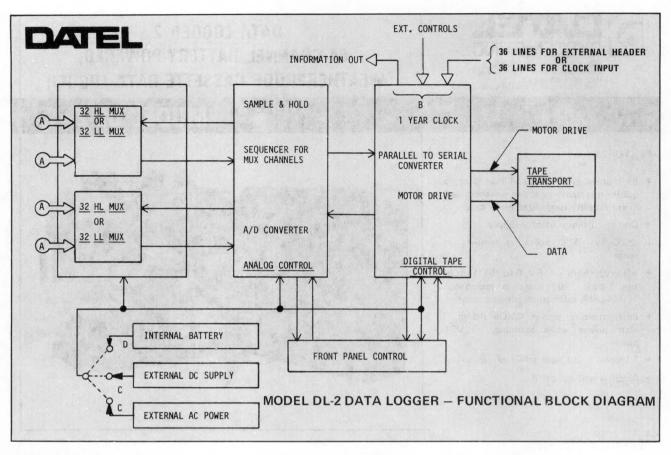
A 5-cell, long life, 10 Amp-hour lithium battery supply is mounted on the front inside cover of the Data Logger 2. A second set of D-size battery holders allows rewiring to alkaline, mercury or carbon-zinc batteries or for a parallel set of lithium batteries, or any other D cells.

The internal CMOS circuitry of the Data Logger 2 features fast power turn-on initiated by the clock control. An MOS high accuracy analog multiplexer is followed by a differential FET front end instrumentation amplifier for low level inputs. A fast acting sample and hold amplifier is followed by a 12-bit A/D converter at the output. The parallel A/D words are then assembled and formatted into serial information fed to the tape head driver amplifiers. Motor stepper drive circuits, clock and control/ addressing systems complete the electronics.

The instrumentation amplifier provides low level differential inputs down to 10mV span full scale. Common mode rejection of 110dB is maintained over $\pm 5V$ for high noise immunity. Overall accuracy (high level) is $\pm .04\%$ of Full Scale $\pm 12ppm/^{\circ}C$ temperature drift. Low level accuracy is $\pm 0.3\%$ of Full Scale $\pm \frac{1}{2}$ LSB (8 bits) $\pm 100ppm/^{\circ}C$ tempco. (See specifications)

The sample and hold exhibits a 100 nsec. aperture time and A/D settling and conversion occurs within 450 microseconds. The tape is stepped at 100 bits per second so that A/D words are written in 160 msec. (120 msec. for the 12-bit data, 20 msec. for the High Level/Low Level bits and 20 msec. for the intercharacter tape gap). A complete recording of a 64-channel scan takes about 11 seconds. This limits the maximum sampling rate unless a smaller number of channels is selected. Tape capacity is about 2 megabits including all gaps. About six hours is required to fill a tape at continuous running.

The complete system weighs 20 lbs. (9, 1 Kg) with batteries and measures $12''H \times 12'W \times 10''D$ (305 mm x 305 mm x 254 mm).



DATA LOGGER 2

Specifications (Typical over -20°C to +70°C unless otherwise noted)

Number of Analog Channels:

Selectable up to 64. Can be mixed up to 32Low Level and 32 High Level channels or up to 64 High Level or Low Level channels.

Power Supply:

+14.75 Volts DC composed of (5) D-size Lithium cells, non-rechargeable, +2.85 to +2.95 Volts per cell. 10 Amp-hours per cell. (10) D-size battery holders provided for customer conversion to NiCad, Alkaline or Carbon-Zinc D-cells, or for a parallel set of Lithium batteries.

Power Supply Requirement:

12V (-.5, +1V):

70 mA typ, 100mA max during motor stepping

 $10\mu A$ typ, $100\mu A$ max during standby

Power Supply Operating Range:

+10 Volts to +14.5 Volts DC. Low battery flag is encoded on tape when voltage drops to +11 Volts or +5.5V at low power supply tap. However, system will continue operating down to +10 Volts at rated specifications.

Battery Power Usage:

Approximately 615mA-Hrs. per cassette.

AC Supplies: (optional)

115VAC ±10% 100VAC ±10%

230VAC ±10%

AC Line Frequencies:

47 to 440 Hz

External Battery Supply:

Connected through sealed I/O connectors. System Weight:

20 lbs. (9, 1Kg)

Dimensions:

 $12^{\prime\prime}H$ x $12^{\prime\prime}W$ x $10^{\prime\prime}D$ (305mm x 305mm x 254mm) System Temperature Ranges:

Operating: -20° to +70°C Storage: -55°C to +70°C

DATA LOGGER 2:

Analog Specifications (Typical over -20 $^\circ\text{C}$ to +70 $^\circ\text{C}$ unless otherwise noted)

Input Ranges:

Low Level differential -5mV to +5mV or 0 to +10mV, (Other LL ranges >10mV span available on special order). High Level single-ended -5V to +5V or 0 to +5V.

Input Impedance:

 \geq 100 megohm single-ended or differential.

```
CMV:
```

±5V (differential only) CMRR:

110dB to 100Hz (differential only with 1K source unbalance). Accuracy:

(High Level) $\pm.04\%$ of Full Scale (± $\frac{1}{2}$ LSB) + (±0.0012%/°C). Accuracy:

(Low Level) ±0.3% of Full Scale (± ½ LSB 8 bits) + (±0.01% FS/°C) + (.002%/°CxGain*).

*Where gain = 10 volts \div FS LL Input Range.

Resolution:

12 binary bits

Aperture Time:

100 nanoseconds max. (sample & hold). A/D Conversion Time: (including input settling time)

450 microseconds.

Sample Time:

150 microseconds.

- Input Connection (Differential, Low Level):
- Analog HI, Analog LO and shield ground for each input. (Single-Ended, High Level): Analog HI and ground

Overvoltage:

±10V (HL)

±5V (LL)



DATA LOGGER 2

Recorder Characteristics

Storage Media:

Standard Philips certified data tape cassette 300' length (91 m). Storage Method:

2 channel complementary NRZI, one recording direction. Storage Density:

615 bits per inch.

Number of Tracks:

Two, data on Track one, data on Track two.

Tape Format:

40-bit digital clock word, 12-bit file gap and one scan of 14 bit binary A/D words (up to 64 A/D words). Internal header 12 bits (4 digit octal) written from front panel push button and 4 digit thumbwheel switch. External header 36 bits written from external source and strobe. (parallel data).

Gaps:

2 bit gap written before every 14 bit A/D word, (12 bit A/D word +2 bit HL/LL Channel ID) 12 bit gap written after every clock or header word (Int. or Ext.)

Tape Storage Capacity:

2.2 megabits (gaps are considered as bits) per 300 ft. cassette. Write Speed:

100 steps/sec. (one bit (data gap)/step). Incremental.

Data Format:

Serial NRZI

Motor:

Single 1.5° angle capstan drive stepper motor coupled to take up reel by slip clutch mechanism.

Capstan:

.250" diameter

Step Angle: 1.5

Angular Accuracy:

±8 min. of arc non-accumulative.

Tape Motion Control:

Single capstan pinch roller. Drive head is engaged mechanically during write time.

Tape Tension:

0.4 oz.

Error Rate:

1 bit in 10⁷

Type of Cassette Loading:

Front (after instrument housing sealed front cover is opened). **Recording Head:**

Dual channel single gap high quality digital type.

Operating Mode:

Write only.

FRONT PANEL CONTROLS:

Scan Rate:

1, 2, 5, 10, 20 or 30 seconds, minutes or hours and max. (Max. is maximum rate allowed by the setting of the scan length switches), to nearest second resolution.

Scan Length:

Four digit octal thumbwheel switch selects the number of channels/scan. (Two digits for High Level and two digits for Low Level), or (two switches for CH-1-32 and two switches for CH33-64 for all HL or LL channels).

Header (Octal):

Four digit octal thumbwheel switch may be entered on tape. (Same switch as scan length).

Enter Internal Header: (Int./Ext.)

Push button switch enters front panel header on tape. (When in the Ext. Mode). Locking toggle switch. When in Int., the Internal Clock has control of the Data Logger via the scan length switches. (Except in between scans, external data may be entered). When in the Ext. position, the logger may be externally controlled; also an Internal Header or External Header may be entered.

Load Forward:

Push button switch will light BOT (Beginning of tape) lamp if tape is over clear leader and will move tape forward to oxide while depressed. (When in the EXT. Mode).

BOT Lamp:

Will indicate, (when load forward button is depressed) when tape is on clear leader. Lamp is on when over clear leader and off when over oxide coating on tape.

Clock Reset:

Push button switch, will reset 1 year internal clock to zero. (When in the Ext. Mode).

Power On/Off:

Toggle switch will turn the power on or off.

Analog Input Selector:

Four position selector switch selects High Level/Low Level, or High Level and Low Level channels to be scanned.

There is also an Ext. position which is used for optional external control of thse functions.

DATA LOGGER 2 **Digital Inputs**

NOTE: CMOS logic levels used. External CMOS driver logic should be used and should track Vdd logic bus from the 3-cell tap or drive through protective external diodes. (Avail. from Ext. connector). 22K ohm pulldowns on all external digital inputs, 1 uSec min.

Clock Inputs:

36 lines for pre-setting internal 1 year digital clock or for entering External Header.

Load Clock:

1 line presets internal clock to comply with 36 line input. Enter Header:

1 line enters External Header. Must be spaced 500 mSec min. from adjacent scans.

Start Scan:

1 line will cause a clock to be written and a word scan to occur (used for external calibration or control). One microsecond minimum duration.

DATA LOGGER 2 **Digital Outputs**

Status Output:

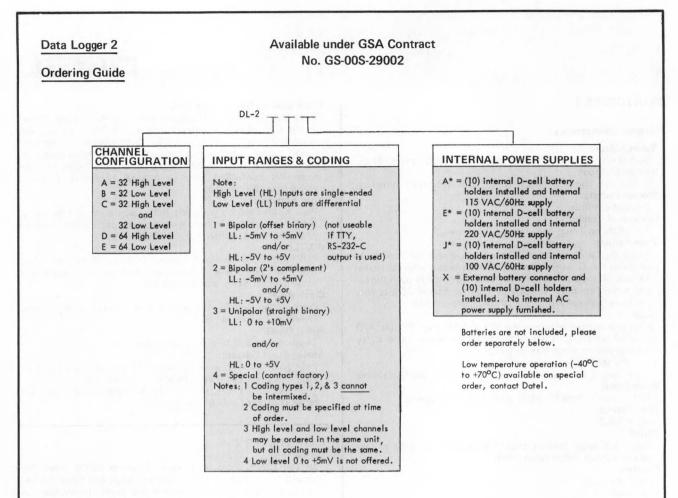
1 line, indicates when system is busy. This line is used if external data is to be written in between scans. 36 bits of external data may be entered on tape from the external header inputs, provided time is allowed by selecting the proper scan rate position for the number of channels to be scanned, plus the 36 external bits. i.e.: it takes 450 ms to write the 36 bits on tape.

Clock Output:

1 line, 1 second time base.

Head Track 1 & 2:

4 lines, represent data written on Track 1 and Track 2 respectively. When the Data Logger 2 Tester is used, these lines are used to recover data from the Head to be displayed on the Tester.



Data Logger 2

Prices (single quantity)

indes (single quantity)			
DL-2A	(32 HL)	\$3995.	
DL-2B	(32LL)	\$4245.	
DL-2C	(32HL & 32LL)	\$4745.	
DL-2D	(64 HL)	\$4495.	
DL-2E	(64LL)	\$4995.	

"Naked DL-2": (Panel-mounting version of any model above less housing and connectors --- less \$1000.



*Add \$175. for A, E, or J power supply options.

Prices include connectors and a cassette but do not include Lithium batteries.

Lithium batteries are D-SIZE "Eternacell" Model 550 manufactured by:

Power Conversion Inc. 70 Mac Questen Parkway South Mt. Vernon, NY 10550 or available from Datel, part number DL-2-12049-24, \$15.00 each. (5 required)

Certified digital tape cassettes, 300 feet (91 m)

Model	Operating Temp.	Price (1-9)
12123-1	+10°C to +45°C	\$ 9.95
12123-2	-40°C to +70°C	\$11.95

PRICES & SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE.



DATA LOGGER II READER DIGITAL CASSETTE TAPE READER

MODEL DL-2R

FEATURES

- Digital tape cassette reader for the 64channel Data Logger II.
- Displays digital calendar clock, binary A/D data words, int. octal or ext. digital header words.
- Provides full parallel computer data buss interfacing or 7/9 track ½" IBM tape interface.
- Also provides teletypewriter (TTY) RS-232-C I/O serial interface.
- Selectable I/O TTL loading and coding options for complete data buss compatibility.
- Complete "handshaking" computer controls and flags, for automatic external computer control, or "off-line" front panel control.



GENERAL DESCRIPTION

Digital cassette tapes written on the Data Logger II containing up to 64 channels of analog data may be read directly on the Data Logger II Reader, model DL-2R. This reader accepts Philips-type tape cassettes written in Datel's NRZI digital format. Information recorded on tape such as temperature, pressure, rainfall, and wind velocity from external sensors may be transferred directly into a mainframe computer or minicomputer data buss using the DL-2R Cassette Reader.

The Data Logger II Reader has two front panel displays, one to list 12 bit binary A/D data words and another decimal display for the calendar clock or external header word. The 9-digit calendar clock in the Data Logger II records up to one year of data with one-second resolution. Using clock words, the DL-2R Reader can be stepped through manually or by computer control to find a particular record written at any time. The binary display also shows octal internal headers and the decimal display can be used for external digital header words.

The Data Logger II Reader has complete front panel controls to select the channel of interest, to properly start the tape and load data into a computer. A complete full parallel computer interface and/or serial teletypewriter/RS-232-C interface is included inside the 19" x 19" x 5¼" cabinet of the DL-2R. The full parallel computer interface features open collector TTL bussing including a variety of output loading and selectable positive or negative-true coding. This flexibility enables universal connection to majority

of digital processors without any modifications.

The serial teletypewriter/RS-232-C interface directly connects to a variety of I/O devices such as CRT terminals, and mainframe computers accessed by remote TTY terminals.

The DL-2R Reader contains special handshaking functions for full computer compatibility. These include word sent and word taken signals and an abort flag which stops the Reader if transmitted words are not accepted 3 times in succession.

Another important feature of the DL-2R Reader is that it connects directly to a variety of Datel data acquisition/processing systems. These include connection to a local, "quick-look" teletypewriter terminal with or without arithmetic capabilities. Another option is direct connection to an IBM compatible 7 or 9-track ½" tape drive. The DL-2R Reader with the Datel processor will correctly format the serial information being read from the cassette tape.

The housing of the DL-2R Reader is brushed aluminum and is 54'' high, 19'' deep, and 19'' wide. It can be rack mounted or set up for stand-alone, table top configuration. The DL-2R Reader is complete and includes AC power supplies for 115/60, 220/50 or 100/60 power voltages.

Cassette tapes are mounted directly on the front panel tape deck. The system can be completely operated through the front panel controls or remotely by computer or teletypewriter terminal.

The complete system weights approximately 25 pounds.



DATA LOGGER 2 CASSETTE TAPE READER

MODEL DL-2R

SPECIFICATIONS (Typical @ +25°C unless otherwise noted)

GENERAL

Function Re	ad Only
MediaSta	andard Philips-type certified digital tape cassette
Number of Tracks	/0
Tape Motion On	e direction, capstan stepper motor drive
Tape Speed 2.7	75 inches per second
Reading Format Co	mplementary NRZI
Reading Density61	5 bits per inch
Bit Rate	00 bits per second
Bit Capacity 2.2	? million bits per cassette (including all gaps)
Record, Word or Intercharacter Gap 2	bits
File Gap 12	bits
Power Required	5/100/230 VAC 47 to 63Hz (specify) 65W max.
Mechanical Dimensions 19	"D x 19"W x 5.25"H (48,3 cm x 48,3 cm x 13,3 cm)

TAPE DATA FORMAT

The DL-2R Reader is designed to respond to the tape data format of the Model DL-2 Data Logger II data acquisition/recording system.

The Data Logger II normally records a full scan starting with a 40-bit clock word, 12 bit gap and up to 64 channels of 12 bit binary A/D words. The exact tape format of the Data Logger II is as follows:

- 2 bit Intercharacter gap 36 bit Calendar clock word
- 4 bit Battery low voltage flag
- 12 bit File gap
- 2 bit Intercharacter gap
- 12 bit Binary A/D data word
- 2 bit High Level/Low Level flag
- 2 bit Intercharacter gap
- 12 bit Binary A/D data word
 - •

.

Up to 64 12-bit A/D data words and 2 bit HL/LL flags and 2 bit gaps per scan.

Note that intercharacter gap, word gap, tape gap and interrecord gap all refer to the 2 bit gap.

The Data Logger II Reader is designed to decode the calendar clock word first and to stop and display this word in the 12-bit file gap. This allows an operator to decide if he wishes to select a particular A/D word in that scan for display. When the system is under external computer control the same sequence applies. That is, the computer decodes each calendar clock word in its search for a particular channel at a given time.



LOCAL MODE

In the Local mode all of the front panel controls and displays may be utilized. They are:

CONTROLS

Local/Remote: Toggle Switch Continuous/Scan: Toggle Switch High Level/Low Level: Toggle Switch A/D or Internal Header Word: Toggle Switch Load Forward: Momentary Switch Start: Momentary Switch Rewind: Momentary Switch Power: ON/OFF key lock switch (key removable in either ON/ OFF position). Displayed Channel (Octal): 2 Octal thumbwheel switches. Channel to be displayed.

INPUT LINES

There are 10 input lines to the Computer Interface Board, they are:

- 1) Level Control Status Output 1 (L Cont 1 Stat Ø)
- 2) Level Control Status Output 2 (L Cont 2 Stat Ø)
- 3) Level Control Data Output 1 (L Cont 1 Data Ø)
- 4) Level Control Data Output 2 (L Cont 2 Data Ø)
- 5) Level Control, Control Input 1 (L Cont 1 I)
- 6) Level Control, Control Input 2 (L Cont 2 I)
- 7) Initialize Input (Init I)
- 8) Word taken Input (WDT I)
- 9) Start Input (STRT I)
- 10) External Rewind

The Level Control Lines determine the logic coding (positive or negative true) of all I/O signals. The 3 sets of these inputs are: Status Output Level Controls, Data Output Controls, and Control Input Level Controls.

LOCAL/REMOTE

When the DL-2R Reader is in the "Local" mode, it is operated from its own front panel controls. In the "Remote" mode, the system is operated by an external computer and its own front panel controls are inoperative except for the Local/Remote switch.

DISPLAYS

7

Internal Header: LED Lamp EOT/BOT: LED Lamp

Busy: LED Lamp

Rewind: LED Lamp Abort: LED Lamp

Clock (ID): LED Lamp

Battery Low: LED Lamp

End of File: LED Lamp

Segment Display

External Header (ID): LED Lamp

A/D or Internal Header Readout: 12 LED Lamps

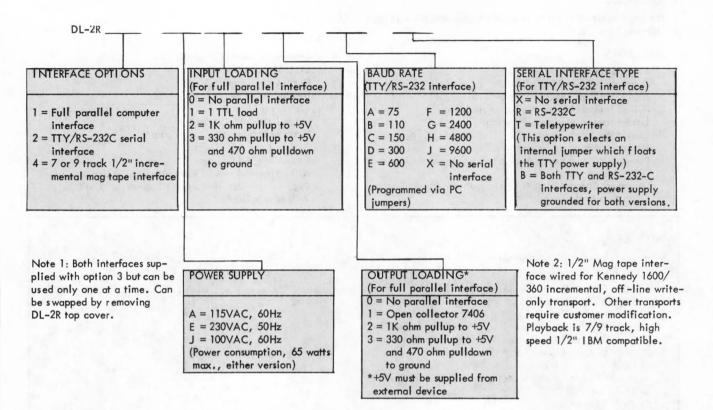
External Header or Clock Readout: 9 Digit

PROGRAM SEQUENCE

When the DL-2R Reader is externally controlled by a "Remote" computer, the program will ordinarily begin its chores by initializing the Reader. This involves checking to see that a number of conditions are met in the proper sequence.

The program will poll various status output lines to see if the cassette is in place, if the head is down, the end of file status, rewind not in progress, local/remote switch position and EOT/BOT status. If all conditions are met, the initialize sequence will begin, proceeding with a Load Forward onto the tape oxide and a Start command if the computer is ready to accept data. Operation then proceeds with simple exchanges of controls between the computer and the DL-2R Reader. The Reader assembles a word in its output register and flags its Word Ready control output. Assuming the computer's input register is ready to accept data, the Word Ready signal will strobe this register and the computer will return a Word Taken signal to the Reader. The return of the Word Taken signal is to inform the DL-2R Reader that the computer is continuing to process data words. The computer also returns a Start signal to keep the tape moving or to start it again if it has stopped in a file gap waiting for the Word Taken signal.

ORDERING INFORMATION



Price for the DL-2R Cassette Reader/Display/Interface are as follows:

DL-2R-1	with full parallel computer interface \$3495.00
DL-2R-2	with TTY/RS232C serial interface \$3895.00
DL-2R-4	with 7 or 9-track ½" tape interface

Covered by GSA Contract No. GS-00S-29002





BATTERY-POWERED, WEATHERPROOF PORTABLE TESTER/CALIBRATOR FOR THE DATA LOGGER 2 MODEL DL-2T

FEATURES

- Completely exercises and calibrates all functions of the Data Logger 2 weatherproof analog cassette recording system.
- Functionally tests all displays and the A/D converter.
- Tests all batteries under full operational load.
- Contains A/D and Digital clock readouts for full calibration and presetting of the Data Logger 2.
- Operates from built-in lithium battery supply or AC power supply.
- Performs a complete self-test to ensure proper Tester operation.

DESCRIPTION

The Data Logger 2 weatherproof, battery-powered data acquisition and cassette data-logging system will normally require a complete system check-out before committing it to prolonged unattended data monitoring. In addition, the Data Logger 2 will occasionally need on-site field calibration to establish its accuracy. The ideal instrument to perform these tests and calibration is the Data Logger 2 Tester, model DL-2T.

The DL-2T Tester is particularly valuable because it tests the Data Logger 2 and itself. The DL-2T Tester completely exercises the Data Logger 2 on location and performs a self-check to be sure all internal systems are functioning properly in the Data Logger 2.

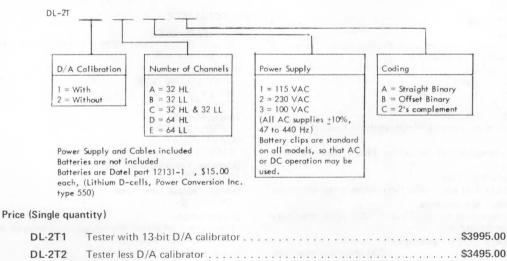


When testing the Data Logger 2, the DL-2T Tester provides input control signals to recover data directly from the head of the cassette transport. Data is displayed on one of two readouts on the front panel of the DL-2T Tester.

To ensure a complete test of all systems, the DL-2T Tester operates from the internal lithium battery power supply of the Data Logger 2 with the exception of display lamps and drivers powered by a separate 6 volt battery in the DL-2T Tester, or from the internal AC power supply.

The Tester has 2 basic operating modes. In the Logger Mode, the Data Logger 2 is tested. In the Tester Mode, the DL-2T tests itself.

ORDERING INFORMATION

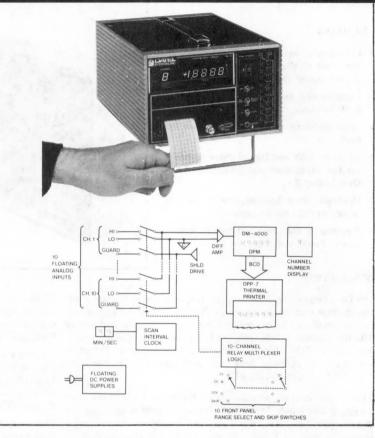




PRINTING DATA LOGGER

MODEL PDL-10





DESCRIPTION

Meeting the demand for a high performance laboratory-grade printing data recorder, Datel's model PDL-10 Printing Data Logger accepts up to 10 floating analog input voltages and automatically prints them out at preselected intervals. The PDL-10 digitizes all selected inputs to 41/2 digit accuracy, displays and prints them out as decimal voltages on a very compact inkless thermal printer. Analog inputs are accepted over ±199.99mV, ±1.9999V and ±19.999 Volt front-panel selected voltage ranges and are printed out every second with the channel number at preselected scan intervals.

PDL-10 SPECIFICATIONS

ANALOG INPUT

Number of Channels
Configuration 3-Wire differential inputs, transformer-isolated using a mechanical relay multiplexer.
Input Voltage Ranges Choice of 3 DC ranges: ± .19999V, ± 1.9999V, ± 19.999V
- resoluted by ten front need alide suitable for each sharped

preselected by ten front panel slide switches for each channel. Overvoltage

Input is diode-protected for up to ±100V maximum continuous.

Common Mode Rejection

108dB, DC to 60 Hz with 1000 Ω maximum input unbalance. Common Mode Voltage Range

±20 volts maximum to signal guard. ±300 volts maximum to AC power ground.

Input Impedance (±20V input max)

(To Signal Guard) 100 Megohms minimum. **Input Bias Current** 500pA typ., 8nA maximum

PERFORMANCE

Accuracy @ +25°C

Within ±0.01% when calibrated due to all effects except temperature drift.

- Resolution 10 µV (200mV range) 100 µV (2V range) 1mV (20V range)
- **Temperature Drift** ZERO: $\pm 1\mu V/^{\circ}C$ GAIN: 20ppm/°C BIAS CURRENT: 1%/°C

Operating Temperature Range 0°C to +45°C

Storage Temperature Range -25°C to +85°C

Sampling Rate

Pre-selected channels are advanced, displayed and printed one channel per second.

Scan Intervals

Intervals from 00 to 99 seconds or minutes

DISPLAYS

Input

Å digital panel meter (DPM) displays the analog input voltage using Light Emitting Diode red digits. The digits are 0.43" high (11 mm) and 4½ digit resolution. Decimal points, overscale, and polarity (\pm) are automatically printed and displayed.

Channel

A single 0.43" (11 mm) red LED digit indicates channel 0 through 9.

Printing Method

Seven segment digits are formed on thermal paper using a thick-film resistor matrix printhead requiring no ink, hammers or ribbons.

Printer Digits

 $7\text{-segment 0 to 9 digits } 0.155^{\prime\prime}$ (4 mm) high. Spacing between printed lines: 0.2 inch (5 mm).

Line Capacity

Approximately 9000 lines.

Printout Format

Printout format is $9\pm$.1.9.9.9.9 with the leading digit indicating channel number. Three lines are skipped between scans.

Printing Paper

Using heat sensitive thermal printing paper, 1.75"W (44, 5 mm) and supplied in rolls 150 feet (45 mm) long.

FRONT PANEL CONTROLS

Channel Select and Input Range

(Ten 4-position slide switches) ",2V, 2V, 2VV and SKIP". "SKIP" prevents the multiplexer relay for the channel from cycling.

Scan Interval

(Two decade thumbwheel switch) Sets the time interval between scan starts from 00 to 99 seconds or minutes.

Minutes/Seconds

(2 position toggle switch) Determines whether the Scan is set for minutes or seconds.

No Print/Run/Reset & Start

(Three position toggle switch) In NO PRINT, the instrument scans and displays but does not print. In RUN the instrument scans, displays and prints out.

In RESET & START, the scan timer is reset and starts timing. One scan is printed out one second from switch release.

One Channel/Scan

(Two position toggle switch) The ONE CHANNEL position prevents the multiplexer relay for the selected channel from disconnecting with each scan. In the SCAN position, normal relay cycling, display and printout occur.

Paper Quantity

A lever indicates relative quantity of paper remaining.

REAR PANEL INPUT CONNECTIONS

Analog input voltages are connected using screwdriver barrier terminal strips. (30 terminals).

POWER SUPPLY

Choice of 115 or 230 VAC \pm 5, 10, 15 or 20 volts at 50 or 60 Hz only. Power voltages and frequency may be rewired by the user. Three-prong grounded U.S. captive line cord supplied. Power consumption (all models) 30 watts, typical.

PHYSICAL DIMENSIONS

Mounting

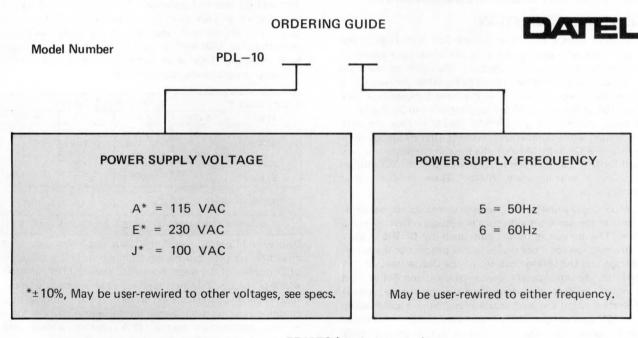
Bench-top mounting with tilt-up stand and mar-proof plastic feet. Users can remove the feet and stand for optional $\frac{1}{2}$ -rack mounting.

Outline Dimensions

5.25"H x 8.5"W x 12"D (133 x 216 x 305 mm)

Weight

12 pounds (5,5Kg)



PRICES (single quantity)

PDL-10......\$1195.00



COMPUTER COMPATIBLE DATA ACQUISITION/ DISTRIBUTION SYSTEM

SYSTEM 256

INTRODUCTION

System 256 is a complete high reliability computer inputoutput system for analog signals. It is capable of operating *on-line* or *off-line*. It has been designed to provide a versatile and permanent solution to the problem of interfacing analog signals to and from a digital computer. The modular principle used throughout enables the user to realize the most economic solution to any problem while maintaining maximum flexibility. Further expansion to an initial system is made by plug-in cards.

A wide range of options outlined elsewhere in this catalog allows a comprehensive system to be specified for applications to an instrumentation or control problem.

System 256 offers the flexibility, speed, economy and reliability necessary in today's world of real time applications.

It can function as an interface between an analog and digital computer in hybrid computer systems or as a peripheral device for general purpose digital computers.

It fills a growing need in industrial process control systems.

The ability to mix Analog Multiplexers, A/D's, Sample and Hold amplifiers and D/A's in virtually any configuration makes System 256 a valuable and dynamic systems tool.

GENERAL DESCRIPTION

The most unique feature of System 256 is its large analog input channel capacity while at the same time providing extremely low power consumption. The power consumed is a fraction of any system offered today while providing four times the channel capacity in the same package area. System 256 offers up to 256 analog channels and 32 Digital-to-Analog channels in a 19"Wx19"Dx3.5"H rack mounted enclosure, while competitors' systems offer 64 analog channels and 8 Digital-to-Analog channels in the same area, and still System 256 consumes less power. System 256 utilizes C/MOS (Complementary Metal Oxide Silicon) logic throughout.

C/MOS logic provides the necessary high-speed capability while at the same time drastically reduces power consump tion. The quiescent power consumed by C/MOS logic i: extremely low, or more precisely, the product of the supply voltage and the leakage current of the device (measured ir pA). Its dynamic power consumption is somewhat more complex in that it is dependent on the supply voltage operating speed and load capacitance. With a supply voltage of +15V operating at IMHz into 15pF, the dynamic power consumption per logic function is approximately ImW. When this is compared with TTL logic at approximately 10.5mW per logic function, both quiescent and dynamic, it can be seen that a considerable reduction in power dissipation throughout the system will result by using C/MOS logic rather than TTL or DTL logic. The advantages of this low power dissipation in the system are obvious - less drift due to temperature rise, smaller power requirements, no cooling required, and more hardware per area.



SYSTEM DESCRIPTION

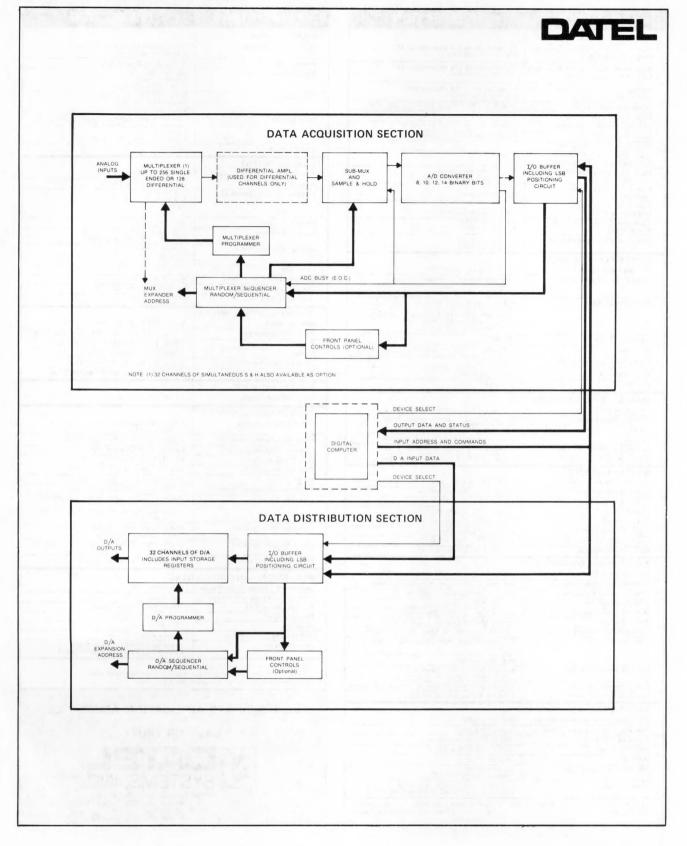
System 256 is designed to accept up to 256 single-ended or 128 differential analog signals plus 64 simultaneous sample & hold channels in the basic package. The analog inputs are multiplexed one at a time into a high Impedance buffer amplifier then supplied to a sample & hold amplifier. The buffered analog signals are converted to digital data via a high speed successive approximation Analog to Digital Converter of up to 14 bits. The analog multiplexing process may be accomplished in either a sequential scan or a random address mode of operation. The digital output data is then fed to an LSB (least significant bit) positioning circuit which assures that regardless of the resolution of the converter, the LSB will always be on the extreme right hand position. This is in compliance with most minicomputer programming requirements.

THROUGHPUT		A/D RES	OLUTION	
TIME	8 Bits	10 Bits	12 Bits	14 Bits
100 KHz	\checkmark	V (opt)	√ (opt)	
70 KHz 50 KHz	E.	\checkmark	\checkmark	
17 KHz				\checkmark

Display and Control in both the Local and Remote mode of operation are provided on the front panel. This includes an LED display of digitized input data and A/D-D/A channel address. The Local Control features allow selection of input A/D channel address via an advance pushbutton switch, continuous conversion cycles on the same channel via a convert pushbutton switch, D/A channel address and manual insertion of D/A data via toggle switches.

Contained in the same package are provisions for supplying up to 32 Digital to Analog Converters. This conversion process again utilizes the LSB positioning circuit and is supplied with C/MOS storage registers. The Digital to Analog Converters accept up to 12 binary bits and generate an analog output corresponding to the selected channel. Four standard voltage range outputs are supplied to provide up to 10 milliamperes.

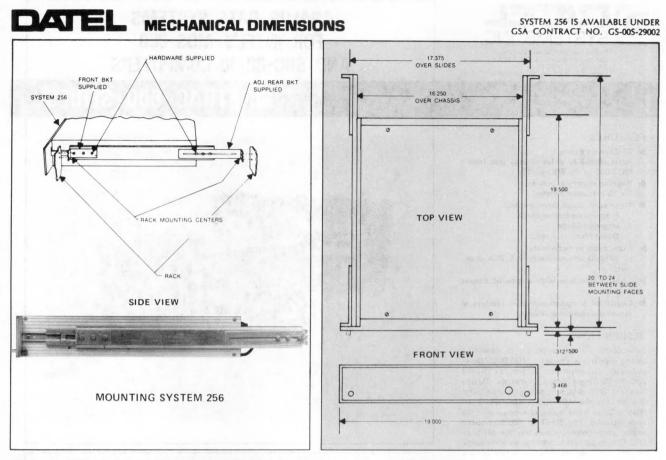
SYSTEM 256 BLOCK DIAGRAM



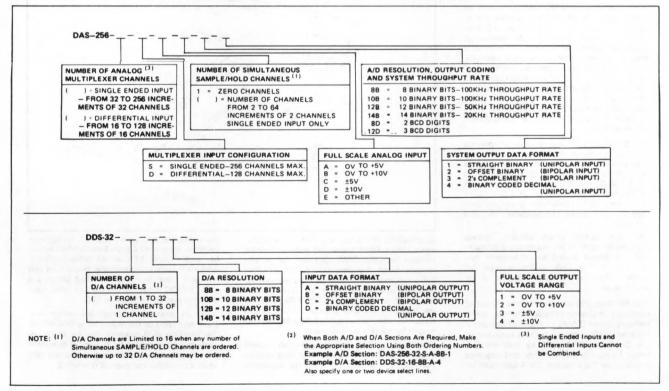
SYSTEM 256 SPECIFICATIONS

PARAMETER	A/D SECTION
ANALOG INPUTS	
Number of Multiplexer Channels Single Ended Input	Expandable to 256 channels in 32 channel increments
Number of Multiplexer Channels Diff. Input (Optional)	Expandable to 128 channels in 16 channel increments
Number of Simultaneous Sample/Hold Channels	Expandable to 64 channels in 2 channel increments
Input Voltage Ranges	+5V FS, + 10V FS, ± 5V FS, ± 10V FS
Channel Input Acquisition Time	5usec to ± 0.025% of FS
Channel Input Impedance	100 Megohms—''on'' or ''off''
Input Configuration	Single ended or Differential
Maximum Input Overload Input Channel Time Skew	± 15V 50 nsec
Simultaneous S/H Section	
Maximum Common Mode Voltage — (3)	Any Combination of 20V P to P - Es + ECM
Common Mode Input	
Impedance — (3) Common Mode Source	>100 Megohms
Impedance — (3)	1 Kohms unbalanced
Common Mode Rejection	60db @ 1 KHz 80db @ 60 Hz
Ratio — (3) Crosstalk (Between inputs)	80db @ 100 Hz
	45db @ 10MHz
SYSTEM PERFORMANCE	and the second
Output Resolution	8, 10, 12, 14 binary bits
Output Data Coding(4)	Straight Binary — unipolar input Offset Binary — bipolar input 2's Complement — bipolar input
Throughput Rate	
rinoughput nate	8 Binary Bits—100 KHz 10 Binary Bits—50 KHz 10 Binary Bits—70 KHz (opt.)
	12 Binary Bits-50 KHz 14 Binary Bits-17 KHz
Aperture Time	50nsec
Accuracy	± 0.02% of FS + 1/2 LSB
Temperature Coefficient	40ppm/°C
Throughput Rate	up to 100 KHz
Linearity	± ½ LSB
DIGITAL CONTROL INPUTS	
Device Select	1 line, 1 TTL Load—Negative True
Random/Sequential	1 line, 1 TTL Load-Negative True (seq.
Reset	1 line, 1 TTL Load-Negative True
Strobe	1 line, 1 TTL Load-Negative True
Convert Command Input Random Address Inputs	1 line, 1 TTL Load—Negative True 9 lines, 1 TTL Load—Negative True
DIGITAL OUTPUTS	
A/D Converter Data	Up to 14 parallel lines-TTL Compatible (1
Serial Output Train	1 line-TTL Compatible (1)
Busy (E.O.C.)	1 line-TTL Compatible (1)
Frame Sync A/D Clock	1 line-TTL Compatible (1) 1 line-TTL Compatible (1)
Input Strobe Output	1 line-TTL (Compatible (1)
Output Strobe Output	1 line-TTL Compatible (1)
Buffer Full Output	1 line-TTL Compatible (1)
FRONT PANEL CONTROLS	
Output Data Display	Up to 14 Bits of A/D Data Read Out
Channel Address Switches	Address Multiplexer in Random Mode Display Multiplexer Position
A/D Mode Switch	Selects A/D Operation
A/D Convert Switch	Will Initiate an A/D Conversion
Reset Switch	Resets Multiplexer to Channel One
Random/Sequential Switch Advance Switch	Selects Multiplexer Mode of Operation Random Mode—Will Select Addressed
	Channel
	Sequential Mode—Will Advance to Next Higher Channel
Local/Remote Switch	Selects Source of System Control. Front Panel Controls or Computer
Last Channel Selector	Short Cycle Multiplexer in Sequential Mo
Power ON/OFF Switch	Applies AC power to System
MECHANICAL-ENVIRONMEN	TAL
Operating Temperature Range	0°C to +70°C
Storage Temperáture Range	-55°C to 85°C
Relative Humidity	10% to 90% Non-condensing
Physical Size Weight	3 ¹ / ₂ " H x 19"W x 19"D 12 LBS (Typ.)
I/O Mating Connectors	Up to Eleven
	Viking #3VH25/IJN5
Input Power	115VAC + 10 VAC @ 47-63Hz 225 VAC + 15 VAC @ 50-400Hz (opt.)
(1) Open Collector. Will Sink 30	ma (3) Pertains only to Differential Inp
(2) Optional	(4) Contact Factory for Binary Cod

xpandable to 32 channels in channel increments
channel increments
, 10, 12, 14 Binary Bits
traight Binary ffset Binary
wo's Complement
TL or TTL compatible egative True Logic oading: one TTL Load
formation must be present at the egister inputs of the DAC prior to
robing. oading: one TTL Load
00 KHz
p to 32 channels 0.01% of FS ± 1/2 LSB
V to + 10V FS V to + 5V FS 10V FS 5V FS
10ma (typ.)
Kohms for + 10V Output 00 ohms for + 5V Output
usec to ±0.025% of F5
1 LSB
1/2 LSB
20ppm/°C of FS 0.01%/6 month period
0.01%/6 month period
line, 1 TTL Load-Negative True
line, 1 TTL Load-Negative True (seq.
line, 1 TTL Load -Negative True
line, 1 TTL Load-Negative True
line, 1 TTL Load - Negative True
lines, 1 TTL Load—Negative True
line, TTL Comp. (1)
llows Manual Loading of Data Into
Each D/A ddress D/A's in Random Mode
hisplay D/A Channel Position
elects D/A Operation
/ill Initiate a D/A Conversion
esets D/A's to Channel One
elects Mode of Operation andom Mode—Will Select Addressed Channel
equential Mode—Will Advance to Next Higher Channel.
elects Source of System Control. ront Panel Controls or Computer.
hort Cycle D/A Channels in Sequential Mode
pplies AC Power to System
AL
°C to + 70°C
55°C to + 85°C 0% to 90% Non-condensing
1/2"Hx19"Wx19"D
2 LBS (Typ.)
iking #3VH25/IJN5
15VAC+10VAC @ 47. 63Hz
15VAC±10VAC @ 47- 63Hz 25VAC±15VAC @ 47-63Hz (opt.)



SPECIFYING SYSTEM 256 TO MEET YOUR PARTICULAR NEEDS





ANALOG DATA SYSTEMS FOR INTEL'S MDS-800 AND SBC-80/10 COMPUTERS

SINETRAC 800 SERIES



- 32-Channel analog
- input capability slides directly into Intel's MDS-800 or the SBC-80/10. Register-to-register interface
- for 75 kHz data transfer.
- Three methods of programming: Program-controlled mode Interrupt Mode **Direct Memory Access**
- Expandable in increments
- of 32 A/D channels and/or 8 D/A channels.
- 12-bit Resolution with choice of output coding.
- Choice of program-controlled random or sequential channel addressing.

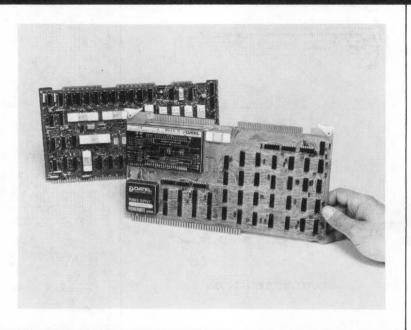
DESCRIPTION

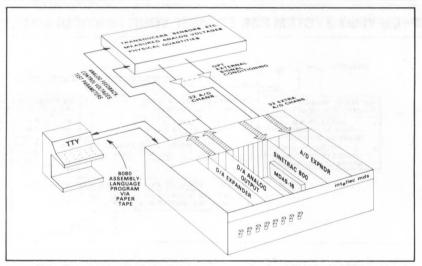
Datel offers a simple approach to measuring analog inputs via the Intel MDS-800 Microcomputer Development System or Intel's SBC-80/10 Single Board Computer. Datel's SineTrac 800 data acquisition module plugs directly into the MDS-800 or SBC-80/10, accepting 32 or more analog channels inside the same housing. The SineTrac 800 high-speed analog card communicates on the MDS or SBC CPU bus and is handled as an addressable peripheral I/O device. Analog connections are made through convenient rear-panel connections on the MDS-800 housing. Programs written in universal 8080 microprocessor assembly language instructions completely control all activities of the SineTrac 800 data acquisition card. These include random or sequential channel addressing with automatic reset on user-specified first and last channels. By using the I/O device communications capability resident in Intel's monitor program, the SineTrac 800 analog inputs can be directly printed out on a teletypewriter, punched onto paper tape or magnetic tape cassette or left in memory for further arithmetic manipulation before printout.

The SineTrac 800 card is ideal for process control, automatic test systems, laboratory measurement systems and similar applications. Additional SineTrac 800 boards allow for (1) A/D channel expansion in increments of 32 channels per board or (2) a D/A board with eight 12-bit D/A analog output converters per board (expandable to 256 channels).

The D/A option board contains storage registers for each 12-bit analog word to maintain a stabilized analog output between output cycles. The D/A option is ideal for plotter, chart recorder, oscilloscope or actuator drive.

The SineTrac 800 can accept three modes of operation including program control, direct memory access (DMA) or interrupt operation. Program mode consists of direct operation of the SineTrac 800 system by assembly language instructions at the time and sequence specified by the program. DMA operation ac-



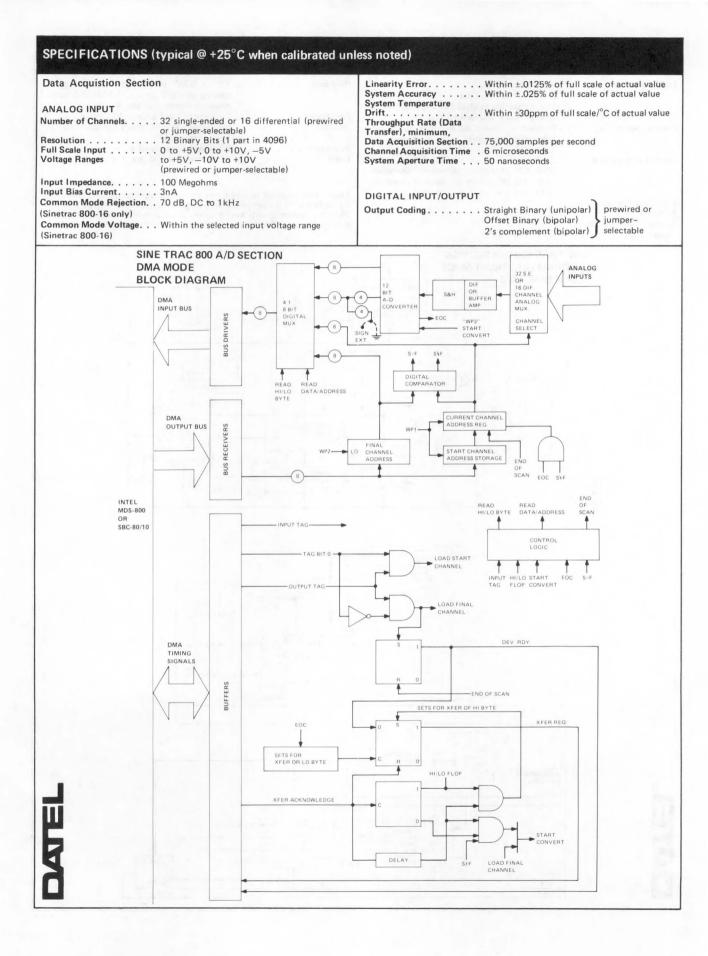


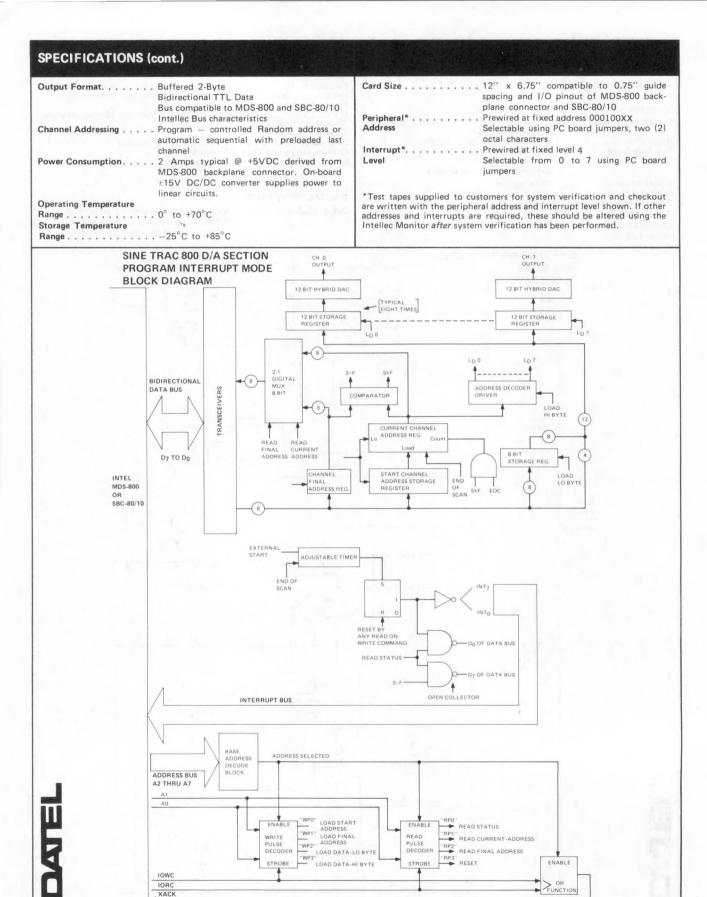
commodates direct memory loading in blocks using Intel's DMA board but without routing through the CPU. DMA operation can accommodate block transfers up to the SineTrac 800's full speed of 75,000 samples per second. Interrupt operation is ideal for serving other peripherals besides the SineTrac 800 whenever the device or the data is ready. Interrupt can accept virtually simultaneous data conversion, output formatting and printout.

The SineTrac 800 card is organized around Datel's MDAS-16, a high density data acquisition module employing a hybrid successive

approximation A/D converter, FET multiplexer switches, integrated circuit Sample/Hold amplifier and tri-state TTL output buffer/registers. Address decoders, bidirectional bus drivers and receivers, status registers, FET MUX switches, a ±15V DC/DC converter and control logic complete the rest of the SineTrac 800.

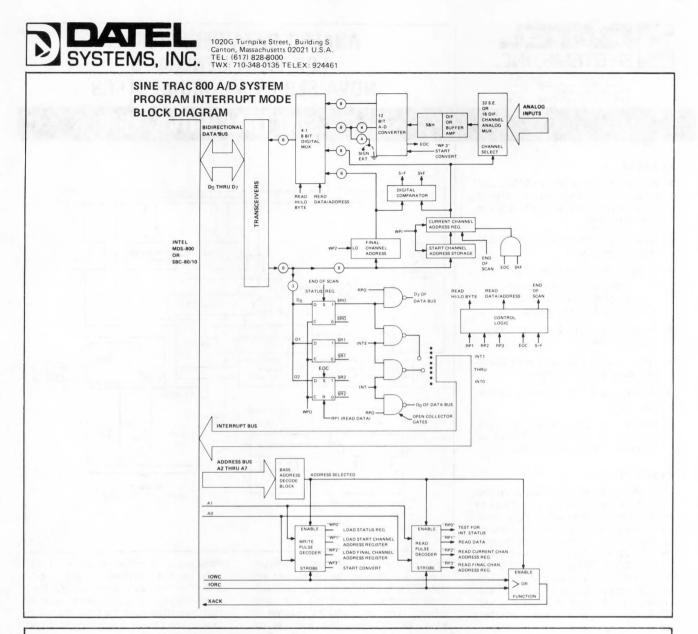
Using an assembly language application program developed on the MDS-800 or SBC-80/10, the SineTrac 800 channels can be randomly addressed or in automatic sequential operation incremented with each conversion and resetting when a preloaded last channel is reached.

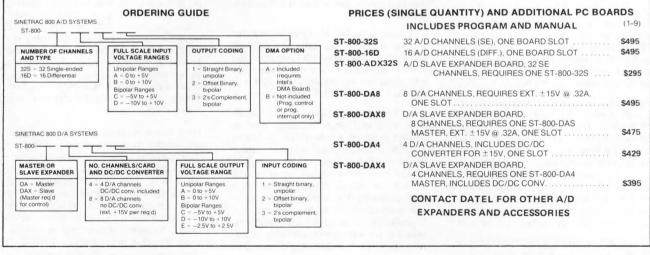




Vol 3/262

Electronic Design's







ANALOG DATA PERIPHERALS FOR DATA GENERAL'S NOVA SERIES MINICOMPUTERS

SINETRAC NOVA SERIES

FEATURES

- 64-channel analog input (A/D) and 4 output (D/A) channels fit directly inside Data General's NOVA series minicomputers.
- Data Acquisition rates up to 75,000 samples per second.
- Three modes of programming.
 - Program-controlled mode
 - Program-interrupt mode
 - Direct Memory Access
- Expandable up to 256 A/D and /or 256 D/A channels.
- 12-bit analog resolution with choice of coding and voltage ranges.
- Optional auto-zeroing and programmable gain.
- Includes on-board control for block transfer and automatic channel sequencing and for random channels.

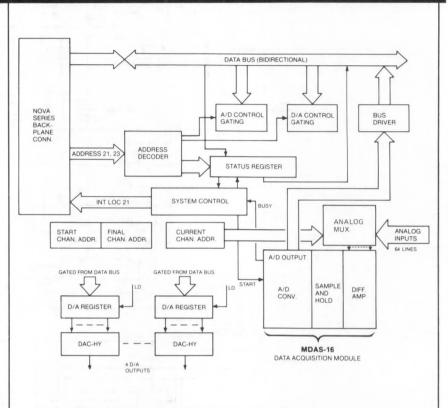
DESCRIPTION

Datel offers a simple approach to providing analog signal inputs and outputs to Data General's popular NOVA series minicomputers. Datel's Sine Trac analog peripheral I/O module plugs directly into the card guides and connector slots inside NOVA, NOVA 800, 1200 and Super NOVA housings. The Sine Trac module accepts up to 64 analog input (A/D) channels and 4 analog output (D/A) channels on the same interface card.

The Sine Trac analog I/O card communicates directly with the NOVA bidirectional bus, thereby, eliminating all CPU cabling. Sine Trac is handled as an addressable peripheral I/O device. Analog connections are made through PC board connectors to the NOVA housing.

Assembly language or high level languages completely control all activities of the Sine Trac analog I/O card. These include random or sequential analog channel addressing with automatic reset on program-specified first and last channels. By using the appropriate I/O instructions, Sine Trac analog channels may be transferred to a teletypewriter, paper or magnetic tape, tape cassettes, CRT terminal or other peripherals.

The Sine Trac board is organized around Datel's MDAS-16, a high density data acquisition module employing a hybrid successive approximation A/D converter



FET multiplexer switches, integrated circuit Sample/Hold amplifier, and tristate TTL output buffer/registers. Address decoders, bidirectional bus transceivers, status and address registers, a ±15V DC/DC converter and control logic complete the rest of the Sine Trac system.

The Sine Trac NOVA card is ideal for process control, automatic test systems, laboratory measurement systems and similar applications. Datel's System 256 will allow for expansion up to 256 A/D channels and/or 256 D/A channels.

The D/A analog output channels available on Sine Trac A/D boards contain storage registers for each 12-bit analog word to maintain a stable analog output between CPU output cycles. The D/A option is ideal for plotter, chart recorder, oscilloscope or actuator drive. It is also excellent for analog feedback or test waveforms to systems under test. Digitally synthesized analog waveforms may be program-generated with a settling time of 4 microseconds per D/A step.

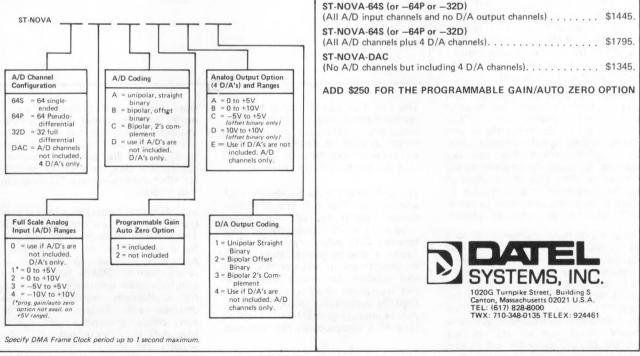
The Sine Trac analog system can accept

three modes of operation including program control, program interrupt mode and direct memory access (DMA). Program control requires simple instruction sequences and controls the interface at the time and sequence specified by the program. Interrupt operation is ideal for releasing the CPU for other chores while an A/D conversion is in progress, DMA operation bypasses the CPU and uses the Sine Trac's start and final channel and word counter registers to transfer Sine Trac-controlled blocks of data addresses sequenced by the Sine Trac's memory address register and frame clock.

Very fast auto zeroing circuits and programmable gains are optional on Sine Trac systems. The auto zeroing corrects for voltage offsets and programmable gains of 1, 2, 5, and 10 provide input ranges down to ±500mV full scale. The gain is program controlled and is ideal for applications requiring extended range. Systems without the auto zero/ programmable gain option have A/D data throughput of 75,000 samples per second. Throughput for systems with the option is 40,000 samples per second.

SPECIFICATIONS (Typical @ +25°C, dynamic conditions unless otherwise specified.)

SINETRAC NOVA SERIES	DYNAMIC CHARACTERISTICS	PHYSICAL
SINETRAC NOVA SERIES ANALOG DATA SYSTEMS DATA ACQUISITION SECTION (A/D Analog Inputs) ANALOG INPUTS Number of Channels 64 single-ended 64 pseudo-differential 32 full differential 32 full differential 128 full differential channels or 128 full differential channels or 128 full differential channels or 128 full differential channels in an external housing] Input Voltage Ranges 0 to +5 Volts 0 to +10 Volts -5 to +5 Volts -10 to +10 Volts Programmable Gains and Auto zero (optional) x1, x2, x5, x10 (not	DYNAMIC CHARACTERISTICS Throughput Rate [withour prog. gain/auto zero]	Operating Temperature Range 0°C to +70°C Storage Temperature Range -25°C to +85°C Card Size 15″ x 15″ x 0.375″ (not including PC card fingers). Card Connection One peripheral 1/O slot in Nova Series backplane connector Humidity 20% to 90% (no condensation) DATA DISTRIBUTION SECTION (D/A Analog Outputs) ANALOG OUTPUTS
avail. 0 to +5 Volt range) Common Mode Range ±10V Volts - guaranteed max. Input Overvoltage, Ind damagei	Channel Addressing RANDOM - Under interface DMA control or under interface DMA	Number of Channels 44 single-ended Channel Expansion 256 channels addressable using Datel's System 256 (separate housing) Output Voltage Ranges 0 to +5 Volts 0 to +10 Volts -5V to +5 Volts* -10V to +10 Volts* -10V to +10 Volts* 0 utput Impedance 50 milliohms Output Current ±5mA, min., short circuit
Gain Error Adjustable to zero Offset Error Adjustable to zero Gain Temperature Within ± 30ppm of full Drift scale/°C Offset Temperature Within ±7ppm of full Drift scale/°C Common Mode Rejection Y0 dB min., DC to 1 kHz Power Supply Rejection 100 dB	channel, final channel, number of channels and next memory address registers. DMA Frame Clock Selectable period up to 1 second per channel (specify with order) INTERFACE ADDRESSING NOVA Sine Traces are supplied with addressing shown below. Contact Datel if other addressing is required. A/D System Device Address	PERFORMANCE Nonlinearity
ORDERING GUIDE Nova Sine Trac Series ST-NOVA	PRICES (Single Quanti ST-NOVA-64S (or64	



GOLD BOOK 76/77



ANALOG DATA PERIPHERALS FOR DEC LSI-11 MICROCOMPUTERS

SINETRAC LSI SERIES

FEATURES

- 64-channel analog input (A/D) and 2 output (D/A) channels fit directly inside DEC's LSI-11 series minicomputer.
- Data acquisition rates up to 75,000 samples per second.
- Two modes of programming.
 - · Program-controlled mode
 - Program-interrupt mode
- Expandable up to 256 A/D and/or 256 D/A channels.
- 12-bit analog resolution with choice of coding and voltage ranges.

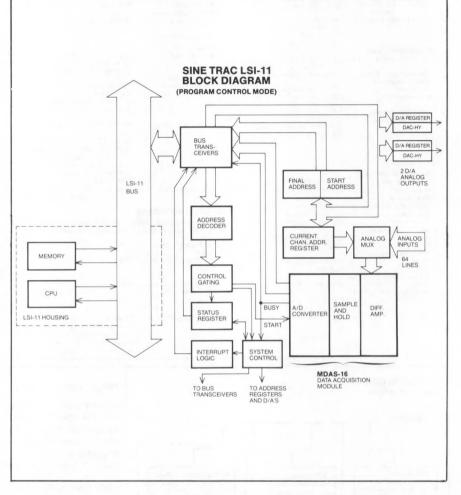
DESCRIPTION

Datel offers a simple approach to providing analog signal inputs and outputs to DEC's popular LSI-11 (PDP-11/03) series microcomputers. Datel's Sine Trac analog peripheral I/O module plugs directly into the card guides in LSI-11 housings or H9270 backplanes. The Sine Trac module accepts up to 64 analog input (A/D) channels and 2 analog output (D/A) channels on the same interface card.

The Sine Trac analog I/O card communicates directly with the LSI-11 bus, thereby, eliminating all CPU cabling. Sine Trac is handled as an addressable peripheral I/O device. Analog connections are made through PC board connectors on the Sine Trac card.

Assembly language or high level languages completely control all activities of the Sine Trac analog I/O card. These include random or sequential analog channel addressing with automatic reset on program-specified first and last channels. By using the appropriate I/O instructions, Sine Trac analog channels may be transferred to a teletypewriter, paper or magnetic tape, tape cassettes, CRT terminal or other peripherals.

The Sine Trac board is organized around Datel's MDAS-16, a high density data acquisition module employing a hybrid successive approximation A/D converter, FET multiplexer switches, integrated circuit Sample/Hold amplifier, and Tristate TTL output buffer/registers. Address decoders, bidirectional bus transceivers, status and address registers, a \pm 15V DC/DC converter and control logic complete the rest of the Sine Trac system.



The Sine Trac LSI-11 card is ideal for process control, automatic test systems, laboratory measurment systems and similar applications. Datel's System 256 will allow for expansion up to 256 A/D channels and/or 256 D/A channels.

The D/A analog output channels available on Sine Trac A/D boards contain storage registers for each 12-bit analog word to maintain a stable analog output between CPU output cycles. The D/A option is ideal for plotter, chart recorder, oscilloscope or actuator drive. It is also excellent for analog feedback or test waveforms to systems under test. Digitally synthesized analog waveforms may be program-generated with a settling time of 4 microseconds per D/A step.

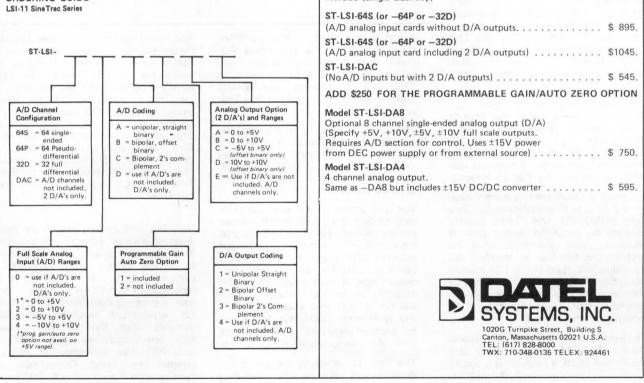
The Sine Trac analog system can accept two modes of operation including pro-

gram control, and program interrupt mode. Program control requires simple instruction sequences and controls the interface at the time and sequence specified by the program. Interrupt operation is ideal for releasing the CPU for other chores while an A/D conversion is in progress.

Very fast auto zeroing circuits and programmable gains are optional on Sine Trac systems. The auto zeroing corrects for voltage offsets and programmable gains of 1, 2, 5, and 10 provide input ranges down to \pm 500mV full scale. The gain is program controlled and is ideal for applications requiring extended dynamic range. Systems without the auto zero/programmable gain option have A/D data throughput of 75,000 samples per second. Throughput for systems with the option is 40,000 samples per second.

SPECIFICATIONS (Typical @ +25°C, dynamic conditions unless otherwise specified.)

NALOG DATA SYSTEMS	DYNAMIC CHARACTERISTICS	DATA DISTRIBUTION (D/A Analog Outputs)
PECIFICATIONS (Typical @ +25°C, dynamic conditions unless otherwise specified.)	Throughput Rate (without prog. gain/auto zero)75,000 samples/sec., max. Throughput Rate (with prog. gain/auto zero)	ANALOG OUTPUTS Number of Channels 2-single-ended Channel Expansion 256 channels addressable using Datel's System 256 (separate
ATA ACQUISITION SECTION (A/D Analog Inputs) NALOG INPUTS Number of Channels 64 single-ended 64 Pseudo-differential 25 full differential 25 full differential channel Expansion up to 256 single-ended channels (using Date's System 256 in an external housing) Input Voltage Ranges 0 to +5 Volts 0 to +10 Volts -5 to +5 Volts -0 to +10 Volts Programmable Gains and Autozero (optional)x1, x2, x5, x10 (not avail. 0 to +5V range) Common Mode Range ±15V, max. sustained Input Impedance 100 megohms differential or to ground Input Bias Current 3nA typical, 10nA max. Input Capacitance (to ground)	A/D Conversion Time 7.3 microseconds Aperture Time	housing) Output Voltage Ranges 0 to +5 Volts 0 to +10 Volts -5V to +5 Volts ' -10V to +10 Volts -5V to +5 Volts ' 'offete binary or 2's complement, specify when ordering] Output Current
(to ground) TupF, OFF channel, TuopF ON channel	POWER CONSUMPTION 2.5 Amps typical @ +5VDC supplied by DEC backplane connector power bus. On- board ±15V DC/DC con- verter powers linear circuits	Power Supply Rejection
Accuracy @ +25°C and 75kHz Sampling	PHYSICAL Operating Temperature Range	D/A channel, Furnished by on board DC/DC converter for A/D-D/A card. ±15VDC ex- ternally supplied for expanded D/A channels.
DRDERING GUIDE SI-11 Sine Trac Series	PRICES (Single Qu ST-LSI-64S (or6	



GOLD BOOK 76/77



ANALOG DATA PERIPHERALS FOR DEC PDP-11 MINICOMPUTERS

SINETRAC PDP SERIES

FEATURES

- 64-channel analog input (A/D) and 2 output (D/A) channels fit directly inside DEC's PDP-11 series minicomputers.
- Data acquisition rates up to 75,000 samples per second.
- ▶ Three modes of programming.
 - Program-controlled mode
 - Program-interrupt mode
 - Direct Memory Access
- Expandaple up to 256 A/D and/or 256 D/A channels. 12-bit analog resolution with choice of coding and voltage ranges.
- Optional auto-zeroing and programmable gain.
- Includes on-board control for block transfer and automatic channel sequencing and for random channels.

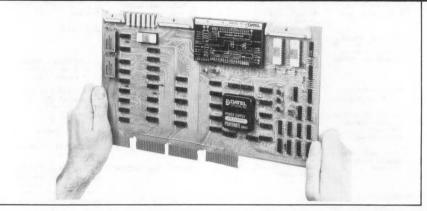
DESCRIPTION

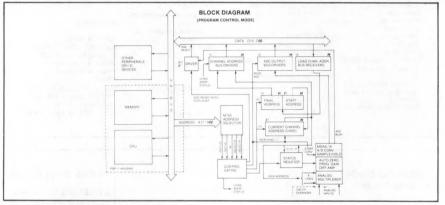
Datel offers a simple approach to providing analog signal inputs and outputs to DEC's popular PDP-11 series minicomputers. Datel's Sine Trac analog peripheral I/O module plugs directly into the card guides and connector slots inside PDP-11 housings. The Sine Trac module accepts up to 64 analog input (A/D) channels and 2 analog output (D/A) channels on the same interface card.

The Sine Trac analog I/O card communicates directly with the PDP-11 unibus, thereby, eliminating all CPU cabling. Sine Trac is handled as an addressable peripheral I/O device. Analog connections are made through the rear cable clamps on the PDP-11 housing.

Assembly or high level languages completely control all activities of the Sine Trac analog I/O card. These include random or sequential analog channel addressing with automatic reset on program-specified first and last channels. By using the appropriate I/O instructions, Sine Trac analog channels may be transferred to a teletypewriter, paper or magnetic tape, tape cassettes, CRT terminal or other peripals.

The Sine Trac board is organized around Datel's MDAS-16, a high density data acquisition module employing a hybrid successive approximation A/D converter, FET multiplexer switches, integrated





circuit Sample/Hold amplifier, and tristate TTL output buffer/registers. Address decoders, bidirectional bus transceivers, status and address registers, a $\pm 15V$ DC/DC converter and control logic complete the rest of the Sine Trac system.

The Sine Trac PDP-11 card is ideal for process control, automatic test systems, laboratory measurement systems and similar applications. Datel's System 256 will allow for expansion up to 256 A/D channels and/or 256 D/A channels.

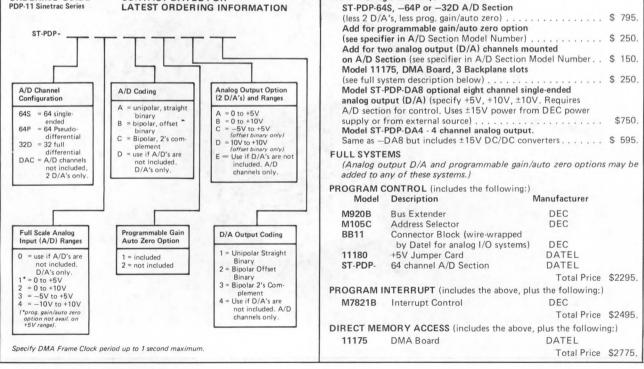
The D/A analog output channels available on Sine Trac A/D boards contain storage registers for each 12-bit analog word to maintain a stable analog output between CPU output cycles. The D/A option is ideal for plotter, chart recorder, oscilloscope or actuator drive. It is also excellent for analog feedback or testwaveforms to systems under test. Digitally synthesized analog waveforms may be program-generated with a settling time of 4 microseconds per D/A step.

The Sine Trac analog system can accept three modes of operation including program control, program interrupt mode and direct memory access (DMA). Program control requires simple instruction sequences and controls the interface at the time and sequence specified by the program. Interrupt operation is ideal for releasing the CPU for other chores while an A/D conversion is in progress. DMA operation bypasses the CPU and uses the Sine Trac's start and final channel and word counter registers to transfer Sine Trac-Controlled blocks of data addresses sequenced by the Sine Trac's memory address register and frame clock.

Very fast auto zeroing circuits and programmable gains are optional on Sine Trac systems. The auto zeroing corrects for voltage offsets and programmable gains of 1, 2, 5, and 10 provide input ranges down to \pm 500mV full scale. The gain is program controlled and is ideal for applications requiring extended dynamic range. Systems without the auto zero/programmable gain option have A/D data throughput of 75,000 samples per second. Throughput for systems with the option is 40,000 samples per second.

SPECIFICATIONS (Typical @ +25°C, dynamic conditions unless otherwise specified.)

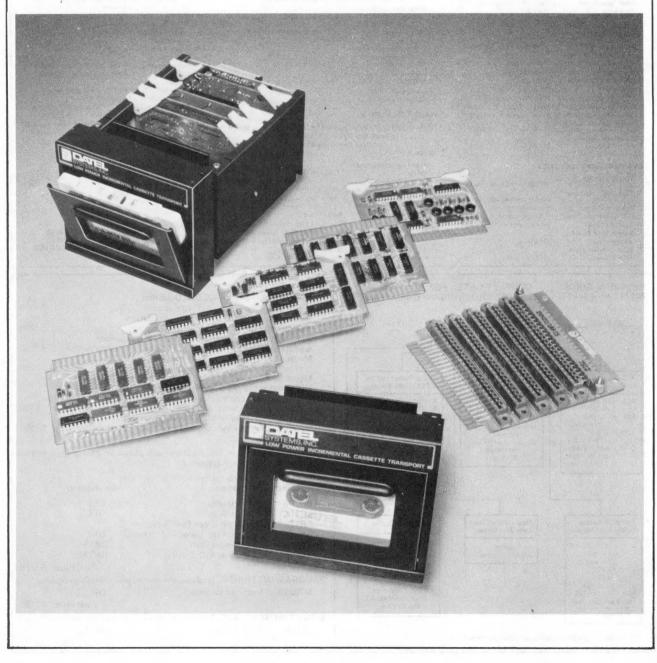
DATA ACQUISITION SECTION (A/D Analog Inputs)	DIGITAL OUTPUTS	DATA DISTRIBUTION SECTION (D/A Analog Outputs)
ANALOG INPUTS	Output Coding	ANALOG OUTPUTS
Number of Channels. 64 single-ended 64 speudo-differential 32 full differential Channel Expansion up to 256 single-ended channels (using Datel's System 256 in externel housing) 128 full differential channels	patible to DEC's bidirectional bus	
Input Voltage Ranges0 to +5 Volts 0 to +10 Volts -5 to +5 Volts -10 to +10 Volts	Sign extension is provided on Bits 12-15. Channel Addressing RANDOM - Under program contro SEQUENTIAL - Under program co trol or under interface DMA contr	-5V to +5 Volts* -10V to +10 Volts* (*offset binary or 2's complement)
Programmable Gains x1, x2, x5, x10 (not available 0 and Autozero (optional) +5V range) Common Mode Range ±10V Volts guaranteed maximu	o using preloaded start channel, fina channel, number of channels and next memory address registers.	I Output Impedance 50 milliohms Output Current
Input Overvoltage, ±15V, max. sustained (no damage)	DMA Frame Clock Selectable period up to 1 second p channel (specify with order).	PERFORMANCE
Input Impedance 100 megohms differential or to ground	INTERFACE ADDRESSING	Nonlinearity ±1/2 LSB, max.
Input Bias Current 3nA typical, 10nA max. Input Capacitance 10pF, OFF channel, 100pF, ON (to ground) channel	PDP-11 Sinetracs are supplied with addressing shown below. Contact Datel if other addressing is required. M105 (Address Selector)	Differential Nonlinearity ±1/2 LSB, max. Gain Error Adj. to zero using pot for each channel
(to ground)	Address	Zero Error Adj. to zero using pot for each channel
ERFORMANCE	DMA Address	Gain Temperature Drift ±30 ppm of output/°C Zero Temperature
Accuracy @ +25°C Within ± 025% of full scale and 75kHz Sampling Resolution 12 Binary Bits	Vector Address-Interrupt Interface (Program Interrupt)	Drift (unipolar output) ±5ppm of full scale range/°C Offset Temperature
Nonlinearity	M7821 (VECTOR BIT 2L) 770 (no jumper cuts) Vector Address (DMA Mode) M7821 (VECTOR BIT 2H) 774 (no jumper cuts)	Drift (bipolar output) ± 15ppm of full scale range/°C Settling Time 4 microseconds to +1/2 LSB Power Supply
Gain Error Adjustable to zero Offset Error Adjustable to zero Gain Temperature Drift Within ± 30 ppm of full scale/°C	Bus Request Level 7 Bus Grant Level 7	Rejection
Offset Temperature Drift Within ± 30 ppm of full scale/°C Common Mode Rejection	POWER CONSUMPTION	D/A channel. Furnished by on-
(with 1 kilohm unbalance) 70 dB min., DC to 1 kHz Power Supply Rejection	2.5 Amps typical @ +5VDC supplied by DEC backplane connect power bus. On-board ±15V DC/DC	D/A card. ±15VDC externally
(to +5V bus) 100 dB	converter powers linear circuits. PHYSICAL	supplied for expanded D/A channels.
DYNAMIC CHARACTERISTICS	Operating Temperature Range	
Throughput Rate (without prog. gain/auto zero) 75,000 samples/sec., max.	Storage Temperature Range	
Throughput Rate (with prog. gain/auto zero) 40,000 samples/sec., max.	Card Size	
Acquisition Time 6 microseconds A/D Conversion Time 7.3 microseconds	6 BB11 card slots.	013
Aperture Time	Card Connection Four BB11 card slots (C thru F). Wire wrapped BB11, power and	
Feedthrough	I/O connectors supplied on full systems (see ordering).	DATEL
OFF Channels	Humidity	





1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

Digital Cassette Recorders & Systems





WRITE-ONLY, ULTRA LOW POWER INCREMENTAL DIGITAL CASSETTE TRANSPORTS AND RECORDER SYSTEMS

ICT-SERIES

TRANSPORT FEATURES

- Simple, reliable capstan/pinch roller stepping motor drive
- Ultra-low power (700 milliwatts while writing) using CMOS electronics
- True standby incremental performance starts writing within 20 milliseconds
- Choice of complementary NRZ or ANSI/ ECMA/ISO phase-encoding formats
- High data capacity: Up to 2.2 million bits per 300 foot cassette

RECORDER SYSTEM FEATURES

- Accepts digitized analog, serial or parallel digital inputs
- Ideal for +12VDC battery portable digital data recorders
- ANSI/ECMA/ISO systems automatically record preamble, postamble, CRC, CR, NULL, LF ASCII characters
- Optional A/D converter, 16 channel analog multiplexer, sample/hold and channel sequencer available
- Reader Systems available to interface most computer terminals, RS-232-C CRT displays, modems and teleprinters (TTY)

INTRODUCTION

Datel presents its ICT-series digital incremental cassette tape transport systems. These unique data recorders and reader systems offer a new concept to the instrument designer—miniature, removable ultra-low power, digital data storage. Using a Philips data tape cassette, low power incremental stepping motor and CMOS electronics, these recorders are ideal for portable-battery-powered data collection instruments.

Datel's cassette systems form the nucleus of your data recorder. They complement your selection of input transducers, signal conditioners and your computer system. Inputs to the optional A/D converter analog section have been standardized to 5 and 10 Volt levels commonly available from many sensors.

Reader/interface systems which are separate from the data recorder provide several output forms (full parallel, TTY/ RS-232-C ASCII, 1/2" mag. tape) to adapt to different computers and printout devices.

Datel also offers a new concept to the engineer or scientist interested in data recording with tape systems. The ICT-series offers a simplified approach with circuit card modules which are specified in terms familiar to circuit designers who know digital logic. Data entry, retrieval and power-up, power-down considerations are simplified to the point of providing and accepting logic levels at the required times. For a complete system design, details of the transport's flux levels and motor drive are transparent to the designer, requiring only a knowledge of ultimate word size, bit rate and data capacity. Yet Datel's transport and individual card modules are fully specified so that customized systems may be created at any level from transports alone up to fully packaged systems.



With very fast power turn on, the tape moves only when actually recording data or creating a gap. At all other times when not recording data, the transport and power-multiplexed electronics remain turned off to save tape and batteries.

The fast turn-on, turn-off feature means that tape is up to writing speed within 10 milliseconds with no coasting when turned off. Data systems such as seismic recorders may be designed to record only when data is actually present, providing a very large data capacity per cassette. Hand-held stock inventory recorders move the tape only when keyboard data has been entered.

MODELS AVAILABLE

Datel offers these cassette recorders and companion readers as complete systems or as general purpose component modules for the widest range of applications. The basic ICT-series transports are available with a family of printed circuit cards, parallel-to-serial/formatter cards, A/D converter, multiplexer and sample/holds for analog inputs. Transport and PC cards may be purchased separately at any time to build complete customized low power digital recording systems.

APPLICATIONS

Complete Cassette Data Logging Systems from Datel are available to record up to 16 or 64 analog channels, both as user-mounted modular systems and as stand-alone, weatherproof automatic data acquisition/logging systems (refer to Datel Models LPS-16 and DL-2). Applications include oceanographic buoys and submersible probes, portable air and water quality environmental monitors, traffic and noise loggers, natural resources exploration, vehicular testing, seismic and geophysical measurements, RF field strength and transmission loggers, unmanned weather stations and biomedical loggers.

RECORDING FORMATS

Datel uses two cassette digital recording methods. A dual-track complementary NRZ (CNRZ) method is used for high noise immunity and self-clocking on playback. This high capacity method uses both tracks of the tape simultaneously and records in only one direction. Using separate 1's and 0's tracks and very small gaps, one cassette can hold up to 2.2 million bits, or 120,000 A/D samples.

Datel also uses a single-track phase-encoding serial method fully compatible with widely accepted ANSI/ECMA/ISO standards. Both sides of the cassette may be written. The ANSI/ECMA/ISO format is 8-bit oriented with optional parity as the 8th bit or fixed at one or zero. This format is ideal for interfacing to ASCII encoded data or to the IEEE-488 instrument interface bus. The proper preamble, cyclic redundancy check characters and postamble are recorded for playback synchronization, start of data recognition and error detection. Datel's ANSI/ECMA/ISO transports are unique from those of other manufacturers in that full incremental operation is a standard feature (rapid start and stop with each byte). Yet the transport retains its ultra low-power stepping motor design. Tapes prepared on Datel's cassette transport may be used on any reader which is fully ANSI/ECMA/ISO compatible. This includes a variety of CRT terminals and computers accepting ASCII coding using a serial interface with EIA RS-232-C electrical specifications.

CASSETTE TRANSPORT FEATURES

Datel's incremental cassette transport features a design simplicity not found in other mechanisms. An elegantly simple tape speed control is provided using a four-winding stepping motor with 48 rotor steps per revolution and geared down capstan drive. The stepping motor relies on electronically rotating the stator field around permanent magnet multi-pole rotors instead of mechanical brushes and a commutator. A CMOS clock sequences the stepping motor drivers. This avoids the usual methold found in continuous recorders employing slotted strobe discs, tachometers or prerecorded clock tracks. All of these methods require some servo slewing time to reach accurate speed, thereby adding a delay in true incremental applications. The stepping motor drive features high electrical to mechanical efficiency since there is no brush friction drag. The complete transport and electronics are optimized for ultra-low power (one watt while stepping) making it ideal for battery-operated portable systems.

Further mechanical simplicity and ultra-low power is enhanced by the single-motor write-only transport. Instead of a second motor to maintain take-up tape tension, a spring-belt and friction clutch takeoff from the capstan drive maintain constant take-up hub torque and tape tension.

The ICT-series write-only transports are optimized for ultra-low battery power with bit writing rates within bytes or words of 50 or 100 bits/second. These bit rates are adequate for a wide variety of portable and long term instrumentation applications. These include hand-held keyboard inventory recorders and field data logging of slowly varying analog parameters such as temperature, pressure, RF field strength, etc. However, on playback, ICT-recorder cassette readers, typically several thousand bits per second. Playback bit rates within blocks or files at a tape speed of 2.5 inches per second are 2 Kilo bits per second or 250 bytes per second.

Special reader transports with appropriate heads and drives available from several manufacturers allow data search speeds up to 30 inches per second or more.



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

RECORDING TECHNIQUES TO CONSERVE POWER AND TAPE

Datel's ICT recorder systems use several methods to save available battery energy and to record a maximum amount of data on tape.

The stepping motor drive allows immediate access (with 10 milliseconds) from data input to writing on tape unless the system is within a gap. This fast turn-on saves time, tape, and battery energy normally required to establish higher tape speeds typical of continuous or constant-speed incremental transports.

The second factor which saves time, tape and batteries is the incremental operating mode. Since tape can be stopped or started at any time except within a byte, word or gap, the transport can be shut off any time data is not ready to record. The

tape is moved only when actually recording data or generating gaps.

The fast turn-off and turn-on are controlled by logic levels generated on the ICT-series circuit cards. Extensive use of digital integrated circuits means that no warm-up time is required. The logic family chosen was CMOS (Complementary Metal Oxide Semiconductor) because of the exceptionally low power required, high reliability and high noise immunity.

For these reasons, Datel's ICT incremental cassette systems comprise one of the more energy-efficient data storage systems that are commercially available.

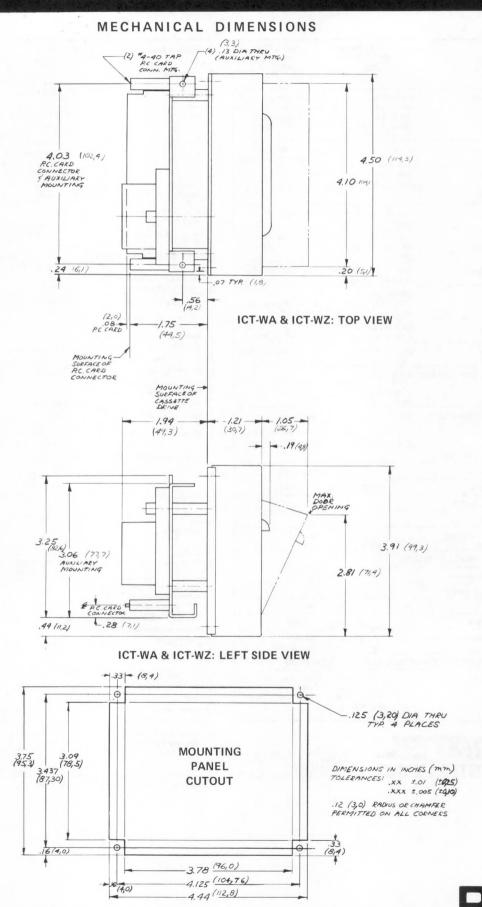
DIGITAL CASSETTE TRANSPORT SPECIFICATIONS (Typical over 0° to +70°C unless noted)

	Model ICT-Wa Biphase- Level ANSI/ECMA/ISO Format	Model ICT-WZ Complementary Format
GENERAL		
Recording Medium	Philips magnetic tape cass operation by using a bit-e The transport is designed plying with ANSIX3. 48, DIS3407 specs.	to accept cassettes com-
Number of Tracks	One half-width track	Two half-width tracks, recorded simultaneously
Recording Direction	Two directions by flipping cassette over	One direction only
TAPE MOTION		
Motor	4-winding 24 pole, perma motor	nent magnet stepping
Equivalent Tape Speed Range	Zero to 0.063 inches per second (1,59 mm/ sec)	Zero to 0.163 inches per second (4, 13 mm/ sec)
Nominal Tape Speed	0.063 in./sec. (1,59 mm/ sec) at 100 steps/sec.	0.163 in./sec. (4, 13mm sec) at 100 steps/sec.
Bit Density	800 bits per inch (1600 FRPI) 32 bits per mm	615 bit per inch (615 FRPI) 24 bits per mm
Bit Cell Spacing	0.00125 inches per bit 0,0318 mm per bit	0.00163 inches per bit 0,0414 mm per bit
Bit Writing Rate	Zero to 50 bits/second, asynchronous	Zero to 100 bits/second asynchronous
STEPPING MOTOR CHARAG	CTERISTICS	
Tape Drive Capstan Diameter	0.118 inches 3,0 mm	0.1246 inches 3,16 mm
Capstan Rotation Step Angle	0.6°	1.5°
Stepping Rate	Zero to 100 steps per second, asynchronous	Zero to 100 steps per second, asynchronous
Number of Stator Windings	4	1
Winding Resistance	450 ohms per winding, \pm 20%	
Winding Inductance	335 millihenries pe	er winding, ± 20%
Motor Steps per Bit Cell	2	1
Winding Voltage	± 10V min. to	± 24V max.
Hub and Capstan Torques and Tape Tension	Suitable for ca ANSI/ECMA/IS	
TAPE HEAD CHARACTERIS	STICS	
Tape Saturation Current	5mA	typ.
Suggested Write Current	7.5mA	typ.
D.C. Resistance	50 ohms	s ± 20%
Effective Track Width	0.057 inches	s (1, 45 mm)
Nominal Space Between Tracks	0.035 inches (0,88 mm) (Tracks are symmetrically spaced)	
DATA CHARACTERISTICS	USING DATEL'S ELEC	TRONICS
Recording Format	Single track full serial, externally clocked using 8-bit bytes phase-encod- ed per ANSI/ECMA/ISO standards	2-track serial com- plementary NRZ 1's on Track 1, 0's on Track 2



Character Record Length	8-bit bytes	8, 10, 12, 14 or 16 bit characters or words
File or Block Length	Blocks consisting of 2 min. up to 256 max. usable data bytes per block	Files consisting of 1, 2, 4, 8, 16, 32 or 64 characters or words per block
Gaps	0.8" (20, 3mm) nominal noiseless gap written between each block. No gaps within blocks. One- half gap generated before each data block and the other half after the data block.	
Gap Stepping Rate	250 steps/sec.	100 steps/sec.
Time to General Full Gap Length	5.1 sec.	0.12 sec.
Power Consumption (Transport & Tapehead only)	700 mW typ. @ (+12VDC @	
DATA CAPACITY (Assuming characters	64 8-bit characters per block and 282 feet (86 m) usable re	or file, plus non-data ecording area)
Block or File Length including Controls and Gaps	1.48 inches (37, 6 mm)	1.06 inches (26, 9 mm)
Block or Files per Cassette	2260 blocks (recording one side)	3200 files
Bit Cells per Block or File (including Gaps and Control Characters)	1200	652
Time per Block or File (not including gaps)	11.2 seconds	6.4 seconds
Time to Fill a Cassette (continuous running at max. step rate)	10.2 hours per side	5.8 hours
Bit Writing Rate	50 bits/sec.	100 bits/sec.
Playback Speed, typical	250 bytes/sec. (2.5 ips) (TI 733 ASR) or higher	1700 bits/sec. (LPR-16 Reader, 2.75 ip
Time to Generate Full Gap* Length	5.1 sec. @ 250 steps/sec.	0.12 sec. @ 100 steps/sec.
Gear backlash, tape creep and sla operations.	ck is taken up by load forwa	rd and gapping
*2.55 second half-gap generated befo PHYSICAL	re and after each data block.	
Weight	1.25 pounds (0,	567 kilogram)
Dimensions	3.91" High x 4.5" Wide x 4.2" Deep (99,3 x 114,3 x 106,7 mm)	
Maximum Extension in Front of Mounting Panel * (door closed) (door open)	1.40" (35,6 mm) 2.26" (57,4 mm)	
Maximum Depth Behind Mounting Panel	1.94" (49,3 mm) from panel front surface	
Mounting Method	Front insertion into a panel cutout, secured by (4) 4-40 bolts inserted from the rear into tapped Helicoil thread inserts, 0.187" (4,76 mm) deep	
Mounting Position	Horizontal or vertical. Recommended with cassette vertical, tapehead at top for easy cassette insertion.	
Temperature Range (Operating and Storage)	-20°C to +70°C standard available on special order,	
Power Consumption (Auxiliary Cards and EOT/BOT Detector)	Phase Board, ANSI Formatter, Block Formatter, and Expander consume approximately 120 micro- watts each (+12VDC @ 10 microamps). The EOT/BOT Lamp and detector consume 900 mW (+12VDC @ 75 mA).	

CASSETTE TRANSPORT OUTLINE DIMENSION - INCHES (MM)

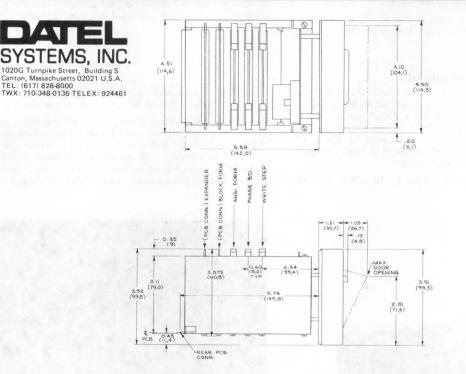


See inside back cover for DATEL sales offices

Electronic Design's

_

RECORDER SYSTEMS CARD CAGE OUTLINE DIMENSIONS - INCHES (MM)



CASSETTE RECORDER SYSTEM MODELS AVAILABLE

Both ICT series write-only recorders are available in many configurations , from transport-only to stand-alone recorders.

The basic ICT transport is a panel mounting assembly which fits through a front panel cutout. The transport includes the stepping motor, tape head, both hub assemblies and optional EOT/BOT photodetector.

All electronics for the ICT systems are mounted in an optional

WHICH DATA FORMAT? CNRZ or ANSI/ECMA/ISO PHASE-ENCODING?

Both CNRZ and ANSI/ECMA/ISO phase-encoding formats have been optimized for ultra-low power incremental recording, yet each has its particular advantages.

CRNZ formatting should be used for noise-immunity and shortest gaps for data logging applications. ANSI/ECMA/ISO phaseencoded formatting should be selected where interchangeability with other makes of writers and readers and most computer terminals is a consideration.

Phase encoded cassettes from Datel's ICT-WA series systems are available with first level (octal or hexadecimal) ASCII printout formatting recorded directly on the write-only system. ICT-WA cassettes may be played back immediately on any ANSI/ECMA/ ISO compatible CRT display terminal or computer teleprinter.

Both formats are readily available with code conversion to ASCII 8-bit formats for later storage or transmission of the data. ANSI/ ECMA/ISO recording may be used for all slowly-varying analog data logging applications except those which cannot wait the 2.55 seconds to generate the half-gap preceding each data block.

Code conversion to ASCII is performed in the write-only system for ANSI/ECMA/ISO formats and in the reader for Datel's CNRZ format. This contributes to tape storage efficiency on CNRZ systems, but also to preformatted interchangeable cassettes on ANSI/ECMA/ISO systems, for playback on many types of five-slot PC card cage which attaches to the rear of the transport. The entire assembly consisting of the cage, PC cards and transport are firmly supported when the transport is mounted to the user's front panel. The five optional cards slide into card guides in the card cage and mate with PC edgeboard connectors mounted on a motherboard on the bottom of the card cage. All signals and power voltages are transferred along a bus on this motherboard which terminates at a rear PC connector for all I/O signals.

Readers. ICT-WZ CNRZ cassettes must use a CNRZ-compatible Reader such as Datel's model LPR-16 (refer to the LPR-16 Reader in the Data Logging section).

Both formats can accept varied block or file length and both require similar cost in electronics to perform the same functions. Datel's ICT-WZ CNRZ systems have room in a single 5-slot card cage for an optional 12-bit analog/digital converter and 16-channel multiplexer (see Model LPS-16). ICT-WA systems require additional area to accommodate an A/D section.

The minimum 5.1 second, 0.8 inch (20,3 mm) gaps required of ANSI/ECMA/ISO formatting become a serious data capacity consideration if blocks cannot contain substantial numbers of bytes. Short blocks waste excessive tape in writing gaps and ANSI/ECMA/ISO data systems frequently use external semiconductor memory storage to produce efficiently-long blocks. ANSI/ECMA/ISO formatting relies on regulated speed control while writing and reading single-track phase-encoded data with two motor steps per bit cell. Data is recorded in blocks. Noiseless gaps of specified minimum length are required before and after each block and these are automatically generated by Datel's circuit card modules.

GOLD BOOK 76/77

FILE OB BLOCK LENGTH

In ANSI/ECMA/ISO formatting, the number of bytes per block is selected using an externally supplied 8-bit block length code which must be stored before writing the block.

The CNRZ format allows for variable file length and jumperselected bits per word. The file length (words per file) may be

MIXED ANALOG AND DIGITAL INPUTS

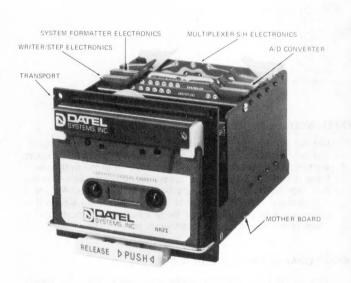
By the simple addition of Datel's A/D converter and Sample/Hold Amplifier PC cards, the ICT-series can record either analog inputs (up to 12 binary bits) or parallel or serial digital inputs. On full data logging systems (model LPS-16), a one line mode control accepts A/D converter parallel binary outputs or full serial external digital inputs synchronously clocked in from outboard serial sources or parallel-to-serial shift registers.

ICT-WZ systems accept digital inputs up to 16 bits in parallel.

internally or externally controlled. An internal word counter may be jumper-programmed to end the file at 1, 2, 4, 8, 16, 32 or 64 words. An external word counter can also end the file at any word count. Bit length per word is jumper selected at 8, 12, 14, or 16 bits.

ICT-WA systems have an optional Expander Board accommodating 1, 2, 3, 4, 5 bytes (up to 40 bits total) of parallel digital inputs.

Both systems can accept Datel's optional 16 channel, high speed. single ended high impedance FET analog multiplexer and Sample/ Hold amplifier. ICT-WA systems require a second short (4-card) card cage to accommodate the analog section plus all the ANSI/ ECMA/ISO tape electronics. System power consumption remains below 1.5 Watts while recording and in the microwatts in standby.





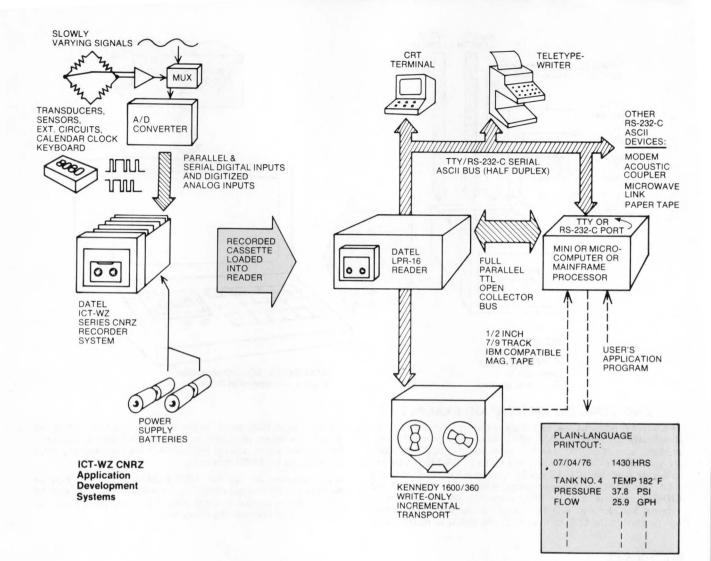
16-CHANNEL **ULTRA LOW POWER** ANALOG DATA LOGGER

MODEL LPS-16

BATTERY POWERED WEATHERPROOF AUTOMATIC ANALOG DATA LOGGER FOR **64 CHANNELS. INCLUDES** ONE YEAR CALENDAR CLOCK MODEL DL-2



Electronic Design's



COMPLEMENTARY NRZ APPLICATION SYSTEM EXAMPLE

The block diagram shown indicates the types of input sources used with the ICT Transport System. Also shown are computer system output devices used when reading cassettes. This particular example shows an analog signal from an input bridge used to measure strain, temperature, etc. The ICT system cannot directly record this analog signal so it must first be digitized using an A/D converter. Datel supplies modular encapsulated 12-bit CMOS A/D converters mounted on cards which slide directly into the ICT series card cage. The digitized analog signals may then be recorded on the cassette.

The block diagram also shows digital signal sources. These can include parallel and serial TTL or CMOS inputs. The TTL signals should be buffered through open collector level shifters to be compatible with the ICT's +12V CMOS logic levels. Serial digital inputs may be shifted into the ICT systems by using the shift clock output.

Not shown in this application diagram are 8-bit bytes in ASCII format externally encoded from portable hand-held keyboards and other sources.

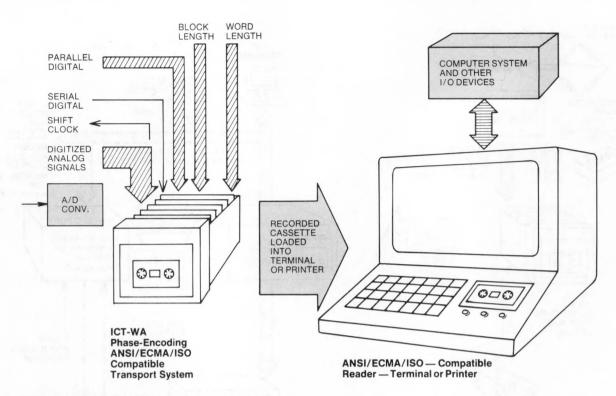
The ICT Transport Systems using CNRZ format must use a CNRZ-compatible Reader such as Datel's model LPR-16 shown here. Refer to the Data Logging section for more information on the LPR-16.

The LPR-16 Reader is available with 3 types of outputs to feed computers and various output and display devices. These outputs are full parallel, full serial or half-inch magnetic tape. Between them, practically every current computer-compatible device can easily by interfaced to.

For example, if you have access to a powerful high speed mainframe computer with BASIC or FORTRAN languages but without convenient electrical input, transcribing cassettes off line onto half-inch magnetic tape is the logical route to follow.

Half-inch tapes are then loaded into mainframe memory and a complete printout is available with user-controlled output formatting, variable labeling and arithmetic functions. The high density tapes can be retained by the user if they ever need to be run again or analyzed differently.

A computer is shown in this block diagram and it will be required in practically all situations needing arithmetic on the data or output formatting. However, the LPR-16 Reader can be operated off-line directly to a local teletypewriter or CRT terminal to get a quick look at the data in hexadecimal output. Simple TTY printout formatting presents A/D samples and digital words as hexadecimal characters with optional channel identification for analog channels. Spacing, carriage returns and line feeds help identify individual words and data files.



ANSI/ECMA/ISO APPLICATION EXAMPLE

The ICT-WA ANSI/ECMA/ISO phase-encoding format is designed specifically for direct compatibility with many terminals, teleprinters, and other I/O devices which accept ASCII characters transferred over TTY 20mA current loops or RS-232-C interface cables. In contrast, ICT-WZ CNRZ systems are not limited to the 8-bit formatting of phase-encoding systems. In fact, ICT-WZ CNRZ transports can be preformatted using the customer's external ASCII formatting electronics. Or the ASCII formatting does

ELECTRONICS

Both cassette systems accept serial and parallel digital inputs. These are presented to input terminals at the proper times and are internally stored. DATA ACCEPTED flag signals appear, allowing the user's external electronics to clear and load the input bus with the next group of data. This can occur in parallel or bit by bit in full serial by using the shift clock output.

Since the transport must run at a given tape speed, data bits must be ready fast enough for input to the write electronics. However, the transport is truly character or word incremental so that the tape can stop within a block or file and wait after writing one word for new data that isn't ready yet.

ICT-WZ COMPLEMENTARY NRZ BOARDS

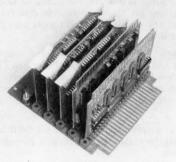
In addition to the Write Step Board, ICT-WZ Recorder systems have the Formatter Board available. An optional A/D Converter Board, and Sample/Hold, Multiplexer, Channel Sequencer are also available for analog inputs. Refer to complete analog systems specifications under Datel's LPS-16 series.

The ICT-WZ Formatter Board accepts parallel CMOS digital words from 8 to 16 bits long, stores them and shifts them over serially to the Write Step Board. The Formatter also supplies a 2-step bitless gap beginning each word to the Write Step Board and a longer 12 step gap at the end of a file or from external command. Word length from 8 to 16 bits is jumper programmed as is a word counter which automatically generates the 12-step file gap after the jumper-selected number of words per file. File length can also be externally controlled.

not have to be done at all. In the case of a long-term analog and digital data logger, most efficient tape use and highest data transfer rate will occur using a full parallel reader without the extra bits required for ASCII characters.

Tapes prepared on ICT-WA ANSI/ECMA/ISO systems may be displayed or printed out directly on an ANSI-compatible terminal I/O device. A computer is not needed but will be required for arithmetic and reformatting the output.

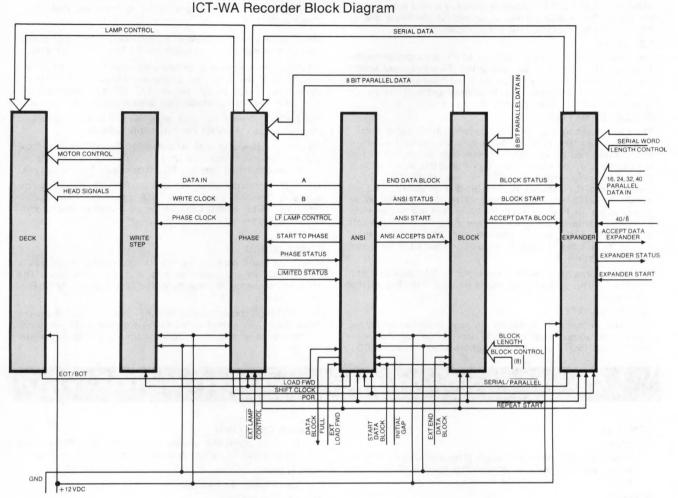
Several circuit boards with similar functions are used on ICT-WA and -WZ systems. The Write Step board drives the 4-phase windings of the stepping motor. The 100 Hz motor clock pulses are also used to sequence input bits which drive the tape head through the Write Step board. Flip flops for the tape head keep track of the present drive state of the head and apply the proper flux change. CNRZ systems route zero and one bits to alternate tracks and phase-encoding systems orient the single-track flux change direction for zeroes and ones. The basic motor clock serves as a master clock for all the remaining logic in either ICT system.



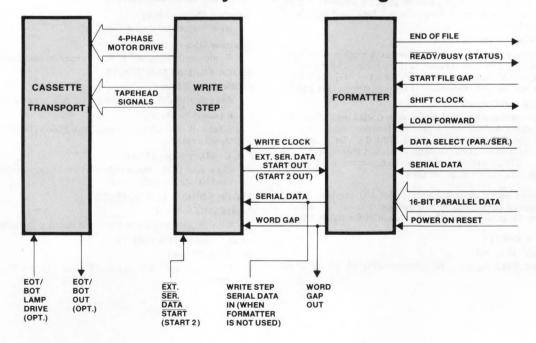
ICT-WA CARDS LESS TRANSPORT (SEE BLOCK DIAGRAM)

Electronic Design's

ANSI/ECMA/ISO



Complementary NRZ ICT-WZ Recorder System Block Diagram



GOLD BOOK 76/77

ICT-WA PHASE-ENCODING PC BOARDS

ANSI/ECMA/ISO ICT-WA Recorders employ several more boards besides the Write Step Board, These include the Phase Board, ANSI Formatter, Block Formatter and Expander.

EXPANDER

Full Parallel inputs of 16, 24, 32, or 40 bits are accepted by the Expander. Two other input lines select the input word length code. The Expander stores both the word length code and full parallel inputs. It flags when data is accepted and shifts inputs out serially to the Phase Board prior to writing on tape.

BLOCK FORMATTER

The Block Formatter Counts the number of bytes being written in a block and terminates the block at a preselected number of bytes determined by an eight-bit input code which is stored at the beginning of the block. The Block Formatter ends the block by automatically generating ASCII carriage return (CR), NULL and line feed (LF) characters. The Block Formatter then commands the ANSI Formatter to sequence the CRC and Postamble generated on the Phase Board to the Write Step Board. The ANSI Formatter completes the block by generating the interblock half gap. The CR, NULL and LF characters can be omitted by short cycling the number of bytes in the block compared to the stored block length code.

The block Formatter provides direct input for 8-bit parallel digital words only. This parallel input would be used if the Expander is not required.

ANSI FORMATTER

The ANSI formatter generates certain gaps, controls whether the Phase Board accepts serial or parallel data and controls the Beginning of Tape (BOT) lamp logic and photodetector until the BOT tape hole is passed. The ANSI Board directs the sequence of bytes generated on the Phase Board including Preamble, Postamble, Data and CRC.

The ANSI Formatter generates an overriding bitless gap at any time on external command (using the EXT. LOAD FWD. input).

An initial gap is externally commanded when the cassette is first mounted and rewound. This bitless gap passes the clear leader/ oxide splice and stops tape motion 1.5'' (38 mm) past the BOT hole, after which the photodetector lamp is turned off.

The 0.4 $^{\prime\prime}$ (11,6 mm) half-gaps beginning and ending each block are generated by the ANSI Formatter automatically.

All gaps are generated with saturated (DC Erase) tape head flux and an accelerated step rate (250 steps/second) to limit the required gap-generating time to 2.55 seconds per half interblock gap.

The ANSI Formatter also commands the Phase Board to generate a tape or file mark block on external command consisting of a preamble, 16-bit NULL CRC (all zeros) a postamble and both beginning and ending interblock gaps.

PHASE BOARD

The Phase Board contains the 100 Hz motor clock, computes the CRC characters and generates preambles and postambles. The recording sequence of these bytes is directed by the ANSI Formatted Board.

The EOT/BOT photodetector sensing circuit is located on the Phase Board. Its output is fed to logic on the ANSI Formatter which decides whether to shutoff the lamp and/or continue tape motion.

ANSI/ECMA/150 ICT-WA RECORDER SYSTEM SPECIFICATIONS

GENERAL

Function

Digital ultra-low power write-only phase-encoding cassette recorder accepting serial or parallel data incrementally in 8-bit bytes.

Data Rate

Writing rate is 50 bits per second within blocks. Parallel inputs may be stored. Input data bus must be valid 100 microseconds minimum at time of start command.

EOT/BOT Photodetector

Optional lamp and photodetector to sense passage of clear leader/oxide splice, BOT (Beginning of Tape) and EOT (End of Tape) holes.

Lamp requires 12V @ 75mA.

For optional long term, low power data logging, automatic circuits provide a load forward past the splice. This continues 1.5 inches (38 mm) past the BOT, then the EOT/BOT lamp is shut off for the remainder of the cassette to save power.

Digital Inputs and Outputs

All input/outputs are compatible with CMOS logic characteristics, using 4000A series devices. Nominal power supply voltage for ICT series electronics is $+12 \pm 0.5$ VDC, regulated. Logic input levels must fall within zero and the power supply voltage. CMOS logic is edge sensitive, requiring 15 microseconds maximum rise or fall times.

The following listing describes only major I/O connections between individual circuit boards and outside circuits. Full descriptions of line functions and timing are shown in the ICT brochure.

EXPANDER INPUTS

Parallel Data (40 Lines)

Accepts digital inputs to be recorded with 16, 24, 32, or 40 bits.

Expander Start (1 line)

Data and commands are stored on rising edge. Phase board initiates shift of parallel data and begins recording on tape.

40/8 (1 line)

Low disables the Expander

Word Length (2 lines)

Selects parallel input length of 16, 24, 32, or 40 bits.

EXPANDER OUTPUTS

Serial Data (1 line)

Parallel data shifted out to phase board.

Expander Status (1 line)

HI when parallel data is being shifted.

Expander Data Accepted

Ready for data when high. Bus may be changed when low.

BLOCK FORMATTER INPUTS

Parallel Data (8 lines)

8-bit parallel data input when Expander is not used.

Block Length (8 lines)

Selects Block Length from 2 to 256 Bytes. This code is stored at start.

Ext. End Data Block (1 line)

Generates CRC, Postamble and interblock half-gap at any time before the block is full.

BLOCK FORMATTER OUTPUTS

Parallel Data (8 lines)

8-bit parallel data bussed to Phase Board as bytes are counted.

ANSI FORMATTER INPUTS

Initial Gap (1 line)

Moves the tape 1.5 inches (38 mm) past the BOT hole and stops.

Start Data Block (1 line)

Generates interblock half-gap, preamble and stops tape, waiting for additional data.

Ext. Load Forward (1 line)

Overriding command to generate a bitless gap at 250 steps/ second at any time.

ANSI FORMATTER OUTPUT

Data Block Full (1 line)

HI flag indicates maximum allowable bytes recorded in a block.

PHASE BOARD INPUTS

Parallel Data (8 lines)

8-bit data bussed from Block formatter.

Serial Data (1 line)

Shifted from Expander

External Lamp Control (1 line)

LO turns EOT/BOT lamp on, HI turns it off. Used for incremental applications.

POWER REQUIREMENTS

Transport and Tapehead

700mW typical @ 100 steps/second (+12VDC @ 60mA)

EOT/BOT Lamp (optional)

900mW typical (+12VDC @ 75mA)

Auxiliary Boards

120 microwatts per board (+12VDC @ 10 microamps)

PHYSICAL

Outline Dimensions (Transport plus Card Cage)

3.91-in. high, 4.50-in. wide, 7.20-in. deep. (99,3 x 114,3 x 182,9 mm). 126.7 cu. in. (2076 cu. cm)

Weight

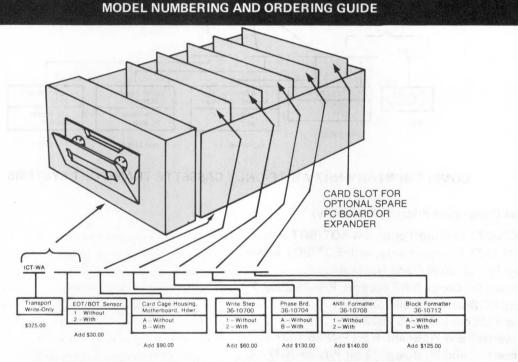
2 pounds (0,9 kg)

Connectors

3 sets of dual-readout 44-pin PC edgeboard fingers (male) are used for external connections. The fingers are spaced on 0.156-inch centers on the BLOCK FORMATTER, EX-PANDER and rear of the MOTHERBOARD. Each PC jack mates to Cinch #251-22-30-160 connector or Viking 2VH-22/1AN or equivalent (Datel #2075060)

Temperature Range (Operating and Storage)

-20°C to +70°C (-40°C to +70°C optional)



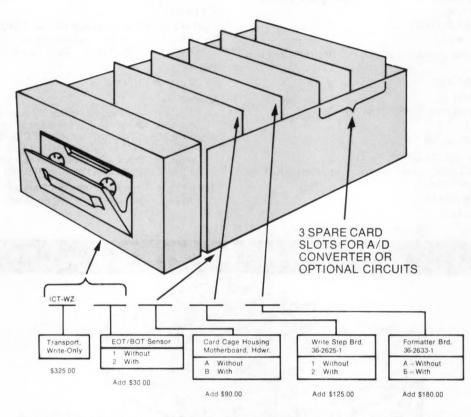


Individual Component Prices (1-9 quantity)

Model ICT-WA1 Transport only, less EOT/BOT sensor	\$355.
Card Cage P/N 36-2669-1 and Hardware	
with 5 card slots and connectors	\$ 55.
Write Step, Motor Clock and Head Drive PC Board, P/N 36-10700	\$ 60.
Phase Board, Parallel/Serial Input, Preamble, Postamble, CRC generators, P/N 36-10704	\$130.
Formatter Board, Gap Control, EOT/BOT spacing, Block counter full flag, P/N 36-10708Block Formatter Board, Generates ASCII CR, LF Chars., Block length short-cycling	
(stored 8-bit input) P/N 36-10712	\$125.
Expanded Board, Accepts 16, 24, 32 or 40 bit full parallel inputs for ANSI/ECMA recording, number of bits controlled by 2-bit modified gray code. Both controls and inputs are stored	
(strobable) P/N 36-10716	\$125.

Model Numbering and Ordering Guide

COMPLEMENTARY NRZ WRITE-ONLY CASSETTE TRANSPORT SYSTEMS



COMPLEMENTARY NRZ WRITE-ONLY CASSETTE TRANSPORT SYSTEMS

Individual Component Prices (1-9 quantity)

Model ICT-WZ1 Transport only, less EOT/BOT sensor Sensor	\$325.
Model ICT-WZ2 Transport only, with EOT/BOT sensor	\$355.
Card Cage P/N 36-2669-1 and Hardware	\$ 35.
Motherboard for Comp. NRZ systems, P/N 36-2699-1	
Write Step PC Board, P/N 36-2625-1	
Formatter PC Board, P/N 36-2633-1	\$180.
A/D Converter* and PC Board, 8-bit P/N 36-1637-1	\$385.
A/D Converter* and PC Board, 12-bit P/N 36-1637-1-2	\$405.
Sample/Hold and 16-channel single-ended analog multiplexer, P/N 36-1711 splus channel sequencer.	\$375.

*Specify input voltage range and output coding when ordering A/D converters.

For full analog 16-channel data logging systems (includes A/D converter, mux, sample/hold and channel sequencer), refer to the model LPS-16 numbering and order guide.



1020G Turnpike Street, Building S Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

Other Datel Brochures

MINI-COMPUTER COMPATIBLE LOW POWER CASSETTE DATA DATA ACQUISTION SYSTEM LOGGING SYSTEM It puts the entire environment within the reach of the computer SYSTEM 256 3 DATEL LOG And And And And **V/F CONVERTERS** DATA CONVERSION PRODUCTS ESIGNER'S GUIDE TO V/F CONVERTERS PREFERRED DATA CONVERSION MODULES A 10 COR DATEL HIGH PERFORMANCE AMPLIFIERS **DIGITAL PANEL METERS** DIGITAL PANEL METER SHORT FORM GUIDE HIGH PERFORMANCE AMPLIFIERS DALE DATE DC POWER SUPPLIES AND THREE RING BINDER CONTAINING **DC-DC CONVERTERS** ALL PRODUCT LITERATURE (1) ENGINEERING POWER SUPPLY HANDBOOK DATE (1) Available upon written request

Extended Performance Modules

MODEL/SERIES	EX	EXX-HS
D/A CO	NVERTERS	
DAC-9	Х	X
DAC-19	Х	X
DAC-29	Х	X
DAC-49	Х	х
DAC-69	Х	
DAC-169	Х	
DAC-CM	Х	x
DAC-DG	х	X
DAC-FI	-X	X
DAC-GI	Х	X
DAC-HB	Х	
DAC-HI	х	X
DAC-HR	х	x
DAC-HV	х	X
DAC-I	х	X
DAC-MI	х	Х
DAC-MV	Х	Х
DAC-R	х	Х
DAC-TR	х	Х
DAC-V	Х	Х
DAC-VR	х	X

MODEL/SERIES	EX	e EXX-HS
A/D CC	ONVERTERS	
ADC-Econov.	Х	х
ADC-89A	Х	х
ADC-149-14B	х	x
ADC-CM	Х	х
ADC-D	X	х
ADC-E	Х	
ADC-EH	Х	x
ADC-EP	Х	
ADC-ER	X	х
ADC-G	X	X
ADC-H	X	х
ADC-K	X	х
ADC-L	х	х
ADC-M	Х	X
ADC-MA	X	х
ADC-N	X	х
ADC-P	X	x
ADC-SH4B	х	х
ADC-UH	Х	х
ADC-VH	х	х



CONVERTER A	CCESSORY MO	DULES
SHM-1	х	Х
SHM-2	х	Х
SHM-2E	х	х
SHM-3	х	х
SHM-4	Х	Х
SHM-5	х	Contraction of
SHM-CM	х	Х
SHM-CMI	х	Х
SHM-UH	х	х
MM-8	х	Х
MMD-8	х	Х
MM-16	х	х
MM-16-1	х	Х
AM-100	х	
AM-201	х	
AM-303	х	
VFV-10K	х	Х
VFV-100K	х	
SCL	х	х

Most of Datel Systems' products are specified over the operating temperature range of 0° C to 70° C (32° F to 158° F) with a storage temperature range of -55° C to $+85^{\circ}$ C (-67° F to $+185^{\circ}$ F). While this operating temperature range is satisfactory for most applications encountered in industrial environments or research laboratories, there are some applications which may require a wider temperature range and/or the additional reliability of hermetically sealed semiconductor components. Datel Systems can supply extended performance versions of most of its modular products in accordance with the following suffix designation:

EX = Extended operating temperature range of -25° C to $+85^{\circ}$ C.

EXX-HS = Extended operating temperature range of -55° C to $+85^{\circ}$ C with all hermetically sealed semiconductor components.

In the following table an "X" indicates availability of the above described options. In addition to the extended performance options Datel Systems also offers standard burn-in options for any of these modules. The burn-in options are indicated by the following add-on suffixes:

BU01	96 hours at +25°C
BU02	96 hours at +85°C
BU03	168 hours at +25°C
BU04	168 hours at +85°C

For pricing and delivery time of any of these options please contact the factory or Datel Systems' local sales office.

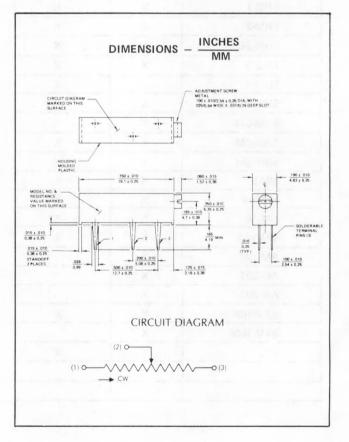
Accessory Products

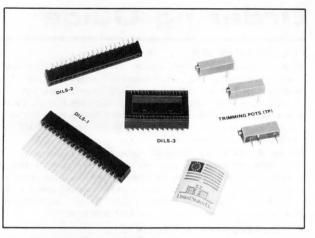
TRIMMING POTENTIOMETERS

- ▶ 15 Turn, 200 cycle rotational life
- Virtually infinite resolution
- 3/4 Watt rating, 25°C (derated to zero at +105°C)
- -55°C to +105°C operating temperature range
- ▶ 100ppm/°C CERMET element
- Clutch action stops, no damage
- Sealed against flux solvents and potting compounds

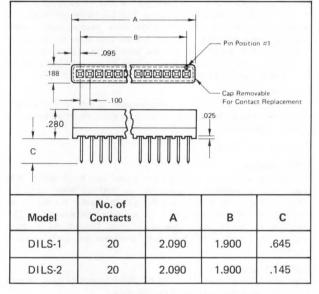
Datel Systems stocks a variety of trimming potentiometers which are used for external adjustment of zero and gain for our A/D & D/A converters, sample-holds, operational amplifiers, etc. We have chosen the Beckman Model 89P for this purpose because of its excellent characteristics. Please refer to the appropriate data sheet for the trimming potentiometer required for a given Datel Systems product.

MODEL	RESISTANCE (±10%)	PRICE
TP20	20 ohms	\$3.00
TP50	50 ohms	\$3.00
TP100	100 ohms	\$3.00
TP200	200 ohms	\$3.00
TP500	500 ohms	\$3.00
TP1K	1K ohms	\$3.00
TP2K	2K ohms	\$3.00
TP5K	5K ohms	\$3.00
TP10K	10K ohms	\$3.00
TP20K	20K ohms	\$3.00
TP50K	50K ohms	\$3.00
TP100K	100K ohms	\$3.00





DILS MECHANICAL DIMENSIONS - INCHES



DIGITAL PANEL METER CONNECTORS

These connectors are dual 18 pin PC edgeboard types with 0.1'' finger spacing on .062'' thick boards.

Connector For DPM Model	Solder Tab Connector Model	Wire Wrap Connector Model
DM-2115	2335-3	2335-4
All Other Models	2335-1	2335-2

DUAL-IN-LINE SOCKETS

DILS-1	20 Contact Strip, wire wrap	\$ 2.50
DILS-2	20 Contact Strip, dip solder	\$ 2.50
DILS-3	24 Pin Socket, dip solder	\$ 1.95

MODULE SOCKETS

MS-1	Socket for 2" x 1" module	\$25.00
MS-2	Socket for 2" x 1.5" module	\$25.00
MS-3	Socket for 2" x 2" module	\$25.00
MS-4	Socket for 2" x 3" module	\$25.00
MS-5	Socket for 2" x 4" module	\$25.00
MS-6	Socket for AM-100 amplifiers	\$ 3.50
MS-7	Socket for 2.5" x 3.5" power supply	\$ 3.50
MS-9	Socket for AM-201 amplifiers	\$ 3.50
MS-11	Socket for AM-303 amplifier	\$ 3.50
MS-12	Socket for FLT series active filters	\$ 5.00
MS-13	Socket for triple output power supply	\$ 3.50

PRINTED CIRCUIT BOARDS

PCB-1 & 2	Printed circuit board for mounting one ADC-D, ADC-K, ADC-M, ADC-E, ADC-89, ADC-L, ADC-H, ADC-N,	
	ADC-P	\$35.00
PCB-3	Printed circuit board for mounting	
	three DAC-I	\$40.00
PCB-4	Printed circuit board for mounting	
	two DAC-I and one BPM-15/50	\$35.00
PCB-5	Printed circuit board for mounting	
	two DAC-V, VR, DAC-HI,	1.00
	DAC-FI, DAC-GI	\$35.00
PCB-6	Printed circuit board for mounting	
	two DAC-HB and one BPM-15/50	\$35.00
PCB-7	Printed circuit board for mounting	
	two UPM-5/300 and two	¢00.00
DOD 0	BPM-15/50	\$20.00
PCB-9	Printed circuit board for mounting	
	two DAC-19, DAC-29, DAC-49,	¢25 00
DOD EV	DAC-69	\$35.00
PCB-EX	Printed circuit board extender.	\$25.00
PCB-CN	2VK22D/1-3 or equiv. 44 solder pin	*
	connector for PCB series	\$ 3.50

Ordering Guide

PLACING AN ORDER

When ordering a Datel Systems product, the complete model number, product description, and option description should be given. For example: Model ADC-M12D1A2, 12 bit A/D converter, input buffer, 0 to +5V input, BCD outputs. Use the product Specification Guides where necessary. Orders may be placed with a Datel Systems field sales representative or with the factory by letter, telephone, TWX, or TELEX. Minimum order is \$30.00.

Outside the U.S.A. and CANADA: Orders should be placed with a Datel Sales Subsidiary (in West Germany, France, and the United Kingdom) or with a Datel overseas sales representative. Orders received directly will be treated the same as if placed through our overseas sales representative. In countries without a Datel Systems representative, orders should be placed by TELEX and confirmed by air mail.

FIELD SALES REPRESENTATIVES

Datel Systems employs field sales representatives throughout the United States, Canada, Europe, and the Far East. In addition, it has a Western Regional Sales Office in Santa Ana, California and Datel Sales Subsidiaries in Munich, West Germany; Paris, France; and London, England. These sales representatives are the only ones authorized by Datel Systems to solicit sales, and any information or data received by sources other than these authorized representatives or the Datel factory cannot be considered binding.

PRICES

All prices are F.O.B. Canton, Massachusetts, U.S.A. in U.S. dollars. Applicable federal, state, and local taxes are extra. Prices are subject to change without notice.

TERMS: Net 30 Days

DISCOUNTS

Quantity discounts are available when placed in a single order. OEM discounts are available on an order or contract basis. Corporate discount plans are available for all catalog items. Consult the factory for details on any of these plans. Most Datel products are covered by GSA contracts for which an appropriate Federal Government discount applies. Price lists with government discounts are available upon request.

QUOTATIONS

Price and delivery quotations made by Datel Systems or its authorized field sales representatives are valid for 60 days.

DELIVERY

Datel uses an IBM System 3, Model 10, for efficient processing of orders. All orders placed with Datel Systems are acknowledged within a few days by an acknowledgement copy of our sales order form. This copy will indicate pertinent information including estimated delivery date. This date has preference over all other agreed upon dates unless otherwise specified.

All products are shipped in rugged commercial containers suitable for insuring safe delivery under normal shipping conditions. Unless shipping method is specified, the best available method will be used. UPS, UPS Blue Label, Parcel Post, and Air Parcel Post are among the methods normally used. Datel recommends insurance on Parcel Post and Air Parcel Post shippents for tracing purposes. Shipping charges are normally prepaid and billed to the customer except for Air Freight charges which are sent collect. The appropriate data sheet and/or instruction manual is packed with each product shipped.

ORDER CANCELLATION

All orders entered with Datel Systems are binding and are subject to a cancellation charge if cancelled before or after the scheduled shipping date on the acknowledgement copy of the sales order form. The normal cancellation charge is 20% but may be higher depending on expenses already incurred and commitments made by Datel Systems.

WARRANTY

Datel Systems warrants that its products are free from defects in material and workmanship under normal use and service for a period of one year from date of shipment for module products and digital panel

meters. For systems and subsystems products, the applicable period is 90 days. Datel Systems' obligations under this warranty are limited to replacing or repairing, at its option, at its factory or facility, any of the products which shall within the applicable period after shipment be returned to Datel Systems' facility, transportation charges prepaid, and which are after examination disclosed to the satisfaction of Datel Systems to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by Datel Systems or which shall bate been subjected to misuse, negligence, or accident. In no case shall Datel Systems' liability exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Datel Systems, Inc.

SERVICE POLICY

During the warranty period, non-catastrophic failures resulting from misuse, negligence, accident, or improper application or installation of modular converter products, modular power supplies, amplifiers, or digital panel meters will be repaired for a flat charge as follows:

PRODUCT PRICE RANGE	FLAT CHARGE
\$20-\$70	\$20.00
\$71-\$150	\$30.00
\$151-\$300	\$40.00
\$301-\$500	\$55.00
\$501-Up	\$75.00 min.

RETURNING PRODUCTS FOR REPAIR

If a Datel Systems product malfunctions during the warranty period, the unit should be carefully checked to determine that the unit is in fact at fault. Then call the factory or field sales representative for authorization to return the unit. The product should be carefully packaged and shipped prepaid with original purchase order number and date and an explanation of the malfunction. Allow 3 to 4 weeks for repair and return of the unit. For out of warranty period repairs, the customer will be invoiced for repair charges. If an estimate of repair charge is required first, the following additional items should be furnished with the return unit.

- 1. A new purchase order number for the estimated repair charge.
- 2. Name of project engineer or other technical person and telephone number for contact reference.

When returning products for any reason, contact the factory first for authorization and shipping instructions. Items should not be returned air freight collect as they cannot be accepted.

Returns Outside the U.S.A. and CANADA: Contact the local sales representative or factory for authorization and shipping instructions first.

EVALUATION SAMPLES

In cases where it is necessary to evaluate the performance of a product before purchasing, a 30 day no charge evaluation model may be obtained by contacting the factory or local Datel Systems sales representative. The request must be accompanied by a purchase order stating "no charge 30 day evaluation unit." At the end of the 30 day period the customer should return the unit in operating condition. Note: module pins should not be soldered on these units. If the customer decides to keep the unit or does not return it at the end of 30 days, the no charge purchase order is converted into a normal purchase order and invoicing is sent out.

CERTIFICATE OF COMPLIANCE

Datel Systems will provide a standard Certificate of Compliance with all shipments when requested by the customer. This request must be specified on the purchase order.



Canton, Massachusetts 02021 U.S.A. TEL: (617) 828-8000 TWX: 710-348-0135 TELEX: 924461

FIELD SALES REPRESENTATIVES FOR DIRECT FACTORY CALL Canton, Mass. (617) 828-8000

NORTHEAST

Metropolitan New York Long Island, New York Northern New Jersey

EASTERN INSTRUMENTATION (516) 466-9505-Great Neck, LI, NY (201) 661-2000-New Jersey Exchange New Er.gland States

Contact Factory (617) 828-8000

Upstate New York R & D ASSOCIATES, INC. (315) 622-2350 - Liverpool, N.Y.

MIDDLE ATLANTIC

Southern New Jersey Eastern Pennsylvania Delaware Maryland Virginia

WASHINGTON, D.C. REGIONAL OFFICE (301) 840-9490 (301) 840-9491 Gaithersburg, Md.

SOUTHEAST

SABER ASSOCIATES (800) 327-1181 No. and So. Carolina. toll-free (800) 432-3007 All-Forida. toll-free

INTL. SCIENTIFIC INSTRUMENTS (205) 533-6880 - Huntsville, Ala

INTERNATIONAL SALES OFFICES

FRANCE SUBSIDIARY

DATEL SYSTEMS SARL 11 Avenue Ferdinand Buisson 75016 Paris, France Tel: 603-06-74 Telex: (842)204280

JAPAN SUBSIDIARY

DATEL KK DATEL KK Kobayashi Building 3-26-3 Higashi Shibuya-ku, Tokyo 150 Tel: Toyko 499-0631 Telex: 2422389

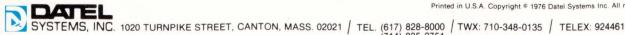
Yachiyo Bldg. Higashikan 33 Daikucho Kita-Ku, Osaka 530 Tel: (06) 354-2025

UNITED KINGDOM SUBSIDIARY

DATEL (U.K.) LTD Stephenson Close Portway Industrial Estate Andover Hants Tel: Andover (0264) 51055

WEST GERMANY SUBSIDIARY

DATELEK SYSTEMS GmbH 8 MUENCHEN 71 BECKER-GUNDAHLSTRASSE 1 Postf. 71-03-04 Tel. (089) 78-40-45 Telex: 5212855



MIDWEST

GEORGE R. PETERS ASSOC. (313) 362-1220 - Troy, Mich

INSTRUMENTATION SYSTEMS INC. Ohio

West Virginia Western Penn. Kentucky (216) 486-0782 — Cleveland, Ohio (513) 294-2838 — Davton, Ohio (412) 243-1111 - Pittsburgh, Pa.

CARTER ELECTRONICS, INC

(312) 585-5485 — Chicago, III.
(414) 464-5555 — Milwaukee, Wis.
(317) 293-0696 — Indianapolis, Ind.
(612) 559-1976 — Minneapolis, Minn.

TECHNICAL REPRESENTATIVES INC. (314) 731-5200 — Hazelwood, Mo. (913) 782-1177 — Olathe, Ks. (319) 396-5662 — Cedar Rapids, Ia. Southern Illinois lowa Nebraska

E & M MICROSYSTEMS MKTG., INC. (713) 783-2900 — Houston, TX (214) 238-7157 — Dallas, TX (512) 266-1750 — Austin, TX

MIDWEST DISTRIBUTOR COMPONENT SPECIALTIES, INC. Dallas, Tx (214) 357-6511 Houston, Tx (713) 771-7237 Austin, Tx (512) 459-3307 Tulsa, Ok (918) 664-2820

AUSTRALIA

DIGITAL ELECTRONICS (MARKETING) PTY. LTD. 4/29 Hotham Parade Artarmon 2064, N.S.W. Australia Tel: 437-6668 Cable: DITRONICS, Sydney

AUSTRIA & E. EUROPE

BACHER ELEKTRONISCHE GERATE GES. M.B.H. Meidlinger Haupstrasse 78 A-1120 Vienna Austria Tel: 83 63 96 0 Telex: (01) 1532

BELGIUM

SIMAC ELECTRONICS spri Bd. du Triomphe 148 1160 Bruxelles Belgium Tel: 02-6724556 Telex: 23662

DENMARK

PARATRON A/S Saxhojvej 19 DK-2500 Valby, Denmark Tel: (01) 74 44 66 Telex: 16444 Cable: PASEINIK

FINLAND

HAVULINNA OY Vuorikatu 16 SF-00100 Helsinki, Finland Tel: (90) 661451 Telex: 12426

ROCKY MOUNTAIN STATES

CLEVELAND ENTERPRISES Arizona Colorado Southern Idaho Nevada New Mexico litah Wyoming (505) 345-2481 — Albuquerque, N.M. (602) 949-0872 — Phoenix, Ariz. (303) 751-3252 — Aurora, Colo.

WEST

WESTERN REGIONAL OFFICE (714) 835-2751 — Santa Ana, Calif. (213) 933-7256 — LA Exchange NO. CALIF. DISTRICT SALES OFFICE (408) 733-2424 - Sunnyvale, Calif.

NORTHWEST TASCO, INC. Oregon Washington (206) 453-1414 | Bellevue, Wash

INDIA

SMITRONIX INTERNATIONAL 201, Mollee Tolla Building 504, Linking Road, Khar Bombay 400 052, India Tel: — 536238 Cable: SMITRONIX

ISRAEL

MTI ENGINEERING LTD. P.O. Box 16349 182 Ben Yehuda Street Tel Aviv, Israel Tel: 244090, 236334 Telex: 32200

ITALY

3G - ELECTRONICS s.r.l. Via Perugino 9 Postale Milano 3/47932 20135 Milano, Italy Tel: 544291, 543096 Telex: 35024

NETHERLANDS

SIMAC ELECTRONICS b.v. Eindhovenseweg 58 Steensel, THE NETHERLANDS Tel: (04970)-2011 Telex: 51037

NEW ZEALAND

DAVID J. REID (N.Z.) LTD. 3-5 Auburn St. Takapuna Auckland 1, New Zealand Tel: 492-189 Telex: 2612

Printed in U.S.A. Copyright @ 1976 Datel Systems Inc. All rights reserved

(714) 835-2751

(408) 733-2424 (213) 933-7256 (301) 840-9490

HAWAII

HAWAII DATA SYSTEMS (808) 946-1533 - Honolulu, Hawaii

CANADA

MULTILEK. INC. (613) 825-4695 — Ottawa, Ontario (416) 245-4622 — Toronto, Ontario (514) 481-1350 — Montreal, Quebec

CANADIAN DISTRIBUTOR (514) 389-8051 — Montreal, Quebec (613) 237-6150 — Ottawa, Ontario (416) 678-0401 — Rexdale, Ontario

FOR APPLICATIONS ASSISTANCE ON DATEL SYSTEMS' PRODUCTS CALL: (213) 933-7256 (714) 835-2751 WESTERN REGIONAL OFFICE SANTA ANA, CALIFORNIA

(617) 828-8000 HOME OFFICE CANTON, MASS.

NORWAY

MORGENSTIERNE & CO. A/S Konghellegate 3 Oslo 5, Norway Tel: 37 29 40 Telex: 11719

SOUTH AFRICA

PETER JONES ELECTRONIC EQUIPMENT (PTY.) LTD. P.O. Box 31582 Braamfontein, Johannesburg South Africa Tel: 22-3658 Telex: 8-6935

SPAIN

AUPOCA ELECTRONICA Y SISTEMAS Colombia, 34 Madrid, Spain-16 Tel: 457 53 12 Telex: 23742

Rosellon 345 Barcelona, Spain-9 Tel: 257 48 98

SWEDEN

AB NORDQVIST & BERG AB NOHDQVIST & BERG Box 9145 Bergsunds Strand 37 S-10272 Stockholm, Sweden Tel: 08-69 04 001 Telex: 10407

SWITZERI AND

TRACO ELECTRONIC CO. LTD. 1 Jenatschstrasse 8002 Zurich, Switzerland Tel: 01/3607 11 Telex: 54318

1/77 BULLETIN LGREJ05701

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

DIGITAL PANEL PRINTER Model DPP-7



DPM's language.