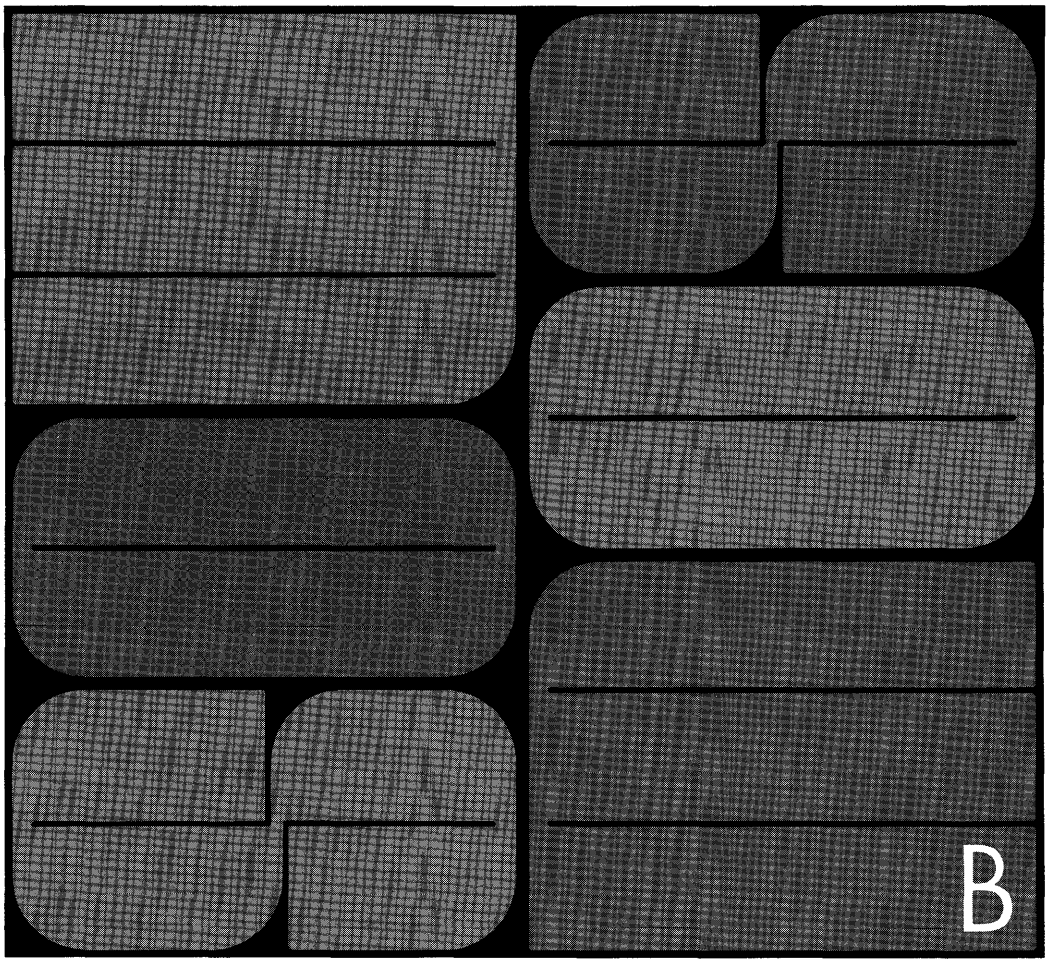
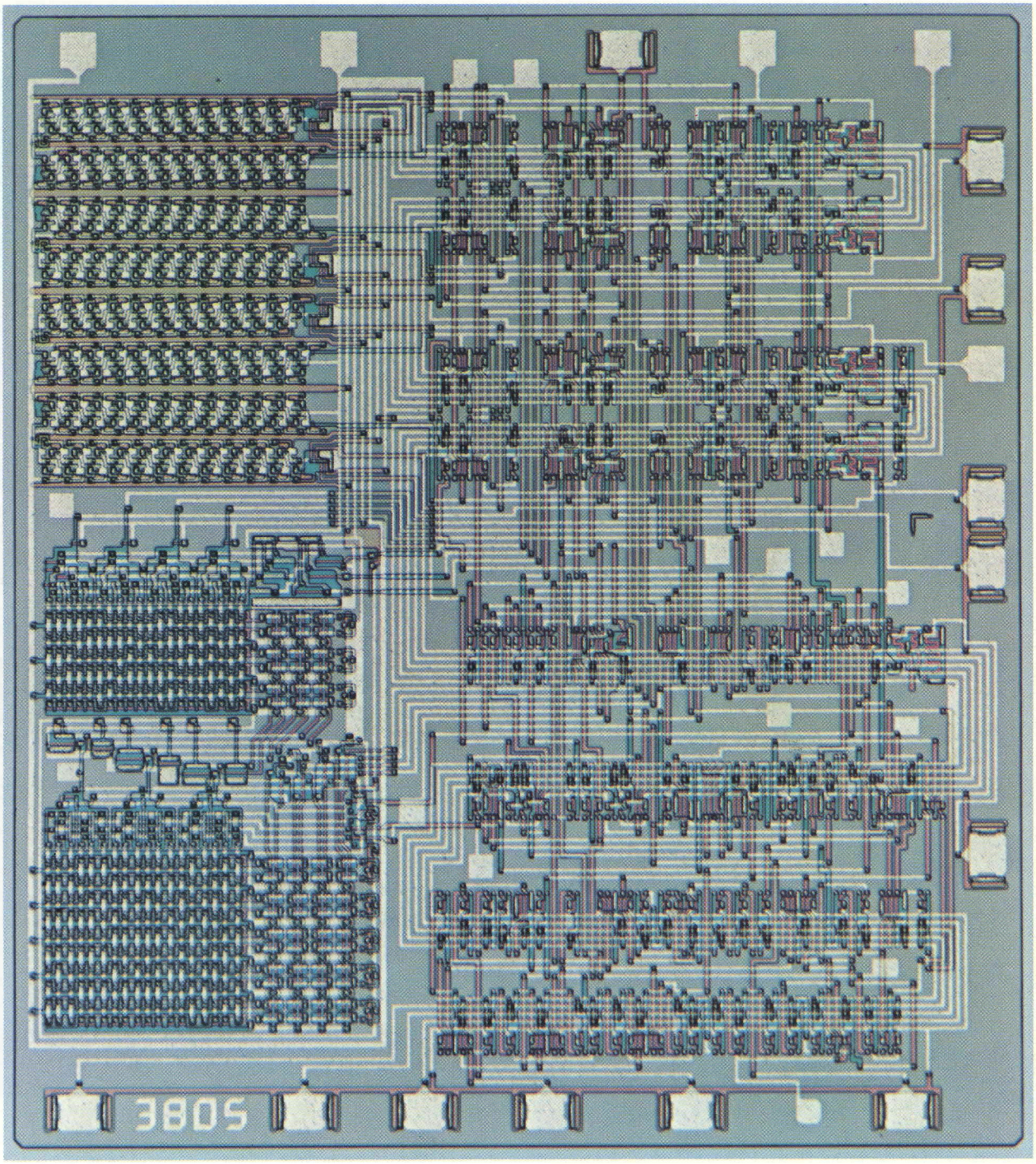
PPS 25–Programmed Processor System



3805 – PPS 25 Arithmetic Unit



APPENDIX B

PPS 25 — PROGRAMMED PROCESSOR SYSTEM

INTRODUCTION

MOS/LSI technology was first applied commercially in electronic desk top calculators. In the late 1960's, virtually every calculator manufacturer had new electronic designs on the market that utilized MOS/LSI chips. The low cost potential of MOS/LSI made possible what is now acknowledged to be a revolution in calculator system design.

The advances of MOS/LSI technology in the 1970's have made possible both increased circuit complexity and performance. In this decade a similar equipment revolution is foreseen in the minicomputer and data processor systems field where required computational speed and logic density are higher than in most calculator systems.

To meet the needs of this market, Fairchild developed a family of micro-programmed MOS/LSI processor blocks called the PPS 25 (Programmable Processor System).

Equipment engineers have long recognized the desirability and flexibility of designing digital systems using a micro-programmed processor as the heart of the design. Such systems are very practical in that they can be readily programmed around specific system requirements. Unfortunately, the size and cost of minicomputers to date have limited their application to relatively large systems. However, with the availability of the PPS 25, small systems can be readily and economically designed. In fact, it is now possible for the equipment designer to develop small programmable digital processing systems for under $50.

The PPS 25 is a buss-oriented system which can be used in a wide variety of ways in data processors. The heart of the system (see *Figure B-1*) is the 3805 Arithmetic Unit and the 3806 Function and Timing Unit, which together perform all timing, control and arithmetic functions. Auxiliary to these chips is the 3810 ROM which stores micro-programs and data look-up tables. The 3808 and 3809 shift register memory devices store data. Keyboards can be attached by using the 3803 and 3807 input devices while data output for displays or other communication equipment is provided by the 3811.

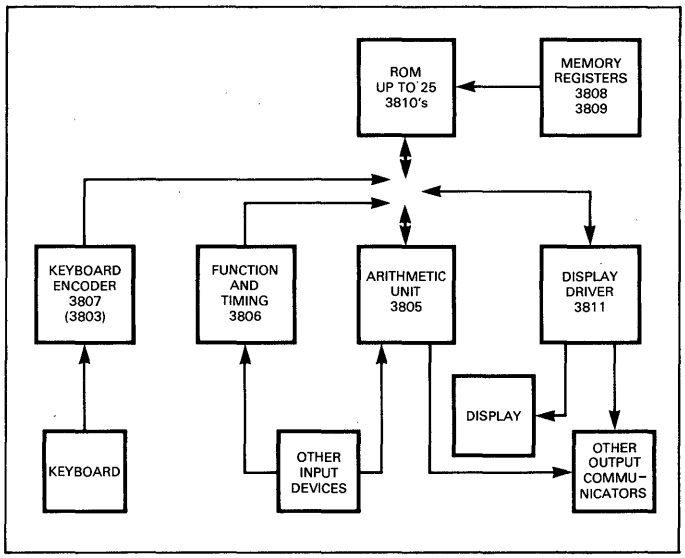


Fig. B-1. PPS-25 Micro-Programmed Processor System

Although the set is comprised of standard devices, it can be personalized to meet unique systems needs by micro-programming the 3810 ROM. The result is system and design economy through the use of standard components, but with customized design through the customer's proprietary ROM code patterns.

FEATURES OF THE PPS 25 SYSTEM

The PPS 25 system was designed to fill the gap between intermediate to upper-end calculators and minicomputers. It substitutes a few MOS/LSI packages where normally several hundred TTL MSI or SSI packages would be required.

The PPS 25 system has a versatile instruction set which permits the system to perform a wide variety of different functions. The basic operating features of the set are summarized below.

- BCD Serial/Parallel Processing Unit with 95 Instructions
- 25-Digit Serial, 4-Bit Parallel Organization
- 62.5 μs Word Time
- 2.5 μs Bit Time
- Programmable Time Enable Patterns Provide Versatile Data Field Selection Within the 25-Digit Word
- 4-Level Subroutine Nesting
- Both 2 and 3-Way Conditional Branch Structure
- External Interrupt Capability
- High Speed Operation Assured by
  - — Basic Serial/Parallel Arithmetic Unit
  - — Overlapped Fetch and Execute Instruction Cycle
  - — Separate Micro-instruction and Data Busses
- Up to Seven 25-Digit Memory Registers Available with Arbitrary Expansion Provided
- Up to 26 Programmable ROMs — 256 x 12 Bits Each
- Input Keyboard Capability for Up to 61 Keys and 32 Mode Switches
- Standard Output Display Chip Available for 16-Digit Display or Communications Interface with Provision for Other Custom Outputs
- Versatile Data Buss Structure Provides Flexible I/O Interface Expansion

APPLICATIONS OF THE PPS 25 SYSTEM

The PPS 25's flexible set of 95 instructions permits the system to perform a wide variety of functions. Examples of systems where the PPS 25 can be employed are:

Upper-End Scientific Calculators

Scientific calculators formed with these MOS/LSI blocks handle up to 25-digit numbers. They can be programmed to handle either fixed point, floating point, or scientific notation, and, in their basic form, will add, subtract, multiply, divide and take square root. They also can perform complex arithmetic functions such as sine, cosine, and log. The programmable ROMs provide a great number of different capa-

bilities. Multiply, for example, can be performed with any one of a number of algorithms. Furthermore, the word length need not be 25 digits. The blocks can be used to build a calculator with any number of digits up to 25.

Internally, the chips handle 25-digit words (stored in four parallel 25-bit shift registers). The word length actually used and the format within the word are entirely optional. A possible format for a calculator with scientific notation would be to devote three digits to the exponent and its sign, leaving 21 digits for the mantissa and one digit for its sign.

All numbers are stored and processed in binary coded decimal form. These four bits are processed in parallel fashion, while the digits are processed in series. The system can be clocked at a maximum rate of 400 kHz. At this rate the digit and word times are 2.5 and 62.5 μs respectively.

Up to 61 keys and 32 mode switches can be handled by the standard keyboard interface circuit, and up to 16 digits of display can be controlled by the 3811 output chip.

Control Systems

Because of the micro-program flexibility, the PPS 25 system can be used in process control systems, vending machine systems, medical instrumentation, numerical machine control, traffic light controllers, and in virtually all medium speed programmed control systems.

Computer Systems

The PPS 25 system is also organized for high speed calculations and data processing. Basic features — serial/parallel word structure, overlapped fetch and execute, and separate data and micro-instruction busses — were designed-in. This was done to extend the application of the set into the fields of electronic point-of-sale terminals, cash registers banking terminals, small business machines, etc. For example, the addition of two 25-digit numbers can be executed in 62.5 μs, and the multiplication of similar numbers can be accomplished in less than 50 ms.

Peripheral Systems

This micro-programmed system is also ideally configured for many peripheral applications. If keyboard entry is required, the 3803 and 3807 devices provide a direct interface, with full n-key rollover and anti-bounce on up to 61 keys, plus 32 mode switches. Other forms of input data can be fed directly into the data source buss. If digit display of up to 16 digits is required, the 3811 device provides the necessary interface; or multiple 3811 devices can serve as a general output communication link.

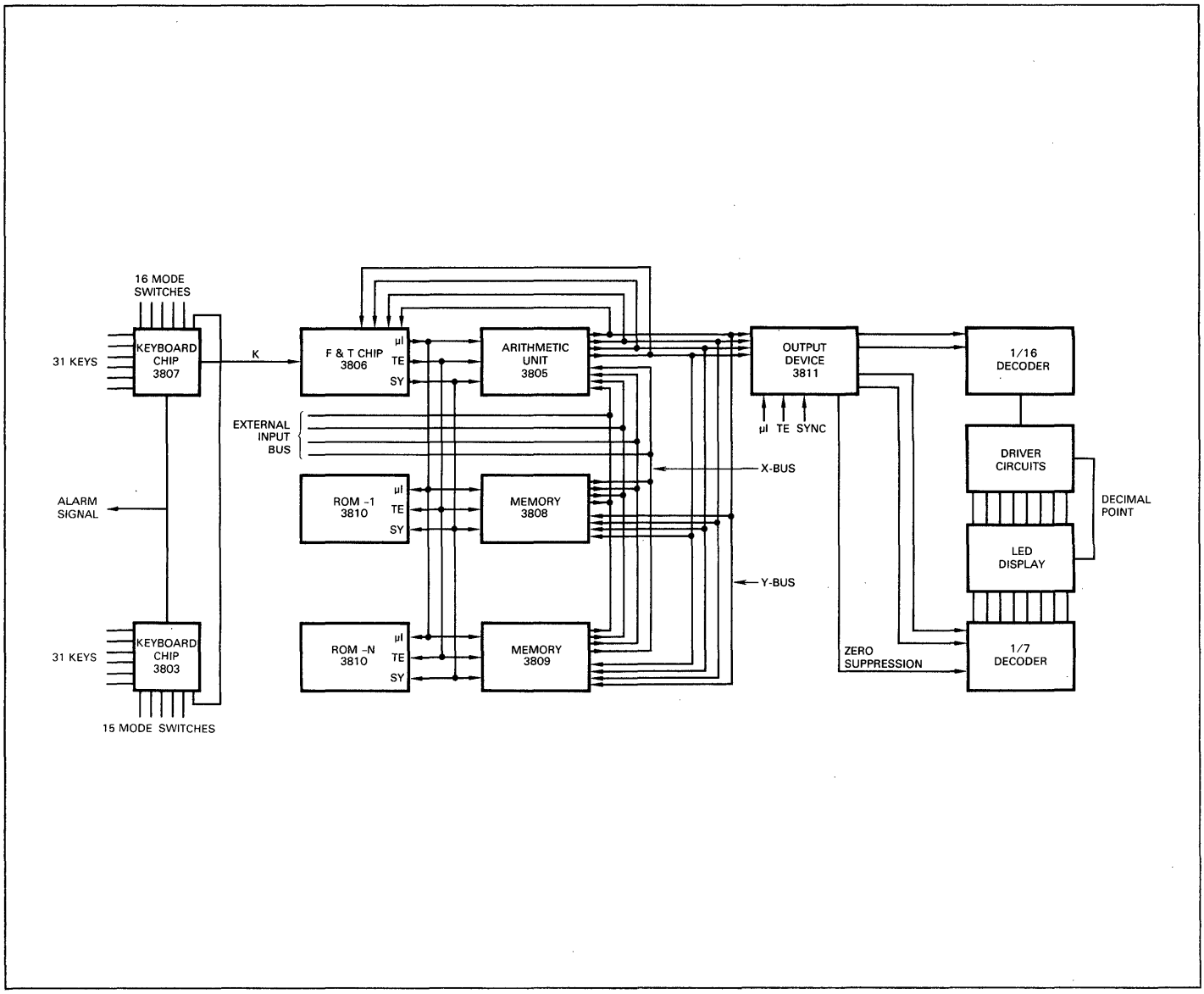


Fig. B-2. Typical Processor System

If special interfaces are required, such as printers or mag card readers, custom interfaces can be provided directly from the destination buss or ROMs can be utilized to emulate the desired interface within the structure of the system.

DESCRIPTION OF THE PPS 25 SYSTEM

The basic MOS/LSI building blocks used in the PPS 25 System are listed in *Table B-1*, along with their pinouts. All of these devices are manufactured with P-channel silicon gate technology. There are 2-phase dynamic logic circuits incorporated. Standard +5 V, -10 V and ground supplies are required. Full TTL compatibility is provided at all external I/O interfaces.

The building blocks are all designed as buss-oriented devices. *Figure B-2* shows how they are connected together to form a typical processor system. As this figure shows, there are two data busses. The X-data buss is the source (or input) data buss. It is four bits wide (BCD), and provides the input for each 25-digit word being processed. The Y-data buss is the destination (or output) data buss. The micro-instruction buss is used to fetch a 12-bit micro-instruction from the selected ROM. Timing for the fetch and execute cycle are provided from the 3806 function and timing chip.

The time enable signal (TE) provides a data field selection within the 25-digit word, as specified by the customer time enable patterns. The K line completes the system. This is the keyboard buss which connects scanned data from the keyboard devices into the 3806 device.

The simplified operation of each of the devices is as follows:

3807/3803 Keyboard Devices

The basic keyboard device is the 3807. The 3803 extends the keyboard capabilities beyond 32 keys. The function of the 3807 device is to generate a 5-bit code for each key that makes a transition from an inactive state to an active state. This 5-bit code is stored on the chip until a command occurs in the program, instructing the chip to supply the 5-bit code to the addressing register in the 3806 function and tuning chip. An anti-bounce feature is provided by a sample and hold circuit in the keyboard scanner.

The keyboard is full "legato", provided that an external diode is used with each key. That is, new entries can be made without having to release previously depressed keys, and up to two key strokes can be stored in their proper sequence by the keyboard during the time the system is processing previous data.

3805 Arithmetic Chip

This chip contains the adder/subtractor plus a 25-digit memory register. The 3805 device, along with auxiliary memory devices 3808 and 3809, receive micro-instructions from the 3810 ROMs. These micro-instructions contain a data source address, a data result destination address, and an operation code. The instructions allow subtractions, additions, or transfers to take place between registers. Incrementing, decrementing, complementing, and clearing of any of the seven registers and other operations can also be performed. Data can be entered either externally or created internally by the use of a "load immediate" micro-instruction.

3806 Function and Timing Unit

This device provides the address and control logic for the PPS 25 system. Included functionally on this device are the following:

- Instruction address register
- Micro-instruction address adder
- Program branch decision logic
- Two 25-bit status registers
- Pointer and status counters
- Time enable pattern generator
- Master timing circuit
- 4-level nested subroutine linkage

This logic provides the traffic control function for the entire PPS 25 system, in that it contains the master timing counter and generates the sync signal.

For example, the time enable portion of the instruction is used to select the portion of the word upon which a given command is to be executed. There are six programmable time enable patterns available, each called up by a different code.

The status registers are used for storing return addresses for subroutine calls, storing program flags, and storing mode control switch status.

3808/3809 Memory Registers

These devices each contain three 4-bit BCD parallel, 25-digit serial register memories. The registers, which can be directly addressed by the arithmetic instructions, work in conjunction with the 3805 arithmetic unit described above.

3810 ROM

The micro-instructions for the PPS 25 are contained in the 3810 read-only memory device. As many as 25 of these devices may be incorporated in parallel in a single system. All ROMs in a system simultaneously receive an 8-bit address, and the selected ROM shifts out the selected 12-bit instruction. Each 3810 device contains 256 x 12 bits, and are mask programmable.

Data (including binary) stored in the ROM program can be transferred to the accumulator. This data is useful in the generation of constants, addresses, etc.

3811 Output Device

The 3811 device provides the necessary latches for receiving, storing, and transmitting the BCD representation of a character. A position counter provides an output code for 1 of 16 positions, necessary to multiplex up to 16 display elements. Decimal point, sign, and general purpose programmed flag outputs are also provided as shown. Leading zero suppression and blanking control are also provided within the logic of the 3811.

Instruction Set

Micro-instructions are classified into three types in the PPS 25 systems: arithmetic, control, and input/output. Arithmetic instructions relate to data movement and manipulation under field selection control of the time enable patterns. Control instructions relate to status conditions affecting ROM address selection and branch structure. There are 64 I/O instructions, many of which are available for customer specified interface requirements.

TABLE B - 1

PPS 25 DEVICE PINOUTS

DEVICE	3803 KEYBOARD	3807 KEYBOARD	3805 ARITHMETIC	3806 F & T	3808 MEMORY	3809 MEMORY	3810 ROM	3811 DISPLAY
PKG. TYPE	7Q	7Q	7T	7R	7K	7K	7K	7R
NO. PINS	40	40	18	24	16	16	16	24
1	D_2	D_2	Y_3	V_{SS}	X_0	X_0		A_1
2	D_1	D_1	X_3		V_{SS}	V_{SS}		A_0
3	V_{SS}	V_{SS}	V_{SS}	V_{GG}	V_{GG}	V_{GG}	V_{SS}	P_1
4	V_{GG}	V_{GG}	X_2	P_2	V_{DD}	V_{DD}	MI	V_{GG}
5	V_{DD}	V_{DD}	X_1	TEN	Y_0	Y_0	MIO	P_2
6			X_0	V_{DD}	Y_2	Y_2		V_{DD}
7	R_5	R_5	V_{DD}	FLAG	SYNC	SYNC	V_{DD}	MI
8	R_4	R_4	P_2	F_1	TEN	TEN		TEN
9	R_6	R_6	V_{GG}	BOROW	P_2	P_2		SYNC
10	R_3	R_3	P_1	TENIN	P_1	P_1		V_{SS}
11	R_7	R_7	MI	MI	X_2	X_2		Y_0
12	R_2	R_2	BOROW	P_1	MI	MI	P_2	Y_1
13	R_8	R_8	SYNC		X_3	X_3	V_{GG}	Y_2
14	R_1	R_1	FLAG	BSTN	Y_3	Y_3	P_1	Y_3
15			TEN	SFT	Y_1	Y_1	SYNC	BN
16	TEST	TEST	Y_0	PFTN	X_1	X_1		K_0
17			Y_1	S25TN				K_1
18	MI	MI	Y_2					K_2
19				Nu				K_3
20				TSY				S
21				KN				M
22	P_1	P_1		MIO				DP
23	P_2	P_2		SYNC				A_3
24				TEST				A_2
25								
26								
27	SYNC	SYNC						
28	S_8	S_8						
29	S_7	S_7						
30	S_6	S_6						
31	S_5	S_5						
32	S_3	S_3						
33	S_4	S_4						
34	S_2	S_2						
35	S_1	S_1						
36								
37	K	K						
38	A	A						
39	D_4	D_4						
40	D_3	D_3						

ARITHMETIC INSTRUCTION TABLE

MNEMONIC	FUNCTION	OPERATION DESCRIPTION
ADD	BCD Addition	The contents of the source register are added to the accumulator and the result is stored in the destination register.
SUB	BCD Subtraction	The contents of the source register are subtracted from the accumulator and the result is stored in the destination register.
MOV	Move	The contents of the accumulator are transferred to the destination register. The contents of the source register replace the original contents of the accumulator.
COM	BCD Complementation	The contents of the source register are complemented (subtracted from zero) and the result is stored in the destination register.
INC	Increment	The contents of the source register are incremented by one and the result is stored in the destination register.
DEC	Decrement	The contents of the source register are decremented by one and the result is stored in the destination register.
LSH	Left Shift	The contents of the selected register are shifted left one digit. The least significant digit position is cleared to zero.
CLR	Clear	The contents of the selected register are cleared.
RSH	Right Shift	The contents of the selected register are shifted right one digit. The most significant digit position is cleared to zero.
SLI	Shift Load Immediate	The contents of the accumulator are shifted left one digit. A 4-bit character from the micro-instruction is loaded into the low digit position. The result is stored in the accumulator.
CR	Change ROM	This command selects a unique ROM for program execution.
BOC	Conditional Branch	When the branch instruction is preceded by a test or an interrogate instruction, conditional branching is provided.
BRU	Unconditional Branch	When the branch instruction is not preceded by a test or an interrogate instruction, the branch instruction acts as an unconditional branch.
NOP	No Operation	No Operation.
SSB	Set Status Bit	Specifies which status bit is to be set to a "1".
RSB	Reset Status Bit	Specifies which status bit is to be reset to a "0".
CSR	Clear Status Register	This execution resets all 25 status bits to "0".
ISB	Interrogate Status Bit	This instruction is used to determine the status ("1" or "0") of a particular bit in the status register.
CSB	Complement Status Bit	Causes the addressed status bit to be conditionally complemented.
EXS	Exchange Status	Exchanges the contents of the two status registers with each other.
STM	Store Modes	This instruction causes the function and timing chip to accept and store mode switch data.
SPT	Set Pointer	Causes pointer counter to be forced to a selected one of 25 positions.
IPT	Interrogate Pointer	Interrogates position of pointer.
PLF	Pointer Left	Moves pointer one position to left
PRT	Pointer Right	Moves pointer one position to right.
SA2	Store Address #1	Causes current address A in addressing register to be stored.
RA1	Recall Address #1	Fetches eight bits stored by SA1 and places them back in addressing register.
SA1	Store Address #2	Causes current address A in addressing register to be stored.
RA2	Recall Address #2	Fetches eight bits stored by SA2 and places them back in addressing register.
BR3	Branch 3	Causes 3-way conditional branch mode to occur.
BR2	Branch 2	Causes 2-way conditional branch mode to occur.
XI/O	Input/Output Commands	There are up to 64 I/O commands available to control customer input/output devices.