CHAPTER 3 FUNCTIONS

This chapter describes the functions of SPC internal registers, memory, and buffers.

3.1 INTERNAL REGISTERS

Indicates the relationship between signal input to access SPC internal registers and accessed registers.
Depending on the type of information, the SPC register where the MPU reads/writes differs (data register or MCS buffer).

■ Internal Register Access

Tables 3.1a and 3.1b show the access state to internal registers for 80 series and 68 series modes.

Table 3.1a Internal Register Access (80 Series Mode)

$\overline{CS0}$	$\overline{BHE}$*1	A0	D15 to D8*2	D7 to D0
1	—	—	HI-Z	HI-Z
0	0	0	Odd address register	Even address register
0	0	1	Odd address register	HI-Z
0	1	0	HI-Z	Even address register
0	1	1	HI-Z	Odd address register

*1 Set $\overline{BHE}$ pin to 1 for 8-bit bus operation.
*2 Connect about 10-kΩ pull-up resistor to the UDP and D15 to D8 when using 8-bit bus..

Table 3.1b Internal Register Access (68 Series Mode)

$\overline{CS0}$	$\overline{UDS}$*2	LDS	A0*1	D15 to D8*3	D7 to D0
1	—	—	—	HI-Z	HI-Z
0	0	0	1	Even address register	Odd address register
0	0	1	1	Even address register	HI-Z
0	1	0	0	HI-Z	Even address register
0	1	0	1	HI-Z	Odd address register
0	1	1	—	HI-Z	HI-Z

*1 Set A0 pin to 1 for 16-bit bus operation.
*2 Set $\overline{UDS}$ pin to 1 for 8-bit bus operation.
*3 Connect about 10-kΩ pull-up resistor to the UDP and D15 to D8 when using 8-bit bus.

■ Data Flow During Transfers

Depending on the type of information, the SPC register where the MPU reads/writes differs (data register or MCS buffer). There are also program transfers and DMA transfers. For DMA transfers, data phases are supported, but messages, commands, and status phases are not.

Table 3.1c shows the relationship between information types and registers (program transfer/ data transfer). Figure 3.1 outlines the internal flow of information.

Table 3.1c Relationship between Information Types and Registers

Transfer / Information	Program transfer (via MPU bus)	DMA transfer (via DMA bus)
Message phase	MCS buffer (32 byte input/output)	Not possible
Command phase		
Status phase		
Data phase	Data register	Data register

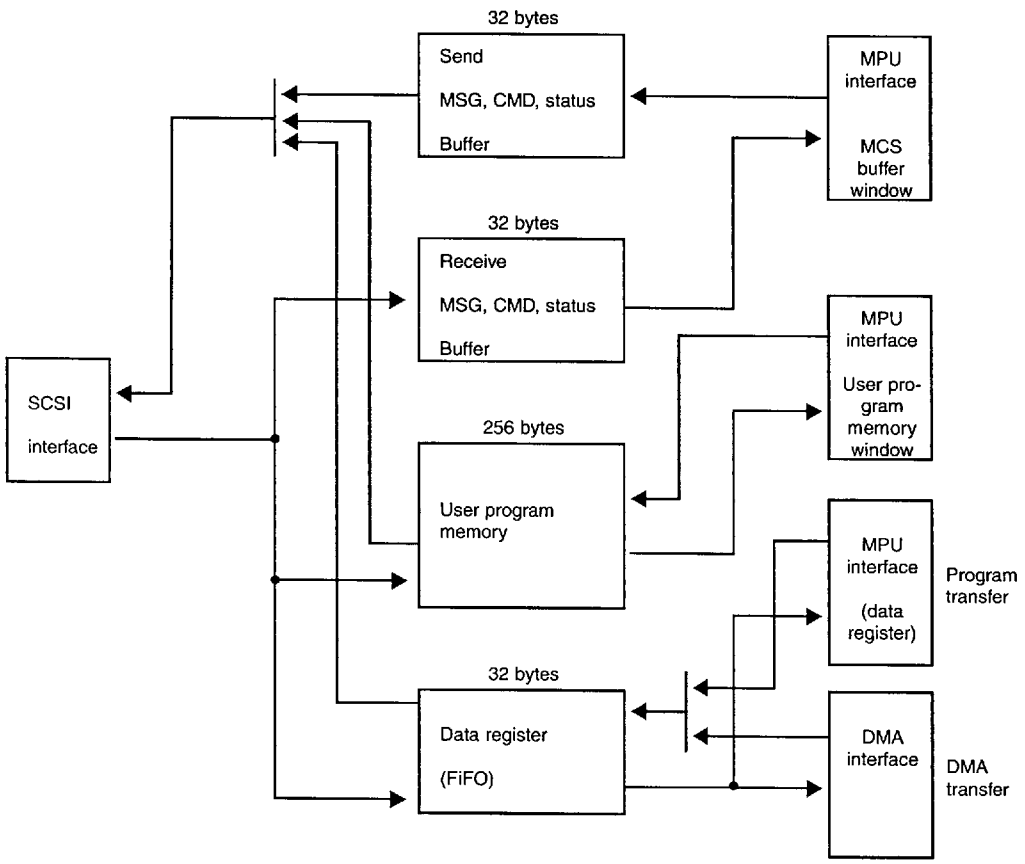
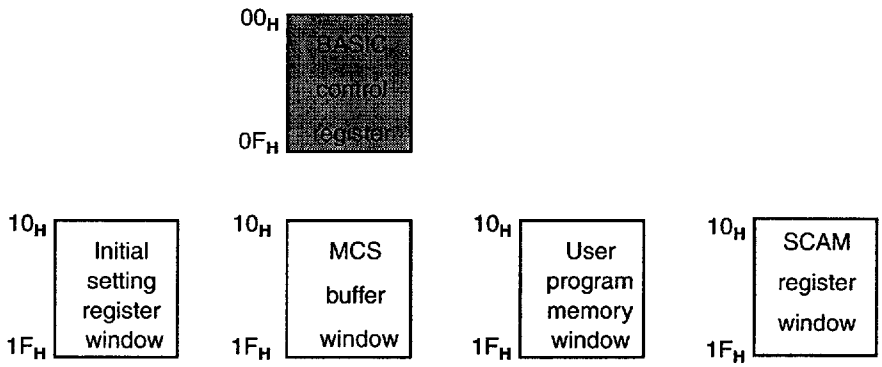


Figure 3.1 Internal Flow of Information

3.2 BASIC CONTROL REGISTER

This register controls the SPC and confirms SPC states.



Note: SCAM register window is available in MB86604L only.

■ BASIC Control Register

Table 3.2 lists the BASIC control register.

Table 3.2 BASIC Control Register List

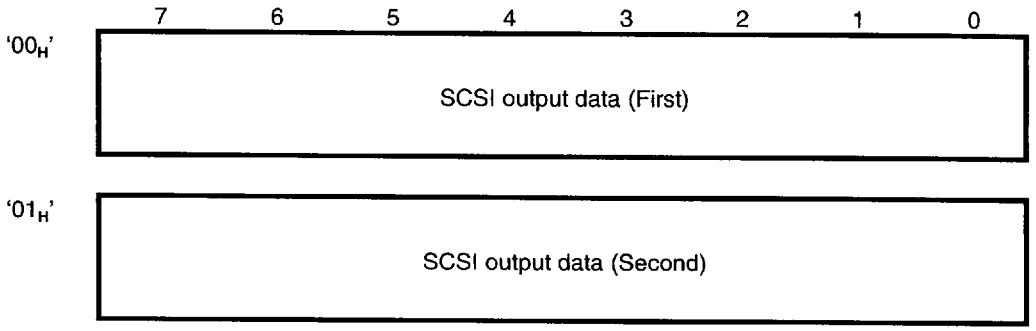
No	Address					Write	Read
	A4	A3	A2	A1	A0		
00	0	0	0	0	0	SCSI output data register (First)	SCSI input data register (First)
01	0	0	0	0	1	SCSI output data register (Second)	SCSI input data register (Second)
02	0	0	0	1	0	Direct control register	SPC status register
03	0	0	0	1	1	(RESERVED)	Nexus status register
04	0	0	1	0	0	SEL/RESEL-ID register	Interrupt status register
05	0	0	1	0	1	Command register	Command step register
06	0	0	1	1	0	Data block register (MSB)	←
07	0	0	1	1	1	Data block register (LSB)	←
08	0	1	0	0	0	Data byte register (MSB)	←
09	0	1	0	0	1	Data byte register	←
0A	0	1	0	1	0	Data byte register (LSB)/MC byte register	←
0B	0	1	0	1	1	Diagnostic control signal register	SCSI control signal status register
0C	0	1	1	0	0	Transfer mode register	←
0D	0	1	1	0	1	Transfer period register	←
0E	0	1	1	1	0	Transfer offset register	←
0F	0	1	1	1	1	Window address register	Modified byte register

3.2.1 Output Data Register (Write)

In the data phase program transfer mode, the output data register outputs data to the SCSI bus.

■ **Output Data Register (Write)**

The output data register configuration is shown below.

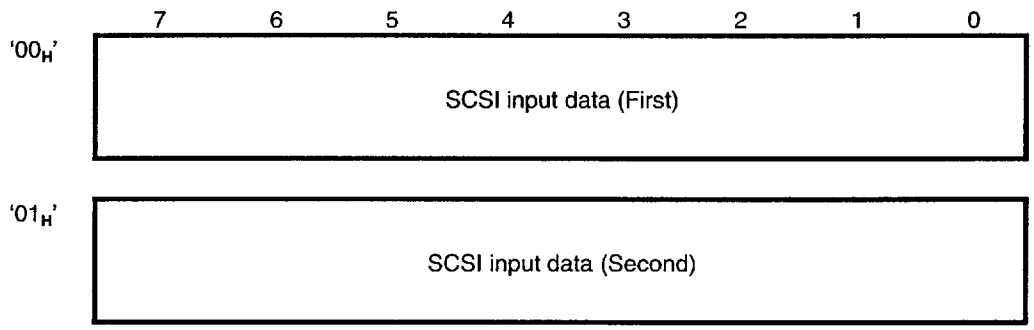


3.2.2 Input Data Register (Read)

In the data phase program transfer mode, the input data register inputs data to the SCSI bus.

■ **Input Data Register (Read)**

The input data register configuration is shown below.



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3.2.3 Direct Control Register (WRITE)

The direct control register (WRITE) provides direct control regardless of whether a command is issued to the SPC.

■ Direct Control Register (WRITE)

The direct control register bit configuration is shown below.

	7	6	5	4	3	2	1	0
'02_H'	DC 7	0	0	DC 4	0	0	0	0

Next, the functionality of each bit is described.

BIT 7: ATN signal control
Control bit for direct control of ATN signal assert.
When the SPC operates as an initiator, the ATN signal is asserted by writing 1 in BIT 7. Effective for interrupting a data phase (produces attention condition).

After writing 1 in BIT 7 and asserting the ATN signal, be sure to write 0 and return to the initial state before issuing the next command. The ATN signal is not negated by writing 0. In order to negate the ATN signal, issue a RESET ATN signal.

In Figure 3.2.3, the relationship between transfers and BIT 7 is diagrammed in a flowchart.

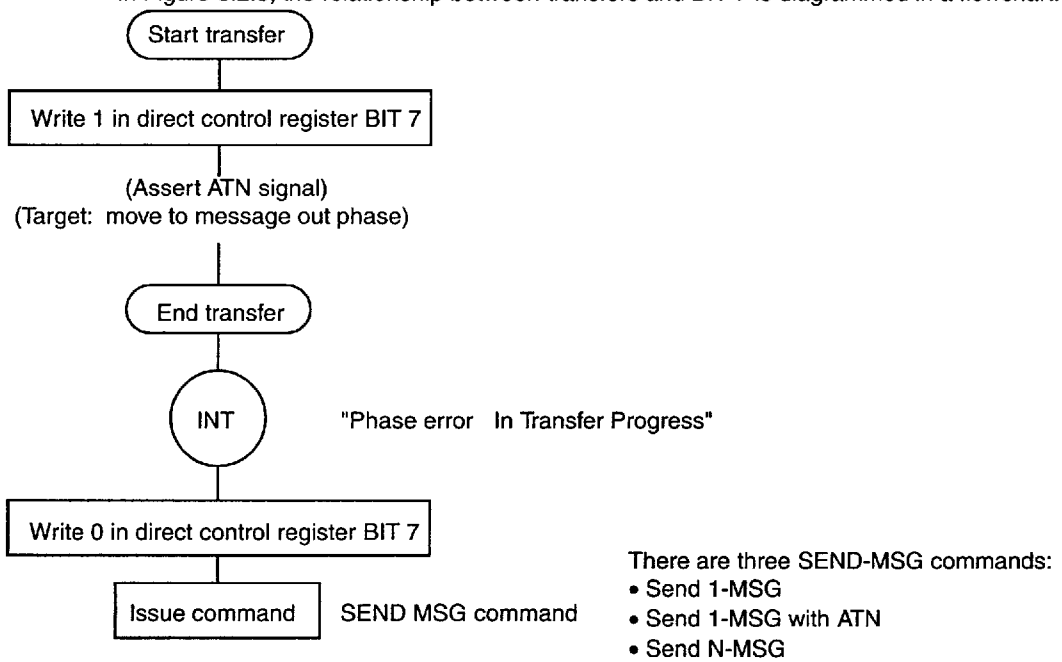


Figure 3.2.3 Transfer Flowchart (Direct Control Register: BIT 7)

BIT 4: TMOUT signal clear

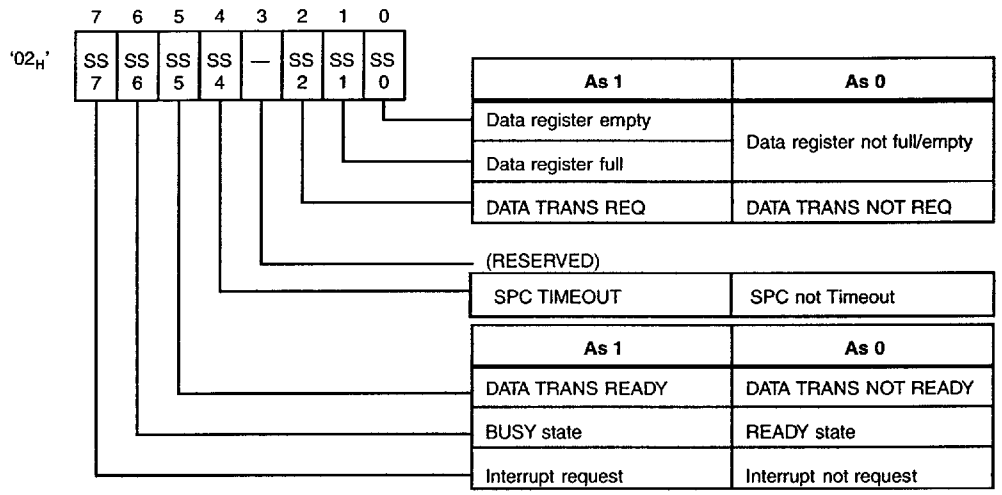
Control bit to clear the TMOUT pin signal.
The TMOUT pin is cleared by writing "1" to this bit while the SPC Busy bit (Bit 6) in the SPC Status Register (02h) = "0". When SPC Busy = "1", the TMOUT pin is not cleared.

3.2.4 SPC Status Register (READ)

The SPC status register shows the operating state of the SPC.

■ **SPC Status Register (READ)**

The SPC status register (READ) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7: Interrupt request
When there is an interrupt request from the SPC to the host MPU, 1 is indicated. While linked to the INT signal (interrupt request signal) to the host MPU, this bit indicates 1 whenever there is an interrupt request regardless the interrupt is enabled or disabled (interrupt enable register).

BIT 6: BUSY state
Shows that the SPC is operating.
When the SPC receives a command or automatically begins operating (at Automatic selection/reselection response mode), 1 is indicated.
When the operation is successfully completed or ends unsuccessfully because of an error, 0 is displayed.
If a command is issued when BIT 6 is 1, except for SOFTWARE RESET, the command is ignored and a COMMAND REJECTED interrupt reported.

BIT 5: DATA TRANS READY state
Shows that a transfer is possible (during transfer).
When the SPC receives a transfer-related command and the SPC internal set-up finishes, 1 is displayed in this bit.

BIT 4: SPC Timeout State
Shows that SPC is operating over the time specified in the SPC timeout Setting register. When the SPC's operation terminated within the time specified, this bit value is "0". This bit can be cleared by writing "1" to the TMOUT pin clear bit (Bit 4) of Direct Control Register while SPC busy=0.

BIT 2: DATA TRANS REQ

Shows state of data phase transfer request.
During SCSI-INPUT, when two or more bytes can be read from the data register (the data register contains two or more bytes) or when the data register contains the last byte, 1 is indicated.
During SCSI-OUTPUT, when two or more bytes can be written in the data register (the data register contains 30 or less bytes) or the last byte can be written in the data register, 1 is indicated. Refer to this bit when conducting a program transfer.
Also, when DMA transfer mode, "1" will be indicated in this bit while the DREQ signal is asserted.

BIT 1: Data Register FULL

When the data register is FULL, 1 is indicated.

BIT 0: Data Register EMPTY

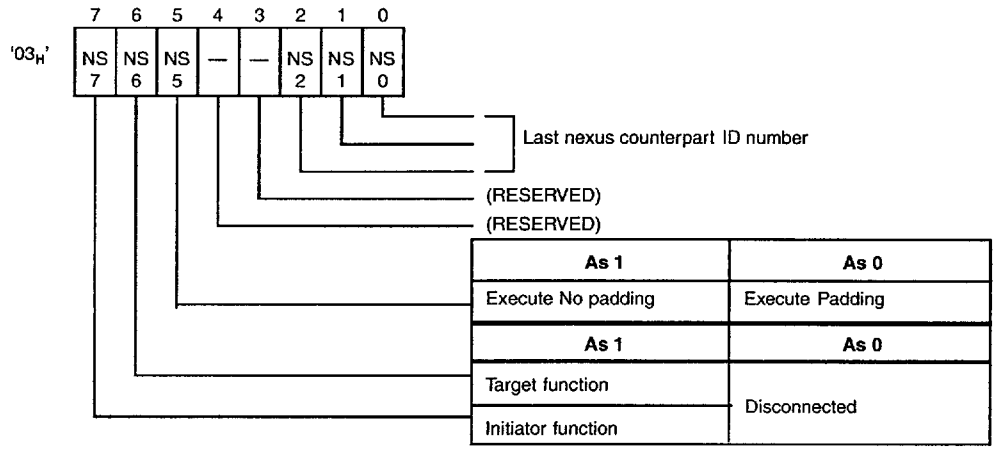
When the data register is EMPTY, 1 is indicated.

3.2.5 Nexus Status Register (READ)

The nexus status register (READ) shows the SPC internal state and the nexus counterpart ID.

■ Nexus Status Register (READ)

The nexus status register (READ) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7: Initiator function

When the SPC starts as the initiator, 1 is indicated. At the following points, 1 is indicated.

- Reselection by the target (SEL and I/O signals are true when the self ID bit is true).
- After acquiring bus usage rights as the initiator and asserting the SEL signal, when the ID bit is sent to the data bus during the selection phase or when the ATN signal is asserted simultaneously.

When the SPC is disconnected by the target and I-T nexus is released, 0 is indicated.

BIT 6: Target function

When the SPC starts as the target, 1 is indicated. At the following points, 1 is indicated.

- Selection by the initiator (SEL signal is true and I/O signal is false when the self ID bit is true).
- After acquiring bus usage rights as the target and asserting the SEL signal, when the ID bit is sent to the data bus during the reselection phase or when the I/O signal is asserted simultaneously.

When the SPC is disconnected and I-T nexus is released, 0 is indicated.

BIT 5: Padding operation

1 is indicated when the SPC receives a data transfer command with padding and then it did not perform the padding transfer after transferring the specified byte data. When the padding transfer is performed, 0 is indicated. This bit does not change if a data transfer command without padding is performed.

Also, please read out the value for this bit until the disconnect is occurred, since this bit is cleared when the device is newly nexused.

Furthermore, this bit can not be referred by the user program.

BIT 2-0: Final nexus counterpart ID

Stores nexus counterpart ID. BIT 2-0 are set at the following points.

- During the initiator function in the selection phase, when a BSY signal is received from the counterpart target.
- During the target function in the reselection phase, when a BSY signal is received from the counterpart initiator.
- During the intiator function, when a BSY signal is asserted in response to a target reselect request.
- During the target function, when a BSY signal is asserted in response to an initiator select request.

Data is stored in those bits even when the SPC is disconnected. This data is rewritten when a new nexus is established.

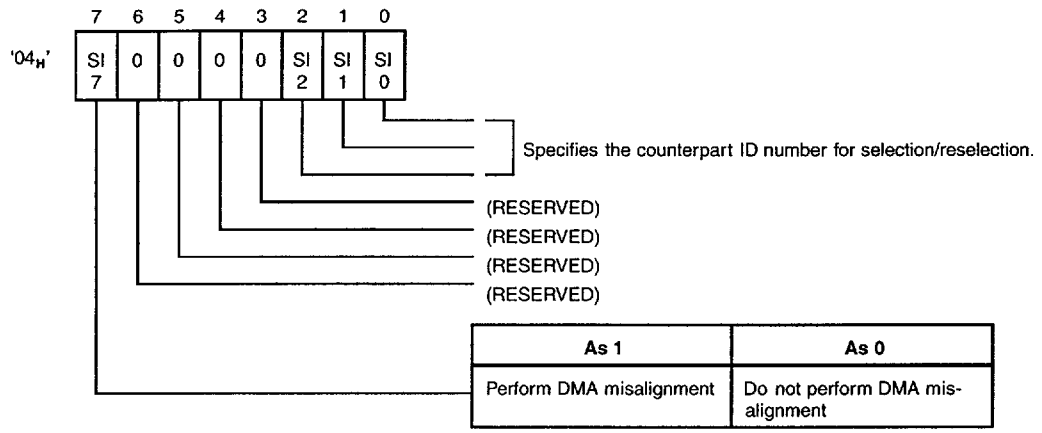
When the SPC is the target in the Automatic selection response mode, it operates automatically up to the command phase. At which time, the host MPU can reference this register to find out the initiator ID number. Also, when the SPC is the initiator in the Automatic reselection response mode, it operates automatically up to the message in phase. At which time, the host MPU can reference this register to find out the target ID number. (See 3.3.4 for more about the Automatic selection/reselection response mode).

3.2.6 SEL/RESEL ID Register (WRITE)

The SEL/RESEL ID register (WRITE) specifies DMA transfer misalignment processing and the selected counterpart bus device ID.

■ SEL/RESEL ID Register (WRITE)

The SEL/RESEL ID register (WRITE) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7: DMA transfer misalignment

Please set when the DMA transfer width is 16 bits, the first MPU/DMA side read/write is done by byte access, and writing to the system memory or reading from the system memory is performed to/from an odd address.

1:Writing to the system memory or reading from the system memory can be performed to/from an odd address.

0:Writing to the system memory or reading from the system memory can be performed to/from an even address.
See 6.2 for more details.

BIT 2-0: Setting SEL-RESEL ID
Specify the counterpart bus device ID number for selection/reselection with a binary digit.

■ Setting Transfer Mode/Transfer Parameters

When setting the transfer mode/transfer parameters (PERIOD, OFFSET), after specifying the counterpart ID number in the SEL/RESEL ID register, set the following.

- Transfer mode register (address $0C_H$)
- Transfer period register (address $0D_H$)
- Transfer offset register (address $0E_H$)

For a target in the selection phase to which only the target ID bit is sent (single initiator), set the transfer parameters with the initiator ID number as 0.

3.2.7 Interrupt Status Register (READ)

The interrupt status register (READ) displays the reason for the interrupt using an 8-bit code.

■ **Interrupt Status Register (READ)**

The interrupt status register (READ) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'04_H'	IS 7	IS 6	IS 5	IS 4	IS 3	IS 2	IS 1	IS 0

The interrupt status register, an FIFO-type register (8 bytes), stores interrupt codes which occur until the command is completed and can store two or more interrupt codes. Read this register when BIT 7 (interrupt request exists) of the SPC status register (address 02_H) is 1.

After each host MPU read operation, this register indicates the next interrupt code.

The interrupt status register value occurs at the step indicated by the command step register (address 05_H). Therefore, read this register and the command step register at the same time.

With an 8-bit MPU, read the command step register after reading the interrupt status register (unless this is done, the next interrupt code will not be shown).

See 5.7 for more on interrupt codes.

Notes on Reading Interrupt Status Register

1) If Bit 7 of automatic operation mode setting register (address 1Ch) is set to "1", all the interrupt code should be read out from this register. Otherwise, any commands issued later will be ignored.

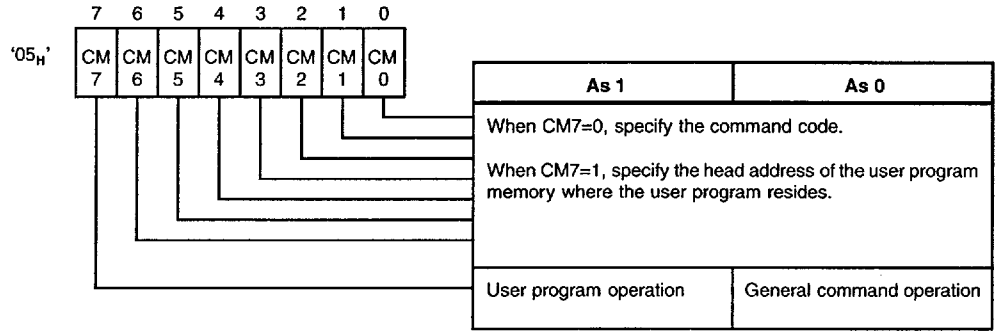
2) Do not access this register until SPC Busy bit (Bit 6 of SPC Status register) becomes "0" after the command was issued. Also, please read out the interrupt codes before issuing new command.

3.2.8 Command Register (WRITE)

The command register (WRITE) issues commands for the SPC.

■ **Command Register (WRITE)**

The command register (WRITE) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7: User program operation
This bit indicates whether the SPC operation will be conducted by the user program or by command. The meaning of BIT 6-0 changes depending on this bit setting.

0:Write the command code in BIT 6-0 (see chapter 4 for more on command codes).

1:Write the head address of the user program in BIT 6-0 (Figure 3.2.8). The SPC starts executing from the command at the address specified in the user program memory written in this bit. The head address of the user program can be specified in 2-byte units (only even address).

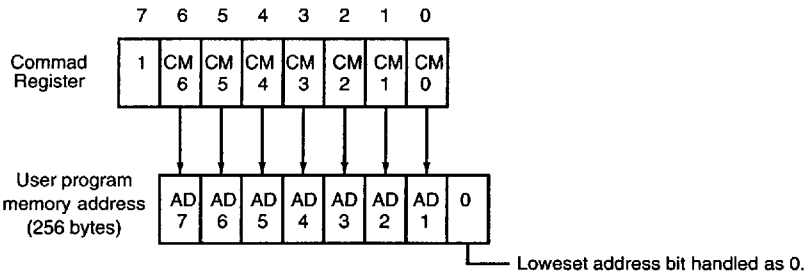


Figure 3.2.8 Relationship between Command Register (BIT 7 = 1) and User Program Memory

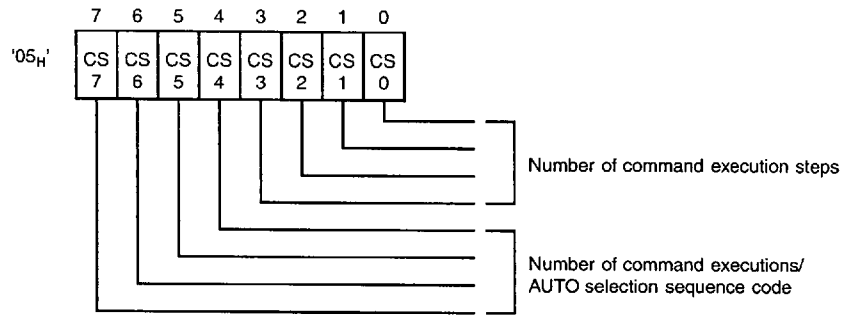
3.2.9 Command Step Register (READ)

The command step register (READ) indicates the number of command execution steps and program steps in the user program.

An FIFO-type register (8 bytes), it stores command steps corresponding to the interrupt status register.

■ **Command Step Register (READ)**

The command step register (READ) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7-4: Number of user program command executions/Automatic selection response mode sequence code

During user program operation: Ring counter which indicates the number of command executions. Advanced with each command execution start.
Only counts discrete commands. Special commands are not counted (see 4.1 for more on discrete commands and special commands).

During Automatic selection response mode (target only) operation: Indicates the type of response operation sequence (see 3.3.4 for more on the Automatic selection response mode).

BIT 3-0:Number of command execution steps

Indicates the number of command execution steps. Step codes are defined for each command (see chapter 4 for more on command steps). Same when set to the Automatic selection/reselection response mode. In the Automatic receive mode, information is received but this bit is not affected.

(Example) When an "Initial phase error & MSG-receive" interrupt occurs, the execution step at which the phase error occurred is indicated.

Notes on Reading Command Step Register

1) The contents of interrupt status register (address 04h) are the interrupt codes generated at the step indicated in this command step register. Therefore, it is necessary to read out this register along with the interrupt status register.

When 8-bit MPU is used, be sure always read out this step register after reading out the interrupt status register. If not, the next interrupt status will not be indicated. Also, if this register is read out before reading out the interrupt status register, the correct interrupt status will not be read out.

2) Please do not access this step register until Bit 6 (SPC Busy bit) of SPC Status register becomes "0" after issuing the command. If a new command is issued, please read out the existing step codes in advance.

3.2.10 Data Block Register (READ/WRITE)

The data block register (READ/WRITE) specifies the number of blocks for data phase transfers.

■ Data Block Register (READ/WRITE)

The data block register (READ/WRITE) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'06_H'	BL 15	BL 14	BL 13	BL 12	BL 11	BL 10	BL 9	BL 8
'07_H'	BL 7	BL 6	BL 5	BL 4	BL 3	BL 2	BL 1	BL 0

Specify the number of blocks to be transferred in the data phase in the data block register bits.

Fixed length: Specify the number of transfer blocks.

Variable length: Enter 0001_H.

This register's read values become valid after the completion report (including abnormal completions),
when the data block register and byte register are both 00 following a normal completion or when the number of untransferred blocks and bytes are reported following an abnormal completion.

(Example)

Set values: Blocks at $000A_H$ and byte length at 000100_H.

Normal: Blocks at 0000_H and byte length at 000000_H.

Abnormal 1: Blocks at 0004_H and byte length at $000AC_H$.

In this case, the untransferred data is four blocks and AC_H bytes. Meanwhile, the transferred data is five blocks and 54_H bytes.

Abnormal 2: Blocks at 0004_H and bytes at 0000_H.

In this case, the untransferred data is four blocks, and the transferred data is six blocks.

Abnormal 3: Blocks at 0005_H and byte length at 0100_H.

In this case, the untransferred data is six blocks (five blocks and 100_H bytes), and the transferred data is four blocks.

■ Data Block Register Access

The data block register becomes valid after the completion report (including abnormal completions). Prior to the completion report, initial values are indicated.

Please specify (set) this register when SPC Busy bit (Bit 6 of SPC status register) = "0".

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3.2.11 Data Byte/MC Byte Register (READ/WRITE)

The data byte/MC byte register (READ/WRITE) specifies the number of transfer bytes for data phase transfers and message phase/ command phase transfers.

■ **Data Byte/MC Byte Register (READ/WRITE)**

The data byte/MC byte register (READ/WRITE) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'08_H'	BY 23	BY 22	BY 21	BY 20	BY 19	BY 18	BY 17	BY 16
'09_H'	BY 15	BY 14	BY 13	BY 12	BY 11	BY 10	BY 9	BY 8
'$0A_H$'	BY 7	BY 6	BY 5	BY 4	BY 3	BY 2	BY 1	BY 0

- Data byte register (BY23-BY0)

  Specify the number of bytes for data phase transfers.

  Fixed length: Specify the length of a single block.
  Variable length: Specify the number of transfer bytes.

- MC byte register (BY7-BY0)

  Specify the number of bytes for message phase and command phase transfers.
  Only specify the number of transfer bytes in this register when the command being issued requires that the number of transfer bytes be set.

This register's read values become valid after the completion report (including abnormal completions),
when the data block register and byte register are both 00 following a normal completion or when the number of untransferred blocks and bytes are reported following an abnormal completion.

(Example)

Set values: Blocks at $000A_H$ and byte length at 000100_H.

Normal: Blocks at 0000_H and byte length at 000000_H.

Abnormal 1: Blocks at 0004_H and byte length at $000AC_H$.

In this case, the untransferred data is four blocks and AC_H bytes. Meanwhile, the transferred data is five blocks and 54_H bytes.

Abnormal 2: Blocks at 0004_H and byte at 0000_H.

In this case, the untransferred data is four blocks, and the transferred data is six blocks.

Abnormal 3: Blocks at 0005_H and byte length at 0100_H.

In this case, the untransferred data is six blocks (five blocks and 100_H bytes), and the transferred data is four blocks.

■ Data Byte/MC Byte Register Access

The data byte/MC byte register becomes valid after the completion report (including abnormal completions). Prior to the completion report, initial values are indicated.

However, when used as the MC byte register, initial values are always shown.

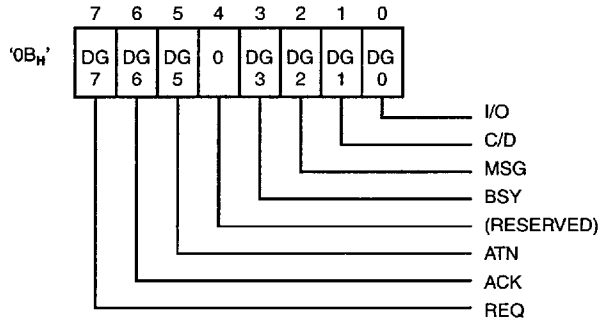
Please specify (set) this register when SPC Busy bit (Bit 6 of SPC status register) = "0".

3.2.12 DIAGNOSTIC Control Register (WRITE)

The DIAGNOSTIC control register (WRITE) emulates the SCSI signal sequence during the Diag mode.

■ DIAGNOSTIC Control Register (WRITE)

The DIAGNOSTIC control register (WRITE) bit configuration is shown below.



This register becomes valid from issuance of **INIT DIAG START** or **TARG DIAG START** command to the **DIAG END** command.

When 1 is written in the bits corresponding to the control signals, this signal is asserted.

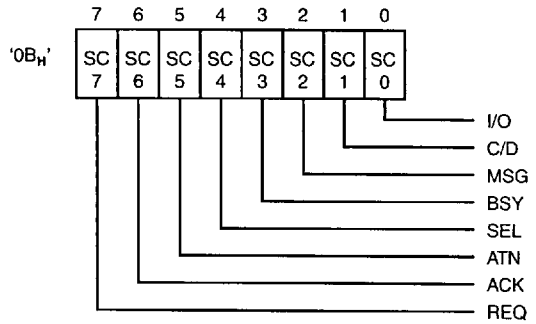
Note:Write "00_H" to this register prior to the issue of **INIT DIAG START** or **TARG DIAG START** command.

3.2.13 SCSI Control Signal Status Register (READ)

The SCSI control signal status register (READ) shows the state of the SCSI control signals.
Valid in Diag mode as well.

■ **SCSI Control Signal Status Register (READ)**

The SCSI control signal status register (READ) bit configuration is shown below.



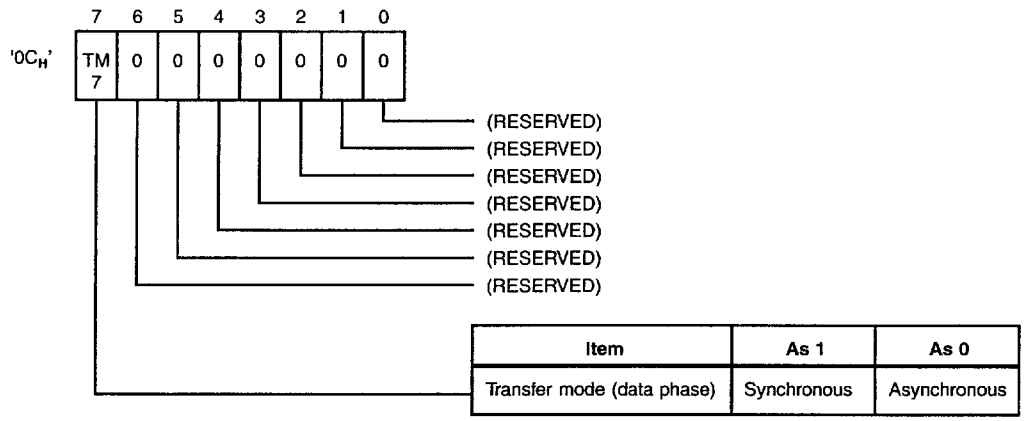
When the control signal corresponding to these bits is asserted, 1 is set.

3.2.14 Transfer Mode Register (WRITE/READ)

The transfer mode register (WRITE/READ) specifies the data phase transfer mode (synchronous transfer/asynchronous transfer).

■ Transfer Mode Register (WRITE/READ)

The transfer mode register (WRITE/READ) bit configuration is shown below.



Item	As 1	As 0
Transfer mode (data phase)	Synchronous	Asynchronous

Next, the functionality of each bit is described.

BIT 7: Transfer mode

Specifies the data phase transfer mode for the bus device ID listed in the SEL/RESEL ID register (address 04_H).

1: Data transfer in synchronous mode.
0: Data transfer in asynchronous mode.

■ Setting Transfer Mode Register

This register can store the transfer mode for each connected device. So, please set this register after the counterpart's ID to perform the data transfer is set to the SEL/RESEL ID register (address 04h). Once setting this register, the transfer mode will be automatically set to this register just only setting the SEL/RESEL ID register later, until a system reset or software reset is performed.

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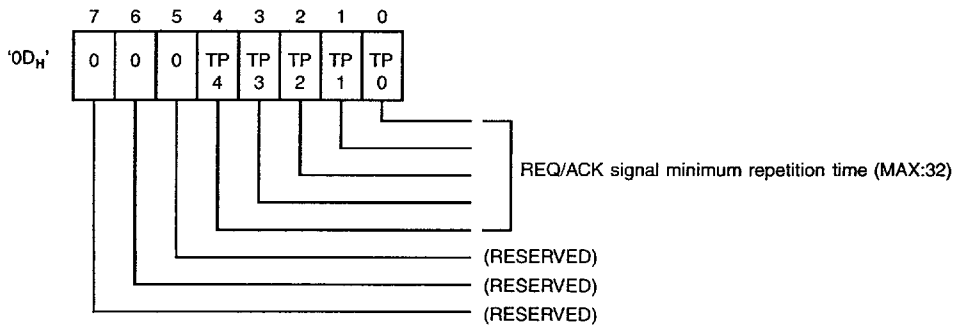
3.2.15 Transfer Period Register (READ/WRITE)

The transfer period register (READ/WRITE) specifies the synchronous transfer period for data phase transfers.

■ Transfer Period Register (READ/WRITE)

The transfer period register (READ/WRITE) bit configuration is shown below.



Set the synchronous transfer period for the bus device ID specified by the SEL/RESEL ID register (address 04_H). Note that higher transfer rate than the actual rate may be set if the input clock is high. (ex. 40 MHz: 04h or higher, 30 MHz: 03h or higher, 20 MHz: 02h or higher)

The following equation shows the relationship between the input block frequency and the maximum synchronous transfer speed.

(maximum synchronous transfer speed) × (transfer period) = input block frequency

(example) 10 Mbyte/s × 2 = 20 MHz

Table 3-5 shows the relationship between the transfer period register bit setting and the REQ/ACK signal minimum repetition time.

Table 3.2.15 Relationship between Transfer Period Register and REQ/ACK Signal Minimum Repetition Time

(unit: Tclf)

TP 4	TP 3	TP 2	TP 1	TP 0	TRANS PERIOD	ASSERT PERIOD	NEGATE PERIOD	TP 4	TP 3	TP 2	TP 1	TP 0	TRANS PERIOD	ASSERT PERIOD	NEGATE PERIOD
0	0	0	0	1	Prohibit	Prohibit	Prohibit	1	0	0	0	1	17	9	8
0	0	0	1	0	2	1	1	1	0	0	1	0	18	9	9
0	0	0	1	1	3	2	1	1	0	0	1	1	19	10	9
0	0	1	0	0	4	2	2	1	0	1	0	0	20	10	10
0	0	1	0	1	5	3	2	1	0	1	0	1	21	11	10
0	0	1	1	0	6	3	3	1	0	1	1	0	22	11	11
0	0	1	1	1	7	4	3	1	0	1	1	1	23	12	11
0	1	0	0	0	8	4	4	1	1	0	0	0	24	12	12
0	1	0	0	1	9	5	4	1	1	0	0	1	25	13	12
0	1	0	1	0	10	5	5	1	1	0	1	0	26	13	13
0	1	0	1	1	11	6	5	1	1	0	1	1	27	14	13
0	1	1	0	0	12	6	6	1	1	1	0	0	28	14	14
0	1	1	0	1	13	7	6	1	1	1	0	1	29	15	14
0	1	1	1	0	14	7	7	1	1	1	1	0	30	15	15
0	1	1	1	1	15	8	7	1	1	1	1	1	31	16	15
1	0	0	0	0	16	8	8	0	0	0	0	0	32	16	16

■ Setting Transfer Period Register

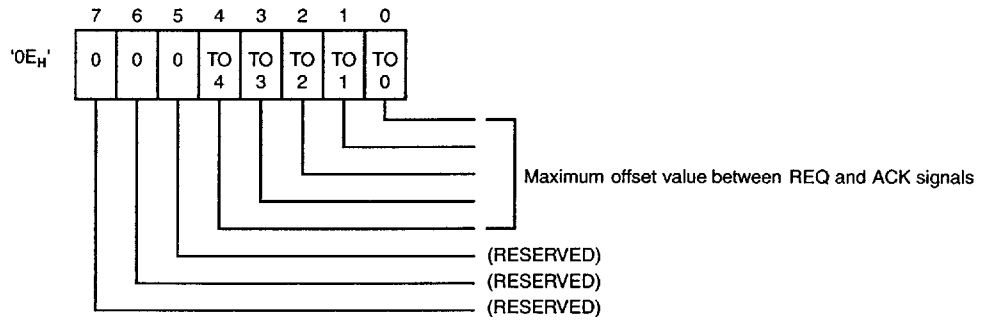
This register can store the transfer period for each connected devices. So, Please set this register after the counterpart's ID number is set to the SEL/RESEL ID register (address 04h). Once setting this register, the transfer period will be automatically set to this register from the next time or later, until a system reset or software reset is performed.

3.2.16 Transfer Offset Register (READ/WRITE)

The transfer offset registers specifies the maximum offset value for data phase synchronous transfers.

■ Transfer Offset Register (READ/WRITE)

The transfer offset register (READ/WRITE) bit configuration is shown below.



Set the synchronous transfer maximum offset value for the bus device ID specified by the SEL/RESEL ID register in the transfer offset register bits.

Table 3.2.16 shows the relationship between the transfer offset register bit setting and the maximum offset value for REQ and ACK signals.

Table 3.2.16 Relationship between Transfer Offset Register and Maximum Offset Value for REQ/ACK Signals

TO 4	TO 3	TO 2	TO 1	TO 0	TRANSFER-OFFSET
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
≈	≈	≈	≈	≈	≈
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31
0	0	0	0	0	32

3.2.17 Window Address Register (WRITE)

The window address register (WRITE) specifies address 10h to 1Fh windows.

Window types include initial setting register window, MCS buffer window, user program memory window, and SCAM register window. (SCAM register window is available in MB86604L only.)

■ **Window Address Register (WRITE)**

The window address register (WRITE) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'$0F_H$'	WA 7	WA 6	0	0	WA 3	WA 2	WA 1	WA 0

Next, the functionality of each bit is described.

BIT 7 to 6: Window selection

These bits select the window type for address 10_H to address $1F_H$.

WA 7	WA 6	Select window
0	0	MCS buffer window
0	1	SCAM register window
1	0	User program memory window
1	1	Initial setting window

Do not make SCAM register window setting in the MB86604A.

BIT 3 to 0: Window change

These bits change the window selection made by BIT 7 to 6. Set the first upper bit for the MCS buffer address and the four upper bits for the user program memory address.

Windows can be changed in 16 byte units.

Set "0" to BIT 3 to 0 to select the Initial Setting Window.

- MCS buffer window

WA 7	WA 6	0	0	WA 3	WA 2	WA 1	WA 0
0	0	0	0	0	0	0	X

First upper bit of MCS buffer address (32 bytes)

X: 0, 1 can be fixed

- User program window

WA 7	WA 6	0	0	WA 3	WA 2	WA 1	WA 0
1	0	0	0	X	X	X	X

Four upper bits of user program address (256 byte)

X: 0, 1 can be fixed

- SCAM register window

WA 7	WA 6	0	0	WA 3	WA 2	WA 1	WA 0
0	1	0	0	0	0	0	0

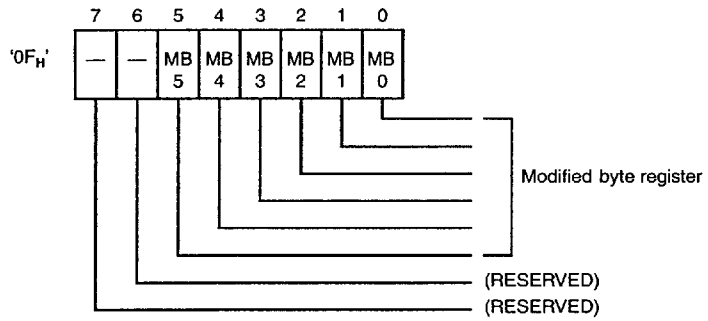
3.2.18 Modified Byte Register (READ)

The modified byte register (READ) is a 6-bit ring counter which indicates the number of bytes transferred by the SPC.

The meaning of this register's values changes by phase.

■ Modified Byte Register (READ)

The modified byte register (READ) bit configuration is shown below.



The meaning of modified byte register values changes by phase.

- In the message, command, status phases, it displays the number of bytes received by the SPC (Receive MCS buffer valid) or the number of bytes issued by the SPC (sent from the Send MCS buffer).
- In the data phase, it displays the number of bytes transferred between the SPC and the MPU or external memory.

The lower 6-bit values in the data byte register are set in the modified byte register and counted down for each single byte transfer.

When data transfer finishes with still remaining in the data register (abnormal completion), the number of remaining data bytes can be calculated from the data byte register and modified byte register values (see 5.9.4 for more on calculations). When the transfer ends with data still in the data register, the data in the data register becomes invalid.

Thus, in order to continue the data transfer, the bytes remaining in the data register must be calculated, the data pointer returned this amount, and the transfer operation started.

- In the Automatic selection response or Automatic receive modes, there are cases where receptions continues through various phases. The modified byte register displays the total number of bytes received during each phase.

3.2.19 BASIC Control Register Access

Indicates items to note during BASIC control register access.

■ **Interupt Status Register (READ), Command Step Register (READ)**

After the command is issued and until SPC BUSY (SPC status register: bit 6) becomes 0, do not access the interrupt status register (READ) and command step register (READ). Also, before a new command is issued, be sure to read interrupts and command steps for the previously executed command.

■ **Data block Register (READ/WRITE)**

Set data block register (READ/WRITE) right before issuing the command for data phase execution and when SPC BUSY (SPC status register: bit 6) is 0.

■ **Data Byte/MC Byte Registers (READ/WRITE)**

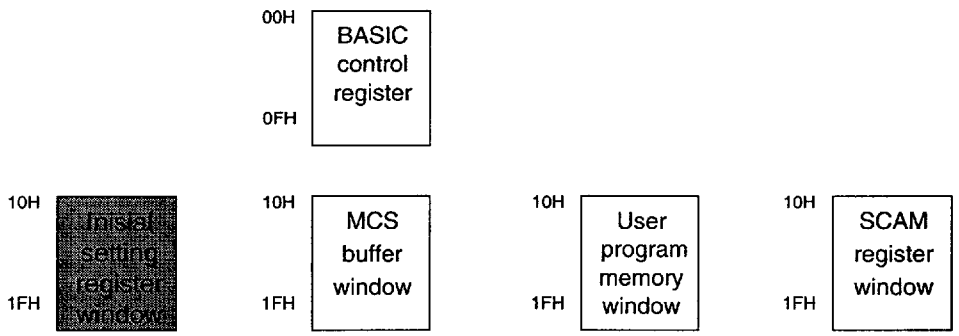
Set the data byte register (READ/WRITE) right before issuing the command for data phase execution and when SPC BUSY (SPC status register: bit 6) is 0.

Set the MC byte register (READ/WITE) right before issuing the commands which require that the MC byte register be set and when SPC BUSY (SPC status register: bit 6) is 0.

3.3 INITIAL SETTING REGISTER WINDOW

When the power is switched on, it is necessary to set initial register values because the internal registers are undefined.

After writing in the initial setting register windows, the SET UP REG command is issued to set initial values in SPC internal registers.



Note: SCAM register window is available in MB86604L only.

■ Initial Setting Register Window

Table 3-3 gives a list of registers in the initial setting register window.

Table 3.3 List of Initial Setting Register Window Registers

No.	Address					Write	Read
	A4	A3	A2	A1	A0		
10	1	0	0	0	0	Clock conversion setting register	←
11	1	0	0	0	1	Self ID setting register	←
12	1	0	0	1	0	Response mode setting register	←
13	1	0	0	1	1	SEL/RESEL mode setting register	←
14	1	0	1	0	0	SEL/RESEL retry setting register	←
15	1	0	1	0	1	SEL/RESEL timeout setting register	←
16	1	0	1	1	0	REQ/ACK timeout setting register	←
17	1	0	1	1	1	Asynchronous setup time setting register	←
18	1	1	0	0	0	Parity error detection setting registen	←
19	1	1	0	0	1	Interrupt enable setting register Group	←
1A	1	1	0	1	0	6/7 command length setting register	←
1B	1	1	0	1	1	DMA system setting register	←
1C	1	1	1	0	0	Auto-operation mode setting register	←
1D	1	1	1	0	1	SPC timeout setting register	←
1F	1	1	1	1	1	Revision indication register	←

■ Making Initial Setting Valid

The SET UP REG command must be issued to make the register values in the initial setting register window valid for the SPC.

These values do not become valid by host MPU write.
Issuing the SET UP REG command to the SPC sets up the internal circuits. When this is completed, a Command Complete interrupt is generated.
The clock conversion setting register (WRITE/READ) specifies the SPC input frequency. Set bit values according to the input frequency.

The initial setting register window registers contain undefined data after the reset release. Therefore, write in all registers.

When the SPC does not receive the command or is operating automatically (Automatic selection/reselection response mode), the SET UP REG command is ignored and a Command Reject interrupt generated. In this case, SPC operation is not altered.

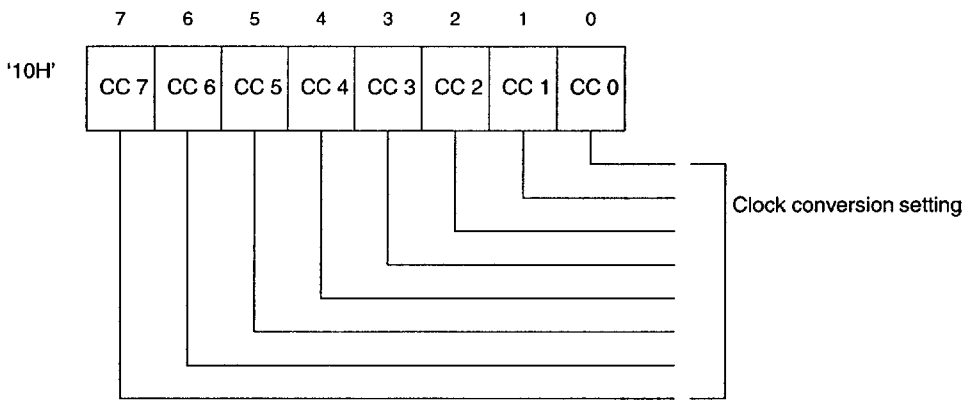
3.3.1 Clock Conversion Setting Register (WRITE/READ)

The clock conversion setting register (WRITE/READ) specifies the SPC input frequency.

SET bit values according to the input frequency.

■ **Clock Conversion Setting Register (WRITE/READ)**

The clock conversion setting register (WRITE/READ) bit configuration is shown below.



Set bit values according to the input frequency.

Table 3-8 shows the relationship between the clock conversion setting register bit setting and the input frequency.

Table 3.3.1 Relationship between Clock Conversion Setting Register Bit Setting and Input Frequency

HEX	CC 7	CC 6	CC 5	CC 4	CC 3	CC 2	CC 1	CC 0	Input Frequency [MHz]	Internal Operating Frequency [MHz]
0B	0	0	0	0	1	0	1	1	20.0	20.0
10	0	0	0	1	0	0	0	0	20.0	10.0
32	0	0	1	1	0	0	1	0	30.0	15.0
38	0	0	1	1	1	0	0	0	30.0	10.0
53	0	1	0	1	0	0	1	1	40.0	20.0
59	0	1	0	1	1	0	0	1	40.0	13.3

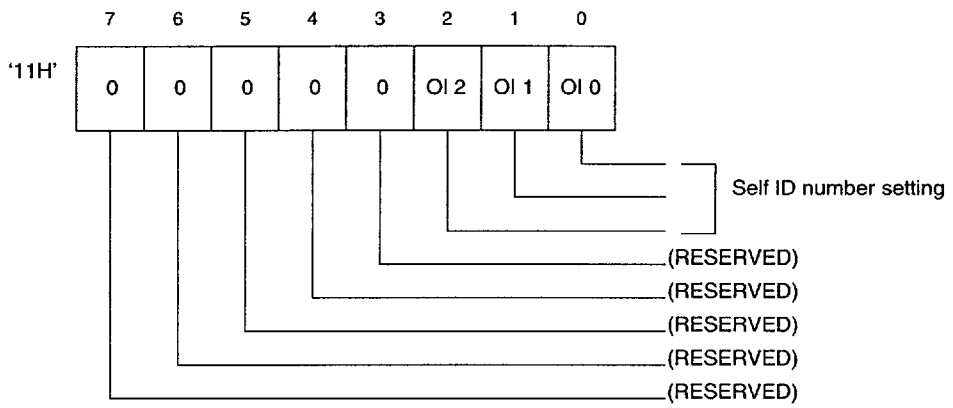
3.3.2 Self ID Setting Register (WRITE/READ)

The self ID setting register (WRITE/READ) specifies the SPC bus device ID number with a binary digit.

Use a binary digit for the SPC bus device ID number.

■ Self ID Setting Register (WRITE/READ)

Self ID setting register (WRITE/READ) bit configuration is shown below.

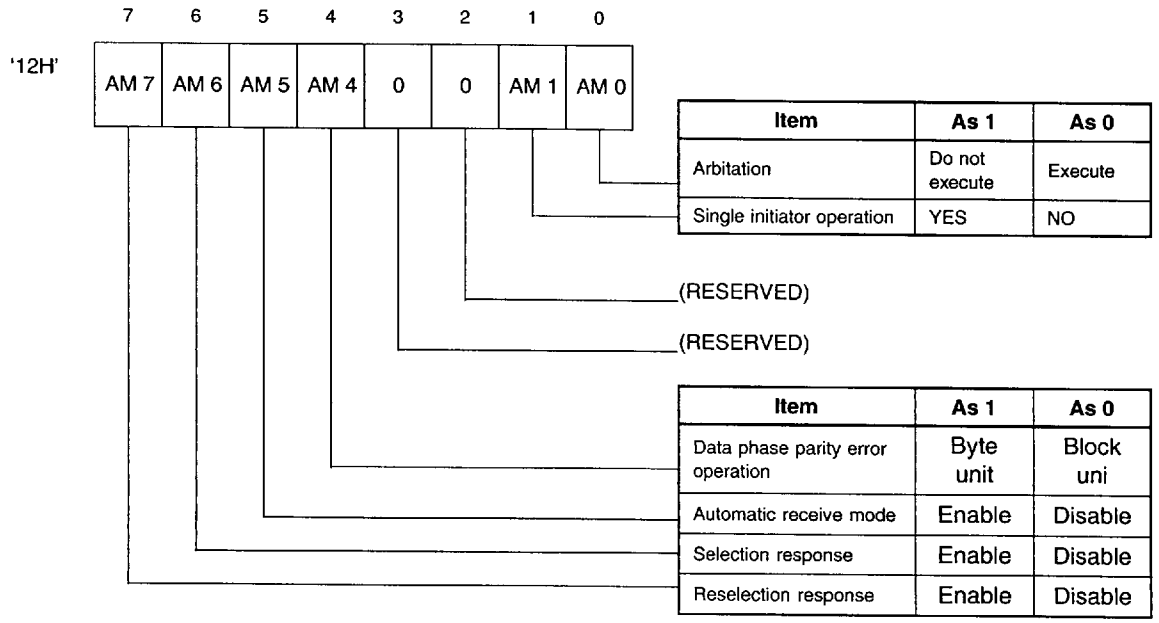


3.3.3 Response Mode Setting Register (READ/WRITE)

The Response mode setting register (READ/WRITE) specifies the SPC mode (see 3.3.3.1 to 3.3.3.6).

■ Response Mode Setting Register (READ/WRITE)

The response mode setting register (READ/WRITE) bit configuration is shown below.



Item	As 1	As 0
Arbitation	Do not execute	Execute
Single initiator operation	YES	NO

Item	As 1	As 0
Data phase parity error operation	Byte unit	Block uni
Automatic receive mode	Enable	Disable
Selection response	Enable	Disable
Reselection response	Enable	Disable

See 3.3.3.1 to 3.3.3.6 for more on bit functionality.

3.3.3.1 BIT 7 (Reselection Response)

BIT 7 (Reselection Response) specifies whether an initiator responds to target reselection.

■ **BIT 7 (Reselection Response)**

1: Respond to target reselect request and establish I-T nexus (see 3.3.4 for more on operation after establishing an I-T nexus).

0: No response to target reselect request (BSY signal not asserted in reselection phase).

3.3.3.2 BIT 6 (Selection Response)

BIT 6 (Selection Response) specifies whether a target responds to an initiator selection.

■ **BIT 6 (Selection Response)**

1: Respond to initiator select request and establish I-T nexus (see 3.3.4 for more on operation after establishing an I-T nexus).

0: No response to initiator select request (BSY signal not asserted in selection phase).

3.3.3.3 BIT 5 (Automatic Receive Mode)

BIT 5 (Automatic receive mode) specifies whether to receive messages in response to an attention condition produced by the initiator when functioning as the target. It also specifies whether to receive requested information (about the error phase) when functioning as the initiator and a phase error occurs during the execution of commands that involve phase transitions.

■ **BIT 5 (Automatic Receive Mode) Settings (Initiator Function)**

• When phase error occurs and target requests message in phase.

1: Phase error is recognized and a single message received.
When an ATN signal is being asserted, one message is received after it was negated.
With the final ACK signal still being asserted, an "Initial phase error & MSG-received" interrupt is reported.

0: Phase error is recognized and "Initial phase error" interrupt reported after negating ATN signal if it was being asserted.

• When phase error occurs and target requests status phase.

1: Phase error is recognized and a single status is received.
When an ATN signal is being asserted, one status is received after negation.
With the final ACK signal still being asserted, an "Initial phase error & status received" interrupt is reported. Whether or not the last ACK signal is negated depends on the ACK RESET mode setting. However, note that the command step reported at this time does not depend on the ACK RESET mode setting.(Regardless of the ACK RESET mode, the step numbers do not change.)

Regarding ACK RESET mode, refer to 3.3.13 Auto-Operation mode setting register.

Also, when an error occurs at the receipt of status, the error is reported. The command step numbers reported this case are the same as those in which a phase error occurs.

0: Phase error is recognized and "Initial phase error" interrupt reported.

The Automatic receive mode is invalid for phase errors that occur during a transfer (all bytes untransferred). When a phase error occurs during a transfer, a "phase error IN TRANSFER PROGRESS" interrupt is reported.

■ **BIT 5 (Automatic Receive Mode) Settings (Target Function)**

• When a command which ends in a phase other than the message out phase is executed and an ATN signal is asserted while the final ACK signal of the final phase is being asserted.

1: Attention condition produced by the initiator is detected, there is a transition to the message out phase, and a single message is received.
A "Command complete (ATN condition detected) & MSG received" interrupt is reported.

0: Attention condition produced by the initiator is detected, and a "Command complete (ATN condition detected)" interrupt is reported.
When an attention condition is detected during the execution of a command which ends with the message out phase, a "Command complete (ATN condition detected) interrupt is produced regardless of this bit setting.

• When a command is being executed as a target, and a transition to the next phase is taking place or an initiator attention condition is detected at the transfer data block boundary.

1: Attention condition produced by the initiator is detected, there is a transition to the message out phase, and as single message is received.

During data phase execution, the transfer is suspended at the transfer block boundary, there is a transition to the message out phase, and a single message is received.

A "Command stop (ATN condition detected) & MSG received" interrupt is reported.

0: Attention condition produced by the initiator is detected, and a "Command stop (ATN condition detected)" interrupt is reported.
During data in phase execution, the transfer is suspended at the transfer block boundary, and a "Command stop (ATN condition detected) interrupt is reported.

During data in phase execution, when a parity errors occurs on the target DMA or MPU side, the transfer is stopped between blocks (block unit stop), and an attention condition is produced by the initiator, "DMA parity error" or "MPU parity error" is reported without responding to the attention condition.

Note: When functioning as the target, after an attention condition is detected, there is a transition to the message out phase, and a single message is received. If another attention condition is detected after that, the following interrupt is reported.
Interrupt code = 61H
Sequence step = XXH (value after adding 1 to the number of steps of the phase prior to the transition to the message out phase)

■ **Storing Information Received by Automatic Operation**

• For Target operation:

If the command executed was not for command phase, the information is stored in Receive MCS buffer from address 0. If it was for command phase, the information is stored from the continuous address of CDB stored in Receive MCS buffer.

• For Initiator operation:

The information is stored in Receive MCS buffer from address 0.

3.3.3.4 BIT 4 (Operation for Data Phase Parity Error)

BIT 4 (Operation for Data Phase Parity Error) specifies SPC operation for when a data phase parity error is detected during SPC target operation.

■ **BIT 4 (Operation for Data Phase Parity Error)**

1: During data phase operation, the transfer is suspended when a parity error is detected, and an interrupt is reported (byte unit stop). See 5.9 for more information.

0: During data phase operation, the transfer is suspended after completing the transfer of the block where the parity error occurs, and an interrupt is reported (block unit stop).
However, when odd value is set in the data byte register, the parity error is detected in 2-block unit.

3.3.3.5 BIT 1 (Single Initiator Option)

BIT 1 (Single Initiator Option) specifies target operation.

When the SPC is incorporated in an application system operating in SCSI-1 mode and using the single initiator option, set this bit to 1.

■ **BIT 1 (Single Initiator Option)**

1: When the SPC is selected as the target, it responds even if the ID bit (target ID) on the data bus during the selection phase is just one bit. Bit 2 to 0 in the nexus status register indicate "000".

0: When the SPC is selected as the target, it does not respond if the ID bit on the data bus during the selection phase is 2 bits (for an initiator ID and the target ID).
When functioning as the initiator, do not set 1 at this bit, and self and target ID bits (2 bits) are always sent to the data bus during the selection phase regardless of this bit setting.

3.3.3.6 BIT 0 (Arbitration)

BIT 0 (Arbitration) specifies whether the SPC conducts arbitration.

When the SPC is incorporated in an application system operating in SCSI-1 mode and arbitration is not conducted, set this bit to 1.

■ **BIT 0 (Arbitration)**

1: Do not execute arbitration phase.

0: Execute arbitration phase.

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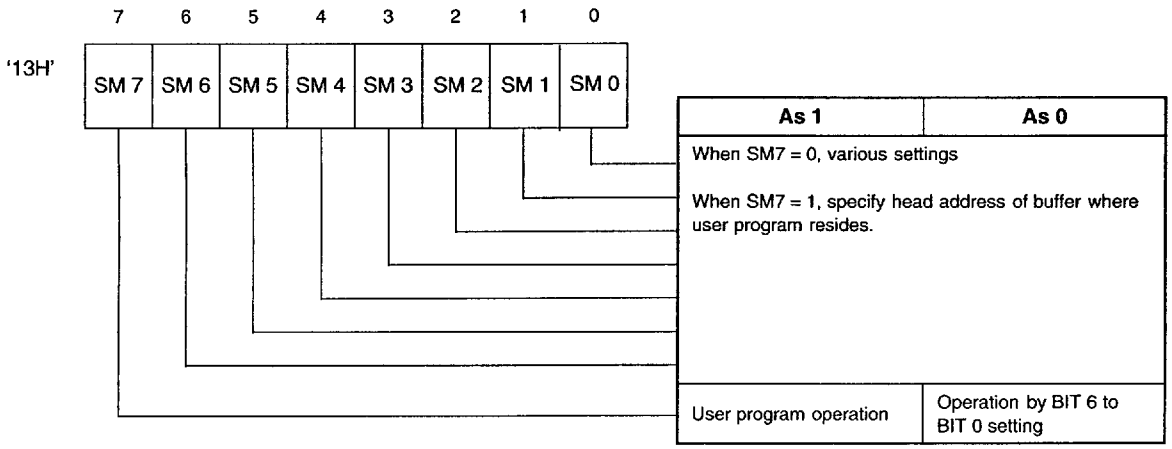
3.3.4 SEL/RESEL Mode Setting Register (WRITE/READ)

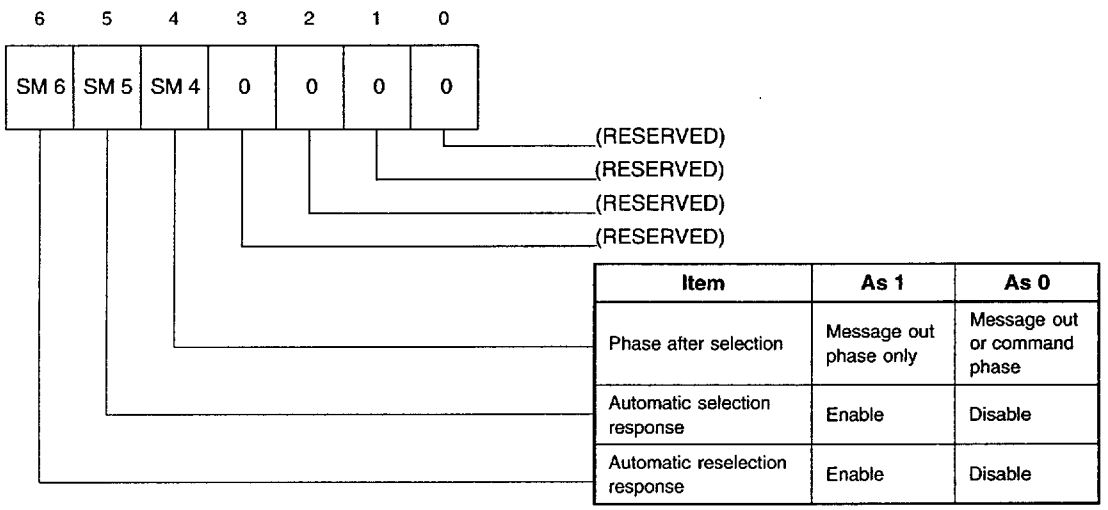
The SEL/RESEL mode setting register (WRITE/READ) specifies automatic response for selection or reselection.

■ SEL/RESEL Mode Setting Register (WRITE/READ)

The SEL/RESEL mode setting register (WRITE/READ) bit configuration is shown below.



(When SM7 = 0)



Item	As 1	As 0
Phase after selection	Message out phase only	Message out or command phase
Automatic selection response	Enable	Disable
Automatic reselection response	Enable	Disable

Next, the functionality of each bit is described.

BIT 7: User program operation

This bit specifies whether to make a response originating from select/reselect with functions set previously in the user program or SPC. The meaning of BIT 6 to 0 is altered by this bit setting.

1: The head address of user program memory is written in BIT 6 to 0.
When the SPC is selected or reselected, process execution begins from the command in the user memory address specified by BIT 6 to 0.
Set the user program memory address at the same time as the command register (see Figure 3.2.8).

0: Provide response already prepared for SPC.

BIT 6: Automatic reselection response

When BIT 7 is 0, this bit setting affects initiator operation for reselection.

1: Respond to reselect request and operate until a message is received (see 3.3.4.1).

0: Respond to reselect request and report a "RESELECTED" interrupt.

BIT 5: Automatic selection response

When BIT 7 is 0, this bit setting affects target operation for selection.

1: Respond to select request and operate until a message or command is received (see 3.3.4.2).

0: Respond to select request and report "SELECTED" or "SELECTED WITH ATN" interrupt.

BIT 4: Post-selection phase

When BIT 7 is 0, this bit specifies the target automatic response. Specifies whether to limit the post-selection phase to the message phase (SCSI-2 mode) or to allow either the message phase or the command phase.

1: Limited to message out phase and when the selection phase ATN signal is not asserted by the initiator, an "AUTO mode phase error" interrupt is reported.

0: Depending on the state of the selection phase ATN signal, either the message out phase or command phase is selected. (Refer to 3.3.3.3 Automatic Receive operation whether or not the message is received transitting to Message-out phase when the SPC detects ATN condition generated by an initiator after receiving a command in command phase.)

3.3.4.1 Initiator Automatic Reselection Response

Figure 3.4 is a flowchart of the initiator automatic reselection response when BIT 6 of the SEL/RESEL mode setting register is set to 1, and Table 3-9 shows the corresponding operation sequence (step code chart).

■ **Initiator Automatic Reselection Response**

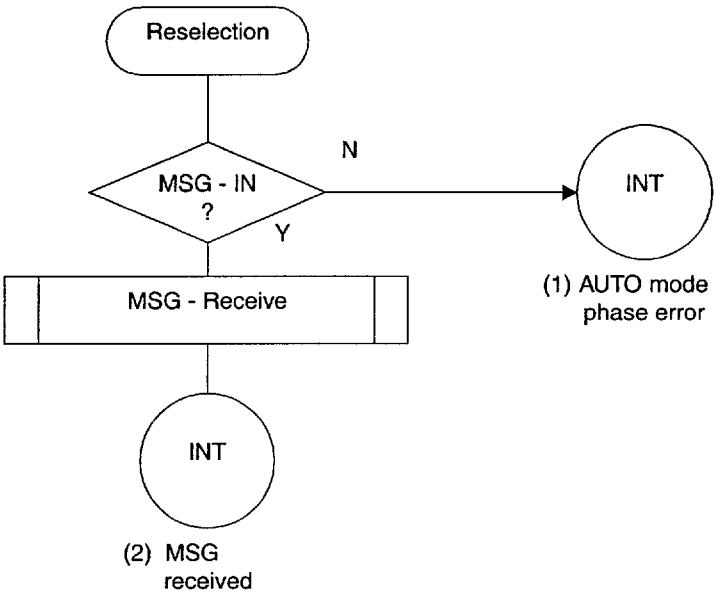


Figure 3.3.4.1 Initiator Automatic Reselection Response Flowchart

Table 3.3.4.1 Initiator Automatic Reselection Response Sequence (Step Code Chart)

Flow chart	Step	Description
Reselection	0	* Detect Reselect Establish nexus
MSG - IN	1	Wait for MSG-IN phase Execute MSG-IN phase
End	2	* Complete MSG receive

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3.3.4.2 Target Automatic Selection Response

Figure 3.5 is a flowchart of the target automatic selection response when BIT 5 of the SEL/RESEL mode setting register is set to 1, and Table 3-10 shows the corresponding operation sequence (step code chart).

■ **Target Automatic Selection Response**

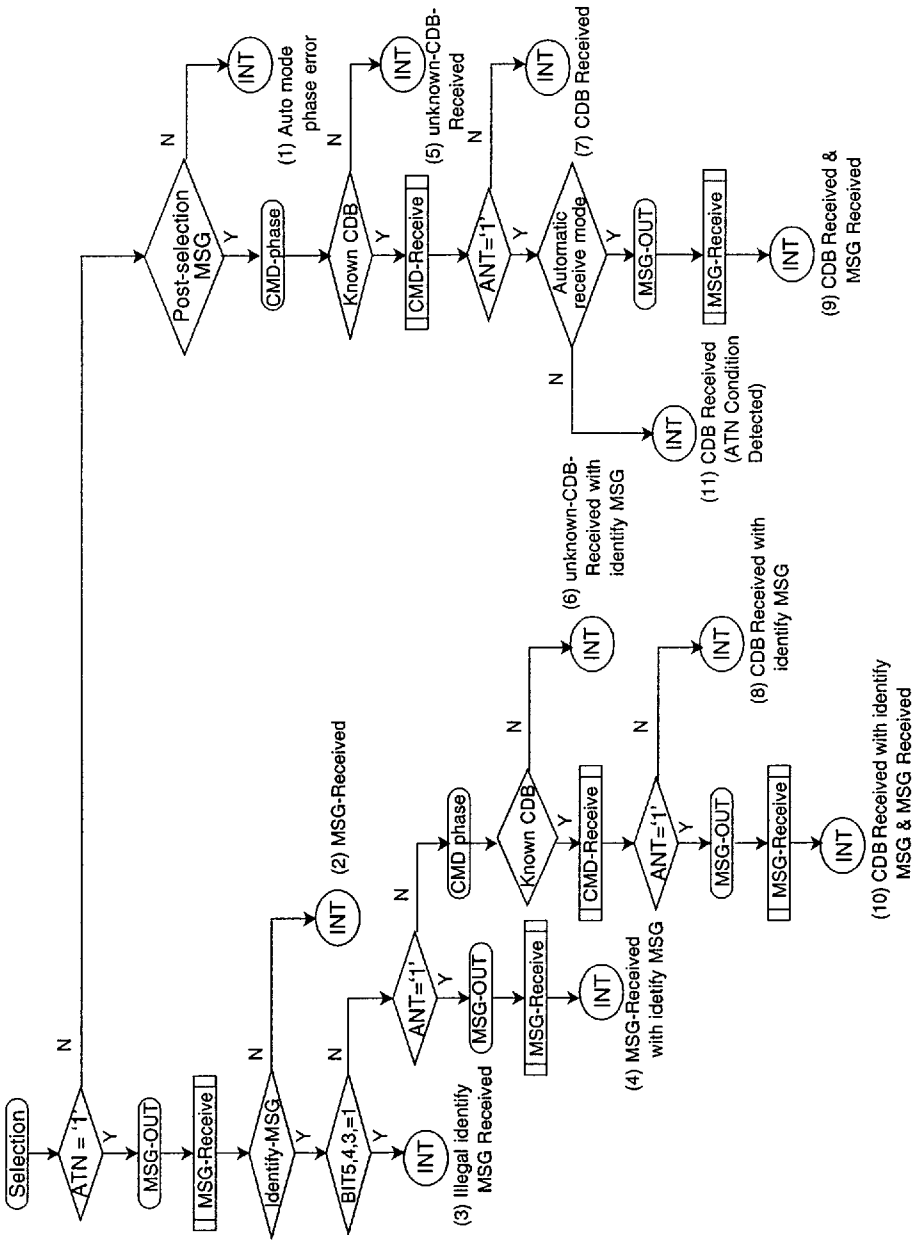
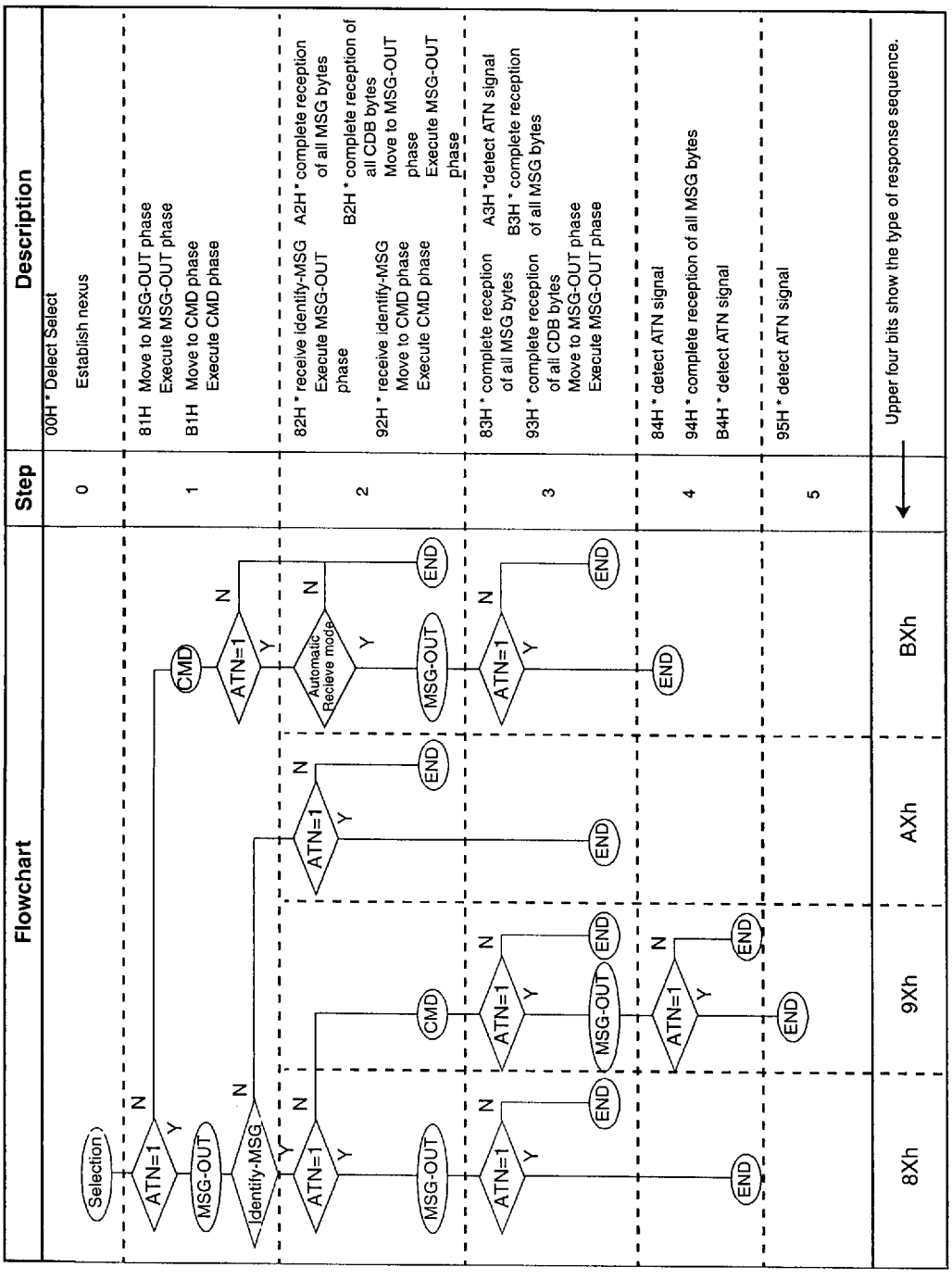


Figure 3.3.4.2a Target Automatic Selection Response Flowchart



Note: When the "identify-MSG" bits 5,4,3 are 1, an "illegal identify-MSG" interrupt is produced. At that time, the command status register code is the following.

- if the initiator is continuously asserting the ATN signal 82_H
- if the initiator is not continuously asserting the ATN signal 92_H

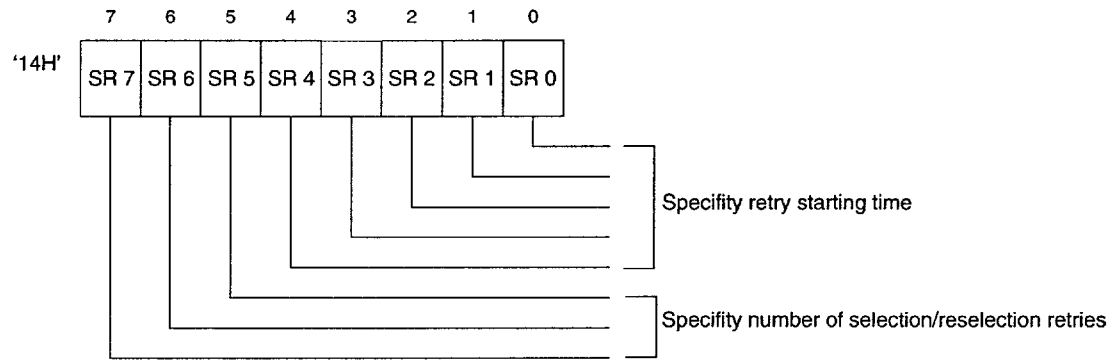
Table 3.3.4.2b Target Automatic Selection Response Sequence (Step Code Chart)

3.3.5 SEL/RESEL Retry Setting Register (READ/WRITE)

The SEL/RESEL retry setting register (READ/WRITE) specifies the number of selection/reselection retries and the retry starting time.

■ SEL/RESEL Retry Setting Register (READ/WRITE)

The SEL/RESEL retry setting register (READ/WRITE) bit configuration is shown below.



Next, the functionality of each bit is described.

BIT 7 to 5: Specifies number of selection/reselection retries

For commands which include selection/reselection, retry is performed the number of times specified by these bits even if selection/reselection timeout occurs. Specify the number of retries in accordance with Table 3-11.

Table 3.3.5 Relationship between SEL/RESEL Retry Setting Register and Number of Retries

SR 7	SR 6	SR 5	Number	SR 7	SR 6	SR 5	Number
1	1	1	Infinite	0	1	1	8
1	1	0	225	0	1	0	2
1	0	1	32	0	0	1	1
1	0	0	16	0	0	0	0

BIT 4 to 0 Specify retry starting time.

When selection/reselection timeout occurs during the initial selection/reselection, a retry is started after the passage of the time specified by this bit from a bus free state.

The time until a retry is determined by the following equation. However, when 00 is specified, there is not time count and retry is started once a bus free state exists.

$t_{CLF} \times C_{NV} \times [(SR^4 \times 2^{19}) + (SR3 \times 2^{17}) + (SR2 \times 2^{15}) + (SR1 \times 2^{13}) + (SR0 \times 2^{11})]$

t_{CLF}: Input frequency 1 cycle

C_{NV}: Calculate as

(value shown by clock conversion register BIT 4, BIT 3)

SR4 to SR0: BIT 4 to 0 setting values

(Example)

When the input frequency is 30 MHz and internal operating clock is 10 MHz:
$t = 33.33$ ns and $C_{NV} = 3$ so

$33.33 \times 3 \times [(SR4 \times 2^{19}) + (SR3 \times 2^{17}) + (SR2 \times 2^{15}) + (SR1 \times 2^{13}) + (SR0 \times 2^{11})]$

Thus, the time range which can be set in this register is as follows.

Maximum (SR4 to SR0 = 1) : 69 msec

Minimum (SR4 to SR1 = 0, SR0 = 1): 204 µsec

3.3.6 SEL/RESEL Timeout Setting Register (WRITE/READ)

The SEL/RESEL timeout setting register (WRITE/READ) specifies the selection/ reselection timeout delay time.

■ SEL/RESEL Timeout Setting Register (WRITE/READ)

The SEL/RESEL timeout setting register (WRITE/READ) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'15H'	ST 7	ST 6	ST 5	ST 4	ST 3	ST 2	ST 1	ST 0

Specify the selection/reselection timeout time in this register.

The timeout time is determined by the following equation. However, when set to 00_H, timeout detection is not performed.

$t_{CLF} \times C_{NV} \times [(ST7 \times 2^{25}) + (ST6 \times 2^{23}) + (ST5 \times 2^{21}) + (ST4 \times 2^{19}) + (ST3 \times 2^{17}) + (ST2 \times 2^{15}) + (ST1 \times 2^{13}) + (ST0 \times 2^{11})]$

t_{CLF}: Input frequency 1 cycle

C_{NV}: Calculate as

(value shown by clock conversion register BIT 4, BIT 3)

ST7 to ST0: BIT 7 to 0 setting values

(Example)

When the input frequency is 30 MHz and internal operating clock is 10 MHz:
t_{CLF} = 33.33 ns and C_{NV} = 3 so

$33.33 \times 3 \times (ST7 \times 2^{25}) + (ST6 \times 2^{23}) + (ST5 \times 2^{21}) + (ST4 \times 2^{19}) + (ST3 \times 2^{17}) + (ST2 \times 2^{15}) + (ST1 \times 2^{13}) + (ST0 \times 2^{11})$

Thus, the time range which can be set in this register is as follows.

Maximum (SR7 to SR0 = 1): 4.4 sec
Minimum (ST7 to ST1 = 0, ST0 = 1): 204 µsec

Note: When 00H is set in this register, the timeout time is determined by the following equation.

$t_{CLF} \times C_{NV} \times 2^{27}$

(Example)

When the input frequency is 30 MHz and internal operating clock is 10 MHz:
t_{CLF} 33.33 ns and C_{NV} = 3 so, $33.33 \times 3 \times 2^{27} \fallingdotseq 13.4$ sec

3.3.7 REQ/ACK Timeout Setting Register (WRITE/READ)

The REQ/ACK timeout setting register (WRITE/READ) specifies the REQ/ACK signal timeout time.

■ REQ/ACK Timeout Setting Register (WRITE/READ)

The REQ/ACK timeout setting register (WRITE/READ) bit configuration is shown below.

	7	6	5	4	3	2	1	0
'16H'	RT 7	RT 6	RT 5	RT 4	RT 3	RT 2	RT 1	RT 0

The specified REQ/ACK signal timeout times are explained below.

For asynchronous transfers (target): Time after the REQ signal is asserted and until the initiator asserts the ACK signal.

For asynchronous transfers (initiator): Time after the ACK signal is asserted and until the target asserts the REQ signal.

For synchronous transfers (target only): Time after the REQ signal is asserted until an ACK signal which makes the offset value 0 is received.

The timeout time is determined by the following equation. However, timeout detection is not performed when set at 00_H.

$t_{CLF} \times C_{NV} \times (RT7 \times 2^{28}) + (RT6 \times 2^{26}) + (RT5 \times 2^{24}) + (RT4 \times 2^{22}) + (RT3 \times 2^{20})$
$+ (RT2 \times 2^{18}) + (RT1 \times 2^{16}) + (RT0 \times 2^{14})$

t_{CLF}: Input frequency 1 cycle
C_{NV}: Calculate as

(value shown by clock conversion register BIT 4, BIT 3), when the clock conversion value is $0X_H$

RT7 to RT0: BIT 7 to 0 setting values

(Example)

When the input frequency is 30 MHz and internal operating clock is 10 MHz:
$t_{CLF} = 33.33$ ns and $C_{NV} = 3$ so

$33.33 \times 3 \times (RT7 \times 2^{28}) + (RT6 \times 2^{26}) + (RT5 \times 2^{24}) + (RT4 \times 2^{22}) + (RT3 \times 2^{20})$
$+ (RT2 \times 2^{18}) + (RT1 \times 2^{16}) + (RT0 \times 2^{14})$

Thus, the time range which can be set in this register is as follows.

Maximum (when RT7 to RT0 = 1): 35.8 sec

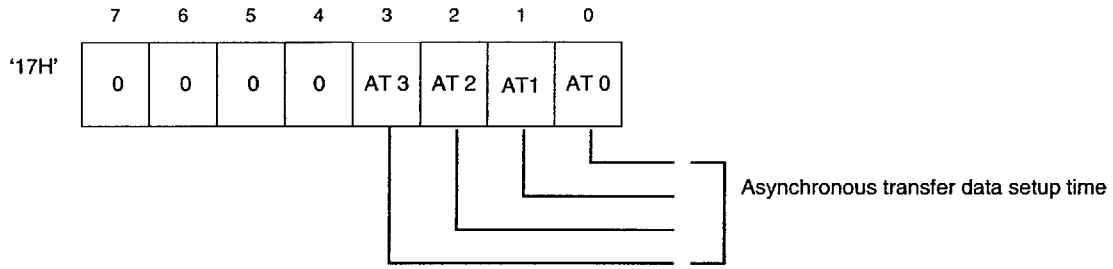
Minimum (when RT7 to RT1 = 0, RT0 = 1): 1.6 msec

3.3.8 Asynchronous Setup Time Setting Register (WRITE/READ)

The asynchronous setup time setting register (WRITE/READ) specifies the timing of asserting REQ/ACK signals for asynchronous data transfers.

■ Asynchronous Setup Time Setting Register (WRITE/READ)

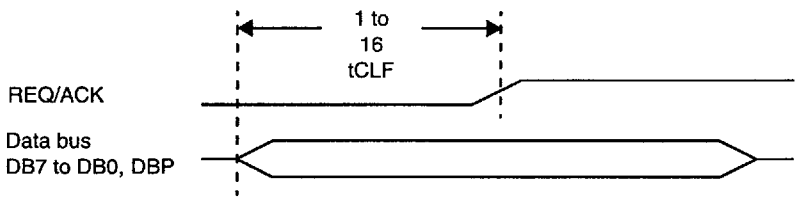
The asynchronous setup time setting register (WRITE/READ) bit configuration is shown below.



The specified data setup times are explained below.

Target: Time from placing the data in the data bus until the REQ signal is asserted.

Initiator: Time from placing the data in the data bus until the ACK signal is asserted.



AT 3	AT 2	AT 1	AT 0	SET UP TI ME
0	0	0	1	1tclf
0	0	1	0	2tclf
0	0	1	1	3tclf
≈				≈
1	1	1	1	15tclf
0	0	0	0	16tclf

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3.3.9 Parity Error Detect Setting Register (WRITE/READ)

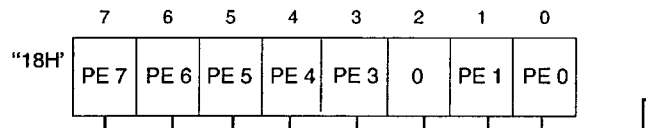
The parity error detect setting register (WRITE/READ) specifies the parity type, generation, and check in accordance with the MPU, DMA configuration.

Parity checks cannot be performed until this register is set up (using the SET UP REG command).

Parity generation enable/disable is only valid for the data phase.

■ Parity Error Detect Setting Register (WRITE/READ)

The parity error detect setting register (WRITE/READ) bit configuration is shown below.



Item	As 1	As 0
DMA parity generate	Yes	No
DMA parity check	Yes	No
(Reserve)		
MPU parity generate	Yes	No
MPU parity check	Yes	No
System side parity type	Odd	Even
SCSI parity generate	Yes	No
SCSI parity check	Yes	No

Next, the functionality of each bit is described.

BIT 7: SCSI parity check

1: Functioning as the initiator , a parity check is performed for message in phase, status phase, and data in phase input data and data out phase output data.

Functioning as the target, a parity check is performed for message output phase, command phase, and data out phase input data and data in phase output data.

0: Parity check is not performed.

BIT 6: SCSI parity generate

1: Functioning as the initiator, parity generate is performed for data in phase input data and data out phase output data.

Functioning as the target, parity generate is performed for data out phase input data and data in phase output data.

0: Parity is not generated.

BIT 5: System side parity type

This bit specifies the MPU/DMA parity type for application systems incorporating the SPC.

1: Odd parity

0: Even parity

BIT 4: MPU parity check

1: During register write, data parity check is performed as data is written to the SPC registers (check is not performed for register read operations).

During data register read/write, a parity check is performed for data written in data registers while the data phase is being executed for program transfer and data read from the data registers.

0: Parity check is not performed.

BIT 3: MPU parity generate

1: Parity is generated for data written in the data register while the data phase is being executed for program transfer and data read from the data registers.

0: Parity is not generated.

During register write, parity is not generated regardless of this bit setting. Also, during register read, parity is generated without any conditions (do not perform MPU parity checks for systems without a parity bit for the MPU data bus).

BIT 1: DMA parity check.

1: When the data phase is being executed for DMA transfers, a parity check is performed for data input from the DMA data bus and data output to the DMA data bus.

0: Parity check is not performed.

BIT 0: DMA parity generate

1: When the data phase is being executed for DMA transfers, parity is generated for data input from the DMA data bus and data output to the DMA data bus.

0: Parity is not generated.

See appendix B for more on how parity check and parity generate are performed within the SPC circuits.

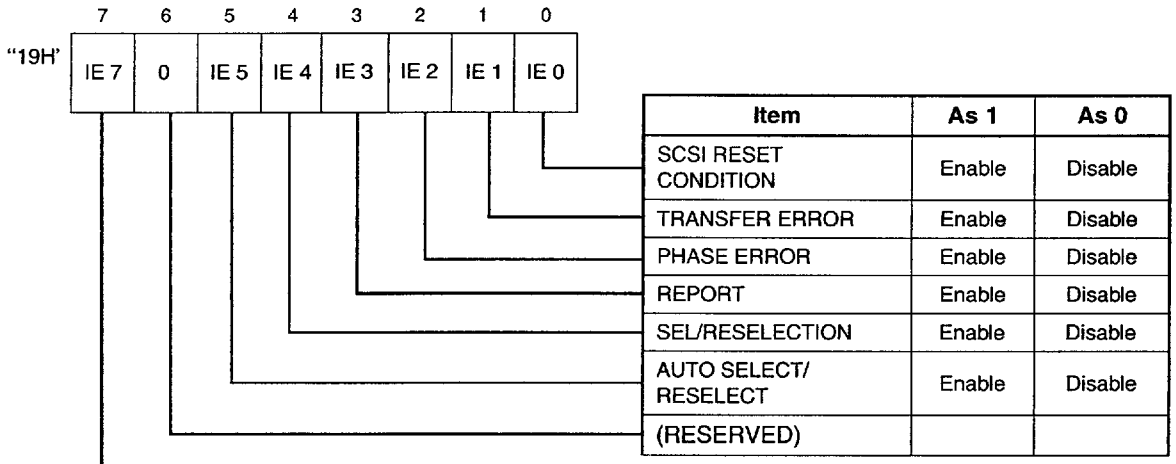
Note: During the external bus access, the parity check and generate are not performed regardless of the register setting. Also, when performing the SCSI bus parity check in an application which does not have the parity bit on the MPU and DMA buses, please make "MPU and DMA parity generations" Enable. Furthermore, please make "Pull-up" for UDP, LDP, UDMDP, and LDMDP pins with approx. 10 kΩ resistor.

3.3.10 Interrupt Enable Setting Register (WRITE/READ)

The interrupt enable setting register (WRITE/READ) masks interrupt signals (INT) by interrupt cause groups.

■ Interrupt Enable Setting Register (WRITE/READ)

The interrupt enable setting register (WRITE/READ) bit configuration is shown below.



Item	As 1	As 0
SCSI RESET CONDITION	Enable	Disable
TRANSFER ERROR	Enable	Disable
PHASE ERROR	Enable	Disable
REPORT	Enable	Disable
SEL/RESELECTION	Enable	Disable
AUTO SELECT/ RESELECT	Enable	Disable
(RESERVED)		

Next, the functionality of each bit is described.

BIT 7: All interrupt causes

1: Depends on BIT 5 to 0 Setting

0: Disable for all interrupt causes regardless of the BIT 5 to 0 setting.

The upper three bit values of the interrupt code shown in the interrupt status register (address 04_H) correspond to bit values of this register (Table 3.3.10).

See 5.7 for more on interrupt codes. Also, SPC reports interrupts to it's interrupt status register (04_H) regardless of this register setting.

Table 3.3.10 Relationship between Interrupt Enable Setting Register and Interrupt Codes

IE BIT	Interrupt code			Interrput code type
	IS7	IS6	IS5	
0	0	0	0	SCSI reset
1	0	0	1	Interrupt related to transfers
2	0	1	0	Interrupt related to phase transitions
3	0	1	1	Interrupt related to reports
4	1	0	0	Interrupt related to selection/reselection
5	1	0	1	Interrupt related to automatic selection/reselection

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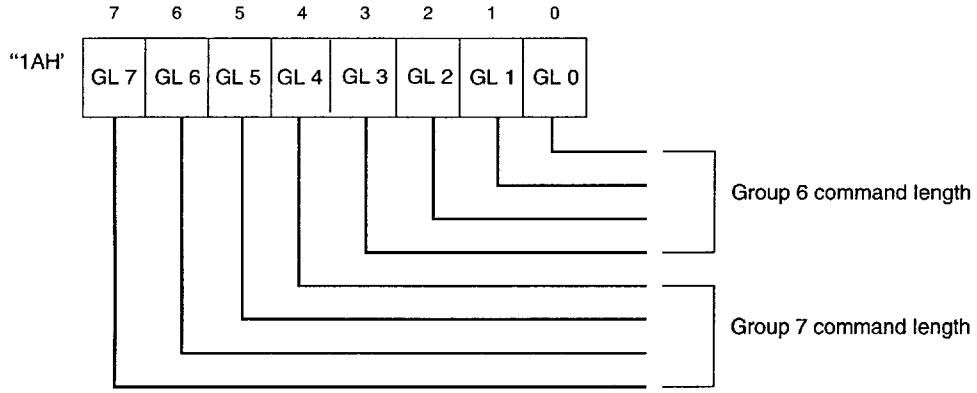
3.3.11 Group 6/7 Command Length Setting Register (WRITE/READ)

The group 6/7 command length setting register (WRITE/READ) specifies the group 6/7 command length.

■ Group 6/7 Command Length Setting Register (WRITE/READ)

The group 6/7 command length setting register (WRITE/READ) bit configuration is shown below.



Set the values shown in Table 3-13 and Table 3-14 in the register bits in accordance with the group 6/7 command length

.

Table 3.3.11 List of Bit Setting for Group 6/7 Command Length Setting Register (Group 6)

GL 3	GL 2	GL 1	GL 0	Group 6 command length
0	0	0	0	Not specified
0	0	0	1	2 byte
0	0	1	0	4 byte
0	0	1	1	6 byte
≈				≈
1	1	1	0	28 byte
1	1	1	1	30 byte

Table 3.3.12 List of Bit Setting for Group 6/7 Command Length Setting Register (Group 7)

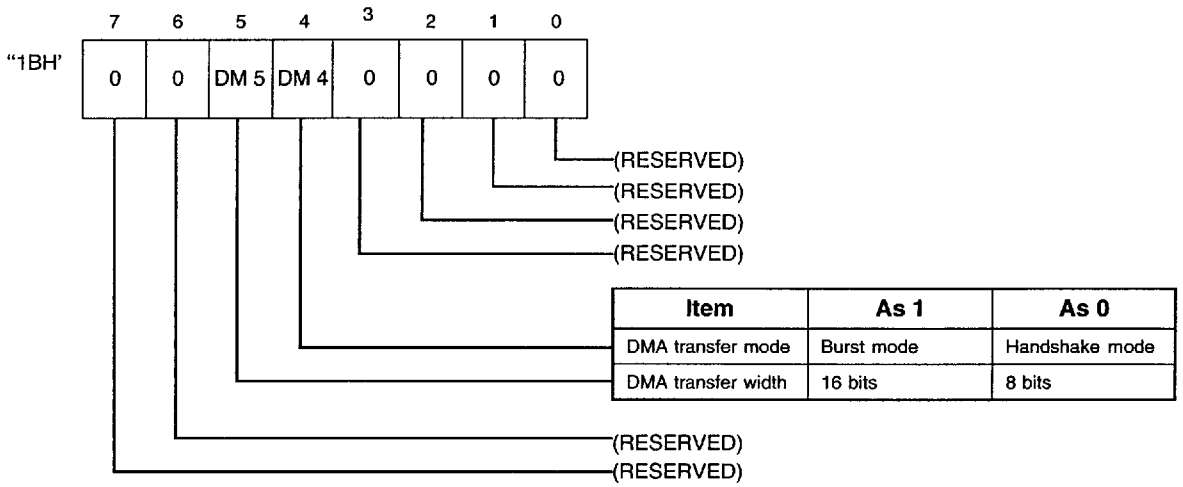
GL 7	GL 6	GL 5	GL 4	Group 7 command length
0	0	0	0	Not specified
0	0	0	1	2 byte
0	0	1	0	4 byte
0	0	1	1	6 byte
≈				≈
1	1	1	0	28 byte
1	1	1	1	30 byte

3.3.13 DMA System Setting Register (WRITE/READ)

The DMA system setting register (WRITE/READ) specifies the DMA transfer mode.

■ **DMA System Setting Register (WRITE/READ)**

The DMA system setting register (WRITE/READ) bit configuration is shown below.



Item	As 1	As 0
DMA transfer mode	Burst mode	Handshake mode
DMA transfer width	16 bits	8 bits

Next, the functionality of each bit is described.

BIT 5: Set DMA transfer width

This bit specifies the DMA transfer width.

1: 16 bits

0: 8 bits

BIT 4: DMA transfer mode

This bit specifies the DMA transfer mode.

1: Burst transfer mode
While DMA transfer is possible, DREQ signal output is kept in an active state.

0: Handshake mode
Transfer is performed by DREQ signal output and DACK signal input.

Handshake: One format for reading and writing data between devices. In this case, the following transfers are performed between the SPC and DMAC.

(1) When data is transferred from the SPC to the DMAC

1. SPC sets up the data to be sent.
2. SPC asserts the DREQ signal.
3. When the DMAC detects that the DREQ signal has been asserted, it receives the data and asserts the $\overline{\text{DACK}}$ signal.
4. When the SPC detects that the $\overline{\text{DACK}}$ signal has been asserted, it negates the DREQ signal.

(2) When data is transferred from the DMAC to the SPC

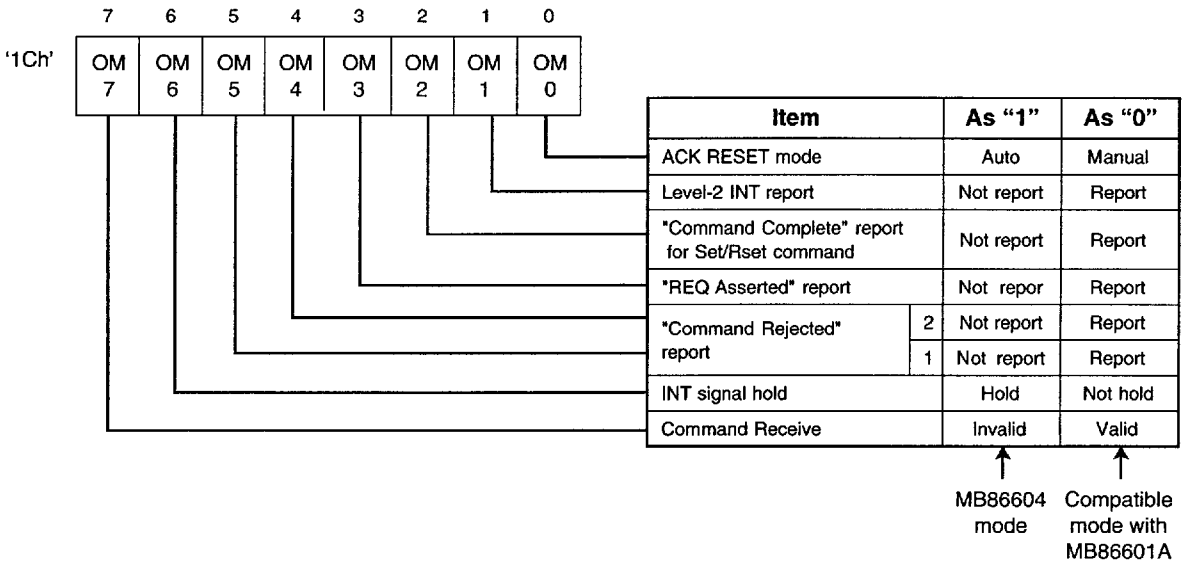
1. SPC asserts the DREQ signal.
2. After the DMAC detects that the DREQ signal has been asserted, the transfer data is sent to the bus.
3. DMAC asserts the $\overline{\text{DACK}}$ signal.
4. When the SPC detects that the $\overline{\text{DACK}}$ signal has been asserted, the DREQ signal is negated.

The next time that data is detected, the steps 1. to 4. are repeated. However, until the $\overline{\text{DACK}}$ signal is negated, the next DREQ signal cannot be asserted.

3.3.14 Automatic Operation Mode Setting Register (WRITE/READ)

This register sets the SPC various operation modes.

■ **Automatic Operation Mode Setting Register (WRITE/READ)**



Item		As "1"	As "0"
ACK RESET mode		Auto	Manual
Level-2 INT report		Not report	Report
"Command Complete" report for Set/Rset command		Not report	Report
"REQ Asserted" report		Not repor	Report
"Command Rejected" report	2	Not report	Report
	1	Not report	Report
INT signal hold		Hold	Not hold
Command Receive		Invalid	Valid

Each bit function is described in the next section.

Bit 7: Command Receive Invalid Mode

This bit specifies whether or not SPC accepts the command received if the interrupt factor (cause) is held in the Interrupt Status Register (address 04_H).

When "1": SPC ignores the command received and does not report the "Command Rejected" interrupt. Once all the interrupt factor is read out from the interrupt status register, it accepts the command.

When "0": SPC accepts and executes the command received.

Bit 6: INT Signal Hold Mode

This bit specifies whether or not the SPC holds the INT signal until all the interrupt factor and step code is read out.

When "1": SPC holds the INT signal until all the interrupt and step code held in the SPC is read out.

When "0": SPC makes the INT signal "Inactive" once an interrupt code is read out, even if SPC is holding multiple interrupt and step codes. Also, SPC makes the INT signal "Inactive" at which SPC BSY bit (Bit 6 of SPC Status Register) becomes "1" even if any interrupt code is read out.

Bit 5: Command Rejected Report Mode -1

This bit specifies whether or not the SPC reports the "Command Rejected" interrupt when the command is received during SPC BUSY state (SPC BSY=1).

When "1": For example, while SPC is responding to the Selection/Reselection; if a command which selects/reselects is issued, SPC reports only the interrupt for the selection/reselection. However, when the selection/reselection command is issued after reading out the interrupt factor for the selection/reselection response, SPC reports the "Command Invalid" interrupt.

When "0": SPC reports the "Command Rejected" interrupt after reporting the interrupt for the command currently in-process or selection/reselection response.

Bit 4: Command Rejected Report Mode -2

This bit specifies whether or not the SPC reports the "Command Rejected" interrupt when SPC responded to the selection/reselection from other device while SPC is executing a selection/reselection command or waiting for it.

When "1": SPC reports only the interrupt for selection/reselection and does not report the "Command Rejected" interrupt.

When "0": SPC reports the interrupt for selection/reselection after reporting the "Command Rejected" interrupt.

Bit 3: REQ Asserted Report Mode

This bit specifies whether or not the SPC reports the "REQ Asserted" interrupt when detecting the REQ signal asserted by a target. (For Initiator operation)

When "1": SPC does not report the "REQ Asserted" interrupt. However, SPC reports it when detecting the REQ signal in the data-phase, regardless of this bit setting.

When "0": SPC reports the "REQ Asserted" interrupt.

Bit 2: Command Complete Report Mode for SET/RESET commands

This bit specifies whether or not SPC reports the "Command Complete" interrupt for the SET/RESET commands.
This is valid in the user program operation.

When "1": SPC does not report the "Command Complete".

When "0": SPC reports the "Command Complete".

The applicable SET/RESET commands for this mode are as follows:

1) Initiator: SET ATN (0Ah), RESET ATN (0Bh), SET ACK (0Ch), RESET ACK (0Dh)

2) Target: SET REQ (31h), RESET REQ (32h)

3) Common: SET RST (48h), RESET RST (49h)

Bit 1: Level-2 Interrupt Report Mode

This bit specifies whether or not the SPC reports the Level-2 interrupts occurred in the user program operation.

When "1": SPC does not report the Level-2 interrupts and does not retain them in the Interrupt Status Register. The result of command execution is retained in the accumulator and within the SPC. The retained values are as follows:

1) If "Command Complete": retains "00h".

2) If "Initial Phase Error" or "ATN Condition Detected": retains "01h".

The result of the execution can be identified by the conditional branch instruction following the execution. See Section 5.4.2 and 5.5.2 for this mode, which shows the examples of user program flow.

When "0": SPC reports the Level-2 interrupts and sequence step codes. In this case, reading out and operating the interrupt and step codes are required every execution of discrete command using MOVE instruction. See Section 5.4.1 and 5.5.1 for this mode, which shows the examples of user program flow.

Bit 0: Auto ACK RESET Mode

This bit specifies how to negate the final ACK signal for the transfer command. (For Initiator operation)

When "1": SPC automatically negates the final ACK signal during the transfer command. (Auto ACK reset)

When "0": SPC does not negate the final ACK signal automatically, but negates it with "RESET ACK" command. (Manual ACK reset)

1) Commands which complete with automatically negating the final ACK regardless of this bit setting:

- SEND 1-MSG with ATN (19h), - SEND or RECEIVE DATA from MPU or DMA / SEND or RECEIVE DATA to MPU or DMA with Padding (14h, 15h, 16h, 17h)

2) Commands/Operations which complete with negating the final ACK by "RESET ACK" Command (Manual ACK Reset) regardless of this bit setting:

- RECEIVE N-BYTE-MSG (07h), - RECEIVE MSG (1Ah), - RESET ATN (0Bh), - When "Initial Phase Error & MSG Received" interrupt is generated. - When Auto-Reselection response is operating.

3) Commands/Operations which depend on this bit setting:

- Transfer Commands except 1) and 2) above.

- SET ATN (0Ah)

- When "Initial Phase Error & Status Received" interrupt is generated.

Please note that the command step number in the Auto ACK Reset Mode will be (08h + Step code with Manual ACK reset mode). However, the following commands and interrupts are the exceptions for this command step number:

- SEND or RECEIVE DATA from MPU or DMA / SEND or RECEIVE DATA to MPU or DMA with Padding (14h, 15h, 16h, 17h)

- RECEIVE N-MSG (07h), RECEIVE MSG (1Ah), RESET ATN (0Bh)

- When "Initial Phase Error & MSG Received" is generated.

- When "Initial Phase Error & Status Received" is generated.

- When Auto-Reselection response is operating.

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3.3.15 SPC Timeout Setting Register (WRITE/READ)

This register specifies the timeout value for SPC BUSY state.

■ SPC Timeout Setting Register

The configuration of this register is shown below.

	7	6	5	4	3	2	1	0
"1DH'	TO 7	TO 6	TO 5	TO 4	TO 3	TO 2	TO 1	TO 0

Set the SPC timeout value at this register. When SPC is in Busy state longer than the time specified in this register, SPC makes TMOUT pin "Active" and sets "1" to the SPC Timeout bit (bit 4 of SPC Status Register) to report "SPC timeout".

SPC does not detect the timeout if "00h" is set at this register.

The SPC timeout is calculated by the following equation:

$t_{CLF} \times C_{NV} \times [(TO7 \times 2^{30}) + (TO6 \times 2^{28}) + (TO5 \times 2^{26}) + (TO4 \times 2^{24}) + (TO3 \times 2^{22}) + (TO2 \times 2^{20}) + (TO1 \times 2^{18}) + (TO0 \times 2^{16})]$

t_{CLF}: Input clock Frequency (1 cycle)

C_{NV}: Value indicated in Bit 4 and Bit 3 of Clock Conversion Register.

TO7 - TO0: The above mentioned register values

3.3.16 Revision Indication Register (WRITE/READ)

This register indicates the SPC chip revision.

■ **Revision Indication Register (WRITE/READ)**

The configuration of this register is shown below.

	7	6	5	4	3	2	1	0
"1FH'	RV 7	RV 6	RV 5	RV 4	RV 3	RV 2	RV 1	RV 0

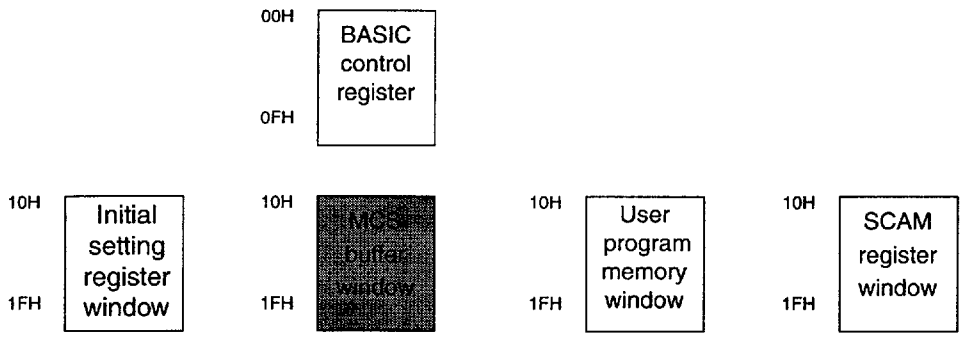
In order to see the device revision code, please take the following ways.

1. Write "00h" to the address "1Fh" at the initial setting.
2. Issue the "Setup REG" command.
3. Read out the value for the address "1Fh" after completing the "Setup REG" command.

The value except "00h" read out is the chip revision.

3.4 MCS BUFFER WINDOW

A 32-byte memory for sending and receiving messages, commands, and statuses with two 16-byte windows.



Note: SCAM register window is available in MB86604L only.

■ MCS Buffer Window

The MCS buffer window buffer list is shown in Table 3-15.

Table 3.4 MCS Buffer Window Buffer List

No	Address					Write	Read
	A4	A3	A2	A1	A0		
10	1	0	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
11	1	0	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
12	1	0	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
13	1	0	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
14	1	0	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
15	1	0	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
16	1	0	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
17	1	0	1	1	1	SEND MCS buffer	RECEIVE MCS buffer
18	1	1	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
19	1	1	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
1A	1	1	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
1B	1	1	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
1C	1	1	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
1D	1	1	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
1E	1	1	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
1F	1	1	1	1	1	SEND MCS buffer	RECEIVE MCS buffer

■ **SEND MCS Buffer (WRITE)**

This buffer is for writing messages, commands, and statuses to be sent (32 bytes).

Start writing the messages, commands, and statuses to be sent form address 0.

The SPC starts sending data from address 0.

When a command that requires the SEND MCS buffer to be accessed is sent, access to the SEND MCS buffer is not allowed until that command is completed.

■ **RECEIVE MCS Buffer (READ)**

This buffer is for reading messages, commands, and statuses received by the SPC (32 bytes).

Start reading the received messages, commands, and statuses from address 0.

The SPC starts saving the received data from address 0.

When a command that requires the RECEIVE MCS buffer to be accessed is sent, access to the RECEIVE MCS buffer is not allowed until that command is completed.

Also, when data is received, be sure to read the RECEIVE MCS buffer (the number of read bytes is displayed in the modified byte register).

Until all the data is read out, the next message, command, or status cannot be received.

Note: Access the RECEIVE MCS Buffer in the following cases.

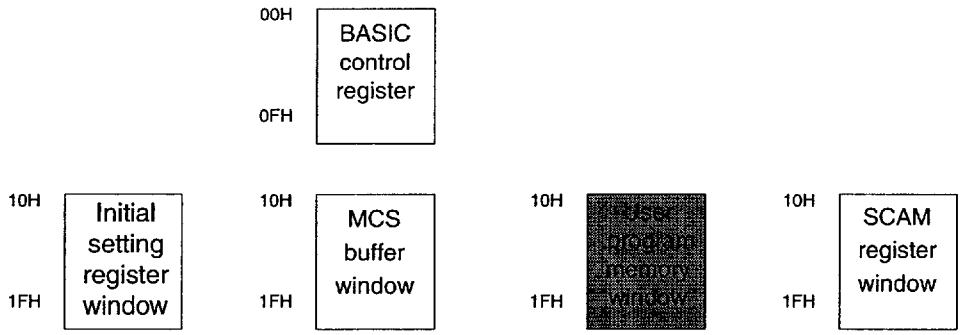
1) Initiator operation:
   Access until a RESET ACK command is issued after completion of the command which receives the data to the RECEIVE MCS Buffer or after completion of the automatic reselection response. When Auto ACK Reset mode is enabling, read out MCS buffer before issuing the next command.

2) Target operation:
   Access until the phase changes after completion of the command which receives the data to the RECEIVE MCS Buffer or after completion of the automatic selection response.

3.5 USER PROGRAM MEMORY WINDOW

A 256-byte memory for reading and writing user programs with 16 16-byte windows.

1.



Note: SCAM register window is available in the MB86604L only.

■ **User Program Memory Window**

A list of user program memory window memory areas is shown in Table 3-16.

Table 3.5 User Program Memory Window Memory Area List

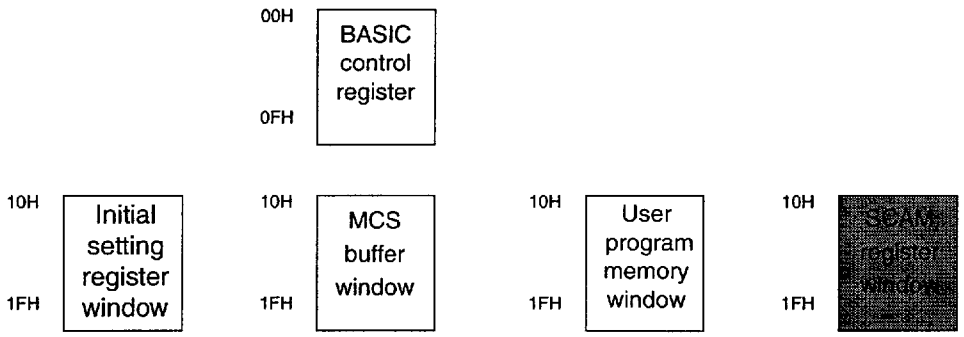
No	Address					Write	Read
	A4	A3	A2	A1	A0		
10	1	0	0	0	0	User program memory	User program memory
11	1	0	0	0	1	User program memory	User program memory
12	1	0	0	1	0	User program memory	User program memory
13	1	0	0	1	1	User program memory	User program memory
14	1	0	1	0	0	User program memory	User program memory
15	1	0	1	0	1	User program memory	User program memory
16	1	0	1	1	0	User program memory	User program memory
17	1	0	1	1	1	User program memory	User program memory
18	1	1	0	0	0	User program memory	User program memory
19	1	1	0	0	1	User program memory	User program memory
1A	1	1	0	1	0	User program memory	User program memory
1B	1	1	0	1	1	User program memory	User program memory
1C	1	1	1	0	0	User program memory	User program memory
1D	1	1	1	0	1	User program memory	User program memory
1E	1	1	1	1	0	User program memory	User program memory
1F	1	1	1	1	1	User program memory	User program memory

■ **User Program Memory (READ/WRITE)**

This memory is for reading and writing user program commands and data.

While the SPC is executing the user program, access to the user program memory and MCS buffers is denied.

3.6 SCAM REGISTER WINDOW



No	Address					Write	Read
	A4	A3	A2	A1	A0		
10	1	0	0	0	0	SCAM Data Bus Register	←
11	1	0	0	0	1	SCAM Control Register	←
12	1	0	0	1	0	(Reserved)	(Reserved)
13	1	0	0	1	1	(Reserved)	(Reserved)
14	1	0	1	0	0	(Reserved)	(Reserved)
15	1	0	1	0	1	(Reserved)	(Reserved)
16	1	0	1	1	0	(Reserved)	(Reserved)
17	1	0	1	1	1	(Reserved)	(Reserved)
18	1	1	0	0	0	(Reserved)	(Reserved)
19	1	1	0	0	1	(Reserved)	(Reserved)
1A	1	1	0	1	0	(Reserved)	(Reserved)
1B	1	1	0	1	1	(Reserved)	(Reserved)
1C	1	1	1	0	0	(Reserved)	(Reserved)
1D	1	1	1	0	1	(Reserved)	(Reserved)
1E	1	1	1	1	0	(Reserved)	(Reserved)
1F	1	1	1	1	1	(Reserved)	(Reserved)

SCAM register window is available in the MB86604L only.

3.6.1 SCAM REGISTER

The SCAM Register is initialized by the external reset or software reset command.

(1) SCAM Data Bus Register

Bank	Address		R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	MT	In									
01	10h		R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Initial Value			'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

This register is used to directly access the SCSI data bus from the system side for execution of the SCAM protocol. The signal level is reserved from those in the SCSI bus (writing 1 outputs low on the SCSI data bus).

(2) SCAM Control Register

Bank	Address		R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	MT	In									
01	11h		'0'	'0'	'0'	'0'	SEL	BSY	MSG	C/D	I/O
Initial Value			'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

This register is used to directly access the SCSI control signals from the system side for execution of the SCAM protocol. The signal level is reversed from those in the SCSI bus (writing 1 outputs low on the SCSI data bus).

Note:

1. When executing the SCAM protocol, set the SCSI driver to the open-drain mode. As for reading the SCSI bus, first write 0 to negate the SCSI driver outputs (Hi-Z) and then, read the SCSI bus.

2. When returning from SCAM protocol to the normal operation, make sure to initialize the SCAM data bus and SCAM control registers by writing 0 at all bits or executing the software reset command.