IC WORKS

W43C94A

SERIALLY PROGRAMMABLE GRAPHICS CLOCK GENERATOR

PRELIMINARY, APRIL 1994

FEATURES

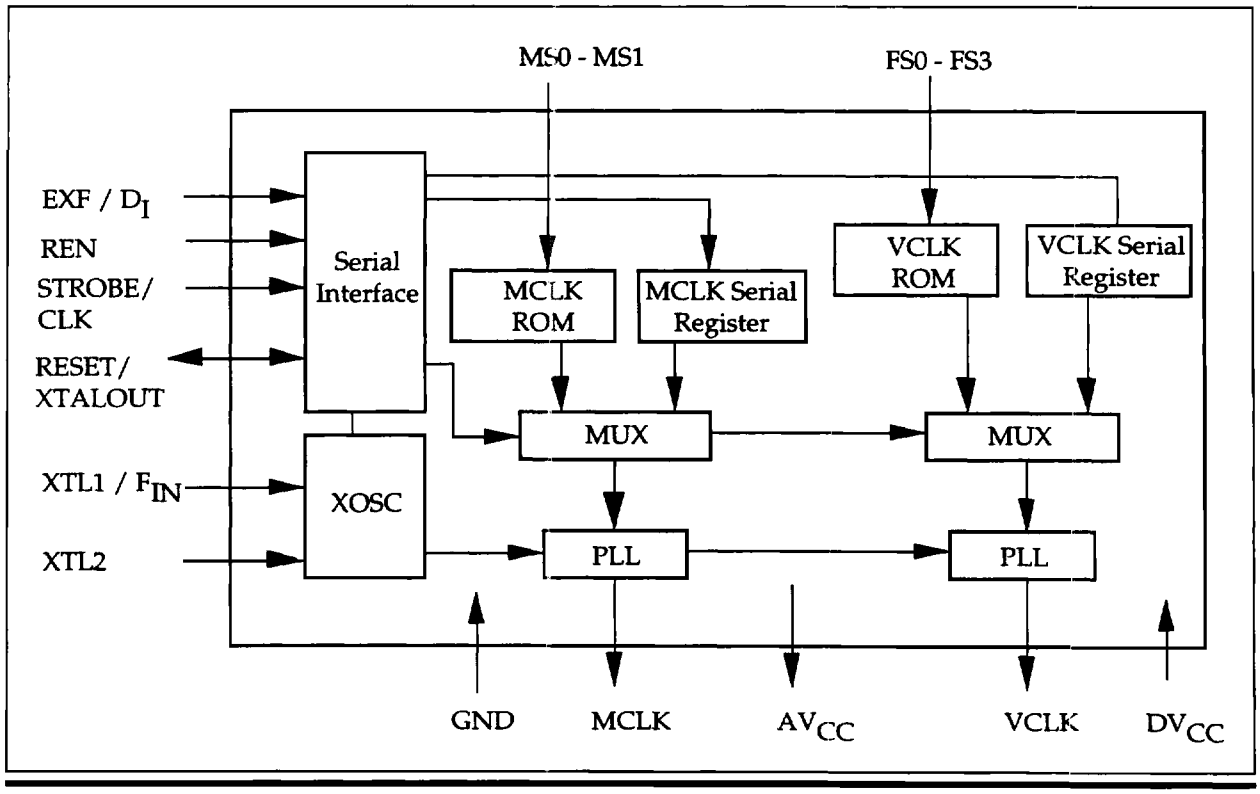
- **Independent clock outputs ranging from 8.75 - 135MHz for VCLK and 20 - 85MHz for MCLK**
- **Serially and individually programmable VCLK and MCLK**
- **16 preprogrammed VCLK frequencies in ROM**
- **4 or 8 preprogrammed MCLK frequencies in ROM**
- **Advanced phase-locked loop design with low phase jitter**
- **On-chip loop filter**
- **3.0V and 5.0V power supply**
- **Pin and functional compatible to W43C94, ICS2494 and AV9194**
- **TTL and CMOS input level compatible**
- **20-pin, SOIC/ DIP package**
- **Custom frequencies available**

GENERAL DESCRIPTION

The W43C94A is a dual phase-locked loop frequency synthesizer in a growing family of high performance, low skewed clock generators offered by IC WORKS, Inc. Fabricated with IC WORKS' advanced CMOS technology, the W43C94A is targeted for use in video/ graphics adapters and accelerators, as video dot clock generator. Due to the wide range of ROM-based preprogrammed frequencies, the W43C94A fulfills many system design requirements in jitter-free clock generation and distribution in video applications such as VGA, SVGA, XGA, graphics subsystems.

Available in industry standard 20-pin plastic DIP and 20-lead SOIC package, the W43C94A is fully pin and backward function compatible with W43C94, ICS2494 and AV9194.

FUNCTIONAL BLOCK DIAGRAM: W43C94A



The W43C94A has 16 preprogrammed clock frequencies for the VCLK and 4 (or 8) for the MCLK. These preprogrammed frequencies are resident in ROM, and are programmed at IC WORKS' factory. In addition to the many standard sets of frequency choices, customers can specify (via metal mask option) their own 16 frequencies within the range of 8.75MHz to 135MHz for the VCLK, and 4 (or 8) frequencies ranging from 20MHz to 85MHz for the MCLK, respectively. Note that W43C94A-13 offers 8 MCLK frequencies. Beyond these ROM-based frequencies, system designers can serially and individually program the VCLK and MCLK, respectively, on-line by using the 20-bit serial programming word. These clock outputs are designed to offer smooth and glitch-free transitions when switching from one clock frequency to another. Printed circuit board testing is simplified as an external clock generated by the ATE tester can be selected as an output permitting synchronous testing of the entire system.

FUNCTIONAL DESCRIPTION

The Functional Block Diagram, shows the reference clock source can be (1) a series-resonant crystal connected across the XTL1/F_{IN} and XTL2 input pins, or (2) an input reference clock connected to the XTL1 input pin. In the latter case, the XTL2 pin must be left open. In an IBM-PC or "compatible" environment, the series-resonant frequency typically is 14.318MHz.

During power up, the device is automatically placed in ROM mode where frequency for the VCLK and MCLK outputs are derived from the on-chip ROM. The W43C94A is capable of multiplexing an externally generated frequency source (EXF on pin 3) of VCLK via a mask option, in addition to its internally-generated clocks.

To provide the broadest possible range of frequencies typically required for video and graphics designs, the target frequencies for the VCLK and MCLK clocks can be selected via the FS0-FS3 and MS0-MS1 inputs, respectively. FS0-FS3 are address inputs that select the preprogrammed frequencies (1 of 16) in VCLK ROM for the VCLK output (pin 19). When STROBE is high , it allows new FS0-FS3 into the frequency select latch. When STROBE is low, it prevents address changes. MS0-MS1 are addresses that select 1 of 4 frequencies in the MCLK ROM. The MCLK clock output is pin 12. The MS0-MS1 bus is not strobed nor latched. If W43C94A-13 is used, MS2 (pin 3) is the most significant bit of MCLK ROM selection. Consult tables for standard frequency set selections with the corresponding part numbers.

In addition, the W43C94A has a XTALOUT pin (pin 18), which rebuffers the reference input clock frequency. The XTALOUT clock can thus be used as a bus clock or other needed clocking functions on motherboard designs.

SERIAL PROGRAMMING

On-line serial programmability of clock frequencies is the most versatile feature of the W43C94A. This programmability makes use of a serial 20-bit word that enables the user to select the VCLK and MCLK, serial mode or ROM frequency selection, and VCLK output drive capability. When in serial programming mode, the device allows the user to write (but can not read) into the MCLK and VCLK serial registers the parameters that will determine the output frequencies (F_O). Such F_O frequencies are determined by the formula described later.

The serial programming process begins when REN, a serial register enable signal, goes high. Pin 3 (EXF/D_I) is used as a data input D_I pin. D_I is clocked in on the rising edge of CLK (written into the serial register) by STROBE/CLK on pin 6, one clock per bit in a serial fashion. Of the 20-bit word, bit 19 (most significant bit) is written in first, and bit 0 last. Consult Figure 7 for detailed timing related to serial programming. An internal pointer controls the bit position when serial programming is in progress. After the entire 20-bit word is loaded into the serial register, the data is then transferred from the serial register to either the VCLK data register or the MCLK data register, depending on bit 19 (VM) of the serial word. This transfer takes place during the falling edge of REN. Bit 18 (RSS) of the 20-bit word selects an input (ROM or Serial Register) to the internal multiplexer.

The structure of the 20-bit word for VCLK and MCLK serial registers and description of all functional fields are presented in Table 1, page 4.

PROGRAMMABLE FREQUENCY

The serial programmable frequency F_O, on the VCLK and MCLK output pins is computed according to the following equation:

$$F_O = F_I^* \ (M * 4) / (N * O)$$

Where F_I is the input frequency (at XTL1/F_{IN}), "M" is the value of the FDIV counter + 1, "N" is the value of the IDIV counter + 1, and "O" is the OUTDIV value. For example, if "M" is desired to be 99 and "N" 34, the FDIV bits 10 - 17 for the VCLK and bits 9 - 16 for the MCLK are set to (01100010) binary, and IDIV bits 0 - 6 for both VCLK and MCLK are set to (0100001) binary, respectively; the "O" value is usually selected first in a serial frequency programming application. The internal VCO frequency range is specified from 8.75 - 135 MHz for the VCLK and 20 -85MHz for the MCLK. The OUTDIV counter has the following selections:

OUTDIV RESULT	DESIRED VCLK (MHz)	DESIRED MCLK (MHz)
+1	70 - 135	40 - 85
+2	35 - 70	20 - 40
+4	17.5 - 35	-
+8	8.75 - 17.5	-

The "N" value is selected next. With "N" close to 30, it yields good results with low noise. "M" is selected last to give the desired frequencies on the VCLK and MCLK.

PIN CONFIGURATION: W43C94A

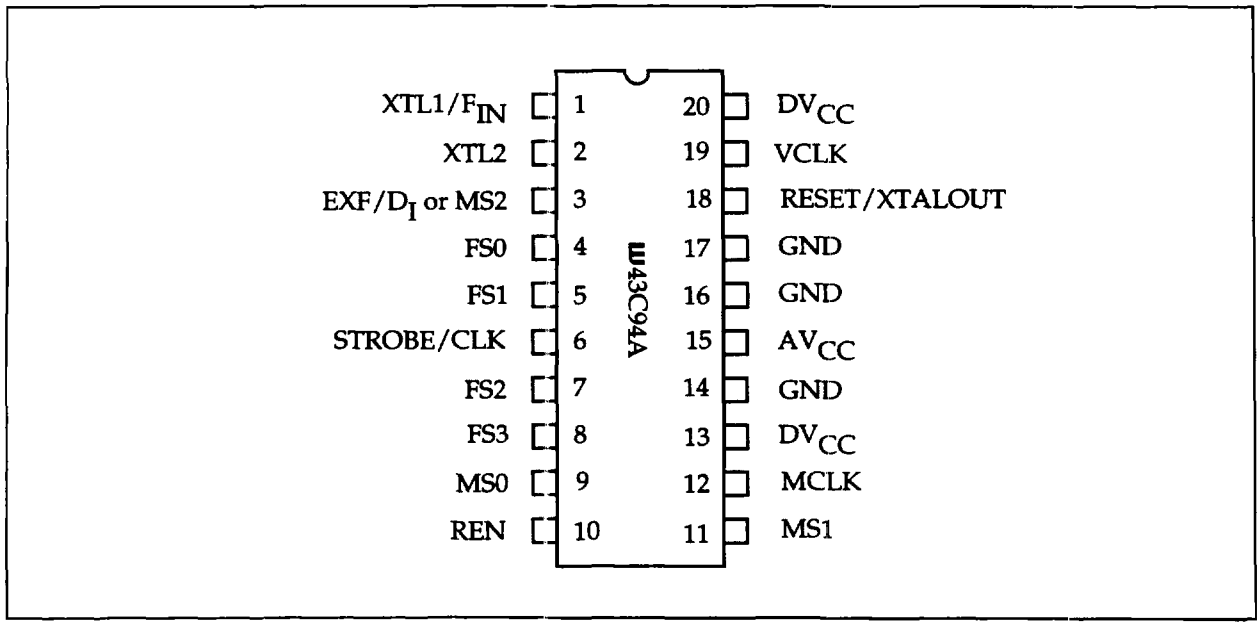


Table 1: SERIAL WORD STRUCTURE AND FIELD DEFINITION

MSB LSB

VCLK REG	D19	D18	D17——— D10	D9 —— D8	D7	D6——— D0
	VM	RSS	FDIV (M)	OUTDIV	OUT DRV	IDIV (N)

MCLK REG	D19	D18	D17	D16 —— D9	D8	D7	D6 — D0
	VM	RSS	MS0	FDIV (M)	OUT DIV	XTAL OUT	IDIV (N)

FIELD DEFINITION FOR TABLE 1:

IDIV (bit 0-6 for both VCLK and MCLK): Input divider. "N" decimal value = Counter binary value + 1.

XTALOUT (bit 7 for MCLK only): Pin 18 functions.
When XTALOUT = 0, pin 18 rebuffers the input clock.
When XTALOUT = 1, pin 18 provides a RESET function to the chip.

OUT DRV (bit 7 for VCLK only): Output driver current sinking capability selection.
When OUT DRV = 0, output current specified is 1X, or 4 mA.
When OUT DRV = 1, output current specified is 2X, or 8 mA.

OUT DIV (bit 8 for MCLK; bit 8-9 for VCLK):
Output divider
For the MCLK:
When value is binary 0, divide by 2
When value is binary 1, divide by 1
For the VCLK:
When value is binary 0, divide by 8
When value is binary 1, divide by 4
When value is binary 2, divide by 2
When value is binary 3, divide by 1

FDIV (M) (bit 9-16 for MCLK; bit 10-17 for VCLK): feedback divider. "M" decimal value = Counter binary value + 1.

MS0 (bit 17): MCLK ROM address select. L = Serial Load, A = ROM Address

RSS (bit 18): Multiplexer input select control.
When RSS = 0, Output from data register is selected to pass through the multiplexer.
When RSS = 1, Output from ROM is selected to pass through the multiplexer.

VM (bit 19): VCLK or MCLK data register selection.
When VM = 0, contents from serial register is transferred to VCLK data register.
When VM = 1, contents from serial register is transferred to MCLK data register.

PIN DESCRIPTION

Pin Name	I/O	Pin #	Description
XTAL1/F_{IN}	I	1	Input reference oscillator for all phase-locked loops (typically 14.318MHz); or an optional reference clock input of any frequency.
XTAL2	I	2	Oscillator output to a reference series-resonant crystal. For higher accuracy, a parallel-resonant crystal is recommended. This pin is not connected if external reference oscillator or external clock source is used.
EXF/D_I or MS2	I	3	An input to digital multiplexer. When this pin is enabled, external frequency signals driving the input will appear at VCLK (19) instead of PLL output. Internally, PLL will remain in lock at the frequency selected by the ROM code. D_I is data input when serial programming mode is activated (REN high). This pin is used as MS2 for W43C94A-13, and does not have a pull-up resistor.
FS0	I	4	VCLK ROM frequency select bit 0, least significant bit of FS3-FS0. Has pull-up resistor. MS2 IS MCLK ROM frequency select 2.
FS1	I	5	VCLK ROM frequency select bit 1. Has pull-up resistor.
STROBE/CLK	I	6	Strobe function. When REN is high, it clocks data (D_I) in.
FS2	I	7	VCLK ROM frequency select bit 2. Has pull-up resistor.
FS3	I	8	VCLK ROM frequency select bit 3, most significant bit of FS3-FS0. Has pull-up resistor.
MS0	I	9	MCLK ROM frequency select 0, least significant bit of MS1-MS0. Has pull-up resistor.
REN	I	10	Enable control for Serial Register. Active high. Data is latched on low-going edge of REN, and transferred to data register.
MS1	I	11	MCLK ROM frequency select 1, most significant bit of MS1-MS0. Has pull-up resistor.
MCLK	O	12	MCLK output (memory clock).
DV_{CC}	P	13, 20	Power Supply for digital circuitry, +5.0V.
GND	P	14, 16, 17	Ground.
AV_{CC}	P	15	Power Supply for analog circuitry, +5.0V.
RESET/XTALOUT	I/O	18	Bidirectional pin. Reset is an active high input. XTALOUT is an output which rebuffers the reference input clock.
VCLK	O	19	VCLK output (video clock).

PCB LAYOUT CONSIDERATIONS

If using a metal can crystal, place as close as possible to W43C94A device. Using a monolithic clock generator puts some constraints on the PCB layout to accomodate a single source of all clocks, particularly at frequencies higher than 50MHz.

It is recommended that a full power (V_{CC}) and ground plane layout should be used under and around the clock generator. The analog power pin (AV_{CC}) should be bypassed to ground with a 0.047 µF multi-layer ceramic capacitor, a 2.2 µF, 10V tantalum capacitor and a Zener diode wired in parallel as shown in Figure 1. Low inductance trace should be used. Both capacitors should be placed within 0.15" of the power pin. A 22Ω series resistor placed between the power supply and the DV_{CC} pin can help to filter any noise found in the supply lines.

An alternate layout configuration is shown in Figure 2. The two by-pass capacitors are connected across the DV_{CC} pin 20 and all ground pins (pins 14, 16, and 17). A 15Ω resistor is connected between the power supply V_{CC}) and all DV_{CC} and AV_{CC} pins (pins 13, 15 and 20) to filter noise generated by the supply lines.

As a sound layout practice to eliminate crosstalk, designer should avoid routing output traces of the clock generatorchip in close parallel proximity. Long traces and large number of fanouts would generally add capacitance to the output drivers. The effect of this capacitance will be to slow the rise and fall times of the output parameters. If and when large fanouts must be provided, the output from the clock chip should be buffered. As a rule of thumb, place the W43C94A as close to the destination device which requires the highest frequency and avoid running any signal lines through the synthesizer section of the printed circuit board.

CIRCUIT CONFIGURATION: W43C94A

Figure 1: Recommended

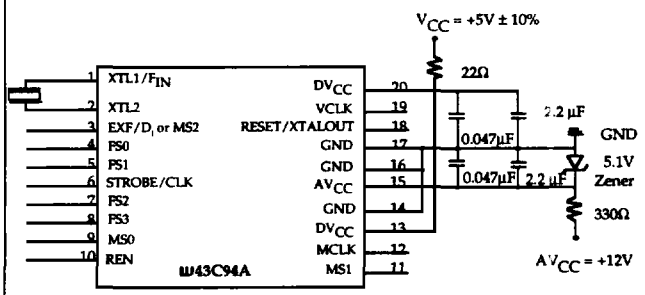


Figure 2: Alternate Recommended

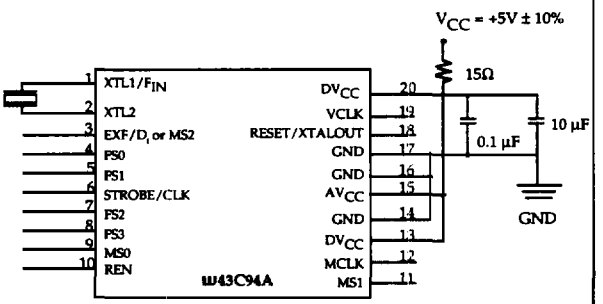
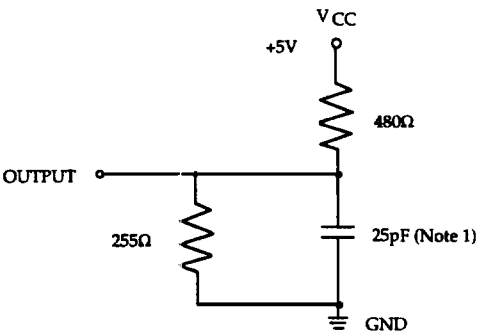


Figure 3: Output Loading Circuit Diagram



Note 1: Including scope and test jig capacitance.

STANDARD FREQUENCY CROSS REFERENCE TABLE: W43C94A

Part # IC WORKS	W43C94A-00	W43C94A-01	W43C94A-02	W43C94A-03	W43C94A-04	W43C94A-05
Cross Ref	ICS2494-237/A-304 AV9194-37 CH9294-E	ICW2494-256 AV9194-56 N/A	ICS2494-275 AV9194-07 N/A	ICS2494-N/A N/A N/A	ICS2494-253 AV9194-53 N/A	ICS2494-236/A-310 AV9194-36 N/A
Compatible VGA Chip Set	Tseng Labs ET4000 ET4000-W32	S3 86C911 S3 86C924	S3 86C801S3 S3 86C805 S3 86C928		NCR77C22E	Cirrus Logic GD6410 GD6412
FS3 - FS0	VCLK FREQUENCIES (MHz)					
0	50.35	25.175	25.175	25.175	25.175	14.318
1	56.644	28.233	28.322	28.322	28.322	60.028
2	65	40	40	40	40	EXF
3	72	EXF	EXF	72	65	36
4	80	50	50	50	44.9	25.127
5	89.8	77	77	77.5	50	28.322
6	63	36	36	36	130	24
7	75	44.889	44.9	44.9	75	40
8	25.175	130	130	63	25.175	44.9
9	28.322	120	120	100	28.322	50.35
10	31.5	31.5	80	80	EXF	16.257
11	36	31.5	31.5	31.5	EXF	32.514
12	40	110	110	110	60	56.644
13	44.9	65	65	65	80	20
14	50	75	75	75	EXF	41.59
15	65	72	94.5	94.5	EXF	80
MS1 - MS0	MCLK FREQUENCIES (MHz)					
0	40	55	45	48	50	32.9
1	41.612	75	38	52.5	60	35.6
2	44.744	70	52	60	65	43.9
3	50	80	50	50	75	49.1
4	-	-	-	-		
5	-	-	-	-		
6	-	-	-	-		
7	-	-	-	-		

STANDARD FREQUENCY CROSS REFERENCE TABLE : W43C94A (con't)

Part # IC WORKS	W43C94A-06	W43C94A-07	W43C94A-12	W43C94A-13	W43C94A-14	W43C94A-15
Cross Ref	ICS2494-N/A N/A N/A	ICS2494-263 N/A N/A	ICS2494-324 N/A N/A	N/A N/A CH9294-G	ICS2494-244/A-317 AV9194-44 N/A	N/A N/A N/A
Compatible VGA Chip Set		NCR77C22E	Tseng Labs ET4000 ET4000-W32	S386C911 S386C924 S386C928 S386C801 S386C805	CPU Motherboard Clocks	
FS3 - FS0	VCLK FREQUENCIES (MHz)					
0	38.88	25.175	50.35	25.175	20	25.175
1	46.2	28.322	56.644	28.322	24	28.322
2	48.182	36	65	40	32	31.5
3	59.318	65	72	72	40	36
4	40.993	44.9	80	50	50	40
5	35	50	89.8	77	66.667	44.9
6	30	80	63	36	80	50
7	40	75	75	44.9	100	65
8	55	25.175	83.078	130	54	75
9	67.899	28.322	93.463	120	70	77.5
10	51.84	EXF	100	80	90	80
11	64	EXF	104	31.5	110	90
12	70	60	108	110	25	100
13	75	80	120	65	33.333	110
14	80	EXF	130	75	40	126
15	85	EXF	134.7	94.5	50	135
MS1 - MS0	MCLK FREQUENCIES (MHz)					
0	18.8096	50	50	55	16	60
1	28.3046	40	55	65	24	50
2	70	65	60	70	50	55
3	80	75	65	80	66.667	50
4	-	-	-	45	-	52.5
5	-	-	-	40	-	57.5
6	-	-	-	60	-	62.5
7	-	-	-	50	-	65

STANDARD FREQUENCY CROSS REFERENCE TABLE : W43C94A (con't)

Part # IC WORKS	W43C94A-16	W43C94A-17	W43C94A-19	W43C94A-20	w43C94A-22	W43C94A-23
Cross Ref	ICS2494A- AV9194-60 N/A	N/A 280 N/A CH9294-G	ICS2494 N/A N/A	ICS2494- 253 N/A N/A	ICS2494- 261 N/A N/A	N/A 259 N/A N/A
Compatible VGA Chip Set	Weitek 5X86	S3 86C911 S3 86C924 S3 86C928 S3 86C801 S3 86C805	NCR77C22E		68800LX (MACH 32)	
FS3 - FS0	VCLK FREQUENCIES (MHz)					
0	25.175	50.35	14.318	50.350	100	9
1	28.322	56.644	16.257	56.644	126	22.8
2	40	33.25	EXF	65	92.40	18
3	EXF	52	32.514	72	36	45.6
4	50	80	25.175	80	50.35	26.784
5	77	63	28.322	89	56.64	26.6648
6	36	EXF	24	63	EXF	35.5574
7	44.889	75	40	75	44.9	35.5574
8	130	25.175	25.175	50.350	135	26.784
9	120	28.322	28.322	56.644	32	33.33
10	80	31.5	36	75	110	65
11	31.5	36	65	44.9	80	36
12	110	40	44.9	59	39.91	24
13	65	44.9	50	64	44.9	44.9
14	75	50	130	80	75	45.6
15	94.5	65	75	95	65	60
MS1 - MS0	MCLK FREQUENCIES (MHz)					
0	55	40	50	35.5	40	50
1	60	33.333	60	41.612	45	40
2	70	45	65	44.744	33	10
3	65	50	75	50	50	28.36
4	-	-	-			
5	-	-	-			
6	-	-	-			
7	-	-	-			

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symb	Rating	Parameter	Symb	Rating
V_{CC} Referenced to GND		7V	V on I/O ref to GND		GND-0.5V to V_{CC}+0.5V
Storage Temperature	T_{STG}	-40°-150°C	Power dissipation	P_D	0.5 Watts
Operating Temperature	T_A	0°-70°C			

Note 1: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure the absolute maximum conditions for extended periods may affect devices reliability.

CAPACITANCE (Frequency = 1MHz, T_A = 25 °C) (Note 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{IN}	Except pins 1, 2, 12, 18 & 19	-	-	7	pF
Load Capacitance	C_L	Pins 1 and 2	-	-	12	pF

Note 2: Guaranteed by design.

DC CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	V_{CC} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{CC} = 5V	2.0			V
Input Low Current	I_{IL}	V_{IN} = 0V	-	-	-5	μA
Input Low Current	I_{IL}	V_{IN} = 0V for pins 4, 5, 7, 8, 9 & 11	-	-	-100	μA
Input High Current	I_{IH}	V_{IN} = V_{CC}	-	-	5	μA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA	2.4	-	-	V
Supply Current	I_{CC}	V_{CC} = Max No load	-	25	40	mA
Output Frequency Change Over Supply and Temperature	F_D	With respect to typical frequency	-	0.002	0.01	%

AC CHARACTERISTICS FOR ROM MODE (V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Units
Programmable Video Frequency	F_{VPRO}	8.75	-	140	MHz
Programmable Memory Frequency	F_{MPRO}	20	-	95	MHz
Reference Oscillator Frequency	F_{REF}	8	14.31818	25	MHz
Crystal Frequency Propagation Delay	T_{XL}	-	-	10	ns
Output Duty cycle: T_{ON}/T_{CYC}	DC	40/60	48/52	60/40	%
Video Output Frequency Error	F_A	-	-	0.5	%
Output Frequency Deviation From Nominal	F_{DEV}	-	-	0.05	%
Output Rise Time, 0.8V to 2.0V	T_R	-	-	2	ns
Output Fall Time, 2.0V to 0.8V	T_F	-	-	2	ns
STROBE Setup Time	T_S	10	-	-	ns
STROBE Hold Time	T_H	10	-	-	ns
STROBE Pulse Width	T_{PW}	10	-	-	ns
Previous Frequency Valid Time	F_{VPF}	0	-	-	ns
New Frequency Settling Time	T_{SNF}	-	-	1	ms

AC CHARACTERISTICS FOR SERIAL MODE (V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Units
Programmable Video Frequency	F_{VPRO}	8.75	-	135	MHz
Programmable Memory Frequency	F_{MPRO}	20	-	85	MHz
Reference Oscillator Frequency	F_{REF}	8	14.31818	25	MHz
Output Duty cycle: T_{ON}/T_{CYC}	DC	40	-	60	%
Nominal Output Frequency Error	F_A	-	-	0.2	%
Output Frequency Deviation From Nominal	F_{DEV}	-	-	0.05	%
Output Rise Time	T_R	-	-	4	ns
Output Fall Time	T_F	-	-	4	ns
Serial Register Cycle Time	T_{SRC}	50	-	-	ns
Setup Time	T_S	5	-	-	ns
Hold Time	T_H	5	-	-	ns
Data Setup Time	T_{DS}	10	-	-	ns
Data Hold Time	T_{DH}	10	-	-	ns
Write Pulse Width Enable	T_{WE}	25	-	-	ns
RESET/XTALOUT/REN Pulse Width Disable	T_{WD}	15	-	-	ns
Serial Register Output Access Time	T_{RD}	-	-	15	ns
Serial Register Output Hold Time	T_{OH}	0	-	-	ns
Previous Frequency Valid Time	F_{VPF}	0	-	-	ns
New Frequency Settling Time	T_{SNF}	-	-	1	ms
RESET Pulse Width	T_{RST}	100	-	-	ns
Hold Time After Reset Before Write	T_{RH}	100	-	-	ns

Figure 4: Rise and Fall Time Timing Diagram

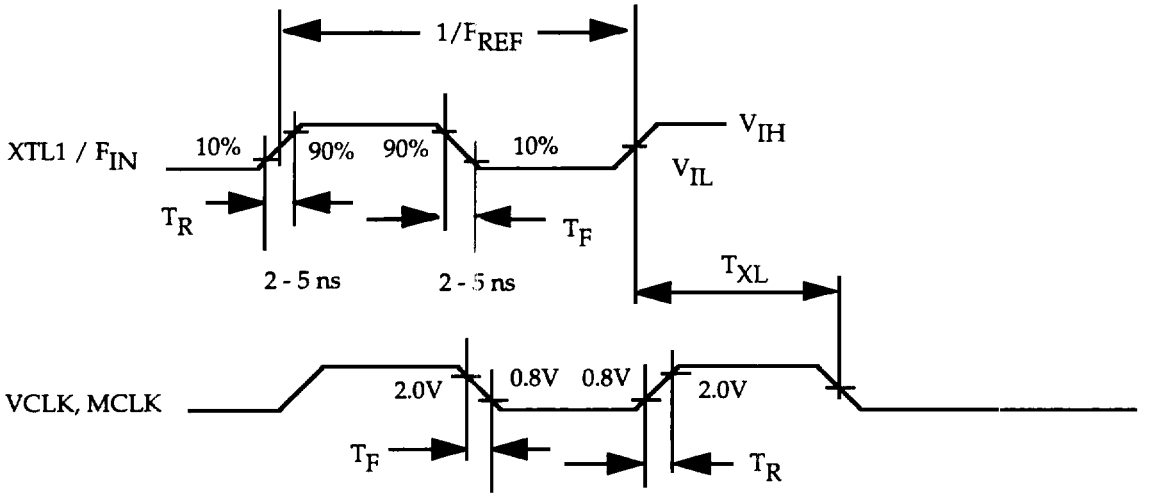


Figure 5: ROM MCLK Selection Timing Diagram

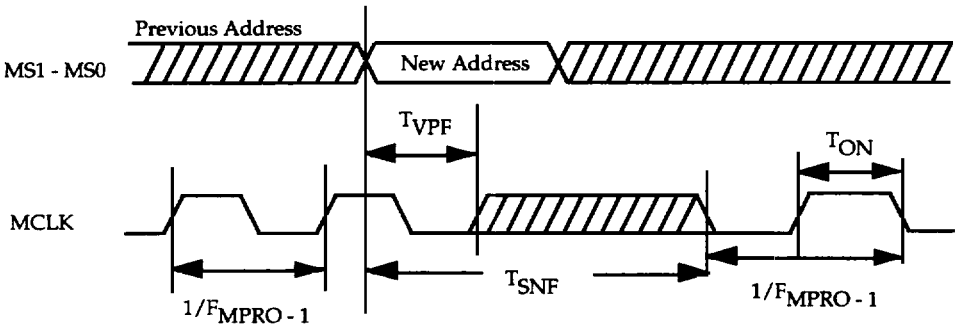


Figure 6: ROM VCLK Selection Timing Diagram

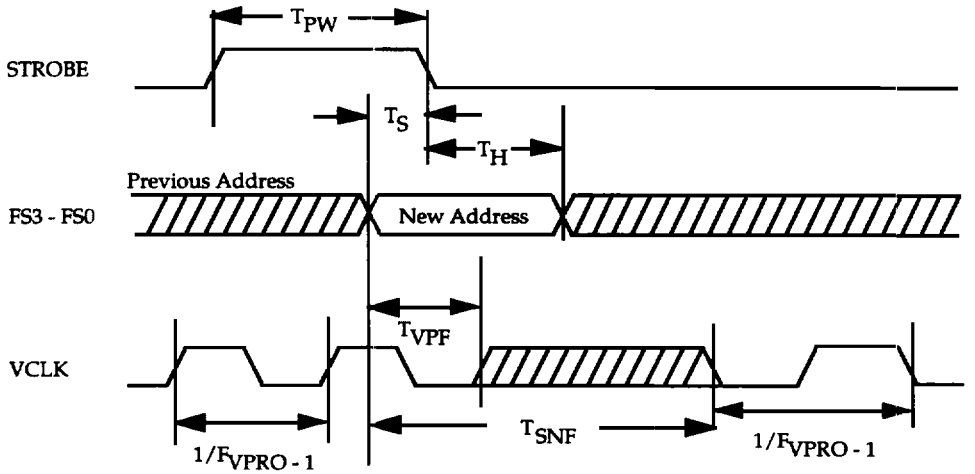


Figure 7: Serial Programming Timing Diagram

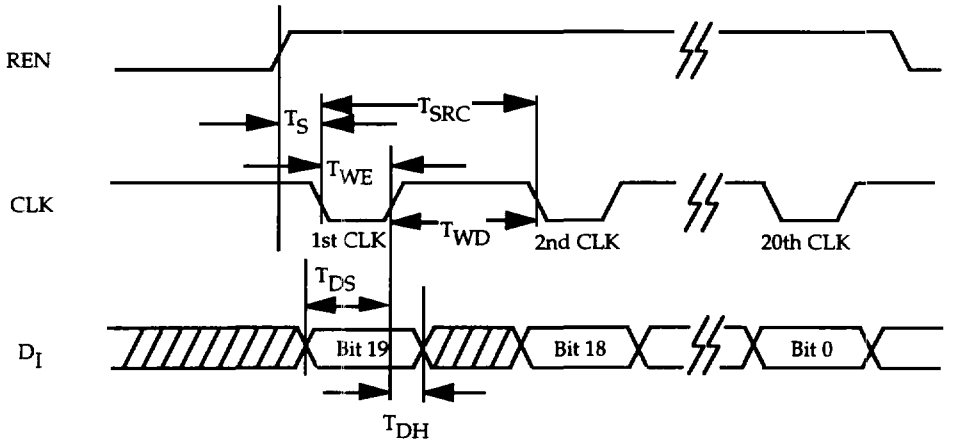


Figure 8: Serial Mode MCLK and VCLK Frequency Transition Timing Diagram

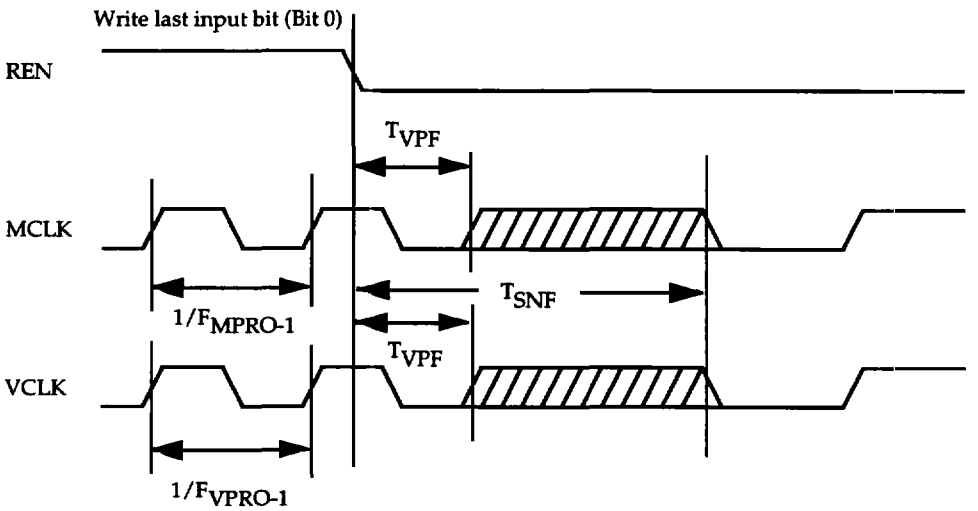
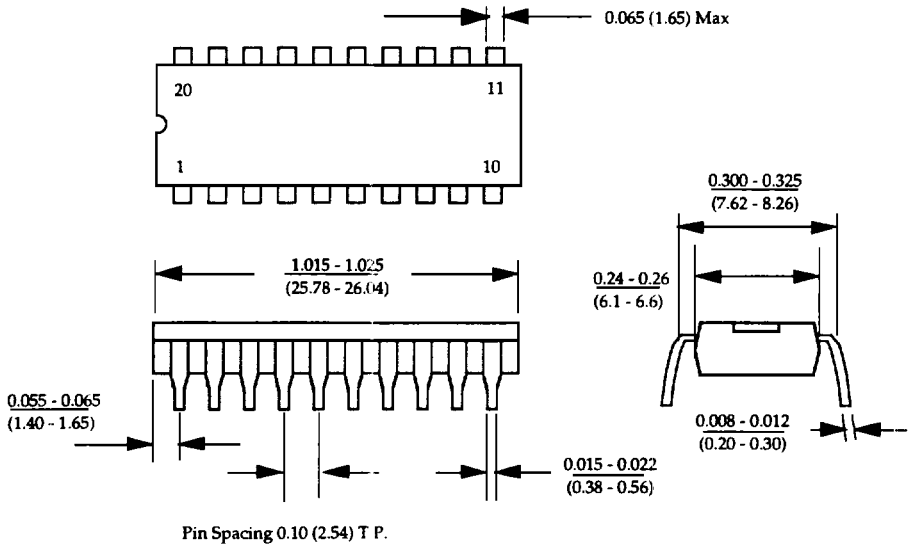
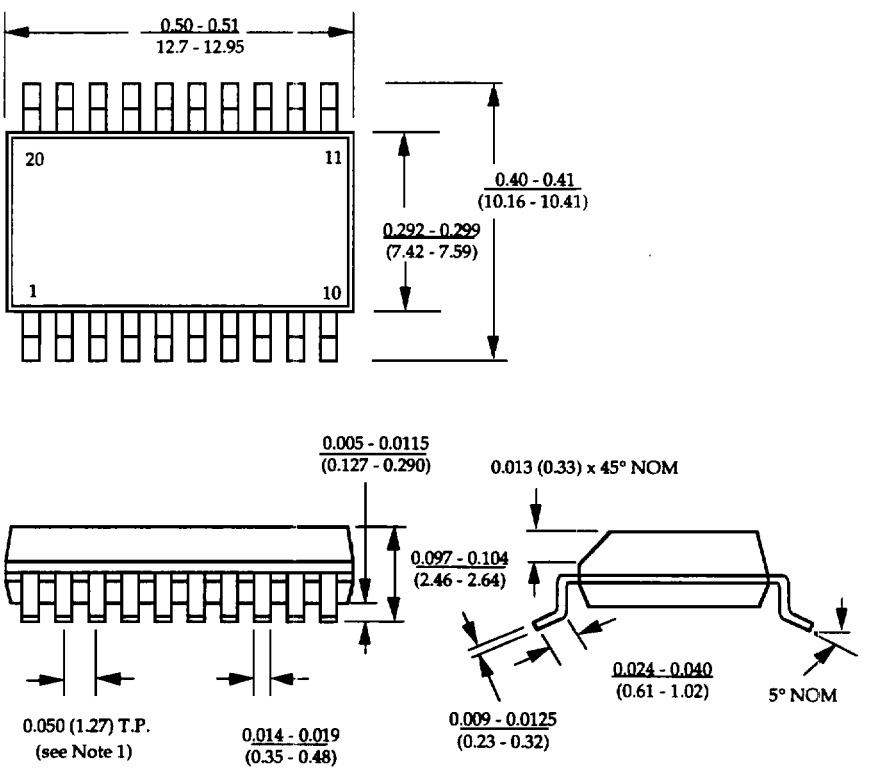


Figure 9: 20 pin Plastic Dual In-Line Package



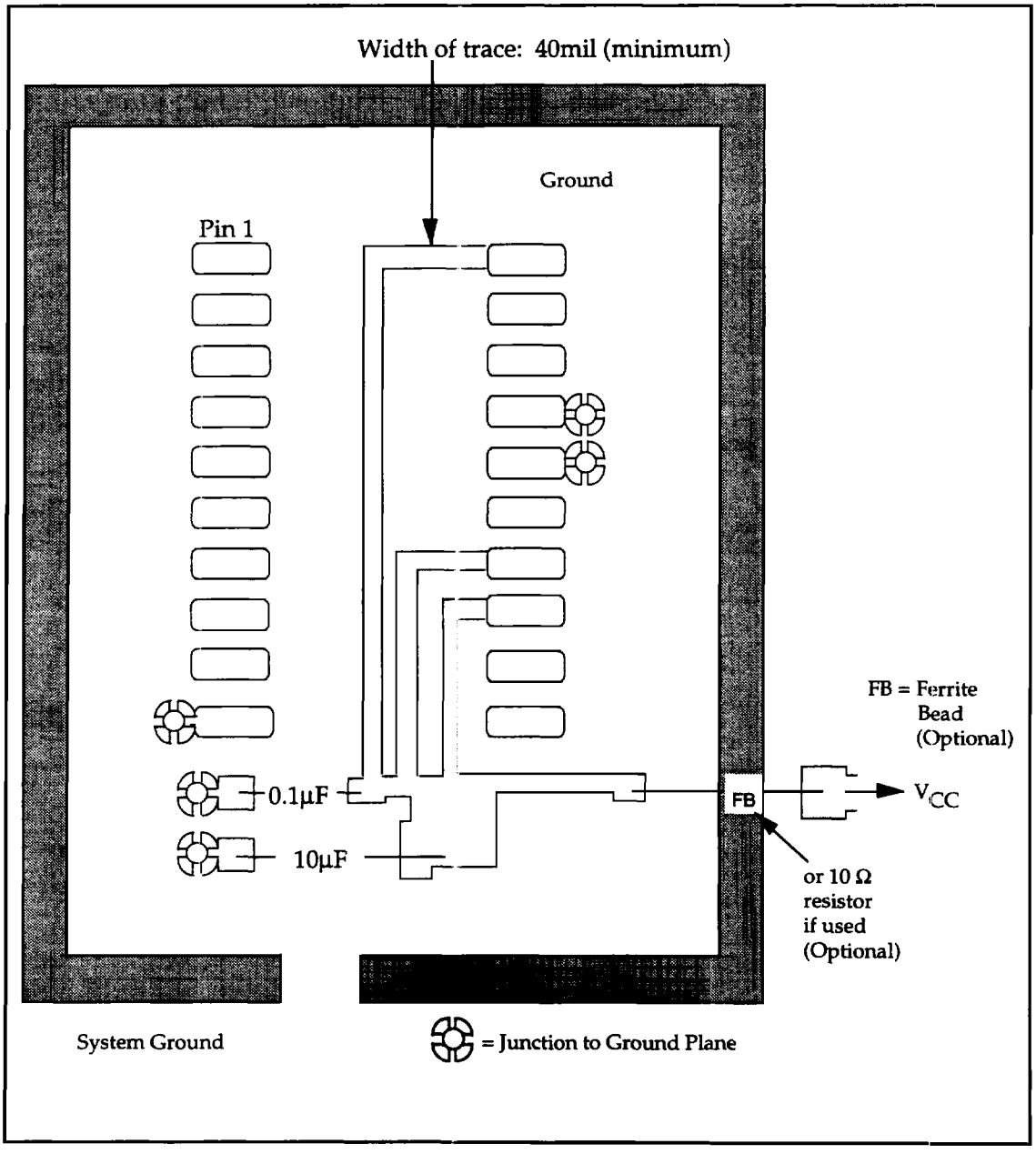
Note: All linear dimensions are in inches and parenthetically in millimeters, min - max.

Figure 10: 20 lead Plastic Small Outline Package



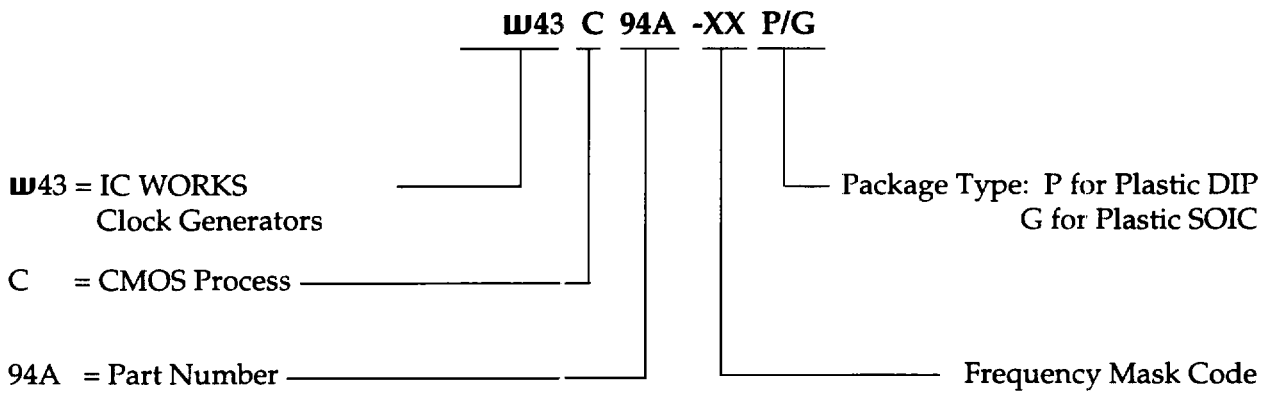
Note 1: Leads are within 0.010(0.25) radius of true position at maximum material condition.
Note 2: All linear dimensions are in inches and parenthetically in millimeters, min - max.

RECOMMENDED BOARD LAYOUT: w43C94A



The key feature is to isolate the w43C94A ground plane from system ground and make one connection between the two near the 0.1µF, 10µF decoupling capacitors.

ORDERING INFORMATION



VALID PART NUMBERS

W43C94A-00	W43C94A-01	W43C94A-02	W43C94A-03	W43C94A-04
W43C94A-05	W43C94A-06	W43C94A-07	W43C94A-12	W43C94A-13
W43C94A-14				

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Document No. 43C94A/00/0494